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Module testing for the CMS Forward Pixel Detector

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Abstract

The Forward Pixel Detector for the CMS Experiment consists of four disks. In total 672 modules are needed to assemble the disks. This translates into 18 million readout channels that need to be tested for their correct functionality making this task extremely challenging. This paper will present the procedure for testing these modules.

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1 Introduction

The Pixel Detector [1] for the CMS Experiment consists of two parts – the barrels and the disks. There are 3 layers of barrel and 2 disks on its either side. These 4 disks constitute the Forward Pixel Detector. The basic detector module is called a plaquette. It is a multilayer structure assembled in many steps. It consists of sensor, readout chips (ROCs), and a flex circuit called Very High Density Interconnect (VHDI) glued to a thin silicon plate. There are 7 different versions of Plaquettes, five of which are physically different sizes and have a single sensor bump bonded to a varying number of ROCs from 2 to 10). The plaquettes size is driven by the geometry of the overall detector. These are glued in groups of 3 or 4 on what is called a panel. Each readout chip in a plaquette has 26 programmable DAC registers that need to be fine tuned in order to perform at their optimum.. There are 4320 ROCs in total on all the plaquettes and each ROC has 4160 pixels [2]. Each pixel has to be tested [3] for its functionality, bump bonding, noise, gain, trim bits and pedestal. In order to make sure that only the best parts get mounted on the disk, a detailed qualification procedure has been developed along with the a custom built test stand and software that is not only robust but also fast. This makes it feasible to meet the goal of completing the testing phase in a timely manner. The assembly of the detector will go in parallel as the parts get tested.

2 Test System Layout

The operating temperature for the pixel detector is -20° C**.** We need to test the plaquettes and panels at -20° C since operating parameters and the noise characteristics can change significantly with temperature.

To keep up with schedule of detector assembly it is required to test at least 6 plaquettes and two panels per day. We have three dedicated test stands to achieve this goal. A test stand encloses a plaquette or a panel in a cold dry box. A system of Peltier cells cools down the plate on which plaquette/panel sits inside the cold box to -20° C. A low voltage power supply powers the ROCs and a Keithley High Voltage Power Supply reverse biases the sensor to -150 V. The plaquette/panel is connected to a TBM-ADC board. This board carries a Token Bit Manager (TBM) and an ADC chip. While TBM orchestrates [4] the readout of the ROCs, the ADC digitizes the signal output from the ROCs at a clock speed of 40 MHz. A PCI based test adaptor (PTA) card and a programmable mezzanine card (PMC) are installed inside the PCI slots. The PTA card carries a memory bank and communicates with the computer and the PMC card talks to the ROCs using the chip custom protocol. A Linux-based fully interactive software tool called "Renaissance" has been developed which is fully interactive and performs all the tests on some or all the ROCs of a plaquette in parallel and saves data to the construction database. Testing a plaquette takes about an hour. A panel is also tested similarly.

There is a burn-in setup also that can simultaneously thermal cycle 20 plaquettes or 10 panels from + 20° C to -20° C. This burn-in step will preceed the detailed testing of plaquettes and panels. The motivation is to find if plaquettes and panels survive the thermal stress cycles.

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3 Testing Procedure

Plaquettes are assembled at Purdue University and undergo a "quick" test to check their basic functionality. Each is of them is then shipped to Fermilab on a plaquette carrier board which directly plugs into the TBM-ADC card and can be tested. 30 plaquette are expected to arrive per week. Plaquette testing is divided into three stages at Fermilab. Upon their arrival, plaquettes are visually inspected and undergo a "plug-in" test to see if all ROCs respond. Then they go through a 3-day of burn-in which followed by a detailed testing and characterization. "Good" plaquettes are then assembled onto Panels. Panels are also tested in the same way as the plaquettes.

The testing of a plaquette should check its performance, DAC functionality and ability to function with right operational parameters and calibrate it. First, sensor current (I) versus voltage (V) values are measured to see if it has not been damaged during shipping. For each ROC to function correctly the value of the analog current

should be around 24 mA. The next test finds the value of the DAC parameter called Vana that gives this current to each ROC. This is followed by adjusting the ADC phase to an optimal value to latch the analog signal. Next, all the 26 DAC registers are tested to see if they can be set correctly. Once these basic tests are done successfully, we proceed for further functionality tests. These are:

Threshold/Timing: finds optimal values for internal charge injection of these two DAC registers - the comparator threshold (Vthr) and the delay of the internal calibrate signal with respect to the trigger signal (CalDel)

Bad Pixels: Finds pixels that disrupt that analog output.
Analog Levels: checks separation of analog address levels.
Decoding: Verifies if pixel address are decoded correctly.
Pulse Height: Finds optimal value of DAC register VHoldDelay corresponding to maximum pulse height.
Pixel Alive: Inject charge into each pixel with calibration capacitor to see if it responds.
Mask Bit: Test functionality of this bit to see if a pixel can be removed from the readout chain.
Bump bond test: To count the number of missing bump bonds that connect sensor pixel to a ROC pixel.
Gain: Find Pulse Height as a function of DAC called Vcal. This DAC controls the amplitude of internal calibrate signal.
Curves: Finds the threshold/noise per pixel.
VTrim: Finds the values of this DAC parameter that maximises the trimming capability. Trimming is a method by which we can control the threshold of an individual pixel using four trim bits. VTrim DAC controls the range of play of these trim bits. Once this range is optimized we do the trim bit test below.
Trim bit test: To check functionality of trim bits responsible for fine tuning threshold of each pixel.

During the burn-in process the plaquettes and panels will be readout and tested for some of the basic functionality tests. Pixel Alive and Bump bond tests will be done once. The temperature DAC of the ROC will also be calibrated.

4 Conclusions

The tools needed to qualify plaquettes and panels for the forward pixel detector are in place and have been well tested with pre-production parts. They will ensure an excellent detector.

References

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