EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH
Laboratory for Particle Physics

Departmental Report

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Thermal Behaviour and Fatigue Estimation of the Switching Regulator for the BTF Power Supply of DAΦNE Injector

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The BTF power supply is used to extract from the beam transfer line the particles pulses coming from the LINAC which normally fill the DAΦNE collider at Frascati INFN Lab. This new power converter has been designed to feed a bending magnet with 447 A at nominal conditions and with a total ramp up and down of 20 ms. This power converter can run either in pulsed mode or in a conventional DC current mode. In pulsed mode the flat top can be streched from 5 ms up to 960 ms allowing a multi-pulse extraction. The heart of the system is based on a static converter with an H bridge topology made of IGBTs with integrated free wheel diodes. On one hand this paper presents the analysis of the thermal behaviour, the fatigue estimation and the impact on the power converter life time. On the other hand the design of a forced air cooling system is presented with the final results.

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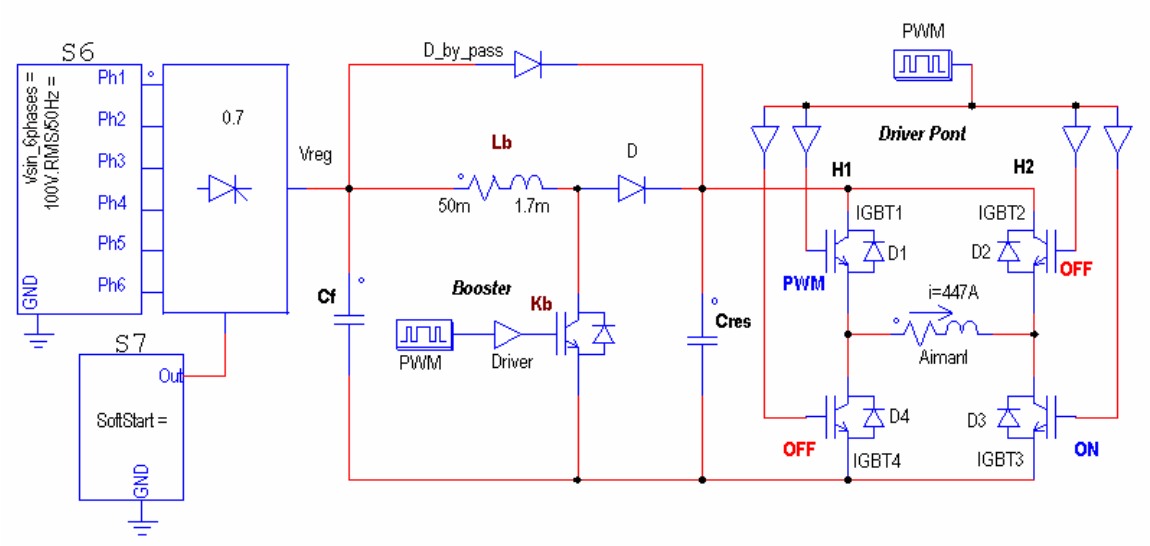
1. INTRODUCTION

Power electronics design using hard switching converters and inductive loads are typically made of IGBT power modules including free wheel diodes. As a result of power losses heat is produced in the power modules. However the maximum junction temperature of the semiconductor (T_{jmax}=150 °C) must not be exceeded. The losses are linked to many different parameters related to static and dynamic behaviour of the IGBT and free wheel diodes. As a consequence, it is important to carry out a thermal study in order to design a suitable cooling system and to evaluate thermal stresses which can dramatically reduce the lifetime of the system. The evaluation must determine the average junction temperature of the power semiconductors and, according to power cycling considerations, the transient thermal behaviour (ΔT_{jmax}) to estimate the thermal fatigue.

2. THE "H" BRIDGE TOPOLOGY

The basic system topology including the "H" bridge is described in figure 2.1. The two arms H_1 and H_2 of the bridge are made of 2 halfs bridge Dynex IGBT power modules DIM800DDM12-A000.
In order to reduce power losses it has been decided to design a control system wherein one IGBT is PWM controlled while the other one is kept closed to avoid the commutation losses. For simplification, the control system is not shown here. The figure 2.1 shows a current with a positive polarity. In such a case the $IGBT_1$ is PWM controlled while $IGBT_3$ is kept closed during the pulse duration that is foreseen to be between 20 ms and 960 ms [1]. When $IGBT_1$ if OFF, the free wheel diode D_4 is driving the load current.



2.1 – Basic system topology including "H" bridge [11] as simulated with PSIM 6.1©

3. BALANCE OF POWER LOSSES

Device power losses are the sum of switching, conduction and leakage losses. Usually forward blocking and driving losses are negligible.

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3.1 IGBT power losses

The total switching power losses in $IGBT_1$ can be calculated with : $P_{tot/T} = P_{fw/T} + P_{on,T} + P_{off,T}$ (1)

With:

$$P_{fwd/T} = \frac{1}{T}\int_0^{t_1} i_C(t).V_{CE}(t)dt$$
$$P_{on/T} = f_S.E_{on/T}(V_{out}, i_{LL}, T_{j/T})$$
$$P_{off/T} = f_S.E_{off/T}(V_{out}, i_{LH}, T_{j/T})$$

- $P_{fw/T}$: on-state power loss which depend on load current, T_J and duty cycles.
- $P_{on/T}$ and $P_{off/T}$: turn on and turn off power dissipations which depend on switching frequency, load current, DC link voltage, T_J.

The conduction losses in the $IGBT_3$ can be calculated with : $P_{cond,avg} = V_{CE(stat)}.I_{moy} + r_i.I_{rms}^2$

3.2 Free wheel diode power losses

The total power losses due to a free wheel diode can be calculated with (2):

$$P_{tot/D} = P_{fw/D} + P_{off,D} \quad (2)$$

With:

$$P_{fwd/D} = \frac{1}{T}\int_{t_1}^{T} V_F(t).i_F(t)dt$$
$$P_{off/D} = f_S.E_{off/D}(V_F, i_{LL}, T_{j/D})$$

- $P_{fw/D}$: on-state power loss which depend on load current, T_J and duty cycles.
- $P_{off,T}$: turn off power dissipations which depend on switching frequency, load current, DC link voltage, T_J.

3.3 An appropriate switching frequency

In an inductive hard switching design, the switching frequency is limited by the minimum and maximum pulse widths as well as conduction and switching losses. The pulse width limitation is due to transient thermal response which may not allow the junction temperature to cool down between large power pulses. To calculate an appropriate switching frequency, several parameters such as the turn on and turn off delays time, the current rise and fall time, the dead time, the free wheel diode reverse recovery time, the noise, etc. have to be considered. To get a frequency limit based on minimum pulse width, one has to define the minimum limit on pulse width such that the total switching time (sum of turn-on and turn-off switching times) must be no more than 5% of the switching period. This switching period limitation on total switching time provides a good margin for this approximation. So the maximum frequency based on minimum pulse width is given by the minimum value between (3) and (4):

$$f_{max1} = \frac{1}{T_S} = \frac{0.05}{t_{d(on)} + t_r + t_{d(off)} + t_f} \quad (3)$$

$$f_{max2} = \frac{1}{t_{diss}} = \frac{\frac{T_J - T_C}{R_{thjc}} - P_{cond}}{E_{on} + E_{off}} \quad (4)$$

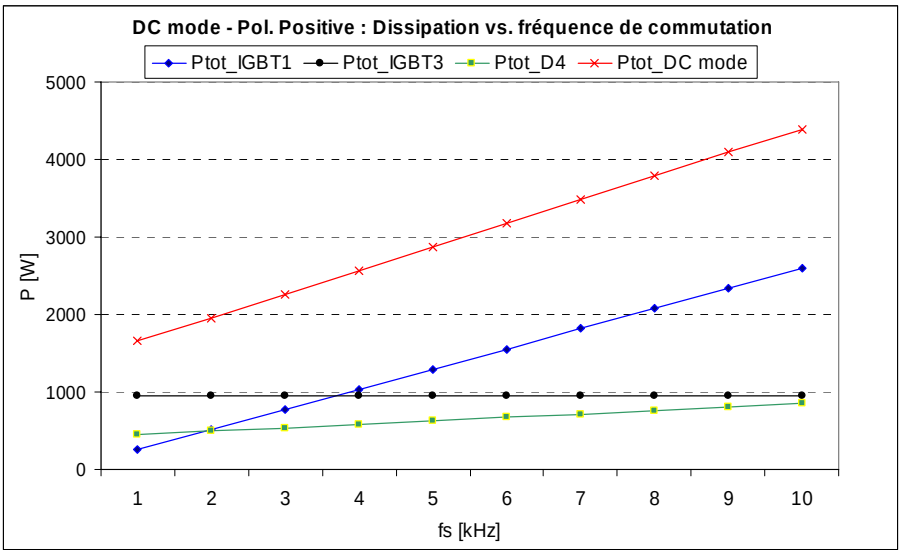
With:

- T_S: switching period defined by the turn on time and the turn off time
- E_{on} and E_{off}: energy required to turn on and turn off the IGBT
- T_J : junction temperature
- T_C : case temperature
- R_{thjc}: junction-case thermal resistance
- P_{cond} : conduction power loss
- t_{diss}: minimum time during which E_{on} and E_{off} can be dissipated to keep specified junction temperature.

The conduction losses is based on a 50% duty cycle assumption, it is independent of the switching frequency. However if P_{cond} increases the time required to dissipate the switching losses will increase. With the values of the Dynex IGBT data sheet, we can calculate:

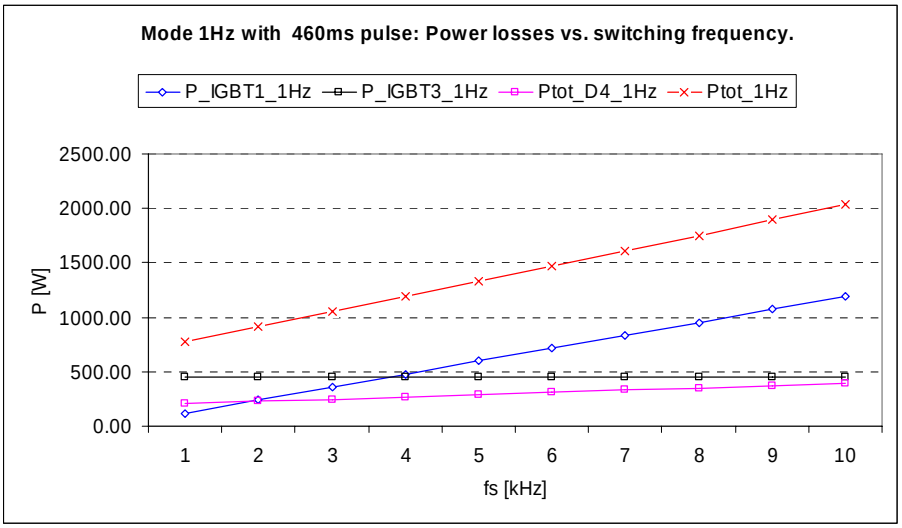
- f_{max1}=21.5 kHz
- f_{max2}=12.7 kHz

The maximum allowable switching frequency is 12.7 kHz. The final switching frequency can be determined by plotting the evolution of the total losses versus switching frequency. The result is plotted on figure 3.1 using the data sheet of the power module for the nominal load current (447A). Considering the DC mode, the figure 3.1 shows the evolution of the losses in the $IGBT_1$, the diode D_4 and the $IGBT_3$ versus the switching frequency. The switching losses increase quickly; over 3.5 kHz the total losses in $IGBT_1$ exceed the conduction losses in $IGBT_3$. The losses due to the free wheel diode increase gradually. On the other hand with an inductive load, the ripple is inverse proportional to the switching frequency. In order to keep switching losses as low as possible with an acceptable ripple, we have decided to use a 5 kHz switching frequency.



3.1 – Switching losses vs. frequency in DC mode at I_{nom} = 447A [11]

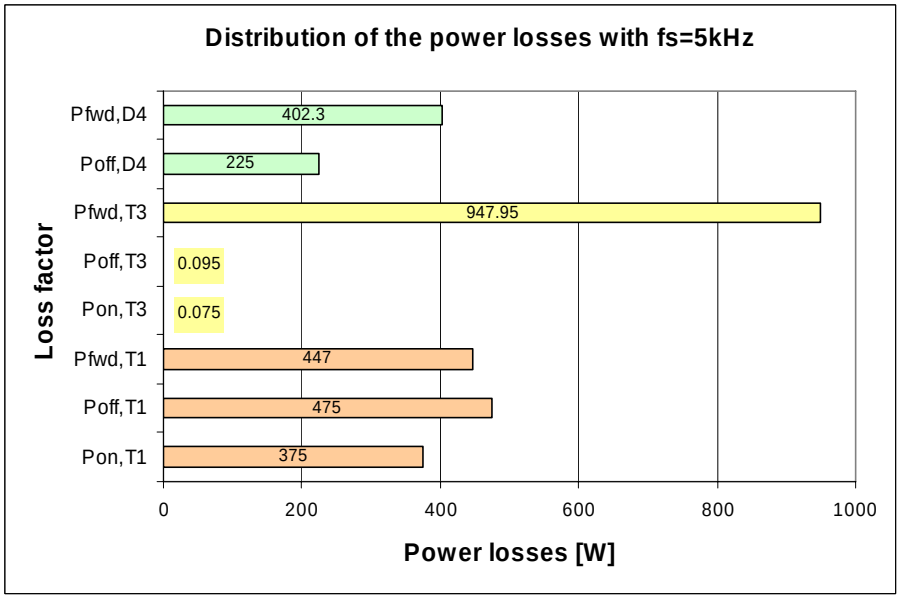
As shown in fig. 3.2, the power losses for the pulsed mode at nominal current are always below those obtained with the DC mode as the duty cycle is lower.



3.2 - Switching losses vs. frequency in 1Hz mode, 460ms pulses at I_{nom} = 447A [11]

3.4 Analysis and distribution of the losses

Assuming a 5 kHz switching frequency and a nominal current of 447A, a distribution of the losses for each single semiconductor can be made. From equations (1) and (2) we have:



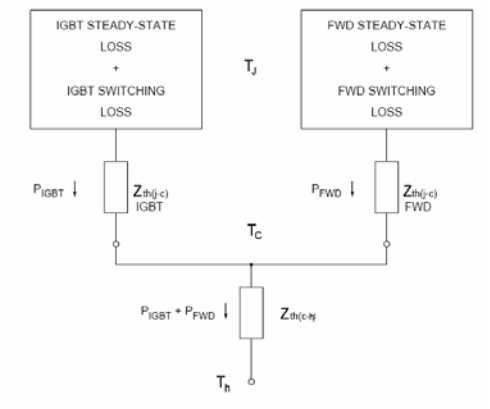
3.3 – Distribution of the losses between power modules for a 5 kHz switching frequency in DC mode [11].

Figure 3.3 indicates that the $IGBT_1$ switching losses exceed its conduction losses. On the other hand only conduction losses are significant for $IGBT_3$. For the operational DC mode, the total average power losses in each power semiconductor are the following:

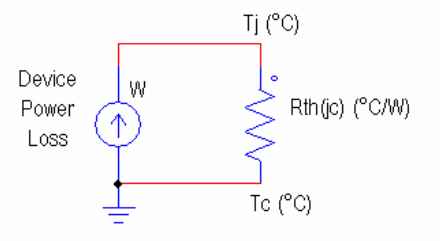
- $P_{tot,\ IGBT1} \sim 1297$ W
- $P_{tot,\ IGBT3} \sim 948$ W
- $P_{tot,\ D4} \sim 627$ W

4. EVALUATION OF THE AVERAGE JUNCTION TEMPERATURE T_{JAVG}

Once the total average power dissipated in the semiconductor device and the module base plate temperature are known, the junction temperature can be estimated using thermal resistance concepts as shown in Figure 4.1. Good design practice is to limit the worst case maximum junction temperature to 125 °C or less. Reliability can be enhanced by operating the semiconductor junction at lower temperatures. An electrical model can be used to predict temperature rise based on steady state power loss as shown in figure 4.2. Power loss is modeled as a current flowing through a thermal resistance which creates a temperature rise modeled as a voltage rise. Additional resistors could be added in series to model case to heatsink $R_{th(ch)}$ and heatsink to ambient $R_{th(ha)}$ thermal resistances.



4.1 – Thermal resistance concept [6]



4.2 – Thermal resistance model

The average junction temperature is calculated using (5).

$$T_{j,avg} = P_{tot,avg}.R_{th(jc)} + T_c \qquad (5)$$

- $P_{tot,avg}$: average total power [W]
- $T_{J,avg}$: average junction temperature [°C]
- $R_{th(jc)}$: junction to case thermal resistance [°C/W]
- $R_{th(ch)}$: case to heatsink thermal resistance [°C/W]
- T_C : case temperature

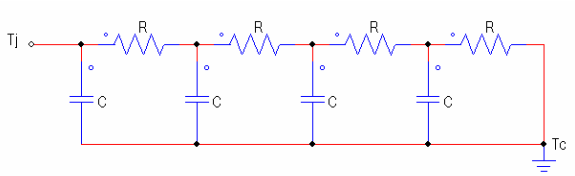
R_{thjc} is specified in the datasheet. Ratings such as maximum continuous DC current, total power dissipation and frequency versus current are based on a maximum $R_{th(jc)}$ value which incorporates margin to account for normal manufacturing variations and provide some application margin as well. The industry trend is toward decreasing the margin between the maximum $R_{th(jc)}$ value and the typical value, which is usually not published [4]. Assuming a case temperature of 70 °C and power losses in §3.4 the junction temperatures are calculated by (5) and given in the table 4.1.

SC	$P_{tot,avg}$ [W]	$T_{J,avg}$ [°C]	For $T_c \leq 70$°C	$T_{J,max}$
$IGBT_1$	1297	$T_c + 23.35$	$T_{J,avg} \leq 93.35$°C	< 150°C
$IGBT_3$	948	$T_c + 26.10$	$T_{J,avg} \leq 86.10$°C	< 150°C
D_4	627	$T_c + 25.09$	$T_{J,avg} \leq 95.09$°C	< 125°C
D_{bypass}	404	$T_c + 56.56$	$T_{J,avg} \leq 126.56$°C	< 185°C

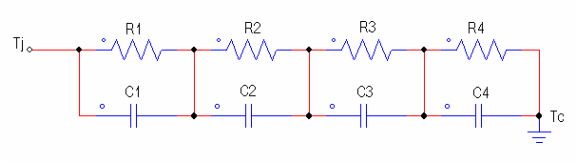
Table 4.1 – Average junction temperature - DC mode (I=447A) [11]

5. POWER CYCLING AND THERMAL FATIGUE

A final thermal design consideration is the temperature range, ΔT_J, through which the junction will cycle as the power module operates in the specified application. The concern here is thermal fatigue due to the heating and the cooling processes which produce mechanical stresses caused by the different coefficients of expansion of the various component materials. This differential expansion puts the intermediate layers under bending and shear stress. With the accumulation of these stress cycles the assembly structure can deteriorate causing eventual failure. The thermal behaviour of semiconductors can be described by the two following models:

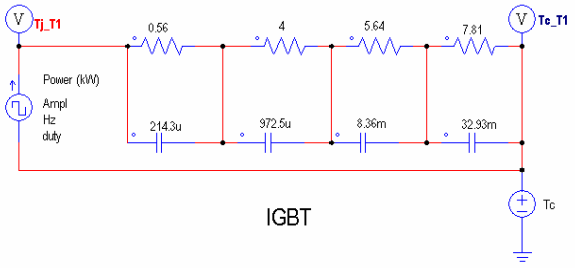


5.1 – Continued fraction model

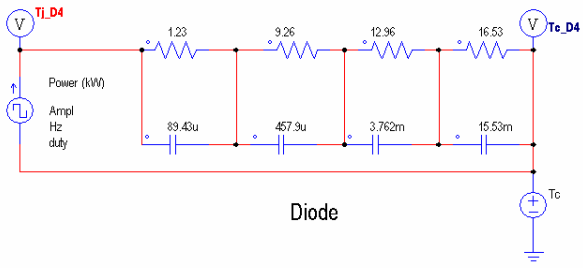


5.2 – Partial fraction model

The continued fraction model (figure 5.1) reflects the physical layer structure of a semiconductor with thermal capacitances and thermal resistances in between. The RC cells are assigned to the layer structure of the module (chip, solder, substrate, baseplate). The separate RC cells of the partial fraction model (figure 5.2) have no physical meaning. Their values are extracted from a measured heating-up curve of the module by an analysis tool. Usually the manufacturer provides these partial fraction coefficients either as a table or as time constant. Considering the switching and conducting losses for the pulse operation modes described in the specifications [1], the junction temperature of the IGBT and the free wheel diode can be simulated according to the following circuit (if available, the modeling of the heatsink may possibly be added).



5.3 - Partial fraction model used for the IGBT [11].

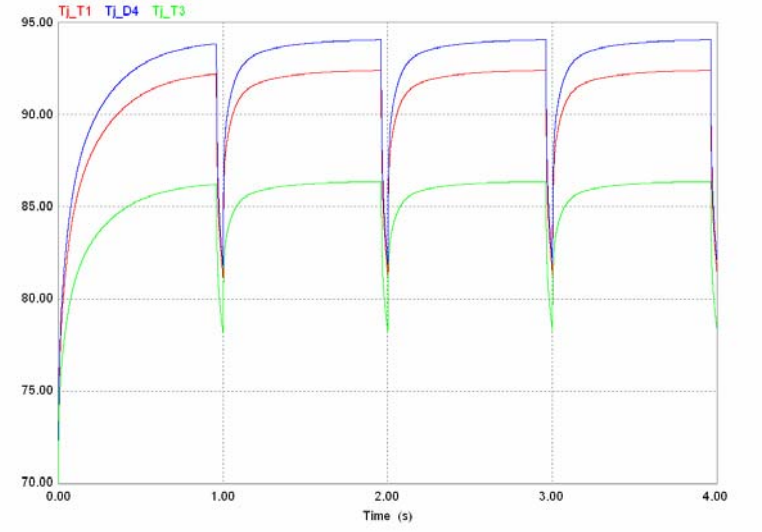


5.4- Partial fraction model used for the fwd diode [11]

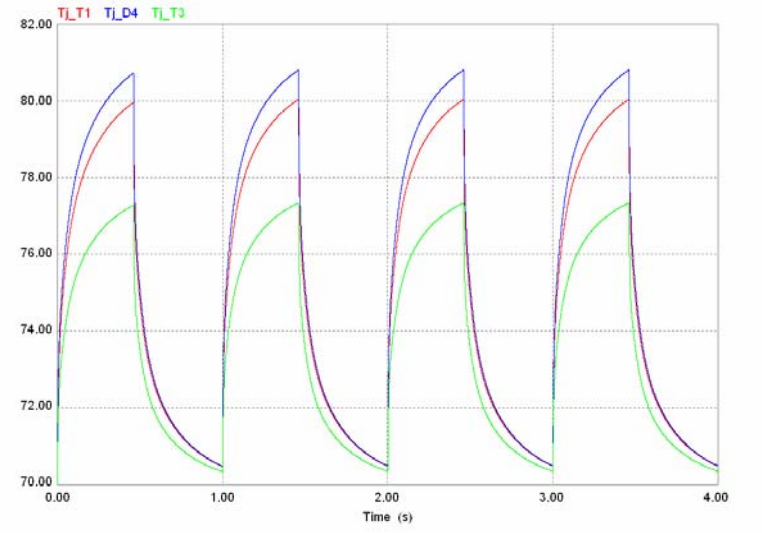
Pulse duration [ms]	$P_{tot,IGBT1}$ [W]	$P_{tot,D4}$ [W]	$P_{tot,IGBT3}$ [W]
960	1245	602	910
460	596	288	436
20	26	12	19

Table 5.1 – Average total power for the specified pulse modes at I_{nom} (447A) and f_s =5kHz.

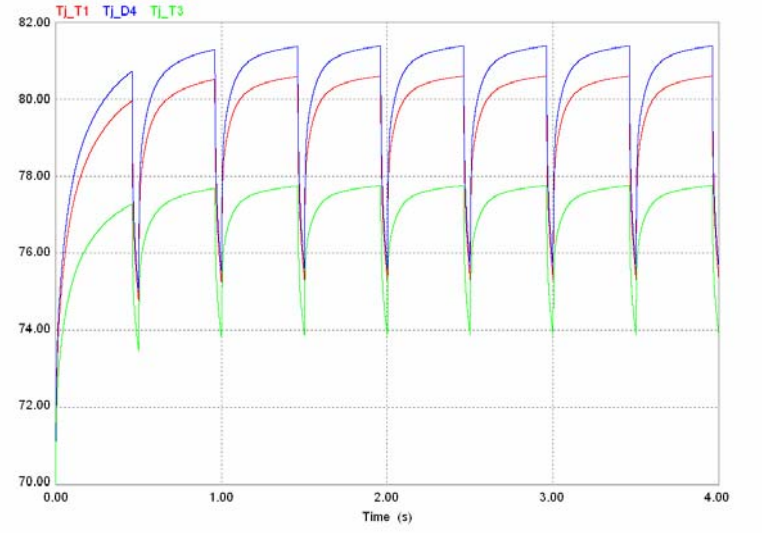
Assuming a T_C of 70°C, the following results are obtained by simulations with PSIM6.1© [11].



5.5 – Simulation of ΔT_J – Mode 1Hz; 960ms pulses.

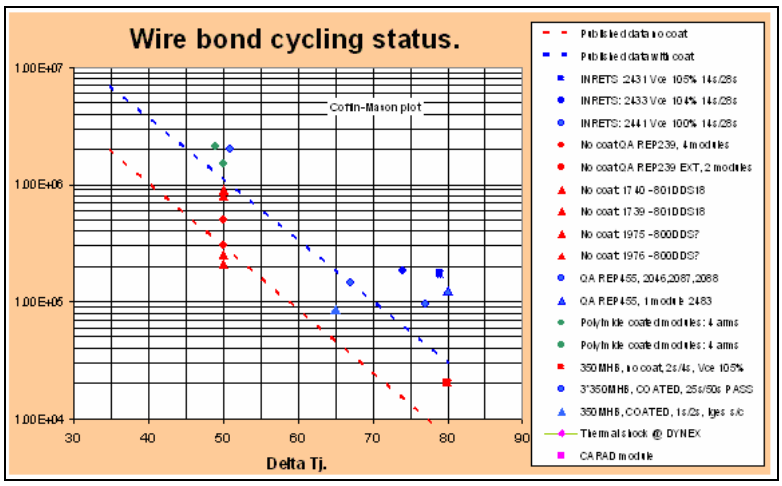


5.6 - Simulation ΔT_J – Mode 1Hz; 460ms pulses.



5.7- Simulation ΔT_J – Mode 2Hz; 460ms pulses.

The simulations indicate that the ΔT_{Jmax}, trought which the junction will cycle, is around 15°C (figure 5.5). Studies of this phenomenon create curves that indicate cycling life as a function of the ΔT_J excursion. These curves are specific to particular temperature, time, and operating ranges, so that a general curve cannot be generated and published. Experimental studies have shown that a relatively long heating and cooling cycle of the order of two minutes that causes the base plate temperature of the module to change along with the junction temperature is usually the worst case. All available information indicates that thermal fatigue is not an issue when ΔT_J is kept below 30 °C [6].

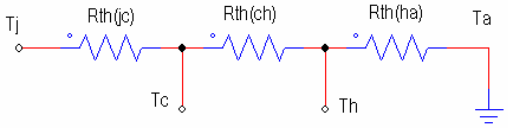


5.8 – Wire bond cycling status of the Dynex IGBT [11]

By extrapolation on the wire bond cycling status provided by the manufacturer (figure 5.8) we can estimate that the wire bond cycling for $\Delta T_J = 15$ °C should be around 5.00E+07 i.e. about 13900 hours considering the worst case i.e. the 1Hz mode with 960ms pulses.

6. DESIGN OF AN APPROPRIATE AIR FORCED COOLING SYSTEM

According the specifications [1] there was no water cooling available so a forced air cooling system has been designed. Average life expectancy for a semiconductor is greatly increased if a lower junction temperature is maintained. The method of cooling must ensure that T_{Jmax} of each module is not exceeded and kept as low as possible. An equivalent circuit based on the thermal resistance concept can be used to represent heat conduction in a semiconductor device.



6.1 – Equivalent circuit for heat conduction in a SC

Considering that the power losses are created in the junction, the average junction temperature can be calculated with (6).

$$T_j = P_{tot,avg}.\left(R_{th(jc)} + R_{th(ch)} + R_{th(ha)}\right) + T_a \quad (6)$$

With:

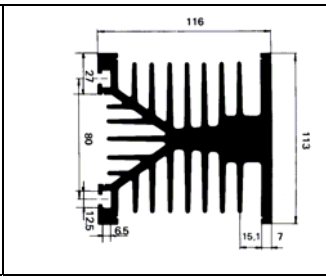
- $R_{th(jc)}$:junction-case thermal resistance
- $R_{th(ch)}$:case-heatsink thermal resistance
- $R_{th(ha)}$: heatsink-air thermal resistance

Because of thermal capacitance, heatsinks generally only respond to average power except at low frequency. As shown, at low frequencies the ΔT_J within a given device may be appreciable.

6.1 Evaluation of the heatsinks

The thermal resistance of a heatsink is governed primarily by its mass, surface area, coolant flow-rate, and the material from which it is made (i.e. specific heat capacity, thermal capacitance and thermal resistivity). Many factors can affect heatsinks performance such as the size of the heat source placed on the heatsink, the orientation of the heatsink, etc. Considering the half bridge power module used here, the thermal resistance of the heatsink must satisfy the equation (6) assuming that the arm H_1 hold $IGBT_1$ and D_4 and arm H_2 hold $IGBT_3$. We have $R_{th(ha)} \leq 70.38°C/kW$. Each power module is equipped with 2 heatsinks whose parameters are shown here below. The diodes are mounted on a copper made heatsink (fig. 6.3), the thermal resistance is calculated as $R_{th(ch)} = \frac{d}{A.\lambda_{th}} = 0.032°C/W$.

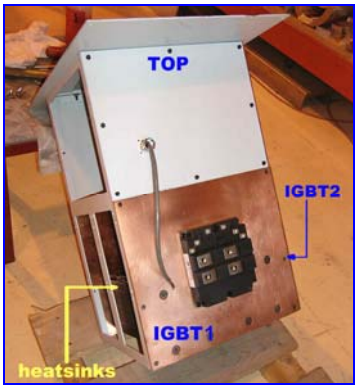
- *Schaffner WA820-0*
- *Aluminium black coated*
- *λ: 204 W/m.K*
- *Lenght/IGBT:2x300 mm*
- $R_{th(ha)}$ *<0.5 °C/W*



6.2 – Heatsinks used for the IGBT power modules

6.2 Design of a cooling case

As described in [2] we were not free to build a complete new system due to the cost constraint which imposed to use at maximum the already existing mechanical solutions. That was the case for the IGBT's cooling tower. As the system has been installed in a 19" ISO rack we have slightly modified the existing mechanics to cope with our requirements. As the connections of the power modules are electrically insulated from their base plates, several devices can be mounted on the same grounded heatsink. Then an external structure has been used. This structure is made of copper plates in order to channel the air flow and maintain a good thermal conduction. The IGBTs are mounted on the external sides while the heatsinks are mounted inside at the back of the modules. This solution provides compactness and allows installing fans on top and bottom as showed on figure 6.3.



6.3 - Cooling case with IGBT power module [11] - Heatsink for the diodes.

6.3 Evaluation of the required volumetric air flow.

The need for forced air cooling should be determined at an early stage in system design. It is important that the design plans for good airflow to heat-generating components also allow adequate space and power for the cooling fan. This technique reduces heatsink size but they need to be enclosed so that air flow is channeled down the fins. The required airflow depends on the heat generated within the enclosure and the maximum temperature rise permitted. The power dissipation figure used should be a worst-case estimate for a fully loaded system. The required volumetric air flow is calculated with (7).

$$G = \frac{Q}{\rho . C_p . \Delta T} \quad (7)$$

- G: volumetric flow rate [m^3/s]
- Q: heat transferred to the system [W]
- ρ : air density [1.293 kg/m^3]
- C_p: specific heat of air [1005J/kg.K]
- ΔT: temp. differential to outside [K]

Assuming the average total power in table 3.1 and a ΔT of 40°C the minimum required volumetric air flow is 196 m^3/h.

6.3.1 *System impedance*

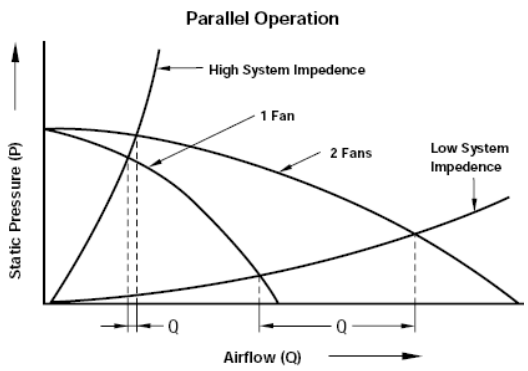
Determining the actual airflow produced by a fan mounted in an enclosure is much more difficult than calculating the airflow required. Obstructions in the airflow path cause static pressure within the enclosure. For a typical fan the relationship between airflow and static pressure is nonlinear. To achieve maximum airflow, obstructions should be minimized. However the system components themselves obstruct the airflow and sometimes channels may be necessary to direct the airflow over the components that need cooling. In practice, empirical methods are normally used to estimate airflow resistance. Experience shows that [10]:

- An empty enclosure usually reduces airflow by 5 to 20 %.
- A densely packed enclosure reduces airflow by 60 % or more.
- Most electronic enclosures have a static pressure between 10 Pa and 40 Pa

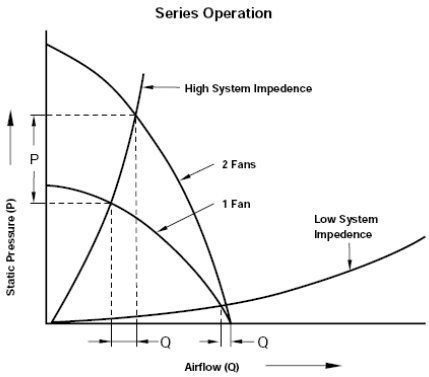
The cooling case equipped with the heatsinks is pretty dense so the reduction of airflow has been estimated between 60% and 80%. This means that the required volumetric air flow must be between 312 and 351 m^3/h.

6.4 Use of multiple fans

In some situations, additional fans are used to increase the dispersion of air within the enclosure. Also, redundant fans may be used to increase system reliability. On the other hand an additional fan can create problems. It doubles the cost, the noise, and the heat generated by fans, and may provide only a minimal improvement to the cooling.



6.4 – Ideal performance of two fans in parallel



6.5 - Ideal performance of two fans in series

Two fans in parallel double the airflow only in the hypothetical free air situation. If the enclosure has a high static pressure, this arrangement provides very little increase in flow. Two fans in series double the static pressure at shut-off but do not increase the airflow in the free air situation. An additional fan in parallel increases airflow in a low static pressure situation and an additional fan in series increases the airflow in a higher static-pressure enclosure (figures 6.4 and 6.5). Fans can be mounted to exhaust warm air from, or blow cool air into, an enclosure. Theoretically, the same volume of air is used to dissipate heat. However in real applications, each arrangement has advantages and disadvantages. Air that is drawn into the fans has a laminar flow, this allows for a uniformly distributed airflow velocity in the enclosure which helps to eliminate stagnant air and hot spots. Air exhausted from the fans is turbulent. Heat dissipation in a turbulent airflow can be up to double that of a laminar flow with the same volumetric flow rate. But, the turbulent airflow region near a fan exhaust is limited. To improve air flow and to have redudancy we have decided to use multiple fans in series and in parallel. One fan on top is used to exhaust warm air from the enclosure (figure 6.6) and four fans on the bottom are used to blow cool air into the enclosure (figure 6.7). The total theoretical volumetric flow rate is 505m^3/h max.

- SFMI type SFP126
- 2750 rpm,
- 220 V, 50 Hz, 48 W
- Diam. 200 mm
- G: 325 m^3/h max.

6.6 – Top side fan used to exhaust warm air from enclosure.

- Type 125XR0181000
- 3000 rpm,
- 220 V, 50 Hz, 15 W
- Diam. 125 mm
- G: 180 m^3/h max.

6.7 – Four fans used to blow cool air into enclosure (bottom side)

7. TESTS AND MEASUREMENT

The measurement reported in table 7.1 has been done using a Tektronix DTM 920 thermometer with a thermocouple K type fitted close to the base plate of the power modules. The operational mode considered here is the DC mode with a current of 450 A. The results are comparable to the values calculated in table 3.1. Nevertheless with a current of 500 A the measurements showed that the case temperature were increasing up to 76.9°C (H_1) and 79.0°C (H_2). As a consequence two lateral fans have been added close to the power modules. Thereafter the measurement done indicated a decrease of the case temperature of about 7°C to 8°C. This is close to the limit (70°C) defined during the design.

Power Module Arm	$P_{tot,avg}$ [W]	T_C Measured [°C]	T_J (T_a~25°C) [°C]	$T_{J,max}$ [°C]
H1	1924	70.3	$T_J \leq 95.3$	<150°C
H2	948	67.5	$T_J \leq 92.5$	<150°C

Table 7.1 – Power module T_C measured with I=450A

7.1 Thermal protection and interlocks

Thermal switches with a thermal threshold fixed at 90°C have been installed on the copper plate closed to each power module base plate. In case of such an interlock the junction temperature will be less than 120°C.

8. CONCLUSION

We learned that the study of the thermal behaviour of such a system must be carefully undertaken at an early stage. The initial design had to be reshuffled by an important modification improving the cooling system. After this modification, the final measurement in DC mode indicated a junction temperature around 95 °C i.e. well below the T_{Jmax}.

In the traction domain the study of the transient behaviour of such complex power modules using conventional approaches and simple thermal models (based on circuit simulators) have encountered significant difficulties in accurately predicting their transient behaviour. In such a case, specific techniques based on electro-thermal coupling simulation have to be used [8].

Finally, the results of the analysis of the thermal behaviour and the fatigue estimation showed that the power converter life time remain acceptable (around 14.000 hours) considering the worst case i.e. the 1 Hz, 960ms pulse operation mode as defined in the specifications. A possible improvement of the system should be to install a water cooling system in order to reduce further the case and junction temperatures.

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