ADCs to DACs (analog-to-digital and digital-to-analog converters)

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Abstract
ADCs and DACs are crucial components in the relentless drive to replace analog circuitry with more controllable and less costly digital processing. This paper reviews the technologies available for measurement and control as applied to accelerators. It covers much of the terminology and 'specmanship' together with an application-oriented analysis of the performance to be expected of the various types. Finally, some guidance on system integration problems is given.

1 Introduction

ADCs and DACs are some of the most important components in measurement and control technology. Their job is to transfer information to and from the real world and the digital world as faithfully as possible. See Fig. 1 for a typical situation.

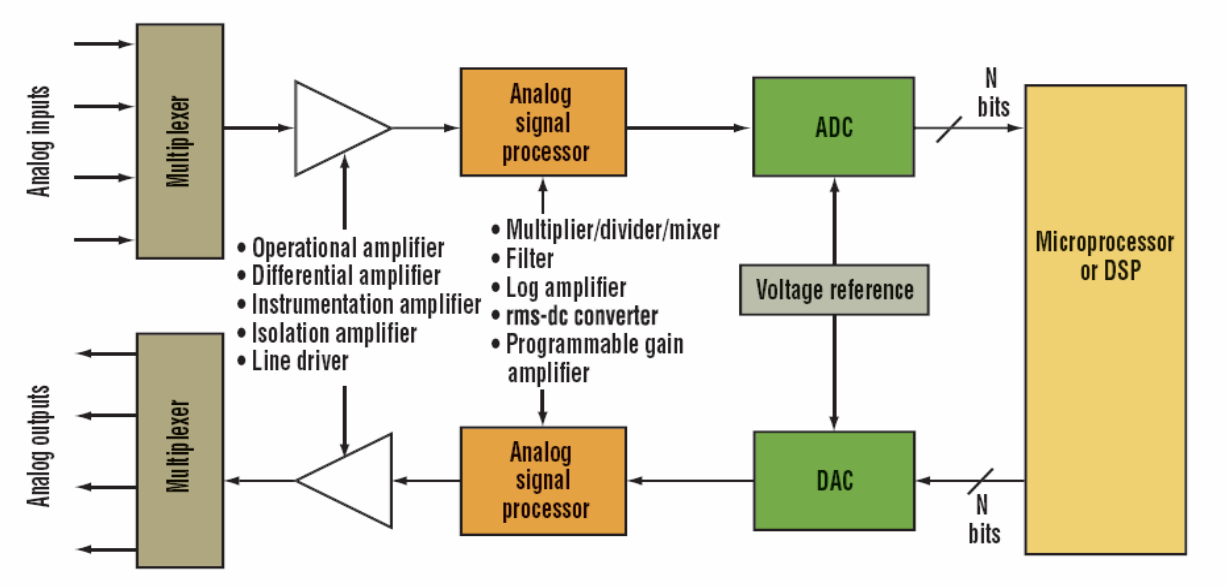

Fig. 1: ADC and DAC in measurement and control loop applications

Because of the advances in digital processing and its continuing improvement in cost effectiveness, it is becoming more and more desirable to trade off analog for digital circuitry. An expression for this, commonly used in the communication business, is the trend to push 'digital to the antenna', thus notionally replacing all of the circuitry in a communication receiver with digital processing. However, the purpose of this article is to consider ADC and DAC use in low-frequency applications, say DC to audio, where some of the newer ADC 'dynamics' terminology is less appropriate.

2 Terms, nomenclature and specifications

Three standards that define specification terms for ADCs and DACs are

– IEC 60748-4, Ref. [1]

– IEEE 1241, Ref. [2]

– DYNAD (DYNamic testing of Analog to Digital converters), Ref. [3]

The IEC standard currently includes general specifications and is being updated to include the dynamic specifications that are covered by the other two standards. These, the IEEE 1241 and DYNAD (which is the output of a European project SMT4-CT98-2214), concern dynamic specifications defined mainly in the frequency domain. These are, perhaps, less important for DC and LF but should be understood because the same terminology is now used in many IC ADCs and DACs manufacturers' data sheets.

3 General specifications

The most important terms are best discussed with reference to simplified diagrams showing a 7-bit converter. In all the ensuing discussions we shall deal only with converters intended to have equal step sizes—(that is each bit or quantization level is of equal weight). This is not true of certain specific converters, for example, companding types.

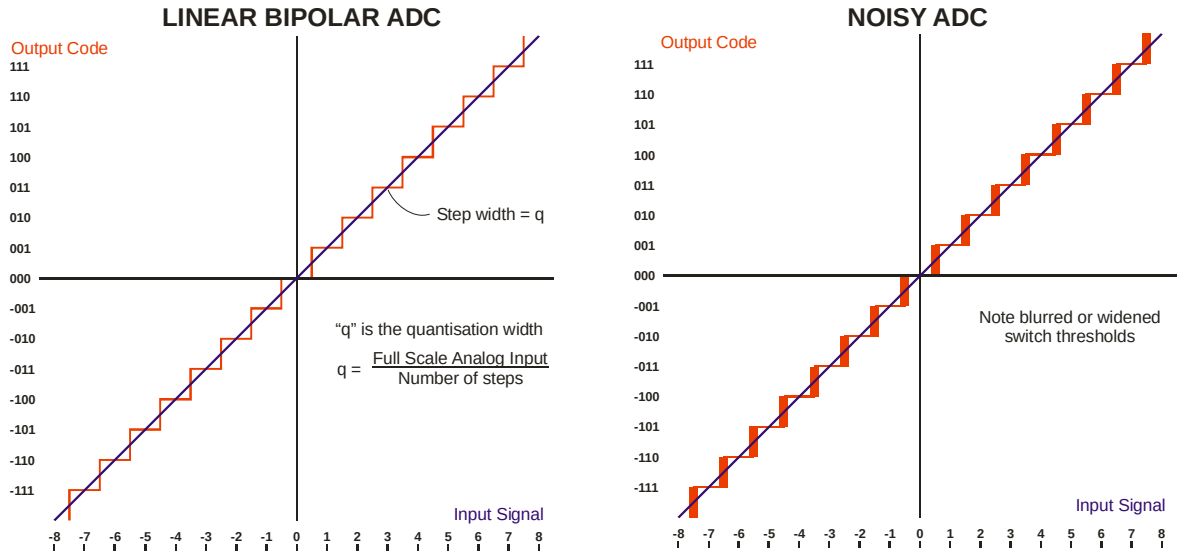

Fig. 2: Ideal bipolar ADC

In Fig. 2 we have an ideal bipolar converter where the vertical scale is the output code and the horizontal scale the analog input. Each step in code represents an analog increment of '*q*', called the step width. As can be seen, starting from 0, each step occurs at *q*/2 analog levels. The second diagram shows the same with some random noise added which results in an uncertainty in the switching thresholds. In these and all of the ensuing descriptions and figures we assume that zero and end-point errors have been corrected by a '$y = mc + c$' calibration.

3.1 Misunderstood terms

There are many misunderstood or misapplied terms of which ‘resolution’ and ‘noise’ are probably the most important.

‘Resolution’ is the smallest discernible increment in analog terms—however, this should be regarded as ‘repeatably’ discernible since all good measurement should be repeatable—another way of saying the increment in question is not buried in noise or instability. A weakness, in this author’s view, of IEC 60748-4 is that it defines resolution as the ‘nominal value of the step width’ which is far too simplistic and misleading for some types of ADC.

‘Noise’ comes from many sources and is not necessarily either random or ‘white’ since 1/*f* noise is always present. As far as specification numbers are concerned, noise is also represented very differently for different applications. In DVMs it usually means ‘peak’ but in most Integrated Circuit (IC) ADCs it is r.m.s. Presenting it as a percentage of full scale is another option. In DVMs full scale is generally considered as the maximum unipolar excursion possible while in IC ADCs as the full range from +ve peak to –ve peak operating range. The result is that the value can vary by 6:1 or more, depending on these definitions.

3.2 Quantization error or noise Q_n

The quantization error of a perfect ADC is that error introduced by the finite number of digital codes, i.e., from the nominal step size. Figure 3 shows this. One can clearly see that the error, as signal is smoothly increased, changes in a saw-tooth manner between +*q*/2 to –*q*/2 where *q* is the nominal step size.

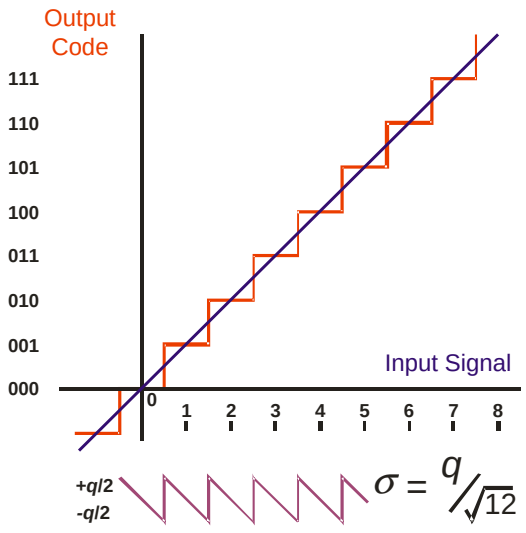

Fig. 3: ADC: quantization error or noise Q_n

This has a standard deviation of $\sigma = q/\sqrt{12}$ and so, in dynamic applications where there is little correlation between the error and the input signal, it is referred to as ‘quantization noise’ and has a magnitude of:

$$Q_n = \frac{q}{\sqrt{12}} \text{ r.m.s.}$$

3.3 Differential non-linearity (DNL)

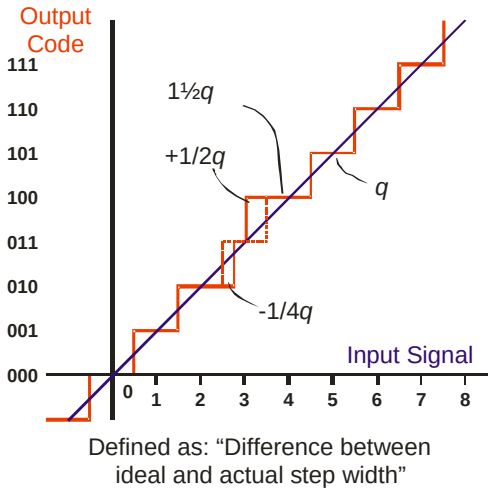

Fig. 4: ADC with differential non-linearity error, monotonic and no missing codes

This is a measure of how individual steps may be in error (for example if the comparator bias is incorrect). It is the difference between the ideal step position (in analog terms) and its actual position. A good ADC will hold this error to $q/2$. (See Fig. 4.)

If the DNL exceeds $q/2$, a missing code may occur, i.e., the converter ‘jumps’ between non-adjacent codes. (See Fig. 5.)

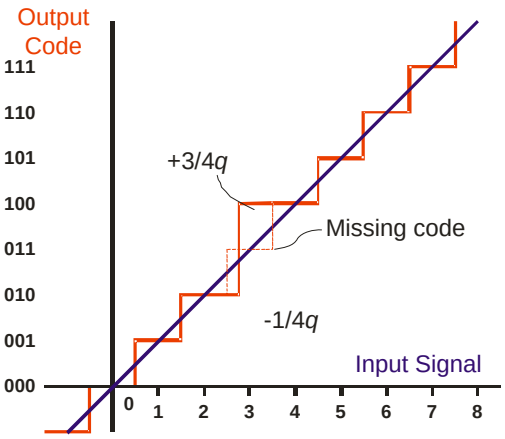

Fig. 5: ADC with differential non-linearity and missing codes

3.4 Non-monotonic

Non-monotonic literally means that two different analog values separated by an appreciable increment produce the same code; this may indeed happen.

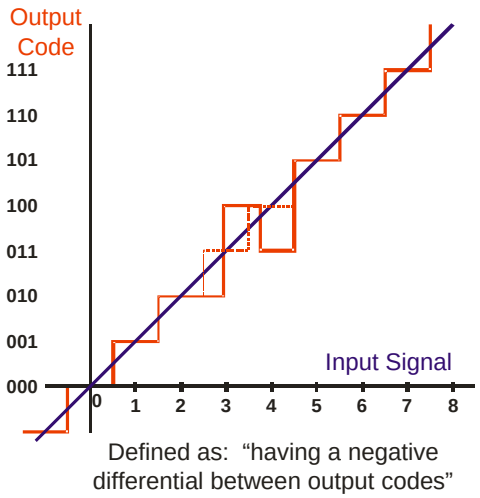

Fig. 6: Non-monotonic ADC, no missing codes

However, although the term 'non-monotonic' is still used, it is better defined as a negative differential of code values for smoothly incrementing analog values. The example of Fig. 6 is a special case, showing how this can happen without there being a missing code, although a missing code is a more likely result.

3.5 Integral non-linearity (INL)

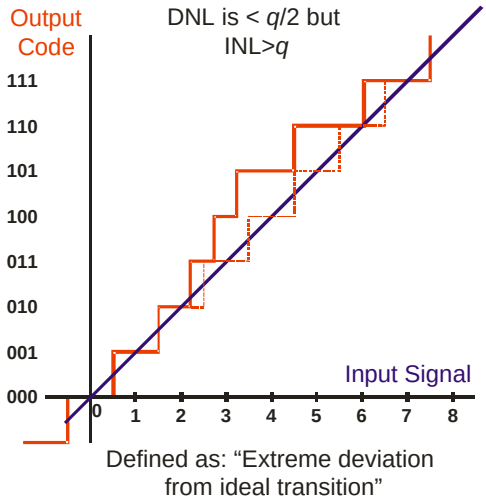

Fig. 7: ADC with integral non-linearity error

The condition shows in Fig. 7 can affect all types of ADC and DAC whereas DNL would not normally affect integrating types such as charge balance and Σ-Δ (delta-sigma). It is defined as the difference between the actual transition at any level and the ideal transition. It occurs where there is an accumulation of very small DNL errors over a range of steps or input signal. It is important to appreciate how it is specified because one can define the ideal transitions as standing on a straight line between zero and full-scale endpoints or as on a 'best fit' regression line. In this case INL errors may be distributed symmetrically about a straight line rather than appearing at twice the magnitude on one side only.

3.6 Dynamic terms

ADC data sheets will often be written in terms of AC 'frequency-domain' specification and it is important to understand some of the terms used even if the application is more 'time-domain' or DC related.

3.6.1 SNR (signal-to-noise ratio)

This and the following terms apply when the ADC is used to digitize a sine wave set to an amplitude whose peak-to-peak value equals the maximum to minimum capability of the ADC. However, this is then translated to ratios of r.m.s. values. SNR is the r.m.s. ratio of the full scale sine wave to the total random noise present, assuming that the quantization noise is random and uncorrelated with signal or other noise. It is a function of the frequency and amplitude of the signal and is therefore specific to a given signal.

3.6.2 SFDR (spurious free dynamic range)

Non-linearities and intermodulation products introduce harmonics and spurs into the output spectrum, usually observed through FFT (Fast Fourier Transform) conversion. The SFDR is the range (in dB) between the fundamental and the highest harmonic or spur that occurs within the Nyquist range of half the clock rate of the ADC (or over a specified range). Clearly it too will be a function of the amplitude and frequency of the applied signal although the full-scale amplitude previously described is usually assumed to give the best ratio.

3.6.3 SINAD (signal to noise and distortion)

This term is used commonly but, whilst useful for an overall system specification, it is less so to a designer choosing an ADC to use. It is the SNR but with the spurs and harmonics of the SFDR included and assumed to be an additional uncorrelated noise source. Clearly, in practice when designing a system, one needs to be able to distinguish between truly random terms and signal-dependent terms, especially if the system performs some sort of filtering or averaging that can reduce the effects of random noise but not of distortion.

3.6.4 N_{ef} or 'ENOB' (effective number of bits)

Most IC manufacturers use the term 'ENOB' where DYNAD uses N_{ef} and IEEE 1241 uses 'Effective bits', E. It is used to specify for an ADC's degradation in resolution when making a measurement where the ADC introduces noise, distortion, and spurs. It is thus related to SINAD and can be shown to be (or is defined to be)

$$N_{ef} = ENOB = \frac{(SINAD - 1.76)}{6.02}\text{dB},$$

where SINAD is expressed in dB of FS.

3.6.5 'Oversampling'

This term is used to describe the operation of a converter where samples are taken at a higher rate than twice the input signal's highest frequency (the Nyquist rate) and some sort of result is obtained by combining these samples. By definition it is implied that the input signal is AC but oversampling ADCs operate by computing their result from many samples and these work just fine with DC! In reality an oversampling ADC is one in which a number of samples of the analog signal are combined to give a better result (usually higher resolution) than any one sample provides. In order to do this there must be a variation in the result of each sample of a perfectly steady signal; this is ensured by inherent or added noise, usually called 'dither'.

4 Types of ADC (and DAC)

4.1 Flash ADCs

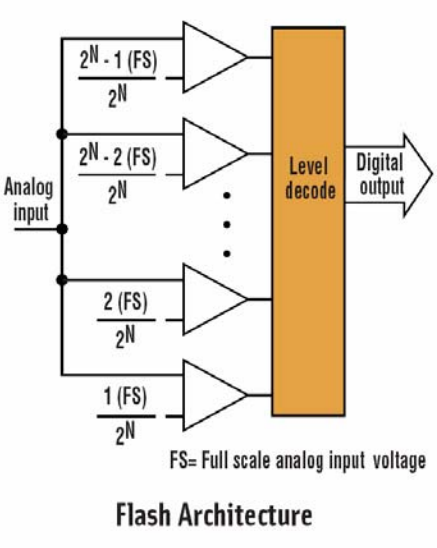

Fig. 8: Flash ADC architecture

Flash ADCs at their simplest can be made with a single comparator which senses a voltage threshold and drives a '1-bit' logic level. More generally they are made with many such arrangements in parallel, each comparator set to a different threshold (Fig. 8). The threshold normally divides a full-scale range by the number of comparators.

With IC densities increasing all of the time, one would think that flash converters would be increasing in resolution and decreasing in cost.

However, modern high-density processing is accomplished mainly in low-voltage technologies which require even greater accuracy and lower noise of the comparator thresholds. This, of course, makes the processing and testing expensive.

The flash ADC is almost unique in not incorporating a DAC in an internal loop. This makes it particularly fast, with a very direct path from analog input to digital output. It is the workhorse component, at varying resolution, from 1 bit to 10 bits, within other types of ADC architecture, particularly 'pipeline' and Δ-Σ.

4.2 Pipeline ADCs

Pipeline converters, as shown in Fig. 9, retain most of the bandwidth capabilities of flash ADCs but at higher resolution.

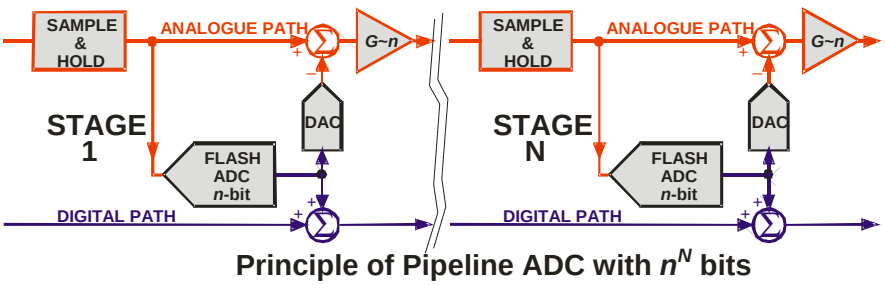

Fig. 9: Principle of pipeline ADC with n^N bits

They do this by incorporating a number of stages of flash ADC and DAC in series. This is the pipeline: each stage converts, say, *n* bits in the flash ADC but then uses the DAC to subtract the actual flash ADC output, converted to analog from the incoming signal, to derive an analog remainder. This is amplified by *n* and fed to the next stage to be digitized. Broadly speaking, with *n* stages, the resolution is n^N but a large degree of self-adjustment has to be incorporated to prevent DNL errors, thus some resolution is 'wasted' at each stage. It should be evident from this description that the bandwidth can be virtually as high as that of the flash ADC converters involved, but that there is an addition of delays through the stages introducing considerable latency or group delay. For many communication applications, and indeed for oscilloscopes, this is not a problem.

4.3 Successive approximation register (SAR) ADCs

SAR ADCs have been around for a long time; even the earliest DVMs used them.

The SAR converter tests whether the input signal is above or below thresholds set by the ladder DAC (Fig. 10). Generally, one starts at one half of FS to determine the MSB then sets either one-quarter or three-quarter scale to determine the next bit and so on. In this example, the ADC in Fig 11 is simply a comparator but more complex arrangements can incorporate a flash converter.

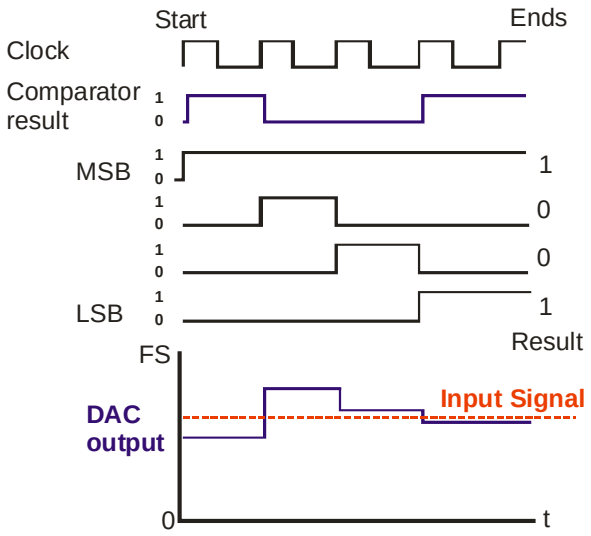

Fig. 10: SAR-ADC operation

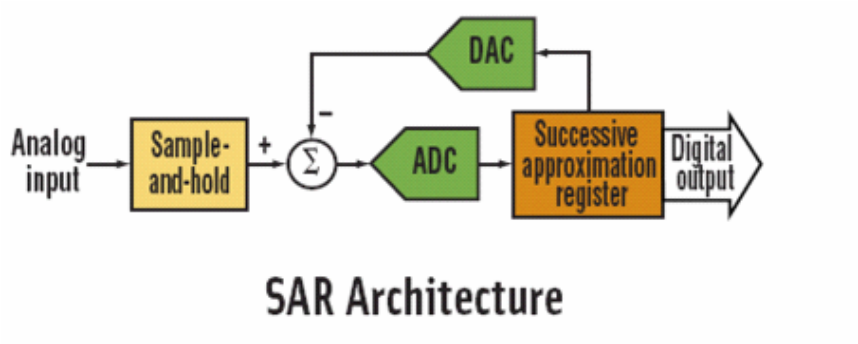

Fig. 11: SAR-ADC architecture

4.4 Charge balance ADCs

4.4.1 Charge balance ADCs with dual slope

The dual-slope converter is the most commonly used charge balance ADC (Fig. 12). For low-frequency measurements in simple DVMs and panel meters, it is very cost-effective indeed.

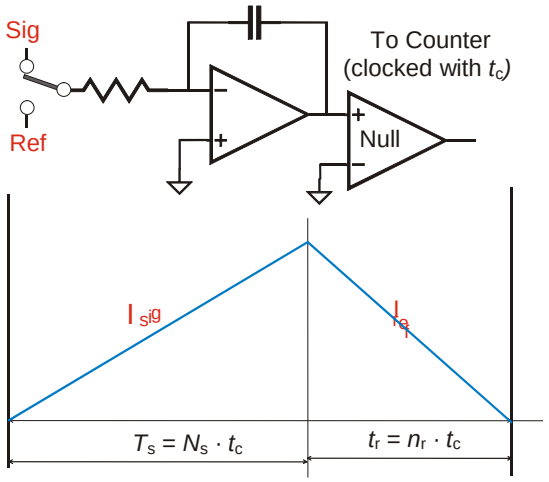

Fig. 12: ADC charge balance type with dual slopes

Basically it utilizes the unknown signal to be measured, to charge a capacitance during a pre-set time. It then discharges through the same components, with a known reference signal, and measures the time this takes. The analog accuracy is thus dependent only (to a first order) on the reference. Compare this to the SAR which needs as good a reference but also needs a highly critical ladder network of precision resistors or capacitors.

4.4.2 Charge balance ADCs with multi-slopes

A further refinement that can be used to get about an order of magnitude improvement in speed and/or resolution is used in 'top-end' DVMs like the Agilent 3458, Datron 1281 and Fluke 8508A. Here, in order to improve resolution, reduce the effects of null detector noise, and allow smaller integration capacitors to be used, glugs of reference current are removed while charging the signal (Fig. 13). As long as charge balance is maintained and 'accounted for' by the logic any such arrangement is valid.

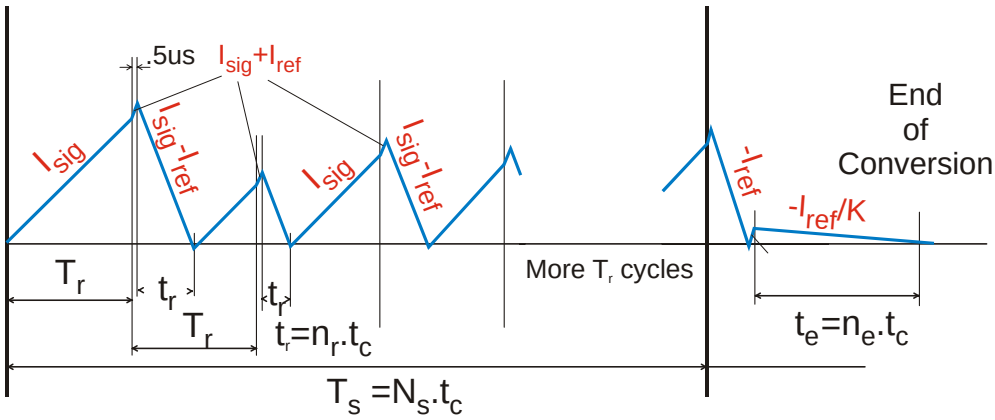

Fig. 13: ADC charge balance type with multi-slopes

As previously stated, there is a large discrepancy in custom and practice between specifying DVMs or ADCs. Table 1 expresses the specifications of top-end DVMs in a typical ADC format.

Table 1: Specifications of top-end DVMs in a typical ADC format

Specification description	DVM data-sheet specification	ADC 'bit' specification
Nominal resolution	±8½ digits	28 + bits
Real (2σ) resolution	±7½ digits	24 + bits
Integral non-linearity (INL)	0.1 ppm (1×10^{-7})	23 bits
Differential non-linearity	No spec. 'perfect'	28 bits

4.5 Sigma-Delta ADCs (Σ-Δ ADCs)

This relatively new conversion technique is usually thought of as a 'charge balance' technique but this is misleading. It is true that over very long periods of time it does maintain a charge balance in its integrator, but it produces valid accurate results much faster than would be expected from charge balance equations. In fact, for high resolution, several orders of magnitude faster. For example, the CERN Σ-Δ converter produces independent 1 ppm resolution conversions in only 1000 clock cycles where dual slope would need 1 000 000. See Ref. [4].

The slow take up of this technology for DC and LF metrology is perhaps due to the difficulty of explaining it with time domain arguments. The frequency domain proponents have no problem! See Ref. [5].

The converter of Fig. 14 uses a 1 bit DAC (which is very accurate in spite of its low resolution) and the action of the feedback loop is to drive the DAC with a bit stream that balances the incoming signal. Confidence in applying negative feedback-loop theory explains the operation in the time domain!

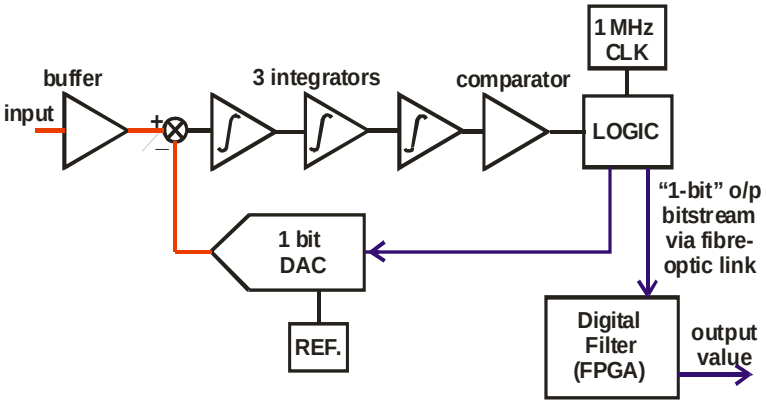

Fig. 14: Sigma-Delta ADC with 1 bit DAC and three integrators

The cumulative gain of the integration stages forming the modulation filter is very high indeed, in the CERN case of the order of 4×10^{11} at 10 Hz! Clearly, at 10 Hz there can be no significant error at the summing junction.

The cleverness of it is in achieving this within a loop whilst maintaining loop stability and, in effect, this is accomplished by feed-forward in the modulation filter. DAC versions of this arrangement, where the input is a bit stream and there is analog feedback around the loop, are

probably the most commonly produced data conversion components of all. They are the basis of the '1 bit' DAC in CD players and have been shipped in millions of units.

Figure 15 shows a simulation result for a 1 bit architecture that uses a digital 4 × 50 stage rolling average filter—thus obtaining all of its information in 200 clocks where dual slope could only achieve 0.5% resolution. The simulator clearly shows that the resolution far exceeds the 'simple' first-order dual slope capability.

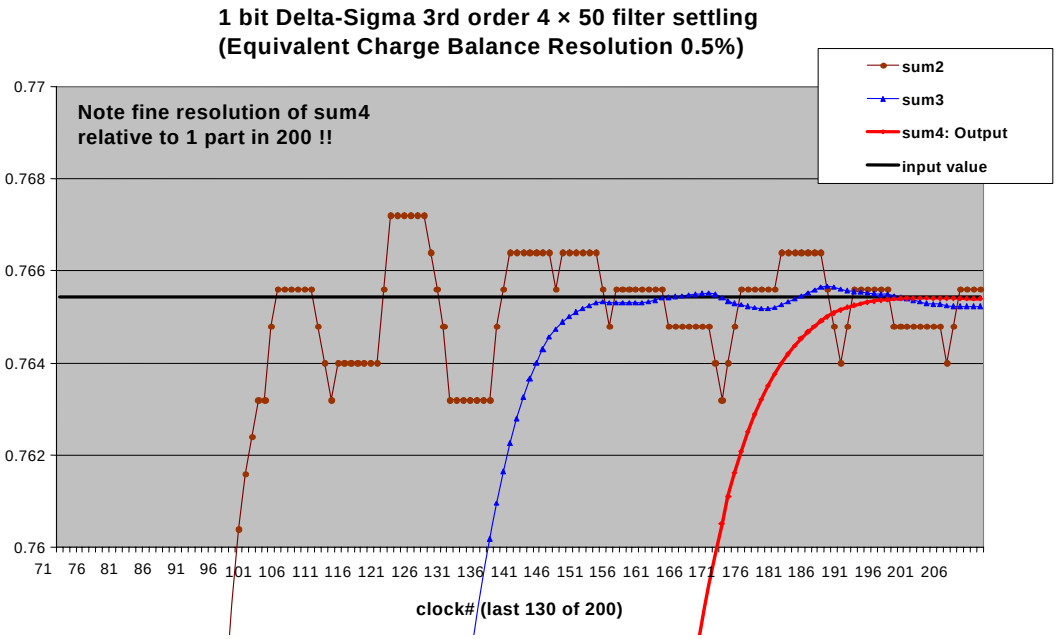

Fig. 15: Simulation results for a Σ–Δ ADC with 1 bit DAC and three integrators

4.5.1 Characteristics of Δ-Σ

Since Δ-Σ seems ideally suited to accelerator DC and LF work, it is useful to look carefully at its characteristics, both good and bad.

Using IC products from 'merchant semiconductor' companies may create some surprises. Since suppliers are mainly aiming Δ-Σ converters at AC applications, both specifications and performance are tailored for this—however, the volume of production brings the cost down.

Bandwidths are usually limited but, because of the very high sampling rate, anti-aliasing filters are simple. The multi-stage digital filters allow very high data rates but there are long delays and much of the data are redundant. Clearly, a newly applied signal must replace all data present from the last one and this typically takes as many clocks as there are filter stages. However, it is possible to 'look ahead' and take data from early stages of the filter concurrently with the final more filtered data. This, of course, can be used for feed-forward in digital control loops.

IC manufacturers promote their devices as, say, '24 bit' or '22 bit' where generally this is the resolution at the 1σ noise level and with the longest integration times (slowest speed) set, i.e., it is the SNR expressed in bits under the most favourable conditions. Linearity (INL) is seldom better than 5 ppm (or 18 bits).

Some problems are unique to Δ-Σ. Normally, because of the very high loop gain, the noise is sufficient to result in a sort of chaotic behaviour, thus there are no systematic errors in the output due to the loop operation. (Of course, there are other systematic errors, for example in the DAC accuracy.) However, it is well known that certain bit patterns in the feedback loop can be favoured which result

in very low frequency, resonance-like behaviour. In the frequency domain, these conditions look like very low frequency tones and they tend to be common when operation is near zero and the pattern therefore tends to be near symmetric. They are therefore called ‘idle tones’. They are, at least in part and perhaps totally, due to unwanted feedback paths (remember how high the loop gain is). They tend to show up more in single-chip devices where modulator and digital filters are in the same device.

Of similar nature and perhaps considered as a ‘zero-beat’ idle tone, is a characteristic called a ‘sticky zero’, a hysteresis condition where there is a tendency to lock at zero until the signal is sufficient to overcome the ‘glue’—an amount greater than the theoretical resolution. Again, great care in preventing unwanted loops between analog and digital seems to prevent this.

5 Choosing the best ADC for the job

Table 2 gives relevant performance against possible requirements. The relative merit scores cannot be taken as correct for all devices under all situations but do at least give an idea. Probably if one looks at the introduction of new devices from IC manufacturers it would be pipeline and Δ-Σ that have become the most prevalent in recent years.

Table 2: Relevant performance against possible requirements

\ADC type Characteristic	**Flash**	**Pipeline**	**SAR**	**Charge balance**	**Sigma-delta**
Throughput	excellent	v. good	good	poor	fair
Bandwidth	excellent	excellent	v.good	v. poor	fair
Resolution	poor	good	v. good	excellent	excellent
Latency/Hz	excellent	fair	v.good	poor	fair
Linearity/bit	v. good	good	fair	v. good	v. good
Multiplexing	excellent	poor	v.good	fair	poor
Other	power! cost	v. fast clock	DNL stability?	DC only	easy anti-aliasing

6 Choosing the right specifications

We have discussed the relative merits of different architectures and pointed out some specification pitfalls. There remain some aspects of system integration that are not always apparent.

1. Many devices have internal references which make it look as though an external component could be done without, but beware—internal references are usually of the band-gap type because of the low voltages available. Internally, a band-gap reference is derived from a very low voltage, 60 mV is common, and thus it is very noisy, particularly with I/f noise. Compensated zeners are at least an order of magnitude better than band-gaps.
2. Bipolar operation may not be easy and often is not ‘true’, that is the ADC is offset by half scale. The resulting zero performance is then dependent on the reference and internal DAC.
3. Ensure that the device you choose produces overload codes and flags that your system can handle—not all of them are user friendly.
4. Remember that INL is often orders of magnitude worse than quoted ‘bit specs’ and, even if the target application system can correct for this, there is usually no stability (of INL) spec.

7 Application problems

Assuming that an application system is designed with care and perhaps verified with simulation, there is still likely to be a 'first-time-round' problem. Noise. Noise problems are unlikely to show up in simulation and are very difficult to predict—experience suggests the following:

- use ground planes
- 'bury' HF traces between planes on inner PCB layers
- if possible make long-path HF signals differential and low voltage level
- use common-mode chokes
- THINK in terms of current paths—where does HF current flow?
- make signal 'flow' smoothly through the system
- do not forget that sampling can alias HF noise and bring it down to the frequency of interest
- HF connect ADC analog and digital grounds on a plane or with caps between planes.

At low frequencies it can also be useful to:

- use 'meccas' (all traces go to mecca!) to control current paths
- remember that $1/f$ noise cannot be averaged out totally and becomes a limit to achievable performance
- use chopper stabilization to overcome drifts and $1/f$ noise in amplifiers. With the availability of suitable components it is now cheap and simple
- prevent differential temperatures from being developed across sensitive circuit areas—i.e., prevent heat flow.

7.1 An example of an application

A very high performance ADC is being developed, see Fig. 16.

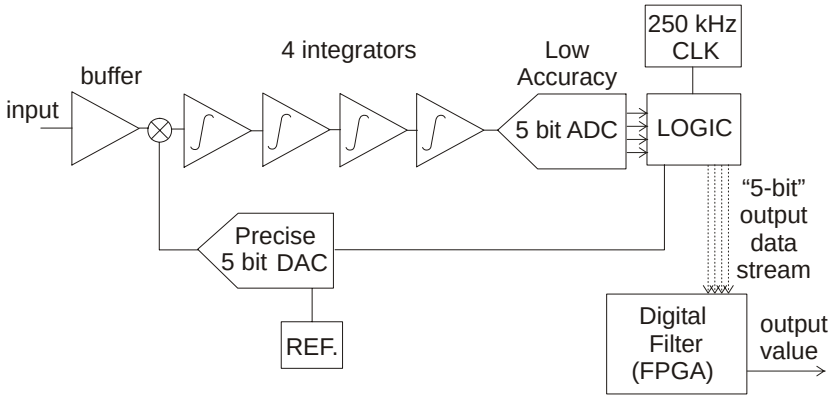

Fig. 16: High-performance Σ-Δ ADC with 5-bit DAC and four integrators

In this the 1-bit DAC is replaced with a 5-bit PWM DAC and the output comparator replaced with a 10-bit pipeline ADC of which five bits are used. This architecture is expected to achieve '28-bit' performance in resolution and 24 bits in linearity.

In order to achieve 5-bit resolution of the PWM at up to 500 kHz it is necessary to clock the pipeline ADC at 20 MHz. We thus have the difficult combination of 20 MHz clocking on the same PCB near to where 100 nV DC performance is needed!

Figure 17 shows the layout arrangement chosen, about half full size.

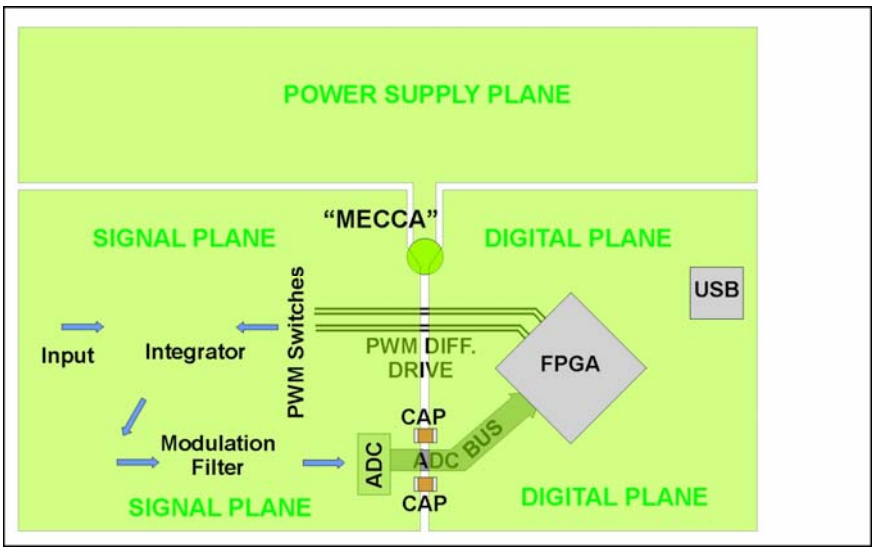

Fig. 17: Layout arrangement of Σ-Δ ADC with 5-bit DAC and four integrators

The PWM drive (with sub n_s edges) is passed from the FPGA to the analog with differential signal traces (and indeed the analog switching is differential). A mecca localizes LF currents and prevents those in power supply and digital planes from causing voltage drops in the signal plane.

However, a problem was found—there was excess HF noise 'everywhere' when the pipeline ADC was operating. A little thought about current flow elucidates this. In driving the FPGA, the ADC drives capacitance loads to ground on the digital plane. This current must pass back to the ADC and has to do so via the mecca creating quite a wide area transmission loop that acts as a transmission antenna. By fitting the capacitors shown (actually on top of the ADC's output bus) a direct return path is made, creating differential flow, without disturbing the integrity of the mecca's operation with LF currents. The result was at least a ten times improvement in HF noise.

8 Finally—the future—cryogenics

The steering magnets at CERN and in many other accelerator projects are cryogenic. Much fundamental metrology is now based on quantum physics operating in liquid helium. Why not put some of the measurement in the cryogenic environment? Figure 18 is a suggestion and is currently being investigated at the UK's National Physical Laboratory.

Its operation is quite simple—the bias DAC is a PWM generator that turns ON and OFF precisely the bias to the Josephson Junction Array (JJ). The operation of the JJ locks the amplitude of the resulting pulse to a quantum level dependent only on fundamental constants and on the SI second. See Refs. [6] and [7].

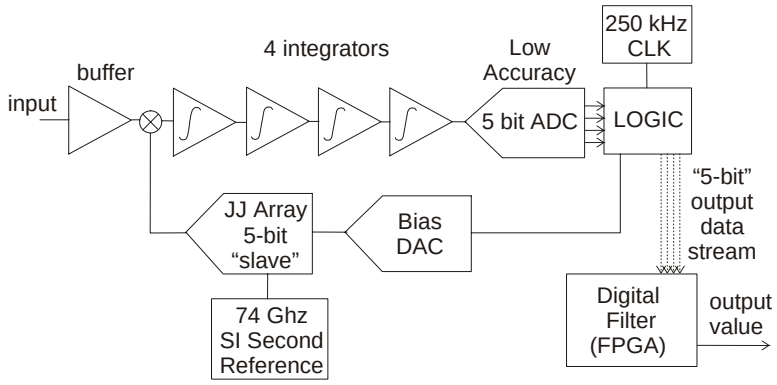

Fig. 18: A suggestion of cryogenic implementation for a high-performance Σ-Δ ADC

References and further reading

[1] http://webstore.ansi.org/ansidocstore/product.asp?sku=IEC+60748-4-2+Ed.+1.0+b%3A1993

[2] http://ieeexplore.ieee.org/xpl/tocresult.jsp?isNumber=20108

[3] http://paginas.fe.up.pt/~hsm/dynad/

[4] J.G. Pett, High accuracy 22 bit sigma-delta etc., adda conf., Glasgow, July 99 (IEE pub 466), p. 46.

[5] J. Candy and G. Temes, *Oversampling Delta-Sigma Converters* (IEEE Press, New York. 1992)

[6] P. Kleinschmidt, P. Patel, J.M. Williams, T.J.B.M. Janssen, R. Behr, J. Kohlmann, J. Niemeyer, J. Hassel and H. Seppa, 10th British Electromagnetic Conference, Harrogate, 2001, Conference Digest.

[7] C.A. Hamilton, C.J. Burroughs and R.L. Kautz, *IEEE Trans. Instrum. Meas.* **44** (1995) 223–225.

There is also much valuable material on many semiconductor manufacturers' web sites.