Four-quadrant power converter based on output linear stage

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Abstract
This paper deals with the design of a true four-quadrant power converter. This converter is intended to be used in the CERN Large Hadron Collider (LHC) project, which will use a huge number of true bipolar power converters. This paper will first describe the state of the art of this power converter family, pointing out drawbacks and advantages of different possible configurations. A specific review of the converter is then presented. Some key parts are detailed, and a practical realization is studied, giving the characteristics of the power converter which will be used in the LHC accelerator to feed 120 A superconducting magnets, ranging from 10 mH up to 4 H.

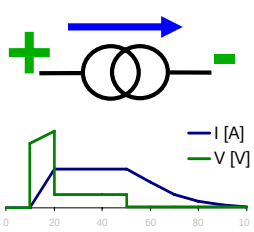
1 Introduction

A four-quadrant power converter design is strongly dependent on its use, considering several criteria reviewed in the first part of this document. Some well-known solutions are commonly used, and a short review and explanation of the principles involved is given as a first step. The second part of this document gives the key points of the design of a specific four-quadrant power converter designed to power superconducting magnets. In this document, the load will always be assimilated to a superconductive magnet, as it is a good and real four-quadrant power load. Since the system under study is highly non-linear and quite complex to simulate (up to three control loops working at the same time), the author lists key points instead of formulae, as this is easier to follow as a first approach to the problems to be solved during the design phase. This paper is mainly focused on low- or medium-output voltages (<100–200 V). For high-voltage converters, a different approach is required, since the availability of components (semiconductor or passive components) will have a strong impact on design choices.

2 Definitions

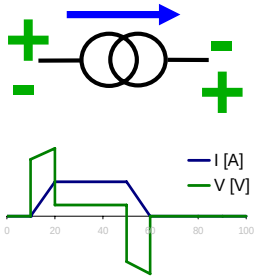
Some basic graphs are presented to summarize different types of power converters, feeding a typical four-quadrant power load: a resistance in series with an inductance (*R*-*L*). Through this load's example, limitations of different topologies can be demonstrated.

One-quadrant mode



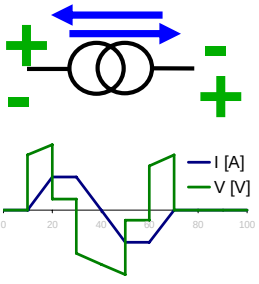
Control of the decreasing current is still possible within drastic conditions and limits ($R_{CIRCUIT}$ acts as discharger)

Two-quadrant mode



Current is controlled when increasing or decreasing, while remaining either positive or negative exclusively.

Four-quadrant mode



No theoretical operation limitation, since this converter is bipolar in current and voltage.

2.1 Conventions

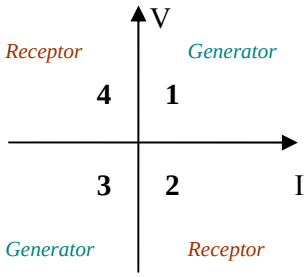


Fig. 1: Quadrant conventions

Figure 1 shows the conventions for quadrant definitions. Quadrants 2 and 4, when current and voltage are of opposite sign, represent receiving quadrants, where power has to be 'extracted' from the load.

2.2 Receptor mode solutions: a brief review

In the receiving quadrants (quadrants 2 and 4), the converter has to extract energy from the load, either by dissipating it or by sending it back to the mains. A four-quadrant power converter should regulate its output conditions while 'absorbing' energy. Basically, the three main possibilities are

– Local storage of energy:

  Even if some designs already include local storage of energy, super-capacitors or superconductive inductors will become a more and more attractive alternative, favouring this topology. This storage capability can be placed either on the primary side, or on the secondary side; the choice is made depending on the voltage used at the output and on the complexity of the final design.

– Sending it back to the mains:

  This design mainly uses thyristor-based topology, and is still massively used when high power is required. Simplicity of design and robustness of this well-known topology are other big advantages. Some high-frequency switching power converter designs have been presented as a valid alternative, even if control is then relatively complex.

– Dissipating it:

  This is surely the least appealing solution, especially when semiconductors are used to dissipate energy as pure heat losses. Nevertheless, this alternative solution can be integrated in modern topologies and presents good performance in the following fields: EMC, bandwidth. This approach can be justified according to the type of cycles the load will operate.

2.3 Influence of load cycle on converter topology

Different types of accelerators use different types of magnets for different purposes. There are basically two main types of use: pulsed or slow, as shown in Fig. 2. A pulse machine design should take into account energy saving aspects. With a high frequency charge and discharge sequence, a true four-quadrant power converter, giving back energy to the mains, or locally storing it for the next run, should be considered. On the other hand, a slow and ultra-high-precision machine (LHC type) will focus on different criteria like, for example, 0 V/0 A operation.

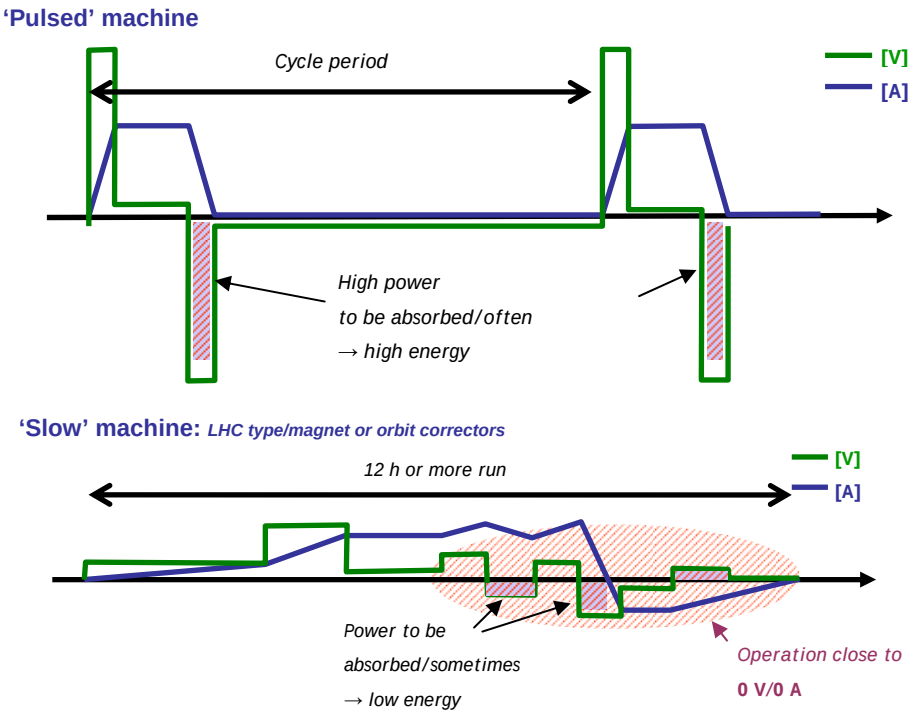


Fig. 2: Typical cycles depending on machine type

2.4 Load influence on design parameters

The LHC will require a very high magnetic field to control the beam, this field being directly proportional to the current reaching up to 600 A. The number of correctors, combined with these levels of current made the superconducting magnets a valid choice. These magnets are by definition lossless loads, since they are pure inductances, of up to several henry. To avoid adding extra losses in the tunnel, the power converter is connected to its load, the magnets, by thick cables. All these boundary conditions lead to very high time constant circuits (large inductance value combined with low resistance value), as:

$$\tau_{\mathrm{CIRCUIT}} = \frac{L_{\mathrm{MAGNET}}}{R_{\mathrm{CABLE}}} \tag{1}$$

with

– L_{MAGNET}: magnet inductance value [H],

– R_{CABLE}: cable resistance value [Ω].

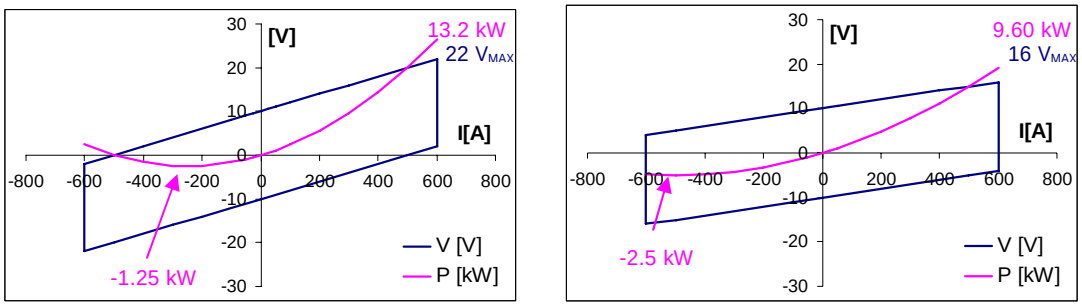
The value of this time constant, inherent from the type and physical characteristics of the circuit (magnet inductance and length and diameter of the cables), combined with the LHC required characteristics gives the range of the current and determines the type of power converters to be used within specific operating areas.

$$P(I) = U(I) \cdot I = R_{\mathrm{CABLE}} \cdot I^2 + L_{\mathrm{MAGNET}} \cdot \frac{\mathrm{d}(I)}{\mathrm{d}t} \cdot I \ . \tag{2}$$

Given an operating range (I_{MAX} and dI/dt) for a dedicated magnet (L_{MAGNET} fixed), a trade-off can be found between generating peak power and regenerating absorbed peak power, by modulating the cable resistance. Of course while increasing cable resistance will increase losses, it will

nevertheless decrease the power absorbed by the power converter. As will be shown later, increasing regenerating power for a four-quadrant converter is a lot more difficult than simply increasing its generating power.

While heat dissipation and heat losses generate costs of cooling and ventilation, increasing cable resistance will reduce the cost of the copper cables, and converter realization will be easier. Figure 3 shows a typical case of the same superconducting magnet used with two cables of different resistance.



(a) 20 mΩ cable (b) 10 mΩ cable

Fig. 3: Influence of circuit parameters on converter operation

In the case of a 20 mΩ cable, the power to be generated is 1.4 times higher while the power absorbed is down to one half. Of course the cable losses are double during magnet operation. Nevertheless, this configuration is really interesting in the case of corrector magnets, seldom at full current (less heat loss), to lower the power converter design constraints.

3 Four-quadrant stage: main topologies

A four-quadrant stage is the dedicated part of a power converter used to manage load voltage and current in the four-quadrant area. This function can be part of the converter topology (thyristor-based topology) or proposed like an extension of a standard generator power converter. This section deals with classical solutions, mainly used in the four-quadrant power converter domain.

3.1 Two thyristor bridges mounted anti parallel.

This standard configuration makes it possible to send energy back to the mains. It is based on two thyristor bridges mounted in anti parallel, using the intrinsic two-quadrant capability of each bridge. This configuration is very well-known and can handle high power constraints.

3.2 Linear dissipative stage

3.2.1 Presentation

A linear dissipative stage relies on a push–pull stage, with transistors used as ‘programmable resistors’ dissipating energy in receiving modes. This stage is usually an additional stage for a standard generator power converter used to provide power at the input of the linear stage.

An alternative configuration exists with polarity switches added to transform a single output into the required double outputs. This configuration, see Fig. 4, is much easier regarding power converter design but it leads to potential distortions when polarity switches operate. It also requires control of additional transistors, while a standard double-output voltage source can use simple

additional rectifiers (an *L-C* filter can be shared between the two outputs, reducing the number of additional components and the cost).

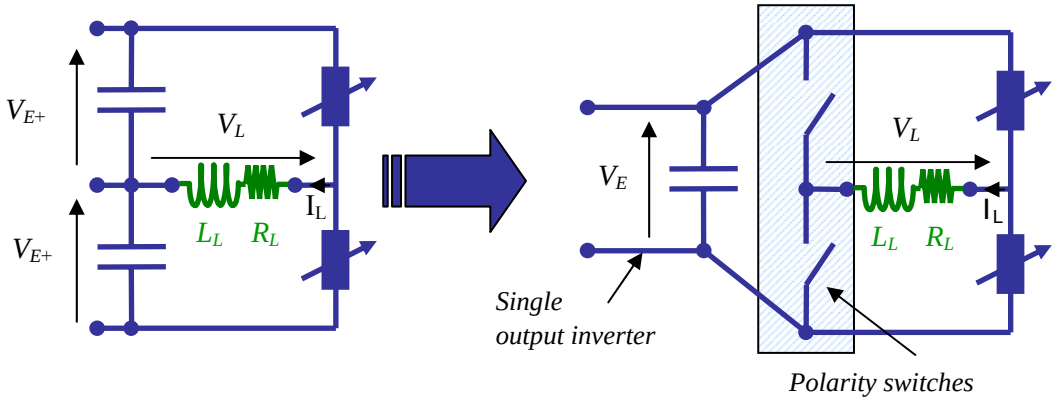


Fig. 4: Linear stage schematic

3.2.2 Operating principle

A dual-output power source is used to power the linear stage, with the usual limitation of the two dual outputs tied together. (Standard configurations are usually based on a dual-output power converter using one inverter stage powering a dual-output transformer.) Two different configurations are possible, with fixed value or variable dual output.

3.2.2.1 DC fixed dual-output configuration

Figure 5 shows voltage and current waveforms on a typical magnet application, highlighting the limitations and the dissipation problem to be dealt with. In the example shown below, a ±10 V ±120 A converter is shown. Since losses in transistors are assumed to be 2 V at the highest current level, a minimum dual voltage of 12 V is required to feed the output linear stage.

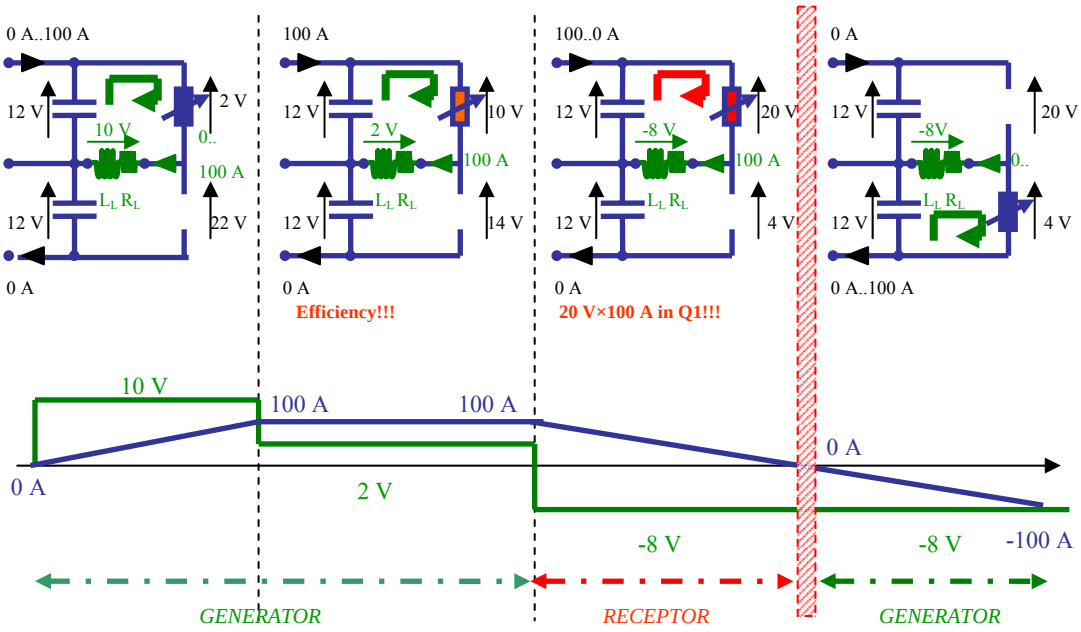


Fig. 5: Four-quadrant linear stage (fixed dc dual voltage)

A dual-output 50 Hz transformer with the adequate rectifying and filtering stage can simply provide the two desired fixed dc sources, schematically represented by capacitors; a modern design would potentially propose a switch-mode power supply, for example, for size reduction. Both voltage sources have to provide a voltage sufficient to compensate the losses generated by the voltage drop across the active switch at maximum current.

While this configuration is very simple, an efficiency problem exists requiring losses to be managed at the transistor level, especially at low-voltage and high-current conditions where the transistor has to dissipate a large part of the energy supplied by the power source. This is particularly true for superconducting magnet power supply, since a high voltage is necessary to raise the current to its maximum losses, while a steady state requires a very low voltage induced by the dc cable losses. A second source of losses is the regenerating phase, where the active transistor has to handle twice the power normally required by the load.

3.2.2.2 Variable dc dual-output configuration

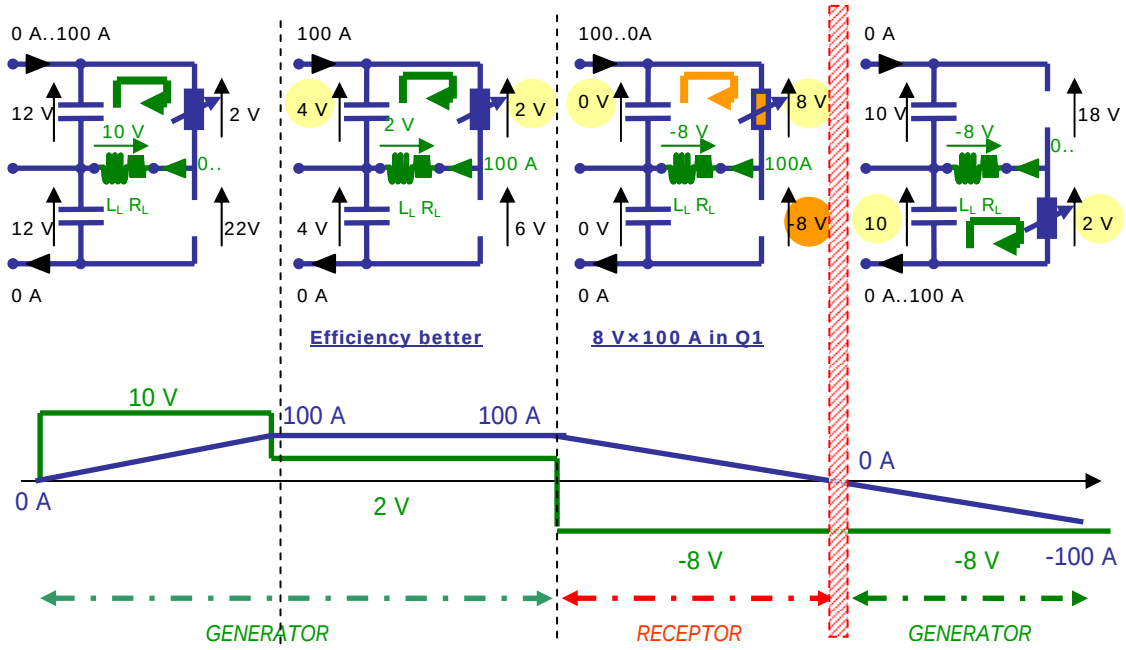


Fig. 6: Four-quadrant linear stage (variable dc dual voltage)

The configuration shown in Fig. 6 is much more efficient; power from the supply mains load one, plus the active transistor conduction losses. Nevertheless, power dissipated in the transistor in dissipative mode is always equal to the load. This can be solved by controlling the dual output sources to be generating only in selected operation quadrants. In that configuration, control complexity grows, as output current sensors are needed to determine the operating quadrant.

On the two schemata proposed, the 0 A zone is always considered to be critical, since a linear stage 'relies' on current going through the relevant transistor to create voltage reference. This state is particularly critical when a 0 A point has to be crossed while voltage has to be present on an inductive load, which is typically the case for a superconducting magnet.

A linear stage should not to be working in saturated mode—even if close to this mode—to ensure output voltage is still regulated; a deeper analysis will show the benefit of using an unsaturated linear stage to provide extra rejection of mains perturbation. This option has an efficiency cost since the active transistor conduction losses will be higher.

3.3 Switching stage

3.3.1 Presentation

A conventional H-bridge stage (*L-C* filter added to filter the switching ripple at the output level) can deal with energy absorbed or generated by the load. Energy has to be managed at the input of the H-bridge level, stored in the capacitor, or discharged by an additional brake hopper.

3.3.2 Operating principle

An H-bridge (see Fig. 7), is a natural four-quadrant power stage, which makes a good candidate for four-quadrant power converter combined with a single voltage power source, providing voltage adaptation and insulation from the mains. This power source can be either a 50 Hz transformer or a modern switch-mode-based solution. This topology is very simple to control, since the duty cycle directly controls the output voltage, without any transition mode problem. Concerns come from important losses due to the hard switching stage dealing directly with the output current and EMC at the output level resulting from the proximity to switching cells. Some converters use a two-operation mode control, transforming the H-bridge into a classical buck converter to reduce losses and current ripple (a leg is inactive, with a switch closed).

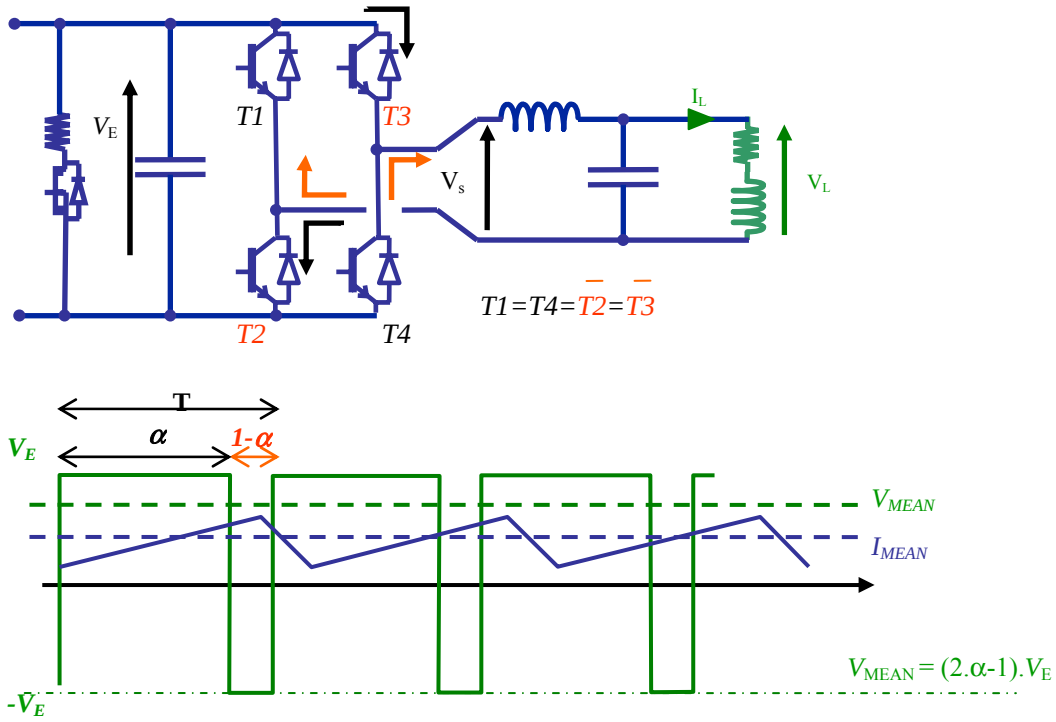


Fig. 7: Four-quadrant switching stage

4 Review of different topologies

Figure 8 gives an overview of different possible combinations for a four-quadrant power converter. All ‘rectifier bridge’ paths indicate a topology where energy cannot be returned to the mains.

The second part of this paper will describe the design and realization of a power converter using a linear stage (indicated in bold on Fig. 8).

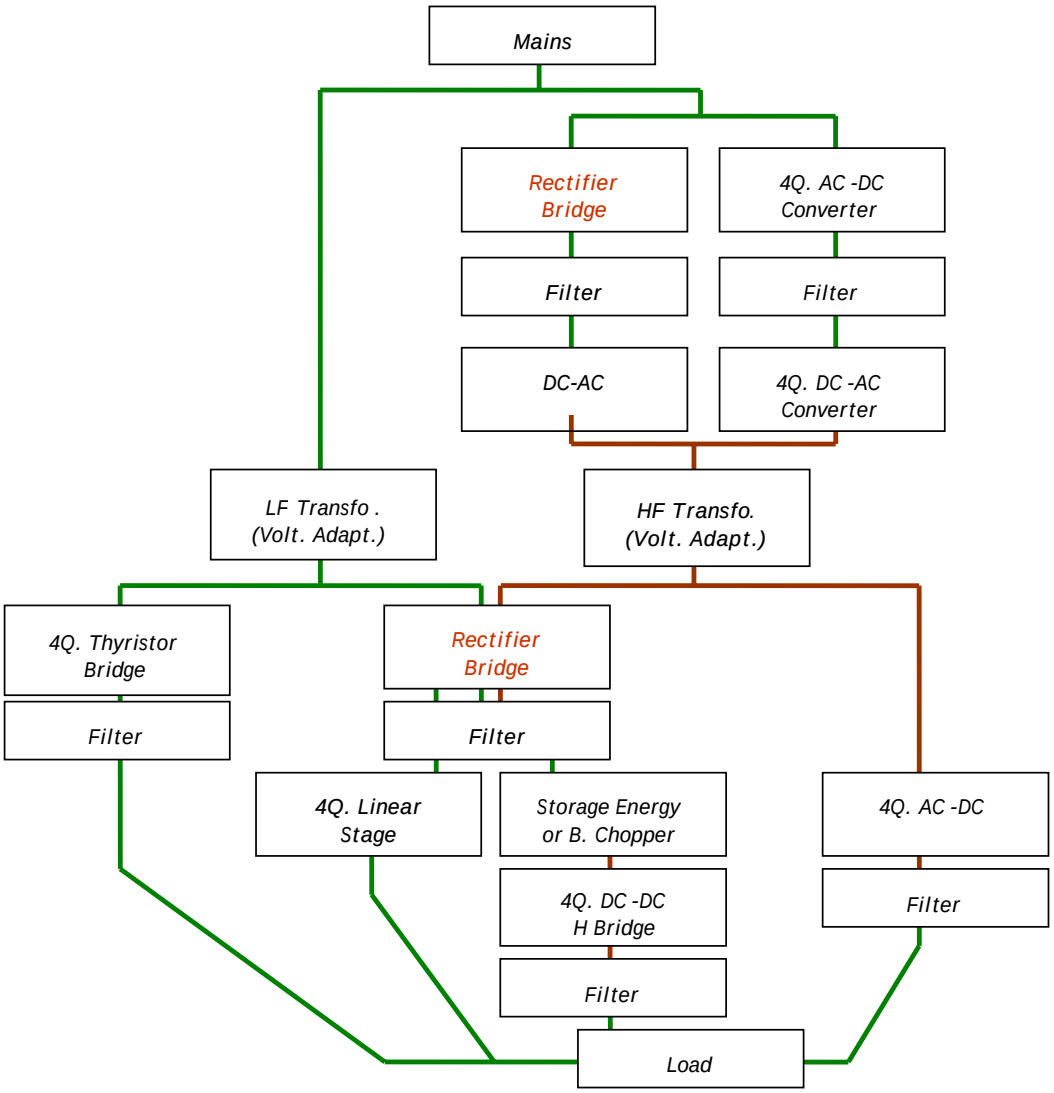


Fig. 8: Overview of possible combinations

5 LHC 120 A power converter design

We describe a practical realization of a ±120 A ±10 V four-quadrant power converter designed at CERN for LHC use.

5.1 Presentation

This converter was designed to be integrated in a high performance environment: its main use is to provide a current precise to some ppm (part per million) to a superconducting magnet. A low level of the EMC perturbations due to the power converter, at the input or output side, and a close respect of the reference voltage to be followed (no distortion, high bandwidth) are high requirements for the precision electronics located in the power rack. The converter integration in the existing tunnel is a constraint which makes the switching base the only adequate topology. High efficiency minimizes the losses to be evacuated from underground installations and the low size and weight are required for installation and maintenance around the 27 km of the LHC tunnel. Durability is also required for a system which is expected to operate for more than 10–15 years.

5.2 Schematic overview

The converter is based on a switching + linear stage topology and can be basically represented as follows.

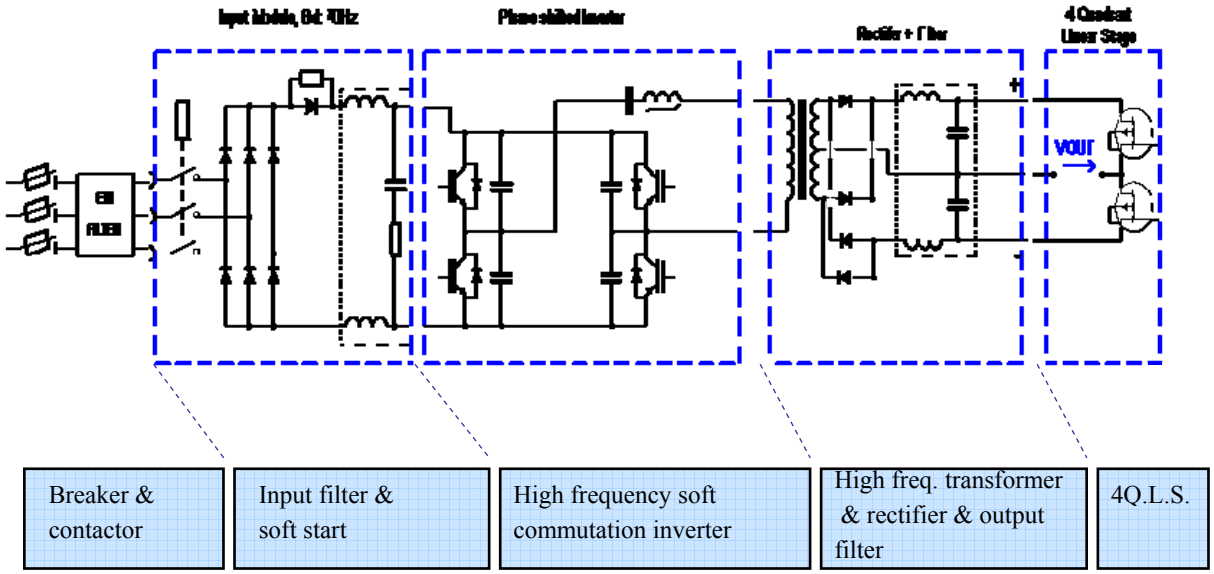


Fig. 9: LHC 120 A–10 V schematic overview

Figure 9 shows the five power converter parts:

1. Protection and power control stage: A breaker and ac contactor powers and protects/isolates the power converter.
2. ac–dc stage: a conventional rectifier bridge and input filter (70 Hz) with soft-start capability provides dc voltage to the next stage.
3. High-frequency dc–ac inverter: a 70 Hz phase-shifted ZVS inverter IGBT-based switches dc voltage for a high-frequency transformer to adapt and isolate for the output side.
4. Isolation and rectifier stage: a high-frequency dual-output power transformer and low-voltage Schottky diodes power the output high-frequency dual dc voltage to the four-quadrant linear stage.
5. Four-quadrant linear stage: based on MOSFET power transistors (mounted in parallel on each side to boost power capability), capable of absorbing and dissipating full load energy, while regulating the operating quadrant, with additional functions: minimum load of previous stage, active filter.

5.3 Four-quadrant linear stage

The main element of this power converter is the four-quadrant linear stage. The choice of MOSFET for this stage leads to a specific design, to handle the inherent limitations of this kind of component (threshold, non-linear component).

5.3.1 Principle

Figure 10 shows different working cases, as a first approach to the system regulation.

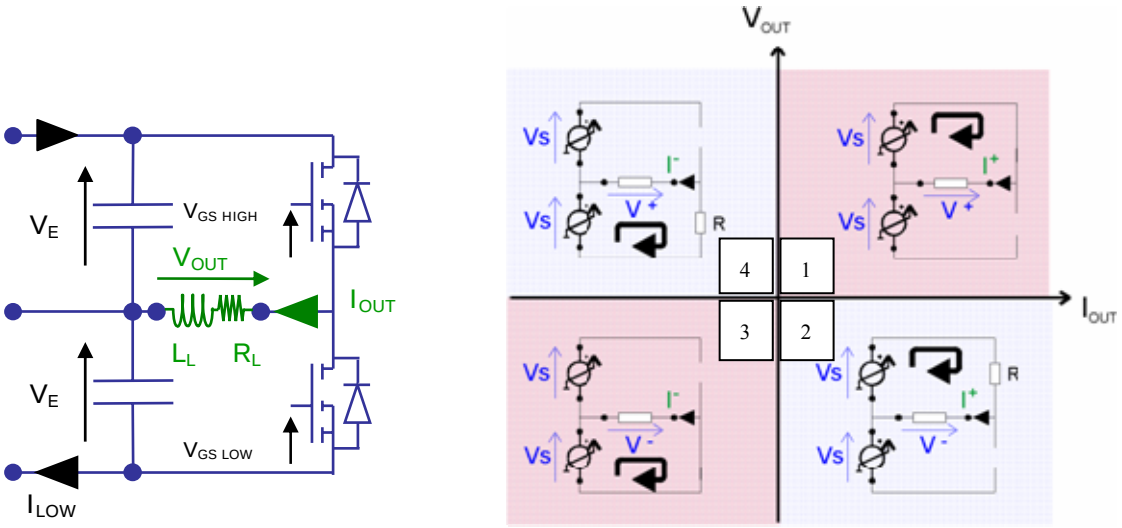


Fig. 10: Four QLS schematics

Control principles can be simplified to two equations (3) and (4), valid each one for two quadrants:

$$V_{\mathrm{OUT}} = +\left(V_{\mathrm{E}} - R_{\mathrm{HIGH}} \cdot I_{\mathrm{HIGH}}\right) \quad \textit{Quadrant 1\&2} \tag{3}$$

$$V_{\mathrm{OUT}} = -\left(V_{\mathrm{E}} - R_{\mathrm{LOW}} \cdot I_{\mathrm{LOW}}\right) \quad \textit{Quadrant 3\&4}\,, \tag{4}$$

with R_{HIGH} and R_{LOW} equivalent MOSFET resistances.

5.3.2 MOSFET characteristics

5.3.2.1 Power MOSFET: a natural current source

A MOSFET is a natural current source, since a gate voltage determines the current flowing into it, independently from the voltage applied to it. This can be easily seen from the manufacturer's data on Fig. 11, where a specific gate voltage leads to a constant current plotted versus the drain-to-source voltage V_{DS}.

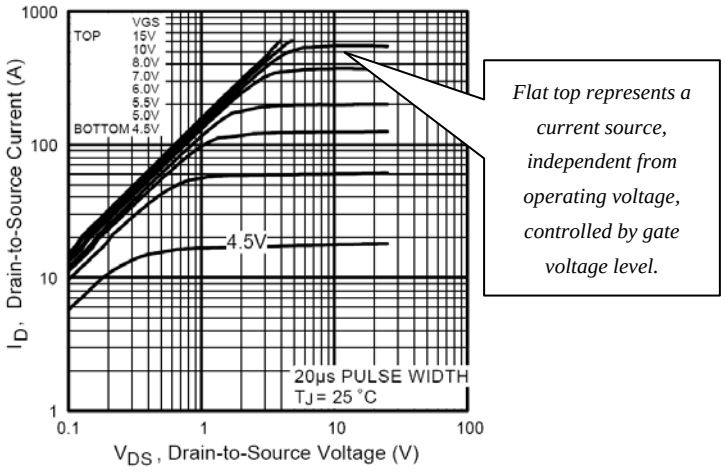


Fig. 11: Typical MOSFET characteristics

A possible complication could result from the nature of the load: a superconducting magnet (current source per excellence) requires an output decoupling filter to be able to connect source and load. However, the values of the load time-constant involved in this realization were in such a wide range that this option was not kept. A complete linear stage was nevertheless built and successfully tested.

5.3.2.2 MOSFET transistor: also a 'controlled resistance'

A MOSFET transistor used as a 'controlled resistance' is a highly non-linear system. The curves of Fig. 12 summarize the main phenomena to be taken into account: the influence of temperature, V_{DS} voltage, Miller capacitance. Of course the internal MOSFET structure should be taken into account, especially with modern MOSFETs, better at switching than at working in linear mode.

– *Main parameters to be taken into account*

Some key parameters are highlighted, always focusing on the gain G:

$$G = \frac{R_{DSON}}{V_{GS}} \tag{5}$$

– *Gain variation over working range*

A classical R_{DSON} versus V_{GS} curve shows several orders of magnitude in static gain to be considered, when a linear model is used around an operating point. If a linear control system is chosen, the working range of the MOSFET should be selected to minimize gain variations. Figure 12 shows the typical curve of a standard power MOSFET.

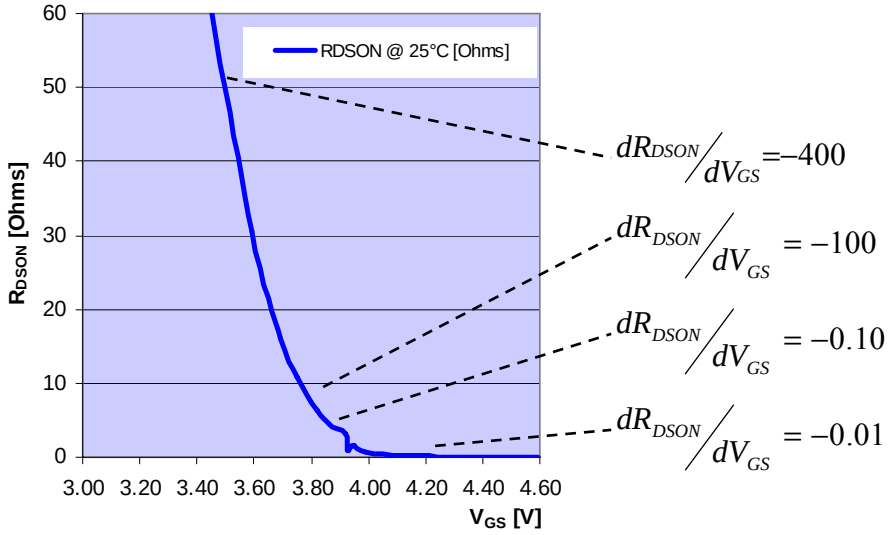


Fig. 12: MOSFET R_{DSON} overview

– *Threshold variations over a batch*

The conduction threshold is a key parameter since a transistor linear stage cannot expect a step voltage control signal from the linear control main loop. This threshold variation has to be known. This parameter can vary from 2.00 V to 4.00 V, a really large range. This means that a fixed threshold to approach linear conductive mode is impossible and cannot be considered for a safe and robust design.

– *Threshold variations due to radiation*

The variation of threshold gate voltage versus radiation dose is a key factor for some converters used in particle accelerators. Figure 13 plots power MOSFET (1000 V 15 A) threshold variation versus radiation dose, this particular power MOSFET being used to control a constant low current (50 mA) in the test configuration.

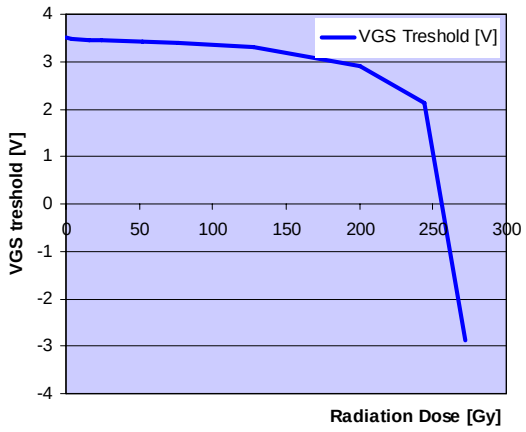


Fig. 13: MOSFET V_{GS} threshold variation vs. radiation dose

– *Influence of temperature*

The influence of temperature on a MOSFET transistor is well known, with $R_{DSON\ SATURATED}$ increasing with temperature. When controlling a MOSFET transistor in linear mode, increasing temperature introduces a negative threshold 'offset' as shown in Fig. 14.

This feature is important since it precludes using a fixed threshold, *even* if each MOSFET threshold level is trimmed.

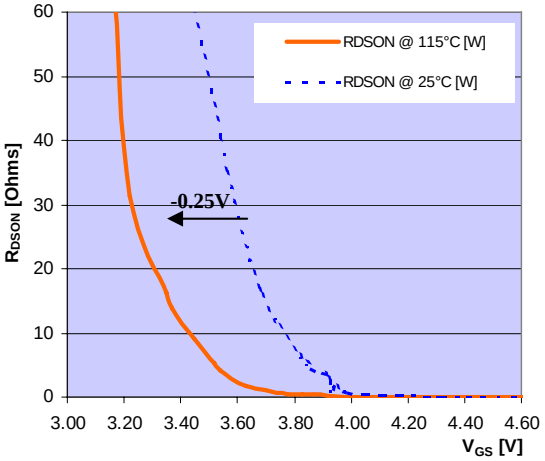


Fig. 14: MOSFET R_{DSON} vs. temperature

– V_{DS} *influence*

The gain is highly influenced by the voltage across the V_{DS} MOSFET. See the curve below in Fig. 15. This curve has to be used to determine the minimum operational value of V_{DS}. Indeed, in a classical linear stage, we shall see that while the maximum voltage is determined by the load operating area, the

minimum value across the MOSFET can be selected based on efficiency and control criteria. Choosing a low operation voltage across the MOSFET will lead to square angle characteristics with a high rate of change difficult to control.

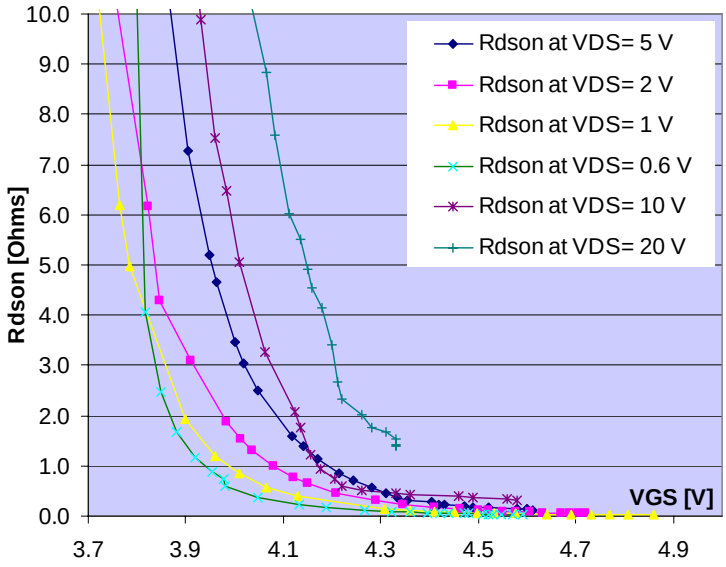


Fig. 15: MOSFET R_{DSON} vs. V_{DS}

– *Miller capacitance effect*

The signal applied to the gate voltage is loaded by a capacitance whose value changes with the MOSFET conduction status. This change could affect the bandwidth of the control signal if a high resistance value is placed in series with the gate. Total gate capacitance is the sum of the gate capacitance itself added to the output capacitance which depends on the MOSFET status: if the MOSFET is conducting, and close to its minimum R_{DSON}, the operation gate capacitance seen from the gate drive can be multiplied by a factor of up to 2–3. In linear mode, this capacitance can easily be derived from manufacturer's data:

$$Q_g = C_{iss} \cdot (V_{GS\ Final} - 0) + C_{iss\ Miller\ add} \cdot (V_{GS\ Final} - V_{GS\ Threshold}) \tag{6}$$

with

– Q_g total gate charge under

– C_{iss} grid capacitance under

– $V_{GS\ Threshold}$ MOSFET conduction threshold

– $C_{iss\ Miller\ add}$ 'Miller capacitance'

The capacitance range can be found from this equation:

$$V_{GS} \leq V_{GS\ Threshold} \rightarrow C_{iss} \tag{7}$$

$$V_{GS} \geq V_{GS\ Threshold} \rightarrow C_{iss} + C_{iss\ Miller\ add} \cdot \tag{8}$$

5.3.2.3 MOSFET model conclusions

Controlling a MOSFET like a 'variable resistance' presents two major problems when using a linear system: a conduction threshold, and a high difference of 'static' gain depending on the desired resistor value.

5.3.3 MOSFET push–pull control

A linear loop control is used to drive the MOSFET push–pull, by sending opposite signals to the gate voltage of the MOSFET transistor branches. In that configuration, the control loop has to provide a threshold voltage added to the small control signal given once the MOSFET reaches the linear zone. It should be noted that when switching from upper to lower leg, the control signal has to be in the form of a step of twice the gate voltage threshold.

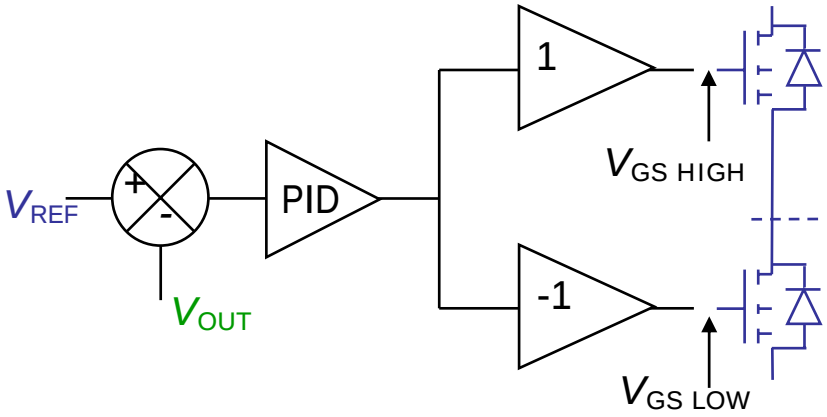


Fig. 16: Push–pull control principle

Even for a highly non-linear behaviour due to MOSFET $R_{DSON,}$ this principle works quite well taking into account that a high level of R_{DSON} is used with low current, while a high level of current requires a low value for R_{DSON}. Indeed, as seen in Fig. 17, signal analysis shows it is possible to choose the working voltage across the MOSFET (design choice) so that these two behaviours compensate each other, thus giving an acceptable gain variation.

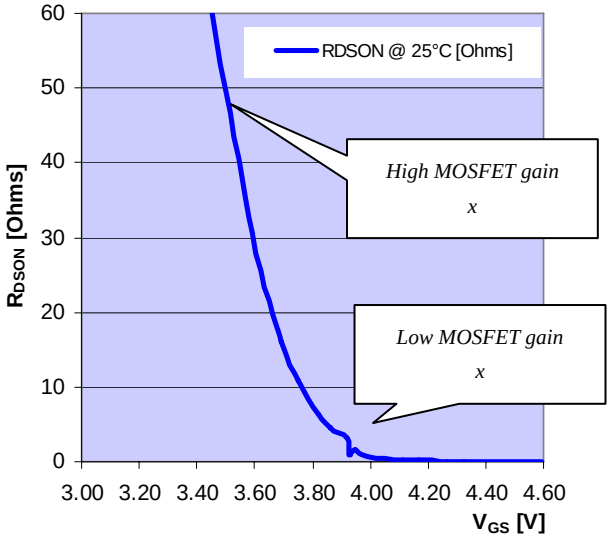


Fig. 17: Detail of small signal analysis

5.3.4 Inherent limitation of a push–pull stage

Even if very simple, a basic push–pull system has an uncontrollable zone at zero current, since voltage cannot be 'obtained' if the current in the load is null. This problem is worsened with a superconductive load, where full voltage can be applied with null current. Likewise, the 0 V 0 A point is an unstable point. In the case of a MOSFET stage, two severe limitations appear:

– The gate voltage threshold makes it difficult to use a simple linear system (the control signal given by the loop has to switch between $+V_{\text{GS threshold HIGH}}$ and $-V_{\text{GS threshold LOW}}$ as fast as possible to avoid uncontrolled output (in the blank area, where no MOSFET conducts). Figure 18 shows the step voltage required from the voltage control loop, reaching 8 V in that example (twice 4 V from each MOSFET threshold level).

– The range of MOSFET use can be very wide, from an almost saturated to an almost open state, giving a four orders of magnitude gain variation, very difficult to control in a simple way, even with the self-compensating effect of the current versus R_{DSON} values.

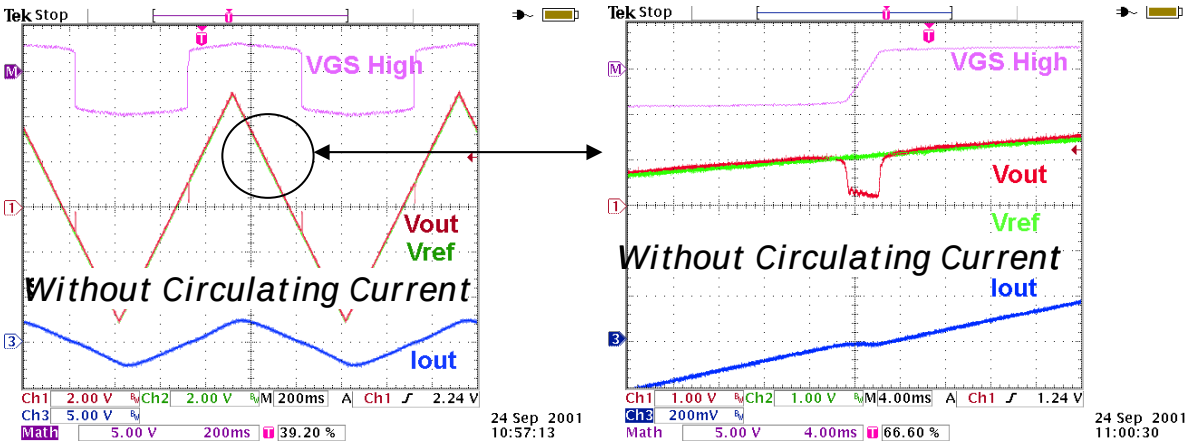


Fig. 18: MOSFET based push–pull stage limitation

5.3.5 Circulating current

A circulating current is a controlled current, internal to the converter—not seen by the load—which maintains in a known state both the dc–dc power converter and the four-quadrant linear stage. This feature is needed to obtain a high level of performance. It provides the following functions:

– Insuring a minimum load of the dc–dc power converter and avoiding a completely non-loaded output side of the dual output dc–dc power converter. The power dc–dc switch mode converter is therefore easily controllable, without the problem of managing continuous and discontinuous modes, and with a clamping voltage on the output capacitors of each side, for all output conditions.

– Pre-conditioning the linear stage power MOSFET close to the threshold gate voltage. The linear stage loop will be able to manage high-side and low-side transitions since neither side of the MOSFETs requires a voltage step to change mode (conductive or not).

– Limiting the working zone of the power MOSFET when used in linear mode:
It is possible to artificially redefine the range of operation of both side MOSFETs in linear mode by just playing with the value of the circulating current and of the operating voltage. This important feature is described in Section 5.3.5.1.

– Less important but very convenient, if a sharing procedure has to be used, is the capability of circulating a current inside the power converter when trimming the MOSFET, in case of use of MOSFET in parallel per side. A power converter can be trimmed without any external load, with the level of current being adjusted to optimize this possible procedure.

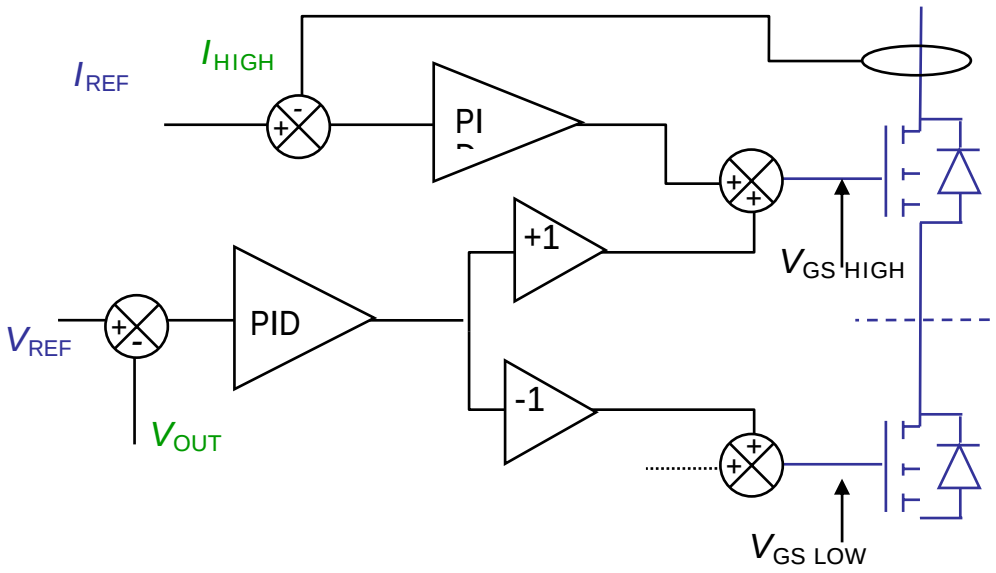


Fig. 19: Push–pull control principle with circulating current loop

Figure 19 is a simplified view of the two loops involved in that mode. Addition of this circulating current loop provides real advantages and gives a possibility to dynamically trim the system very deeply (in case the value of the circulating current is controlled by an adjustable limit on the output current). It is nevertheless an additional loop, which should not disturb the two loops already in place: MOSFET push–pull and power dc–dc control. The bandwidth of this loop must be carefully chosen, as the high signal dynamic performance of the overall power converter partly depends on this loop's characteristics.

5.3.5.1 Influence of the circulating current on the operational range

The circulating current can be used to drastically reduce the highly non-linear zone to a more convenient one by limiting the high gain zone. This is quite interesting since it does not cost too much in efficiency and touches the less controllable and unstable linear zone of the MOSFET (high resistance, high gain). It is especially critical to avoid this problem with a superconductive load, where the power converter maximum output voltage can be applied in a receiving quadrant while the current, even if slightly varying, is very low. Indeed if the linear stage provided full voltage at a current close to zero, the MOSFET would be used at a high resistance value, inducing a very high gain, and thus would be in a critical zone for linear loop stability. The circulating current strategy ensures a minimum current flow in each MOSFET, allowing then to produce the desired output voltage with medium values of R_{DSON}, without relying on output current only. Figure 20 shows a drastic reduction of the R_{DSON} range, using only 1 A of circulating current.

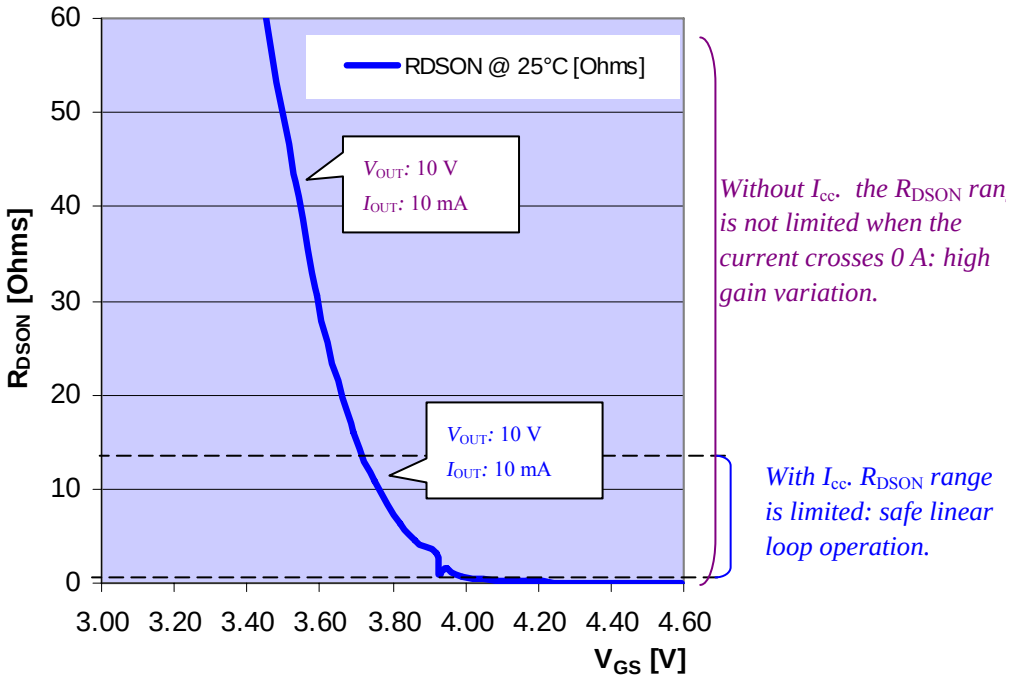


Fig. 20: Detail of small signal analysis

5.3.5.2 Circulating current implementation

Implementing this feature requires the addition of one current transducer per side. (Note that these two sensors can be used to measure the output current of the load, as is often required for load protection.) In such a case, it can be noted that:

- knowing output current will permit adjusting the circulating current level to improve overall efficiency;
- while these sensors' precision can be low (a few per cent), they should possess a sufficiently high bandwidth so that they do not interfere too much with the inner loop;
- it is possible to use shunts in series with each MOSFET to provide a self-damping behaviour if the gate voltage is applied to the MOSFET gate + shunt.

It is mandatory to use a reading range higher than the current produced by the power converter, since each sensor will alternately—depending on current polarity—see output current + circulating current at maximum output current if non null at this level. It is nevertheless possible to use circulating current only around the 0 A area, making it possible to use a low current sensor. This cost-effective solution will limit the potential benefit of a circulating current loop addition.

5.3.5.3 Circulating current results

Figure 21 shows the result of circulating current on gate voltage, the latter remaining constantly close to the threshold voltage of each MOSFET.

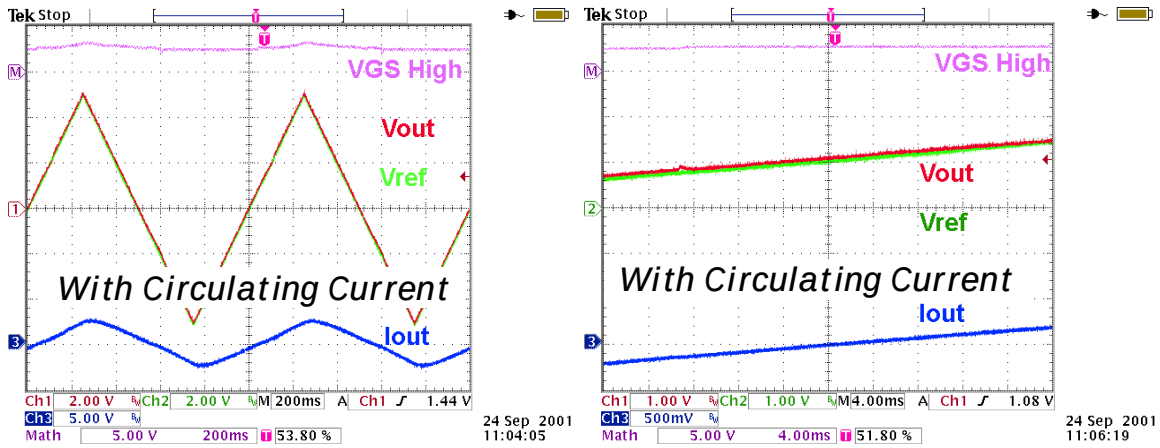


Fig. 21: Circulating current improvement effect

5.3.5.4 *Circulating current possible operation*

The circulation current generates losses, especially when the output conditions are far away from 0 A. The worst case is at full output voltage, where the circulating current causes the highest energy losses in the power transistor. Considering this circulating current is only useful close to 0 A output current, different strategies can exist to avoid extra losses with I_{LIMIT} close to 0 A output current.

1. $I_{OUT} < I_{LIMIT}$ $I_{CC} \rightarrow ON_{high\ value}$ Operating close to 0 output current is possible
   $I_{OUT} > I_{LIMIT}$ $I_{CC} \rightarrow OFF$ Output current far from 0 A: no circ. current needed

2. $I_{OUT} < I_{LIMIT}$ $I_{CC} \rightarrow ON_{high\ value}$ Operating close to 0 output current is possible
   $I_{OUT} > I_{LIMIT}$ $I_{CC} \rightarrow ON_{low\ value}$ I_{CC} present for loading inactive side.

The I_{CC} low value is set so that the high-frequency dual output voltage dc–dc is sufficiently loaded on the non-leading side to avoid over voltage. It can be noticed that a very low level of I_{CC} is sufficient to polarize both MOSFETs, thus avoiding too long a delay before entering the safe 0 A crossing zone.

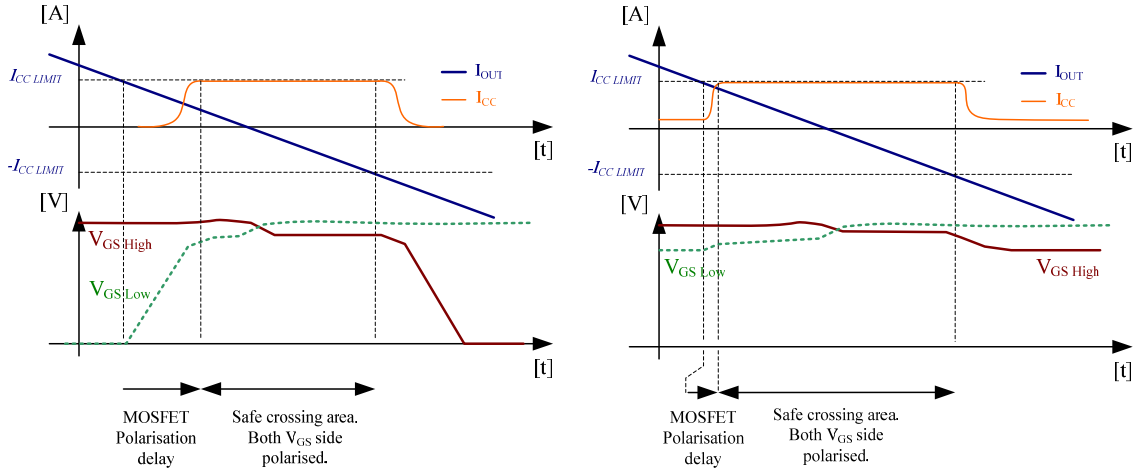


Fig. 22: Non-null circulating current

Figure 22 shows the beneficial effect of a non-null circulating current on the ability to deal with a high current change rate. If the two operating cases seem almost equal for operating close to 0 A

output current, the result is nevertheless different when taking into account the speed of the circulating current loop. Indeed, this additional loop is lower than the main controlling loop and the stabilization time can become critical if d*I*/d*t* is too fast. In this case, the second solution is a lot better. This is particularly interesting when the converter has to work on a pure resistive load, where d*I*/d*t* is not limited by the load.

5.3.5.5 Influence of the number of MOSFETs on linear loops

The minimum number of MOSFETs to be used is determined by the power—energy—to be absorbed by the linear stage.

It is obviously possible to use a large number of MOSFETs so that the V_{BIAS}—V_{DS} voltage across the MOSFETs in generator mode—value can be decreased, still keeping a reasonably controllable area for MOSFETs when used at high current in generator mode. Reducing V_{BIAS} makes it possible to increase efficiency, at the price of additional MOSFETs. Nevertheless, this improvement is balanced by the fact that MOSFETs will work in a higher gain area, due to R_{DSON} characteristics, when absorbing energy from the load, leading to a potential instability. While this design feature can easily be taken into account, increasing the power of an existing converter means not only increasing the number of output power MOSFETs: the control loops have to be re-worked to ensure proper operation.

5.4 Converter control loops

Since a four-quadrant linear stage is fed by the power dc–dc (inverter + dual output filter), a control strategy for power dc–dc, four-quadrant linear stage and circulation current loops has to be decided. Since cascaded loops are involved, power dc–dc and four-quadrant linear stage loop speeds differ by a factor of ten. The four-quadrant linear stage is the fastest loop, since generating and absorbing mode both use the four-quadrant linear stage, but not the generating one. Indeed, the four-quadrant linear stage is fed by the load in quadrants 2 and 4, and power dc–dc can be transparent in that mode. This control strategy is depicted in Fig. 23.

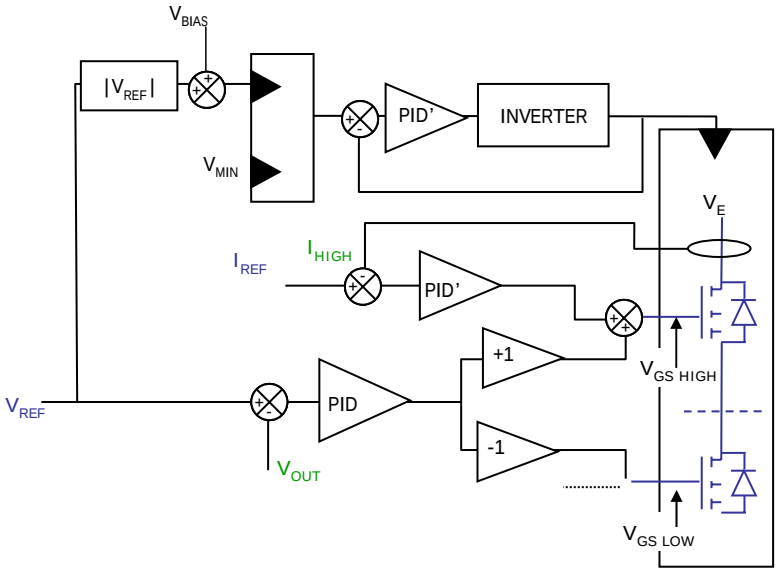


Fig. 23: Overall control strategy

The circulation current loop is always the slower one, since the polarization of the MOSFET should appear completely transparent from the other loops. The current rate can impart a minimum speed to this loop to achieve undistorted crossings.

5.4.1 Power dc–dc loop

This loop is at least ten times slower than the four-quadrant linear stage. The voltage reference coming from the converter used was chosen to be the same bandwidth as the power dc–dc, to keep the four-quadrant linear stage from being faster than that of the power dc–dc which would lead to conflicts. Two settings are used in this case to trim the power dc–dc reference: V_{BIAS} and V_{MIN}. The first one is used so that the four-quadrant linear stage can work in a given, not too saturated, operating range, as described in previous sections. The second one keeps the circulating current in the power dc–dc and the output voltage reference at a minimum level, thus resulting in minimum power. It also makes the loops more robust close to the 0 A, 0 V point, limiting the operating zone where all three loops are active at the same time. See Fig. 24.

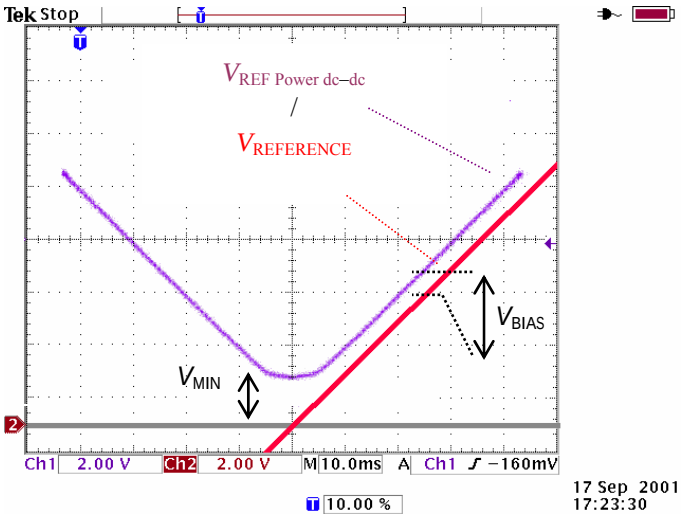


Fig. 24: Typical power dc–dc reference versus converter reference

6 Practical results

The converter was manufactured by the Portuguese company EFACEC, also in charge of the rack design and of the industrialization of the proposed solutions, according to the CERN design. The converter module, including interlocks and signal capabilities is housed in a 5 U 19” 45 kg power module, as shown in Fig. 25.

Fig. 25: LHC 120 A 10 V power module

The power converter operating characteristics demonstrated the initial choice of topology. The system is robust, with a bandwidth of 1 kHz, without any distortion of the voltage while crossing the 0 A point, and a very low EMC level. The different trimming possibilities (V_{BIAS}, V_{MIN}, circulation current levels (low and high) and its current limit when changing level), and the cascade type design made adjustments easy, since the system is not too interleaved. The measured efficiency is relatively low (72% at full power), due to linear stage losses.

Figure 26 show a typical 0 A crossing plot, without any distortion, on a superconducting magnet (0.6 H).

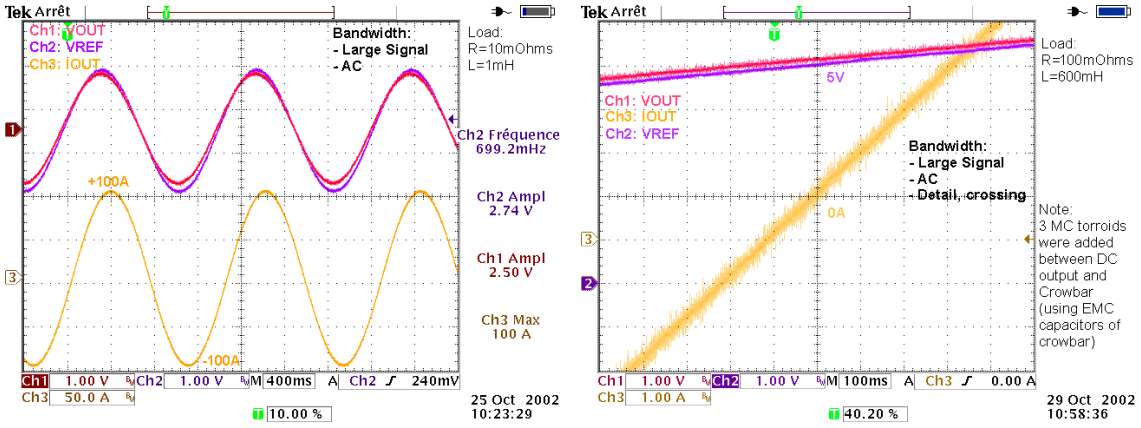


Fig. 26: Crossing 0 A

Moreover, the bandwidth of the system is constant whatever the quadrant used, ensuring a safe operation on a superconducting magnet at a very high precision level (some ppm) of the current loop, which will be maintained at all load operating conditions. Figure 27 shows a typical plot of a generator and receptor bandwidth. A voltage step is required, with a small signal added, so that the converter operates in generator, then receptor mode. The current does not change at this time-scale, since the superconducting magnet keeps it stable (large time constant).

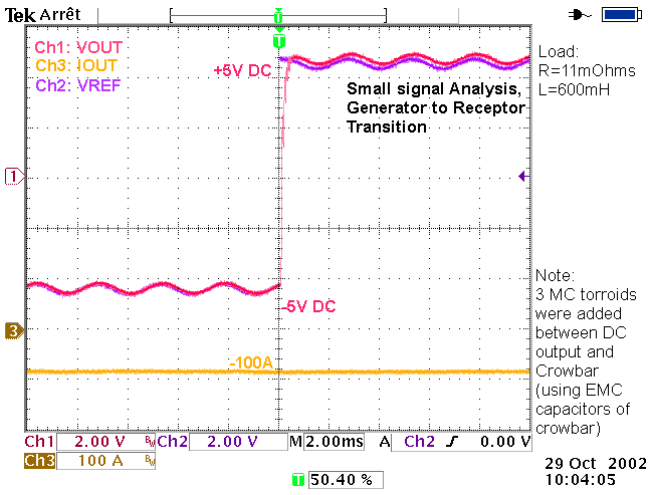


Fig. 27: Small signal analysis in receptor quadrant

EMC levels were measured on the ac side (input) and the dc side (user side, superconducting magnets in series over hundreds of metres). If the ac level is low, according to the IEC regulation standards, the dc side was found extremely low, especially in the high-frequency range. This result is

mainly due to the soft commutation inverter, added by the one switching stage only topology. This choice made it possible to deal easily with parasitic components (limiting common and differential mode capacitors of transformers and secondary side rectifiers) by using the output filter as an additional EMC component. The linear stage is obviously a 'quiet' element which does not influence the EMC of the converter, as opposed to a second switching stage. See Fig. 28 for a typical plot at maximum current and voltage.

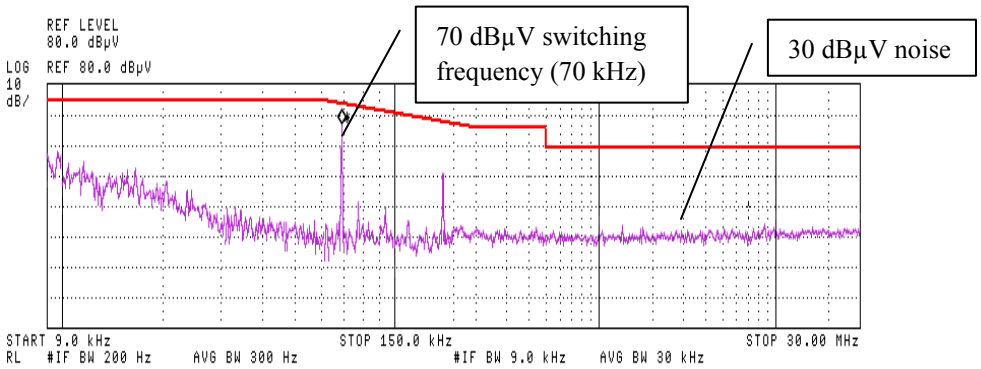


Fig. 28: EMC curve of dc output side (1500 Ω probe)

7 Conclusion

This paper briefly describes four-quadrant power converter topologies. Key technical points of a CERN internal design were presented, together with practical results obtained on series converters built for the LHC accelerator. The paramount requirement for an undisturbed operating zone (especially around 0 A 0 V) was met thanks mainly to the circulating current loop, which avoids dead zones and optimizes MOSFET control. While it was relatively easy to obtain a working converter (a simple assembly of parts), going further required a deep understanding of output linear stages, and of MOSFET gain variations, as described in this paper.

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