ATLAS SCT End-Cap Module Production

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Abstract.

The challenges for the tracking detector systems at the LHC are unprecedented in terms of the number of channels, the required read-out speed and the expected radiation levels. The ATLAS Semiconductor Tracker (SCT) end-caps have a total of about 3 million electronics channels each reading out every 25 ns into its own on-chip 3.3 μs buffer. The highest anticipated dose after 10 years operation is 1.4×10^{14} cm^{-2} in units of 1 MeV neutron equivalent (assuming the damage factors scale with the non-ionising energy loss). The forward tracker has 1976 double-sided modules, mostly of area ≈ 70 cm^2, each having 2×768 strips read out by 6 ASICs per side. The requirement to achieve an average perpendicular radiation length of 1.5% X_0, while coping with up to 7 W dissipation per module (after irradiation), leads to stringent constraints on the thermal design. The additional requirement of 1500 e$^-$ equivalent noise charge (ENC) rising to only 1800 e$^-$ ENC after irradiation, provides stringent design constraints on both high-density Cu/Polyimide flex read-out circuit and the ABCD3TA read-out ASICs. Finally, the accuracy of module assembly must not compromise the 16 μm (r-φ) resolution perpendicular to the strip directions or 580 μm radial resolution coming from the 40 mrad front-back stereo angle.

2196 modules were built to the tight tolerances and specifications required for the SCT. This was 220 more than the 1976 required and represents a yield of 93%. The component flow was at times tight, but the module production rate of 40 to 50 per week was maintained despite this. The distributed production was not found to be a major logistical problem and it allowed additional flexibility to take advantage of where the effort was available, including any spare capacity, for building the end-cap modules. The collaboration that produced the ATLAS SCT end-cap modules kept in close contact at all times so that the effects of shortages or stoppages at different sites could be rapidly resolved.

1. Introduction.

The ATLAS experiment [1] at the CERN Large Hadron Collider (LHC) [2] is a general purpose detector, aiming at a TeV-scale reach for new physics. The LHC is expected to start with luminosities ramping first to 10^{33} cm^{-2}s^{-1} in its initial running and gradually increasing up to 10^{34} cm^{-2}s^{-1} (corresponding to an integrated luminosities of up to 10^5 pb^{-1} per year). The semiconductor tracker is required to reconstruct isolated leptons with a transverse momentum of p_T>5 GeV with 95 % efficiency out to $|\eta| \leq 2.5$, to measure momentum even at p_T = 500 GeV with better than 30% precision, to track back to the vertex z-coordinate with better than 1 mm accuracy, achieve two track resolution of better than 200 μm at 30 cm radius and represent no more than 20% X_0 in total [3].

To achieve this, a design consisting of 4 barrels of 2112 silicon modules in total and 2 sets of 9 disks (each set comprising 988 end-cap modules) was adopted by ATLAS. Roughly speaking, the barrel region covers $|\eta|\leq1$ on its own, with the disks needed to extend the coverage to $|\eta|\leq2.5$ while minimising the material seen by the highly inclined tracks in these directions.

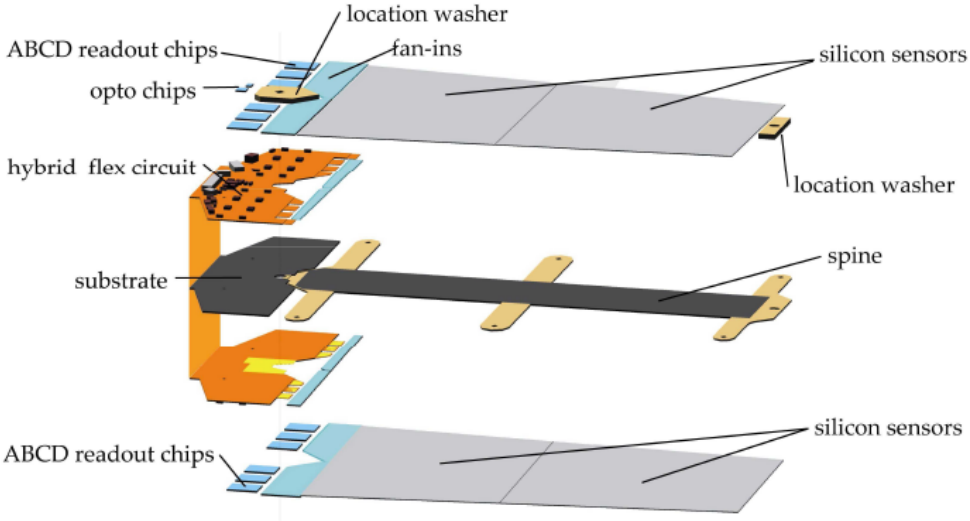

Figure 1.1. Exploded view of an SCT end-cap module showing the different components.

While the barrel only requires one module type [10], the end-cap region has four module types and five different sensor types. The end-cap sensors have also been purchased from two different suppliers. However, all the end-cap modules, as seen in Figure 1.1, have, located at one end, identical high density Cu/Polyimide flex circuits [5], *hybrids*, to house the ABCD3TA read-out ASICs [6]. They also share the same thermal design, with the sensors sandwiched round a thermal pyrolytic graphite (TPG) [11], *spine*, which conducts heat away from the sensors to the cooling block contacts. The two-sided hybrid circuit is laminated around a high conductivity carbon-carbon (CC) substrate which contacts the main cooling block directly, such that no heat from the read-out chips should flow into the sensors. The hybrid and the sensors are, in addition, separated by a thermal break bridged by fan-in structures used to connect the sensors to the ASICs. This is important since the sensors need to be kept cool, -7^{o}C, to *freeze out* radiation damage annealing effects [12] and to keep the irradiated sensor currents below ~0.5 mA each. For most module types, two sensors per side are *daisy-chained* together to give ~12 cm strip length per channel. The requirement of negligible shot-noise contribution and the physics of the annealing process (which leads to additional degradation with time unless cooled) drive the sensor temperature requirements. A further demand on the thermal design comes from the need to avoid silicon self-heating, since this will drive up the leakage current, in turn leading to further self-heating and possible "thermal runaway".

Figure 1.2. ATLAS SCT end-cap modules. From left to right: outer, middle and inner. There is a fourth type, the short-middle, that follows the design of a middle module with only a pair of silicon sensors.

Mechanical tolerances for the building of the 1976 (+ spares) end-cap modules of the ATLAS SCT are very tight to ensure that the intrinsic spatial resolution of the silicon detectors is in no way compromised. The complexity and extreme requirements for 10 years LHC operation as a high resolution, high efficiency, low noise tracking system have resulted in demanding and time consuming quality assurance procedures for every module. The assembly and testing has been distributed over 14 institutes based in Australia, the Czech Republic, Germany, the Netherlands, Poland, Spain, Switzerland and the United Kingdom. The final assembly of modules onto their disks is carried out for "End-cap A" in the Netherlands and for End-cap C" in the UK, prior to both assemblies being transported to CERN for integration into the ATLAS Experiment.

2. Layout of the ATLAS Silicon Tracker.

This section describes the arrangement of tracking sub-detectors employed in ATLAS to measure charged particle 3-momenta, determine their charge, reconstruct secondary and tertiary vertices, and identify interactions with the material in the tracking volume.

2.1. Physics Goals of the ATLAS Silicon Tracker.

The ATLAS Inner Detector (ID) is 2.3 m in diameter, 7 m in length and consists of the Semiconductor Tracker (SCT), with the Pixel detector within it and the gaseous/polypropylene foil Transition Radiation Tracker (TRT) surrounding it [3]. The ID sits within a 2 T magnetic field, provided by the superconducting central solenoid, integrated inside the cryostat of the Liquid Argon electromagnetic calorimeter.

The very high interaction rate at full luminosity and the high energy of jets, lead to requirements of both high granularity and high spatial resolution. These effectively determine the strip dimensions, given also that the

ABCD3TA [6] read-out chips give a binary read-out with a variable threshold typically set to 1 fC for unirradiated operation. The resolution requirements for isolated tracks are set by the transverse momentum precision of ≤30 % at 500 GeV discussed above. In practice, this is readily achieved by measuring 4 space points along the track with the 16 μm resolution in the φ coordinate provided by the 80 μm pitch (two sided with 40 mrad stereo) of the SCT modules, even without the charge interpolation possibilities which would come from analogue read-out. More severe are the requirements on the granularity to maintain typical hit occupancies of order 1 % or less, even within high p_T jets. Also, because the capacitive load on the ABCD3TA chips cannot exceed 18 pF if noise of 1500 e^- ENC is to be achieved, the length of the strips cannot exceed 12 cm for 1.2 pF/cm capacitance (when also allowing for fan-in and bonds).

The layout described below was chosen to ensure four space points in the SCT (where the orthogonal coordinate to φ measurement comes from the small angle stereo between front and back strips) on any track from the primary interaction region. The geometry is chosen to satisfy this for interaction points up to two standard deviations away from the detector centre along the *z*-axis. The standard deviation of the interaction point in *z* is expected to be 76 mm at nominal LHC operation.

2.2. Operating conditions in ATLAS

The modules of the ATLAS SCT have been designed to withstand doses of up to 2.14×10^{14} n_{eq}/cm^2 normalised using the non-ionising energy loss (NIEL) cross-sections to the expected damage of 1 MeV neutrons [3]. This assumes a 3 year start up at lower luminosity followed by 7 years at design luminosity and includes a 50 % additional safety factor on the simulated particle fluences. The radiation environment largely determines the other operating conditions which are designed to ensure the modules remain performant to the end of such an operating scenario.

Key to retaining good performance is limiting the "reverse annealing" of the sensors. It has been one of the key observations of operating irradiated high-resistivity silicon micro-strip detectors that their depletion voltage, V_{dep}, and hence their required operating voltage for high efficiency, varies with time long after exposure to radiation. Furthermore, while the radiation induced currents fall with time [13], the behaviour of the effective doping concentration, N_{eff}, (which determine the V_{dep} value) shows a more complicated behaviour [14].

The first observation is that N_{eff} initially drops with dose for p^+-in-n^- sensors, but after about 2×10^{13} n_{eq}/cm^2 the material effectively inverts space-charge from being n-type and acts as if it is increasingly p-doped with dose [15]. Furthermore, the effective doping after inversion tends to grow with time, "reverse anneals", but in a way that is strongly dependent on operating temperature. This motivates the requirement of an average operating temperature on the sensors of -7°C which effectively "freezes out" the reverse annealing, at least during data taking. A uniformity of better than 5°C across the silicon is also required. Finally, once one takes account of realistic maintenance scenarios [3] it is required that one allows for V_{dep} values of up to 300 V and corresponding operating voltages of up to 350 V.

The requirements of cold operation of the sensors, given the 7 W module power dissipation after irradiation, lead to the need for coolant temperatures of down to -25°C. This in turn requires the dew-point in the detector environment to be well below this value, leading to the need to flush the SCT with nitrogen or very dry air. The requirement to operate cold, as well as dry, is reflected in the testing of the modules discussed below.

2.3. End-cap Mechanical Layout

A view of the ID is shown in Figure 2.1. The ID consists of both barrel and end-cap regions to minimise the material seen by traversing particles as a function of polar angle. The barrel region is made of 4 cylindrical layers and the end-caps consist of 9 disk layers. The geometry is determined by the 4 space point requirement above, with a coverage in η out to 2.5 (allowing for the *z* dispersion of the primary interactions). The resulting tracking detector has $63m^2$ of silicon micro-strip detectors with just under 40 % in the two end-caps.

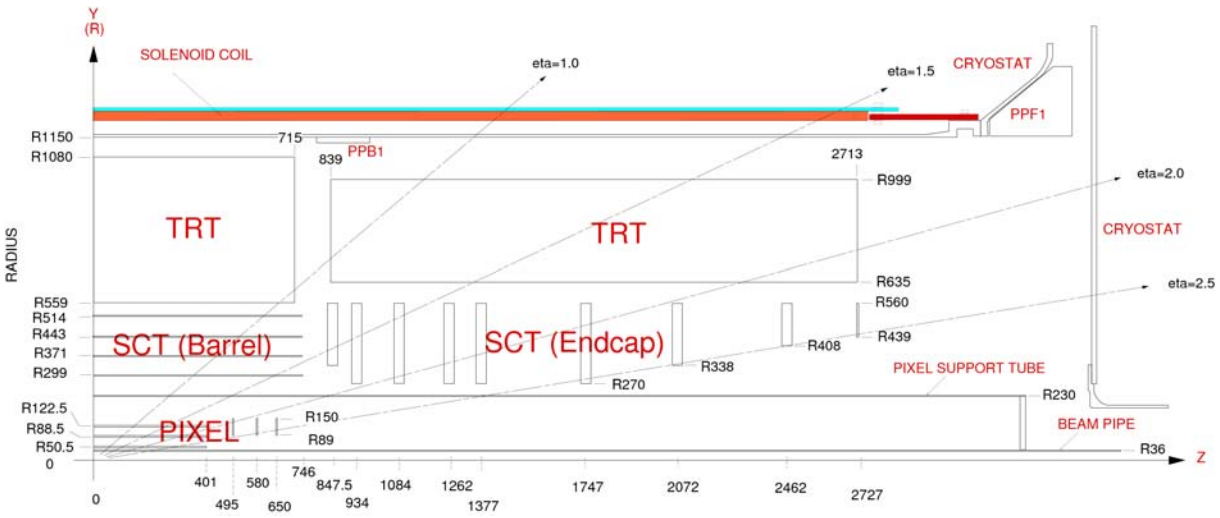

Figure 2.1. A quarter section view of the ATLAS Inner Detector (ID).

2.4. Spatial Resolution Requirements

The physics specification for the p_T resolution of 500 GeV tracks in the inner detector is $\Delta p_T/p_T < 30$ % at $|\eta| < 2$, relaxed to 50 % for $|\eta|$ up to 2.5 [4]. The p_T resolution of the final inner detector design is shown in Figure 2.2 at 20 GeV and 1000 GeV. Clearly it depends on the spatial resolution of all three sub-detectors; pixels measuring 3 points with 12 µm resolution, SCT measuring 4 points with 16 µm resolution and TRT measuring 36 points with 170 µm resolution. If this specification were the only one that mattered to the SCT an increase in the pitch would be possible. However, the argument for limiting the pitch to around 80 µm is based primarily on occupancy.

Pattern recognition performance in the tracker is fundamentally limited by occupancy. In the case of the SCT with binary readout, the only way to resolve two tracks is to see them as two hit strips with at least one empty strip in between. The noise occupancy of the SCT is very low (< 0.1 %) by design, and its occupancy due to underlying events at full luminosity is also low at around 0.5 %. These levels do not pose a significant problem for track finding. However, the occupancy of a module hit by a *b* jet is typically 1.5 % and this can make track finding difficult. Figure 2.3 shows track reconstruction efficiency as a function of distance from the jet axis. The efficiency is already down at 89 % (compared with 98 % for isolated muons) because we are dealing with pions with p_T down to 1 GeV. The efficiency drops further to 78 % near the core of the jet, indicating pattern recognition difficulties. An indication of the role of the SCT in track finding in jets is that the average efficiency of the whole tracker is 89.5 % with a fake rate of 0.24 %. If one layer of the SCT is removed, the efficiency only drops to 89.0 %, but the fake rate doubles to 0.46 % [3]. These numbers show that high occupancy is already a cause of some tracking inefficiency with 80 µm SCT pitch and would be worse with larger pitch. Lower pitch would give lower occupancy but is ruled out on grounds of cost and power density.

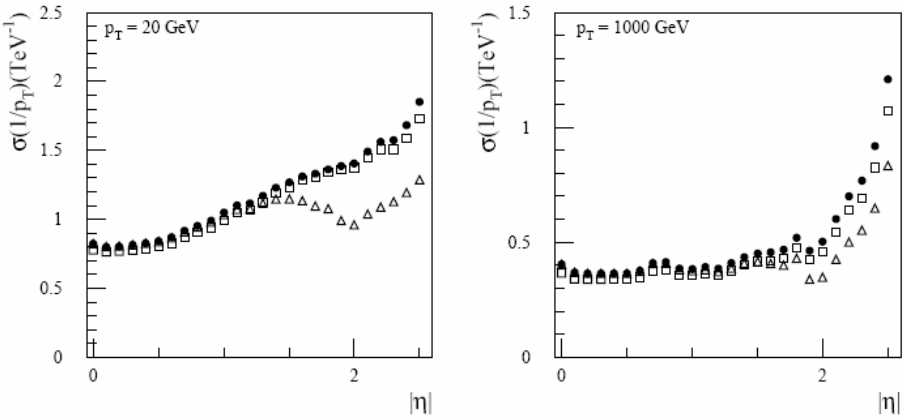

Figure 2.2. p_T Momentum resolution as a function of $|\eta|$ for simulated muons of various momenta. Results are shown for a solenoidal field without (circles) and with (squares) a beam constraint and for a uniform field without a beam constraint (triangles).

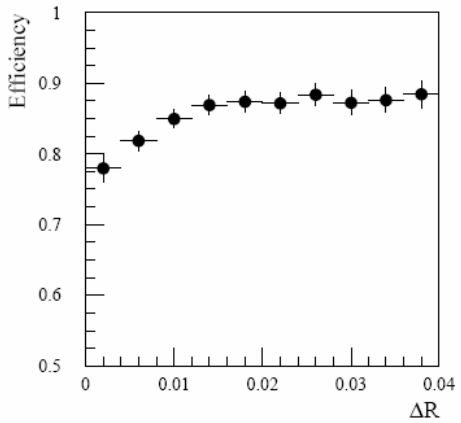

Figure 2.3. Track reconstruction efficiency as a function of distance from the jet axis.

There is a small stereo angle between the front and back detectors of an SCT module. As stereo angle is reduced, it reduces the number of allowed combinations of a φ strip with a stereo strip, but at the same time it degrades the space-point resolution in the radial direction making it more difficult for pattern recognition software to choose the right combination. Simulation studies showed that these competing effects largely cancel, so that pattern recognition performance is weakly dependent on stereo angle in the range 40 to 80 mrad. We chose to use 40 mrad because it reduces the size of the corner regions, where the corner of a stereo detector sticks out beyond the sensitive area of a φ detector, or vice versa. Small corner regions make it easier to tile an area with modules efficiently and make pattern recognition less sensitive to module misalignments.

Having designed a high resolution tracker, it is required that any misalignment of its components should lead to negligible loss of resolution. It was chosen to define 'negligible' as a 20 % loss of track parameter resolution, relative to the performance of a perfectly aligned inner detector. A simulation study was performed to find a set of misalignment tolerances appropriate to each sub-detector, such that the resolution of the whole ID was within 20 % of its ideal value. All five helix track parameters were considered in this study but in fact only the p_T and impact parameters turned out to be relevant. The alignment required for the SCT end-caps is shown in Table 2-1. These tolerances apply to the total errors, made up from of uncertainty about the module position combined with uncertainty about the position of the four detectors within the module. The former uncertainty will be by far the most difficult to control, so we assign to it most of the error budget and use one third of the budget for the tolerance on the relative positions of detectors within the module.

Table 2-1. Alignment accuracy required for the SCT (μm r.m.s.)

	Total error budget	Detector alignment within module
$r.\varphi$	12	4
z	200	67

2.5. Description of the Module Geometries

The geometries of the four types of end-cap module are closely coupled to the constraints of processing on 4” wafers, the z-position of disks in the end-cap and the engineering design of the support disks.

The physics requirements of 4 r-φ / r hits up to η = 2.5 together with the overall detector active volume constraints on the radius 275 mm < r < 560 mm and |z| < 2800 mm lead to a layout consisting of 9 disks. Each disk has one, two or three rings of modules, named Outer, Middle and Inner. All modules belonging to a particular ring type are identical. The active length of the modules for the outer and middle rings is ~120 mm whilst that of the inner ring is ~ 55 mm. Each module consists of two planes of sensors glued ‘back-to-back’ around a central spine. In the case of Outer and Middle modules, each side contains two daisy chained sensors to achieve the required active length. There is a relative angular rotation between the two planes of sensors of 40 mrad to give the required position resolutions in r-φ (16 μm) and r (500 μm).

The coverage of each disk is required to be fully hermetic, except for the unavoidable dead area between the two sensors in each plane for outer and middle modules, for tracks above a transverse momentum of 1 GeV. Moreover, the layout allows sufficient overlapping active area between neighbouring modules for the module alignment parameters to be efficiently determined. As a consequence, the shape of the modules is trapezoidal, resulting in a variable strip pitch.

The number of modules in a given ring was determined in the process of defining the module geometries by requiring that the total number of modules, and therefore silicon sensors and hence cost, was minimised. This is equivalent to using the largest sensor geometries that could be accommodated on a wafer.

The active area overlap between neighbouring modules in r-φ is achieved by staggering modules in z by ±1.5 mm about the mean z of the ring. The design of the disk is such that the outer and inner rings are mounted on the side towards the interaction point ('front') whilst the middle ring modules are mounted on the side away from the interaction point ('rear'). The distance in z between upper modules on either side of the disk is 34.0 mm.

Table 2-2. Sensor dimensions, module locations on the disks, their tolerances and rφ overlap between neighbouring modules.

Module	Sensor Type	Sensor Centre mm	½ length mm	Rin mm	Rout mm	rφ Overlap (mm)	rφ tolerance (μm)
Inner	W12	304.550	29.5500	275.00	334.10	0.442	67
Middle	W21	369.163	31.5625	337.60	400.73	0.588	99
	W22	429.063	26.2375	402.83	455.30		
Outer	W31	470.555	31.7900	438.77	502.35	1.437	286
	W32	532.223	27.7775	504.45	560.00		

The final geometries for the 5 individual silicon sensors needed were determined in an iterative fashion starting with a nominal physics layout. The geometry of the two sensors making up the outer ring module was determined using the outer active radius in ATLAS of 560.0 mm and the constraint that there must be no feature extending beyond a radius of 44.72 mm from the centre of the undiced 100 mm wafer. The outermost sensor is denoted W32 and its partner is W31. The innermost edge of W31 defines the limit of coverage of the outer module.

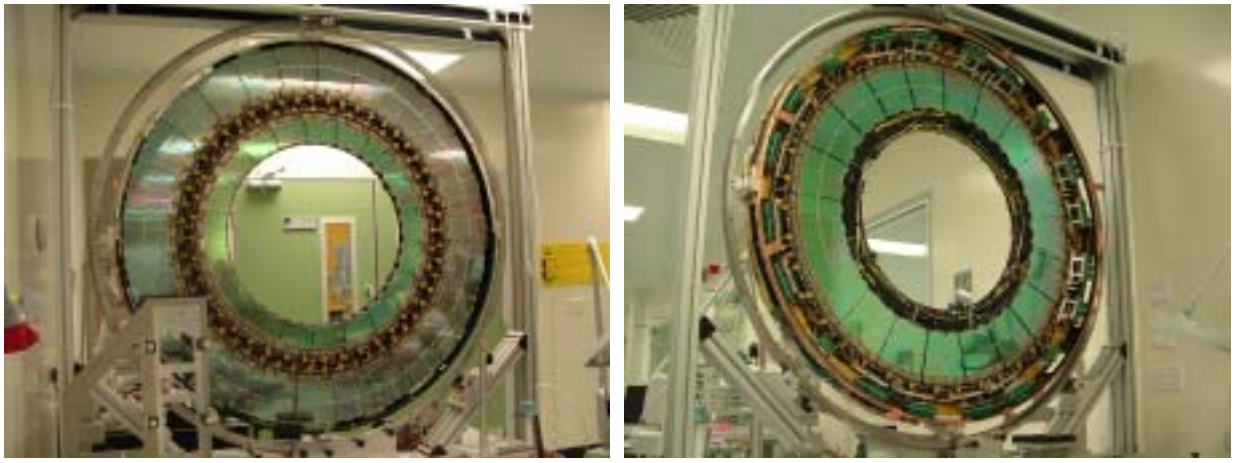

Figure 2.4. Modules mounted on the disk. The left picture shows the outer and inner rings on one side of the disk and the picture on the right shows the middle ring on the other side of the disk.

The effective radius of the inner corners of W31 together with the requirement of hermeticity defines the outer radius of the middle ring. This is fixed by extrapolating a line corresponding to an infinite momentum track, originating from $z = -2\sigma_z$ (σ_z the beam spread in z) over the 34 mm gap that separates the middle and outer rings at the z position corresponding to disk 1. As above, the geometry of the two sensors was determined by the 44.72 mm processing constraint. Here the sensors are denoted W21 and W22. The inner

edge of W21 defines the limit of coverage for the middle ring. Similarly, the geometry of the inner ring was determined from the inner active edge of W21 and the 34 mm front-to-back module separation. This time the limiting case is disk 6. Again, the limiting processing radius then defines the inner edge of the inner sensor, denoted W11.

Following the basic definition of the module geometry, further studies with stiff tracks were used to refine the positions of the disks and to optimise which disks have inner rings of modules. These studies showed that the best overall tracking performance was achieved with a layout that is only fully hermetic for disk 3 onwards. The layout resulting from the process is summarised in Table 2-2 and Table 2-3.

The detailed sensor dimensions are documented in a set of detailed sensor definition drawings at [12].

Table 2-3. Module distribution between disks.

Disk	1	2	3	4	5	6	7	8	9
z (mm)	853.8	934	1091.5	1299.9	1399.7	1771.4	2115.2	2505	2720.2
Outer	52	52	52	52	52	52	52	52	52
Middle	40	40	40	40	40	40	40		
Short Middle								40	
Inner		40	40	40	40	40			

The final disk positions are defined in the note [20] which develops on previous work documented in [17]. Table 2-3 shows the z position of each disk and the numbers of each module types assigned to them. At the z position of disk 8, a line corresponding to η=2.5 would cut a standard middle module in half. To reduce cost the "short-middle module" was developed. This uses just the W22 sensor and has an inner active radius of 402.83 mm. Also, in order to give a disk 9 position within the allowed z constraints whilst maximizing the coverage in η, disk 9 is rotated about the vertical axis so that the outer module ring is to the rear.

The definition of the main parameters of the module design are determined by the sensor geometries and the design of the individual components, such as the hybrid, fan-ins etc which comprise the module. These parameters then feed in to the specifications for the engineering parameters (eg. mounting block position) for the disk.

A consistent CAD model of each module type was generated in Pro-Engineer. From this model the individual sub-component part drawings were generated for manufacture. The use of Pro-Engineer also allowed the module models and disk models to be combined to ensure consistency in the module-to-disk interfaces.

2.6. Module Layout on Disks

The layout of modules on the 9 discs at each side is organised to ensure coverage to $\eta \leq \pm 2.5$ on each side. This is achieved with disks arranged out to 2800 mm in z, either side of the nominal interaction point (see Figure 2.1above). The 4 module types described above are distributed as shown in Table 2-3. It should be noted that to allow for initial yield estimates and possible damage during assembly, 20 % more modules of each type were built than the numbers listed in this table for each end-cap.

3. Overview and Motivation for the ATLAS End-cap Module

This section describes the technical choices made to deliver a detector system with the required physics performance. Many of the constraints come from the very high luminosity of the LHC, with its 25 ns beam-crossing interval, very high number of tracks per event, and extreme radiation environment.

3.1. Electrical and Optical Interfaces.

The sensors are readout by twelve ASICs housed in the hybrid, a double sided, Cu/Polyimide flexible circuit laminated onto a carbon-carbon substrate. The chips should be radiation resistant, up to 10 MRad, fast in order to efficiently identify the beam crossings, low noise, low power and capable of keeping the data in on-detector buffers during the first level trigger latency time.

The Atlas Binary Chip (ABCD3TA [6]]) has been designed to meet the imposed requirements. It has been fabricated using the Radiation Hard DMILL technology [7] and implements a binary readout architecture in a single chip. Binary readout offers advantages in terms of higher data transmission bandwidth, less stringent requirements on the quality of the data links and simpler off-detector electronics. On the other hand, it is more immune to external electromagnetic interference and special care has been taken in the design and grounding of the system to avoid problems. In addition, the proper threshold setting and channel-to-channel matching is crucial for a binary system, as it is impossible to distinguish between large noise fluctuations and genuine signal after the discriminator.

The ABCD3TA chip has 128 channels and comprises front-end circuitry (employing a bipolar transistor at the input stage), discriminators, binary pipeline, derandomising buffer, data compression logic and readout control logic. The 25 ns peaking time is short enough to keep the time-walk in the range of 16 ns and the double peak resolution below 50 ns, ensuring that the fraction of events shifted to the wrong beam crossing is below 1 % and that less than 1 % of the data will be lost at the highest occupancies. To compensate the expected drop of the DC current gain after irradiation, a 5-bit DAC has been implemented in the chip to adjust the collector current of the input stage and optimise the noise performance. In addition, the bias current of the following stages is also controlled by another 5-bit DAC. The preamplifier-shaper stage is followed by a discriminator with a common threshold for all the channels that is controlled by an 8-bit DAC. To maintain the channel-to-channel variation of the threshold below the 4%, especially after irradiation, the ADCD3TA implements an individual threshold correction in each channel with a 4-bit DAC with four selectable ranges. Data from the discriminator output is latched in the input register every 25 ns, either in edge sensing or level mode, and clocked into a 132-cell pipeline that matches the first level trigger latency time. Upon reception of a trigger, the data are transferred from the pipeline to the second level buffer, eight events deep. Data is then compressed by the data compression logic and read out via a token ring, allowing for the readout of the six chips in a hybrid side through a single data link. On top of that the chip implements a calibration circuitry and a redundancy mechanism that redirects the output and the readout control signals of the chip so that a failing die can be bypassed.

The sensor bias voltage is filtered in a dedicated network at the hybrid as shown in Figure 3.1. The high voltage is then supplied by the hybrid at a pad in an extension of the hybrid flex (*finger*) that contacts a metal trace on one of the AlN cross pieces of the spine, into which the sensors are glued with a conductive epoxy. At the interface of the cooling block the hybrid implements a shielding scheme that will shunt any noise from the cooling block into the main analogue ground. For the sensors a shunt shield also needs to be implemented. This is done using the spine TPG acting as a conductive layer between sensors and cooling blocks. The TPG is electrically insulated from both and, in order to behave as a shunt shield, connected to the analogue ground through a capacitor (see Figure 3.1 at the top). In order to have the TPG and the sensors at the same DC level, the TPG is connected to the detector bias through a 1 MΩ resistor. This connection is done with another finger similar to the one used for the sensor bias.

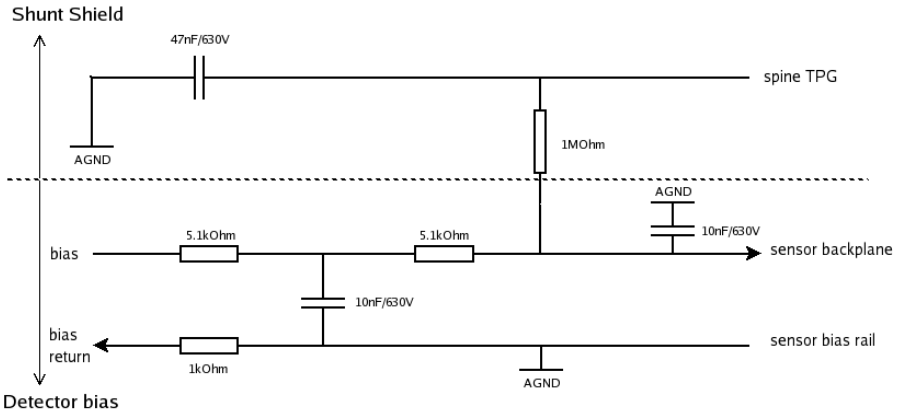

Figure 3.1. Filter network implemented in the hybrid for the high voltage supply

The electrical interface between the end-cap modules and the disk services occurs mainly at the hybrid level. Power supply currents and DC levels, needed to operate the ASICs and to bias the sensors, are carried by power tapes that will connect the module to the periphery of the disk with minimal radiation length. As for the grounding, the modules' power return will be shorted to the cooling tubes at the module mounting point. The connection is made by means of an additional small kapton finger with a copper trace which is to be soldered to each module end of the power tape.

The data transmission off detector is also an important issue given the huge data rates expected. A system based on optical fibres [8][9] has been designed because of its low mass and the absence of electromagnetic interference. Optical links will also be used to distribute timing, trigger and control (TTC) data from the counting room to the front-end electronics. There are two data fibres per module. In normal operation each fibre reads out the data corresponding to one side of the module. The system contains immunity to single point failure. The redundancy is implemented in the module in two levels. For the data links, when one link fails, all the data from that module can be routed through the other fibre. At the expected occupancies this will not lead to any loss of data. As for the TTC data, the redundant lines are distributed electrically from one module to the neighbour.

3.2. Thermal Design, Simulation and Prototyping.

Outer and middle modules are supported and cooled by their contact with two cooling blocks; the main block (area 230 mm²) is shared between the hybrid and the spine, while the far block (78 mm²) cools only the spine. Inner modules are cooled by the main block and in this case the far block is only for mechanical support. Figure 3.2 illustrates the heat paths in an outer module.

3.2.1. Thermal Loads and Interfaces.

The electrical power input to the whole hybrid is typically 5.4 W but it can be as high as 7.5 W in the worst case, so the design was based on that value. The electrical power input from the unirradiated detectors is negligible. Thereafter it depends on irradiation and annealing history and temperature. After the fast components of annealing are complete, the leakage current is simply proportional to radiation dose and the constant of proportionality is taken from the tests on pre-production detectors. The voltage needed to fully deplete the detectors also grows with radiation and is expected to be around 300 V in the worst case after 10 years. However, the design was made for the maximum voltage available from the power supply; 500 V minus a 40 V drop in the filter. The outcome [18] is that the maximum detector power, including safety factors to allow for uncertainties, is predicted to be 185 W/m^2 at 0°C. The temperature dependence of the detector power is given by

$$P(T) = P(T_0)\left(\frac{T}{T_0}\right)^2 \exp\left[-\frac{E_g}{2k}\left(\frac{1}{T}-\frac{1}{T_0}\right)\right]$$

where $P(T_0)$ is the power at T_0=273 K, T is temperature in Kelvin and k is the Boltzmann coefficient; for the energy gap the value E_g= 1.20 eV, based on measurements of irradiated detectors, is taken.

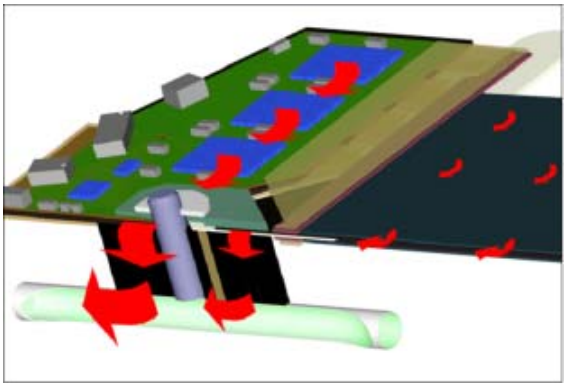

Figure 3.2. Heat flow at the hybrid end of an outer module.

There is a heat load on the detector part of a module due to convection from the surrounding gas. This load was simulated with Computational Fluid Dynamics (CFD) and measured in a mock-up of a full disk [20]. Both approaches predict that the load is strongly dependent on position, being maximal for the outer modules at the top of a disk. Based on these results an upper limit on the detectors convective load was estimated to be 0.8 W for middle and outer modules and 0.4 W for inner modules. This heat is coming mainly from the hybrids and the rest is from the power tapes.

Evaporative C_3F_8 cooling has been chosen for the SCT. The coolant is injected through capillaries into the ∅ 3.6 mm cooling pipes, where it arrives mainly in the liquid phase. Then it runs through the pipe on a wiggly circuit, passing through the cooling/mounting blocks of 10 to 13 modules, before exiting the SCT mainly in

the gaseous phase. By adjusting the pressure at the exhaust we the operating temperature can be tuned over the range –10 to –30°C, though it operates most efficiently near the middle of this range. An important property of the coolant is the heat transfer coefficient (HTC) between the pipe wall and the fluid which shows a strong rise with the power density and is moderately dependent on several other factors. In this system we find that a conservative parameterisation is to take HTC = (1800 + 330×ρ) $Wm^{-2}K^{-1}$, where ρ is the power density in Wcm^{-2} [21].

3.2.2. Thermal Specifications.

The equivalent noise charge of the ABCD3TA readout chip has a temperature dependence of 6 electrons per Kelvin before irradiation and 24 electrons per Kelvin after irradiation [25]. This temperature dependence is not negligible compared with the design noise level of around 1500 e^- ENC, so there is a motivation to keep the readout chips reasonably cool.

There is a shallow optimum between harmful and beneficial annealing effects in the silicon detectors at a temperature of –7°C. It is likely that there will be some accidental or planned warm-ups of the SCT for maintenance; therefore we specify that the operating temperature of the detectors at maximum power should be below –7°C.

A stronger constraint on detector temperature comes from the possibility of thermal runaway. Heat will be extracted from the detectors mainly by conduction, which is linear with temperature. But the heat generated in the detectors grows exponentially with temperature, doubling every 7 Kelvin. This can lead to an unstable situation called thermal runaway in which the detector temperature rises by positive feedback until limited by some external factor, in this case the HV power supply limit at about 2.5 W. This is a hard failure mode, unlike the chip noise and detector annealing, so we add an extra 30 % safety factor to the detector power and we specify that the module must not go into thermal runaway when the detector power is 240 W/m² at 0°C and the other loads are as specified in 3.2.1.

3.2.3. Split Module and Split Block Design

Thus we have a strong specification on the temperature of the detectors, which generate around 2 W, and a weaker specification on the temperature of the chips, which generate around 7 W. So we can benefit by providing separate heat paths to the coolant from the detectors and from the chips. This leads us to our design of a module that is thermally split between the detector part and the hybrid part. The glass substrate of the fan-ins and plastic base of the location washer provide mechanical connection combined with thermal isolation between the two halves of the module. The TPG spine and the carbon-carbon (CC) substrate of the hybrid provide low resistance heat paths to the cooling block within their respective parts of the module. Having split the module, we found that we could also benefit by introducing a thermal split into the main cooling block. This was done by making the block from a CC-PEEK-CC sandwich, where the 1mm layer of PEEK is aligned with the thermal split in the module.

The thermal performance of modules has been simulated with FEA programmes and measured in several dummy modules and one real irradiated module. The results are reported below, starting with the hybrid part of the module.

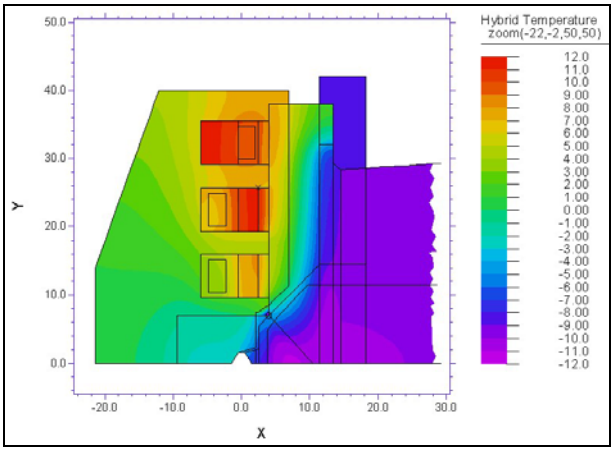

Figure 3.3. The hybrid end of an outer module simulated at full power and with the coolant at –20°C. The simulation has a 2-fold symmetry (zero stereo angle) so only half of the module is shown.

3.2.4. Hybrid Thermal Performance

Figure 3.3 shows the hybrid end of a full module thermal simulation at maximum load. It illustrates the large temperature gradient across the fan-in and the rather uniform temperature of the near-by detector. The hybrid is simulated in some detail, showing that the chip farthest from the cooling block has its thermal plug under the analogue part where most of the heat is generated, while the others are cooled by plugs under the digital part.

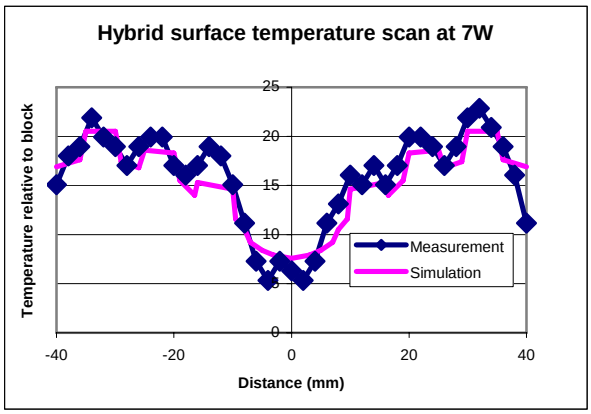

Figure 3.4. Measurement and simulation of the hybrid surface temperature profile on a line passing through the six ABCD chips. Temperature is relative to the cooling block.

Figure 3.4 shows a measurement of the chip temperatures using an infra-red sensor scanned in a straight line across a hybrid operating at maximum power. The sensor sees an area of 2×2 mm² and is calibrated for the emissivity of the chips with an accuracy of ±2 K. The result is compared with a simulated temperature profile. We conclude that the chip temperatures are reasonably well understood and are not excessively high.

Table 3-1 illustrates how the simulated total temperature difference of 29 K between chip 2 and the coolant is built up from smaller temperature differences along the heat path. This apportioning of the temperature drop into a series of steps can only be approximate since the real heat path is three-dimensional.

Table 3-1. Showing how the temperature difference between the middle chip and the coolant is built up.

Step	Material	ΔT [K]
Chip to substrate below chip	AlN plug and two glue layers	4
Within substrate	Carbon-carbon composite	9
Substrate to surface of block	Thermal grease	3
Within block to pipe	Carbon-carbon composite	4
HTC into coolant	C_3F_8	9
TOTAL		29

3.2.5. Spine Thermal Performance

Figure 3.5 shows the simulated temperature of the detector part of an outer module at full power. It shows that the detector temperature is rather uniform, covering a range from –9.1°C to –11.7°C. More details of the behaviour of inner and outer modules are shown in

Table 3-2. A consequence of the uniform detector temperature is that the thermal behaviour of a module is accurately predictable from a single thermal resistance value, defined as the area-averaged detector temperature, relative to the block, when a power of 1 W is applied uniformly to the detectors. This resistance value was measured and simulated in both middle and inner modules [19]. The simulation matched the measurement within 20°%, validating the simulation at this level of accuracy.

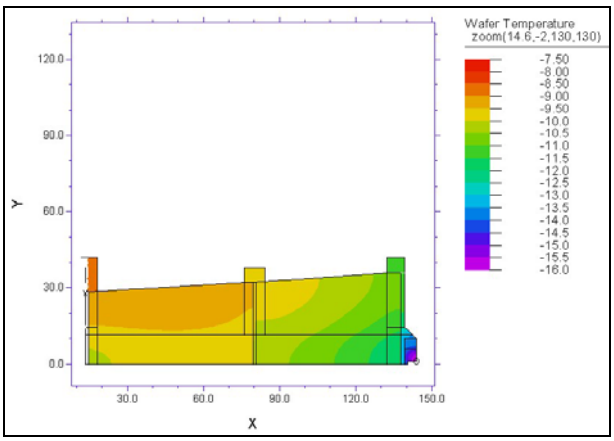

Figure 3.5. The detector part of an outer module simulated at full power and with the coolant at –20°C

Finally we measured the thermal runaway of an irradiated inner module. The radiation damage was not enough to bring the detector power up to the specification level of 185 W/m² at 0°C; it could only reach 107 W/m² at 0°C when biased to 500 V. By running the coolant at –5°C we were able to bring this module into thermal runaway, and a simple scaling law [21] allows us to predict the behaviour of the same module at higher radiation damage and lower coolant temperature. Figure 3.6 shows these results.

Table 3-2. The performance of inner and outer modules, simulated with the coolant at –20°C. Middle and outer modules are identical in terms of thermal properties.

Coolant at -20°C	Module type	
	Outer	Inner
Detector temperature (°C)		
Maximum	-9.1	-6.4
Average	-10.1	-7.1
Heat taken out (W)		
hybrid part of main block	6.8	6.8
detector part of main block	0.7	1.2
far end block	1.3	
Runaway power (W/m^2 at 0°C)	280	290

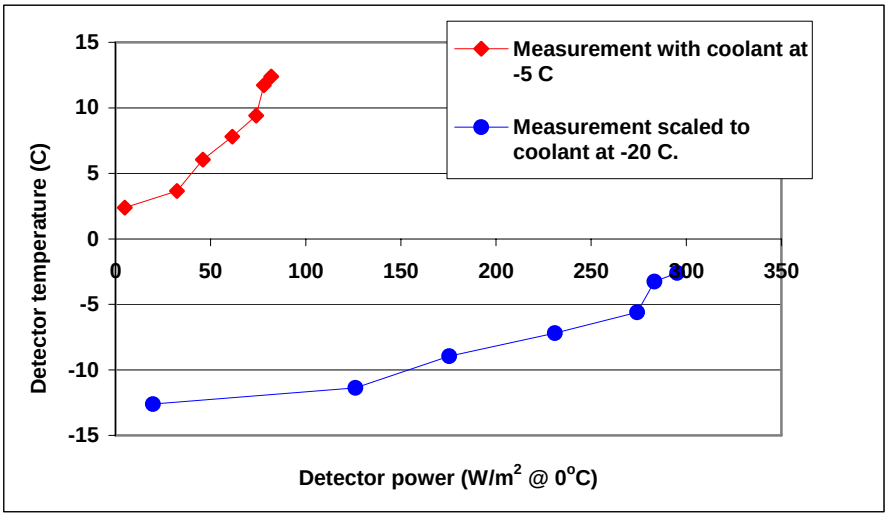

Figure 3.6. Measurement of thermal runaway in an irradiated inner module and extrapolation of the result to a lower coolant temperature.

3.3. Clearances and Mechanical Tolerances

Mechanical tolerances and clearances come, mainly, from positioning requirements and envelopes. The former is driven by the required physics performance, hermeticity, resolution, overlap for alignment, etc., while the latter are set to avoid physical interference of items.

As already mentioned in section 3.2, the modules are attached to two blocks which support them at precise locations as shown in Figure 3.7. The block at the hybrid end provides the accurate positioning of the module, while the slot at the far end provides the module rotation which is set at either plus or minus 20 mrad, depending on the disk number. The accuracy of the z position of the modules will be determined by the tolerances on the block heights while the $r\varphi$ position is determined by the precision of placing rotation holes in the modules and locator pins in the blocks. Also co-planar block surfaces are essential to avoid distortion of modules when they are mounted to the disk, and to maintain cooling contact at the block surfaces.

A given ring has alternating high and low modules with an overlap between neighbours that provides the required hermeticity and allows for the relative alignment of the modules within the same ring using tracks that hit both modules. This overlap in $r\varphi$ determines the tolerances in positioning the module in that direction and these tolerances are different depending on the ring radius, as shown in Table 2-2[23].

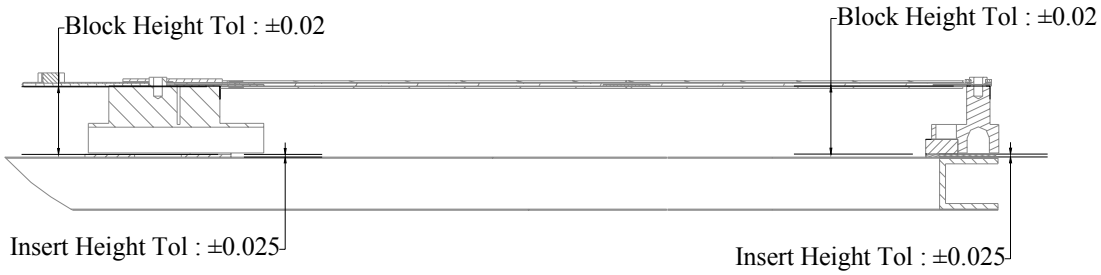

Figure 3.7. Location of a module on top of the two blocks: at the hybrid end (left) and at the far detector end (right).

Mechanical interference constraints require a clearance of 0.5 mm for the position of high to low modules, while 1 mm is required between module components at high voltage and disk services. Figure 3.8 shows the details assuming a wire bond height of 0.6 mm.

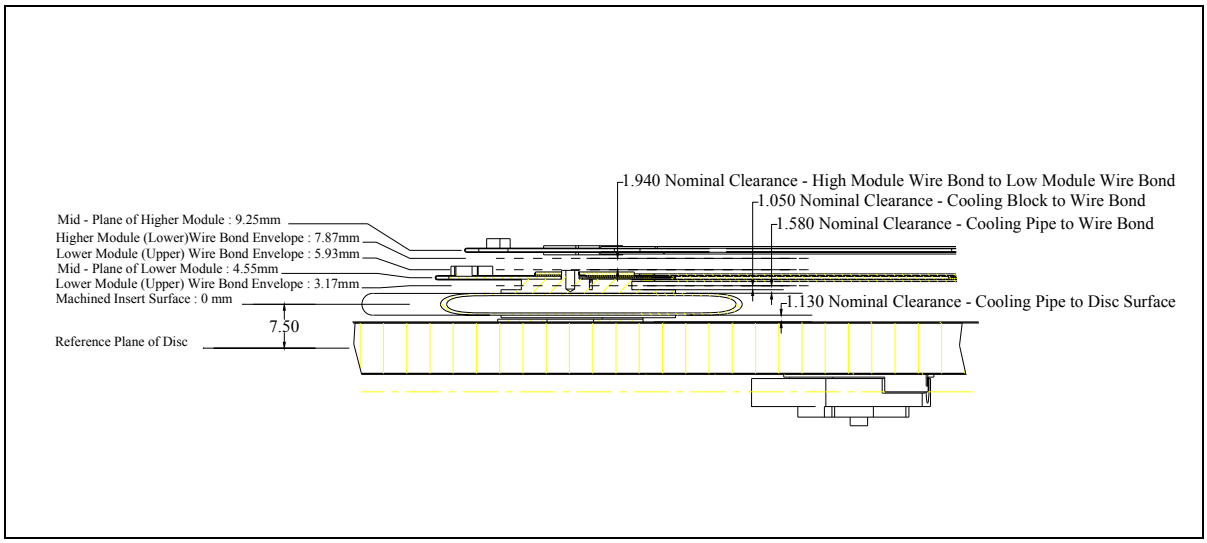

Figure 3.8. Nominal position of high and low modules with respect to disc services.

4. ATLAS End-cap Module Components.

4.1. Sensor designs, Specifications, Testing and Results

The ATLAS micro-strip sensors are fabricated using p^+ implanted ~20 μm wide strips in high resistivity ($\rho > 4$ kΩ/cm) n^- substrate, 285 μm thick, but with a number of features to ensure high voltage operation to cope with the substrate effective doping changes following heavy irradiation. There are 5 different types of forward silicon sensors. They are referred to as W12, W21, W22, W31, W32. W21+W22 are used together to make the middle modules, and W31 + W32 form a pair for the outer modules. W12 is used by itself for the inner modules.They all have 768 read-out plus two edge strips and a wedge-like geometry with a strip pitch varying with the overall device width (see Table 4-1) while allowing always 1000 μm distance from the sensitive area to the physical cut edge. The guard region was optimised by each manufacturer according to their processing to guarantee the current(voltage) requirements outlined below. The implanted strips were required to have $\rho < 200$ kΩ/cm and to be capacitively coupled (>20 pF/cm) to aluminium read-out strips ($\rho < 15$ Ω/cm) matching the implant dimensions. The implants are biased by resistors of 1.25±0.75 MΩ.

Table 4-1. Sensor properties

	Barrel	W12	W21	W22	W31	W32
Length (mm)	64.000	61.060	61.085	54.435	65.540	57.515
Outer width (mm)	63.360	55.488	66.130	74.847	64.636	71.810
Inner Width (mm)	63.630	45.735	55.734	66.152	56.475	64.653
Strip pitch (μm)	80	57-69	70-83	83-94	71-81	81-90
Interstrip angle (μrad)	0	207	207	207	161.5	161.5

The sensors were required to hold up to 350 V with < 20 μA leakage current at room temperature, be able to run to 500 V and to draw < 6 μA at the initial operating voltage of 150 V. Good strip capacitors were required to hold 100 V and the total strip failure rate (capacitor breaks, implant shorts or opens, metal shorts or opens, broken bias connections etc) were required to be < 1%. These specifications were observed by the manufactures and checked by the sensor reception centres of the collaboration. The measurements of the manufacturers were confirmed with high accuracy. For those sensors meeting our specifications, Table 4-2 and Figure 4.1 show the statistics obtained.

Depending on the manufacturer, humidity dependent breakdown effects, which also related to the storage history of the sensors, were sometimes observed [24]. With suitable precautions and after appropriate screening, these issues were not found to affect the performance of any of the modules assembled onto the disks.

Table 4-2. Statistics of the sensor characteristics, showing average values for the percentage of defective strips per sensor and measured currents at 150 V and 350 V.

	Number Built			Defect. strip/sensor			I (μA) @ 150V			I (μA) @ 350V		
	CiS	Ham.	All	CiS	Ham.	All	CiS	Ham.	All	CiS	Ham.	All
W12	776	692	1468	2.3	0.3	1.4	0.751	0.087	0.438	2.532	0.310	1.485
W21	860	757	1617	2.1	0.5	1.3	0.532	0.124	0.339	1.265	0.257	0.790
W22	1114	810	1924	2.2	0.4	1.4	0.689	0.166	0.443	2.176	0.699	1.480
W31	373	2645	3018	3.5	0.5	2.1	0.759	0.286	0.536	1.857	0.817	1.367
W32	363	2596	2959	4.1	0.4	2.3	0.838	0.255	0.563	1.255	0.692	0.990

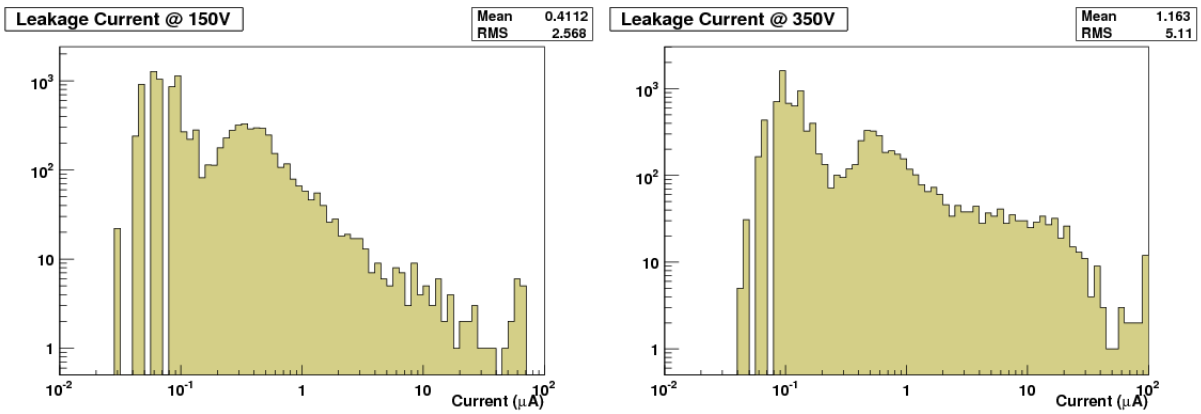

Figure 4.1. Leakage current distribution of all the sensors.

4.2. Hybrid Design, Specifications, Testing and Results.

The end-cap electronics hybrid provides the electrical interface between the module and the disk services. The basic design of the hybrid is six layers of kapton wrapped around a carbon core. It carries 12 ABCD3TA readout ASICs, six on each side of the hybrid, and two ASICs for optical communication, DORIC4A and VDC, on the front side. All are provided with analogue and digital supply voltages. The sensors are connected via the hybrid to the HV power supplies. A direct contact of the carbon-carbon substrate to the cooling system efficiently removes the heat dissipated from the readout chips.

4.2.1. Design.

To achieve the required specifications on electrical stability, mechanical rigidity and thermal performance, the production version of the hybrid was laid out as a flexible printed circuit board folded around and glued onto a unidirectional carbon-carbon substrate with a high thermal conductivity. Details on the substrate are presented in Table 4-3.

Table 4-3. Properties of the carbon-carbon substrate

Thermal conductivity in fibre direction	600-650 W/m K
Thermal conductivity perpendicular to fibre direction	20-30 W/m K
Density	1.9 g/cm³
Young's modulus in fibre direction	300 GPa
Tensile strength in fibre direction	300 MPa
CTE in fibre direction	(-1.0 to -0.5) ppm/K
CTE perpendicular to fibre direction	(10 to 20) ppm/K

In the area where the substrate is mounted onto the cooling block, the flex circuit is cut out to ensure a close thermal contact between the cooling system and the hybrid substrate. To compensate for this cut-out in the analogue ground plane the substrate in the cut-out region is plated with a 22 µm copper layer in a galvanic process. This copper layer is soldered to the analogue ground layer (layer six) at the backside of the flex circuit during the lamination of the flex to the substrate, effectively forming one continuous analogue ground layer.

It is vital to avoid any feedback from digital switching into the analogue part of the ABCD3TA. This required very stable supply voltages and led to an increase in the number of layers from four to six, as two solid planes for analogue ground and power had to be introduced. To further improve the connection of analogue ground and power between front- and backside of the hybrid, there is not only a connection across the wrap around, but also a solid solder connection between the tabs or fingers at the opposite side of the wrap around. Analogue and digital power are decoupled on both sides of each chip and additionally on the front side as well as on the backside to improve the electrical stability of the ABCD3TAs at low thresholds.

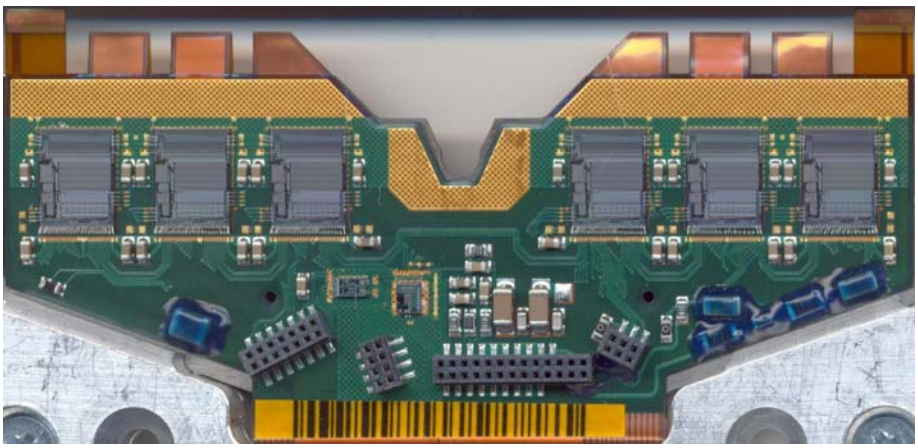

Figure 4.2. Front side of hybrid.

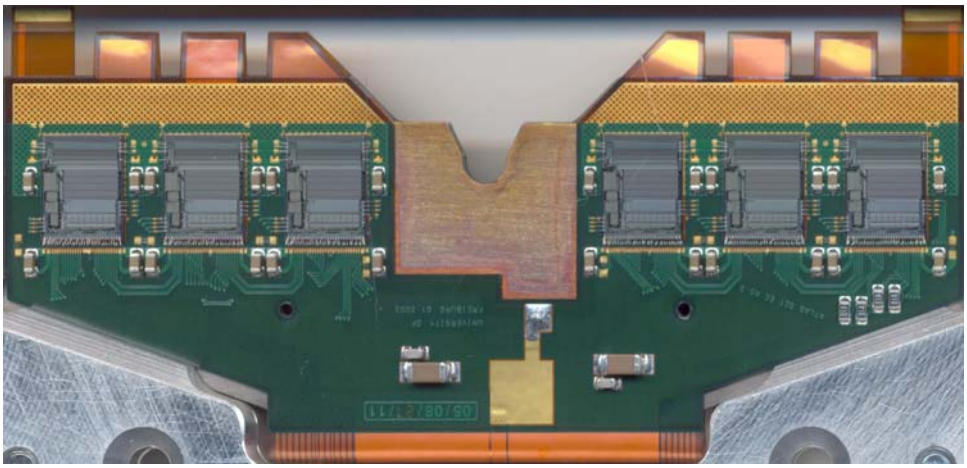

Figure 4.3. Back side of hybrid.

To improve the heat flow away from the chips, the flex has small cutouts underneath each chip. These recesses are filled with ceramic inlays made from aluminium nitride (AlN) with high thermal conductivity (150-180 W/m K). The inlays are glued directly onto the carbon-carbon substrate using a cut-to-shape thermally conductive (3.7 W/m K) boron nitride filled glue foil. These 'thermal plugs' are staggered so that the ABCD3TAs furthest from the cooling block have their thermal plugs underneath the analogue part of the chip, which dissipates more heat than the digital part. The other two chips share the same heat path with thermal plugs under the digital part of the chip. This ensures that the outermost chips have their own heat pipe along the fibres of the substrate, resulting in a more even temperature of all chips. Simulations of the thermal behaviour and a comparison to measured data can be found in 3.2.4.

Hybrid Construction

To attach the ASICs to the flex, electrically conductive silver loaded epoxy[1] was chosen. The coverage of the thermal plugs with conductive glue has to be 100% to ensure a good thermal contact between ASICs and the substrate; the bottom of the ASICs has to be covered with glue on more than 80% of the die area. The ABCD3TAs have to be placed relative to fiducial marks on either side of their chip pad with a precision of 50 µm. The serial number of the ABCD3TA mounted at each of the 12 positions on the hybrid is recorded and uploaded to the production database.

For the wire connections from the chips' pads to the flex circuits' pads Al wedge-wedge bonding was chosen since this process allows for the bond wire connections to be made at room temperature. The wire thickness was 25 µm. The SMD and bond pads on the hybrid consist of copper, which is protected against oxidation by a nickel layer and thin flash of gold deposited in the "electroless" Nickel Gold (ENIG) process. The gold layer prevents the nickel surface from oxidising. The actual bond is made through the gold layer to the nickel surface. Pull strength tests were carried out regularly on samples and showed good adhesion of the bond wire. The average pull strength during production was measured to be around 8 g. After wire bonding, the

[1] Eotite P102.

hybrids were thermally cycled to probe for weak wire bonds, using 10 cycles between –30 °C and +50 °C. The hybrids were then electrically tested with the "*CompanyTest*" procedure (described in 4.2.4) and hybrids passing these tests were delivered to the hybrid QA centres for more thorough electrical tests as described in Section 5.5.

4.2.2. Redundancy

The ABCD3TAs can be configured to three different operation modes; *master*, *end* and *slave*. The default configuration is realised by wiring the appropriate bond pads on the ASICs to the digital ground potential. In addition, this settings can be changed through the TTC commands. The six chips on each side form a chain with the master and the end chip at the 'ends' of the chain. Each chain is read out serially using a token-based scheme. Upon a 'level 1 accept' command, the master chip sends its data to the VDC and when the master chip has finished it passes its token to the next slave chip in the chain. Each chip sends its data to the preceding chip in the chain until the token is passed to the end chip which sends an end-sequence after its data. In such a token-based readout scheme, single chip failure can cause the loss of all data from the following chips. To avoid this, a bypass scheme is implemented to cope for single chip failures without loosing the data of the remaining chips. The only limitation is that the failing chips must not be immediate neighbours.

Both the ASIC that converts the optically transmitted signals to LVDS signals for the ABCD3TAs (DORIC4A) and the ASIC that drives the VCSELs to send the data off the hybrid (VDC) are assembled onto the front side of the hybrid, as seen in Figure 4.2.

To cope with a failure in the optical transmission of the TTC signals on the hybrid (DORIC4A, PIN-diode or optical fibre) each DORIC4A can provide two sets of commands and clock. One set is utilised for normal operation of the hybrid on which the DORIC4A is mounted. The second set of clock and commands is electrically routed through a redundancy link to the neighbouring module and can replace missing clock and command signals there if required.

Each VDC incorporates two channels which in normal operation mode are connected to the front- and back-side respectively. A failing channel (broken optical fibre, VCSEL or VDC channel) can be bypassed by reading the whole hybrid through one channel. The master chip of the problematic side and the end chip of the functional side are configured as additional slave chips. The former master chip sends its data to the former end chip of the functional side.

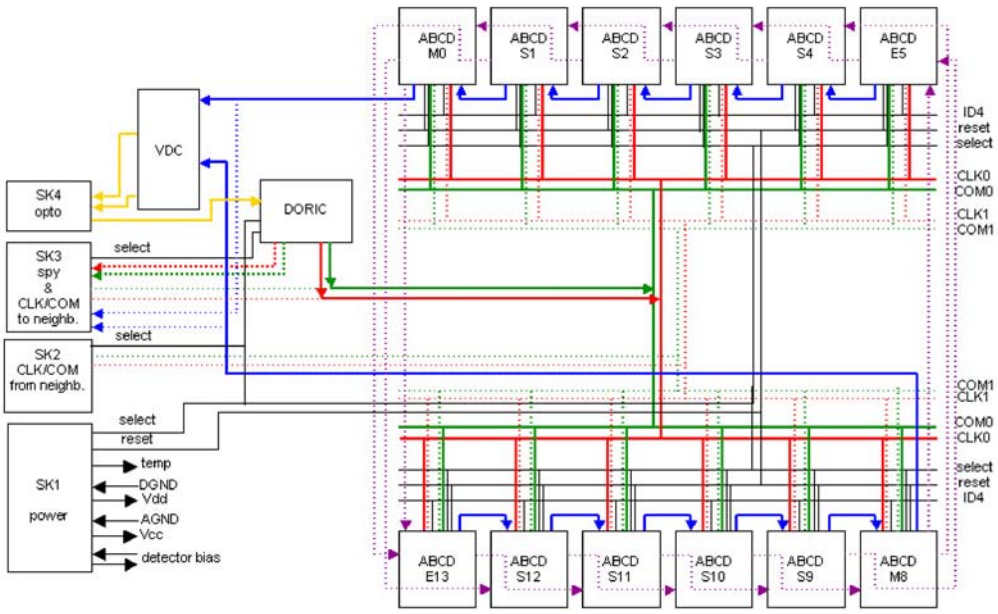

Figure 4.4. Bypass circuit schematic.

4.2.3. Mechanical tests

Before gluing the prepared copper-plated substrate and bare flex together, the thickness and the flatness of the substrate are checked using a simple jig. Flex, glue foil and substrate are aligned using precision pins in the lamination jig together with precision holes in the glue foil and bare flex. After reflow soldering the SMD components to the bare laminated flex, the correct positioning of the opto-connector is checked using a space model of the opto-plugin, as shown in Figure 4.5. The test is passed if the gauge fits onto the connector and can be pushed all the way down to the surface of the hybrid without touching other connectors. This ensures that there is sufficient space for the real opto-plugin. Only hybrids which pass this test may be used for further assembly steps.

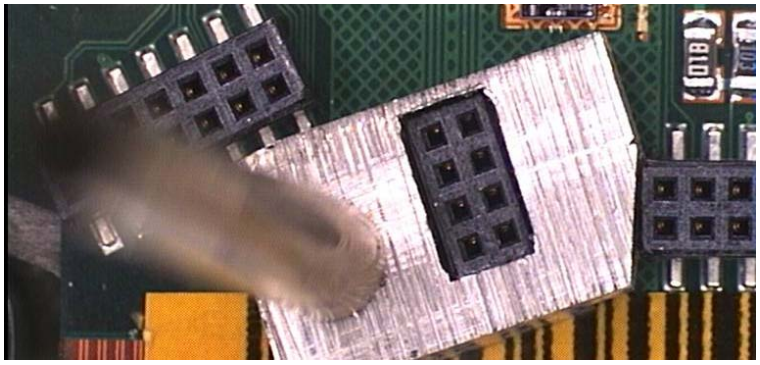

Figure 4.5. The gauge to test the opto-connector position.

Next, the VCC and AGND tabs from each side, visible at the top of Figure 4.2, are soldered. It is verified that they do not protrude beyond the flex surface on either side.

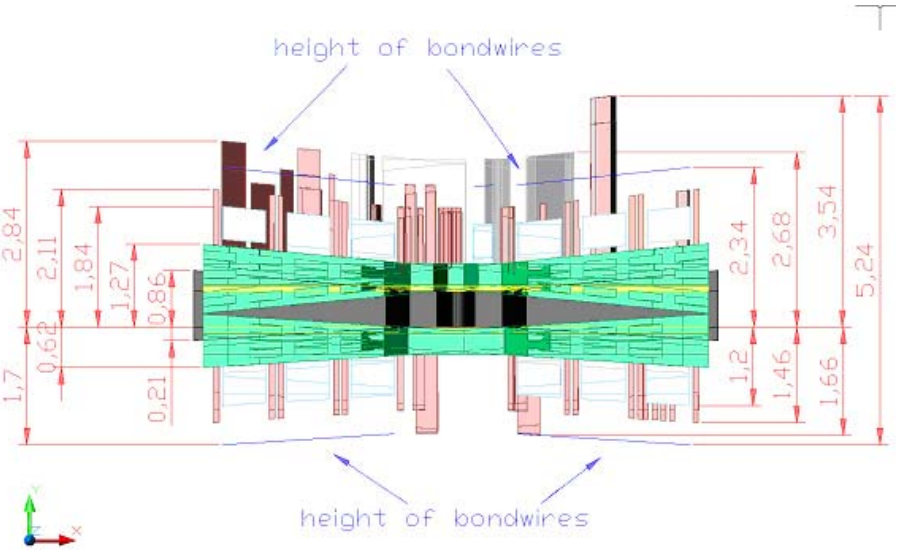

Figure 4.6. The hybrid envelope. For better visibility the vertical scale is enlarged by a factor 10. Dimensions in mm.

After coating the HV parts on the hybrid with polyurethane, it is subject to bending measurements with a measuring microscope to ensure that the bare hybrid complies with the hybrid envelope. It is verified that the thermal plugs do not protrude over the chip pad surface to keep the hybrid inside the envelope and to avoid any tilting of the ABCD3TAs after die bonding.

4.2.4. Electrical tests

The electrical integrity of the hybrid is checked for shorts and correct SMD mounting after the SMD reflow soldering process. The solder joints between the connector pins and the flex surface are checked where possible. The values of all resistors as well as the resistance between all lines routed to a connector pin are measured to ensure that no trace in the wrap-around region has been broken during the lamination of the flex to the substrate. The HV line is probed for continuity with an ohmmeter from the connector pin to the HV fingers. The measurement is done manually since the connections to the pads on the two fingers cannot be measured with the automatic connector tester. The HV part of the hybrid has to pass a HV stability test at an applied DC voltage of 500 V. The leakage current is measured after one minute, and is required to be below

100 nA. Hybrids passing the connector test, HV continuity and leakage current tests are transferred to the bending test before assembling the ASICs. The chip mounting (COB) and wire bonding were carried out in industry as well.

The first electrical test of the die-bonded ASICs takes place during the CompanyTest which is run in pseudo-optical readout mode (see Section 5.5) to test the optical ASICs, as well. The CompanyTest consists of two basic tests that allow a quick verification of the functionality of all active components assembled onto the hybrid: The RedundancyTest and the FullBypassTest. The RedundancyTest checks both the normal operation mode and the redundant mode of the DORIC4A. The FullBypassTest examines both the normal operation data/token transmission and the bypass data/token scheme including the readout over each individual side of the hybrid. It uses single VDC channel readout at different digital supply voltages ranging from the nominal VDD = 4.0 V down to VDD = 3.5 V in steps of 0.1 V.

Hybrids passing these tests were delivered to the three hybrid QA centres. There they were all visually inspected and the analogue and the digital part of the ABCD3TAs were thoroughly tested. The test sequence used in hybrid QA includes a confirmation sequence, a long-term test at elevated temperature and the final cold characterisation. A more detailed description of the tests performed during the characterisation sequence can be found in Section 5.5.

4.2.5. Hybrid production

All necessary assembly steps to build the final hybrid were developed at Freiburg University and then transferred to industrial partners. By implementing a fast feedback between the production companies and Freiburg University it was possible to minimise losses of limited material (especially the ABCD3TAs) and to supply all module assembly sites with a sufficient flow of hybrids to continuously work throughout the production period. It was also of invaluable help in detecting any quality variations or other problems during the mass production.

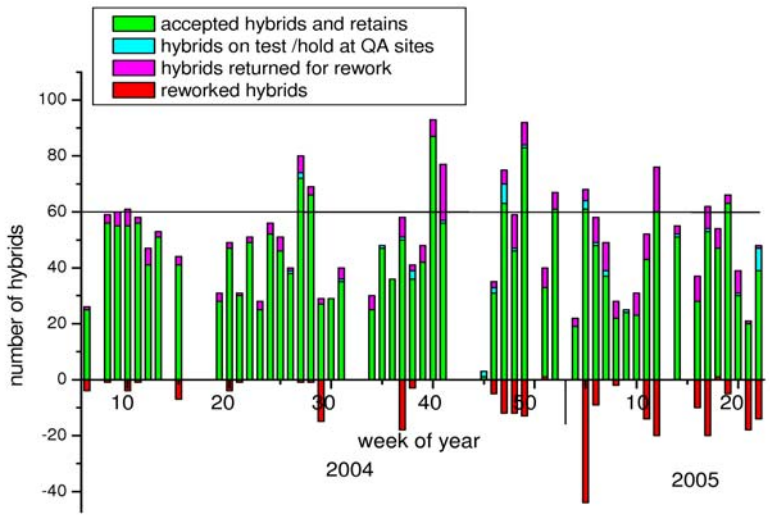

Figure 4.7. Hybrid delivery rate.

One observed problem were delaminations between the individual flex circuit layers, which occurred without a change in process parameters. The root cause of the delaminations was high ambient humidity at the production site in summer. The problem was overcome by adding extra drying steps in the processing to drive out any residual humidity. These drying steps however made the whole circuit more rigid, which meant that some cracks were observed in the wrap-around region. This in turn was cured by bending the circuit in that region over a fixed radius and inserting glue to stabilise the wrap-around.

Another problem was reduced bondability on a few particularly exposed gold bond pads, which occurred again whilst process parameters remained unchanged. This problem was eventually traced to the slow degradation of galvanic baths in the ENIG process, and was overcome once the bath was replaced.

2,587 fully assembled hybrids were produced in industry. Of these, 2,489 were delivered to the module assembly sites and 32 were declared lost due to massive electrical problems. In total 296 hybrids required the replacement of at least one ABCD3TA and 53 hybrids were returned twice for rework. Eleven hybrids were sent to be reworked three or more times. Figure 4.7 shows the hybrid delivery rate over the production period.

4.3. Fan-in Design, Testing and Results

Each of the sides of the SCT end-cap module has 768 sensor channels that are connected to 6 ABCD3TA chips for the signal readout. Therefore, each group of 128 sensor channels has to be wire bonded to a different chip, but the chips are glued in the hybrid with a significant separation from each other. In addition, the pitch of each row of output pads on the sensors in the SCT end-cap module varies between 140 µm and 190 µm for the different types of modules, while the corresponding pitch of the input pads of the ABCD3TA readout chips is 96 µm. Finally, for the sake of position sensing, the sensors are glued in the module with an angle of 40 mrad from each other. This means that the rows of output pads of the sensors face the rows of input pads of the chips with an angle of 20 mrad. All these factors make impossible the direct and automatic wire bonding of the sensors to the readout chips and force the use of pitch adaptors or fan-ins for this function.

The purpose of the fan-ins is, therefore, the electrical connection of every channel from the sensors to the readout chips (see Figure 4.8), adapting the different pad pitch and configuration. They also contribute to the mechanical support between the hybrid and the sensors, and maintain an effective barrier to heat flow between these parts.

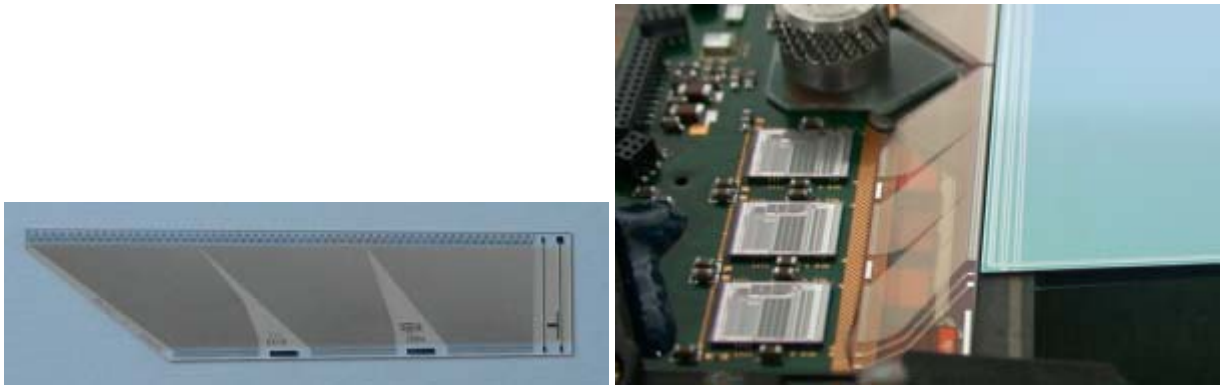

Figure 4.8. Left. A fan-in showing the traces from the ASICs (bottom) to the sensors (top). Right. Fan-in glued to the hybrid and the spine spacers.

4.3.1. Description

A set of four fan-ins is used for each module. Each fan-in connects three readout chips with half the channels of each side of the module. Hence, there are 128 x 3 = 384 metal tracks in every fan-in. There are three different types of fan-ins, one for each type of module: OUTER, MIDDLE, and INNER, and of each of them, there are two kinds: LEFT and RIGHT, for each half of the sensor.

Mechanical dimensions are specified in Figure 4.9. All dimensions refer to cut pieces, with a tolerance of ±50 µm. All types of LEFT fan-ins have the same mechanical dimensions, and so do the RIGHT ones.

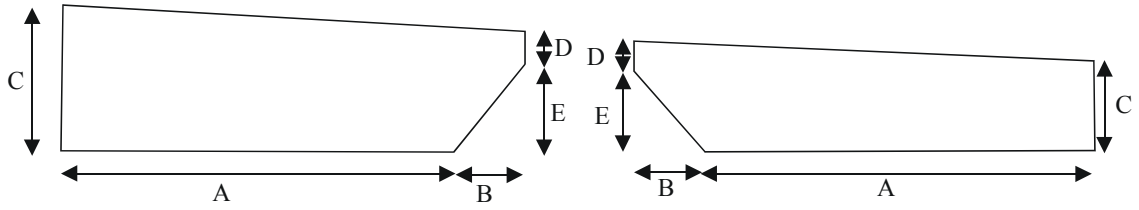

Figure 4.9.Fan-in dimensions.

Table 4-4. Fan-in dimensions in mm.

	A	B	A+B	C	D	E	D+E
LEFT	28.95	7.65	36.60	10.19	2.20	7.25	9.45
RIGHT	28.88	10.12	39.00	8.67	1.40	8.05	9.45

The fan-ins are made of high density metal tracks deposited on top of an isolating glass substrate. A passivation layer covers the tracks for both mechanical and chemical protection.

The metal is made of an alloy of aluminium (99.5%) and copper (0.5%), which is a standard alloy used to increase the electro-migration hardness. The metal is deposited by sputtering from a high purity target. This metal layer is later etched using a standard photolithographic process to define the tracks and bonding pads. The metal lines are protected by a passivation layer with openings at the pads for the wire bonding. This layer is made of a standard positive photolithographic resist which is spin deposited on the substrates. The characteristics of the different materials used in the fan-in fabrication are specified in Table 4-5. A detailed description of the technology used for the fabrication of the fan-ins can be found in [26].

Table 4-5. Characteristics of the materials used.

Component	*Material*	*Thickness*
Glass substrate	Type DESAG 263T	300±20 µm
Metal tracks	Sputter deposition Al(99.5%) Cu(0.5%)	1.00 ± 0.25µm
Passivation	Positive Photoresist HiPR6512 (Arch Chemical Inc.)	2.00 ± 0.25 µm

CAD design tools were used in the design of the fan-ins. A specific design rules file was created and automated violation checks were run on the final designs. Also specifically developed applications, within the Cadence Design Framework II software [27], were run to check for connectivity between the correct pads.

4.3.2. Quality Assurance

The fan-ins must withstand radiation levels up to the doses achieved in the ATLAS-SCT environment after 10 years of operation which, after including a 50% safety factor, corresponds to 10 Mrads and $2x10^{14}$ 1 MeV eq. neutrons. Irradiation tests with neutrons, protons, and X-rays have to be performed on the fan-ins to ensure that they do no suffer significant degradation under the mentioned conditions. Mechanical and electrical quality tests have been carried out after irradiation ensuring good radiation hardness of the technology up to the specified levels. Track resistance, inter-strip conductivity and inter-strip capacitance have been measured after irradiation. No changes have been observed in any of these electrical parameters from their pre-irradiation values.

Nano-indentation tests have also been carried out on the passivation layer in order to assure that there is no degradation in its mechanical parameters. Universal Hardness (H) and Elastic Modulus (E) have been obtained for this layer before and after irradiation, demonstrating that there is no degradation in its mechanical properties. Table 4-6 shows the results of these experiments. It can be seen that there are no appreciable differences in resist layer mechanical parameters before and after irradiation

.

Table 4-6. Hardness test results.

Sample	*Number of Indentations*	*H(GPa)*	σ_H *(rms)*	*E(GPa)*	σ_E *(rms)*
Not irradiated #1	9	0.540	0.012	8.31	0.53
Not irradiated #2	10	0.536	0.025	8.38	0.50
Not irradiated #3	10	0.539	0.013	8.55	0.42
Neutrons irrad.	20	0.535	0.015	8.32	0.35
Protons irrad.	20	0.534	0.014	8.46	0.59

As mentioned above, the fan-ins are intended to facilitate the automatic wire bonding of the sensors to the chips. Therefore, it is very important to ensure the excellent bondability of their bonding pads. In order to guarantee this characteristic pull tests have been carried out on sample pieces from the fabricated batches. The pull tests have been performed using a *DAGE Pull Tester model 4000* with an ascending speed of 700 μm/s. This system can perform destructive tests in which the instrument pulls up from the bonding wire until the bond breaks. From the force applied by the instrument at the breaking and the height of the wire at that moment, the bond force can be calculated. An average bond force of 12 g has been obtained with this technique for wire bonds made on the sample fan-ins. The measured bond force was always well above the specified minimum pull force of 6 g for the ATLAS-SCT modules, always having wire breaks before the bond became loose.

Tape peel tests have been also performed ensuring a good adherence of both the metal traces and the passivation layer to the substrate.

Electrical tests have been performed on fabricated fan-ins in order to ensure good metal conductivity, good isolation between tracks, and low inter-strip capacitance. Resistance of the order of 30 Ω for 1 cm long, 16 μm wide tracks are obtained, with bigger than 1000 MΩ resistance between tracks separated by 15 μm. Inter-strip capacitances are in the ranges of 0.8 pF for those geometries and are constant for a wide frequency range. Metal sheet resistance has been also routinely measured through specifically designed test structures [28] obtaining values of 0.04 Ω/sq.

All fan-ins are tested for defects before being supplied. A thorough visual inspection is performed in order to assure continuity in the lines and absence of short-circuits. This quality assurance test guarantees the specified condition that all delivered fan-ins have no more than one shorted pair of neighbour strips or one broken strip.

4.3.3. Production.

The production of the fan-ins was carried out, after a selection process, in the Centro Nacional de Microelectrónica (CNM-CSIC), Barcelona, Spain. The fabrication started early in September 2002 in order to assure the availability of components for the assembly sites qualification, and to allow a through evaluation by the Collaboration.

Figure 4.10 shows the production progress during the whole period including shipments and accumulated stock. The production extended over 32 months, 1639 glasses were processed resulting in 2642 fan-in sets shipped to the module production sites, together with more than 600 dummy fan-in sets.

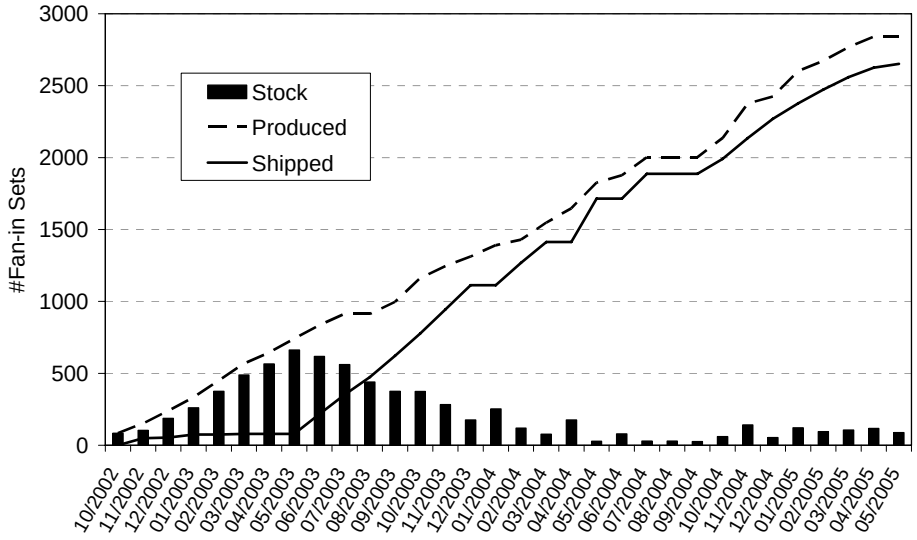

Figure 4.10. Fan-in delivery rate

The final average yield was 70% during the production selection, and a further 3% of the fan-ins were rejected by the assembly sites. An average production rate of 103 sets/month was achieved, reaching a rate of ~120 sets/month in the last period.

4.4. Spines Design, Testing and Results

The silicon sensors are glued back to back onto a support structure built from thermalised pyrolytic graphite (TPG)[29][30][31], with aluminium nitride (AlN), and aluminium oxide (Al_2O_3), ceramic parts required for mechanical considerations. This structure is known as a spine and is shown in Figure 4.11. To minimise the overall material within a module the spine must have the lowest possible mass, it must be mechanically rigid, and provide the interface for the module cooling contacts. The TPG backbone of the spine transports the heat from the sensors, which produce up to 2 W after the expected radiation dose from 10 years of ATLAS operation, to the module mounting/cooling blocks at each end which are held at around -15°C. The thermal performance of the TPG is vital to keep the sensors cold for the lifetime of the experiment. The thermal performance of the spine has been simulated using finite element calculations [18] and compared with experimental data [19]

To achieve precise tracking in the SCT the position and orientation of the individual sensors relative to the module mounting point have to be known with high accuracy and within a tight envelope, described in Section 3. The size and shape of the module in the perpendicular direction to the sensor plane is strongly dependent on the size and shape of the spine, most notably on any bow in the TPG, therefore the TPG must be kept within a tight mechanical tolerance during production.

4.4.1. Spine Design

The design of the spine is given in Figure 4.11, and in [32]. The basic structure is the 500 ± 25 μm thick TPG heat spreader with the AlN ceramic supports. The TPG functions as the thermal path between the sensors and cooling contact at each end. In order to achieve electrical insulation and mechanical protection the TPG is coated with a 10 μm layer of Parylene-C. Parylene-C was chosen because it has a low tendency to penetrate into the TPG layers during deposition. Such an effect was observed with Parylene-N which leads to an increase of the TPG thickness at the cut edges. Since TPG is fragile and tends to delaminate the structure of the spine has to be reinforced using AlN ceramic sections. AlN has a rather high thermal conductivity, of 180 W/mK at 20°C, and a similar thermal expansion coefficient to silicon, thus reducing mechanical stress during any temperature changes. AlN plates of thickness 225 ± 25 μm cover the TPG at the cooling contacts to ensure good thermal contact to the cooling points while protecting the soft TPG from mechanical damage. To maintain a spine of constant thickness the TPG is profiled at each end where the ceramic sections are glued; the glue is used to correct for any thickness variation. The hybrid end ceramic has a v-groove to enable mechanical assembly of the final module. The far-end cooling point has an oval slot to enable the sliding joint. The wings supporting the sensors and providing mechanical stiffness to the sensor-spine

assembly have a thickness of 500 ± 25 μm. The AlN pieces at the hybrid end and the central wings contain metal traces to distribute the sensor bias voltage. The bias is supplied from the hybrid to one side of the spine and therefore one of the AlN wings has metalized through hole to electrically connect both sides of the spine.

Attached to the AlN wing at the hybrid end there is an Al_2O_3 spacer required to match the thickness of the spine to the hybrid for assembly. Al_2O_3 was chosen as it has a low thermal conductivity so as to maintain the thermal break between the hybrid and the sensors. Attached to the far-end cooling point is a precision washer, constructed from FR4 and 0.5mm of aluminium, which defines the precise oval slot. The distance between the v-groove and the centre of the far-end washer's slot defines the spine length and ultimately the length of the module. The spine has been designed for ease of construction as well to supply the required high thermal functionality.

4.4.2. Materials Used in the Spine

The TPG used in the spine is an anisotropic material having both mechanical and thermal properties that, due to the planar mosaic ordering of the carbon structures, are basically constant within the plane of a substrate sheet and are significantly different in the orthogonal direction. Table 4-7 summarises the properties of the TPG, AlN and Al_2O_3 used in the construction of the spine. The ceramic data are from CERAMTEC[33], unless noted otherwise.

Table 4-7. Properties of materials used in the spine.

Property	TPG	AlN	Al_2O_3
In-plane thermal conductivity at 20°C, (W/mK)	1550 ± 130	180	20
Out of plane thermal conductivity at 20°C, (W/mK)	8.9 ± 0.4	n/a	n/a
Density, (g/cm³)	2.15 ± 0.2	3.3	3.75
Transverse pull strength, (N/cm²)	56.5 ± 14.2		
In-plane electrical conductivity, (Ω^{-1} cm^{-1})	1.63 x 104	10^{-3} to 10^{-5}	
In-plane thermal expansion coefficient at 20°C, ($°C^{-1}$)	-1.17 ± 0.15 x 10^{-6}	3.1 x 10^{-6} [7]	6.7 x 10^{-6}
Out of plane thermal expansion coefficient at 20°C, ($°C_{-1}$)	26.8 ± 0.4 x 10^{-6}	n/a	n/a

The TPG was glued to the thin AlN sheets at the cooling block connections with ELASTOSIL 137-182[34] which was chosen as it has a thermal conductivity, measured to be 1.79 ± 0.1 W/m K. This is superior to ARALDITE 2011 with 25% boron nitride filler which has a conductivity of 0.87 ± 0.06 W/m K. It also exhibits pull strengths superior to ARALDITE, with no deterioration observed after an irradiation up to a fluence 2.7 x 10^{15} 24 GeV/c protons/cm².

4.4.3. Construction Process

The TPG for the spine was produced at NIIGraphite[35]. The TPG was delivered roughly cut into plates of 145 x 25 x 0.7 mm^3 for outer and middle modules and 80 x 25 x 0.7 mm^3 for inner modules. These plates were mechanically lapped and polished into the exact thickness at NIITAP [36]. The TPG was cut to shape with laser ablation, the end profiles of the TPG were then fabricated via further grinding and polishing. The TPG was heated to 200°C for 30 min and kept for 45 minutes under vacuum to avoid later out-gassing. Finally the TPG was coated with a 10 μm layer of Parylene-C. The bias contact hole in the Parylene-C was made using plasma etching. During the processing of the TPG, rolling was used to correct any mechanical deformation. The AlN ceramic parts were laser cut and profiled at NIITAP. Conductive Al layers, which build up at the cut edge during cutting, were removed using NaOH. Afterwards the pieces were cleaned with distilled water. The metal traces were fabricated using vacuum evaporation of Ti-Cu-Ni. The total thickness of the three layers is 2 μm. The electrical resistivity was measured and kept lower than 20 Ohm between any two points of a trace. The through contact between the bias line and the backside metallization of the contact hole was also made using Ti-Cu-Ni. The Al_2O_3 spacers were cut and metalized at NIITAP using the same techniques.

The components were shipped to IHEP[37] for assembly and QA. After assembly the spines were visually inspected and the thickness of each was measured at 25 pre-defined points. The flatness was measured and

spines which were bowed by more than 1 mm were rolled flat or rejected if the bow could not be rectified. The electrical continuity of each spine was checked by measurement between the contact pads on the AlN facings and the HV openings on the TPG area. Data for each spine were stored in a local database.

The assembled spines were shipped to CERN where an IHEP technician performed a visual reception step before attaching the far-end washer to the spine with the use of special jigs. The technician performed a final QA step including the measurement of the far-end spacer position with respect to the spine's v-groove, the measurement of the Al_2O_3 spacer position with respect to the v-groove and electrical conduction measurements of the traces on the AlN ceramic sections. The spines were finally shipped by the ATLAS SCT collaboration to the module production sites. Any spines rejected by, or damaged at, the module production sites were returned to CERN, with details of the problem, where they were repaired by the IHEP technician.

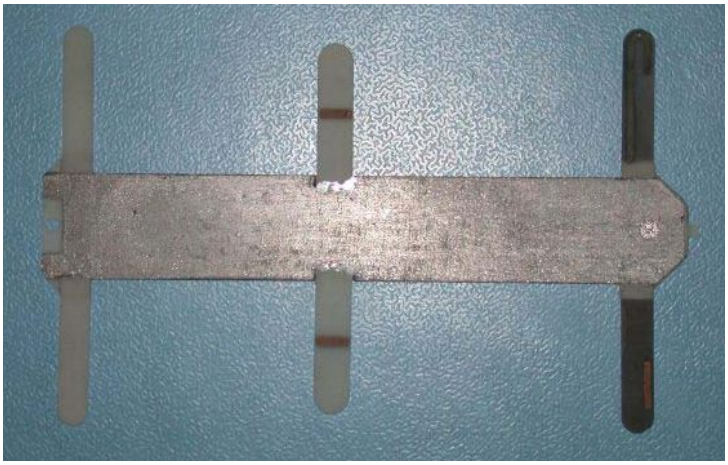

Figure 4.11. Photograph of an end-cap module spine.

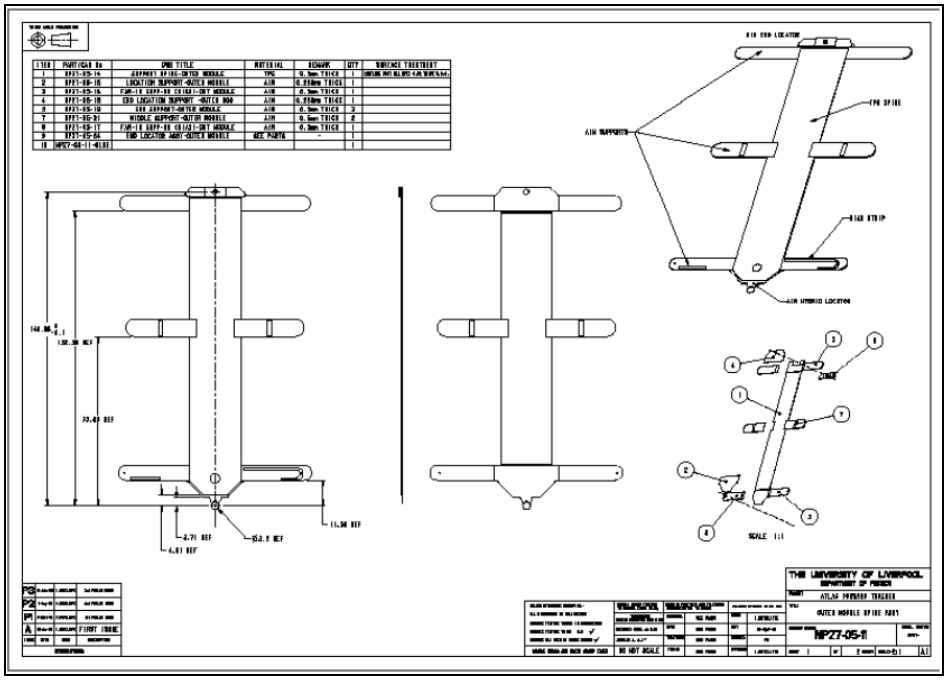

Figure 4.12. Design of the end-cap outer module spine.

4.4.4. Production.

2650 spines were shipped to CERN from the start of 2003 until April 2005. This represents an extra 12% of spines over the number of modules that were to be made during production. The final spine assembly and QA were performed at CERN and the spines were then sent onto the module production sites. The total number of spines shipped from CERN was 2505 which consisted of the spine types; outer: 1250, middle: 831, inner: 569. Figure 4.13 shows the cumulative totals. The number of spines required at the module production site was in excess of the number of modules produced by the sites due to the yield in spines, and

more importantly due to the fact that dummy and pre-production modules were also constructed by the module sites. A spine on arrival at the module production site is inspected and either accepted, marked as defective and returned to CERN for repair, or considered beyond repair and marked as trashed in the production database. In total 219 (8.7% of) spines were returned to CERN where 199 of them were successfully repaired and re-sent to production sites. The total number of trashed spines was 135 (5%)

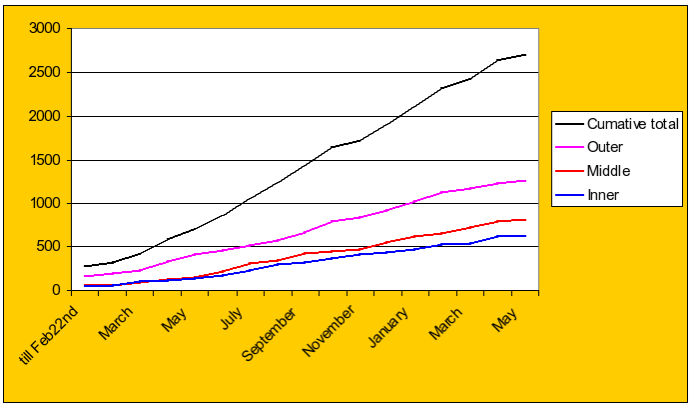

Figure 4.13. Total number of spines shipped from CERN, detailed by type and as the total

4.5. Module Descriptions in ATLAS Simulation

4.5.1. Radiation Length

We have calculated the radiation length of SCT end-cap modules, based on our knowledge of their composition and measurements of their mass [38]. First we checked the design compositions and masses of samples of the module components. All masses were consistent with expectations from design except the hybrid, which was 0.28 g heavier. This was traced to the copper layers in the flex circuit being on average about 17 μm thick, compared with the design value of 15 μm. With this correction taken into account, the individual component masses and the masses of production modules are consistent with expectation. The final radiation lengths of average production modules, estimated to be accurate to better than 1%, are shown in Table 4-8. These radiation lengths are normalised to the sensor areas of the modules in order to show the average impact of a module at normal incidence.

Table 4-8. Composition of modules, expressed as percentage of a radiation length at normal incidence

	Module type		
	Inner	Middle	Outer
Normalisation area (mm^2)	3090	7803	7893
Hybrid substrate	0.149	0.059	0.058
Hybrid flex circuit	0.595	0.236	0.233
Other hybrid components	0.477	0.189	0.187
Spine and location washers	0.388	0.226	0.243
Fan-ins and wire bonds	0.099	0.038	0.039
Sensors	0.609	0.609	0.609
Assembly glue	0.027	0.019	0.020
Total average radiation length (%)	2.345	1.375	1.388

4.5.2. Simulation

In order to simulate reliably the tracking performance of the SCT (including material effects), the modules must be properly defined in the geometry used by the simulation. The geometry and material descriptions of the SCT end-cap modules were prepared in the Athena framework for simulation in the standard ATLAS software environment. In this description, the module consists of the silicon sensors, the support structure, and the electronics hybrid populated with passive components and readout chips. A compromise between a full detailed geometrical description and a simple average mass of materials was developed, with the goal of ensuring a correct representation of the module radiation length without excessive computing time.

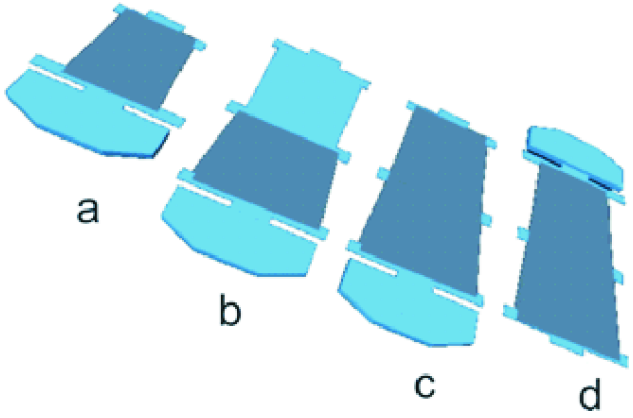

Figure 4.14. Layout of the SCT end-cap modules in the Athena framework: inner (a), short middle (b), middle (c) and outer (d).

Description of the Geometry

All four different types of modules are described in the Athena framework [Figure 4.14] and converted to a Geant4 readable format for standard simulations of propagation of particles in matter. All parameters describing modules are divided into two groups: common parameters for all types and parameters specific for each type. Furthermore, all specific parameters are sorted according to module components which they describe. Finally the parameters were written to the Detector Description database.

By comparison of the geometry in the Athena framework with calculations from real modules it was confirmed that:

- All strips are in the proper position (with precision of about 1 μm), so the contribution to the module misalignment is negligible with respect to the permitted values.
- The sensor has a dead margin where the deposited energy can be seen but, as no strip is there, no signal appears; and the dimensions of this margin correspond to the sensor layout.
- The gap between sensors on each side has the correct size.

Module Materials

The definitions of the various module materials were constrained by the requirement to minimize number and complexity of components in order to reduce the simulation computational load. Table 4-9 shows differences of real materials in each component and their setting in the Athena framework.

Table 4-9. Comparison of materials in different types of modules in real measurement and in Athena simulation framework

Summary table of materials in module (all in grams)									
Component	Material	Outer		Middle		Short Middle		Inner	
		Real	Athena	Real	Athena	Real	Athena	Real	Athena
Sensors	Silicon	10.53	10.53	10.41	10.41	10.70	10.70	4.12	4.12
Hybrid	Composite	7.66	7.66	7.66	7.66	7.66	7.66	7.66	7.66
Spine	Composite	2.81	5.74	2.64	5.49	2.64	5.49	1.33	3.86
Subspine	AlN	2.04	2.04	1.08	1.08	1.08	1.08	0.91	0.91
Others	Composite	2.93	0.00	2.85	0.00	2.85	0.00	2.53	0.00
Module		25.97	25.97	25.37	25.37	25.66	25.66	16.56	16.56

Table 4-10. . Composition of material of hybrid

Hybrid material composition		
Material	Weight [g]	% of mass
Cu	2.20	28.74
CC	1.82	23.76
Si	0.78	10.24
Kapton	0.80	10.50
Adhesive	0.74	9.67
AI203	0.41	5.31
Plastic	0.17	2.26
Sn/Pb	0.42	5.54
AIN	0.14	1.79
EotiteP102	0.10	1.28
AIT	0.04	0.46
scr. Epoxy	0.04	0.46
Hybrid	7.66	100.00

Table 4-11 Composition of then spine in the Athena framework.

Spine material composition						
	Outer		Middle		Inner	
Material	Weight [g]	% of mass	Weight [g]	% of mass	Weight [g]	% of mass
Carbon	2.81	48.94	2.64	48.15	1.33	34.37
AlN	0.87	15.11	0.87	15.76	0.85	21.96
Elastosil	0.03	0.52	0.03	0.56	0.03	0.78
Araldite	0.05	0.90	0.05	0.90	0.05	1.26
Aluminium	0.12	2.07	0.11	2.09	0.11	2.91
Araldite	0.01	0.09	0.00	0.09	0.00	0.13
FR4	0.37	6.39	0.35	6.44	0.35	8.98
Glass D263	0.87	15.14	0.84	15.26	0.82	21.27
Aluminium	0.00	0.03	0.00	0.03	0.00	0.05
Araldite	0.62	10.80	0.59	10.71	0.32	8.30
Spine	5.74	100.00	5.49	100.00	3.86	100.00

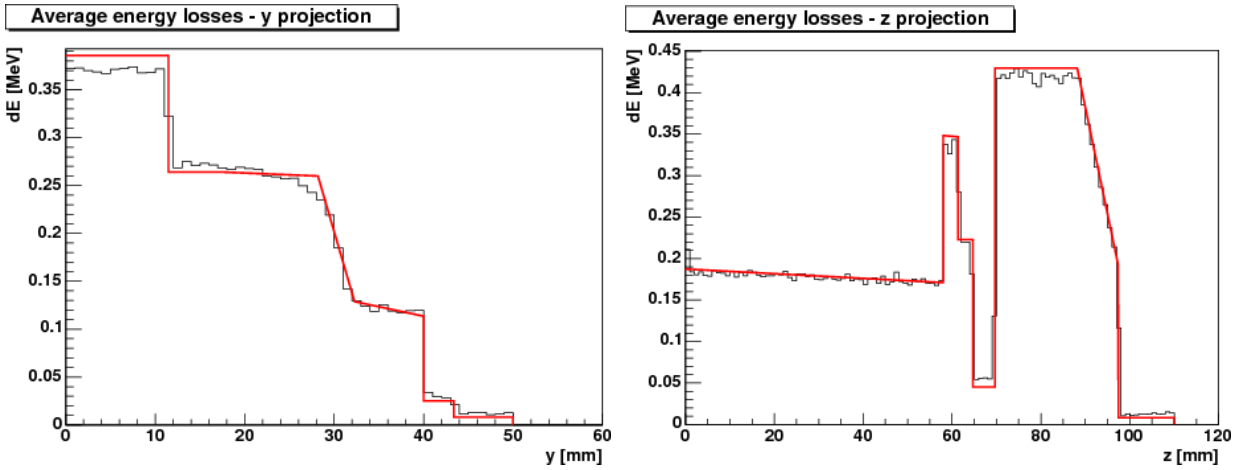

Figure 4.15. Average energy loss in the module. Histogram is Geant4 simulation. Straight lines are the theoretical prediction.

To validate the material in the model, a distribution plot of energy losses was produced by firing parallel muon beam through a simulated set-up composed of only one outer module inside a box filled by air. Two projections of the average muon energy loss versus position are shown in Figure 4.15. The theoretical predictions of the energy loss are shown by the straight lines. The measured values from the simulation correspond very well with these.

5. ATLAS End-cap Module Assembly and Testing

This section describes the detailed module specifications, outlines the assembly and quality assurance (QA) steps taken to ensure modules meet these requirements and discusses the results for all the modules produced.

On average, the whole process of assembling and testing a module took about 100 hours of which 70 hours were fully dedicated to testing the various aspects of the module. An average of 20 staff-hours were required to produce one module. Three different sets of tests could be identified: reception of module components,

tests made during assembly and, finally, the tests made on the module as a whole. All of them are fully described in [50] and will be outlined in this section.

Components arrived at module assembly sites having all passed their own quality assurance so only reception tests, aimed at catching any damage that could have occurred in transit from the QA site to the assembly site, were needed consisting, mainly, in visual inspection and confirmation that their main properties were still within the specifications. In particular, for silicon sensors an *IV* characteristic curve was measured. For spines the curvature along the TPG, and for hybrids the digital circuitry of the ASICs as well as the gain, noise and dead channels were measured.

During the assembly phase of the module, and before gluing the hybrid to the detector-spine assembly, an IV curve of each sensor was measured up to 500 V. At the end of this phase, and prior to the bonding process, all the metrology parameters were measured during the first period of the production in order to trace any mechanical deformation that could occur during the thermal cycle of the module.

Fully assembled modules were subject to thorough testing which included

- Thermal cycling: the module was cycled 10 times between -35°C to 35°C with ramp up/down times not smaller than 30 minutes and soak time of also 30 minutes.
- Full metrology survey
- IV curve.
- Long-term test and electrical and leakage current stability: the modules were kept in a controlled environment and were clocked and configured during 24h with the detectors biased at 150 V. Every hour a minimal performance test was performed consisting on the gain, noise and dead channel determination as well as the configurability of the ASICs.
- Full electrical characterization: in these tests all the analogue and digital features of the module were tested.

5.1. Mechanical Assembly Specifications

The module assembly specifications are derived from Table 2-1, where an r.m.s. accuracy of 67 µm is required in the *z* direction and 4 µm in the *r*-ϕ direction.

The thin flat shape of modules with tight *z* tolerance allows to decouple the *z* (out-of-plane) specification from the *xy* (in-plane) specification.

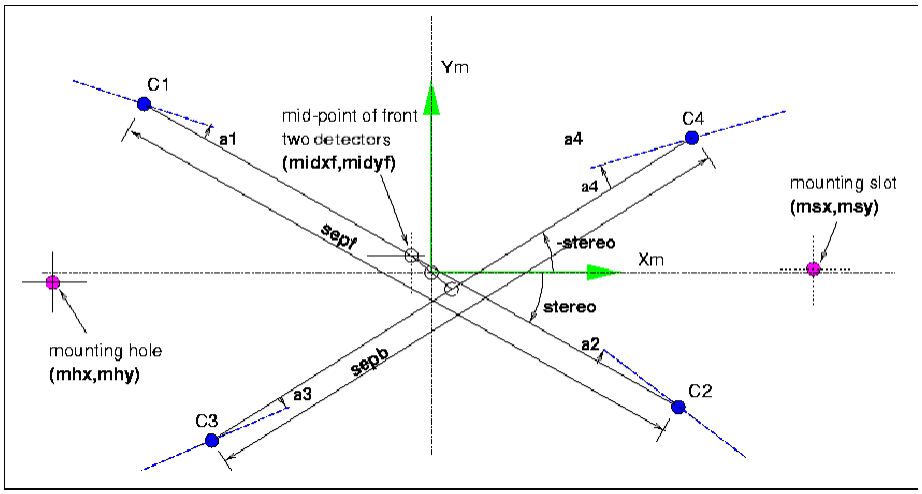

Figure 5.1 Thirteen parameters specify the geometry of an outer or middle module in the *xy* plane. The four spots (C1-C4) represent the sensor centres and dash lines the detector orientations

Figure 5.1 shows the geometry description of a module in the *xy* plane. Points *C1* to *C4* are the centres of the four detectors, determined by surveying fiducial marks on the detector corners and forming the centre-of-gravity of the four results. The module coordinate system (*Xm*,*Ym*) is defined by the centre-of-gravity of the four detector centres. The direction of the *Xm* axis is chosen so that it bisects the angle between and line joining *C1* to *C2* and a line joining *C3* to *C4*. The first parameter, *stereo*, defines the angle between *Xm* and the line joining *C1* to *C2*. The next pair of parameters, (*midxf*,*midyf*), specify the mid-point of the front pair of sensor centres (the mid-point of the back pair is at (-*midxf*,-*midyf*) by construction). *sepf*, specifies the separation between the front pair of detectors, and *sepb* that of the back pair. The angular deviation of each

detector centre line from the line joining it to its partner give the four parameters *a1* to *a4*. The remaining four parameters describe the position of the main location hole (*mhx*,*mhy*) and the far-end location slot (*msx*,*msy*). Inner and short-middle modules, having only two detectors, use a sub-set of these parameters with slightly different definitions as shown in Figure 5.2.

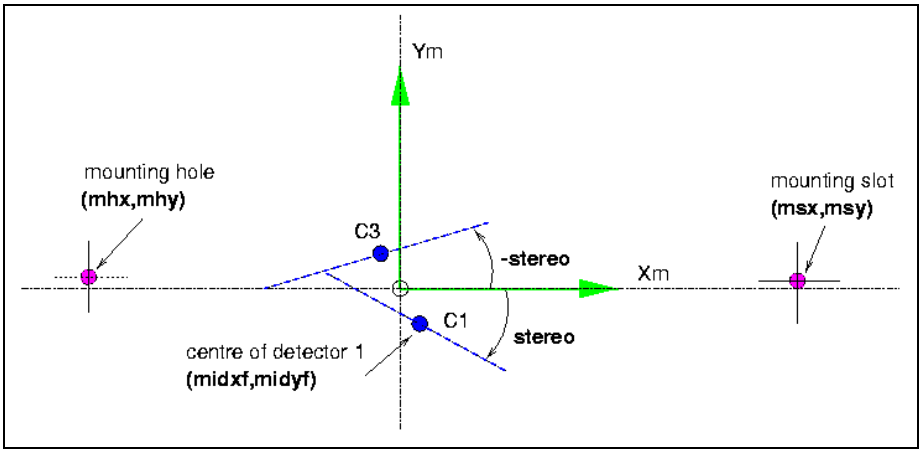

Figure 5.2 Nine parameters specify the geometry of an inner or short-middle module in the *xy* plane.

Table 5-1 shows the nominal values of these parameters for all module types and the assembly tolerances that are allowed on each parameter. The tolerances on *stereo*, *midyf* and *a1* to *a4* are chosen to just satisfy the 4 micron *r*-ϕ specification. The tolerances on *msy* and *mhy* are chosen as small as can reasonably be achieved, to minimise the loss of overlap between adjacent modules in the *r*-ϕ direction

Table 5-1. *XY* parameter values and tolerances

Parameter (unit)	Tolerance	Nominal values			
		Outer	Middle	Short-mid	Inner
mhx (mm)	0.020	-78.136	71.708	41.764	45.060
mhy (mm)	0.020	0.000	0.000	0.000	0.000
msx (mm)	0.100	62.244	-66.672	-96.616	-34.320
msy (mm)	0.020	0.000	0.000	0.000	0.000
midxf (mm)	0.010	0.000	0.000	0.000	0.000
midyf (mm)	0.005	-0.040	-0.053	-0.652	0.000
sepf, sepb (mm)	0.010	61.668	59.900	*	*
a1 - *a4* (mrad)	0.130	0.000	0.000	*	*
stereo (mrad)	0.130	-20.000	-20.000	-20.000	-20.000

The *z* tolerance is derived directly from the specification of 67 µm r.m.s. deviation from the nominal value. Assuming that the distribution of *z* values is flat within the allowed tolerance band, leads to a choice of +/- 115 µm for the tolerance. *z* is measured perpendicular from the surface on which the module is mounted, with positive *z* being towards the front face of the module.

Figure 5.3 shows the points at which the *z* value of the detector surface is measured. The open squares are at the detector corner fiducials and the filled squares are on a 5 × 5 array uniformly interpolated between the open squares. All 50 measurements (25 for short modules) on each side of the module must be within the *z* tolerances defined in Table 5-2.

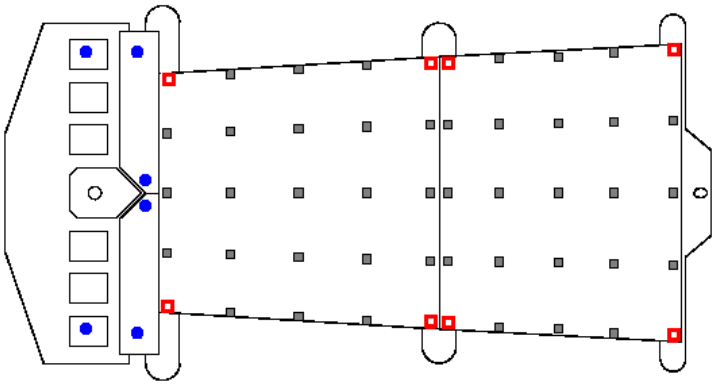

Figure 5.3 *z* survey points on an outer module.

In addition to the *z* tolerances on the detector position derived from physics, a number of other constrains stem from clearance to adjacent modules, services and the cooling block. These are shown by the circles in Figure 5.3 and their tolerances are given in Table 5-2.

Table 5-2 *Z* tolerances.

	Object	Tolerance (mm)
Front Face	Detector surface	0.875 +/- 0.115
	End chips	< 1.893
	Fan-in near end chips	< 1.751
	Fan-in near middle	< 1.751
Back Face	Detector surface	-0.375 +/- 0.115
	End chips	> -1.249
	Fan-in near end chips	> -1.057
	Fan-in near middle	> -0.857

5.2. Electrical Performance Specifications

The LHC operating conditions demand challenging electrical performance specifications for the SCT modules and the limitations [39] mainly concern the accepted noise occupancy level, the tracking efficiency, the timing and the power consumption. The most important requirements the SCT module needs to fulfil are discussed below.

5.2.1. Noise Performance

The total effective noise of the modules is the result of the combination of several factors: the front-end electronics noise, the gain spread and the offset spread. The former is the Equivalent Noise Charge (e^- ENC) for the front-end system including the silicon strip detector. It is specified to be less than 1500 e^- ENC before irradiation and 1800 e^- ENC after the specified dose of 2.14×10^{14} n_{eq}/cm^2 which includes a 50% safety factor on top of the anticipated dose. Assuming the non-ionising energy loss hypothesis, this is very roughly equivalent to 3×10^{14} protons/cm^2 at the CERN PS. The other two factors affect the channel-to-channel threshold matching which, in turn, influences the final noise occupancy. The noise hit occupancy (NO) needs to be significantly less than the real hit occupancy to ensure that it does not affect the data transmission rate, the pattern recognition and the track reconstruction. The foreseen limit of NO < 5×10^{-4} per strip requires the discrimination level in the front-end electronics to be set to 3.3 times the equivalent noise charge. To achieve this condition with an operating threshold of 1 fC, the total equivalent noise charge should never be greater than 1900 e^- ENC, including the electronics noise as well as the offset and gain spread in the chips. If the noise is higher, the operating threshold could be increased provided that it does not compromise the efficiency.

5.2.2. Tracking Efficiency

The tracking performance of a particle detector depends on the intrinsic precision and efficiency of the detector elements. In this respect we specify less than 16 dead readout channels for each module to ensure at least 99% of channels working.

5.2.3. Timing Requirements

For a correct track reconstruction, every hit has to be associated to a specific bunch crossing. For ATLAS operation, the fraction of output signals shifted to the wrong beam crossing is required to be less than 1%. This requires a time-walk of less than 16 ns, where the time-walk is defined as the maximum time variation in the crossing of the discriminator threshold at 1 fC over a signal range of 1.25 to 10 fC.

5.3. Assembly Procedures

The collaboration approach has been to build modules to meet a well-defined QA specification, rather than to specify in detail the procedures and jigs that the module assembly sites should use. This has allowed pre-existing equipment to be used, as long as each site has been able to demonstrate a consecutive run of at least 5 modules produced to all the required specifications and yields. However, the early exchange of experience when setting up -mostly with dummy components- and of tackling common problems has led to almost the same module assembly procedure, with just two main variants. Similarly, the production sites have converged on two designs of jig sets, which have a lot in common so no distinction will be made between them in this section.

The first step is to align the pairs of detectors that will make up the front and back faces of the module. A pair of detectors is placed on a pair of vacuum chucks, each of which is mounted on a compact XYΘ stage integrated with a measuring microscope. The XYΘ stages had a step size of 0.5 μm and 0.001˚, and the measuring microscope had an accuracy of ~ 1 μm over 15 cm. The detector positions were measured using fiducial marks in the aluminium layer, near the detector corners. Recognition and measurement of fiducials and movement of the stages and microscope were controlled by a LabVIEW programme, which was able to place a pair of detectors at the required position within 1 μm after a small number of iterations, taking a few minutes.

After alignment, a pair of detectors is moved to another vacuum chuck which will transfer them to their final positions on the module. The move is done by placing the transfer chuck so that it rests on or just above the pair of detectors, then switching the vacuum off at the alignment chucks and on at the transfer chuck. Viewing holes above the detector fiducials in the transfer chuck allow measurement of the detector positions after the vacuum switch; if the detectors are now misaligned by more than 2 μm the alignment and transfer steps have to be repeated, but this is not usually necessary. The *xy* position of the transfer chuck in this and later assembly steps is defined by plain contact bearings of hardened steel pressed together with a spring, giving reproducibility better than 1 μm.

Glue (Araldite 2011) is then distributed onto both sides of the spine, either in the form of a few lines or an array of dots using a simple XYZ robot and a volumetric or pressure-time dispenser. Either way, the aim is to achieve maximum coverage of glue between detectors and spine, while avoiding an excess that can squeeze out onto the front face of the detectors. A number of small spots of electrically conducting glue (Tra-duct) are added by hand to distribute the detector bias voltage from a trace on one wing of the spine to the back planes of all four detectors.

With the spine in a frame the two pairs of detectors on transfer chucks are sandwiched around it and left clamped there overnight for the glue to cure. Part of the frame is shaped like the cooling blocks that will eventually support the module. The spine is clamped onto these blocks, defining its position in the *z* direction and ensuring that it will make good contact with the real blocks. The *xy* position of the spine within the frame is controlled at the hybrid end by the V shaped groove pressed against a 3.2 mm pin and at the other end by the slot washer fitting over a 2 mm precision pin. The position of the transfer chucks in the *z* direction is set such that glue layer will be 90 μm thick if the spine and detectors have their nominal thickness. Component tolerances mean that the actual glue thickness can vary by ± 50 μm.

At this point in one variant of the assembly procedure the spine-plus-sensors assembly was tested for alignment and detector leakage current. If it failed either test the module was aborted, to avoid wasting a hybrid. The other variant was to run the two gluing steps together and have only one curing step, giving a

higher rate of production from each jig set but wasting a few percent of hybrids that could have been saved by the intermediate test.

The final step is to glue on the hybrid, fan-ins and main location washer. The hybrid is clamped against the cooling block template, to ensure that it will be coplanar with the matching surface of the spine. Its *xy* location is defined by a U shaped notch fitting against the same pin as the V tooth of the spine. A spot of conducting glue makes the detector bias contact from a tab on the hybrid to a trace on the spine. The fan-ins are held on vacuum chucks, similar to the transfer chuck but with less precision. The module is then removed from its jigs and placed in a transport frame for testing, wire-bonding and thermal cycling. The first thermal cycle could be considered as the last part of the assembly procedure because it is specified to go up to 40 C and stay there for 30 minutes to post-cure the Araldite.

5.4. Mechanical Assembly and Testing

All the institutes involved in the module construction have clean room areas for the assembly activities with a maximum of class 10000, typically with features like temperature and humidity control as well as anti-static floor and mat. Dust, metal debris or vapor oil deposition can be a problem for electrical behaviour and also for bondability. Static discharge can damage the detectors and chips. Operators had to follow basic rules, like wearing ESD cleanroom shoes and and working with mask, cap and gloves.

During the various assembly steps the modules move from one working place to a test bench or storage place for queuing into the pipe line. The internal organization of this was left to the individual institutes which put the basic information for every module onto a traveller document that was signed off at each stage. Important information like identity of components and details of wire bonding and tests were put into the SCT production database (See section 7.3). The main tests performed during the assembly are the following:

- Visual inspection after each assembly step to check for any damage or glue overflow
- IV measurements of the individual detectors after assembly and then of the whole module after wire bonding
- XYZ-metrology survey after thermal cycling.

5.4.1. Visual Inspection

The visual inspection after each assembly step allowed us to identify many problems. The most common problems and the actions taken are listed below:

Glue overflow on the edge of the silicon sensors or the fan-ins towards the bonding pads. The operator must decide if the excess of glue is a problem for the wire bonding. An IV scan of the detector may help to decide on the action to be taken.

Scratches on the silicon sensor surface or on in the fan-in strip region, which can lead to severe electrical damage. In some cases rework cannot be done, but the problem is registered in various places: traveller document, database and manuscript or electronic logbook. If a problem is detected in subsequent testing it can then be correlated to the scratch.

Mechanical damage on the ceramic cooling contact area. If cracks are identified, the ceramic pieces must not be loose. There is no possible rework in such case.

Deformed wire bonds. Rework on the wire bonder is always possible at any stage of the production.

5.4.2. IV Scans

IV characteristics may change after gluing and wire bonding and it is important to track this in the database. An excess of current after any assembly operation may occur for three reasons:

Mechanical stress induced by the detector gluing. The detectors are inherently bowed by 100 to 200 μm, and when gluing them flat using the assembly jigs they are stressed and can show higher current. The current can often increase by a factor of about 2 after the detector gluing (See Figure 5.4).

Some charges can be trapped on the surface and can induce an excess of leakage current. This type of current should decrease after several hours of biasing to the original expected value.

Conductive debris as small as few tens of μm in a specific edge region of the detector can lead to an IV breakdown. This region is located between an n+ implantation (at the same potential as the detector

backplane) and the p+ implantation of the guard ring. This region is supposed to be passivated, but it was found than the SiO2 does not always cover the aluminized edges on top of the implanted regions. When the detector is biased this region can experience a very high electric field. An edge inspection with a microscope may help to detect and then remove such debris.

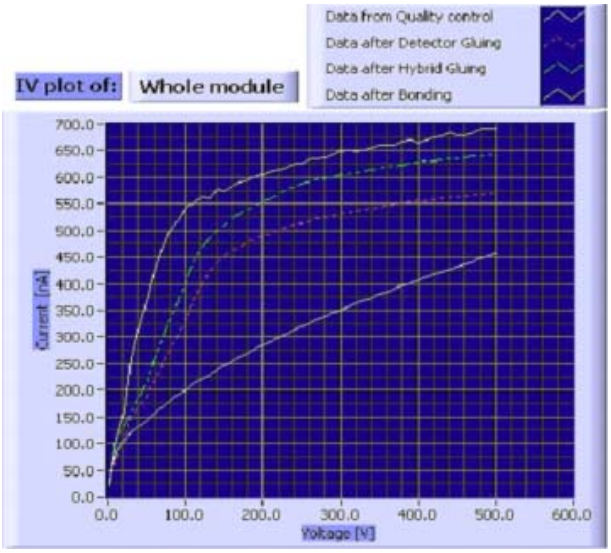

Figure 5.4: Example of IV scans up to 500V at various steps of a module assembly.

5.4.3. Module Metrology Survey

Once the module is fully assembled the *XYZ* metrology can be performed, using one of several systems. Figure 5.5 illustrates one system where a module is mounted on a frame in an optical probe Coordinate Measuring Machine (CMM).

A Labview program treats the raw data to display a set of pre-defined parameters that are uploaded into the database. Thirteen *x* and *y* parameters are extracted (see Section 5.1). From the 100 detector profile points (over the 2 sides of the modules) sixteen *z* parameters are also extracted. If any parameter is outside the tolerances a warning is displayed and the database test pass record is filled with "No". In addition some metrology is done on the chips and the fan-ins to check that the module will stay in its specified envelope given the maximum tolerance on the wire bond loop height.

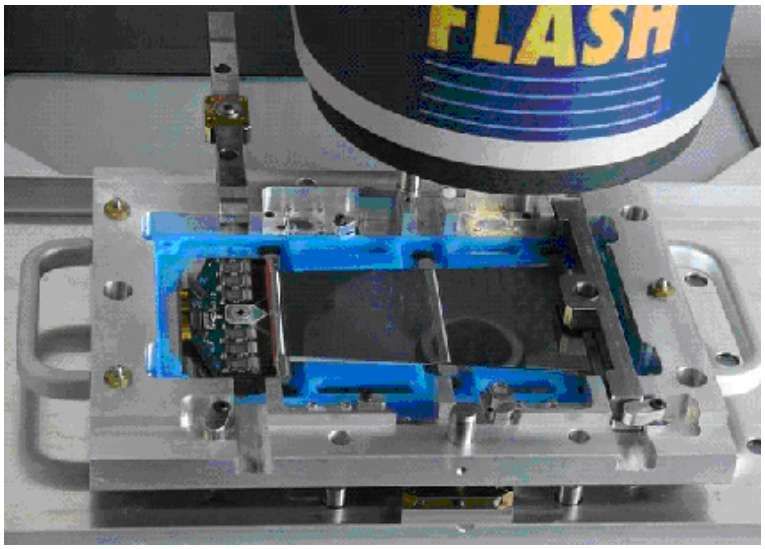

Figure 5.5: Module on a metrology frame that is located on the precision coordinate measurement system.

5.5. Electrical Test Equipment and Procedure

The tests described in this section, aim to verify the hybrid and sensor functionality after the module assembly and characterise the electrical performance of the completed module. The standard data acquisition system used to perform the electrical tests of the modules is also described.

5.5.1. Data Acquisition System (DAQ)

In some early measurements, the ABCD3TAs were powered and read out using the redundancy links, which are all electrical. This meant bypassing the optical ASICs, thereby removing the need for expensive optical interfaces and delicate optical fibres. However, there is a requirement for the optical ASICs to be tested in the module readout, as this is the primary data route in the experiment. A scheme has been devised which reads out up to six modules using the optical ASICs electrically while also testing the functionality of the module redundancy links. This system contains the following VME modules:

- CLOAC (CLOck And Control)[40]: CLOAC generates the clock, fast trigger and reset commands for the SCT modules in the absence of the timing, trigger and control system.
- SLOG (SLOw command Generator) [41]: SLOG generates slow commands for the control and configuration of SCT front-end chips for up to 6 modules. It fans out clock and fast commands from an external source (CLOAC). Alternatively an internal clock may be selected, allowing SLOG to generate clock and commands in stand-alone mode. When the SLOG runs in stand-alone mode, the CLOAC is not used in the set-up.
- AERO (ATLAS End-cap Read-Out) [42]: One AERO card provides an electrical interface for up to 6 end-cap modules. Data communication to and from the modules is via their onboard optical ASICs - DORIC4A and VDC (data receiver and transmitter respectively). AERO encodes the module Clock and Command signals onto a single BPM carrier signal for transmission to DORIC4A. The two module data links are transmitted back to AERO via the VDC and then routed to MuSTARD. Configuration of the channel allows the module to be read out using either the primary (optical) or redundant data routes.
- MuSTARD (Multichannel Semiconductor Tracker ABCD Readout Device) [43]: MuSTARD receives, stores and decodes the data from multiple SCT modules. Up to 12 data streams (six modules) can be read out from one MuSTARD card.
- SCTHV [44]: A prototype high voltage unit providing detector bias to four SCT modules.
- SCTLV [45]: A custom-designed low voltage power supply for two SCT modules.

A module 'patch card' (see Figure 5.6) is also required to interface a single AERO channel to a module. The connections to AERO are made via two standard ethernet category 5(E) screened cables, allowing separation of the primary and redundant data routes onto the individual balanced cables. Using screened twisted pair cables and differential signals should result in a system with low electromagnetic interference and good immunity to external noise.

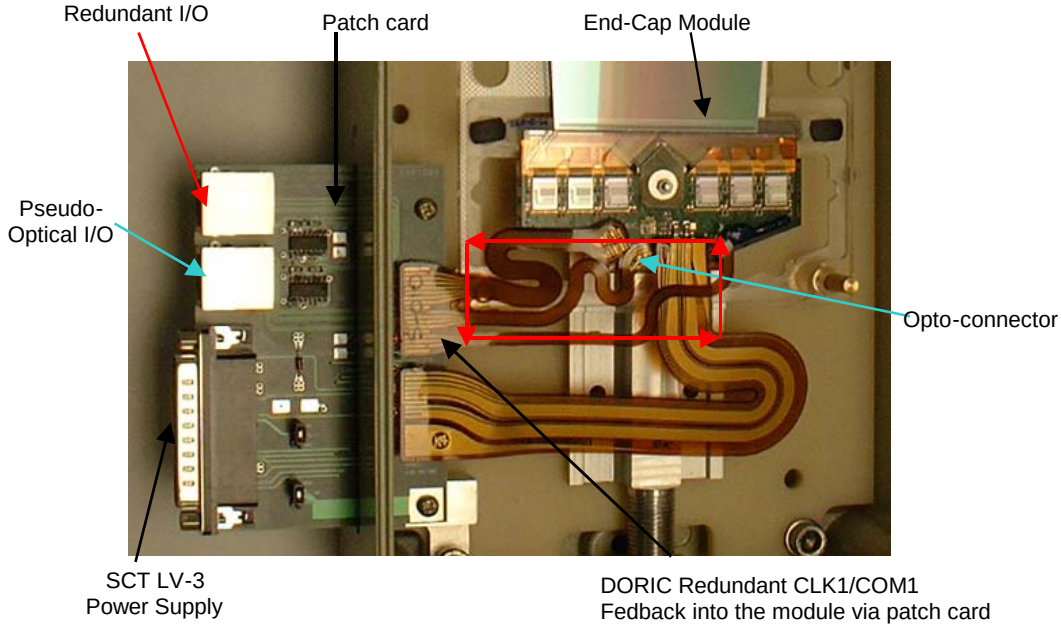

Figure 5.6. Photograph of a patch card linked to an end-cap module.

The AERO card provides three readout modes, sketched in Figure 5.7, for testing a module or hybrid, as follows:

- Primary mode: The module is configured and read out via the Opto Chips DORIC4A and VDC
- VDC Bypass test mode: The module is configured via the DORIC4A outputs CLK/COM and the module data is read out via the Master ABCD3TAs. This scheme is used so that the VDC is bypassed for data transmission from the module whilst retaining the DORIC4A for module configuration.
- Redundancy Mode: The module is configured via the Redundant CLK1/COM1 provided from SLOG and the module data is read out via the Master ABCD3TAs.

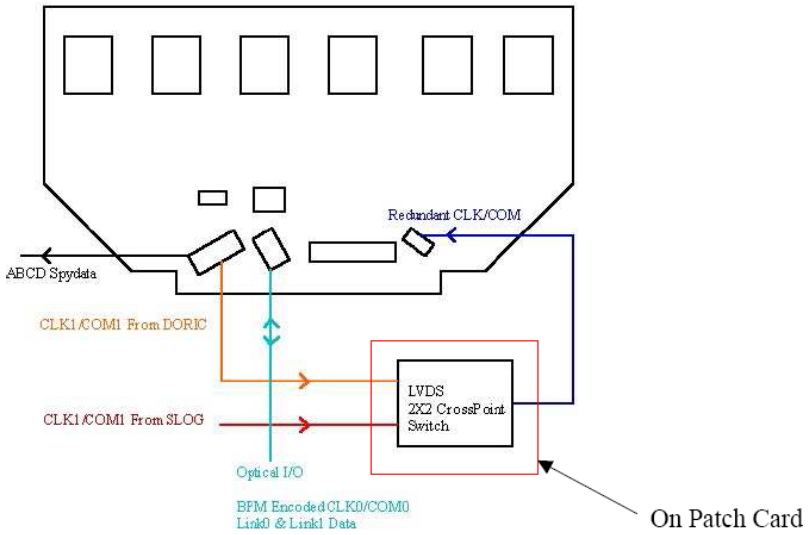

Figure 5.7. Module readout modes.

The SCTDAQ [46] software package has been developed for testing both the bare hybrids and the modules using the VME units described above. SCTDAQ consists of a C++ dynamically linked library and a set of ROOT [47] macros which analyze the raw data obtained in each test and store the results in a database. A schematic diagram of SCTDAQ is shown in Figure 5.8

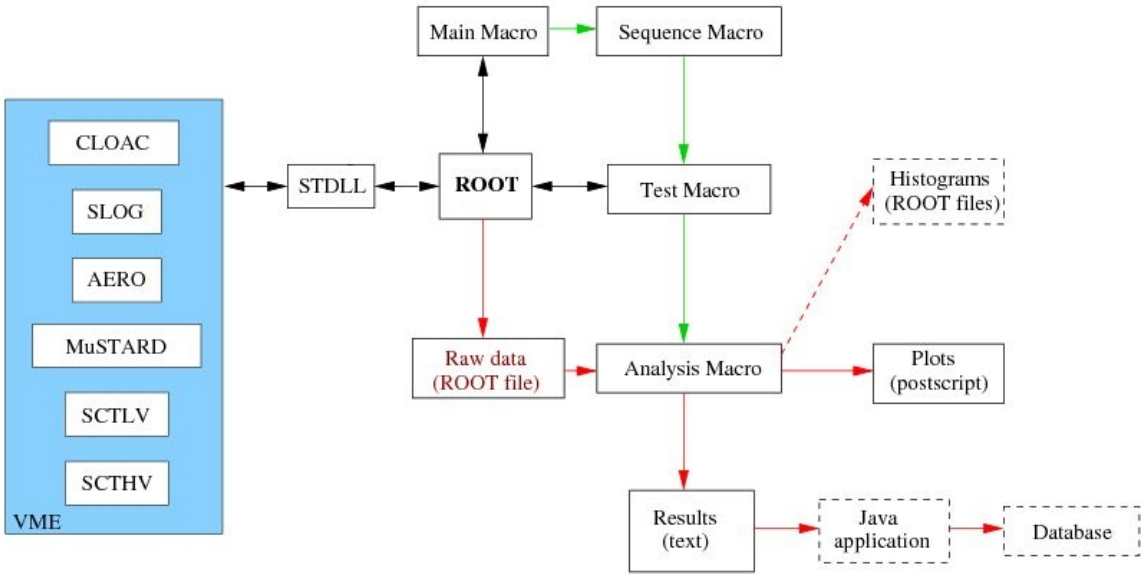

Figure 5.8. Schematic diagram of the SCTDAQ system

5.5.2. Electrical Tests

After the thermal cycling, the module is placed inside a light-tight aluminium test box where it is supported at the two cooling blocks of the spine. The test box provides dry-air flow and cooling through a channel connected to an adjustable liquid coolant system (Figure 5.9). Up to six modules in their test boxes are

placed inside an environmental chamber and tested simultaneously. Careful optimization of the grounding and shielding scheme is necessary.

Figure 5.9. Photo of an outer end-cap module supported by its transport frame inside its aluminium test box. The dry-air and coolant inlets are visible, as well as the support card.

Every module is electrically characterized with the temperature on the hybrid, measured by an integrated thermistor, at (10±5) ºC. Using the internal calibration circuit of the ABCD3TA chips to inject charge of adjustable amplitude in the preamplifier of each channel, the front-end parameters such as gain, noise and channel-to-channel threshold spread are measured. The characterization sequence[48] includes the following steps:

- Digital tests are executed to identify chip or hybrid malfunction. These include tests of the redundancy links, the chip by-pass functionality and the 128-cell pipeline circuit
- Optimization of the delay between calibration signal and clock (strobe delay) is performed on a chip-to-chip basis
- The channel by channel gain and electronic noise are measured by analysing S-curves obtained through repeated threshold scans performed for ten different values of injected charge, ranging from 0.5 to 8 fC (Response Curve procedure, see Figure 5.10). For each injected charge the threshold is scanned and the occupancy is fitted with a complementary error function. The value of the threshold in mV corresponding to 50% occupancy is the *vt50* parameter. The gain and offset are deduced from the correlation of the voltage output in mV versus the injected charge in fC. The input noise is given by dividing the output noise by the measured gain.
- To minimize the impact of the threshold non-uniformity across the channels on the noise occupancy, the ABCD3TA allows one to adjust the discriminator offset using a digital-to-analogue converter (Trim DAC) per channel with four selectable ranges (common for each chip). This trimming procedure is important due to the increase of the offset spread with radiation dose. The effect of trimming on the threshold uniformity is evident by comparing the first plot of Figure 5.10 with Figure 5.11
- A threshold scan without any charge injection is performed to obtain a direct measurement of the noise occupancy (NO) at a threshold of 1 fC. NO is the probability for a channel to produce a hit for a certain event due to noise (Figure 5.12). Trimmed discriminator offsets are applied to ensure a uniform measurement across the channels. It is expected that the SCT modules will operate at a threshold set to 1 fC ENC, or slightly higher after heavy irradiation. This value is chosen to minimize noise occupancy while retaining a high signal sensitivity.
- A dedicated scan is also executed to determine the time-walk. Setting the discriminator threshold to 1 fC for each value of injected charge ranging from 1.25 to 10 fC a complementary error function is fitted to the falling edge of a plot of efficiency versus strobe delay to determine the 50%-efficiency point. The time-walk is given by the difference between delays calculated for a 1.25-fC and for a 10-fC injected charge.

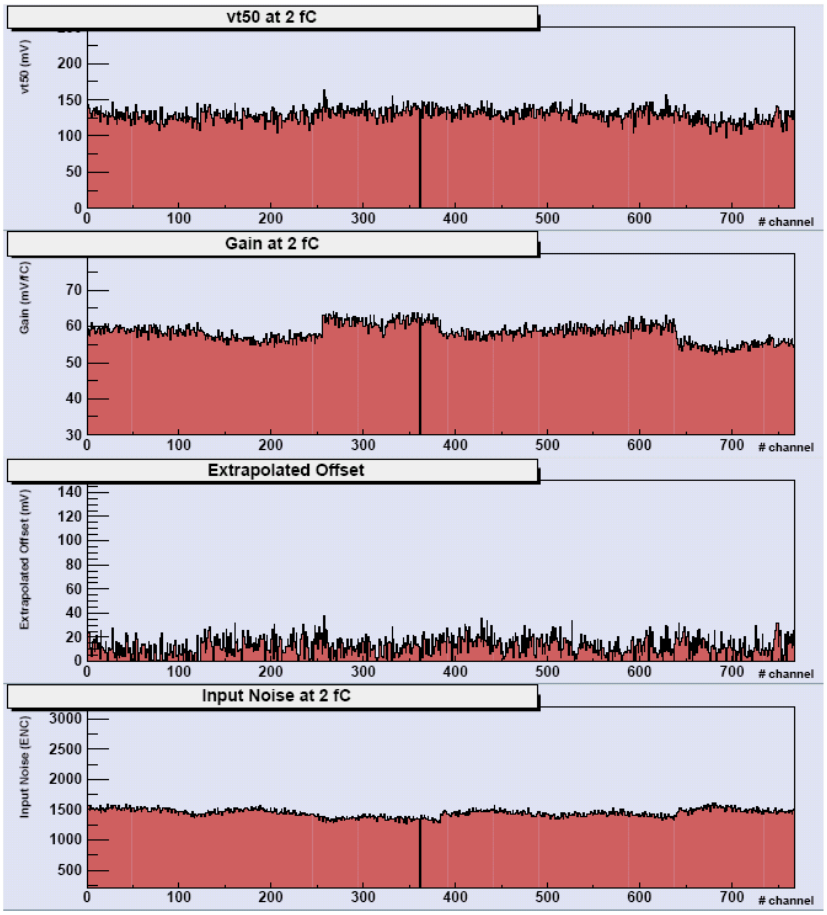

Figure 5.10. Typical set of plots obtained with the Response Curve procedure before trimming for one data steam, corresponding to six chips (768 channels). From top to the bottom the *vt50* value, the gain, the offset and the input noise are shown for each channel. The empty channels are the small number of dead channels.

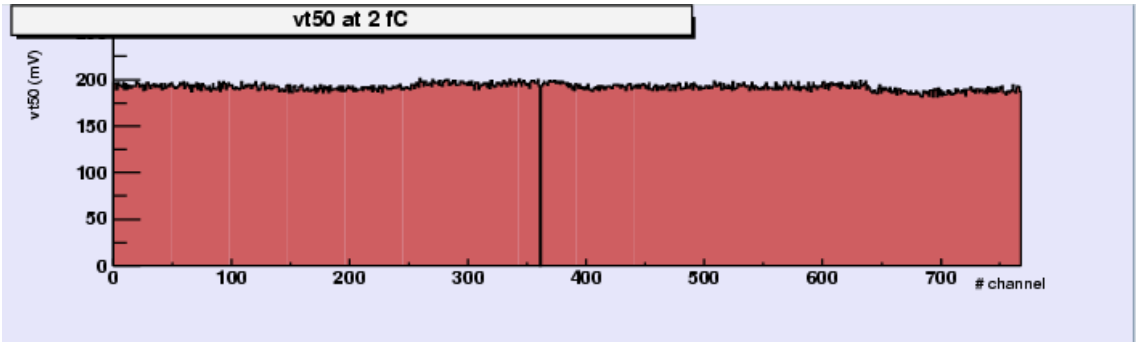

Figure 5.11. The *vt50* value after trimming for the same module as in Figure 5.10

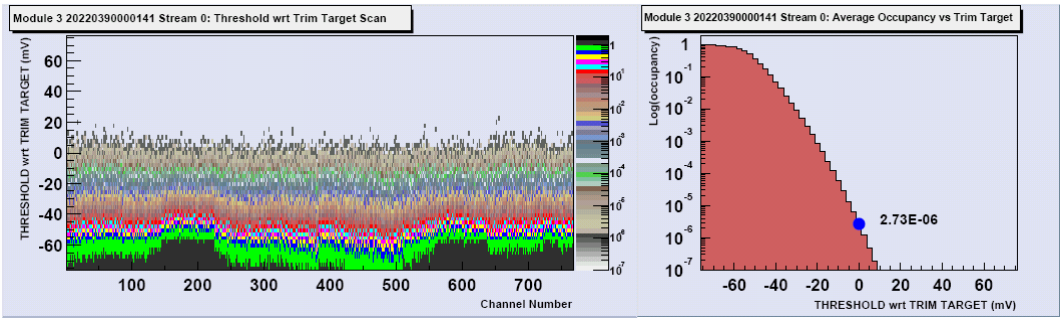

Figure 5.12. Noise occupancy, at 1 fC threshold, plot for one data stream: occupancy vs. channel number and vs. threshold (left); average occupancy for the stream vs. threshold (right). The threshold is expressed with respect to the 1-fC point (0 mV) as determined during the trimming procedure.

A long-term test with electrical readout is performed to confirm each module's long term electrical and leakage current stability at low temperature. The ASICs are powered, clocked and triggered during at least

18 hours while the sensor bias voltage is 150 V and the temperature measured by the hybrid thermistor is (10±5) ºC. The bias voltage, chip currents, hybrid temperature and the leakage current are recorded every 15 min. Every two hours a test is performed to verify module functionality and measure the noise occupancy (Figure 5.13).

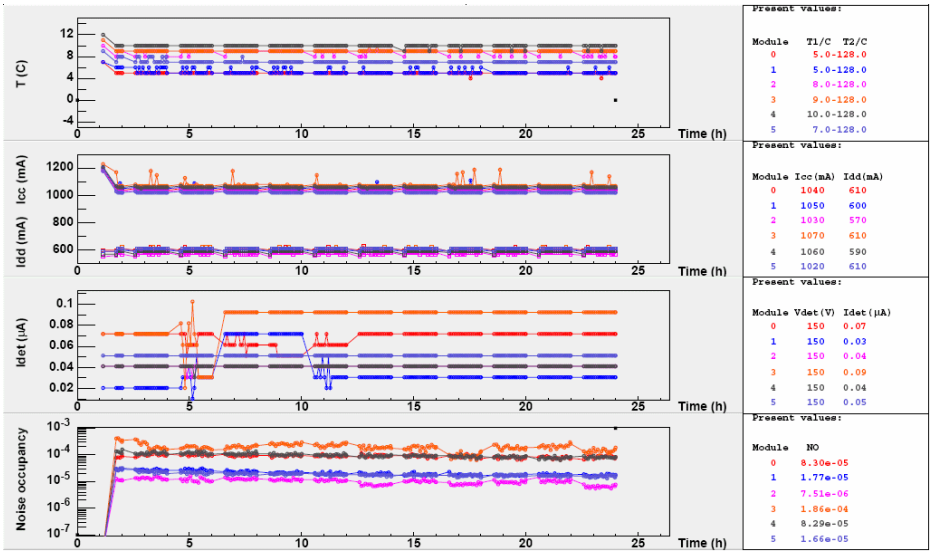

Figure 5.13. Long-term test results for six modules showing from top to bottom: hybrid temperature; analog (I_{cc}}) and digital (I_{dd}) current; detector leakage current (I_{det}); and noise occupancy as a function of time.

A final IV scan is performed at 20 ºC and the current values at 150, 350 and 500 V are recorded and compared with measurements before and after the module assembly.

All the results are uploaded to the SCT production database.

5.6. Overview of Performance

5.6.1. Result From Tests During Construction

A total of 2380 module were assembled and their main performance parameters measured and compared to the nominal values in order to ascertain the usability of the module. As already mentioned, mechanical and electrical properties were the main issues checked during the production process.

Figure 5.14 left shows the deviation of the *xy* metrology parameters from their nominal values normalized to their tolerances. The vast majority of the modules were within mechanical specifications. From the figure, one can see that one of the most critical parameters was *midyf* but, still, only a small fraction of the modules had to be rejected because of that parameter being out of specifications. Figure 5.14 right shows the *z* metrology parameters of all the modules. The picture shows that for some modules there were some regions (the *max*, *min* and *rms* parameters) out of specifications but, in general, the average values were well centred in the nominal values.

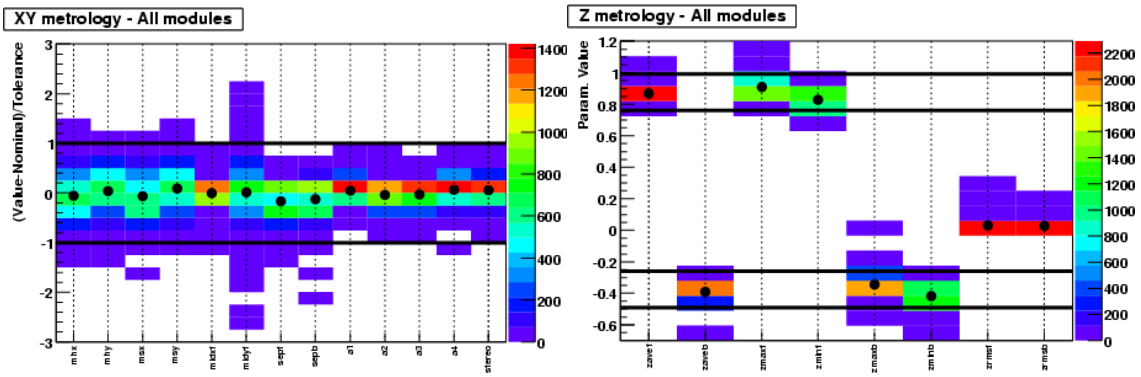

Figure 5.14 Deviation from nominal values, normalized to the tolerance, of the *xy* and *z* metrology parameters. The black dots show the average value and the colour scale the number of modules with a given deviation. The thick horizontal lines represent the tolerances.

Of the total module production, about 3% are out of *xy* tolerance and about 2.6% are out of *z* tolerance. However, some of these fall into a 'PASS' category, and are still usable, as detailed in Section 6.4.

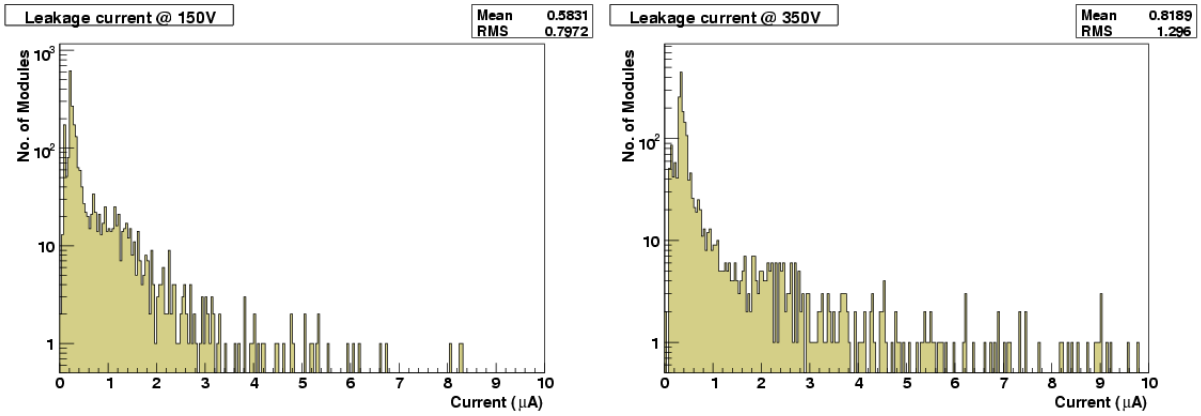

Figure 5.15. Leakage current in μA for all the modules.

Similarly, Figure 5.15 shows the leakage current distribution of all the modules, regardless of the strip length. Only about 1.4% of the modules failed the IV test irrecoverably and had to be rejected.

Figure 5.16 shows both the noise occupancy and the electronics noise as measured in the electric tests of the modules. The noise occupancy is well below the upper limit in the specifications and the noise figure shows how the modules cluster according to the sensor length.

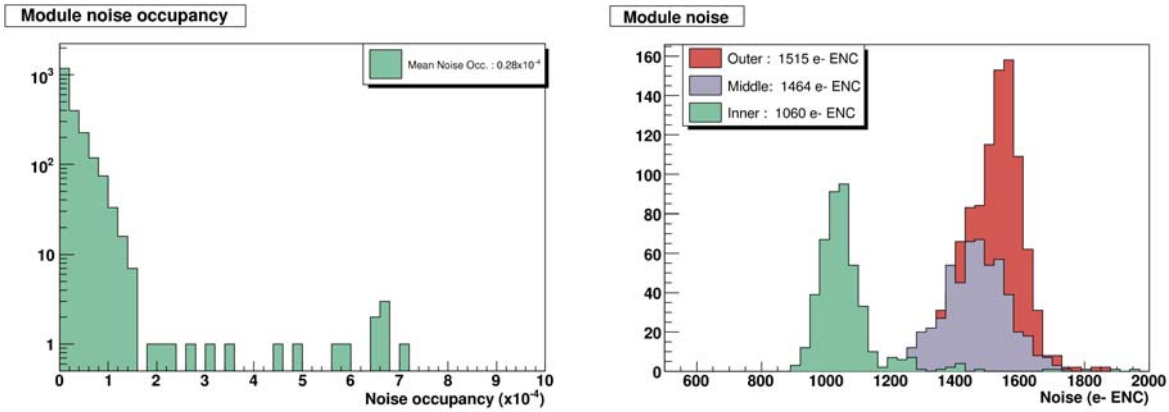

Figure 5.16. Noise occupancy at 1 fC threshold (left) and noise of the modules (right).

Figure 5.17 shows the number of bad channels. On average, after module assembly, one finds about 3 more dead channels than were found when measuring the bare hybrid. This excess contains both the sensor defects and the channels lost during the assembly process. Further information on electrical tests results of production modules is available in [49].

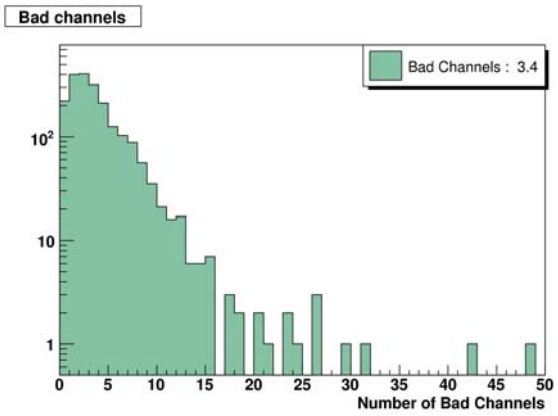

Figure 5.17. Number of bad channels.

Table 5-3 summarises the failure modes of the production modules. Overall, only 7% of the production modules were rejected. Some modules failed in more than one way.

Table 5-3. Failure modes of rejected modules

TEST	MODULES REJECTED
VISUAL INSPECTION	2.5%
IV	1.4%
ELECTRICAL	3.9%
XY SURVEY	1.2%
Z SURVEY	0.6%

5.6.2. Tests in Particle Beams

In addition to the tests made in the construction phase, a set of prototype modules were used in beam tests at the CERN SPS and KEK accelerators. Unirradiated and irradiated modules were tested in a beam of high energy particles.

The hit detection efficiency as a function of threshold set is displayed at Figure 5.18.

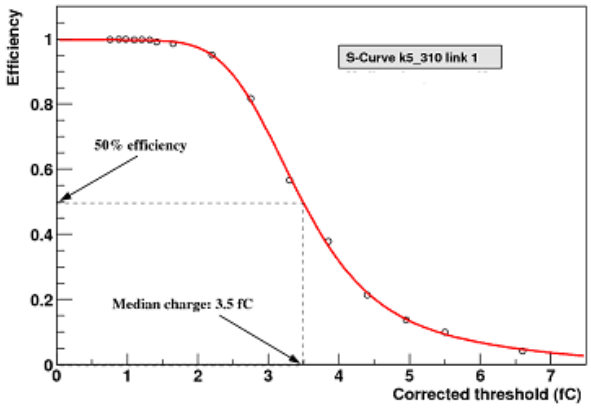

Figure 5.18. S-curve, measured with particle tracks.

From this plot the median of the charge collection distribution can be determined. It corresponds to the 50% efficiency point as shown in the plot. The average median charge of unirradiated end-cap modules is (3.5+/-0.1) fC.

The main parameters driving the performance of a binary system are the noise occupancy, which should be low, and the efficiency, which must be as high as possible. Unfortunately, they are correlated and the optimal settings are a trade-off between the two. This is shown in the expanded plot around the nominal threshold of 1 fC shown in Figure 5.19 for unirradiated and irradiated end-cap modules.

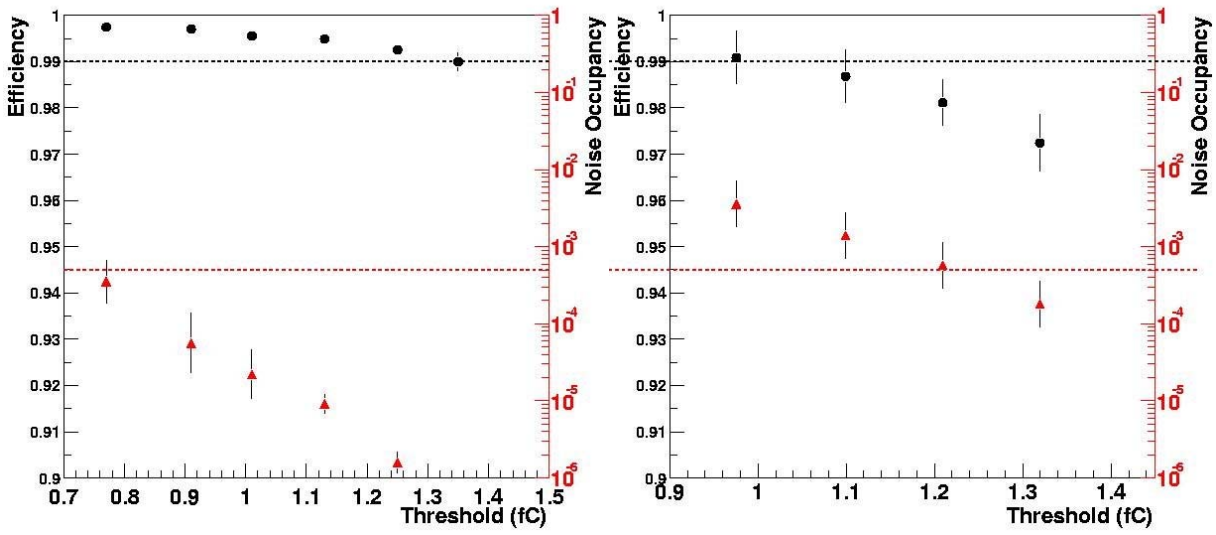

Figure 5.19. Efficiency and noise occupancy for unirradiated modules (left) and irradiated modules (right)

Before irradiation the efficiency is higher than the nominal value, shown by a dashed line, over a wide range of operating thresholds while the occupancy is within specifications. In the case of irradiated modules, however, the range of thresholds for which both the efficiency and the noise occupancy are within the specification is narrower and one needs to operate with a threshold greater than 1 fC

Signal-to-noise figures after irradiation are shown in Figure 5.20 as a function of bias voltage. The value of the signal is that of the median, instead of the peak of the charge distribution.

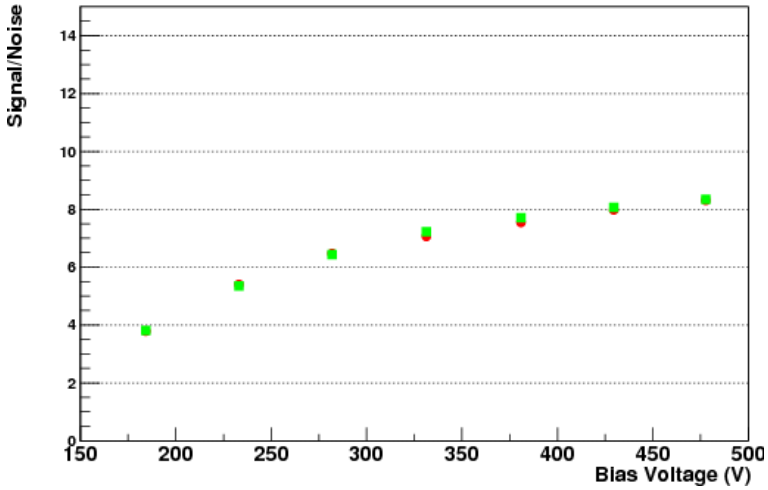

Figure 5.20 Signal over noise as a function of the sensor bias voltage

Figure 5.21 shows residuals of the space point reconstructed on a single irradiated module with respect to the interpolation from the beam telescope measurements (both in precise (y) and less precise (x) coordinate). The resulting y spatial resolution corresponds well to the 23 µm theoretical limit for the binary readout

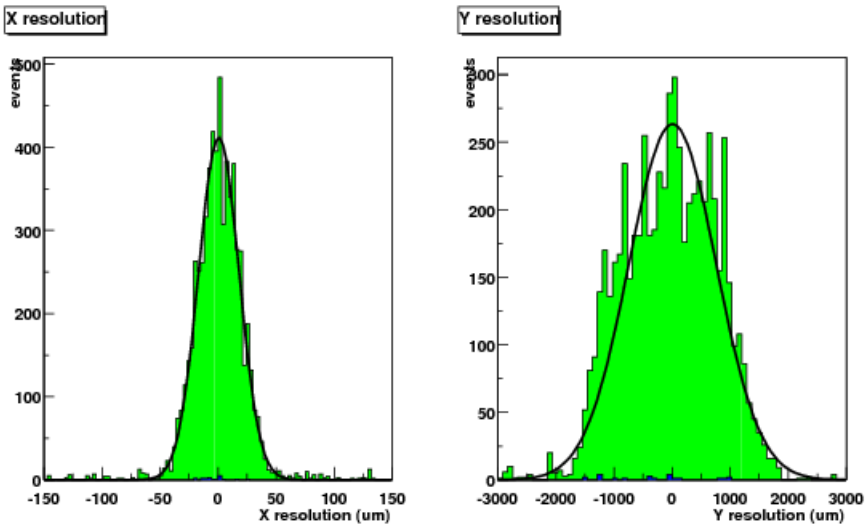

Figure 5.21.Residuals

Detailed description of the testing methods and results achieved can be found at [51] and [52]

6. Overview of ATLAS End-cap Module Production Organization

6.1. Distribution of Tasks and Flow of Components

The basic components for the module were the ASIC and fully equipped hybrids, the fan-ins, the spines and the sensors. Other items were supplied by one institution to all such as the glue and the electrical test boxes (Valencia), the test read-out kaptons (Geneva) the washers (Manchester), the module boxes (Liverpool) and the transport boxes (Prague, Charles). The fan-ins were produced by CNM Barcelona and also supplied via CERN to all module assembly sites. The spines were produced under the control of IHEP Protvino and provided to CERN where washer mounting, spine testing and distribution were organised by Glasgow and

Protvino personnel. Hybrids produced in industry under the control of Freiburg, were distributed to Freiburg, Krakow and RAL for testing before being forwarded to the module assembly sites.

The end-cap module production organised itself into three assembly lines to optimise the use of the available personnel and expertise. The diagram of component and module flow is displayed in Figure 6.1. Hybrids tested by Krakow were forwarded to Geneva and Melbourne. Those at Geneva were assembled into outer modules, wire bonded and tested for mechanical accuracy (both before and after thermal cycling) and for basic electrical functionality. They were then forwarded to CERN for full electrical testing including the long-term tests. Those at Melbourne underwent full assembly into outer modules and in-house testing. The modules were finally packaged and sent to the disk assembly sites at Liverpool and NIKHEF. The Hamamatsu sensors for these modules were nearly all tested at Prague AS CR but with some, for extra modules, tested at Lancaster.

Hybrids tested at Freiburg were forwarded to NIKHEF and MPI Munich. In the former case they were assembled into inner modules with CiS sensor measured by MPI and fully electrically tested at NIKHEF. In the latter case, they were assembled into middle modules with CiS sensors at Munich and checked for metrology and basic electrical functionality there. The modules went through their complete electrical quality assurance in Prague at both the Charles and Czech Technical Universities. Freiburg also assembled completely tested inner modules using both CiS and Hamamatsu sensors, mostly tested at MPI but with some, for additional modules, from Lancaster.

The RAL hybrids went to Manchester and Valencia. At Manchester they were mechanically assembled and checked for metrology using sensor sets tested by both Lancaster and Sheffield for all three module types. Only Hamamatsu sensors were used at Manchester. The wire bonding and electrical testing were carried out at Glasgow and Liverpool, with Liverpool completing the thermal cycling and final metrology before assembly to disk. Valencia used mostly Hamamatsu sensors tested by themselves to make complete and tested outer and middle modules. They also constructed additional middle modules using sensors tested by Lancaster.

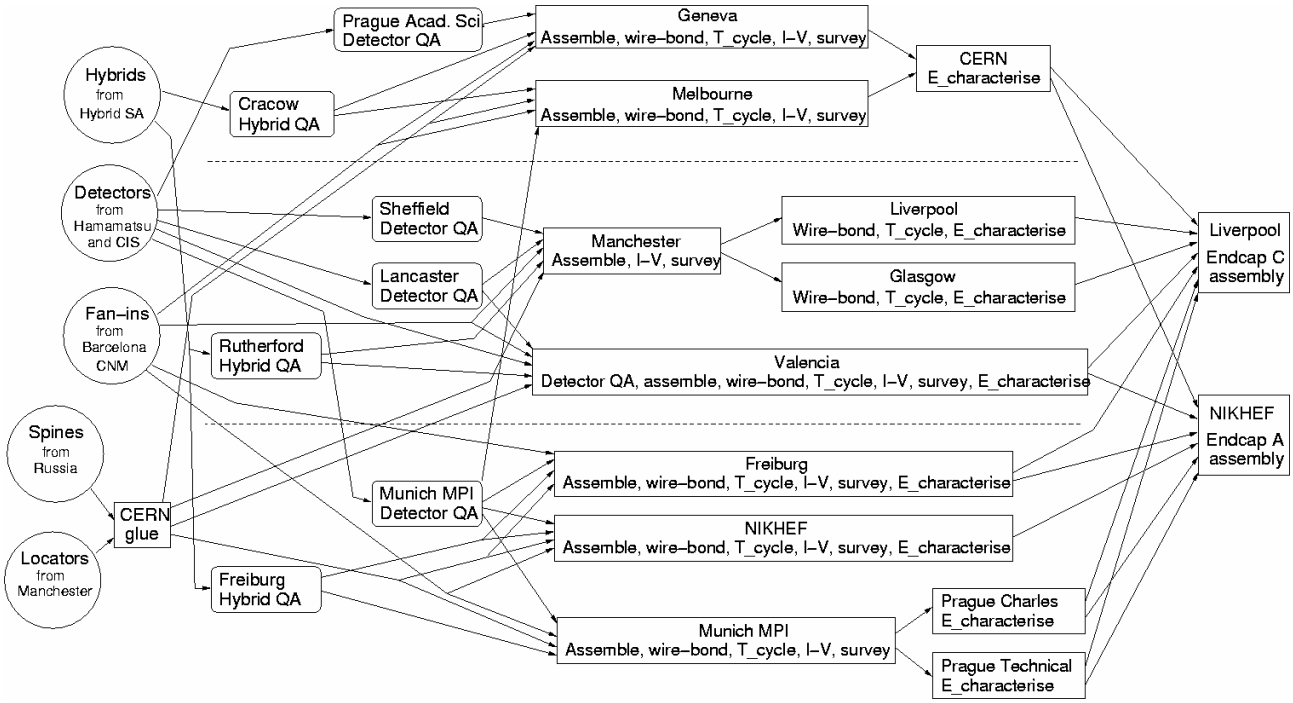

Figure 6.1. Diagram of SCT end-cap production organisation

6.2. Quality Assurance Organization

ATLAS SCT is required to deliver high performance in a very harsh environment with effectively no access after installation. A quality assurance (QA) plan [50] was therefore agreed at an early stage of the project.

QA was realised in three stages of the project:

6.2.1. Design

All components were extensively prototyped and their performance was evaluated before and after irradiation to the expected dose [6][13][25]. Module prototypes were shown to have the required electrical [25] mechanical and thermal [18][19] properties, and to work with the required precision and efficiency in particle beams [52] even when fully irradiated

6.2.2. Site Qualification

All sites taking part in module production were subject to a thorough qualification procedure, where all aspects of production and testing were reviewed, including documentation, cleanliness, ESD safety, component traceability and accountability, etc. Each production line was required to produce at least 5 modules fully within specifications. Modules were exchanged between sites to ensure uniform quality and comparability of measurements.

6.2.3. Production Quality Control

The tests each module was required to pass are described in Section 5. Each module and its components were tracked through their history by means of the SCT production database (DB). This meant that details of tests, component trees, movements between sites and overall status of modules were available to the whole collaboration, and fostered a culture of transparency. The DB also allowed easy monitoring of site production statistics and component supplies [53].

Additionally, the full raw test data is archived at each test site, together with traveller documents, check sheets and high resolution optical scans of assembled modules.

6.3. SCT Production Database

The complexity of the SCT project prompted the development of a relational database (DB) [54][55][56] to manage it. The DB and most of the features needed were already working when the module production started. The architecture for the ATLAS-SCT database is based on the client-server model, with a main Oracle (kernel 9i) application server at the University of Geneva. Access is granted from client machines communicating over the network, either by means of dedicated programs to monitor particular aspects of the production, through specialized applications for massive data upload or with the help of a WWW portal developed in Geneva [57] (See Figure 6.2). The access is secure and an institute-based authentication mechanism has been implemented.

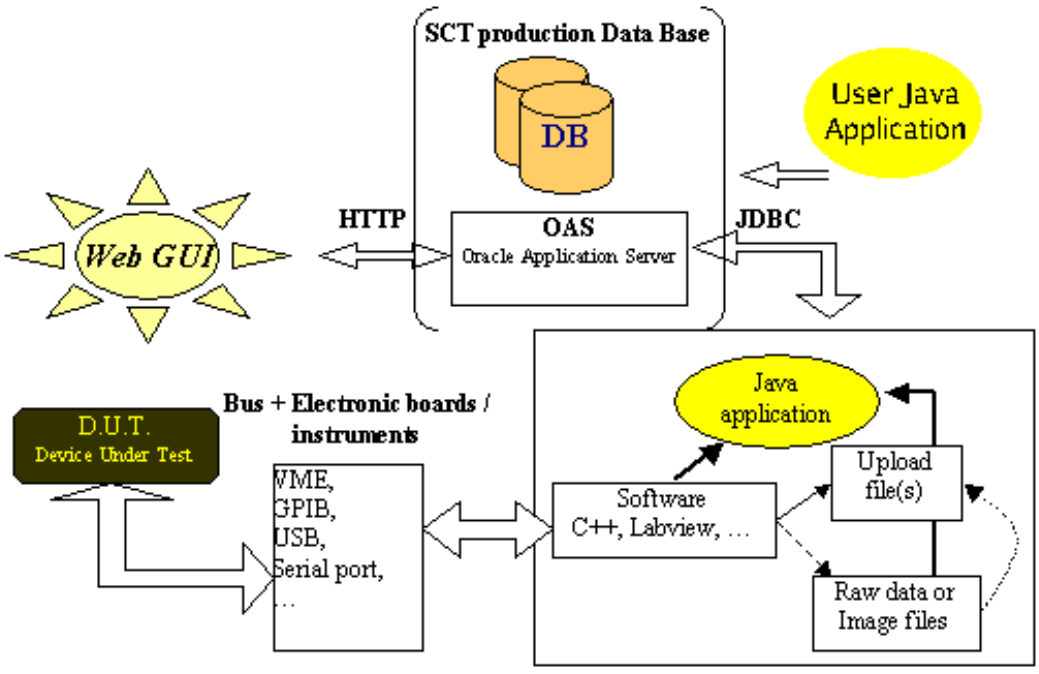

Figure 6.2. User access scheme for recording the data into the SCT production DB

The data in the database is organized hierarchically starting from the building blocks, *items*, that group into the so called *assemblies*, which in turn can be assembled to form bigger *assemblies*. Every object has associated a unique identifier and some specific fields. Associated with those objects is a data structure containing the list of tests, together with their results, performed on each item of the *assembly*. The database allowed one to also store the location of any of the *items*, together with the so called *shipments*, so that one could always trace back the origin of any module or module component, as well as component availability.

The database has proven to be an excellent tool to monitor the location, the assembly and QA progress of the module production. In particular it allowed to pinpoint possible problems in the supply of components, monitor and to optimize the production.

6.4. Acceptance Criteria and Selection for Assembly to Disks

Modules were selected for assembly to disks according to an agreed set of criteria [60] based on test results stored in the production database. Each grouping of production sites was responsible for evaluating the quality if its modules and placing them into four categories:

- Good: Pass all acceptance tests.
- Pass: Fails one test, but within 'pass' tolerance.
- Hold/Rework: Outside 'pass' tolerance. May be usable if reworked.
- Fail: Too bad to use, but stored safely.

The mechanical tolerances (Table 5-1 and Table 5-2) were originally set more tightly than required by spatial resolution requirements alone. In the light of experience we created a set of 'pass' tolerances for some parameters which were 50 % wider. Modules with one parameter (or two Z parameters) in this 'pass' band are assigned to the Pass category. The RMS of the detector alignment distributions are still well within the spatial resolution requirements even when Pass modules are included, so there will be no effect on physics performance. For Good + Pass modules, the distribution of *midyf*, the most sensitive alignment parameter, has an RMS of 2.0 μm, well within the target of 4 μm.

'Good' and 'pass' modules could be used anywhere in the end cap; there was no selection for more or less demanding locations. Disk assembly went on in parallel with module production, and some fine tuning was done to allow for projected module yield while always preserving quality.

7. Conclusion

The production of the ATLAS SCT modules has been a successful, long and complex process that needed about 24 months for completion. The production was planned with a contingency of 20% allowing for losses of 15% during module assembly and a further 5% when mounting modules on disks. More than 2350 SCT end-cap modules have been built with a yield of 93%, despite the complexity of the design and the tight mechanical specifications. 14 institutes with a wide geographical spread have participated in the process in a remarkably collaborative way which has been key to this success.

The production had two different phases. In a first phase, the different sites had to undergo a pre-qualification process in order to ensure that production tooling and procedures were in place to produce modules reliably within specifications. In order to exercise and test the procedures the production sites were supplied with second grade components. The full qualification process, however, was made with production grade components and was also intended as a short ramp-up to production. The delivery of components for the qualification also followed as close as possible the production procedures in order to exercise and find the weaknesses of the component distribution.

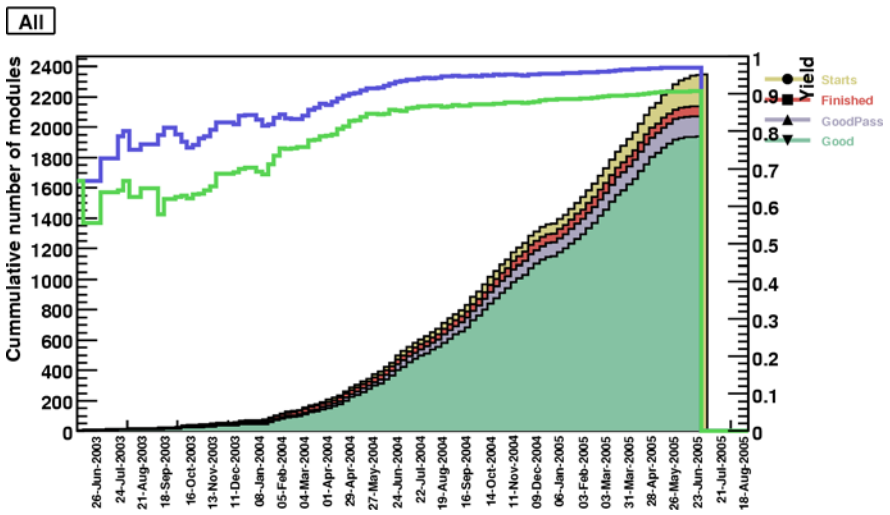

Figure 7.1. Module production performance. The filled histograms show the cumulative number of modules built as a function of time (Starts) and the number of finished, assembled and tested, modules of each variety. Also shown is the production yield (right scale) both considering just GOOD modules and also GOOD+PASS modules

Table 7-1 shows a breakdown of module production statistics according to the module type and module quality. Figure 7.1, on the other hand, shows the cumulative number of modules built as a function of time together with the yield both in terms of strictly GOOD modules and GOOD+PASS modules. The first part, where the production rate is smaller, corresponds to the period in which the different sites went through the qualification process. That process took almost one third of the total time. After that period a production rate between 40 and 50 modules per week was achieved almost immediately with a constant yield above 90%.

The flow of components and a very tight schedule have been the most notable problems during the module production. Although the delivery of the module components has not been constant, the production was never stopped for that reason, mainly because of the close cooperation of all groups participating in the project. However, setting into production mode in the different components' manufacturers was the main reason for a late start at full production rate at the different assembly sites.

The production was organized in a flexible, cooperative collaboration of the different laboratories. Some of them carried out all the steps of the module fabrication in house, while others were specialized only in some aspects of it, like assembly or testing. Also, some of the institutes have produced only one of the four different module types while others were able to produce more than one type. This structure allowed overcoming the problems that appeared during the production.

Table 7-1. Statistics of the SCT end-cap module production.

Category	**Inner**	**Middle(S+L)**	**Outer**	**All**
Modules assembled	495	772	1113	2380
Good	394	665	995	2054
Pass	39	60	61	160
Hold/Rework	46	42	23	111
Fail	16	5	34	55
Good+Pass (G+P)	433	725	1056	2214
G+P Required to equip end-caps	400	640	936	1976

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