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# A self-triggered, high-resolution data acquisition system for the KASCADE-Grande experiment

M. Brüggemann[e], T. Antoni[a], W.D. Apel[b], F. Badea[b,1], K. Bekk[b], A. Bercuci[c], M. Bertaina[d], J. Blümer[b,a], H. Bozdog[b], I.M. Brancus[c], P. Buchholz[e], A. Chiavassa[d], K. Daumiller[b], F. Di Pierro[d], P. Doll[b], R. Engel[b], J. Engler[b], F. Feßler[b], P.L. Ghia[f], H.J. Gils[b], R. Glasstetter[g], C. Grupen[e], A. Haungs[b], D. Heck[b], J.R. Hörandel[a], K.-H. Kampert[g], H.O. Klages[b], Y. Kolotaev[e], G. Maier[b,2], H.J. Mathes[b], H.J. Mayer[b], J. Milke[b], B. Mitrica[c], C. Morello[f], M. Müller[b], G. Navarra[d], R. Obenland[b], J. Oehlschläger[b], S. Ostapchenko[b,3], S. Over[e], M. Petcu[c], T. Pierog[b], S. Plewnia[b], H. Rebel[b], A. Risse[h], M. Roth[a], H. Schieler[b], J. Scholz[b], O. Sima[c], M. Stümpert[a], G. Toma[c], G.C. Trinchero[f], H. Ulrich[b], S. Valchierotti[d], J. van Buren[b], W. Walkowiak[e], A. Weindl[b], J. Wochele[b], J. Zabierowski[h], S. Zagromski[b] and D. Zimmermann[e]

*(a) Institut für Experimentelle Kernphysik, Universität Karlsruhe, 76021 Karlsruhe, Germany*
*(b) Institut für Kernphysik, Forschungszentrum Karlsruhe, 76021 Karlsruhe, Germany*
*(c) National Institute of Physics and Nuclear Engineering, 7690 Bucharest, Romania*
*(d) Dipartimento di Fisica Generale dell'Università, 10125 Torino, Italy*
*(e) Fachbereich Physik, Universität Siegen, 57068 Siegen, Germany*
*(f) Istituto di Fisica dello Spazio Interplanetario, INAF, 10133 Torino, Italy*
*(g) Fachbereich Physik, Universität Wuppertal, 42097 Wuppertal, Germany*
*(h) Soltan Institute for Nuclear Studies, 90950 Lodz, Poland*
[1] *on leave of absence from Nat. Inst. of Phys. and Nucl. Engineering, Bucharest, Romania*
[2] *now at University Leeds, LS2 9JT Leeds, United Kingdom*
[3] *on leave of absence from Moscow State University, 119899 Moscow, Russia*
Presenter: H. Rebel (Heinrich.Rebel@ik.fzk.de), ger-rebel-H-abs2-he15-poster

In order to achieve a measurable energy range of $10^{14}$ eV – $10^{18}$ eV for primary cosmic particles which includes the expected second knee, the detection area of the detector field array KASCADE has been extended from $0.04\,\text{km}^2$ to about $0.5\,\text{km}^2$ by an array of 37 scintillator stations, which form the Grande array. KASCADE and the Grande array take data in coincidence since December 2002 and allow a multiparameter measurement of extensive air showers up to above $10^{18}$ eV. The quality of the data will be improved by the usage of a new self-triggered, high-resolution data acquisition system based on signal digitization by FADCs and optical data transmission, which is unaffected by external noise.

## 1. Introduction

The FADC data acquisition system has two important features – it is self-triggering and dead-time free. These properties enable us to analyse air showers with higher resolution and allow to look for new time critical phenomena in the development of extensive air showers. While it is common for scintillation detectors to measure only one quantity – the overall energy deposited by cosmic particles passing the detector – the FADC system will provide additional time information by sampling the photomultiplier pulses. The complete signal shape can be analyzed later in full detail using offline reconstruction algorithms. Example applications are to resolve the internal structure of the shower disc based on the analysis of the signal variation with time and an improvement of the signal to noise ratio by noise reduction via digital filters.

## 2. The FADC system

The KASCADE-Grande FADC data acquisition system is a modular system comprising three custom made electronic parts. Digitizer boards, which sample the analog input signals from photomultipliers, form the first part of the system. Those boards are being installed in each detector station. The second part of the FADC system consists of receiver boards, which receive the digitized data transmitted by the digitizer boards of up to eight detector stations via an optical link. PCI interfaces connected to the receiver boards assure a fast data transmission rate to a PC farm and form the third part of the FADC system.

**Digitizer board.** The concept of signal treatment by the digitizer board is depicted in figure 1. On each board four FADCs per analog input channel running at 62.5 MHz with a 12-bit resolution are operated in interleaved mode with a displacement of 4 ns to reach an effective sampling frequency of 250 MHz. The FADCs are digitizing the signals permanently, while the data transmission is triggered by a comparator logic, which fires as soon as the input signal exceeds a programmable threshold. In case of a threshold transition, the digitizer board produces a data packet comprising a 1 $\mu$s long snapshots of the two input signals, timestamp information received from the experiment as well as the identification number of the detector station and transmits this data via an optical link to a receiver board. This process runs for each detector independent of other detectors which means that each detector runs self-triggered. For long signals, additional 1 $\mu$s sampling periods can be appended without gap to avoid dead-time.

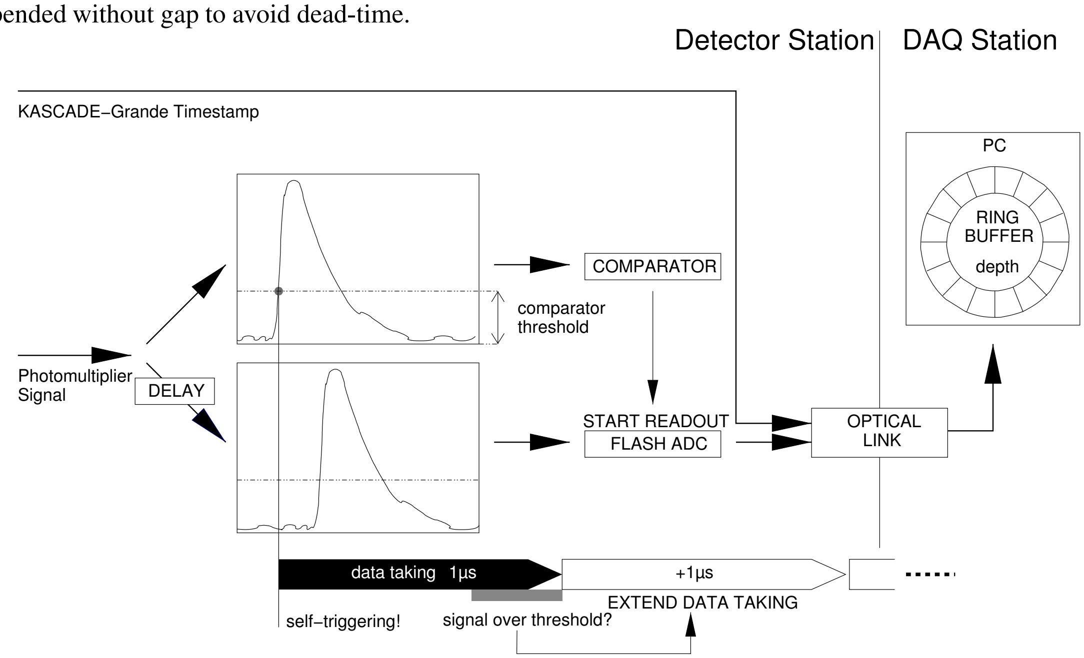


**Figure 1.** Concept of the FADC-based data acquisition system on the transmission side

**Receiver board.** The receiver board is a 9U VME board equipped with 8 optical links, which receive data packets from up to 8 digitizer boards. It derandomizes the data from the detector stations by the use of one FIFO per input channel, which can hold up to 16 data packets. The optical signals are converted into electrical signals and the data packets are then multiplexed to one common output buffer. Finally, the data is handed over to a PCI interface via a 32-bit wide LVDS link. The VME bus is used to configure the receiver board and allows hardware based debugging.

**PCI-Interface.** The PCI interface is the last stage of the FADC system. It consists of a commercial PCI prototyping board and a custom made piggy-back card and serves as the connection between the custom made electronics and a PC farm. It receives data from the receiver board and provides a fast data transfer rate into the memories of farm PCs via direct memory access (DMA). While the size of one data packet amounts to 1 KB, the rate of data packets to be transferred into the PC memories is given by the rate of uncorrelated particles passing the detector stations. The data acquisition system currently taking data measures a rate of 2.5 kHz for those particles. Taking this as a reference rate, each detector station provides a data rate of 2.5 MB/s. With 8 stations connected to a receiver board, the PCI interface has to provide an average transfer rate of at least 20 MB/s. Test measurements have shown that a maximum transfer rate of 85 MB/s can be reached.

**Event building and data storage.** All data packets transmitted by the digitizer boards are kept in the memory of the 5 farm PCs for approximately 40 s. A master PC looks for coincidences in the timestamp values of the data packets it receives from the farm PCs. Only those data packets are written to the mass storage which lie with a timestamp within a programmable time window around the coincidence. This reduces the amount of data to be stored permanently to approximately 100 kB/s. The path of the detector data after transmission by the digitizer boards onwards is shown in figure 2.

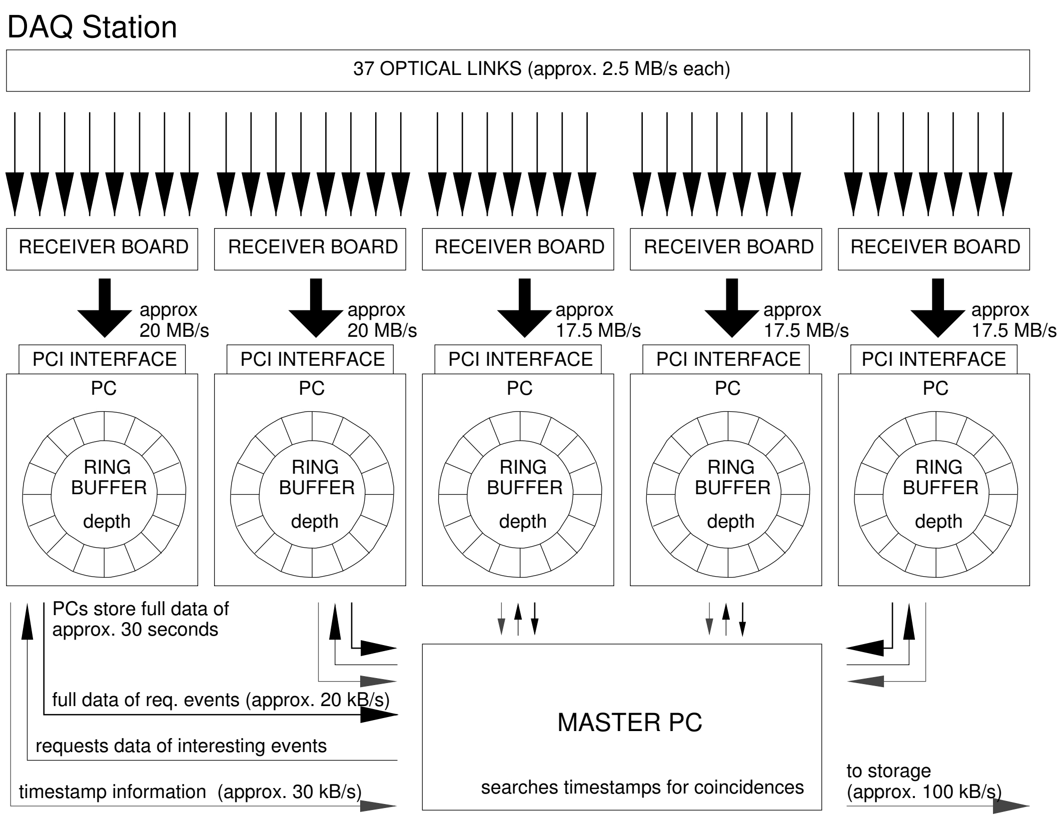


**Figure 2.** Data collection and event building on the receiving side

**First data.** After the installation of the first digitizer boards, the system has been tested by taking calibration spectra by measuring uncorrelated muons. Since the integral of the digitized signal shape is a measure for the energy deposit in the detector, the integrals of these single particle events have been accumulated in the calibration spectrum depicted in figure 3. The upper part of the figure also shows a typical photomultiplier pulse shape of an uncorrelated particle recorded by the FADC system. To avoid that noise dominates the values of the integrals, the integration was constrained to the peak region indicated by the vertical dashed lines in the upper plot. The resulting calibration spectrum in the lower part of the figure was fitted with a parametrization

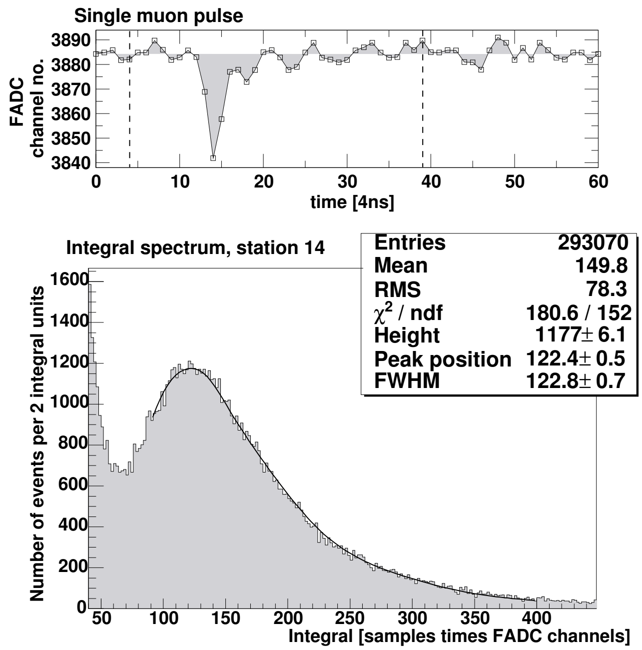


**Figure 3.** *Top:* Pulse shape of a single particle traversing the detector recorded by the FADC system. The limits of the constrained integration are indicated. *Bottom:* Calibration spectrum for station 14 resulting from constrained integration of single particle pulses.

of a simulated single muon spectrum, which is shown as smooth line. The peak position of the parametrization gives in integral units the most probable energy deposit of single muons passing the detector.

## 3. Status and Outlook

The FADC system is completely installed and currently being commissioned. As soon as the system is in full operation we look forward to take at least two years of high-quality data with the FADC system.

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