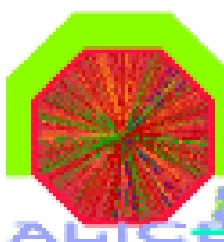


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**The single channel TripOff and the channel grouping on  
the WINER PL500F8 for the HMPID LV system**

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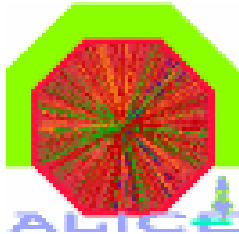
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**Abstract:**

The aim of the work is to describe the main improvements added on the WIENER low voltage power supply Mod. PL500F8 to complement some missing control features on the company version. They are mandatory prerequisites to fulfil the control requirements for the low voltage system of the High Momentum Particle Identification Detector (HMPID). Via an upgraded firmware on the CAEN CANbus controller A1676W, driving up to eight WIENER PL500F8 crates, the single channel On/Off, the single channel TripOff and the channel grouping for bipolar electronics, have been successfully provided. The trip-off time response and the details on the firmware upgrading are also given.

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A special acknowledgment goes to Claudio Raffo, as CAEN supervisor of the joint project CAEN-HMPID, and to Nicola Paoli for the relevant information he got from the WIENER Company.

## **Introduction**

In the Chapter 1 is described the architecture of the HMPID LV system. It is based on the CAEN SY1527 mainframe, the CANbus controller A1676W and the WIENER PL500F8 LV Power Supply. In this Chapter it is emphasized the necessity to achieve a fast and reliable control at level of the single channel operation for the PL500F8, and are presented the desired solutions to be implemented via the upgrading of the A1676W firmware.

In Chapter 2 are reported the technical specifications of the PL500F8 along with a series of tests results meant to explore and measure both the static and the dynamic behaviors of both the power supply and the single channel.

In Chapter 3 the A1676W CANbus controllers and the PL500F8 CAN control are described.

In Chapter 4 the implementation of the single channel On/Off, the single channel TripOff and the channel grouping on the PL500F8 with some details on the improved version R. 3.07 of the A1676W firmware, are presented. Moreover, test results on the time response of the single channel TripOff, in a three crates configuration are reported with an estimate in a configuration with eight crates.

In Chapter 5 are described the complementary improvements to fulfill the safety requirements of the HMPID control system. They are the interlock line between the SY1527 and the WIENER PL500F8 and the remote software reset of the board A1676W. Finally in the APPENDIX 1 more details on the firmware structure, with the help of flow charts and timing, are provided.

## 1. The HMPID low voltage system

### 1.1. Description of the LV apparatus

The layout of the low voltage system for the HMPID, including the control, is shown in figure 1.1.

The CAEN system crate SY1527 [1] houses the HV boards for the HMPID and the A1676W CANbus controller [2] which allows for the control of the WIENER LV power supply, model PL500F8 RATON version [3,4]. The PL500F8 is a 4U frame (including the fan tray) that can be equipped with 4 modules, for a total of eight channels 2-7 V 25 A, which fits the requirements of the FERRO (front-end or read-out) sectors in the HMPID. The A1676W is connected to the PL500 via a twisted pair (suitable for the CANbus technical specification) and it can control up to eight crates for a total of 64 channels. A telnet session on the SY1527 allows the user to operate any WIENER LV channel as belonging to a CAEN LV board.

The HMPID Detector Control System (DCS) resides on a Windows based PC, and it operates all the detector sub systems as: High Voltage (HV), Low Voltage (LV), C<sub>6</sub>F<sub>14</sub> liquid circulation, gas and physical parameters. The System control and Data Acquisition (SCADA) running at this level is the ETM PVSS. Data exchange between PVSS and the hardware is ensured via the CAEN OPC Server and the PVSS OPC Client.

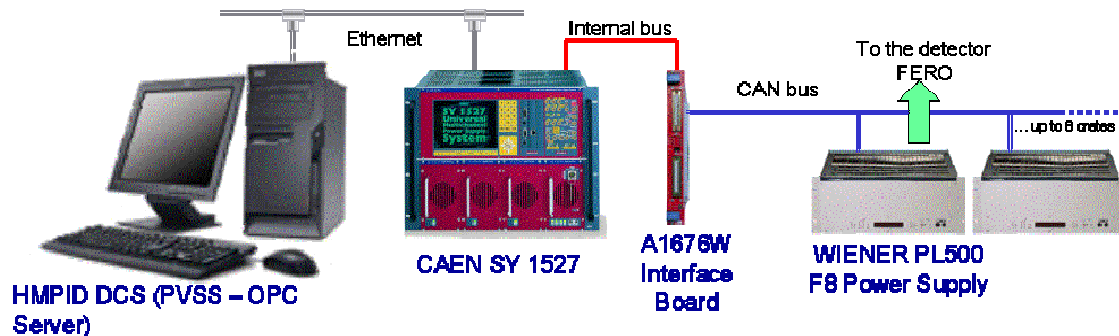


Figure 1.1 - The architecture of the HMPID LV System.

### 1.2. The CAEN A1676W as enhanced control for the PL500F8

The PL500F8 has attractive but not complete features on the control side. The single channel TripOff and the channel grouping are not implemented: a single channel error (Ovc, Unc, Ovv, Unv, and Ovp) results in the entire crate switched off. According to the adopted FERRO segmentation on each HMPID module [5], this would result then in the data lost from one half of the module. In addition since the FERRO electronics is bipolar, to avoid the unbalanced feeding (potentially harmful), the LV channel grouping is mandatory.

A first attempt to implement the single channel TripOff and the channel grouping was done in PVSS during the 2003. The long delay in the reaction time (2-4 s to switch off a single channel), and the reduced reliability of the entire system (no PVSS control no LV control) made this work an academic exercise.

An alternative detected solution was to modify the firmware of the PL500F8. After a first investigation, the WIENER Company raised insurmountable problems on the hardware design of the PL500 series preventing the implementation of the aforementioned features. Of course this solution would have been the most effective for a fast response time and reliability.

However, as can be seen in the LV set up reported in fig. 1.1, an alternative and satisfying solution could be implemented via the upgrading of the CAEN A1676W firmware. In fact its CANbus connection with the PL500F8 was judged fast and reliable enough to support the requested improvements

It has been then started a cooperation project with the CAEN to first evaluate the project feasibility and then its implementation and test.

## 2. The WIENER PL500F8

### 2.1 Technical specifications

The PL500F8 (Figure 2.1) is a 4U frame (including the fan tray) that can be equipped with 4 modules for a total of 8 channels. The PL500 series is designed to provide large numbers of external load-channels with high power consumption over long distances. The internal processor controls and monitors voltages, currents, temperatures, output power and illegal modes of operation as Over voltage (Ovv), Over current (Ovc), Under voltage (Unv), Under current (Unc), Over voltage Protection (Ovp)...

Some switches and an alphanumeric display are provided on the crate for the manual control and diagnostic.

The unit can be remotely programmed both via a RS 232 port and by a CANbus interface.



**Figure 2-1** - Power Supply System PL 500 front side

The selected LV module for the HMPID is the MDH floating type, which contains two LV channels. This power supply embeds two types of voltage regulation circuits: a fast remote sense circuit for short wires (0.5 m) that keeps the dynamic voltage deviation under 100 mV and a slow remote sense circuit whose regulation depends on filter

capacitors at load side only. The last one keeps in a static situation the voltage deviation below 01 %.

As regarding the noise performances, a  $< 10\text{mVpp}$  (0-20MHz) and a  $< 3\text{mVpp}$  (0-300MHz) noise ripples have been measured on a 0.5m and 10m wires respectively.

The power supply is compliant to the emission CE EN 50081-1 and immunity CE EN 50082-1 or 2 rules.

Other technical specifications on the HDH module type provided by the manufactory are:

- Min. to max. range: 2... 7V
- Max. output: (+/-) 25A / 165W
- Current setting accuracy: 1/20 A
- Voltage setting accuracy: 1/100 V
- Sense compensation range limited to  $\leq 10\text{V}$  of nominal voltage
- Operation temperature: 0...50°C without derating, storage: -30°C till 85°C
- Temp.- Coefficient:  $< 0.2\%$  / 10K
- Stability (Condition const.):  $< 5\text{mV}$  or 0.1% within 24 h,  $< 20\text{mV}$  or 0.5% within 6 months
- Current limiting: 100% of nominal values, programmable to lower values via Interface or display tableau
- Voltage rise: monotonously within 50ms (factory settings), different ramps and timing programmable
- Voltage set: discharge of output capacitors after DC off.
- Over voltage protection: Factory setting to 125% of nominal values
- Status control DC Off (trip off): within 5ms if  $> 2\%$  deviation from nominal or programmed values, after overload, overheat, over voltage, under voltage
- Temperature limits 110°C heat sink, 70°C ambient, all trip off points processor controlled, programmable / disabling
- Interlock input: High level or open: All outputs DC off
- Temperature limits: 110°C heat sink, 70°C ambient intern
- Efficiency (pro Module): 75% 2V/ -83% 5V/ -85%  $\geq 12\text{V}$
- M T B F, at 40°C ambient:  $> 65,000$  h (blower), electronics  $> 100,000$  h

## 2.2 Characterization of the power supply functionalities

This paragraph reports some measurements on the activation sensitivity of the error conditions and the ramp-up/down cycles carried out on the WIENER PL500F8. The following setup was used: one PL500F8 equipped with four MDH modules (8 channels) connected through a 150 m long cable to the A1676W CANbus interface housed in a CAEN SY1527 (@ 250 Kbit/s CANbus speed). A purely resistive load ( $R=1\Omega$ ) has been mounted on two channels, using a 40 meters long cable. The output voltage from one channel was recorded with a Lecroy 9310AM digital oscilloscope (1 Gs/s).

A first set of measurements, reported in section 2.2.1 verifies the Vset precision via the measurement of Vmon. The different Vset are changed via a telnet session on the SY1527 from where the Vmon and Imon are read. Using the power supply error conditions, the incertitude to set stably the Ovv and Ovc error rate is measured.

In order to carry out these measurements, the PL500F8 TripOff enable/disable is exploited: if it is enabled, at the occurrence of the Ovc all the eight channels are switched off. If the crate TripOff is disabled then only at  $V_{out} > Ovp$  the power supply is switched off anyway. In this setting an over current doesn't result in any action and it is simply flagged with the corresponding Ovc bit.

Section 2.2.2 contains results on the dynamic behavior of the power supply as during the cycles of the ramp-up/down and the Vset and Iset changing while  $V_{out}$  is different from zero.

### 2.2.1. Study on the sensitivity of the error conditions

The Table 2.1 reports the measured values of  $V_{mon}$ , Vset and  $I_{mon}$  for the Channel 01. These values are read by a telnet session on the SY1527 and Vset is varied in the range  $0 \div 2.50$  V with a step of 0.50 V. Pw is the crate power ON/OFF, and affects all the 8 channels, while Status is the code of the error condition, relative to the channel 01. If Status is null, the channel is not in error. The channel settings are the following:  $ClSet = 3.50$  A,  $OvvSet = 3.50$  V,  $OvcSet = 3.50$  A,  $OvpSet = 7.00$  V while the crate TripOff is enabled.

$V_{mon}$	$I_{mon}$	Vset	Pw	Status
0.09	0.14	0.00	On	
0.49	0.48	0.50	On	
0.99	0.91	1.00	On	
1.49	1.35	1.50	On	
1.99	1.79	2.00	On	
0.00	0.00	2.50	Off	Ovc

**Table 2.1** – Monitoring and status parameters for channel01. Trip Off enabled.

Although unexpected the error condition at  $V_{set}=2.50$  ( $OvcSet$  is greater than 2.50 A) has occurred. As will be detailed in section 2.2.2, the over current is due to an unexpected voltage overshoot during the Vset changing from 2 V up to 2.5 V. If the transition from 2 to 2.5 V is performed in many steps (i.e. 5 steps of 100 mV each), this condition is far from to occur because of the corresponding overshoot is of the order of hundreds mV.

As can be seen the difference  $V_{set} - V_{mon}$  is of the order of 0.01V which is compatible with the declared precision on the Vset .

The same setup but with the crate TripOff disabled, was used for another test where the  $OvcSet = 1.50$  A.

The Ovc condition was studied around the threshold. The test results are presented in the Table 2.2.

The \* means that a not stable over current state was observed. To get a stable error state the measured  $I_{mon}$  has to be  $\sim 20$  mA higher than the Ovc set. The amplitude of this incertitude doesn't depend on the output current.

Vmon	Imon	Vset	Pw	Status
1.39	1.30	1.40	On	
1.49	1.35	1.50	On	
1.58	1.45	1.60	On	
1.71	1.50	1.70	On	
1.74	1.50	1.75	On	Ovc*
1.80	1.69	1.80	On	Ovc

**Table 2.2** – Monitoring and status parameters for channel01. OvcSet = 1.50 A and TripOff disabled.

The current limiting functionality (CISet) was also tested with the following channel settings: CISet 1.50 A, OvvSet = 3.50 V, OvcSet = 3.50 A, OvpSet = 7.00 V and the power supply TripOff disabled. The test results are reported in the Table 2.3.

Vmon	Imon	Vset	Pw	Status
1.99	1.83	2.00	On	
2.11	1.88	2.10	On	
2.21	1.98	2.20	On	
2.30	2.08	2.30	On	
2.39	2.17	2.40	On	
2.46	2.27	2.50	On	
2.46	2.27	2.60	On	
2.46	2.27	2.70	On	

**Table 2.3** – Monitoring and status parameters for channel01. OvcSet = 1.50 A and TripOff enabled.

As can be seen the output current is limited at Imon= 2.27 A, which is 0.77 A greater than the value of the CISet= 1.5 A. We have verified that this offset is independent from CISet.

Finally the over voltage (Ovv) error condition was tested around the Ovv set value. The channel setting was OvvSet =1.50 V, CISet = 3.50 A, OvcSet = 3.50 A, OvpSet = 7.00 V and the power supply TripOff disabled. The test results are reported in the Table 2.4. The \* means that a not stable over voltage status is observed. In order to get it stable Vset has to be set 50 mV above Ovv.

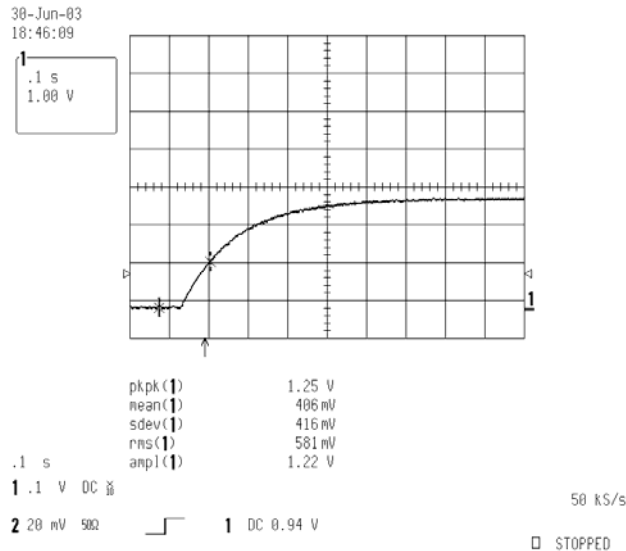
Vmon	Imon	Vset		Status
0.99	0.91	1.00	On	
1.08	1.01	1.10	On	
1.16	1.11	1.20	On	
1.30	1.20	1.30	On	
1.39	1.30	1.40	On	
1.49	1.35	1.50	On	Ovv*
1.54	1.40	1.55	On	Ovv

**Table 2.5** – Monitoring and status parameters for channel 01. OvvSet = 1.50 V and TripOff disabled.



### 2.2.2. Time respons on the error condition and ramp-up/down cycles

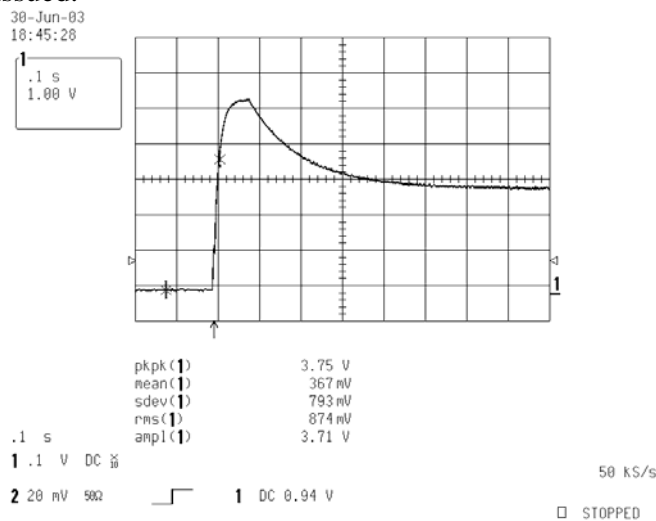
The transient analysis shows the existence of two different ramp-up procedures, which are generated according to the initial state of the channel. One is the *soft power on*, that is performed when from  $V_{set}=0$  a different value is set. Figure 2.2 shows the voltage transient at the load for a  $V_{set}$  command on channel 01 in a single step from 0 to 3V.



**Figure 2.2** – Transient at channel1 for a VSET step from 0 to 3V. The connecting cable length is 40 m.

Since the initial condition is  $V_{set} = 0$  the channel smoothly gets 3 V with a rise time of about 300 ms.

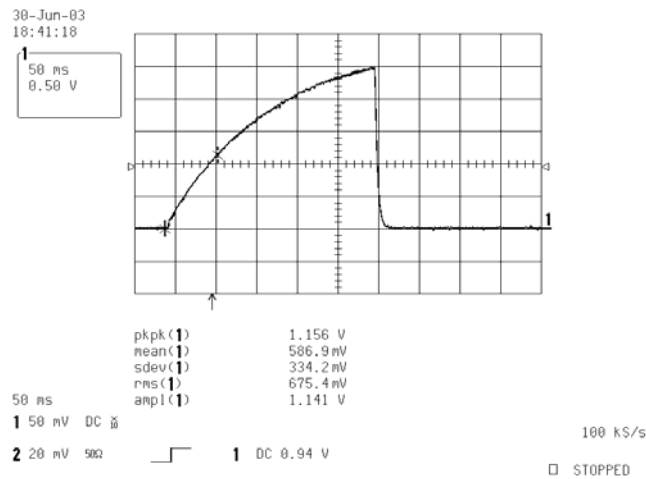
The second type of ramp-up is performed when it starts from  $V_{set}$  different from zero. In this case a voltage overshoot, 160 ms FWHM, is observed before the channel  $V_{out}$  gets the set value. In fig. 2.3 is shown the corresponding overshoot when a  $V_{set}$  changing from 10 mV to 3 V is issued.



**Figure 2.3** – Transient at channel1 for a VSET step from 10 mV to 3V. The cable length is 40 m.

Disconnecting the cable and the load, the settling time of the overshoot (i.e. time for which  $V_{mon}$  is within 90 % of its final value) results to be much longer than before. We believe that this is due to the increasing value of the load resistance, represented in this case by the 1 M $\Omega$  input impedance of the oscilloscope. This behavior suggests two things: the sense wires regulating circuit controls the ramp-up starting from  $V_{set} \neq 0$ , and it takes a longer time to correct the output voltage in a circuit with a higher RC value.

Finally the ramp-down time when an Ovv occurs, has been measured. Ovv is set at 2.5V with the crate TripOff enabled. A  $V_{set}$  command has been issued on the channel 1 in a single step from 0 up to 3V. Figure 2.4 shows the transient signal on channel 01. At  $V_{out} = 2.5$  the ramp-down starts and takes about 5 ms as declared in the technical specifications to get  $V_{out} = 0$ . All the 8 channels are in this case simultaneously switched off.



**Figure 2.4** – Over voltage and trip off of the power supply.

### **3. The CAEN A1676W CANbus controller**

#### **3.1. Technical specifications**

The Model A1676W is a single width board designed for the CAEN system crate SY1527/2527/3527 family. Via the CANbus protocol it allows for a full control of up to eight WIENER PL500F8 crates, for a total of 64 LV channels. A dedicated firmware in the A1676W provides via the SY crate all the settings and monitoring features of the PL500F8 crate and the housed channels. They appear to be respectively as a CAEN board and a CAEN channel.

This CANbus interface is equipped with the STMicroelectronics ST10F168 microprocessor at 25 MHz, a Xicor 28C256 256Kb E<sup>2</sup>PROM and an Intel 82527 CANbus controller.

#### **3.2. The PL500F8 remote control via CANbus**

The PL500F8 is equipped with a CANbus interface, which allows for a full power supply remote control. The CANbus card embeds a PHILIPS micro controller P80C592 including an 80C51 CPU kernel and a CAN Controller compliant with the Can 2.0A specifications.

The user remotely can control and monitoring all the crate and channel parameters as:

- Channel voltage
- Current limit
- Over- and Under voltage trip off values
- Overcurrent trip off points
- Temperature measurements:
  - Power supply
  - Fan tray air inlet
  - Air outlet temperature on top of slot
- Status signals
- Average speed of the fans and display of every single fan speed
- Identification of the crate
- Configuration and adjustment

For a detailed description of the WIENER CANbus protocol see ref. [6].

## 4. The improved features for the PL500F8 with the A1676W

### 4.1. Overview of the A1676W firmware

In this paragraph the standard version of the firmware for the CANbus controller A1676W, as provided by the CAEN before our cooperation project, is presented.

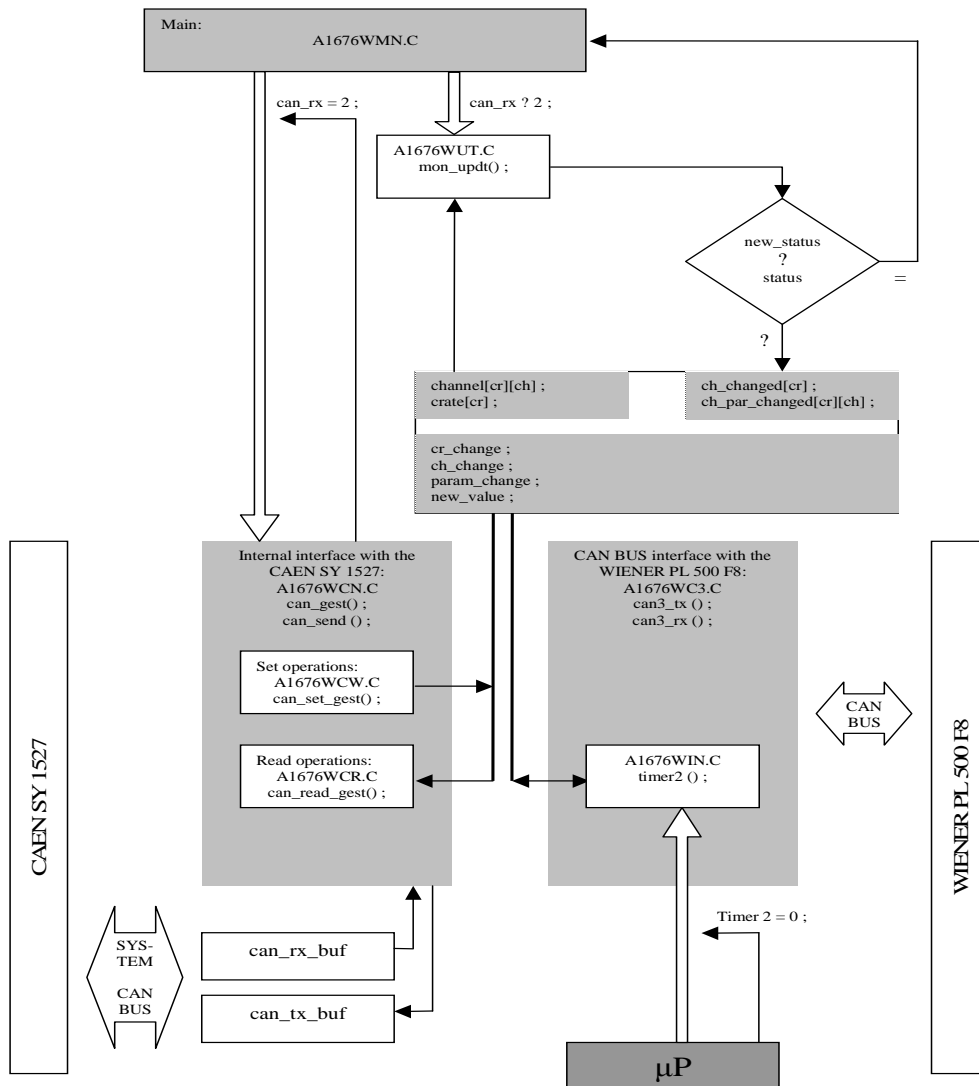
A simplified scheme is reported in figure 4.1. The rectangles correspond to the routines, whose name is written in capital letters. The names of the main sub-routines are also reported. As can be seen, the A1676W is an interface between two different systems: the SY1527 on the left side and the WIENER PL500F8 on the right side. The connection between these two systems is ensured via a dedicated CANbus line. In the SY crate family the communication between the hosed boards and the crate is also based on the CANbus protocol, so to distinguish between them, here the SY bus is called 'system Can Bus'.

The main program in the firmware is the A1676WMN.C. It verifies if the system buffers (can\_rx\_buf and can\_tx\_buf) are empty. If not, an operation on the bus of the SY1527 (read/write operation), is pending and must be executed.

In this case, the main program calls the subroutine A1676WCN.C, which handles the reading and setting operation. During a set operation (i.e. Vset = 1V on Channel1 of Crate1), the internal registers are filled with the values of the variables containing the crate address (cr\_change, from 1 to 8), the channel address (ch\_change, from 1 to 64), the name of the parameter to be set (param\_change), and the value at which this parameter must be set (new\_value). The command is executed only after the request is sent to the WIENER. This task is performed by the subroutine A1676WIN.C, which manages the CANbus communication with the PL500F8. The subroutine implements a finite state machine clocked by the Timer 2. Each time the routine is called, the branch controller sends a command to one of the connected crate via the CANbus. The response time of the system strictly depends on the efficiency of the A1676WIN.C and on the Timer 2 frequency.

If there are no action to be performed, the subroutine A1676WUT.C (mon\_updt() function) is called. It updates the monitored parameters as voltages and currents, and the channel status as Ovv, Ovc..... It compares, channel by channel, the actual status (new state) with the old one and if the two states are different, then the procedure send to the SY1527 the name of the parameter (ch\_par\_changed) and the channel number (ch\_changed) to be updated. In the readout of the monitoring parameters the scanning cycle inquires always eight crates even if some of them are not connected. For those disconnected after the inquiring there are no parameters to be readout, however some time is lost for the crate inquiring.

In case of Ovc, Ovv,.. in whatever channel in the crate, the routine accordingly sets the variables cr\_change, ch\_change, param\_change, and new\_value.



**Figure 4.1** – Simplified scheme of the A1676W firmware main routines

## 4.2. The improved features of the A1676W firmware

In this paragraph the description of the requested new features on the PL500F8 and their implementation via the A1676W firmware are presented.

In case of error (Ovc, Ovv...) in any channel, to switch off the affected FERRO sector (powered by two LV channels), the control features of the PL500F8 have to be endowed with the following new functionalities:

- The single channel On/Off;
- The single channel TripOff;
- The channel-grouping mode.

The single channel On/Off is the basic feature that will be exploited for the implementation of the single channel TripOff and the channel grouping. For any unipolar electronics the channel On/Off provides the users of an extended flexibility. It has to be pointed out that in the standard version is the crate PL500F8 that can be switched off/on but not the single channel.

The single channel TripOff is requested to avoid the crate power off when a single channel is in error.

The channel grouping is mandatory for :

- A1.preventing the unbalanced feeding of the FERO bipolar electronics at the On/Off;
- A2.switching off the group if any of the channels in the group is in error.

The new release R3.07 of the A1676W firmware, implements all the aforementioned improvements that are described in the following paragraphs.

#### **4.2.1. The single channel On/Off**

To power off a single channel the CANbus controller executes the operation  $VSET = 0$  on the addressed channel, while the *original* value of VSET is stored in the E<sup>2</sup>PROM on the board. At the next channel power on, a second CANbus operation set  $VSET=original$ . In this way from the E<sup>2</sup>PROM it is possible to recover the original setting also in case of a board power cut. To make effective this implementation the WIENER Company has been asked to modify the pl500F8 firmware. In fact on the standard version, delivered before our request ( Apr. 2003), at  $Vset=0$  a residual output voltage up to 300-500 mV was still present on the channel.

#### **4.2.2. The single channel TripOff**

As seen on Chapter 2, the crate TripOff enable/disable is provided in the standard firmware of the PL500F8. If enabled at any error occurrence on whatever channel, the crate shuts down all the other plugged channels. If disabled, the crate still remains on and the error status is notified at the A1676W during the relevant readout cycle.

An error is generated by one of the following conditions:

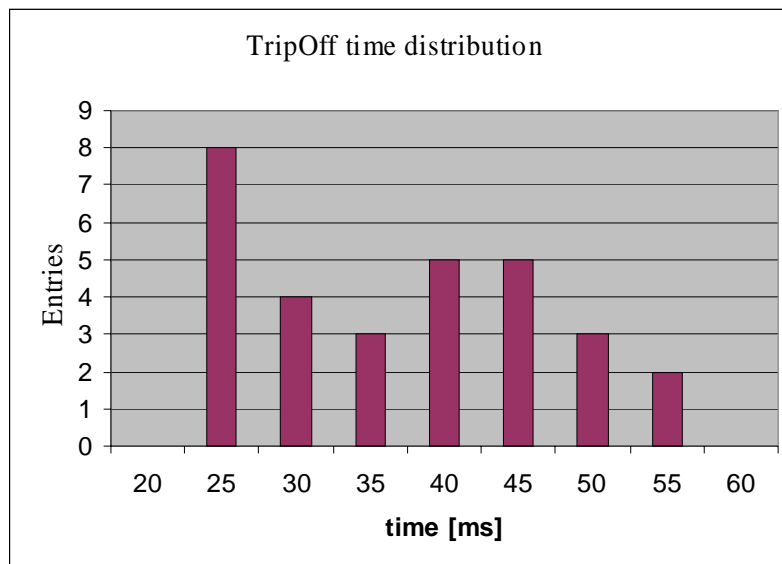
- Ovv (channel in OVERVOLTAGE ,  $V_{mon} > OvvSet$ )
- Unv (channel in UNDERVOLTAGE,  $V_{mon} < UnvSet$ )
- Ovc (channel in OVERCURRENT,  $I_{mon} > OvcSet$ )
- Unc (channel in UNDERCURRENT ,  $I_{mon} < UncSet$ )
- Ovp (channel in OVERVOLTAGE protection,  $V_{mon} > OvpSet$ )

In the new A1676W firmware, the single channel TripOff operation has been implemented in the following way. Once the crate TripOff is disabled then in case of error the crate remains ON while the error state is notified at the A1676W during the parameters reading. As soon as the error condition is detected (Ovv, Unv ...) the firmware execute a  $VSET=0$  on the affected channel (see 4.2.1). In this way all the other

channels in the crate are not affected. When the error condition is removed then the channel can be again powered on and its error condition is automatically reset. The response time of the single channel TripOff is defined as the total time requested to ramp-down the channel to zero. Of course, the software implementation of the single channel TripOff takes more than the 5 ms of the crate hardware TripOff. So in order to reduce the channel TripOff the following improvements in the A1676W firmware have been done:

- the clock frequency of the Timer 2 has increased from 40 Hz to 200 Hz. In this way the time interval between two CANbus operations is 5 ms instead of 25ms;
- an automatic procedure identifies how many crates are daisy chained and optimize the readout cycles of all the parameters from the PL500F8's;
- the status bytes are readout more frequently than the other monitoring parameters since they are used to react on the error conditions. In this way for a eight crates configuration the single channel TripOff time is in the range 25-100 ms.

With the latest version R 3.07 of the firmware, the response time has been measured with three connected crates at 1Mbps Can Bus speed (1 m of cable). An over current condition has been repetitively produced (approx. 30 times) by shortcutting the channel 1 polarities. Figure 4.2 shows the time distribution. The minimum value, the mean value and the standard deviation are respectively 25 ms, 35 ms and 10 ms. A maximum of 53 ms has been measured and is in agreement with the expected value in this set up.

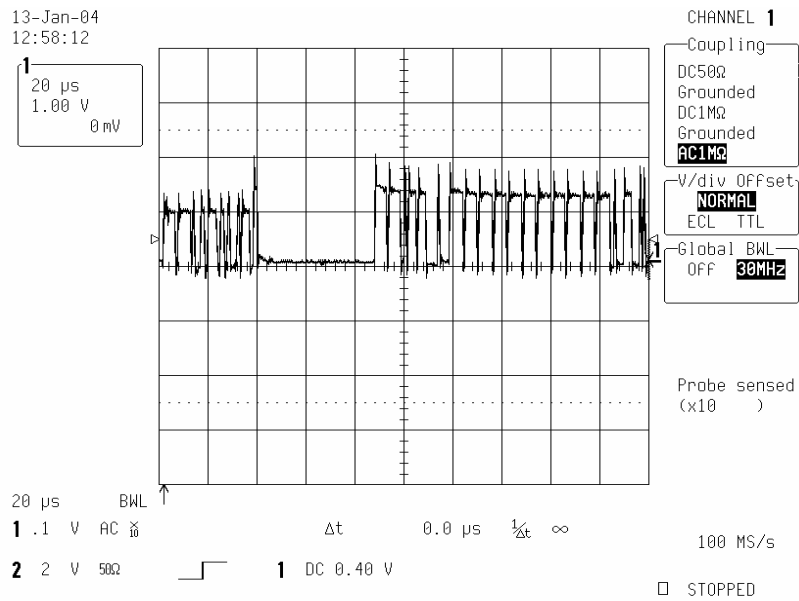


**Figure 4.2** – Channel TripOff distribution.

In the APPENDIX 1 are reported more details on the parameter readout from the PL500F8 and the related timing.

For a complete configuration with 8 crates, according to the previous results and the firmware timing, the minimum, the mean and maximum values are expected to be 25 ms, 60 ms and 100 ms respectively.

Figure 4.3 shows the two bursts on the CANbus lines corresponding the first on the left to a request from the A1676W and the second to the PL500F8 response. The total communication time is approximately 200  $\mu$ s. At the operation frequency in the experimental site, it will become about 1 ms at the CANbus speed of 250 KHz that still results negligible on the system time response. In fact 1ms is still less than the Timer 2 period of 5 ms.



**Figure 4.3** – Caen-WIENER CANbus send/receive sequence @ 1Mbps

#### 4.2.3. The channel grouping mode

To safely power on the bipolar FERRO electronics, the LV channel grouping is strongly recommended. Also this option (not available on the standard power supply version) has been added on the A1676W firmware. In particular, each crate can work in two modes:

- grouping off (Cr GRP Off) : the channel power On/Off commands are independent .
- grouping on (Cr GRP On): the 8 channels are grouped in four groups of two channels each (Ch.#1 - Ch.#2; Ch.#3 - Ch.#4; Ch.#5 – Ch.#6; Ch.#7 - Ch.#8) and for the group operation only the even channels are endowed of the channel On/Off command.

When the grouping is enabled, if one channel goes in error then both the channels in the group are switched off. In this case the delay between the two channels switching off is 5 ms (Timer 2 period). This delay should not be harmful for any bipolar electronics. The grouping enable/disable can be selected via the SY1527 by entering the *transparent mode* on the A1676W board and it is allowed only when all the channels are off. Figure 4.4 is a snapshot of the telnet session on the SY1527. The grouping is enabled for the crate 1. The



Pw button is missing (“--“) for the odd channels belonging to the crate 1 (CR1\_CH1, CR1\_CH3, CR1\_CH5 and CR1\_CH 7). The Pw status of these channels is given by the Pw status of the grouped channel.

Channel Name	UMon	IMon	Pw	Status	Trip	SUMax	Ch#
CR1_CH0	0.99 U	0.04 A	On		--	--	0.00.000
CR1_CH1	0.99 U	0.00 A	--		--	--	0.00.001
CR1_CH2	0.00 U	0.04 A	Off		--	--	0.00.002
CR1_CH3	0.00 U	0.00 A	--		--	--	0.00.003
CR1_CH4	0.00 U	0.04 A	Off		--	--	0.00.004
CR1_CH5	0.00 U	0.00 A	--		--	--	0.00.005
CR1_CH6	0.00 U	0.00 A	Off		--	--	0.00.006
CR1_CH7	0.00 U	0.04 A	--		--	--	0.00.007
CR2_CH0	0.00 U	0.00 A	On		--	--	0.00.008
CR2_CH1	0.00 U	0.00 A	On		--	--	0.00.009
CR2_CH2	0.00 U	0.00 A	On		--	--	0.00.010
CR2_CH3	0.00 U	0.00 A	Off		--	--	0.00.011
CR2_CH4	0.00 U	0.00 A	Off		--	--	0.00.012
CR2_CH5	0.00 U	0.04 A	Off		--	--	0.00.013
CR2_CH6	0.00 U	0.04 A	On		--	--	0.00.014
CR2_CH7	0.00 U	0.00 A	Off		--	--	0.00.015
CR3_CH0	0.00 U	0.04 A	Off		--	--	0.00.016
CR3_CH1	0.00 U	0.04 A	On		--	--	0.00.017
CR3_CH2	0.00 U	0.04 A	Off		--	--	0.00.018
CR3_CH3	0.00 U	0.04 A	Off		--	--	0.00.019

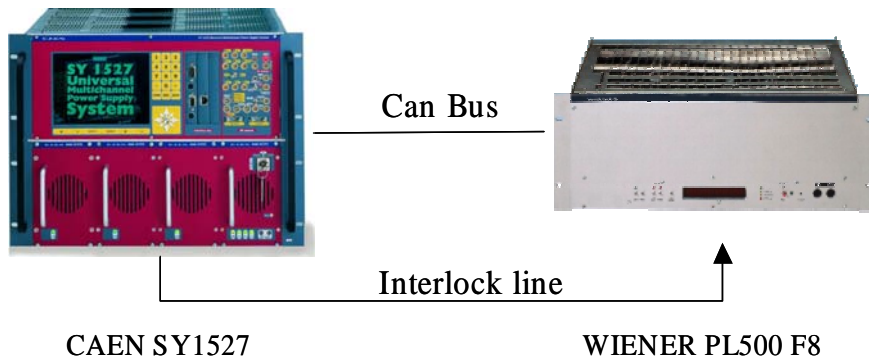
Figure 4.14 – Snapshot of the telnet connection on the SY1527. The channel grouping on the PL500F8 CR1\_CH0-7 is shown with the CH0-1 group On.

## 5. Complementary improvements

### 5.1. The SY1527-PL500F8 interlock line

In this apparatus set up the remote control of the PL500F8 is reduced when the CAEN SY1527 is off. In fact, in this case also the A1676W board is OFF. So with the crate TripOff disabled, in case of Ovc on any channel, only the current limit on the PL500F8 (ClSet) is active.

To prevent the risks arising from a reduced control, an interlock line keeps the WIENER Off when the SY1527 (figure 5.1) is Off. In turn in this hardware configuration there are two benefits: the control performance of the A1676W doesn't depend on the Ethernet traffic and if the network connection on the SY1527 is lost, the board still continues to control the LV PS. In addition if for any reason the CANbus connection with any PL500F8 is lost, the A1676W shows the “unplugged” condition for the affected crate(s) that at the supervisory level of a control system can be properly managed.



**Figure 5.1** – The SY1527-PL500F8 Interlock line: the PL500F8 is kept off if the SY1527 is off

## 5.2.The A1676W software reset

The CANbus controller is endowed with a reset button; however in the new firmware version 3.07 the software reset has also been added. This feature shows to be very useful especially when the SY crate is located far from the operator. In fact after a temporary lost of the CANbus connection (cable disconnection for more than 1-2 seconds), the board tags the crate as ‘UNPLUGGED’, and stops to send/receive commands to/from it. So to recover the connection the operator can simply issue a remote reset.

## 6. Conclusion

In order to minimize the impact on the data taking caused by a failure of a LV channel, the FERRO electronic of the HMPID on each module have been divided in sectors. The LV power supply WIENER PL500F8 fits the voltage and current requirements for any FERRO sector. The floating MDH channel type, housed in the PL500F8, endowed with remote sensing wires, provides 2-7 V and 25 A (30 peak). Although the LV power supply control didn't provide in its standard version a full single channel control, in a joint project with the CAEN, by means of the firmware upgrading of the CAEN CANbus interface A1676W, the single channel On/Off, the single channel TripOff, and finally the channel grouping for the bipolar electronics have been successfully added. Thanks to an optimized sequence of the parameter exchanging between the A1676W and the PL500F8, a considerable improvement on the time response is reached.

The test results with the new firmware release R 3.07, in a 3 crates configuration have shown a TripOff time in the range 25- 55 ms. According to the previous results and the firmware timing, the reaction time in a configuration with eight crates (64 channels), is expected to be in the range 25-100 ms, which is still suitable to prevent any harmful condition for the HMPID FERRO electronics. With the grouping on any error condition in the channel group switch Off both the channels with a time difference of 5 ms.

For safety reasons, if the SY1527 is off, an interlock line switches off all the controlled PL500F8 crates. In fact, in this case also the A1676W board would be off and only the

hardware current limit on the LV crate would be active. The remote reset complete the list of the complementary improvements provided for the PL500F8.

## 7. Appendix 1

### A1.Details on the A1676W firmware

A detailed description of the A1676WIN.C is here given. Figures A.1 – A.6 represent the state diagrams of the finite state machines and the flowcharts of the program.

Once the interrupt of Timer 2 is activated (fig. 4.1), the code pointed by the *phase* variable is executed (fig. A.1). When the *break* command is encountered, the Timer 2 is rearmed, the routine is skipped and the microcontroller executes the main program.

Any complex operation on the CANbus is composed by more than one phase. Generally one phase is needed to transmit (TX) a request from the A1676W to the PL500F8, and one or two phases are needed to check that the transmission and the reception (RX) were successful. In some cases, as for the power on of a crate, the branch controller has to ‘wait’ until the operation is terminated. All the operations start from the phase 10. The crates are polled sequentially. Only the connected crates are processed, while the others stay UNPLUGGED. If the variable *cr\_change* is different from zero, it means that a SET operation is pending, ready to be processed. This can be a crate operation (crate ON/OFF or crate Trip Off ON/OFF), or a channel operation (i.e. channel ON/OFF, VSET, OVVSET). While the request of a crate operation is executed (in the phase 20) at the next T2 clock pulse, the request of a channel operation is transmitted (TX) in the present clock cycle. This speeds up the response time in case of channel TripOff.

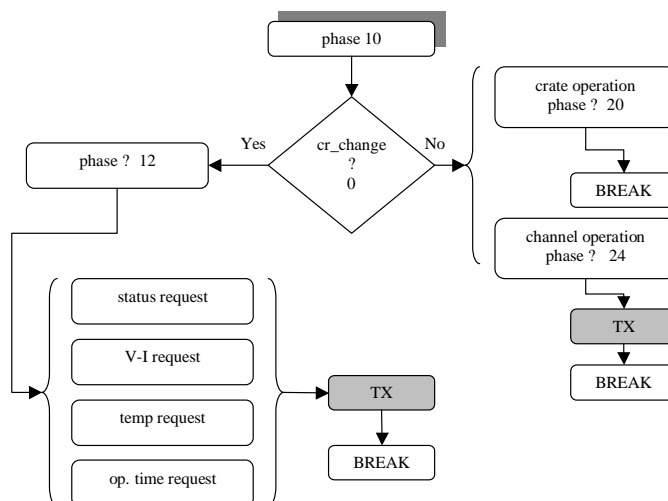
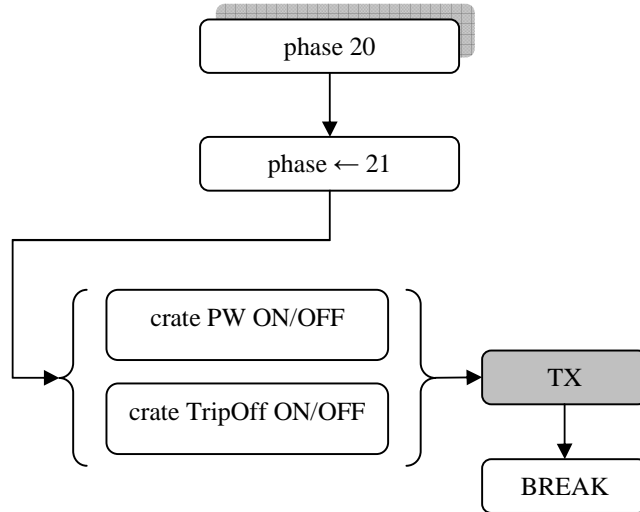


Figure A.1 – R 3.07 timer 2 routine: phase 10.

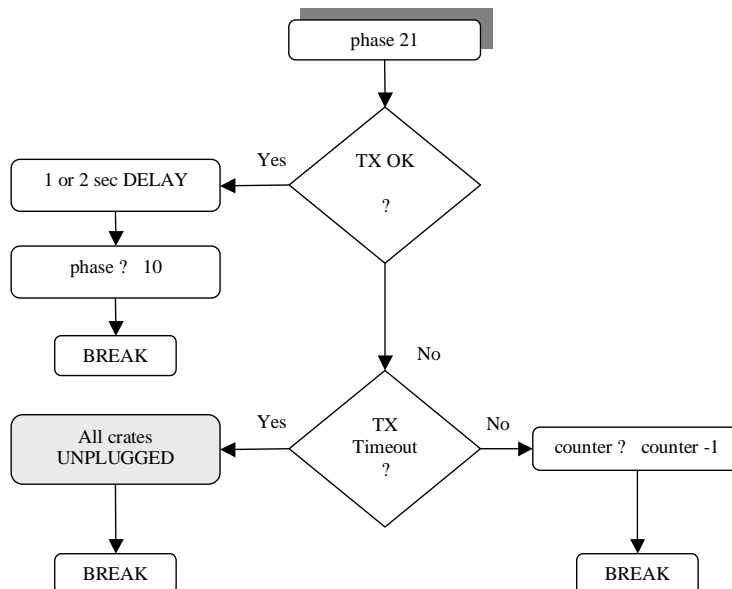
If the variable *cr\_change* is zero, one of the following tasks is executed: the reading of the status byte of a crate, the monitoring of the voltages and currents of a crate, the reading of the crate temperature, the reading of the crate operating time. The sequences of

these operations, as well as the order with which the crates are addressed are described later. Before exiting the cr\_change check, the respective request is transmitted to the PL500F8 and the phase variable is set to 12. Figure A.2 reports the phase 20. Here the request of the particular crate operation is transmitted and the phase variable is set to 21.



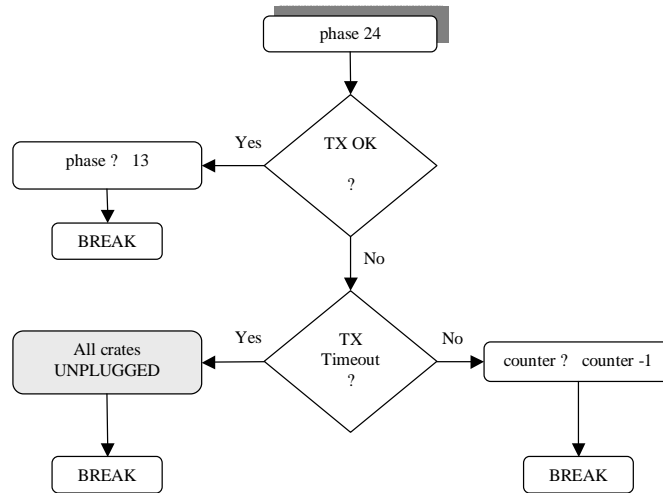
**Figure A.2** – R 3.07 timer 2 routine: phase 20.

Figure A.3 shows the phase 21 (Crate power on/off) . A check of the success of the transmission is initially performed. If the check is ok, a delay is set accordingly to the time needed by the PL500F8 to perform the requested operation: 1 second in case of a crate Trip-Off ON/OFF (corresponding to the crate TripOff enable/disable) and 2 seconds for a crate ON/OFF. If the check is unsuccessful, a timer is scaled down and the routine is skipped. In case of time out on the operation under way, all the crates are set as UNPLUGGED.



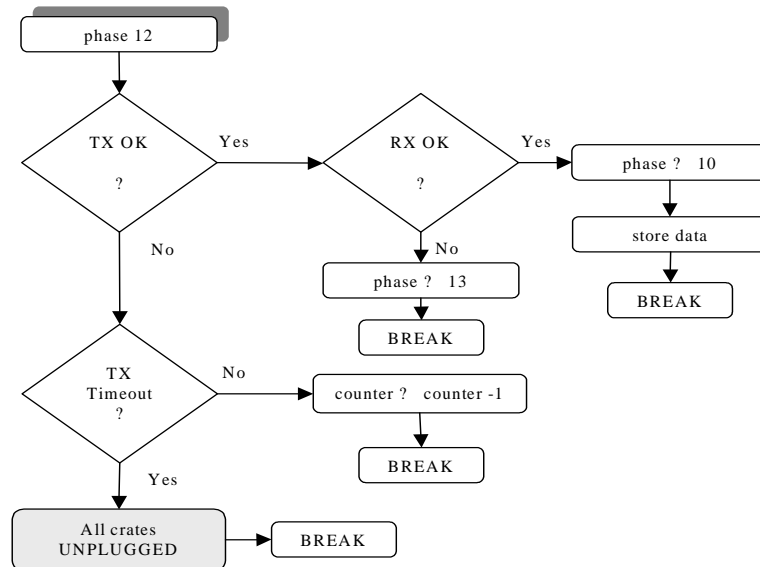
**Figure A.3** – R 3.07 timer 2 routine: phase 21.

Figure A.4 shows the phase 24. It checks if the transmission is carried out successfully. If the check is passed, the phase is set to 13 and the routine skipped. If not, a timer is scaled down and the routine is skipped. In case of time out, all the crates are set as UNPLUGGED.



**Figure A.4** – R 3.07 timer 2 routine: phase 24.

Figure A.5 shows the phase 12, which sequentially after the Tx check the Rx. If the information coming from the PL500F8 has been received correctly, the data is stored in the internal registers and the routine is skipped after having set the phase back to 10. If the response hasn't yet been received, the phase variable is set to 13 and the routine is skipped.



**Figure A.5** – R 3.07 timer 2 routine: phase 12.

Figure 4.6 shows the phase 13. A check of the reception of the PL500F8 response is initially performed.

Once the response arrives, the data is stored in the internal registers and the routine is skipped after setting the phase back to 10. If not, a timer is activated. In case of time out only the channels belonging to the addressed crate are set as UNPLUGGED and the phase is set back to 10.

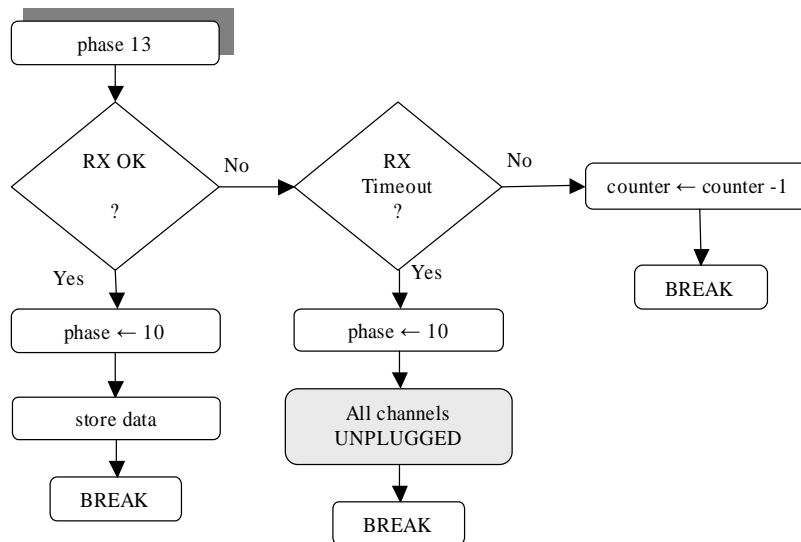


Figure A.6 – R 3.07 timer 2 routine: phase 13.

## A2. Time response on the single channel TripOff

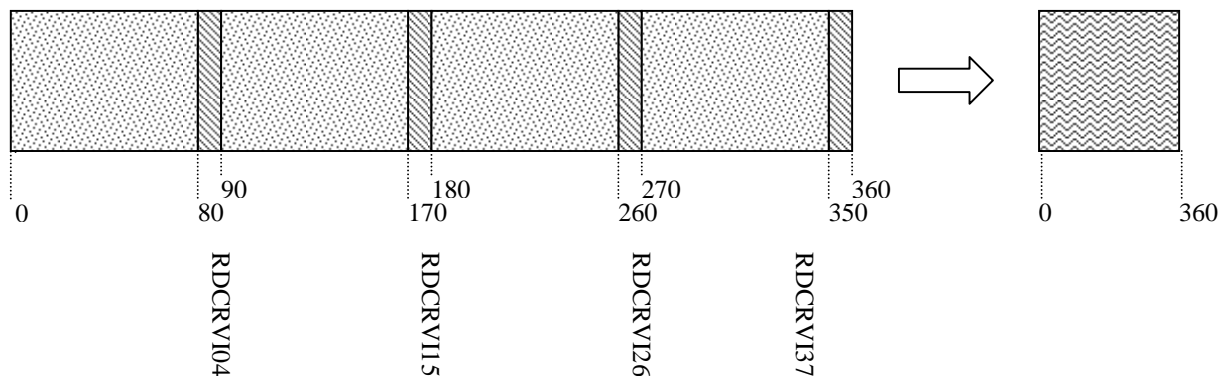
The response time for a single channel TripOff is given by the sum of the reading time of the status bytes from the power supply, plus the time needed to send back to the PL500F8 the command channel OFF. In the original version of the firmware the Timer 2 period was set to 25 ms. In the new version 3.07 pushing it down to 5 ms (the minimum time compatible with the system architecture), the time requested for a single operation on the PL500F8 is 10 ms. Therefore, the reading cycle of the status bytes in a configuration with eight crates, takes 80 ms. This calculation is valid under the hypothesis of a successful transmission and reception at the first execution of the phase 12 (see figure A.5). If a channel trips immediately before the affected byte status is read then only 20 ms are enough to power off the affected channel. If a channel trips just after the affected byte status is read then to the 80 ms to recycle the eight bytes status, 10 ms of monitoring parameters along with 10 ms for the command channel OFF have to be added. In this case the maximum expected TripOff time for a single channel becomes 100 ms. In order to keep as short as possible this reaction time in a configuration with less than eight crates, in the new firmware version R 3.07, the software detects the number of crates connected on the CANbus and adapt accordingly the reading cycle of the status bytes. In this way if only three crates are present (as in the test) then adding 10 ms for the channel off time, 10 ms for the monitoring cycle (see A2 and A3) and the phase

difference with the Timer 2, a maximum total time of 55 ms is reached, as measured in fig. 4.1.

### A3. Monitoring sequence of the Imon and Vmon

The byte status reading from the crate needs one request RDCRSTAT. The monitoring of crate voltages and currents requires 4 different requests: RDCRVI04, RDCRVI15, RDCRVI26, and RDCRVI37 while the crate temperature and the power supply operating time need one request each (RDCRTEMP and RDCRTOPSOT respectively).

In fig. A.7 is reported the best optimization of the byte status reading, while preserving the monitoring functionality. The monitoring parameters are interleaved with the status requests. With eight crates daisy chained, first the eight status bytes are read, then after four readings cycle all the monitoring parameters for one crate are read as well for a total of 360 ms.

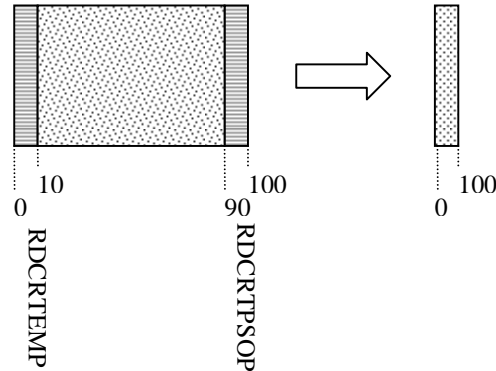


**Figure A.7** – In this figure is shown the reading sequence of the status bytes of eight crates (dotted area) interleaved with the Vmon Imon of one crate (dashed area). The time duration are reported in ms.

The monitoring parameters for eight crates are thus updated every 2880 ms.

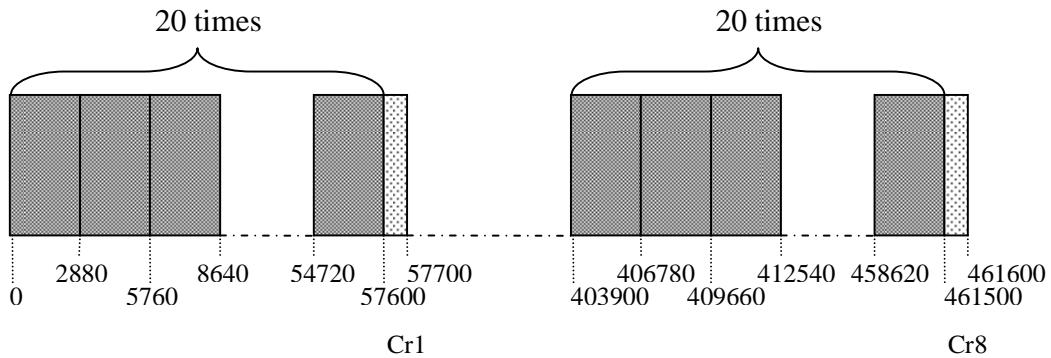
### A4. Monitoring sequence of the crate Temperature and Time Operation

Since the crate temperature and the operation time of crate are not critical parameters, once all the Vmon and Imon are read, then the temperature and operating time reading, (Figure A.8), take place. The 2 requests for temperature and operating time reading are performed at the beginning and at the end of the status bytes requests. In a configuration with eight crates it takes 100 ms per crate.



**Figure A.8** – The reading operations of temperature and operating time for a generic crate.

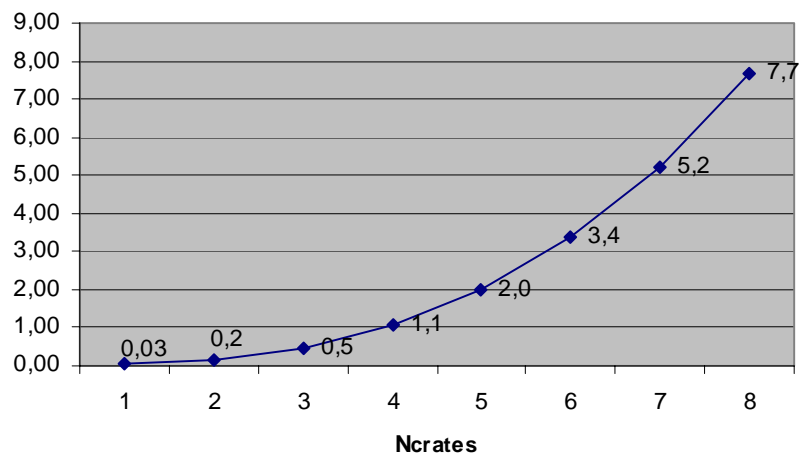
In fig. A.9 is shown the complete reading cycle of the status bytes, the monitoring parameters (Vmon, Imon), the temperature and crate operation time in a configuration with eight crates. The figure is not in scale. The reading cycle of temperature and the power supply operating time for one crate is interleaved each 20 scans over the reading cycle of the status bytes and monitoring parameters. The refresh rate of the crate temperature and the power supply operating time for 8 crates is thus:  $((2880 * 20) + 100) * 8 = 461600 \text{ ms} \approx 8 \text{ min}$ .



**Figure A.9** – The complete reading cycle of the status bytes, Vmon, Imon, the temperature and operating time for eight PL500F8 crates. Time not in scale.

The refresh rate of the crate parameters, when a generic number,  $N_{\text{crates}} (< 8)$ , of crates are connected can be calculated by:  $[((10 * N_{\text{crates}} + 10) * 4 * N_{\text{crates}}) * 20 + (10 * N_{\text{crates}} + 20)] * N_{\text{crates}}$ . This formula is plotted in figure A.10, where  $N_{\text{crates}}$  varies from 1 to 8. As can be seen, the curve exhibits a non linear dependence from  $N_{\text{crates}}$ .





**Figure A.10** – Time needed for a complete reading cycle v.s. the number of daisy chained crates. Time in seconds.

## References

- [1] Official Caen web site: <http://www.caen.it/>
- [2] A1676W (preliminary) data sheet:  
[http://www.caen.it/nuclear/technical\\_documents.php](http://www.caen.it/nuclear/technical_documents.php)
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- [6] “CAN-BUS Interface for WIENER Crate Remote Control”, A. Ruben, A. Koster, WIENER Plein & Baus GmbH, Jan. 1996.
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