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MODIFICATION OF PSB FAST PHASE SHIFTER FOR 2002

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Introduction

It was discovered during the 2001 PSB physics run, that some of the Fast Phase Shifters (designed by J-L. Vallet) used in the proton beam control, had a bug at power up causing a random offset. It was noted that 4 out of the 10 units installed in the proton and future ion beam control developed this random offset when the power was switched on, or when a power glitch reset the units. This would produce an offset that required an intervention by the RF team, each time there was a power glitch.

The original series of Fast Phase Shifter (FPS) installed in the PS did not exhibit this characteristic, so it was decided to study the source of the problem in some of the PSB units.

The source of the problem

The operation of the FPS in the PSB requires only one digital phase control input, where the unit has the possibility of 2 inputs. The input data is 23 bits with a strobe, ensuring that each input word is strobed into a latch when the input data changes, but independently of the other input. These words are buffered via the latches, before being applied to the two data inputs of an Arithmetic Logic Unit (ALU), which performs the addition of the two words.

It was observed that at power up, there would be no strobe available from the input data until the data was changed, and that if there were no input connected, we would have to rely on the correct power up sequence to ensure the latches performed correctly. When this sequence was studied, it was obvious that there was a difference between a unit that did not generate a random offset an one that did.

When the output of the flip-flop that performs the clocking of the latched input data was observed, the difference between the 2 units became obvious. It could be seen that initial clock generated at power up by the flip-flop on a bad unit, was 300 µs shorter and only 1.25V instead of 2.5V.

A study of the differences observed between a good and a bad unit showed that the clocking circuit was constructed of IC's produced by different manufacturers. The correct combination of manufacturers was found to be essential for the correct operation of the FPS, the details of which will be outlined in the next section.

The correct choice of components for FPS

The drawing in fig. 1 shows the section of the circuit that was found to cause the improper operation of the FPS.

Observing pin 9 of IC 11 or IC 34 on an oscilloscope as shown in fig. 2, we can see that Channel 2 (green) demonstrates a pulse at power up that is too short and too low to clock the input data into the latches. Channel 1 demonstrates the response of a good unit at power up giving time for all data bits to be clocked high.
To achieve the correct pulse shape at power up, table 1 shows the good and bad combinations:

Good Combinations		Bad Combinations	
IC 11+29	IC 13+34	IC 11+29	IC 13+34
Motorola F742BV713	Texas SN74F244N	SIGNETIC 74F74D	SIGNETIC 74F244N
Motorola F74XAC503	Texas SN74F244N	SIGNETIC 74F74D	Motorola MC74F244N
Motorola F74XAC503	Motorola MC74F244N	Any Motorola F74	SIGNETIC 74F244N
Motorola F74XAA504	Motorola MC74F244N		
Motorola F74XAA504	Texas SN74F244N		

Table 1

A further modification to ensure the correct operation of the FPS

After a discussion with the PS-RF-LL section, it was decided to try to find a solution to the power up glitch problem, without relying on the correct choice of IC manufacturer.

As only one digital phase input will be required on the FPS for the foreseeable future, it was decided that the unused input should be clocked in a way that it would always receive the required pulse, even in the case of a power glitch. The single input that is required, receives a strobe to clock the latches every cycle in the PSB, and so will only hold any offset for one PSB cycle after a power glitch.

It was considered desirable to keep the option of reusing the second input in the future, so any modification should be minimal and not endanger the use of this feature.

It would have been interesting to use part of the programming of the logical function of the ALU to ensure that only the first digital phase input would be used in the operation, but the pcb layout prevented this. It was found that pins 48(Rs0), 49(RS1) and 50(FTAB) of the ALU were connected together under the 68-pin socket, making for a very difficult modification. After the operation of the ALU was understood and any simple modification found impossible, it was decided to look else where for a solution.

The simplest solution seemed to be to use the available 8 MHz clock that was connected to pin 11 of IC11 (see fig.1) to permanently strobe or clock the latches of the unused input. Soldering a connection between pin 11 and pin 3 of IC 11 achieved just this.

There are, however, 2 disadvantages to the above solution, the first being the fact that we have the clock connected to the front panel via the strobe pin for SK2, and the second that the Data Loaded LED flashes permanently on the front panel since input 2 is being clocked at 8 MHz.

To solve the first problem an open 26-pin 3M connector is used to block the second input, to ensure nothing is connected, and the input labeled accordingly.

The second problem required that the clock generated by pin 9 of IC 11, which also goes to pin 5 of IC 30, be disconnected, so as to make sure that the Data Loaded LED

flashes only when phase input 1 is strobed. It was necessary to ground pin 5 of IC30 after the clock was disconnected to ensure the OR operation of IC 30.

A note on the power supply of the ALU: IC21

Whilst investigating the operation of the ALU in the hope of modifying it's operation, a number of interesting points were noted regarding the power supply for the this chip, pin 18 (Vcc) and the Ground pin 19.

It was discovered that while the pcb was being designed, the Vcc had never been connected to the +5V, and the ground had also never been connected to earth. This did not seem to greatly affect the operation of the chip in this application, and if measured with a voltmeter, the Vcc pin showed a tension of 4.25V.

It was decided to modify all existing units in the PS and PSB machines to ensure that all had the ALU connected to the power supply.

Conclusion

The result of the modifications outlined above gave a suitable solution to the problem as experienced in the PSB. All 10 units in the PSB have been modified accordingly, and when tested proved to be bug free.

It should be noted that the units used in the PS never experienced the same bug, and so continue to operate with only the power supply to the ALU having been modified.

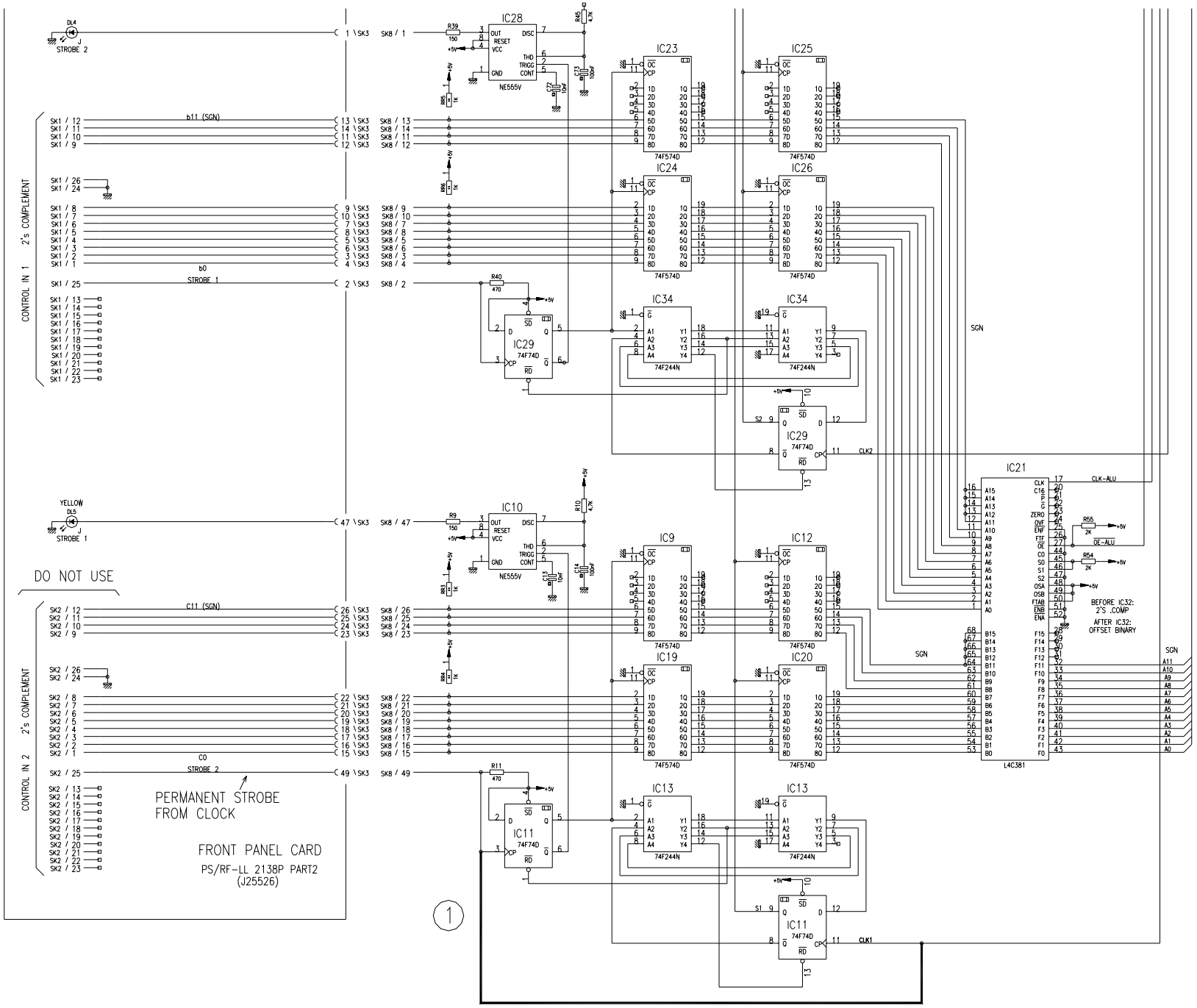
CONTROL IN 1 2's COMPLEMENT
CONTROL IN 2 2's COMPLEMENT
DO NOT USE
STROBE 2
STROBE 1
b11 (SGN)
C11 (SGN)
b0
C0
PERMANENT STROBE FROM CLOCK
FRONT PANEL CARD
PS/RF-LL 2138P PART2
(J25526)
IC28
IC23
IC25
IC24
IC26
IC34
IC29
IC10
IC9
IC12
IC19
IC20
IC13
IC11
IC21
74F574D
74F244N
74F74D
NE555V
L4C381
SGN
CLK2
CLK1
CLK-ALU
OE-ALU
BEFORE IC32: 2'S .COMP
AFTER IC32: OFFSET BINARY

FIG. 1

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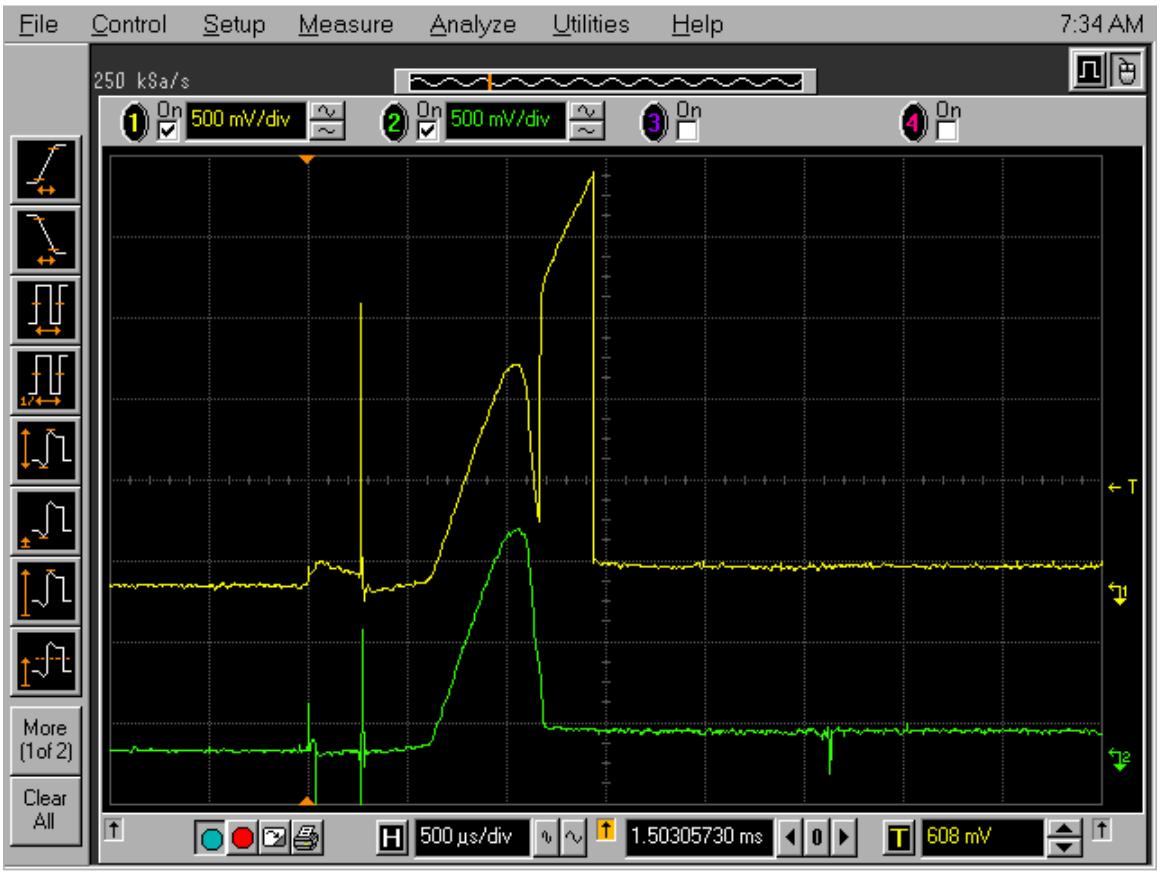

Acquisition	Sampling mode real time Memory depth automatic Memory depth 1255pts Sampling rate automatic Sampling rate 250 kSa/s Averaging off 9-bit BW Filter off Interpolation on
Channel 1	Scale 500 mV/div Offset 655.0 mV BW limit off Coupling DC Impedance 1M Ohm Attenuation 10.00 : 1 Atten units ratio Skew 0.0 s Ext adapter None Ext coupler None Ext gain 1.00E+00 Ext offset 0.0E+00
Channel 2	Scale 500 mV/div Offset 1.6740 V BW limit off Coupling DC Impedance 1M Ohm Attenuation 10.00 : 1 Atten units ratio Skew 0.0 s Ext adapter None Ext coupler None Ext gain 1.00E+00 Ext offset 0.0E+00
Time base	Scale 500 µs/div Position 1.5030573 ms Reference center
Trigger	Mode edge Sweep triggered Hysteresis normal Holdoff time 60 ns Coupling DC Source channel 1 Trigger level 608 mV Slope rising

Figure 2