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CERN - PS DIVISION

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A NEW RF SYNCHRONIZATION PROCESS

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Ref. PS/RF-LL

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1 PREAMBLE

At injection or extraction, in synchrotrons, the beam needs to be synchronized with an external reference. The aim is to obtain a fast but adiabatic synchronization process.

The synchronization method used until now in the PS complex is a 3-stage process :

a) Wait for flattop
b) Force (with a beating loop) the rf frequency to a value equal to the reference frequency plus an offset, in order to obtain a beating on the phase discriminator.
c) Close the synchronization loop when the measured phase crosses zero (making sure the discriminator is on its linear domain).

This method is not fully satisfactory since it requires a few tens of milliseconds to settle, and also because it undergoes two transients – beating and synchronization – that may trigger some instabilities on the beam.

Another method, making use of a **moving reference,** allows the synchronization process to start during acceleration. The principle is to transpose the rf frequency to the reference value by adding a pre-programmed offset. This frequency offset is cancelled before flattop in order to end with a transposed rf (called "moving reference") equal to the rf itself. As the manipulation is accomplished on the frequency value, the control of the phase is not possible unless the frequency behaviour (typically its integral) is reproducible during the process. With this method the beam is made available straight from flattop, but it still undergoes two transients and is not very robust in terms of phase precision, as it needs a very reproducible frequency history.

The proposed new scheme provides a synchronized beam straight from flattop, with no previous knowledge of the beam phase during acceleration and without any transient applied to the phase loop. It is an extrapolation of the moving-reference method. It also provides a synchronization phase control that saves up the use of an external phase shifter.

The project of the new synchronization was mainly triggered by a visit to BNL in August 1998 were Mike Brennan exposed his method to synchronize the Booster to the AGS using a moving reference. In October 99 a proposal was exposed to the PS/RF/LL section without any further action. The need to improve the process for the new coming beams motivated the employment of a technical student (Françoise Courthieu) to start the development in April 2000. Unfortunately this person was hired elsewhere before she could finish the project. The process is now rehabilitated and this note serves as a formal starting point.

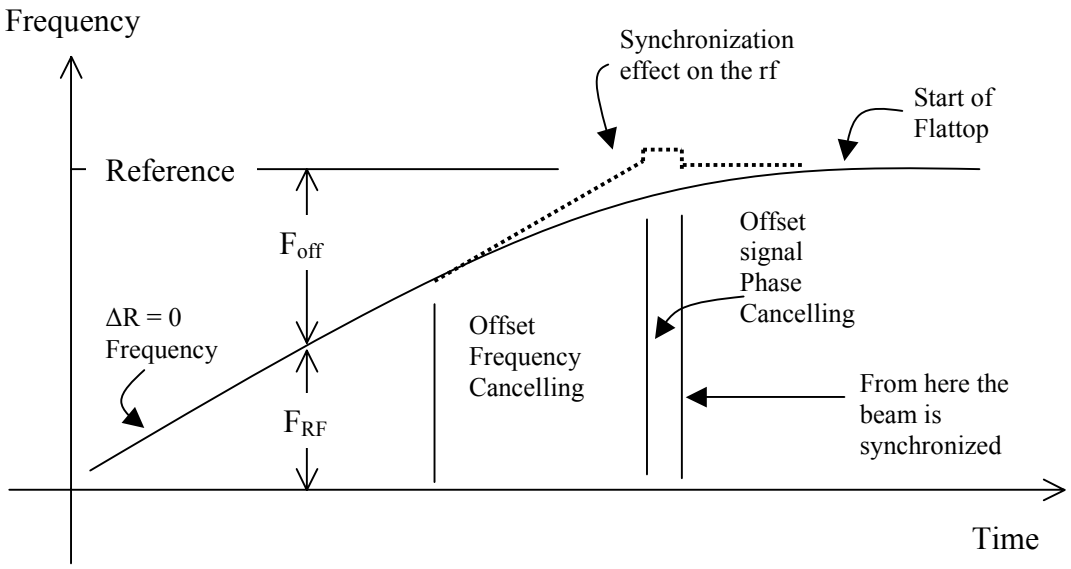
The motives for changing the actual synchronization system are mainly coming from the PSB were there are the following constraints:

- Fast (600 ms cycles)
- Adjustable (ppm working mode)
- Adiabatic (typically all beams)

For practical reasons the resulting module should be universal, remote controlled, simple (in terms of hardware) and re-programmable (FPGA).

2 EXPECTED BEHAVIOUR

The case will be discussed for an accelerating non-relativistic machine. The analysis can be extrapolated to other types - relativistic (fixed frequency) or decelerating synchrotrons.



This graph defines the offset frequency – F_{off} - as the difference of reference and rf. The sum of rf and offset is called "moving reference" and can be compared (and locked) to the real reference anytime during the accelerating cycle.

The theoretical frequency, corresponding to the central orbit $\Delta R = 0$, is represented by a solid line. The dotted line represents the expected behaviour with the new synchronization module active. It can be observed that during offset frequency cancelling, the frequency goes off the nominal value, creating a radial offset for the beam. This effect is strictly under control in the process and can be set to zero, as will be explained later.

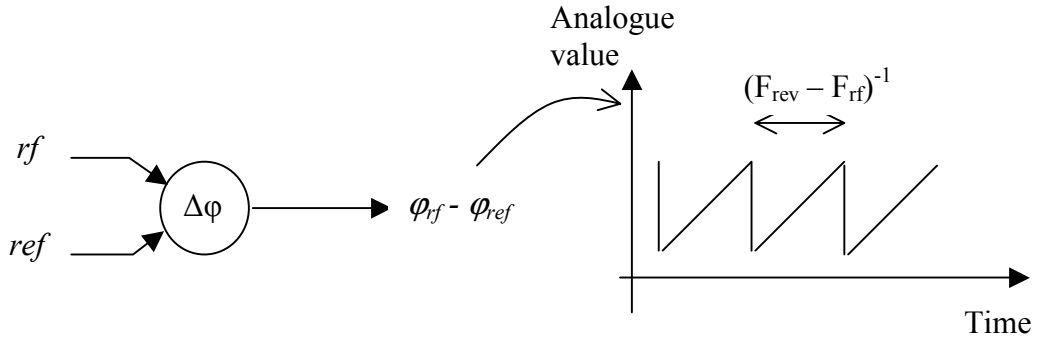
To set the offset phase to zero, a frequency step is applied. This step and related effects on the beam are also under control and can be set arbitrarily low.

3 BASIC CONCEPTS

Synchronization means that the rf, and thus the beam, is rigidly phased (on average) with the reference:

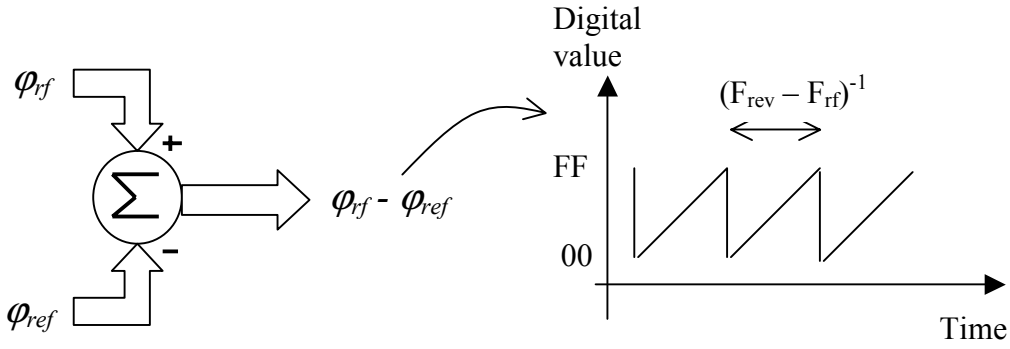
$$\varphi_{rf} - \varphi_{ref} = \varphi_{set}$$

With the classical (analogue) synchronization system, the parameter of final importance – the loop error signal - is the rf versus reference phase difference.



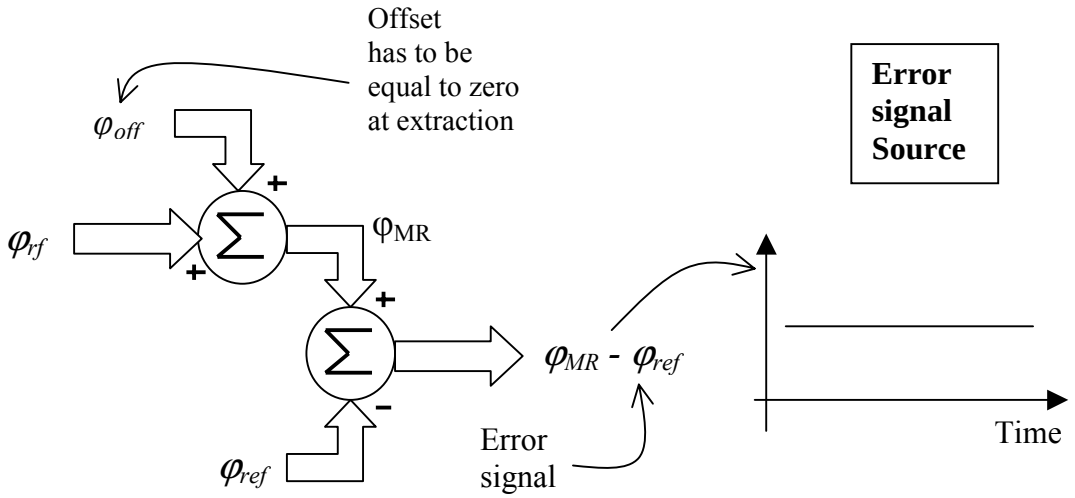
In the new system, same thing! The slight difference is that, instead of the rf analogue signals, we compare the digital phase values of rf and reference. The digital phase value of an rf signal is typically available at the output of a phase accumulator in a digital synthesizer.

We end up with the following comparator:



During acceleration the value of φ_{ref} and φ_{rf} is incremented at each clock cycle (the clock is supposed to be common). If reference and rf were at the same frequency, the output of the phase subtracting point would be constant. In the general case it will be a saw tooth with a repetition rate equal to the frequency difference.

It can be done by keep the output of the phase comparator constant during acceleration by using an **offset signal**.



The error signal is now the difference of an extrapolated (or estimated) rf phase φ_{MR} (the moving reference phase) and the reference phase φ_{ref}. The principle is that the increment per clock period of φ_{off} plus the increment of φ_{rf} is equal to the increment of φ_{ref}. The resulting $\varphi_{MR} - \varphi_{ref}$ is thus constant during the accelerating cycle. This trick enables the synchronization loop to be closed at any time.

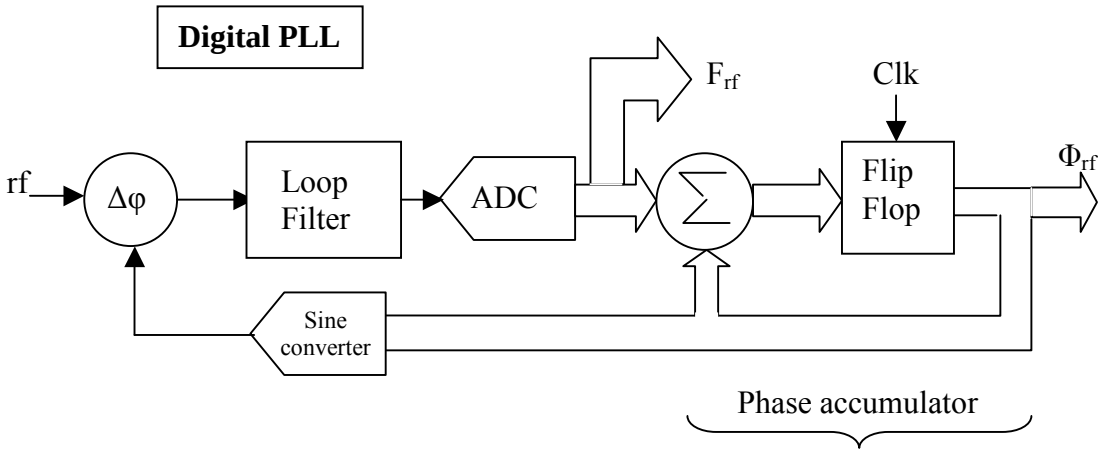
The synchronization loop being closed, the performance of the mechanism will entirely rely on how you bring the moving reference phase to zero. This is the crucial point of the method.

4 CREATION OF DIGITAL, PHASE AND FREQUENCY WORDS

4.1 Reference and RF

Reference and rf were until now represented by their phase value incremented at each clock cycle. The way these are created is described below.

The phase word is created at the output of a phase accumulator the input of which is fed by a value equal to the phase jump per clock cycle. This $\Delta\varphi/T_{clk}$ at the input is proportional to the frequency obtained at the output. This frequency word may come from various places. It can be a fixed value, as for the reference; it can be derived from a pre-programmed table, as for the rf; or it may come from a phase discriminator in a phase-locked-loop when the phase value needs to be extracted from an analogue signal. The digital PLL circuit is described below:

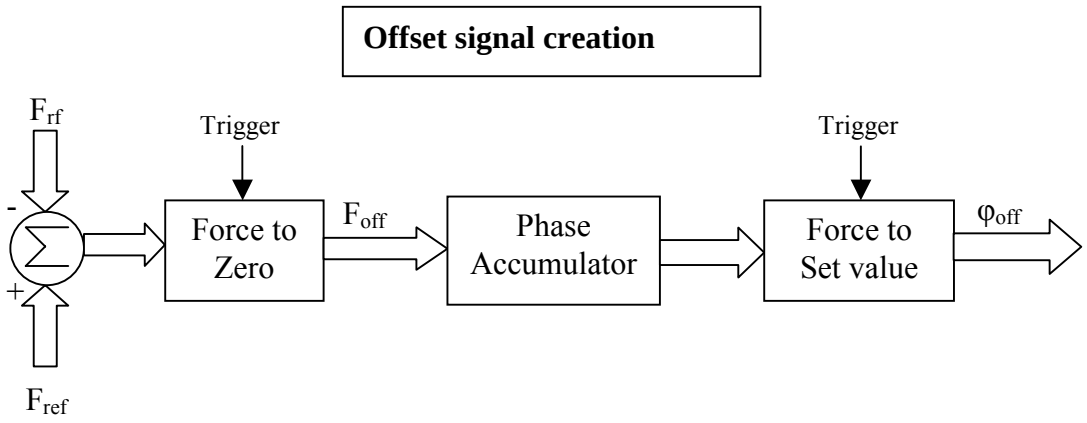


This simplified figure shows how the frequency and phase words can be extracted from an analogue rf signal. The rf is fed into a phase discriminator where it is compared to the phase word φ_{rf} reconstructed into a sine wave.

This diagram is not practical as it would require a 23-bit ADC in the CERN PS context. This can be avoided by injecting (adding) a pre-programmed frequency at the input of the phase accumulator, thus letting the DAC taking care of the LSB's only, with the advantage of a faster settling time. In applications where the response time is not critical, the implementation of a second phase accumulator (used as an integrator) in front of the one in place would also require a smaller ADC.

4.2 Offset frequency

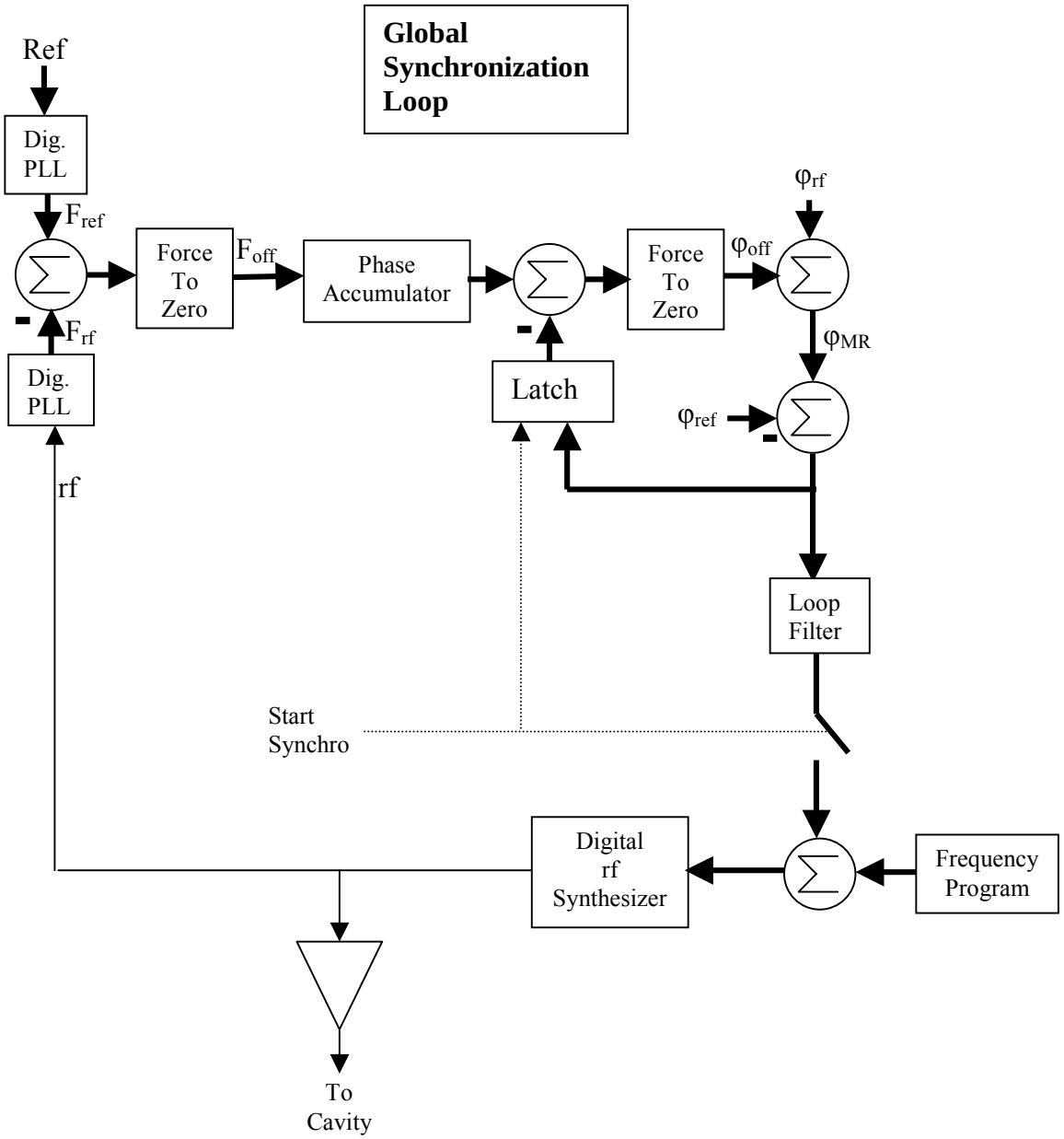
For reasons that will be presented later, φ_{off} cannot just be the difference of φ_{ref} and φ_{rf} . It needs some degree of freedom! The way it is constructed is shown in the following picture.



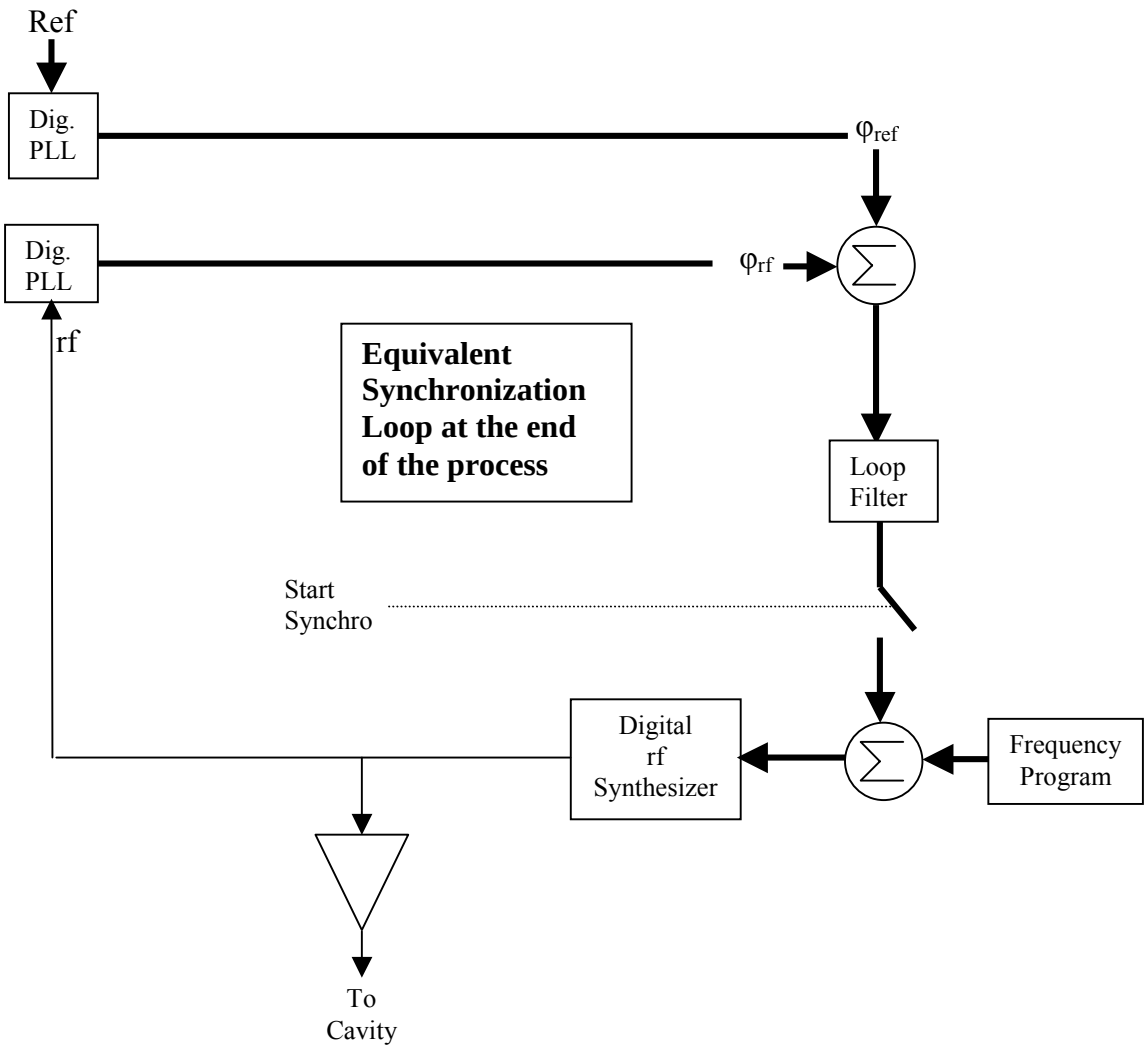
This diagram shows that F_{off} is obtained by subtracting reference and rf frequency words. A phase accumulator is then creating φ_{off}. Note the presence of two "force to zero" boxes; their function is essential as the moving reference is to become null at the end of the synchronization process. Instead of null, φ_{off} may as well settle down to a constant set-value to change the synchronization phase. This explains the "force to set value" box.

5 GLOBAL SYNCHRONIZATION PROCESS

The digital phase value of rf, reference and offset being obtained, the global synchronization mechanism can be described.



When the moving reference is cancelled this diagram shrinks to become as follow:



When the moving reference has been forced to zero, the equivalent loop diagram is typically of a classical type. The only novelty is the digital Phase Locked Loop from where the phase value is obtained as a binary word.

Being convinced that the circuit ends up as a classical type (known to be effective), one should focus on how the offset signal is cancelled (or how the moving reference becomes rf).

6 MOVING REFERENCE EVOLUTION

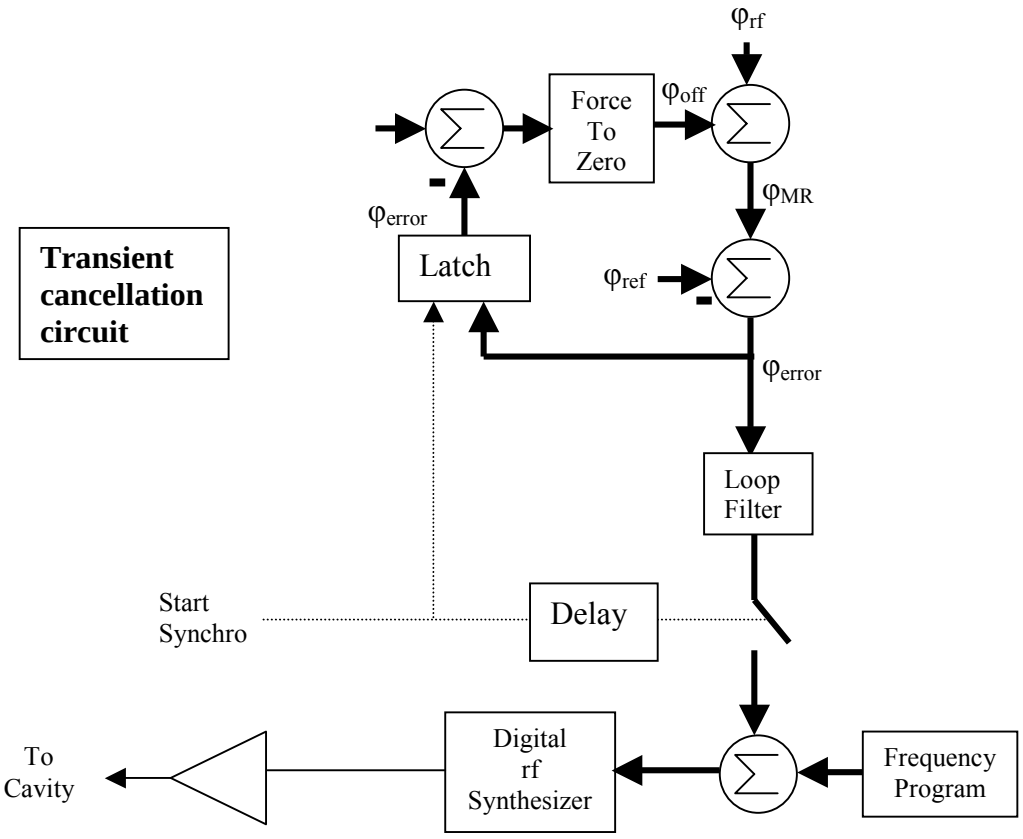
During the accelerating cycle, the frequency addition of offset and rf (= F_{MR}) is equal to reference.

$$F_{off} + F_{rf} = F_{MR} \equiv F_{ref}$$

The phases of reference and moving reference thus differ by a constant value: the error signal.

$$\varphi_{MR} = \varphi_{ref} + \varphi_{error}$$

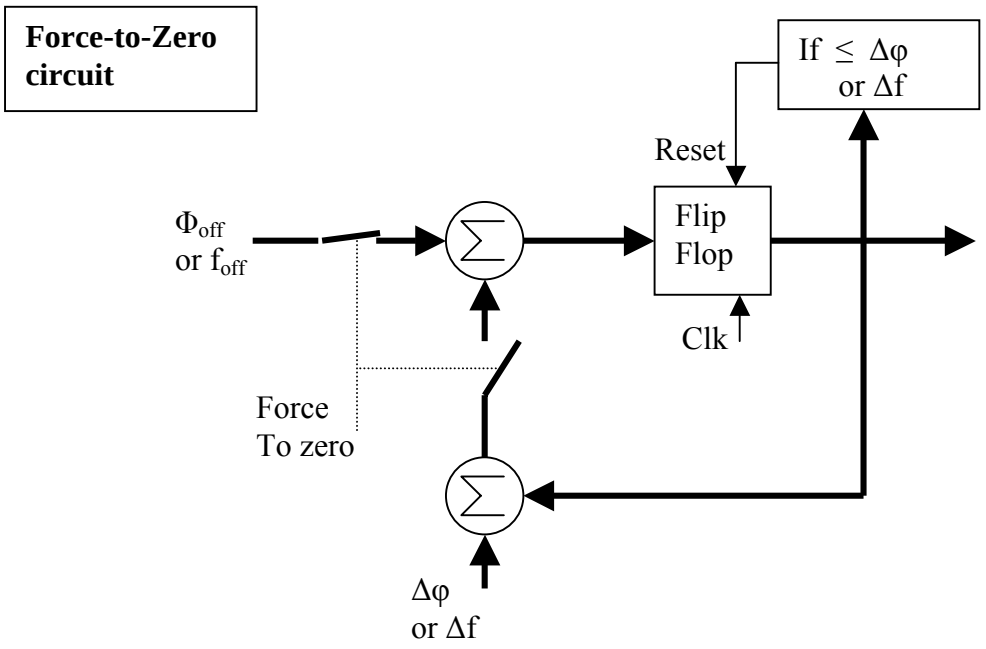
At any time the error signal can be set to zero, by a retro fit of φ_{error} on the moving reference (or offset). This allows to close the synchronization loop without applying any transient to the rf equipment (after a delay corresponding to the propagation time through the summations).



After being closed smoothly, the synchronization loop should have no effect on the main phase loop as the error signal is kept to zero by the very manner the moving-reference is created (feed forward process). It can be interpreted as a zero gain loop.

Then comes the time, during acceleration, where one may decide to take control of the moving-reference. As described earlier, the aim will be to bring the offset smoothly to zero (or to a set value).

The "force-to-zero" will be operated in two stages. First it will be applied to the offset frequency, then to its phase. For simplicity, the decrease might be linear. In both cases the principle is based on an accumulator fed by a slope value ($\Delta\varphi/T_{clk}$ or $\Delta f/T_{clk}$).



When the force-to-zero circuit is not activated, φ_{off} or f_{off} are just passing through (with one clock delay due to the flip-flop). When it is decided to activate the process, both switches are triggered: one is closing the accumulator loop to memorize the last value of φ_{off} or f_{off} , the other is isolating the φ_{off} or f_{off} input. At that time, the force-to-zero progression is entirely determined by the value of $\Delta\varphi/T_{clk}$ or $\Delta f/T_{clk}$ that feeds the accumulator. The sign of ramping coefficient ($\Delta\varphi$ or Δf) needs to be opposite to the one of φ_{off} or f_{off} when starting the process.

7 CONCLUSION

It has been shown how the rf could be compared to the reference signal during the acceleration process by "adding" an offset to the rf such as:

rf + offset = moving reference ≡ reference.

The moving reference represents thus the rf, extrapolated to the reference value in terms of frequency.
As moving reference and reference have the same frequency, they can be phase compared. This artifact allows to close the synchronization loop during acceleration.

It has been shown how rf analogue signals could be transformed into their digital counterparts in terms of frequency and phase words, using a "digital PLL".

The way frequencies are added is explained and makes use of summation of the phase words:

$$(f_{rf} + f_{offset}) \alpha \ (\Delta\varphi_{rf}/T_{clk} + \Delta\varphi_{offset}/T_{clk}) = \frac{\Delta\varphi_{rf} + \Delta\varphi_{offset}}{T_{clk}}$$

The phase step at each clock period represents the frequency. By adding phase steps from different sources, one ends up with a phase progression corresponding to the sum frequency.

If the phase progression of the moving reference needs to be the same as for the reference, the absolute phase of MR is arbitrary. To avoid transients, it will be forced to the same value as the reference value just before closing the loop.

In order to be of any interest to the system, the moving reference needs to represent absolutely (same phase and frequency) the rf at the end of the process. This is made possible by forcing to zero the offset added to the rf while the synchronization loop is closed. First the frequency offset is cancelled at a chosen rate and then the phase. The availability of frequency and phase words makes it easy to achieve this.