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PS/RF/Note 99-06

RF TAGGING & DISTRIBUTION

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Geneva, Switzerland
20 June 1999

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1. Introduction

The “RF Tagging and Distribution” module generates a common h=128 clock “tagged” at the reference revolution frequency (fclock/128). It has been developed for the beam control of the anti-proton production beam in the CERN PS, for the needs of the Anti-proton Decelerator (AD). It would probably be used also for the LHC beam control in PS

Each output is supposed to drive a RF Synthesis module, MHS [1] or MHSDO [2] with a clock at the 128th harmonic of the beam revolution frequency f_{REV}. A "tag" at f_{REV} is transmitted simultaneously with the clock signal so that every synthesizer are phase locked unambiguously.

The RF clock input of this tagging and distribution is provided by the Frequency Translator [3] which transpose 12 to 20 MHz into 53.2 to 61.2 MHz inside the same module. The block diagrams in figure 1 show the basic ideas.

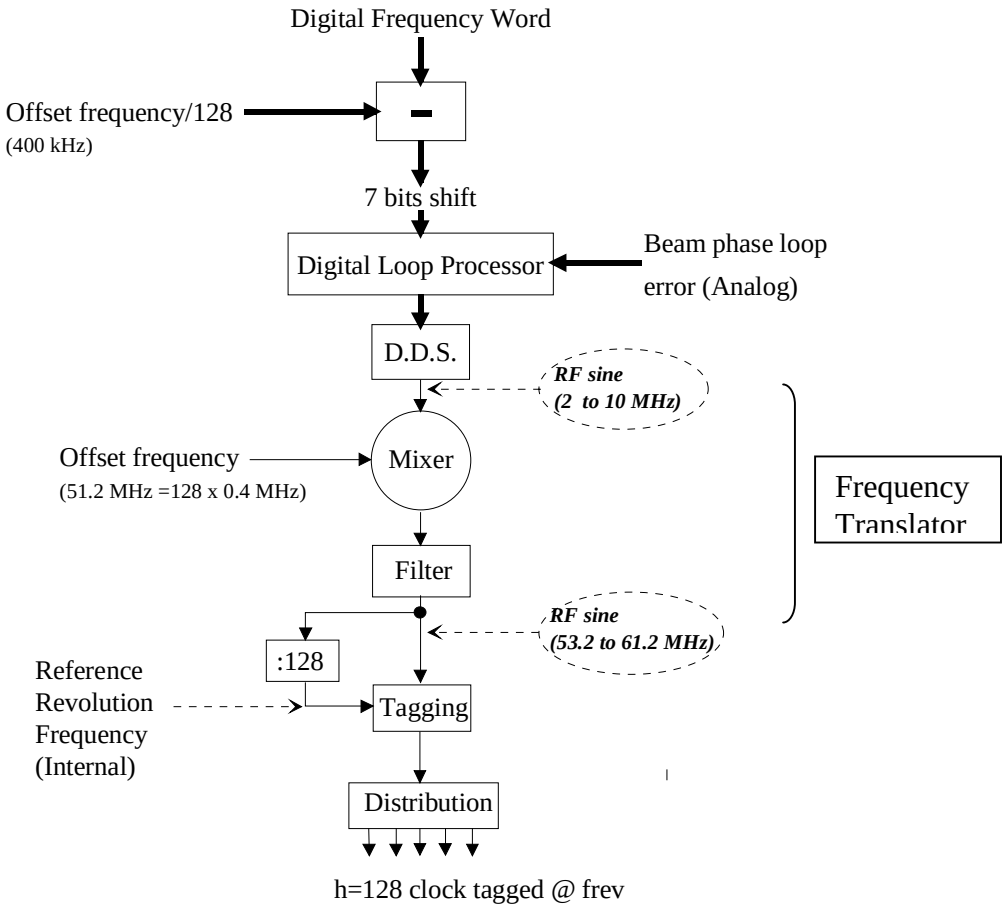

Figure 1: Clock generation @ h=128

2. Principle

The “tag” is transmitted simultaneous with the clock signal by means of pulse width modulation (Fig. 2). This function is implemented inside a re-programmable Altera device (IC6). A 7 bit counter is used to add a short pulse, the “tag”, every 128 clock period. That TTL tagged clock is then converted into a differential ECL form and distributed via clock drivers (Fig. 3).

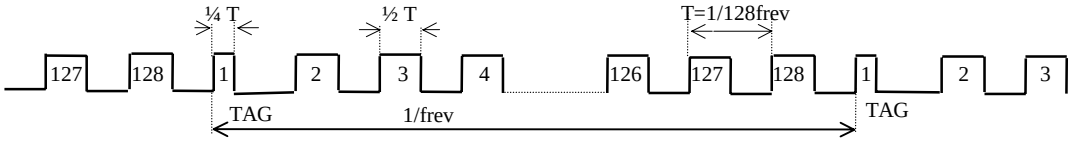

Figure 2

3. Specifications

Size / format:

one slot wide NIM module including the Frequency Translator, the RF Tagging and Distribution.

Input:

RF IN, clock frequency at f_{clock}=128 f_{REV} from Frequency Translator [3] which transpose 12 to 20 MHz into 53.2 to 61.2 MHz. This signal can be ±16dBm, the Schmitt trigger convert it into ECL level.

Outputs:

tagged clock at f_{clock}=128 f_{REV} (14 outputs),

⇒ type: differential ECL level

⇒ required frequency range: 53.2 to 61.2 MHz for the energy range 1.4 to 26 GeV in the PS

Test ***Outputs:***

- TAG’D CK, TTL representation of the distributed clock
- RF IN, TTL representation of the clock at 128 f_{REV} from the Frequency Translator which is inside the same module
- Frev, TTL representation of the revolution frequency

Display:

LED indicating the presence of the 128 f_{REV} signal at the input of the tagging circuit.

4. Module description

The module block diagram is shown on Fig. 3, the schematic capture and front panel (FP) - in Appendix 1. The pulse width modulation is implemented inside a re-programmable logic device (PLD) from Altera, thus the module functionality can changed simply by replacing the configuration of the Altera device.

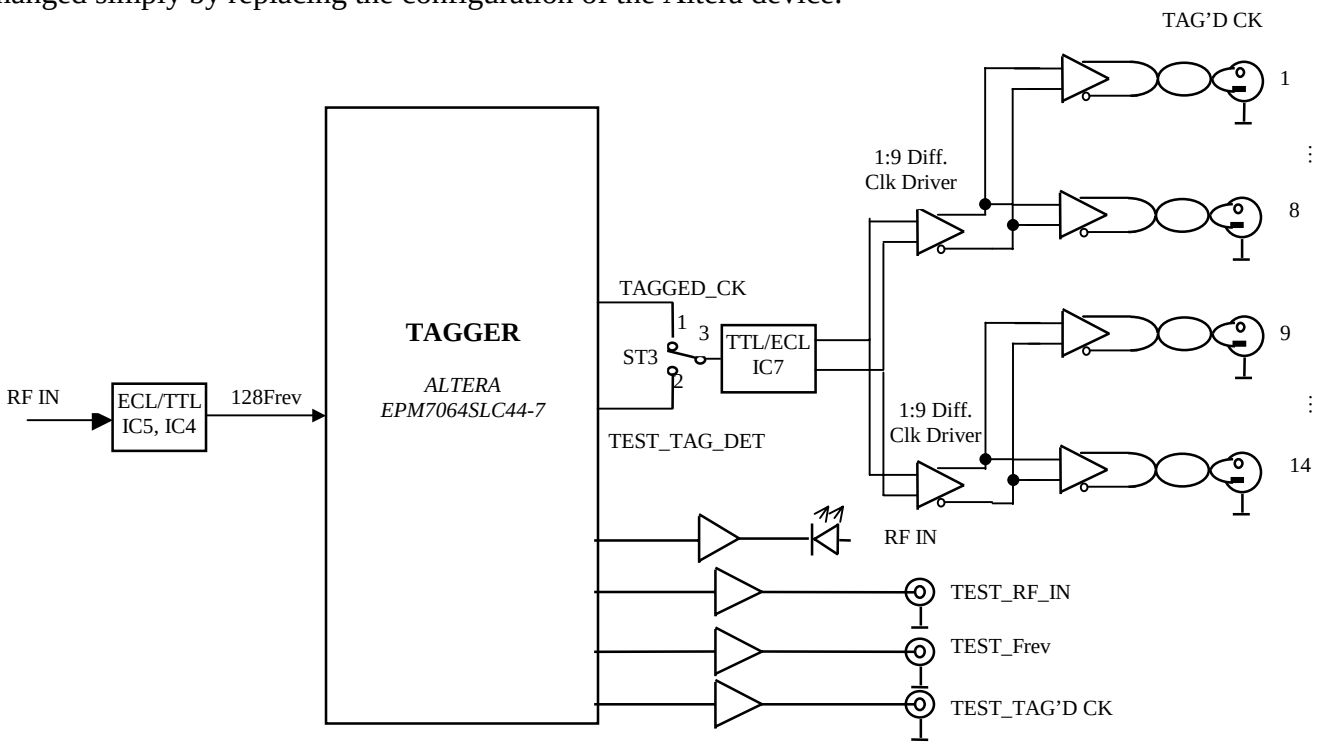

Figure 3

The clock input (RF IN) is converted to a TTL level (IC4) to feed the PLD. The tagging is done inside the TAGGER unit. The h=128 clock tagged at the revolution frequency is converted to differential ECL level and distributed to 14 outputs.

The presence of the input signal is indicated on the FP when the "RF IN" LED is ON.

A test signal providing a tag each 256 Trev instead of 128 is available when ST3 closes pin 2 and 3. When this signal drives a MHS the TAG error detection LED (on MHS) should turn on.

5. The TAGGER unit (Altera device)

The Tagger unit is described as a graphic design file in MaxPlus2 ver8.3 development system - Appendix 2.

All files can be found in G:\home\a\aozturk\Public\tagger\ directory and in the PS/RF data base at the following address: http://wwwps1/psrf/hardware/design.html. The "Tagger.pof" file should be used for programming Altera devices from PC.

6. Test procedure

At first, the Frequency Translator [3] must be tested. See the test procedure in PS/RF/Note 98-20.

Jumper ST1 should close pin 7 and 8, ST2's position is not crucial, ST3 must connect pin 1 and 2 in normal mode.

A variable signal of **+16 to -16dbm** should be applied to the RF IN input in order to adjust P1 so that the TTL level on pin 5 of IC4 does not change in term of duty factor.

The clock signal from the Frequency Translator can be now connected to RF IN input. RF IN indicating LED should turn on

Check then each test output and the 14 TAG'D CK outputs.

The last test may be to check the RF Tagging and Distribution module with a multi-harmonic RF source, applying the tagged clock output to the TCLK input. Verify the TAG error detection plugging the ST3 jumper on pin 2 and 3.

7. Power Supply requirements

+6V	250 mA
-6V	812 mA
+12V	94 mA
-12V	94 mA

8. Conclusion

The RF Tagging & Distribution module will be at the heart of the beam control for the anti-proton production in the PS. One module will be used for tagged clock generation and two modified versions for the clock distribution to the RF synthesiser.

9. Acknowledgements

Thanks to all colleagues for their helpful assistance, which made possible to accomplish this work especially to T. Anguelov, J.L.Vallet, R. Garoby and J. Bento for their shared know-how and practical experience.

10. References

[1] Multi-Harmonic RF Source, T. Anguelov, R. Garoby, A. Ozturk, PS/RF/Note 98-16.
[2] Multi-Harmonic RF Source Delayed Outputs, R. Garoby, A. Ozturk, J.-L. Vallet, PS/RF/Note 99-05.
[3] Frequency Translator, J. Provost, J.-L. Vallet, PS/RF/Note 98-20.

Appendix 1 - The module schematics and layout

Appendix 2 - The TAGGER (Altera device) schematic