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SPARE CAVITY GROUP SELECTION

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Table of content

1. Introduction

The Spare Cavity Group Selection (SCGS) is a double slot wide NIM module. Designed to select the frequency grouping of the spare cavity, it is implemented in a re-programmable Altera device.

It has been developed for the Anti-proton Decelerator (AD) and h=8 & h=16 beam controls in the CERN PS, that's why it can be configured to operate either in serial mode for the AD beam control or pulses mode in the other case.

In serial mode, it will provide the selected group's harmonic number to the Multi-Harmonic RF Source [1] that generates the RF for the spare cavity. In pulses mode, it will generate pulses for selecting the right frequency source.

The group for each cavity can be pre-selected from front panel rotating switches. For each cavity, there are 4 possibilities, 1 to 4. Currently, the cavities are grouped only into 3 or 2 frequencies. The fourth group is intended for future possible beam controls.

2. Specifications

Size / format:

- double slot wide NIM module

Inputs:

- replaced cavity status, from Voltage Program Selector (VPS), parallel input of 10 exclusive bit for the 10 cavities 10MHz in the PS.

- 4 pulses inputs (P1, P2, P3 and P4). These pulses can be blocking level, namely about 20V in 50 Ω and 2μs in width.

- 4 serial pulse inputs (S1, S2, S3 and S4) corresponding to the frequency control word h (harmonic number) of the 4 possible groups. The frequency control word is a serial pulse train of 16 pulses, compatible with GFAS format (16 bit serial, Return to Zero). The first 6 pulses represent the integer part of the harmonic number, the remaining 10 pulses - the fraction. The binary value is pulse width encoded. The format and timing specifications are shown in Fig. 1.

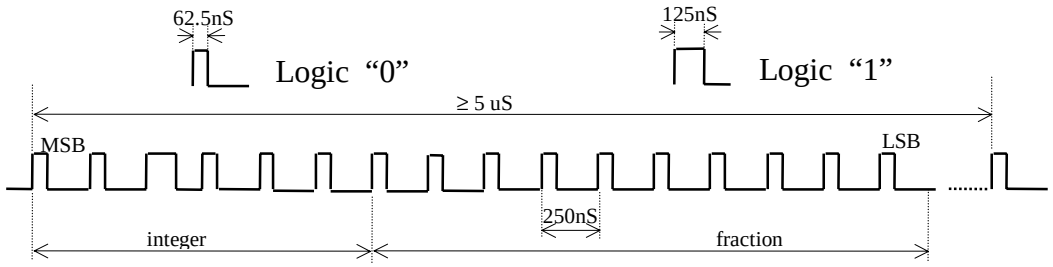

Figure 1

Outputs:

- 2 identical serial pulse outputs corresponding to the selected group.
- 4 pulses (G1, G2, G3 and G4) of +12V in 50 Ω (1μs width) are provided according to the selected frequency group.
- auxiliary output is the duplicate of the replaced cavity status from VPS.

Display:

- LED indicating the replaced cavity
- LED indicating the frequency group to which the replaced cavity belongs to

3. Module description

The module block diagram is shown in Fig. 2, the schematic capture, pcb layout and front panel (FP) - in Appendix 1. The spare cavity group selection is implemented in a re-programmable Altera device (IC6) - the SCGS unit. Thus simply replacing the reconfiguration PROM of the Altera device could change the module functionality.

Fixed function devices are used mainly for interfacing purposes, buffering and pulses generation.

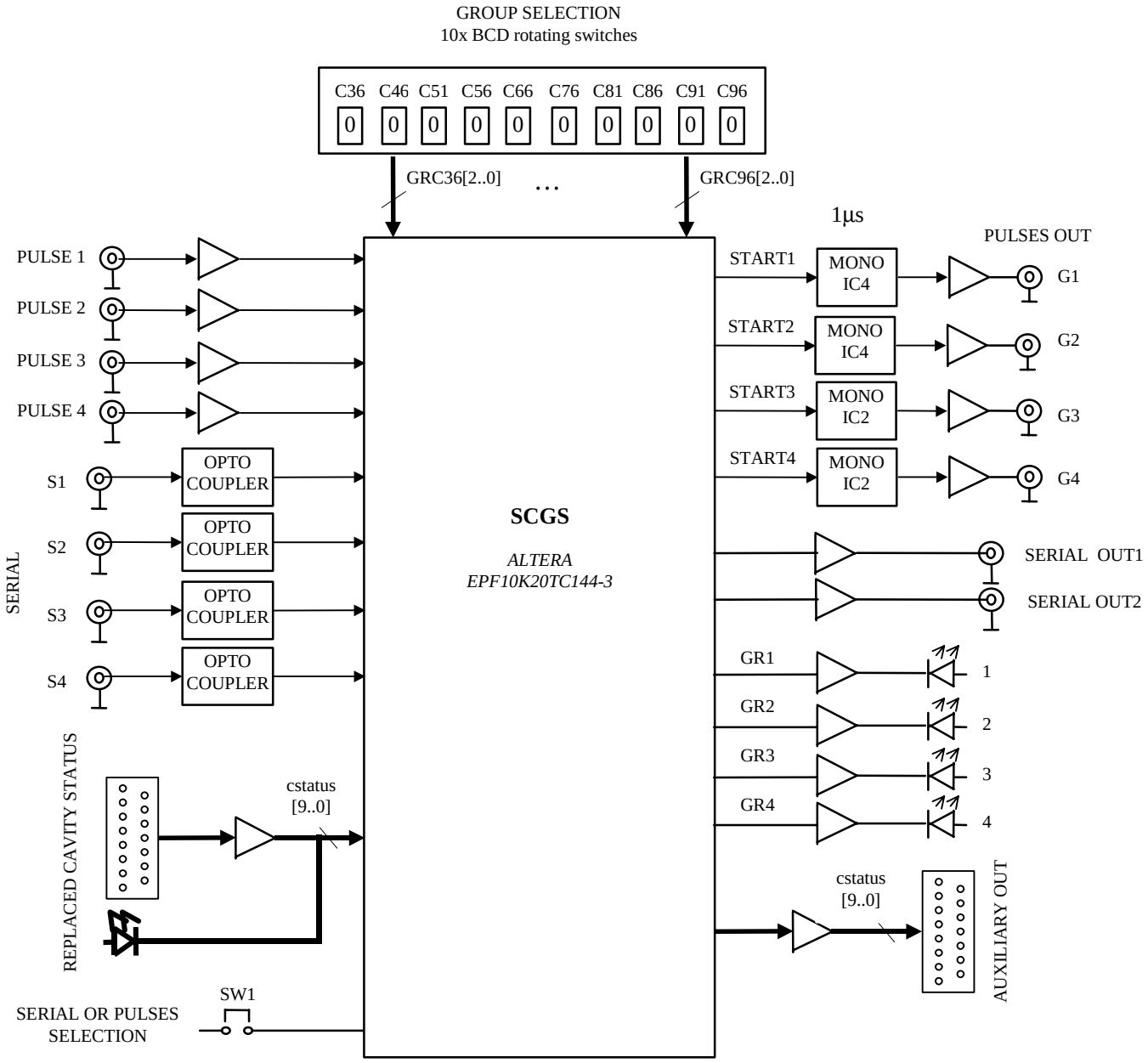

Figure 2

The SW1 jumper is used to configure the module in serial or pulses operation mode.

The ten rotating switches on the FP enable the selection of the frequency group for each cavity.

The parallel input, in TTL bar level, from the voltage program selector (VPS), provides the number of the cavity that must be replaced. The replaced cavity and its group are indicated on the front panel.

The replaced cavity status from VPS is copied out to the auxiliary output

The serial inputs corresponding to h (harmonic number), encoded as described in figure 1, are optically de-coupled. The selected group's input data is transferred to both serial outputs.

In pulses operation mode, the module provide pulses at the selected frequency group output.

4. The SCGS unit (CPLD device)

The SCGS unit is described as a hierarchical graphic design file in MaxPlus2 ver9.21 development system - Appendix 1. The top design file scgs2.gdf contains one subdesign file in VHDL describing logically separated parts inside the SCGS – radio.sym and two macrofunctions 74151 – 8 line to 1 line multiplexer, and 74175 – Quad D-Type Flipflop.

The multiplexer is used to select the output serial data according to the selected frequency group. The flipflop is not used in the current release.

The group settled by FP rotating switches could be from 0 to 4. The BCD (binary coded decimal) value is used to extract the group for each cavity.

All files can be found in G:\home\a\aozturk\Public\Scgs\ directory and in the PS/RF data base at the following address: http://wwwps1/psrf/hardware/design.html.

They can be used as a reference or after compilation - for simulation.

The SCGS unit is implemented into a CPLD (Complex Programmable Logic Device) –EPF10K20TC144-3 from Altera. The reconfiguration data (".sof" file) can be loaded from PC via download cable (Byte Blaster) to the J3 connector on the SCGS board or from configuration PROM – IC1. When download cable is used, the configuration PROM must be plugged out from the socket.

5. Test facility

Test facilities include test points (TP18 – TP1), any internal SCGS signal could be passed to the test points. In the current release user can observe the selected group status (grsel1 to grsel4) at the test points TP1 to TP4, and the received pulses at TP11, TP16, TP17 and TP18. Nevertheless the user could observe any other signals by modifying the SCGS design files.

5.1 Test procedure

The required test equipment is indicated in Figure 3.

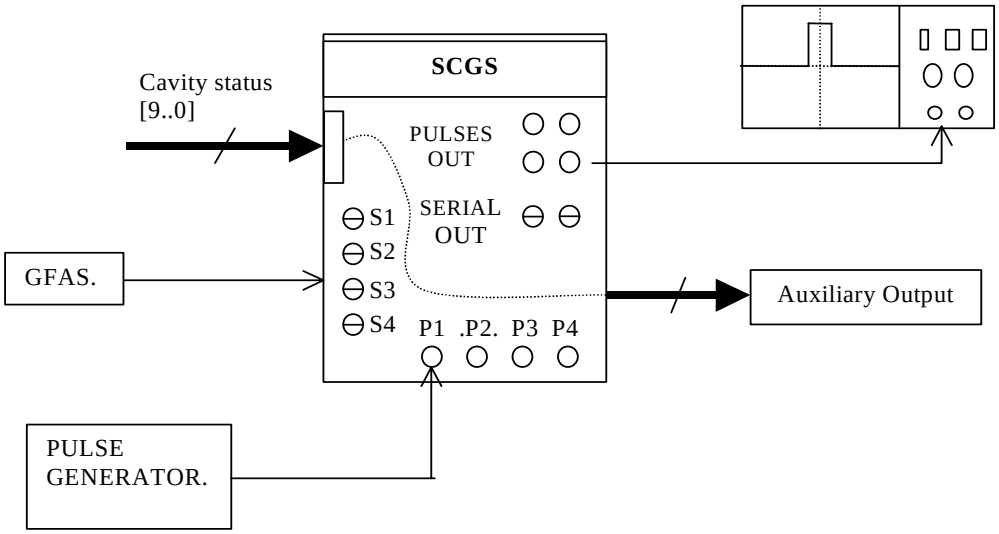

Figure 3 : SCGS module test layout

First, select the cavity to be replaced by the spare one forcing to low level the corresponding input. This status should be copied to the corresponding auxiliary output.

In pulses mode, the SW1 must be plugged in.

Apply a pulse to the selected input and check the corresponding output. This test should be done for each input and all the cavities.

Remove the jumper and then test each serial input and output with any harmonic number received from GFAS system. Repeat this test also for several cavities.

6. Power Supply requirements

+6V 320 mA

+24V 1,3 μA

7. Conclusion

The SCGS module will root one of the serial inputs to the serial outputs or generate pulses according to the selected group. The group selection for each cavity on the front panel of the SCGS will enable easy modification of the cavities frequency grouping.

This module is very compact and efficient thanks to the specific features incorporated into the ALTERA chip.

8. Acknowledgements

Thanks to all our colleagues, for their helpful assistance that made possible the accomplishment of this work.

9. References

[1] Multi-Harmonic RF Source, T. Anguelov, R. Garoby, A. Ozturk, PS/RF/Note 98-16

Data sheet:

1. Altera – ByteBlaster. Parallel port download cable

Appendix 1 - The module schematics and layout

Appendix 2 - The SCGS (CPLD device) schematics