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PS/RF/Note 99-05

MULTI - HARMONIC RF SOURCE DELAYED OUTPUTS

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1. Introduction

The multi-harmonic RF source with delayed outputs (MHSDO) is a modified version of the standard multi-harmonic source MHS [1]. It is designed to generate sine and cosine RF waveforms with a user defined delay. It has been developed for the beam control of the antiproton-production beam in the CERN PS, for the needs of the Anti-proton Decelerator (AD). It would probably be used also in the beam control for triple and quadruple splitting for LHC.

It uses direct digital synthesis techniques to provide an output frequency f_{RF} proportional to a 16 bits digital input word h and to the clock frequency f_{clock}, according to the formula:

$$f_{RF} = \frac{h}{2^{17}} \cdot f_{clock}$$

The phase of the output signal is the sum of the phase accumulator snapshot and the phase offset corresponding to the delay value (from front panel rotating switches), which will provide an automatic cancellation of the differential delay between RF reference and beam PU signal.

The MHSDO is supposed to be driven with a clock at the 128th harmonic of the beam revolution frequency f_{REV}. A "tag" at f_{REV} is transmitted simultaneously with the clock signal by means of pulse width modulation. Whenever the output frequency is an integer multiple of f_{REV} (= when the lower 10 bits of h are at 0), the phase accumulator is reset. This allows to phase lock together unambiguously any number of MHS or MHSDO.

2. Principle

As the MHS, the MHSDO is implemented as a direct digital synthesiser (DDS). The DDS block diagram is shown in Fig. 1.

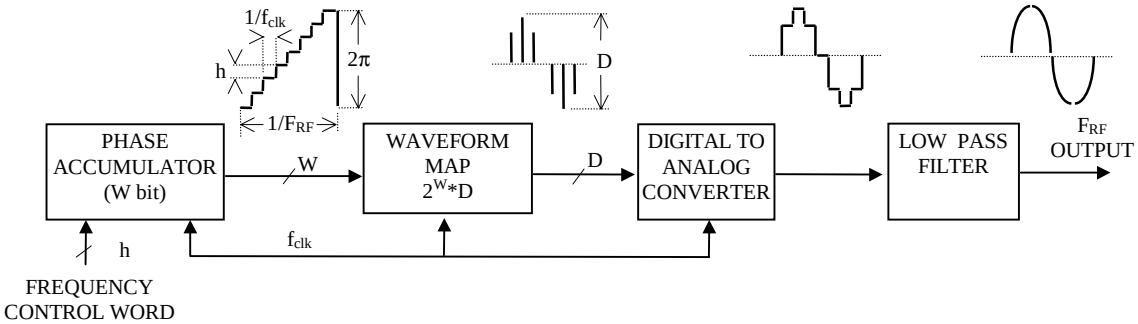

Figure 1

The basic component of any DDS system is a phase accumulator. It increments on each clock with a number given by the harmonic number. This number specifies the phase progression of the output F_{RF}. Any change of h leads to a quasi-instantaneous change of the output frequency without phase discontinuity. This is the most important advantage of DDS comparing to other frequency synthesis methods.

The phase accumulator output addresses a functional mapping device (usually read-only memory - ROM) that transforms the phase snapshot to a number (D) corresponding to the amplitude value of a mapped function. There are two functions simultaneously mapped in the MHS - sinus and cosinus.

An analogue signal is obtained from D by a digital to analogue conversion - DAC. A low pass filter after the DAC rejects the spurious and high order harmonics from the output signal. The output frequency is:

$$F_{RF} = f_{clk} * h \ / 2^W$$

where:
f_{clk} - phase accumulator clock frequency
W - phase accumulator width
h - frequency control word

To satisfy Nyquist theorem stating that $F_{RF} \leq f_{clk}/2$, the harmonic number should not exceed the number $(2^W-1) / 2$.

3. Specifications

Size / format:

- double slot wide NIM module

Inputs:

- clock frequency at f_{clock}=128 f_{REV}, which corresponds to 53.2 to 61.2 MHz for the energy range 1 to 26 GeV in the PS. This clock is transmitted in differential ECL, and pulse width modulation is used to communicate the "tag" at the reference revolution frequency (Fig. 2). Maximum permitted clock frequency: 70 MHz.

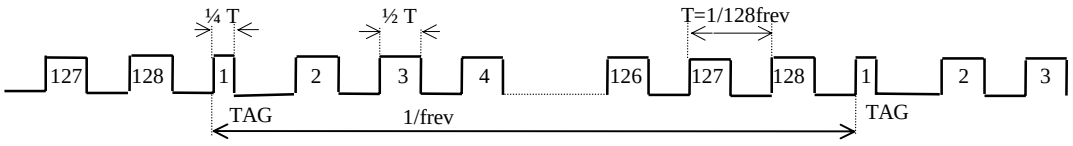

Figure 2

- revolution frequency, from Digital Frequency Program (F REV PROG), parallel input of 24 bits, 23 bits of which represent the revolution frequency and one the strobe. Only 18 most significant bits are used inside the DELAYED_DDS unit.

- frequency control word h (harmonic number), compatible with GFAS format (16 bit serial, Return to Zero). The frequency control word is a serial pulse train of 16 pulses. The first 6 pulses represent the integer part of the harmonic number, the remaining 10 pulses - the fraction. The binary value is pulse width encoded. The format and timing specifications are shown in Fig. 3.

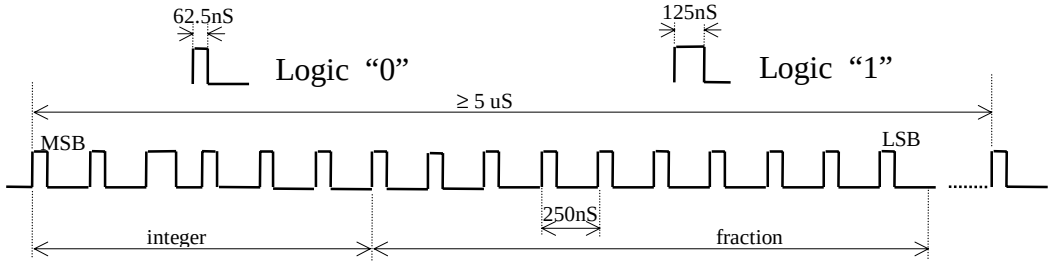

Figure 3

- blank input (TTL, active high) to clear errors indicators on front panel
- sgn input (TTL, active high) to invert the sign of the output waveforms.

Outputs:

- sine and cosine waveforms at

$$f_{RF} = \frac{h}{2^{17}} \cdot f_{clock} = \frac{h}{2^{10}} \cdot f_{REV}$$

⇒ amplitude: +10 dBm in 50 Ω (2 Vpp),
⇒ required frequency range: 3.4 to 10.1 MHz
[Maximum possible output frequency: 10.7 MHz]
⇒ maximum spurious level: -60 dBc

Test Outputs:

- analogue voltage proportional to the control word - h (2,5V for h = 32)
- analogue voltage proportional to the RF- h*F REV (2,5MHz/V)
- analogue voltage proportional to the phase offset -φ OFFSET (50mV/°)

Display:

- LED indicating an error in the transmission of harmonic number (see page 7)
- LED indicating a bad clock transmission by detection of a missing tag

Special features:

- 17 bits phase accumulator

- output waveform phase control taking into account the delay (in nanosecond) which is entered using front panel rotating switches.
- phase synchronisation when crossing an integer harmonic number. The phase accumulator reset takes place on the first tag after the harmonic number h has reached an integer value. Tag to output action takes approximately 300 ns (pipelined ROM plus filter delay).

4. Module description

The module block diagram is shown in Fig. 4, the schematic capture, pcb layout and front panel (FP) - in Appendix 1. The phase accumulator, phase control logic, sinus ROM, error detection and test logic are implemented in a re-programmable Altera device (IC13) - the DELAYED_DDS unit. Thus the module functionality could be changed by simply replacing the reconfiguration PROM of the Altera device. Fixed function devices are used mainly for interface purposes, filtering, buffering and digital to analogue conversion.

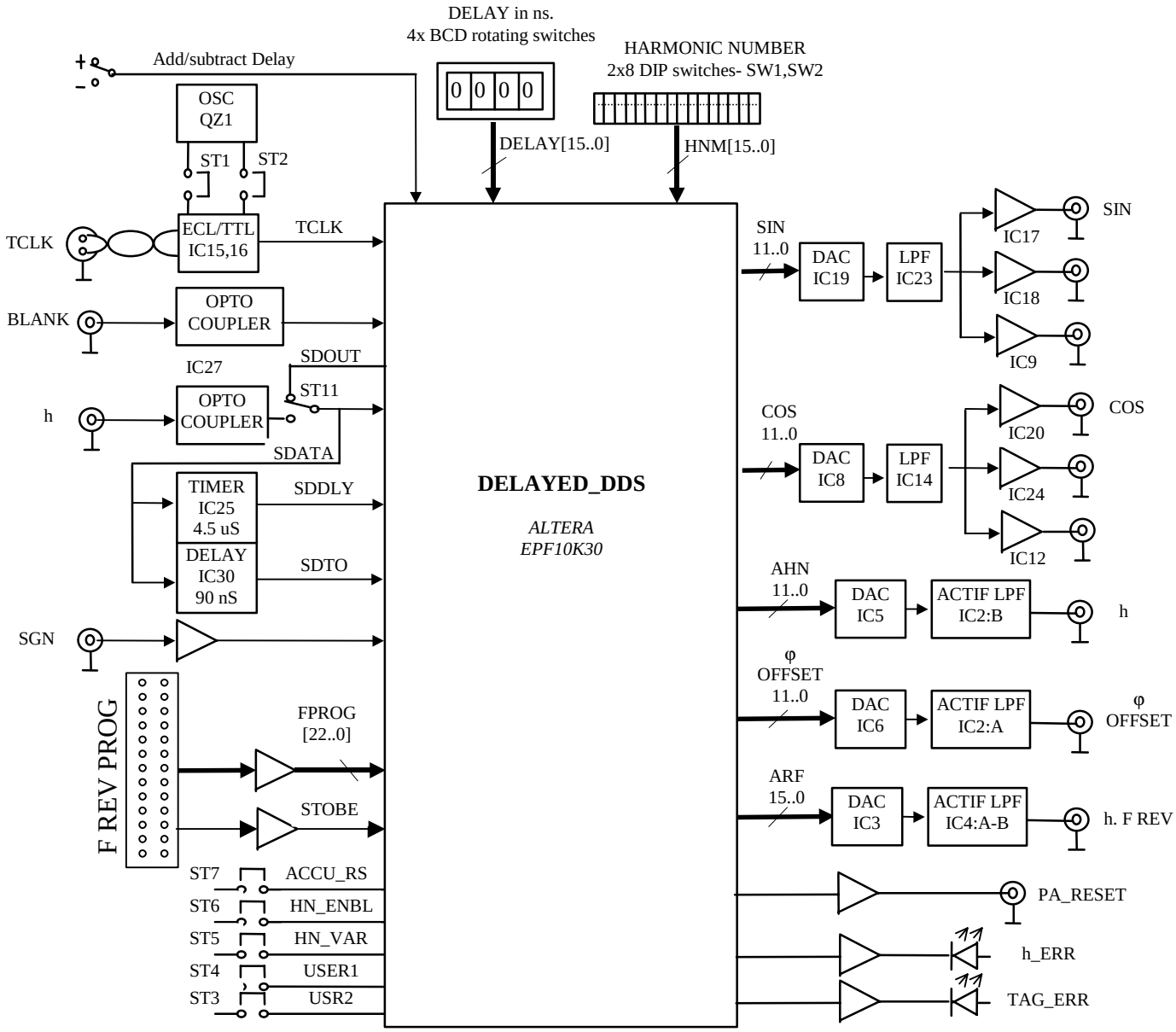

Figure 4

The differential ECL clock on the clock input (TCLK) input is converted to a TTL level (IC15, IC16). The tag detection is done inside the DELAYED_DDS unit. Tag de-synchronisation is indicated on the FP as TAG error LED is turned on. A local oscillator without tag (QZ1) is provided for test purposes.

The h (harmonic number) input, encoded as described in figure 3, is optically decoupled. A delay line (IC30) delays incoming pulse train (SDATA) by 90 ns. The delayed signal (SDDLY) is used for self-extraction of a harmonic number value. The first train pulse triggers a timer IC25 which generates a time out pulse (SDTO), used for pulse train error detection. If the number of pulses received within time-out period differs from 16 a h ERROR indicator is switched on. To test the MHSDO without an external

harmonic number source a test signal (SDOUT) is provided. The test pulse train is encoded by means of two 8x DIP switches – SW1 and SW2.

The BLANK input clears error indicators.

The SGN input enables the output signals inversion.

The four rotating switches on the FP decimally encode the delay that must be applied to the output waveforms with a nanosecond precision. The decimal value is converted into binary by the d2b block of the DELAYED_DDS unit. The phase offset corresponding to the delay is added to or subtracted from phase accumulator according to a position of the FP switch (+/- DELAY).

Digital outputs for the sinus and cosinus waveform SIN[11..0] and COS[11..0] are converted to their analogue equivalent by digital-to-analogue converters SPT9713 - IC8 and IC19.

The low pass filters (IC14, IC23) after DAC are Chebishev type from Mini Circuits.

The outputs are buffered by closed loop buffer amplifiers (IC17, IC18, IC9, IC20, IC24, IC12).

An analogue representation of the last received harmonic number is provided on the **h** output. The most significant 12 bits of 16 bit digital harmonic number are converted by the DAC AD667 (IC5). A 500Hz, 2-pole, active low pass filter rejects the spurious and high order frequency from the output signal. The full scale is 5V for h = 64.

An analogue representation of the phase offset corresponding to the delay is provided on the **φ OFFSET** output. The most significant 12 bits out of a 16 bit phase offset are converted by an offset binary configured DAC AD 667 (IC6). The sign of this offset depends on the position of FP switch (+/- DELAY). A 500Hz, 2-pole, active low pass filter rejects the spurious and high order frequency from the output signal.

An analogue representation of the RF corresponding to the integer part (6 bit) of the harmonic number multiplied by 18 bit revolution frequency can be observed on the **h*F REV** output. The most significant 16 bits out of 24 bit digital RF are scaled so that the DAC AD6999 (IC3) gives 2.5 MHz per volt. A 2kHz, 4 pole active low pass filter rejects the spurious and high order frequency from the output signal.

✍ **Remark**: The active filters have been calculated from the table II in the AD706 Operational Amplifier data sheet, using a scaling factor.

Jumper ST3 – ST7 are used for test and debugging.

5. The DELAYED_DDS unit (CPLD device)

The DELAYED_DDS unit is described as a hierarchical graphic design file in MaxPlus2 ver9.21 development system - Appendix 2. The block structure of the DELAYED_ DDS core logic is depicted on Figure 5. The top design file delayed_dds.gdf contains four subdesign files describing logically separated parts inside the DEALYED_DDS - a decimal to binary converter (d2b.gdf), a test harmonic number

generator (hnm.gdf), a harmonic number multiplier and synchronism signal provider (hmult_sync.gdf) and a sinus/cosinus mapping block (sincos.gdf). The content of the sinus function ROM is in two files - sinc.mif and sinf.mif. All files can be found in G:\home\a\aozturk\Public\Delayed_mhs\ directory and in the PS/RF database at the following address : http://wwwps1/psrf/hardware/design.html. They can be used as a reference or after compilation - for simulation.

The DELAYED_DDS unit is implemented into a CPLD (Complex Programmable Logic Device) –EPF10K30RC240-3 from Altera. The reconfiguration data (".sof" file) can be loaded from PC via download cable (Byte Blaster) to the J14 connector on the MHSDO board or from configuration PROM - IC29. When download cable is used, the configuration PROM must be plugged out from the socket.

The logical units are described in this document by the function name (in capitals) and a unique number given by the development system on the left bottom corner of the unit symbol - for example LPM_SHIFTREG:20. The internal signal names are in italic in the following text and with light characters on schematic capture.

5.1 Phase accumulator

The harmonic number is self extracted from the incoming pulse train at LPM_SHIFTREG:20 by clocking the shift register with the same pulse train delayed by 90 ns. At the end of the last pulse the harmonic number is synchronised with *TCLK* and loaded into harmonic number register - LPM_FF:23.

The phase accumulator is implemented into LPM_ADD_SUB:92 as registered adder whose output is fed to one of the inputs. The other input is driven from harmonic number register LPM_FF:23. The phase accumulator is reset by a pulse *parst* from DFF:127. The *parst* is` active when *pend_rst* is active and is synchronised by tag strobe - *tagstb*.

The *pend_rst* (pending reset) is true when the current harmonic number has an integer value (detected by LPM_OR:240 as all ten LSB equal zero) and that integer is different from the previous last integer harmonic number (output of the comparator LPM_COMPARE:110). The condition for a pending reset is stored in the DFF:117 until *tagstb* resets it

The signal *tagstb* is active when either a tag (the output of the DFF:382) arrives or an internal tag image *f/128* is generated. The internal tag is synchronised with the external tag and replaces it in the case of a missing tag. This improves module reliability.

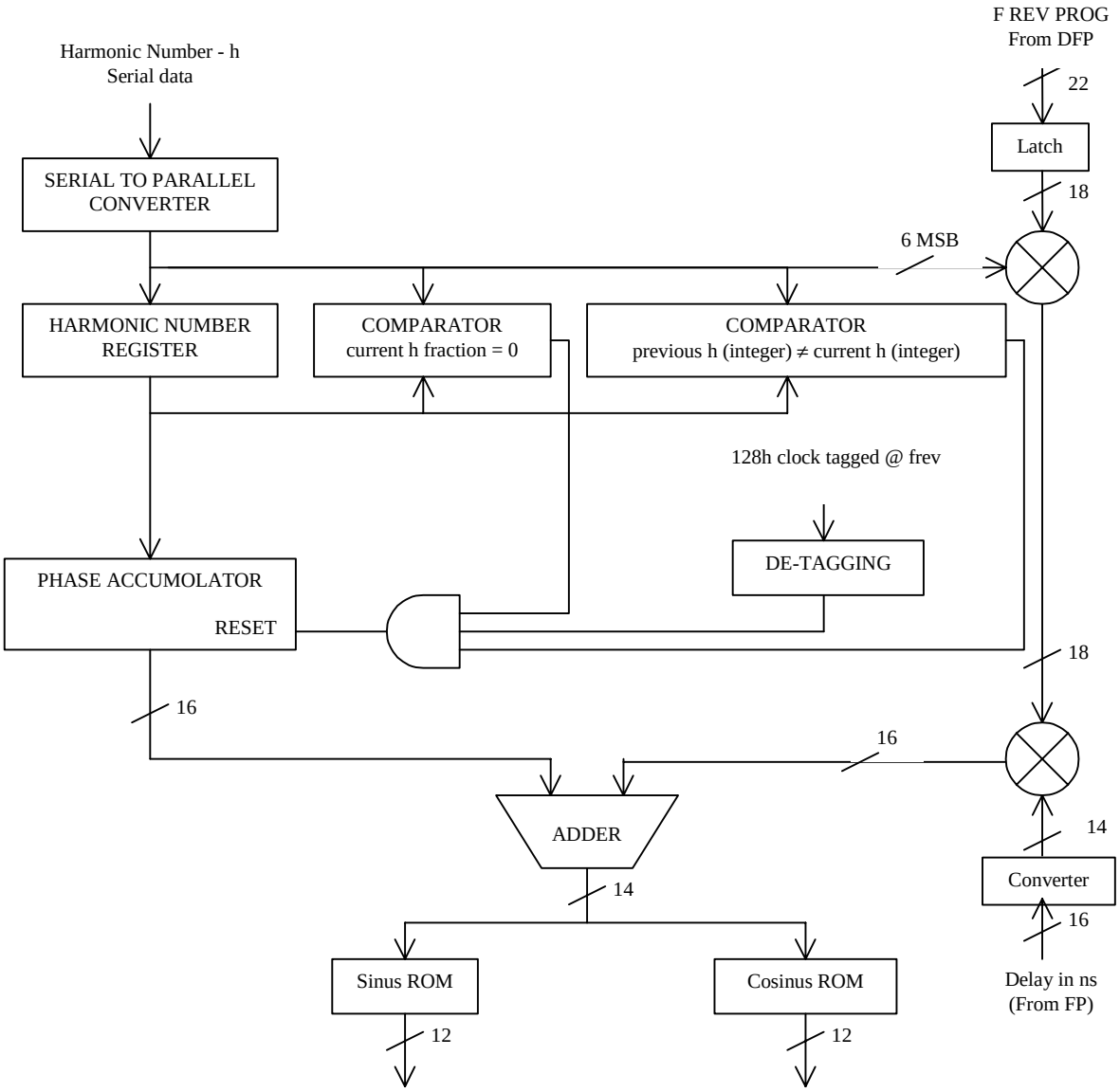

Figure 5

5.2 Phase offset

A phase offset *po[15..0]* is added to (depends on the position of the front panel +/- switch) or subtracted from phase accumulator value in LPM_ADD_SUB:108. The output of this adder is truncated to 14 bit and is used as ROM address bus.

The phase offset is obtained from parallel multipliers implemented with LPM_MULT:563 (inside the *hmult-sync* subdesign files) which multiplies the 6 most significant bits of the harmonic number by the 18 most significant bits of the revolution frequency and LPM_MULT:538 which multiplies the result of the previous multiplier by the binary value of the delay.

The 18 most significant bits of the revolution frequency are received on each STROBE, double synchronised with TCLK and loaded into LPM_FF: register that is clocked by sync3 (Fig. 6). The 6 most significant bits of the harmonic number are loaded with the same signal, sync3, so that data do not change during multiplying operation. The output of this first multiplier is truncated to 18 bit and loaded into DFF: register on sync2. An analogue representation of this digital RF signal can be observed on the h*F REV test output.

The delay settled by FP rotating switches could be from 0 to 9999 ns in 1 ns increment. The BCD (binary coded decimal) value is converted to 14 bits hexadecimal value from 0 to 31FEh by “d2b” converter. This value is latched with sync2 signal and multiplied by the digital RF signal to form corresponding phase offset which is synchronously loaded with sync1 into DFF:541 register.

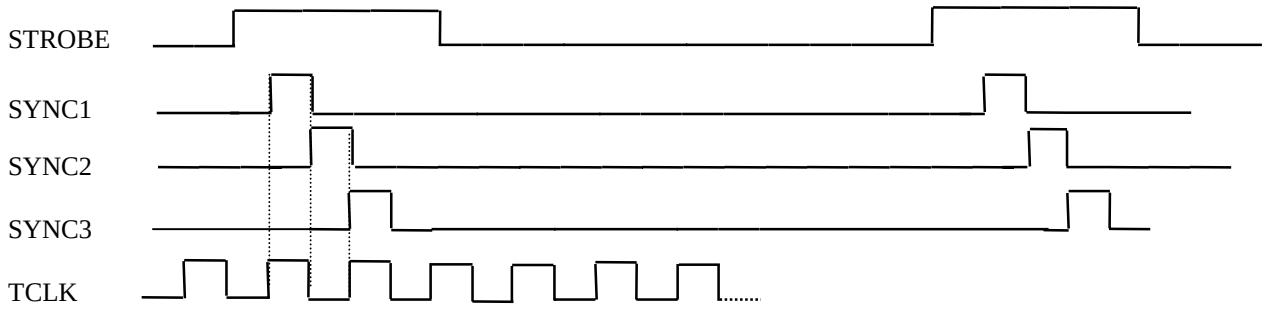

Figure 6 : Synchronism signals

5.3 Sinus ROM

See Appendix 1 for schematics and PS/RF/Note 98-16 for explanation of the implemented ROM.

5.4 Error detection

The harmonic number error is detected whenever the number of pulses on the h input differs from 16. The error detection logic (OR2:291 and DFFE:282) uses time-out pulse *SDTO* to check the actual number of pulses (from LPM_COUNTER:24). The *SDTO* is externally generated by IC25.

A tag error is generated whenever the received tag does not lag exactly by 128 clock periods from the preceding one. The LPM_COUNTER:285 is synchronised by the first tag and together with LPM_AND:284 and DFF:433 generates an internal tag - *f/128*. The internal tag is XOR-ed with the external tag in XOR:305 and the mismatch arms a latch DFF:461.

The *BLANK* clears both error indication.

6. Test facility

Test facilities include test points (TP7 – TP1), a 3MP-connector (J15) and predefined or user defined control inputs (ST7 – ST3). Any internal DELAYED_DDS signal could be passed to the test points. The 3MP connector can be used to observe any signal with a decimal display. In the current release the test point TP7 is used as sign input and 17 pins of the 3MP connector are tied to the phase accumulator bus but the user could observe any other signals by modifying the DELAYED_DDS design files. The predefined control inputs are:

- Phase accumulator reset (ACCU_RESET) – ST7. When a jumper is plugged in ST7 the phase accumulator is reset and stays zero until the jumper is removed. This is used to check the impact of the delay switches on the SIN and COS outputs.
- Enable an internally generated harmonic number (HN_ENABLE) – ST6. SW1 and SW2 define the internal harmonic number value. The bottom SW2 position encodes the first pulse in a pulse train. The top SW1 position encodes the last pulse. The internal harmonic number can be used when a selector ST11 is in position that connects SDOUT with SDATA. One internal harmonic number is generated when the pin 31 of ST6 is connected to the pin 24 of ST3.
- Variable harmonic number (HN_VAR) – ST5. When a jumper is plugged in ST5 the internal harmonic number does not depends anymore of SW1, SW2. Instead a variable harmonic number is generated on each plugging out of a jumper on ST6 or a positive TTL level edge on pin 31 of ST6. A positive TTL level edge is available on pin 26 of ST4. When theses pins are connected the harmonic number increments from h = 8 to h = 20 and back to h = 8.
- User may define the ST4 and ST3 to implement any other possible test or control function of DDS.
- The phase accumulator reset *parst* is fed out of DELAYED_DDS unit for test purposes and is available on the FP as PA_RESET high impedance output.

6.1 Test procedure

The required test equipment is indicated in figure 7. The configuration of the DFP is depicted in figure 8

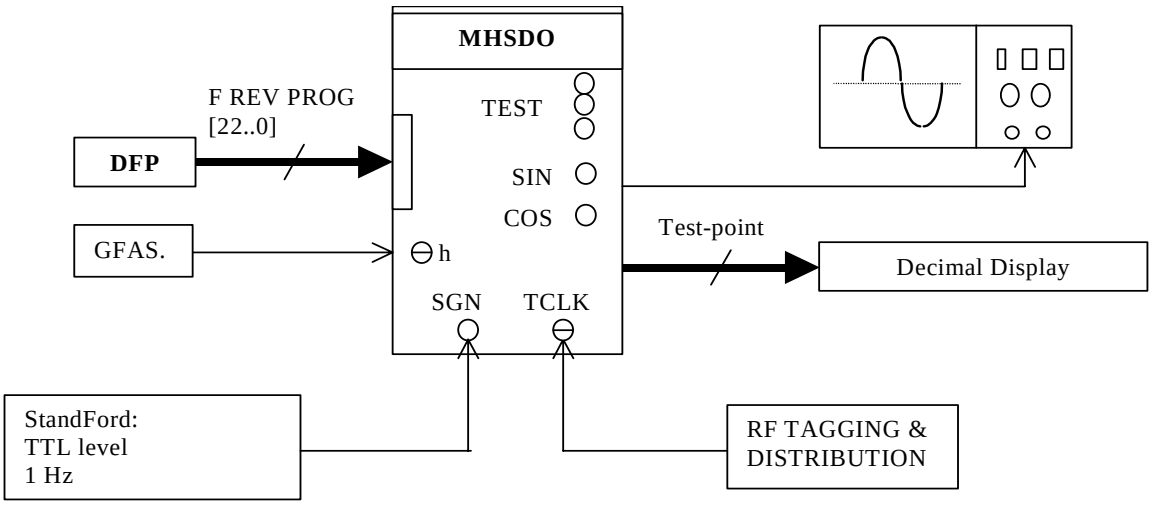

Figure 7 : MHSDO module test layout

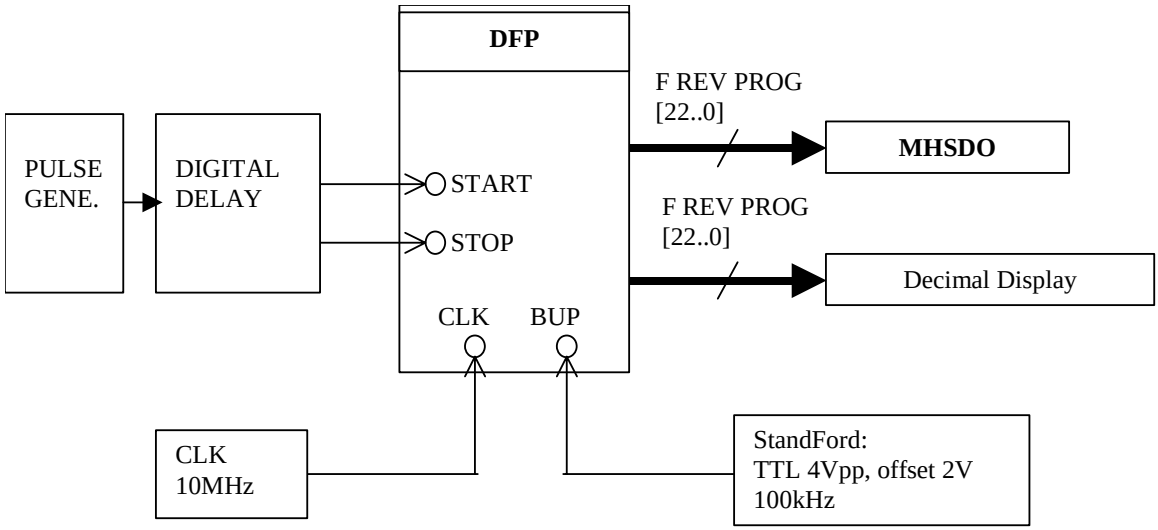

Figure 8 : DFP module Configuration layout

The module can be tested using the internal clock from QZ1 – the both jumpers ST1 and ST2 must be plugged in. From SW1 and SW2 the user can specify the harmonic number which will be generated on the output SDOUT when the ST6 is plugged out. The pins 21 and 22 of the ST11 should be connected.

To generate variable frequency waveform which correspond to harmonic number from 8 to 20 ST5 should be plug in and low frequency clock applied to pin 31 of ST6. Pin 26 of ST4 is a low frequency output that can be used for this purpose.

Reset accumulator function could not be tested with the internal clock source since it does not generate tagged clock. To test this function a clock distributor module [3], generating a tagged clock is needed. The both jumpers ST1 and ST2 must be disconnected. The external tagged clock (ECL differential levels) is applied to the TCLK input.

When the harmonic number is received from GFAS system the ST11 should closes pins 22 and 23.

Plugging a 50Ω resistor can test the BLANK input. This action should turn off error indicators.

When a TTL signal is applied to SGN input, the sign of the output waveforms is inverted on each positive edge. This may be observed with an oscilloscope. It is also possible to measure the 180° phase jump using an auxiliary Phase Discriminator module and a standard MHS configured with the same harmonic number. This test equipment can also be used to compare the **φ OFFSET** test output with the Phase Discriminator's ΔΦ output(Figure 9).

The following figures illustrate the output signals form. This measurement have been done with :

- DELAY = + 5 µs
- local harmonic number h = 10
- TCLK = 55MHz
- DFP: 380 ms delay between Start and Stop pulses.

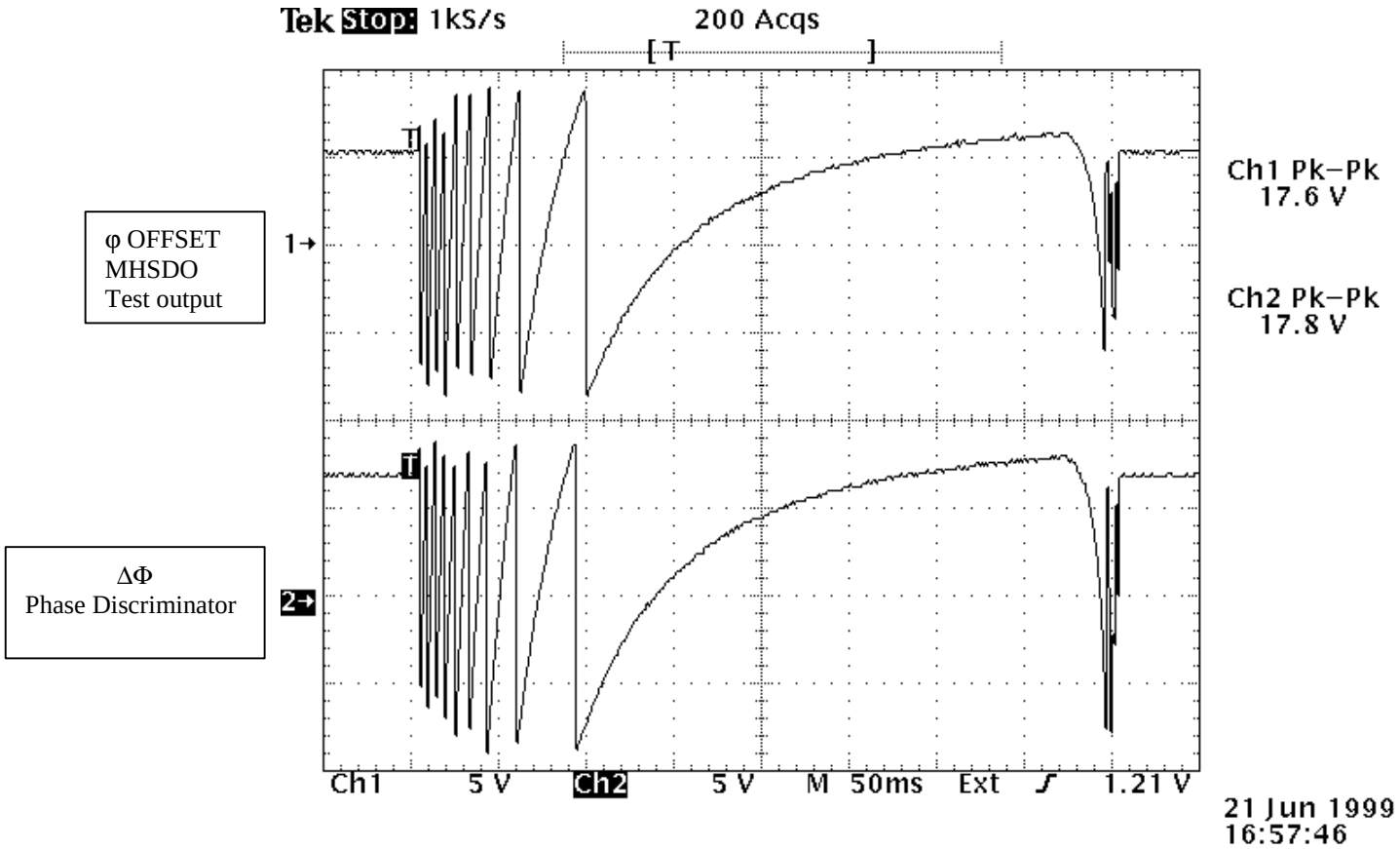

Figure 9 : Phase offset compared to the ΔΦ from an auxiliary Phase Discriminator module.

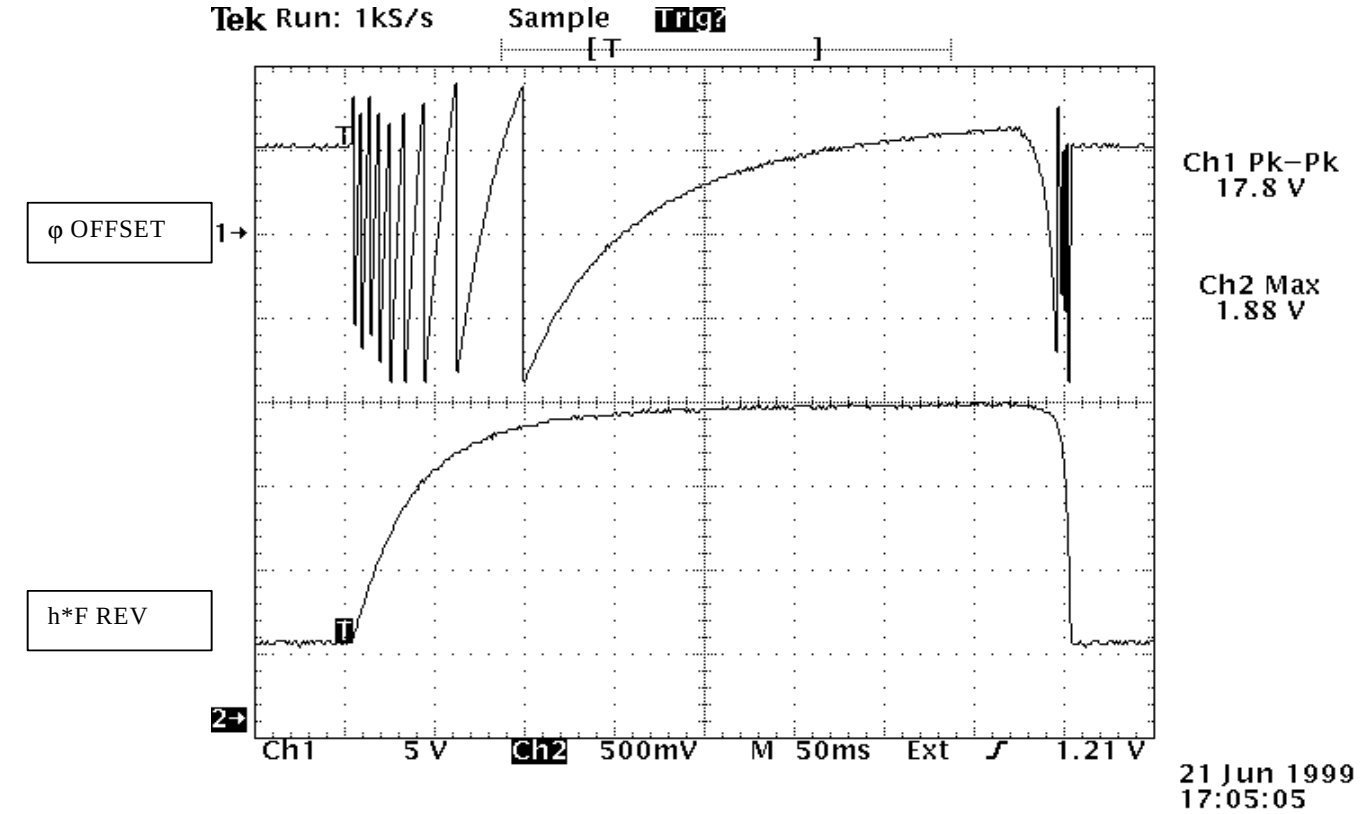

Figure 10 : Phase offset and h*F REV test outputs

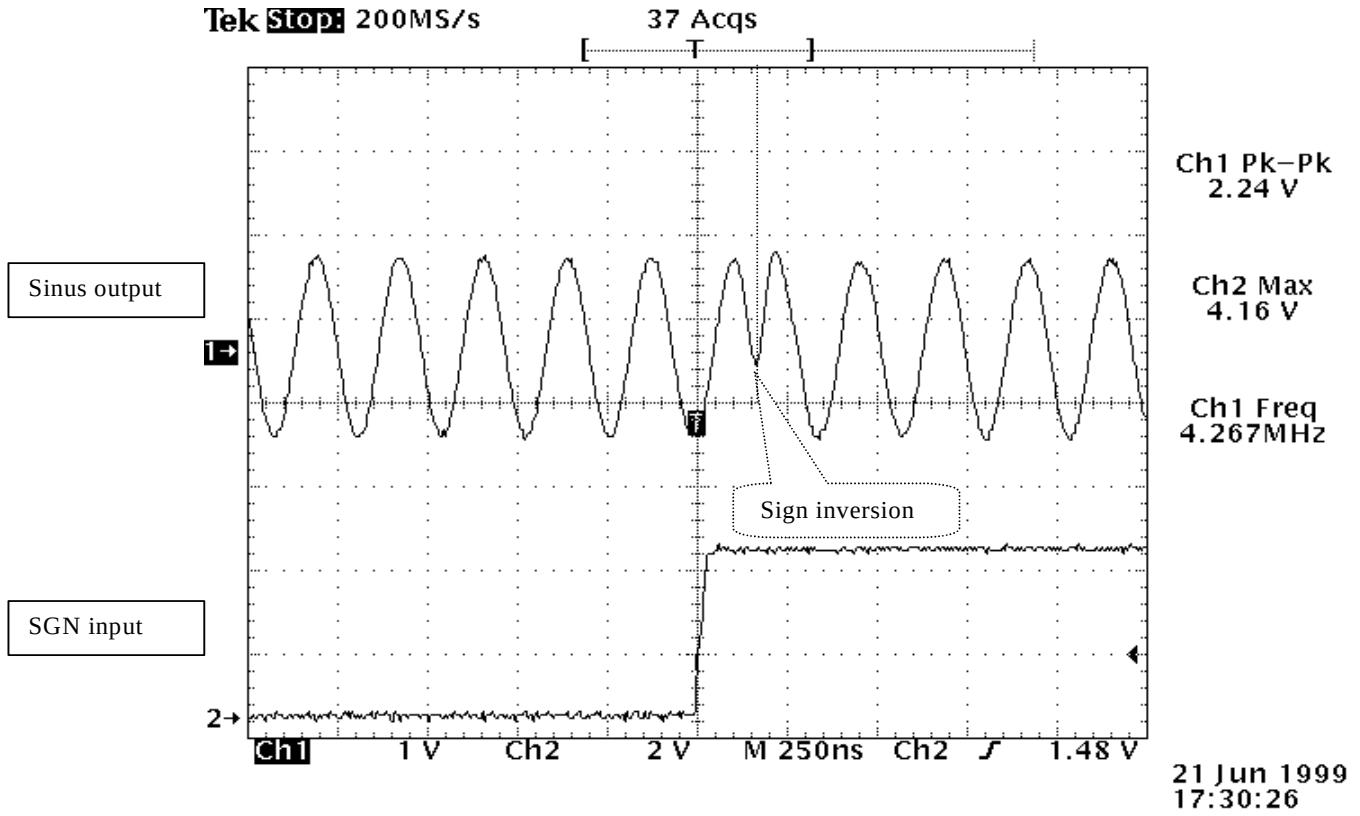

Figure 11 : Sign inversion observed on sinus waveform.

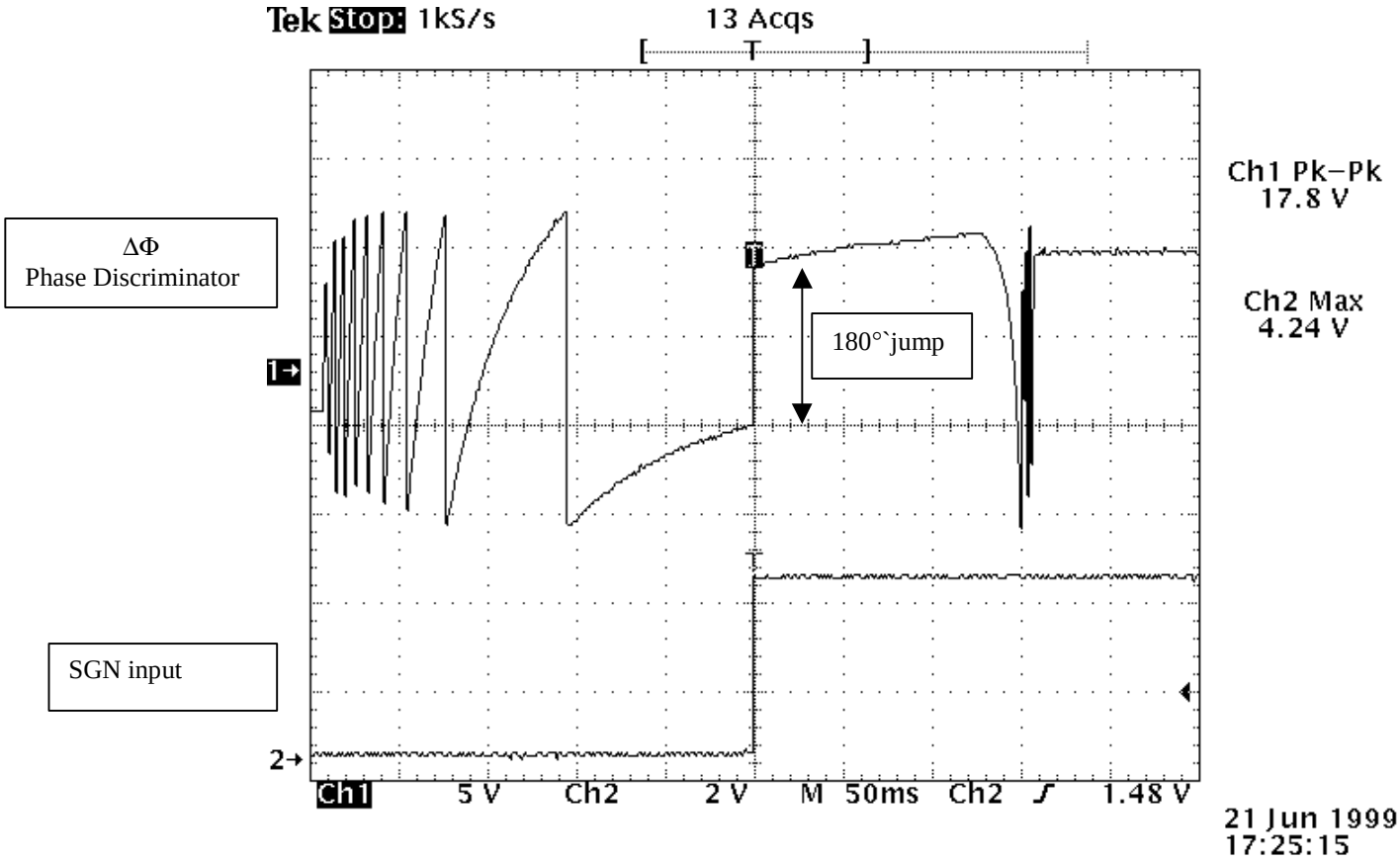

Figure 12 : 180° phase jump on the positive edge of SGN signal.

7. Power Supply requirements

+6V	1.6 A
-6V	0.48 A
+12V	0.03 A
-12V	0.05 A

8. Conclusion

The MHSDO module will drive the sine and cosine inputs of a Digital Phase Discriminator (DPD) module which will measure the beam phase in real time during the changes of harmonics and provide the possibility to have a phase loop during the gymnastics of Batch Compression. The delay control on the front panel of the MHSDO will provide an automatic compensation of the differential delay between RF reference and beam PU signal.

This 2 modules phases measurement set-up is very compact and efficient compared to classical alternative. Moreover, much less external control parameters and interconnections will be required, thanks to the specific features that could be incorporated into the ALTERA chip.

9. Acknowledgements

We thank all our colleagues for their helpful assistance that enabled us to accomplish this work.

10. References

[1] Multi-Harmonic RF Source, T. Anguelov, R. Garoby, A. Ozturk, PS/RF/Note 98-16.
[2] Digital Phase Discriminator (DPD), T. Anguelov, R. Garoby, PS/RF/Note 98-17.
[3] RF Tagging and Distribution, A. Ozturk, R. Garoby, PS/RF/Note 99-06.

Data sheets:

1. Signal Processing Technology - SPT9713 - 12 bit, 100MWPS D/A Converter.
2. Analog Device - AD667 - Microprocessor-Compatible 12-Bit D/A Converter.
3. Analog Device - AD669 - Monolithic 16-Bit DACPORT.
4. Analog Device – AD586 - High Precision 5V Reference.
5. Analog Device - AD9630 - Low Distortion, 750 MHz Closed-Loop Buffer Amp.
6. Analog Device - AD9617 - Low Distortion, Precision,Wide Bandwidth Op Amp.
7. Analog Device - AD706 - Dual Picoampere Input Current Bipolar Op Amp
8. Altera – ByteBlaster. Parallel port download cable

Appendix 1 - The module schematics and layout

Appendix 2 - The DELAYED_DDS (CPLD device) schematics