MEMS Relays for Make-Break Power Switching Applications: {111} Silicon Etched Planar Electrical Contacts

by

Alexis Christian Weber

S.M., Massachusetts Institute of Technology, 2002
B.S.E., Tecnológico de Monterrey (ITESM), México, 1998

Submitted to the Department of Mechanical Engineering
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2008

Author .....
Department of Mechanical Engineering
May 15, 2008

Certified by .....
Alexander H. Slocum
Professor of Mechanical Engineering, MacVicar Faculty Fellow
Chairman of the Comitee, Thesis Supervisor

Certified by .....
Jeffrey H. Lang
Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Accepted by .....
Lallit Anand
Chairman, Department Committee on Graduate Students

MEMS Relays for Make-Break Power Switching Applications: {111} Silicon Etched Planar Electrical Contacts

by

Alexis Christian Weber

Submitted to the Department of Mechanical Engineering
on May 15, 2008, in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

Abstract

Relays and switches are of interest in applications such as test equipment, radar, communications, and power systems, amongst others. Unlike solid state switches, mechanical relays provide galvanic isolation across the power ports. This characteristic is important because, for safety reasons, electrical codes stipulate that loads in certain power applications must be disconnected by open gaps. This requirement imposes significant isolation, heat dissipation, tribology and reliability constraints on a relay.

The objective of this research is to explore power handling by a MEMS device in a relay context. This work presents concepts, analytical performance models, fabrication processes and design rules for MEMS relays capable of hot-switching inductive loads in power applications. To this end, a horizontal-displacement, electrostatically-actuated, MEMS relay for make-break power switching applications is presented. The MEMS-relays are etched in (100) Si through a combination of KOH etching, and DRIE, bonded to a glass substrate, and plated with a 10 μm thick buffer film of either copper or nickel-cobalt, and a 1-2 μm thick film of a platinum-family metal such as palladium, rhodium, and alloyed palladium (palladium-cobalt).

The relays feature {111}-plane silicon-etched electrical contacts. The {111}-plane contacts provide travel of 30-80 μm, which prevents arcing. Their oblique geometry introduces contact wipe, which is known to enhance the contact reliability. Further, the contact geometry allows for an enhanced metallization process which provides lower on-state contact resistance than traditional horizontal displacement MEMS-relays. Experimental relays exhibit a best-case total on-state contact resistance of 130 $m\Omega$, a response time of 750 μs, a settling time of 3 ms, electrical isolation in excess of 1 kV (tested to 997 V with available equipment), a hot switched current of 800 mA using resistive loads, and a hot switched current of 350 mA using a 1 mH inductive load. The relays have been hot-switched in excess of 10^5 cycles without signs of performance degradation.

Thesis Supervisor: Alexander H. Slocum
Title: Professor of Mechanical Engineering, MacVicar Faculty Fellow

Thesis Supervisor: Jeffrey H. Lang
Title: Professor of Electrical Engineering and Computer Science

Acknowledgments

Graduate school at MIT has been an incredible journey of discovery both academically, personally, and professionally. I am honored to have had the opportunity of collaborating with a wonderful group of faculty, staff and fellow students who have made this research possible. Besides academics, MIT and Cambridge have provided a rich environment for personal development. Non of the work here presented would be possible without the, advice, support, guidance, encouragement and help from many people.

- Alex Slocum and Jeff Lang for their enthusiasm, enduring patience, continuous encouragement and for always being there whether to discuss a design idea, debug a circuit, make sense of the data, or to "jump into the trenches" to make things happen. I could have not asked for better advisors, and better friends.

- Funding for this project has been provided by a major leader in power and automation technologies.

- The founding source Corporate Research Director, Corporate Program Manager, and Business Technology Managers for their continuous support, insightful discussions, and for fostering a strong collaboration.

- National Science Foundation (NSF), for a collaborative grant which supported part of this research in 2007–2008.

- Dr. Hanqing Lee at MTL, for his help and candid advice in the clean room, for his expert advice "tweaking" DRIE etch recipes, for the time shared in the cleanroom and for his friendship.

- Dr. Rod Martens, Dr. Mike Armstrong and Dr. Doyeon Kim at FormFactor Inc. for insightful discussions and help with the electroplating process.

- Robert Pilawa for writing the original LabView code to test the device.

- The MTL staff for process related advice, insightful discussions and for keeping the fab running.

- Fellow lab mates at PERG, past and present. It has been an honor to share lab space, long hours working on problem-sets or research, and preparing for the qualifying exams. Thank you for your friendship.

- Friends in Boston, MIT, Mexico, and beyond for their sincere friendship.

- Dr. Eduardo Torres-Jara, for the interesting conversations, his help with computer related issues and for being the best room mate one could ask for.

- To my family for continuous encouragement, support and for their love.

- Last but not least, to Carissa for the friendly smile, the continuous encouragement, her undying patience, the sparkle in her eyes, and for proofreading this thesis.

Contents

List of Figures

List of Tables

Chapter 1

Motivation and outline

The objective of this doctoral research, is to explore power handling by a Micro-Electro-Mechanical-Systems (MEMS) device in the context of a mechanical switch, or relay.

Switches are electrically or mechanically controlled devices used to make, break, or change electric connections in conductors, such as wires, bus bars, and transmission lines. The toggling function in a mechanical switch is achieved when one or more contacts are displaced between two discrete positions: an isolation position, in which the switch is said to be in its *off-state* or *open-circuit* configuration, and a conductive, or capacitively coupled position, in which the switch is said to be in its *on-state* or *closed-circuit* configuration. The closed circuit configuration can be achieved through *metal-contact* or through *capacitive-coupling.* Switches may be arranged in *series* or in *shunt* configurations. In the case of low frequency and direct current (DC) applications, a metal-contact series switch is normally employed. In a metal-contact switch, the load is energized when the contacts are physically touching each other and ohmic contact is established, as represented schematically in Figure 1-1. When the switch contacts separate, the current flow to the circuit is interrupted and the circuit is turned off.

Switches are ubiquitously employed to control high-voltage circuits with low-voltage signals, to control high electrical current circuits with lower currents, and to isolate the controlling circuits from the controlled circuits.

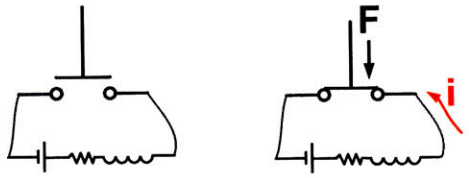


Figure 1-1: Schematic representation of a cross-bar relay arranged in series configuration: (L) device shown in its off-state; (R) device in its on-state. An actuator provides the force needed to displace the moving contacts.

In a strict sense, the term *relay* is used to describe an electromagnetically actuated mechanical switch. However, in the field of Micro-Electro-Mechanical-Systems (MEMS), the terms *relay* and *switch* are often used interchangeably, regardless of the principle of actuation [1]. In this text, the term *MEMS relay* will be used over its synonym *MEMS switch* mostly for historic reasons [2].

1.1 Motivation

Micro-Electro-Mechanical-Systems (MEMS) relays are of interest to academia and industry for applications in commercial and industrial applications, automotive systems, automatic test equipment and instrumentation, satellite communications equipment, radar systems, and wireless communication systems, amongst others. Unlike solid-state devices, mechanical relays provide galvanic isolation between the control and power ports. Relays in telecommunications, for example, may be subject to surges of up to 2.5 kV and several Amperes; these excursions cannot be handled in a reliable manner by conventional radio-frequency (RF) MEMS switches. Electrical codes stipulate that, for safety reasons, loads in certain power-system applications must be disconnected by open gaps; this requirement can neither be fulfilled by solid-state devices nor by conventional MEMS switches. From a performance point of view, mechanical relays are often desired over solid state devices because they offer improved linearity, absence of leakage currents, higher robustness to overload, excess temper-

[1] As an analogy consider the terms *solid state relay* and *solid state switch* which are also used interchangeably

[2] MIT Ph.D. thesis of Jo-Ey Wong in 2000, Jin Qiu in 2003, and Jian Li in 2004

ature conditions, electromagnetic interference, and lower control power consumption [43, 70, 24, 25].

Electromagnetic relays are bulky and cannot be easily integrated with microelectronics. Electromagnetic relays are comprised of more than a dozen components which require labor intensive assembly. The MEMS relays presented in this thesis are comprised of three elements, including the package. MEMS provides the benefits of microelectronic fabrication processes, such as miniaturization, tighter quality and tolerance control, and batch fabrication. MEMS technology allows the integration of transducers and computation on a single package, which could lead to"smart" interruption through the application of appropriate algorithms.

The realization of a reliable MEMS-relay for light-duty (load currents up to 1 A) and perhaps medium-duty (load currents of 1 to 10 A) applications relies on the adequate design of the electrical contacts. In order to achieve reliable performance and a high current-carrying capacity, the contacts must enable low contact resistance in order to reduce Joule heating, and provide a sufficiently large contact stand off to prevent arcing during hot switching.

The contact materials must be both durable and have good electrical properties. They must withstand hot-switching, and provide good electrical properties under light loads, typically in the mN range. Hot-switching is the process of toggling the switch while it is connected to an energized load. Under certain conditions, described in this thesis (i.e. inductive and capacitive loads), hot-switching may quickly degrade the electrical contacts.

1.2 Thesis Outline

This thesis presents a study on power handling by a Micro-Electro-Mechanical-Systems (MEMS) device in the context of a relay. To this end, concepts, analytical performance models, fabrication processes, design rules, and horizontal-displacement, electrostatically-actuated, MEMS relays for make-break power switching applications are presented. The published MEMS relay literature is reviewed in Chapter 2. This

section also discusses contact materials and contact architecture. Chapter 3 discusses the functional requirements of a MEMS relay for power switching applications and presents analytical mechanical, thermal and electrical models for the relay. The next chapters present the design, fabrication, and test of the relays in chronological order. The first device fabricated, *MEMS relay 1*, is presented in Chapter 4, and the second device fabricated, *MEMS relay 2*, is presented in Chapter 5. Next, conclusions are drawn and future work is outlined in Chapter 6. Finally, a concept for an out-of-plane motion MEMS relay with {111}-contacts is presented in Chapter 7.

Chapter 2

Background and Literature Review

MEMS relays have a rich history dating back to the late 70's. One early example is Kurt Petersen's seminal paper on "Micromechanical Membrane Switches on Silicon" [40]. The majority of the publications on MEMS-relays focus on switching of signals, particularly in the Radio-Frequency (RF) spectrum, commonly referred to as *RF-MEMS*.

While many aspects between signal-switching and power-switching devices overlap, there are also important differences. Consider, for example, the main functional requirements of RF-MEMS relays, as follows. Indicated in parenthesis is the desired state.

- Insertion loss (minimize)
- Isolation (maximize)
- Linearity (increase band-width)
- Response (minimize response time)
- Cross talk (minimize)
- Size (minimize)
- Actuation power (minimize)

Consider now the main functional requirements for MEMS relays for power-switching applications. They are as follows.

- Current carrying capacity (maximize)
- Contact resistance (minimize)
- Stand-off voltage (maximize)
- Arcing (maximize reliability)
- Thermal management (maximize reliability)
- Material transfer (minimize)
- Electrotribology (minimize wear)

Previous reports in the literature for MEMS power relays point to the need for improved performance to meet the desired power requirements. For example, surface electroplated contacts [30] with electrostatic actuation exhibit low contact resistances (e.g., 30 mΩ) and maximum current capacity of 1-2 A, but have an open gap of only 3 μm which limits the stand-off voltage to less than 300 V (Section 3.6). Power relays with larger current capacity (e.g., 3 A) and larger open gaps (e.g., 10 μm) exist, however, they also exhibit much higher contact resistances (e.g., 100-1300 mΩ) [42], [56]. Similarly for signal relays [72], the reported contact resistances are too high and the current carrying capacities are too low to support the power required for the proposed applications. Additionally, none of these relays has an open gap approaching 25-100 μm, as is required to safely stand off the six hundred volts typically encountered in light duty and medium duty power switching applications. In each of these cases, the lowest contact resistances were observed for those surfaces with the lowest surface roughness. Most of the literature relating to microfabricated electrical contacts describes the use of gold and its alloys. Gold, however, is too soft and has too low a melting point for make-break hot-switching applications. The material of choice for telecommunications and signal relays is palladium due to the combination

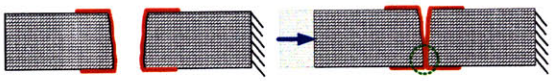


Figure 2-1: Horizontal displacement contacts, schematic

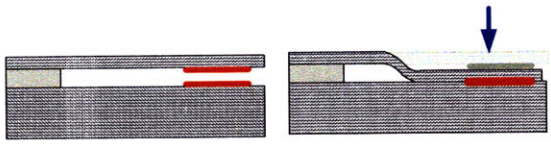


Figure 2-2: Vertical displacement contacts, schematic

of good electrical, and excellent mechanical and electro-tribological performance. Refractory metals are preferred over gold for their durability, in spite of lower thermal and electrical conductivity. Further discussion on materials is given in Section 3.4.3.

2.1 Contact architecture in MEMS-relays

MEMS-relays can be grouped, based on the configuration of the contacts, into vertical displacement, or horizontal displacement, metal contact or capacitive devices [43]. Devices with vertical displacement contacts, shown in Figure 2-2, are characterized by having limited contact travel in the order of 1-5 μm and contact resistance values down to the order of 30 μm [30]. Devices with horizontal displacement contacts, shown in Figure 2-1, have larger contact travel, in the order of tens of μm to one hundred μm but have rough, non parallel contact surfaces, on which it is difficult to deposit metal. Because of the small effective contact area, horizontal displacement contacts exhibit large contact resistance values on the order of tens of Ω [41] [56]. A MEMS switch with electroplated Au horizontal displacement contacts has been reported to maintain a contact resistance of 10 mΩ for 10 billion cycles [50] while cold-switching. The low contact resistance on this switch is attributed to the structure flatness, density and low surface roughness of the electroplated contacts. The durability is attributed to a self cleaning effect due to the contact geometry. However, the structural material of this device is SU-8, a photo curable epoxy based resin [16], which makes the device not suitable for power switching applications because of the materials thermal and

structural properties.

2.2 Current capacity and stand-off voltage

Figure 5-43 shows the stand-off voltage, also known as the break-down voltage and the current carrying capacity of MEMS relays cited in the literature. This graph differentiates between hot-switched data (relay is cycled with a load) and cold-switched data (relay is cycled without a load, once the relay is closed the load is connected). Many of the previously published relays exhibit a maximum voltage-standoff below 325 V. This voltage matches the minimum breakdown-voltage of air at 1 atmosphere, as described by Paschen's law (Fig 5-28). Most relays falling in this category have contact travel on the order of $1 - 10\mu$m, and are typically out-of-plane contact motion relays. Relays with lower breakdown-voltage (i.e. 200 V) probably experience breakdown of dielectric thin-films and not breakdown at the contacts. A discussion on electric breakdown is given in Section 3.6. Only the relay presented here, and JPL's magnetostatic switch [69] exhibit a breakdown-voltage of 1000 V.

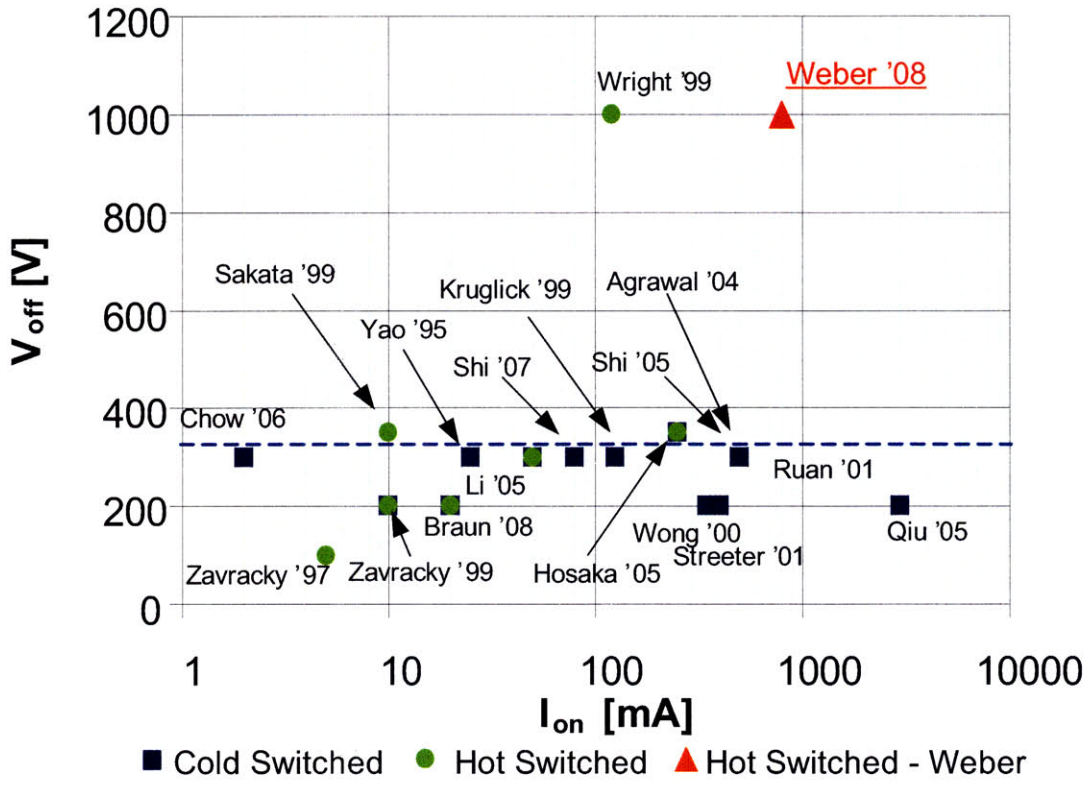


Figure 2-3: Voltage-standoff and current-carrying-capacity comparison of *MEMS relay 2* to previously published MEMS relays. Notice that many of the previously published relays exhibit a maximum voltage-standoff of 325 V, the minimum on the Paschen curve in air, as indicated in Fig 5-28.

Chapter 3

MEMS-relay analysis and design

This chapter describes the analysis and design of the MEMS relays with particular emphasis on the relay contacts. The relay's functional requirements are defined and constraints inherent to microelectronic processes and materials are reviewed. A {111} contact error budget is used to determine the effect of fabrication tolerances on the etched contact geometry, specifically on the travel and overlap of the contacts. The characteristics of the KOH etch bath used, such as the (100)/(111) selectivity and mask undercut, are determined through test patterns. Electro-mechanical models based on elastic deformation, plastic deformation, and electrical constriction are presented. A description on contact material selection follows. Several thermo-mechanical models are used to predict the maximum current capacity of the MEMS contacts.

3.1 Functional requirements of a MEMS-relay for make-break power switching applications

The MEMS relays in this thesis are developed for light-duty (load currents up to 1 A) and medium-duty (load currents of 1 to 10 A) make-break switching. The target specifications are to reliably hot-switch currents on the order of 1 A, and to provide galvanic isolation in excess of 600 V. Based on these specifications, the following

functional requirements are identified.

- Galvanic isolation, is the principle of electrically separating functional sections of a circuit such that no current can flow between the isolated sections. For our application, we seek electrical isolation in excess of 600 V between the control and load terminals, and between the two load contacts when the relay is in an open state.

- Low electrical contact resistance, is desired in order to reduce Joule heating and thus increase the current carrying capacity of the relay.

- Large contact stand-off or contact travel. A minimum separation between two electrical contacts must be maintained to prevent arcing. For arcs operating in air at atmospheric pressures, the minimum distance is on the order of 10 μm as expressed in Paschen's law [71, 20]. Contact erosion, material transfer and formation of nano-wires [39] may lead to unwanted bridging of the contacts, thus a larger contact separation in excess of 30 μm is preferred.

- Contact wipe. Small amplitude sliding motion at the contact interface after ohmic contact has been established is known as *contact wipe* or *contact scrub* [51]. Wipe affects the reliability and performance of the contacts. Controlled wipe can provide lower weld forces and remove contaminating films such as oxides and frictional polymers which increases reliability. In an extreme case, contact wipe may lead to fretting. For the relays developed in this thesis, controlled contact wipe is desired to improve reliability.

- Reliable contact materials. Relay contacts are subject to failure mechanisms induced by electrotribological effects. Corrosion may arise in dry environments causing oxidation, in wet environments causing pore and creep corrosion, and by fretting. Contact erosion may be caused by pure mechanical stresses leading to wear, thermal stresses leading to creep and thermoflow, and thermally accelerated mechanisms. Other important electrotribological effects such as arc-opening and bridge transfer may cause contact erosion or hot spots leading

to performance degradation and even contact failure. Contact materials must have good electrical properties and durability. Good electrical properties are essential to provide low and stable contact resistance at light loads. Hard and corrosion resistive materials are essential to prevent material transfer and contact adhesion. Contact materials should also have high minimum arc-voltages and arc-currents, as well as, high melting and boiling temperatures.

In addition to the functional requirements, the following constraints inherent to MEMS-materials, microelectronics processes, and MEMS-devices must be considered.

- Actuation forces. Actuation principles include electrothermal, piezoelectric, electrostatic, and magnetic. Typical actuation forces range from $50\,\mu$N to $300\,\mu$N for electrostatic actuators, and on the order of mN for electrothermal actuators. Each actuation principle has its own set of performance advantages and limitations, such as, switching speed, operating voltages, power requirements, drift, hysteresis, etc. A minimum force must be applied on the contacts to achieve a stable contact performance. The value of the minimum closing force depends on the contact material, and ranges from 0.1-0.6 mN for soft metals, such as gold (Au), to 5-10 mN for hard metals, such as ruthenium (Ru) [47]. An opening force must be applied to overcome contact adhesion forces. The adhesion force is material dependant, and ranges from 0.15 mN for hard materials such as rhodium, 0.45 mN for hard gold (AuNi5), and over 4 mN for gold [47].

- Actuation travel, for vertical-displacement electrostatic actuators, and horizontal-displacement electrostatic actuators in MEMS is typically on the order of 1-5 μm and $100\,\mu$m respectively. A horizontal displacement device is the only candidate to achieve large enough standoff to meet the breakdown-voltage requirements.

- Surface forces. In most MEMS devices, adhesion and other surface forces dominate. Typical adhesion forces of soft metals can be as high as 0.1-2.7 mN [47]. Metal adhesion must be overcome by large enough restoring forces supplied by either actuators and/or springs in order to open the contacts.

- Processing of metal films in MEMS. The contacts in horizontal displacement MEMS-relays are difficult to metallize through evaporation and sputtering due to the limited projected area. Also difficult to metallize are the acute angled corners between the wafer surface and the perpendicular trench. This leads to high contact resistance and thus limits the relay's current carrying capacity.

3.2 Electrical contact architecture

Based on the functional requirements of low contact-resistance, large contact separation, and reliability, the oblique contacts shown in Figure 3-1 have been conceived. The contacts consist of atomically parallel {111} silicon surfaces fabricated through wafer-front and wafer-back side anisotropic etching of silicon using a crystalline orientation dependant etchant - potassium hydroxide (KOH) - solution. In essence, the {111} contacts are fabricated as follows. A self terminating V-groove is etched on the wafer top-side with KOH, indicated by the red triangle in Figure 3-1(b). Next, the etched geometry is passivated through nitride or oxide, and a self terminating V-groove is etched on the wafer back-side using KOH solution, indicated by the blue triangle in Figure 3-1(b). An offset between the wafer-top and the wafer-bottom KOH masks produces the substrate's contact geometry shown in Figure 3-1(a). A thermal oxide is then grown on the patterned silicon substrate to provide electrical isolation. A conductive film is then deposited on the oxidized, patterned substrate through e-beam evaporation. A detailed description of the process is given in Sections 4.2, 5.3, and in Appendices A.1, A.2.

The {111}-plane contacts offer several advantages over traditional MEMS-relay metal contacts, such as vertical displacement contacts (VDC) and horizontal displacement contacts (HDC). VDC, shown in Figure 3-2, have a contact travel on the order of 1-5 μm [43, 70]. This is less than the 30 μm required to withstand contact erosion [39] and the 10 μm required to prevent arcing [71]. Traditional HDC, shown in Figure 3-3, have resistances on the order of 1-10 Ω [42, 56]. This leads to excessive Joule heating while handling the currents in our application. It is difficult to deposit metal

onto these contacts making continuity challenging. The {111} contacts [65] provide large travel on the order of 30-70μm, which prevents arcing, and introduce contact wipe known to enhance the contact reliability [51].

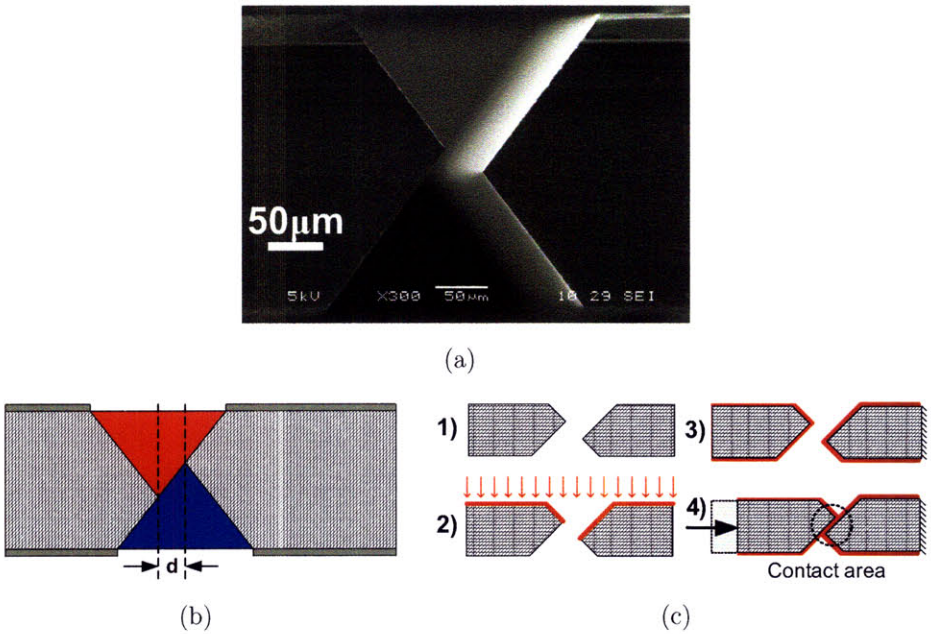


Figure 3-1: {111} Si etched planar electrical contacts. (a) Fabricated {111} contacts. (b) Fabrication schematic. The contacts are fabricated by etching a self-terminating v-groove on the wafer top side (red), followed by passivation, and a self terminating v-groove etched on the wafer bottom-side (blue). (c) Metallization schematic. (1) {111} contacts. (2) wafer top-side metallization. Next, metal is deposited on the wafer back (not shown). (3) Metallized relay contacts in open-state. (4) Metallized relay contacts in closed-state.

Most engineering surfaces have significantly higher roughness values and higher flatness errors than the {111} contacts. Classical contact theory [19] dictates that contact resistance is a function of the contact force and of the hardness of the contacting bodies, and that contact resistance is independent of the dimensions of the contacting bodies. For this reason, the contact geometry of choice for classical (meso-scale, light-duty and medium-duty electrical contacts), as well as most out of plane moving MEMS contacts (RF MEMS), are spherical bumps or spherical on flat bumps [10].

It is hypothesized here, that the {111} contact architecture may enable lower

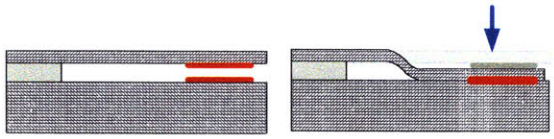


Figure 3-2: Vertical displacement contacts, schematic

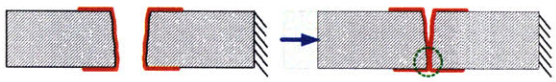


Figure 3-3: Horizontal displacement contacts, schematic

closed-state electrical and thermal contact resistance in MEMS-relays than that obtained by vertical-displacement and by horizontal-displacement MEMS contacts. This argument was elucidated as follows. The contacts are complimentary and parallel: atomically parallel as they are etched in single crystalline silicon along parallel crystalline planes, and planar with nanometer-scale roughness. As these surfaces touch, larger effective contact area may be achieved than in traditional vertical contacts which have significantly higher roughness values and larger parallelism errors. However the metal films deposited onto the {111} contacts through e-beam evaporation exacerbated the roughness of the patterned substrate.

A particular advantage of the {111} contacts is that the oblique geometry allows for an enhanced metallization process. This results in better corner coverage between the wafer surface and the contact. Thicker metal is deposited on the contact since there is a larger projected area exposed during metallization. In general, better contact metallization yields lower contact resistance.

3.2.1 Crystalline orientation dependant etching

Certain aqueous alkaline solutions, such as ethylenediamine-pyrocatechol-water (EPA), alkali-hydroxides, such as potassium-hydroxide (KOH), and quaternary-ammonium-hydroxides, such as tetramethylammonium-hydroxide (TmAH), have the characteristic of etching crystalline materials at rates which vary with crystalline orientation. Solutions which exhibit this property are known as crystalline orientation dependant etchants (CODE). The difference in etch rates, which can be as high as 150:1

for (110)/(111) for 34% per weight KOH solutions at 70°C, promotes the etching of faster-etching planes, such as {100}, and the exposure of the slower etching planes, such as {111}.

KOH-based etchants are preferred over TmAH because of their faster etch rates, however they can result in rougher surfaces than those obtained through TmAH. The use of KOH saturated with isopropyl alcohol, and the use of surfactants in the KOH solution can reduce surface roughness for certain crystallographic orientations of Si. Cleaning pre-treatments and surfactants can reduce the peak-to-valley roughness by nearly an order of magnitude [14]. The addition of Si and ammonium persulfate additives to the TmAH solution results in a Ra of 40 nm [62], while TmAH concentrations greater than 15% by weight, yield etched surface roughness below 20 nm [8]. For the MEMS-relays described in this thesis, all the crystalline orientation dependant etching was performed with KOH solutions due to the significant faster etch rates of Si over TmAH. A concentration of 33% per weight at 80° C is used. This etch-bath concentration and temperature performed well for our application, although further optimization of the etch bath is possible.

3.2.2 {111} Contact error budget

The contact geometry consists of atomically parallel {111} silicon surfaces which have been micromachined through wafer-front and wafer-back side anisotropic etching of (100) silicon using a crystalline orientation dependant etchant – potassium hydroxide (KOH) – solution. To fabricate this geometry, a self terminating V-groove is etched on the wafer *top side*. After etch completion, the exposed {111} planes are passivated with SiO_2 or with Si_3N_4. Next, a self terminating V-groove is etched on the wafer bottom-side. Finally, the passivation layers are selectively etched away, and the silicon is oxidized and metallized.

The offset between the wafer-top and the wafer-bottom KOH masks produces the contact geometry, as shown in Figure 3-1. A thermal oxide is then grown on the patterned silicon substrate to provide electrical isolation, and a conductive film is deposited on the oxidized patterned substrate through e-beam evaporation.

A sensitivity analysis was performed to determine the fabrication tolerances and their effect on contact travel. This study also served to optimize the etch mask dimensions as well as the etch parameters used. In the {111} contacts, travel and overlap are coupled. The resulting dimensions are affected by the etch conditions, the thickness of the substrate, and by the wafer-front to wafer-back KOH mask offset. Misalignment of the etch-mask to the substrate crystalline plane introduces a sine error causing an increase in travel.

Case 1: perfect etch conditions. Consider the perfect case, shown in Figure 3-4(a). All dimensions are fabricated to specifications: the substrate thickness (T), the wafer-front (W_t) and wafer-back (W_b) etch masks, the wafer-front to wafer-back mask offset (d). The masks are exactly aligned to the substrates crystallographic orientation. Assuming infinite selectivity, no etch-rate along the (111) direction, the top etch will self terminate at a depth H_t and the bottom etch at a depth H_b. The resultant {111} contact dimensions are

$$\begin{aligned} \text{Contact travel:} \quad & t = 2d \\ \text{Contact overlap:} \quad & y = d/tan(54.7°) \end{aligned} \tag{3.1}$$

Case 2: Mask misalignment error e; *decreased* mask offset d. Consider now the case of perfectly sized masks (W_t, W_b), and substrate thickness (T), an error (e) which *decreases* the mask offset (d), as shown in Figure 3-4(b). In this condition both contact overlap (y) and contact travel are reduced from their nominal values

$$\begin{aligned} \text{Contact travel:} \quad & t_2 = 2d - e \\ \text{Contact overlap:} \quad & y_2 = (d - e)/tan(54.7°) \end{aligned} \tag{3.2}$$

Case 3: Mask misalignment error e *increasing* mask offset d. Consider perfectly sized masks (W_t, W_b), and substrate thickness (T), an error (e), which

increases the mask misalignment (d), as shown in Figure 3-4(c). In this condition, the wafer-top and wafer-bottom etches form non-intersecting *V-grooves*, and the contacts are not released.

Case 4: Mask undercut u causing blowout. Consider perfectly sized (W_t, W_b), and offset (d) masks, perfect substrate thickness (T), and a mask undercut (u), which causes blowout of the etched geometry, as shown in Figure 3-4(d). In this condition the contact overlap remains constant but the contact travel is increased to

$$\begin{aligned} \text{Contact travel:} \quad & t_4 = 2(d+u) \\ \text{Contact overlap:} \quad & y_4 = y \end{aligned} \tag{3.3}$$

Case 5: Mask thickness out of specification - *thinner* substrate. Consider perfectly sized (W_t, W_b), and offset (d) masks, thinner than specified substrate thickness (T) by an amount (δt), no mask undercut (u), as shown in Figure 3-4(e). In this condition, the contact overlap remains constant, but the contact travel is increased to

$$\begin{aligned} \text{Contact travel:} \quad & t_5 = 2d + \delta t/tan(54.7°) \\ \text{Contact overlap:} \quad & y_5 = y \end{aligned} \tag{3.4}$$

Case 6: Mask thickness out of specification - *thicker* substrate. Consider perfectly sized (W_t, W_b), and offset (d) masks, thicker than specified substrate thickness (T) by an amount (t), no mask undercut (u), as shown in Figure 3-4(f). In this condition, the wafer-top and wafer- bottom etches form non-intersecting *V-grooves*, similar to case 3, and the contacts are not released.

More than one of the above mentioned conditions may occur at the same time so the effect on the final contact dimensions will be additive. The selectivity of the KOH is cited amply [68]; however the cited values differ significantly. Selectivity in

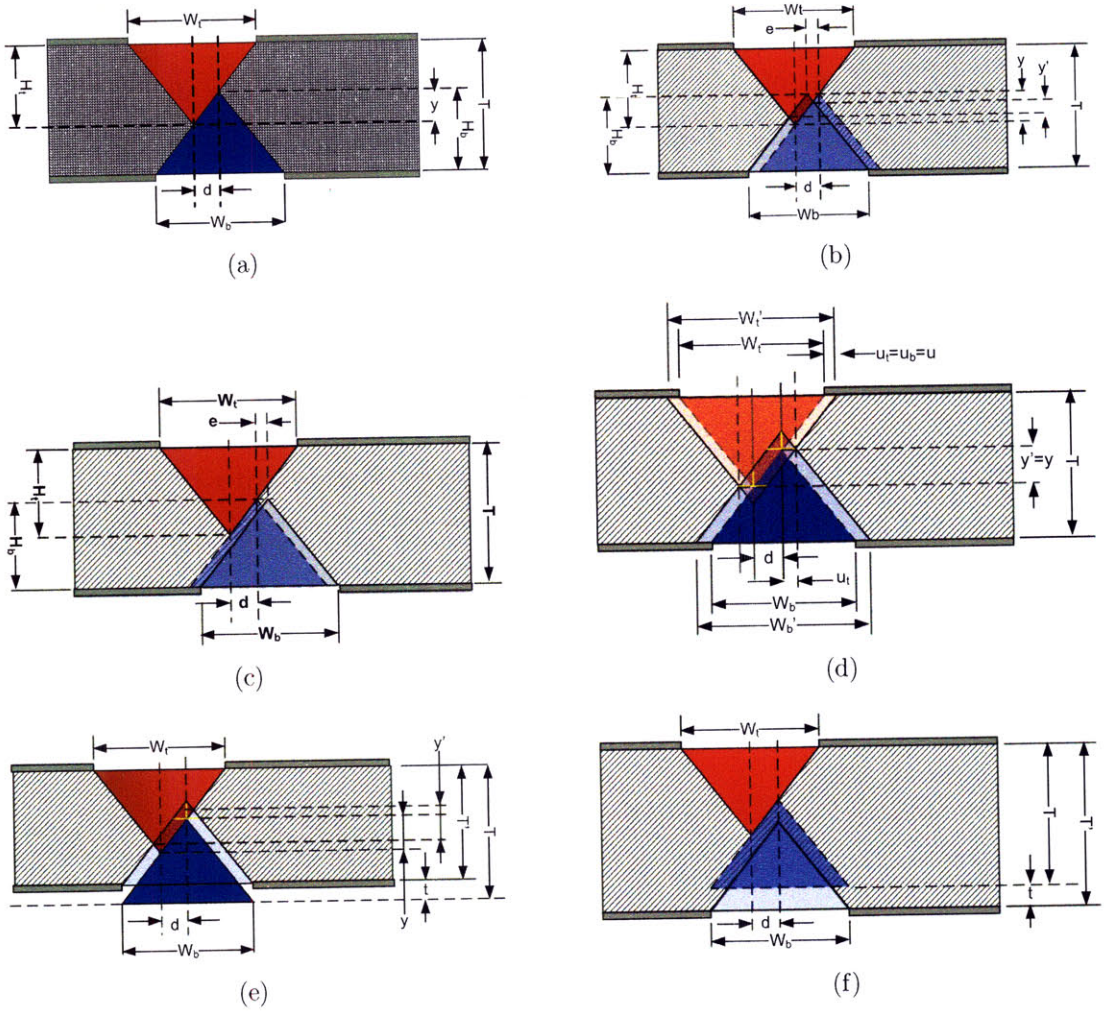


Figure 3-4: Error stack for {111} contacts: (a) perfect geometry; (b) *decreased* mask offset by alignment error e; (c) *Increased* mask offset by alignment error e; (d) mask *undercut* by amount u; (e) substrate thickness *under* specification by amount t; (f) substrate thickness *over* specification by amount t.

Table 3.1: Test pattern contact dimensions

	Mask dimensions $[\mu m]$	Fabricated dimensions $[\mu m]$
KOH window ($W_t = W_b$):	236	252
Mask offset (d):	16	15.8
Wafer Thickness (T):	300	298
Travel:	32	64

CODE is strongly dependant on the etchant concentration, temperature, substrate type (p-type vs. n-type), the doping concentration, light conditions, and even on the growth conditions of the Si substrate (float zone vs. CZ growth) as trace amounts of oxygen precipitation in the ingot affect the selectivity [48].

A test pattern for the contacts was etched in 33% KOH solution by weight at 80° C (bath temperature was set at 83° C), and resulted in the geometry dimensions listed in Table 3.1. Notice that the wafer-front to wafer-back offset is very close to the target value, which validates the capability to align the masks within fractions of a micrometer. Notice as well, that the etched geometry is sized larger than the dimensions on the mask. This indicates undercut of the mask during etching which may be caused by a finite etch rate along the (111) direction, misalignment of the etch mask to the substrates crystallographic plane, or by etching into the silicon as the mask is patterned.

3.3 Analysis of the {111} contacts: mechanical, electrical and thermal domains

Analysis of the {111} contacts requires models in the mechanical, electrical and thermal domains. Elastic and plastic contact mechanics models are used to determine the size of the mechanical, or load-bearing contact area as a function of contact force and the mechanical properties. Once the mechanical contact area has been established, electro-thermal models are used to determine the electrical and thermal constriction

at the contact interface. The electrical and thermal constriction resistances are used in a thermal model to determine the current capacity of the {111} contacts. While the {111} silicon surfaces are planar (with nm-scale roughness) and parallel, after evaporation and electroplating, the metal surface is granular with μm-scale features (see for example Figure 5-36). Therefore, the use of an asperity contact model is justified.

3.4 Contact resistance and contact physics

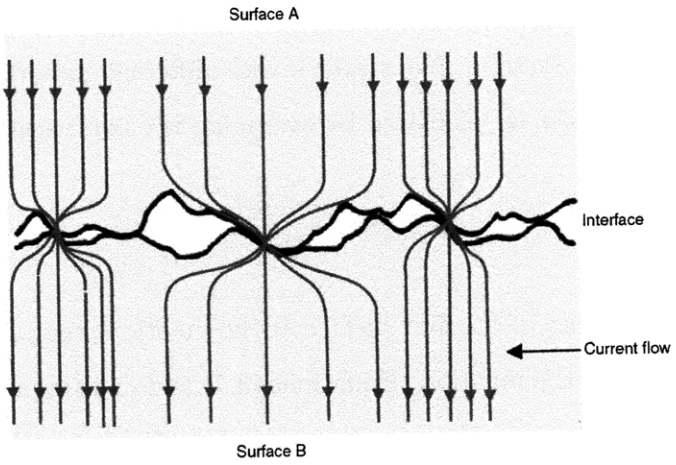
3.4.1 Contact resistance

All engineered surfaces have shape and roughness on a characteristic scale. In the case of electrical contacts, the roughness is on the μm or nm scale. As two metal surfaces are brought into mechanical contact with each other, asperities on both surfaces touch and deform. A very small fraction of the macroscopic contact area, or *apparent area*, establishes physical contact. This area is known as the *load bearing area*. Under large enough contact loads, ohmic contact is established at the interface. Only a small fraction of the load bearing area establishes ohmic contact between the surfaces. The areas of ohmic contact are referred to as *a-spots*. Current lines and heat flowing across the two contacts are geometrically constricted at the *a-spots*, as shown in Figure 3-5(a). The constriction results in electrical and thermal resistance [19, 59].

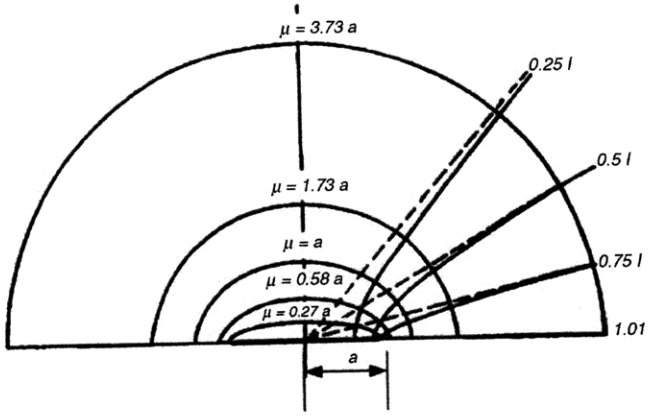
Consider a single-asperity contact model of two semi-infinite bodies contacting over a circular a-spot of radius a. The constriction resistance can be determined from the Laplace equation [19]. Concentric ellipsoids originating at the a-spot describe surfaces of equal potential (Figure 3-5(b)). In cylindrical coordinates, these ellipsoids are defined by

$$\frac{r^2}{a^2+\mu^2}+\frac{z^2}{\mu^2} \tag{3.5}$$

where μ is a geometric parameter, and (r,z) are the cylindrical coordinates. The



(a)



(b)

Figure 3-5: Electrical constriction in a bulk interface. Figure from [19]. (a) Schematic of asperities making contact at a mechanical interface. Ohmic-contact is established at discrete a-spots leading to constriction of the current flow. (b) Single asperity model equipotential surfaces and current flow lines near an a-spot.

resistance between the a-spot and an equipotential surface of vertical axis length μ is

$$R(\mu, a) = \frac{\rho_e}{2\pi} \int_0^{\mu} \frac{d\mu}{(a^2 + \mu^2)} = \frac{\rho_e}{2\pi a} \arctan(\mu/a) \tag{3.6}$$

where ρ_e is the resistivity of the contact material. At a large distance away from the a-spot ($\mu \gg 1$), the constriction resistance over the total geometry is given by

$$R_c = \frac{\rho_e}{2a} \tag{3.7}$$

Equation (3.7), also known as the spreading resistance or Maxwell resistance, describes a monometallic system. For systems with different materials on each body, the constriction resistance is calculated by averaging the two resistivity values

$$R_c = \frac{\rho_{e1} + \rho_{e2}}{4a} \tag{3.8}$$

where ρ_{e1} is the resistivity of the first surface at the junction, and ρ_{e2} is the resistivity of the second surface at the junction. Equations (3.7) and (3.8) apply to clean surfaces only. Dielectric contaminant films, such as oxides, sulfides and hydrocarbons, are practically always present on the surface of metallic contacts, even on new and "clean" metallic surfaces. These films provide a film resistance R_f described by

$$R_f = \frac{\rho_{ef} d_f H}{F} = \frac{\sigma_f H}{F} \tag{3.9}$$

where ρ_{ef}, and d_f are the resistivity and thickness of the contaminant film, H is the hardness of the metallic contact, and F is the contact force. The product of the film resistivity and thickness is known as the film resistivity σ_f. The electrical contact resistance is the sum of the constriction and contaminant film effects:

$$R_C = R_c + R_f \tag{3.10}$$

The use of equations (3.5), (3.6), (3.7), and (3.8) require knowledge of the contact area (a-spot) size. The a-spot size can be calculated from solid mechanics models. At sufficiently small spot sizes, on the order of the electronic mean free path of the material ($\sim nm$), the classical electrical flow model does not apply [60]. As the conduction mechanism becomes predominately ballistic electronic motion, Sharvin resistance sets in. An alternative expression for Equation (3.7) at the transition between classical and ballistic conduction is given by Wexler [66].

3.4.2 Contact mechanics

Depending on the value of the contact pressure, the asperities can undergo elastic, plastic, or elasto-plastic deformation. The study of MEMS contacts, from an experimental and modeling point of view, is an ongoing research field which spans across many diverse disciplines. Classical contact theory [19, 51, 59, 4], which applies for macro-scale contacts, provides a basis for this endeavor. In this thesis, elastic and plastic deformation models are presented. These models represent the two extremes of the physical phenomena and therefore likely bound the solution. Under low contact pressures ($P_c < 0.6\,H$), the asperities undergo elastic deformation, while at high contact pressures ($P_c \geq 0.6\,H$) the asperities are plastically deformed. For traditional, macro-switch contacts, the asperity deformation is mostly plastic [17]. For MEMS contacts, which operate at lower contact forces, both elastic and plastic deformation are possible. For example, elastic deformation has been reported for Au and Au-Ni MEMS contacts for forces on the order of mN [47, 46, 21].

3.4.2.1 Elastic model

The problem of two bodies in point contact was first solved by Heinrich Hertz in 1882 for the elastic case [26]. An approximate solution to this problem is given by the *gap bending hypothesis* [53]. The hypothesis states that "the effect of geometry on the system in the contact region is a function of the algebraic sum of the curvatures of the two bodies in contact" [61]. This approximation solves the problem of two-curved surfaces in contact by developing an "equivalent" model based on the superposition of an elastic sphere on a rigid flat contact problems, which have a well known closed form solution. Consider two spheres of radius r_1 and r_2 that are pressed together with a force F. The equivalent modulus of elasticity ($\widetilde{E}$) for this system is given by

$$\widetilde{E} = \left(\frac{1-\nu_1^2}{E_1} + \frac{1-\nu_2^2}{E_2} \right)^{-1} \tag{3.11}$$

where E_1, E_2, ν_1, ν_2 are the elastic modulii and Possion ratios of materials 1 and 2. The equivalent radius of the system ($\tilde{r}$) is

$$\tilde{r} = \left(\frac{1}{r_{11}} + \frac{1}{r_{12}} + \frac{1}{r_{21}} + \frac{1}{r_{22}} \right)^{-1} \tag{3.12}$$

the equivalent circular contact area radius (a_h) is

$$a_h = \left(\frac{3}{2} \frac{F \tilde{r}}{\tilde{E}} \right)^{1/3} \tag{3.13}$$

and the deflection of the two bodies relative to each other (total deflection) (δ_h) is

$$\delta_h = \frac{1}{2} \left(\frac{1}{\tilde{r}} \right)^{1/3} \left(\frac{3}{2} \frac{F}{\tilde{E}} \right)^{2/3} \tag{3.14}$$

For equal radii ($r_1 = r_2 = r$) and materials ($E_1 = E_2 = E$, $\nu_1 = \nu_2 = \nu$), equations (3.12), (3.13), and (3.14) reduce to

$$\tilde{r} = \frac{r}{4} \tag{3.15}$$

$$a_h = \left(\frac{3}{4} F r \frac{1 - \nu^2}{E} \right)^{1/3} \tag{3.16}$$

$$\delta_h = 1/2 \, r^{-1/3} \left(3 F \frac{1 - \nu^2}{E} \right)^{2/3} \tag{3.17}$$

Substituting (3.16) into (3.7) yields the expression for the constriction resistance R_{ce} caused by elastic deformation

$$R_{ce} = \rho_e \left(\frac{E}{6 F r (1 - \nu^2)} \right)^{1/3} \tag{3.18}$$

In the case of elastic deformation ($P_c < 0.6H$), the constriction resistance relates to the contact force by $R_{ce} \propto F^{-1/3}$, and is dependant on the asperity radius by $R_{ce} \propto r^{-1/3}$.

3.4.2.2 Plastic model

At high contact pressure the deformation is plastic [17]. The area of mechanical contact (A_c) is related to the hardness of the softer material at the interface by [3]

$$F = A_c H \tag{3.19}$$

where F is the force exerted between the surfaces, and H is the hardness of the softer material. Combining (3.7) and (3.19) yields the expression for constriction resistance caused by plastic deformation R_{cp}

$$R_{cp} = \sqrt{\frac{\rho_e^2 \eta \pi H}{4F}} \tag{3.20}$$

where η is an empirical coefficient of order unity. In the case of plastic deformation ($P_c \geq 0.6H$), the constriction resistance is solely a function of the applied load ($R_{cp} \propto F^{-1/2}$) and of the physical material properties. The constriction resistance does not depend on the physical size or shape of the contacting bodies.

3.4.2.3 Effect of contact force (F) on contact resistance (R_C)

As described by equations (3.9), (3.18) and (3.20), the relationship between contact resistance and contact force is

$$R_c \propto F^{-\beta} \tag{3.21}$$

where $\beta = 1/3$ in the elastic regime, $\beta = 1/2$ in the plastic regime, and $\beta = 1$ for the cases where film contamination dominates. Section 3.4.4 presents calculated contact resistance values for various metals using the elastic and plastic contact models.

3.4.3 Material properties

Processes used to deposit thin films in microelectronics include: evaporation, sputtering, electrodeposition, chemical vapor deposition, solgel processing, and LASER pulse deposition. The formation-technique and process parameters (i.e film thickness,

pressure, deposition rate, deposition temperature, thermal history, etc.) significantly affect the film structure and its mechanical properties [57, 37, 6]. For example, the hardness of electroplated and sputtered gold films are 1 GPa and 3 GPa respectively [43], while the hardness for bulk gold is between 200 and 700 MPa [51]. In general, thin films are harder than the same material tested in bulk [43]. This is a result of intrinsic stress and St. Venant's principle [36, 53]. This principle states that the effects of a load on a solid body become negligible at a typical distance of 3-5 characteristic lengths away from the application of the load [34]. This means that for thin films, the thickness of the film must be at least 3-5 times thicker than the maximum indentation depth. This principle sets a limit on the minimum plating thickness of a MEMS contact.

The strong interdependence between formation-technique, process-condition, and film properties causes the experimental property values to differ significantly between various published references, for example see Table 3.2. In addition, the characterization techniques in microelectronics and in MEMS are not universal. Nanoindentation, for example, is a good technique to measure yield stress, flow stress, and hardness of bulk materials. However, the use of this technique on thin films and on anisotropic materials is more ambiguous as nanoindenters tend to pick up the properties of the underlying substrate, particularly if the indentation depth exceeds 1/10 of the film thickness [58].

Table 3.2 lists average electrical and mechanical properties of metals used in electrical contacts for both MEMS-relays and in traditional, macro-scale contacts. Notice the large range of the reported values for the same material; unfortunately the formation and characterization-techniques used are not always reported with the data. Included in Table 3.2 are normalized resistivity $\widetilde{\rho_e}$, hardness $\widetilde{H}$ and contact resistance $\widetilde{R_c}$. The references used for normalization are the average properties of bulk gold films

$$\text{Normalized resistivity: } \widetilde{\rho_e} = \frac{\rho_e}{\rho_{e-Au}}$$

$$\text{Normalized hardness: } \widetilde{H} = \frac{H}{H_{Au}}$$
$$\text{Normalized contact resistance: } \widetilde{R_c} = \frac{R_c}{R_{c-Au}} \tag{3.22}$$

Bulk gold properties were selected as the reference because of its ubiquity in the MEMS contact literature. Bulk properties, not thin-film properties, are used as reference values because the properties of most other metals were also measured in bulk. Figure 3-6 shows the contact resistance as a function of force for the metals listed in Table 3.2; the values were calculated using Equation 3.19.

- **Gold** is the most extensively used material for MEMS contacts due to its good thermal and electrical properties, and its corrosion robustness, particularly as it does not form an oxide. However, it is soft, exhibits strong adhesion forces, and is prone to cold-welding. Gold was selected as the reference material because of its ubiquity in MEMS contact literature.

- **Copper** exhibits 45% lower resistance than gold. However, copper has low resistance to oxidation, and corrosion [51].

- **Silver** exhibits a 10% improvement in contact resistance over gold. However, it has low resistance to sulphurization and oxidation, low melting and boiling-points, low mechanical strength, is prone to sticking, and exhibits material transfer at higher loads [25, 19, 51].

- **Nickel** and **platinum** exhibit a contact resistance 4-5 times higher than gold. These materials have high resistance to oxidation and corrosion and are used extensively in macro-scale contacts for light-duty applications. Platinum is prone to the formation of frictional polymers under fretting conditions [51].

- **Rhodium** exhibits 6 times higher contact resistance than gold, but is hard and very resistant to corrosion and tarnishing [51].

- **Iridium**, **palladium**, and **tungsten** exhibit contact resistance 8 times higher than that of gold. Palladium has lower oxidation resistance than platinum, and

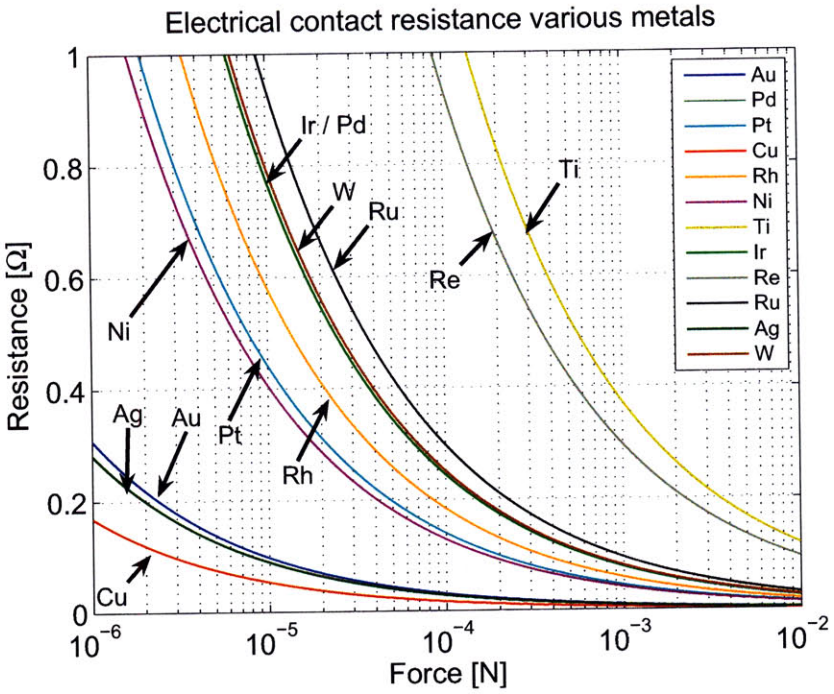


Figure 3-6: Contact resistance as a function of force for common contact metals; value calculated by (3.20)

oxidizes readily at 350° C. Palladium is also prone to formation of frictional polymers due to its catalytic property.

- **Ruthenium** exhibits almost 10-times the contact resistance of gold. It is characterized by its low material transfer [25].
- **Rhenium** and **titanium** exhibit contact resistances exceeding 30-times that of gold contacts.

3.4.4 Discussion of the contact-physics model

Figures 3-7, 3-8, 3-9, show the calculated constriction resistance R_c as a function of contact force for the elastic and plastic models. The constriction resistance is calculated from (3.18) and (3.20), with the material properties listed in Table 3.3, and an asperity radius of 0.1 μm for the elastic model. The asperity radius was determined from standard grain size values of evaporated and electrodeposited films.

Table 3.2: Contact metals, electrical and mechanical properties. Normalized film properties and contact resistance are included for material performance comparison. Note that property values in bulk and thin-film vary drastically. Formation-technique, and process conditions affect the mechanical properties of thin films.

Material	Resistivity ρ_e $[\mu\Omega - cm]$	Hardness H $[MPa]$	Manuf. process[a]	Ref.	$\widetilde{\rho_e} = \frac{\rho_e}{\rho_{e-Au}}$	$\widetilde{H} = \frac{H}{H_{Au}}$	$\widetilde{R_c} = \frac{R_c}{R_{c-Au}}$
Gold, Au	3.93	1770	sputt.	[12]	1	1	1
	3.6	1040	sputt.	[29]			
	-	1000	evap.	[43]			
	2.2	150-350	-	[43]			
	2.19	200-700	bulk	[51]			
Silver, Ag	1.78	1310	sputt.	[12]			
	1.59	300-700	bulk	[51]	0.72	160	0.91
Cobalt, Co	6.22	-	bulk	[51]	2.83	-	-
Copper, Cu	1.7	100-150	sputt.	[43]	0.77	0.5	0.55
	1.65	400-900	bulk	[51]			
Iridium, Ir	5.3	2700	bulk	[51]	2.41	10.8	7.92a
Nickel, Ni	7	400-450	sputt.	[43]	3.18	1.7	4.15
	6.84	80-180	bulk	[51]			
Palladium, Pd	13.75	2870	sputt.	[12]			
	10.8	400-900	bulk	[51]	4.91	2.60	7.92
Platinum, Pt	13.88	3550	sputt.	[12]			
	10.6	5360	sputt.	[29]			
	10.6	220	sputt.	[43]	4.82	0.88	4.52
	10.6	400-850	bulk	[51]			
Rhenium, Re	19.3	2500-3500	bulk	[51]	8.77	12.0	30.39
Rhodium, Rh	4.93	-	evap.	[27]	2.05	8.4	5.94
	9.3	9750	sputt.	[31]			
	4.51	1200-3000	bulk	[51]			
Ruthenium, Ru	13.8	15280	sputt.	[29]			
	6.71	2500	bulk	[51]	3.05	10	9.64
Titanium, Ti	40	-	sputt.	[43]	18.18	4.40	38.14
	41.6	1100	bulk	[51]			
Tungsten, W	5.55	1200-4000	bulk	[51]	2.52	10.4	8.14

[a]Sputtering (sputt.), evaporation (evap.)

Table 3.4 lists the contact forces needed for a constriction resistance of $100\,m\Omega$ for a variety of materials, according to the elastic and plastic contact models. Also included in the table is the contact radius (a_h) calculated from (3.7). As would be expected, the elastic contact model predicts a higher constriction resistance than the plastic contact model. According to the plastic deformation model, a contact force on the order of 2-5 mN is required to achieve a constriction resistance of $R_c \approx 100\,m\Omega$ using refractory metals. These values are the same order of magnitude of previously published experimental values: 0.4 mN to 10 mN for $0.1\,\Omega < Rc < 1\,\Omega$ [46, 21, 43], as shown in Figure 3-10. The difference between experimental and modeled contact resistance may be attributed to surface contamination and to variations in the mechanical properties.

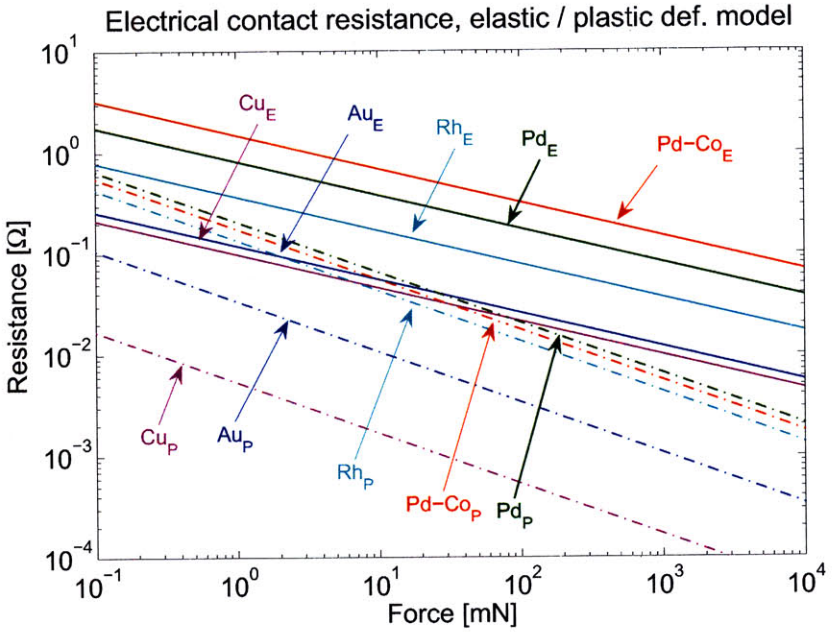


Figure 3-7: Contact resistance as a function of force; elastic (solid lines)& plastic deformation models (dashed lines)

3.5 Thermal analysis

The asperities on the surface of the contacts not only cause constriction in the electrical domain, but also in the thermal domain. Upon application of a current through

Table 3.3: Physical material properties used for Figures 3-7, 3-8, 3-9. The material properties are from [15, 43, 29, 1, 12].(* Assumed to be the same as Pd)

Mat'l	ρ_e $[\mu\Omega - cm]$	E $[GPa]$	ν	H [MPa]
Au	2.2	86	0.44	2000
Pd	13.75	117	0.39	2870
Pd-Co	25	117*	0.39*	625
Rh	4.9	257	0.26	9750
Cu	1.7	115	0.34	125

Table 3.4: Elastic and plastic contact-mechanics models. Material properties and calculated forces for $R_c = 100\,mA$. The asperity radius is $r = 10^{-7}m$. (* Assumed to be the same as Pd)

Mat'l	ρ_e $[\mu\Omega - cm]$	E $[GPa]$	ν	H [MPa]	F_e $[mN]$	F_p $[mN]$	a_h $[nm]$
Au	2.2 [15, 43]	86 [29]	0.44	1770 [12]	1.72	$6.75 \cdot 10^{-2}$	110
Pd	13.75 [15]	117 [12]	0.39	2870 [12]	543	4.27	687.5
Pd-Co	25 [15]	117*	0.39*	625 [1]	3267	3.07	1250
Rh	4.9 [15]	256.8 [29]	0.26	9750	49.1	1.84	245
Cu	1.7 [43]	115	0.34	125	0.97	$2.8 \cdot 10^{-3}$	85

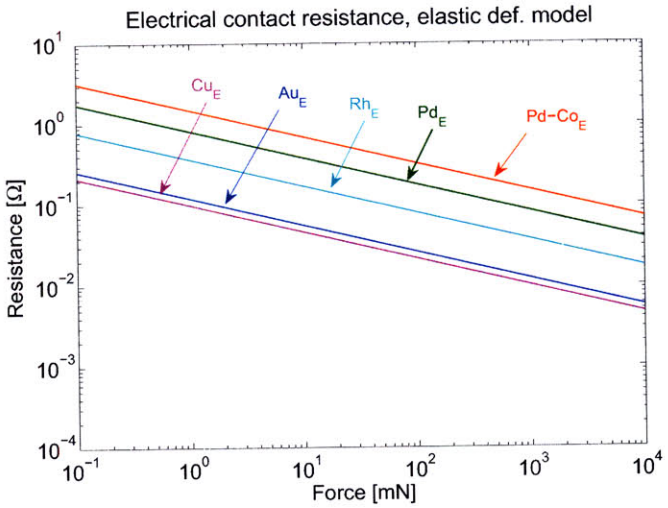


Figure 3-8: Contact resistance as a function of force; elastic deformation model. Same Figure as 3-7, reprinted for clarity

the interface, large current densities are developed at the constrictions, which lead to localized Joule heating. Although the time constant of an electrically heated a-spot is on the order of nanoseconds [43] (Section 3.5.1.2), the localized energy release may lead to softening and melting of the contacts, cold welding, and oxidation. It is therefore important to calculate the temperature at the contact interface to determine the maximum current carrying capacity. Three thermal models are presented. The first model, derived from first principles, describes the temperature rise at the a-spot during steady-state conditions. The second model, a closed form solution of a point heat-source on a semi infinite body, describes the constriction temperature in steady-state and transient conditions. This model, in conjunction with the plastic deformation model, describe the temperature rise at the constriction as a function of the actuation force. The third model describes the temperature of an electrically heated a-spot as a function of the potential drop at the constriction. This temperature is compared to the softening and melting temperatures of various materials.

3.5.1 First thermal model: first principles

This thermal model, developed from first principles, calculates the a-spot temperature under steady-state conditions. The model considers temperature effects on the

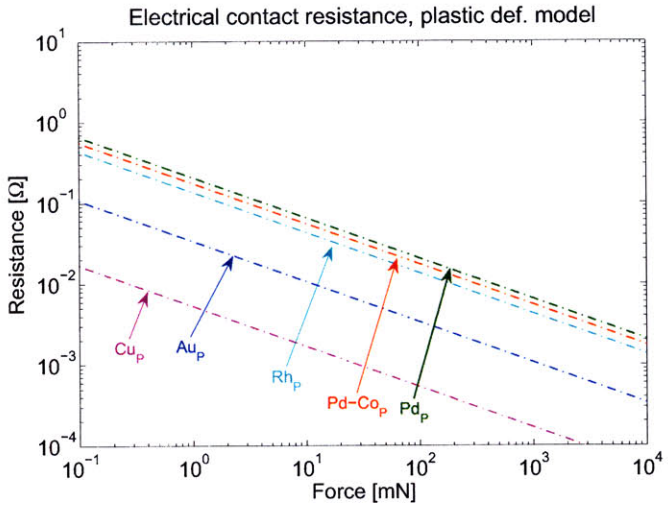


Figure 3-9: Contact resistance as a function of force; plastic deformation model. Same Figure as 3-7, reprinted for clarity

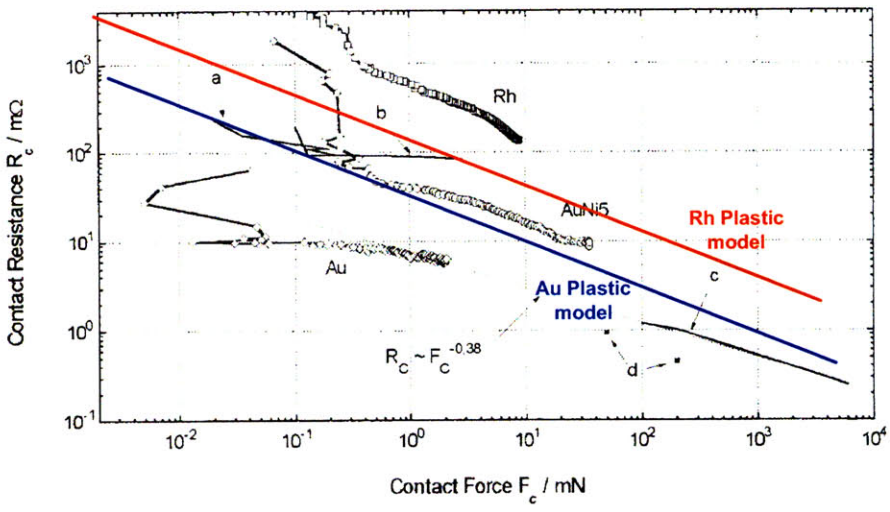


Figure 3-10: Elastic-plastic deformation

constriction resistance, which is modeled after a self heated resistor [49].

3.5.1.1 Thermal coefficient of resistance

In most materials, the electrical resistivity changes with temperature [1]. For metals operating over moderate temperature excursions, this dependance can be approximated

[1]The exception are some engineered alloys and materials, i.e. invar (FeNi36), designed to be close to temperature invariant over a specific temperature range.

as linear [63], the proportionality factor being the thermal coefficient of resistance α_R (TCR)

$$R(T) = R_0[1 + \alpha_R(T_s - T_0)] \tag{3.23}$$

where R_0 is the electrical resistance at reference temperature T_0, and $R(T)$ is the electrical resistance at temperature T_s. The expression for the steady-state temperature rise (ΔT_{ss}) of a self-heated resistor under constant current is given by [49]

$$\Delta T_{ss} = \frac{R_0 R_t I^2}{1 - \alpha_R R_0 R_t I^2} \tag{3.24}$$

where R_0 is the electrical resistance at the reference temperature (ambient), R_t is the thermal resistance, and I is the current. Equation (3.24) becomes indeterminate if $[\alpha_R R_0 R_t I^2] \rightarrow 1)$, and the device experiences thermal runaway ($\Delta T_{ss} \rightarrow \infty$). This condition is explained by a rapid decrease in thermal conductivity and a slow increase in electrical resistance as the temperature of the resistor increases. Thermal runaway is the principle under which a fuse operates to protect a circuit.

3.5.1.2 Steady-state conduction thermal model

The heat source in this model is Joule heating originating at the constriction. As in most MEMS devices, heat transfer is dominated by conduction. Convection and radiation are thus ignored in this analysis. The constriction is modeled as a Joule heat-source with temperature dependant electrical and thermal properties. For algebraic simplicity, consider the constriction volume to be embedded in the contact and be a half-sphere geometry, as shown in Figure 3-11. The heat capacity of the constriction is given by

$$C_t = \rho_m \frac{2}{3} \pi b^3 C_m \tag{3.25}$$

where ρ_m is the density, b is the radius of the heat source, or embedded a-spot, and C_m is the specific heat of the contact material. Because the load bearing area is significantly larger than the a-spot size in an electrical contact (Section 3.4.1), it is conceivable that the thermal contact area, defined by the radius b in this model, may

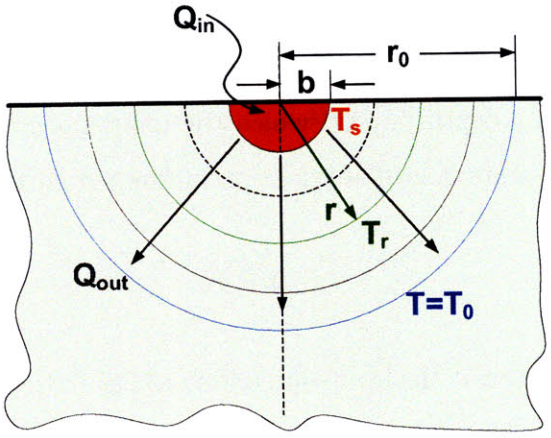


Figure 3-11: First thermal model: steady-state conduction with heat generation. Model based on [49]

also be larger than the a-spot size. In this model, heat will flow spherically from the heat source into the contact as shown in Figure 3-11. For simplicity, the temperature inside the heat source of radius b is considered uniform at T_s.

The one-dimensional, steady-state, conductive, heat flow equation (Fourier's law) of a spherical wall with heat generation is given by [22]

$$\begin{aligned} q'' &= -k \bigtriangledown T \\ \frac{1}{r^2}\frac{d}{dr}\left(r^2\frac{dT}{dr}\right) + \frac{\tilde{q}}{k} &= 0 \end{aligned} \tag{3.26}$$

where q'' is the heat flux, k is the thermal conductivity, and $\tilde{q}$ is the energy generated per unit volume. Equation (3.26) can be integrated and solved for the energy generated ($\dot{q}$)

$$\dot{q} = 2\pi r^2 k \frac{\partial T}{\partial r} \tag{3.27}$$

and integrated again to solve for the temperature distribution $T(r)$

$$\begin{aligned} T(r) &= \int_b^{r_0} \frac{\dot{q}}{2\pi k r^2}\, dr \\ &= -\left|\frac{\dot{q}}{2k\pi}\frac{1}{r}\right|_b^{r_0} \end{aligned}$$

$$= \frac{\dot{q}}{2\,\pi\,k}\left(\frac{1}{b}-\frac{1}{r_0}\right) \tag{3.28}$$

where r_0 is the contact depth beyond which the temperature is assumed to remain constant. The steady-state heat flow equation in lumped parameter form is

$$\dot{q} = \Delta T / R_t \tag{3.29}$$

Equating the temperature at the heat source from (3.28) to the temperature rise from the lumped parameter heat flow equation (3.29) yields the solution to the thermal resistance R_t between the heat source ($r = b$) and the thermal sink ($r = r_0$)

$$R_t = \frac{1}{2\,\pi\,k}\left(\frac{1}{b}-\frac{1}{r_0}\right) \tag{3.30}$$

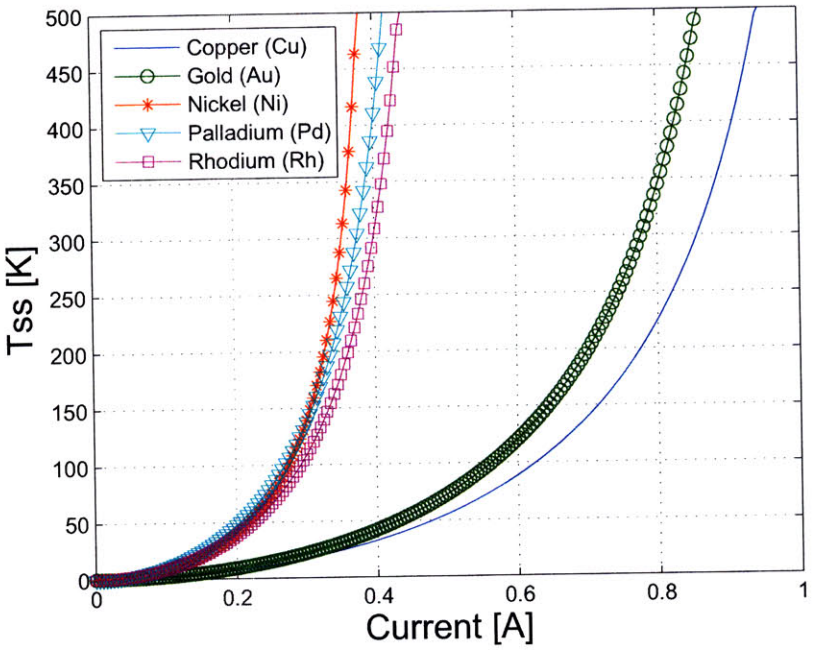
The thermal response time τ_t is approximated as the product of the thermal resistance R_t and the heat capacity C_t

$$\tau_t = R_t\,C_t \tag{3.31}$$

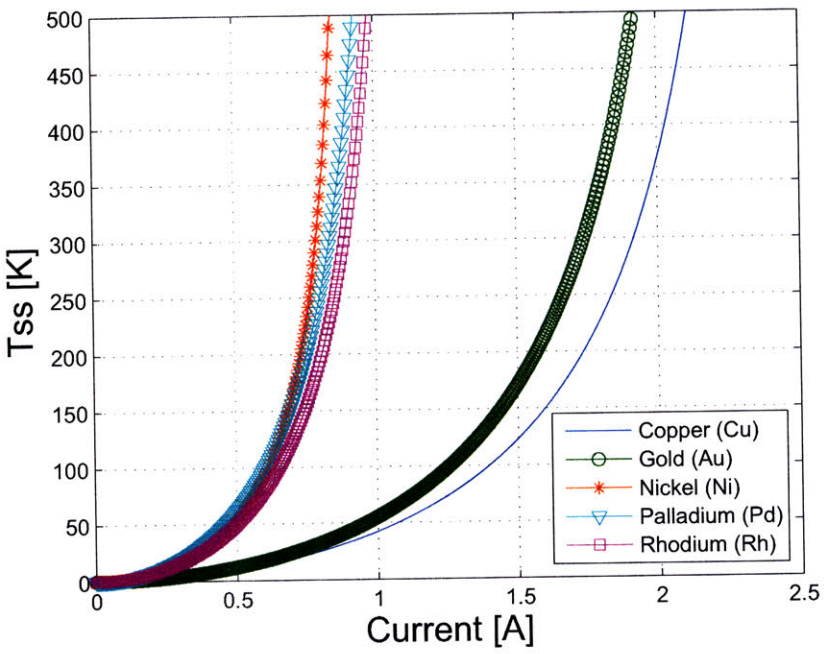
Numerical example. Equations (3.30),(3.25) require the thermal contact radius b to be known. As described in Sections 3.4.1, and 3.5.1.2, it may be conceivable for the thermal contact radius to be larger than the ohmic contact radius a, perhaps even as large as the load bearing area. For a conservative calculation, let the $b = a$. For a constriction resistance of $R_c = 500\,m\Omega$, it follows from (3.7) that $a \approx 1 - 6\,\mu m$. The steady state temperature rise calculated by (3.30) and (3.24) is shown in Figure 3-12 for $b = 1\,\mu m$, and $b = 5\,\mu m$. The thermal time constants for $b = 1\mu m$ and $b = 5\mu m$ are 2-13 ns and 64-327 ns, respectively.

3.5.2 Second thermal model: point heat source acting on a spherical wall

Consider the model of an instantaneous point heat source being released into an infinitesimal area on a semi-infinite body. The wall of the body is adiabatic, and the



(a) $b = 1\mu m; R_c = 0.5\,\Omega$



(b) $b = 5\mu m; R_c = 0.5\,\Omega$

Figure 3-12: Steady state temperature increase, first thermal model. (a) Thermal contact radius $b = 1\mu m$, contact resistance $R_c = 0.5\,\Omega$. (b) Thermal contact radius $b = 5\mu m$, contact resistance $R_c = 0.5\,\Omega$.

Table 3.5: Thermal material properties. Data compiled from [22, 51, 43, 27].

Mat'l	Density	Specific heat	Thermal conductivity	Thermal coeff. res.	Softening temperature	Melting point	Softening voltage	Melting voltage	Min. arc. voltage	Min arc. current
	ρ_m $[\frac{kg}{m^3}] \cdot 10^3$	C_m $[\frac{J}{kg\,K}]$	k $[\frac{W}{mK}]$	TCR $[\frac{1}{K}] \cdot 10^{-3}$	T_{soft} [° C]	T_{melt} [° C]	V_{soft} $[mV]$	V_{melt} $[mV]$	V_{arc} $[V]$	I_{arc} $[mA]$
Au	19.32	129	317	4	100	1063	80	420	12.5	350
Cu	8.933	385	401	4.3	190	1358	120	430	13	400
Ni	8.9	444	90.7	6.8	520	1453	160	540	13.5	500
Pd	12.02	244	71.8	3.8	-	1552	-	570	14	800
Rh	12.41	247	88	4.4	-	1966	-	700	13	350

body has an initial temperature $T(r,t) = T_0$.

The heat diffusivity α_t is defined by

$$\alpha_t = k/(c_m\,\rho_m) \tag{3.32}$$

where k is the thermal conductivity, c_m is the specific heat capacity, and ρ_m is the density.

The temperature distribution as a function of the heat Q released is [4, 7]

$$T(r,t) = \frac{Q}{4\,\rho_m\,c_m\,(\pi\,\alpha_t\,t)^{3/2}} \exp\left(-\frac{r^2}{4\,\alpha_t\,t}\right) \tag{3.33}$$

where r is the radial distance to the heat source.

For a constant, continuous heat release rate $\dot{q}$, the heat released in a small interval Δt is $dQ = \dot{q}\Delta t$. The released energy dQ will increase the temperature of the body (ΔT) by

$$\Delta T = \frac{\dot{q}\,\Delta\,t}{4\,\rho_m\,c_m\,(\pi\,\alpha_t\,t)^{3/2}} \exp\left(-\frac{r^2}{4\,\alpha_t\,t}\right) \tag{3.34}$$

Equation (3.34) can be integrated to determine the temperature distribution across the body

$$T(r,t) = \frac{\dot{q}}{2\,\pi\,k\,r}\,\mathrm{erfc}\left[r\,(4\,\alpha_t\,t)^{-1/2}\right] \tag{3.35}$$

Steady-state is reached at times $t \geq \frac{r^2}{2\alpha_t}$. The steady-state temperature distribution $T_{ss}(r)$ is given by

$$T_{ss}(r) = \frac{\dot{q}}{2\,\pi\,k\,r} \tag{3.36}$$

Combining (3.36), and (3.7), the steady state temperature can be expressed by

$$T_{ss}(r) = \frac{I^2\,\rho_e}{4\,\pi\,a\,k\,r} \tag{3.37}$$

The steady-sate temperature rise is a function of the material properties $(\frac{\rho_e}{k})$, and of the contact spot size (a)

$$T_{ss}(r) \quad \propto \rho_e/k$$

$$\propto 1/a \tag{3.38}$$

Based on the elastic and plastic contact models, the contact spots size (a) is a function of

$$\begin{aligned} a_h E &\propto \left(F \frac{1-\nu^2}{E} \right)^{1/3} \\ T_{ss}(r) &\propto \left(\frac{F}{H} \right)^{1/2} \end{aligned} \tag{3.39}$$

According to (3.39), the current carrying capacity can be increased by adequate material selection and large actuation forces. Contact materials which minimize ρ_e/k, and soft, low stiffness materials are advantageous. However, other properties such as corrosion resistance, adhesion, softening, and melting temperatures, must be considered as well.

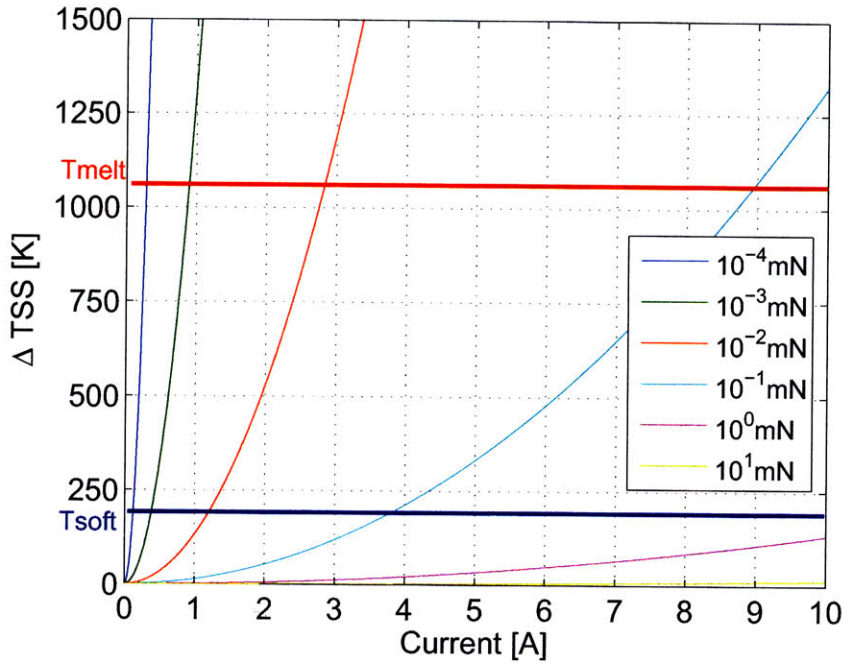
Let the ratio between the thermal contact radius (b) and a-spot radius (a) be

$$\gamma_t = b/a \tag{3.40}$$

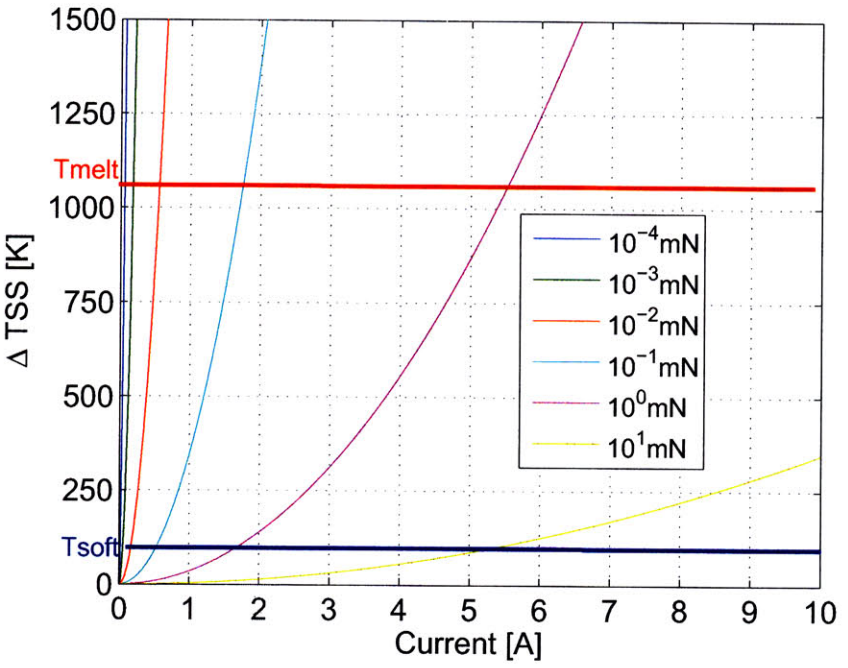
Assuming the deformation is plastic, the steady state temperature rise at the constriction can be expressed as a function of force by combining (3.7),(3.36), (3.20) and (3.40)

$$Tss = \frac{I^2 \rho_e \eta H}{4k\gamma F} \tag{3.41}$$

Discussion. The second thermal model does not consider the temperature dependance of electrical resistance and thermal conductivity. Hence, it will under predict the steady state constriction temperature. The calculated actuation forces for *MEMS-relay 1* and *MEMS-relay 2* are 5 mN and 40 mN at 70 V and 100 V respectively. If this force is achieved, the deformation is plastic, and (3.41) holds, then the calculated maximum current carrying capacity of relay-1 and relay-2 is in excess of 10 A. However, the presence of oxide, sulfides and organic dielectric films can reduce the a-spot

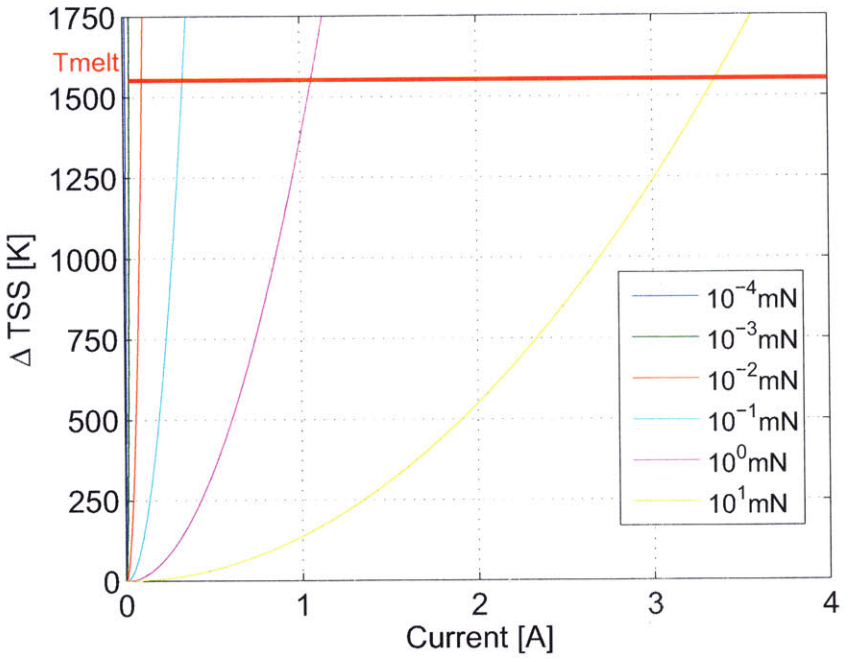


(a)

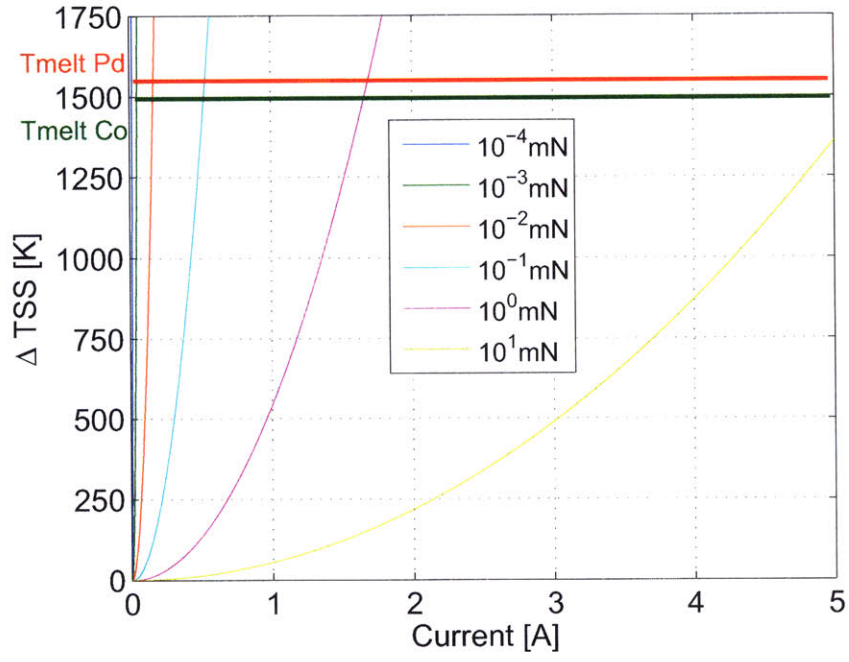


(b)

Figure 3-13: Steady-state temperature rise as a function of contact force; plastic contact model, per equation (3.41) and $\gamma = 1$. (a) Copper (Cu), (b) Gold (Au).



(a)



(b)

Figure 3-14: Steady-state temperature rise as a function of contact force; plastic contact model, per equation (3.41) and $\gamma = 1$. (a) Palladium (Pd), (b) palladium-cobalt (Pd-Co).

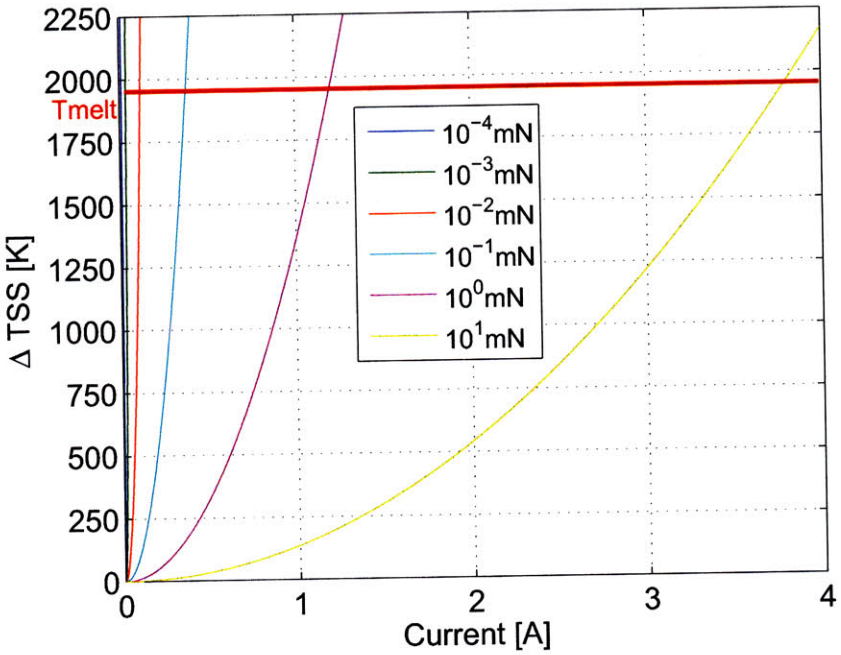


Figure 3-15: Steady-state temperature rise as a function of contact force – Rh; plastic contact model, per equation (3.41) and $\gamma = 1$.

size, so these results are optimistic.

3.5.3 Third thermal model: Kohlrausch equation and the melting voltage

Kohlrausch recognized in 1900 that in an electrically heated a-spot, not subject to convective heat losses, the electrical potential (Figure 3-5(b)) and the isothermal surfaces coincide [19, 59]. This recognition led to the development of the voltage-temperature relation, which relates voltage drop at the constriction to the maximum temperature at the interface. For a monometallic system the voltage-temperature relation is

$$V = 2\left[2\int_{T_1}^{T_{max}} k\,\rho_e\,dT\right]^{1/2} \tag{3.42}$$

where T_{max} is the maximum temperature at the constriction, T_1 is the bulk temperature of the connector, k is the thermal conductivity, and ρ_e is the electrical conductivity. For moderate temperature excursions, assuming constant thermal conductivity k

and electrical resistivity ρ_e, the temperature at the a-spot T_{max} is

$$T_{max} - T_1 = \frac{V^2}{8\,k\,\rho_e} \tag{3.43}$$

where T_1 is the reference temperature. The term $T_{max} - T_1$ is commonly referred to as the *super temperature*.

Over a wide temperature range the temperature dependent conductivity ($k(T)$) and resistivity ($\rho_e l(T)$) of metals can be expressed by

$$k(T) = k_0(1 - \beta T) \tag{3.44}$$

$$\rho_e(T) = \rho_{e\,0}(1 - \alpha T) \tag{3.45}$$

where k_0 and $\rho_{e\,0}$ are the conductivity and electrical resistivity at 0°C, β and α are the temperature coefficients of conductivity and resistivity respectively. Equation (3.43) can be modified to reflect the temperature dependance of thermal conductivity k and electrical resistivity ρ_e [59]

$$V^2 = 8k_0\rho_{e\,0}(T_{max} - T_1) + \frac{1}{2}(\alpha - \beta)(T_{max}^2 - T_1^2) - \frac{1}{3}\alpha\beta(T_{max}^3 - T_1^3) \tag{3.46}$$

A more general form of (3.46) is formulated through the Wiedemann-Franz law. The Wiedemann-Franz law states that the ratio of the thermal conductivity k to the electrical conductivity $1/\rho_e$ of a metal is proportional to the temperature:

$$k\rho_e = LT_{abs} \tag{3.47}$$

where L is the Lorentz number ($L = 2.45 \cdot 10^{-}8\,(V/K)^2$) and T_{abs} is the absolute temperature. Combining (3.47) and (3.43), the voltage-temperature relationship for all metals is

$$V^2 = 4L(T_{max}^2 - T_1^2) \tag{3.48}$$

Table 3.5 lists the softening and the melting temperatures and voltages for different metals. The current at which softening and melting will occur can be determined

Table 3.6: Maximum current carrying capacity before softening and melting. Contact force $F = 10^{-4}\,N$.

Mat'l	R_c $[m\Omega]$	I_{soft} $[A]$	I_{melt} $[A]$
Au	82	0.975	5.12
Pd	652.8	-	0.873
Rh	428.8	-	1.635
Cu	16.8	7.124	25.52

Table 3.7: Maximum current carrying capacity before softening and melting. Contact resistance $R_c = 0.5\,\Omega$.

Mat'l	F $[mN]$	I_{soft} $[A]$	I_{melt} $[A]$
Au	$2.7 \cdot 10^{-3}$	0.160	0.8413
Pd	170.5	-	1.14
Rh	73.5	-	1.40
Cu	$1.13 \cdot 10^{-4}$	0.24	0.86

through Ohm's law from the softening and melting voltages. For example, consider the maximum current carrying capacity of a contact with contact resistance of $R_c = 0.5\,\Omega$, prior to softening and melting. Depending on the contact material, the current ranges from 1 A to 7 A for the softening temperature limit, and from 0.8 A to 25 A for the melting temperature limit, as shown in Table 3.6. However, different contact loads must be applied to achieve the same contact resistance with different materials.

A more illustrative exercise is to compare the current carrying capacity of different materials under the same contact load. Assuming the plastic contact model applies, the maximum current capacity prior to contact softening is $I_{soft} \leq 300\,mA$, and the maximum current capacity prior to contact melting is $I_{soft} \leq 1.4\,A$, as shown in Table 3.7.

3.6 Stand-Off voltage

The maximum voltage that can be applied between two isolated conductors prior to breakdown is known as the stand-off voltage. There are different theories explaining the breakdown mechanism in gaps; each theory applies to particular conditions. For large gaps ($> 6\mu m$) not under vacuum, the electrical breakdown is caused by the Townseed electron avalanche breakdown process. F. Paschen determined empirically in 1889 that the potential required to initiate breakdown is a function of the pressure-gap product, as shown in the Paschen curve of Figure 3-16(a). Breakdown occurs when an electron injected into the gap collides with a molecule to release an additional electron. The newly released electrons collide with other molecules liberating additional electrons ultimately leading to glow discharge and to an arc [71]. Because the mean free path is inversely proportional to pressure, as the pressure-gap product is reduced, the breakdown voltage is reduced until the Paschen minimum is reached. At smaller pressure-gap products than the curve minimum, a higher voltage is needed to maintain the ionization due to fewer collisions.

Figure 3-16(a) shows the Paschen curve for different gases. The minimum breakdown voltage (U_{bd}) is plotted versus the pressure-gap product ($P \cdot d$). For air at atmospheric pressures ($1013\,hPa$) the breakdown voltage reaches a minimum of approximately $U_{bd} \approx 350\,V$ at $10\,\mu m$. Different literature [52] reports the minima for air at atmospheric pressure at $325\,V$ and $7.5\,\mu m$. According to the avalanche breakdown theory and ignoring field enhancement effects, a maximum of approximately 350 V can be applied at a gap of $10\mu m$ before breakdown occurs. The curve suggests that at gap-lengths smaller than the curve minima ($10\mu m$), the breakdown voltage increases rapidly. This is because at smaller gap-lengths the mean free path is too short for the free electrons to gain enough energy to initiate the ionization process. However, Slade and Taylor have shown [52] that Paschen's law only holds for air gap-length pressure products greater than the minima. For gaps smaller than $4\,\mu m$ operating in air at atmospheric pressures, experimental breakdown voltage data shows a linear dependence on contact gap, similar to the breakdown of contacts in vacuum [52], as

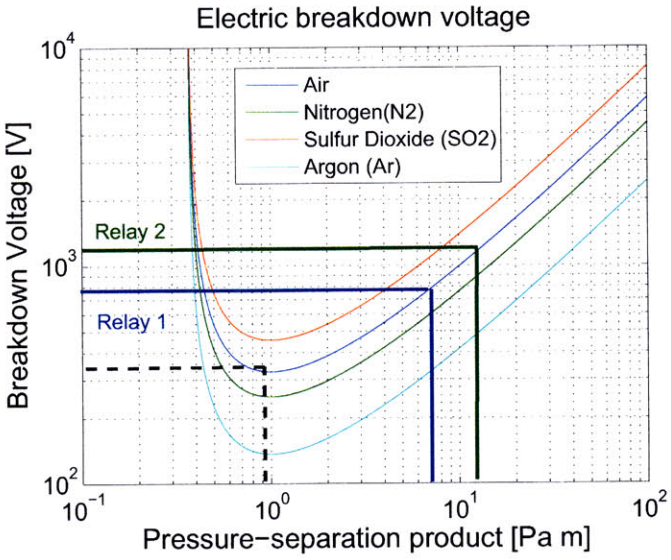
shown in Figure 3-16(b).

According to Paschen's law, a minimum gap of $d \approx 100\,\mu m$ is needed to prevent arcing at $1000\,V$ while operating in air at ambient pressure. Most MEMS relays have travel on the order of several (2-3) micrometers up to $10\,\mu m$. These devices will experience breakdown at voltages below 350 V, which is consistent with the published data (Figure 2-3).

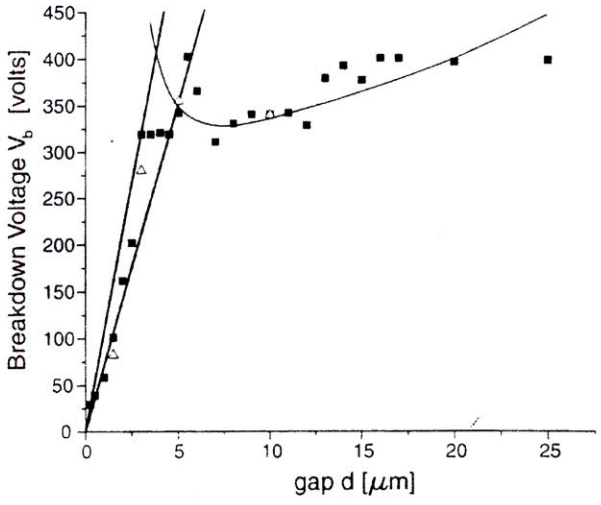
One of the relay's functional requirements is a minimum stand-off voltage of 600 V (Section 3.1). To this end, the relays in this thesis are designed with a travel of $35\,\mu m$ and $70\,\mu m$ for *MEMS-relay 1* and *MEMS-relay 2* respectively. In a "cross-bar" relay, the effective gap is twice the travel. At one atmosphere, the gap-pressure products for the two relays are $7.1\,Pa \cdot m$ and $14.18\,Pa \cdot m$. According to the Paschen curve, the expected stand-off voltages are $800\,V$ and $1050\,V$. However, Paschen's law does not account for field enhancement. Lower experimental breakdown values at the relays are expected due to field enhancement at the apex of the $\{111\}$ contacts.

MEMS relay 1 has a breakdown path across the $200\,nm$ thick SiO_2 between the static contacts and a common, highly-doped silicon substrate. With a typical breakdown strength of 5 MV/cm [5], the theoretical break-down across $2 \cdot 200\,nm$ of SiO_2 is $200\,V$, well below the $800\,V$ breakdown strength across the gap. A breakdown voltage of 200 V was confirmed experimentally for *MEMS relay 1* (Section 5.1.2).

On *MEMS relay 2* the breakdown path across the oxide was eliminated. The minimum-voltage breakdown path for this relay is at the gap, between the static contacts and the moving contact. Experimental *MEMS relays 2* were tested up to $450\,V$ continuously without breakdown. The voltage applied during these tests was limited by the test equipment. Higher voltages, exceeding $1\,kV$ were measured during hot switching without signs of breakdown (Section 5.4.3.3). Because the arcing event is a probabilistic event, continuous application of a high voltage is more likely to cause break-down than a high voltage impulse, such as the transient caused during the switching of an inductive load.



(a)



(b)

Figure 3-16: Electrical breakdown in a gap. (a) Breakdown voltage for various gases as a function of the pressure-gap product according to Paschen [71]. Note that about $100\,\mu m$ gap is needed to withstand $1000\,V$ while operating in air at 1 atm. (b) Experimental data indicating linear dependance of pressure-gap products below a $4\,\mu m$ gap. Figure from [52]

3.7 Design and analysis conclusions

This chapter presented the functional requirements for a MEMS relay for power switching applications. Key requirements are galvanic isolation, low contact resistance, large contact travel and adequate metallization. All of these functional requirements may be fulfilled with the {111}-contacts. Although the {111} contacts are highly planar and parallel, deposited polycrystalline metallic films exacerbate the surface roughness. Thus, the contacts can be modeled using elastic and plastic asperity deformation models. The maximum current carrying capacity is limited by softening and melting at the constriction. Current capacity may be increased through adequate contact material selection, large contact loads and through multiple contacts in a compliant design which uses multiple contacts as a means to increase the contact area, similar to a wiffle-tree.

Chapter 4

First MEMS-relay

This chapter presents the design, fabrication and test of the first MEMS relay. This relay served as a test bed for the fabrication and electrical characterization of the {111} contacts. It demonstrated that the KOH-etch process could be integrated with DRIE through the use of nested masks and shadow wafers to fabricate the relay. The {111} relay concept is presented first. Next, design details are discussed. The fabrication process and key fabrication steps are described. Finally, the test results are presented and discussed. Key shortcomings of the first relay are identified to be addressed on *MEMS relay 2*.

4.1 Concept and design

Based on the functional requirements of low contact-resistance, large contact separation and reliability described in Section 3.1, the MEMS relay shown in Figures 4-1 and 4-2 was designed. Structurally, the MEMS relay is comprised of an etched silicon device layer bonded to a Pyrex handle wafer. Etched into the device layer are the contacts, the compliant mechanism, and the actuators. The Pyrex handle wafer serves as support for the bonded structures while providing electrical isolation. The relay is comprised of a compliant mechanism (1), a pair of engaging (2a, 2b) and a pair of disengaging (3a, 3b) rolling-contact "zipper" actuators [32, 33], and a pair of {111}-contacts (4, 5), on which three metal films (6a, 6b, 7) have been deposited

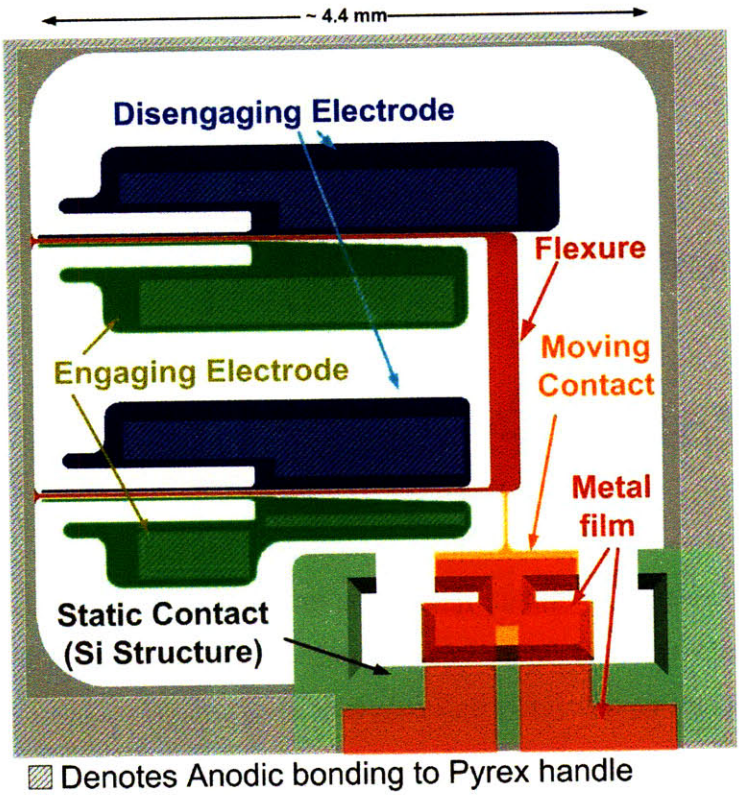


Figure 4-1: *MEMS relay 1*, schematic device layer

through e-beam evaporation.

4.1.1 Actuator design

Various actuation methods have been reported for MEMS devices. Electrothermal actuation can provide larger force output and large travel, however, it has a limited response time in the order of 1-2 ms which is the time needed to conduct heat away from the electrothermal actuator. Furthermore, use of electrothermal actuation reduces the amount of energy that can be handled by the relay contacts. Piezoelectric actuation provides very large forces, and very fast response times, but is limited in travel. Travel can be increased through mechanism design, for example monomorph or bimorph benders. Creep is the major limitation of piezoelectric actuation operating in DC. The principle of electrostatic actuation is used for the first MEMS-relay because it offers minimal power consumption and fast response time. Rolling contact

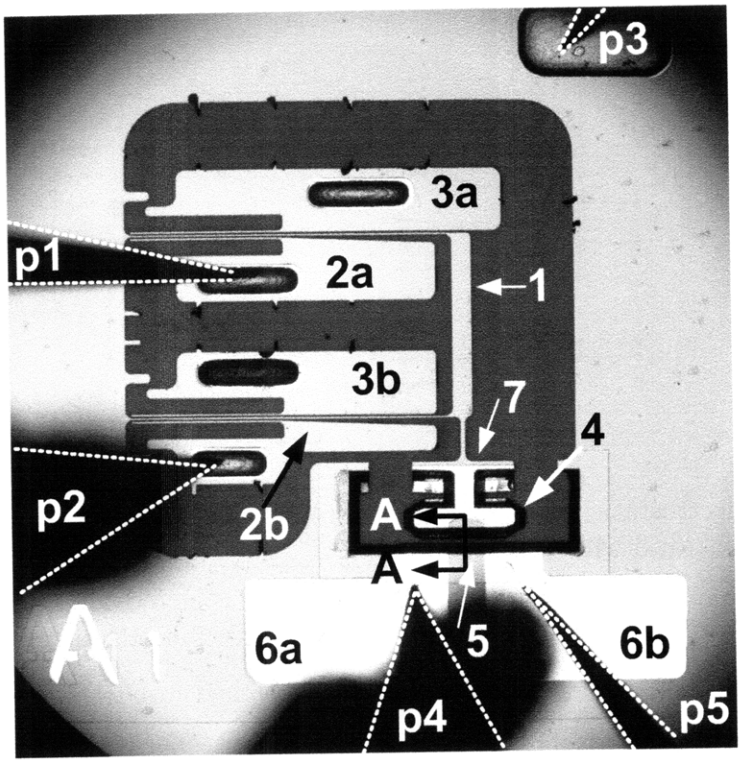


Figure 4-2: *MEMS relay 1*, fabricated device under test

electrostatic actuators [32] are used to provide low pull-in voltage and large contact travel. The actuators are designed for a nominal travel of 30 μm and a 5 mN force. Modeling of the actuation is based on [33] with modified boundary conditions for the selected geometry. Figure 4-3 shows the force-travel curves predicted by the model. The model predicts a theoretical force of 5 mN force at full travel (30 μm) with 70 V actuation voltage.

4.2 Fabrication

The fabrication process for *MEMS relay 1* is shown in Figure 4-4. A detailed process plan is included in Appendix A. Nested masks are used to pattern both wafer-through etches. The process starts the fabrication by patterning a low stress silicon nitride film on both sides of the wafer (a). This film serves later in the process as a KOH mask. A silicon oxide film is deposited on the KOH mask (b). The compliant mechanism

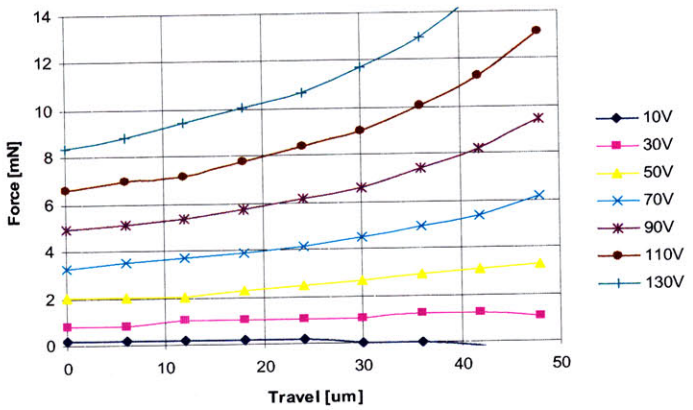


Figure 4-3: Electrostatic actuator Zipper forces - *MEMS relay 1.* A 5 mN force is provided at full travel with 70 V.

and actuators are then etched through deep reactive ion etching (c) and a second Si_3N_4 film is deposited to passivate the surfaces etched in DRIE. The second Si_3N_4 film is patterned using a "shadow" (through etched) wafer as a mask. The oxide is selectively etched away revealing the buried Si_3N_4 mask (d). Next, the substrate is etched in aqueous KOH solution to form the wafer top {111} contacts (e). The wafer is passivated with Si_3N_4 and steps (d), and (e) are repeated on the wafer back side to pattern the bottom {111} contacts (f,g). Both Si_3N_4 and SiO_2 films are stripped and a thermal oxide, which insulates both the electrostatic actuators and the relay contacts form the rest of the device, is grown (h). Gold is evaporated over both sides of the insulated contacts (i) and the device wafer is anodically bonded to a Pyrex handle wafer (j). The insulated contacts are then wire bonded and electroplated. The fabricated relay is shown in Figures 4-2, and 4-5.

4.3 Test

Experimental pull-in and drop-out voltages of 70 V and 40 V respectively agree with the analytical actuator model. The contact resistance was measured using the 4-point probe method, and determined to be as low as 120 mΩ. However the repeatability is poor and low contact resistance is not consistently achieved. It is believed that

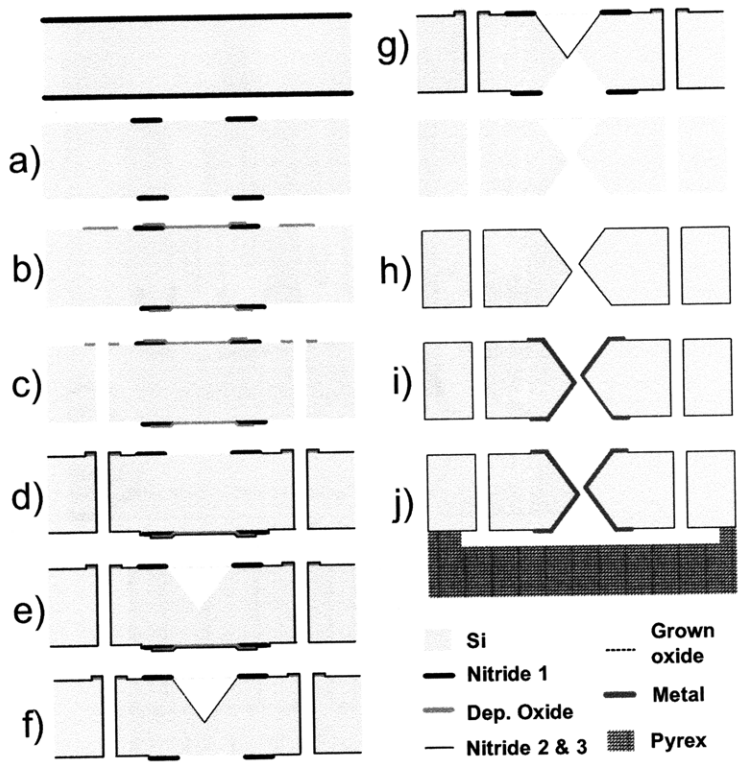


Figure 4-4: Process plan, *MEMS relay 1*

process inherent inaccuracies reduce the actuation force and that this causes poor repeatability in the experimental data. While the predicted contact force is 5mN, the actual force could not be experimentally determined. Experimental relays exhibited a break down voltage of 200V. This is in agreement with the breakdown strength of oxide 400 nm thick (200 nm under each static contact). Figure 4-6 shows the contacts prior to testing. At current values higher than 3 A the electrical probes which were used to connect the MEMS device to the test setup failed, as shown in Figure 4-7. Limited performance tests were performed due to the lack of consistency in performance.

4.4 Summary, first MEMS-relay

The first relays demonstrated the fabrication process, particularly the integration of KOH etching and DRIE through the use of nested masks and shadow wafers. These

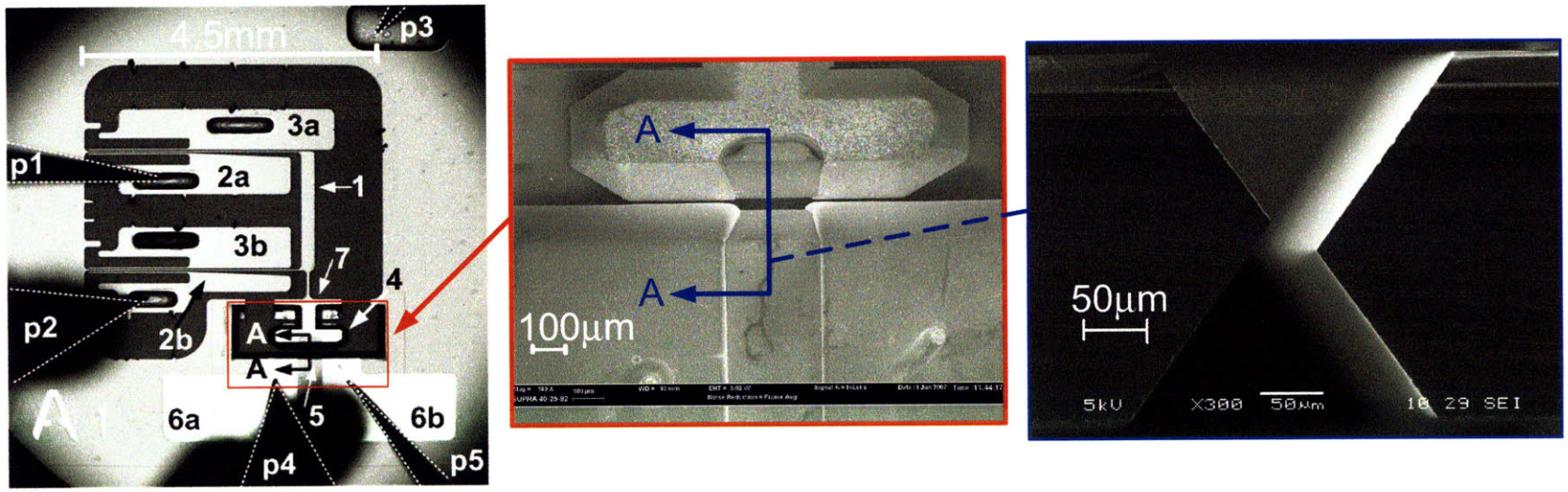


Figure 4-5: Fabricated *MEMS relay 1*

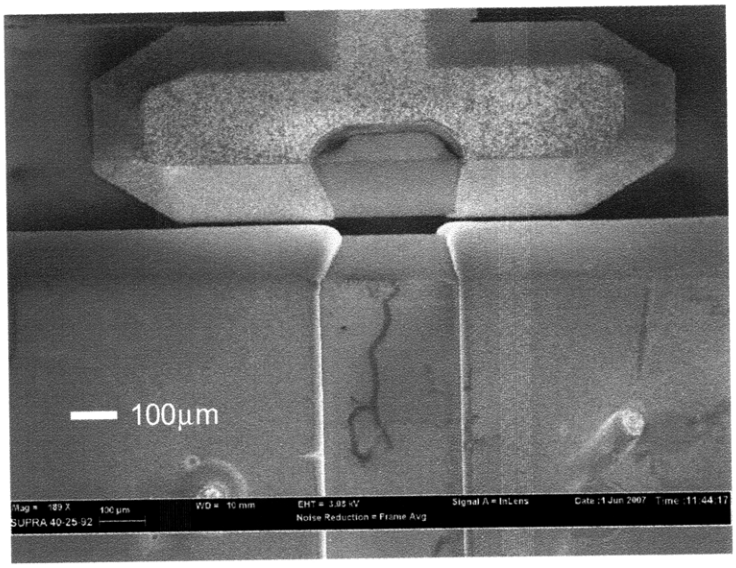


Figure 4-6: Contacts prior to testing *MEMS relay 1*

relays also served as test subjects for characterization of the {111} contacts. Shortcomings in fabrication and in performance were addressed in the design of the second MEMS relay, presented in Chapter 5. These shortcomings are: (1) elimination of the shadow-wafers used to etch the {111} contacts; (2) increased isolation of the static contacts; (3) increased actuation force and travel; (4) decoupling of the compliant mechanism and the actuators; (5) die level packaging; (6) actuator isolation and device release after bonding.

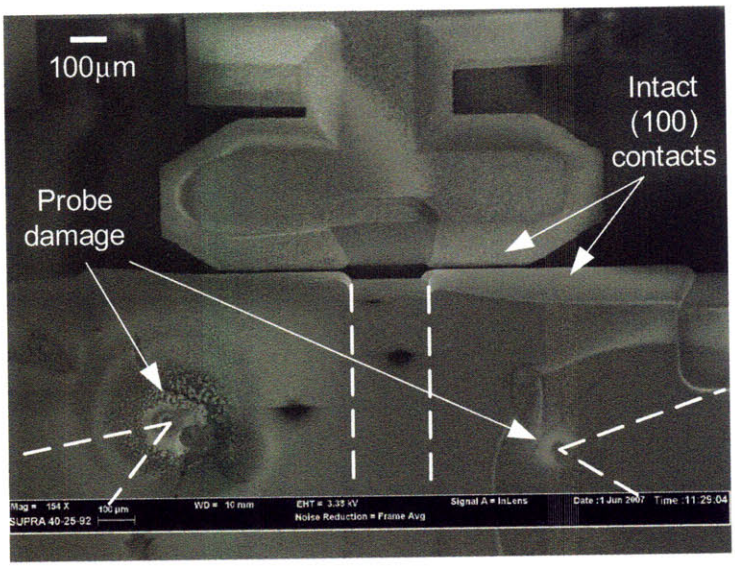


Figure 4-7: Contacts after testing *MEMS relay 1*. Notice damage at the probe

.

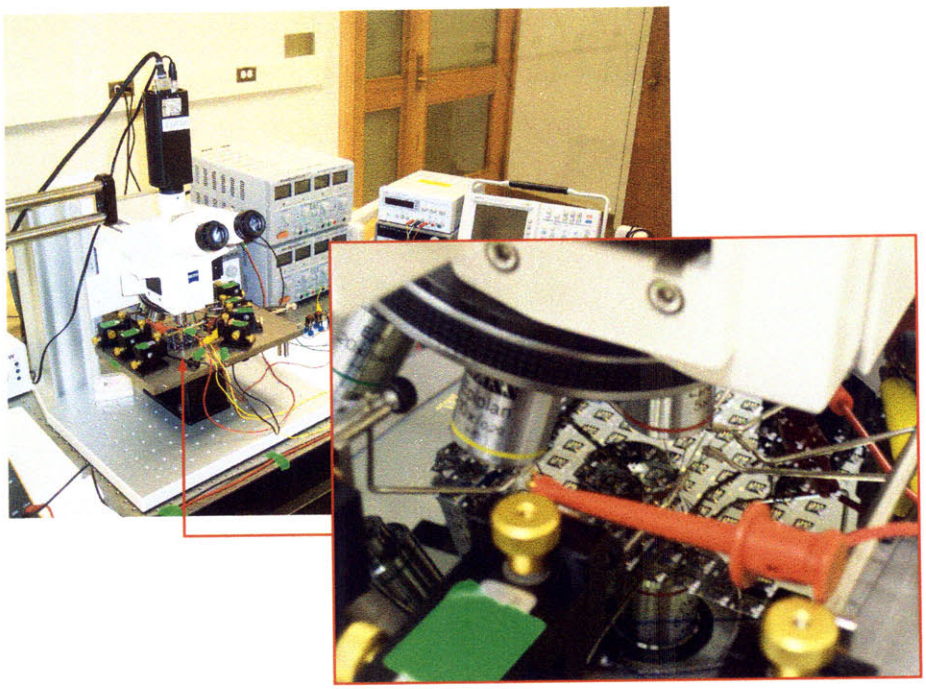


Figure 4-8: Test setup *MEMS relay 1*

Chapter 5

Second MEMS-relay

This chapter presents the design, fabrication and test of the second MEMS relay. Strategies to correct the shortcomings of *MEMS relay 1* are presented together with experimental tests used to validate the implementation of these strategies. Design details are discussed. The new fabrication process is described. The test setup and the test results are discussed.

5.1 Revisions to the first relay: strategies and fabrication tests

The first relays served as a test bed for the fabrication and electrical characterization of the {111} contacts. These relays demonstrated that the KOH-etch process could be integrated with DRIE through the use of nested masks and shadow wafers to fabricate the device. However, the first relays exhibited several fabrication and performance deficiencies which were addressed on the second relay design. The main changes incorporated into the second MEMS relay affect performance, fabrication, and testing. These changes are: (1) elimination of the shadow-wafers used to etch the {111} contacts; (2) increased isolation of the static contacts; (3) increased actuation force and travel; (4) decoupling of the compliant mechanism and the actuators; (5) die level packaging; (6) actuator isolation and device release after bonding. The changes are

motivated by observations made on the first prototype during fabrication and test, as well as by test runs used to validate the new strategies.

5.1.1 Elimination of shadow-wafers in the fabrication of the {111} contacts

The main change to the fabrication process of the second relay eliminates the use of shadow wafers[1] to pattern the nested masks. This is achieved through an SiO_2 KOH mask, local oxidation of silicon (LOCOS), and a selective wet etch (hot phosphoric acid).

The change in KOH mask material from Si_3N_4 to SiO_2 is not trivial. Silicon rich LPCVD nitride[2] has a negligible etch rate in KOH compared to that of SiO_2 which can be as high as 8 nm/min [67, 68]; silicon rich Si_3N_4 films may have lower residual stress (-50 to +800 MPa [49]), than thermally grown oxides, (-300 MPa [49]); Si_3N_4 is also less susceptible to pinholes than SiO_2.

A test run validated the use of SiO_2 as a KOH masking and passivation layer material in the fabrication of the {111} contacts. The purpose of the test run was to: (1) characterize the etch rate and selectivity of thick deposited and grown oxides; (2) determine the amount of mask undercut expected during the KOH etch; (3) determine the effect of film stress on the integrity of the mask during etching, particularly to assess the oxides robustness as a passivation material when etched from both sides during the KOH etch, and as the mask film is undercut and becomes suspended; (4) and to determine the optimum tools and parameters to pattern the films while avoiding etching into the silicon substrate as this causes mask undercut.

For this test, a 5 μm thick oxide was deposited through chemical vapor deposition (CVD) on the front and back of 300 μm thick (100) Si wafers. Because of the thickness required, the oxide film was deposited and not thermally grown. The deposited oxide

[1] Shadow wafers are hard masks made by etching through a Si wafer typically using DRIE. They are aligned to the device wafer using the wafer aligner/bonder tool (Electronics Visions 620) and fixed to the device wafer with a few dabs of photo-resist placed on the edge of the aligned wafers with a swab.

[2] Si_3N_4 deposited in TRL's VTR

was annealed in a N_2 atmosphere at 950 ° C for 1 hr. The oxide on the wafer top side was patterned with a CVD oxide etch tool (Applied Materials Centura 5200), and etched in 33% KOH solution by weight at 80 ° C. The etched wafer was passivated through the growth of 1.7 μm of SiO_2 (grown through three subsequent thermal 1 μm oxidations). Next, the SiO_2 on the wafer-back side was patterned with the CVD oxide etch tool, and the wafer was etched in 33% KOH solution by weight at 80 ° C. Finally, the oxide mask film was stripped in 49% hydrofluoric acid (HF).

The etch profile of this test, shown in Figures 5-1 and 5-2, indicates that the contacts etched using oxide masks are comparable to those etched using nitride masks. It also shows that the new fabrication process is as controllable as the one using silicon nitride as a KOH mask and as a passivation layer. This test also indicates that the minimum deposited oxide thickness needed for a 2-3 hr KOH etch is 1.6 μm, and that the SiO_2 film does not crack due to residual stress during undercut, yielding sharp {111} contacts.

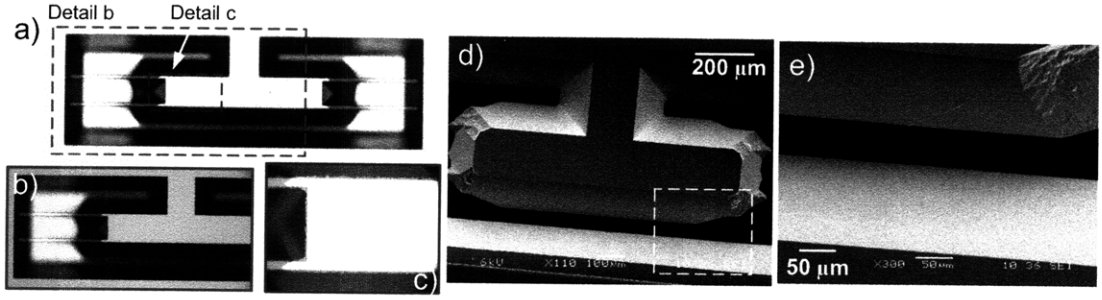


Figure 5-1: {111} contacts etched with an oxide mask - process test. Optical micrographs after the first etch (a-c). The deposited oxide remains intact during etching to yield sharp {111} planes. Note the jagged edge of the mask caused by the limited resolution of the transparency masks. SEM top view after wafer-front and wafer-back KOH etch and oxide strip (d,e).

5.1.2 Increase in breakdown voltage at the contacts

The open-circuit break-down voltage is limited in *MEMS relay 1* to 200 V. This is because both static contacts are evaporated on a common oxidized silicon substrate (0.01-0.02 Ω-cm, n-type), as shown in Figure 5-3. Since the silicon substrate is highly

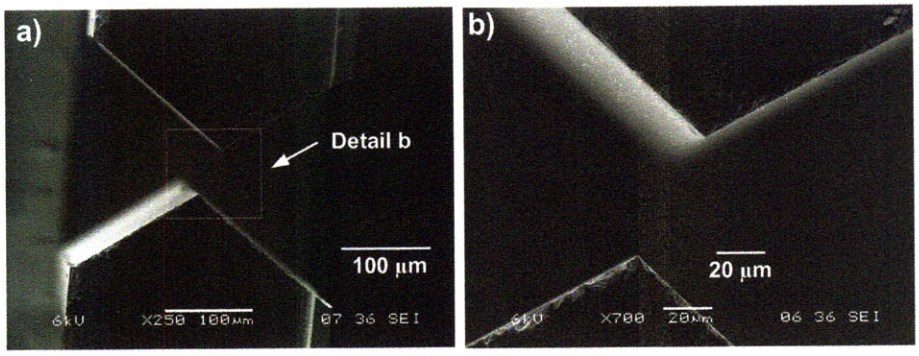


Figure 5-2: Contact cross section using oxide as a KOH mask and as a passivation layer.

doped, thus electrically conductive, the isolation between the two static contacts is solely provided by the 2000 Å thick thermal SiO_2 under each static contact. Thermal SiO_2 has a breakdown voltage of 5 MV/cm [5], both SiO_2 films being in series yields the total breakdown voltage of 200 V.

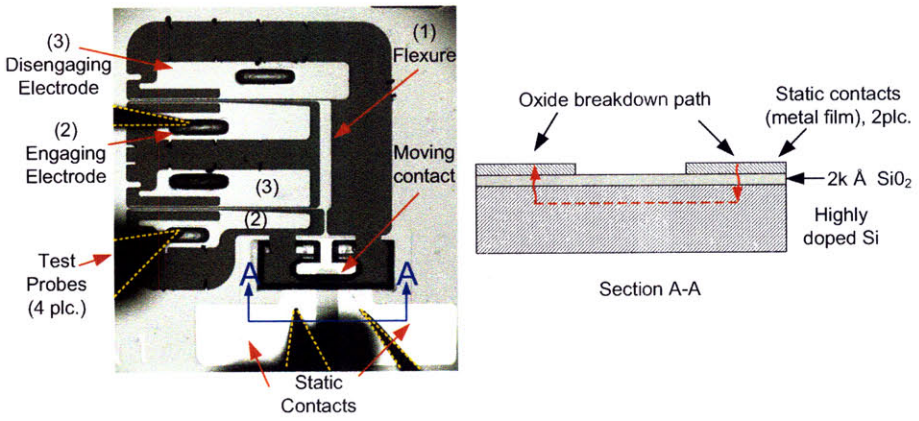


Figure 5-3: Contact isolation in *MEMS relay 1* and the breakdown path. The isolation is provided by a 2 kÅ thick SiO_2 deposited over a highly-doped common Si substrate. Breakdown occurs through the SiO_2 between the metal contacts and the common Si substrate.

5.1.2.0.1 Increase in breakdown voltage through thicker oxide films.

One possible way to increase the relay's breakdown voltage would be to increase the thickness of the SiO_2 film under the static contacts.

A single 2 μm thick thermal SiO_2 film, or for our particular application, a 1 μm thick film under each static contact would provide a dielectric strength of 1 kV. The

same silicon dioxide film serves as a dielectric film for the actuators, maintaining isolation between the zippers and the electrodes.

For the zipper actuators, the relationship between actuation force F_z and the dielectric film thickness h_o is

$$F_z \propto h_o^{-3/2} \tag{5.1}$$

A five-fold increase in the thickness of the dielectric film from 2000 Å to 1 μm would reduce the actuation force by approximately 70 %. A further disadvantage of this isolation strategy is that 1 μm is close to the practical limit of thermal oxide growth. For higher breakdown voltages it would be difficult to grow thermal oxide films thicker than 1 μm because during thermal oxidation the oxide is formed at the Si-SiO_2 interface. Oxygen must diffuse through the oxide to reach the interface, which takes longer as the thickness of the oxide increases.

Thermally grown SiO_2 films over 1 μm are not practical. Thicker silicon dioxide films are possible through CVD, however, the dielectric quality of deposited films is not as good as that of thermally grown films which affects breakdown.

For the previous reasons, the use of a thick dielectric film to increase breakdown voltage is not a plausible strategy. This strategy was not pursued.

5.1.2.0.2 Increase in breakdown voltage through dielectric isolation plugs.

A different strategy to increase the breakdown voltage is to introduce an isolating *plug* in-between the static contacts, analogous to a via, but fabricated with a dielectric material.

There are several advantages of having the isolation in the wafer plane as opposed to on the surface of the wafer: thicker dielectric films are possible; isolation plugs allow subsequent processing on the surface of the wafer; in some cases plugs may eliminate the need for a handle wafer to provide isolation and structural rigidity. Such isolation plugs have been used in igniters [35]. The fabrication process involves etching of a blind trench into the silicon, filling of the trench with a conformal oxide such as one deposited through the pyrolytic oxidation of tetraethylorthosilane (TEOS), backside etching to isolate the structures, and planarization of the wafer surface through

chemical-mechanical-polishing (CMP).

Planarization is needed to eliminate excessive topography, which may cause fabrication problems during downstream processing, such as during subsequent photolithography steps. Since the *MEMS relay* requires patterning of films on both sides of the wafer, the trench etched from the wafer-back should also be filled with conformal oxide and be planarized.

Figure 5-4 shows the proposed isolation trench geometry and the proposed process flow. Notice that after etching of the {111} contacts the oxide protrudes from the static contacts. The protruding SiO_2 can be removed prior to bonding through a selective etch such as a buffered-oxide-etch (BOE).

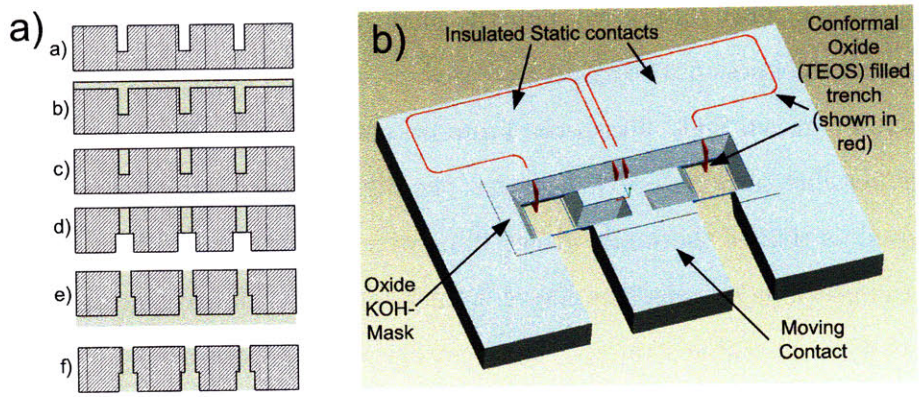


Figure 5-4: SiO_2 filled trench contact isolation test. Proposed process flow (a); trench etch (a,d), TEOS deposition (b,e), planarization CMP (c,f). Solid model SiO_2 filled trench isolation strategy (b).

This strategy was attempted on a test structure using TEOS and low-pressure-chemical-vapor-deposition (LPCVD) SiO_2 films, as shown in Figure 5-5.

Different geometries such as straight and wavy trenches were included in the test structures. The purpose of the wavy trench geometry is to increase the stiffness of the substrate and plug interface by providing a locking mechanism similar to that of a jig-saw puzzle. The isolation trenches in the test structures were etched to the same aspect ratio as the igniter plugs. In spite of using the same equipment and process parameters as the igniter plugs, the oxide deposition was not conformal enough to fill the trenches. Very little SiO_2 was deposited on the bottom of the trench, while the

trench easily filled at the surface of the wafer resulting in keyholes. The strategy of isolating the contacts through the use of dielectric plugs was not pursued.

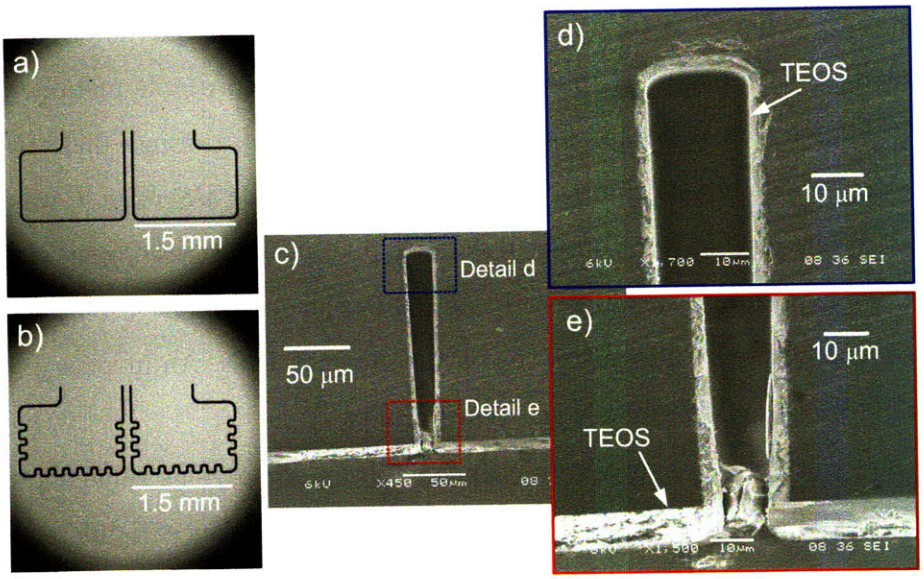


Figure 5-5: SiO_2 filled trench contact isolation test cross section. Top view micrographs of straight (a) and wavy (b) geometries. The wavy trench geometry is intended to lock the silicon structures and increase the stiffness. Cross section (c) and trench bottom (d) and top (e) details. Notice the SiO_2 deposition does not fully fill the trench satisfactorily, only the wafer-top etch was tried.

5.1.2.0.3 Increased breakdown voltage through an unfilled isolation trench.

A third strategy to increase breakdown voltage is to structurally isolate the two static contacts from each other through an unfilled trench. This is not a trivial geometry to fabricate as the isolation trench intersects the KOH mask forming convex corners, which, if let uncompensated for, bevel due to exposed fast-etching {411} crystalline planes. In our application, such a beveling would significantly reduce the length of the contact overlap.

Traditional, convex corner compensation mask geometries [38] cannot be implemented into these trenches due to size constraints. A new method was developed to fabricate perfect corners at intersecting V-grooves and trenches. This process, which is based on vertical convex corner compensation, localized oxidation of silicon (LOCOS) and on shaped trench geometry, is discussed in detail in Section 5.2.1.

5.1.3 Increase in actuation force

Electrical contact resistance is a function of the mechanical properties of the contacting films, such as hardness and conductivity, and of the contact pressure. A minimum contact force must be applied to achieve a reliable and repeatable metallic contact. This is the force that is needed for the asperities to break through dielectric layers such as oxides and organic films. The performance of *MEMS relay 1* was not repeatable. While cycling, the contact resistance fluctuated between open circuit and 130 mΩ. We hypothesize this was partly caused by the design, but also by the particularly low contact force, designed to be on the order of 5 mN. An increase in contact force would increase performance and repeatability.

The new relay was designed for a 40 mN actuation force. This value allows a systematic study of contact resistance and contact force dependance of different contact materials using the *MEMS relay* as a test vehicle. Eight pairs of zipper electrostatic actuators are employed to achieve this force.

5.1.4 Die level packaging: structure release, actuator isolation, wire-bonds, and ceramic package

The die level packaging for *MEMS relay 2* involves the release of the moving structure, the isolation of actuators and contacts after bonding, the integrated circuit (IC) package, and the wirebonds that connect the device to the IC package.

5.1.4.0.4 Structure release and actuator isolation. During processing and prior to bonding, sacrificial structures are needed to provide support and electrical conductivity to the zipper electrodes. After bonding and electroplating, these connecting structures must be removed to isolate the actuator electrodes. In *MEMS relay 1*, sacrificial tethers were employed for this purpose. The tethers were snapped-off using a probe needle, which generates large amounts of Si particles. The ejected silicon particles have to be removed by blowing nitrogen on the die or by sonication in a solvent. The processes of snapping the tethers, and removing the ejected silicon

particles from the die are cumbersome and time consuming.

Two alternative methods of isolation and release are explored for *MEMS relay 2*: ablation and cutting of the tethers. Silicon ablation with an excimer LASER is a slow serial process, that is prone to re-deposition of silicon and glass in a region 2-3 spot sizes around the ablation site. The die-saw can isolate multiple structures in each die through a single cut.

The test, shown in Figure 5-6, demonstrated that silicon particles and the die-saw cooling water entered the structure. Most debris stemming from the die-saw isolation process is confined to the vicinity of the cut, and can be removed through sonication in solvents. In general, smaller particles are generated with the die-saw than those formed by breaking off the tabs with a probe.

Alternatively, the connecting tethers could be removed by melting through a high current. However, the literature cites low yields and great probability of material re-deposition [9]. The actuator isolation and release strategy selected for *MEMS relay 2* is to perform a cut through the silicon using the die saw. The height of the blade can be adjusted to clear the glass handle, and to cut only through the silicon.

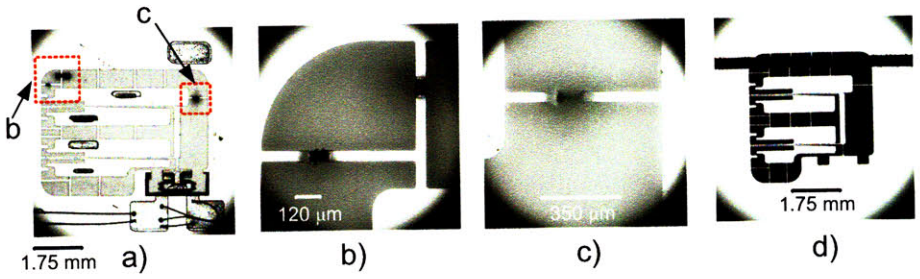


Figure 5-6: Structure release and actuator isolation tests. Ablation of connecting tethers with an excimer LASER (a,b,c), notice damage is constrained to the ablation site; the process however is slow as each tether must be ablated sequentially. Isolation through a die-saw cut through the connecting tethers (d); multiple tethers can be isolated through a single die-saw cut.

5.1.4.0.5 Packaging strategies. The test strategy for *MEMS relay 1* was to test at the wafer level. Power and signals were interfaced through probe needles using micropositioners (Quater Research and Development, Bend OR). The lack of

die level packaging made testing cumbersome since a total of seven needles had to be individually adjusted over each device to be tested. This setup also limited the maximum load current which could be tested as the probe needles failed at currents exceeding 3 A.

A die level package was sought for *MEMS relay 2* to simplify testing, and to provide a reliable interface capable of handling higher load currents than with the probe needles. The packaging strategy selected for *MEMS relay 2* is to singulate the wafer into individual die and to mount them onto a pin grid array (PGA) IC package. The die is then connected to the PGA via 1 mil Au wire using a ball-wedge wire bonder. The packaged die is then tested on a zero-insertion-force (ZIF) test socket[3]. The PGA[4] has a square cavity size of 1.3 in and 180 pins.

5.1.5 Increase in contact overlap and contact travel

In the {111} contact geometry, both contact overlap and travel are inherently coupled. An increase in overlap was sought for *MEMS-relay 2* in order to increase the apparent contact area without increasing the contact footprint. On *MEMS relay 2*, the contact travel was increased from 32 μm to 70 μm, which increased the contact overlap from 27 μm to 54 μm. The planar dimensions of the moving contact were maintained at 1 mm.

Overall, the planar contact length was reduced by the width of the isolating trench: 150 μm for the straight trench and 300 μm for the shaped isolation trench.

5.1.6 Decoupling of compliant mechanism and actuators

In *MEMS relay 1*, the zippers served both as moving electrodes for the electrostatic actuators and as flexural elements for the compliant mechanism. While this strategy may reduce the footprint of the die, it also presents its own drawbacks. It was noted from the operation of *MEMS relay 1* that process inherent tolerances produced slight

[3]3M/TEXTOOL, P/N 2181-6319-9UA-1902, purchased from Linear Sales Inc., Marlton NJ.

[4]Kyocera, P/N IPKX8F0-2096A, purchased from Spectrum Semiconductor Materials, San Jose, CA

differences in geometry between the top and the bottom spring. Further, it was observed that the zipper's point of contact did not run exactly at the same rate in both the upper and the lower spring.

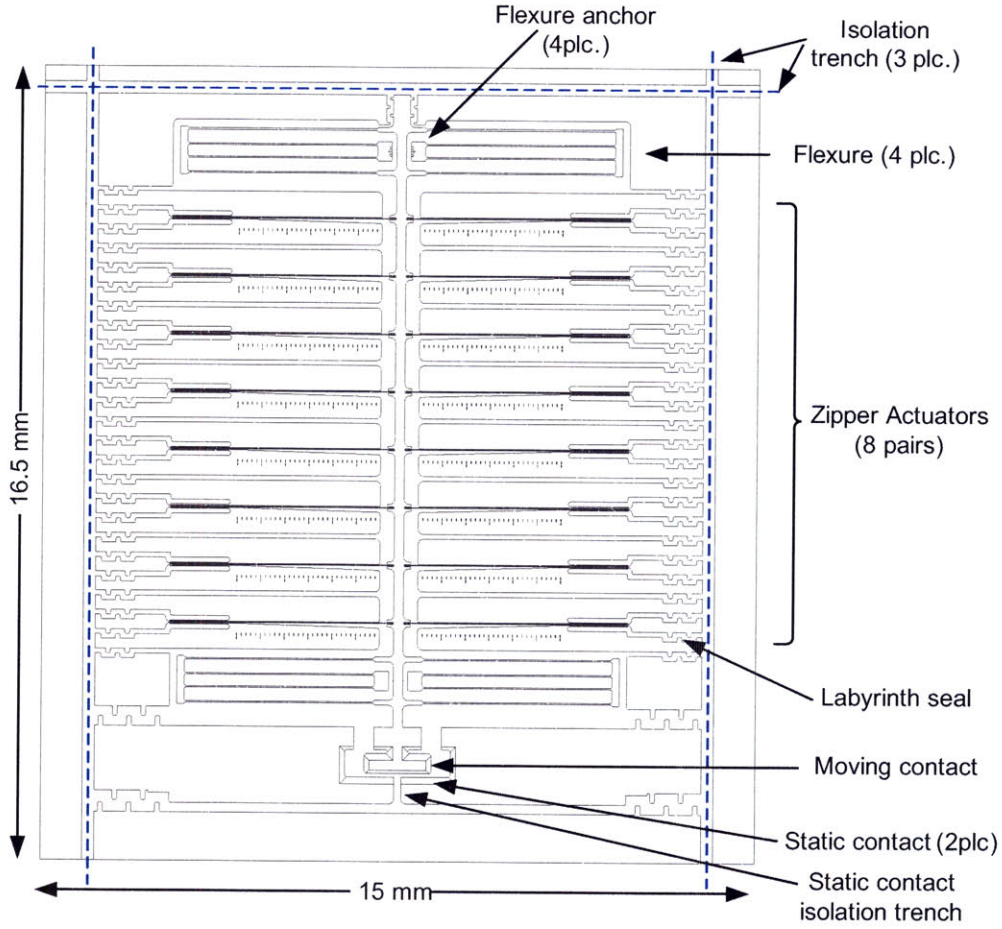
During operation, significant performance variation was observed as *MEMS relay 1* cycled. The electrical contact resistance varied significantly with values ranging from open-circuit to 130 mΩ. This variation was attributed to a low actuation force and to an over-constrained condition of the spring-zipper elements. For *MEMS relay 2*, it was decided to decouple the actuators from the compliant mechanism in order to alleviate this condition.

5.2 Design of the second relay

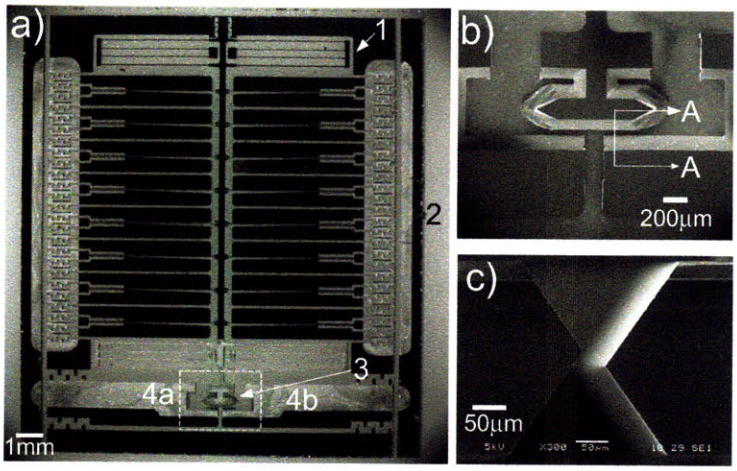
The second MEMS-relay was redesigned based on the functional requirements listed in Section 3.1, and on the criteria listed in Section 5.1. As in the previous design, the new relay is comprised of a silicon device layer, micromachined through a combination of DRIE and KOH etching, which is bonded to a glass handle. The glass handle provides mechanical structure and electrical isolation.

The second relay, shown in Figure 5-7, employs the following elements: (1) a pair of static and one moving {111} contacts; (2) a compliant mechanism comprised of four double parallelogram flexures; (3) eight pairs of Zipper electrostatic actuators, and (4) packaging which includes: features for isolation of the actuators, singulation of the dies, a Pin Grid Array (PGA) IC package, and wire bonds.

Although not absolutely necessary, the symmetric layout of the actuators and the flexures reduces parasitic motion caused by fabrication inaccuracies, and can accommodate a large number of actuators for an increased actuation force. The compliant mechanism consists of two pairs of double parallelogram flexures attached to the ends of a connecting beam. The connecting beam acts as the primary stage of the double parallelogram flexures and supports the moving contact. The Zipper actuators connect to the beam through patterned slots. Figure 5-8 shows a modified view of *MEMS relay 2* in which the zipper actuators have been removed for clarity.



(a)



(b)

Figure 5-7: Second relay – *MEMS relay 2*: (a)*MEMS relay 2* concept. For clarity, the handle wafer and the metal film are not shown; (b)*MEMS relay 2* fabricated device: a) device top view; b) contact detail prior to metal deposition; c) contact cross section A-A

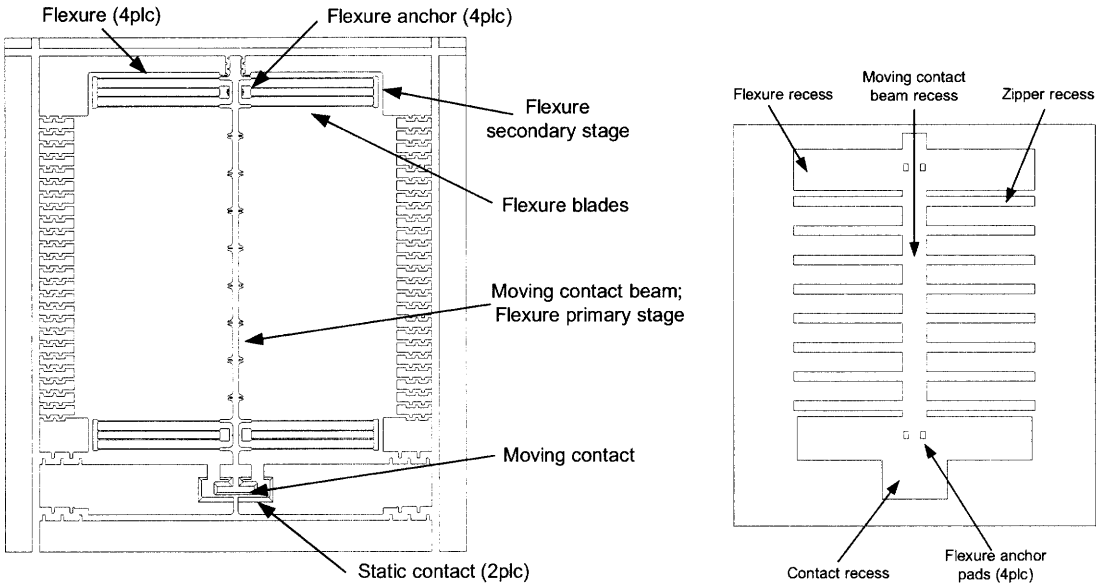


Figure 5-8: *MEMS relay 2* device and handle wafer: (a) Modified view of the device layer to highlight the flexure arrangement. In this view the zipper actuators and the handle wafer have been removed for clarity. (b) Handle wafer. A recess for the moving elements and the contacts is bulk micromachined into the glass. Notice the Flexure anchor pads to which the flexures are anodically bonded to the glass handle.

Eight pairs of zipper electrostatic actuators are arranged in-between the double parallelogram flexures. Through multiple zippers, the actuation force is increased while the pull-in voltage is held constant. This is because the pull-in voltage is a function of the initial gap between the starting electrode and the actuator's compliance.

Figure 5-9 shows a variation of *MEMS relay 2* which includes a flexural element between the moving contact and the contact beam. The compliance provided by the contact flexure is intended to accommodate small fabrication and electroplating inaccuracies. These inaccuracies could otherwise keep the moving contact from establishing ohmic contact with both static contacts upon relay closure. This was confirmed during testing. Dies with both geometries (with and without the contact flexure) were fabricated on the same wafer.

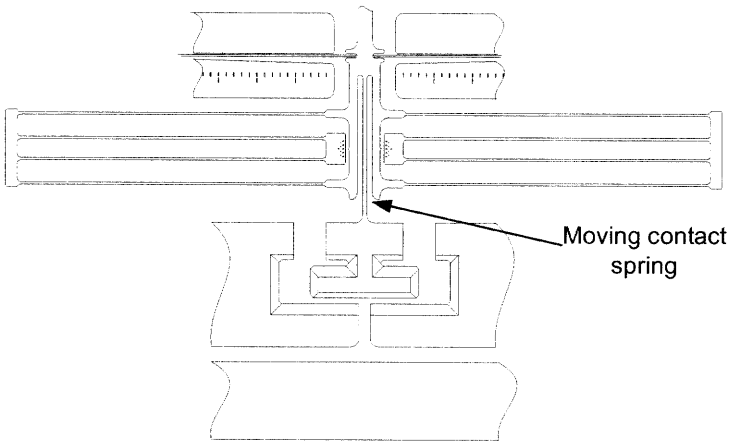


Figure 5-9: *MEMS relay 2* concept variation - moving contact spring. The flexural element at the base of the moving contact can accommodate small fabrication and electroplating inaccuracies to evenly distribute the contact force between the moving contact and each one of the two static contacts.

5.2.1 {111} Contacts: isolation of the static contacts

The main difference in the contact geometry between the first relays and the second relays is the introduction of a trench that isolates the two static contacts from each other. Through this trench, the breakdown path between the static contacts through

the common silicon substrate described in Section 5.1.2 is avoided. The edges between the isolation trench side-wall and the KOH mask form convex corners. Unlike concave corners, which are self-terminating when etched in orientation dependant etchants, convex corners are not self-terminating and will bevel if left unprotected or uncompensated. There are many techniques used to keep convex corners from beveling during orientation dependant etching; these techniques can be grouped into compensating structures and into passivating techniques.

Convex corner compensating structures (CCCS), which may be square, rectangular, triangular, or polygon in shape [38], are sacrificial structures added to the etch-mask. The sacrificial structures are etched away during the orientation dependant etch, leaving behind the desired geometry. The main benefit of using CCCS is that no additional processing is required. Although often employed, CCCS have two drawbacks: (1) they are not self-terminating, and (2) their design is highly dependant on the etch chemistry, on substrate conditions, and processing sequence. The selectivity of fast-etching higher order planes such as {411} to slower etching planes such as {111} is highly dependent on the etchant chemistry and concentration, temperature, use of additives such as surfactants, substrate properties such as doping type, doping concentration, method of crystal growth (Czochralski growth, CZ, or float-zoning, FZ), lighting conditions during the etch [48], and even on the previous processing steps [18]. Thus a design which yields perfect convex corners is difficult to achieve and often involves several iteration steps. Since CCCS are not self terminating, their use relies on adequate timing of the etch. If the etch is stopped slightly too early, part of the CCCS will remain. On the other hand, if the etch is stopped slightly too late, then some beveling will occur.

Passivation techniques are self terminating and thus more robust to implement from a design and a fabrication point of view. The main drawback is that passivation techniques require one or more additional fabrication steps. Examples of passivation techniques are the fabrication of perfect {111} intersecting geometries to form the contacts in this thesis, intersecting {111} geometries in microfluidic channels [28, 23], and the use of LOCal Oxidation of Silicon (LOCOS) in vertical geometries to form

vertical convex corner compensation [11]. By growing oxide over etched trenches using the LOCOS process, the passivated vertical sidewalls protect the convex corners and keep them from beveling.

Figure 5-10 shows a detail of the interface between the KOH mask and the DRIE isolation trench. Three types of corners on the KOH mask are indicated: (1) self terminating concave corners, (2) convex corners masked with convex corner compensating structures (CCCS) also used in *MEMS relay 1*, and (3) convex corners masked with vertical sidewall compensation.

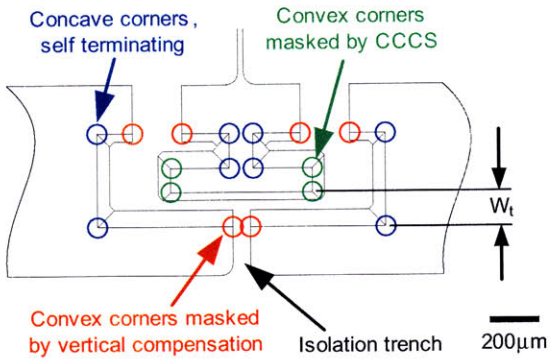


Figure 5-10: *MEMS relay 2* contact detail - convex and concave KOH mask corners. Three types of corners on the KOH mask are indicated: (1) self terminating concave corners, (2) convex corners masked with convex corner compensating structures (CCCS) , and (3) convex corners masked with vertical sidewall compensation.

The KOH mask width dimension was adjusted to account for mask undercut per the results of the design of experiments presented in Section 3.2. Since the mask undercut is difficult to control, relays with three different KOH mask dimensions $W_t = W_b$ were fabricated on the same wafer, as indicated in Table 5.1. The mask offset between the wafer front and the wafer back KOH masks was maintained constant for all die with a nominal value of $30\,\mu$m.

Two isolation trench shapes were patterned. The first trench geometry, a (110) oriented slot shown in Figure 5-11, resulted in small protrusions projecting from the bottom of the {111} contact at the intersection with the isolation trench. The second tench geometry, a tapered shape as shown in Figure 5-12, eliminated the formation of the protrusions seen in Figure 5-11.

Table 5.1: KOH mask dimension *MEMS relay 2*; $W_t = W_b$

Split	Corrected mask undercut [μm]	Mask dim. [μm]	Fabricated dim. [μm]
A	2.5	237.5	260.3
B	5	232.5	254.6
C	7.5	227.5	253.6

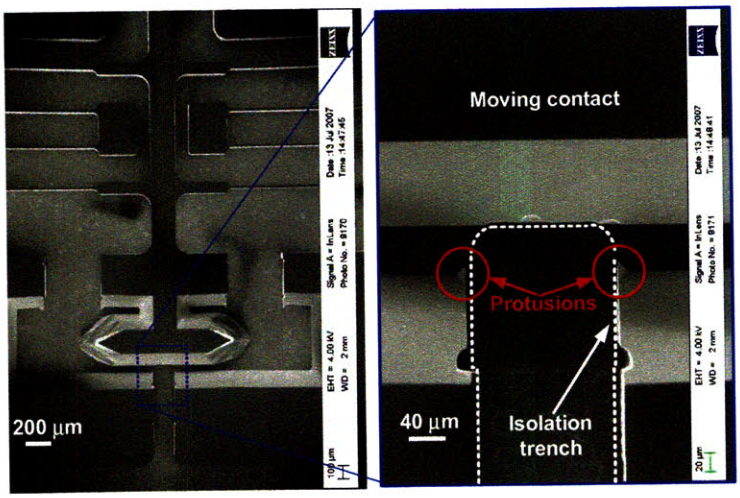


Figure 5-11: Straight isolation trench *MEMS relay 2* - fabricated contacts. The straight isolation trench geometry results in the small protrusions extending from the bottom of the {111} contact at the intersection with the isolation trench.

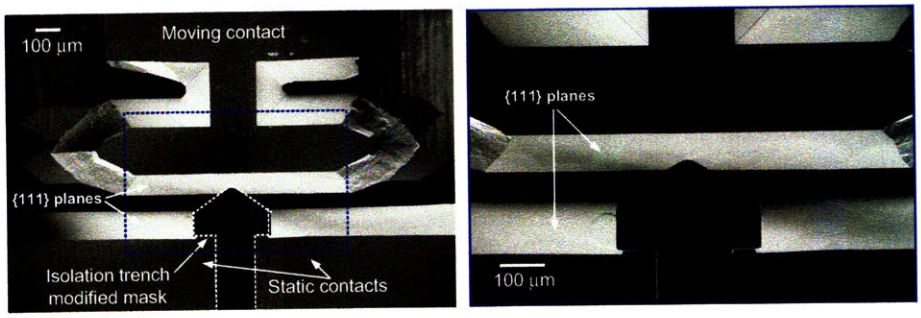


Figure 5-12: Shaped isolation trench *MEMS relay 2* - fabricated contacts. The wedge shaped isolation trench geometry eliminates the formation of the small protrusions formed with a straight trench geometry.

5.2.1.0.6 Wafer front to wafer back alignment features. A scale was patterned on the wafer back alignment mark, to allow for variations in the wafer-front to wafer- back KOH mask offset. Although this feature was not used to alter the mask offset from its nominal value it could have been used to adjust for mask undercut and to adjust the contact travel.

5.2.2 Flexures

The compliant mechanism for the second relay is comprised of four double parallelogram flexures mounted on the four corners of the moving contact beam, as shown in Figure 5-8(a), and in detail in Figure 5-13. These flexures provide rectilinear motion in the direction normal to the blades. Compared to a single-stage parallelogram flexure, the two stage symmetry in the double parallelogram flexure cancels the parasitic error normal to the direction of motion, and provides half the traverse stiffness of a single-stage parallelogram flexure.

Double parallelogram flexures, are susceptible to parasitic errors, which are reduced by having symmetric designs, and by applying the loads at the center of the primary stage[55, 2]. Once bonded to the handle wafer, the anchor pads of the flexures close to the moving contact are temporarily wire bonded to the static contacts. This allows electroplating of the moving contact. Alternative strategies to electroplate the moving contact are (1) to make ohmic contact to the gold seed layer through the highly doped silicon substrate, or (2) to run a conductive trace along the length of the beam connecting the flexures. The main disadvantage of electroplating through the underlying silicon is that the breakdown-voltage between the zipper actuators and the moving contact is reduced by 100 V, namely the dielectric strength provided by 2 k AA of thermally grown silicon dioxide. Running a conductive trace along the length of the moving structure is difficult to mask due to the limited width of the moving structure.

The stiffness of a double parallelogram flexure, derived from beam-bending theory is

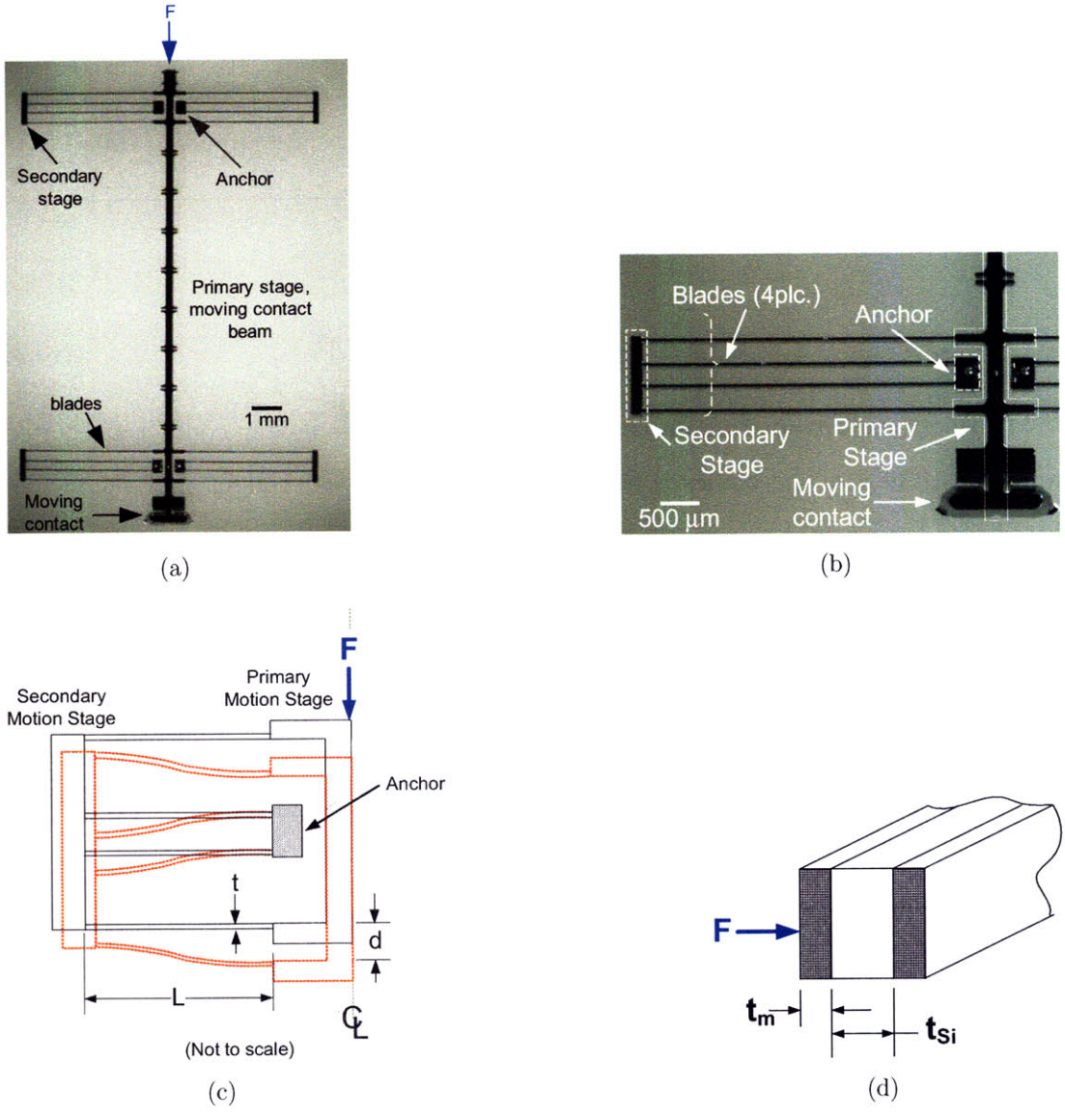


Figure 5-13: Flexure details *MEMS relay 2*. (a) Optical micrograph of the moving elements: the flexures, the beam, and the moving contact; (b) optical micrograph detail of the flexure; (c) flexure concept; (d) flexure cross section after electroplating

Table 5.2: Second relay flexure dimensions and stiffness values

	Units	Designed	Fabricated
Blade length L:	μm	2000	2000
Blade breadth b:	μm	300	300
Blade thickness t_{Si}:	μm	25	25
Plated thickness t_{metal}:	μm		10
Unplated single flexure stiffness k_{Si}:	μN/μm	11	11
Plated single flexure stiffness k_{metal}:	μN/μm		90
Total plated flexure stiffness $4k_{Si} + 2k_{metal}$:	μN/μm	44	224

$$k_{\delta_x F_x} = (12EI_{zz})/(L^3) = Eb(t/L)^3 \tag{5.2}$$

During the electroplating process, both flexures by the moving contact are plated and the stiffness of the blades is increased. Initially, it was thought that the evaporated seed layer would be very thin along the blades and would only be plated a small amount. However, it was found that as much as $10\,\mu$m of metal were electroplated on each face of the blades. This increased the stiffness of the flexures five-fold.

Table 5.2 shows the designed and fabricated flexure dimensions and stiffness values. The material properties of silicon and copper used in the calculations are $E_{Si} = 160\,GPa$, $E_{Cu} = 130\,GPa$. The flexures were designed not to exceed the allowable stress of 170 MPa for Si and 200 MPa for Cu.

The natural frequency of the flexures at various stages during processing (prior to bonding and release, before and after KOH etching) was determined analytically and through finite element analysis (FEA) using Pro/Mechanica[5].

The modal analysis of the relay after bonding and release sets a theoretical limit on the maximum frequency of operation. The modal analysis prior to bonding and release is important in terms of fabrication. As a rule of thumb, a minimum fundamental resonance frequency of 1 kHz is recommended in order to withstand processing in tools such as the spin-rinse-dryer (SRD).

The out-of-wafer-plane modes are of particular concern as was determined dur-

[5]Settings: multi-pass adaptive, 6th order polynomial, 10% conversion

Table 5.3: Modal analysis second relay, prior to KOH-etch and structure release

	Frequency [kHz]	Plane
First Mode f_1:	1.415	In the wafer plane
Second Mode f_2:	3.848	In the wafer plane
Third Mode f_3:	8.617	Out of the wafer plane
Fourth Mode f_4:	11.123	Out of the wafer plane

Table 5.4: Modal analysis second relay, after KOH-etch and prior to structure release

	Frequency [kHz]	Plane
First Mode f_1:	0.748	In the wafer plane
Second Mode f_2:	1.10	Out of the wafer plane
Third Mode f_3:	1.34	In the wafer plane
Fourth Mode f_4:	1.4	In the wafer plane

ing the fabrication of the first relay. This is because the radii between the etched structures and the wafer plane are practically non-existent in this direction.

The lowest mode is below the recommended 1 kHz value, the first mode out of the wafer plane is slightly above the recommended value. As would be expected due to the larger mass, the modes after KOH etching are lower than those prior to KOH etching.

The first four modes of the structure during fabrication (prior to bond and structure release) are given in Tables 5.3, and 5.4 while the shape of the modes are given in Figures 5-14, and 5-15.

Note that the modes *prior to KOH etch* are listed in Table 5.3 and Figure 5-14, while the modes *after KOH etch* are listed in Table 5.4 and Figure 5-15.

5.2.3 Zipper Actuators

Eight pairs of compliant-starting-zone zipper actuators [32, 33] provide a theoretical force of 40 mN during the closing and opening events, a pull-in voltage of 65 V and a 70 μm travel. Electrostatic actuation was chosen due to its low, virtually negligible, power consumption and heat generation. Compliant-starting-zone Zipper actuators

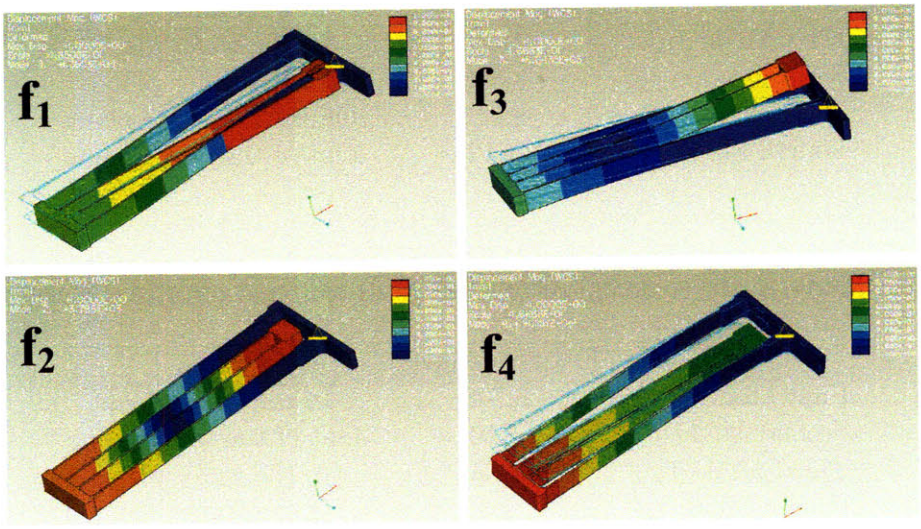


Figure 5-14: Modal analysis prior to KOH etch and structure release

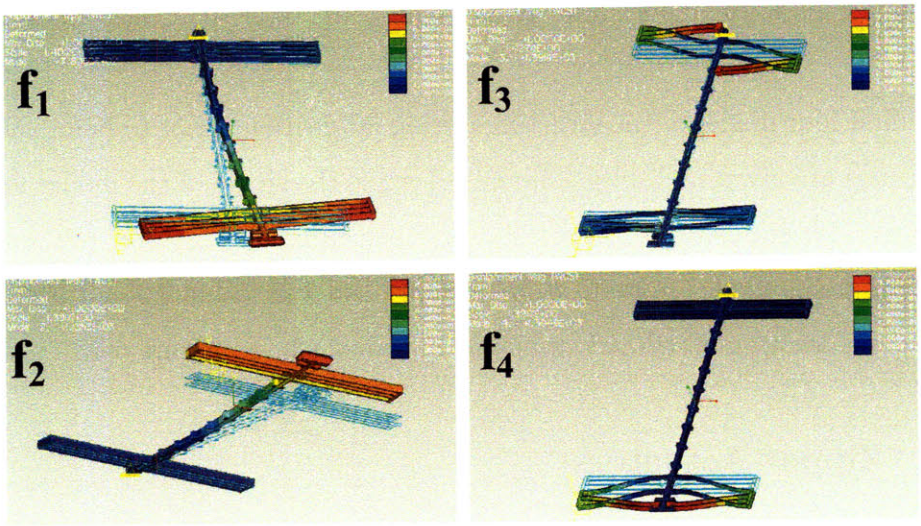
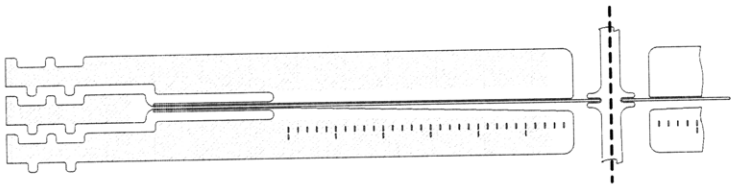
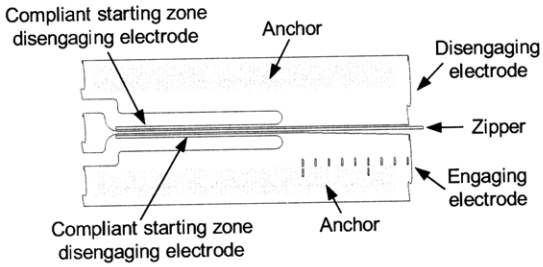


Figure 5-15: Modal analysis after KOH etch and prior to structure release

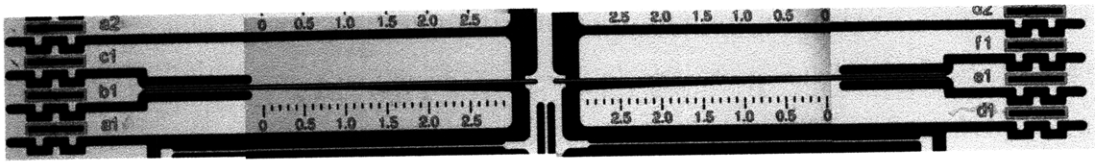
were selected to reduce the pull-in voltage, while providing the required displacement and force.



(a)



(b)



(c)

Figure 5-16: Zipper actuator details *MEMS relay 2.* (a) Zipper actuator concept; (b) Zipper compliant starting zone detail; (c) Optical micrograph of a fabricated pair of zipper actuators.

The force-displacement expression of a pair of Zipper actuators [32, 33] is described by

$$F_{zipper} = 0.614 \frac{E^{1/4} b}{(\Delta - d)^{1/2}} \left(\frac{\varepsilon_o \varepsilon_r U^2 h}{h_o} \right)^{3/4} \tag{5.3}$$

where E is the Young's modulus of Silicon ($160\,GPa$), b is the wafer thickness ($300\,\mu m$), Δ is the maximum travel ($70\,\mu m$), d is the travel, ε_o is the permittivity of free space ($8.85 \cdot 10^{-12} \frac{F}{m}$), ε_r is the relative permittivity of SiO_2 (3.8), U is the voltage applied, h is the thickness of the zipper ($20\mu m$), and h_o the total dielectric thickness ($2 \cdot 200\,nm$). The constant (0.614) is derived from FEA [33].

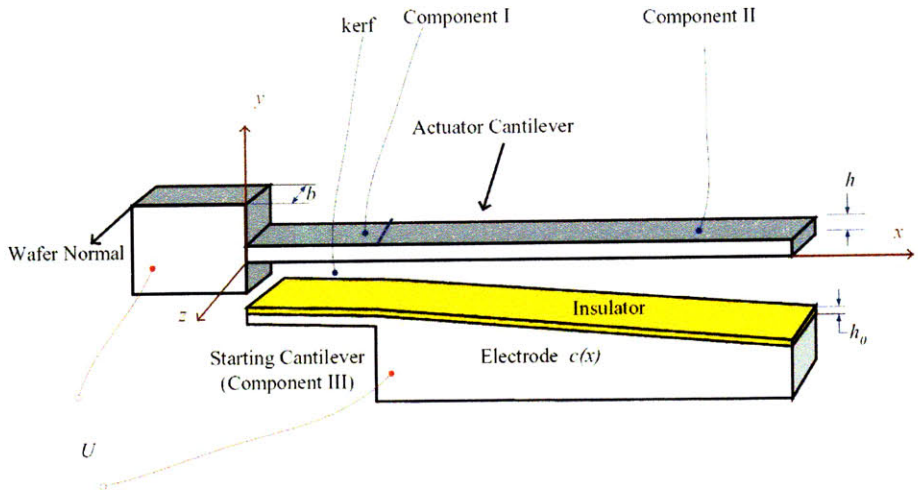


Figure 5-17: Zipper actuator variable definitions, reproduction from [33]

Figure 5-18 shows the calculated force output per pair of electrostatic actuators. This force accounts for the strain in the zipper actuators, but not for the strain of the compliant mechanism springs or for the strain in the contact spring. The model assumes perfectly etched geometry. In practice, the zipper geometry after DRIE-etch is not perfect. The DRIE introduces taper of about 2.5 μm on each side of the zipper with the bottom being wider than the top. This condition increases the effective minimum separation between the zipper and the electrode, which in the case of ideal geometry equals the thickness of the dielectric film h_0. Considering the geometric inaccuracies introduced by the DRIE step, the calculated force exerted by a pair of zipper actuators is about half of the theoretical value [33], or 5 mN in our case. The effective actuation force of 8 pairs of zippers at 100 V and full travel is 40 mN.

5.2.4 Packaging

The anodic bonding process provides structural rigidity and electric isolation of the different functional elements in the relay, such as the actuators and the static contacts. After anodic bonding and electroplating, the actuators and the static contacts must be isolated from the rest of the die, and the moving structure must be released. This is done through three blind cuts made with the diesaw. The device side of the wafer stack is protected with dicing tape during the dicing operation at which the diesaw

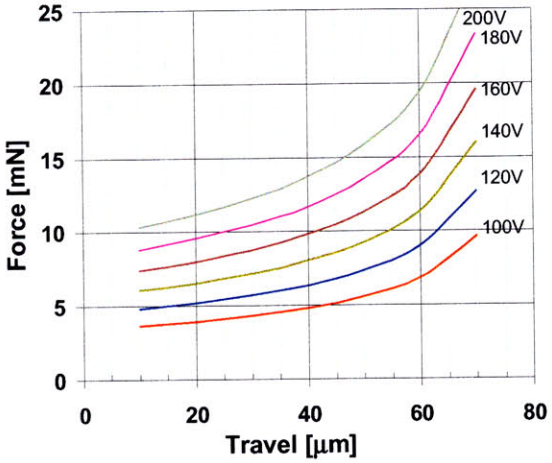


Figure 5-18: Electrostatic zipper actuator forces per zipper pair, perfect etch geometry

blade is set high enough to cut through the device wafer and 50μm into the handle wafer. Figure 5-7(a) shows the location of the die-saw cuts.

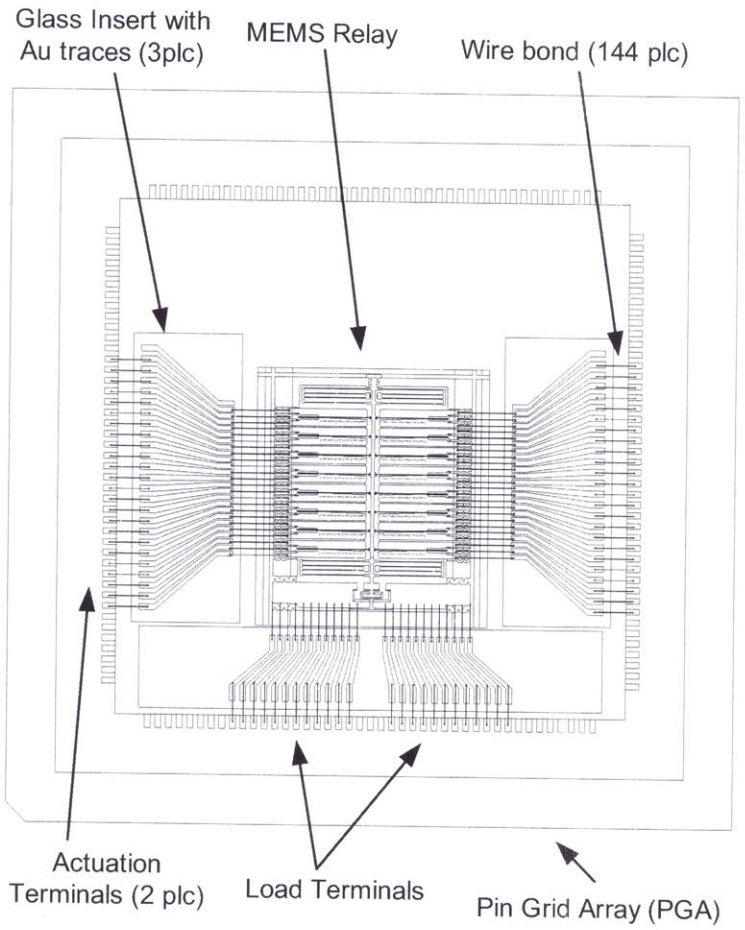
A labyrinth seal provides a torturous path which keeps the diesaw slurry, and particles from entering the delicate parts of the die, such as the zippers. This seal is very effective. The debris generated by the diesaw accumulates in the outer part of the seal where it was easily flushed using solvents in an ultrasonic bath. After the actuators have been isolated and the structure has been released, the diesaw is used to singulate the individual relays which are then mounted onto a Pin Grid Array (PGA)[6] IC package and wire-bonded for testing, as shown in Figure 5-19.

The 33 mm (1.3 in) PGA cavity is much larger than the 15 mm x 16.5 mm relay die. In order to keep the wirebonds as short as possible, glass inserts with patterned gold traces are mounted onto the PGA. The gold traces are wirebonded to the PGA and to the die.

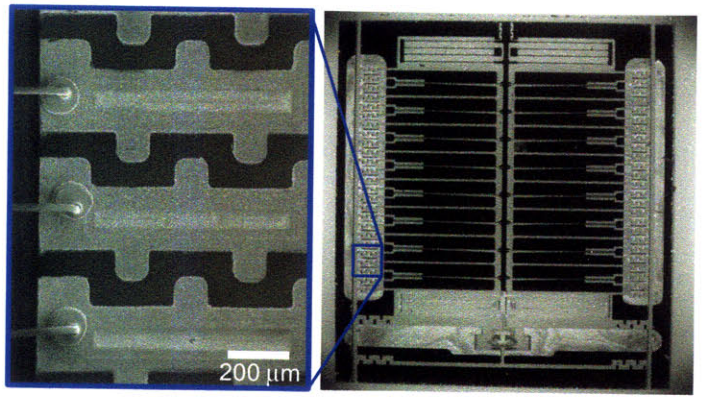
5.3 Fabrication, second MEMS relay

The *MEMS relay 2* fabrication process is based on the perfect corner KOH etching process using passivation [23, 28], and on the vertical convex corner compensation

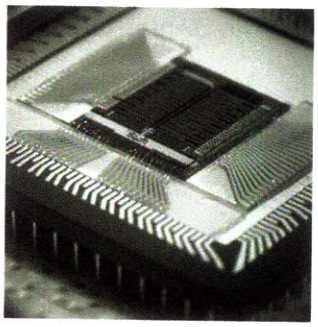
[6]Kyocera, P/N IPKX8F0-2096A, purchased from Spectrum Semiconductor Materials, San Jose, CA



(a)



(b)



(c)

Figure 5-19: *MEMS relay 2* packaging. (a) Packaging concept; (b) Detail of the die-saw isolation cut, the actuator wire bonds, and the labyrinth seal; (c) Optical micrograph of the packaged relay.

process for orientation dependant etching [11]. Similar to the fabrication of *MEMS relay 1*, alternating patterned Si_3N_4 and SiO_2 films serve as nested masks for the KOH etch. The fabrication process of *MEMS relay 1* employed Si_3N_4 as a KOH mask and as a passivation layer. The new fabrication process utilizes CVD SiO_2 as a KOH mask, and LOCOS SiO_2 as a passivation layer. This change in materials enables simple wet etches to replace the shadow wafers used to pattern the nested masks, streamlining the fabrication process. The new fabrication process is summarized in Figure 5-20, and presented in detail in Appendix A. Die level views of the masks used in this process are given in Appendix B.

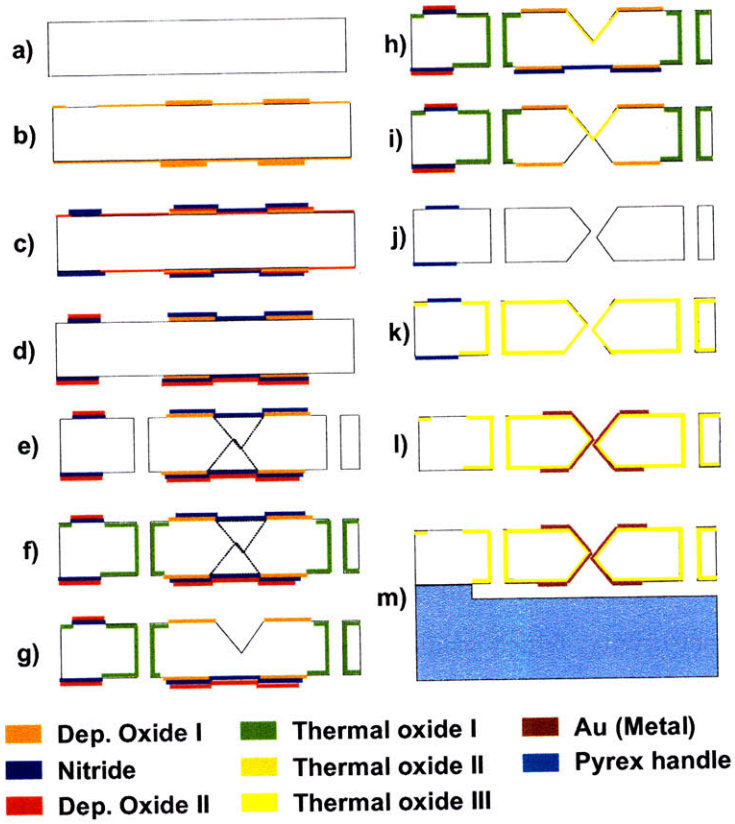


Figure 5-20: Fabrication process *MEMS relay 2*

The relay is fabricated on 6-inch, n-type, highly doped (0.01-0.02 Ω-cm), (100), $300 \pm 5\,\mu$m thick, DSP silicon wafers[7]. A low resistivity substrate is needed since the electrical connection to the actuators is routed through the silicon. N-type doping

[7]Supplied by Silicon Quest International (SQI), Santa Clara, CA.

is required to avoid the Schottky contact formed between metallization layers and a p-type substrate. The substrate's thickness is set by a 25:1 aspect ratio limit on the DRIE etch, while the thickness tolerance is determined by the {111} contact error-budget presented in Section 3.2.2. The substrate's (100) orientation is required for etching of the {111} contacts.

The substrate thickness and tolerance are non-standard for 6-inch silicon wafers. Therefore, the wafers are ground and polished to specification by the vendor. Initially, the grinding and polishing process was carried out on a single side of the substrate, which resulted in extremely fragile wafers due to stress concentration at the edge of the substrate. Double-sided grinding and polishing of the substrates yielded a rounded, "bullet" shaped edge, which resulted in less fragile substrates. Wafer edge grinding is a common process used on standard thickness substrates to reduce stress concentration at the wafer edge. This step could not be performed on the wafers used here due to the specified thickness and tolerance.

5.3.1 Nested KOH masks

Initially, alignment marks are patterned on both sides of the wafer. A 3μm thick oxide film is deposited through CVD[8], and is patterned on both wafer sides to define the KOH mask using masks C and D, as shown in Figure 5-20(b). The oxide etch is carefully characterized and monitored to avoid excessive etching of the silicon, caused by low selectivity, which would affect the {111} contact travel as described in Section 3.2.2. The 3μm thick oxide is designed to withstand two consecutive three hour long KOH etches, various dry- and wet-etch steps, and to prevent damage caused by pin-holes in the oxide. Experiments demonstrated a CVD SiO_2etch-rate of 6.1 nm/min for with our particular etch chemistry. This is lower value than the 8 nm/min published in the literature [68, 67].

After definition of the KOH mask, a 500 Å thick CVD oxide etch stop is deposited and patterned on both sides of the wafer. Mask E defines the contact pads for wire

[8]Deposition in Centura 5200 CVD system, etching in Centura 5300 High Density Plasma SiO_2 etcher; both tools by Applied Materials

bonding to the zipper actuators.

A 2.5 kÅ silicon-rich nitride[9] cover is patterned through DRIE[10] on both wafer sides, stopping on the 500 Å oxide etch-stop, as shown Figure 5-20(c). The nitride cap prevents oxidation of the area to be etched in KOH during the LOCOS process. Ideally, a reactive-ion-etch (RIE) tool with SF_6 and O_2 chemistry, such as Applied Materials AME5000 or LAM490B, would be used to pattern the nitride cap. These tools are more selective and uniform than DRIE and do not need an etch-stop. Unfortunately, the handling and clamping mechanisms of both the AME5000 and the LAM490B damage the 300 μm thick wafers. Therefore, the Si_3N_4 is patterned through DRIE using an SiO_2 etch-stop.

A CVD oxide is deposited and patterned on top of the nitride cap using masks F and G. The SiO_2 is 1.75μm thick on the wafer-front-side and 5k Å thick wafer-back-side. The purpose of the SiO_2 cap is to protect the wafer back KOH mask and the actuator contact pads during the first selective wet etch.

The nested masks are completed after stripping the SiO_2 etch-stop through a 1 minute long BOE etch, as shown in Figures 5-20(d) and 5-21.

5.3.2 DRIE and passivation

After patterning the nested masks, 9 μm of AZP-4620 photoresist is spun on the wafer-front to mask the DRIE (Mask J, Figure 5-20(j)). Figure 5-22 shows a die level view of the DRIE mask and of the fabricated device. Large areas that need to be removed have been patterned with *halos*. Halos are unsupported structures which separate from the substrate once the DRIE is completed. These structures maintain a uniform line-width exposed to the plasma, increasing the etch uniformity.

Blue dicing tape[11] is applied to the wafer-back-side, after it has been coated with 1 μm of OCG-825 photoresist. The dicing tape holds the halos in place after the etch is completed. Without the tape, thousands of halos would be dislodged from the

[9]LPCVD deposition in Thermco Systems Vertical Thermal Reactor (VTR) furnace.
[10]Surface Technology Systems STS
[11]Semiconductor Equipment Corporation, Moorpark, CA

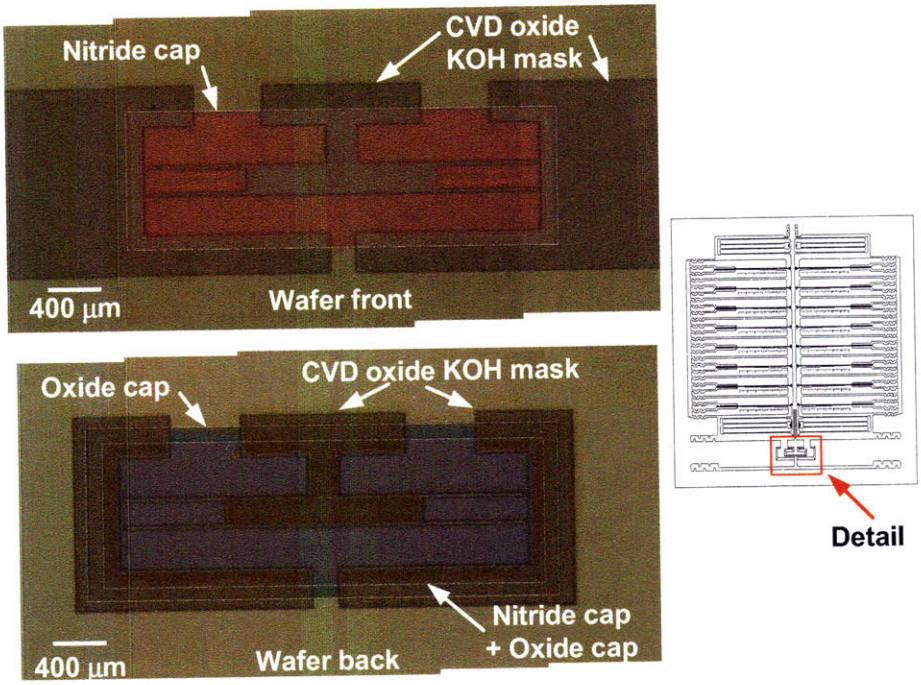


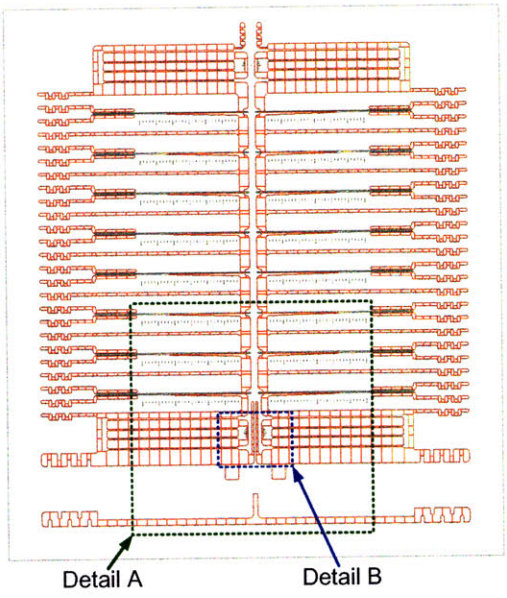
Figure 5-21: Micrograph detail of fabricated nested masks, *MEMS relay 2*. These views correspond to step *d* in Figures 5-20.

wafer through pressure and electrostatic forces and may contaminate the chamber. In addition to the dicing tape, the wafer is mounted on a quartz handle wafer with 8520 photoresist using a"bulls-eye" pattern. The quartz handle is required to protect the device wafer from being damaged by the DRIE-tool[12] clamping mechanism. The clamping mechanism is not aligned with the lip seal. This results in a bending moment applied to the edge of the wafer, causing damage to the etched substrate, as shown in Figures 5-23.

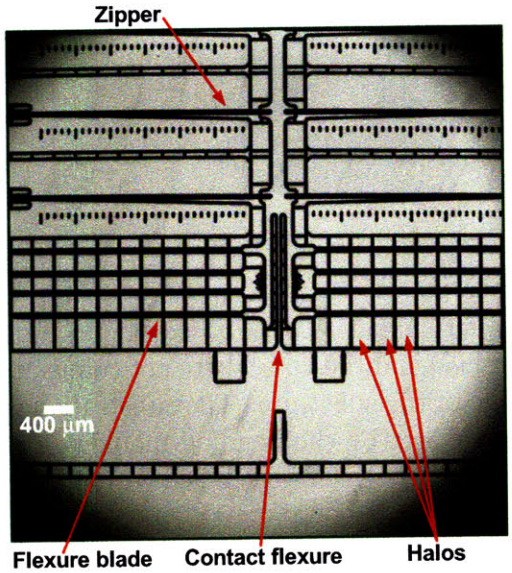
After completion of the DRIE, the wafer is demounted from the dicing tape and from the Quartz handle in solvents. A 2:1 Methanol-Acetone solution minimizes swelling and shrinking of the dicing tape, which can cause damage to the etched device wafer during demounting.

The etched wafer is passivated through the growth of a 1.7 μm thick thermal SiO_2, as sown in Figure 5-20(f). It takes three consecutive runs of a standard 1 *mu*m recipe to grow the 1.7 μm thick thermal SiO_2.

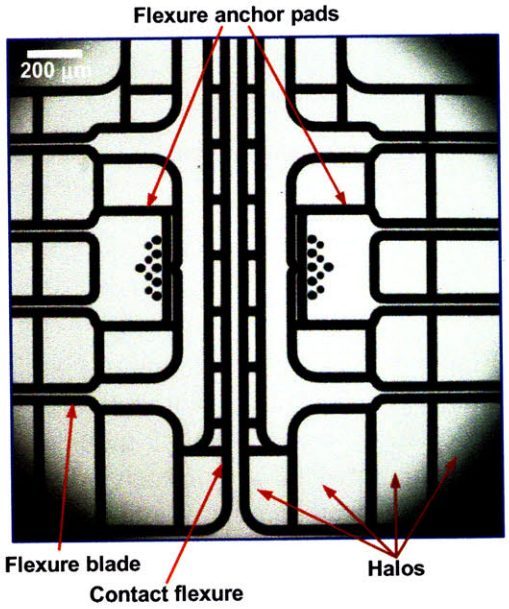
[12]Surface Technology Systems (STS)



(a)



(b)



(c)

Figure 5-22: DRIE mask and fabricated device - *MEMS relay 2*. (a) DRIE mask. The halos are shown in red. (b) Detail A - Optical micrograph of the fabricated device after DRIE. (b) Detail B - Optical micrograph of the fabricated device after DRIE.

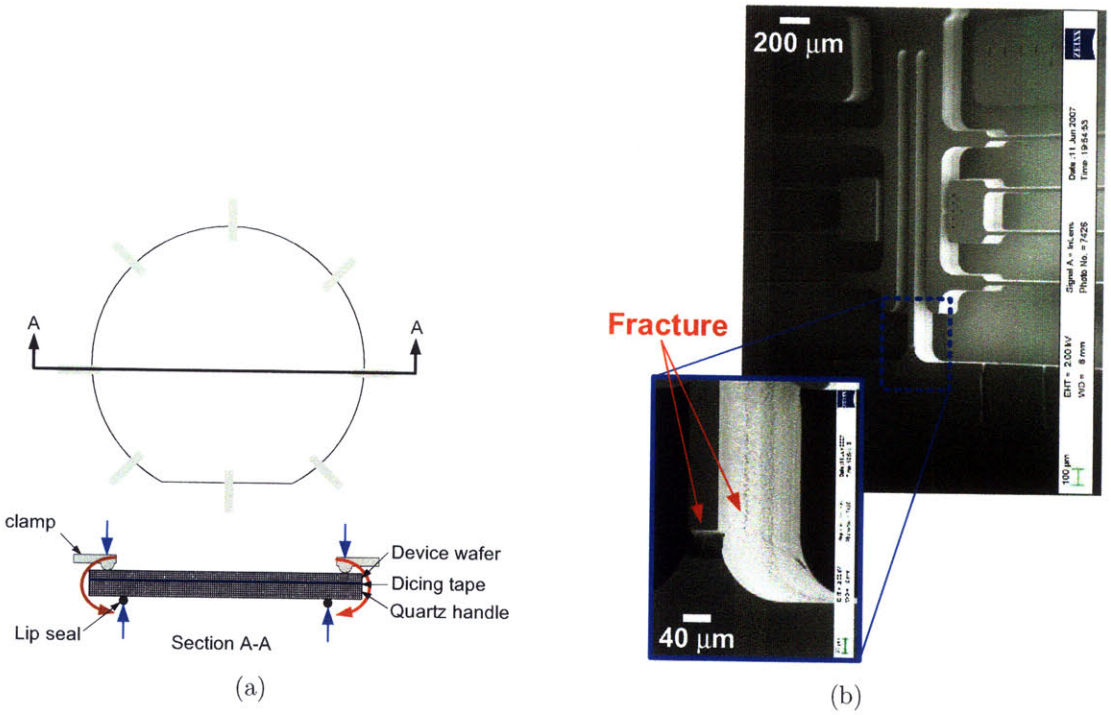


Figure 5-23: DRIE clamping mechanism and wafer damage - *MEMS relay 2.* (a) STS clamping mechanism. Notice that the clamping load and the lip-seal are not collinear, which introduces a bending moment on the edge of the substrate. The substrate has been mounted on a Quartz handle to prevent damage by the bending moment; (b) Scanning electron micrograph of a fractured test device which was etched without the quartz handle.

5.3.3 KOH etch

After DRIE and passivation, the KOH mask on the wafer top side is revealed through selective etching of the nitride cover. A 1 minute long BOE dip strips the oxy-nitride layer formed on the silicon-rich nitride during thermal oxidation. The nitride is etched in phosphoric acid at 165°C. Next, the wafer is etched in a KOH solution, 33 % by weight at 83°C to define the top {111} contacts on the wafer-top (Figure 5-20-g). The contacts are then passivated with a 1.7 μm thick thermal SiO_2 (Figure 5-20-h). The previous wet etch sequence (BOE-dip, hot phosphoric acid etch, KOH etch) is repeated to pattern the {111} contacts on the wafer-back-side (Figure 5-20-i). The nested masks and passivation layers are then stripped through BOE and hot phosphoric acid. Alternatively, straight HF [13] can be used. Straight HF etches SiO_2 at 2300 nm/min [67], and silicon rich Si_3N_4 at 5.4 nm/min, slightly slower than the 20 nm/min etch rate in hot phosphoric acid [67]. A 2 kÅ thick thermal oxide is grown over the device wafer (Figure 5-20-k). This oxide serves as dielectric to the zipper actuators. Finally, the Si_3N_4 cap over the zipper wire bonding contacts is etched in hot phosphoric acid.

5.3.4 Metallization: evaporation, anodic bonding, and electroplating

After the {111} contacts have been etched, both sides of the wafer are metallized with a 2 kÅ thick Ti adhesion layer, and a 0.7 μm thick Au film. These metals are deposited through e-beam evaporation[14] using shadow wafers (Figure 5-20-l). A shadow wafer is a hard mask made by etching through a wafer with DRIE. The shadow wafer is aligned to the device wafer using a wafer-aligner tool[15], and the substrates are fixed with dabs of OCG-825 photoresist placed on the edge of the aligned wafers. After metal deposition, the shadow wafers are dismounted in acetone and the wafer is stripped from organics in an oxygen plasma using an asher. The device wafer is then

[13] 49%

[14] Themascal Semiconductor Products

[15] EVG620 wafer aligner, Electronics Vision Group, St. Florian/Inn, Austria.

Table 5.5: Electroplated films, *MEMS relay 2*

Wafer	Buffer layer material	Buffer layer plating	Hard layer material	Hard layer plating
DW-5, b-1:	Cu	-	2μm Pd-Co (5% Co)	-
DW-A, b-2:	12 μm Ni-Co	600 mA, 30 min	1.5μm Pd	300 mA, 4.5 min
DW-B, b-2:	15 μm Ni-Co	600 mA, 37 min	1.5μm Rh	300 mA, 12 min, pulse

bonded to a borosilicate glass[16] handle wafer through anodic bonding[17](Figure 5-20-m). The handle wafer was previously etched in 660:140:220 H_2O:HNO_3:HF using an evaporated gold mask [64] to create a cavity for the moving elements in the relay: zipper, flexures, moving contact, and contact beam. After anodic bonding, the wafer is electroplated with a buffer metal, and with a noble metal film[18]. The buffer metal serves as a strain relief for the hard metal, which can have film stresses of 300-500 MPa, and to calibrate the travel due to fabrication inaccuracies. The noble metal provides a reliable contact. The moving contact is isolated from the underlying silicon substrate, and is electroplated by wirebonding the front flexure bonding pads to the static contacts. The gold film evaporated over the front flexures is conductive enough to plate the moving contact. After electroplating, the wirebonds are removed under the microscope using a fine pair of tweezers. Table 5.5 summarizes the electroplated films and the plating conditions.

5.3.5 Packaging

Once the electroplating is complete, a diesaw is used to release the actuators and to release the moving contact. During this process, the blade is set to cut only through the device layer, and to clear the glass handle. After isolation and release, the individual die are singulated by cutting with the die-saw through both the device

[16]Borofloat-33 by Schott AG, Mainz, Germany
[17]EVG420
[18]The electroplating process is performed at FormFactor Inc, Livermore, CA

layer and glass handle. The die is then mounted onto a PGA using epoxy resin[19] and wirebonded for testing. Figure 5-24 shows a device after isolation, release and singulation.

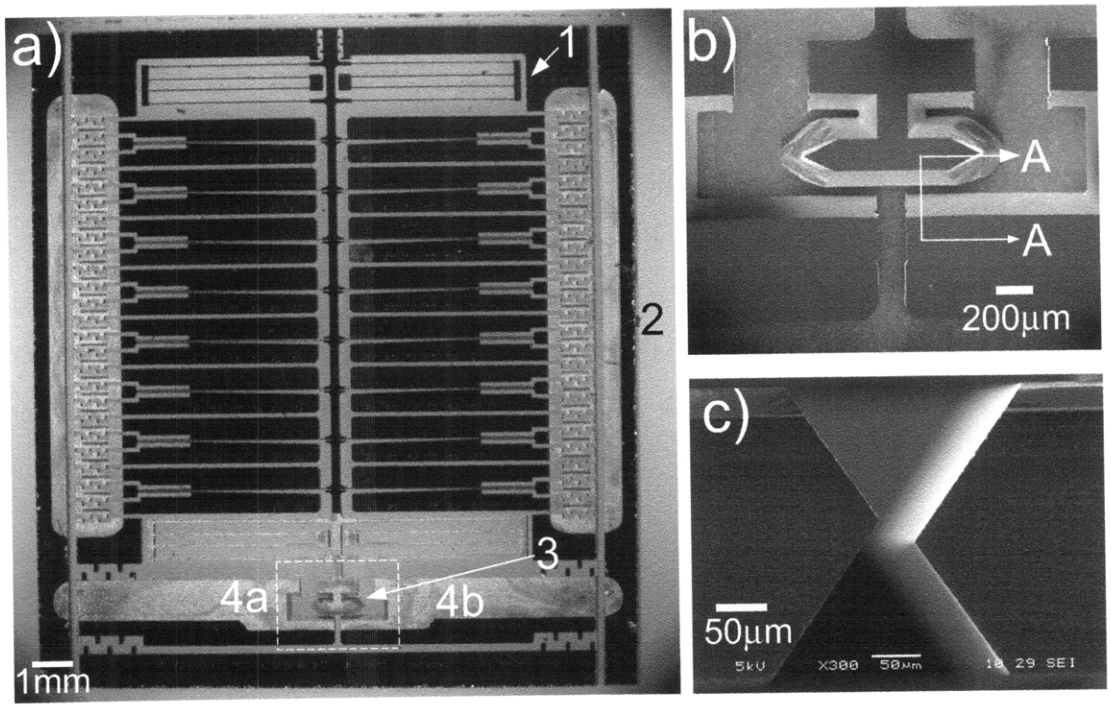


Figure 5-24: *MEMS relay 2*-as fabricated: a) device top view; b) contact detail prior to metal deposition; c) contact cross section A-A.

5.4 Testing of the second MEMS relay

Lack of consistent performance is the main shortcoming of the first relay, so a full characterization of the second relay is the focus of the first tests. These tests are run either without a load, or in the case of the contact resistance measurements, with a very low load current (10-25 mA) also known as a *dry load*. The device characterization tests consist of: (1) actuation, (2) dynamic response, (3) off-state isolation or breakdown, (3) on-state resistance. After device characterization, the relay is hot-switched with increasing resistive and inductive loads until there is any sign of temporary contact

[19]Double/Bubble Hardman by Royal Adhesives, Belleville, NJ.

sticking. Metrology of the contacts is performed through optical and scanning electron microscopy (SEM), before and after hot-switching, to determine wear or erosion patters on the {111} contacts.

5.4.1 Driver circuit

Electrostatic actuators are affected by dielectric charging [44, 45, 5, 43]. This condition develops when charges, injected by strong electric fields, become trapped in a dielectric layer. Charging can be reduced, amongst others, through the use of a bipolar driver, a *peak and hold* actuation voltage, by lowering of the electric field, and through the use of lower trap density dielectric materials. The bipolar driver [33] used for *MEMS-relay 2* is shown in Figure 5-25. This driver reduced the charging effect and increased reliability, as the polarity is switched every time the relay opens and closes.

5.4.2 Test setup

During testing of *MEMS relay 2*, voltages and currents are continuously monitored as the relay cycles, and the instantaneous contact resistance is computed. The test setup is shown in Figure 5-26. Agilent 34401 Multimeters synchronously monitor the voltage across both static contacts ($V_{m\ 1}$), the voltage across the right static contact and the moving contact ($V_{m\ 2}$), and the load current (I_m) as the relay cycles. The relay's transient response is captured with an oscilloscope. The location of the oscilloscope probes are: ($V_{s\ 1}$, $V_{s\ 2}$, $V_{s\ 3}$, and $V_{s\ gnd}$), indicated in Figure 5-26. The multimeters are interconnected via GPIB; a Labview program is used for data acquisition and to control the test instruments. The Labview code is given in Appendix C.

5.4.3 No-load / dry-load tests

5.4.3.1 Actuation

The fabricated zippers fully pull-in at 120 V. This is higher than the calculated value of 90 V for a 14 μm wide initial zipper-to-electrode gap. This difference is attributed

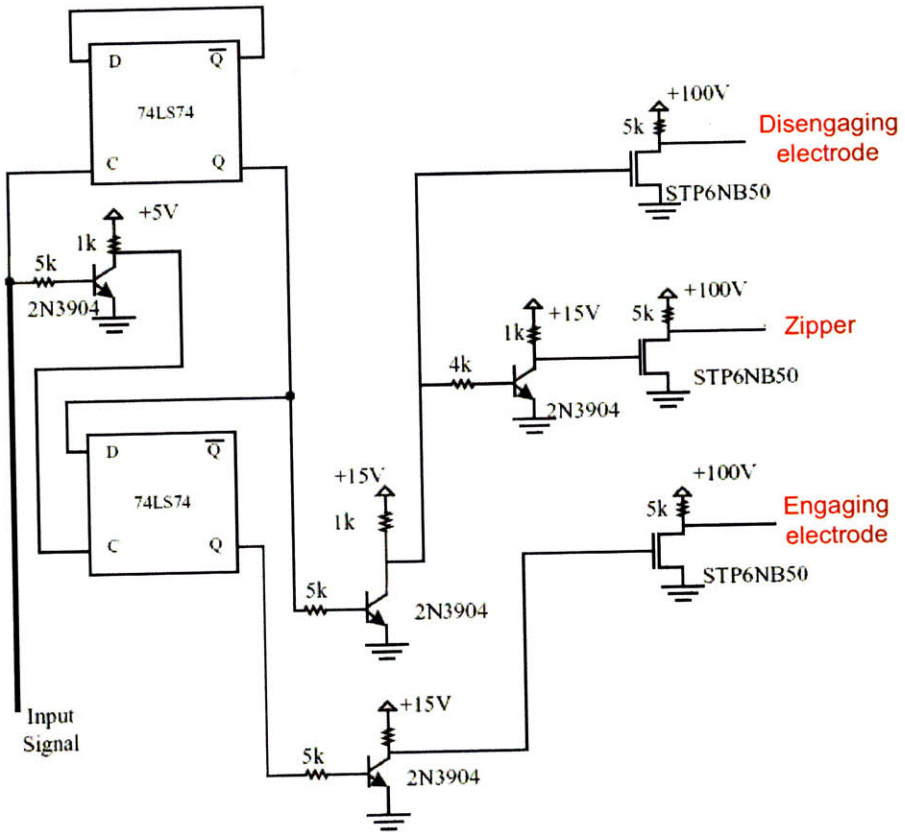


Figure 5-25: Bi-polar driver, after J. Li. Image reproduced from [33]

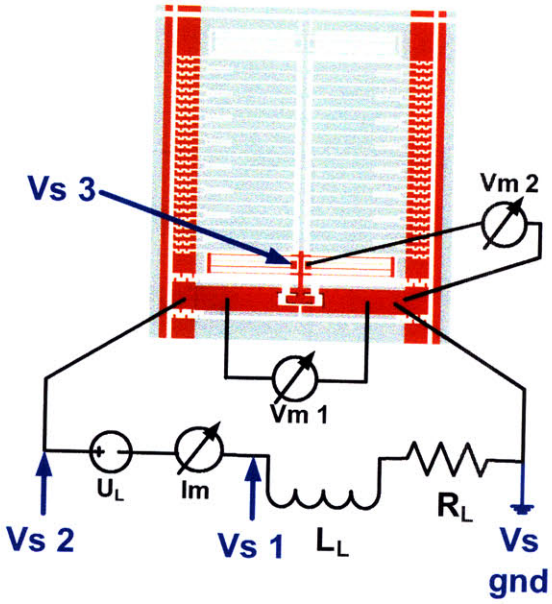


Figure 5-26: Test setup *MEMS relay 2.* A load impedance (R_L, L_L) is connected to the static contacts through a load source (U_L). Agilent 34401 multimeters measure: (1) the total voltage across the relay ($V_{m\ 1}$), (2) the partial voltage - across the moving contact and the right static contact ($V_{m\ 2}$), and (3) the current through the relay (I_m). An oscilloscope captures the transient response, probe locations are: $V_{s\ gnd}$, $V_{s\ 1}$, $V_{s\ 2}$, and $V_{s\ 3}$.

to fabrication inaccuracies, as the fabricated gap measures 17 μm on the wafer-top-side, and 13 μm on the wafer-bottom-side. The on-state resistance varies significantly between cycles at actuation voltages of 120-140 V. This indicates intermittent ohmic contact. At actuation voltages above 140 V, the on-state resistance is repeatable indicating a reliable ohmic contact is established when the relay closes.

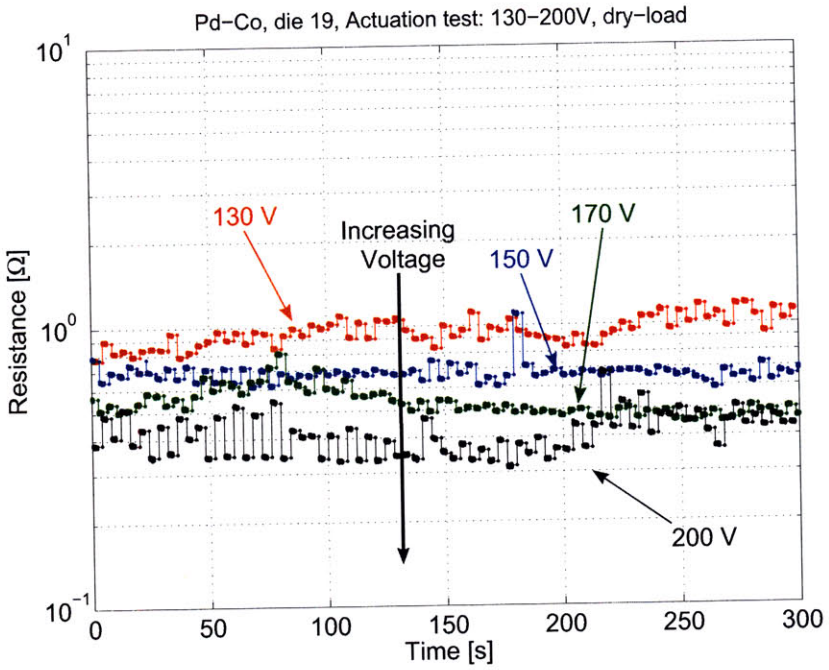
5.4.3.2 On-state resistance

The closed-state total contact resistance under dry-load conditions (I=20 mA), is in the order of 300 $m\Omega$. The lowest value observed is 130 $m\Omega$, while the a typical range is between 200 and 800 $m\Omega$, dependant on the contact metal and on the actuation voltage.

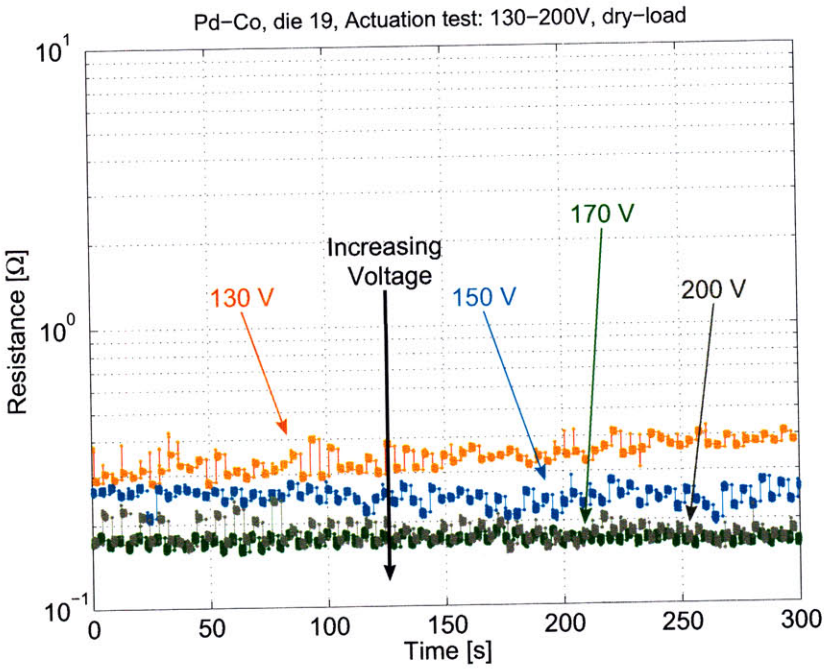
Figure 5-27 shows the total on-state resistance of a relay cycling at 250 mHz. Only the on-state resistance values have been plotted for clarity. The actuation voltage during this test ranges from 130 to 200 V. As expected, the on-state contact resistance is reduced as the actuation voltage is increased. However at 200 V, the relay exhibits charging, causing variation in the contact resistance. Figure 5-27 shows the on-state resistance values between each static contact and the moving contact for the same experiment. Notice that due to fabrication inaccuracies, mostly attributed to the electroplating process, the resistance is not shared equably among both static contacts. This indicates that the moving contact is not loading the two static contacts symmetrically.

5.4.3.3 Stand-off voltage

The theoretical isolation of *MEMS relay 2* is in excess of 1 kV. This is indicated by Paschen's law [71] for arcs forming across 70 μm wide gaps in air at atmospheric pressures, as shown in Figure 5-28 and in Section 3.6. Note that since this is a cross-bar relay, the effective gap is twice the contact travel. Experimental relays were tested up to 997 V continuously without breakdown. The voltage applied during these tests was limited by the test equipment. Higher voltages, exceeding 1 kV were measured during hot switching without signs of breakdown. Because the arcing event



(a)



(b)

Figure 5-27: On-state resistance *MEMS relay 2*, dry-load. (a) Total resistance. (b) Partial resistance: right-static-contact to moving-contact. The resistance is reduced the higher the actuation voltage with signs of charging at 200 V. The resistance of the left static contact dominates.

is probabilistic in nature, continuous application of a high voltage is more likely to cause break-down than a high voltage impulse, such as the transient inductive switching event.

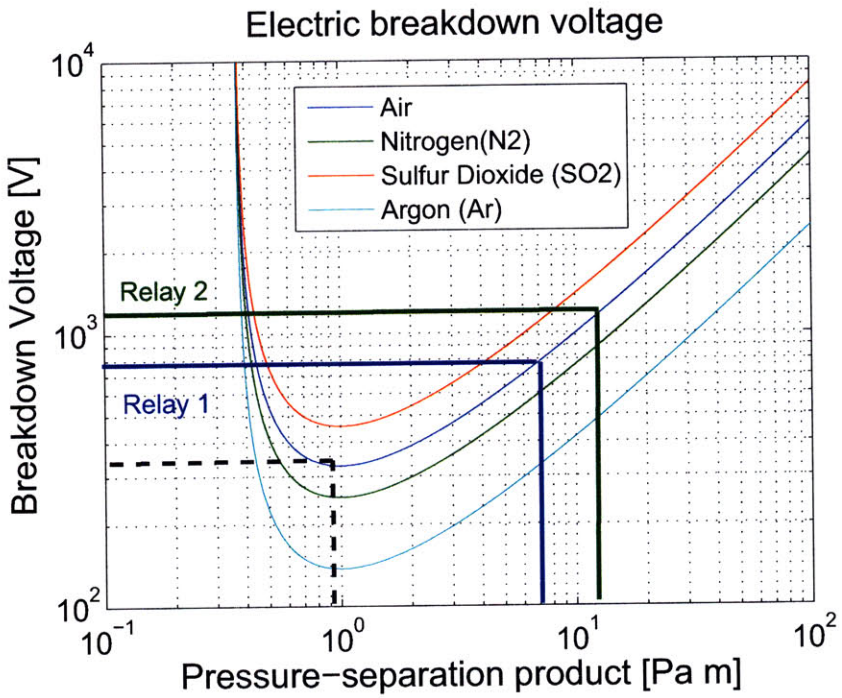
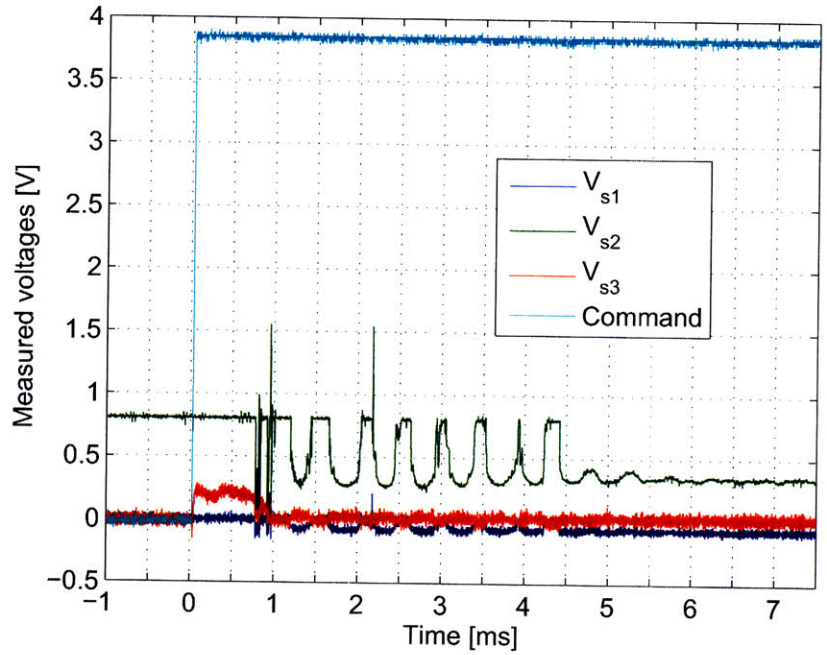


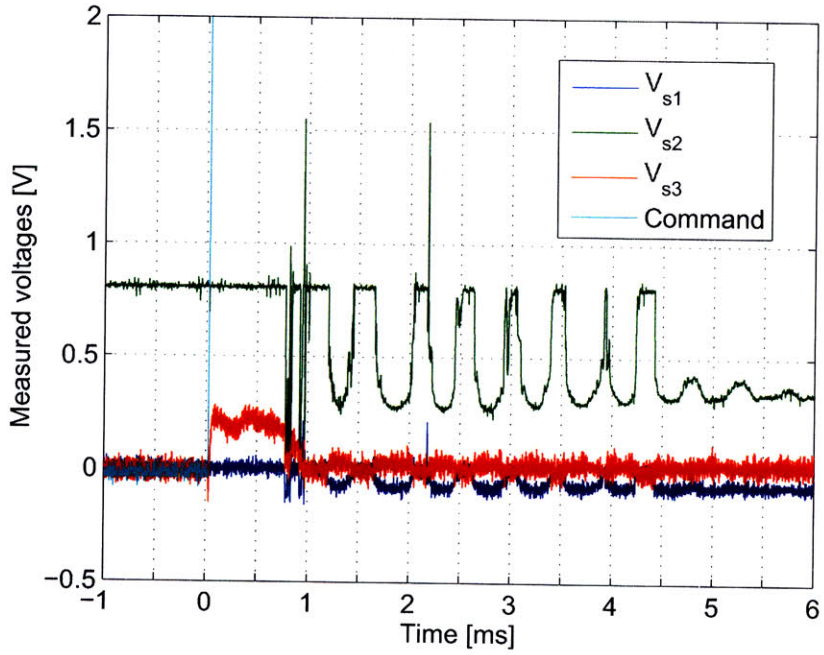
Figure 5-28: Electric breakdown voltage for various gases as a function of the gas-pressure – gap-length product, after [71]. Note that a gap length of about 70 μm is needed to withstand 1000 V while operating in air at 1 atm.

5.4.3.4 Dynamic response

The dynamic response of *MEMS relay 2* is shown in Figure 5-29. The relay exhibits a 750 μs delay between the command signal and contact closure. The relay closure is followed by contact bounce lasting approximately 3.5 ms. Notice that the signals V_{s2} and V_{s3} indicate the relay is bouncing and not "rocking" between the two static contacts. Contact bounce can be reduced through "peak and hold" actuation wave-forms and through "soft landing" wave forms [13]. These waveforms were not implemented.



(a)



(b)

Figure 5-29: Transient response *MEMS relay 2.* Voltages V_{s1}, V_{s2}, and V_{s3} are defined in Figure 5-26. (a) Complete plot, (b) detail, from Figure 5-29(a)

5.4.4 Hot-switching

During hot-switching tests, the relay is cycled continuously for at least 1200 cycles (typically for 300 s at 250 mHz). The contact resistance is continuously monitored to ensure no switching event is missed. Once the test is completed, the load voltage and the current limit are increased and a new test is performed. This sequence is repeated until the relay shows any signs of temporary contact sticking.

5.4.4.1 Pd-Co contacts (die 19)

Figure 5-30 and Table 5.6 show the load conditions used for each hot-switching test performed on the relays plated with Pd-Co. In all cases (sequence A, B, C, and D), the seized contacts separated through cycling after the load had been disconnected. In the case of palladium, the minimum arc voltage and arc current values are: 14 V and 800 mA, respectively [51].

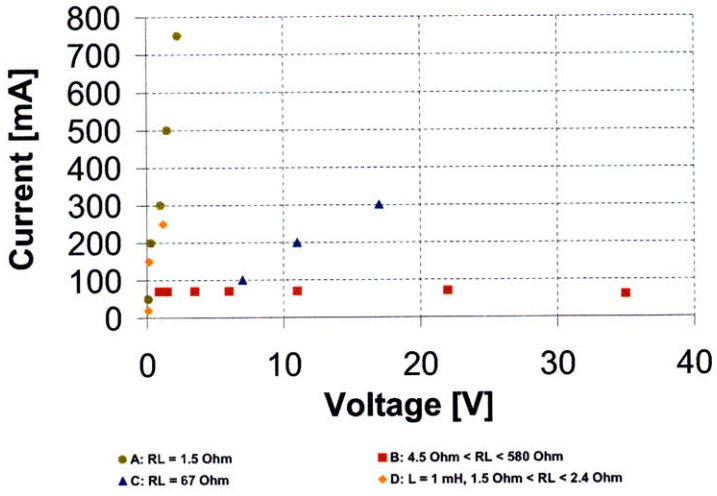


Figure 5-30: Load during hot-switching. *MEMS relay 2*, Pd-Co contacts (die 19). (A-C) Resistive loads, (D) resistive and inductive loads.

Sequence A - resistance at low load-voltages. Figures 5-31, and 5-32 show the results of the hot-switching sequence-A tests performed on *MEMS relay 2* with

Table 5.6: Load conditions during hot-switching tests *MEMS relay 2*, Pd-Co contacts (die 19)

Sequence	Load impedance R_L [Ω], L_L [mH]	Load current I_m, [mA]	Source voltage U_L, [V]	Failure criteria
A	1.5Ω	$50 - 800$	< 2.3	$I_L > 750\,mA$
B	$4.5 - 580\Omega$	< 100	$0.9 - 35$	$U_L > 35\,V$
C	$67\,\Omega$	< 350	< 17	$I_L > 350\,mA$
D	$1\,mH$	< 450	< 1.2	$I_L > 250\,mA$
	$1.5 - 2.4\Omega$			

Pd-Co contacts. Sequence-A is as defined in Figure 5-30. Notice the difference between the left-side contact resistance and the right-side contact resistance in Figure 5-32; the left-side contact resistance may be computed as the difference between the total and the right-side contact resistance values. This indicates asymmetric contact forces resulting in asymmetric contact resistance values. The test sequence is stopped at 800 mA at which point the contacts experience intermittent sticking.

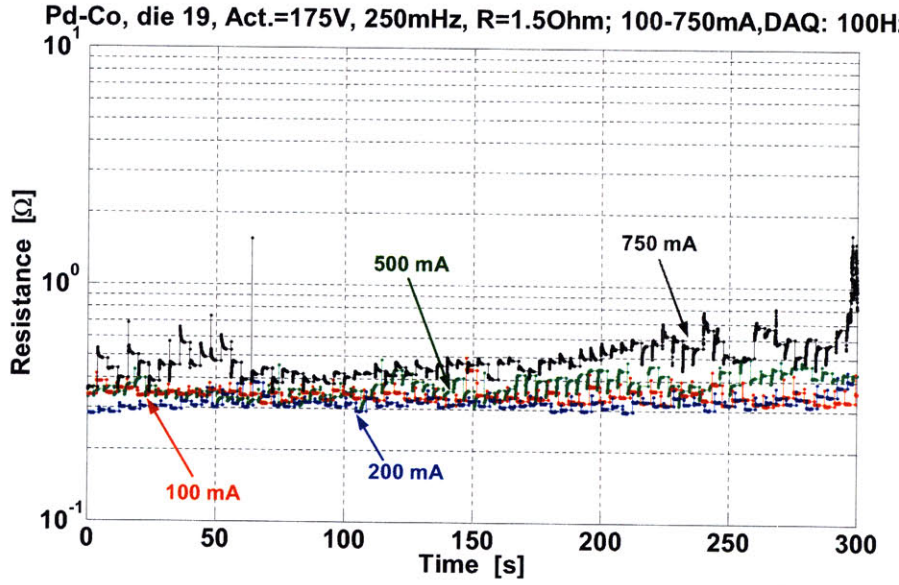


Figure 5-31: Total contact-resistance. Hot-switching, sequence A, *MEMS relay 2*, resistive load, Pd-Co contacts (die 19).

Sequence B - resistance at low load-currents. Figure 5-33 shows the results of the hot-switching series-B tests performed on *MEMS relay 2* with Pd-Co contacts.

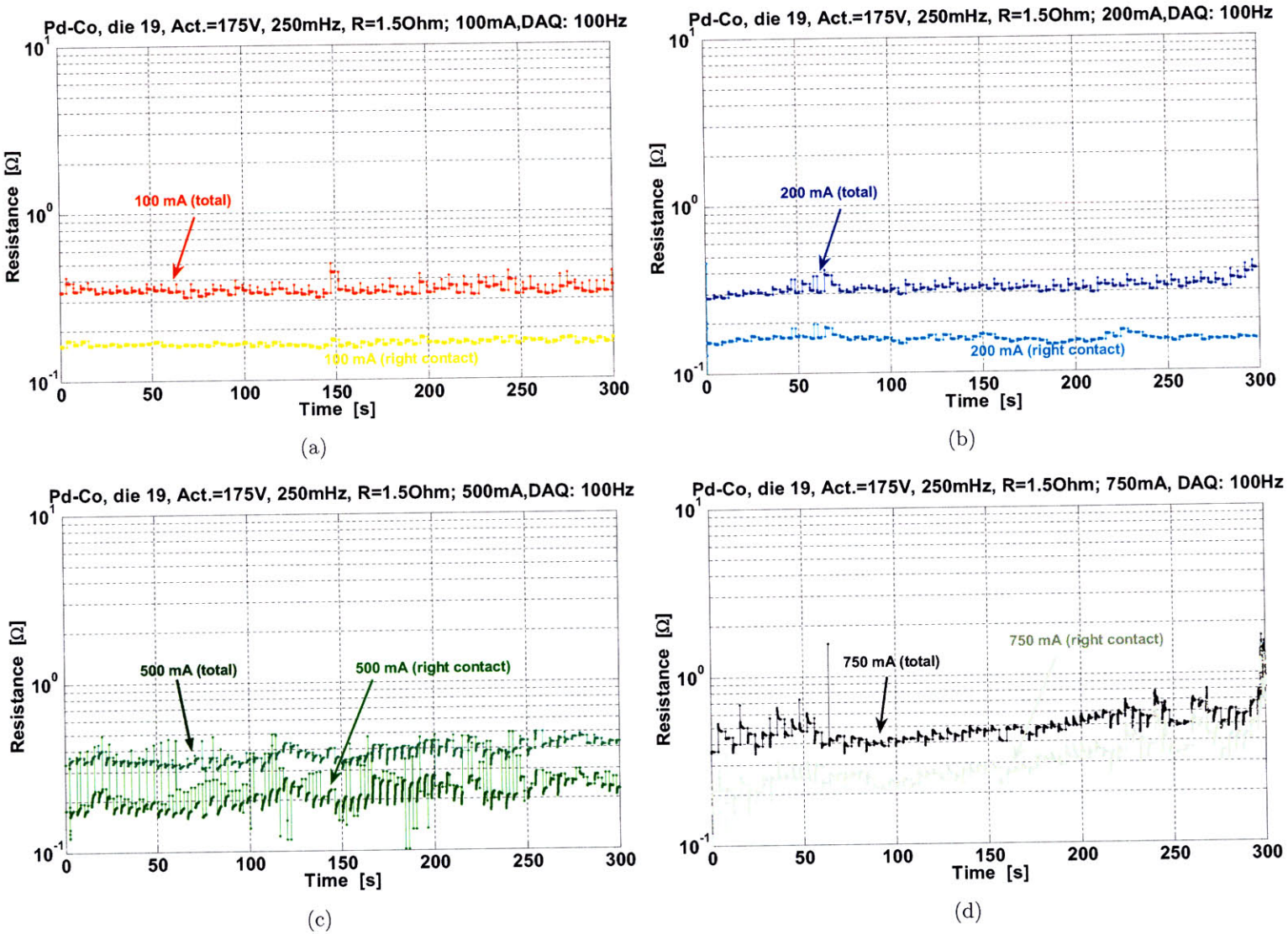


Figure 5-32: Total and right-side contact-resistance. Hot-switching of *MEMS relay 2*, Pd-Co contacts under different load currents - Sequence A (die19). (a) $I_L = 100\,mA$. (b) $I_L = 200\,mA$, (c) $I_L = 500\,mA$. (d) $I_L = 750\,mA$.

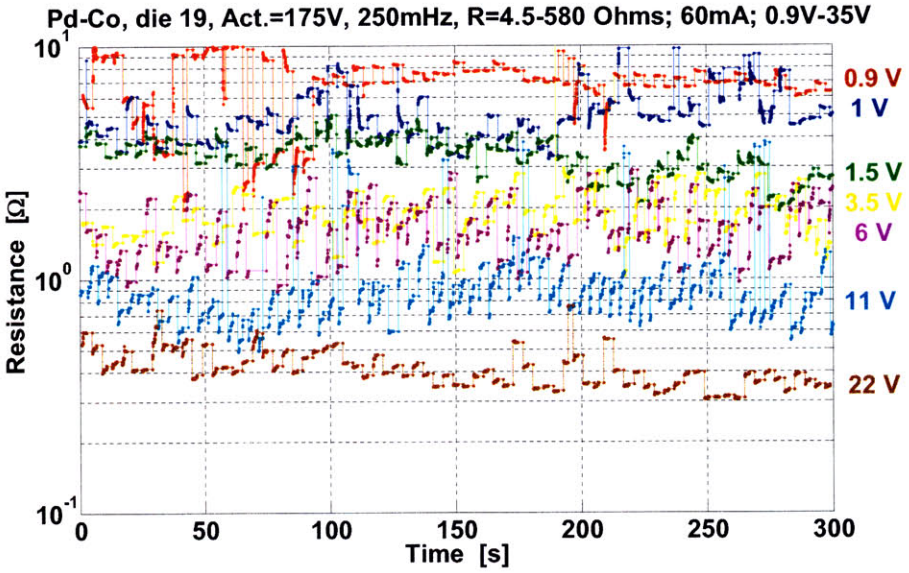
During these tests the load resistance was increased to keep the current below 100 mA with increasing load voltage. Notice that the resistance between the left static-contact and the moving-contact dominates. This performance asymmetry is caused by the protrusion defect as shown in Figure 5-36. The cobalt in the Pd-Co alloy was found to oxidize in a non-inert atmosphere at elevated temperatures. This was confirmed by an orange coloration of the metal surface, and by a poor adhesion during wire bonding. Notice also that the left-side contact resistance (total resistance minus right-side resistance) drops significantly as the voltage rises. The left-side contact has a pronounced protrusion as shown in Figure 5-36. The protrusion was formed during KOH etching using a straight isolation trench, as shown in Figure 5-11. After KOH etching, the protrusions were ablated with a LASER; the protrusion on the left-contact, however, was not fully removed.

It is hypothesized that the drop in resistance with increased voltage observed on the left-side contact may be attributed to a removal of dielectric material. This process of cycling the relay with a high supply-voltage and current-limiting at the 50 mA level is known as *self-cleaning* [19] or *Schaltreinigung*[20][47]. Switching at high voltages generates an arc which removes dielectric films from the contacts through evaporation and sputtering. In our case, it could also be that high current density during the previous hot-switching experiments (Series-A) caused localized thermal damage on the left-static-contact which was self-healed through localized metal softening during the application of high load-voltages.

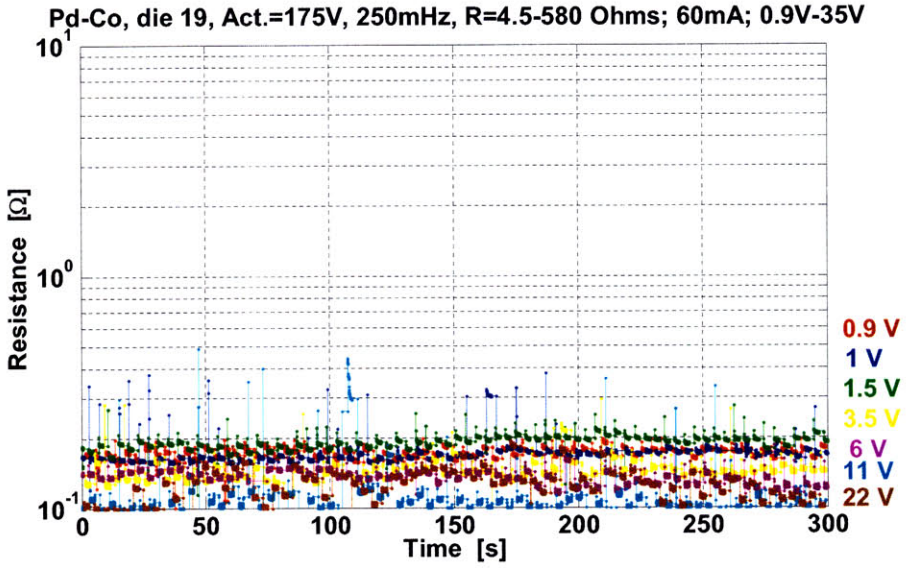
Sequence C - resistance at increasing load-currents and load-voltages. After having identified the maximum voltages and currents at which the contacts experienced sticking (Sequences A and B), the load is selected to increase both voltage and current, as shown in Figure 5-30. The contact-resistance remains stable up to a current of 300 mA after which the contacts again experience sticking.

Sequence D - Inductive load. The relay was cycled with a 1 mH inductor for increasing currents up to 350 mA, as sown in Figure 5-35. At currents up to 100 mA the contact resistance remained stable throughout the test, while at currents above

[20]The term Schaltreinigung means *cleaning through switching* in German



(a)



(b)

Figure 5-33: Hot-switching, *MEMS relay 2*, Sequence B, 0.9-35 V, Pd-Co contacts (die 19). (a) Total resistance. (b) Partial resistance: right-static-contact to moving-contact. The load-resistance is increased to keep the load current below 100 mA while increasing the load-voltage. Notice the drastic reduction in total resistance as the load-voltage is increased.

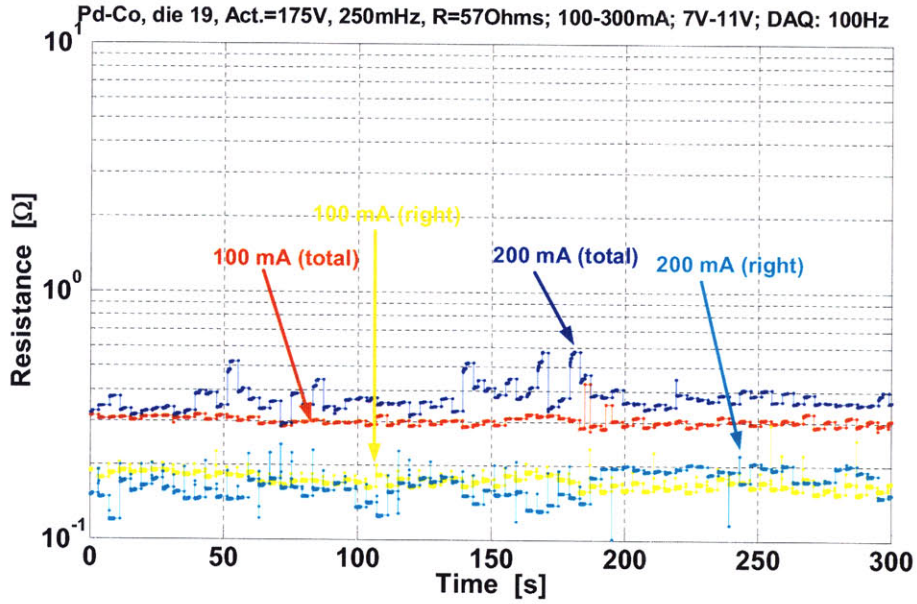
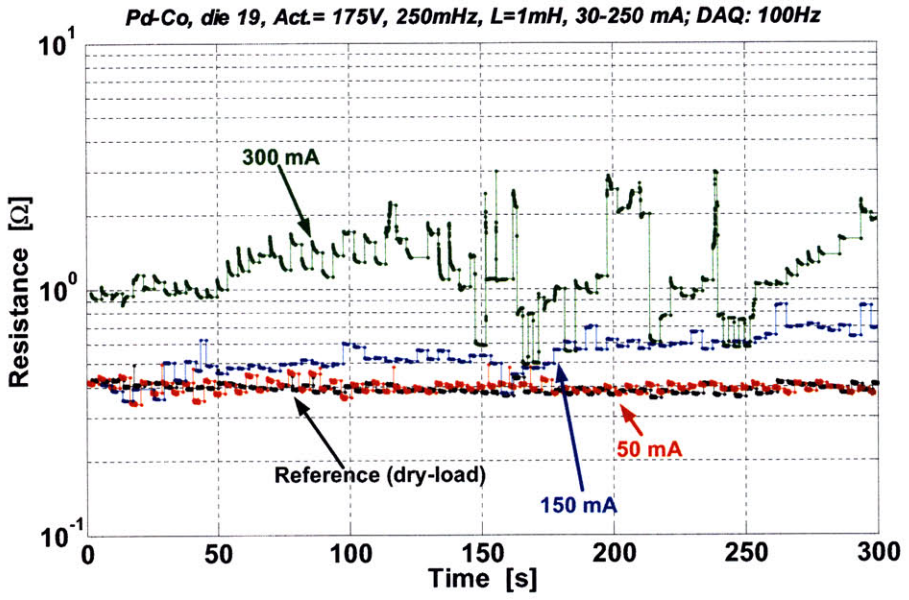


Figure 5-34: Total resistance, hot-switching, Sequence C.*MEMS relay 2*, Pd-Co contacts (die 19).

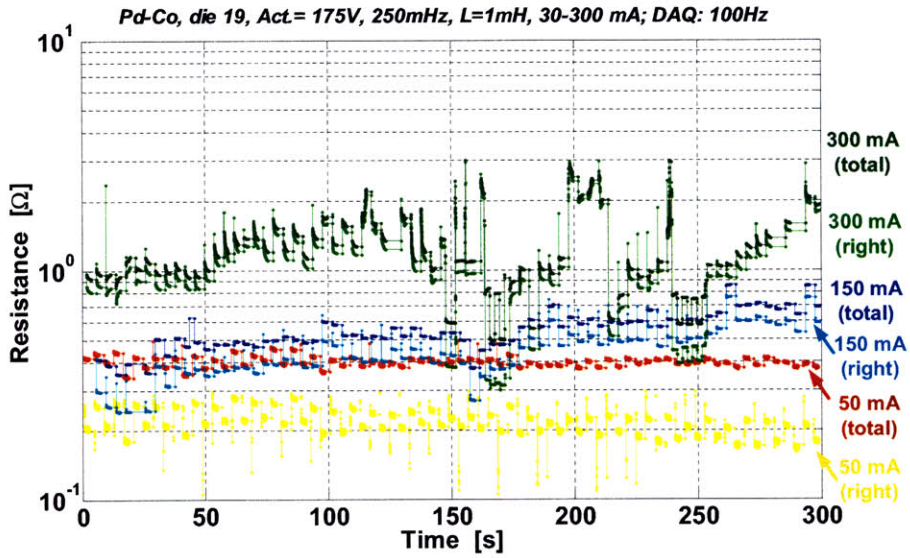
150 mA the contact-resistance increased over time. At currents above 350 mA the contacts started to exhibit sticking.

Metrology of contact surfaces before and after hot-switching, Pd-Co contacts. Figure 5-36 shows the contacts before and after hot-switching. This wafer was processed with a straight isolation trench, which formed triangular protrusions during KOH etching, as shown in Figure 5-11. These protrusions were removed with a LASER prior to metallization. However, part of the protrusion on the left static contact remained creating a noticeable defect after plating. It is hypothesized that the protrusion significantly reduced ohmic-contact area on the left static contact contributing to the disparity in contact-resistance between the left-side contact and the right-side contact. The surface of the protrusion on the left static contact changes after hot-switching while the rest of the left static contact, and the right static contact show no signs of wear or thermal damage. This indicates most damage occurred on one contact. The Palladium-Cobalt alloy used for die 19 of *MEMS relay 2* oxidized at high temperatures in the presence of oxidizing atmospheres.

The test-data indicates a device fabricated without the KOH-protrusion defects



(a)



(b)

Figure 5-35: Hot-switching, *MEMS relay 2*, Sequence D, 1 mH inductive load-impedance, Pd-Co contacts (die 19). (a) Total contact resistance. (b) Total and right {111}-contact resistance.

Table 5.7: Load conditions during hot-switching tests *MEMS relay 2*, Pd-Co/Pt contacts (die 34)

Sequence	Load impedance R_L [Ω], L_L [mH]	Load current I_m, [mA]	Supply voltage U_L, [V]
A	57 Ω	50 – 600	< 30
B	1.5 Ω	< 700	< 1
C	1.5 Ω	< 800	< 3

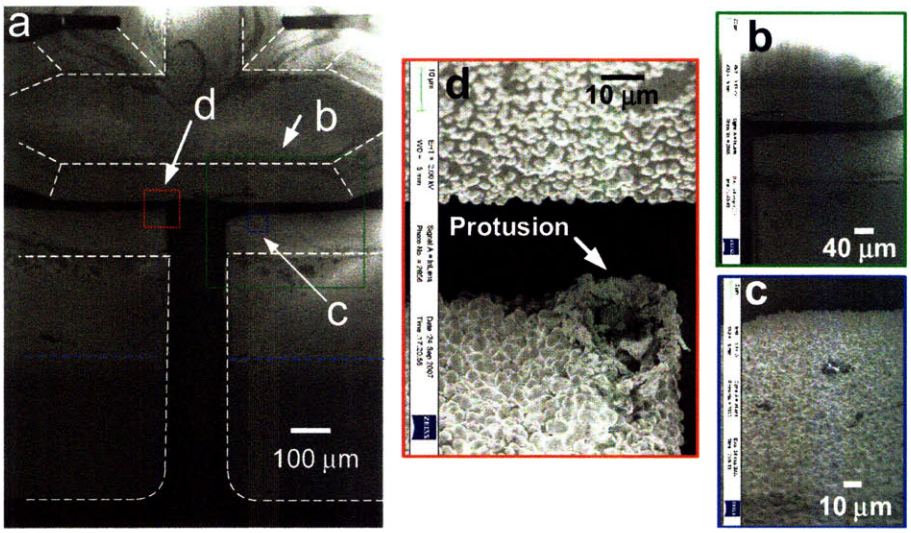
and without the cobalt should perform better than the device tested (die 19). The relays fabricated after die 19 employed the shaped trench geometry shown in Figure 5-12 to avoid the triangular protrusions created during KOH-etching.

5.4.5 Pd-Co and Pt contacts (die 34)

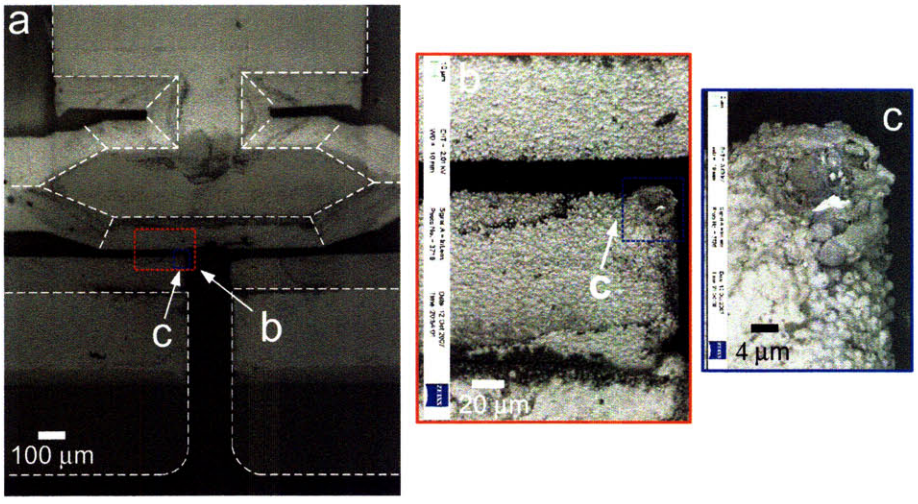
Traditional tribology theory states that adhesion can be reduced when dissimilar materials are used for contacting. To test a different material combination, Pt was evaporated through a shadow wafer on the top surface of a die with electroplated Pd-Co contacts. Platinum was only deposited on the wafer-top-side after bonding, which covered the static {111} contact. The moving {111} contact remained with the Pd-Co alloy electroplated originally. Figure 5-37 and Table 5.7 show the load conditions used for each hot-switching test performed on the relays plated with Pd-Co/Pt. For all sequences (A, B, and C) the "seized" contacts separated through cycling after the load had been disconnected. This contact material combination showed a slight improvement over the Pd-Co contacts, reaching 800 mA as the maximum hot-switched current at low supply voltages, and 500 mA at increasing supply-voltage and supply-current. The initial contact resistance for the Pd-Co/Pt relay contacts is 1 Ω, a higher value than that of Pd-Co contacts (die 19).

5.4.6 Rh contacts (die 04)

Figure 5-38 shows the load conditions used for the hot-switching test performed on the relay plated with Rh. Contact resistance is maintained stable up to currents



(a)



(b)

Figure 5-36: Pd-Co contacts *MEMS relay 2* (a) Contacts prior to hot-switching. Notice the protrusion the left static contact; (b) Contacts after hot-switching.

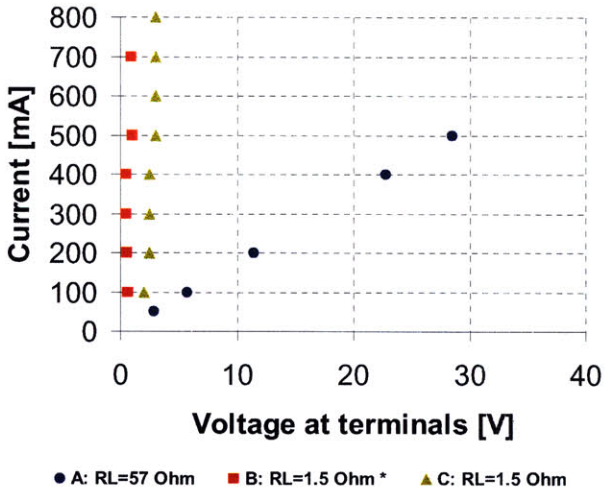


Figure 5-37: Load during hot-switching. *MEMS relay 2*, Pd-Co/Pt contacts (die 34). (A) 57 Ω resistive load, (B) 1.5 Ω resistive load, (C) 1.5 Ω resistive load. During run B, the driver applied half the actuation voltage during the off-state

above 1 A, at which the contacts experienced sporadic sticking. As was the case with the previous hot switching tests, the seized contacts separated through cycling after the load had been disconnected. This contact material combination showed better performance over the previous metals, reaching 900 mA as the maximum hot switched current. The contact-resistance for the Rh contacts is $1.1, \Omega$. This value is higher than that of the relay with Pd-Co contacts, which is expected due to the higher resistivity and hardness. Figures 5-39 and 5-40 show the contacts before cycling. Notice that the grain size is much smaller than that of Pd-Co. This is attributed to the use of Ni-Co as a buffer material vs. Cu which was used as a buffer material for the Pd-Co (die 19) and Pd-Co + Pt (die 34) die.

5.4.7 Discussion, tests *MEMS relay 2*

In order to compare the experimental data to the models, the actuation force must be known. Since the contact force could not be determined experimentally, it was obtained from (5.3) using the fabricated dimensions measured with the SEM ($h = 17.5\mu m$). On the zipper actuators, the output force F_{zipper} is related to the travel d, and the maximum travel Δ by $F_{zipper} \sim (\Delta - d)^{-1/2}$. Process tolerances and plating

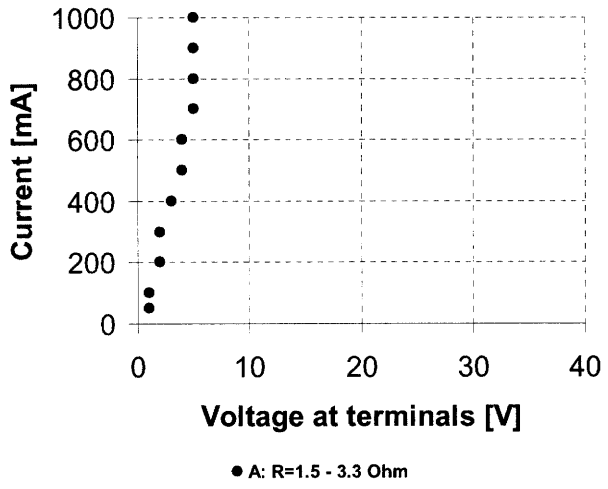


Figure 5-38: Load during hot-switching. *MEMS relay 2*, Rh contacts, die 04.

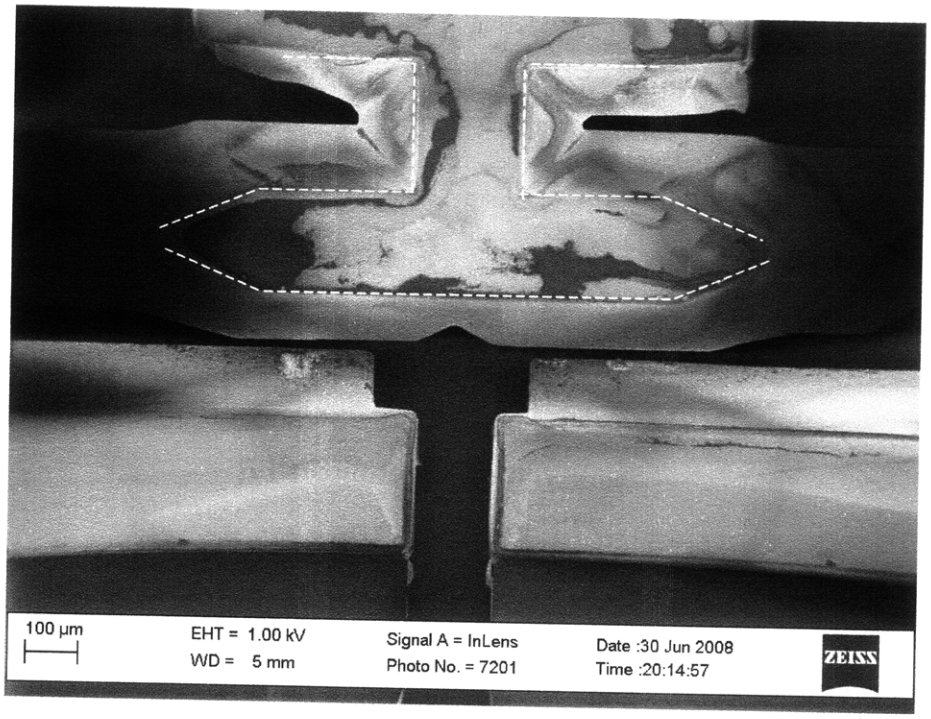
thickness variations led to significant variations in contact travel between fabricated wafers which affect the contact force. The maximum displacement Δ of each die was determined using markers on the moving contact after the relay had closed electrically.

The total contact force however is not distributed equally among both contacts, as seen from the difference in contact resistance between the left-side and right-side contacts. The proportion of the total force, or force fraction, distributed to each contact was determined from the difference in resistance by the following relation

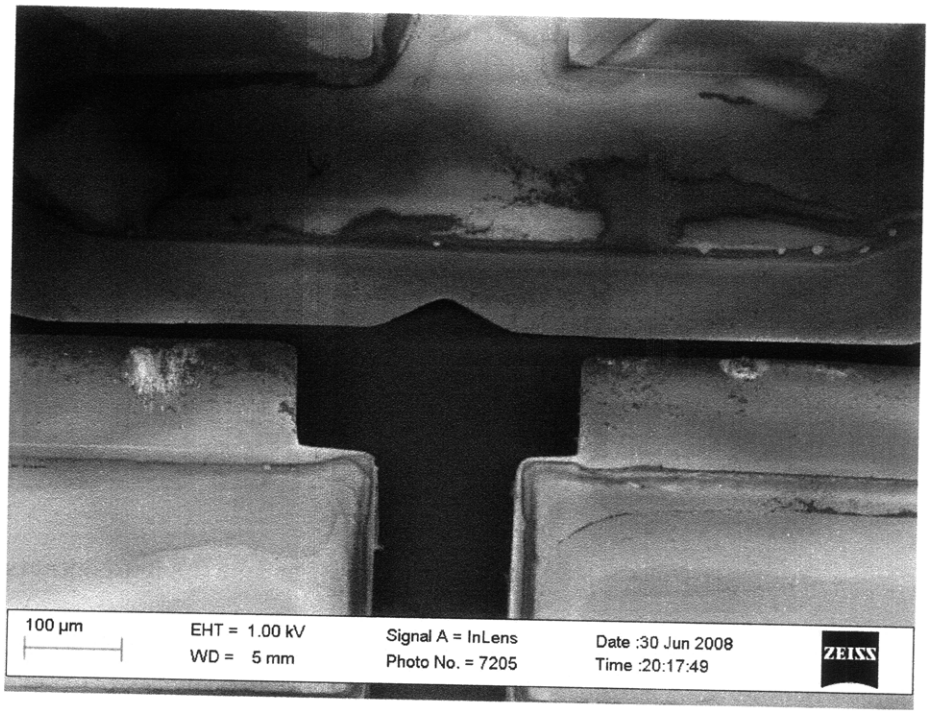
$$\begin{aligned} f_R &= \frac{1/R_{c-R}^2}{1/R_{c-R}^2+1/R_{c-L}^2} \\ f_L &= \frac{1/R_{c-L}^2}{1/R_{c-R}^2+1/R_{c-L}^2} \end{aligned} \tag{5.4}$$

where f_{frac-R}, f_{frac-L} are the force fractions for the right and the left contacts respectively, R_{c-R} and R_{c-L} are the right-contact and left-contact resistances respectively. The rationale behind (5.4) is that the force is proportional to the area through (3.19), and that the area is inversely proportional to the resistance squared through (3.7). The total contact force on each side contact is

$$F_{R-total} = F_{zipper} \cdot n \cdot f_R \cdot C1 \cdot C2 \cdot k_{flexure} \cdot d$$

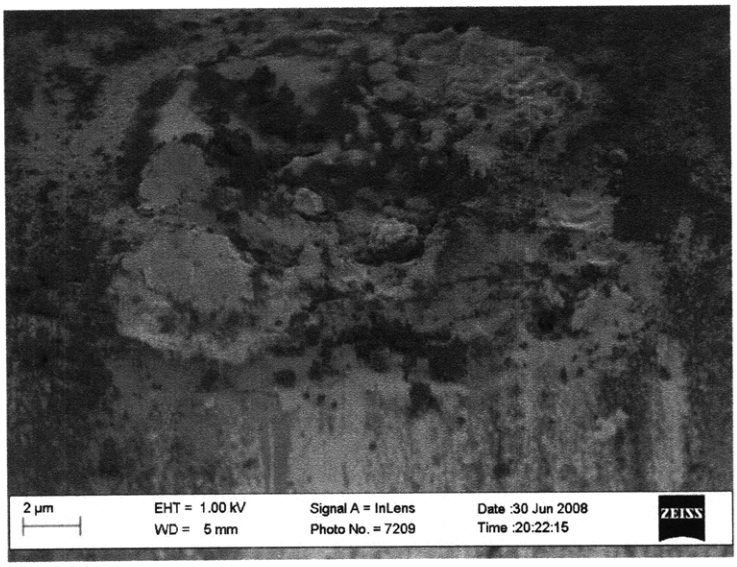


(a)

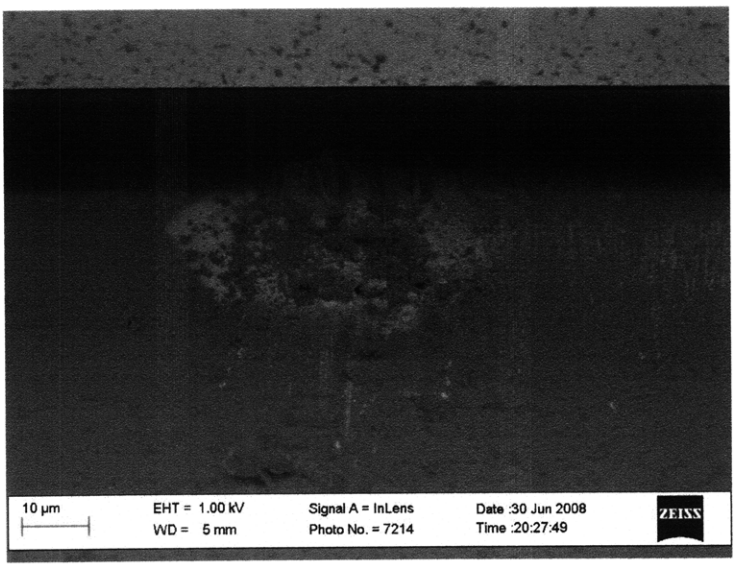


(b)

Figure 5-39: Relay contacts before hot-switching tests, *MEMS relay 2*, Rh (die 04). (a) Contacts after hot-switching. (b) Detailed view of the contacts.



(a)



(b)

Figure 5-40: Relay contacts before hot-switching tests, *MEMS relay 2*, Rh (die 04). (a) Detail damage left-side contact. (b) Detail damage right side contact.

$$F_{L-total} = F_{zipper} \cdot n \cdot f_L \cdot C1 \cdot C2 \cdot k_{flexure} \cdot d \tag{5.5}$$

where F_{zipper} is the zipper force, n is the number of actuator pairs (8 for a fully functional device, less if any actuators are damaged), $C1 = 0.5$ is a correction factor to account for deviations between experiment and numerical modeling [33], $C2 = 0.5$ is a correction factor to account for area lost due to porosity caused by inadvertent KOH-etching through oxide pin holes, $k_{flexure}$ is the total flexure stiffness from Table 5.2, and d is the contact travel.

Figure 5-41 shows the experimental and the modeled contact resistance for the different relays. The experimental relationship between contact force and contact resistance shows the same slope as given by the plastic model. However, there is a multiplicative increase in resistance (10-100) which is attributed to reduction of ohmic-contact area as a consequence of dielectric films i.e. oxidation, adsorbed hydrocarbons, etc.

Based on the models in Section 3.3, the ohmic-conduction area and the mechanical load-bearing area of the right and left-side contacts can be calculated from the measured contact resistance and the calculated contact force. The ohmic-conduction area is determined from (3.7), and the mechanical load bearing area is computed under the assumption of plastic mechanics form (3.19). A comparison of the two areas is shown in Figure 5-42. It is important to note that the ohmic-conduction area is consistently between 1% and 10% of the load bearing area, further suggesting that non conducting films i.e. oxides cover the majority of the load bearing contact area. These films contribute to the increased contact resistance above the ideal models observed in Figure 5-41.

Table 5.11 summarizes the test results for *MEMS relay 2*. Figure 5-43 compares the experiential stand-off voltage and on-state current of *MEMS relay 2* to data published by other researchers, as described in Chapter 2. Notice that many of the previously published relays exhibit a maximum voltage-standoff of 325 V. This voltage matches the minimum breakdown-voltage of air at 1 atmosphere, as described by Paschen's law (Fig 5-28). Most relays falling in this category have an out-of-

Relay	Contact Material	Actuator Voltage [V]	Contact Side	Nominal Resistance [Ω]	Contact Resistivity [μΩ-cm]	Area [(μm)²]
Die 04	Rh	190	Right	0.450	4.93	0.0093
			Left	0.550		0.0062
Die 19	Pd-Co	130	Right	0.350	25	0.4007
		130	Left	0.650		0.1162
		150	Right	0.250		0.7854
		150	Left	0.450		0.2424
		170	Right	0.175		1.6029
		170	Left	0.325		0.4647
		200	Right	0.175		1.6029
		200	Left	0.225		0.9696
Die 34	Pd-Co & Pt	200	Right	0.300	17.8	0.2765
			Left	7.700		0.0004

Table 5.8: Data used to compute the electrical a-spot contact area. Note that the resistivity used for Die 34 is an average of Pd-Co and Pt.

plane contact motion, as indicated in Chapter 2, or travel on the order of 10μm. Relays with lower breakdown-voltage (i.e. 200 V) probably experience breakdown of dielectric thin-films and not breakdown at the contacts, as was the case in *MEMS relay 1*. Only the relay presented here and JPL's magnetostatic switch [69] exhibit a breakdown-voltage of 1000 V.

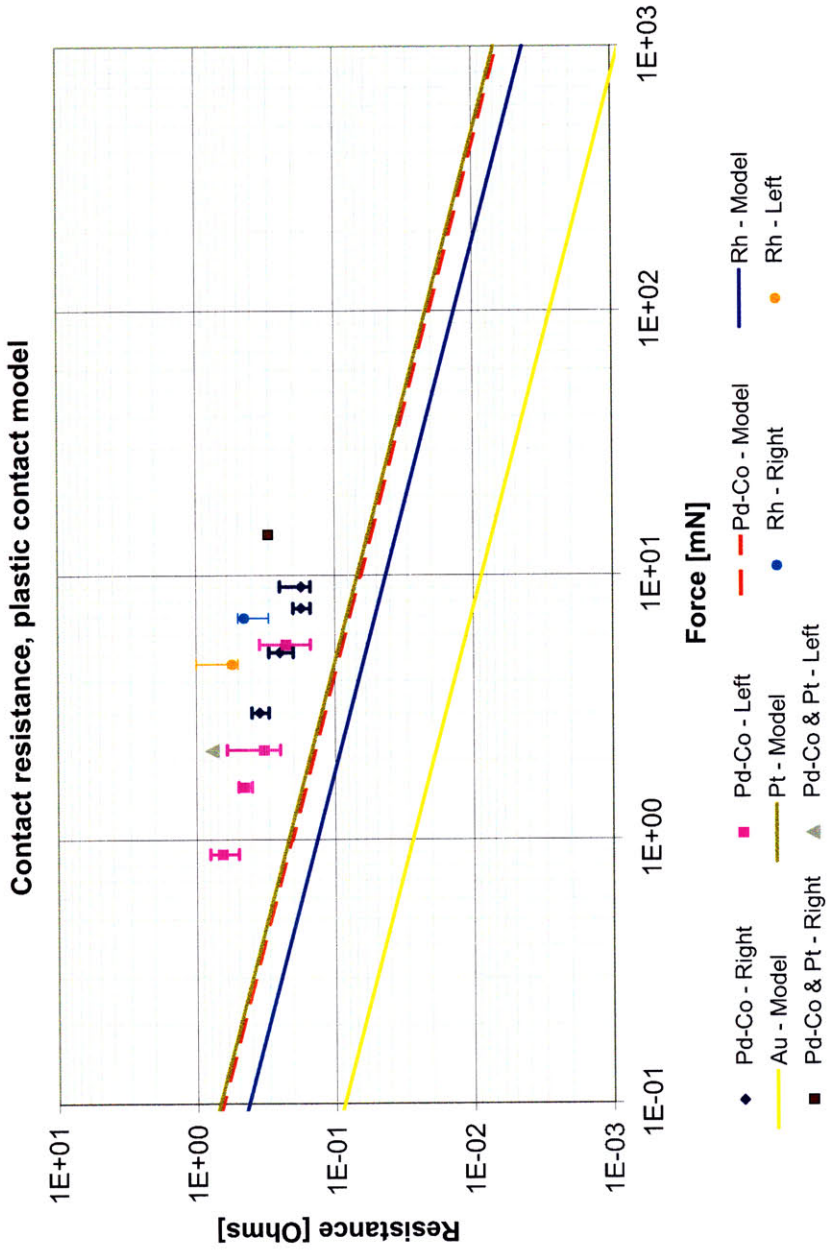


Figure 5-41: Experimental and modeled contact resistance for the different relays. Notice the experimental data shows the same slope as given by the plastic model. The multiplicative increase in resistance (10-100) is attributed to a reduction of ohmic-contact area as a consequence of dielectric films.

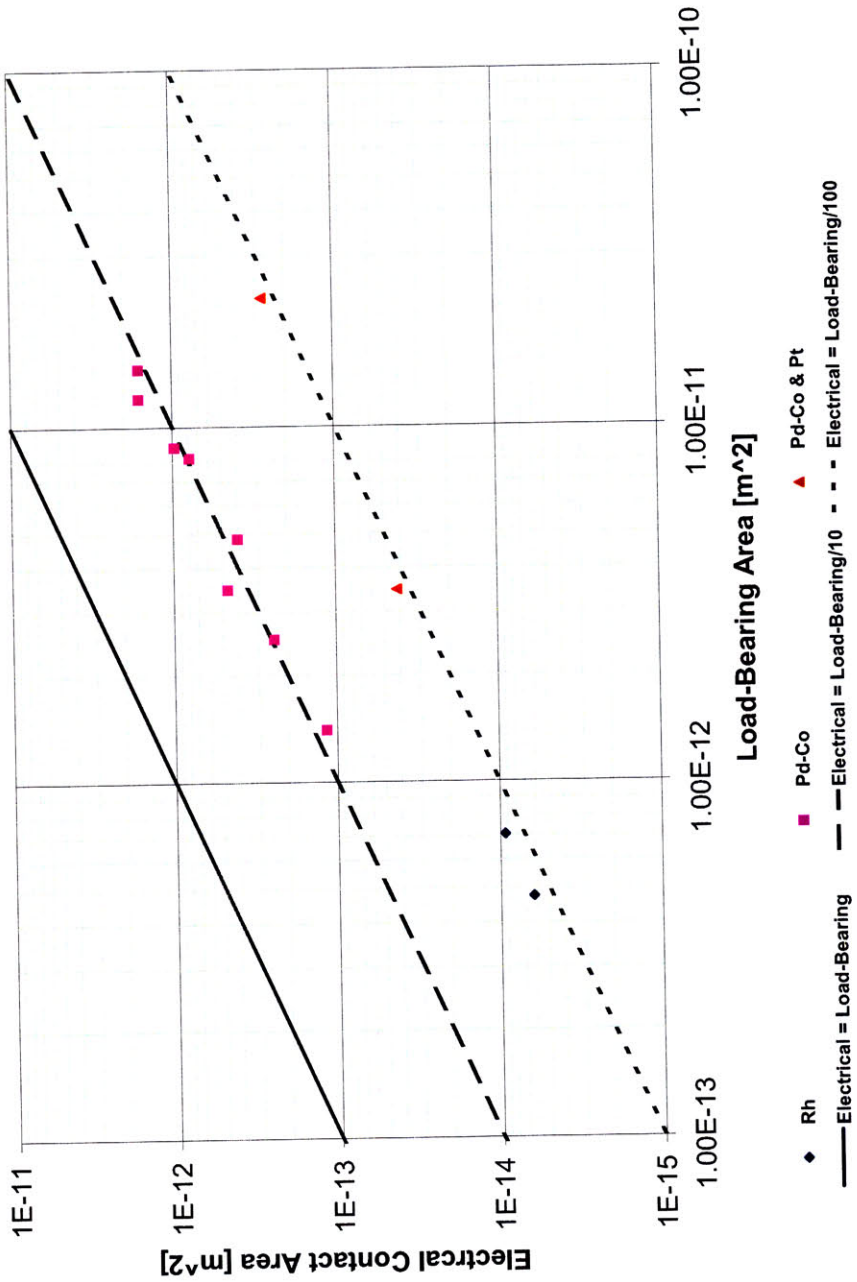


Figure 5-42: Ohmic-conduction area and mechanical load-bearing area comparison for the right and left-side contacts. The ohmic-conduction area is determined from (3.7), and the mechanical load bearing area is computed under the assumption of plastic mechanics form (3.19).

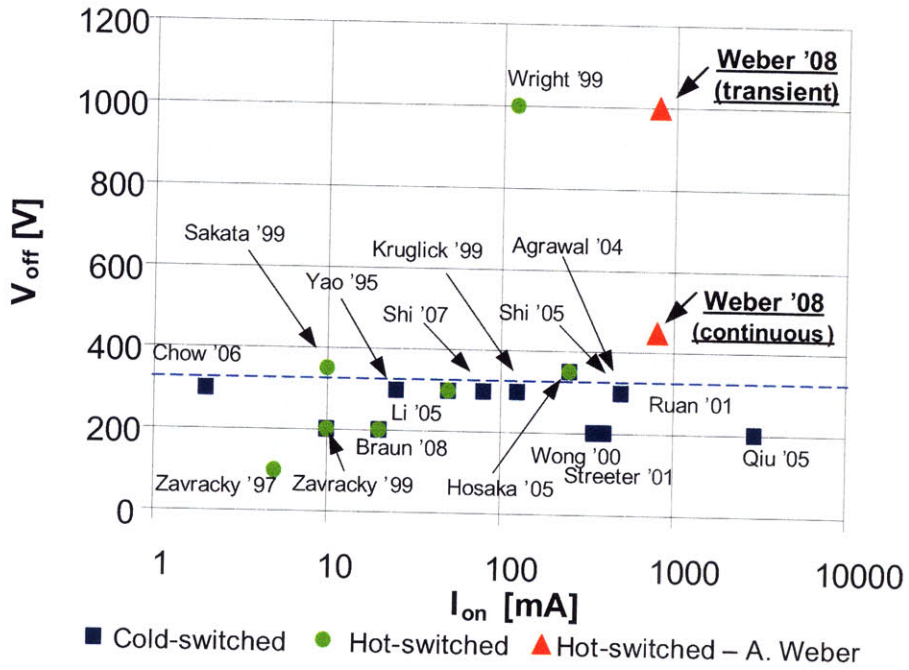


Figure 5-43: Voltage-standoff and current-carrying-capacity comparison of *MEMS relay 2* to previously published MEMS relays. Notice that many of the previously published relays exhibit a maximum voltage-standoff of 325 V, the minimum on the Paschen curve in air, as indicated in Fig 5-28.

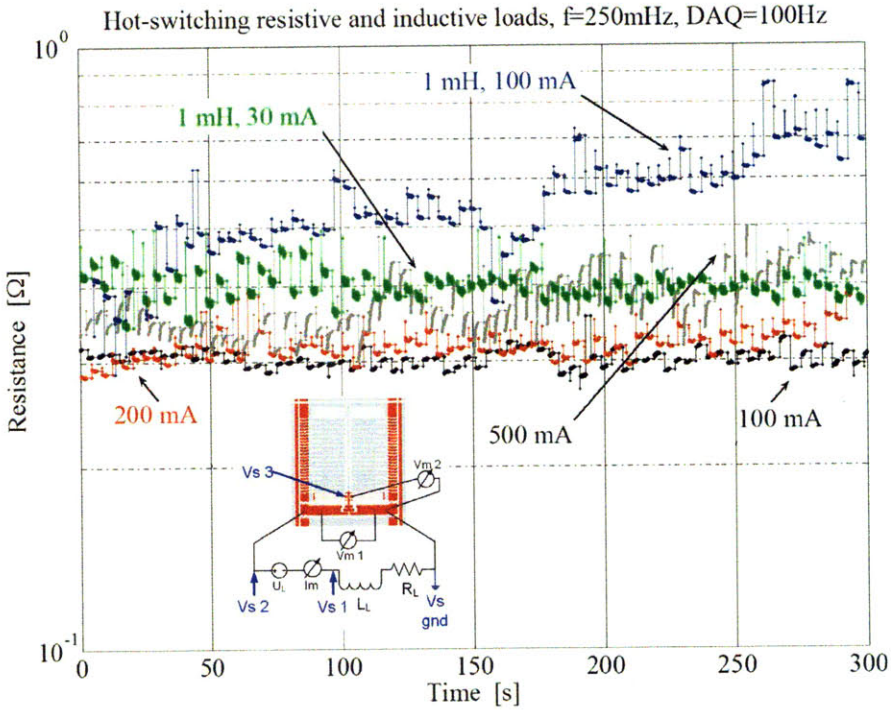


Figure 5-44: Total hot-switched contact resistance *MEMS relay 2*. Notice the various resistive and inductive loads.

Relay	Contact Material	Actuator Voltage [V]	Number Of Zippers	Max Contact Travel Δ [μm]	Contact Travel d [μm]	Total Force [mN]	R-Side Force [mN]	L-Side Force [mN]
Die 04	Rh	190	14	78	37.1	11.52	6.90	4.62
Die 19	Pd-Co	130	15	78	49.8	3.90	3.02	0.88
		150				6.69	5.11	1.58
		170				9.69	7.51	2.18
		200				14.54	9.06	5.48
Die 34	Pd-Co & Pt	200	15	78	35.0	16.44	14.27	2.17

Table 5.9: Data used to compute the force on both sides of the contacts after subtraction of the flexure force; the flexure spring constant is $k_{flexure} = 224\,\mu N/\mu m$ from Table 5.2, and the travel is d. Note that the net contact force is distributed between the right-hand and left-hand contacts in proportion to the inverse square of the corresponding resistances shown in Table 5.8.

Relay	Contact Material	Actuator Voltage [V]	Contact Side	Nominal Force [mN]	Contact Hardness [MPa]	Area [$(\mu m)^2$]
Die 04	Rh	190	Right	6.90	9750	0.708
			Left	4.62		0.474
Die 19	Pd-Co	130	Right	3.02	625	4.834
		130	Left	0.88		1.402
		150	Right	5.11		8.181
		150	Left	1.58		2.525
		170	Right	7.51		12.021
		170	Left	2.18		3.485
		200	Right	9.06		14.503
		200	Left	5.48		8.773
Die 34	Pd-Co & Pt		Right	14.27	625	22.834
		200	Left	2.17		3.466

Table 5.10: Data used to compute the mechanical load-bearing contact area. Note that the hardness used for Die 34 is that of Pd-Co, which is assumed to be softer than Pt. Further, the contact force is taken from Table 5.9.

Table 5.11: Test summary *MEMS relay 2*.

Parameter	Units	Functional requirement	Measured value	Observation
Isolation V_{off}	V	600	440 (continuous) 1000 (transient)	test equipment limited during hot-switching
Current I_{on}	A	$1-10$	0.9	Resistive load, hot-switched
	A	-	0.35 at 1	Inductive load, hot-switched
Travel	μm	70	70	-
Actuation	μJ	10	10	-
Response time	μs	-	750	-
Life time	-	-	$5 \cdot 10^6$	Pd-Co contact

Chapter 6

Summary and conclusions

6.1 Contributions of this thesis

This thesis explored power handling by a MEMS device in the context of a relay. To this end, design concepts, analytical performance models, fabrication processes and design rules were developed. Two designs of MEMS-relays were fabricated and tested. The relays were hot-switching with inductive and resistive loads while monitoring the contact resistance. The major contributions of this thesis are as follows.

- A thorough literature review of published work on MEMS relays, and light duty macro-scale relays, contact physics, contact materials, and on crystalline orientation dependant etching (Chapter 2, Section 3.2.1, and Figure 5-43).
- A study of the fundamental limits of power handling by a MEMS relay was presented based on mechanical, electrical and thermal analyses:
  - Solid mechanics models based on elastic and plastic deformation were used to determine the mechanical load-bearing contact area (Section 3.4.2).
  - Electrical and thermal models were used to determine the electrical contact resistance and the temperature at the constriction (Section 3.4.1, 3.5). The temperature at the constriction limits the current carrying capacity of the relay (Section 3.5).

- New designs for {111} contacts, MEMS relays, and their fabrication processes were developed.

  - Three different MEMS relays with {111} contacts are described in Chapters 4, 5, and 7, respectively. The description includes analysis, design, fabrication and testing.

  - A study of the sensitivity of the {111}-plane contact geometry during fabrication including mask misalignment, misalignment to the substrate's crystalline plane, substrate tolerances, and process inherent tolerances, i.e. during etching, is presented in Section 3.2.2.

  - Fabrication processes for the {111} contacts and relays are developed in Sections 4.2 and 5.3. A "nested mask" process is used to achieve perfect corners during KOH etching, along with vertical sidewall convex corner compensation, and local oxidation of silicon (LOCOS).

  - A relay packaging concept is developed to reliably handle currents on the order of 10 A and to simultaneously control 16 actuators.

  - A testing setup and protocol which allows continuous monitoring of the contact resistance is described in Section 5.4.2.

6.2 Conclusions and future work

This section offers a variety of conclusions concerning the modeling, design, fabrication, and testing of the MEMS relays. It also concludes with several suggestions for future work, the most important of which address contact force and hence contact resistance.

Observations on analytical techniques and fundamental limits

- The maximum current carrying capacity of the relay is limited by the softening and melting of the contact a-spots; see Sections 3.5, 4.3, and 5.4.4. Thermal management of the die has limited effect as the heating is highly localized at

the a-spots. In order to increase the current carrying capacity, the contact resistance must be lowered. This can be done by increasing the contact force. Alternatively, the ohmic-contact area can be increased by introducing multiple, elastically supported contacts [54]. In the limit, these structures may resemble the geometry of gecko feet. Another strategy to reduce the contact resistance is to use a more conformal metallization process in order to preserve the complementary {111} silicon geometry. For example, sputtering of metals yields a finer grain than evaporation and is deposited more uniformly. Deposition of these films through atomic layer deposition, i.e. diamond-like-carbon would have preserved the underlying geometry. Alternatively, the uniformity in electrodeposition can be increased through optimum use of brighteners and process optimization.

The relays described here carried currents up to 0.8 A before contact sticking was observed. Forces near 10 mN were required; see Figure 5-41. In order to carry currents up to 10 A it is estimated that a 100-fold reduction in contact resistance for the same power dissipation, requiring a 100-fold increase in contact force.

- The multi-physics models predict the temperature rise at the a-spots, and set a limit on the relay's current carrying capacity. The values obtained in the model are in agreement with models used in the design of macro-scale relays and contacts. The current limits are also in agreement with experiments presented here. The relays presented here have a carrying capacity of about 1 A; see Section 5.4.6.

- The analysis and experiments confirm that equations governing macro-scale contact design are applicable for the MEMS-relays described. Although more elaborate models exist for micro-scale contacts, the conventional macro-scale models provide a good estimate of the performance.

- Hertz contact theory and plastic deformation models can be used to estimate the performance of the design. However, MEMS relays are more susceptible

to resistance caused by dielectric films. This is because MEMS relays operate at actuation forces at least 1-2 orders of magnitude smaller than conventional relays, and large contact forces are required to break through dielectric films; see Sections 3.4.4 and 5.4. It has been routinely observed that the electrical ohmic-contact area is only 1-10% of the mechanical load-bearing contact area presumably because of these films; see Figure5-42.

Observations on the design

- This thesis initially postulates the hypothesis that KOH etched {111} contacts could yield atomically smooth and parallel surfaces, which might provide low contact resistance through an increased effective contact area. While KOH etching yields parallel surfaces as it etches along the substrate crystalline planes, the etched surfaces are not "atomically" smooth due to oxygen precipitation, etch defects, etc. The roughness is further exacerbated when the metal films are electroplated onto the contacts.

- Few references exist on the smoothness of {111} planes as most publications report on the smoothness of 100 surfaces after KOH etching. This may be due to the fact that {111} are oblique and therefore more difficult to characterize, or perhaps because for most applications the quality of the {111} surfaces are not of particular importance.

Fundamental limits and modeling

- The maximum current carrying capacity is set by softening and melting at the a-spots. In order to increase the current carrying capacity more force is needed. Alternatively, the current carrying capacity may be increased through a compliant design which uses multiple contacts as a means to increase the contact area (wiffle-tree).

- The thermal and mechanical models were validated through experiments, however it was necessary to estimate the contact force in the process.

MEMS relay design and {111} Si etched surfaces as electrical contacts

- The contacts are not atomically flat due to oxygen precipitates, defects, etc. Rather, they are parallel but with significant roughness on the nm scale.
- The effective contact area is not increased with {111} plane contacts due to the roughness of the evaporated and the electroplated metal films.
- Film stresses (i.e. delamination of plated materials) and fabrication inaccuracies lead to uneven loads being applied to the two sides of the contacts; see Chapter 5. Torsional compliance of the cross bar is required to balance the contact forces.
- The oblique geometry of the {111}-contacts significantly improves the electrical conductivity between {100} and {111} planes.
- Metal softening and mechanical contact degradation are observed in Figures 5-36, 5-39, 5-40, but a corresponding electrical degradation was not observed.
- Palladium-Cobalt oxidizes readily in a non-inert atmosphere, and so it was a poor contact material. Its performance could be improved by cleaning with diluted sulfuric acid, but the improvement was short lived. Rhodium performed much better. No cold-welding was observed since the contact resistance did not drop when the relay contacts experienced "sticking".
- Use of any material other than Au in a non-inert environment will eventually degrade due to oxide formation. A vacuum package or an inert atmosphere may increase the reliability.
- One of the reasons that the contact force does not reach the design goal of 40 mN, is that the contact travel was not large enough as fabricated. This was mostly due to a poor control of the electroplating process.
- Given the fabrication inaccuracies, the load is not equally distributed on the left and right side contacts, and the maximum contact resistance increases on one

side. This becomes a bottleneck to performance. A potential solution would be to have a single gap, and bring the current in through a wire bonded to the flexure anchors, or through the silicon substrate to avoid wirebonding for the electroplating step.

Fabrication observations

- KOH-etching is hard to control for the tolerances required by the relay; see the tolerance analysis in Section 3.2.2. For the relay application, the resultant dimensions of KOH etching is hard to predict because of misalignment and oxygen precipitation on the substrate; see Section 3.2.1. The etch bath conditions must be tested and optimized for critical applications.

- The combination of KOH and DRIE, particularly when geometric features etched with each process intersect, is fabrication intensive but possible. Two processes combining these etches are presented, and both were successful. The first used a Si_3N_4 mask and shadow wafers, and the second used an SiO_2 mask without shadow wafers; see Sections 4.2, and 5.3.

- The electrical isolation of structures through die-sawing after wafer bonding worked well. The labyrinth seals used to contain die-saw slurry from entering the relay volume also worked well when capped with dicing tape; see Section 5.2.4.

- Oxide pin-holes and poor trench wall passivation led to actuator porosity removing perhaps 50% of the actuator contact area.

- Anodic bonding through thick oxides ($0.2\,\mu$m) was successful but the small contact pads led to weak bonding.

- During electroplating the spring sidewalls plated quite thickly. This was undesired as it increased the spring stiffness. A single gap relay design would alleviate this problem.

- The deposited SiO_2 films worked well as a KOH masks. However, thick oxide films had to be used due to the lower selectivity in KOH etching compared to

Si_3N_4 films.

- The wire bonding step with gold wire to hard metals (Pd, Pd-Co, Rh) was successful at high energy and temperature settings. The surface has to be stripped of oxides using diluted sulfuric acid.

Proposed future work

- The current carrying of the relays is limited to 1 A particularly due to the contact resistance. In order to lower the contact resistance, it is necessary to increase the contact force or, alternatively, to increase the fraction of load bearing area that contributes to conduction.

- The easiest way to improve the contact force with the present design is to utilize the full travel of the actuators. This can be achieved through a better controlled electroplating process, or alternatively through the use of other metal deposition techniques.

- One possible method to increase the electrical contact area is to package the relay in an inert environment, thereby eliminating contact oxidation.

- Chapter 7 presents an alternative relay concept using the {111}-contacts that offers larger forces, and potentially simpler fabrication, while retaining galvanic isolation.

Chapter 7

Concept for an out-of-plane displacement MEMS relay using {111} contacts

The fabrication of a MEMS relay with oblique, atomically parallel and planar, insulated contacts and out-of-plane motion is proposed. These contacts consist of {111} Si surfaces which have been bulk micromachined by wafer-front and wafer-back anisotropic etching of {100} silicon wafers using, for example, potassium hydroxide (KOH) or tetramethylammonium hydroxide (TmAH) solutions. The contacts are subsequently coated with conductive films. The oblique geometry of the contacts provides low on-state contact resistance. This is because the proposed contacts are complimentary (highly parallel and planar), and as these surfaces touch, they do so in a large effective contact area which lowers contact resistance and increases the devices current carrying capacity. The oblique geometry of the contacts allows for an enhanced metallization process resulting in better corner coverage and thicker metal on the contact surfaces, which further reduces the contact resistance. This is because a larger projected area is exposed during metallization. Additionally, the proposed contact design provides a large stand-off between the contacts, which is needed to prevent arcing. Further, the proposed oblique contact geometry introduces contact wipe, which is known to enhance the contact reliability by "cleaning" the contacts

as the relay cycles. The contact configuration keeps particles from being "trapped" between the contacts which may lead to hot-spots and contact failure.

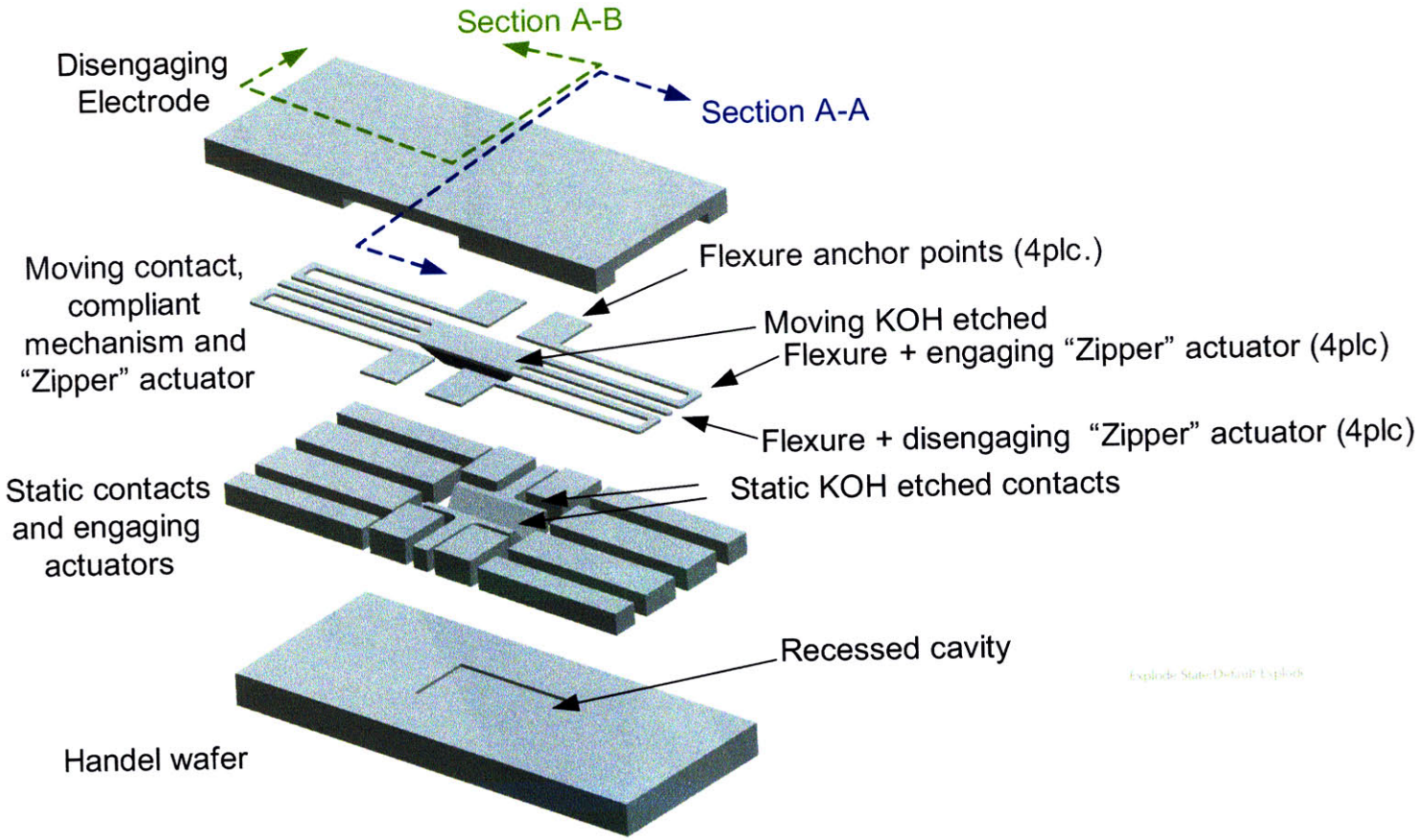


Figure 7-1: Concept for an out-of-plane motion MEMS relay with {111} contacts. Exploded assembly view

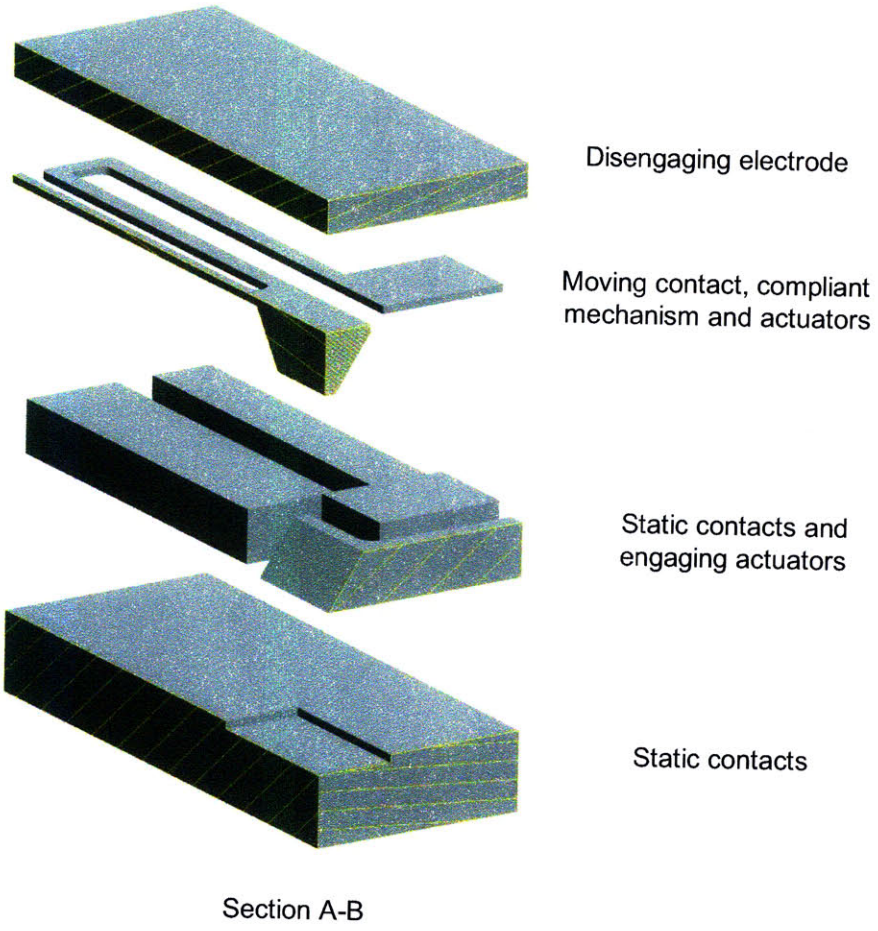


Figure 7-2: Concept for an out-of-plane motion MEMS relay with {111} contacts. Sectioned view.

Appendix A

Detailed Process Plan

Detailed fabrication process plans for *MEMS-relay 1* and *MEMS-relay 2* are presented next. Several fields are indicated.

- **Operation** describes the main process step.
- **Operation number (OP)** is the process step number.
- **Lab** refers to the specific lab in MIT's Micro Technology Laboratories (MTL) where the process step is carried out. The labs used are TRL (Technology Research Lab), and ICL (Integrated Circuit Lab).
- **Machine** is the tool name as described in MTL's Process Technology Committee (PTC) process matrix:
  `http://www-mtl.mit.edu/services/fabrication/ptc_matrix.html` .
- **Recipe** lists specific process details, chemistry or settings used on a specific process step.
- **Description** provides additional information or comments on specific process steps.
- **Wafer** describes the attributes of the wafer in the spirit of a contamination protocol, as listed in the PTC process matrix. The particular attribute determines which tool the wafer can be processed in. Green: CMOS compatible process,

previously exposed to Photo Resist. Brown: Wafer has undergone RCA cleaning process, required for certain diffusion tubes. Yellow: Wafer has undergone KOH processing. Red: Wafer has been exposed to a tool which handles non CMOS metals.

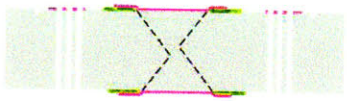
A.1 Fabrication process *MEMS relay 1*

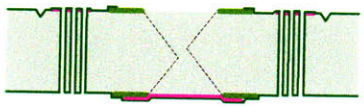
A detailed fabrication process plans for *MEMS relay 1* is presented next. The masks for this process are shown in B.

Start with: 6 inch, 300 um, (100), n-type, 0.01-0.02 Ohm-cm, DSP wafer

Operation	OP	Lab	Machine	Recipe	Description	Wafer
Premetal piranha	5	ICL	**Premetal**	piranha	premetal clean	
Deposit VTR Nitride 1	10	ICL	**VTR**	2000A	**VTR Nitride**	
Photolitography, wafer FRONT, Mask: A	20	TRL	HMDS	-		
	22	TRL	Coater (w. back side)	1 um	OCG resist	
	23	TRL	Pre-bake oven	90℃, **5 min**	Prebake P.R.	
	24	TRL	Coater (front side)	1μm	Spin positive P.R. wafer **front** side	
	25	TRL	Pre-bake oven	90℃, **30 min**		
	26	TRL	**EV1, mask A**	3s	**Wafer front,** Mask A, align to major flat	
	27	TRL	Photo-wet develop			
	28	TRL	Post bake oven	30 min	Post bake	
Pattern Nitride 1, wafer FRONT	30	ICL	**LAM**	Nitride_CF4 time	**Pattern Nitride 1,** wafer **front** side	
	35	ICL	Asher	-	Strip PR	
	37	ICL	Acidhood	-	clean	
KOH etch cryst. align. feat.	40	ICL	**KOH-hood**	KOH	**Timed KOH etch (15h)**	
	45	TRL	Acidhood	2X piranha +30s HF dip	Post KOH clean	
Photolitography, wafer FRONT, Masks: B. (Protect wafer back side)	50	TRL	HMDS	-		
	51	TRL	Coater (back side)	1μm	Spin + P.R. wafer **back** side	
	52	TRL	Pre-bake oven	90℃, **5 min**	Prebake P.R.	
	53	TRL	Coater (front side)	1μm	Spin positive P.R. wafer **front** side	
	54	TRL	Pre-bake oven	90℃, **30 min**		
	55	TRL	**EV1, mask B**	1.5s	**Wafer front,** Mask B, align to mask A	
	56	TRL	Photo-wet develop			
	57	TRL	Post bake oven	30 min	Post bake	
Pattern Nitride 1, wafer FRONT	60	ICL	**LAM**	SF6	**Pattern Nitride** 1 wafer **front** side	
	62	TRL	Asher	-	Strip PR	
	64	TRL	Acidhood	Piranha	Clean	

Operation	OP	Lab	Machine	Recipe	Description	Wafer
Photolitography, wafer BACK, Masks: C. (Protect wafer front side)	70	TRL	HMDS	-		
	71	TRL	Coater (front side)	1µm	Spin + P.R. wafer **font** side	
	72	TRL	Pre-bake oven	90℃, **5 min**	Prebake P.R.	
	73	TRL	Coater (back side)	1µm	Spin positive P.R. wafer **back** side	
	74	TRL	Pre-bake oven	90℃, **30 min**		
	75	TRL	**EV1, mask C**	1.5s	**Wafer front,** Mask B, align to mask A	
	76	TRL	Photo-wet develop			
	77	TRL	Post bake oven	30 min	Post bake	
Pattern Nitride 1, wafer BACK	80	ICL	**LAM**	SF6	**Pattern Nitride** 1 wafer **back** side	
	82	TRL	Asher	-	Strip PR	
	84	TRL	Aicidhood	Piranha	Clean	
Deposit & anneal oxide 1	90	ICL	Premetal clean	-	Pre-metal clean (Piranha + 15s HF dip)	
	92	ICL	**DCVD**	0.5 um	**Deposit oxide** wafer **front** side	
	94	ICL	**DCVD**	0.5 um	**Deposit oxide** wafer **back** side	
	96	TRL	**Tube B-3**	1h, 900 C	**Anneal**	
Photolitography, wafer FRONT and back sides, Masks: D & E	100	TRL	HMDS	-		
	101	TRL	Coater (back side)	1µm	Spin positive P.R. wafer **back** side	
	102	TRL	Pre-bake oven	90℃, **5 min**	Prebake P.R.	
	103	TRL	Coater (front side)	1µm	Spin positive P.R. wafer **front** side	
	104	TRL	Pre-bake oven	90℃, **30 min**		
	105	TRL	**EV1, w. front, Mask D**	1.5s	**Expose P.R.,** use mask D	
	107	TRL	**EV1, w. back, Mask E**	3-4 min	**Expose P.R.,** use mask E	
	108	TRL	Photo wet -1	3-4 min	**Develop. USE CASSETTE**	
	109	TRL	Post bake oven	30 min	Post bake	
Pattern Oxide 1, FRONT & BACK	110	TRL	Acidhood	BOE	**Pattern oxide**	
	112	TRL	Asher		Strip PR	
	114	TRL	Acidhood	Piranha	Clean	

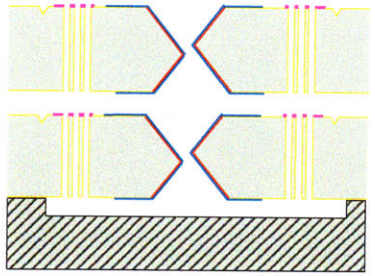




Operation	OP	Lab	Machine	Recipe	Description	Wafer
Photolitography, wafer FRONT, Mask: F	120	TRL	HMDS	-		
	122	TRL	Coater	8µm	Spin thick P.R. wafer **front** side	
	124	TRL	Pre-bake oven	90℃, 30 min	Prebake P.R.	
	126	TRL	**EV1**	20s (4 times 5s + 5s wait)	**Wafer front** side, mask F	
	128	TRL	Photo wet -1	~ 1:40 min	Develop P.R.	
	129	TRL	Post bake oven	30 min	Post bake	
Tape wafer back	130	TRL	Coater	1µm	Spin wafer back, thin resist	
	131	TRL	Prebake oven	20 min	Pre bake	
	132	TRL	-	-	Cover w. back side with blue dicing tape	
DRIE through-etch	140	TRL	**STS 2**	JBETCH, P=28mTorr, t ~ 4h	DRIE through wafer	
	142	TRL	**-**	-	Remove tape (peel off)	
	144	TRL	Solvent hood	Acetone release	Demount	
	146	TRL	Asher	-	Post STS clean (strip teflon)	
	148	TRL	Acidhood	Piranha	clean	
Deposit VTR Nitride 2	150	TRL	Acidhood	Piranha	Premetal clean	
	150	ICL	**VTR**	2000A	Deposit **nitride (2000A)**	
Mount shadow wafer on wafer front (Mask G)	160	TRL	**EV-620 / Microscope**		**Align top KOH S/W to device wafer**	
	162	TRL	Solvent hood		Apply PR drops to wafer OD to attach S/W to device wafer	
	164	TRL	Prebake oven	Prebake 15 min		
	166	TRL	Solvent hood	Mont on Handle wafer		
	164	TRL	Prebake oven	Prebake 20 min		
Pattern Nitride 2, wafer FRONT	170	TRL	**STS-2**	SF6, "nitride" recipie	**Pattern Nitride (top rough KOH mask)**	
	172	TRL	Solvent hood	Acetone demount	**Dismount handle and shadow wafer**	
	174	TRL	**Asher**	-	**PR/Teflon strip**	
	175	TRL	Acid hood	Piranha	Clean	
Etch sacrificial Oxide	180	ICL	Acid hood	BOE (6 min)	Etch oxide	

Operation	OP	Lab	Machine	Recipe	Description	Wafer
KOH etch through (contacts) wafer front	190	ICL	**KOH-hood**	KOH (33% 80C after 1 min 50:1 HF dip)	**Through etch**	
	195	TRL	Acidhood	2X piranha + HF dip	Post KOH clean	
Deposit VTR Nitride 3	200	ICL	**VTR**	2000A	Deposit **nitride (2000A)**	
Mount shadow wafer on wafer back (Mask H)	210	TRL	**EV-620 / Microscope**		**Align bot KOH S/W to device wafer**	
	212	TRL	Solvent hood		Apply PR drops to wafer OD to attach S/W to device wafer	
	214	TRL	Prebake oven	Prebake 15 min		
	216	TRL	Solvent hood	Mont on Handle wafer	Apply PR drops to wafer OD to attach S/W to device wafer	
	218	TRL	Prebake oven	Prebake 20 min		
Pattern Nitride 2,3, wafer BACK	220	TRL	**STS-2**	SF6, nitride recipie	**Pattern Nitride (top rough KOH mask)**	
	222	TRL	Solvent hood	Acetone demount	**Dismount handle and shadow wafer**	
	224	TRL	**Asher**	-	**PR/Teflon strip**	
	226	TRL	Acid hood	Piranha	Clean	
Etch sacrificial Oxide	230	ICL	Acid hood	HF / BOE	Etch oxide	
KOH etch through (contacts) wafer back	240	ICL	**KOH-hood**	KOH (33% 80C after 1 min 50:1 HF dip)	**Through etch**	
	245	TRL	Acidhood	2X piranha + HF dip	Post KOH clean	
Strip nitride (1-3)	250	ICL	Hot phosphoric	150 min	Strip nitride	
Strip oxide	260	TL	Acidhood	49% HF, 30s	Strip oxide	
Strip nitride (1)	270	ICL	Hot phosphoric		Strip nitride 1 (buried under oxide)	
Grow oxide 3	280	TRL	RCA station	-		
	285	TRL	A2	2000A	Grow thermal oxide	

Operation	OP	Lab	Machine	Recipe	Description	Wafer
Mount shadow wafer {Mask I}	290	TRL	**EV-620/microscope**		**Align top KOH S/W to device wafer**	
	292	TRL	Solvent hood		Apply PR drops to wafer OD to attach S/W to device wafer	
	294	TRL	Prebake oven	Prebake 15 min		
	296	TRL	Mount on handle	-		
	298	TRL	Prebake oven	Prebake 20 min		
Pattern Oxide 3, wafer FRONT	300	TRL	**STS-2**		**Pattern Oxide 3 (top contact pad mask)**	
	302	TRL	Solvent hood	Acetone demount	**Dismount handle and shadow wafer**	
	304	TRL	**Asher**	-	**PR/Teflon strip**	
	306	TRL	Acid hood	Piranha	Clean	
Mount front and back metallization shadow wafers {Masks J & K}	310	TRL	**Microscope**		Align "top metalization" SW to device wafer	
	312	TRL	Solvent hood		Apply PR drops to wafer OD to attach S/W to device wafer	
	324	TRL	Prebake oven	Prebake 15 min		
	316	TRL	**Microscope**		Align "bottom metalization" SW to dev. wafer	
	318	TRL	Solvent hood		Apply PR drops to wafer OD to attach S/W to device wafer	
	319	TRL	Prebake oven	Prebake 15 min		
Evaporate metal, wafer TOP & BOTTOM	320	TRL	**E-beam**	200A Ti + 0.7 um Au	**Evaporate Au top** wafer side	
	322	TRL	**E-beam**	200A Ti + 0.7 um Au	**Evaporate Au bottom** wafer side	
	324	TRL	Acidhood	Piranha	Demount shadow wafers	
Anodic Bond	330	TRL	**EV 620 / EV501**	Flag contact to device!!!	**Align & bond dev. wafer to handle**	



Si | VTR nitride 1 | Dep. oxide | VTR nitride 2 | VTR nitride 3 | Thermal SiO2 | Thermal dielectric Oxide | Gold | Pyrex

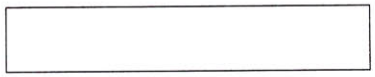
Change Log:

8-Sep-06 Created + submited to PTC

A.2 Fabrication process *MEMS relay 2*

The masks for this process are shown in B.

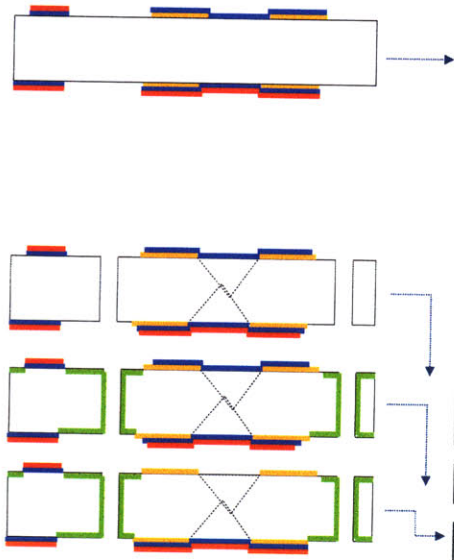
A detailed fabrication process plans for *MEMS relay 2* is presented next.



Start with: 6 inch, 300 um, (100), n-type, 0.01-0.02 Ohm-cm, DSP wafer

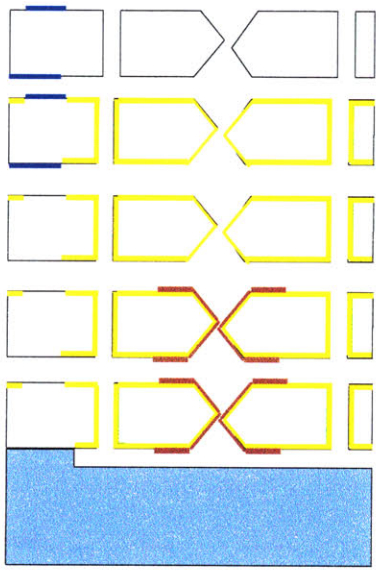
Operation	OP	Lab	Machine	Recipe	Description	Wafer
Photo, wafer FRONT, Mask A1: Alignment mark	10	TRL	HMDS	Setting 5	Adhesion promoter	
	11	TRL	Coater	1 um, OCG resist, wafer front	OCG resist, w. front	
	12	TRL	Pre-bake oven	90℃, **30 min**	Pre bake	
	13	TRL	**EV1**	2.5s	Mask A, wafer front, align to major flat & wafer OD	
	14	TRL	Photo-wet develop	~90s	934 1:1	
	15	TRL	Post bake oven	30 min	Post bake	
Pattern Si (alignm. marks) wafer front	20	TRL	**STS**	SF6, "alignment mark" recipie, ~10s	Alignment marks	
	21	TRL	**Asher**	1h	Strip teflon	
	22	TRL	**Piranha**	10 min	PR strip/clean	
Photo, wafer BACK, Mask A2: Alignment mark	30	TRL	HMDS	Setting 5	Adhesion promoter	
	31	TRL	Coater	1 um	OCG resist, w. front	
	32	TRL	Pre-bake oven	90℃, **30 min**	Pre bake	
	33	TRL	**EV1**	2.5s	**Exp. P.R., w. back,** Mask A, align to wafer front AM	
	34	TRL	Photo-wet develop	~90s	934 1:1	
	35	TRL	Post bake oven	30 min	Post bake	
Pattern Si (alignm. marks) wafer back,	40	TRL	**STS**	SF6 ("alignment mark"), ~10s	Short etch (~10s ALIGN recipie) of the alignment marks	
	41	TRL	**Asher**	1h	Strip teflon	
	42	TRL	**Piranha**	10 min	PR strip	
Photo, wafer FRONT, Mask B: Streets + labels	50	TRL	HMDS	Setting 5	Adhesion promoter	
	51	TRL	Coater (wafer frontside)	1 um, 2-3kRPM	OCG resist, w. front	
	52	TRL	Pre-bake oven **(STD, 30 min)**	90℃, **30 min**	Pre bake	
	53	TRL	**EV1**	2.5 s	**Expose P.R., w. front,** Mask B , align to w. front AM	
	54	TRL	Photo-wet develop	~1 min	934 1:1	
	55	TRL	Post bake oven	120C, 30 min	Post bake	
Pattern streets, wafer front	60	TRL	**STS**	"ALIGN" 10s	Short etch (~10s ALIGN recipie)	
	61	TRL	**Asher**	1h	Strip teflon	
	62	TRL	**Piranha**	10 min	PR strip	
Premetal cl'n	70	ICL	**"Premetal" clean**	piranha	premetal clean	
Deposit & anneal Oxide	71	ICL	**DCVD**	3um (1.1um needed for 3h KOH etch)	**Deposit Oxide wafer front + back side**	
	72	TRL	**Tube B-3**	1h, 900 C, 51% N2	Anneal	
Photo, wafer FRONT, Mask C: KOH top	60	TRL	Coater (wafer frontside)	1 um	OCG resist, 1kRPM	
	61	TRL	Pre-bake oven short **(15 min)**	90℃, **15 min**	Pre bake (short)	
	62	TRL	Coater (wafer frontside)	1 um	OCG resist, 1kRPM	
	63	TRL	Pre-bake oven short **(15 min)**	90℃, **15 min**	Pre bake (short)	
	64	TRL	**EV1**	10s	**Expose P.R., wafer front,** Mask KOH top, align to front	
	65	TRL	Photo-wet develop	1min 30s-1min 45, 934 1:1	934 1:1	
	66	TRL	Post bake oven	120C, 30 min	Post bake	
Pattern Oxide w. front	70	ICL	**Centura**	~ 340s (2 steps w. metrology in between)	**Pattern Oxide wafer front**	
	71	TRL	**Acidhood**	piranha	PR strip/clean	

Operation	OP	Lab	Machine	Recipe	Description	Wafer
Photo, wafer FRONT, Mask D: KOH bot	80	TRL	Coater (wafer frontside)	1 um	OCG resist, 1kRPM	
	81	TRL	Pre-bake oven short (15 min)	90℃, 15 min	Pre bake (short)	
	82	TRL	Coater (wafer frontside)	1 um	OCG resist, 1kRPM	
	83	TRL	Pre-bake oven short (15 min)	90℃, 15 min	Pre bake (short)	
	84	TRL	EV1	10s	Expose P.R., w. back, Mask KOH bot, align to w. back	
	85	TRL	Photo-wet develop	1min 30s-1min 45, 934 1:1	934 1:1	
	86	TRL	Post bake oven	120C, 30 min	Post bake	
Pattern Oxide w. back	90	ICL	Centura	~ 340s (2 steps w. metrology in between)	Pattern Oxide wafer front	
	91	TRL	Acidhood	piranha	PR strip/clean	
Premetal cl'n	100	ICL	"Premetal" clean	piranha	premetal clean	
Deposit & anneal Oxide	101	ICL	DCVD	500A, wafer front & back	Deposit Oxide wafer front + back side	
	102	TRL	Tube B-3	1h, 900 C, 51% N2	Anneal	
Photo, wafer FRONT, Mask E: Thin oxide	110	TRL	Coater (wafer frontside)	1 um	OCG resist, 1kRPM	
	111	TRL	Pre-bake oven short (15 min)	90℃, 15 min	Pre bake (short)	
	112	TRL	Coater (wafer frontside)	1 um	OCG resist, 1kRPM	
	113	TRL	Pre-bake oven short (15 min)	90℃, 15 min	Pre bake (short)	
	114	TRL	EV1	10s	Expose P.R., wafer front, Mask E, align to front	
	115	TRL	Photo-wet develop	1min 30s-1min 45s, 934 1:1	934 1:1	
	116	TRL	Post bake oven	120C, 30 min	Post bake	
Pattern Thin Oxide w. front	120	ICL	Centura	~ 10s	Pattern Thin oxide wafer front	
	121	TRL	Acidhood	piranha	PR strip/clean	
Premetal cl'n	130	TRL	"Premetal" celan	Piranha	premetal clean	
Deposit Nitride	131	ICL	VTR	2500A		
Photo, wafer FRONT, Mask F: "Nitride top"	140	TRL	Coater (wafer front side)	1 um	OCG resist, 1kRPM	
	141	TRL	Pre-bake oven short (15 min)	90℃, 15 min	Pre bake (short)	
	142	TRL	Coater (wafer frontside)	1 um	OCG resist, 1kRPM	
	143	TRL	Pre-bake oven short (15 min)	90℃, 15 min	Pre bake (short)	
	144	TRL	EV1	10s	Expose P.R., w. front, Mask F, align to w. front	
	145	TRL	Photo-wet develop	1min 30s-1min 45, 934 1:1	934 1:1	
	146	TRL	Post bake oven	120C, 30 min	Post bake	
Pattern nitride w. front	150	TRL	STS-3 (STS-2)	"nitride" recipie, 7.5-8 min (ER 500A/s)	Pattern nitride	
	151	TRL	Asher	1h	Remove teflon	
	152	TRL	Piranha	10 min	strip PR	
Photo, wafer FRONT, Mask G: "Nitride Bot"	160	TRL	Coater (wafer back side)	1 um	OCG resist, 1kRPM	
	161	TRL	Pre-bake oven short (15 min)	90℃, 15 min	Pre bake (short)	
	162	TRL	Coater (wafer back side)	1 um	OCG resist, 1kRPM	
	163	TRL	Pre-bake oven short (15 min)	90℃, 15 min	Pre bake (short)	
	164	TRL	EV1	10s	Expose P.R., w. back, Mask G, align to w. back	
	165	TRL	Photo-wet develop	1min 30s-1min 45, 934 1:1	934 1:1	
	166	TRL	Post bake oven	120C, 30 min	Post bake	
Pattern nitride w. back	170	TRL	STS-3 (STS-2)	"nitride" recipie, 7.5-8 min (ER 500A/s)	Pattern nitride	
	171	TRL	Asher	1h	Remove teflon	
	172	TRL	Piranha	10 min	strip PR	



Operation	OP	Lab	Machine	Recipe	Description	Wafer
Premetal cl'n	180	ICL	**"Premetal" clean**	piranha	premetal clean	
Deposit & anneal Oxide Cap	181	ICL	**DCVD**	1.75 um w. front, 5kA wafer back	**Deposit Oxide wafer front + back side**	
	182	TRL	**Tube B-3**	1h, 900 C, 51% N2	Anneal	
Photo, wafer FRONT, Mask H: Oxide Cap Top	190	TRL	Coater (wafer frontside)	1 um	OCG resist, 1kRPM	
	191	TRL	Pre-bake oven short **(15 min)**	90℃, **15 min**	Pre bake (short)	
	192	TRL	Coater (wafer frontside)	1 um	OCG resist, 1kRPM	
	193	TRL	Pre-bake oven short **(15 min)**	90℃, **15 min**	Pre bake (short)	
	194	TRL	**EV1**	10s	**Expose P.R., wafer front,** Mask H, align to AM	
	195	TRL	Photo-wet develop	1min 30s-1min 45, 934 1:1	934 1:1	
	196	TRL	Post bake oven	120C, 30 min	Post bake	
Pattern Oxide cap w. front	200	ICL	**Centura**	~ 180s	**Pattern Oxide wafer front**	
	201	TRL	**Acidhood**	piranha	PR strip/clean	
Photo, wafer Back, Mask I: Oxide Cap BotKOH bot	210	TRL	Coater (wafer back side)	1 um	OCG resist, 1kRPM	
	211	TRL	Pre-bake oven short **(15 min)**	90℃, **15 min**	Pre bake (short)	
	212	TRL	Coater (wafer back side)	1 um	OCG resist, 1kRPM	
	213	TRL	Pre-bake oven short **(15 min)**	90℃, **15 min**	Pre bake (short)	
	214	TRL	**EV1**	10s	**Expose P.R., wafer back,** Mask I, align to back	
	215	TRL	Photo-wet develop	1min 30s-1min 45s, 934 1:1	934 1:1	
	216	TRL	Post bake oven	120C, 30 min	Post bake	
Pattern Cap Oxide w. back	220	ICL	**Centura**	~ 75s	**Pattern oxide cap wafer back**	
	221	TRL	**Acidhood**	piranha	PR strip/clean	
BOE	230	TRL	BOE	2 min	Clear oxide left due to CENTURA hotspot	
Photo, wafer FRONT, Mask: J DRIE	240	TRL	HMDS	Thick resist setting (#3)	Adhesion promoter	
	241	TRL	Coater	8μm thick resist	Spin thick P.R. wafer **front,** 3k RPM	
	242	TRL	Pre-bake oven	90℃, 30 min	Prebake P.R.	
	243	TRL	**EV1**	20s (4 times 5s + 5s wait)	**Expose PR,** use Mask "**DRIE**" wafer **front** side	
	244	TRL	Photo wet -1	~ 1:40 min	Develop P.R.	
	245	TRL	Post bake **(prebake oven)**	30 min	Post bake	
Tape wafer back	250	TRL	Coater	1μm	Spin wafer back, thin resist	
	252	TRL	Prebake oven	20 min	Pre bake	
Mount on Quartz handle	253	TRL	-	-	Cover wafer back with blue dicing tape	
	260	TRL	Coater -	Target mount on quartz handle wafer		
DRIE through-etch	270	TRL	**STS 2**	JBETCH, P=28mTorr, t ~ 4h	DRIE through wafer	
	271	TRL	-	-	Remove tape (peel off)	
	272	TRL	Solvent hood	1:1:1 Acetone-Toluene-methanol	Demount	
	273	TRL	Asher	-	Post STS clean (strip teflon)	
	274	TRL	Acidhood	Piranha	clean	
Grow passivation oxide I	280	TRL	RCA station	-	-	
	281	TRL	A2	Wet oxidation; 3x1um recipie T=1050C	Grow thermal oxide 1.9um	
BOE Dip	290	TRL	BOE	1 min	Strip oxy-nitride layer	
Strip nitride	291	ICL	Hot phosphoric	~150 min	Strip nitride	

Operation	OP	Lab	Machine	Recipe	Description	Wafer
KOH etch wafer front	300	ICL	**KOH-hood**	KOH 33% 80C	**Through etch**	
	301	TRL	Acidhood	2X piranha + HF dip	Post KOH clean	
Strip Oxide Cap Wafer Bottom	310	TRL	Acidhood	BOE: Strip oxide cap wafer back		
Grow passivation oxide II	320	TRL	RCA station	-		
	321	TRL	A2	Wet oxidation; 3x1um recipie T=1050C	Grow thermal oxide 1.9um	
BOE Dip	330	TRL	BOE	30s	Strip oxy-nitride layer	
Strip nitride	331	ICL	Hot phosphoric		Strip nitride	
KOH etch wafer back	340	ICL	**ICL KOH hood**	50:1 HF dip :30s		
	341	ICL	**KOH-hood**	KOH 33% 80C	**Through etch**	
	342	TRL	Acidhood	2X piranha + HF dip	Post KOH clean	



Operation	OP	Lab	Machine	Recipe	Description	Wafer
Strip oxide	350	TL	Acidhood	49% HF, 30s	Strip oxide	
Grow dielectric oxide III	360	TRL	RCA station	-		
	361	TRL	A2	Wet thermal growth, 2000 A	Grow thermal oxide	
BOE Dip	370	TRL	BOE	30s	Strip oxy-nitride layer	
Strip nitride	371	ICL	Hot phosphoric	TBD	Strip nitride	
Mount front and back metallization shadow wafers (Masks J & K)	380	TRL	**Microscope / EV620**	Align "top metalization" shadow wafer on top side of device wafer		
	381	TRL	Solvent hood	Apply PR drops to the wafer OD to attach Shadow wafer to device wafer		
	382	TRL	Prebake oven	Prebake 15 min		
	383	TRL	**Microscope**	Align "bottom metalization" shadow wafer on top side of device wafer		
	384	TRL	Solvent hood	Apply PR drops to the wafer OD to attach Shadow wafer to device wafer		
	385	TRL	Prebake oven	Prebake 15 min		
Evaporate metal, wafer TOP & BOTTOM	390	TRL	**E-beam**	200A Ti + 0.7 um Au	**Evaporate Au top** wafer side	
	391	TRL	**E-beam**	200A Ti + 0.7 um Au	**Evaporate Au bottom** wafer side	
	392	TRL	Acidhood	Piranha	Demount shadow wafers	
Anodic Bond	400	TRL	**EV 620 / EV501**	Flag contact to device!!!	**Align & bond device wafer and handle wafer**	

Change log:
19-Jan-07 Process Created / PTC aprooved
10-May-07 Updated recipies
5-Jun-07 Added BOE etch step after Centura oxide cap patterning
15-Jun-07 Changed solvent demount mixture step 332 from Acetone to 1:1:1 Acetone-methanol-toluene

Appendix B

Masks

B.1 Masks *MEMS relay 1*

The masks used in the fabrication of *MEMS relay 1* are presented next. A wafer level mask is provided.

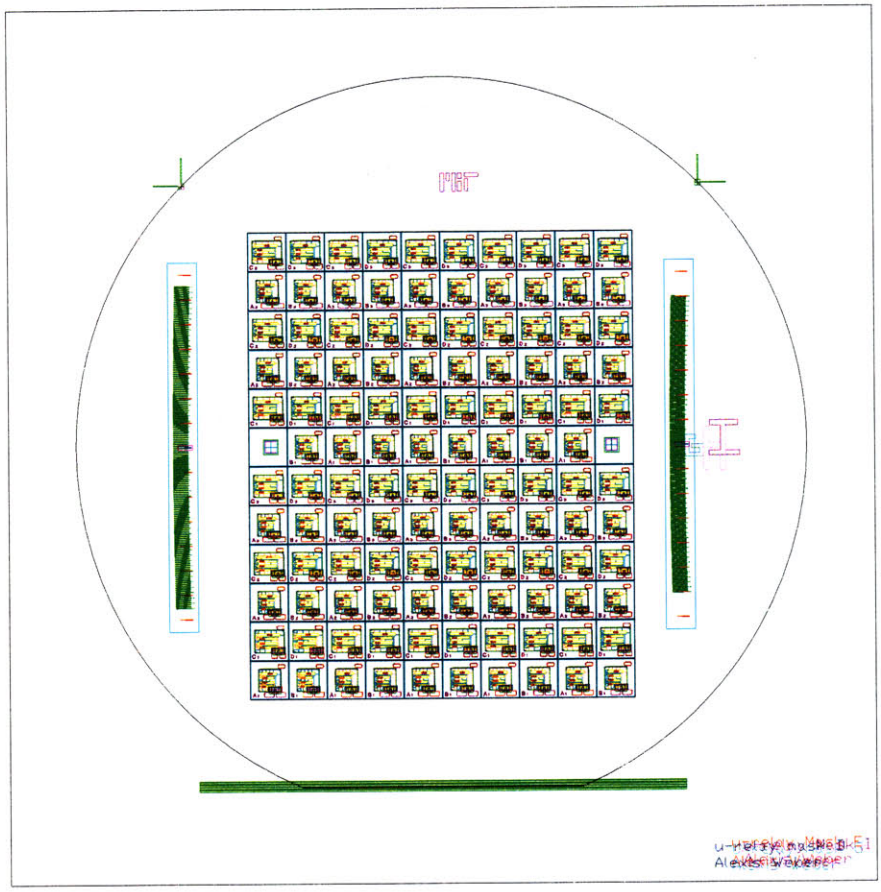


Figure B-1: All masks overlaid.

B.2 Masks *MEMS relay 2*

The masks used in the fabrication of *MEMS relay 2* are presented next. Note that for clarity the masks are shown at the die level.

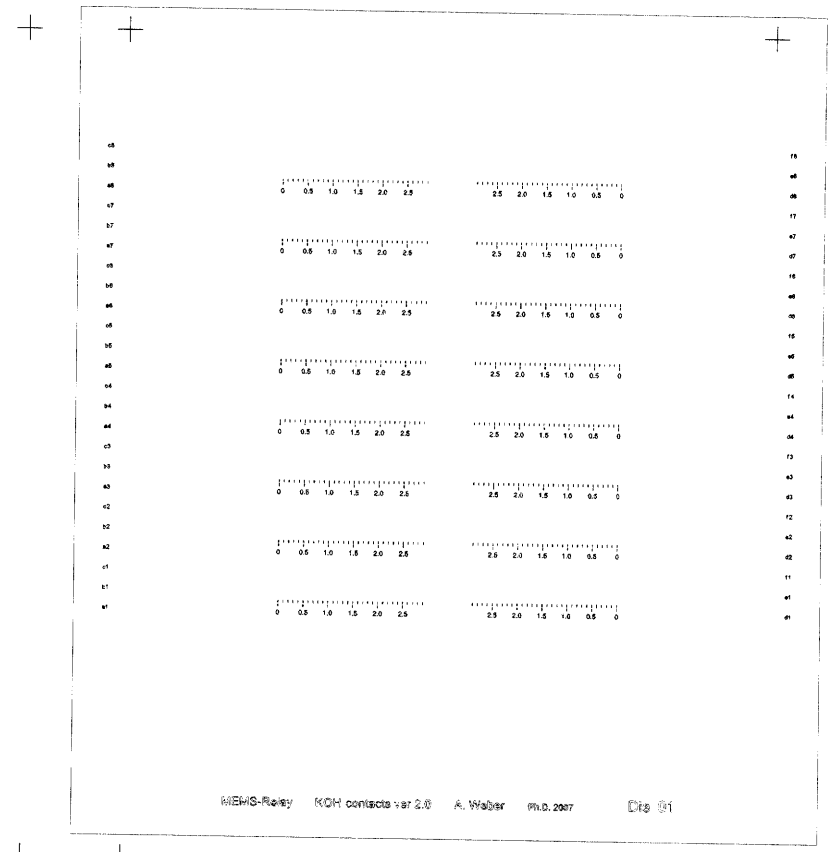


Figure B-2: Mask A: labels.

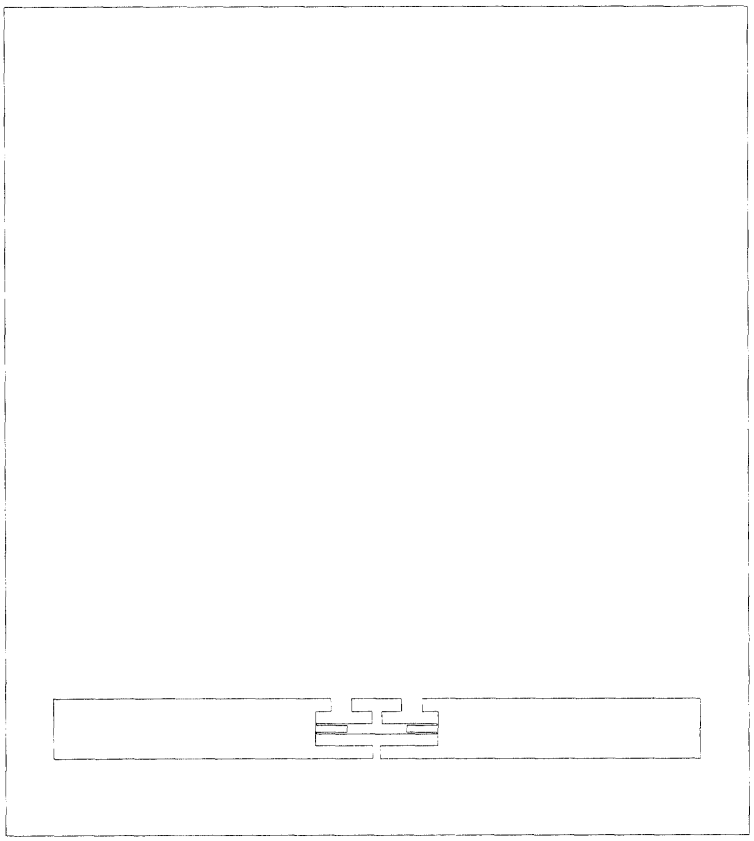


Figure B-3: Mask B: Oxide KOH mask, wafer top.

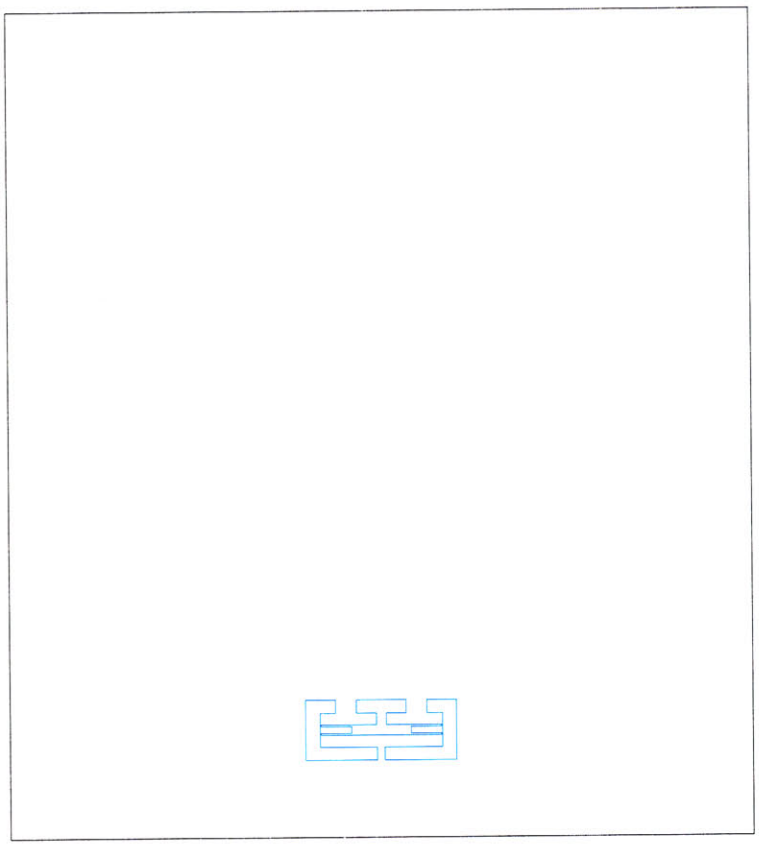


Figure B-4: Mask C: Oxide KOH mask, wafer bottom

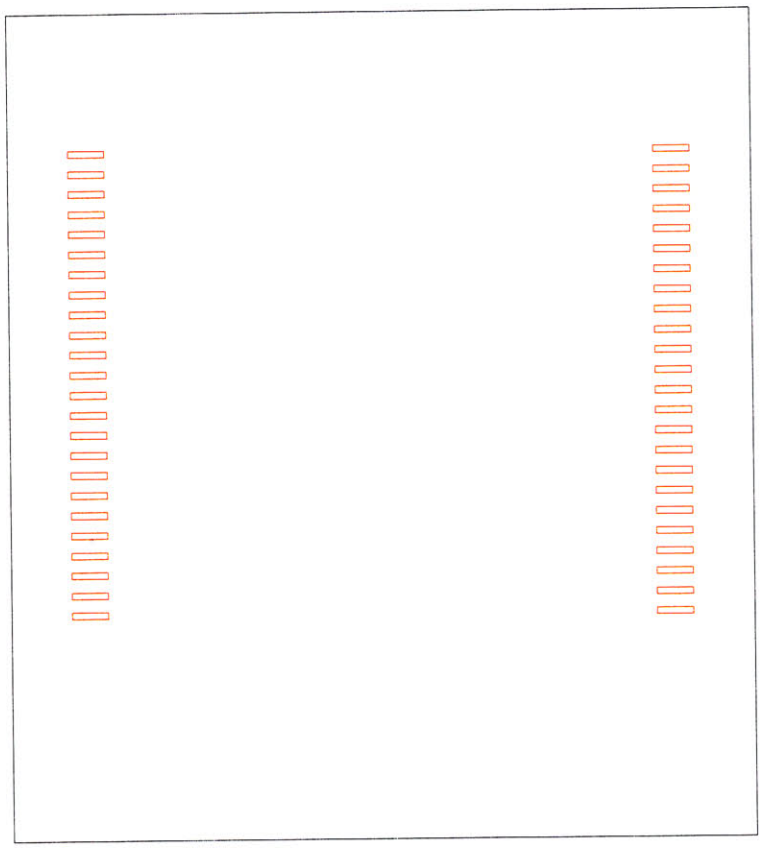


Figure B-5: Mask D: Thin oxide, wafer top.

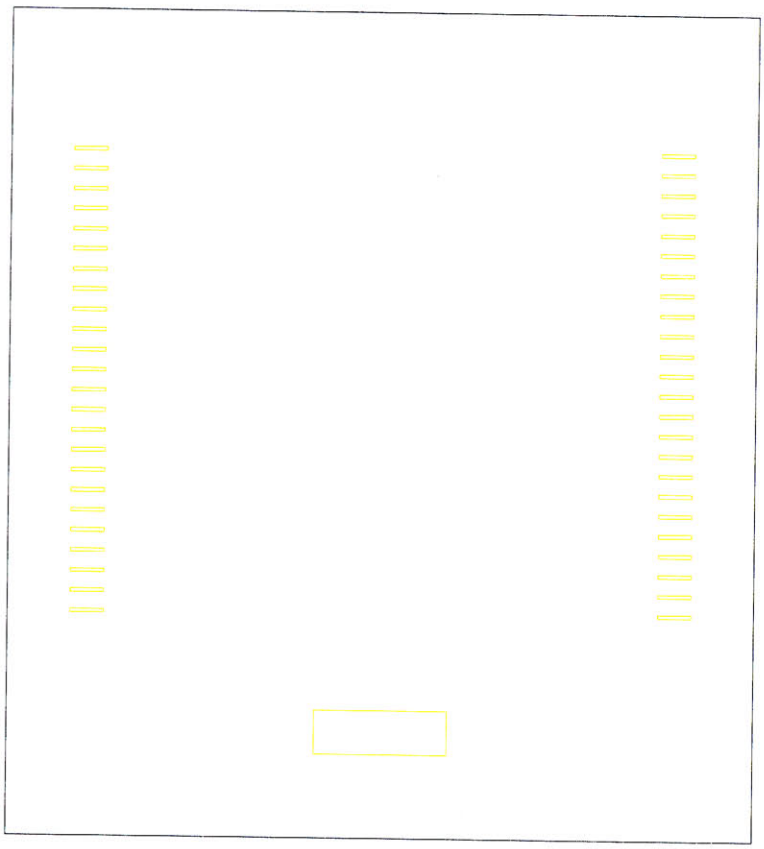


Figure B-6: Mask E: Nitride, wafer top

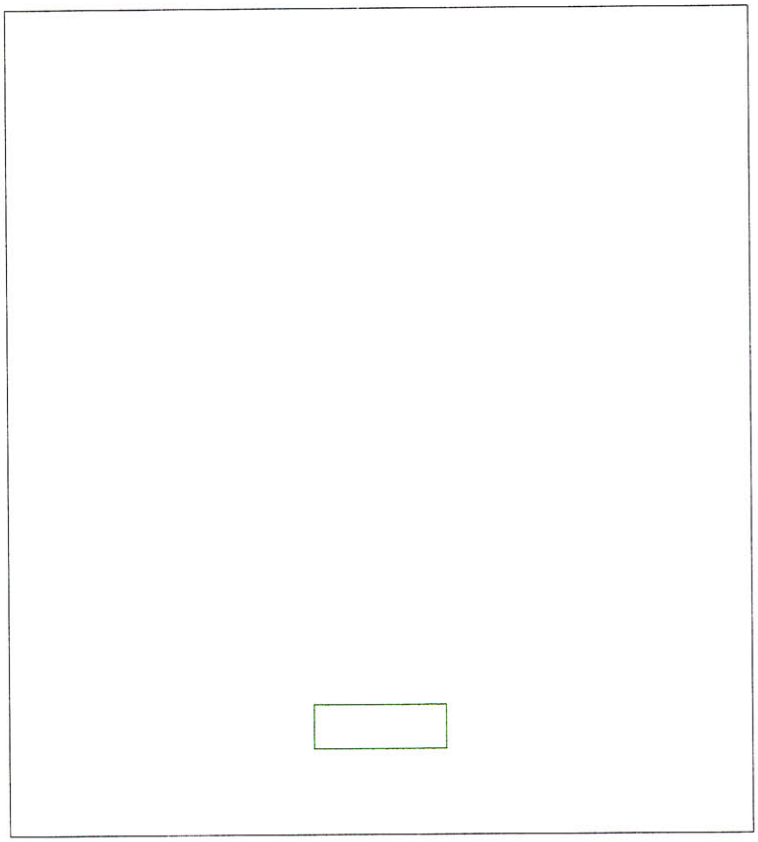


Figure B-7: Mask E: Nitride, wafer bottom

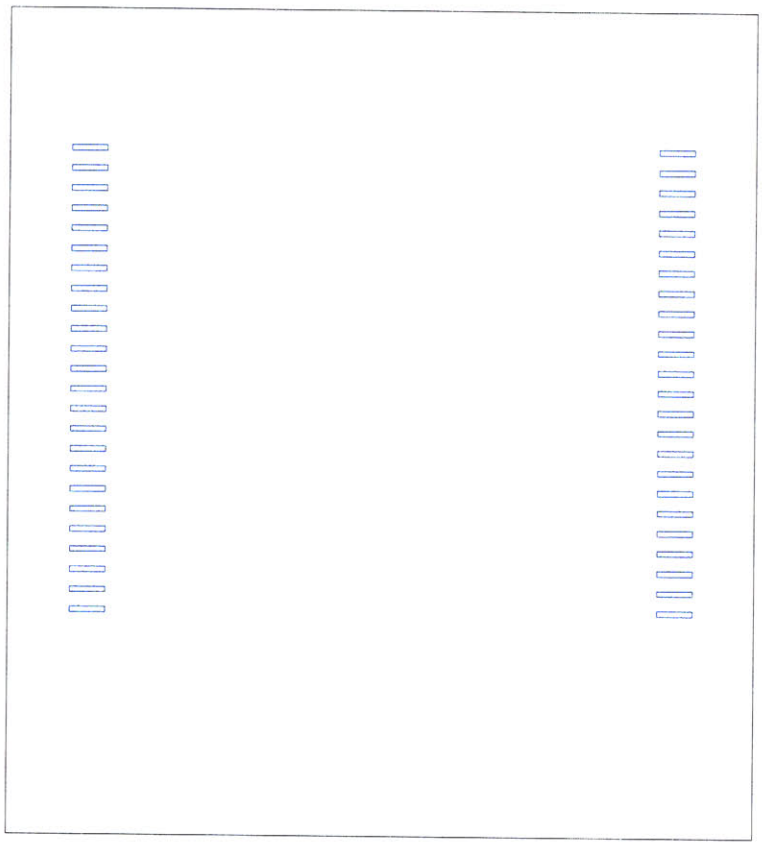


Figure B-8: Mask G: Oxide cap, wafer top

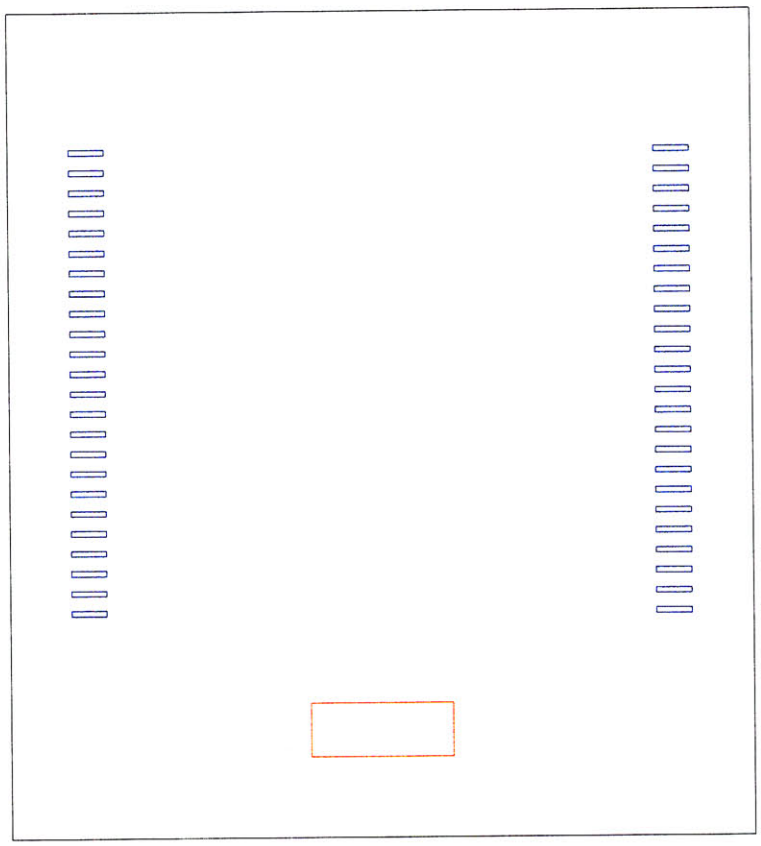


Figure B-9: Mask H: Oxide cap, wafer bottom

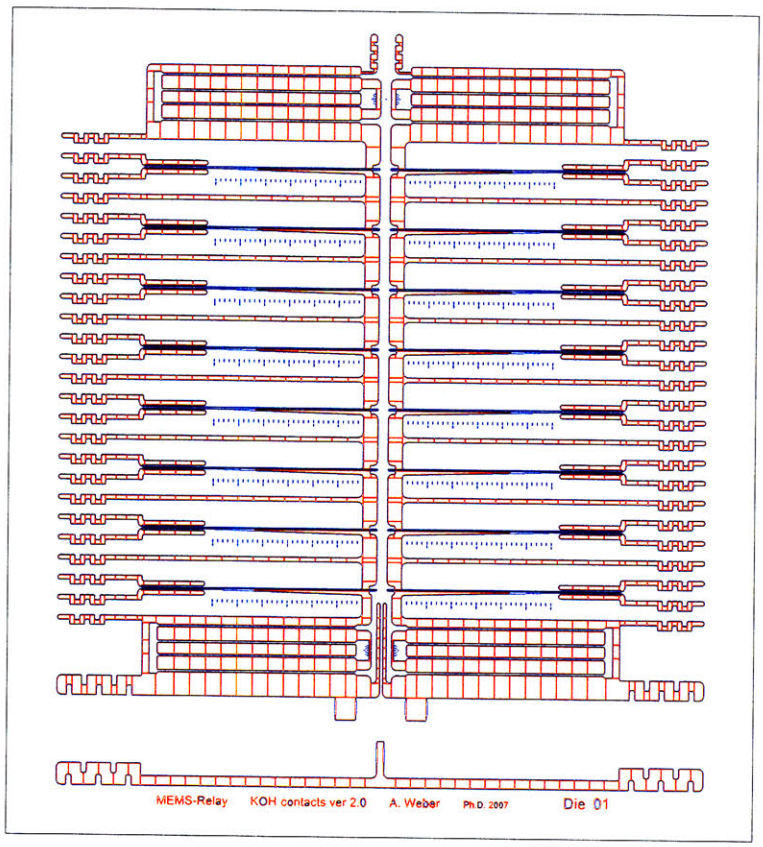


Figure B-10: Mask I: DRIE

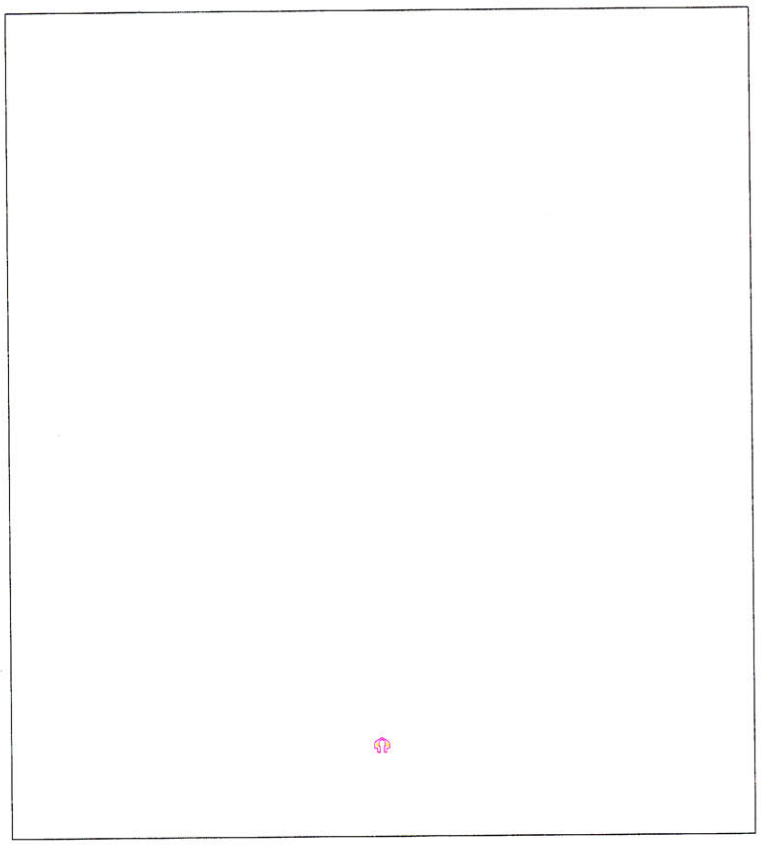


Figure B-11: Mask J: DRIE shaped trench correction. This mask is to be exposed after the DRIE mask and before development in order to correct the shape of the isolation trench. The geometry could be combined with mask I. A low resolution "transparency" mask was used to avoid a new expensive, e-beam written masks.

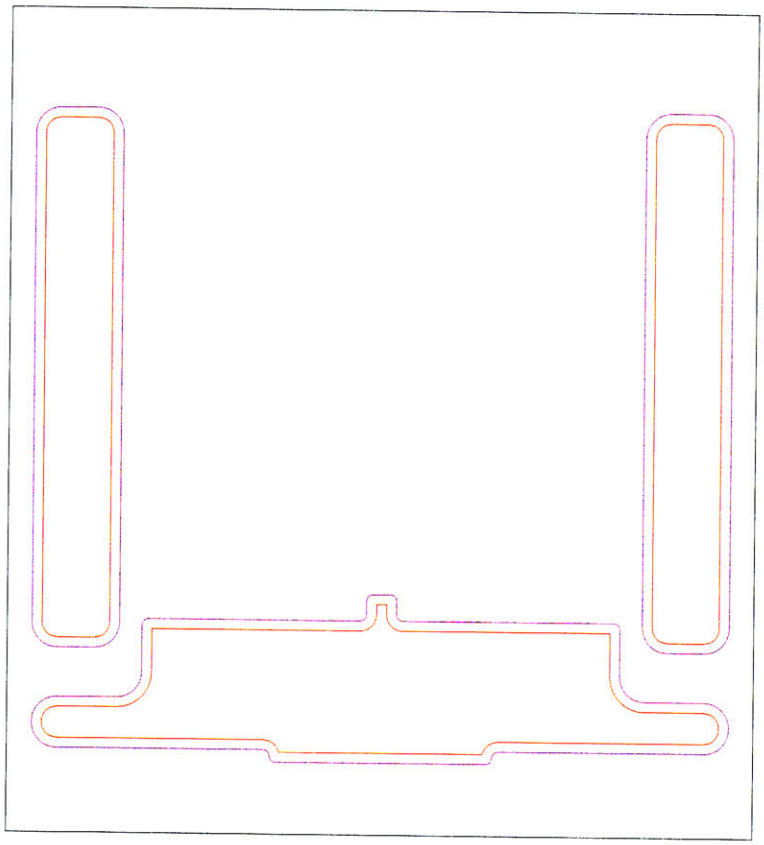


Figure B-12: Mask K: Au shadow wafer, wafer top

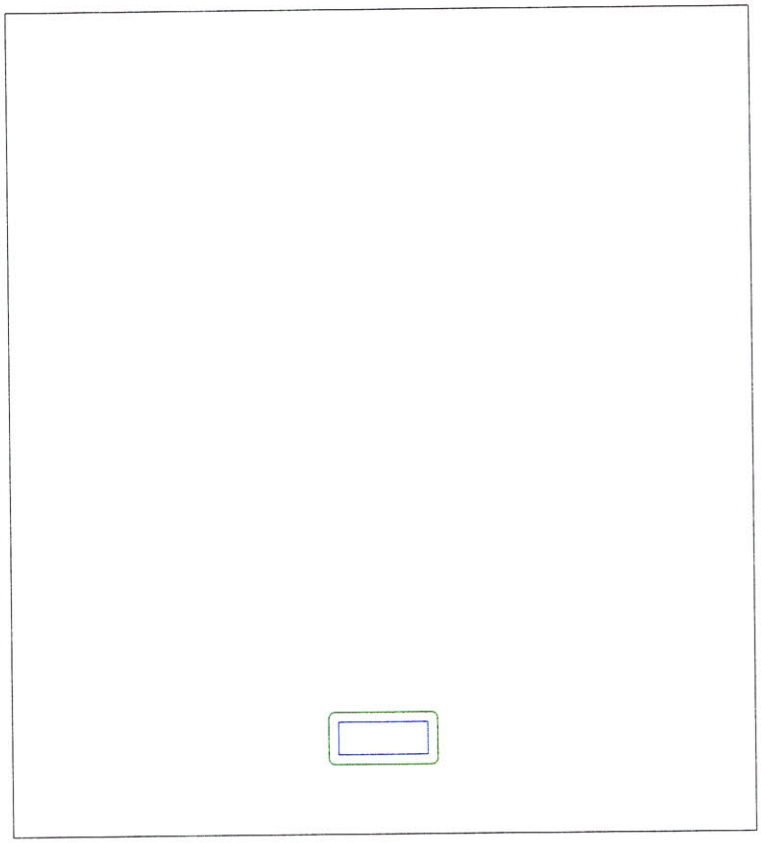


Figure B-13: Mask L: Au shadow wafer, wafer bottom

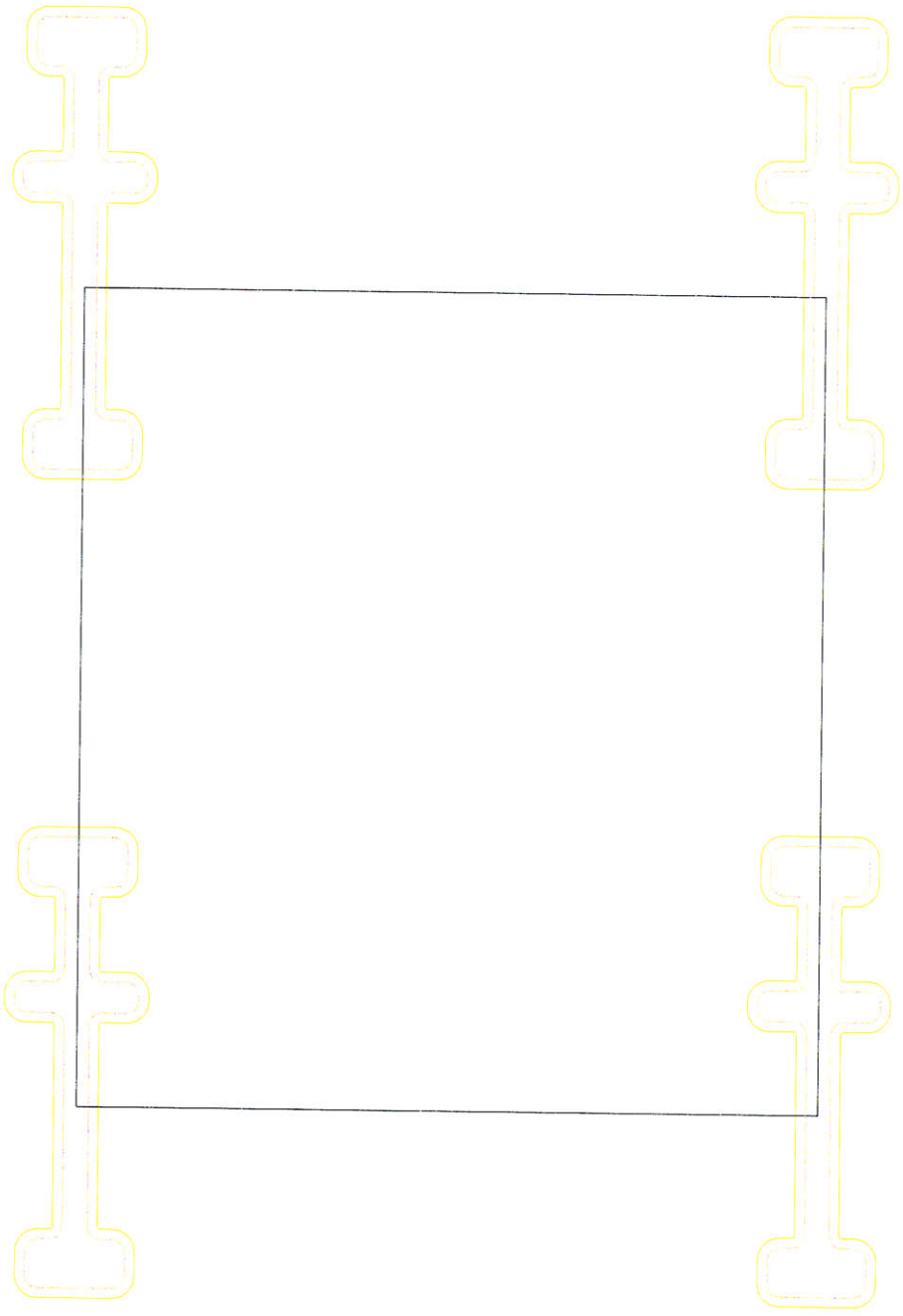


Figure B-14: Mask M: Au shadow wafer, "jumper wires". This mask interconnects all the thin film metal static contacts for electroplating

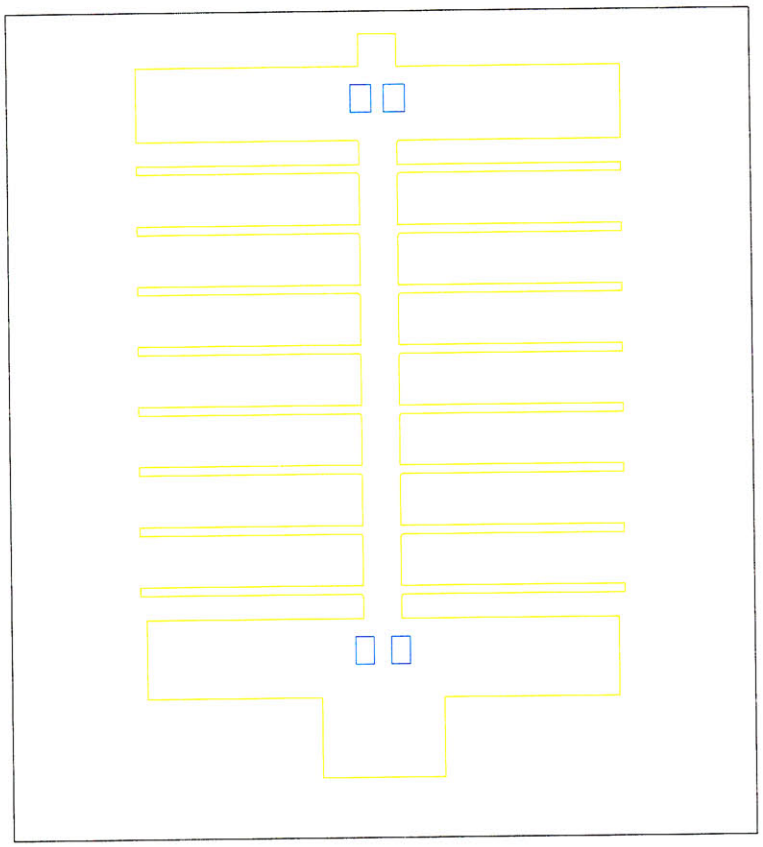


Figure B-15: Mask N: Handle wafer

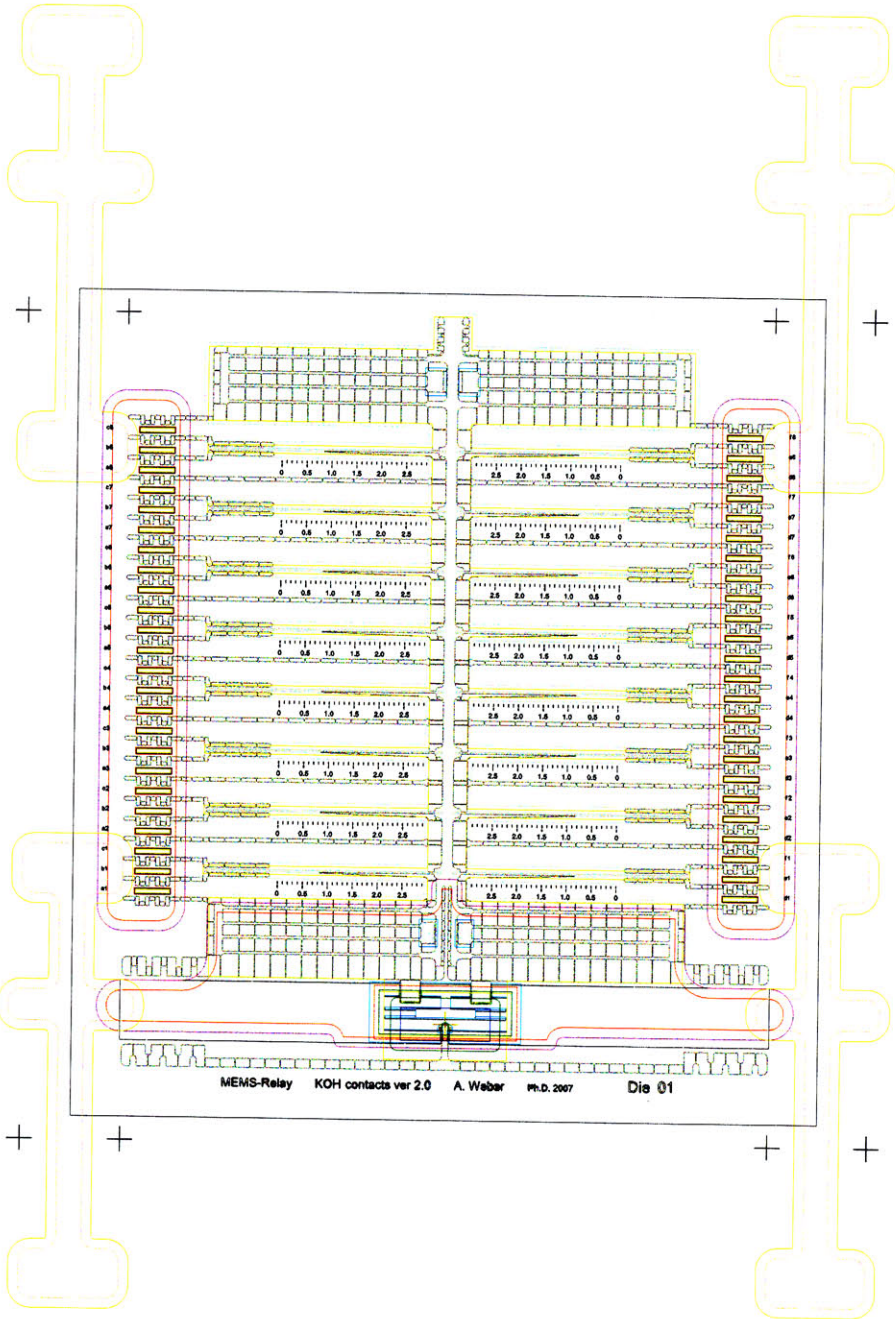


Figure B-16: All masks overlaid - die level

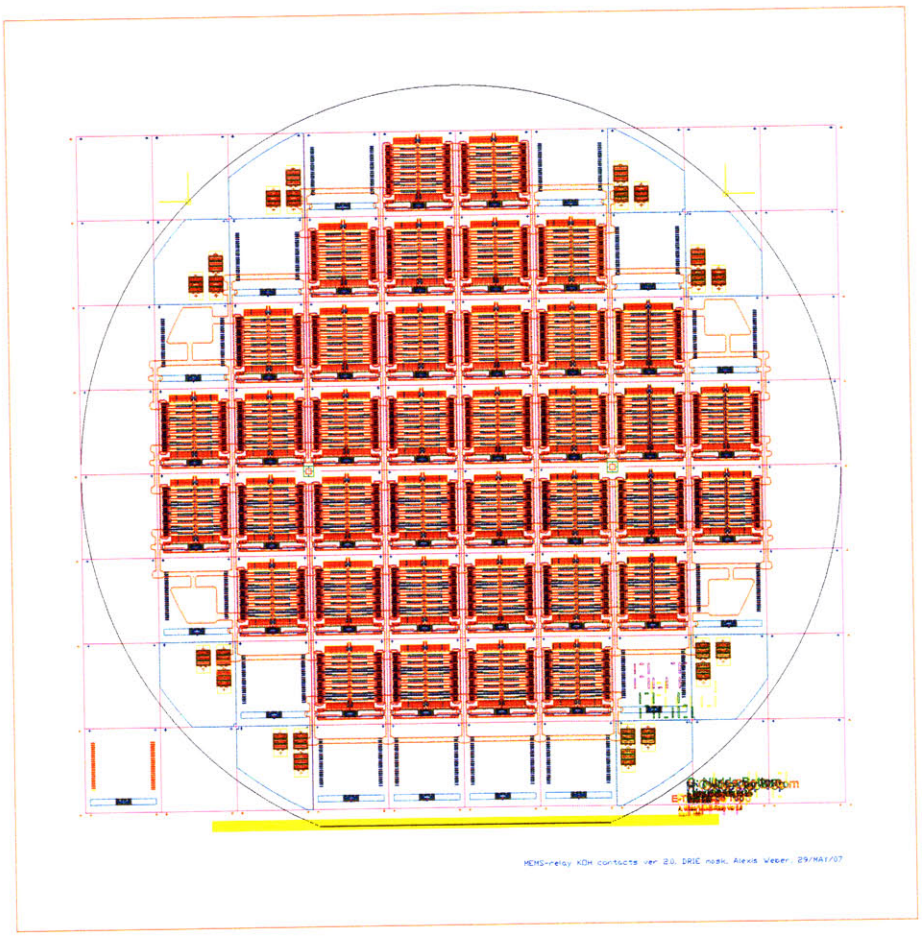


Figure B-17: All masks overlaid - wafer level

Appendix C

LabView code

The LabView virtual instrument used for data acquisition of *MEMS-relay 2* is presented next.

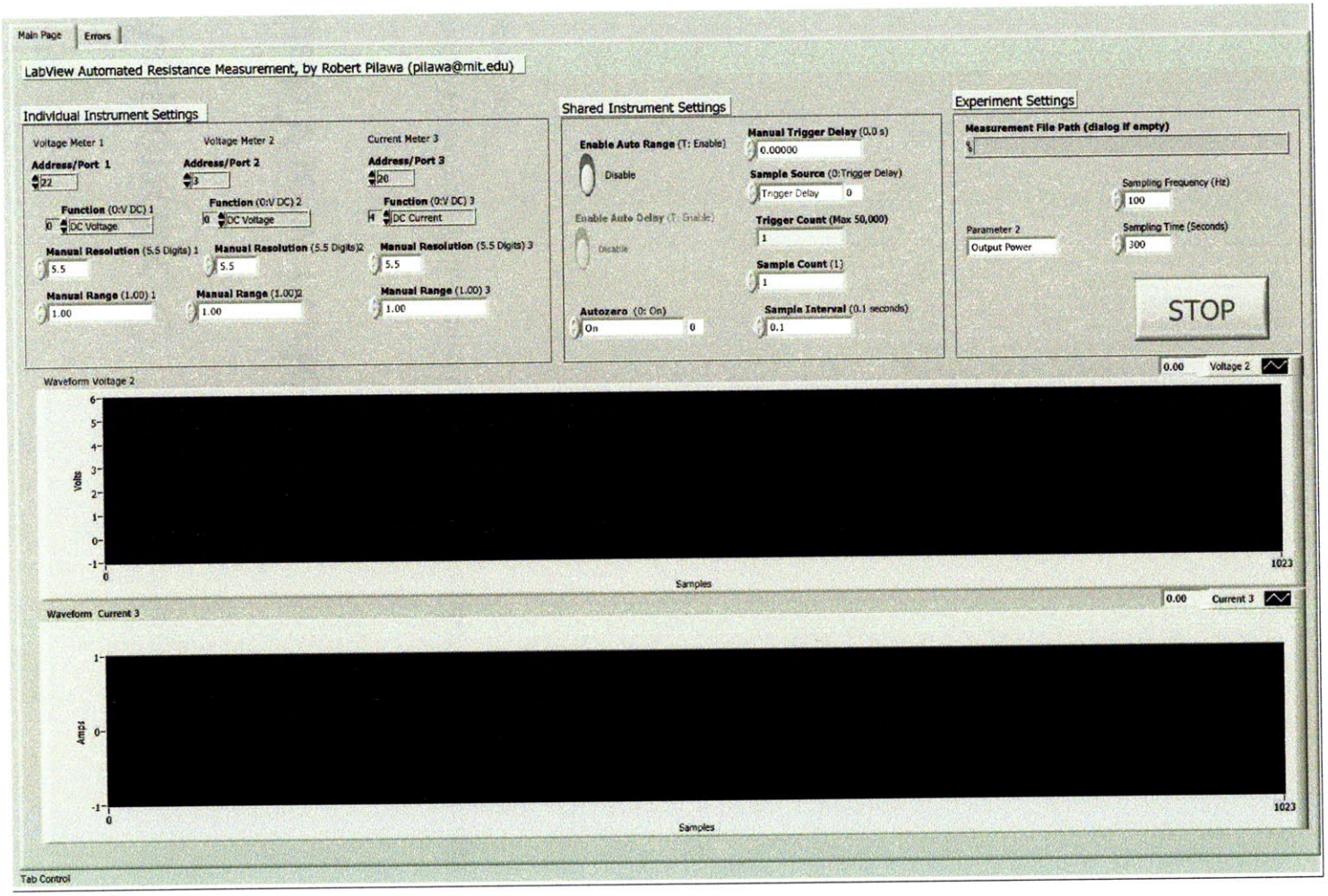


Figure C-1: LabView code, front panel

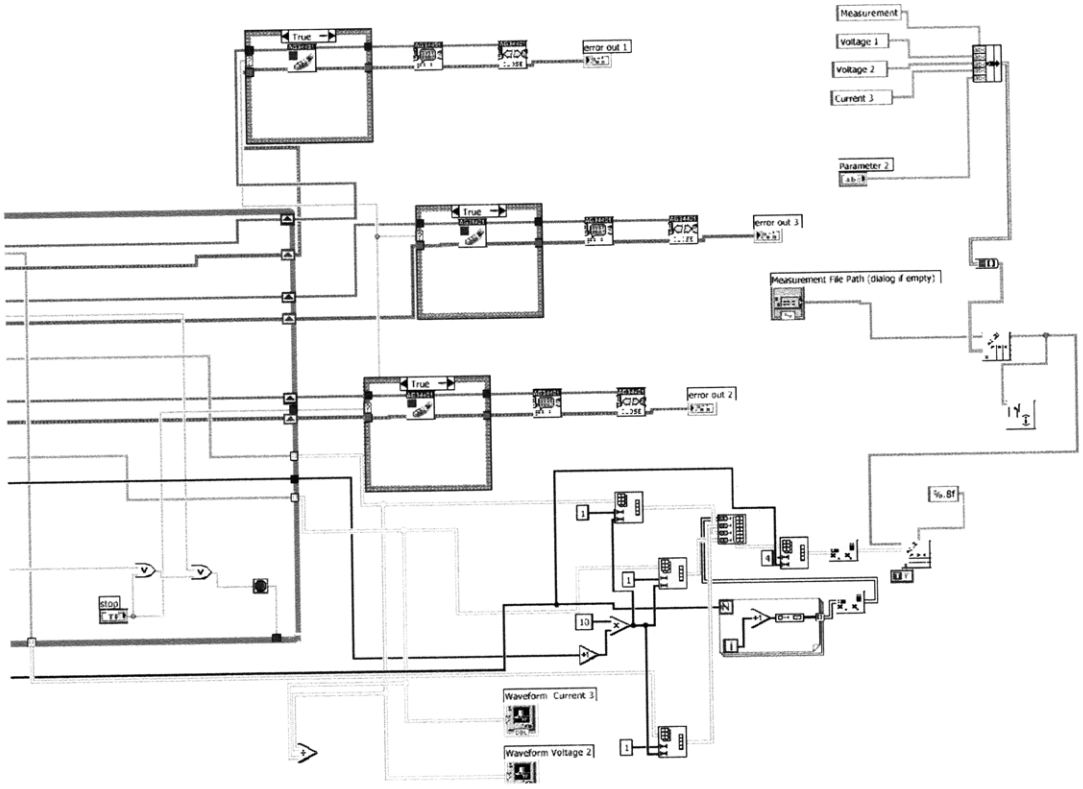


Figure C-3: LabView code, wiring diagram 2

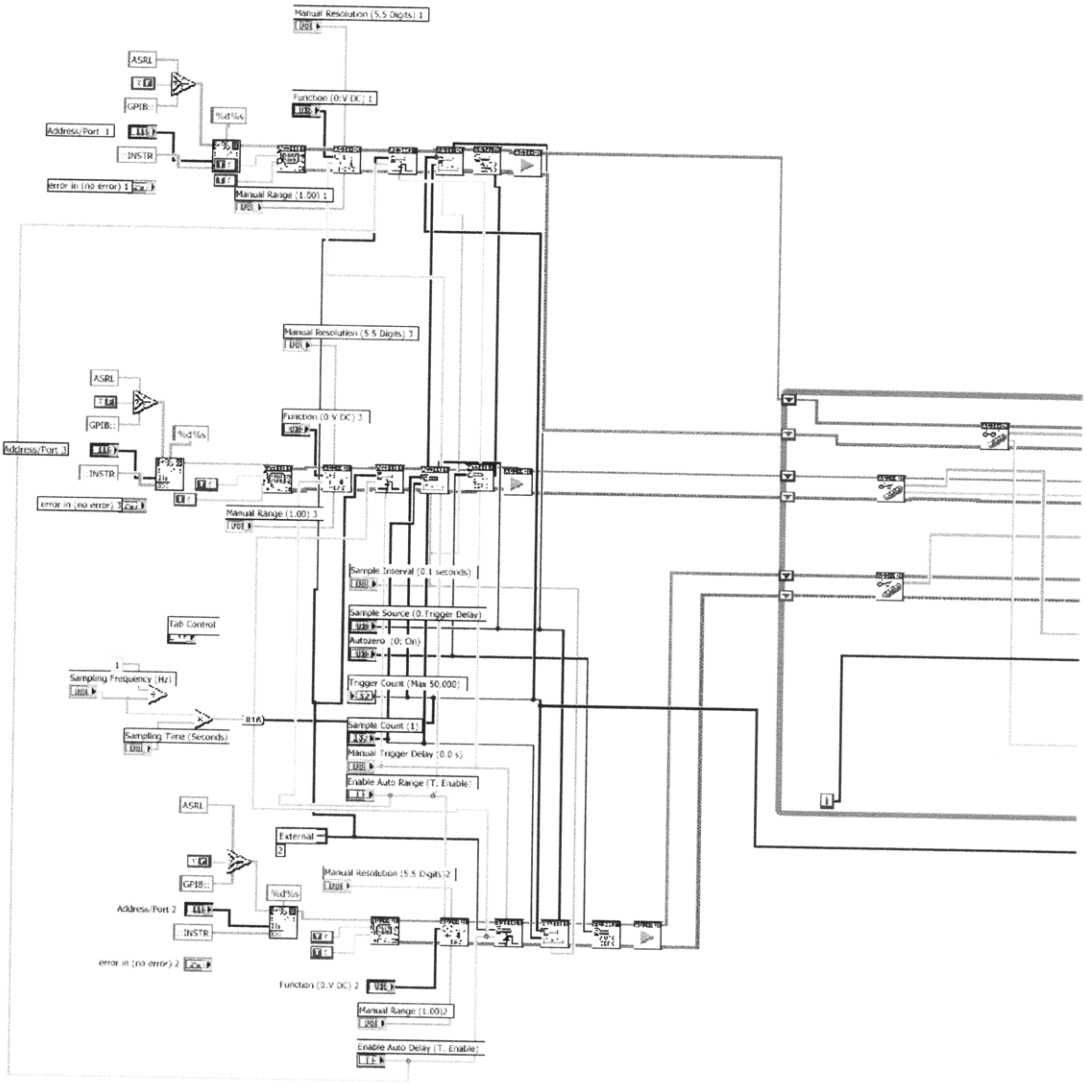


Figure C-2: LabView code, wiring diagram 1

Bibliography

[1] Rika dehnsi america inc., 2008.

[2] S. Awtar. *Synthesis and Analysis of Parallel Kinematic XY Flexure Mechanisms.* PhD thesis, Massachusetts Institute of Technology, 2004.

[3] FP Bowden and D Tabor. *Friction and lubrication of solids, Vol. II.* Oxford University Press, 1964.

[4] M. Braunovic. *Electrical contacts: fundamentals, applications and technology.* CRC Press, 2007.

[5] C. Cabuz, E. I. Cabuz, T. R. Ohnstein, J. Neus, and R. Maboudian. Factors enhancing the reliability of touch-mode electrostatic actuators. *Sensors and Actuators a-Physical*, 79(3):245–250, 2000.

[6] S.A. Campbell. *The Science and Engineering of Microelectronic Fabrication.* Oxford University Press, 1996.

[7] H. S. Carslaw and J.C. Jaeger. *Conduction of heat in solids.* Oxford University Press, 1959.

[8] P. H. Chen, H. Y. Peng, C. M. Hsieh, and M. K. Chyu. The characteristic behavior of tmah water solution for anisotropic etching on both silicon substrate and sio2 layer. *Sensors and Actuators a-Physical*, 93(2):132–137, 2001.

[9] Y. S. Chiu, K. S. Chang, R. W. Johnstone, and M. Parameswaran. Fuse-tethers in mems. *Journal of Micromechanics and Microengineering*, 16(3):480–486, 2006.

[10] L. L. W. Chow, J. L. Volakis, K. Saitou, and K. Kurabayashi. Lifetime extension of rf mems direct contact switches in hot switching operations by ball grid array dimple design. *Ieee Electron Device Letters*, 28(6):479–481, 2007.

[11] H. Y. Chu and W. L. Fang. A vertical convex corner compensation and non 111 crystal planes protection for wet anisotropic bulk micromachining process. *Journal of Micromechanics and Microengineering*, 14(6):806–813, 2004.

[12] R. A. Coutu, P. E. Kladitis, K. D. Leedy, and R. L. Crane. Selecting metal alloy electric contact materials for mems switches. *Journal of Micromechanics and Microengineering*, 14(8):1157–1164, 2004.

[13] D. A. Czaplewski, C. W. Dyck, H. Sumali, J. E. Massad, J. D. Kuppers, I. Reines, W. D. Cowan, and C. P. Tigges. A soft-landing waveform for actuation of a single-pole single-throw ohmic rf mems switch. *Journal of Microelectromechanical Systems*, 15(6):1586–1594, 2006.

[14] R. Divan, N. Moldoven, and H. Camon. Roughening and smoothing dynamics during koh silicon etching. *Sensors and Actuators a-Physical*, 74(1-3):18–23, 1999.

[15] GT Dyos and T. Farrell. *Electrical Resistivity Handbook*. Peter Peregrinus Ltd., London, UK, 1992.

[16] JD Gelorme. Photoresist composition and printed circuit boards and packages made therewith, 1989.

[17] J.A. Greenwood and JBP Williamson. Contact of nominally flat surfaces. *Proc. Roy. Soc. A*, (A 295:300), 1966.

[18] A. Hein, S. Finkbeiner, J. Marek, and E. Obermeier. The effects of thermal treatment on the anisotropic etching behavior of cz- and fz-silicon. *Sensors and Actuators a-Physical*, 86(1-2):86–90, 2000.

[19] R Holm. *Electrical Contacts Theory and Application.* Springer-Verlag, Berlin, Germany, 4th edition, 1976.

[20] H. Hosaka, H. Kuwano, and K. Yanagisawa. Electromagnetic microrelays - concepts and fundamental characteristics. *Sensors and Actuators a-Physical*, 40(1):41–47, 1994.

[21] D. Hyman and M. Mehregany. Contact physics of gold microcontacts for mems switches. *Ieee Transactions on Components and Packaging Technologies*, 22(3):357–364, 1999. Times Cited: 54.

[22] F.P. Incropera. *Fundamentals of heat and mass transfer.* John Wiley & Sons, 1996.

[23] J.H. Jerman. Micromachining process for making perfect exterior corner in an etchable substrate, 1994.

[24] W. Johler. Ruthenium and tungsten as contact materials in hermetically plastic sealed telecom- and signal-relays. *Ieee Transactions on Components and Packaging Technologies*, 27(1):19–29, 2004.

[25] W Johler. The design challenges involved in miniaturization of electromechnaical relays. In *52nd. IEEE Holm Conference on Electrical Contacts 2006, Morton Antler Lecture*, Montreal, Canada, 2006. IEEE.

[26] K.L. Johnson. *Contact Mechanics.* Cambridge University Press, 1985.

[27] J. Koshy. The resistivity and temperature-coefficient of resistivity of polycrystalline rhodium thin-films. *Journal of Physics D-Applied Physics*, 13(7):1339–1342, 1980.

[28] J. W. Kwon and E. S. Kim. Multi-level microfluidic channel routing with protected convex corners. *Sensors and Actuators a-Physical*, 97-8:729–733, 2002.

[29] H. Lee, R. A. Coutu, S. Mall, and K. D. Leddy. Characterization of metal and metal alloy films as contact materials in mems switches. *Journal of Micromechanics and Microengineering*, 16(3):557–563, 2006.

[30] H. S. Lee, C. H. Leung, J. Shi, and S. C. Chang. Electrostatically actuated copper-blade microrelays. *Sensors and Actuators a-Physical*, 100(1):105–113, 2002.

[31] S. D. Lee, B. C. Jun, S. D. Kim, H. C. Park, J. K. Rhee, and K. Mizuno. An rf-mems switch with low-actuation voltage and high reliability. *Journal of Microelectromechanical Systems*, 15(6):1605–1611, 2006.

[32] J. Li, M. P. Brenner, T. Christen, M. S. Kotilainen, J. H. Lang, and A. H. Slocum. Deep-reactive ion-etched compliant starting zone electrostatic zipping actuators. *Journal of Microelectromechanical Systems*, 14(6):1283–1297, 2005.

[33] Jian Li. *Electrostatic Zipping Actuators and Their Applications to MEMS.* PhD thesis, Massachusetts Institute of Technology, 2004.

[34] AEH Love. *A Treatise on the Mathematical Theory of Elasticity.* at the University Press, 1906.

[35] A. Mehra, X. Zhang, A. A. Ayon, I. A. Waitz, and M. A. Schmidt. Through-wafer electrical interconnect for multilevel microelectromechanical system devices. *Journal of Vacuum Science and Technology B*, 18(5):2583–2589, 2000.

[36] R. v. Mises. On saint venant's principle. *Bulletin of the American Mathematical Society*, 51-8:555–562, 1945.

[37] Milton Ohring. *The Materials Science of Thin Films.* Academic Press, 1992 edition, 1992.

[38] P. Pal, K. Sato, and S. Chandra. Fabrication techniques of convex corners in a (100)-silicon wafer using bulk micromachining: a review. *Journal of Micromechanics and Microengineering*, 17(10):R111–R133, 2007.

[39] S. T. Patton and J. S. Zabinski. Fundamental studies of au contacts in mems rf switches. *Tribology Letters*, 18(2):215–230, 2005.

[40] K. E. Petersen. Micromechanical membrane switches on silicon. *IBM J. Res. Develop.*, 23(4):376–385, 1979.

[41] J. Qiu, J. H. Lang, and A. H. Slocum. A curved-beam bistable mechanism. *Journal of Microelectromechanical Systems*, 13(2):137–146, 2004.

[42] J. Qiu, J. H. Lang, A. H. Slocum, and A. C. Weber. A bulk-micromachined bistable relay with u-shaped thermal actuators. *Journal of Microelectromechanical Systems*, 14(5):1099–1109, 2005.

[43] G.M. Rebeiz. *RF MEMS theory, design and technology.* John Wiley and Sons, 2003.

[44] X. Rottenberg, S. Brebels, P. Ekkels, P. Czarnecki, P. Nolmans, R. P. Mertens, B. Nauwelaers, R. Puers, I. DeWolf, W. De Raedt, and H. A. C. Tilmans. An electrostatic fringing-field actuator (effa): application towards a low-complexity thin-film rf-mems technology. *Journal of Micromechanics and Microengineering*, 17(7):S204–S210, 2007.

[45] X. Rottenberg, I. De Wolf, Bkjc Nauwelaers, W. De Raedt, and H. A. C. Tilmans. Analytical model of the dc actuation of electrostatic mems devices with distributed dielectric charging and nonplanar electrodes. *Journal of Microelectromechanical Systems*, 16(5):1243–1253, 2007.

[46] J. Schimkat. Contact materials for microrelays. In *11th International Conference on Microelectromechanical Systems*, pages 190–194, Heidelberg, Germany, 1998.

[47] J. Schimkat. Contact measurements providing basic design data for microrelay actuators. *Sensors and Actuators a-Physical*, 73(1-2):138–143, 1999.

[48] M. A. Schmidt. Personal communication, 07 2007.

[49] SD Senturia. *Microsystem Design.* Kluwer Academic Publishers, 2000.

[50] Kim S.G. Shi, Y. A lateral, self cleaning, direct contact mems switch. In *18th. IEEE Conference on MEMS*, pages 195–198, Miami, FL, 2005.

[51] P. G. Slade. *Electrical Contacts: Principles and Applications.* Marcel Dekker, 1999.

[52] P. G. Slade and E. D. Taylor. Electrical breakdown in atmospheric air between closely spaced (0.2 mu m-40 mu m) electrical contacts. *Ieee Transactions on Components and Packaging Technologies*, 25(3):390–396, 2002.

[53] A. H. Slocum. *Precision Machine Design.* Prentice Hall, 1992.

[54] A. H. Slocum and A. C. Weber. Precision passive mechanical alignment of wafers. *Journal of Microelectromechanical Systems*, 12(6):826–834, 2003.

[55] S.T. Smith. *Flexures: elements of elastic mechanisms.* Gordon and Breach Science Publishers, 2000.

[56] W. P. Taylor, O. Brand, and M. G. Allen. Fully integrated magnetically actuated micromachined relays. *Journal of Microelectromechanical Systems*, 7(2):181–191, 1998.

[57] C. V. Thompson. Structure evolution during processing of polycrystalline films. *Annual Review of Materials Science*, 30:159–190, 2000.

[58] C. V. Thompson. Material selection for mems; 2.373 mit lecture notes, 2003.

[59] R. S. Timsit. Electrical contact resistance: Properties of stationary interfaces. *Ieee Transactions on Components and Packaging Technologies*, 22(1):85–98, 1999.

[60] R. S. Timsit. Electrical conduction through small contact spots. *Ieee Transactions on Components and Packaging Technologies*, 29(4):727–734, 2006.

[61] J. Tripp. Hertzian contact in two and three diemensions. *NASA Tech. paper 2473*, 1985.

[62] J. Tsaur, C. H. Du, and C. Lee. Investigation of tmah for front-side bulk micromachining process from manufacturing aspect. *Sensors and Actuators a-Physical*, 92(1-3):375–383, 2001.

[63] V. A. Vertogradskii. The correlation between temperature dependence of electrical resistance, resistivity, and thermal conductivity of metals. *Journal of Engineering Physics and Thermophysics*, 27(4):1212–1215, 1974.

[64] J. Voldman. *A microfabricated dielectrophoretic trapping array for cell-based biological assays.* PhD thesis, MIT, 2001.

[65] A. C. Weber. 111 si etched elecrtical contacts for power mems-relays. In *The 53rd. IEEE Holm Conference on Electrical Contacts*, pages 156–159, Pittsburgh PA, 2007. IEEE.

[66] G. Wexler. The size effect and the non-local boltzmann transport equation in orifice and disk geometry. *Proc. Phys. Soc.*, 89:927, 1966.

[67] K. R. Williams, K. Gupta, and M. Wasilik. Etch rates for micromachining processing - part ii. *Journal of Microelectromechanical Systems*, 12(6):761–778, 2003.

[68] K.R. Williams. Silicon wet orientation-dependent (anisotropic) etch rates. In Robert Hull, editor, *Properties of Crystalline Silicon*, pages 815–824. IET, 1999.

[69] J.A. Wright and Y.C. Tai. Magnetostatic mems relays for the miniaturization of brishless dc motor controllers. In *12th. IEEE International Conference on Microelectromechanical Systems*, pages 954–959, 1999.

[70] J. J. Yao. Rf mems from a device perspective. *Journal of Micromechanics and Microengineering*, 10(4):R9–R38, 2000.

[71] Markus Zahn. Solid, liquid, and gaseous electrical insulation. In *Encyclopedia of Applied Physics*, volume 18, pages 431–466. VCH, 1997.

[72] P. M. Zavracky, S. Majumder, and N. E. McGruer. Micromechanical switches fabricated using nickel surface micromachining. *Journal of Microelectromechanical Systems*, 6(1):3–9, 1997.