An Organic Thin-film Transistor Circuit for Large-area Temperature-sensing

by

David Da He

B.A.Sc. Electrical Engineering
University of Toronto, 2005

Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degree of

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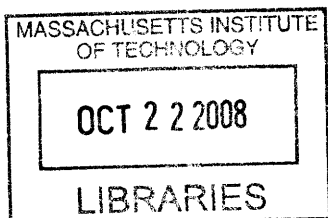at the

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Author . . . .
Department of Electrical Engineering and Computer Science
July 29, 2008

Certified by . . . .
Charles G. Sodini
Professor of Electrical Engineering
Thesis Supervisor

Accepted by . . . .
Terry P. Orlando
Chairman, Department Committee on Graduate Students

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Abstract

This thesis explores the application of organic thin-film transistors (OTFTs) for temperature-sensing. The goal of this work is twofold: the understanding of the OTFT's electrical characteristics' temperature dependence, and the creation of OTFT temperature-sensing circuits. We find that OTFTs have temperature-dependent current-voltage (I-V) characteristics that are determined by trap states inside the bandgap. Based on this understanding, a DC OTFT circuit model is developed which accurately fits the measured I-V data in all regions of device operation and at different temperatures. Using this model, we design and fabricate two OTFT temperature-sensing circuits. The first circuit achieves a responsivity of $22mV/^{\circ}C$ with $12nW$ of power dissipation, but has a nonlinear temperature response that is dependent on threshold voltage shifts. The second circuit achieves a responsivity of $5.9mV/^{\circ}C$ with $88nW$ of power dissipation, and has a highly linear temperature response that is tolerant of threshold voltage shifts. Both circuits exceed silicon temperature sensors' typical temperature responsivity of $0.5 - 4mV/^{\circ}C$ while dissipating less power. These traits, along with the OTFT's ability to be fabricated on large-area and flexible substrates, allow OTFT temperature sensors to be used in both existing and new application environments.

Thesis Supervisor: Charles G. Sodini
Title: Professor of Electrical Engineering

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Contents

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Chapter 1

Introduction

The organic thin-film transistor (OTFT) is a field-effect transistor technology that uses an organic material as the semiconductor.

Recently, OTFTs have generated much research and commercial interest because of their electronic and mechanical properties. Electronically, OTFTs have field-effect mobilities and on/off current ratios that are comparable to those of hydrogenated amorphous silicon (a-Si:H) TFTs [1]. Mechanically, because organic molecules interact by weak Van der Waals forces, they have low melting temperatures and can be soluble at room temperature [2]. The possibility of low temperature processing allows inexpensive methods such as inkjet and roll-to-roll processing, and permits substrates that are low-cost and mechanically flexible [3].

As a result, the target applications for OTFTs are large-area and mechanically flexible electronics. Such applications include display backplanes, imagers, photovoltaics, radio frequency identification tags, and transparent electronics [3, 4].

This thesis explores the novel application of OTFTs for temperature-sensing. The goal of this work is to understand the OTFT's temperature characteristics and to create OTFT temperature-sensing circuits. Traditionally, several technologies have been used for temperature-sensing:

- Silicon BJT and MOSFET integrated temperature sensors use the ΔV_{BE} principle [5–9] or the ΔV_T principle [10, 11] to create proportional-to-absolute-

temperature (PTAT) circuits. These silicon PTAT circuits typically offer a temperature responsivity of 0.5 to $4mV/°C$ [10], consume tens of nano-watts to tens of micro-watts of power [11–13], and are used for temperatures lower than $150°C$ [14].

- Resistance temperature detectors (RTDs) use metal's electrical resistance's characterized temperature dependence to sense temperature [15]. RTDs typically offer $0.1°C$ of resolution [16], consume micro-watts of power [17], and can operate at temperatures up to $600°C$ [18].

- Thermocouples measure the temperature-dependent voltage difference between two metals according to the Seebeck Effect [19]. Thermocouples typically offer tens to hundreds of $\mu V/°C$ of responsivity [20, 21], use no external power, and can operate at temperatures up to $1,200°C$ [22].

The most obvious advantage of an OTFT temperature-sensing circuit over the above technologies is the OTFT's ability to be fabricated on large-area and flexible substrates. However, it will also be shown that the OTFT's temperature characteristics allow OTFT temperature-sensing circuits to exceed the above technologies' temperature responsivities while dissipating nano-watts of power. Two such OTFT circuits will be presented. The first circuit has the greater temperature responsivity, while the second circuit achieves high linearity with temperature while compensating for common-mode threshold voltage shifts.

This thesis begins by describing the OTFT's device structure, electrical characteristics, and temperature characteristics in Chapter 2. From these characteristics and using device physics, a unified DC OTFT circuit model is developed in Chapter 3. This model is used for the temperature-sensing circuit design in Chapter 4, where the two temperature-sensing circuits are presented with measured results.

Chapter 2

The Organic Thin-film Transistor

This chapter is divided into three sections. The first section treats the OTFT from a device perspective. The second section treats the OTFT as a circuit element by presenting its electrical characteristics. The third section discusses the OTFT's temperature characteristics.

2.1 Device Description

This section describes the OTFT from a device perspective, starting from the device materials, to the fabrication process, and finally to the basic operating principle.

2.1.1 Device Materials

The OTFT uses pentacene as the semiconductor, parylene-C as the gate dielectric, and gold as the gate and source-drain metal. The transistor is classified as thin-film because pentacene and parylene are deposited as thin-films.

Pentacene is chosen as the semiconductor material because of its relatively high charge mobility of approximately 1.0 cm^2/Vs [1]. Chemically, pentacene is a hydrocarbon consisting of five fused benzene rings ($C_{22}H_{14}$), as shown in Figure 2-1.
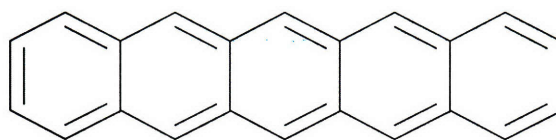
Figure 2-1: Pentacene, $C_{22}H_{14}$.

Data type	Height
Z range	50.00 nm
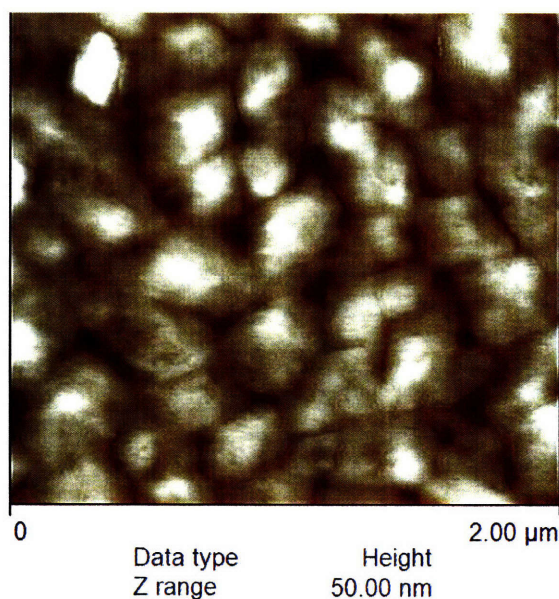
Figure 2-2: Atomic force microscopy (AFM) image of the amorphous pentacene film used in this work as deposited on parylene (image by permission, Sung Gap Im, MIT).

The pentacene films used in this work are amorphous, as seen in Figure 2-2. Charge transport is typically modeled by hopping between localized trap states, which represents the movement of charges in the overlapped π-orbitals between molecules. Charge transport in pentacene consists of holes, thus making pentacene a p-type semiconductor. The low electron mobility means that pentacene conducts only by hole accumulation, not by electron inversion.

Parylene-C is used for both the gate dielectric and the encapsulation material. Chemically, parylene-C consists of a chlorine atom attached to a benzene ring (C_8H_8Cl), as shown in Figure 2-3.

Cl

$-(CH_2 - \quad - CH_2)_n$
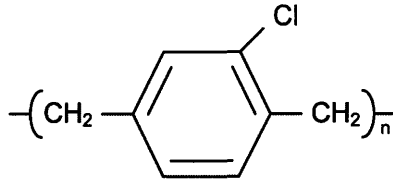
Figure 2-3: Parylene-C, C_8H_8Cl.

Parylene-C is chosen for the following reasons:

- It is chemically compatible with pentacene.

- It can be deposited at room temperature as a conformal and smooth thin-film.

- Its high electrical insulation (1015 Ωcm) and high dielectric strength (2.7 MV/cm) make it an excellent dielectric material (dielectric constant of 3.10 at 1 kHz).

- Its low moisture and low gas permeability make it suitable as an encapsulation layer to protect pentacene.

Gold is used as the gate and source-drain metal because gold's high workfunction decreases the energy difference between gold's Fermi energy level and pentacene's highest occupied molecular orbital (HOMO) energy level. This leads to a lower hole injection barrier [23], which decreases contact resistance. An additional benefit of gold is that it does not oxidize in air.

2.1.2 Device Fabrication Process

The OTFTs are fabricated using a photolithographic process developed by Kymissis et al. [24]. The process flow is illustrated in Figure 2-4:
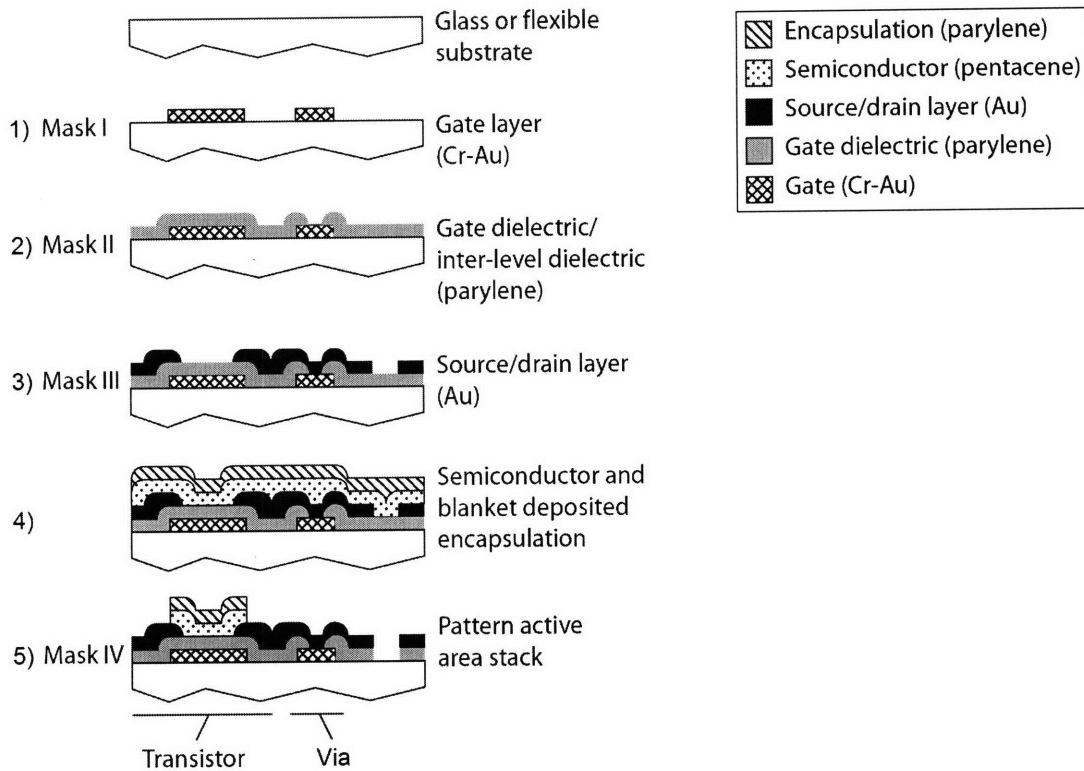
Figure 2-4: The OTFT photolithographic process flow (figure by Kymissis [24]).

Each step in Figure 2-4 is described below:

1. 100Å of Cr (to promote adhesion to the substrate) and then 600Å of Au are e-beam evaporated onto the substrate. The patterned result forms the gate layer.

2. 2000Å of parylene is deposited via chemical vapor deposition (CVD) and is subsequently patterned. This forms the gate dielectric layer.

3. 400Å of Au is e-beam evaporated onto parylene and is subsequently patterned. This forms the source-drain layer.

4. 150Å of pentacene is deposited via thermal evaporation ($\leq 95°C$), and then 2000Å of parylene is deposited via CVD as an encapsulation layer.

5. The active layer is patterned.
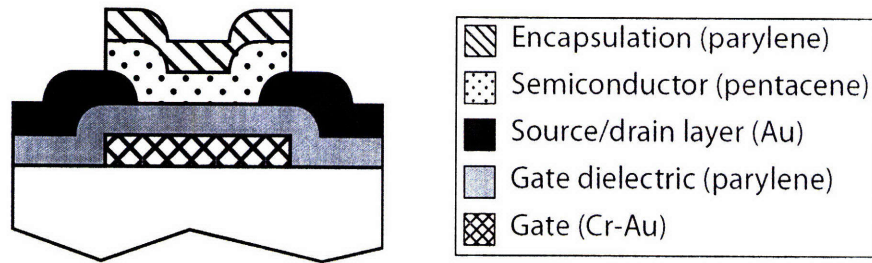
Figure 2-5: The OTFT device cross-section.
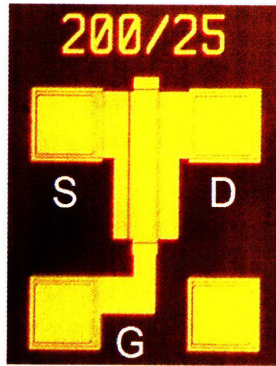
Figure 2-6: Top view of an OTFT, $200\mu m/25\mu m$.

The resulting OTFT cross-section in Figure 2-5 shows a bottom-contact inverted-staggered-gate field-effect transistor. "Bottom-contact" refers to the position of the source-drain metals relative to the pentacene. Bottom-contact OTFTs suffer from higher contact resistances [23, 25], but the pentacene is deposited after the source-drain metal is e-beam evaporated, thus avoiding damage to the pentacene. Unlike silicon MOSFETs, the OTFT structure is called "inverted" in the sense that the gate layer is underneath the semiconductor layer and the source-drain layer. Again, this arrangement is to protect the pentacene by depositing it after the metal.

In the above process, the maximum temperature is $95°C$, the minimum feature size is $3\mu m$ (limited by mask supplier), and the alignment tolerance is $1\mu m$. Figure 2-6 shows the top view of an OTFT. A completed wafer on a 4-inch glass substrate is shown in Figure 2-7.
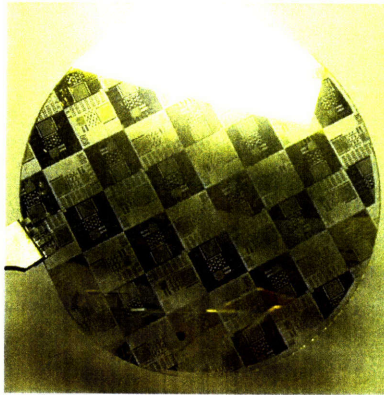
Figure 2-7: A 4-inch OTFT wafer on a glass substrate.

2.1.3   Basic Device Operation

Similar to MOSFETs, OTFTs operate by field-effect. The fabricated devices are enhancement-mode because the drain current is small under zero gate bias[1]. Under negative gate bias, holes will accumulate in the pentacene, thus forming a conductive channel between the source and the drain. When a positive source-drain voltage is applied, holes will travel through the channel by hopping between localized trap states. The device operation for a negative gate bias and a positive source-drain bias is illustrated in Figure 2-8.
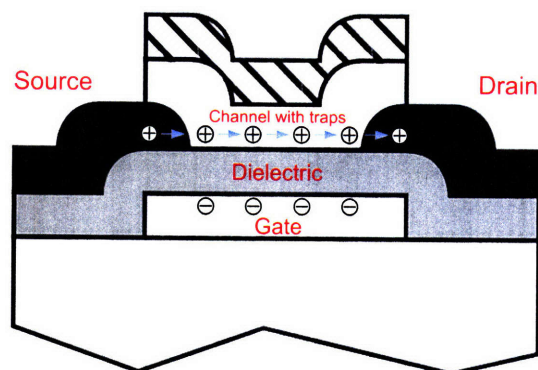
Figure 2-8: The OTFT device operation under a negative gate bias and a positive source-drain bias.

[1]Under zero gate bias, the drain current is in the subthreshold region and is typically six to seven orders of magnitude less than the on-current. See Section 2.2 for plots.

2.2 Current-voltage Characteristics

This section describes the OTFT from an electrical perspective using current-voltage (I-V) characteristics. Figure 2-9 shows the OTFT current and voltage conventions used in this work, where $V_{GS} = V_G - V_S = -V_{SG}$ and $V_{DS} = V_D - V_S = -V_{SD}$. All characteristics were measured with a Signatone S-250 probe station and an Agilent 4156C parameter analyzer. Wafer temperature was controlled by a Silicon Thermal TH170 thermal head attached to a LB320 thermal controller.
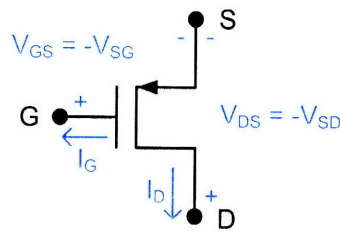
Figure 2-9: The OTFT current and voltage conventions.
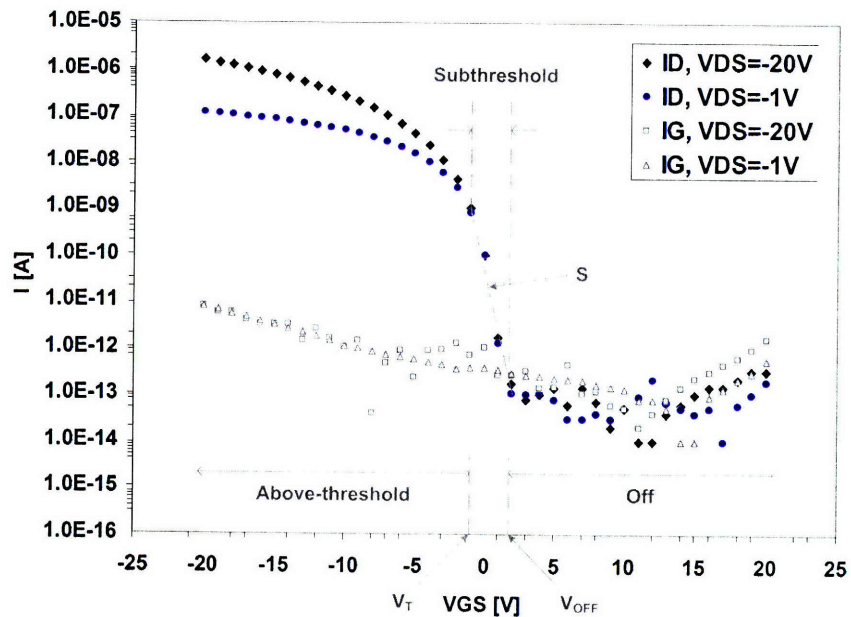
Figure 2-10: Typical OTFT transfer characteristics on a semi-log scale, $200\mu m/25\mu m$.

Figure 2-10 shows typical transfer characteristics obtained at $V_{DS} = $ -20V and -1V on a semi-log scale. From Figure 2-10, one can see three distinctive regions:

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- **Off Region**, $V_{OFF} < V_{GS}$: At V_{GS} greater than a certain voltage, the transistor is turned off. Here, I_D is dominated by the gate leakage current I_G. The lowest V_{GS} at which $I_D = I_G$ is defined[2] as the off-voltage, or V_{OFF}. We will treat I_D as effectively zero in this region.

- **Subthreshold Region**, $V_T < V_{GS} < \mathrm{V}_{OFF}$: In the subthreshold region, I_D is approximately exponentially controlled by V_{GS}. The effectiveness of V_{GS} control is quantified by the inverse subthreshold slope, S (mV of V_{GS} per decade of I_D). The V_{GS} at which I_D starts to deviates from the exponential increase is defined[3] as the threshold voltage, V_T.

- **Above-threshold Region**, $V_{GS} < V_T$: When V_{GS} is sufficiently negative, I_D ceases to increase exponentially and the transistor enters the above-threshold region.

2.2.1 Above-threshold Current-voltage Characteristics

Figure 2-11 re-plots Figure 2-10 on a linear scale. One can see that at $V_{DS} = -1V$, I_D increases in a linear relationship versus V_{GS}, whereas when $V_{DS} = -20V$, I_D increases in a power relationship versus V_{GS}.
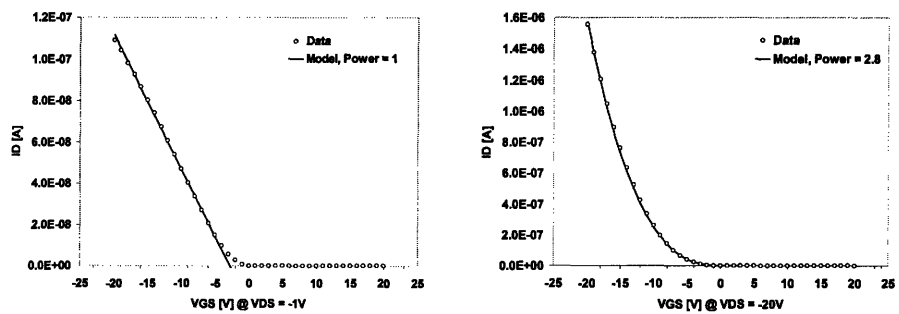
(a) $V_{DS} = -1V$. (b) $V_{DS} = -20V$.

Figure 2-11: Transfer characteristics on a linear scale, $200\mu m/25\mu m$.

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[2]This definition makes V_{OFF} dependent on I_G. However, this is a weak (logarithmic) dependence because I_G is in the subthreshold I_D range.

[3]To be physically accurate, this voltage should be named the flat-band voltage. However, "threshold" voltage is used to allow terminologies such as "subthreshold" and "above-threshold."

However, Figure 2-11(a) is misleading because, at a small V_{DS}, contact resistance has a significant effect on the drain current. We plot the transfer curves again in Figure 2-12 for a longer channel device, for which contact resistance has a proportionally smaller impact.

(a) $V_{DS} = -1V$.

(b) $V_{DS} = -20V$.
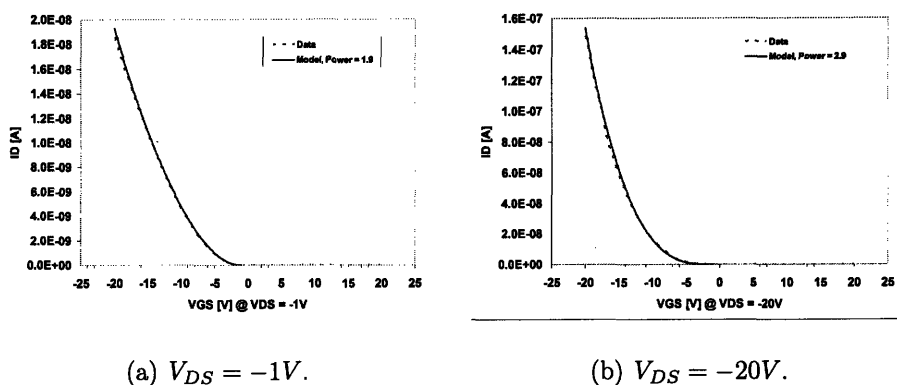
Figure 2-12: Transfer characteristics on a linear scale, $100\mu m/200\mu m$.

As shown in Figure 2-12, when contact resistance's effect is diminished, both V_{DS}'s yield power relationships versus V_{GS}. The power dependence is a consistent result for a device whose mobility increases with negative V_{GS} [25]. The power difference of "1" between low V_{DS} and high V_{DS} is consistent with a p-type transistor going from the linear region to the saturation region.

Figure 2-13 shows the output characteristics obtained at V_{GS} = -20V to 0V.
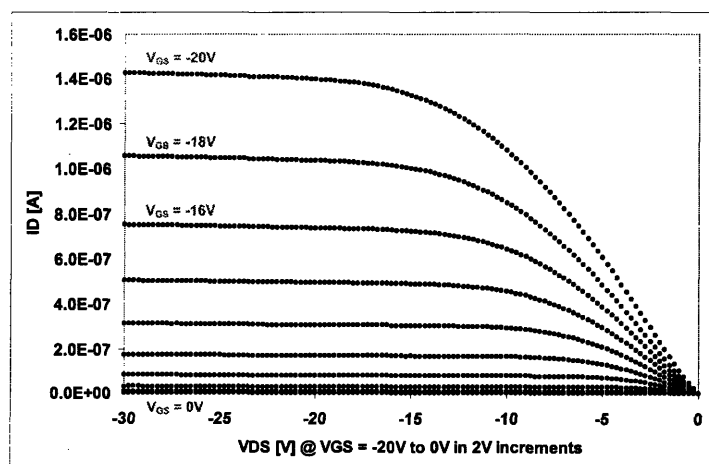
Figure 2-13: Typical OTFT output characteristics, $200\mu m/25\mu m$.

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Figure 2-13 shows that the OTFT has a linear region at small[4] V_{DS}'s and a saturation region at large V_{DS}'s. In the linear region, I_D increases linearly with V_{DS}. In the saturation region, I_D is relatively unaffected by V_{DS}.

2.2.2 Subthreshold Current-voltage Characteristics

The subthreshold region is defined by I_D's apparently exponential dependence on V_{GS}. In Figure 2-14, I_D begins to increase exponentially at $V_{GS} < V_{OFF} = 0.1V$. The exponential increase occurs with a slope of $S = 0.36V/dec$. At $V_{GS} < V_T = -0.5V$, I_D ceases to increase exponentially, and the exponential model begins to deviate from data. The subthreshold output characteristics in Figure 2-15 show that for any appreciable V_{DS}, the subthreshold I_D is saturated.
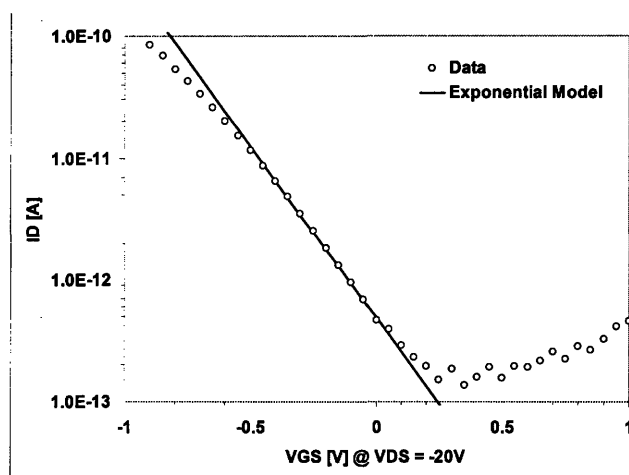
Figure 2-14: Subthreshold region transfer characteristics on a semi-log scale, $1,000\mu m/5\mu m$.

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[4]The concave curvature at V_{DS} near zero is due to contact resistance. This behavior can be modeled by a series resistor and a pair of anti-parallel Schottky diodes at the source and the drain [26].
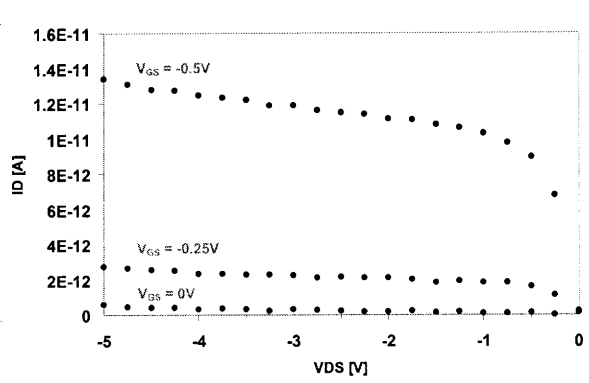
Figure 2-15: Subthreshold region output characteristics, $1,000\mu m/5\mu m$.

2.2.3 Typical Characterized Parameters

Typical characterized I-V parameters are shown in Table 2.1. The data is measured from nine wafers fabricated over the span of two years. Some parameters are normalized per micron of channel width. All characterized transistors have $5\mu m$ channel length. I_{ON} is defined as the drain current at $V_{GS} = V_T - 20V$ and at $V_{DS} = -20V$. Mobility is calculated using the method outlined by Ryu et al. [25]. V_{SHIFT} is obtained from the double-sweep capacitance-voltage (C-V) plot's voltage hysteresis, and is a rough measure of device stability under bias. $R_{CONTACT}$ is obtained by the transmission line method (TLM) [27] and is used to calculate mobility.

Parameter	Mean	Std. Dev.	Maximum	Minimum
V_T $[V]$	-0.42	0.79	1.0	-2.0
I_{ON} $[nA/\mu m]$	11	7.5	29	3.3
$Mobility$ $[cm^2/Vs]$	0.024	0.016	0.062	0.0030
S $[V/dec]$	0.71	0.32	1.5	0.34
$I_{G,leak}$ $[fA/\mu m]$	10	11	40	1.8
$I_{DS,leak}$ $[fA/\mu m]$	1.2	0.38	2.1	1.0
V_{SHIFT} $[V]$	0.18	0.16	0.40	0.10
$R_{CONTACT}$ $[M\Omega \cdot \mu m]$	6.3×10^2	3.4×10^2	1.4×10^3	82

Table 2.1: Compiled OTFT I-V parameters.

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2.3   Temperature Characteristics

So far, the OTFT's transfer and output characteristics in both subthreshold and above-threshold regions have shapes that are very similar to silicon MOSFET's. However, we observe differences once the device temperature is varied.
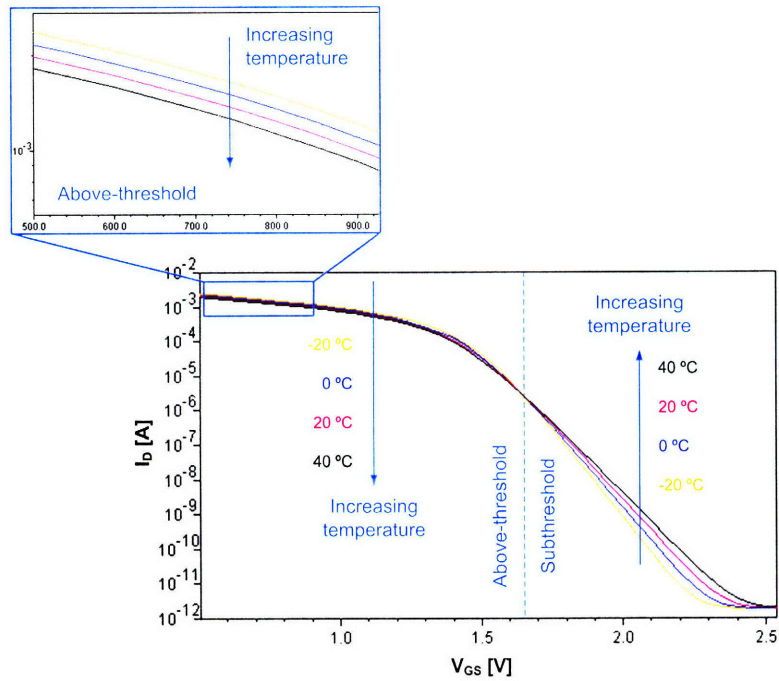
Figure 2-16: BSIM3 silicon MOSFET's temperature characteristics.
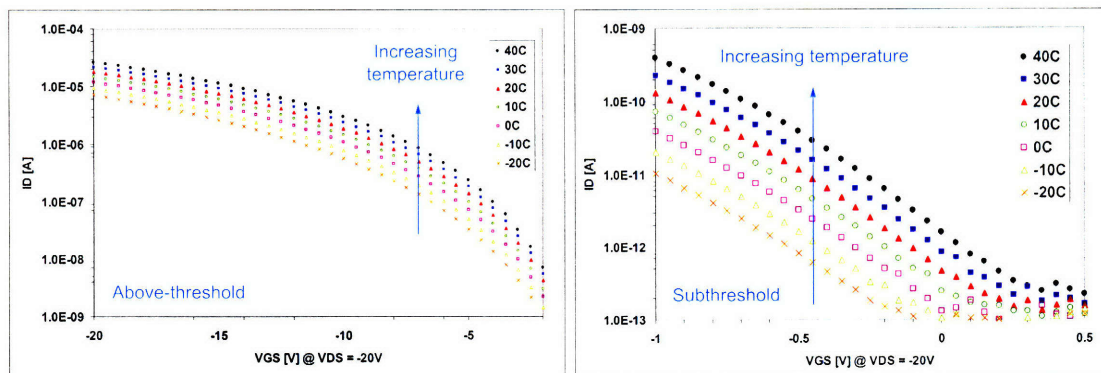
Figure 2-17: OTFT's measured temperature characteristics.

The silicon MOSFET's temperature characteristics (BSIM3 model) are shown in Figure 2-16. Two properties should be noted. First, the subthreshold current

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increases with temperature, while the above-threshold current decreases with temperature[5]. Second, the MOSFET's inverse subthreshold slope becomes softer as temperature increases. This is because $S = (nkT/q)ln(10)$ [28]. For comparison, OTFT's measured temperature characteristics are shown in Figure 2-17. Unlike MOSFETs, the OTFT's current increases with temperature in both subthreshold and above-threshold regions. Furthermore, the OTFT's S appears to be temperature independent. These observations have also been made in [29, 30].

This suggests that fundamental differences exist between the MOSFET and the OTFT. Indeed, as mentioned in Section 2.1.1, an important difference is that the MOSFET is an inversion-mode transistor, while the OTFT is an accumulation-mode transistor. Another significant difference is that pentacene contains substantial trap states in its bandgap [31, 32] whereas silicon does not. This is illustrated in Figure 2-18. The trap states will be revisited in Chapter 3 to develop the OTFT circuit model.
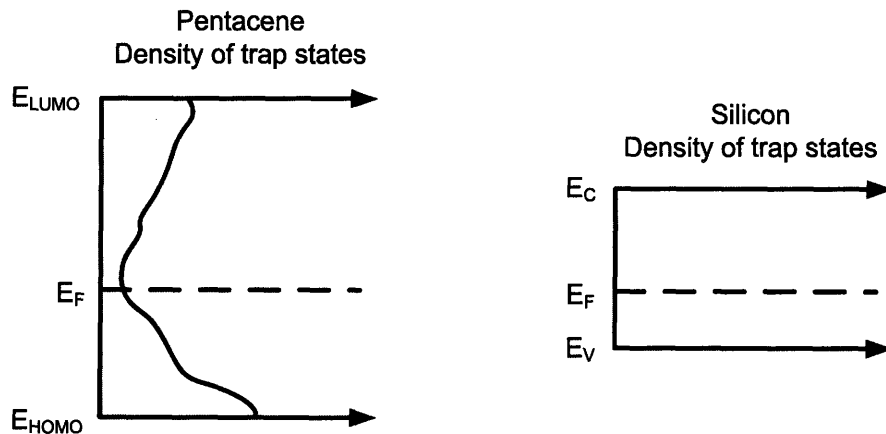
Figure 2-18: Pentacene contains substantial trap states in the bandgap, whereas silicon does not.

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[5]In the subthreshold MOSFET, the channel's carrier concentration increases exponentially with temperature. In the above-threshold MOSFET, the degradation of carrier mobility with temperature is the dominant reason behind the current decrease.

2.3.1 Above-threshold Temperature Characteristics
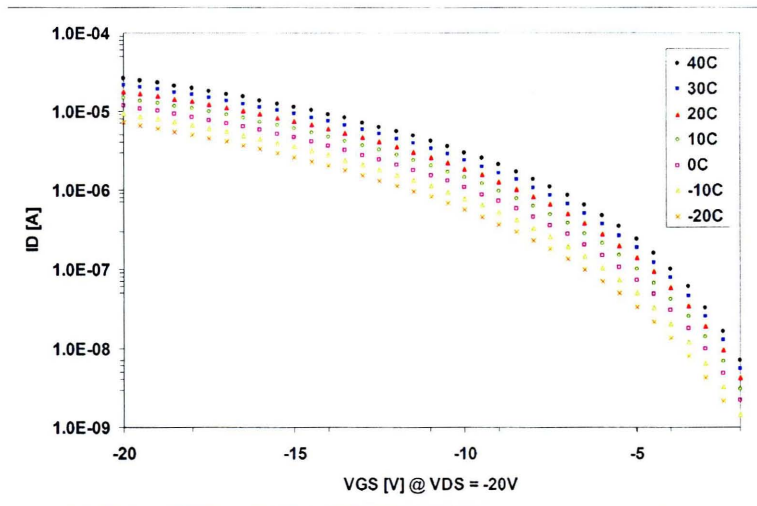
Figure 2-19: Saturation region temperature characteristics on a semi-log scale, $1,000\mu m/5\mu m$.
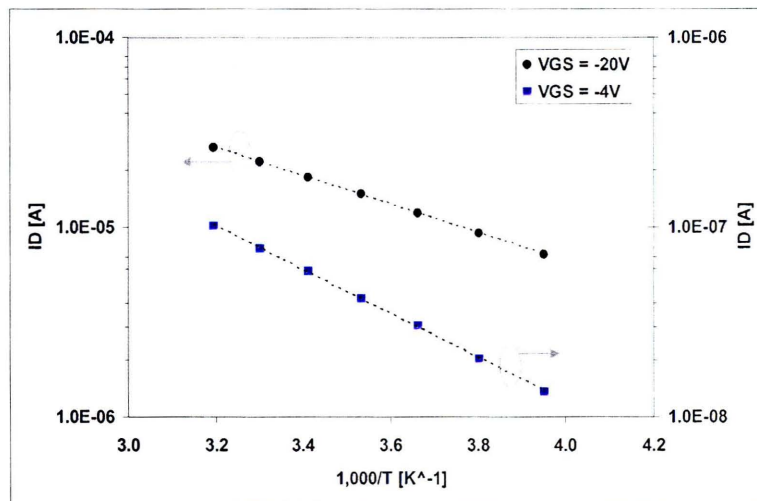
Figure 2-20: Arrhenius plot of saturation region I_D at two V_{GS}'s, $1,000\mu m/5\mu m$.

The OTFT temperature characteristics in the saturation region are shown in Figure 2-19, where one can see that the I-V shape remains similar as the temperature is varied. To investigate further, we graph an Arrhenius plot of I_D at two V_{GS}'s in Figure 2-20. Figure 2-20 shows that I_D is thermally activated. Its temperature dependence can

be modeled by $I_D \propto exp(-\alpha/T)$, where α decreases with increasingly negative V_{GS}. This is equivalent to saying that the activation energy of carriers decreases as V_{GS} becomes more negative, which implies that additional trap states are filled and the energy required for charges to reach the HOMO energy level is reduced [31, 32].

The temperature characteristics in the linear region are shown in Figure 2-21.
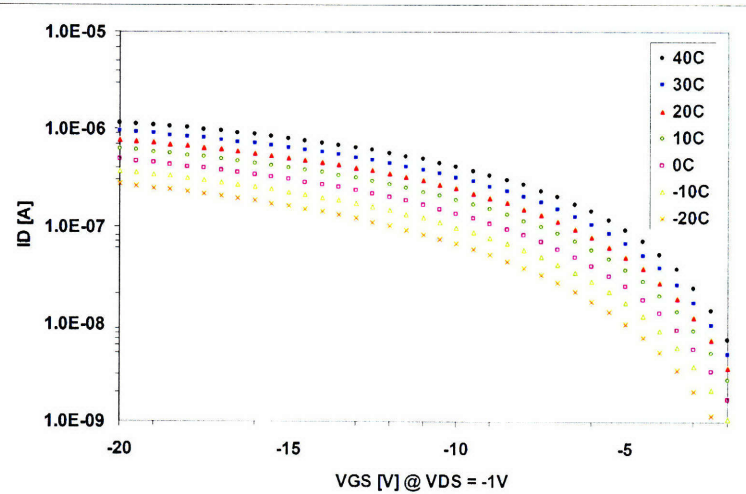
Figure 2-21: Linear region temperature characteristics on a semi-log scale, $1,000\mu m/5\mu m$.

We graph an Arrhenius plot of I_D at two V_{GS}'s.
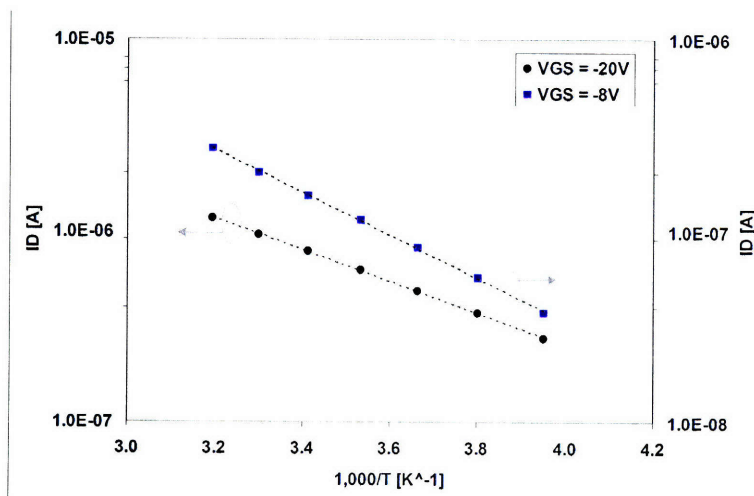
Figure 2-22: Arrhenius plot of linear region I_D at two V_{GS}'s, $1,000\mu m/5\mu m$.

Again, the Arrhenius plot shows that I_D's temperature dependence can be modeled by $I_D \propto exp(-\alpha/T)$. Also, as in the saturation region, α decreases with negative V_{GS}.

2.3.2   Subthreshold Temperature Characteristics
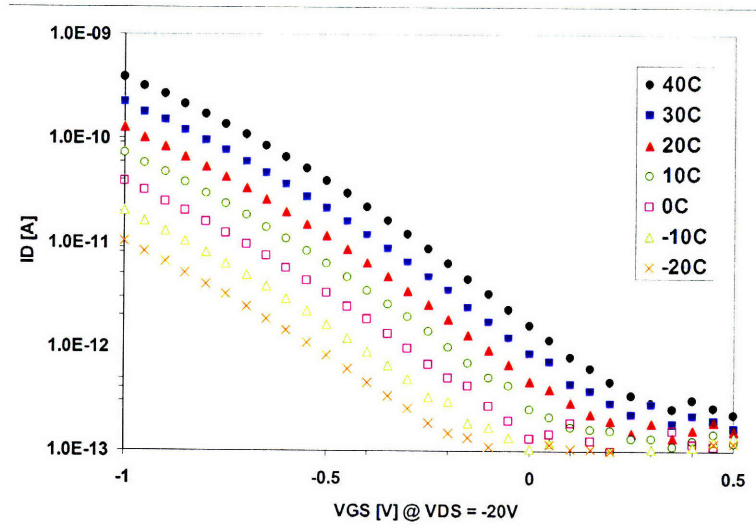
Figure 2-23: Subthreshold region temperature characteristics on a semi-log scale, $1,000\mu m/5\mu m$.

The subthreshold temperature characteristics are shown in Figure 2-23. Unlike silicon MOSFETs, where S is temperature dependent, OTFT's S is not affected by temperature in the temperature range tested[6]. This is shown in Figure 2-24.

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[6]As temperature nears the processing temperature of $95°C$, the pentacene morphology becomes irreversibly changed. As temperature decreases to below $-50°C$, Knipp et al. [33] show that the inverse subthreshold slope of OTFTs becomes temperature dependent.
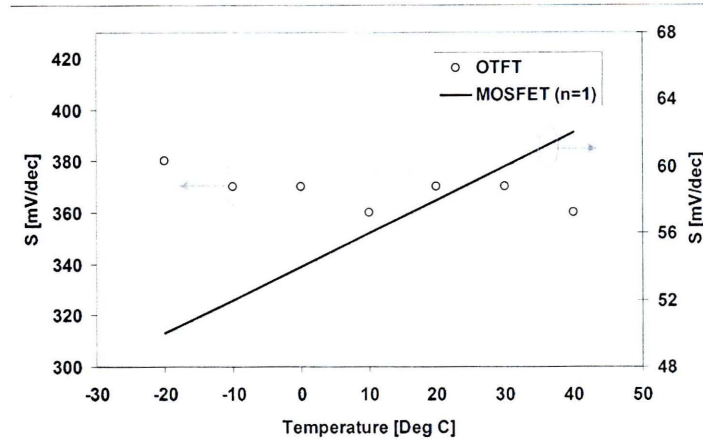
Figure 2-24: Subthreshold slope versus temperature, for the OTFT (measured) and the MOSFET (modeled).
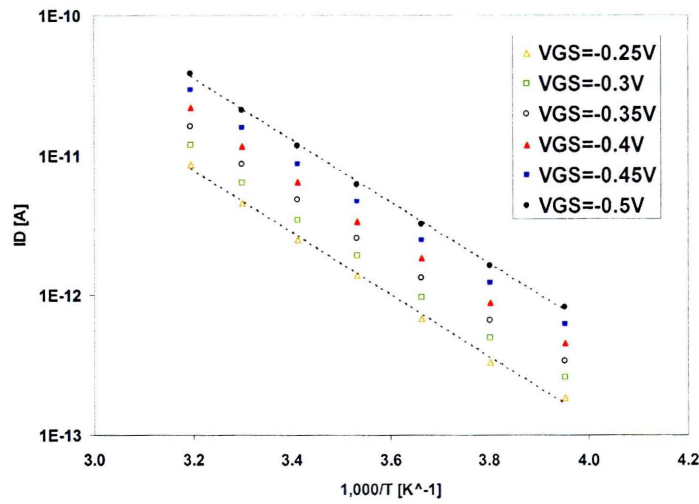
Figure 2-25: Arrhenius plot of subthreshold I_D at various V_{GS}'s, $1,000\mu m/5\mu m$.

Further insight can be gained by graphing an Arrhenius plot of I_D at various V_{GS}'s in Figure 2-25. Again, the temperature dependence can be modeled by $I_D \propto exp(-\alpha/T)$. However, as shown by Figure 2-25, subthreshold OTFT's α does not change with V_{GS}, unlike subthreshold MOSFET's $\alpha = qV_{GS}/(nk)$.

A detailed model in all regions of operation will be developed in Chapter 3.

Chapter 3

A Unified OTFT DC Circuit Model

This chapter develops a unified OTFT DC circuit model for all operating regions and under varying temperatures. This model will serve as an analysis and simulation tool for the circuit design in Chapter 4.

3.1 Model Development

The development of the model is based on the Rensselaer Polytechnic Institute (RPI) a-Si transistor model [34, 35]. It is chosen because it models the a-Si transistor, which is an amorphous, trap-dominated, and accumulation-mode thin-film transistor just like the OTFT. In addition, this model is derived from device physics [34, 36, 37] that may apply to OTFTs [38, 39].

Bandgap trap states are central to the model. As previously mentioned in Section 2.3, OTFTs contain significant trap states in the bandgap. As done in [31, 32], we assume that the traps have an exponential density of states. The expressions for

the density of states are shown below in terms of energy (E) and potential (V).

$$g(E) = g_0 exp\left(\frac{E_{F0} - E}{E_{trap}}\right) \tag{3.1}$$

$$g(V) = g_0 exp\left(\frac{V}{V_{trap}}\right) \tag{3.2}$$

In Equation 3.1, E_{F0} is the Fermi level at equilibrium, E_{trap} is the characteristic trap energy, and g_0 is the density of states at E_{F0}. In Equation 3.2, V is defined as $V = (E_{F0} - E)/q$, and $V_{trap} = E_{trap}/q$.

The density of trap states is illustrated in Figure 3-1, where E_{LUMO} is the lowest unoccupied molecular orbital (LUMO) energy level, and E_{HOMO} is the highest occupied molecular orbital (HOMO) energy level. This figure is based on Figure 5-1 in [34].
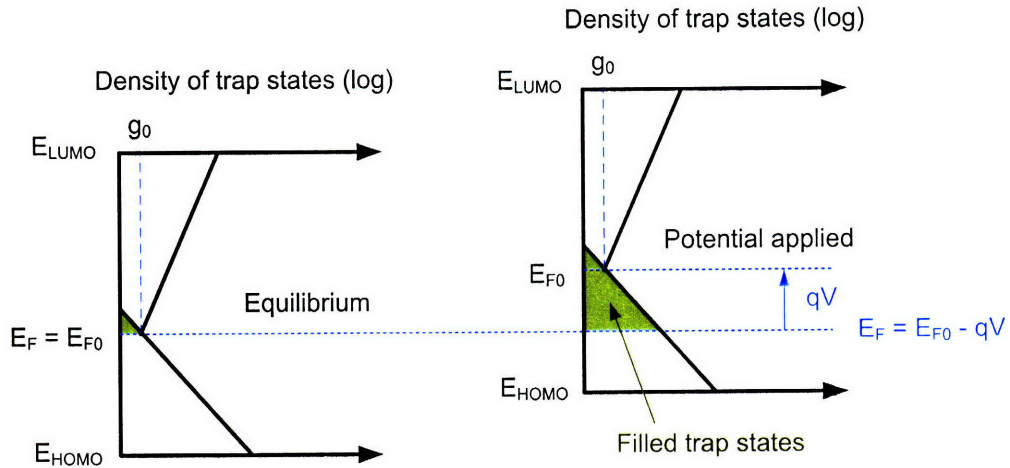
Figure 3-1: Exponential density of trap states in pentacene, under equilibrium and under bias.

3.1.1 Above-threshold Model: Linear Region

Assuming that the diffusion current is negligible when above-threshold, we begin by stating that the drain current is the product of the channel width (W), the elementary

charge (q), the charge velocity (v), and the sheet density of free holes (p_s).

$$I_D = Wqvp_s \tag{3.3}$$

We will first treat p_s, which can be found by integrating the volume density of free holes (P_v) over the vertical thickness of the free hole layer (t):

$$p_s = \int_0^t P_v \, dy \tag{3.4}$$

The volume density of free holes, P_v, can be found by Boltzmann statistics[1]:

$$P_v = P_{v0} exp\left(\frac{qV}{kT}\right) \tag{3.5}$$

$$P_{v0} = N_{HOMO} exp\left(-\frac{E_{F0} - E_{HOMO}}{kT}\right) \tag{3.6}$$

In Equations 3.5 and 3.6, P_v is the free hole volume density under an applied potential of V, P_{v0} is the free hole volume density at equilibrium, and N_{HOMO} is the HOMO energy level's effective density of states. We substitute P_v into Equation 3.4 to obtain p_s:

$$p_s = \int_0^t P_v \, dy \tag{3.7}$$

$$= P_{v0} \int_0^t exp\left(\frac{qV}{kT}\right) dy \tag{3.8}$$

$$= P_{v0} \int_0^{\phi_s} \frac{1}{E(V)} exp\left(\frac{qV}{kT}\right) dV \tag{3.9}$$

Instead of integrating over thickness in Equation 3.8, an indirect but simpler method is to integrate over potential from deep substrate (zero potential, equilibrium) to the dielectric-semiconductor interface (surface potential, ϕ_s). This change of variables is done in Equation 3.9, where $E(V) = -dV/dy$ is the vertical electric field.

Two unknowns, the electric field ($E(V)$) and the surface potential (ϕ_s), need to be found before Equation 3.9 can be integrated. $E(V)$ can be stated in terms

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[1]We make the reasonable assumption that the semiconductor is not degenerate.

of charge density (ρ) by using Poisson's equation in Equation 3.10 and by using $E(V) = -dV/dy$ in Equation 3.12.

$$\frac{dE(V)}{dy} = \frac{\rho}{\epsilon_s} \tag{3.10}$$

$$-\frac{dE(V)}{dy}dV = -\frac{\rho}{\epsilon_s}dV \tag{3.11}$$

$$E(V)\,dE(V) = -\frac{\rho}{\epsilon_s}dV \tag{3.12}$$

$$E(V)^2 = -\frac{2}{\epsilon_s}\int_0^V \rho(V')\,dV' \tag{3.13}$$

To find the charge density, we use the density of states equation (Equation 3.2) to sum the trapped holes in the bandgap.

$$\rho(V) = -q\int_0^V g(V')\,dV' \tag{3.14}$$

$$= -qg_0V_{trap}\left(exp\left(\frac{V}{V_{trap}}\right) - 1\right) \tag{3.15}$$

$E(V)$ can be calculated by substituting Equation 3.15 into Equation 3.13:

$$E(V) = \left(\frac{2qg_0V_{trap}}{\epsilon_s}\int_0^V \left(exp\left(\frac{V'}{V_{trap}}\right) - 1\right)dV'\right)^{1/2} \tag{3.16}$$

$$= \left(\frac{2qg_0V_{trap}{}^2}{\epsilon_s}\left(exp\left(\frac{V}{V_{trap}}\right) - \frac{V}{V_{trap}} - 1\right)\right)^{1/2} \tag{3.17}$$

Next, the surface potential (ϕ_s) can be found by defining V_T as the voltage when the device reaches flat-band condition[2]. In Equation 3.18, V_{GT} is defined as the overdrive voltage, and it is assumed that $V_{GT} \gg \phi_s$ when strongly above-threshold.

$$V_{GT} = V_{SG} + V_T = E_{ox}t_{ox} + \phi_s \approx E_{ox}t_{ox} \tag{3.18}$$

E_{ox} can be found by the continuity of fields:

$$E_{ox} = \frac{\epsilon_s E_s}{\epsilon_{ox}} \tag{3.19}$$

---

[2]As previously mentioned in Section 2.2, the threshold voltage is actually the flat-band voltage.

In Equation 3.19, E_s is the electric field at $V = \phi_s$. We use Equation 3.17 to find E_s:

$$E_s = E(\phi_s) = \left(\frac{2qg_0V_{trap}^2}{\epsilon_s} \left(exp\left(\frac{\phi_s}{V_{trap}}\right) - \frac{\phi_s}{V_{trap}} - 1 \right) \right)^{1/2} \tag{3.20}$$

$$\approx \left(\frac{2qg_0V_{trap}^2}{\epsilon_s} exp\left(\frac{\phi_s}{V_{trap}}\right) \right)^{1/2} \tag{3.21}$$

In Equation 3.21, we assume that $\phi_s \gg V_{trap}$. This is a reasonable assumption because $V_{trap} \approx 0.03V$ for the tested OTFTs. Using Equations 3.18 and 3.19, V_{GT} can be rewritten in terms of E_s:

$$V_{GT} = \frac{\epsilon_s E_s t_{ox}}{\epsilon_{ox}} \tag{3.22}$$

After substituting E_s from Equation 3.21 into Equation 3.22 and rearranging, we obtain an expression for ϕ_s:

$$\phi_s \approx V_{trap}ln\left(\frac{\epsilon_{ox}^2 V_{GT}^2}{2q\epsilon_s t_{ox}^2 g_0 V_{trap}^2} \right) \tag{3.23}$$

With both $E(V)$ and ϕ_s known, we can finally calculate p_s from Equation 3.9:

$$p_s = P_{v0} \int_0^{\phi_s} \frac{1}{E(V)} exp\left(\frac{qV}{kT}\right) dV \tag{3.24}$$

$$\approx P_{v0}t_m\frac{2kT}{2qV_{trap} - kT} \left(\frac{t_m}{t_{ox}} \frac{\epsilon_{ox}}{\epsilon_s} \frac{V_{GT}}{V_{trap}} \right)^{\frac{2qV_{trap}}{kT}-1} \tag{3.25}$$

$$= N_{HOMO}exp\left(-\frac{E_{F0} - E_{HOMO}}{kT} \right) t_m\frac{2kT}{2qV_{trap} - kT} \left(\frac{t_m}{t_{ox}} \frac{\epsilon_{ox}}{\epsilon_s} \frac{V_{GT}}{V_{trap}} \right)^{\frac{2qV_{trap}}{kT}-1} \tag{3.26}$$

where t_m is defined below [34]:

$$t_m = \left(\frac{\epsilon_s}{2qg_0} \right)^{1/2} \tag{3.27}$$

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Looking back at the initial current equation (repeated below), we have found the sheet density of free holes, p_s, but we still need to find the charge velocity, v.

$$I_D = Wqvp_s \qquad (3.28)$$

To find v, we assume that v is proportional to the lateral electric field. As done for MOSFETs, we name the proportionality constant as mobility, or μ. This is a reasonable assumption because the lateral field is low when in the linear region. The low field also permits the assumption that the field is constant in the channel.

$$v = \mu E_{lateral} \qquad (3.29)$$

$$= \mu \frac{V_{SD}}{L} \qquad (3.30)$$

To investigate μ's dependencies, we plot the measured exponent of V_{GT} (from transfer characteristics) versus temperature in Figure 3-2.
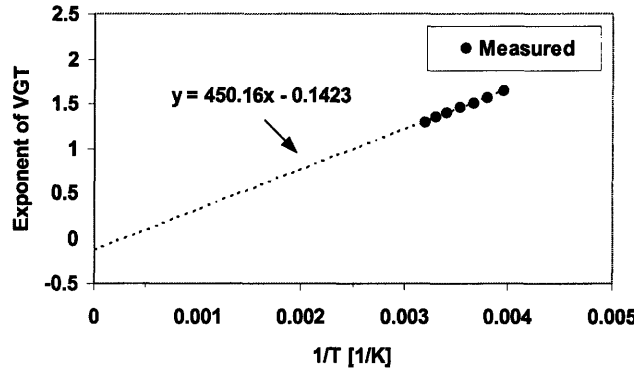
Figure 3-2: Exponent of V_{GT} versus $1/T$ for a $1,000\mu m/5\mu m$ device in linear region.

According to Equation 3.26, the exponent of V_{GT} versus $1/T$ should have a y-axis intercept at -1 because p_s yields a V_{GT} exponent of $2qV_{trap}/(kT) - 1$. However, based on Figure 3-2, the y-axis intercept is -0.14. This discrepancy can be modeled by a mobility[3] that increases with V_{GT}, or $\mu = \mu_o(V_{GT}/V_\mu)^n$, where μ_o, n, and V_μ are

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[3]This mobility is affected by contact resistance because, as seen in Section 2.2.1, the V_{GT} exponent in linear region is limited by contact resistance.

constants. This results in the following empirical model for the charge velocity:

$$v = \mu \frac{V_{SD}}{L} \tag{3.31}$$

$$= \mu_o \left(\frac{V_{GT}}{V_\mu}\right)^n \frac{V_{SD}}{L} \tag{3.32}$$

Inserting Equations 3.31 and 3.26 into Equation 3.28 yields the equation for the drain current in the above-threshold, linear region:

$$I_D = \frac{W}{L} q\mu V_{SD} N_{HOMO} exp\left(-\frac{E_{F0} - E_{HOMO}}{kT}\right) t_m \frac{2kT}{2qV_{trap} - kT} \left(\frac{t_m}{t_{ox}} \frac{\epsilon_{ox}}{\epsilon_s} \frac{V_{GT}}{V_{trap}}\right)^{\frac{2qV_{trap}}{kT} - 1} \tag{3.33}$$

3.1.2 Above-threshold Model: Saturation Region

As observed in the output characteristics in Figure 2-13, the OTFTs devices saturate at a sufficiently large V_{SD}. This behavior may be attributed to the decreased accumulation layer in the channel near the drain. The decrease in accumulated charges will decrease the channel conductance in the region. Therefore, additional V_{SD} will be dropped across this region instead of increasing the lateral field and the current in the channel.

We use the empirical approach described in [34, 37] to model saturation. This approach replaces V_{SD} with an effective V_{SDE}. At low V_{SD}, $V_{SDE} \approx V_{SD}$. At high V_{SD}, $V_{SDE} \approx \alpha_{sat} V_{GT}$, thus increasing the overall exponent of V_{GT} by one and is consistent with Figure 2-12.

$$V_{SDE} = \frac{V_{SD}}{\left(1 + \left(\frac{V_{SD}}{\alpha_{sat} V_{GT}}\right)^m\right)^{\frac{1}{m}}} \tag{3.34}$$

In Equation 3.34, α_{sat} adjusts the onset of saturation with respect to V_{GT}, and m adjusts the width of the transition region. This transition is illustrated in Figure 3-3.
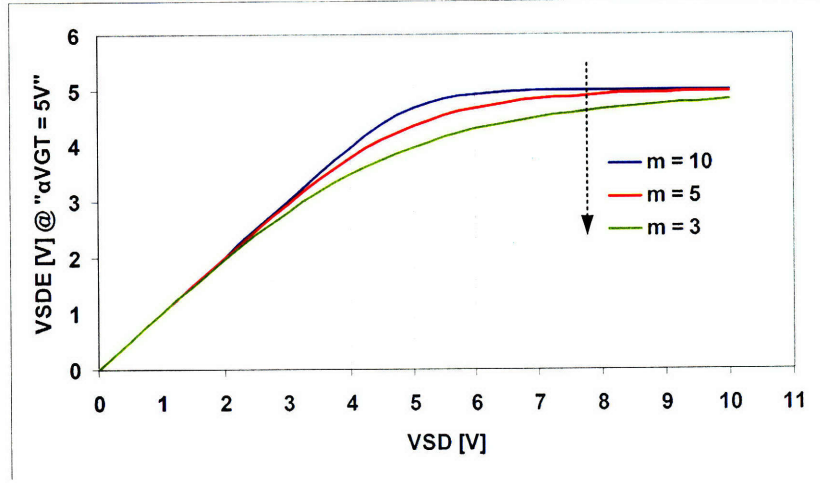
Figure 3-3: V_{SDE} versus V_{SD}, with $\alpha_{sat}V_{GT} = 5V$ and $m = 3, 5, 10$.

3.1.3 Subthreshold Model

Figure 2-14 shows that the subthreshold current has an apparently exponential dependence on V_{GT}. However, the transition between subthreshold and above-threshold regions is gradual. Furthermore, using an exponential model for the subthreshold region and a power model for the above-threshold region would make simulation convergence difficult. For these two reasons, we opt for an approximation of the exponential behavior by using a power model as done in [34]. To do this, V_{GT} is replaced with an effective V_{GTE}. At low V_{GT}, V_{GTE} is approximately exponentially dependent on V_{GT}. At high V_{GT}, $V_{GTE} \approx V_{GT}$.

$$V_{GTE} = \frac{V_{MIN}}{2} \left(1 + \frac{V_{GT}}{V_{MIN}} + \sqrt{\delta^2 + \left(\frac{V_{GT}}{V_{MIN}} - 1 \right)^2} \right) \qquad (3.35)$$

In Equation 3.35, δ is a transition parameter, and V_{MIN} is a convergence parameter. The use of V_{GTE} effectively unifies the above-threshold and subthreshold regions in a smooth manner, as shown in Figure 3-4.

40
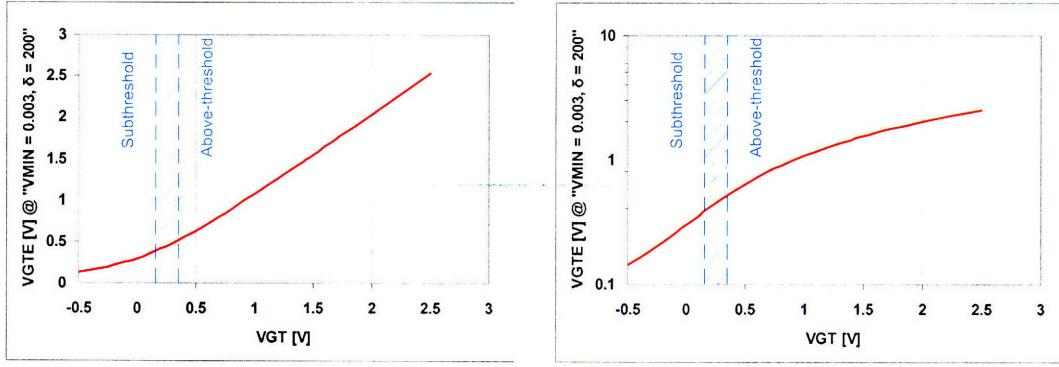
(a) Linear scale. (b) Semi-log scale.

Figure 3-4: V_{GTE} versus V_{GT}, with $\delta = 200$ and $V_{MIN} = 0.003$, on (a) linear and (b) semi-log scales.

3.1.4 The Unified Model

By using V_{SDE} and V_{GTE}, we obtain a unified model that is valid for both linear and saturation regions, and for both above-threshold and subthreshold regions. The unified model is shown below, followed by a summary of parameters in Table 3.1.

$$I_D = \frac{W}{L} q \mu V_{SDE} N_{HOMO} exp\left(-\frac{E_{F0} - E_{HOMO}}{kT}\right) t_m \frac{2kT}{2qV_{trap} - kT} \left(\frac{t_m}{t_{ox}} \frac{\epsilon_{ox}}{\epsilon_s} \frac{V_{GTE}}{V_{trap}}\right)^{\frac{2qV_{trap}}{kT} - 1}$$

(3.36)

where:

$$V_{SDE} = \frac{V_{SD}}{\left(1 + \left(\frac{V_{SD}}{\alpha_{sat} V_{GTE}}\right)^m\right)^{\frac{1}{m}}} \tag{3.37}$$

$$V_{GTE} = \frac{V_{MIN}}{2} \left(1 + \frac{V_{GT}}{V_{MIN}} + \sqrt{\delta^2 + \left(\frac{V_{GT}}{V_{MIN}} - 1\right)^2}\right) \tag{3.38}$$

$$V_{GT} = V_{SG} + V_T \tag{3.39}$$

$$\mu = \mu_o \left(\frac{V_{GTE}}{V_\mu}\right)^n \tag{3.40}$$

$$t_m = \left(\frac{\epsilon_s}{2qg_0}\right)^{1/2} \tag{3.41}$$

Parameter	Unit	Description
α_{sat}	$-$	Onset parameter for current saturation.
δ	$-$	Transition parameter for the subthreshold region.
E_{F0}	eV	Fermi energy level at equilibrium.
E_{HOMO}	eV	HOMO energy level.
ϵ_{ox}	$-$	Relative dielectric constant of the gate dielectric.
ϵ_s	$-$	Relative dielectric constant of the substrate.
g_0	$cm^{-3}eV^{-1}$	Density of states at E_{F0}.
L	μm	Channel length.
m	$-$	Transition parameter for current saturation.
μ_o	$cm^2/(Vs)$	Mobility parameter.
n	$-$	Exponent of mobility's power dependence on V_{GTE}.
N_{HOMO}	cm^{-3}	Effective density of states at HOMO energy level.
t_{ox}	m	Gate dielectric thickness.
V_{MIN}	V	Convergence parameter for the subthreshold region.
V_μ	V	Mobility's V_{GTE}-dependence parameter.
V_{trap}	V	Characteristic voltage for the trap states.
W	μm	Channel width.

Table 3.1: Summary of model parameters.

3.2 Model Versus Measured Data

The model is validated by its accuracy in fitting the measured OTFT characteristics. First, the above-threshold transfer characteristics are compared in Figure 3-5. Arrhenius plots of the above-threshold I_D are compared in Figure 3-6. Both figures use the parameters in Table 3.2.
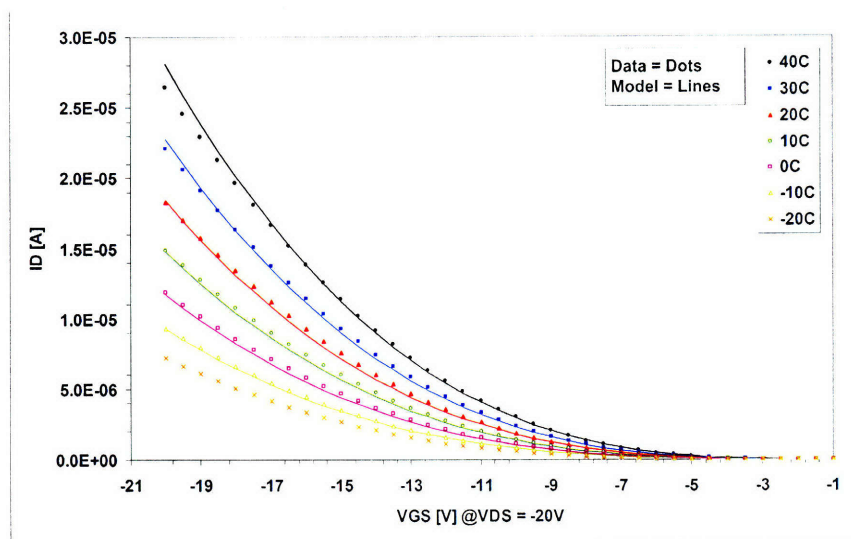
(a) Linear scale.
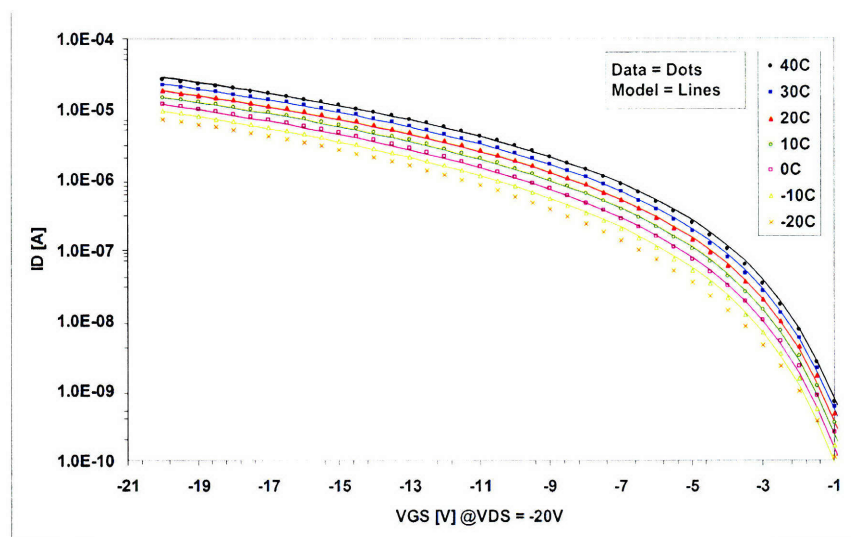
(b) Semi-log scale.

Figure 3-5: Measured versus modeled above-threshold transfer characteristics, $1,000\mu m/5\mu m$, on (a) linear and (b) semi-log scales.

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Figure 3-6: Measured versus modeled above-threshold Arrhenius plots of I_D at two V_{GS}'s, $1,000\mu m/5\mu m$.

Parameter	Value	Parameter	Value
α_{sat}	0.64	δ	120
$E_{F0} - E_{HOMO}$	$0.2eV$	ϵ_{ox}	3
ϵ_s	6	L	$5\mu m$
m	4.4	n	1.5
μ_o	$0.009cm^2/(Vs)$	N_{HOMO}	$2.2 \times 10^{19}cm^{-3}$
t_m	$5.2nm$	t_{ox}	$200nm$
V_{MIN}	$0.01V$	V_μ	$1V$
V_T	$-1V$	V_{trap}	$0.02V$
W	$1,000\mu m$		

Table 3.2: Model parameters used in Figures 3-5 and 3-6.

Next, subthreshold transfer characteristics are compared in Figure 3-7. Arrhenius plots of the subthreshold I_D are compared in Figure 3-8. Both figures use the parameters in Table 3.3. Some parameters are different from Table 3.2 because the subthreshold characteristics were measured separately and the devices had been stressed from the above-threshold measurements[4].

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[4]As a reminder, because the model contains empirical components, there may be more than one set of parameters that fit a group of transfer characteristics. Therefore, one cannot extract physical values from the parameters.

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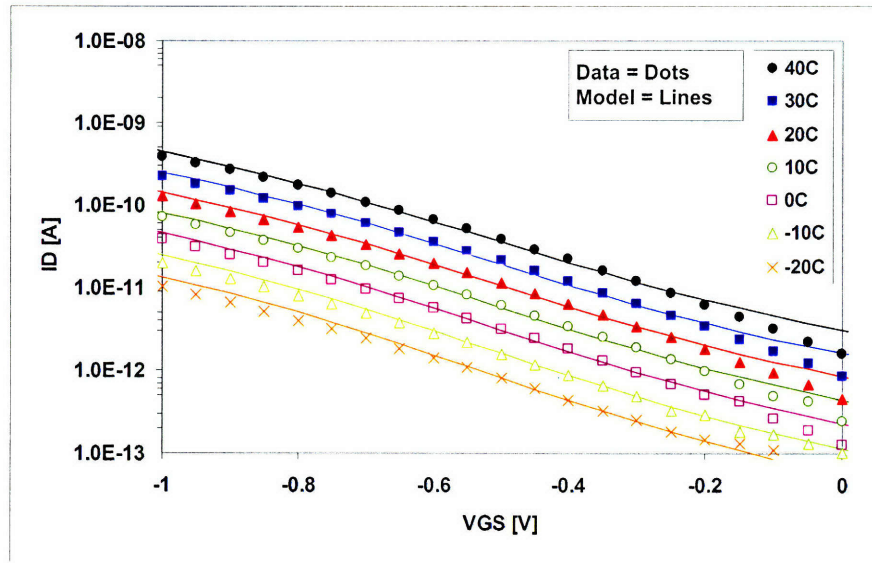
Figure 3-7: Measured versus modeled subthreshold transfer characteristics, $1,000\mu m/5\mu m$.
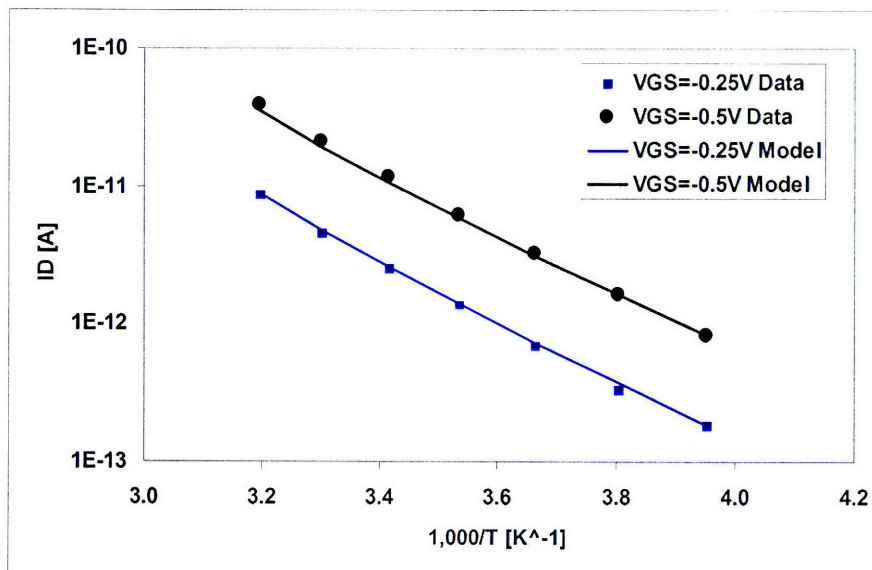
Figure 3-8: Measured versus modeled subthreshold Arrhenius plots of I_D at two V_{GS}'s, $1,000\mu m/5\mu m$.

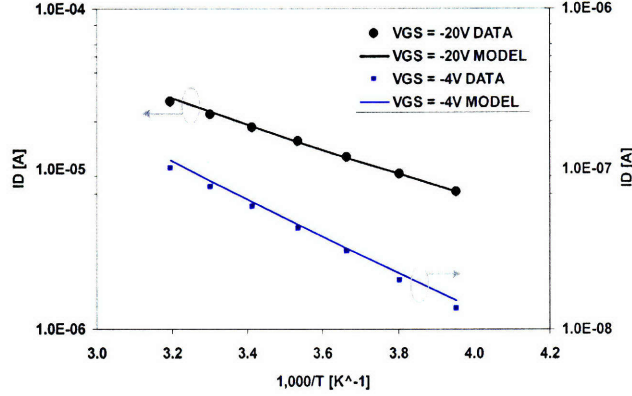| Parameter	Value	Parameter	Value
α_{sat}	0.64	δ	90
$E_{F0} - E_{HOMO}$	$0.25eV$	ϵ_{ox}	3
ϵ_s	6	L	$5\mu m$
m	4.4	n	1.5
μ_o	$0.009cm^2/(Vs)$	N_{HOMO}	$2.2 \times 10^{19} cm^{-3}$
t_m	$5.2nm$	t_{ox}	$200nm$
V_{MIN}	$0.005V$	V_μ	$1V$
V_T	$-0.5V$	V_{trap}	$0.016V$
W	$1,000\mu m$		

Table 3.3: Model parameters used in Figures 3-7 and 3-8.

Lastly, the output characteristics at room temperature are modeled in Figure 3-9 using the parameters from Table 3.4. The parameters are different from Table 3.2 because a device with a longer channel is used to minimize the effects of contact resistance.
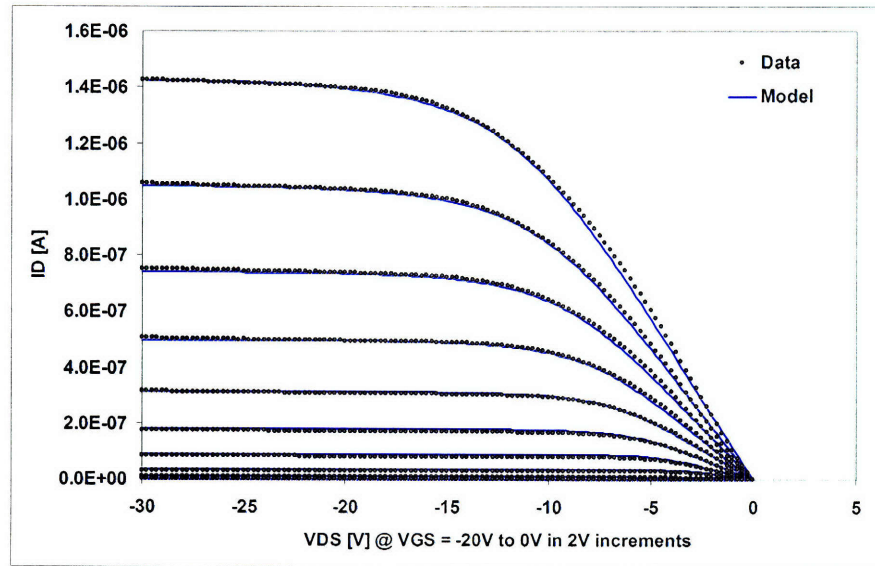
Figure 3-9: Measured versus modeled output characteristics at room temperature, $200\mu m/25\mu m$.

Parameter	Value	Parameter	Value
α_{sat}	0.64	δ	120
$E_{F0} - E_{HOMO}$	$0.2eV$	ϵ_{ox}	3
ϵ_s	6	L	$25\mu m$
m	4.4	n	1.2
μ_o	$0.025 cm^2/(Vs)$	N_{HOMO}	$3.0 \times 10^{19} cm^{-3}$
t_m	$5.5nm$	t_{ox}	$200nm$
V_{MIN}	$0.01V$	V_μ	$1V$
V_T	$-0.5V$	V_{trap}	$0.022V$
W	$200\mu m$		

Table 3.4: Model parameters used in Figure 3-9.

3.3 Model Implementation in Verilog-A

Verilog-A is an analog behavioral modeling language that can be used to model an arbitrary device as a circuit element. The Verilog-A code specifies the device's ports and the I-V relations between the ports. The specified device can then be used as a circuit element in circuit simulators such as SPICE or Spectre.

The OTFT is represented by a three-port device (drain, gate, and source), and the unified OTFT model (Equation 3.36) is used to relate I_D to V_{GS} and to V_{DS}. The Verilog-A code is included in Appendix A. Figure 3-10 shows the simulated temperature characteristics using the parameters from Table 3.2.
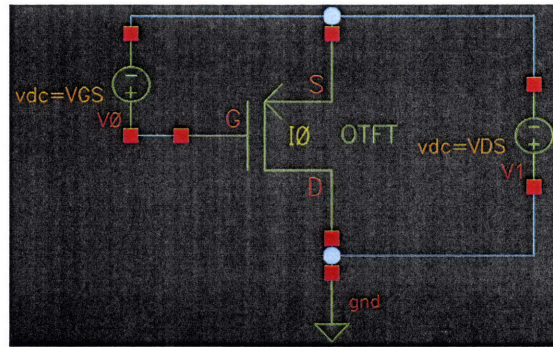
(a) Simulation schematic.
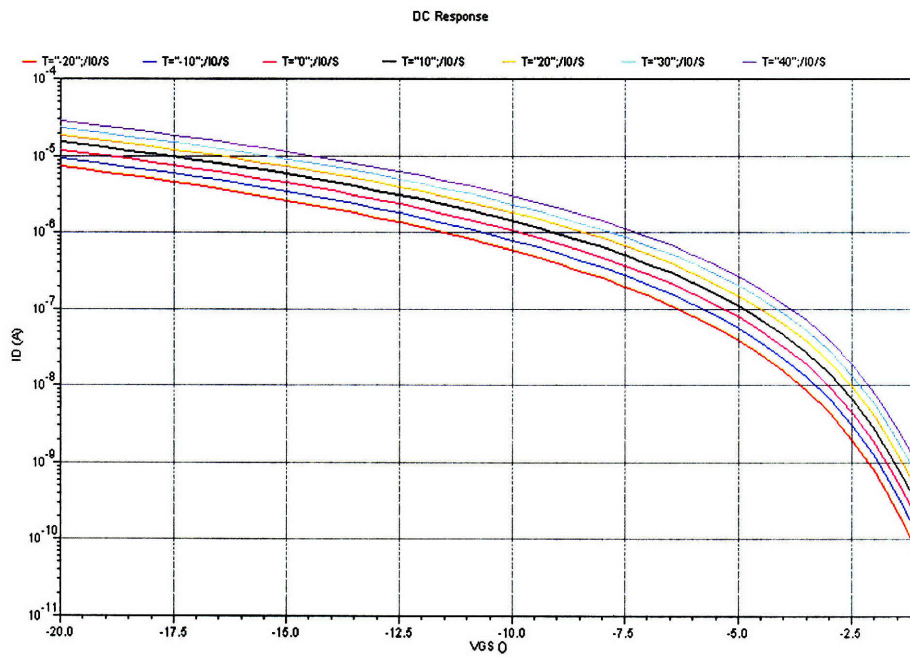
(b) Simulation result.

Figure 3-10: Simulated transfer characteristics at various temperatures using Verilog-A model, $1,000\mu m/5\mu m$. Cadence's Virtuoso Spectre Circuit Simulator is used.

The simulation exactly matches the model from Figure 3-5 because the same equations and parameters are used. The Verilog-A model will be a design tool for the temperature-sensing circuit design in Chapter 4.

Chapter 4

OTFT Temperature-sensing Circuits

In this chapter, temperature-sensing circuits are designed using the OTFT circuit model as a tool. First, the single-ended circuit topology is discussed, and then the improved differential circuit topology is presented.

4.1 The Single-ended Topology

This section describes the circuit design and the measured results of the single-ended topology.

4.1.1 Single-ended Topology Circuit Design

The design of a temperature-sensing circuit begins with the OTFT temperature characteristics, which are repeated in Figure 4-1.

49
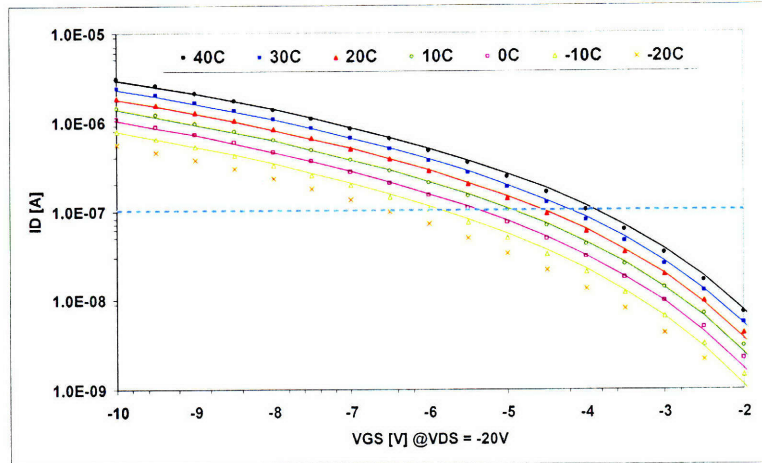
Figure 4-1: Temperature characteristics on a semi-log scale, $1,000\mu m/5\mu m$.

In Figure 4-1, the dotted line represents a constant I_D bias. By looking at the operating points on the dotted line, one notices that V_{GS} is a function of temperature when I_D is held constant. Using V_{GS} to detect temperature is the key principle of operation for the temperature-sensing circuits in this work.
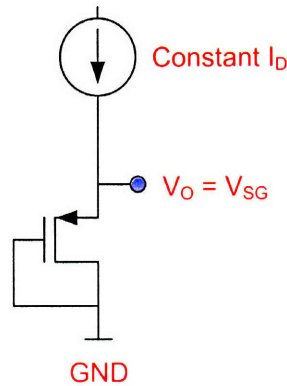
Figure 4-2: The single-ended temperature-sensing circuit.

A circuit that implements this idea is shown in Figure 4-2, where the OTFT is diode-connected to ensure that it operates in the saturation region. For this circuit, the dependence of V_{GS} on temperature can be found by using the circuit model from Chapter 3. The model in saturation region is repeated below in a simplified form

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where A, B, C, and D are constant with temperature[1].

$$I_D = Aexp\left(-\frac{B}{T}\right)\frac{T}{C-T}(DV_{GTE})^{\frac{C}{T}+n} \tag{4.1}$$

where:

$$A = 2\frac{W}{L}q\mu_o\frac{1}{(V_\mu)^n}N_{HOMO}t_m\alpha_{sat}\frac{1}{D^{n+1}} \tag{4.2}$$

$$B = \frac{E_{F0} - E_{HOMO}}{k} \tag{4.3}$$

$$C = \frac{2qV_{trap}}{k} \tag{4.4}$$

$$D = \frac{t_m}{t_{ox}}\frac{\epsilon_{ox}}{\epsilon_s}\frac{1}{V_{trap}} \tag{4.5}$$

We rearrange Equation 4.1 for an expression of V_{GTE}.

$$V_{GTE} = \frac{1}{D}\left(\frac{I_D}{A}\frac{C-T}{T}exp\left(\frac{B}{T}\right)\right)^{\frac{T}{C+nT}} \tag{4.6}$$

Subsequently, V_{GTE} can be converted to V_{GS} using Equation 3.38. Using the equations, we can calculate the output of the circuit, $V_O = V_{SG}$. V_O versus temperature for several I_D's is plotted in Figure 4-3. Values from Table 3.2 are used for the constants.
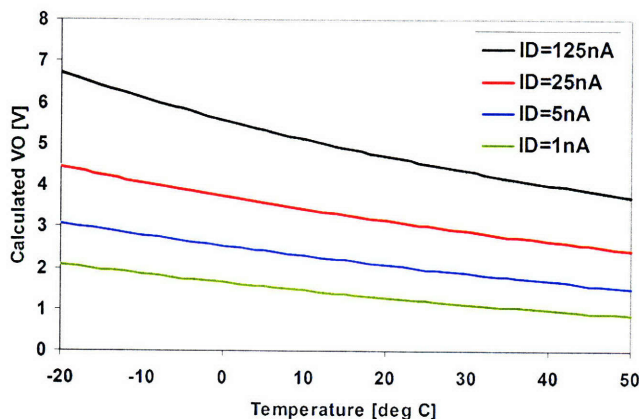
Figure 4-3: Calculated V_O versus temperature using the model, at several I_D's. $1,000\mu m/5\mu m$.

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[1]Sample values using the parameters from Table 3.2: $A = 1.2 \times 10^{-5}$, $B = 2,300$, $C = 460$, $D = 0.65$, $n = 1.5$.

An important figure of merit is the temperature responsivity in $mV/^\circ C$, which is the absolute value of the slope of the plots in Figure 4-3 and is defined in Equation 4.7.

$$responsivity(T_o) = \left| \frac{\partial V_O}{\partial T} \right|_{T=T_o} \tag{4.7}$$

In Figure 4-3, the responsivity depends on I_D. In fact, responsivity also depends on the parameters A, B, C, and D. However, to the circuit designer, the only alterable parameters are I_D and W/L. Therefore, we focus on the slope's dependence on I_D and A $(A \propto W/L)$.

The model allows us to find responsivity by differentiating[2] V_{GTE} with respect to T. The calculated result for responsivity versus I_D is shown in Figure 4-4, which demonstrates that a higher drain current results in a greater responsivity.
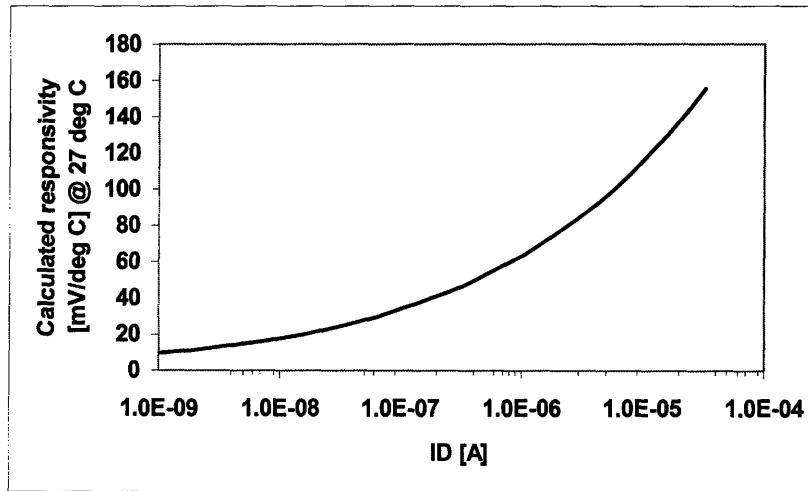
Figure 4-4: Calculated responsivity versus I_D at $27^\circ C$. $1,000\mu m/5\mu m$. Parameters values are from Table 3.2.

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[2]Because $V_{GTE} \approx V_{SG} = V_O$, this is only an approximation. However, V_{GTE} is used because there is a closed-form solution to $\partial V_{GTE}/\partial T$, whereas $\partial V_{SG}/\partial T$ does not have a closed-form solution.

The calculated result for responsivity versus W/L is shown in Figure 4-5.
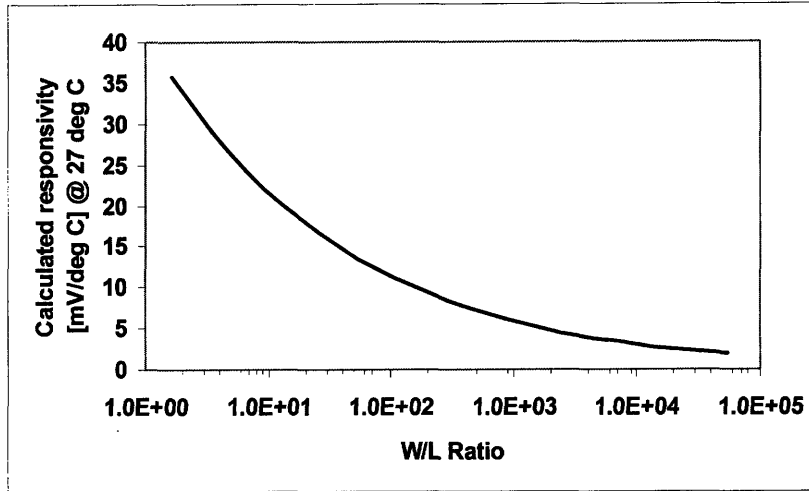
Figure 4-5: Calculated responsivity versus W/L at $27°C$. $I_D = 1nA$. Parameters values are from Table 3.2, except W and L.

Figure 4-4 shows that a lower W/L results in a greater responsivity, in a manner that is inverse to I_D's effect. The inverse behavior is expected because I_D/A is a coefficient in Equation 4.6. In other words, responsivity is related to the current density (I_D/W) when L is fixed. The disadvantage in having a high current density is a higher V_{SG}, which leads to a higher voltage supply and greater power dissipation.

4.1.2 Single-ended Topology Circuit Results

The singled-ended topology with an external current source is tested at three settings of I_D. The die photo and the circuit schematic are shown in Figure 4-6.
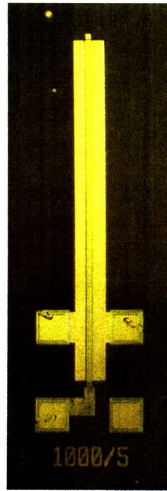
(a) Die photo ($1,000\mu m/5\mu m$ OTFT).   (b) Circuit schematic.
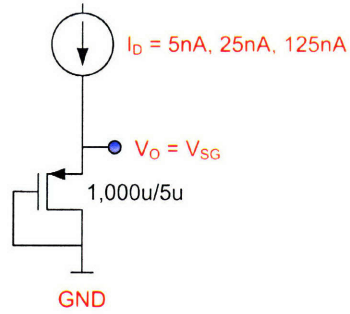
Figure 4-6: Die photo and circuit schematic of the singled-ended topology with external current source.

The V_O measurement is done by sweeping the die temperature from $-20°C$ to $50°C$ in $10°C$ increments. At each temperature, 20 to 30 samples of V_O are taken at 2 samples/second. The raw data of V_O versus time for $I_D = 5nA$ is shown in Figure 4-7.
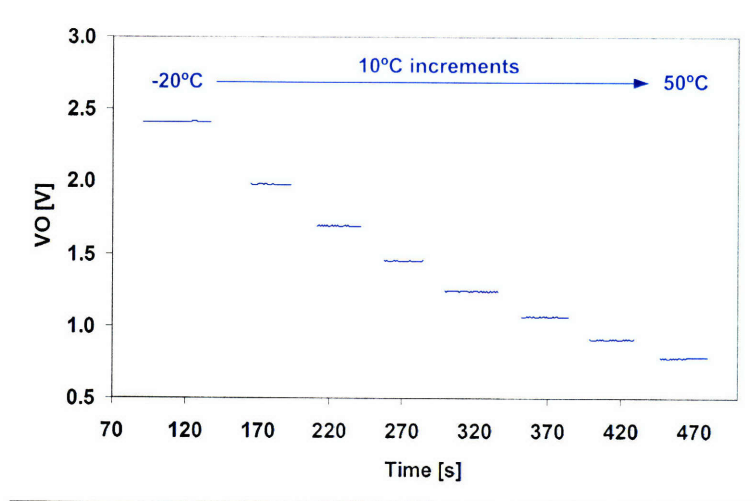
Figure 4-7: Measured V_O versus time for $I_D = 5nA$ as temperature is swept from $-20°C$ to $50°C$ in $10°C$ increments.

At each temperature, one can notice fluctuations in V_O. These fluctuations are

magnified in Figure 4-8.
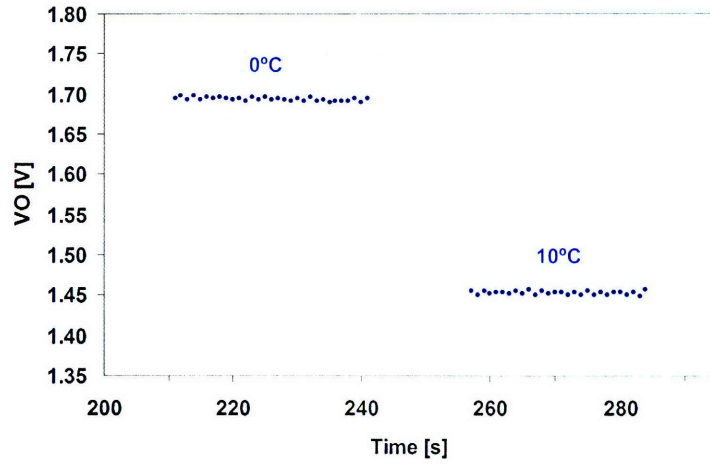
Figure 4-8: Measured V_O fluctuations at $0°C$ and $10°C$. $I_D = 5nA$.

The fluctuations can be characterized in two ways: standard deviation and histogram. The standard deviation at each temperature and at each I_D setting is plotted in Figure 4-9. The standard deviations increase with I_D because the responsivities increase with I_D. In fact, as seen later in Table 4.1, the average standard deviation increases with I_D at approximately the same rate as the responsivity's increase with I_D.
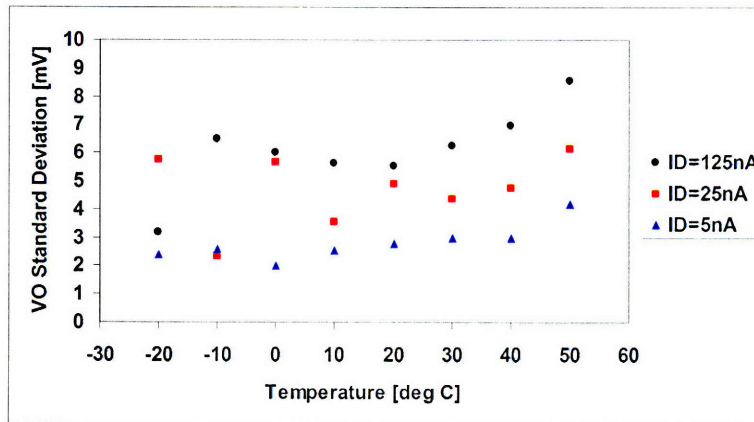
Figure 4-9: Standard deviations of sampled V_O at each temperature setting and at each I_D setting.

A typical histogram of samples is plotted in Figure 4-10.
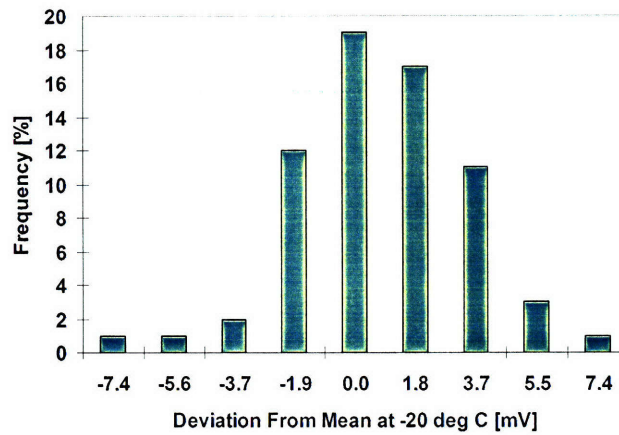
Figure 4-10: Histogram of sampled V_O for $I_D = 125nA$ at $-20°C$.

Finally, the samples at each temperature are averaged to a single V_O value. The averaged V_O values are plotted versus temperature in Figure 4-11 at three I_D settings. At each temperature, the standard deviation of the V_O samples is represented as a vertical error bar. The error bars are very small because the standard deviations of V_O are insignificant when compared to V_O.
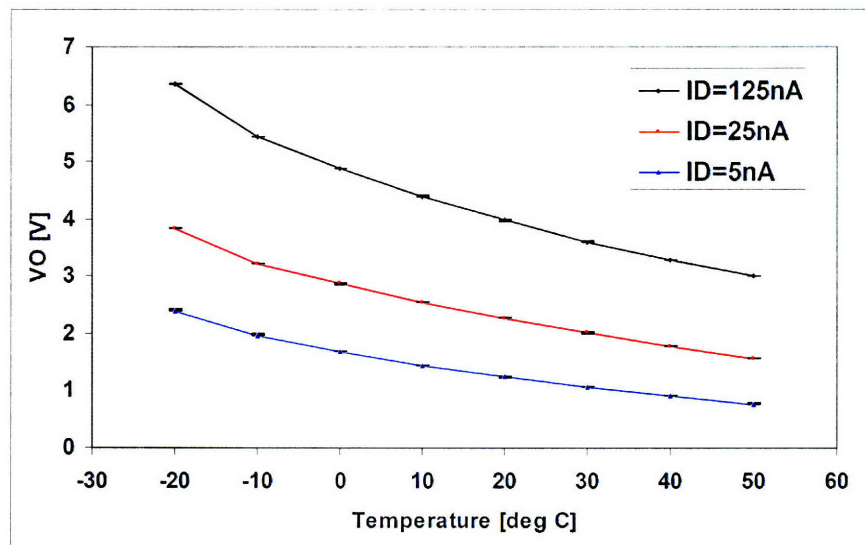
Figure 4-11: Averaged V_O versus temperature at three I_D settings with standard deviations of V_O samples as vertical error bars.

Figure 4-11 corresponds well with the calculated V_O in Figure 4-3. Both calculated and measured V_O's have concave curvatures and shift higher with increased I_D. As predicted, responsivities increase with greater I_D. The small discrepancy between measurement and calculation is due to the use of different $1,000\mu m/5\mu m$ OTFTs for modeling and measurement.

Table 4.1 summarizes the measured results. One notices that the ratio between standard deviation and responsivity is nearly independent of I_D. In other words, the V_O fluctuations increase proportionally when V_O is more responsive to temperature changes. Furthermore, the highest sensitivity is achieved at low I_D because responsivity increases with I_D at a slower rate than the overall V_O.

Figure of merit	$I_D = 5\ nA$	$I_D = 25\ nA$	$I_D = 125\ nA$
Maximum power dissipation [nW]	12	96	790
Responsivity at 20 °C [$mV/°C$]	22	31	46
Sensitivity at 20 °C, $(\partial V/\partial T)(T[°K]/V)$ [ppm]	4.7×10^6	3.7×10^6	3.2×10^6
Maximum standard deviation of samples [mV at 50 °C]	4.2	6.1	8.6
Average standard deviation of samples [mV]	2.8	4.7	6.1

Table 4.1: Measured results for the temperature-sensing circuit shown in Figure 4-6(b).

4.2   The Differential Topology

The single-ended topology, though simple, has two disadvantages. The first disadvantage is the single-ended output V_O's direct dependence on V_T. This is demonstrated in the equation below, where it is shown that V_O not only contains the temperature

dependence offered by V_{GT} (Equation 4.6), but V_O also contains a V_T term.

$$V_O = V_{SG} = V_{GT} - V_T \tag{4.8}$$

The problem with V_O's dependence on V_T is that the OTFT's V_T shifts with time and bias. This behavior is well documented in several studies [40–42]. The undesired result is that the single-ended circuit's V_O will track V_T's uncontrolled shift. The second disadvantage with the single-ended circuit is nonlinearity. As seen in Figure 4-11, the output voltage V_O is nonlinear versus temperature. A nonlinear V_O requires either a look-up table or a curvature correction circuit before the temperature can be extracted, thus voiding the simplicity that the single-ended circuit offers.

The following sections will show that both mentioned problems can be solved by using a differential topology.

4.2.1   Differential Topology Circuit Design

The differential topology is simply two branches of the single-ended topology, as shown in Figure 4-12.
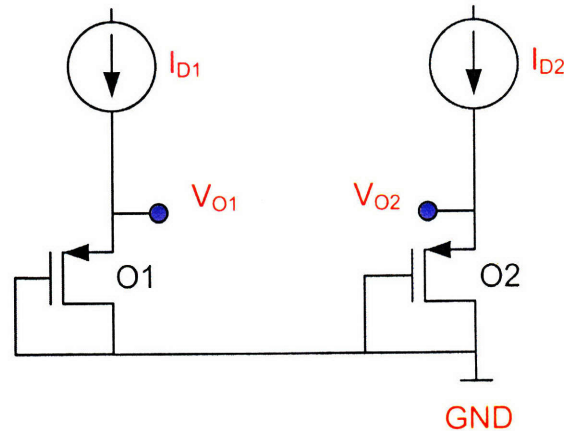
Figure 4-12: The differential topology for the temperature-sensing circuit.

The differential topology effectively cancels the V_T dependence because V_T is a common-mode component in the output voltage V_O. This is shown by the following

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equations.

$$V_{O1} = V_{SG1} = V_{GT1} - V_T \tag{4.9}$$

$$V_{O2} = V_{SG2} = V_{GT2} - V_T \tag{4.10}$$

$$V_O = V_{O1} - V_{O2} = V_{GT1} - V_{GT2} \tag{4.11}$$

Even if the two OTFTs have different V_T's, V_T's effect on V_O is a constant offset as long as both OTFT's V_T's shift in the same manner. To ensure device similarity, O1 and O2 are designed to have the same channel dimensions W and L. In the calculations to follow, we assume that O1 and O2 have identical parameters A, B, C, D, and V_T. This is a reasonable assumption because interdigitated or common-centroid layout can be used to minimize device variations between the two identically-sized OTFTs.

Prior to investigating the curvature correction, we need to first calculate V_O. We begin with the V_{GTE} expression from Equation 4.6 and calculate the differential V_O.

$$V_{GTE} = \frac{1}{D}(I_D)^{\frac{T}{C+nT}} \left(\frac{C-T}{AT} exp \left(\frac{B}{T} \right) \right)^{\frac{T}{C+nT}} \tag{4.12}$$

$$V_O = V_{O1} - V_{O2} \tag{4.13}$$

$$= V_{GT1} - V_{GT2} \tag{4.14}$$

$$\approx V_{GTE1} - V_{GTE2} = \frac{1}{D} \left(\frac{C-T}{AT} exp \left(\frac{B}{T} \right) \right)^{\frac{T}{C+nT}} \left((I_{D1})^{\frac{T}{C+nT}} - (I_{D2})^{\frac{T}{C+nT}} \right) \tag{4.15}$$

Equation 4.15 shows that V_O is temperature dependent if $I_{D1} \neq I_{D2}$. V_O can be rewritten as an I_D-independent term $g(T)$ multiplied by an I_D-dependent term

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$h(T, I_{D1}, I_{D2})$.

$$V_O = g(T)\, h(T, I_{D1}, I_{D2}) \tag{4.16}$$

where:

$$g(T) = \frac{1}{D}\left(\frac{C-T}{AT}exp\left(\frac{B}{T}\right)\right)^{\frac{T}{C+nT}} \tag{4.17}$$

$$h(T, I_{D1}, I_{D2}) = (I_{D1})^{\frac{T}{C+nT}} - (I_{D2})^{\frac{T}{C+nT}} \tag{4.18}$$

Figure 4-13 plots $g(T)$ using the parameters[3] from Table 3.2.
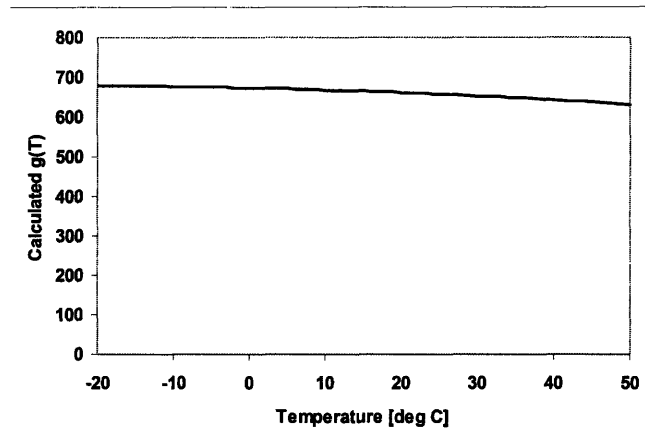
Figure 4-13: $g(T)$ versus temperature using extracted parameters from Table 3.2.

In Figure 4-13, $g(T)$ has a negative slope and a slightly convex shape. Next, $h(T, I_{D1}, I_{D2})$ is plotted in Figure 4-14 using the same parameters and using $I_{D1} = 10nA$ and $I_{D2} = 10pA$ to $5nA$.

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[3] $A = 1.2 \times 10^{-5}$, $B = 2,300$, $C = 460$, $D = 0.65$, $n = 1.5$.
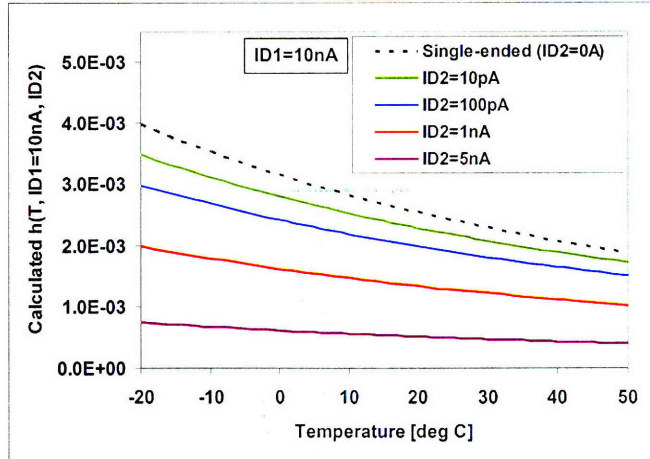
Figure 4-14: $h(T, I_{D1}, I_{D2})$ versus temperature using extracted parameters from Table 3.2. $I_{D1} = 10nA$. $I_{D2} = 10pA, 100pA, 1nA$, and $5nA$.

Figure 4-14 shows that $h(T, I_{D1}, I_{D2})$ has a negative slope and a concave shape. Compared to $g(T)$, which changes by 7% over the $70°C$ temperature range, $h(T, I_{D1}, I_{D2})$ changes by more than 47% over the same range. Consequently, we expect the plot of $V_O = g(T)h(T, I_{D1}, I_{D2})$ to resemble $h(T, I_{D1}, I_{D2})$. Figure 4-15 confirms this. The calculated responsivities for the four I_{D2}'s range from $3mV/°C$ to $15mV/°C$.
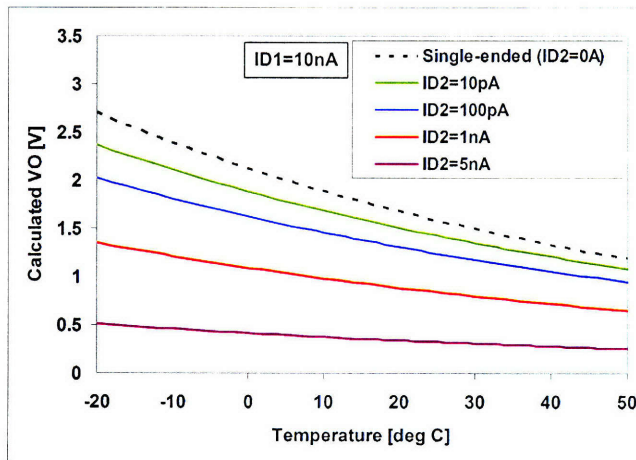
Figure 4-15: Calculated V_O versus temperature for the differential topology at several I_{D2}'s. Parameters used are from Table 3.2.

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The dependence of V_O on I_{D2} can be understood by rewriting $h(T, I_{D1}, I_{D2})$:

$$h(T, I_{D1}, I_{D2}) = (I_{D1})^{\frac{T}{C+nT}} - (I_{D2})^{\frac{T}{C+nT}} \qquad (4.19)$$

$$= (I_{D1})^{\frac{T}{C+nT}} \left(1 - \left(\frac{I_{D2}}{I_{D1}}\right)^{\frac{T}{C+nT}}\right) \qquad (4.20)$$

Equation 4.20 shows that when $I_{D2} \ll I_{D1}$, $h(T, I_{D1}, I_{D2}) \approx (I_{D1})^{\frac{T}{C+nT}}$, and the circuit transforms into the single-ended topology. As $I_{D2} \to I_{D1}$, $h(T, I_{D1}, I_{D2}) \to 0$, resulting in zero differential output. These behaviors are evident in Figure 4-14, where the $I_{D2} = 10pA$ plot approaches the single-ended plot, and the $I_{D2} = 5nA$ plot approaches zero. Therefore, the differential topology is a compromise between two extremes: 1) the single-ended topology that has the highest responsivity $(mV/^\circ C)$ but has zero common-mode rejection of threshold voltage shifts, and 2) the common-mode topology that has complete common-mode rejection of threshold voltage shifts but has zero responsivity.

In addition to changing the ratio of I_{D2}/I_{D1}, the circuit designer can also change I_{D1} and W/L [4]. The effects are identical to the single-ended topology because the expression for V_O has the same form. Namely, increasing I_{D1} will increase responsivity as shown in Figure 4-4, and increasing W/L will decrease responsivity as shown in Figure 4-5. Of course, the absolute responsivity for the differential topology will be lower than the single-ended topology's responsivity in Figures 4-4 and 4-5 because I_{D2} decreases responsivity, as shown previously in Figure 4-15.

So far, the differential V_O's curvature remains nonlinear versus temperature. To investigate how a differential topology can perform curvature correction, we need to look at a more practical implementation. This implementation replaces the two current sources with a current sink and current mirrors, as shown in Figure 4-16.

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[4] $W/L = W_1/L_1 = W_2/L_2$ because, as previously mentioned, both O1 and O2 have the same W/L to minimize device parameter variations.
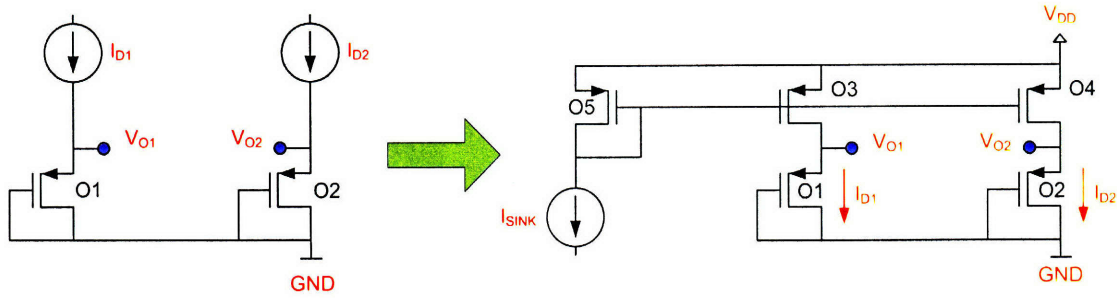
Figure 4-16: A more practical implementation of the differential topology.

In Figure 4-16, the branch currents are controlled by the mirror sizings as follows:

$$I_{D1} = I_{SINK} \left(\frac{W_3/L_3}{W_5/L_5} \right) \tag{4.21}$$

$$I_{D2} = I_{SINK} \left(\frac{W_4/L_4}{W_5/L_5} \right) \tag{4.22}$$

$$\tag{4.23}$$

We use simulation to investigate the new implementation because it requires iterative solutions. The chosen device sizes and currents are shown in Figure 4-17. I_{D1} is chosen to be $10nA$ and I_{D2} is chosen to be $1nA$ in order to have an even trade-off between responsivity and rejection of threshold voltage shifts (see Figure 4-15). Also, the chosen I_D's ensure that all transistors stay above-threshold.
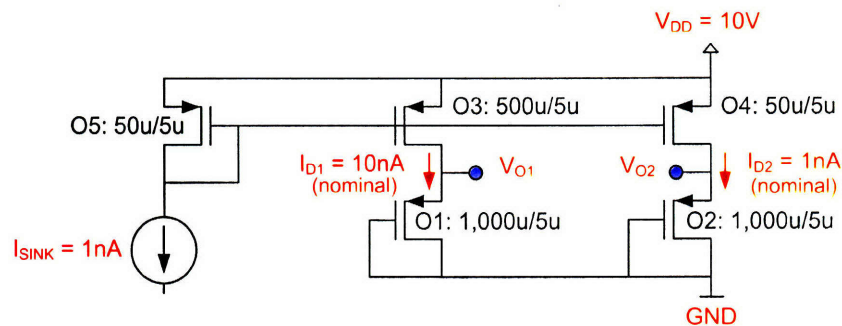
Figure 4-17: The differential circuit schematic used in simulation.

The simulated output voltages V_{O1} and V_{O2} along with $V_O = V_{O1} - V_{O2}$ are plotted in Figure 4-18.

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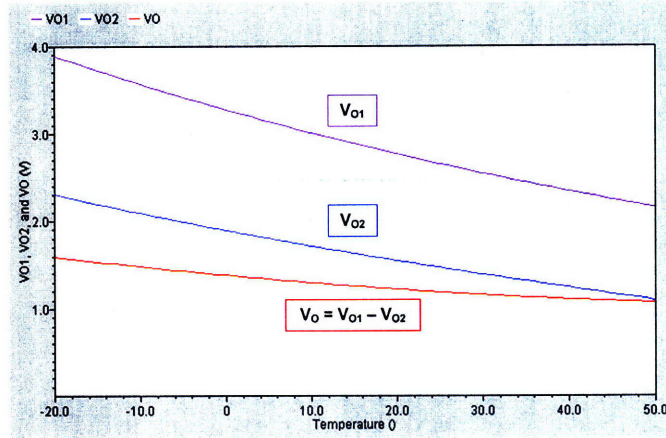
Figure 4-18: Simulated output voltages V_{O1}, V_{O2}, and V_O versus temperature for the differential topology. Parameters used are from Table 3.2.

As expected, both the differential and single-ended output voltages have concave shapes. Also, the differential output's responsivity at $27°C$ ($8mV/°C$) is indeed lower than the single-ended outputs' responsivities (V_{O1} : $25mV/°C$, V_{O2} : $17mV/°C$). However, we observe an interesting effect on V_O as I_{SINK} is varied. This effect is demonstrated in Figure 4-19.
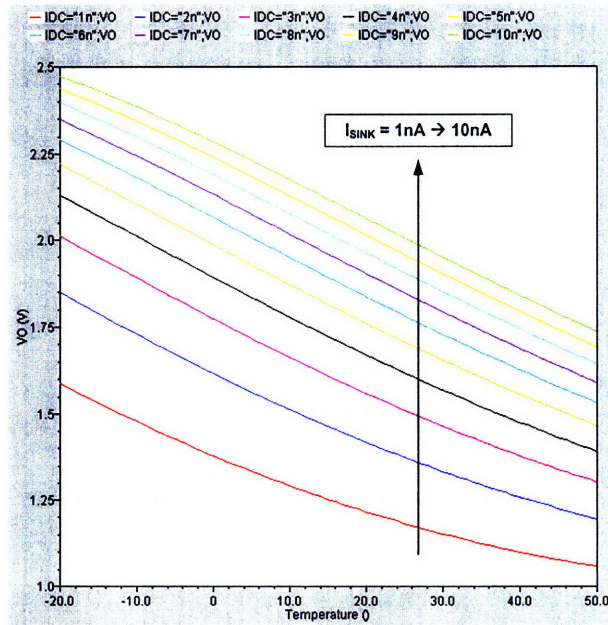
Figure 4-19: Simulated differential output voltage V_O versus temperature as I_{SINK} is varied from $1nA$ to $10nA$. Parameters used are from Table 3.2.

From Figure 4-19, we make three observations:

1. V_O's curvature progresses from being concave at $I_{SINK} = 1nA$ to being convex at $I_{SINK} = 10nA$. At $I_{SINK} = 6nA$, V_O is approximately linear versus temperature.

2. V_O is shifted higher with increased I_{SINK}. This is expected from Equation 4.20, which shows that a greater I_{SINK} (equivalent to a greater I_{D1} and a constant I_{D1}/I_{D2} ratio) increases $h(T, I_{D1}, I_{D2})$ and thus V_O.

3. Responsivities are within 5% of each other even as I_{SINK} is changed from $3nA$ to $10nA$.

We focus on the first observation because it offers a method of curvature correction for the differential V_O. To explain the dependence of V_O's curvature on I_{SINK}, we need to inspect I_{D1} and I_{D2}. We set I_{SINK} to $6nA$, and plot V_O, I_{D1}, and I_{D2} in Figure 4-20. Note that the simulated currents are negative by convention.
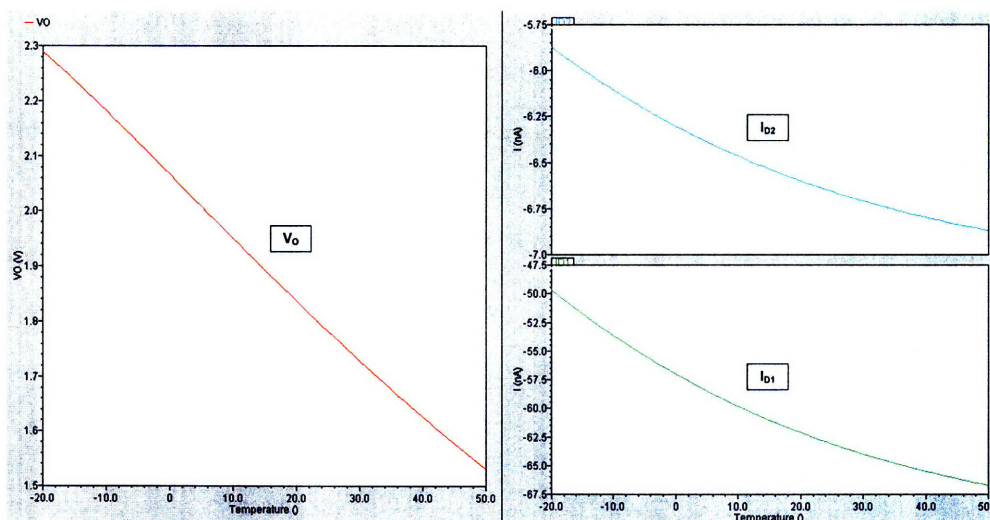
Figure 4-20: Simulated V_O, I_{D1}, and I_{D2} versus temperature at $I_{SINK} = 6nA$. Parameters used are from Table 3.2.

If the current mirror transistors O3 and O4 were ideal, then $I_{D1} = 60nA$ and $I_{D2} = 6nA$. However, in Figure 4-20, we observe that the currents increase in magnitude

as temperature increases, past their nominal values. To explain this, we refer to the OTFT's output characteristics shown previously in Figure 2-13, where the OTFT's I_D increases with V_{SD} in both linear and saturation regions due to increasing lateral electric field and due to finite output resistance, respectively.

The dependence of currents on V_{SD}'s prompts a closer inspection of the V_{SD}'s of the current mirror transistors O3, O4, and O5:
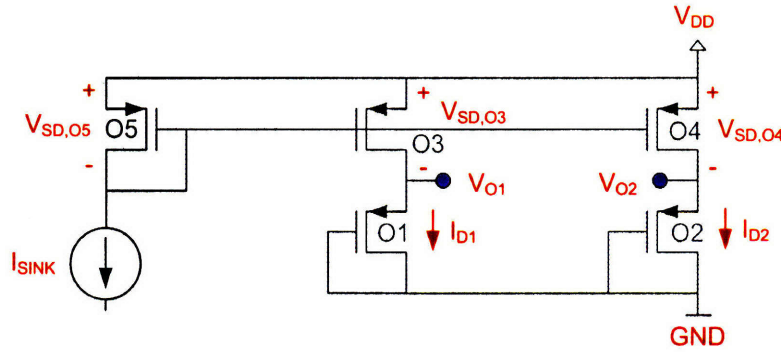

Figure 4-21: The differential circuit schematic showing the V_{SD}'s of the current mirror transistors.

- The V_{SD} of transistor O3 can be rewritten as $V_{SD,O3} = V_{DD} - V_{O1}$ as shown in Figure 4-21. Figure 4-18 and the single-ended topology show that V_{O1} decreases with temperature. Therefore, we conclude that O3's V_{SD} increases with temperature.

- The V_{SD} of transistor O4 also increases with temperature for the same reason as O3. However, $V_{SD,O4} > V_{SD,O3}$ because $V_{O2} < V_{O1}$, which is in turn because $I_{D2} < I_{D1}$ by design.

- The V_{SD} of transistor O5 is equal to $V_{SG,O5}$ because O5 is diode-connected. As seen in Figure 4-1, when the current is fixed as in the case of O5, V_{SG} decreases with temperature. Therefore, $V_{SD,O5}$ decreases with temperature.

For verification, the simulated V_{SD}'s of O3, O4, and O5 are plotted in Figure 4-22. From the markers in this figure, one also notices that $I_{D1} = 60nA$ and $I_{D2} = 6nA$ only when $V_{SD,O3}$ and $V_{SD,O4}$ are respectively equal to $V_{SD,O5}$.

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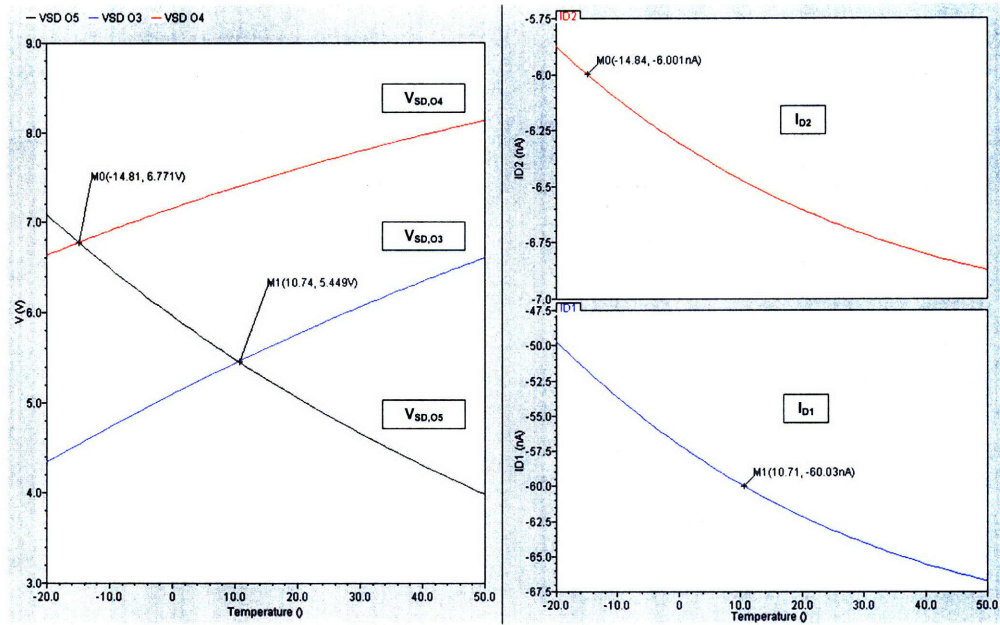
Figure 4-22: Simulated V_{SD}'s of O3, O4, and O5 versus temperature at $I_{SINK} = 6nA$. Parameters used are from Table 3.2.

In summary, the V_{SD} of O5 decreases with temperature, but the V_{SD}'s of O3 and O4 increase with temperature. Both trends lead to an increase in I_{D1} and I_{D2} with temperature. Next, we analyze how I_{D1} and I_{D2}'s temperature dependence affects V_O's curvature. To do so, we plot several scenarios of I_{D1} and I_{D2}'s temperature dependence.

(a) Constant I_{D1} and I_{D2}.

(b) Linear I_{D1} and I_{D2}.

(c) Saturating I_{D1} and I_{D2}.
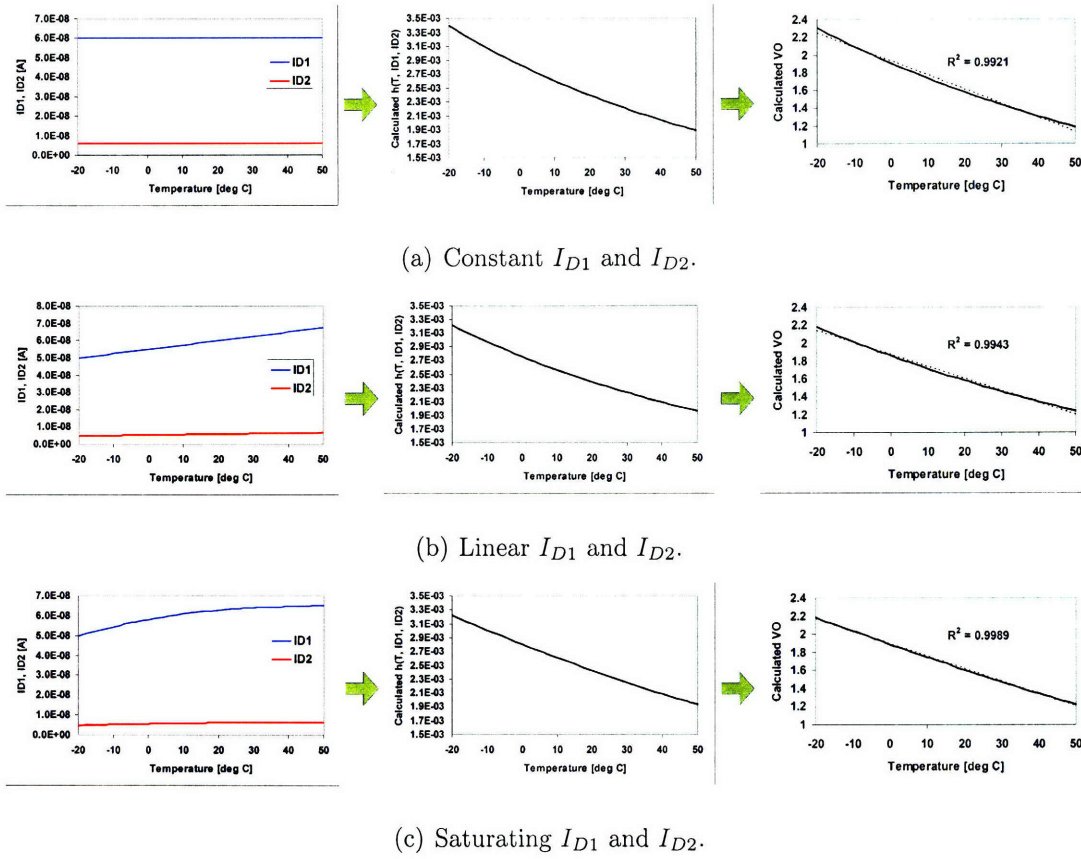
Figure 4-23: Three calculated scenarios of I_{D1} and I_{D2}'s temperature dependence and the resulting shapes of $h(T, I_{D1}, I_{D2})$ and V_O. R-squared values for linear V_O fit (dotted) are included. $I_{SINK} = 6nA$.

In Figure 4-23(a), the ideal scenario is presented. Here, I_{D1} and I_{D2} are constantly equal to their respective nominal values of $60nA$ and $6nA$. These ideal mirrors make the circuit equivalent to the original differential circuit presented in Figure 4-12. As expected, the V_O is concave. In Figure 4-23(b), I_{D1} and I_{D2} increase linearly with temperature. This scenario assumes that O3 and O4 are operating in the linear region of the output characteristic. Despite the linear increase in currents, V_O remains concave and its linearity only incrementally improves. In Figure 4-23(c), I_{D1} and I_{D2} increase with temperature, but with a saturating characteristic. This scenario assumes that O3 and O4 are in the wide transition region between linear and saturation region. As a result, the currents exhibit a convex shape. This leads to an $h(T, I_{D1}, I_{D2})$ that is slightly concave, and when multiplied by the slightly convex $g(T)$ (Figure 4-13), V_O

becomes linear and curvature correction is achieved.

Altogether, the differential topology offers two advantages over the single-ended topology. First, the differential setup allows common-mode rejection of threshold voltage shifts, albeit at the cost of temperature responsivity. Second, at a certain I_{SINK} bias setting, I_{D1} and I_{D2} acquire a particular saturating characteristic that corrects the curvature in V_O. In the next section, the measured results of the differential circuit are presented

4.2.2 Differential Topology Circuit Results

The differential temperature-sensing circuit's die photo and circuit schematic are shown in Figure 4-24. One difference between the actual circuit and the simulated circuit is that O1 and O2 are $10,000\mu m/5\mu m$ instead of $1,000\mu m/5\mu m$. The wider channel is a design choice that allows temperature sampling of a larger surface area. The wider channel also reduces the V_{O1} and V_{O2} for the same current, thus lowering the V_{DD} requirement. As mentioned in Section 4.2.1, the trade-off in using a larger W/L is a lower responsivity.

(a) Die photo.   (b) Circuit schematic.
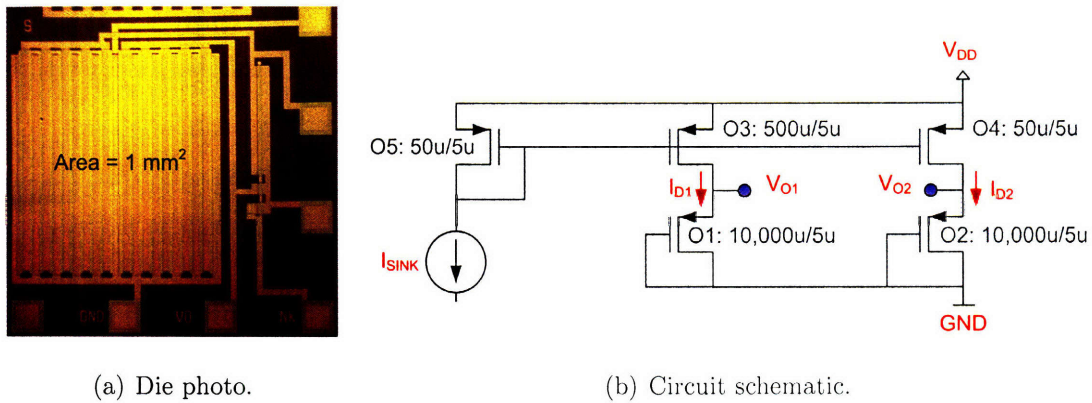
Figure 4-24: Die photo and circuit schematic of the fabricated differential temperature-sensing circuit.

First, the bias settings of the circuit need to be determined. Because of the wider O1 and O2, V_{DD} can be decreased from $10V$ to $4V$ and still provide sufficient headroom for V_{O1} and V_{O2}. Prior to setting I_{SINK}, we verify if the branch currents

indeed possess a saturating characteristic (Figures 4-20 and 4-23(c)) that is required for curvature correction. Figure 4-25 plots the total current supplied from V_{DD} (sum of I_{SINK}, I_{D1}, and I_{D2}) versus temperature as I_{SINK} is swept from $1nA$ to $10nA$.
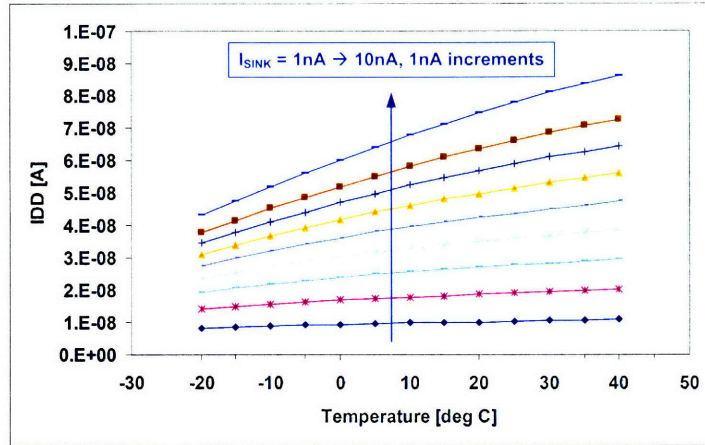
Figure 4-25: $I_{DD} = I_{SINK} + I_{D1} + I_{D2}$ versus temperature as I_{SINK} is swept from $1nA$ to $10nA$ in $1nA$ increments

Having confirmed the saturating characteristic in Figure 4-25, we can proceed to setting I_{SINK}. To do so, I_{SINK} is swept to determine the setting that yields the most linear V_O. This sweep is shown in Figure 4-26.
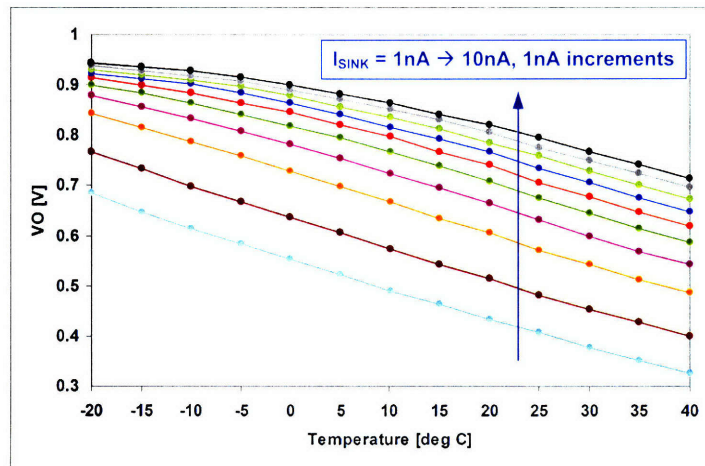
Figure 4-26: Measured differential output voltage V_O versus temperature as I_{SINK} is swept from $1nA$ to $10nA$ in $1nA$ increments.

Just as simulated in Figure 4-19, Figure 4-26 shows that V_O indeed shifts from a concave curvature to a convex curvature as I_{SINK} is increased. In addition, at between $I_{SINK} = 2nA$ and $I_{SINK} = 3nA$, V_O has the highest linearity. Therefore, we choose $I_{SINK} = 2.5nA$ as the bias current. Figure 4-27 summarizes the bias settings.
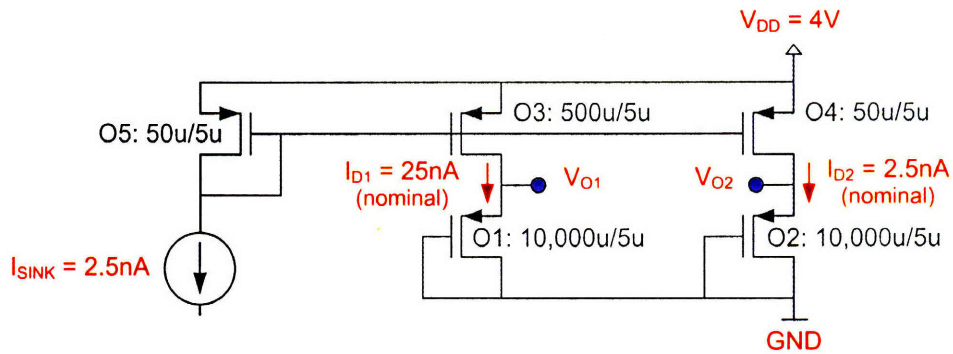
Figure 4-27: Differential circuit schematic with bias settings shown.

At this bias setting, we proceed to make a detailed measurement of V_O versus temperature. The measurement is done by sweeping the die temperature from $-20°C$ to $45°C$ in $5°C$ increments. At each temperature, 30 to 40 samples of V_O are taken at 1 sample/second. The raw data of V_O versus time is shown in Figure 4-28.
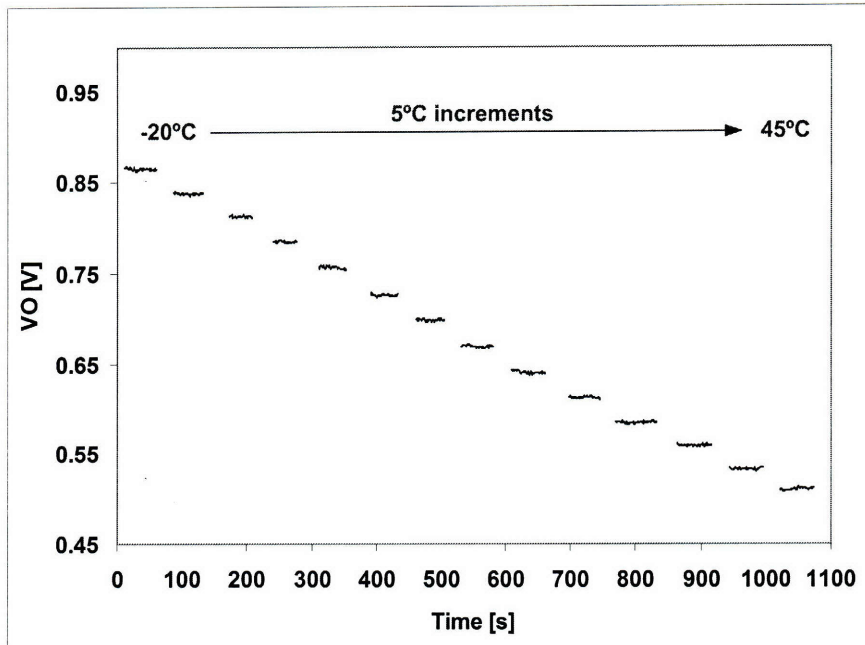
Figure 4-28: Measured V_O versus time as temperature is swept from $-20°C$ to $45°C$ in $5°C$ increments.

Just like the single-ended circuit, one can notice fluctuations in V_O at each temperature. These fluctuations are magnified in Figure 4-29.
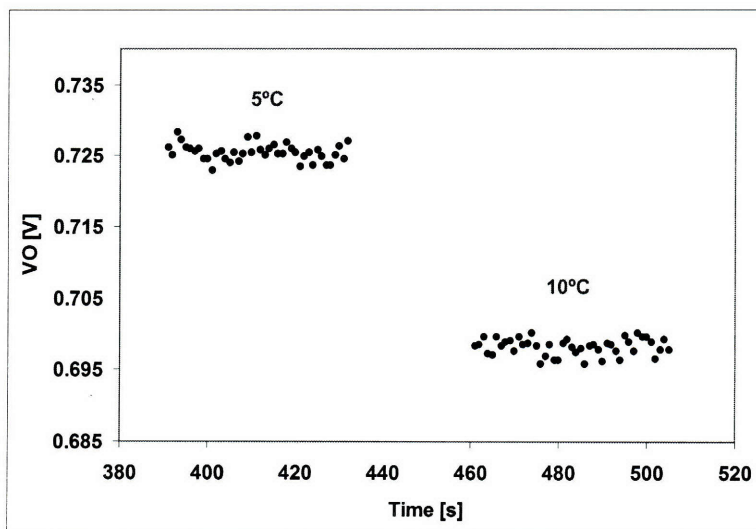
Figure 4-29: Measured V_O fluctuations at $5°C$ and $10°C$.

As done in Section 4.1.2, the fluctuations can be characterized by standard de-

viation and histogram. The standard deviation at each temperature is plotted in Figure 4-30. The standard deviations are $1.3mV$ on average, with a maximum of $1.6mV$ at $20°C$.
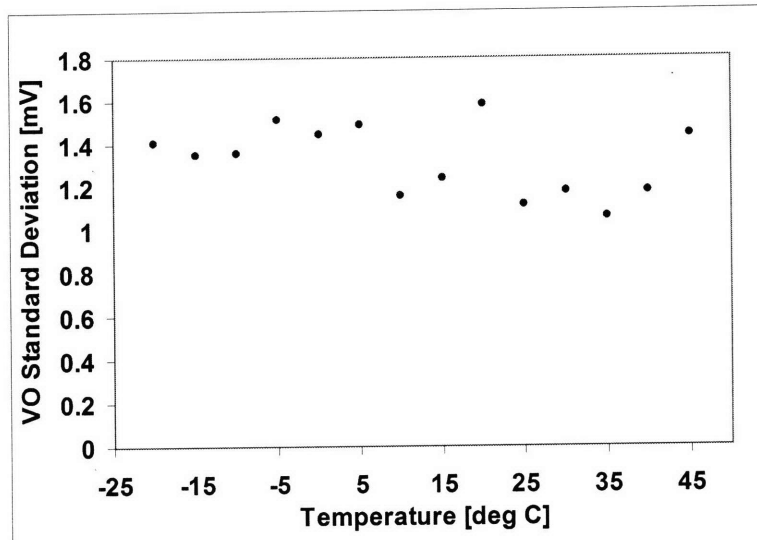
Figure 4-30: Standard deviations of sampled V_O at each temperature setting.

At the temperature with the highest standard deviation of samples $(20°C)$, a histogram of samples is plotted in Figure 4-31. The histogram shows a Gaussian-like distribution of samples.
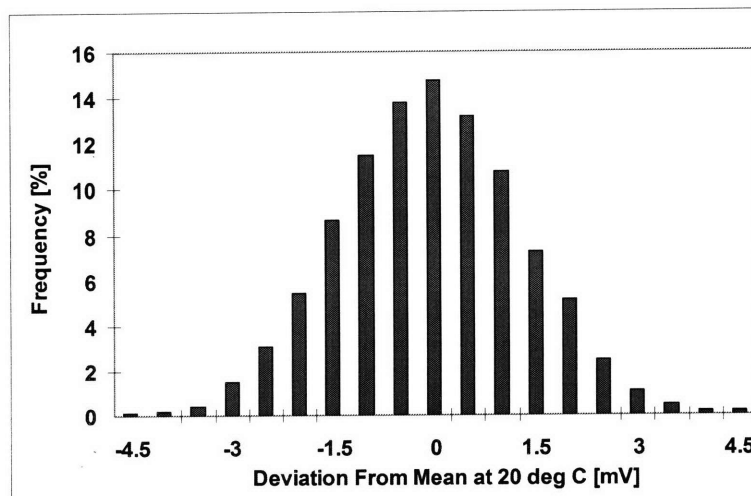
Figure 4-31: Histogram of sampled V_O at $20°C$.

Finally, the samples at each temperature are averaged to a single V_O value. These V_O values are plotted versus temperature in Figure 4-32. At each temperature, the standard deviation of the V_O samples is represented as a vertical error bar. The error bars are very small because the standard deviations of V_O are insignificant when compared to V_O. In addition, a best-fit line is superimposed on the data, with an R-squared value to gauge V_O's linearity.
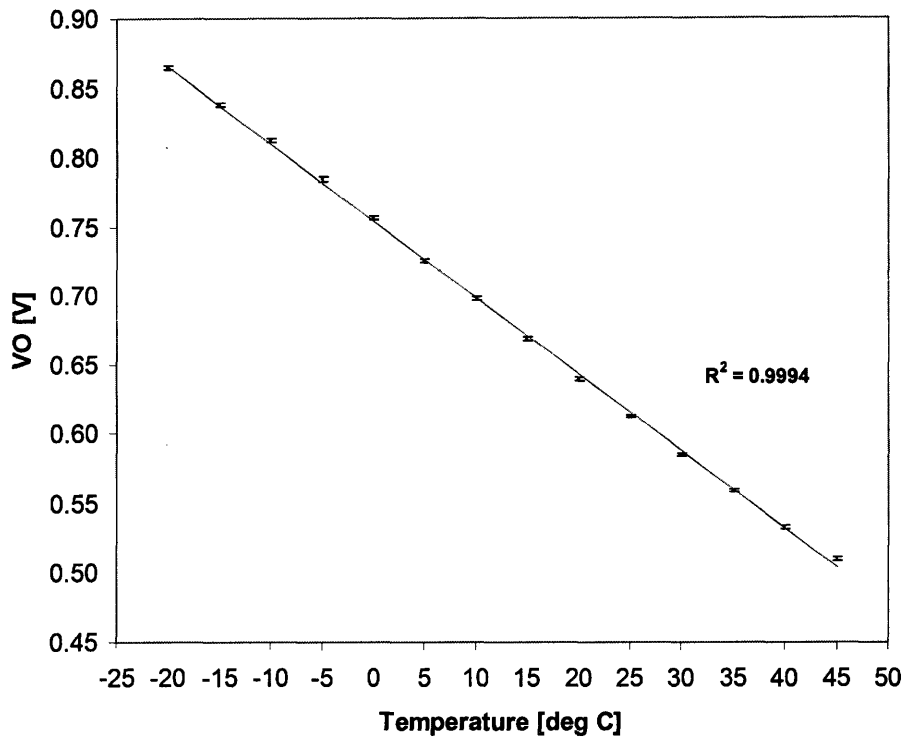
Figure 4-32: Averaged V_O versus temperature, with standard deviations of V_O samples as vertical error bars, and with a superimposed best-fit line (R-squared value displayed).

Several figures of merit for the temperature-sensing circuit are shown in Table 4.2.

Figure of merit	Value
Maximum power dissipation	$110nW$
Responsivity	$5.6mV/°C$
Sensitivity at 20 °C, $(\partial V/\partial T)(T[°K]/V)$	$2.3 \times 10^6 \; ppm$
Maximum standard deviation of samples	$1.6mV$ at $20°C$
Average standard deviation of samples	$1.3mV$
Average standard deviation of samples, in unit of temperature[a]	$0.23°C$
Maximum deviation from straight line	1.4% at $20°C$
Average deviation from straight line	0.44%

[a]Converted by dividing the average standard deviation of samples by the responsivity.

Table 4.2: Measured figures of merit for the temperature-sensing circuit shown in Figure 4-27

The above measured result is confirmed on a different die. This additional measurement, shown in Figure 4-33, yields a slightly higher responsivity ($5.9mV/°C$), a lower maximum power dissipation ($88nW$), and a greater linearity ($R^2 = 0.9999$). It should be noted that an increase in responsivity is possible by simply decreasing the channel widths of O1 and O2 because, as mentioned in Section 4.2.1, responsivity and power dissipation increase with the current densities of O1 and O2.
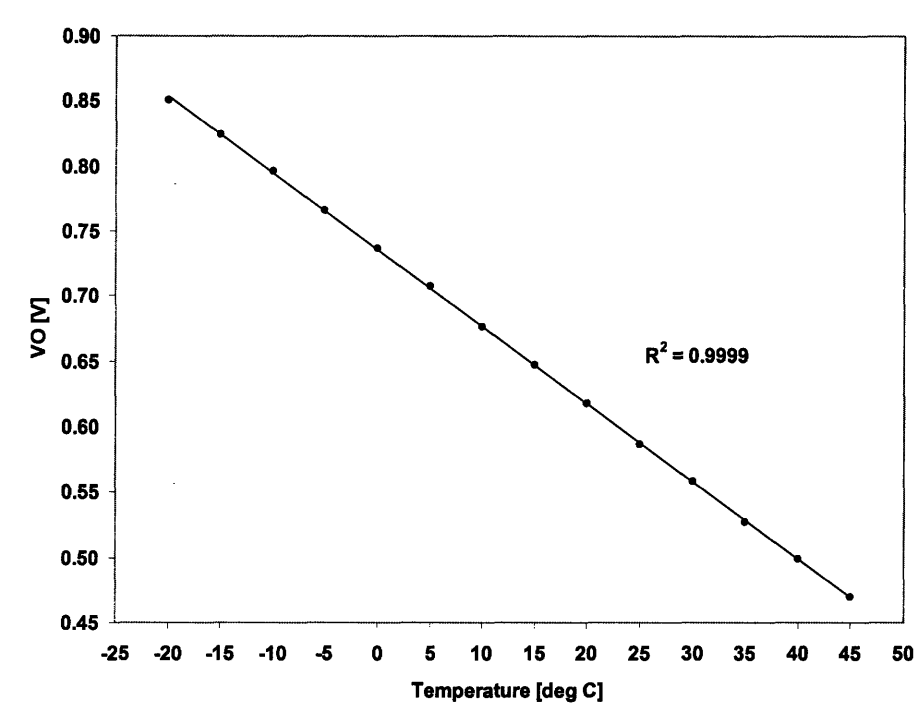
Figure 4-33: Averaged V_O versus temperature as measured on a different die, with a superimposed best-fit line (R-squared value displayed).

In summary, the differential OTFT temperature-sensing circuit is verified to perform as designed and as simulated. The differential circuit is tolerant of common-mode threshold voltage shifts and has a linear temperature response. As predicted, this linear response comes at the cost of decreased temperature responsivity when compared to the single-ended circuit.

Chapter 5

Conclusion

The goal of this work is twofold: the understanding of the OTFT's temperature characteristics, and the creation of OTFT temperature-sensing circuits.

For the first goal, we begin with electrical characterizations of the OTFT. From these characterizations, we find OTFTs' I-V characteristics to be similar to those of silicon MOSFETs. However, we notice that OTFTs have different temperature characteristics. This difference is due to the OTFT's population of trap states inside the bandgap. From this physical reasoning, a DC OTFT circuit model is developed. The model development is based on the RPI a-Si model, and offers a physical understanding of the OTFT's temperature dependence. The model is verified to be an excellent match to the characterized data in all regions of device operation and at different temperatures.

With the understanding of the OTFT's temperature characteristics and with a model as a circuit design tool, we proceed to design OTFT temperature-sensing circuits. Two circuit topologies are presented. The single-ended topology achieves high responsivity at low-power. However, the single-ended output is nonlinear with temperature and is dependent on threshold voltage shifts. Both problems are addressed by the differential topology, which has a highly linear temperature response and is tolerant of common-mode threshold voltage shifts.

Both circuits exceed silicon temperature sensor's temperature responsivity while dissipating less power. These traits, along with the OTFT's ability to be fabricated

on large-area and flexible substrates, allow OTFT temperature sensors to be used in both existing and new application environments.

Appendix A

OTFT Model's Verilog-A Code

```
// VerilogA for OTFT_Circuits
`include "constants.vams"
`include "disciplines.vams"

module OFET(G, S, D);
inout G, S, D;
electrical G, S, D;

parameter real AA = 1.65e-8;
parameter real ASAT = 0.64;
parameter real DD = 0.62;
parameter real DEF = 0.2;
parameter real DELTA = 120;
parameter real L = 5e-6;
parameter real MSAT = 4.4;
parameter real N = 1.5;
parameter real T = 27;
parameter real VTRAP = 0.021;
parameter real VMIN = 0.01;
parameter real VT = -1;
```

```
parameter real W = 1000e-6;


real ID, k, q, TKel, VDS, VSDE, VGS, VGT, VGTE;


analog begin
  k = 1.3807e-23;
  q = 1.6e-19;
  TKel = T + 273.15;


  VGS = V(G,S);
  VDS = V(D,S);
  VGT = -VGS+VT;
  VGTE = VMIN/2*(1+VGT/VMIN+sqrt(DELTA*DELTA+pow(VGT/VMIN-1,2)));


  begin
  if (VDS < 0)
    begin
      VSDE = -VDS/pow((1+pow((-VDS/(ASAT*VGTE)),MSAT)),1/MSAT);
      ID = AA*W/L*pow(VGTE,N)*VSDE*exp(-DEF*q/(k*TKel))*2*k*TKel/...
           ...(2*q*VTRAP-k*TKel)*pow(DD*VGTE,2*VTRAP*q/(k*TKel)-1);
    end
  else
    ID = 0;
  end
  I(S,D) <+ ID;
  I(G,D) <+ 0;
  I(G,S) <+ 0;
end
endmodule
```

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