THE DESIGN OF AN ARRAY PROCESSOR FOR PATTERN RECOGNITION STUDIES

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ABSTRACT

Present day general purpose digital computers can, in theory, solve any well defined problem. However, they are relatively inept at solving problems, such as pattern recognition, in which the data is in spatial form. Efficient handling of spatially arranged data can only be accomplished by a machine capable of some form of parallel action. One such machine is a rectangular array of logical modules controlled by a conventional computer. The design of such an array is discussed in the light of size, cost and speed requirements. Two alternate designs are proposed, one using Cryotrons, the other Tunnel Diodes. The sole advantage of the tunnel diode array is its speed, while both its power and size requirements are considerably larger than is desirable. The Cryotron array, while slower, is potentially less expensive to build, requires less power and occupies less space.

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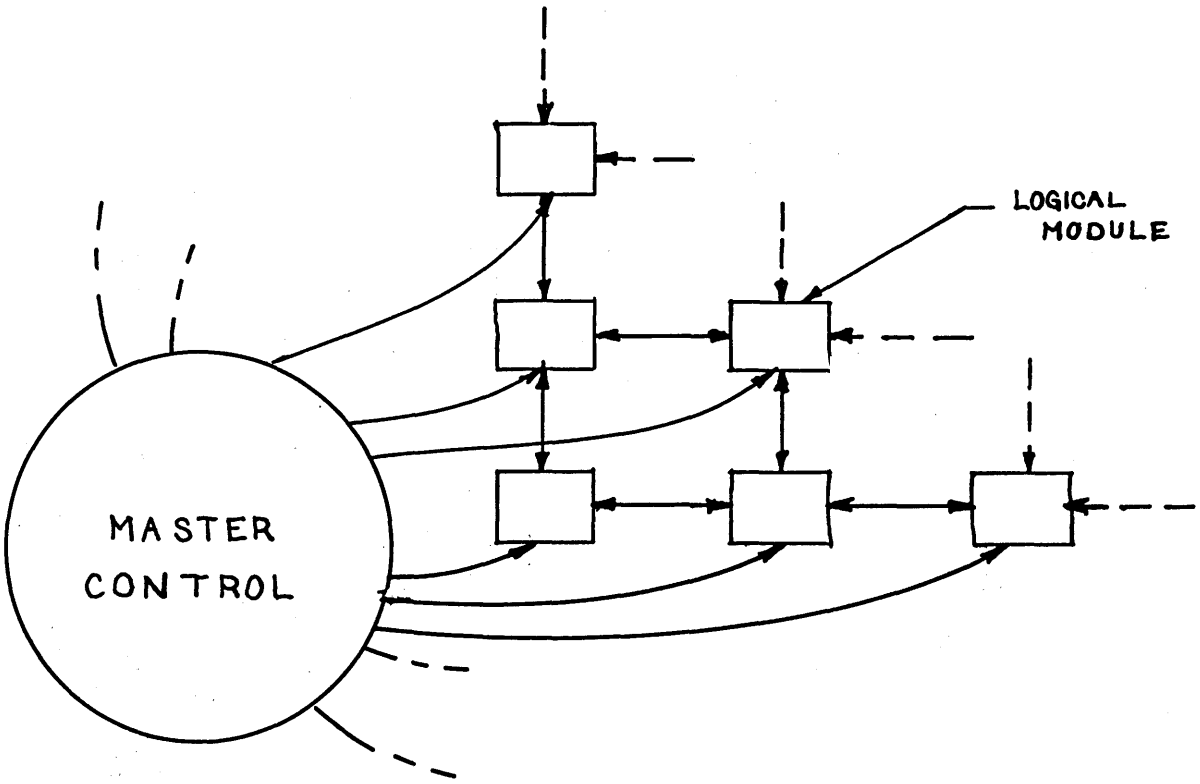
INTRODUCTION

Background

Present day general purpose digital computers can, in theory, solve any well defined problem. However, they are relatively inept at solving problems in which the data is arranged in a spatial form. While the machine may greatly surpass human capabilities in arithmetic computation and solution of linear differential equations, it is incapable of playing a game of chess with a competent human opponent. Another field in which the machine cannot perform as well as its designers is pattern recognition. Both of these problems have the data arranged in a spatial form, and the difficulty seems to be that the computer is only capable of handling a small amount of data at one time. Efficient handling of spatially arranged data can only be accomplished by a machine capable of some form of parallel action.

S.H. Ungar [1,2] has proposed that such a "spatial computer" be composed of a rectangular array of logical modules and a master control (see Fig. 1). Each module communicates with its four neighbors, and receives orders from the master control, which is itself a conventional digital computer. Pattern recognition has been carried out successfully on an IBM 704 computer which has been programmed to simulate the array of modules. Since the 704 must perform the parallel operations serially, this simulation is considerably slower than the "spatial



Organization of a Spatial Computer

Figure 1

computer" would be.

Scope of Thesis

The purpose of this thesis is to investigate the feasibility of building such an array processor (abbreviated AP) for pattern recognition. The nature of the problem dictates that the AP be of considerable size, a 32 x 32 array may be considered a minimum for a typical problem. This large number of modules accentuates the problems of size, cost of components and power requirements. It is also necessary that the speed of the AP be comparable to that of the high speed conventional computer used as a master control.

Section I will deal with the specifications which the AP has to meet in order to be able to solve the pattern recognition problem, and will present a logical design capable of meeting those specifications.

Section II will present two alternatives for the design of the basic hardware of the AP. One utilizes tunnel diodes and magnetic cores, the other thin film cryotrons. For the purposes of this thesis I have assumed that both these components are available in quantity at a cost considerably below that of a tube or a transistor.

Section III discusses the merits and drawbacks of each alternative and reaches a conclusion as to which would result in an AP closer to optimum at reasonable expense.

SECTION I

Circuitry Requirements

Each module of the AP will have its own one bit accumulator, random access n-bit memory, and logical circuitry which will enable it to perform the basic operations which are needed to solve pattern recognition problems.[1]

In addition to performing these basic operations, through use of the master control, it should be possible to: read out the number of ones in any row or column, isolate any portion of the array so that operations will be performed only in that section, and to create a random array.

Basic Operations

The basic operations, mentioned above, which the computer must perform are:

Order	Abbreviation	Meaning
add	ADD	add logically the contents of the *specified address to the contents of the accumulator
multiply	MPY	multiply logically the contents of the *specified address to the contents of the accumulator
complement	COM	complement the contents of the accumulator

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*Specified address refers to any one of the n memory bits or the accumulator above (or below, or to the left, or to the right) of the module.

store	STO	store the contents of the accumulator in the specified memory bit
shift right	SHR	shift the contents of the accumulator to the accumulator to the right (or left, or above, or below). The modules on the left (or right, or lower, or upper) edge of the array will have zeros set in the accumulator.
shift right around	SRA	same as shift except that the contents of the accumulator on the right (or left, or upper, or lower) edge of the array will be shifted around to the module on the left (or right, or lower, or upper) edge.
link	LNK	record in memory elements located between adjacent pairs of modules whether or not ones are contained in both accumulators. (Diagonally touching modules are considered adjacent for this command and the next one.)
expand	EXP	add logically ones to the accumulators of those modules connected through a chain of active

inter-module memory elements of the kind specified in the order (horizontal, vertical, positive diagonal, or negative diagonal) to some module with a one in its accumulator.

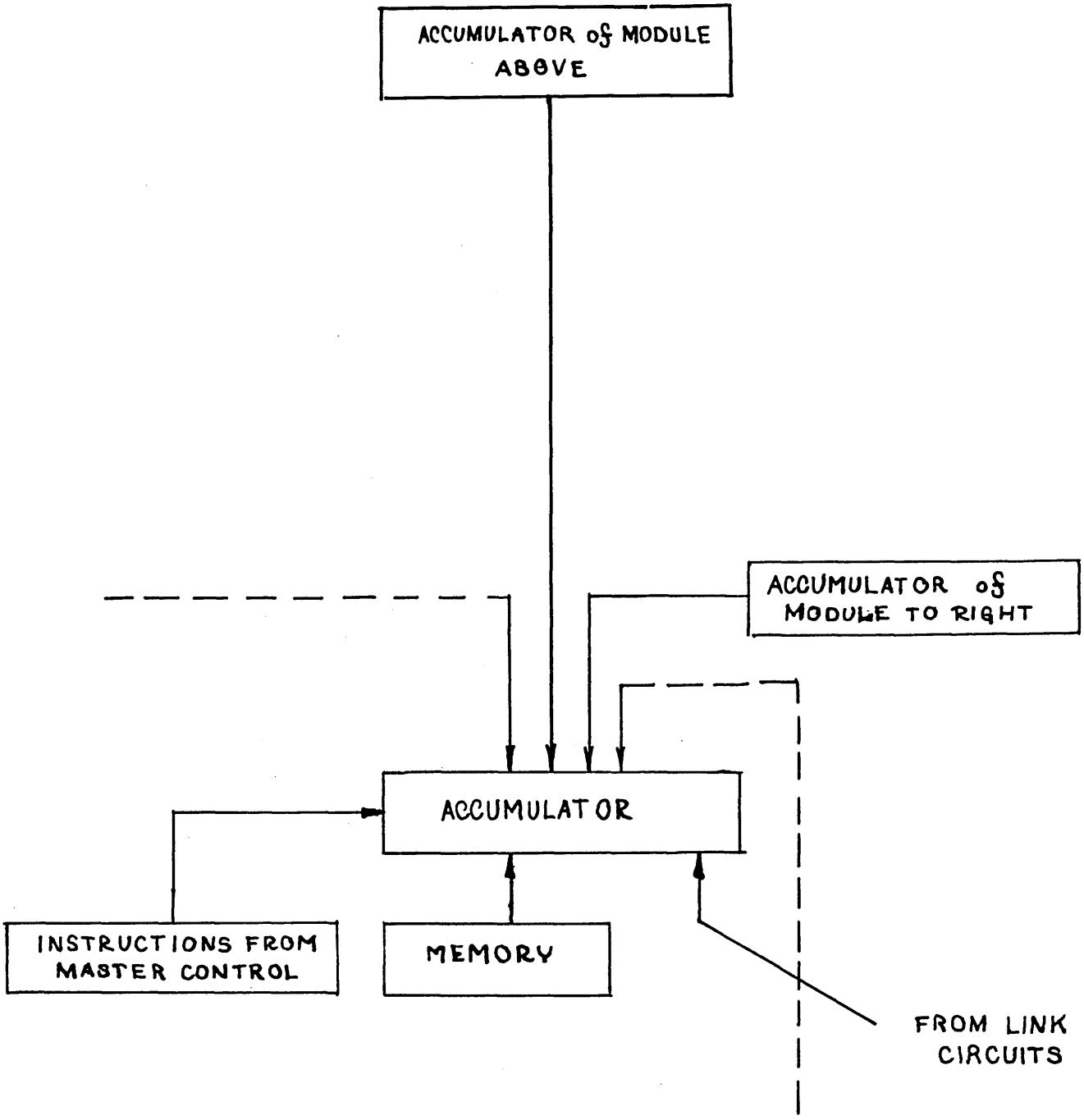
Logical Design

A schematic diagram for a typical module of the AP is shown in Fig. 2.

Random arrays may be generated by continual reading into the first column of the AP, random numbers generated in the master control, and shifting these across the array. The reading out of the number of ones in any row or column may be accomplished by placing a binary counter (see Fig. 3) at the end of each row or column. By shifting 32 times the counter will record the number of ones in the row (or column). The contents of the counter can be fed to the in-out register of the master control and stored in its memory.

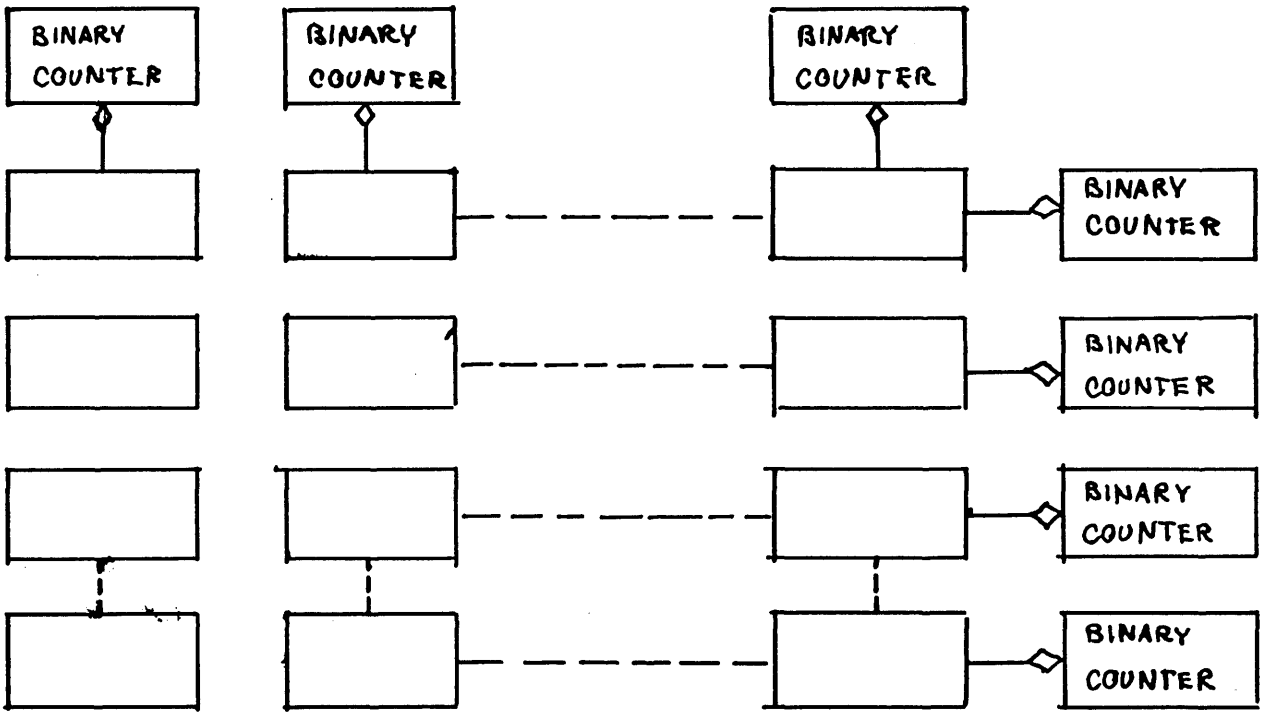
The isolation of any portion of the array may be accomplished by the insertion of "and" gates in the links between the master control and each module. The inputs to these "and" gates can be controlled by the master control.

The special circuity needed in the modules on the edges of the array to perform the "shift" and "shift around" operations is shown in Fig. 4.



Schematic Module Circuitry

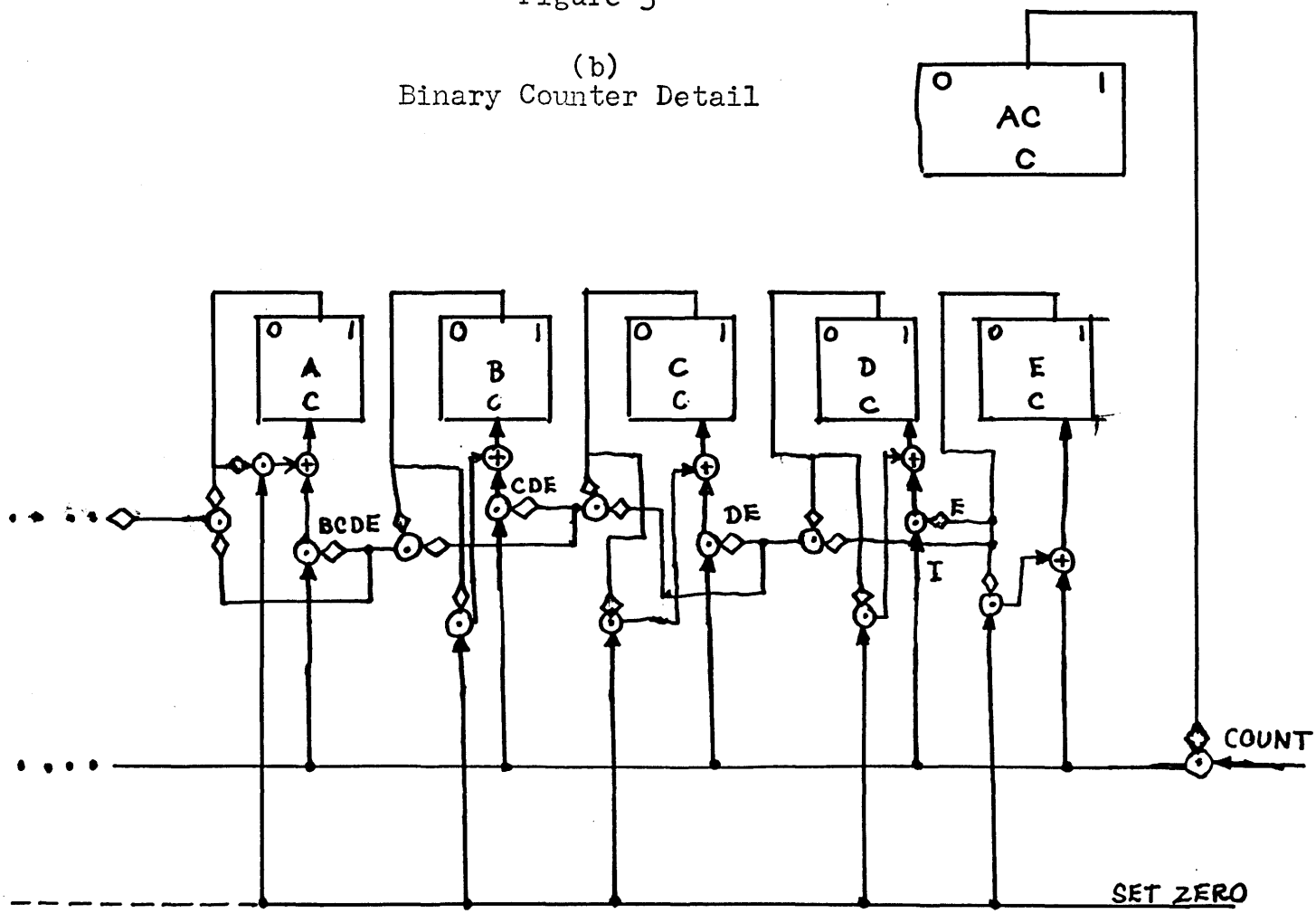
Figure 2

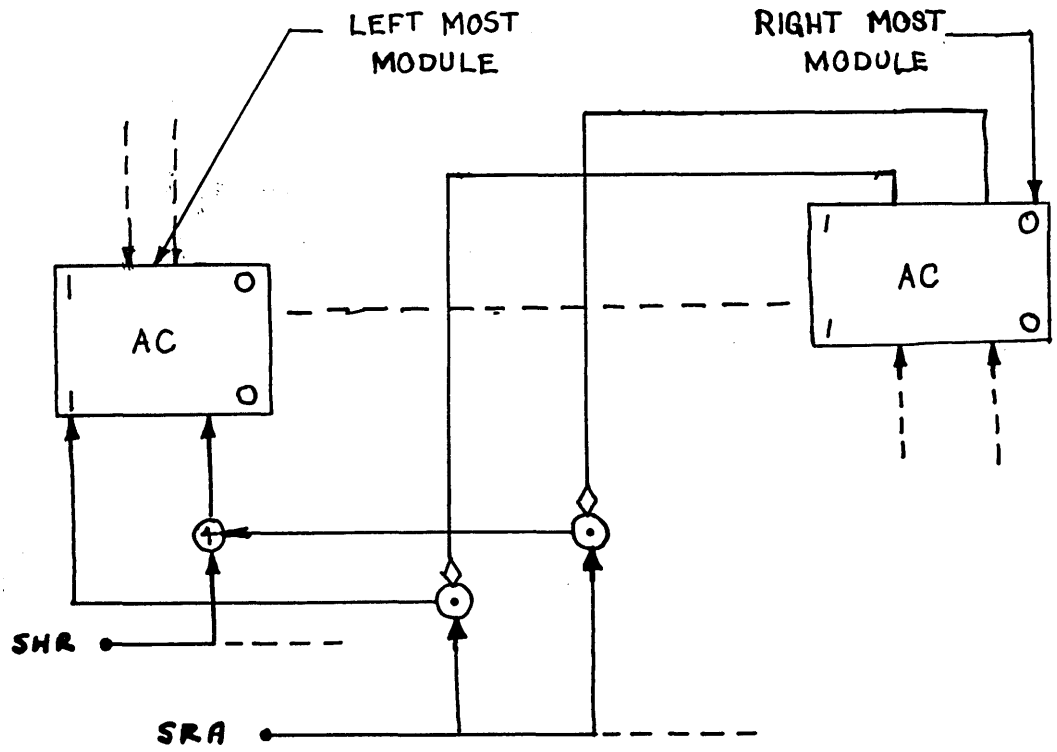


(a)
Read Out Array

Figure 3

(b)
Binary Counter Detail





Shift Logic of Modules on

Edge of Array

Figure 4

SECTION II

Tunnel Diode

A new electrical device whose v-i characteristic has a negative resistance region is the tunnel diode. (see Fig. 5) This negative resistance region allows us to construct a bistable device which we can use as a flip flop in the AP.[3] (see Fig. 6) The principle of operation of the flip flop is as follows: The D.C. source which supplies the two series-connected diodes has a magnitude which constrains one diode to be in the high voltage-low current state, while the other is in the low voltage-high current state. The difference in the diode currents flows through the inductor. Under steady state conditions, there is no voltage drop across the inductor. However, when an input pulse triggers the zero diode to one a voltage is induced across the inductor which sets the other diode from one to zero.

Logic Circuits Using Tunnel Diodes

Conventional diode gates cannot be used to perform the logical operations in the module for the following reasons: It is necessary to have an inverter circuit, which is impossible to construct using only conventional diodes. The diode gates do not have a "logical gain", [A] so they cannot be cascaded in sufficient numbers to perform the logic. The tunnel diode flip flop has a voltage range from 50mv to 450mv while a conventional diode is

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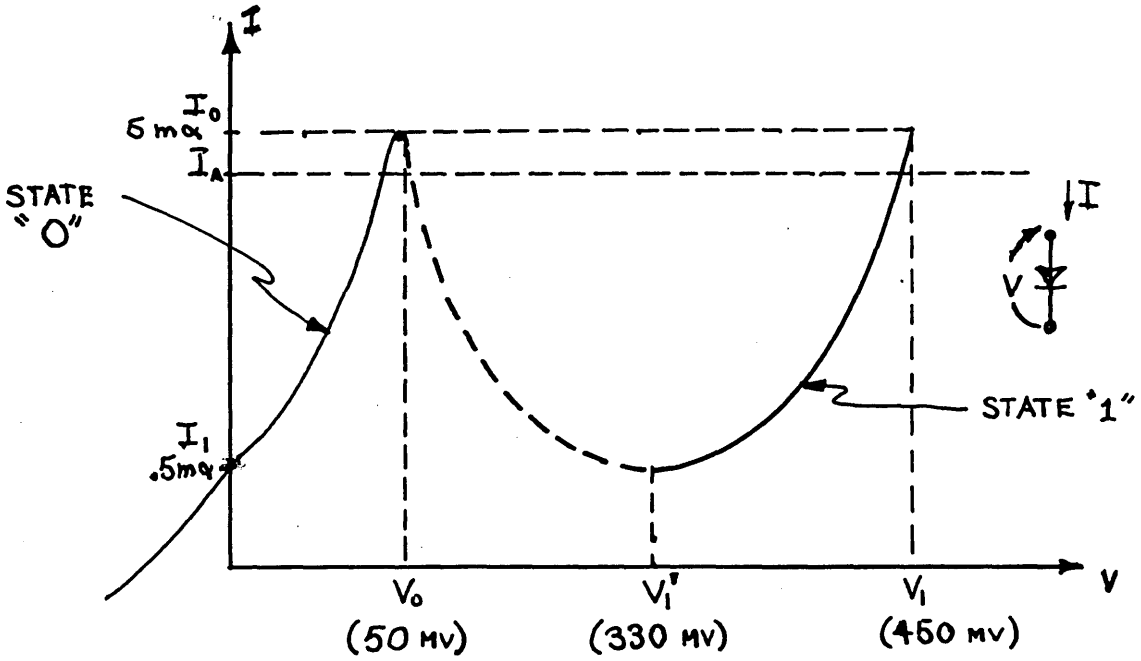
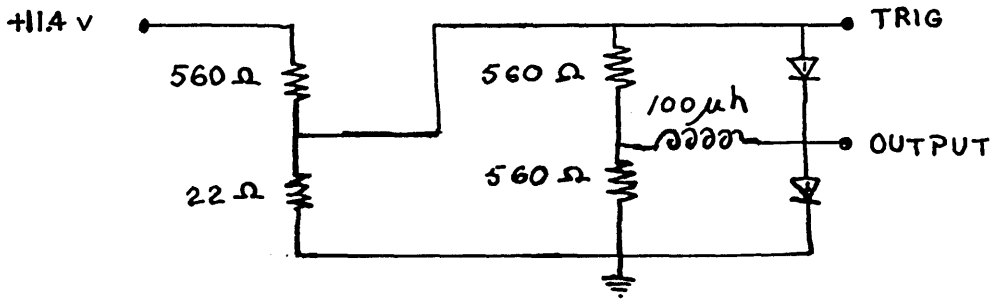
A. See Appendix for detailed explanation of "logical gain" and why cascading of diode gates is impractical.



Tunnel Diode Static Characteristic[4]
(Values indicated for a typical Germanium unit)

Figure 5



Tunnel Diode Flip Flop

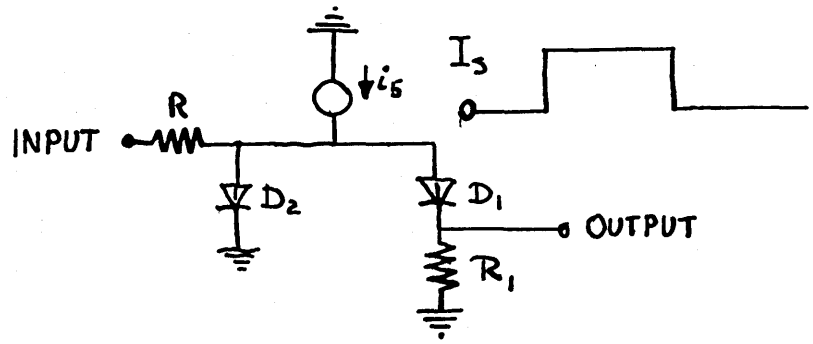
Figure 6

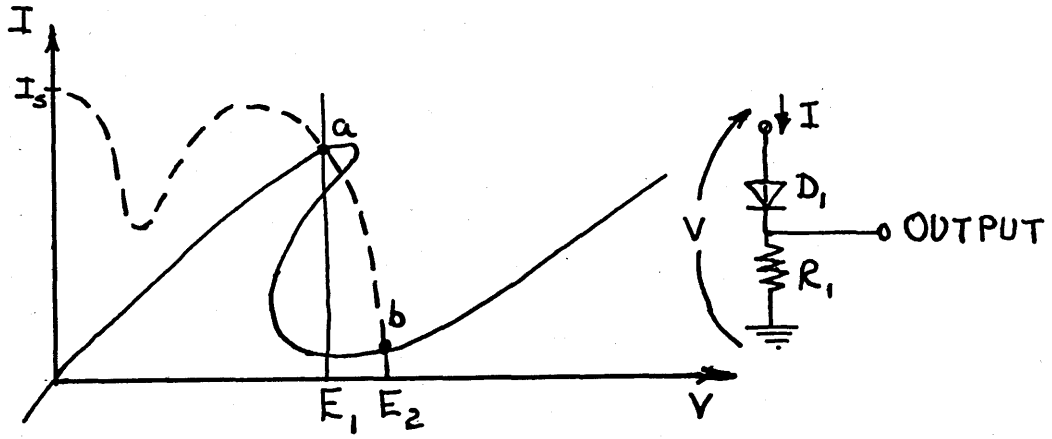
extremely non-linear and cannot be operated satisfactorily in this region. Hence, the two components are not compatable.

For these reasons it was decided to use tunnel diode logic circuits. Since the tunnel diode is a bistable device which will not return to the zero state when its inputs are removed, in order for our logic circuits to be combinational (i.e. have no memory) we must reset the device after each set of inputs. Momentary removal of the power supply is the method used to reset the gates. The sequence of operation of the device is as follows: Having been reset, the device is in a given state, if the combination of inputs is favorable it will switch to the other state. The state of the device is then detected by the next stage of the computer. Finally the device is reset and is ready to receive new inputs.

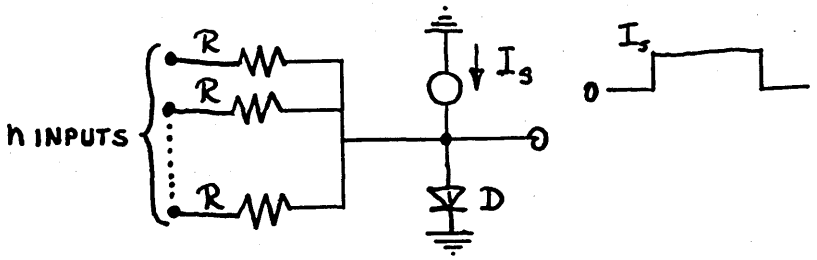
The timing of the reset pulse is crucial in the case of the inverter. Once the device has been reset it will immediately return to the one state if there is not a one input to the inverter, and a subsequent one will not change the circuit back to the zero state. This means that we cannot reset the inverter circuit until after the contents of memory have been put in the Memory Buffer Register. All the other logic gates may be reset at the same time the inverter is reset without introducing any logical ambiguity. The tunnel diode inverter[4] is shown in Fig. 7a; here is how it operates. The composite load line of a tunnel diode D_1 in series with a resistor is the

(a)
Inverter Circuit



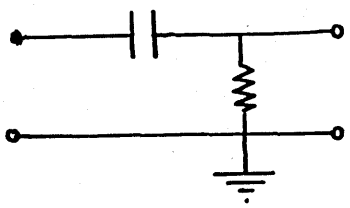


(b)
Characteristic of D_1 and R_1 in Series, and Load Curve Formed by D_2 and I_s
Figure 7



Tunnel Diode "And" Gate

Figure 8



Differentiator

Figure 9

solid curve in Fig. 7b. Another tunnel diode D_2 is used to simulate a voltage source giving us the circuit in Fig. 7a. The load-curve determined by D_2 and I_s is the dotted curve in Fig. 7b. Points a and b are the only stable operating points. Taking the voltage across R_1 as the output, we see that point a gives a high output (high current through resistor; high voltage) and point b gives a low output (low current through resistor; low voltage). Thus if the curcuit is always at a for a zero input and at b for a one input we have an inverter. If we select V_1 as our zero output voltage level and $V > V_2$ for our one output voltage the required operation is achieved.

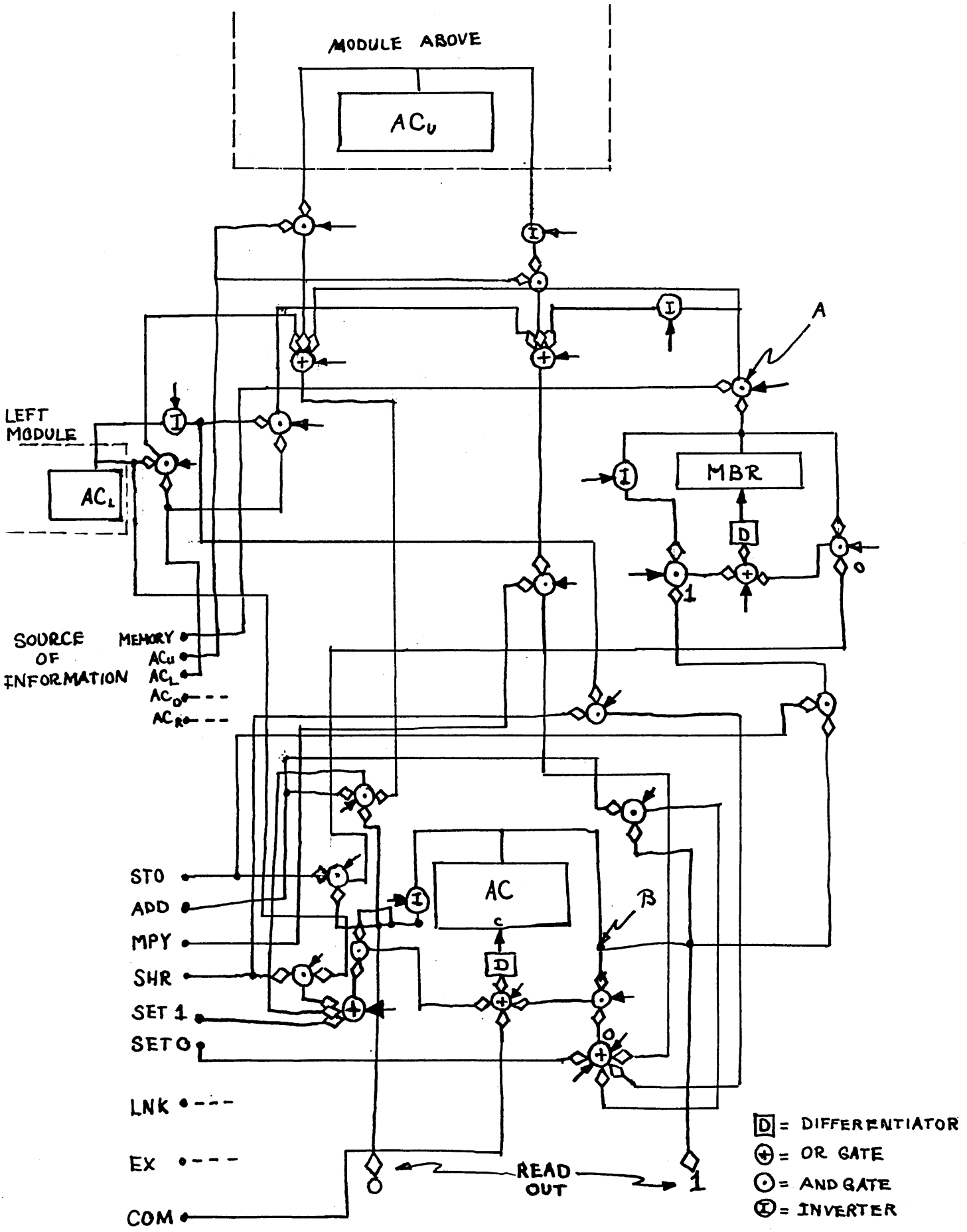
For our "and" and "or" gates we will use the circuit shown in Fig. 8[4]. As long as the tunnel diode is in the zero state the current into D in addition to I_s is $M(V_1-V_0)/R$, where M is the number of inputs which are one. The diode will switch when $I_s+M(V_1-V_0)/R > I_0$. Once it has switched it will remain in the one state even though the current falls well below I_s (which corresponds to loading), thus the curcuit is capable of "logical gain". By appropriate selections of I_s we can make M equal 1,2 ...n. When M equals 1 we have an "or" and when M equals n we have an "and" gate. In order to trigger the flip flop with the output of a logic gate it is necessary that a differentiator (Fig. 9) be inserted in series with the input. The differentiator will take the zero to one level change of the gate and convert it into a pulse of

sufficient magnitude to trigger the flip flop. In actual practice the flip flop itself will supply the parallel resistor, so all we need do is insert a capacitor in series with the trigger input. The module and link logic designed using tunnel diode logic circuits is shown in figures 10 and 11. The reset pulses are schematically represented by the arrows.

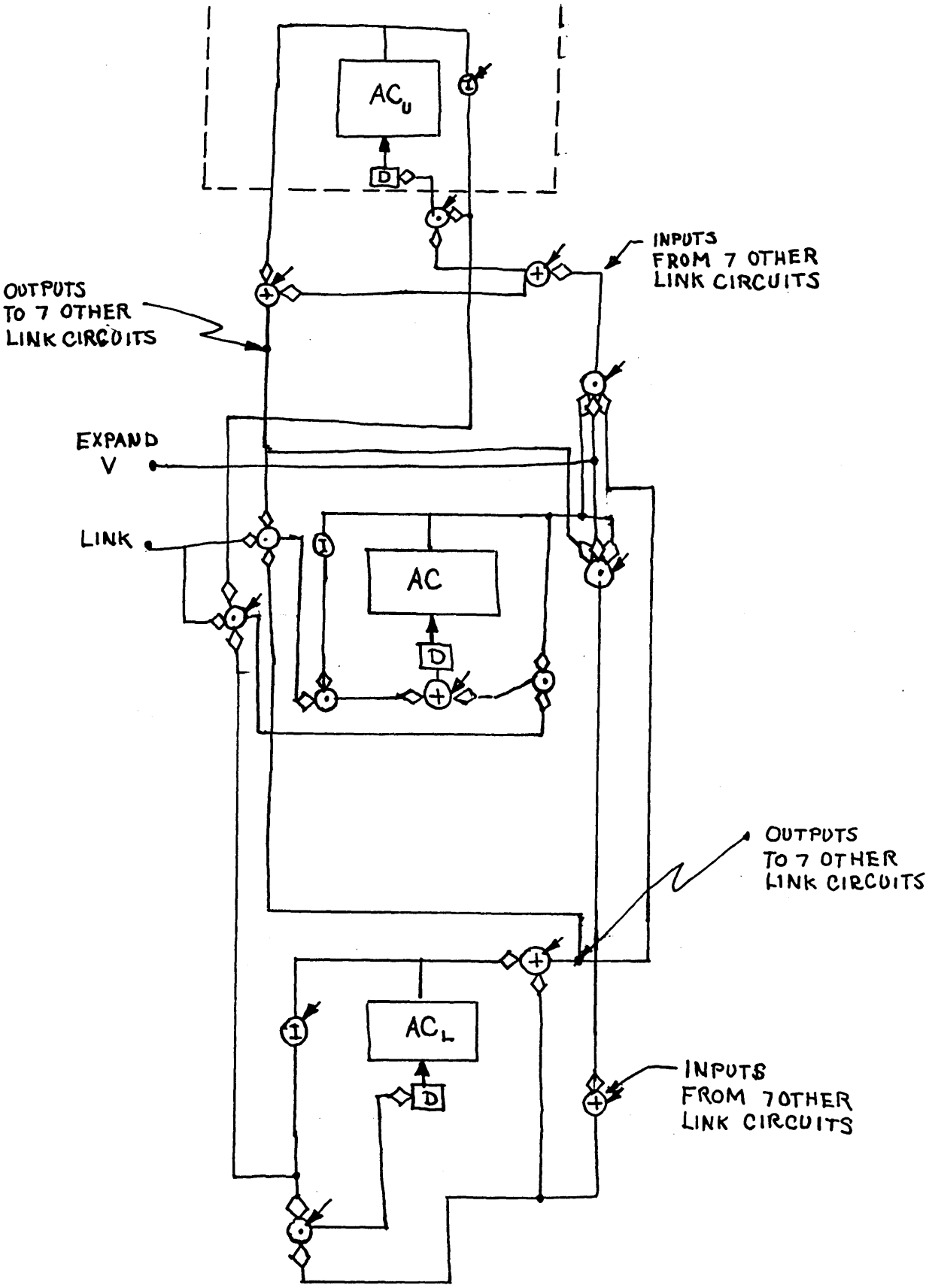
Principles of Operation of a Magnetic Core Memory

The hysteresis loop of a ferrite core (see Fig. 12) suggests that it can be utilized as a bistable device to store information. Let us establish the convention that a current of I_a is sufficient to set the core in the one state and that a pulse of $-I_a$ is sufficient to set the core in the zero state. Once the core is set in either state it will stay there indefinately until it is disturbed by another pulse of sufficient magnitude to change the state of the core.

By applying a pulse of $-I_a$ the core is set in the zero state and is ready to be used as a memory element. It is now either set in the one state by a current of I_a (I_{ri} or read-in current) or left in the zero state, depending on which digit we wish to store in memory. We can tell whether a zero or a one is stored in the core by pulsing the core with $-I_a$ (I_{ro} or read-out current). If a zero is stored in the core the core will not change state and the voltage across the core will remain constant. If a one is stored the core will change state and a voltage will appear across it. This change in voltage is detected

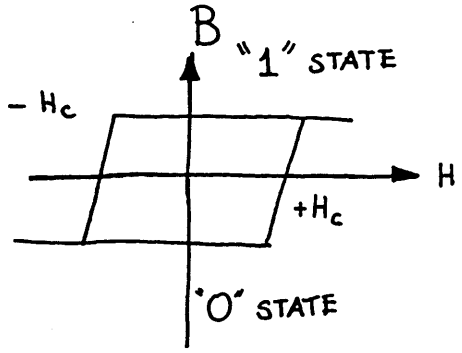


Module Logic Using Tunnel Diodes
Figure 10



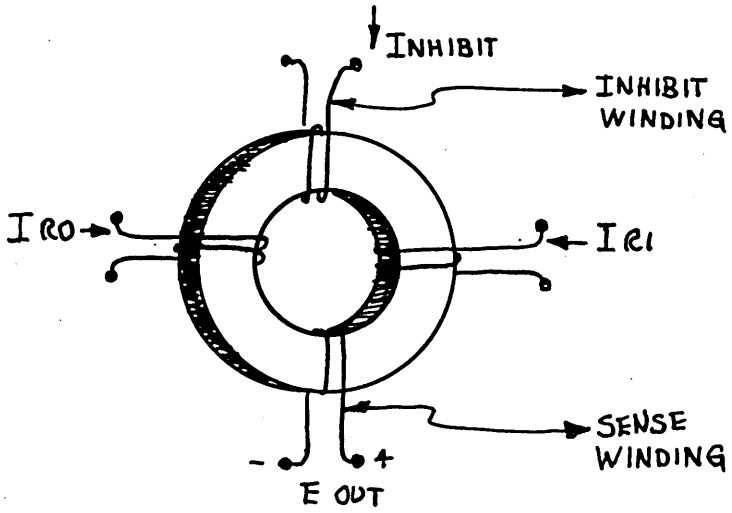
Link Logic Using Tunnel Diodes

Figure 11



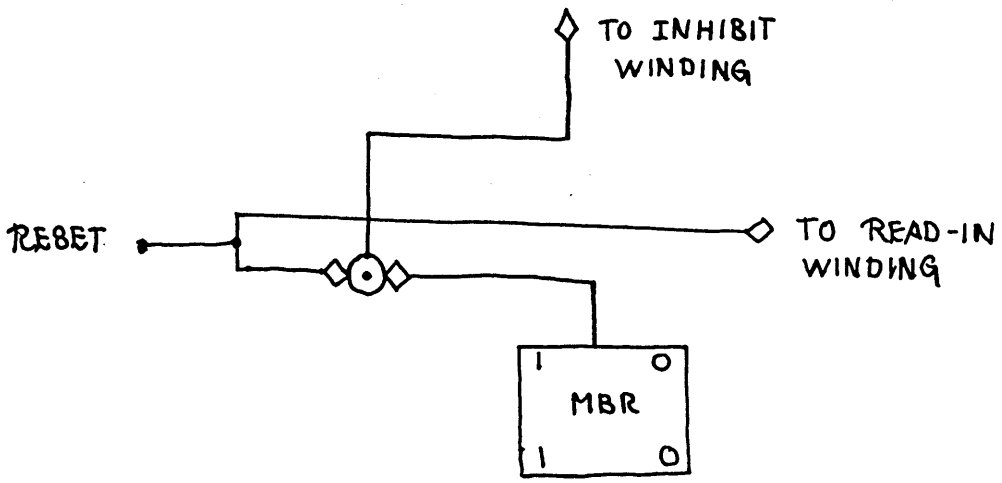
Ideal Hysteresis Loop of Ferrite Core

Figure 12



Schmetic Representation of Windings on Ferrite Cores

Figure 13



Reset Logic for Ferrite Cores

Figure 14

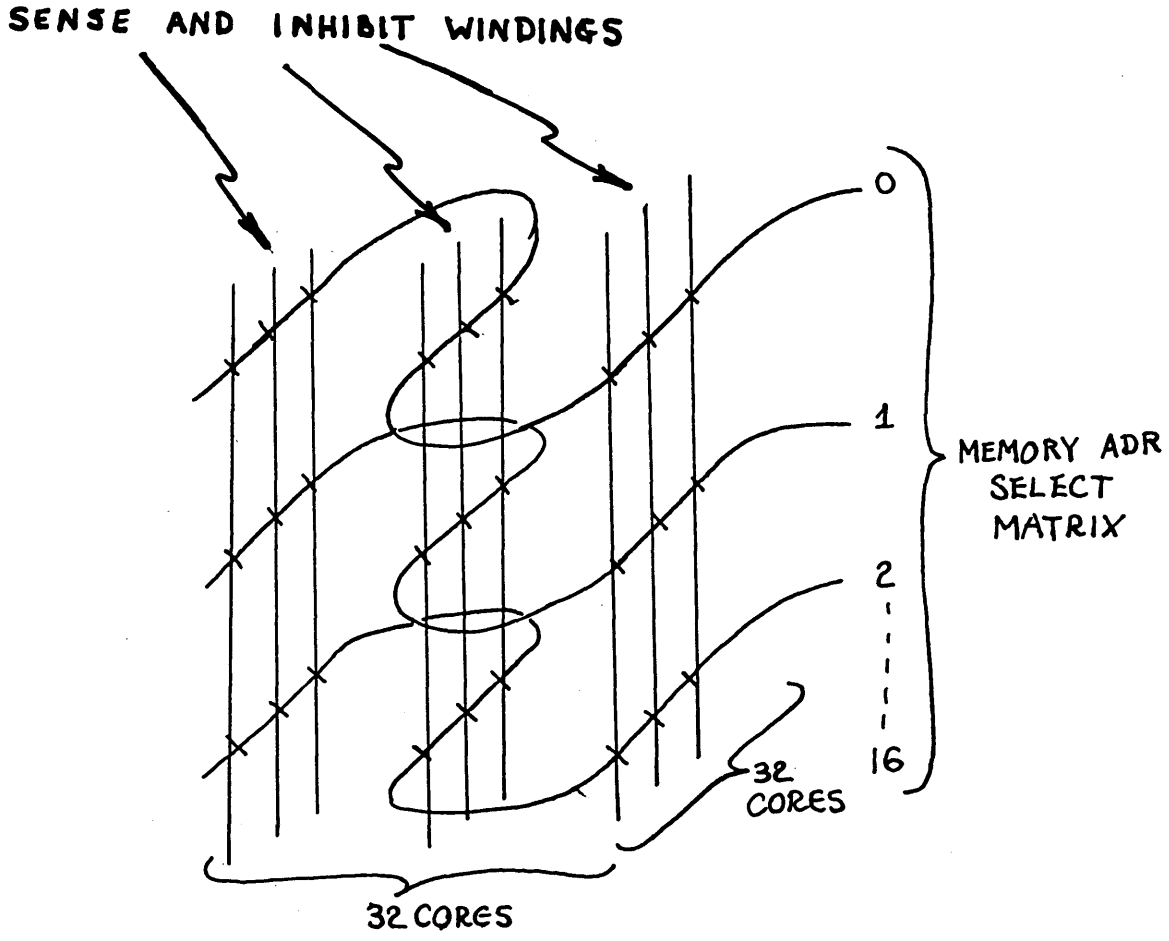
by a sense winding around the core, (see Fig. 13) and is sent to the Memory Buffer Register (abbreviated MBR). The MBR is a flip flop, initially set in the zero state, which will be set to one if there is a voltage pulse on the sense winding. As the MBR is the link between the memory and the rest of the computer, it is only by the value of the MBR that the computer knows what was stored in the magnetic core.

Notice that regardless of what was stored in the core originally, once it has been interrogated by I_{ro} the core is always in the zero state. If we are to preserve the information stored in memory we must reset the core to the one state if it contained a one and leave it in the zero state if it contained a zero. This is done through use of the MBR and the Inhibit winding. The Inhibit winding is a winding on the core whose flux opposes that of the read-in winding.

When the Inhibit winding is excited, I_{ri} is not sufficient to set the core to the one state. The logical diagram of this reset operation is shown in Fig. 14.

Memory For AP

The memory to be used in conjunction with the tunnel diode logic is a magnetic core memory, which will utilize the time pulses of the master control to interrogate the cores. The memory is arranged with a layer of cores for each address, with one core for each bit in every layer (see Fig. 15). We may interrogate and set the cores using one winding which excites every core in the plane. By



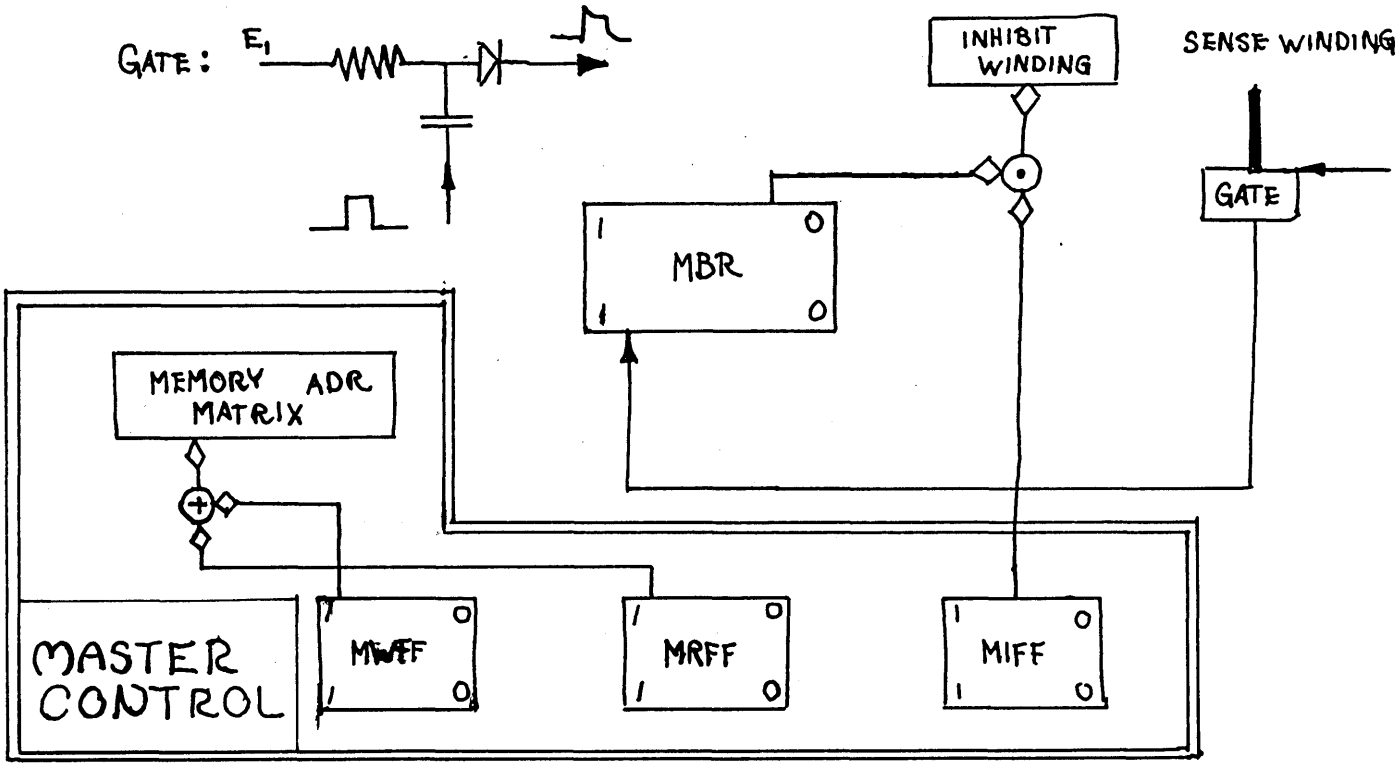
Core Array for Memory
Figure 15

passing the inhibit and sense windings vertically through one core in each plane and through to that module's MBR we may read out the information stored in each address into each module. Because only one address plane can be excited at a time, the pulse seen on the sense winding must be the contents of the particular address being excited. The logic for the memory input and output is shown in Fig. 16. The Memory Address Matrix, Memory Write Flip Flop, Memory Read Flip Flop, and Memory Inhibit Flip Flop are all contained in the master control.

Also contained in the master control are the pulse generator and timer which control the memory cycle in each module. The TX-0 may be considered as a typical computer which may be used as a master control. Its memory pulse chain is given below as an example of the type necessary to run the AP magnetic core memory. Memory cycle zero does not occur at all in the AP. During cycle zero the master control interrogates the program stored in its own memory to see what it should do to the information stored in the array. Memory cycle one is performed in the array in the following manner:

Time Pulse	All Commands Except STO	STO
1	1 → MRFF	1 → MRFF
2	0 → MBR	AC → MBR
3	CM → MBR	--
4	0 → MRFF	0 → MRFF

Memory Input and Output Logic



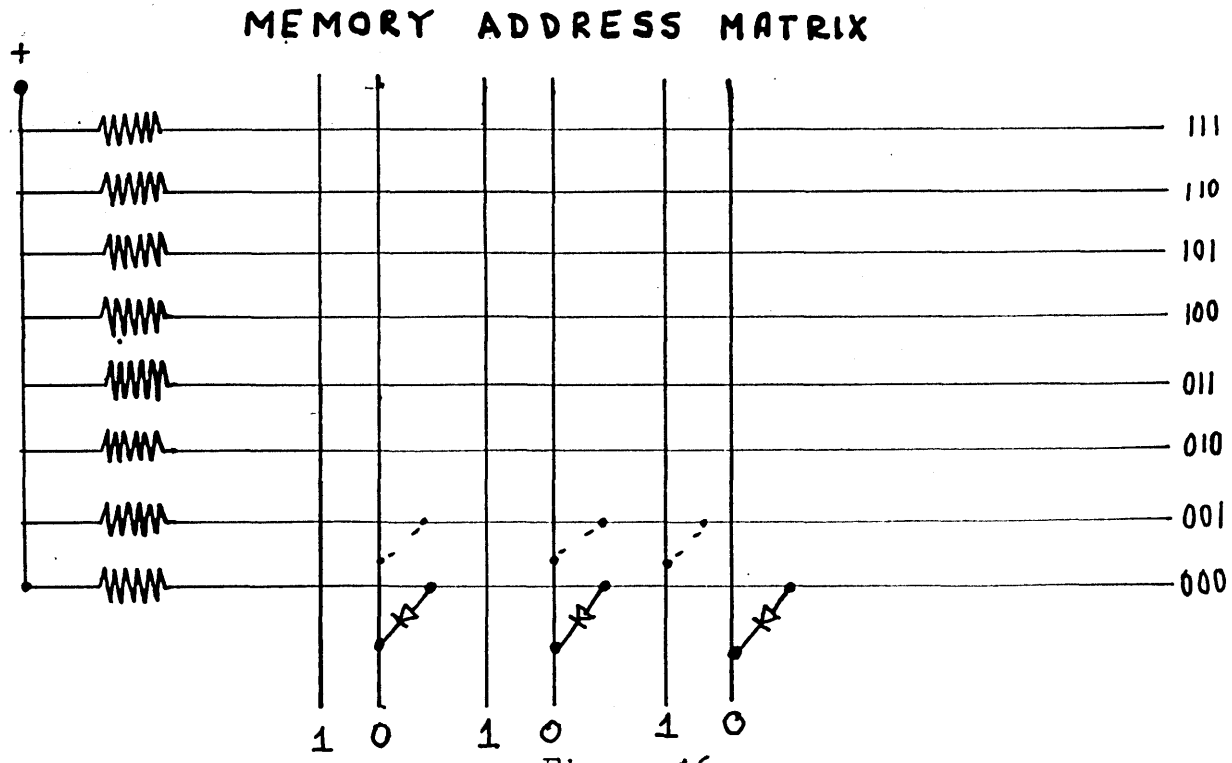


Figure 16

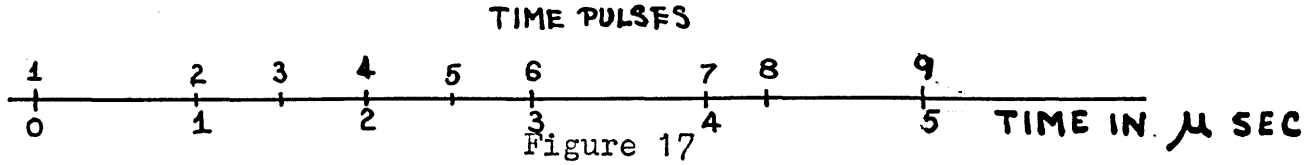


Figure 17

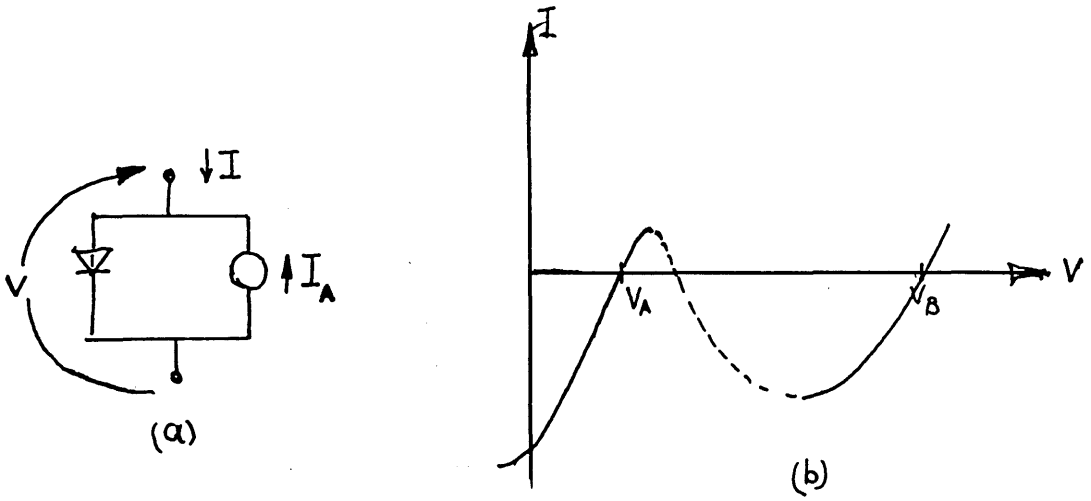
5	1→ M1FF	1→ M1FF
6	1→ MWFF	1→ MWFF
7	0→ M1FF	0→ M1FF
8	0→ MWFF	0→ MWFF
9	RESET LOGIC CIRCUITS	

The actual timing of the pulses is shown in Fig. 17.

While the output voltage of the magnetic core memory is compatible with the tunnel diode circuits, it takes considerably more current to set and read the cores than the diodes can handle. This current is supplied directly from the master control. However, there is still the problem of how the low level voltage output of the MBR will be able to gate the inhibit current. Even though the master control supplies the setting current we still have the power problem of supplying a source large enough to set a plane of 32 X 32 cores.

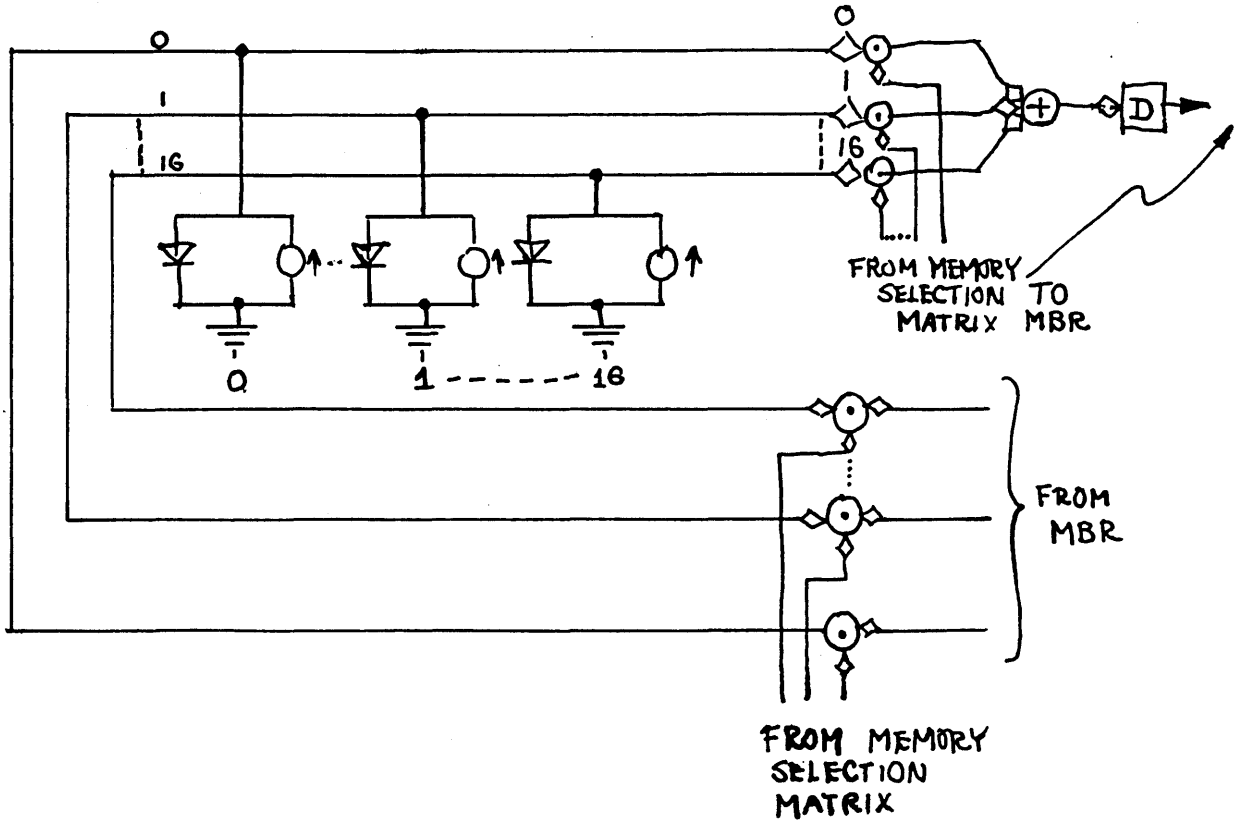
Tunnel Diode Memory

Because of these difficulties, an alternate design has been made using a tunnel diode memory. The basic storage element is shown in Fig. 18a. It is a voltage-controlled storage device with a v-i characteristic that is simply the tunnel diode characteristic (see Fig. 5) moved down by I_a. The new characteristic is shown in Fig. 18b. In actual practice the I_a source will be a voltage source in series with a resistance so that the I_a load line in Fig. 5 (which is coincident with the i=o line in Fig. 18b) will not be horizontal but will have a slope of E/R. However, the principles of operation



Tunnel Diode Storage Element

Figure 18



Tunnel Diode Memory Array

Figure 19

will be the same. We will consider V_a as the zero voltage level and V_b as the one level. Note that it is easy to set the device from the zero to one state, while it is hard to reset it to the zero state from the one state.

The tunnel diode memory array is shown in Fig. 19. The current sources shown are actually in the master control. All 32 X 32 memory elements with the same address are supplied by one voltage source in the control. The read-out is as follows: when one of the 16 bits is selected by the memory address matrix in the master control the output of that particular bit is fed to the MBR. When we wish to read the contents of the MBR into memory, the master control first resets every one of the selected bits to the zero state by a momentary interruption of I_a. If there is a one in the MBR the bit is then set to one. Notice that when the read-in "and" gates are not being selected, the low voltage at their output will not be able to reset a memory bit from one to zero.

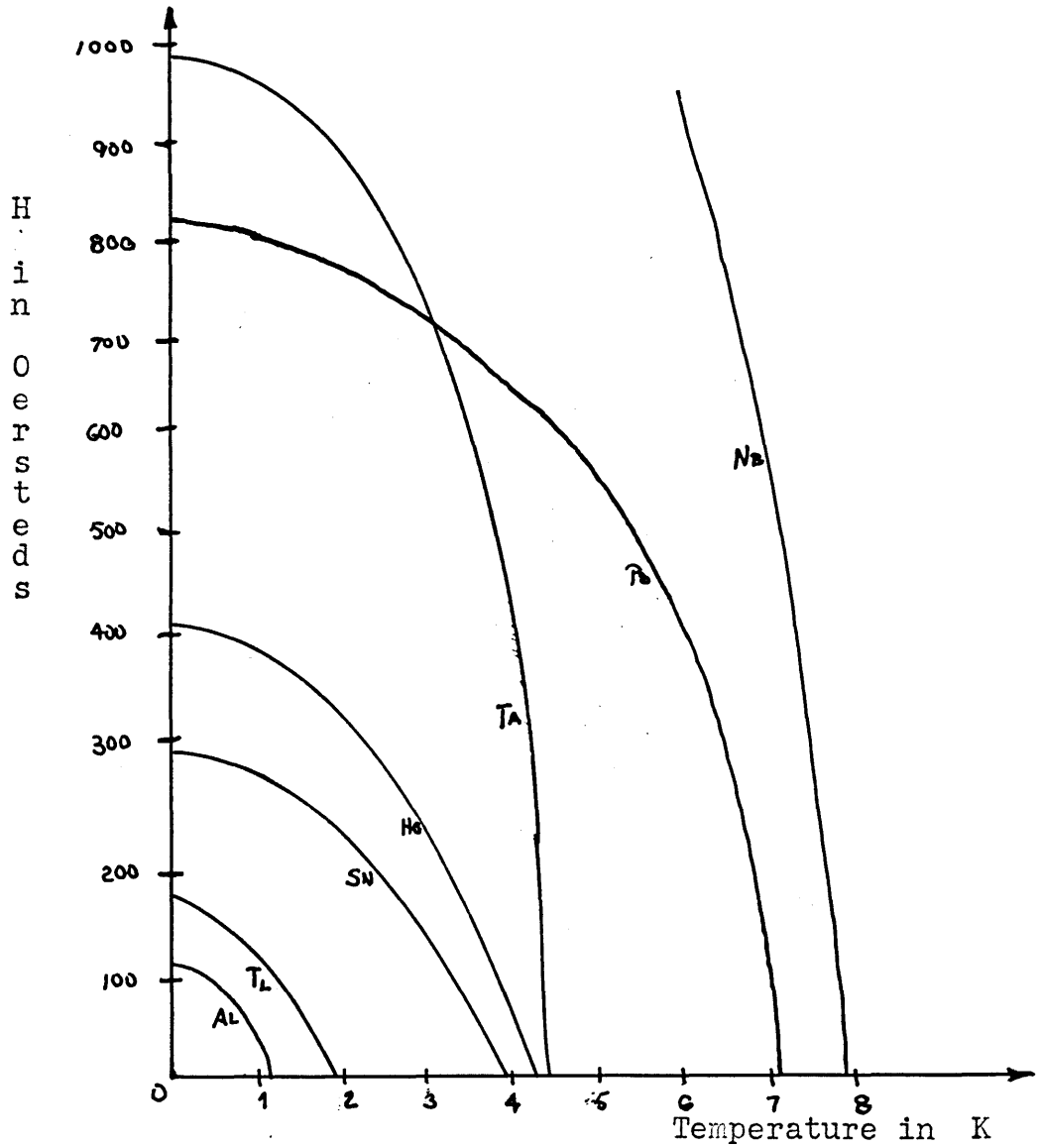
Unlike the magnetic core memory the read-out from the tunnel diodes is not destructive. In our magnetic core memory the function of the Memory Buffer Register was to allow us to read back into memory what we had just read out, it serves no useful purpose here, and for simplicity's sake may be eliminated. If we simply connect the output of the memory to "and" gate A in Fig. 10 and connect the input to B, the output of the accumulator, we may eliminate the MBR entirely.

A time pulse chain similar in nature to that used in the magnetic core memory is needed for operation of the tunnel diode memory.

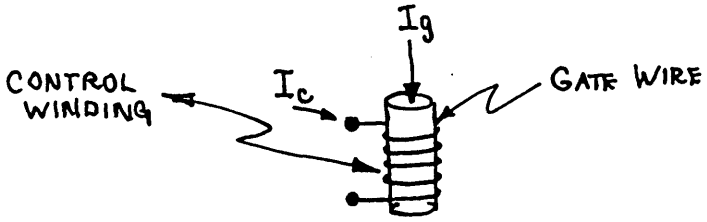
Principles of Operation of the Cryotron

Another bistable device which can be used to construct flip-flops and logic gates is the cryotron.[5] The basic phenomena underlying its operation is superconductivity. This is the property which some materials have of exhibiting zero resistance when cooled below some transition temperature. This transition temperature is below 8°K and its exact value varies from material to material. If a magnetic field is applied to the material, the onset of superconductivity occurs at a lower temperature. A plot of transition temperature as a function of the applied magnetic field is shown in Fig. 20. If the temperature is held below the transition temperature for the material, its resistance is zero. The resistance will remain zero as a magnetic field is applied until that magnetic field reaches a critical value. Above this value the normal resistance returns. Raising and lowering the magnetic field thus controls the resistance to the material by causing it to shift from its superconducting state to its normal state (quenching) and back again without changing the temperature. If we operate at a temperature about .2°K below the zero field transition temperature we can see that a field of only 50 or 100 oersteds will be needed to do this switching.

Early cryotrons were simply short straight pieces of



Threshold Magnetic Field vs. Temperature[5]
for Several Common Superconductors
Figure 20



Wire Wound Cryotron
Figure 21

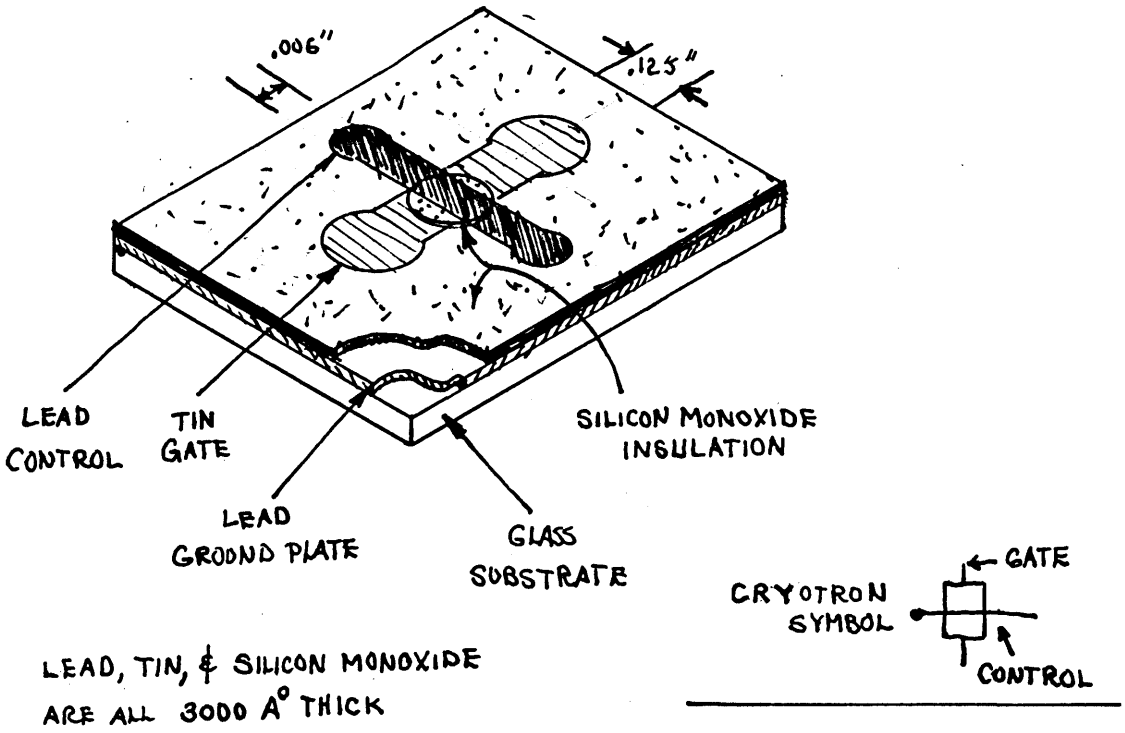
wire with a single layer winding around them (see Fig. 21). The resistance being controlled was the central (or gate) wire, and the magnetic field was generated by the control winding. Tantalum was chosen for the gate wire since liquid helium at normal pressure(4.2°K) would hold the wire at about .2°K below its zero field transition temperature. Niobium was used in the control winding because it had a very high transition temperature and would therefore be superconducting no matter in which state the central wire was.

Recently cryotrons utilizing thin superconducting films have been developed[6] (see Fig. 22). These thin-film cryotrons are easier to fabricate and are 1000 times faster than their wire wound predecessors.

Cryotrons are connected in circuits in a manner very similar to relays, and it is not necessary to use any component other than the cryotron to design a circuit. The low resistance characteristics of the cryotron necessitates the use of a current source and this current flows in series through the gates and controls of the circuits. The current gain of a cryotron is defined as "the maximum current the gate can carry without quenching, divided by the minimum current in the control necessary to quench the gate."[6]

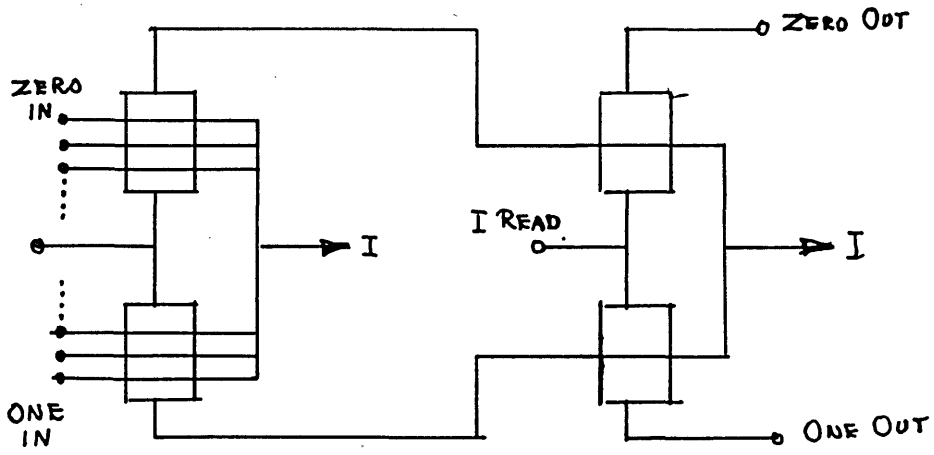
$$G = \frac{\text{Critical gate current}}{\text{Critical controlling current}}$$

Since the same current is to flow in both the gate and control, the current gain must be at least one and should be two or three to provide insurance against a variation



Thin-Film Cryotron

Figure 22



Flip Flop
Using Thin-Film Cryotrons

Figure 23

in cryotrons.

Cryotron Flip Flop and Logic Circuits

A flip flop using thin-film cryotrons is shown in Fig. 23 [6]. Initially the current is divided equally between the two superconducting legs of the device. When there is either a zero or one input the control gate of one of the cryotrons is excited. This increases the resistance of that leg causing all the current to flow through the other, superconducting, leg. The increase of current in the superconducting leg causes the cryotron in that side of the read-out network to become resistive, forcing the read-out current through the read-out leg associated with the side which has just been set. Once the flip flop has been set the setting current may be removed, since inductive lag will keep the circuit in the set position until reset. Notice that by using parallel inputs we have "and" gates in the input circuits. "And" and "or" gates which are set and read-out in the identical manner as the flip flop are shown in Fig. 24.

The module and link logic for the cryotron AP is shown in figures 25 and 26. It is important to note that each variable and its complement are available at all times and both must be used, since an alternate superconductive path for the source current must always be furnished. If we do not offer the current an alternate path, and force it instead to flow through a resistive path, we introduced Joule heating which will raise the surrounding temperature

Logic Gates
Using Thin-Film Cryotrons

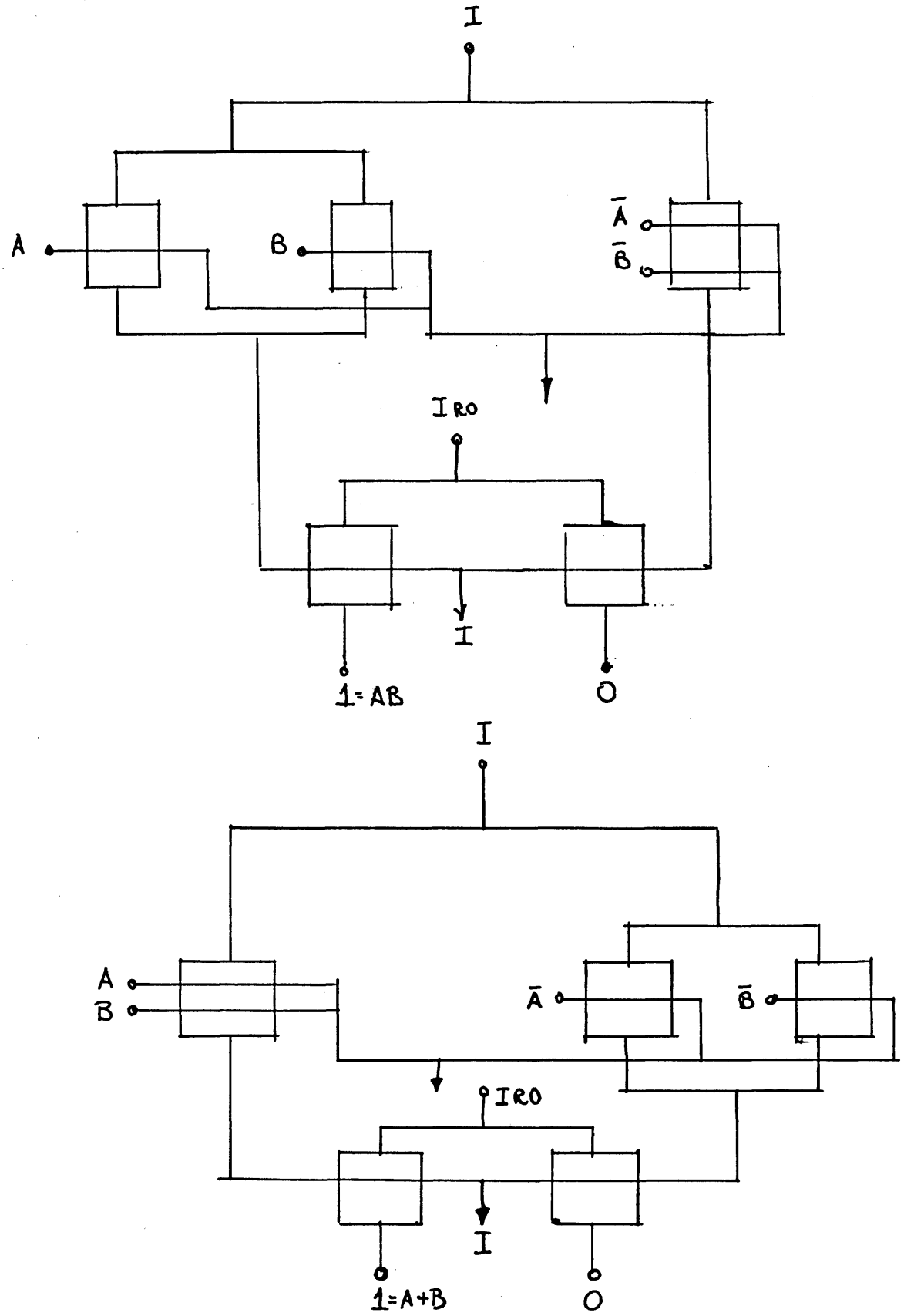


Figure 24

Module Logic Using Thin-Film Cryotrons

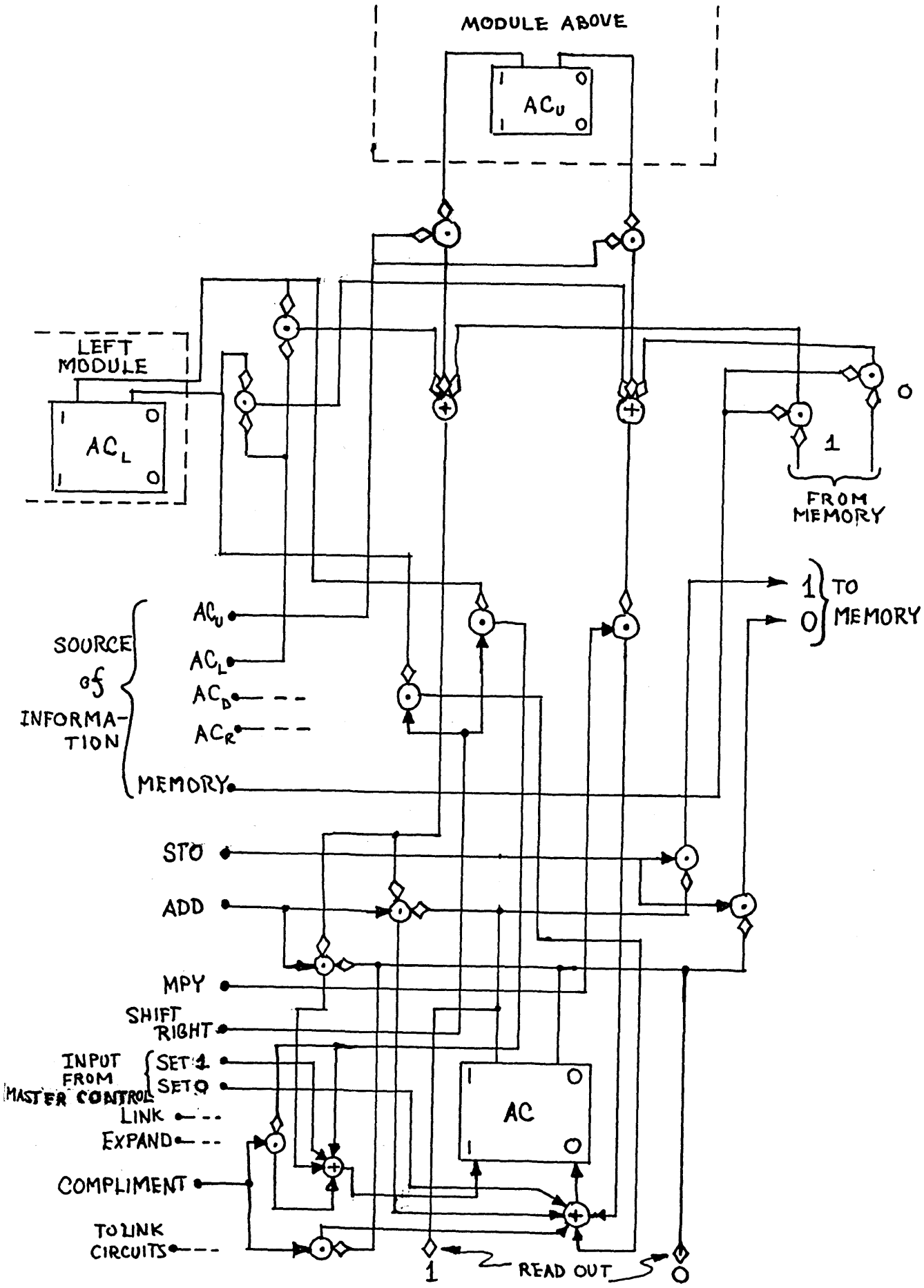


Figure 25

Link Circuit Logic Using Thin-Film Cryotrons

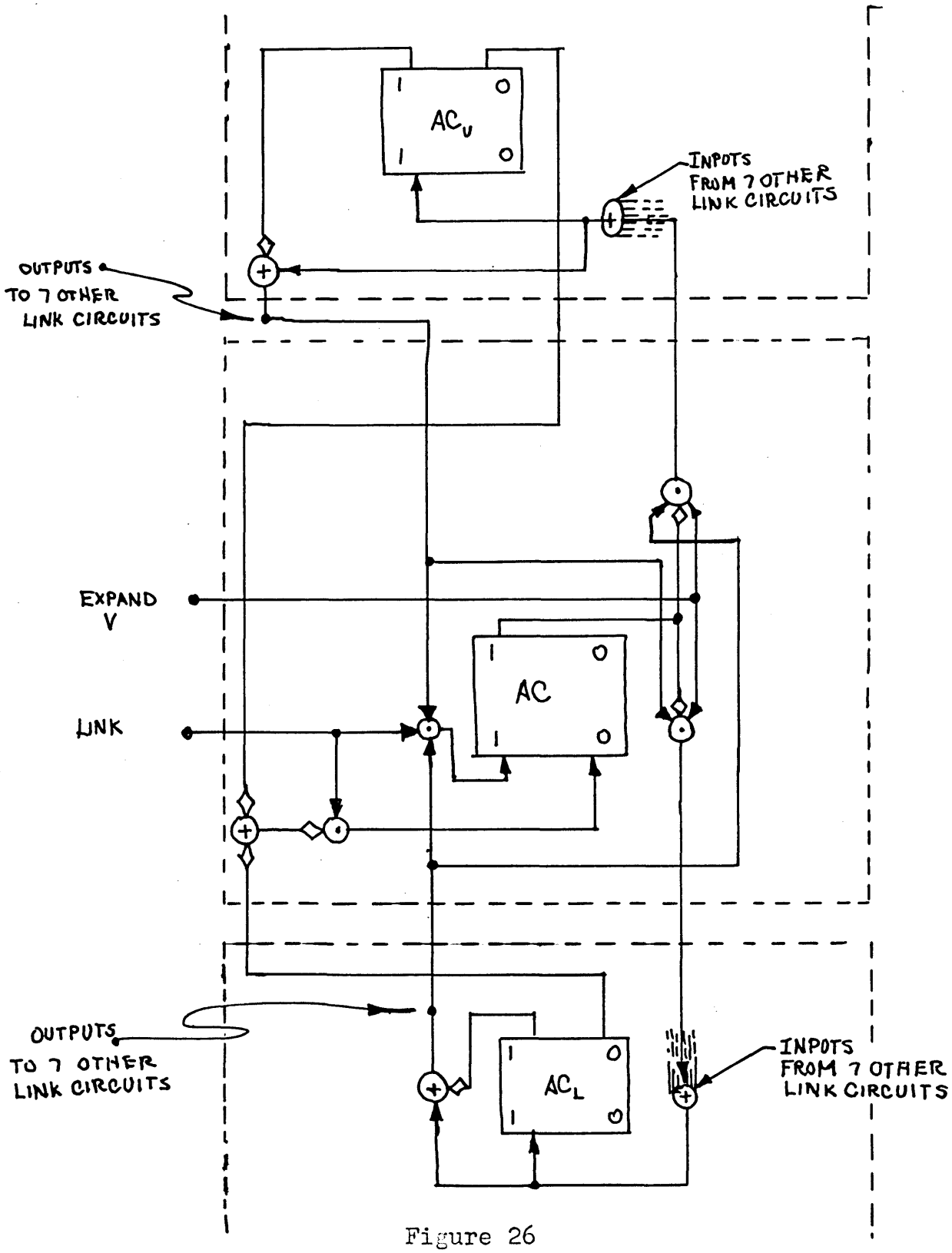


Figure 26

above the transition temperature. Figure 27 shows some of the actual circuitry required to perform the add operation.

Cryotron Memory

The circuit diagram for a memory using thin-film cryotron flip flops as storage elements is shown in Fig. 28, as with the tunnel diode memory there is no MBR. The I_{ri} input to the read-in matrix and the I_{ro} input to the memory bit are selected by the memory address matrix shown in Fig. 29. The passing of the control wire under the gate is used to show that the control cannot quench that particular gate. For any input address there will be only one super conducting gate and the selection current will flow through that gate.

The memory address matrix and the read-in matrix are both part of the master control while each module has its own sixteen-bit memory. The sixteen bits of memory are connected in series, and a current is induced in the circuit. Due to the super conductivity of the circuit, this current will flow indefinitely without the need for a source to be connected in the circuit.

This completes the construction of the AP using cryotrons.

Example of Actual Cryotron Circuitry

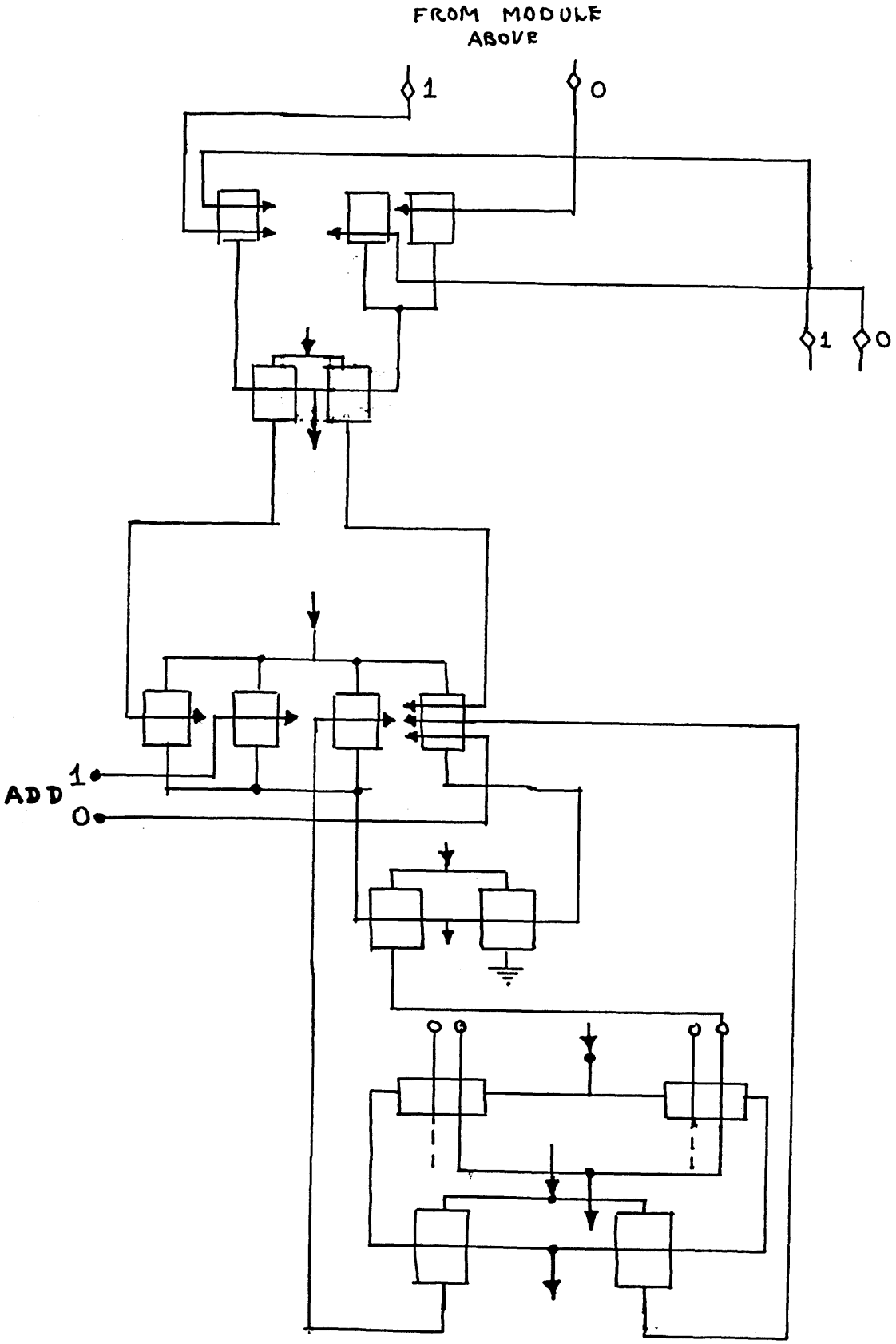
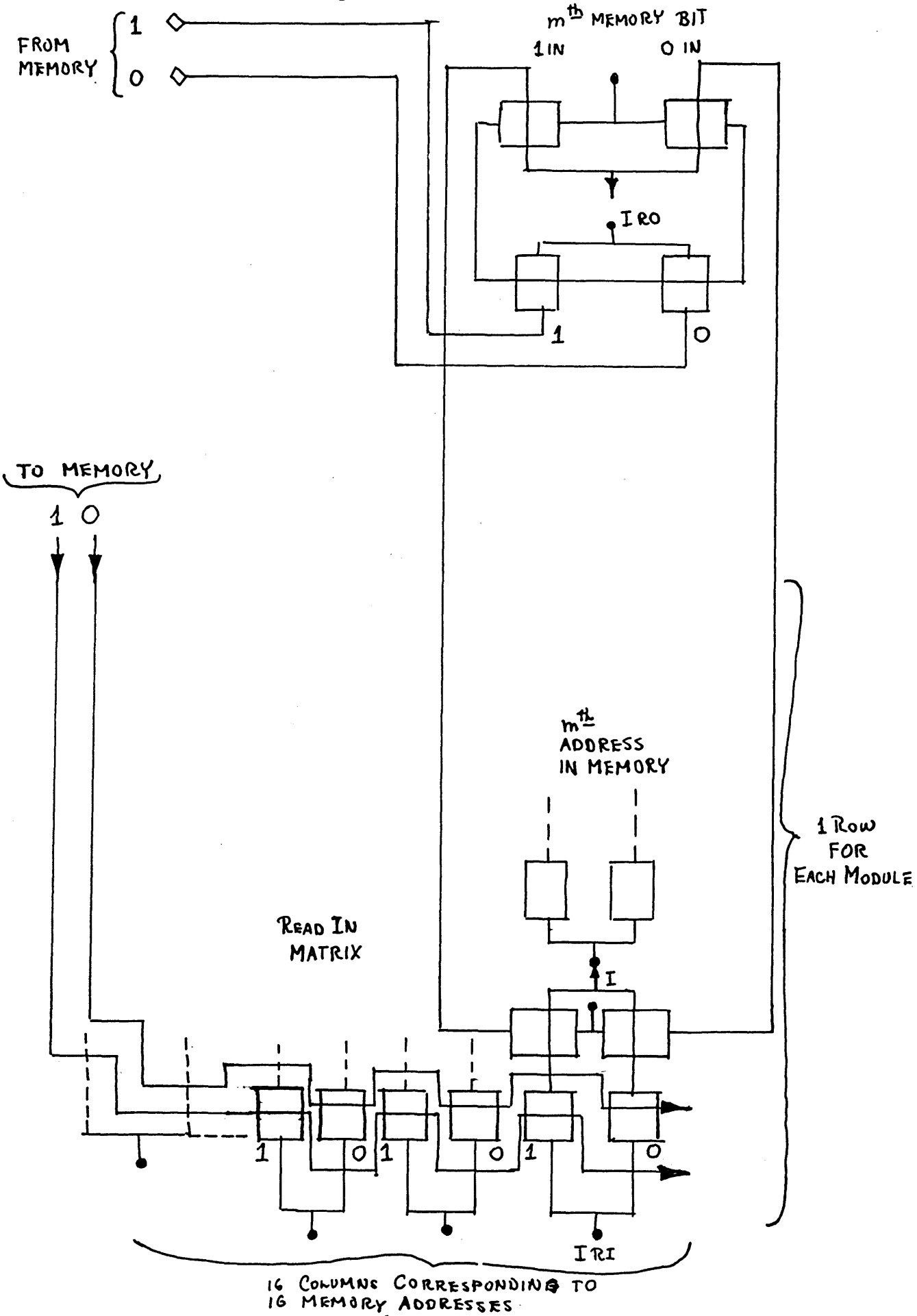
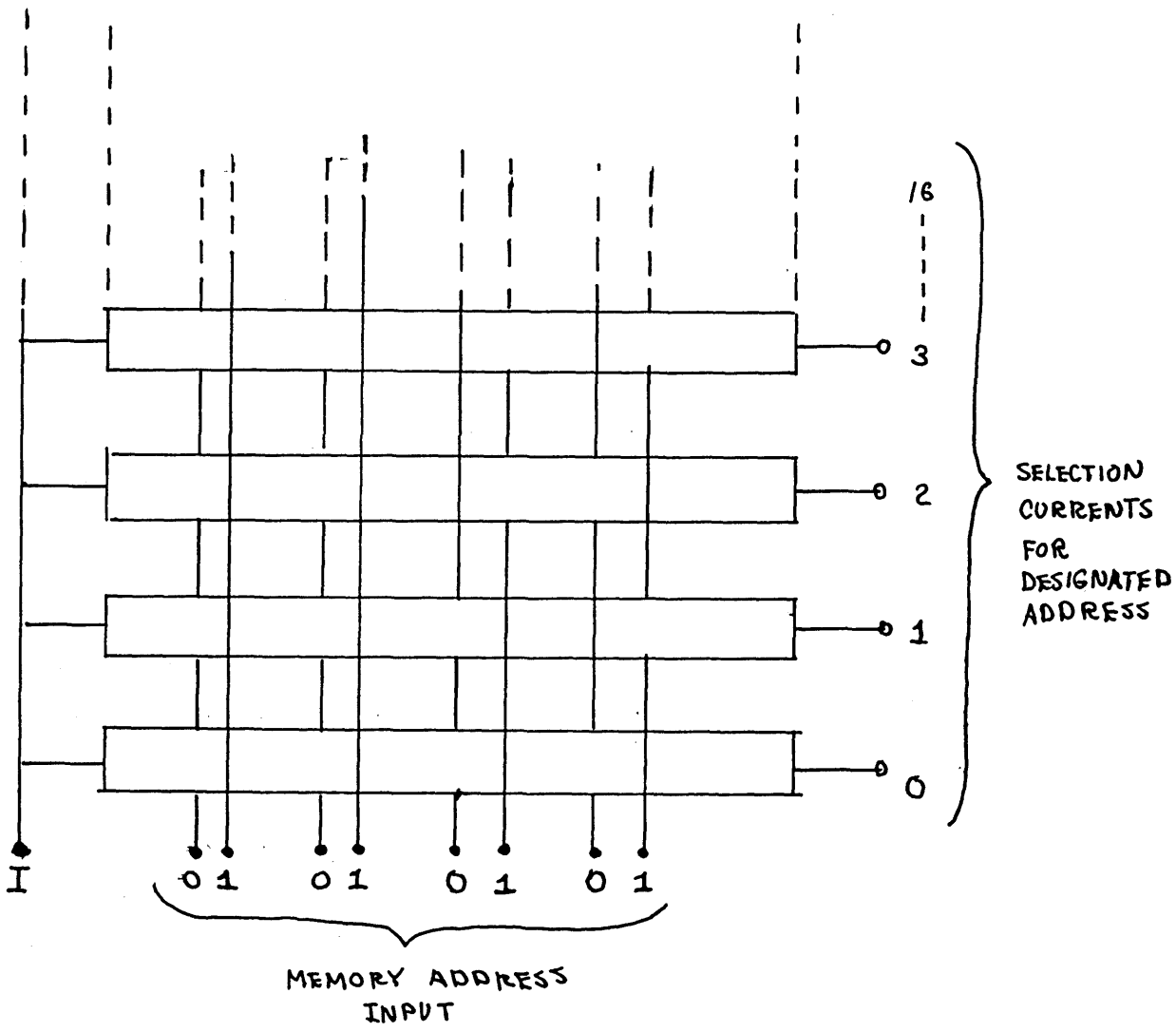


Figure 27

Memory Using Thin-Film Cryotrons
Figure 28





Memory Selection Matrix

Figure 29

Optimum Characteristics

In building an AP there are two primary considerations. The large number of modules (a minimum of 32 x 32) presents both a size and power problem. The AP must be miniaturized to the point where it is possible to house and cool the components without huge expense. The speed of the AP must be great enough so that the array will be compatable with the solid state computer which is used as the master control.

In addition to these considerations there is the problem of cost and uniformity of components. Both the tunnel diode and thin-film cryotron are now in the primitive first stages of development. However, for the purposes of this study I will assume that modern technology will make these components available at low cost, with uniform characteristics.

Tunnel Diode Array

The tunnel diode is a solid state device and is capable of extremely fast operation, "units with time constants of fractions of a millimicrosecond have been fabricated"[4]. There is no problem in speed of operation. The circuits are reliable with respect to variation in parameters, the "and" and "or" gates will operate with a 5% shift in source current. The flip flop was designed to operate with "a tunnel-diode peak current of ± 5%, a resistor tolerance of ± 5%, a DC-supply variation of ± 12%, and a variation of input-pulse amplitutde from -20% to plus several hundred percent"[3].

Because the tunnel diode is such a low impedance element it is not practical to assume a constant voltage source is available to supply power. Thus a current source is required which must generate enough power to supply all the diodes. At the present time this is quite a large problem. Experiments are being made which should lead to diodes which will draw only one milliamp of current and still switch at the same speed. This will reduce the power problem but not eliminate it.

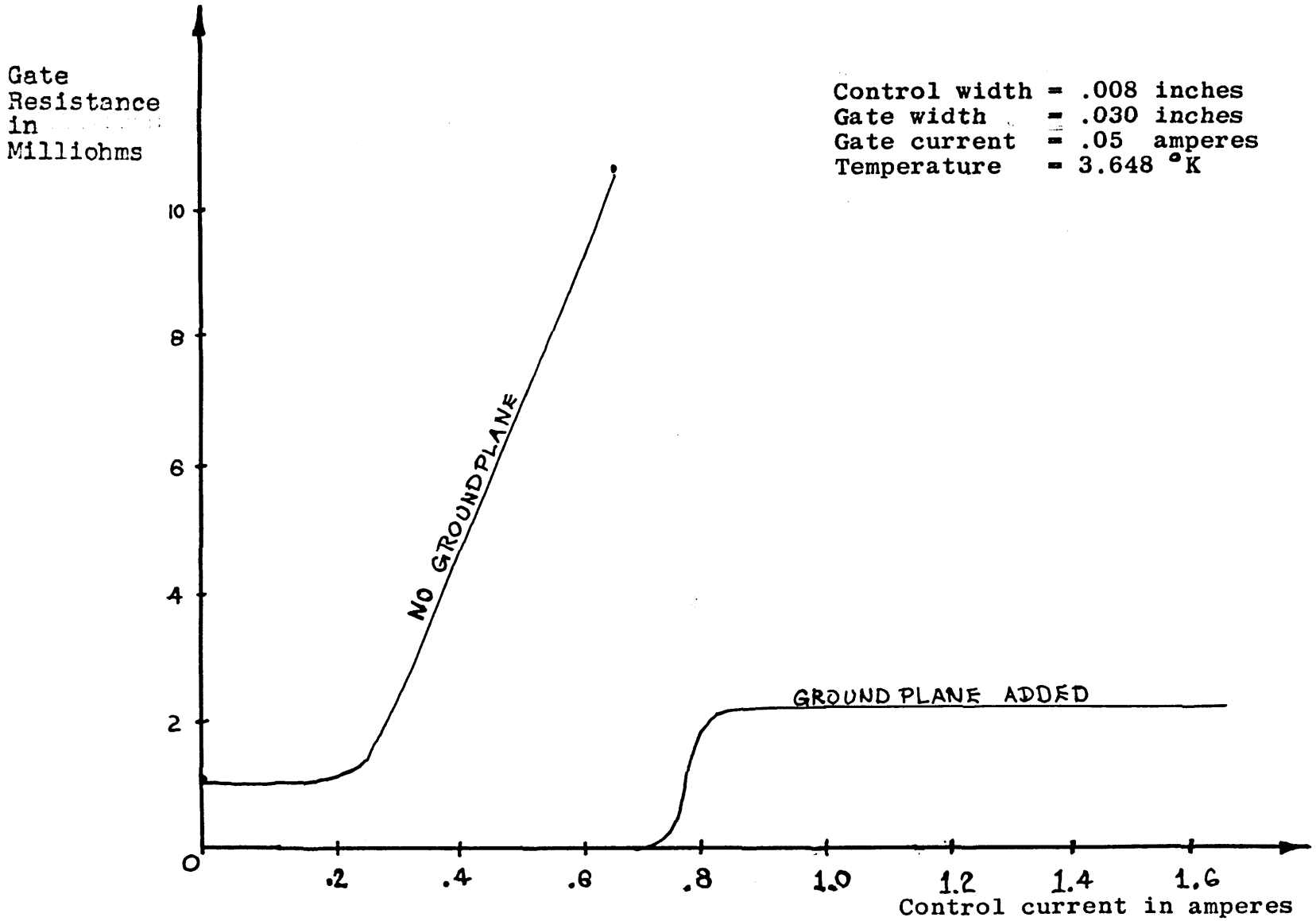
Another objection to the tunnel-diode configuration is its size. The tunneling region of the tunnel-diode characteristic is essentially temperature independent, so that the threshold current for the "and" and "or" gates will not change with temperature. This makes our miniaturization problem somewhat simpler since we do not have to make elaborate allowances for cooling, but we are still faced with the fundamental limitation of the size of the component. It is not possible to miniaturize the the tunnel-diode AP beyond the present size of conventional solid state computers.

Cryotron Array

The extremely small size of the thin-film cryotron lends this component to use in "microminiaturized" circuits. "A computer or memory containing one million elements can be accomodated in a one-cubic-foot liquid helium container using presently available refrigeration methods."[8] The primary drawback to use of the cryotron lies in its relatively slow operation.

In cryotron circuits, the impedance levels are so low that capacitance may be ignored. The switching speed of the circuit is dependent upon its L/R time constant. The ground plane (see Fig. 22) is important because it reduces the inductance of the cryotron and its interconnecting leads. It does this in the following manner: Since the ground plane is lead, because of its high transition temperature, it is always superconducting during the operation of the circuit.. Because flux can not penetrate a super conducting metal, the normal components of magnetic field at the surface of the plane must be zero.[7] The plane accomplishes this by generating eddy currents which produce a field that exactly opposes the applied field. Since the plane is a super conductor these currents do not decay with time. "Typical values of inductance for conductors .02cm wide with and without a superconductive ground plane are 10^{-11} henrys/cm and 10^{-8} henrys/cm, respectively."[6] The resistance restored in a gate as a function of control current is plotted in Fig. 30.

The time constant of a single cryotron is defined as the inductance of the control divided by the gate resistance. This time constant for the cryotron shown in Fig. 22 is in the order of 6×10^{-8} seconds. The time constant for the redistribution of current from the zero path to the one path of the flip flop in Fig. 23 is 2.4×10^{-7} seconds. This time is considerably longer because of the inductance of the interconnecting leads which is about



Restoration of Gate Resistance vs. Control Current for[6]
A Cryotron with and with a Ground Plane

Figure 30

twice the inductance of a single cryotron. The flip flop in Fig. 23 was designed to minimize this inductance. This time constant is a theoretical limit; in actual laboratory tests the complement time was about 2 microseconds. The time constant of the "and" and "or" gates is of the same order of magnitude. This means that one operation would take about 14 microseconds, a rather slow operation time compared with modern solid state machines.

However, the cryotron has many advantages. Because of the superconductive nature of the circuit, all currents can be hooked up in series, thus reducing source requirements. In the memory elements a current can be induced which will circulate for years without dacaying. The thin-film cryotrons are easier and cheaper to manufacture than tunnel diodes. The small size of the cryotron makes miniaturization extremely simple, and the AP would be much more compact than any built with solid state devices.

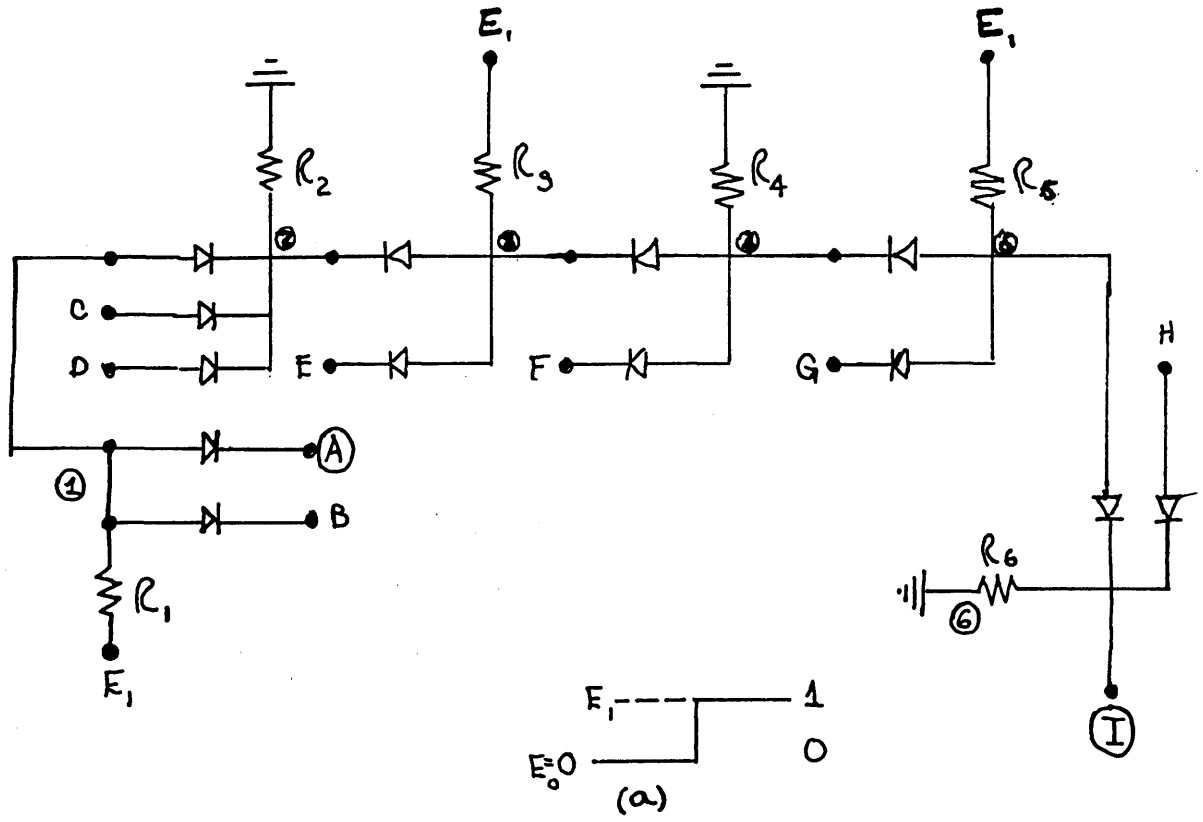
Conclusion

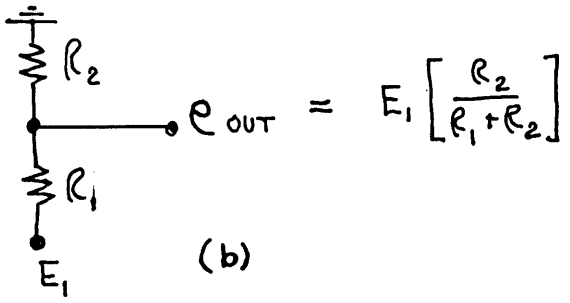
If speed of operation is not of prime importance, a compact, efficient, and inexpensive AP can be built using cryotrons which will be satisfactory in every respect. The AP using tunnel diodes is more difficult to realize because of size and power limitations. I feel the cryotron version has a much better future.

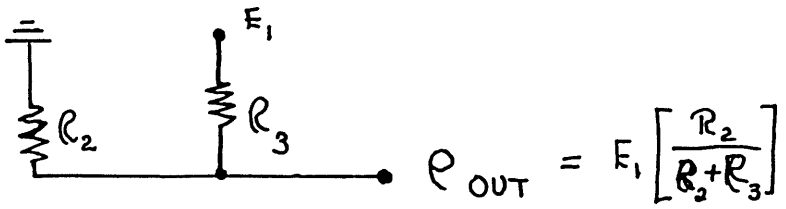
APPENDIX

Drawbacks of a Cascaded Diode Gate Circuit

The use of conventional diode "and" and "or" gates presents the problem of no "logical gain". In Fig. A we see the actual circuit for a typical path from the memory buffer register to the accumulator. Let us look at gates 1, 2 and 3 for a moment. We observe that gate 1 which multiplies A and B is supplied from E_1 and its output becomes one of the inputs of the "or" gate (gate 2). Resistance R_2 is connected to the zero level of voltage. Now, if A=B=1 we observe that R_1 and R_2 are in series between E_1 and E_0 (see Fig. Ab). If R_1 is some finite value, even though AB=1 and the output of gate 2 should be one, this output voltage can <u>never</u> quite reach E_1. Indeed in order to obtain reasonable definition between the one and zero states R_2 must be much larger than R_1. In the next stage of the circuit the output of gate 2 becomes one of the inputs to "and" gate 3. If all the inputs to gate 2 are low, then R_3 and R_2 are in series between E_1 and E_0 (see Fig. Ac). In this state if the output of gate 3 is to be nearly E_0 it is necessary that R_3 be much greater than R_2. Thus we have a two-fold problem. For every stage added, we must increase the size of the gate resistor by a large factor and our output voltage becomes more poorly defined. Diode gates are incapable of driving other diode gates in cascade without a loss of signal definition, this is referred to as a lack of "logical gain".







(C)

Cascaded Diode Gates

Figure A

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