Electronic Properties of Gallium Nitride Nanowires

by

Joonah Yoon

B.A., University of California at Berkeley (1995)

Submitted to the Department of Physics
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 2008

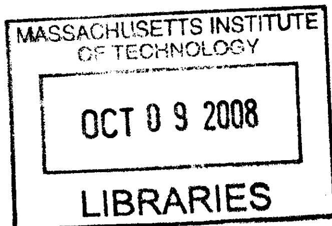
© Massachusetts Institute of Technology 2008. All rights reserved.

Author ....
Department of Physics
December 20, 2007

Certified by..
Venkatesh Narayanamurti
John A. and Elizabeth S. Armstrong Professor and Dean of the
School of Engineering and Applied Sciences, and Professor of Physics
Harvard University
Thesis Supervisor

Certified by..
Mildred S. Dresselhaus
Institute Professor of Electrical Engineering and Physics
Massachusetts Institute of Technology
Thesis Supervisor

Accepted by..
Prof. Thomas Greytak
Associate Department Head for Education



ARCHIVES

Electronic Properties of Gallium Nitride Nanowires

by

Joonah Yoon

Submitted to the Department of Physics
on December 20, 2007, in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

Abstract

This thesis presents a systematic study of the electrical transport in GaN nanowires. Particularly, the effect of the surrounding dielectric on the conductivity of GaN nanowires is experimentally shown for the first time. Our GaN nanowires are grown by catalytic vapor growth methods, specifically hydride vapor phase epitaxy (HVPE) and chemical vapor deposition (CVD). TEM and XRD studies indicate that both of our HVPE and CVD grown GaN nanowires have the wurtzite single crystal structure. The crystal orientations along the wire axis are (1000) and $(10\bar{1}0)$ for our HVPE and CVD grown nanowires, respectively. The mean diameters are 200 nm and 46 nm for the HVPE and the CVD grown nanowires, respectively. CVD GaN nanowires with three different surrounding configurations are prepared to study the effect of the surrounding dielectric. The GaN nanowires are either laid directly on a SiO_2/Si substrate, or freely suspended between metal contacts, or embedded in SiO_2. The conductivity is measured as a function of temperature, nanowire diameter, and the surrounding dielectric. The donor ionization energies are extracted from the temperature dependence of the conductivity. In all cases, two sets of the activation energies are obtained. One set of these activation energies shows an inverse dependence on nanowire radius and the other set is found to be independent of the radius. The inverse radius dependence of the activation energy is explained by the polarization charges, which are induced by the donor ions, at the interface between the nanowires and their surroundings. This so-called dielectric confinement is found to have a substantial effect, more than the quantum confinement effect, for GaN nanowires with diameter larger than 10 nm or so. The radius-independent activation energy is found to be due to the impurity band conduction near the surface.

We also successfully fabricated nanowire field-effect transistors (FETs) using both HVPE and CVD grown GaN nanowires. For the thinnest CVD grown nanowires, complete control of the carrier density was achieved. The field-effect mobility of the CVD grown GaN nanowires is estimated to be $\sim 18\ cm^2/V{\cdot}s$, which is more than an order of magnitude smaller than that of the bulk GaN. A redshift of the near-band-edge emission in the room-temperature photoluminescence measurements of the CVD grown GaN indicates a high impurity concentration. The metallic approximation

using a capacitor model shows the carrier density to be $\sim 4 \times 10^{19}\text{cm}^{-3}$. Reduction of the background impurities is expected to decrease the scattering from the ionized impurities and to improve the carrier mobility and switching behavior of the nanowire FETs.

Thesis Supervisor: Venkatesh Narayanamurti
Title: John A. and Elizabeth S. Armstrong Professor and Dean of the School of Engineering and Applied Sciences, and Professor of Physics
Harvard University

Thesis Supervisor: Mildred S. Dresselhaus
Title: Institute Professor of Electrical Engineering and Physics
Massachusetts Institute of Technology

Acknowledgments

First of all, I would like to thank my parents Young Yoon and Jimmy Yoon, and my brother Keunah Yoon for providing a strong foundation of love and support for me during the toughest time throughout my graduate studies. To my family I was always able to turn for an advice whatever was bothering me at that time. I would also like to thank my soon-to-be wife, Hyunsook Kim, who is presently busy preparing for our wedding in Korea by herself so that I can focus on finishing up the thesis at MIT. I am very fortunate to have met her during my last year in graduate school. She gave me extra strength and incentive for me to wrap up my study as soon as possible. I am very much grateful for her love and support.

I went through various different projects including high T_c superconductor, semiconductor laser, memory devices, ballistic electron emission microscopy, carbon nanotube spin transport, and semiconducting nanowires across two greatest institutes MIT and Harvard. I am very much thankful for opportunities given to me in these various projects. I would like to thank Prof. Mildred Dresselhaus, Prof. Rajeev Ram, Dr. Jagadeesh Moodera, and Prof. Venkatesh Narayanamurti. I have learned one valuable lesson from these experiences, that is to invest my time and energy wisely because they are limited resources.

I would like to thank my Harvard advisor, Prof. Venkatesh Narayanamurti, for his patience and continued financial support throughout my entire stay in his research group. Without his support, my thesis would not have been finished.

I am also indebted to Prof. Mildred Dresselhaus for agreeing to serve as my MIT advisor. Through interaction with her, I saw a person who is not only achieved in science but also humble and kind, which are vary rare qualities. She set a great example for me and all other aspiring young students around her.

I also wish to thank the rest of my thesis committee members, Prof. John Joannopoulos, and Prof. Ray Ashoori, for their precious time and numerous scientific advices. Several thesis committee meetings with them led to many new ideas and clearer direction for my thesis research. I am very much grateful for their guid-

ance.

I would also like to mention members in my group who were involved in the semiconducting nanowire project. HVPE (hydride vapor phase epitaxy) GaN and InN nanowires were grown by Dr. George Seryogin. George was always willing to share his knowledge on the crystal growth. George was the person who kept most of our lab spaces tidy and neat. He would, for example, order a tank of liquid nitrogen when it runs low and make numerous phone calls to have building maintenance facility to repair the broken stuff in the lab, ranging from water leaks in the ceiling to problems with the fume hood. CVD GaN nanowires were grown by Dr. Ilan Shalish.

I would like to thank fellow graduate students Kasey Russell and Ed Likovich, who took over a lot of tasks which George used to take care of, after he left the group to start his industry job. Kasey and Ed also provided energy into the Narayanamurti group.

There are many former members of the Narayanamurti group who helped me in numerous ways. Dr. Chavva Reddy was one of the initial group members. I could always count on having joyful conversation with Reddy. He was a very witty and cheerful fellow. Dr. Ramesh Mani was also one of the starting members of the group. He possessed a solid understanding of solid state physics, and we were able to turn to him for an engaging discussion of physics. Dr. Igor Altfeder was a pragmatic experimentalist who was often found smoking outside McKay building. Igor could work through the toughest experiments. I received many experimental advices from Igor especially while I was working on the cryogenic ballistic electron emission microscopy project.

My search for the wisdom of science went well beyond my own research group. Outside my group, I have many people to thank, especially members from the Tinkham group, the Westervelt group, the Marcus group, the Hongkun Park group, the Capasso group, and the Lieber group. There were many intelligent and kind people who were willing to help you if you just asked them. Dr. Steve Cronin, whom I knew previously from the Dresselhaus group at MIT, came to Harvard as a postdoctoral fellow in the Tinkham group. He renewed my interest in carbon nanotube, and a set

of basic experimental skills I learned from him later became the valuable tools for the current thesis project. Steve has an easygoing and pleasant personality which, I think, he acquired through playing guitar in a rock band for many years. The Tinkham group had another nice fellow, Dr. Sergio Valenzuela. He was a talented experimentalist from whom I often seeked advices on fabrication techniques. I also met many talented minds from the Westervelt group on the second floor of McKay laboratory. Dr. Ian Chan introduced me to a dilution refrigerator for the first time. Dr. Andy Vidan was kind enough to lend me his hands and his equipments when I needed them. Dr. Hakho Lee whom I first met in the Narayanamurti group and later in the Westervelt group continued to keep in touch with me for many years. Hakho's down-to-earth personality always kept my own feet on the ground when I was losing focus from my research project. I remember having many lunches with him at the local fast-food place "Three Aces" and miss having interesting discussions over a wide range of topics ranging from Korean politics to the world economy.

I would also like to express my gratitude to all technical staffs at McKay laboratory. They did more than just maintaining equipments. Their care and interest for each student's project really made a difference. The current and past technical staff members include Mr. Steve Shepard, Dr. Jiandong Deng (JD), Mr. John Tsakirgis, Dr. Ling Xie, Mr. Ed Macomber, Dr. David Bell, Mr. Yuan Lu, Dr. Richard Schalek, Mr. Noah Clay, and Dr. Jim MacArthur. Particularly, Dr. David Bell spent a lot of his time helping me image the GaN nanowire disks which were microtomed by Dr. Richard Schalek.

There were also non-technical staff members who helped me to stay focus on my work. I want to thank Ms. Martha Mooney for taking care of my Harvard ID card. Ms. Moriah Freeman provided me with professional administrative support, ranging from printing out a long thesis draft to making appointments with Venky. I would also like to thank Ms. Laura Doughty for cheerful small talks we had while I was visiting Prof. Mildred Dresselhaus and many more administrative support she willingly provided. Dr. Gene Dresselhaus also helped out by sending me the PDF files containing Prof. Mildred Dresselhaus' comments on my thesis draft.

The Narayanamurti group has drawn many visiting professors over the years I stayed in the group. These visiting professors oftentimes brought new ideas and energy into our group, and I would like to thank them for enriching my research experience in the Narayanamurti group. They are Prof. Clive H. Perry, Prof. Henryk Temkin, Prof. Sandip Tiwari, and Prof. L. Ramdas Ram-Mohan. Prof. Henryk Temkin suggested a Hall effect measurement on semiconducting nanowires to me. This idea isn't feasible at present time but still is an interesting idea. Prof. Sandip Tiwari also showed a very strong interest in the semiconducting nanowire project and he came up with some novel way to make efficient p/n junction LEDs out of semiconducting nanowires. His energy and intuition for science impressed me. I had closest interaction with Prof. Ram-Mohan and his student Alexi Girgis out of all the visiting scientists. I remember explaining to Prof. Ram-Mohan my experimental result which showed the dielectric confinement effect on GaN nanowires, and he was so excited about the result that by the next day he already had several of his students at WPI working on the project applying his expertise in the finite element method.

Graduate school can be an emotionally very tough place to survive. I used many extracurricular activities and friends I met from those activities as the means to keep my sanity intact. I was an active member of several MIT sports clubs and I thank them for great workouts and letting me relieve stresses from my research group. I participated in MIT sports Taekwondo club, MIT Kendo club, HoHo's kickboxing class, and MIT KGSA (Korean Graduate Student Association) Soccer team over many years of my graduate school training.

I would also like to thank Ashdown House community at MIT. Ashdown House became my home and I met many good friends from this oldest graduate dormitory at MIT. I met Dr. Tony Eng, Dr. Chris Fang-Yen, Dr. Wonshik Choi, and Prof. Terry Orlando and his wife Dr. Ann Orlando. Prof. Terry Orlando lent me his ears when I went through frustrating experiences and gave me many sound and practical advices on academic and research issues. I will always remember and miss spending Thursday evenings with other fellow graduate students during Ashdown House coffee hours filled with assorted sweets and snacks. Also Sunday brunches and frequent outings

to local restaurants were few of many social activities Ashdown House provided to many graduate students like myself over numerous years. I just hope that this great tradition and culture of Ashdown House last for many more years to come. I would also like to commemorate a friend from Ashdown House, Mr. Bhuwan Singh, who died on May 7, 2004. I would like to thank him for being a caring friend and pray for his soul.

My stay at Harvard would have been much less enjoyable without a group of Korean friends whom I have known. They provided me with a strong sense of identity and security. They are Dr. Eunsoo Park, Dr. Byungha Shin, Mr. Taeseok Kim, Dr. Hakho Lee, Dr. Jeehoon Kim, Dr. Taegon Kim, Dr. Eunsoo Nam, and many more. Dr. Jeehoon Kim, a newest addition to the Korean society at Harvard, volunteered to stay into the late night so that I can have one more practice talk with him before my thesis defense next morning. I thank him for a kind offering. Dr. Eunsoo Park became a very close "Dong Sang" (younger brother in Korean) and supported me through some of the most difficult times at graduate school. He also introduced me to his church, served me green tea over a pleasant small talk, and many more. I had many lunches with Dr. Byungha Shin while he was a student in the Aziz group. We shared a lot of laughter together, and he served as a trusty designated driver for many of Korean gatherings with beers and Soju. Mr. Taeseok Kim and his lovely wife generously invited me to their home countless times for deliciously home-cooked meals. Taeseok and I also had many fruitful research discussions ranging from electron-beam lithography to nanowire growth. Dr. Taegon Kim offered me many advices on job, women, marriage and anything important in life. Last but not least, Dr. Eunsoo Nam and his graceful wife, while they were on sabbatical at Harvard, graciously invited many of Korean students to their home and served us with wonderful Korean food and drinks so that we can recharge ourselves for the continued endeavor towards our academic goals. I would like to thank all of my Korean friends again.

I would also like to thank my friends at First Korean Church in Cambridge for many prayers, encouragement and love I received during the last year of my PhD

program.

Finally, I would like to dedicate this thesis to my grandma who passed away several years ago in Korea. She would have been ecstatic and much proud knowing that her grandson is graduating with PhD and getting married at the same time. I thank you grandma for your love and courage you have given me when I was a young boy.

Contents

1 Introduction **21**

1.1 Motivation 21

1.2 Overview of the Thesis 23

2 Background Theory **25**

2.1 Vapor-liquid-solid Nanowire Growth 25

2.2 FET Device Physics 27

2.3 Dielectric Confinement effect 35

2.3.1 Single Planar Dielectric Interface 37

2.3.2 Dielectric Quantum Well 39

2.3.3 Dielectric Quantum Dot 41

2.4 Solid State Physics of GaN 43

2.4.1 Crystal Structure 43

2.4.2 Electronic Band Structure 45

3 Experimental Methods **53**

3.1 Catalytic synthesis of GaN Nanowires 53

3.1.1 GaN Nanowires grown by Hydride Vapor Phase Epitaxy . . . 54

3.1.2 GaN Nanowires by Chemical Vapor Deposition 62

3.1.3 Photoluminescence Measurement on GaN nanowires 66

3.2 Fabrication of Nanowire Devices 68

3.2.1 Substrates 68

3.2.2 Substrate Preparation 70

3.2.3 Deposition of Nanowires 72
3.2.4 Electron-Beam Lithography 74
3.2.5 Wire bonding 81
3.2.6 Photolithography 82
3.2.7 Sample Safeguarding 84

4 Measurements on a Nanowire Field Effect Transistor **87**
4.1 Introduction 87
4.2 Experimental Details 88
4.3 Results and Discussion 89
4.4 Conclusions 95

5 Transport Properties of GaN Nanowires **97**
5.1 Introduction 97
5.2 Experiments 98
5.2.1 Nanowires on a SiO_2/Si substrate 98
5.2.2 Suspended Nanowire over a trench 99
5.2.3 SiO_2 coated Nanowires 101
5.3 Results and Discussion 103
5.3.1 Size-dependent Ionization Energy in GaN Nanowires 103
5.3.2 Confirmation of a Size-dependent Ionization Energy in GaN Nanowires 108
5.3.3 Hopping Conduction in GaN Nanowires 109
5.4 Conclusions 116

6 Conclusions and Future Directions **117**
6.1 Conclusions 117
6.2 Future Directions 120

List of Figures

2-1 Schematic diagram illustrating the VLS growth of nanowires. Reactant materials are preferentially absorbed on the liquid alloy and deposited at the liquid-solid interface. 28

2-2 Schematic picture of nanowire capacitors with two different configurations: (a) a nanowire embedded in a SiO_2 dielectric, and (b) a nanowire on top of a SiO_2 dielectric. 29

2-3 Potential contour plots from FEM calculations for a non-embedded nanowire (a) and for an embedded nanowire (b) (taken directly from Ref. [1]). 31

2-4 Calculated capacitance for a nanowire-oxide-metal device for a semiconducting nanowire with three different doping concentrations and for a metallic nanowire approximation. (The metallic approximation is denoted by the open circles.) 34

2-5 Schematic diagram showing a real charge q, and fictitious image charges q' and q'', all at a distance l away from the interface between two dielectrics with relative dielectric constants κ_1 and κ_2. 37

2-6 Electrostatic self-energy of an electron in a GaN wafer in ambient air. 39

2-7 Schematic diagram of a dielectric quantum well: semiconductor in the middle, and an insulating barrier on an each side. 40

2-8 Schematic diagram of a charge q in a dielectric quantum dot (κ_1) embedded in a dielectric (κ_2). 42

2-9 (a) A top view of wurtzite GaN (0001) (b) GaN wurtzite structure. (c) Brillouin zone of the hexagonal lattice corresponding to the wurtzite structure. 44

2-10 Schematic electronic energy band structure near the direct fundamental gap of Wurtzite GaN. The top of the valence band is split by the crystal field and by the spin-orbit interaction into $A(\Gamma_9)$, $B(\Gamma_7)$, and $C(\Gamma_7)$ states. Note: $k_{\parallel} \parallel k_z$ and $k_{\perp} \perp k_z$. HH=heavy hole band, LH=light hole band, and CH=crystal field split-off band. 47

2-11 The prefactor γ for GaN nanowire as a function of the dielectric constant for the surrounding insulator κ_i. The vertical dotted lines indicate the dielectric constants of bulk SiO_2 (κ_i=3.9) and GaN (κ_i=8.9). 51

3-1 (a) Picture of our HVPE system. (b) Schematic diagram of the horizontal HVPE reactor. 55

3-2 X-ray diffraction pattern from HVPE nanowires grown on sapphire substrate (directly taken from Reference [2]). The inset shows the SEM image of the nanowires. (Scale bar: 2μm) 57

3-3 Histogram of the diameters for GaN Nanowires from HVPE. 58

3-4 (a) Low resolution BF (bright field) STEM image shows hexagonal facets of the nanowire; the right side of the sample is chipped off during a microtome procedure. (b) High angle annular DF (dark field) HR STEM shows a hexagonal lattice. Inset shows a selected area diffraction pattern (SADP) indicating the (0001) crystal growth direction . 59

3-5 High Resolution TEM image of a microtomed HVPE GaN nanowire with scale bar of 5 nm (courtesy of JEOL). 60

3-6 EDX spectrum of a microtomed HVPE GaN Nanowire. The inset shows the EDX linescan in the STEM mode with a spot size of 1 nm. Guiding white lines are drawn over the colored lines for clarity. (color) 61

3-7 (a) Picture of our CVD system. (b) Schematic diagram of the horizontal CVD reactor: the 1 cm x 1 cm silicon chip is inside a 1" quartz tube, metal gallium is in a graphite crucible, and mass flow controller (MFC) controls the gas flow. 63

3-8 SEM image of CVD synthesized GaN nanowires. 64

3-9 Histogram of the diameter distribution for GaN Nanowires grown by CVD. 65

3-10 TEM study of a CVD grown GaN nanowire:(a) low resolution BF (bright field) TEM image of a GaN nanowire exhibits dark fringes possibly due to thickness variation or strain, (b) high resolution BF TEM image shows a defect-free lattice, and (c) a selected area diffraction pattern indicates a $(10\bar{1}0)$ crystal growth direction. 67

3-11 Photoluminescence spectra obtained from HVPE and CVD grown GaN nanowires at room temperature. The HVPE and CVD nanowires have diameters of $\sim$ 150 nm and $\sim$ 50 nm, respectively. 69

3-12 SEM image on a 20 μm scale of a deposited GaN nanowire on a substrate with numerical markers (see text). 74

3-13 Schematic view of the electron-beam lithography process. (a) First, nanowires are deposited on the chip. (b) A bilayer of MMA/PMMA is spun on the chip in the spin coating process. (c) An electrode pattern is written on the chip after development. An undercut is formed by using MMA. (d) Metal is then evaporated on the chip. (e) The remaining resist is dissolved in acetone and only the metal electrode pattern remains after the lift-off process. (f) The chip is then wire bonded and mounted on a chip carrier for measurements. 76

3-14 Schematic illustration of Write-field Stitching. 78

3-15 SEM image of multiple contacts made on a short and a long GaN nanowire fabricated by photolithography. 83

3-16 SEM image of a burned-out GaN nanowire due to static electricity. . 85

3-17 Schematic diagram of a low-pass filter attached to the sample. 86

4-1 SEM image (top) and a schematic diagram (bottom) of a nanowire-channel field-effect transistor. 90

4-2 Current I_{SD} versus Voltage V_{SD} at gate biases from -40 to 40 V with 10 V increments. (color) 91

4-3 The resistivity distribution of a sample of 52 CVD-grown GaN nanowires. 92

4-4 A plot of the source-drain current, I_{SD}, versus gate voltage, V_G, for source-drain voltages from 0.1 to 1 V in 0.1 V increments. The inset shows the same data in a log plot. (color) 94

4-5 The resistivity distribution of a sample of 37 HVPE-grown GaN nanowires. 95

5-1 SEM image of a suspended GaN nanowire. 100

5-2 SEM image of a GaN nanowire coated with PECVD SiO_2. 102

5-3 The conductivity versus 1000/T for 15, 25, 45, and 60 nm diameter wires. The points represent experimental data while the lines represent fits over the entire temperature range. The donor activation energy and other fitting parameters are reported in Table 5.1. The inset shows a scanning electron micrograph of an actual nanowire device described in the text. 104

5-4 Activation energies from the fit of the data given in Figure 5-3 as a function of inverse wire radius. The lines are linear fits to the experimental data. 106

5-5 The conductivity versus 1000/T for suspended nanowires with 20, 28, and 40 nm diameters. The points represent experimental data while the lines represent fits over the entire temperature range. 110

5-6 Activation energies for the suspended nanowires from the fit of the data given in Figure 5-5 as a function of inverse wire radius. The lines are linear fits to the experimental data. 111

5-7 The conductivity versus 1000/T for the SiO_2 coated nanowires with 27, 36, and 96 nm diameters. The points represent experimental data while the lines represent fits over the entire temperature range. For the 27 nm diameter nanowire, the fitting does not include the last two data points because at these low temperature points a gap structure developed for this nanowire. 112

5-8 Activation energies for the SiO_2 coated nanowires from the fit of the data given in Figure 5-7 as a function of inverse wire radius. The lines are linear fits to the experimental data. 113

5-9 A plot of $\ln \sigma$ versus inverse temperature in the low temperature region for the 60 nm nanowire. The fitting parameters for the Mott hopping conduction are reported in Table 5.2. 115

List of Tables

2.1 Lattice constants a, c, and unit cell parameter u for GaN at room temperature, and coefficient of thermal expansion for GaN [3]. . . . 45

2.2 Comparison of values for the fundamental band gap of wurtzite and zincblende GaN at room temperature reported in the literature [4]. . 46

3.1 Growth Data for HVPE and CVD. 65

4.1 Electrical Data for HVPE and CVD Nanowire FETs. There are missing values for some parameters for HVPE wires because even the thinnest of HVPE wires was too thick to reach a complete depletion of the carriers, which is needed for some of the characterizations. 96

5.1 The fitting parameters for the conductivity as a function of temperature given in Eq. (5.2) for nanowires with four different diameters. The 15nm nanowire has a large $\tilde{\chi}^2$ value because the curve fitting is poor in the low temperature region. The deviation of the fitting curve from the experimental data points is not noticeable in the provided linear plot (Figure 5-3). We also didn't find two values for the ionization energy for the 15 nm nanowire and therefore excluded the data point for the 15 nm nanowire in Figure 5-4. 105

5.2 The fitting parameters to Eq.(5.5) for the nanowire with a diameter of 60 nm. Other nanowires did not display the clear characteristics of the variable-range hopping conduction. 114

Chapter 1

Introduction

1.1 Motivation

In the field of solid-state physics, the advancement of materials growth and physics seems to progress hand in hand. For example, the experimental observation of the Quantum Hall Effect in the 2D electron gas in 1980 [5] wasn't possible until the science of crystal growth was mature enough to produce a material with a high chemical purity and a nearly perfect crystal structure. The present capability to grow a nearly perfect crystal and to do high resolution lithography opened up a new exciting branch of physics. The study of quantum effects in reduced dimensional system has been an active field of research for more than two decades now. In a structure where one or more dimensions is comparable to or smaller than the Fermi wavelength, or the elastic scattering length of the carriers, or both, quantum effects, such as electron interference and diffraction effects, can be observed. Another interesting reduced dimensional system is the 0D quantum dot system. A quantum dot is a small box about 100 nm on a side with a tunable number of electrons and is often nicknamed an "artificial atom" [6, 7, 8]. A quantum dot became an ideal testing bed for quantum mechanics and the effects of electron-electron interactions because of the ability to readily tune the relevant parameters in the quantum dot. In addition to semiconductor quantum dots, large molecular structures, such as carbon nanotubes [9, 10] and C_{60} buckyballs [11] were used to study quantum phenomena in reduced dimensional systems.

In addition to the desire to study quantum physics in small structures, there has been a need to miniaturize electronic devices. The advantage of smaller devices includes a higher density of integration, faster response, lower cost, and less power consumption. The growing needs for faster computer processors and high-density memory devices have been driving the microelectronics industry to decrease the size of the individual circuit components by pushing the limits of current silicon-based transistor technology, such as silicon-on-insulator, vertically stacked three-dimensional transistors, and thinner dielectric insulators with a higher dielectric constant. The advancement of the silicon transistor technology relies on the top-down approach, where the size of a component is set by lithographic limitations. The lithographic limitations are fundamentally set by the optics, and practically by the cost of improving optical systems. Eventually the cost of reducing the size of devices will exceed the economic gain from a new line of devices and this prediction prompts an entirely new approach to fabricating smaller devices.

The recent surge of research activities to synthesize nanostructured materials chemically is largely due to the aforementioned impending limitation of the current top-down approach. One example is the discovery of carbon nanotubes by Iijima in 1991 [12]. A carbon nanotube is a graphene sheet wrapped seamlessly into a cylinder. The diameter can vary from ~1nm for single-walled nanotubes to ~10nm for multi-walled nanotubes. Due to the near atomic size of carbon nanotubes, there have been various reports of novel phenomena such as ballistic conduction [13, 14], coulomb blockade effects [9, 10], single electron tunneling, and spin-charge separation, known as the Luttinger-liquid [15]. Even though a carbon nanotube is a fascinating material, its application to electronic devices is limited due to two major drawbacks. First, nanotube growth yields either a metallic or semiconducting tube depending on its diameter and helicity [16, 17]. Therefore, the selective growth of carbon nanotubes does not seem feasible at this time. Secondly, the controlled doping of semiconducting nanotubes is not viable. However, semiconducting nanowires don't suffer from these constraints on carbon nanotubes [18]. Besides being semiconducting, nanowires are also reported to display mechanical robustness [19], higher

luminescence efficiency [20], lowered lasing threshhold [21], and enhanced thermoelectric performance [22, 23, 24]. These attractive traits give semiconducting nanowires potential advantages for advanced materials for the next generation of devices.

The GaN nanowire is our choice of a nanostructured material for detailed study because of its potential applications in nanotechnology. Due to its wide bandgap (3.4 eV for bulk wurtzite GaN at 300 K), GaN is a key material for a UV/blue laser diode used in high-density optical drives (DVD player/recorder) and high-power/speed transistors. Further, a GaN nanostructure can potentially have even superior device performance relative to devices based on bulk GaN, such as an enhanced optical efficiency and a lowered lasing threshold due to the quantum confinement effect.

There are two basic questions which this thesis tries to answer: (1) What are the device characteristics of GaN semiconducting nanowires ? What limits their device performance? What can be done to improve their device performance? (2) What do the electronic properties of nanowires depend on? How does the size of a nanowire affect the electronic properties of a nanowire in the mid-size range (20 nm $\sim$ 100 mn)? How does the surrounding dielectric affect the electronic properties of nanowires ?

1.2 Overview of the Thesis

Chapter 2 tries to provide the necessary background material on the physics of semiconductor nanowires, and discusses vapor-liquid-solid (VLS) synthesis of a semiconductor nanowires, the modeling of a field effect transistor based on a nanowire, the crystal structure and electronic band structure of GaN nanowires, and the dielectric confinement effect in semiconducting nanostructures.

Chapter 3 covers the experimental methods used in the study of semiconductor nanowires. The actual synthesis methods used in this work, namely hydride vapor phase epitaxy (HVPE) and chemical vapor deposition (CVD), are described in detail. The grown nanowires are crystallographically and chemically characterized by transmission electron microscopy (TEM) and scanning electron microscopy (SEM). Photoluminescence data from HVPE and CVD grown GaN nanowires are compared

and discussed. Following the description of the synthesis of GaN nanowires, the fabrication process of a field effect transistor is given, and recipes for the processing are listed as needed.

Chapter 4 is devoted to the electrical measurements and characterization of GaN nanowire field effect transistors. The drain and source metal electrode contacts are made to GaN nanowires using electron-beam lithography, and capacitive gate coupling is provided by the degenerately doped backside silicon substrate, and the details of the device preparation and characterization are described. The carrier density of a GaN nanowire is extracted along with an electron mobility, a switching on-off ratio, a mean resistivity, and a contact resistivity.

Chapter 5 presents the heart of this thesis, the transport properties of GaN nanowires. The conductivity of GaN nanowires is measured as a function of temperature, wire diameter, and the surrounding dielectric constant. This chapter discusses the size-dependent confinement effect present in the mid-sized nanowires with a diameter larger than 20 nm. Discussion of a possible hopping conduction mechanism in a nanowire is also given.

Lastly, Chapter 6 summarizes the findings of this thesis, and suggestions for future experiments are presented.

Chapter 2

Background Theory

In this chapter, we try to provide pertinent background material on semiconducting nanowires. Section 2.1 describes how nanowires grow by a catalytic growth mechanism called the vapor-liquid-solid (VLS) mechanism. In section 2.2, the capacitor model for nanowire devices is discussed using both metallic and non-metallic approximations and a comparison between the two results is given. In section 2.3, the size effect due to the dielectric confinement in nanostructures is discussed using classical electrostatics for simplified cases. Lastly, in section 2.4, the crystal structure and electronic band structure for bulk GaN are presented along with a necessary dielectric confinement correction that is calculated for the ionization energy of an impurity in GaN nanowires.

2.1 Vapor-liquid-solid Nanowire Growth

The catalytic growth of nanowires is based on the vapor-liquid-solid (VLS) mechanism [25], where nanowires grow from a seed, which is a catalyst eutectic droplet. Let us first examine the example of silicon nanowire growth from an Au nanoparticle catalyst. A liquid droplet of catalytic material and semiconducting material forms above the eutectic temperature. As the liquid droplet becomes saturated by semiconducting material, two phases, the Au-Si alloy liquid phase and the Si solid phase, develop. This is when the nanowire nucleation starts (Figure 2-1).

In the VLS mechanism, the diameter of a nanowire is controlled by three major factors [26]. First, the size of the catalyst defines the size of the eutectic droplet for the growth seed. Second, the size of the droplet is further determined by the growth temperature which controls the solubility of the reactants. Last, vapor-solid growth can take place on the surface of nanowires and can increase the diameter when the vapor pressure of the reactants is above a critical value.

The nanowire lengthwise growth results from the difference in accommodation coefficient of the eutectic liquid droplet and the nanowire as illustrated in Figure 2-1. The accommodation coefficient of the eutectic liquid droplet is orders of magnitude larger than that of the nanowire. In another words, the eutectic liquid droplet is the preferential site for absorption of the gaseous reactants. When the droplet is saturated, the semiconducting solid nucleates and crystallizes at the liquid-solid interface. One-dimensional nanowire growth continues as long as the catalyst remains liquid and the gaseous reactants are supplied. When the reaction furnace cools down, the growth of the nanowire terminates with the solid alloy nanoparticle remaining on the tip of the nanowire. As discussed so far, thermodynamics determines whether or not a nanowire can grow under a given condition of temperature, pressure, and concentration for each composition material.

Kinetic theory determines how fast the nanowire can grow and what this growth rate depends on. The lengthwise growth rate was studied as a function of the wire diameter, and the growth rate was observed to be slower with the smaller diameter wire [27]. This growth rate dependence can be described by a Gibbs-Thomson effect:

$$\delta\mu = \delta\mu_0 - \frac{4\Omega\sigma_s}{d}, \tag{2.1}$$

where $\delta\mu$ is the difference in the chemical potential between the gas and solid phase of the nanowire material, $\delta\mu_0$ is for the bulk case ($d \to \infty$), σ_s is the surface free energy of the nanowire, and Ω is the atomic volume of the nanowire. The $\delta\mu$ term drives the nanowire growth and the growth terminates when $\delta\mu = 0$. Therefore, we

can determine the critical diameter for the nanowire growth:

$$d_c = \frac{4\Omega\sigma_s}{\delta\mu_0}. \tag{2.2}$$

The nanowire growth dependence on the diameter of the nanowire is generally accepted but the actual minimum diameter for a particular nanowire requires more detailed atomistic theory and this topic is still under debate [28, 29, 30]. Furthermore, the recent in situ TEM experiment by Kodambaka *et al.* [31] revealed that the nanowire can still grow below the eutectic temperature under certain conditions either by VLS (vapor-liquid-solid) or VSS (vapor-solid-solid) mechanisms. All these nanowire growth studies were done on a limited number of rather simple semiconducting systems, such as Si [28, 29, 30] and Ge [31]. Understanding of the GaN nanowire growth process has been much less investigated. A good ternary phase diagram does not presently exist, which adds difficulty to understanding the GaN nanowire growth process.

2.2 FET Device Physics

Dating back to the first time nanotubes were introduced, one of the first devices based on the nanotube was a field effect transistor device [32], an elemental building block for nanodevices. The model that was developed at that early time was based on a metal cylinder-oxide-metal plate. This simple model worked well for a carbon nanotube FET because a nanotube is a hollow cylinder made out of a graphene sheet. Following this approach, when semiconducting nanowires were first synthesized successfully [18, 20], there were a lot of reports about fabricating field effect transistors from them and the same exact model used for carbon nanotubes was used to extract their carrier density (Eq. (2.19)), and carrier mobility (Eq. (2.20)) [18, 33]. The question is whether this same model is valid for semiconducting nanowires. This section of chapter 2 describes the model used for a nanowire field effect transistor (FET) device and discusses the constraints and limitations of the model.

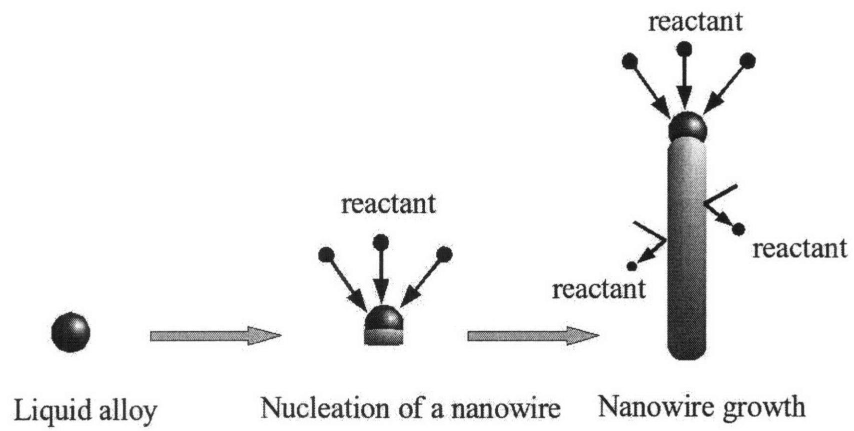


Figure 2-1: Schematic diagram illustrating the VLS growth of nanowires. Reactant materials are preferentially absorbed on the liquid alloy and deposited at the liquid-solid interface.

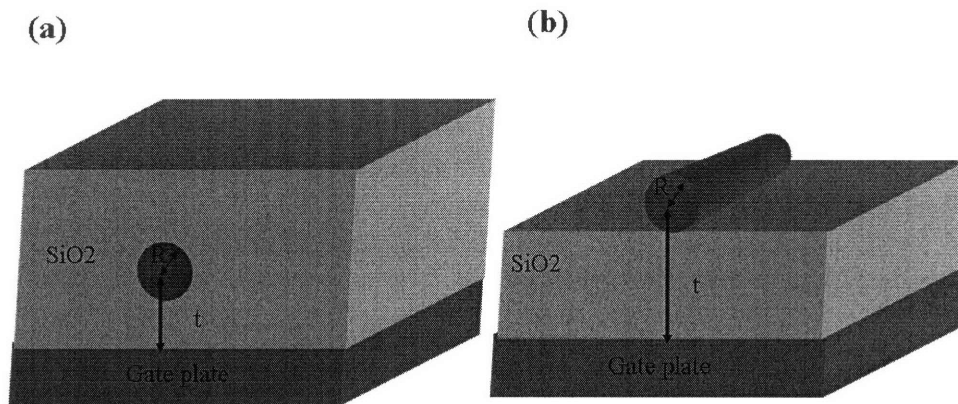


Figure 2-2: Schematic picture of nanowire capacitors with two different configurations: (a) a nanowire embedded in a SiO_2 dielectric, and (b) a nanowire on top of a SiO_2 dielectric.

First, we will consider two different configurations for nanowire FETs as shown in Figure 2-2 and discuss how these two differ from each other. Next, we will derive the expression for the capacitance of a metal cylinder-oxide-metal plate, and a semiconducting wire-oxide-metal plate [34]. Lastly, we compare each model and discuss the condition in which the metallic approximation is still valid.

A field effect transistor based on nanowires has been frequently fabricated using a back-gate geometry because of the ease of fabrication. Our work also uses the back-gate geometry where a nanowire is placed on top of a degenerately doped oxidized silicon wafer (Figure 2-2(b)). However, the better configuration is the so-called wrap-arround gate where a nanowire is embedded in a dielectric material. This configuration enhances the gate coupling and also the gate breakdown voltage according to Wunnicke [1]. For the back-gate configuration (Figure 2-2(b)) with a missing dielectric material around the nanowire, the analytic expression for the capacitance (Eq. (2.5)) gives an upper limit for the capacitance. This overestimation can lead to an underestimation for the field effect mobility values in the literature according to Eq. (2.20). This overestimation of the capacitance can be remedied by using a smaller effective dielectric constant for the oxide provided that the dielectric constant for the oxide is not too different from that of the ambient atmosphere. For the case of SiO_2, the effective dielectric constant is found to be 2.2 [1]. According to the finite element method (FEM) calculation [1] shown in Figure 2-3, the electric field crowds under the nanowire much more for the back-gate configuration (Figure 2-3(a)) than the embedded nanowire configuration (Figure 2-3(b)). This field crowding effect results in a breakdown of the oxide at a lower gate bias for the back-gate configuration than for the embedded wire configuration.

The model used for nanowire FETs by most workers is a metallic cylinder-oxide-metal plate. This model is known to still be valid for nanowires with a doping concentration of 10^{17} cm^{-3} or higher [35]. Let us explore this issue.

Let us now consider an infinitely long metallic cylinder of radius R with charge per unit length $\delta\lambda$, embedded in a medium with a dielectric permittivity of κ_i and distance t away from the metal gate, as illustrated in Figure 2-2(a). The capacitance

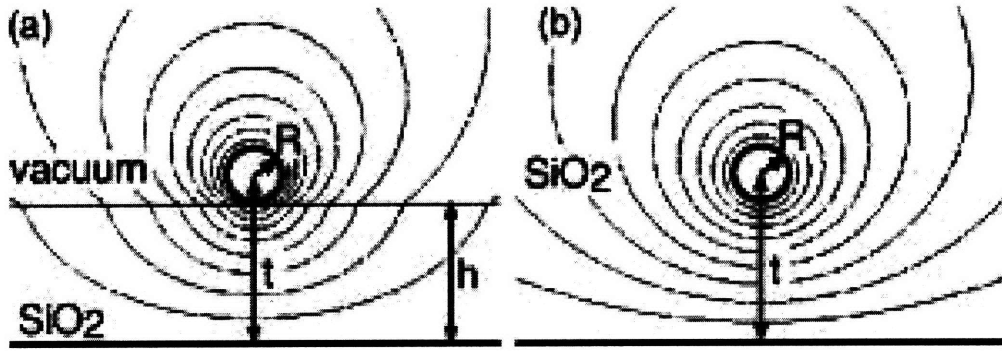


Figure 2-3: Potential contour plots from FEM calculations for a non-embedded nanowire (a) and for an embedded nanowire (b) (taken directly from Ref. [1]).

per unit length is defined as

$$\frac{C}{L} \equiv \frac{\delta\lambda}{\delta\phi}, \tag{2.3}$$

where $\delta\phi$ is the change in the electrostatic potential and the expression for the metallic cylinder is

$$\frac{C}{L} = \frac{2\pi\kappa_i\varepsilon_0}{\cosh^{-1}(t/R)}. \tag{2.4}$$

When $t/R \gg 1$, which is the case with our nanowire FETs (see Figure 2-3), the expression is further reduced to

$$\frac{C}{L} \approx \frac{2\pi\kappa_i\varepsilon_0}{\ln[2(t/R)]}. \tag{2.5}$$

The definition for the capacitance Eq. (2.3) holds for metallic conductors since $\delta\phi$ is constant for the whole body of the conductor. This isn't true for a semiconducting nanowire because the electric field can penetrate into the body of the wire and the electrostatic potential $\delta\phi$ has a radial dependence now. Thus we cannot use Eq. (2.3) to calculate the capacitance for a semiconducting nanowire.

For a non-metallic nanowire, the semiclassical model developed by Krčmar *et al.*[34] is used. For our nanowire system with a diameter larger than 20 nm, a semiclassical model is valid because the density of states is quasicontinuous. For a non-metallic

nanowire, the density of states at the Fermi level is finite and this can lead to a non-uniform carrier density. In this case, the drift-diffusion equation gives the current density as

$$\mathbf{j} = \sigma \mathbf{E} - D \nabla \rho, \tag{2.6}$$

where D is a diffusion constant and ρ is the charge density. Combining with the steady current condition

$$\nabla \cdot \mathbf{j} = 0, \tag{2.7}$$

leads to the differential equation

$$\nabla^2 \rho - \frac{\rho}{l^2} = 0, \quad l = \sqrt{\frac{\varepsilon_0 D}{\sigma}}. \tag{2.8}$$

The length l introduced here is the distance which an added electron penetrates into the bulk of the wire and it is called the screening length. This is the parameter which is needed to describe the electrostatics in a non-metallic nanowire.

According to Büttiker [36] and Natori [37], the experimentally relevant capacitance for a nanostructured semiconductor is the electrochemical capacitance which is defined as

$$\frac{C}{L} \equiv -e \frac{\delta \lambda}{\delta \tilde{\mu}}, \tag{2.9}$$

where the electron electrochemical potential is defined as $\delta\tilde{\mu} = \mu - e\phi$ and it is constant throughout the bulk of a non-metallic conductor in thermodynamic equilibrium. Using this new definition for the capacitance (Eq. (2.9)), Krčmar *et al.*[34] derive an expression for the electrostatic field inside a non-metallic cylinder as

$$\phi_{in} = A I_0(k_b r) - \frac{\delta\tilde{\mu}}{e}, \quad k_b \equiv \left(\frac{\kappa_{nw}\varepsilon_0}{e^2} \left. \frac{\partial \mu_b}{\partial n_b} \right|_{n_{b0}} \right)^{-1/2}, \tag{2.10}$$

where k_b is the inverse of the screening length, n_{b0} is the equilibrium electron number density for $\delta\lambda$=0, $I_n(x)$ is the nth order modified Bessel function and A is a constant.

The field outside the wire is calculated using the method of images. The method of images gives the change in the electrostatic potential on a symmetry plane directly

below the nanowire due to the added charge per unit length of $\delta\lambda$ as [35]

$$\phi_{out}(r) = \frac{\delta\lambda}{2\pi\kappa_{out}\varepsilon_0} \ln\left(\frac{2t-r}{r}\right). \tag{2.11}$$

The constants A and $\delta\tilde{\mu}_b$ are determined from the boundary conditions at $r = R$ on the symmetry plane

$$\phi_{in} = \phi_{out}, \qquad \kappa_{nw}\frac{\partial\phi_{in}}{\partial r} = \kappa_{out}\frac{\partial\phi_{out}}{\partial r}. \tag{2.12}$$

Once the constants A and $\delta\tilde{\mu}_b$ are solved for, the capacitance per unit length for the non-metallic conductors can be found by employing Eq. (2.9) with $\delta\tilde{\mu} = \delta\tilde{\mu}_b$ [34]. Applying the boundary conditions Eq. (2.12) yields

$$A = -\frac{\delta\lambda}{2\pi\kappa_{nw}\kappa_{out}\varepsilon_0}\frac{2t}{(2t-R)R}\frac{1}{k_b I_1(k_b R)}, \tag{2.13}$$

$$\text{and} \quad \delta\tilde{\mu} = -\frac{e\delta\lambda}{2\pi\kappa_{out}\varepsilon_0}\left[\ln\left(\frac{2t-R}{R}\right) + \frac{1}{\kappa_{nw}k_b R}\frac{2t}{2t-R}\frac{I_0(k_b R)}{I_1(k_b R)}\right]. \tag{2.14}$$

Finally, the capacitance per unit length of the non-metallic wire shown in Figure 2-2 (a) is

$$\frac{C}{L} = 2\pi\kappa_{out}\varepsilon_0\left[\ln\left(\frac{2t-R}{R}\right) + \frac{1}{\kappa_{nw}k_b R}\frac{2t}{2t-R}\frac{I_0(k_b R)}{I_1(k_b R)}\right]^{-1}. \tag{2.15}$$

For $t \gg R$, Eq. (2.15) reduces to

$$\frac{C}{L} \approx 2\pi\kappa_{out}\varepsilon_0\left[\ln\left(\frac{2t}{R}\right) + \frac{1}{\kappa_{nw}k_b R}\frac{I_0(k_b R)}{I_1(k_b R)}\right]^{-1}. \tag{2.16}$$

The capacitance per unit length for a semiconducting nanowire with three different doping concentrations, $N_D = 1.3 \times 10^{18}$, 10^{17}, and 10^{16} cm^{-3}, are calculated using Eq. (2.16) and the results are plotted in Figure 2-4. For the calculation of the capacitance for a nanowire with $N_D = 1.3 \times 10^{18}$ cm^{-3} (degenerate case), the Thomas-Fermi screening length (Eq. (2.17)) is used, and for the lower concentrations (non-degenerate case), the Debye screening length (Eq. (2.18)) is used. Here we assume the effective mass for GaN to be 0.22 m_e and the temperature to be 300 K. We also used an effective dielectric constant of $\kappa_i = 2.2$ for SiO_2 as discussed in the

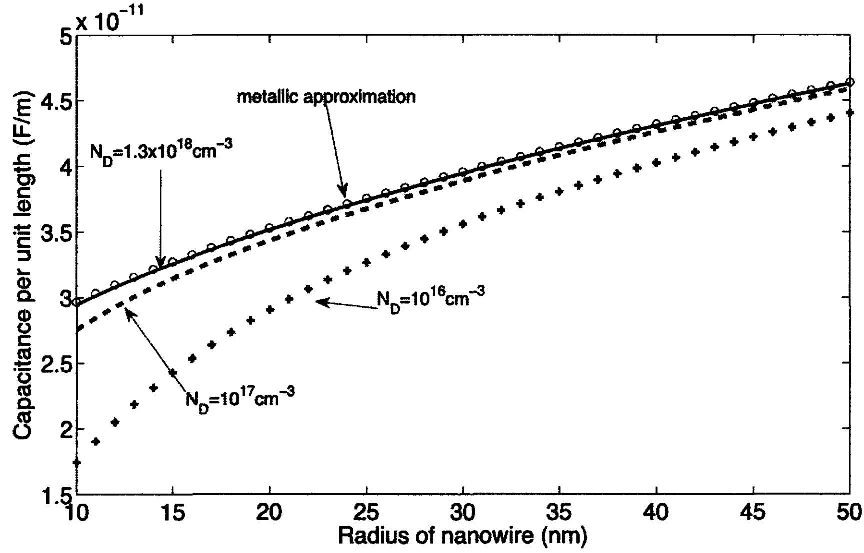


Figure 2-4: Calculated capacitance for a nanowire-oxide-metal device for a semiconducting nanowire with three different doping concentrations and for a metallic nanowire approximation. (The metallic approximation is denoted by the open circles.)

beginning of this section. The metallic nanowire calculation is done using Eq. (2.5). As we can see from Figure 2-4, the calculated capacitances using the model for a semiconducting wire and for a metallic wire fall on top of each other for a doping concentration of around 10^{18} cm^{-3}. Even the capacitance for a doping concentration of 10^{17} cm^{-3} is not too far off from the metallic approximation for wires with a radius larger than 20 nm or so. This calculation shows that the metallic approximation for a semiconducting nanowire system is valid for nanowires with large diameter (D>20 nm) and a moderately high doping level ($N_D \geq 10^{18}$ cm^{-3}). We also note that a similar calculation was done by Vashaee *et al.* [35]. The Thomas-Fermi screening length is given as

$$r_{TF} = \pi^{2/3}\sqrt{\frac{\kappa_{nw}\epsilon_0\hbar^2}{e^2m^*(3n)^{1/3}}}, \tag{2.17}$$

where n is the carrier density which is assumed to be the same as the doping concentration and the Debye screening length is

$$r_D = \sqrt{\frac{\kappa_{nw}\epsilon_0 k_B T}{e^2 n}}. \tag{2.18}$$

The carrier density can be calculated using

$$n = V_{th}C/(e\pi R^2 L), \tag{2.19}$$

where R and L are radius and length of the nanowire, respectively. The field effect mobility μ_{FE} is estimated by

$$\mu_{FE} = \frac{dI_{SD}}{dV_G}\frac{L^2}{CV_{SD}}, \tag{2.20}$$

where I_{SD}, V_{SD}, and V_G are source-drain current and bias, and gate bias, respectively.

As we discovered earlier, we can use the metallic approximation for GaN nanowires with a doping concentration higher than 10^{18} cm^{-3} and thus the capacitance values for our GaN nanowires are calculated using the metallic approximation (Eq. (2.5)). Once the capacitance value is known and the threshold voltage V_{th}, which is applied to deplete the carriers completely from the nanowire, is measured, the carrier density n in the nanowire is approximated by Eq. (2.19). This calculation shows that our CVD GaN nanowires have a carrier concentration of $\sim 4 \times 10^{19}$ cm^{-3}.

2.3 Dielectric Confinement effect

The discussion in this section is mostly inspired and borrowed from the book by Delerue and Lannoo [38]. Typical nanodevices are made out of a semiconductor nanostructure, metal electrodes, and dielectrics. Having dielectric discontinuities in a nano-sized semiconductor device can modify the electric field lines in and out of the semiconductor and thus lead to an enhancement or reduction of the long-range Coulomb interaction depending on the relative sizes of the pertinent dielectric constants. The so-called dielectric confinement effect was first predicted by Keldysh [39]. The dielectric confinement effect modifies not only the field produced by the charge but also introduces a new term called the self-energy correction, which relates to the charge's own field acting on itself by inducing polarization charges on nearby surfaces and interfaces. Relating to this effect, a question arises about whether the macro-

scopic dielectric model is still valid for nanostructures and, if so, to what extent is it valid. It has been pointed out by Delerue *et al.* [40] that the macroscopic dielectric constant is the bulk value a few Fermi wavelengths away from the surface and the average dielectric constant decreases with decreasing size of the nanostructure due to the increasing contribution from the surfaces. This means that we can still use the macroscopic dielectric constant for our nanowires, which have diameters larger than 15 nm.

Now we develop a general expression for the self-energy. The Coulomb interaction between point charges q and q', both in an homogeneous bulk solid with dielectric constant κ_b, is

$$V_b(\mathbf{r}, \mathbf{r}') = \frac{qq'}{4\pi\kappa_b\epsilon_0|\mathbf{r} - \mathbf{r}'|}. \tag{2.21}$$

However, the actual Coulomb interaction, $V(\mathbf{r}, \mathbf{r}')$, can differ from the bulk Coulomb interaction due to the nearby surfaces or interfaces. Let us imagine bringing infinitesimal charges dq' at the position $\mathbf{r}$ to accumulate a total charge q. The electrostatic potential due to a point charge q' is

$$\phi(\mathbf{r}) = \frac{q'}{4\pi\kappa_b\epsilon_0 r} = f(\mathbf{r})q'. \tag{2.22}$$

Then the electrostatic energy required to add infinitesimal charge dq' to q' is $f(\mathbf{r})q'dq'$. A simple integration gives us the self-energy of the charge q as

$$\Sigma(\mathbf{r}) = \int_0^q f(\mathbf{r})q'dq' = f(\mathbf{r})\frac{q^2}{2} = \frac{1}{2}q\phi_{ind}(\mathbf{r}), \tag{2.23}$$

where $\phi_{ind}(\mathbf{r})$ is the macroscopic electrostatic potential due to the polarization charges at the surfaces and interfaces of the system. The factor $\frac{1}{2}$ comes from the adiabatic building up of the total charge q. The induced potential can be obtained by removing the bulk potential part from the total potential [38]:

$$\phi_{ind}(\mathbf{r}) = \lim_{\mathbf{r}' \to \mathbf{r}} \left[\phi(\mathbf{r}') - \phi_b(\mathbf{r}')\right]. \tag{2.24}$$

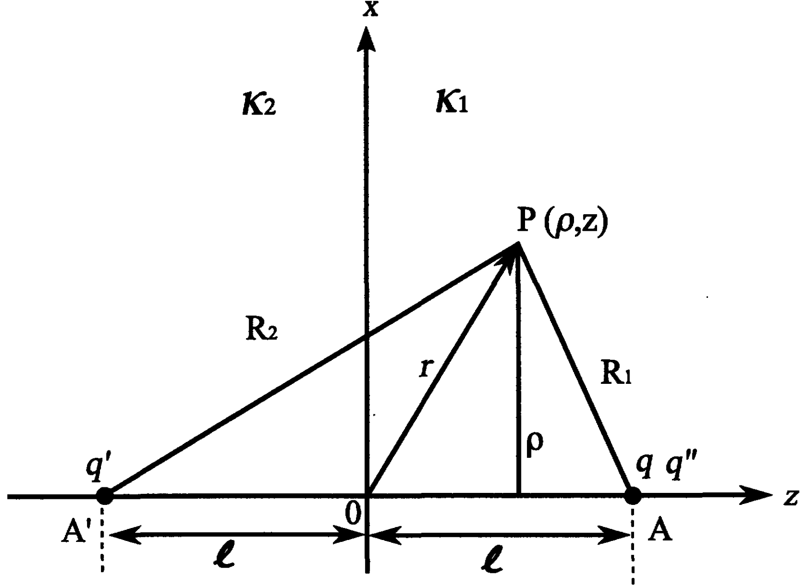


Figure 2-5: Schematic diagram showing a real charge q, and fictitious image charges q' and q'', all at a distance l away from the interface between two dielectrics with relative dielectric constants κ_1 and κ_2.

Using Eq. (2.23) and Eq. (2.24) together, we get

$$\Sigma(\mathbf{r}) = \frac{1}{2} \lim_{\mathbf{r}' \to \mathbf{r}} \left[V(\mathbf{r}, \mathbf{r}') - V_b(\mathbf{r}, \mathbf{r}') \right]. \tag{2.25}$$

In the following sections, we apply classical electrostatics to a number of simple structures to get further insight into how the presence of a dielectric interface modifies the Coulomb energy of the system. The method developed here will prepare us to understand the dielectric confinement effect in nanowires.

2.3.1 Single Planar Dielectric Interface

The following example illustrate the self-energy correction due to the existence of the polarization charges at the interface between two different dielectrics. Let us consider a point charge q embedded in a semi-infinite dielectric at a distance l from the plane interface between two dielectrics 1 and 2 with relative dielectric constants κ_1 and κ_2,

respectively, as shown in Figure 2-5. The charge q induces polarization charges at the interface and this adds a self-energy term to the electrostatic energy of the charge q. Using the method of images [41], we can calculate the electrostatic field in both dielectrics 1 and 2. In region 1 ($z > 0$), the electrostatic potential at a point P is due to the real charge q and a fictitious charge q'. The sum of the two potential gives

$$\phi_1(\mathbf{r}) = \frac{1}{4\pi\kappa_1\epsilon_0}(\frac{q}{R_1} + \frac{q'}{R_2}), \tag{2.26}$$

where $R_1 = \sqrt{\rho^2 + (l-z)^2}$, and $R_2 = \sqrt{\rho^2 + (l+z)^2}$ in cylindrical coordinates (ρ, ϕ, z).

In the region 2 ($z < 0$), the potential is equivalent to that of a fictitious charge q'' at the position A:

$$\phi_2(\mathbf{r}) = \frac{1}{4\pi\kappa_2\epsilon_0}\frac{q''}{R_1}. \tag{2.27}$$

The charges q' and q'' can be expressed in terms of q using the boundary conditions at the interface ($z = 0$):

$$\begin{aligned} \kappa_1 E_z(0^+) &= \kappa_2 E_z(0^-), \\ E_x(0^+) &= E_x(0^-), \\ E_y(0^+) &= E_y(0^-). \end{aligned} \tag{2.28}$$

Then the image charges q' and q'' are

$$\begin{aligned} q' &= \frac{\kappa_2 - \kappa_1}{\kappa_2 + \kappa_1} q, \\ q'' &= \frac{2\kappa_2}{\kappa_2 + \kappa_1} q. \end{aligned} \tag{2.29}$$

Using the expressions Eq. (2.25), the electrostatic self-energy of the charge q is

$$\Sigma(l) = \frac{qq'}{16\pi\kappa_1\epsilon_0 l} = \frac{q^2}{4\pi\kappa_1\epsilon_0 l}\frac{\kappa_1 - \kappa_2}{4(\kappa_1 + \kappa_2)}. \tag{2.30}$$

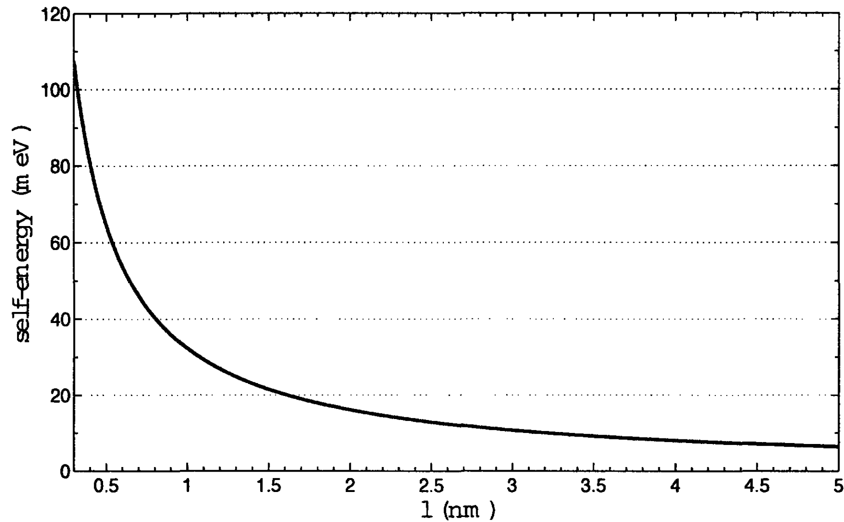


Figure 2-6: Electrostatic self-energy of an electron in a GaN wafer in ambient air.

From this simple calculation we can find the self-energy as a function of the distance l which denotes the distance from a real charge q to the interface between dielectrics. The electrostatic self-energy can be substantial in nanostructures where there is a significant mismatch between nearby dielectrics. To illustrate this point, we calculated the self-energy of the electron embedded in a semi-infinite GaN solid ($\kappa_1 \approx 8.9$) in an ambient gas ($\kappa_2 = 1$) using Eq. (2.30) and plotted the result in Figure 2-6. The self-energy is shown to range from a few tens of meV for an electron at distance a few nanometers away from the interface with the ambient gas to large values of more than 100 meV when l reaches the unit cell dimension of GaN (0.3 nm).

2.3.2 Dielectric Quantum Well

The enhancement of the long-range Coulomb interaction in a so-called dielectric quantum well structure was first studied by Keldysh [39]. The enhanced long-range Coulomb interaction comes from the reduction of the effective dielectric constant of the whole system due to the penetration of the electric field into the barriers with a smaller dielectric constant than the well. This effect can be exploited to control the optical properties such as the binding energy and oscillator strength of exci-

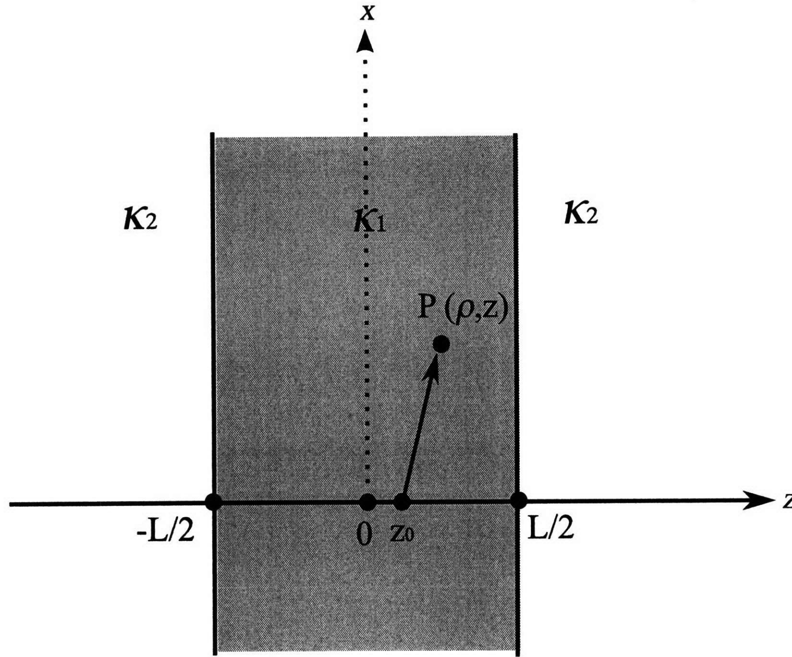


Figure 2-7: Schematic diagram of a dielectric quantum well: semiconductor in the middle, and an insulating barrier on an each side.

tons in semiconducting devices [39, 42]. Let us consider a sandwich structure of an insulator-semiconductor-insulator structure with a charge q sitting at the position $(\vec{\rho}=0, z=z_0)$ in a cylindrical coordinate system, as shown in Figure 2-7.

The calculation shown here was done using the method of images following the work by Kumagai *et al.* [42]. For the system with two image planes, an infinite series of image charges are formed at the points given by

$$z_n = nL + (-1)^n z_0, \quad n = \pm 1, \pm 2, \ldots. \tag{2.31}$$

Applying boundary conditions at each interface, we get all of the image charges:

$$\begin{aligned} q_n &= q\gamma^{|n|}, \quad \gamma = \left(\frac{\kappa_1-\kappa_2}{\kappa_1+\kappa_2}\right) \quad (n=0,\pm 1,\pm 2,\ldots), \\ q_n' &= q_n\frac{2\kappa_2}{\kappa_1+\kappa_2} \quad (n=0,1,2,\ldots), \\ q_n'' &= q_n\frac{2\kappa_2}{\kappa_1+\kappa_2} \quad (n=0,-1,-2,\ldots), \end{aligned} \tag{2.32}$$

where q_n, q'_n, and q''_n produce the electrostatic field in the middle well , left barrier, and right barrier, respectively. We note that q'_n and q''_n share the same values due to the two symmetric barriers. Summing up the contribution from all q_n's leads to the total electrostatic potential in the well:

$$\phi(\rho, z) = \sum_{n=-\infty}^{\infty} \frac{q\gamma^{|n|}}{4\pi\kappa_1\epsilon_0\{\rho^2 + [z - (-1)^n z_0 - nL]^2\}^{1/2}}. \tag{2.33}$$

The above equation predicts an enhancement or a reduction of the long-range Coulomb interaction depending on the sign of γ. For $\kappa_1 > \kappa_2 \quad (\gamma > 0)$, the sum in Eq. (2.33) is larger than the single term with $n = 0$, namely the bulk potential (ϕ_b) and for $\kappa_1 < \kappa_2 \quad (\gamma < 0)$ the sign of the image charges alternates between positive and negative, and thus the sum is less than the bulk potential (ϕ_b). As we have already seen from the previous example, a dielectric quantum well can result in an enhancement of the long-range Coulomb interaction, i.e. exciton binding energy.

The self-energy can be also found by applying Eq. (2.25):

$$\Sigma(z) = \frac{1}{2} \sum_{n=\pm1,\pm2,\ldots} \frac{q^2\gamma^{|n|}}{4\pi\kappa_1\epsilon_0|z - (-1)^n z - nL|}. \tag{2.34}$$

2.3.3 Dielectric Quantum Dot

Let us imagine that a quantum dot of radius R and relative dielectric constant κ_1 is embedded in a medium of relative dielectric constant κ_2 (Figure 2-8). Then the electrostatic potential at $\vec{r}$ (for $s \le r \le R$) due to a charge q positioned at ($\rho = s, \theta = 0, \varphi = 0$) inside the dot can be expressed in terms of Legendre polynomials. Applying proper boundary conditions (Eq. (2.36)) gives [43]

$$\phi(\vec{r}) = \frac{q}{4\pi\kappa_1\epsilon_0}\left\{\frac{1}{|\vec{r} - \vec{s}|} + \sum_{n=0}^{\infty} \frac{r^n s^n P_n(cos(\theta))}{R^{2n+1}} \frac{(\kappa_1 - \kappa_2)(n+1)}{[\kappa_2 + n(\kappa_1 + \kappa_2)]}\right\}. \tag{2.35}$$

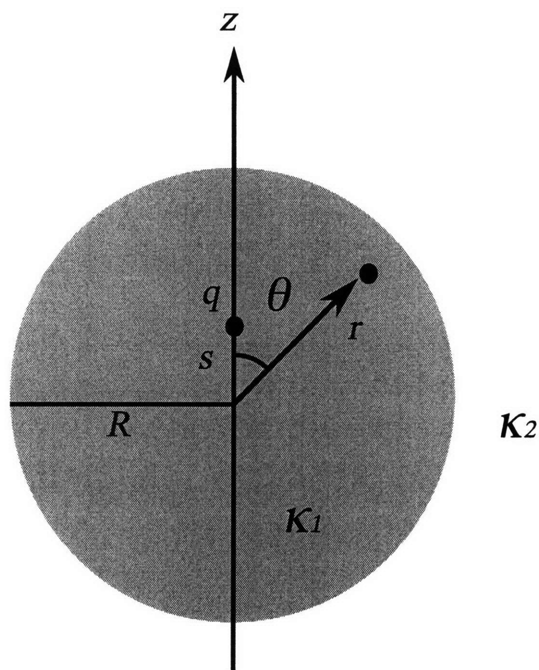


Figure 2-8: Schematic diagram of a charge q in a dielectric quantum dot (κ_1) embedded in a dielectric (κ_2).

$$
\begin{aligned}
\phi_2|_{r\to\infty} &= 0, \\
\phi_1|_{r=R} &= \phi_2|_{r=R}, \\
\kappa_1 \frac{\partial \phi_1}{\partial r}\bigg|_{r=R} &= \kappa_2 \frac{\partial \phi_2}{\partial r}\bigg|_{r=R}.
\end{aligned}
\tag{2.36}
$$

We recognize the first term in Eq. (2.35) as the bulk potential $\phi_b(\vec{r})$, then the self-energy of the charge q in the dielectric dot is

$$
\Sigma(\vec{r}) = \frac{q^2}{8\pi\kappa_1\epsilon_0} \sum_{n=0}^{\infty} \frac{r^{2n}}{R^{2n+1}} \frac{(\kappa_1 - \kappa_2)(n+1)}{[\kappa_2 + n(\kappa_1 + \kappa_2)]}. \tag{2.37}
$$

We can get a simpler expression for the self-energy of the charge q located at the center of the dielectric dot:

$$
\Sigma(0) = \frac{q^2}{8\pi\epsilon_0 R} \frac{\kappa_1 - \kappa_2}{\kappa_1\kappa_2}. \tag{2.38}
$$

Here the self-energy of a semiconducting dot is shown to increase with decreasing R.

In this section, we examined several different dielectric interfaces, a single planar interface, a double planar interface, and a spherical interface, and showed that the self-energy in these systems is size dependent. This theoretical study provides the basis for using a dielectric confinement effect in the interpretation of our transport data that were obtained for GaN nanowires.

2.4 Solid State Physics of GaN

2.4.1 Crystal Structure

GaN can grow in either the wurtzite or zincblende crystal structures. However, the thermodynamically stable structure for GaN is wurtzite and both HVPE and CVD methods in this work produced GaN nanowires in the wurtzite crystal structure only. Therefore we focus our study on the wurtzite crystal structure here. Both the wurtzite and zincblende structures have Ga-atoms tetrahedrally coordinated by N-atoms and vice versa. The Bravais lattice of the wurtzite structure is hexagonal, and the three

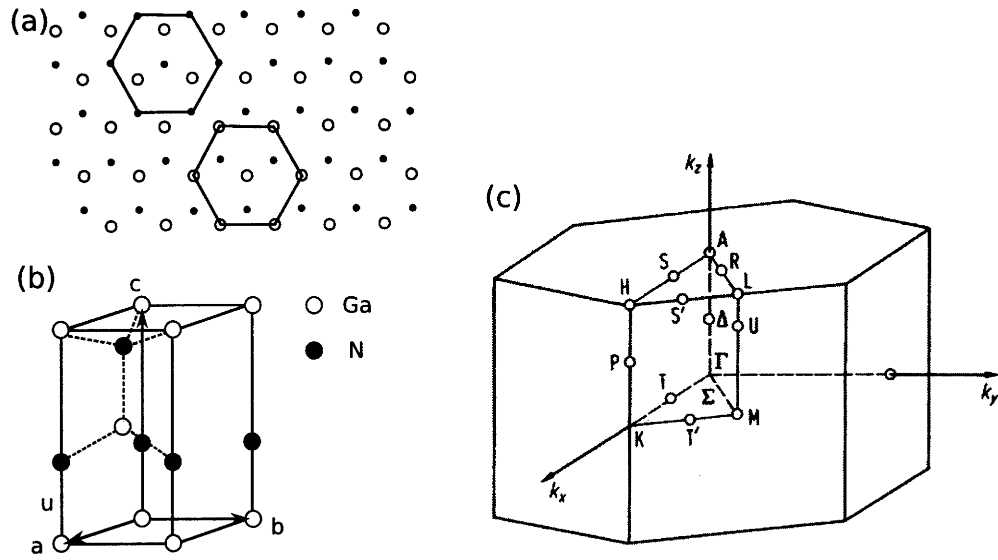


Figure 2-9: (a) A top view of wurtzite GaN (0001) (b) GaN wurtzite structure. (c) Brillouin zone of the hexagonal lattice corresponding to the wurtzite structure.

vectors, $\vec{a}$, $\vec{b}$, and $\vec{c}$, define the lattice as shown in Figure 2-9(a). Both the wurtzite and zincblende structures are built by stacking layers of atoms with the same element along the c-axis. The difference is in the stacking order. For the wurtzite structure the stacking order is:

... Ga(A)N(A)Ga(B)N(B)Ga(A)N(A)Ga(B)N(B)Ga(A)N(A)Ga(B)N(B)...

while for the zincblende the stacking order is:

... Ga(A)N(A)Ga(B)N(B)Ga(C)N(C)Ga(A)N(A)Ga(B)N(B)Ga(C)N(C)...

The wurtzite structure, the more common crystal structure for GaN, has a hexagonal unit cell with 3 atoms of each type (Figure 2-9(a)). The unit vectors $\vec{a}$, and $\vec{b}$ are equal in length, and $\vec{c}$ is perpendicular to the two other vectors. The wurtzite structure consists of two interpenetrating hexagonal close-packed (hcp) sublattices, each with one type of atom, shifted along the c-axis by the distance 3c/8: Ga-atoms are positioned at (0,0,0) and (2/3, 1/3, 1/2), while N-atoms are positioned at (0, 0, u) and (2/3, 1/3, 1/2+u).

Table 2.1: Lattice constants a, c, and unit cell parameter u for GaN at room temperature, and coefficient of thermal expansion for GaN [3].

	length	coefficient of thermal expansion
a	3.189 Å	5.59×10^{-6}/K
c	5.185 Å	3.17×10^{-6}/K
u	0.377	-

2.4.2 Electronic Band Structure

In this section, we focus our discussion mainly on GaN in the wurtzite crystal structure because our GaN nanowires grow only in the wurtzite structure. An accurate determination of the band structure near the fundamental gap is essential for reliable device design calculations. GaN has a direct band gap which enables efficient light emission and lasing. The band structure of wurtzite GaN is similar to that of zincblende GaN. One major difference is that the degeneracy in the valence band is further lifted by the crystal field interaction in addition to the spin-orbit interaction for wurtzite GaN. The valence electrons in a wurtzite lattice experience an extra field from the sites beyond the next nearest neighbors. By including the crystal field interaction and the spin-orbit coupling, the upper valence band is split into three states, $A(\Gamma_9)$, $B(\Gamma_7)$, and $C(\Gamma_7)$. Figure 2-10 shows the calculated band structure near the Γ point of wurtzite GaN. In the quasi-cubic model [44, 45], three valence bands of the wurtzite crystal are thought to be coming from the combined effect of the spin-orbit interaction and the crystal-field interaction. The energy of the split-off valence bands can be expressed in terms of the matrix element of the spin-orbit interaction Δ_{so} and that of the crystal-field interaction Δ_{cr} [44, 45]:

$$\begin{aligned} \Delta E_{AB} &= \frac{\Delta_{so}+\Delta_{cr}}{2} - \sqrt{\left(\frac{\Delta_{so}+\Delta_{cr}}{2}\right) - \frac{2}{3}\Delta_{so}\Delta_{cr}}, \\ \Delta E_{AC} &= \frac{\Delta_{so}+\Delta_{cr}}{2} + \sqrt{\left(\frac{\Delta_{so}+\Delta_{cr}}{2}\right) - \frac{2}{3}\Delta_{so}\Delta_{cr}}. \end{aligned} \tag{2.39}$$

While the conduction band near the Γ point is s-orbital-like and assumed to be

parabolic, the valence band at the Γ point is p-orbital-like and highly anisotropic. We can check the anisotropy of the valence bands in the band diagram (Figure 2-10). The effective hole mass of the Γ_9 band is heavy in all k directions, while that of the upper Γ_7 band is somewhat light in the $k_\perp$ direction but heavy in the $k_\parallel$ direction. The trend is reversed for the lower Γ_7 band: heavy in the $k_\perp$ direction but light in the $k_\parallel$ direction. The anisotropy and the band mixing of the valence bands can complicate the band calculation for wurtzite GaN.

Table 2.2: Comparison of values for the fundamental band gap of wurtzite and zincblende GaN at room temperature reported in the literature [4].

Wurtzite GaN (eV)	Zincblende GaN (eV)	Method	Reference
3.44	3.17	Ellipsometry	[4]
-	3.23	Modulated Photoreflectance	[46]
3.54	3.37	Reflection	[47]
3.45	3.21	Cathodoluminescence	[48]
3.44	3.28	Photoluminescence	[49]
-	3.45	Cathodoluminescence	[50]

The measured fundamental band gap values in the literature for wurtzite GaN depend on the experimental methods used as shown Table 2.2. The published values for the splitting energies of the valence bands at the fundamental gap varies widely as well [51]:

ΔE_{AC}=22 meV [52], 18 meV [53], 28 meV [54], 24 meV [55], 43 meV [56],

ΔE_{AB}=6 meV [52, 53, 54, 55], 8 meV [56].

As seen from the spread of the experimental band data on GaN, a more reliable and consistent method to determine the band structure of GaN is needed.

So far we discussed the electronic band structure for bulk wurtzite GaN, and the question is whether this same band structure applies to GaN nanowires with the same geometric atom positions. The answer, of course, depends on the size of the nanowires. It is well known that the quantum confinement effect creates quantum subbands in nanowires with a diameter of the orders of the Fermi wavelength of carriers because the motion of carriers is restricted in the plane perpendicular to

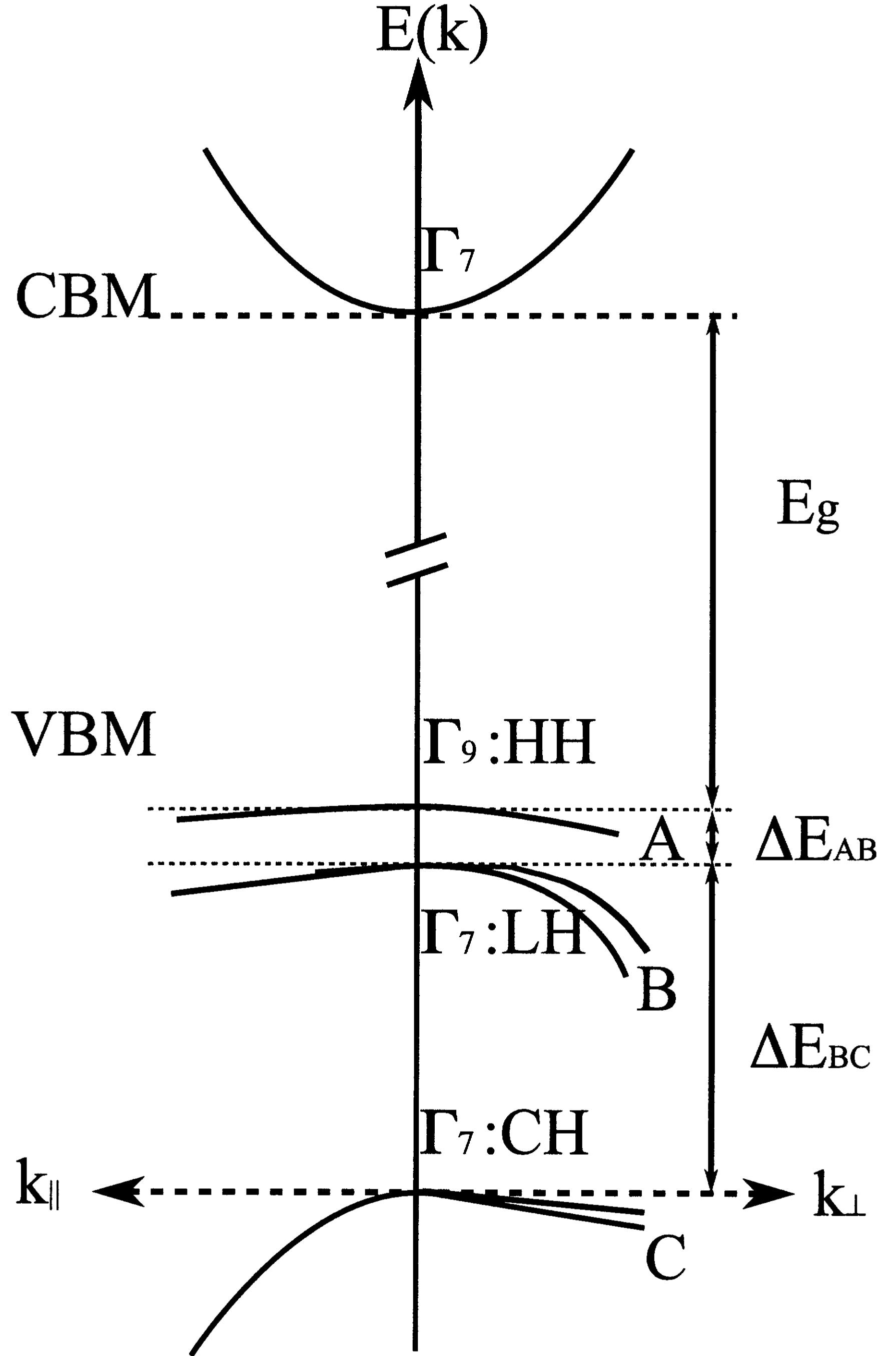


Figure 2-10: Schematic electronic energy band structure near the direct fundamental gap of Wurtzite GaN. The top of the valence band is split by the crystal field and by the spin-orbit interaction into A(Γ_9), B(Γ_7), and C(Γ_7) states. Note: $k_{\|} \parallel k_z$ and $k_{\perp} \perp k_z$. HH=heavy hole band, LH=light hole band, and CH=crystal field split-off band.

the wire axis. Another important modification of the electronic structure due to the quantum confinement effect is the enhancement of the impurity binding energy as the diameter of a nanowire becomes on the order of the effective Bohr radius [57, 58]. The effective Bohr radius is estimated to be

$$r_B = \kappa_{nw}(\frac{m_0}{m_e})a_0, \tag{2.40}$$

where κ_{nw} is the dielectric constant for the nanowire, m_0 is the electron mass, m_e is the effective mass of electrons in the nanowire, and a_0 is the Bohr radius of an electron (0.53 Å). The effective Bohr radius for our GaN nanowire is about 2 nm and we can safely assume that the quantum confinement effect does not have a significant effect in our nanowires which typically have diameters larger than 10 nm. However, even above the quantum size regime, the size effect can show up when there is a significant dielectric mismatch between the nanowire and its surrounding medium [59]. This so-called dielectric confinement effect can enhance the ionization energy of impurities in a semiconducting nanowire and play a major role in their transport properties [60].

The discussion here is taken from Diarra *et al* [60]. The Hamiltonian for semiconducting nanostructures is given as

$$H = H_0 + U_i + \Sigma, \tag{2.41}$$

where H_0 is the Hamiltonian of the nanowire with surface passivation. The term U_i is the potential at a location $\mathbf{r}$ due to the impurity nucleus located at $\mathbf{r_0}$ and given as $U_i = \pm V(\mathbf{r}, \mathbf{r_0})$. The (+) and (−) signs are for an acceptor and a donor, respectively. The potential V is calculated by solving the Poisson equation for a cylinder of radius R and of relative dielectric constant κ_{nw} embedded in a medium of relative dielectric constant κ_i. Screening of a coulomb potential in a nanowire (1D) is much weaker than that in a bulk semiconductor because of the surface effect in the nanowire and this leads to the enhancement of the impurity binding energy in nanowires. The screened potential by a charge e at $\mathbf{r_0}$ in a bulk semiconductor is $V_b(\mathbf{r}, \mathbf{r_0}) = e^2/\left[\kappa_{nw}\epsilon_0|\mathbf{r} - \mathbf{r_0}|\right]$ as the rest of the total charge e, $e(1 - 1/\kappa_{nw})$, is repelled at infinity. However, in a

semiconducting nanowire, the screened out charge $e(1-1/\kappa_{nw})$ is relocated at the surface of the nanowire, which is close enough to the impurity and leads to an extra term V_s in the potential, $V = V_b + V_s$. In other words, the term V_s is due to the surface polarization charge $e(1-1/\kappa_{nw})$ induced by the impurity nucleus.

The last term Σ in the Hamiltonian (Eq. 2.41) is the self-energy potential which is due to the surface polarization charges of the charge carriers. As discussed in section 2.3, $\Sigma(\mathbf{r}) = \pm\frac{1}{2}V_s(\mathbf{r},\mathbf{r})$, where the (+) and (−) signs are for an electron and a hole, respectively. The factor $\frac{1}{2}$ comes from the adiabatic build-up of the charge distribution [59]. However, this self-energy correction for a free carrier at $\mathbf{r}$ is almost the same as that for a bound electron at $\mathbf{r_0}$ because $V_s(\mathbf{r},\mathbf{r_0})$ is slowly varying in the limit of thick nanowires with an effective Bohr radius r_B much smaller than the nanowire radius R. Their contributions to the ionization energy of the impurity cancel each other. Therefore the net effect of the surface of the nanowire on the ionization energy of the impurity is mainly due to the interaction between the carrier and the surface polarization charge $e(1-1/\kappa_{nw})$ induced by the impurity nucleus (V_s in U_i). Thus the increase in the ionization energy is

$$\Delta E_I \approx \langle V_s \rangle = 2\langle\Sigma\rangle(R), \tag{2.42}$$

where $\langle\Sigma\rangle(R)$ is given in Eq. (2.45).

The self-energy correction inside the nanowire with radius R is calculated from the electrostatic analysis of a nanowire, with relative dielectric constant κ_{nw}, embedded in an insulator with κ_i. The result from Reference [59] is

$$\Sigma(r) = \left[1 - \frac{\kappa_i}{\kappa_{nw}}\right] \sum_{n\geq 0} \int_{-\infty}^{+\infty} \frac{dk}{2\pi}(2-\delta_{n,0}) \frac{K_n(|k|R)K_n'(|k|R)I_n^2(|k|r)}{D_n(\kappa_{nw},\kappa_i,|k|R)}, \tag{2.43}$$

where $D_n(\kappa_{nw},\kappa_i,|k|R) = \kappa_i\epsilon_0 K_n'(|k|R)I_n(|k|R) - \kappa_{nw}\epsilon_0 K_n(|k|R)I_n'(|k|R)$, and $I_n(x)$ and $K_n(x)$ are the modified Bessel functions of the first and second kind, respectively. We now calculate the self-energy correction for the free carriers assuming an infinite well boundary condition at $r = R$ and the single band, isotropic effective mass

approximation. The envelope function used is [59]

$$\varphi(r) = \frac{1}{\sqrt{2\pi K}R} J_0\left(\alpha_0 \frac{r}{R}\right), \tag{2.44}$$

where $J_0(x)$ is the zeroth-order Bessel function of the first kind, $\alpha_0 = 0.2404$, and $K = 0.1347$. The constants α_0 and K are given by $J_0(\alpha_0) = 0$ and $K = \int_0^1 x J_0^2(\alpha_0 x) dx$. Then,

$$\begin{aligned} \langle \Sigma \rangle (R) = \langle \varphi | \Sigma | \varphi \rangle &= \frac{1}{KR^2} \int_0^R r \Sigma(r) J_0^2 \left(\alpha_0 \frac{r}{R}\right) dr \\ &= \frac{1}{\kappa_{nw} R} \frac{\kappa_{nw} - \kappa_i}{\kappa_{nw} + \kappa_i} F\left(\frac{\kappa_{nw}}{\kappa_i}\right), \end{aligned} \tag{2.45}$$

where

$$F(t) = \frac{t+1}{\pi K} \sum_{n \geq 0} \int_0^\infty dy \int_0^1 dx (2 - \delta_{n,0}) \frac{x K_n(y) K_n'(y) I_n^2(xy) J_0^2(\alpha_0 x)}{K_n'(y) I_n(y) - t K_n(y) I_n'(xy)}. \tag{2.46}$$

The function $F(t)$ has been numerically calculated by Niquet *et al.* for $10^{-2} < t < 10^2$ and $0 < y < 512$ using 128 Bessel functions [59]. For practical applications, the function $F(t)$ is fitted with the Padé approximant [59]:

$$F(t) \approx \frac{0.0949t^3 + 17.395t^2 + 175.739t + 200.674}{t^2 + 50.841t + 219.091} \quad [\text{eV}\cdot\text{nm}]. \tag{2.47}$$

As we can see from the result in Equations (2.42) and (2.45) , the dielectric confinement effect disyplays the inverse R dependence. The prefactor γ in $\Delta E_I = \gamma / R$ is plotted in Figure 2-11 for GaN nanowire (κ_{nw}=8.9). This result shows that the prefactor γ will decrease with the decreasing dielectric mismatch between the nanowire and its surrounding dielectric and this behavior has been observed in our measurements described in chapter 5.

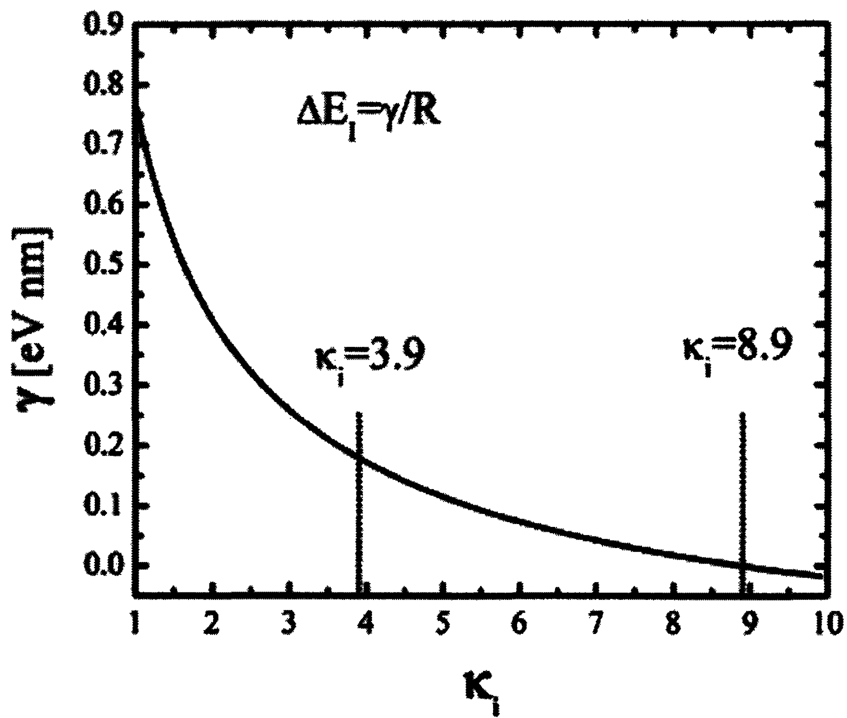


Figure 2-11: The prefactor γ for GaN nanowire as a function of the dielectric constant for the surrounding insulator κ_i. The vertical dotted lines indicate the dielectric constants of bulk SiO_2 (κ_i=3.9) and GaN (κ_i=8.9).

Chapter 3

Experimental Methods

In this chapter, we illustrate experimental methods used to synthesize GaN nanowires and the fabrication technique used to make electrical contacts to the nanowires. Section 3.1 describes the synthesis mechanism of semiconductor nanowires and their characterization. Subsections 3.1.1 and 3.1.2 deal with hydride vapor phase epitaxy (HVPE) and chemical vapor deposition (CVD), respectively. Once the nanowires are grown, a nanowire based FET (Field Effect Transistor) is fabricated as given in section 3.2.

3.1 Catalytic synthesis of GaN Nanowires

Single-crystalline, one-dimensional semiconductor technology has been drawing a lot of interest and effort for its potential to replace the current technology based on thin film semiconductors, such as FETs, optoelectronics, and sensors. The background on the vapor-liquid-solid growth mechanism is given in the section 2.1. In this section we describe the HVPE and CVD synthesis methods used to synthesize GaN nanowires in this work.

3.1.1 GaN Nanowires grown by Hydride Vapor Phase Epitaxy

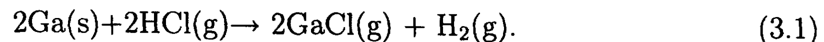
Synthesis

In this section we describe how we synthesize GaN nanowires using Hydride Vapor Phase Epitaxy (HVPE) [2]. Synthesis of gallium nitride nanowires is performed in an in-house built HVPE system (Figure 3-1(a)). The system consists of a high temperature furnace, a horizontal reactor, a gas panel, a control system, and a scrubber. Figure 3-1(b) shows the schematic diagram for the horizontal reactor.

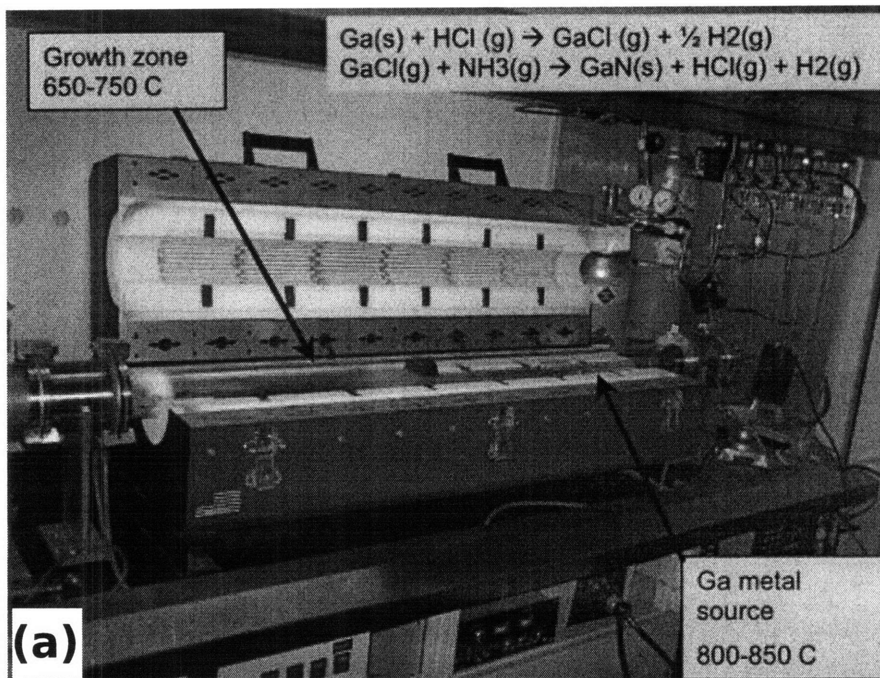
The reactor has a 75 mm round quartz tube, installed inside a three-zone Mellen horizontal furnace. The actual reaction takes place inside a rectangular quartz tube, which promotes laminar flow and thus suppresses turbulence in the growth zone. All process gases, GaCl, HCl, NH_3, and N_2, are delivered into the rectangular tube by two of the 10 mm quartz tubes.

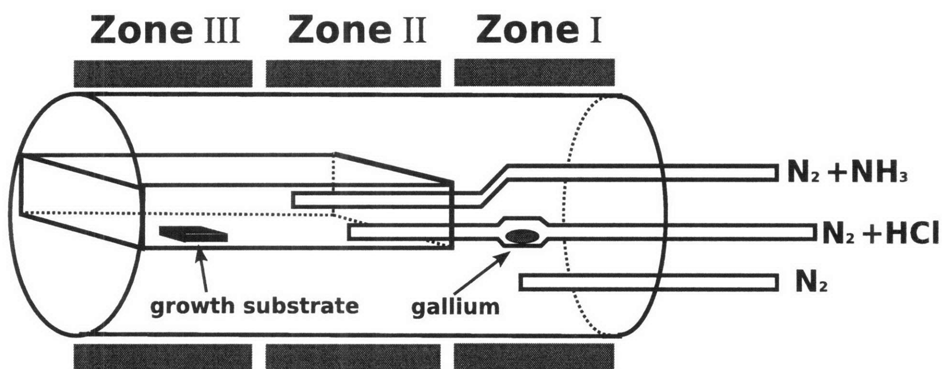
As a growth substrate, silicon (111) and c-plane sapphire substrates are used. We tried gold and nickel as a catalyst for VLS growth. Even though gold is commonly used as a catalyst for growth of silicon and germanium nanowires, it wasn't suitable for the growth of gallium nitride nanowires because of the low solubility of nitrogen in gold [61]. Therefore nickel is used as a catalyst for the growth of GaN nanowires. Typically a 5 nm thick nickel thin film was thermally evaporated on the growth substrate or a drop of nickel nitrate ($Ni(NO_3)_2$) solution, prepared by dissolving 0.1 M $Ni(NO_3)_2 \cdot 6H_2O$ in isopropyl alcohol, was applied to the substrate and air-dried. At the high growth temperature for the nanowire (given below), $Ni(NO_3)_2 \cdot 6H_2O$ most likely decomposes to form NiO [62], which acts as a catalyst for the nanowire growth.

For a gallium source, gallium metal is placed in the wide part of the quartz tube in zone I (Figure 3-1(b)). GaCl gas is formed from the reaction between molten gallium metal and HCl gas in the 10 mm tube in zone I at 800-850°C and carried by N_2 gas into the rectangular tube. The reaction in zone I is as follows:



$$2Ga(s) + 2HCl(g) \rightarrow 2GaCl(g) + H_2(g). \quad (3.1)$$





(b)

Figure 3-1: (a) Picture of our HVPE system. (b) Schematic diagram of the horizontal HVPE reactor.

The growth zone (zone III) is maintained at 650-750°C for the duration of the nanowire synthesis. During the synthesis, ammonia (NH_3) gas, which is pushed into the growth zone by nitrogen (N_2) gas, reacts with GaCl gas to form the final product, GaN nanowires, on the growth substrate. The reaction is described by the following equation:

$$GaCl(g)+NH_3(g) \rightarrow GaN(s) + HCl(g) + H_2(g). \quad (3.2)$$

Ultrahigh purity nitrogen gas (99.999 %) is used as the carrier gas with a flow rate of 3000 sccm (standard cubic centimeter per minute). The HCl and NH_3 gas flow rates are 1-10 and 50-200 sccm, respectively. The typical growth run lasts for around 5 minutes and GaN nanowires longer than 10 μm are thus synthesized. Figure 3-2 (inset) shows the SEM image of GaN nanowires synthesized by the HVPE method. A Lab Guard wet scrubbing system is used to neutralize the acidic exhaust gas and trap the resulting ammonium chloride (NH_4Cl) powder.

XRD Study of HVPE GaN Nanowires

Control over the nanowire growth direction is desired as many materials properties, such as the thermal and electrical conductivity, index of refraction, piezoelectric polarization, and band gap, are anisotropic. The appropriate selection of the lattice matched substrate is used to control the growth direction [63]. We used a c-plane sapphire substrate to grow GaN nanowires epitaxially. The epitaxial growth is confirmed by the x-ray diffraction peaks from the (0002) and (0004) planes of the hexagonal GaN as shown in Figure 3-2.

TEM Characterization of HVPE GaN Nanowires

Our HVPE grown GaN nanowires display a tapering shape, thick at the base and thinner at the tip. The wire diameter ranges between 40 and 400 nm with the mean value of 198.5 nm (Figure 3-3). Nanowires grown by the VLS mechanism typically end up with a metal catalyst particle at the tip of the nanowire. GaN nanowires

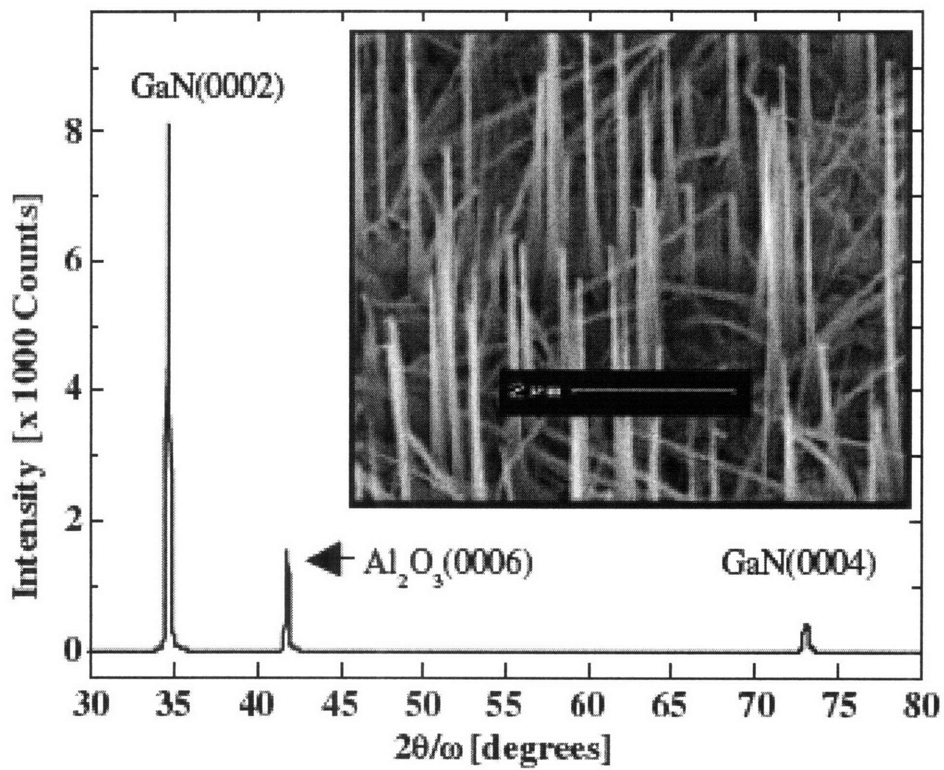


Figure 3-2: X-ray diffraction pattern from HVPE nanowires grown on sapphire substrate (directly taken from Reference [2]). The inset shows the SEM image of the nanowires. (Scale bar: 2μm)

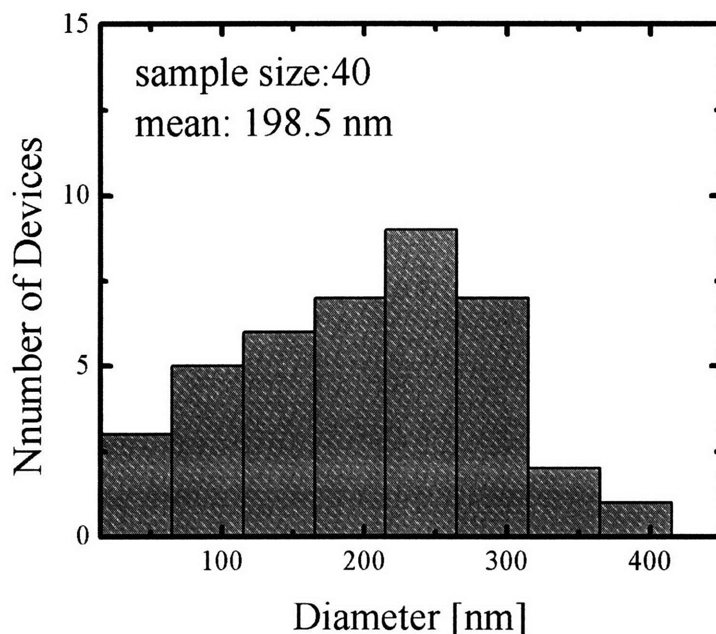


Figure 3-3: Histogram of the diameters for GaN Nanowires from HVPE.

have been grown using various metal catalysts, such as Ni, Fe, Au, AuPd, In, and Ga [63, 64, 65, 66, 67]. Among these different catalysts used, only Au and AuPd were reported on the tip of the nanowires [63, 65]. SEM images indicated that our GaN nanowires grew only where catalyst nanoparticles were deposited. However, we rarely observed Ni nano particles on the tip of the nanowires. We speculate that Ni might have been etched away due to the HCl gas present in the HVPE reactor. Another scenario is that Ni atoms dope the nanowire during the growth and the Ni catalyst gets consumed in this way. These two scenarios might explain the tapering nanowire growth. The size defining catalyst becomes smaller during the growth and thus nanowires grow with a tapering shape.

In order to examine the crystal quality and the chemical makeup of the nanowires, TEM (Transmission Electron Microscopy) and EDX (Energy dispersive X-ray spectroscopy) were performed. Basically, we wanted to check the core and surface of our nanowires for any visible defects, impurities, and oxides. A microtome procedure

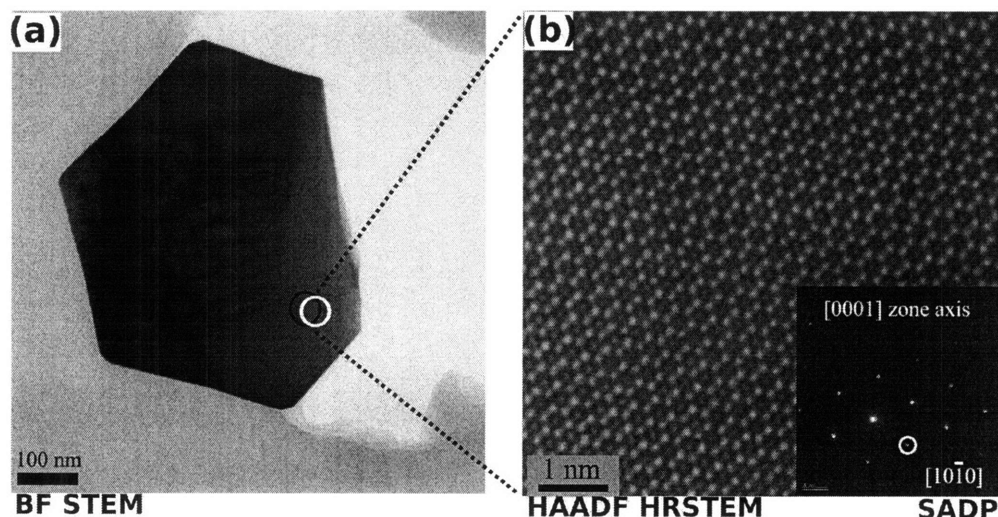


Figure 3-4: (a) Low resolution BF (bright field) STEM image shows hexagonal facets of the nanowire; the right side of the sample is chipped off during a microtome procedure. (b) High angle annular DF (dark field) HR STEM shows a hexagonal lattice. Inset shows a selected area diffraction pattern (SADP) indicating the (0001) crystal growth direction

was performed on thick HVPE GaN nanowires to examine the core and shell of the nanowires. The nanowires were embedded in epoxy resin and 80nm thick slices were shaved off from the composite. In Figure 3-4 a low resolution image (a) shows a hexagonal facet of the nanowire; a part of right edge was chipped off most likely during a microtome procedure. The nanowires exhibit the wurtzite single crystal structure and a (0001) growth orientation as demonstrated in the selected area diffraction pattern (inset of Figure 3-4(b)). A high angle annular dark field (HAADF) high resolution (HR) scanning transmission electron microscope (STEM) image reveals atom sites as the light spots (Figure 3-4(b)).

A high resolution TEM image in Figure 3-5 shows a 1 - 2 nm amorphous layer at the boundary of the HVPE GaN nanowire. It has been reported that bulk GaN terminates with a monolayer thick native oxide [68] but our GaN nanowires seem to

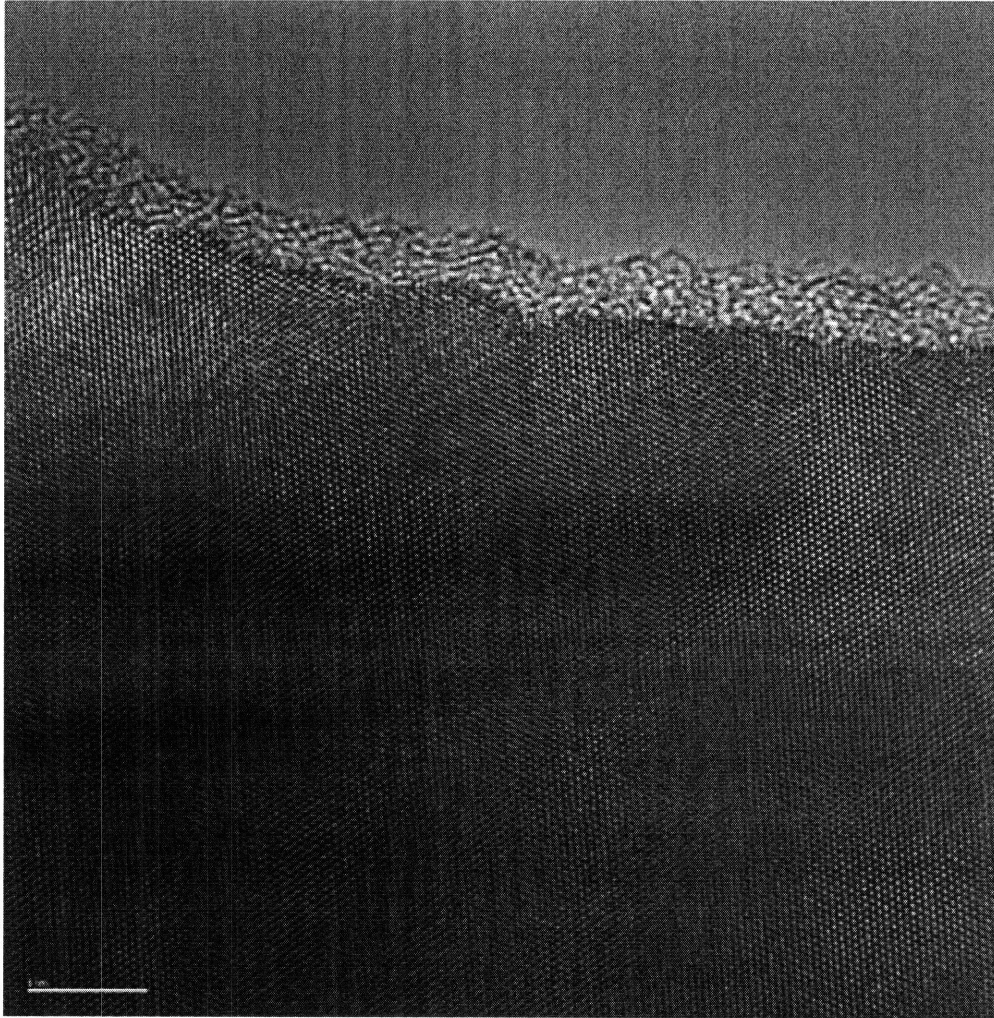


Figure 3-5: High Resolution TEM image of a microtomed HVPE GaN nanowire with scale bar of 5 nm (courtesy of JEOL).

terminate with several layers of oxide.

Energy-dispersive x-ray (EDX) spectroscopy was employed to look for any foreign material in our GaN nanowire growth (Figure 3-6). A clear peak for Ga is shown and kind of weak signal for N, which is typical since N is a light element. The Cu peak is from the TEM grid. Within the detection limit of EDX (0.5 at. %), Ni was not detected. The EDX spectrum also shows rather strong Si and O peaks but we concluded that these peaks are from the epoxy which the microtomed nanowire discs are embedded in and not from the GaN nanowire because EDX linescan in the inset of Figure 3-6 does not show any traces of Si or O.

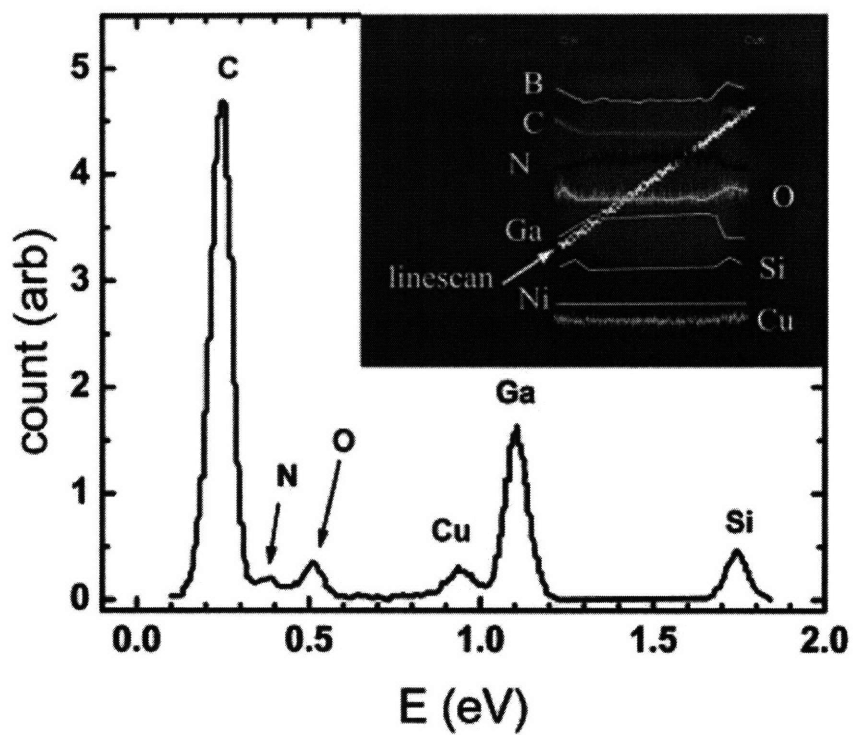


Figure 3-6: EDX spectrum of a microtomed HVPE GaN Nanowire. The inset shows the EDX linescan in the STEM mode with a spot size of 1 nm. Guiding white lines are drawn over the colored lines for clarity. (color)

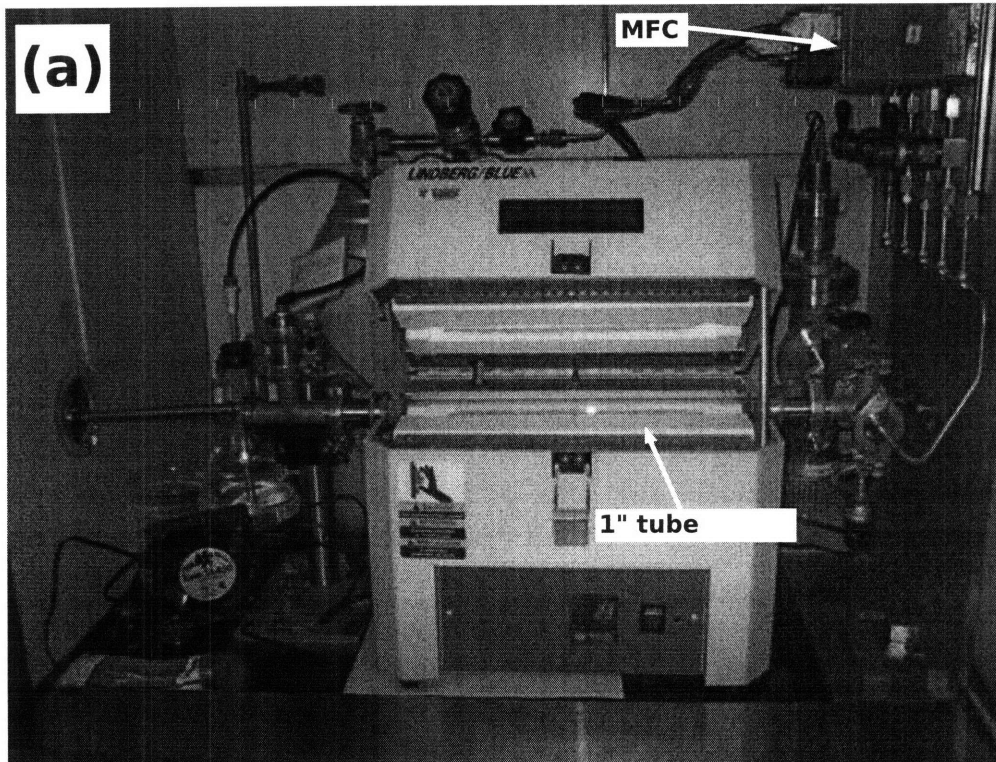
We have shown that our HVPE GaN nanowires grow by the VLS mechanism as a single crystal relatively defect free, and the diameter of the nanowire can be controlled by the size of the catalyst nanoparticles, and the growth orientation can be controlled through the epitaxial growth. However, the question remains as to the whereabouts of the Ni catalyst particles after the growth and the origin of the high doping level observed in the FET measurements (section 4.3).

3.1.2 GaN Nanowires by Chemical Vapor Deposition

Synthesis

In this section we describe the synthesis of GaN nanowires using the chemical vapor deposition (CVD) method. The CVD synthesis is carried out in a 1" tube furnace, Lindberg/Blue Tube furnace TF 55035A-1 (Figure 3-7(a)). The CVD system consists of a 1" quartz tube placed in a hot-zone horizontal furnace, a mass flow controller (MFC), and a turbopump.

For a gallium source, about 2 gm of high purity metal Ga (purity 99.999 %) is placed in a graphite crucible. The silicon substrate, around 1 cm $\times$ 1cm, is used as a growth substrate, which is cleaned with a typical acetone/isopropyl alcohol rinsing step. We deposit a drop of nickel nitrate hexahydrate ($Ni(NO_3)_2 \cdot 6H_2O$) solution, prepared by dissolving 0.1 M $Ni(NO_3)_2 \cdot 6H_2O$ in isopropyl alcohol, on the substrate and we let the substrate air-dry. Nickel oxide from the decompostion of $Ni(NO_3)_2 \cdot 6H_2O$ acts as a catalyst [62]. The growth substrate is placed downstream of the gas flow, about 1cm away from the gallium source. Prior to the growth, the quartz tube is pumped down to 2×10^{-5} Torr and filled with ultrahigh purity argon (Ar) gas (purity 99.999 %). The furnace is heated to the desired temperature of 900°C. Both the Ga source and the substrate are pushed by a manipulator from the end of the quartz tube into the hot zone, preheated to 900°C, and the Ga source and the silicon substrate are maintained there for an hour with a 60:1 mixture of $Ar:NH_3$ at a flow rate of 30 sccm. The chemical reaction between Ga gas and ammonia gas can be expressed as in Equation (3.3).



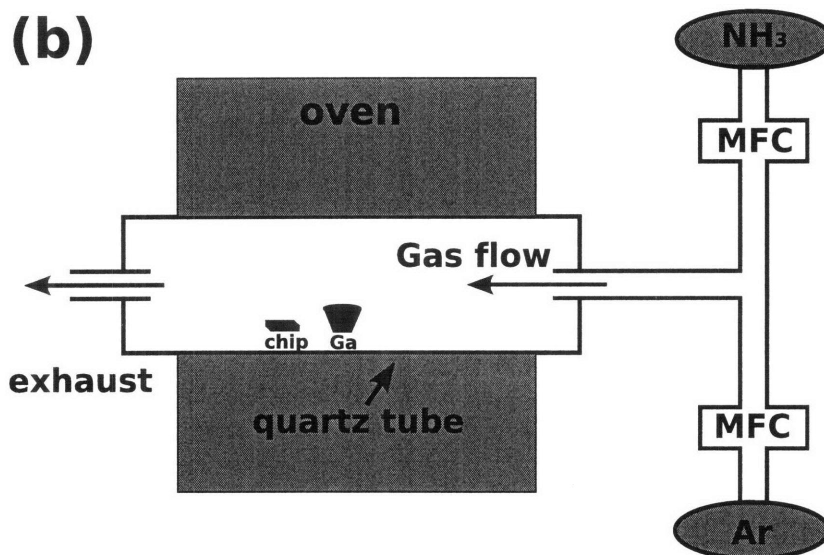


Figure 3-7: (a) Picture of our CVD system. (b) Schematic diagram of the horizontal CVD reactor: the 1 cm x 1 cm silicon chip is inside a 1" quartz tube, metal gallium is in a graphite crucible, and mass flow controller (MFC) controls the gas flow.

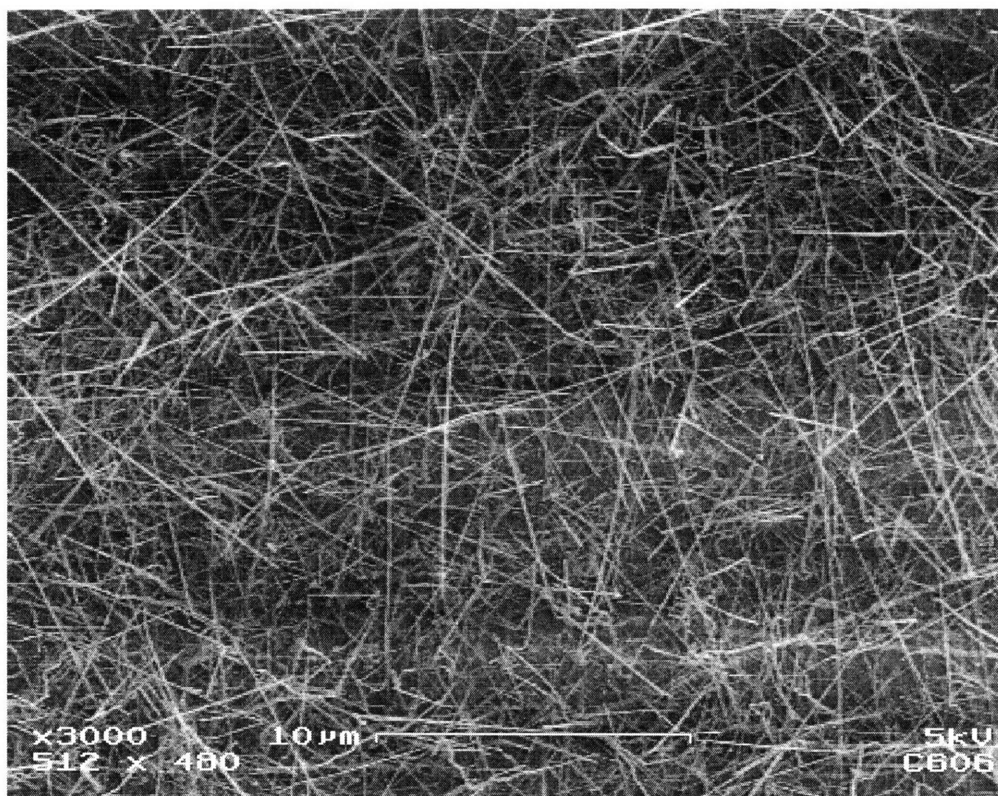
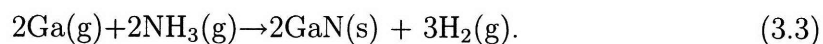


Figure 3-8: SEM image of CVD synthesized GaN nanowires.



$$2Ga(g) + 2NH_3(g) \rightarrow 2GaN(s) + 3H_2(g). \tag{3.3}$$

The ammonia flow is usually kept on until the furnace is cooled down to room temperature to avoid the possible formation of a nitrogen vacancy defect, which is known to be the cause of the unintentional high doping level in GaN. A successful synthesis run yields a layer of light yellow wool-like products on the growth substrate, which can be observed under an optical microscope.

Characterization of the GaN Nanowire Growth

Figure 3-8 shows a successful synthesis imaged with SEM. Non-epitaxial growth of GaN nanowires from a silicon substrate is observed, contrasting the epitaxial growth of HVPE growth method (inset of Figure 3-2).

The diameter of CVD grown nanowires ranges between 10 and 110 nm with the

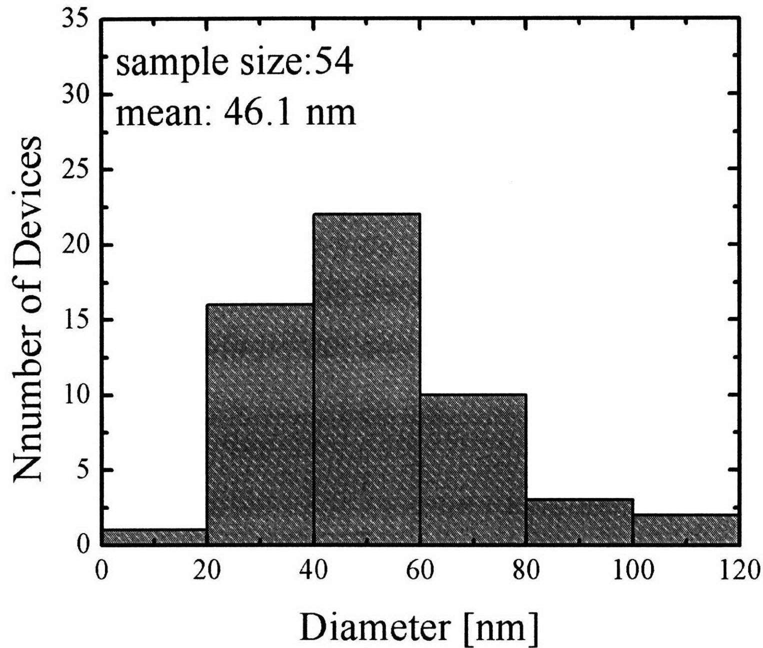


Figure 3-9: Histogram of the diameter distribution for GaN Nanowires grown by CVD.

mean value of 46 nm (Figure 3-9). A pronounced tapering growth observed in the HVPE is also missing from the nanowires produced by CVD growth (Figure 3-10(a)). The nanowires grown by the CVD method were much thinner than by the HVPE growth. The HVPE growth conditions might have included the VS (Vapor-Solid) growth, which tends to allow lateral growth, besides the VLS (Vapor-Liquid-Solid) growth mechanism. A comparison between the two growth methods is given in Table 3.1.

Table 3.1: Growth Data for HVPE and CVD.

	HVPE	CVD
Growth Orientation	(0001)	$(10\bar{1}0)$
Mean Diameter (nm)	199	46

We didn't notice any nickel catalyst at the tip of the nanowires from all the TEM

images taken for the CVD grown nanowires. Since the CVD synthesis doesn't involve any acid such as HCl which is present in the HVPE synthesis, nickel might be actually doping our GaN grown nanowires. energy-dispersive x-ray (EDX) spectroscopy was employed to look for traces on nickel in the CVD grown GaN nanowires, but nickel was not detected within the detection limit of EDX (0.5 at. %). Alternatively, a chemical analysis method, such SIMS (secondary ion mass spectroscopy) [69] or LEAP (local electrode atom probe) [70], can be used to identify the impurities in the nanowires. Figure 3-10 shows TEM images taken for the CVD grown nanowires. The nanowires are straight without a tapering shape, as shown in Figure 3-10(a). The dark fringes observed along the length of the nanowire indicate a thickness variation or strain. The preferred growth direction for the CVD GaN nanowires turns out to be $\langle 10\bar{1}0 \rangle$ when the nanowires are grown non-epitaxially (Figure 3-10(c)). The high resolution TEM image in Figure 3-10(b) shows a defect free single crystal growth with a 1-2 nm amorphous layer on the surface.

In summary, CVD grown nanowires are quite different from HVPE grown nanowires in terms of size, and shape. Asides from a missing tapering shape, the CVD nanowires also do not seem to have hexagonal facets.

3.1.3 Photoluminescence Measurement on GaN nanowires

As-grown CVD and HVPE GaN nanowires are optically excited at room temperature by a HeCd laser (325nm, 8mW). The luminescence signal is monochromatized, filtered, and detected by a Si charge coupled device camera. The resulting PL spectra is shown in Figure 3-11. Both of the CVD and the HVPE grown GaN nanowires display a redshift of the near-band edge emission, which indicates the presence of a bandgap renormalization due to a high concentration of carriers in our GaN nanowires. The redshift values, calculated assuming a bandgap of 3.4 eV for bulk wurtzite GaN, are 150 meV and 100 meV, respectively, for the CVD and the HVPE grown GaN nanowires. This difference is probably due to a different concentration of impurities in GaN nanowires prepared by the two different growth methods rather than the different diameter of the nanowires. Otherwise, a blueshift is expected to occur rather

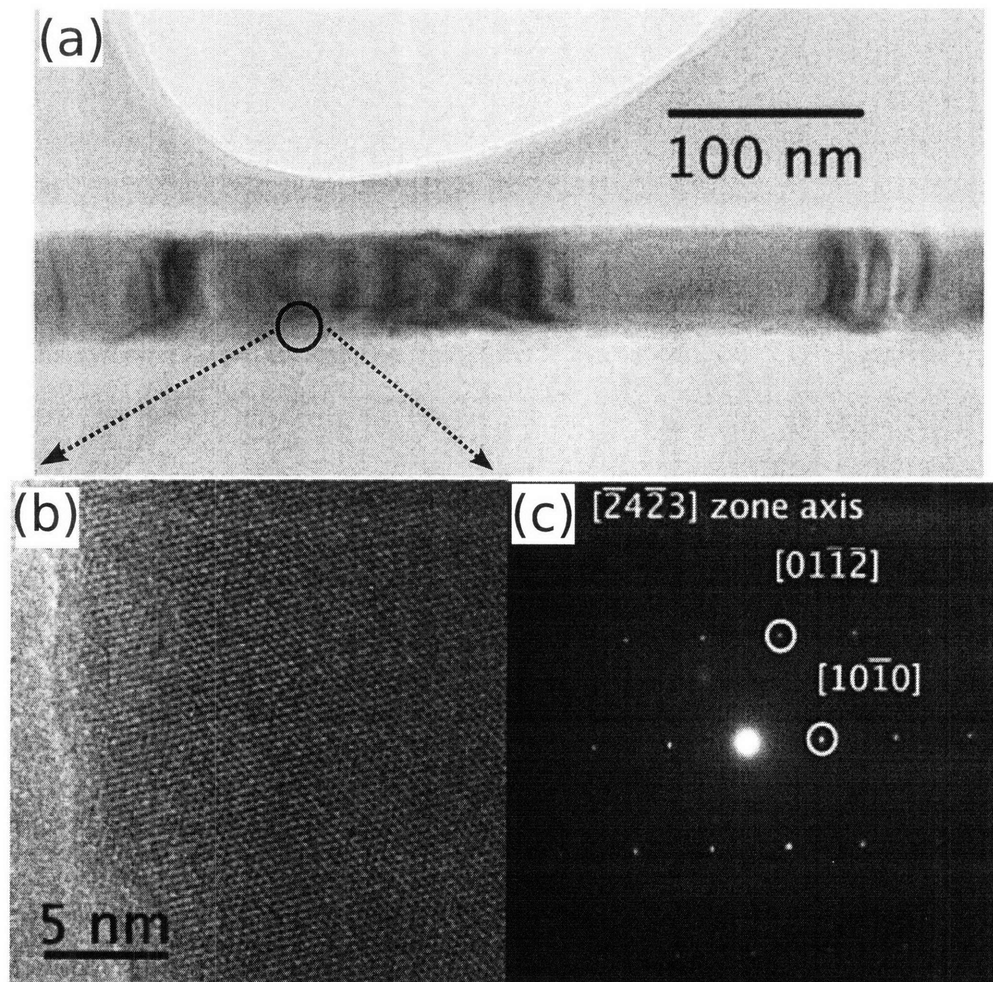


Figure 3-10: TEM study of a CVD grown GaN nanowire:(a) low resolution BF (bright field) TEM image of a GaN nanowire exhibits dark fringes possibly due to thickness variation or strain, (b) high resolution BF TEM image shows a defect-free lattice, and (c) a selected area diffraction pattern indicates a $(10\bar{1}0)$ crystal growth direction.

than a redshift as the diameter of the nanowire decreases. The CVD grown GaN nanowires might have a few times higher impurity concentration than the HVPE counterpart.

We also notice an extra broad sub-bandgap luminescence peak in the PL spectrum for the CVD grown GaN nanowires. The PL spectrum for the HVPE GaN nanowires shows only a small hillock in the sub-bandgap region and the location of this hillock seems to be somewhat different from the CVD case. This broad sub-bandgap peak is known to be due to the deep-defect levels in GaN, and furthermore, these deep-defect levels tend to segregate to the surface layer of nanowires because the surface of a nanowire is the energetically favorable location for these defects. Therefore, the ratio between sub-bandgap and band edge luminescence peak intensities increases as the diameter of the nanowires decreases from $\sim$ 150 nm (HVPE nanowire) to $\sim$ 50 nm (CVD nanowire), similar to the observation made on ZnO nanowires [71]. This result suggests that defects and impurities tend to segregate to the surface of GaN nanowires.

3.2 Fabrication of Nanowire Devices

Both HVPE and CVD nanowires were used to fabricate the devices. For fabricating metal electrodes on GaN nanowires, we use both electron-beam lithography and photolithography. The basic strategy is to use "blind" photolithography to test samples quickly not worrying too much about whether or not a single wire is contacted and to use electron-beam lithography once all the plans are laid out.

3.2.1 Substrates

A substrate is an integral part of a nanoscale device. For example, the morphology of the surface of the substrate can affect the properties of the thin metal film, since the electrical properties of nanoscale devices are strongly affected by the substrate on which they are lying [72]. The substrate provides not only a mechanically supporting structure, but also a dielectric environment, which is known to change the electronic

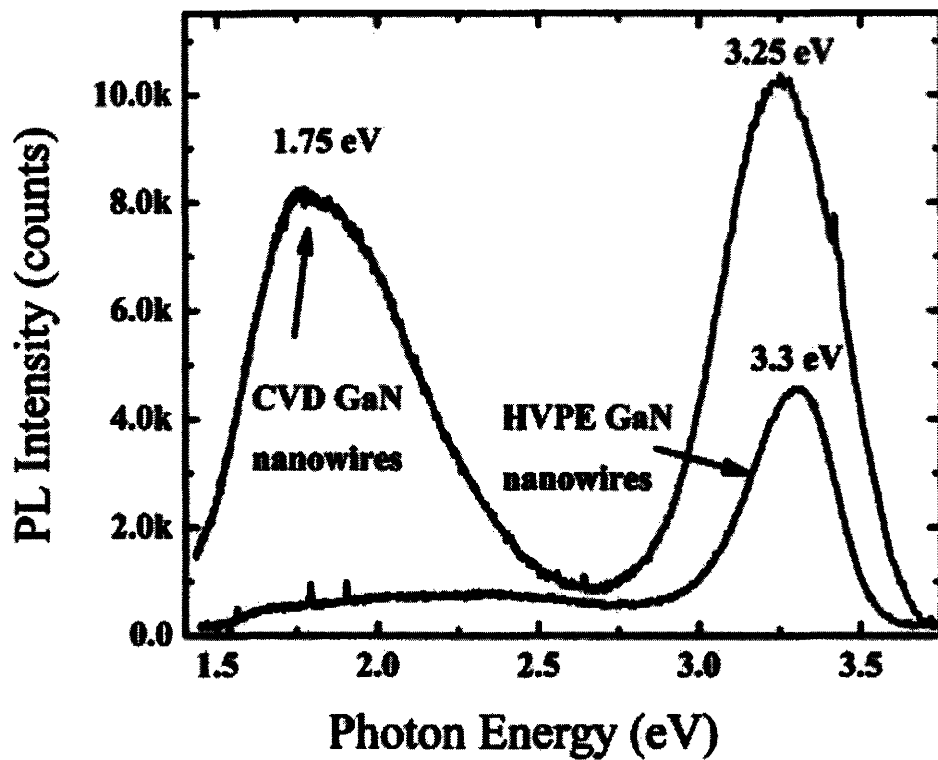


Figure 3-11: Photoluminescence spectra obtained from HVPE and CVD grown GaN nanowires at room temperature. The HVPE and CVD nanowires have diameters of $\sim$ 150 nm and $\sim$ 50 nm, respectively.

properties for nanoscale devices significantly [59, 60].

We used silicon wafers as device substrates because of their availability. Heavily doped p-type Si wafers were used as a backgate for nanowire field effect transistors (NWFET). The silicon wafers were purchased with a thin layer of insulator, which acts a gate dielectric, already grown on top of the silicon wafer. We used 300 nm SiO_2 on Si wafers for typical FET devices. We also used 50 nm Si_3N_4 to increase the gate coupling to the nanowires. The relative dielectric constant for SiO_2 is 4.5 and that for Si_3N_4 is 7.5. However, given that our GaN nanowires are heavily doped, 50 nm Si_3N_4 was too thin to withstand the high gate bias required to deplete charge carriers from our nanowires. Therefore SiO_2 is the preferred dielectric thin film for our devices. Also the SiO_2 layer can be easily removed by the HF acid, which is convenient for further fabrication, such as for etching trenches.

A wet etching step is often used as a part of the fabrication processes. Hydrofluoric (HF) acid burns to the human skin are particularly hazardous. A dangerous aspect of HF burns is that it does not produce any burning sensation until it has already done irreversible damage. An extreme precaution needs to be practiced when using HF acid, since an exposure to HF can results in massive tissue damage. When exposed to HF, the affected area should be thoroughly washed off with plenty of cold water including under the nails for the minimum of 15 minutes. After flushing with water, calcium gluconate gel can be liberally applied to the affected area and kept on until medical help arrives.

3.2.2 Substrate Preparation

The cleanness of the substrate is important for electrical device fabrications because the electrical properties of the deposited thin metal film is strongly affected by any debris on the substrate and nanowires. When silicon wafers are first purchased, they arrive in a clean condition. It is important to keep these wafers free from dust particles. We found that the best way to do this is to keep these brand new wafers inside the nitrogen dry box in a cleanroom after spin coating them with a photoresist such as Microposit S1805. In this way, wafers will stay clean for future fabrication

steps.

The first step of the device fabrication is cutting down a 3 inch wafer into small squares that are 5 mm wide. This step is called cleaving. A whole wafer can be cleaved with a cleaver machine, which is a convenient way to cut a large wafer into chips of a fixed size. For this step we used a Loomis LSD-100 Scriber/Cleaver. The LSD-100 can scribe Si, glass, and sapphire wafers up to 4 inches in diameter. The scriber is computer controlled using a real-time imaging and pattern recognition option for precise scribing. For casual cleaving, a diamond scriber is used to scribe a notch on the surface of a wafer and the wafer is placed on a slightly elevated surface. We used a glass slide for this surface. The wafer is aligned so that the notch is at the edge of the glass slide. Then pressure is applied on either side of the notch with tweezers with a soft tip until the chip snaps off. During this process, care is taken not to scratch the surface of the chip in the region where the device will be fabricated. The cleaving will generate silicon fragments and dust. However, since wafers are already coated with the photoresist, subsequent contamination will only affect the surface of the photoresist layer, which can be readily removed with acetone. Once the protective photoresist is off, small chips should be stored with care to minimize the exposure to dust. Typically antistatic chip trays from Entegris (www.devicecare.com) or gel-boxes from Gel-Pak (www.gelpak.com) are used to store bare silicon chips.

The main goal of the cleaning process is to remove chemical and particulate contaminants from the surface of the chip in order to ensure successful device fabrication. Chemical contaminants include grease from human contact and polymers left from the previous processing steps. Grease and polymer residue can interfere with the good adhesion of the deposited metal layers. Particulate contaminants, such as dust and silicon fragments, can create pinholes in dielectric layers deposited on the chips and lead to short circuits between the top metal gate and the underlying metal contacts to the nanowires. The standard cleaning procedure is as follows:

1. 2 minutes of oxygen plasma cleaning using the 100 Watts power setting.

2. 5 minutes in hot trichloroethylene (TCE)

3. 5 minutes of ultrasonication in acetone

4. 5 minutes of ultrasonication in isopropyl alcohol (IPA)

5. blow-drying in nitrogen gas

All the organic solvent cleaning should be performed inside a fume hood, where a person's exposure to hazardous fumes is limited. Oxygen plasma cleaning is used to remove any photoresist or e-beam resist from the surface of the chip, remaining from the previous processing steps. TCE is used to degrease the chips. The TCE step should be done in a glass or Teflon beaker because a plastic beaker can be dissolved by TCE. The TCE step can be also done at an elevated temperature of about 70°C if needed to enhance the cleaning performance. If inhaled, TCE is carcinogenic. Therefore the TCE step should be done inside a fume hood. The third step is ultrasonication in acetone. This step is used to shake off the particulate contaminants from the surface of chips. Ultrasonication can be skipped or kept minimal if submicron sized metal contacts or nanowires are already on the chip. Otherwise, you are running a risk of removing those small objects off the chip along with particulate contaminants. The fourth step is done in isopropyl alcohol. The IPA step is used to remove any remaining contaminants including acetone traces. Although IPA is a weaker solvent than acetone, IPA itself doesn't leave any residue on the chip when it dries. When all the solvent cleaning is done, a nitrogen gun is used to dry the chip completely. The blow drying step is done with the chip securely pressed on a layer of lint-free cleanroom wipes with a pair of tweezers to prevent chips from flying off.

3.2.3 Deposition of Nanowires

Our GaN nanowires are usually grown on silicon or sapphire substrates. The GaN growths are scattered randomly throughout a substrate as shown in the Figure 3-8. These nanowires need to be transferred to an appropriate substrate, as discussed in section 3.2.1, in order to make electrical measurements on individual nanowires. The nanowires were either wet or dry transferred to the measurement substrate,

which has pre-made location markers as shown in Figure 3-12. As a quick and dirty method, one can use a so-called dry transfer method. In the dry transfer method, nanowires can be collected off the growth substrate with a piece of filter paper and brushed onto the measurement substrate while the growth substrate is left intact . However, the dry transfer method tends to deposit nanowires unevenly and it is harder to control the density of the deposited nanowires using dry transfer. For the aforementioned reason, the wet transfer of wires is the favored method as the density of the deposited nanowires can be readily controlled by changing the volume of the solvent. In the wet transfer method, the nanowires were harvested by ultrasonic agitation in Isopropyl Alcohol and a drop of the resulting nanowire suspension was transferred to degenerately doped p++ Si(100) wafers with a $\sim$300 nm thermally-grown oxide layer on the surface. After the transfer of the nanowires, locations of randomly deposited nanowires are mapped out from a scanning electron micrograph (SEM).

The location markers are an array of square dots 2 μm on a side with a period of 40 μm. Each dot has one column and one row number assigned to it. Several images like Figure 3-12 are taken to select suitable nanowires for measurements. SEM imaging is used here but in some cases atomic force microscope (AFM) images or even optical microscope images are used. The optical microscope can be used for nanowires longer than 10 μm even though the wire diameter is much smaller than the diffraction limit of light. SEM is the preferred method since it can provide a detailed picture of individual wires. However, exposing nanowires to high energy electron beams can lead to an alteration of the nanowire properties, and therefore the usage of SEM should be limited and used with caution.

The SEM used in this work is a LEO Field Emission Electron Microscope with a nominal resolution of 1.2 nm. Typical imaging parameters are 6 nm for the working distance and 3-5 kV for the acceleration voltage. A higher acceleration voltage produces a better image resolution but a lower image contrast. Figure 3-12 is a typical SEM image taken to locate nanowires. Ideally, isolated long straight nanowires are selected for device fabrications. Generally speaking, nanowires longer than 10 μm are

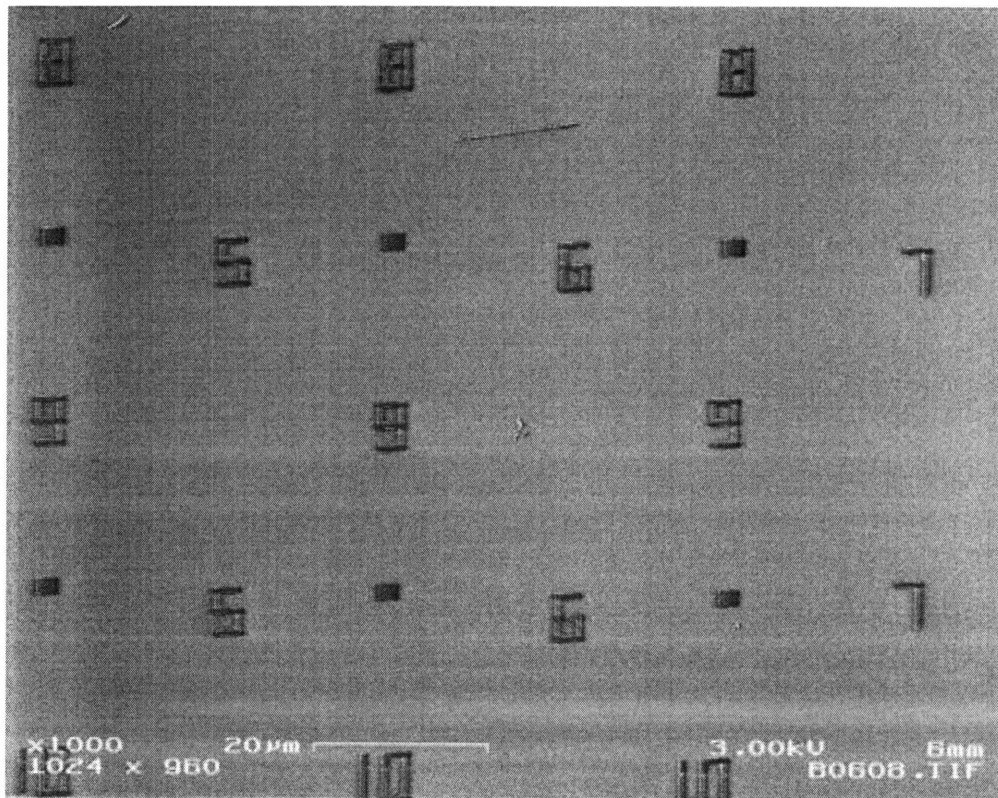


Figure 3-12: SEM image on a 20 μm scale of a deposited GaN nanowire on a substrate with numerical markers (see text).

necessary for 4-point measurements.

3.2.4 Electron-Beam Lithography

Electron-beam lithography is a pattern transfer technique just like photolithography. The electron-beam lithography technique is useful for writing submicron sized features because a beam of electrons does not suffer from the diffraction limit, which exists with photolithography. Thus electron-beam lithography is ideal for writing contact electrodes on nanowires. We can pack a multiple number of contact electrodes within the length of a nanowire with the fine resolution of the electron-beam writing technique. Also in this way the precise placement of the electrodes with respect to the nanowire is possible. Even though small features can be written with electron-beam lithography, its writing coverage is fairly limited due to the slow writing speed. The electron-beam writes patterns in a serial manner, which is slow compared to the

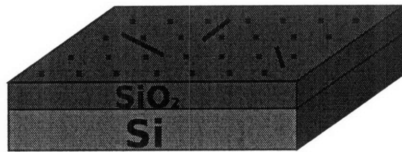
parallel process of photolithography. Photolithography transfers the entire pattern to the resist layer at once. Therefore the electron-beam lithography is exclusively used in academia while photolithography is much preferred in industry. Chemicals used in the developing process can also determine the accessibility of a particular lithographic method. All of the chemicals used in electron-beam lithography are neutral while strong basic developers are used in photolithography as will be discussed in section 3.2.6.

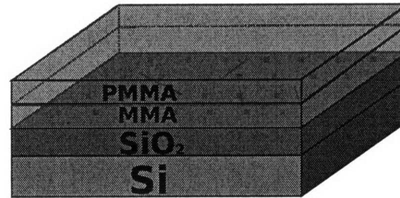
The step-by-step process of fabricating metal electrodes on nanowires by electron-beam lithography is shown in Figure 3-13. A detailed description of each step is given below.

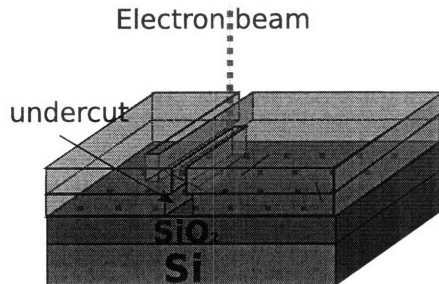
PMMA spin coating

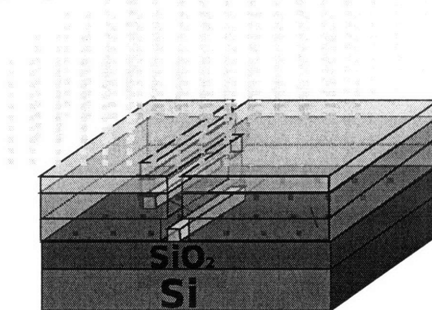
Polymethyl methacrylate, PMMA, is a transparent plastic which is electron-beam sensitive. The resists used in this work are 950K PMMA, and copolymer MMA or 495K PMMA. The numbers 950 K and 495 K indicate the molecular weight of the resin in the solvent which is either chlorobenzene or the safer anisole. The copolymer MMA is formulated in the solvent ethyl lactate. After all the imaging of the wires is done, a bi-layer of e-beam resists is spin coated on top of the nanowires. Typically, a bi-layer of MMA EL-10 and 950K PMMA C2 is used to achieve undercut development, which facilitates the lift-off process for thick metal deposition. The diameters of nanowires are between 20 nm and 100 nm on average, which means that the deposited metal should be at least 150 nm thick to avoid a break in the deposited metal electrodes. The undercut produced by MMA EL-10 adds 500 nm width in each direction, which means that the separation between two adjacent electrode patterns should be larger than 1 μm. For a closely placed electrode pattern, the MMA layer can be replaced with 495K PMMA, which creates a lesser undercut.

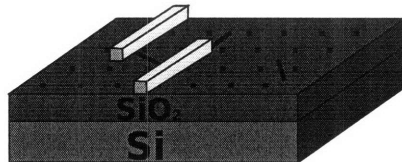
The actual spin coating recipe is the following. A single drop of MMA EL-10 solution is deposited on the chip spinning at 500 rpm. The spinning rate is then stepped up to 4000 rpm which is maintained for 40 seconds to evenly coat the chip. After spinning the MMA layer on, the chip is baked on a hot plate at 180°C for 5











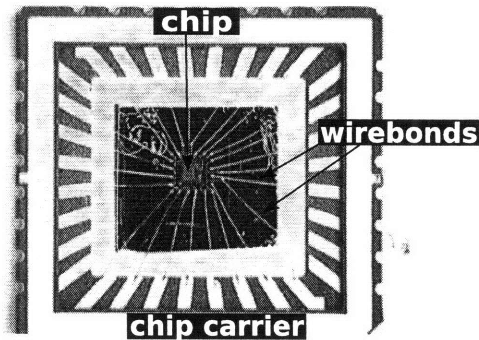


Figure 3-13: Schematic view of the electron-beam lithography process. (a) First, nanowires are deposited on the chip. (b) A bilayer of MMA/PMMA is spun on the chip in the spin coating process. (c) An electrode pattern is written on the chip after development. An undercut is formed by using MMA. (d) Metal is then evaporated on the chip. (e) The remaining resist is dissolved in acetone and only the metal electrode pattern remains after the lift-off process. (f) The chip is then wire bonded and mounted on a chip carrier for measurements.

minutes to remove any remaining solvent from the chip. The same recipe is used for the second layer of PMMA. At this spinning speed, the EL-10 forms about a 500nm thick layer and 950K C2 PMMA forms a layer around 100nm thick.

E-beam writing

This step is the actual writing of the electrode pattern using an electron-beam writer. Currently, we have three different writing systems available at Harvard University where this work is done. The three systems are the old JEOL 6400/Nabity system, the relatively new Raith system, and the newest addition, JEOL JSM-7000F system. The JEOL 6400 is actually a scanning electron microscope and it was modified to work as an electron-beam writer with the addition of the Nabity Pattern Generation System (NPGS). The JEOL 6400/Nabity system is useful for quickly writing large patterns such as bonding pads, since its filament can generate very large currents (>200 nA). The newest member of the JEOL family is the JEOL JSM-7000F, whose beam current is also fairly large (10pA-200nA). The Raith 150 electron-beam lithography system is used in this work. The Raith 150 is an ultra-high resolution electron beam lithography system capable of writing patterns with resolutions of 50 nm for direct-write lithographic applications. The system also has a Scanning Electron Microscope to facilitate imaging and navigation of the sample. The main advantage of this system is its capability to write over an entire wafer as large as 6 inches by a write-field stitching technique. The maximum width of one write-field is around 800 μm but we typically limit the write-field to 100 μm for better writing accuracy. The idea behind write-field stitching is the following. In order to write a design larger than one write-field, which is often what is needed, it is necessary to write over several write-fields by putting several write-fields adjacent to each other. For accurate stitching, the sample stage is translated by a combination of servo-motors and piezo-electric actuators guided by a laser-interferometer. A high precision with 5 nm resolution can be achieved by such a system. Figure 3-14 illustrates write-field stitching.

Based on the location of nanowires, the electrodes pattern is designed and fed into

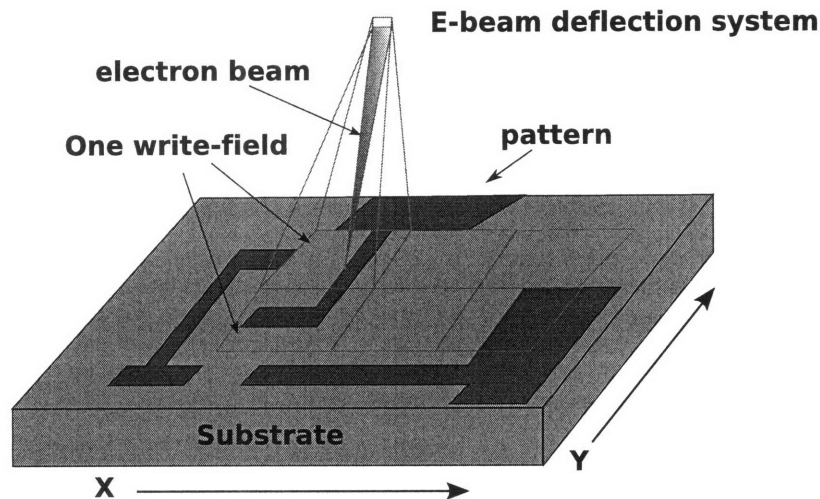


Figure 3-14: Schematic illustration of Write-field Stitching.

the computer which controls the Raith 150 electron-beam lithography system.

For writing large features over 1 μm, a 120 μm aperture is used to speed up the writing process. For submicron features, the smaller 30 μm aperture is used. Whenever possible, it is better to avoid using more than one aperture. Otherwise, re-alignment of the aperture and of the focus is necessary for each aperture setting. The electron-beam writing is done on the bi-layer of the e-beam sensitive resists. The resists used are poly methyl methacrylate (PMMA) and copolymer MMA. When exposed to the electron beam, these complex macromolecules get broken down into simpler compounds, which can be easily dissolved in a chemical developer. The developer used is a cocktail of 3 parts IPA and 1 part methyl-isobutyl ketone (MIBK) by volume. The typical development time is one minute in the 1:3 MIBK:IPA developer. The development can be promoted further by stirring the developer solution or moving the chip around vigorously in order to supply fresh developer and bring it into contact with the resist. Some precaution needs to be practiced before the development to remove any possible contaminants, such as carbon particles and sil-

ver particles from fixing the chip on the sample stage. Such particles can clog the PMMA resist pattern and cause a break in the deposited metal film later on. Rinsing in isopropyl alcohol (IPA), followed by the nitrogen blow dry step can be used for this purpose. After the development, a rough examination of the developed pattern can be done under an optical microscope to check if nanowires bridge the electrode pattern properly.

Metallization

The metallization is the fabrication step in which electrical interconnects are formed with selected metals. We have used three different methods of metallization. They are thermal evaporation, electron-beam evaporation, and sputtering. Thermal evaporation works by heating a metal source until it melts and starts evaporating. Joule heating is provided by flowing a high current through a metal boat, which holds a material source. A thermal evaporator is a clean method to deposit relatively low melting point metals, such as chromium and a gold layer (Cr/Au) or titanium and a gold layer (Ti/Au). The need for other methods of metallization arises when the evaporation of certain metals is difficult. For example, platinum (Pt) has a high melting temperature of 1768.3°C. At this temperature, the tungsten boat, which is used to hold Pt pellets, is prone to break. The other popular method of evaporation is e-beam evaporation. E-beam evaporation uses an electron beam with a high energy of several keV to boil off a small spot of a source material in the crucible. With local heating of a source material, e-beam evaporation is a better choice to deposit low vapor pressure materials like platinum. Some dielectric materials like aluminum oxide (Al_2O_3) or silicon dioxide (SiO_2) can also be evaporated using an e-beam evaporator. However, e-beam evaporation is not the best way to deposit compound materials. The stoichiometry of the source material is not preserved when evaporated, because the evaporation rate depends on the atomic weight of each element. When a conformal coating is required, sputtering is much better than either of the evaporation methods. For the evaporation methods, the pressure inside the evaporation chamber is about 10^{-6} or 10^{-7} Torr. At this low pressure, the mean free path of the evaporated

atoms is of the same order of magnitude as the vacuum chamber dimensions, so these atoms travel in straight lines from the source to the substrate. This behavior results in a shadow effect and a break can form in the deposited electrode over nanowires. On the other hand, with the sputtering technique, atoms in a solid target material are dislodged or sputtered off by the plasma of a noble gas such as Argon and are deposited on the substrate. The presence of the plasma causes multiple scattering events before sputtered atoms reach the substrate. These multiple scattering events result in conformal deposition of the source material. However, the subsequent lift-off process can be hampered by conformal deposition. Another advantage of the sputtering technique is that the deposited thin film has the same stoichiometry as the target material, which is useful for deposition of compounds materials.

Once the electrode pattern has been written on the resist layer, a metal can be evaporated or even sputtered. Typically Ti/Au or Cr/Au metal contacts are deposited by thermal evaporation. The titanium and chromium layers are used to form ohmic contact with GaN nanowires [73]. The gold layer is a capping layer. Right before the deposition, the samples are exposed to an O_2 plasma at 50 Watts for 60 seconds to remove residual polymer from the previous lithographic procedure and the samples are dipped in 1:7 HF:NH_4F_3 for 3 seconds to etch any oxide layer from the contact area of wires.

Lift-off

The evaporation step leaves the chip with a blanket coating of a gold layer. The lift-off process takes care of the excess metal by dissolving the PMMA resist in acetone. A thick layer of deposited metal can often lead to difficulties in the lift-off process by forming a continuous metal layer across the developed area, which is a recessed part in Figure 3-13(c), and the undeveloped area. Therefore, the evaporation thickness should be no more than about 70% of the resist thickness to avoid a lift-off problem. In addition to using a thick layer of resist, the bi-layer with the undercut in the bottom resist can assist in the lift-off process. To check that all the excess metal has been lifted-off, the chip can be inspected under an optical microscope. The inspection

is done best while the chip is still wet with acetone, otherwise the excess metal will stick to the chip and won't come off. To keep the chip wet in acetone under the optical microscope, we use a shallow petri dish. If all the excess metal isn't lifted-off, the chip can be soaked in acetone for longer or even a short burst of ultrasonication can be used. However, with nanowires already present on the chip, we usually avoid using ultrasonication. When the lift-off of excess metal is completed, the chip is squirted with isopropyl alcohol and blown dry with a nitrogen gun.

Annealing of Ohmic Contacts

In order to study the material properties of GaN nanowires, it is necessary to have ohmic contacts, and this is especially true if 2-point measurements are used. Most of the metal contacts on our GaN nanowires show ohmic contact without any high temperature annealing step. Occasionally we used the Jeptec Rapid Thermal Annealer to achieve a better contact to the GaN nanowires. The annealing step is done for 1 minute at 550°C in a slightly overpressured nitrogen gas atmosphere.

3.2.5 Wire bonding

Wire bonding is the process of making electrical interconnections between the device and the outside world. A picture of a wire bonded and mounted sample is shown in Figure 3-13(f). The chip is first mounted with silver paint on a 32-pin leadless chip carrier (LCC03218) bought from www.spectrum-semi.com. It usually takes 10 minutes or so for silver paint to dry. The silver paint provides a good electrical contact to the backside silicon gate as well as thermal contact [74]. The LCC03218 chip carriers can be fitted into LCC sockets obtained from www.locknest.com. Once the chip is mounted on the chip carrier, wire bonding is done to complete the device fabrication process. Wire bonding works by rubbing a fine metallic wire onto the bonding pad with ultrasonic energy. The typical bonding wire we use is 99.99% pure aluminum with a diameter of 1 mil and 1-3% elongation. We usually wire bond to the gold-plated nickel lead of the chip carrier first and then to the bonding pad on the

chip. As a precaution against possibly poor wire bonding or bad wiring in the sample probe, important devices can be wire-bonded multiple times or bonded to multiple leads of the chip carrier.

3.2.6 Photolithography

As discussed in section 3.2.4, e-beam lithography is mostly used for fabricating electrodes on a single nanowire for its precise alignment capability and high resolution. However, the time- consuming part of the processing is locating a suitable nanowire with respect to the location markers and designing a new writing pattern for every sample. An area of 600×600 μm^2 must be surveyed in order to find the nanowires that are long, straight, and isolated from other wires and from any unwanted debris. To cut down the initial preparation time for the fabrication of nanowire devices, we seek after an alternative lithography method. The current photolithography technique can comfortably pattern 2-point contacts on nanowires, longer than 10 μm. We have even occasionally fabricated 4-point contacts on long nanowires using photolithography. We designed a photomask with multiple electrode patterns covering most of the chip, which has a 5×5 mm^2 area. A "blind" photolithography is performed on the chip, and the chip is scanned for successful metal contacts on individual nanowires. Using this scheme, around 10 nanowire devices, on average, are fabricated on a chip with an area of 5×5 mm^2.

Figure 3-15 shows an unusually long nanowire, longer than 30 μm, along with a short nanowire, which overlaps the left part of the long nanowire. A 4-point contact, denoted by numbers 1 through 4, is made on the right part of the long nanowire. Even if the short wire shown in Figure 3-15 possibly connects the leads 1 and 2, voltage drop across the leads 2 and 3 is not influenced by this short as long as a constant current is supplied between the leads 1 and 4. Photolithography processing is basically the same as the e-beam lithography process shown in Figure 3-13; PMMA spin coating is replaced by photoresist spin coating and UV light exposure is used instead of e-beam writing. Our recipe for photolithography is as follows:

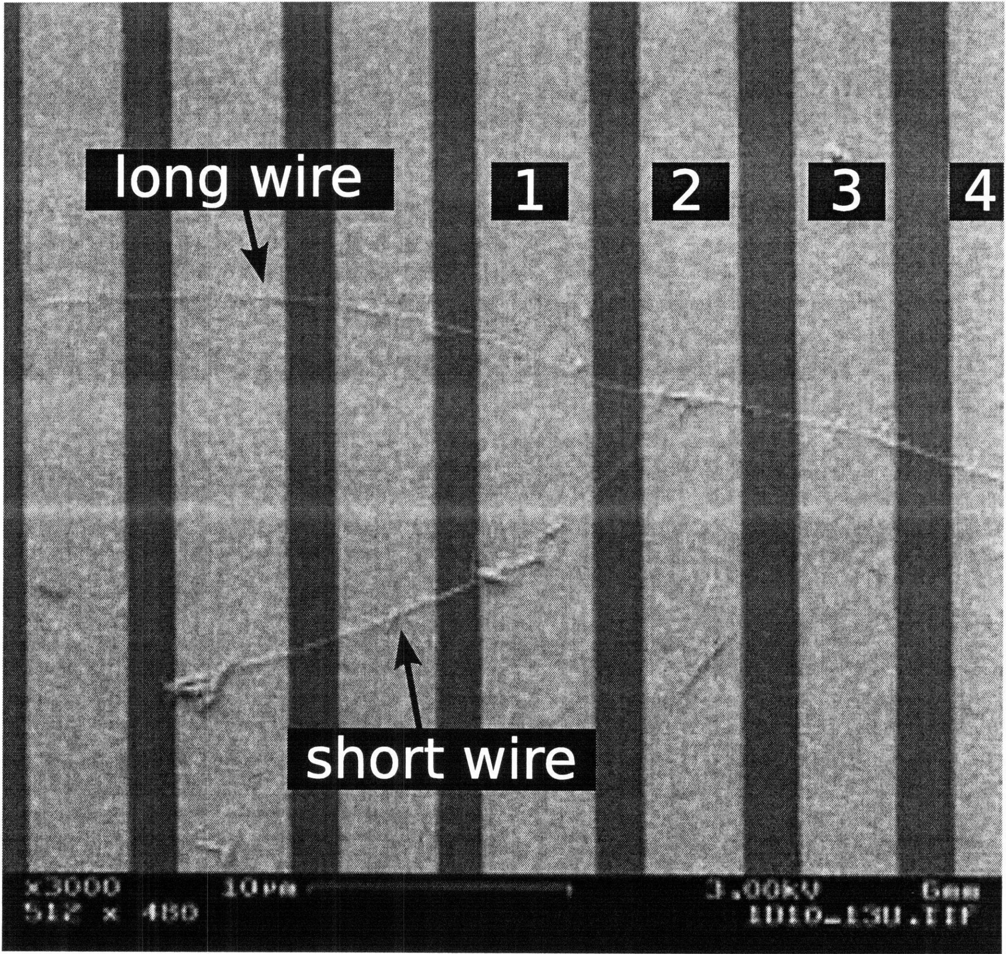


Figure 3-15: SEM image of multiple contacts made on a short and a long GaN nanowire fabricated by photolithography.

1. Deposit nanowires on the chip.
2. Remove water molecules from the chip by baking on a hotplate at 200°C for 5 minutes.
3. Spin coat LOR-3A at 500 rpm for 5 seconds, followed by 4000 rpm for 40 seconds.
4. Bake on a hotplate at 170°C for 5 minutes.
5. Spin coat Shipley S1805 photoresist at 500 rpm for 5 seconds, followed by 4000 rpm for 40 seconds.
6. Bake on a hotplate at 115°C for 5 minutes.
7. Expose in Karl Suss MBJ-3 mask aligner for 1.85 seconds.
8. Develop in MF CD-26 for 1 minute, followed by rinsing in DI (de-ionized) water and blow dry.
9. Bake on a hotplate at 125°C for 5 minutes (optional)
10. Evaporate metal up to 300 nm thick.
11. Lift off using microchem's "Remover PG" or NMP (N-methylpyrrolidone) at room temperature; elevate the temperature to 70°C if the sample has been exposed to a high temperature, above 190°C.

3.2.7 Sample Safeguarding

One bad winter, we lost more than 80% of our devices due to static electricity. Static electricity is much worse in winter than in summer because the air is much drier in winter than in summer. Dry air is a relatively good insulator and charges tend to build up in one place. In contrast, humid air with polarized water molecules can promote discharging of a charged object. Figure 3-16 illustrates what happens to the nanowire when static electricity attacks. To avoid destroying our devices from

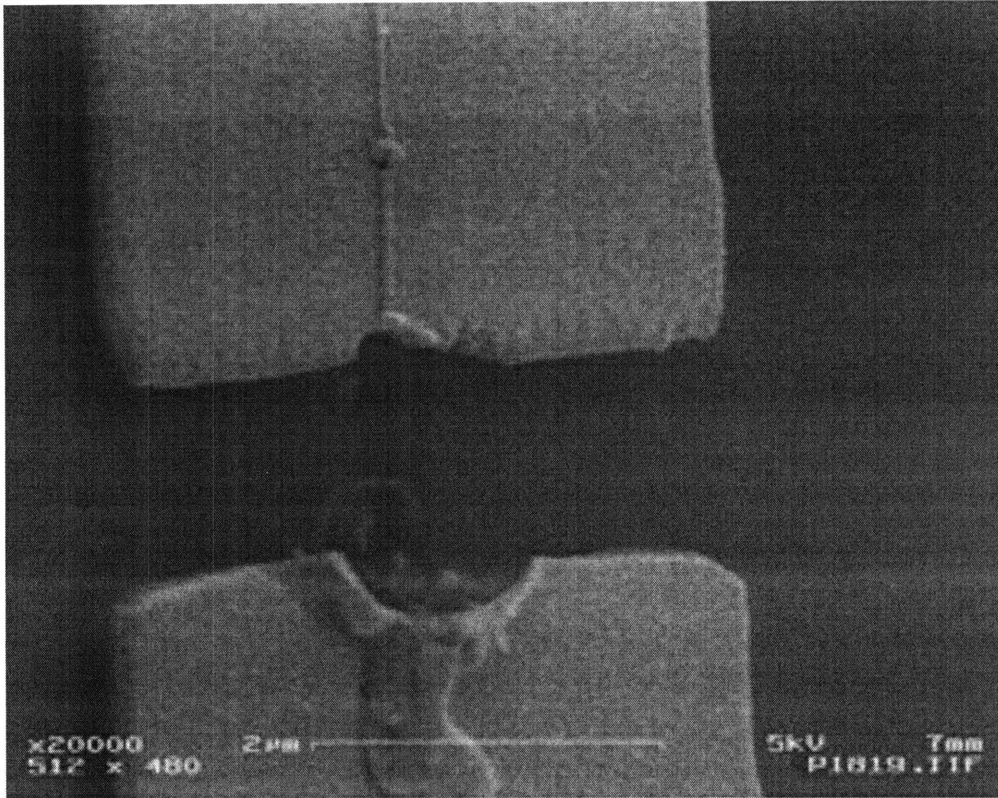


Figure 3-16: SEM image of a burned-out GaN nanowire due to static electricity.

static electricity, we make sure we discharge ourselves when we handle our devices by wearing the ESD (electrostatic discharge) wrist strap, which safely channels the static electricity to a proper ground. The samples are also stored in a static free container, which is made out of conductive material to avoid electric charge buildup inside the container. Also any electrical access to the sample is done via a low-pass filter with a cut-off frequency of 16 MHz, which safeguards the samples from spikes created by repeatedly connecting and disconnecting BNC cables to the multiple BNC box (Figure 3-17).

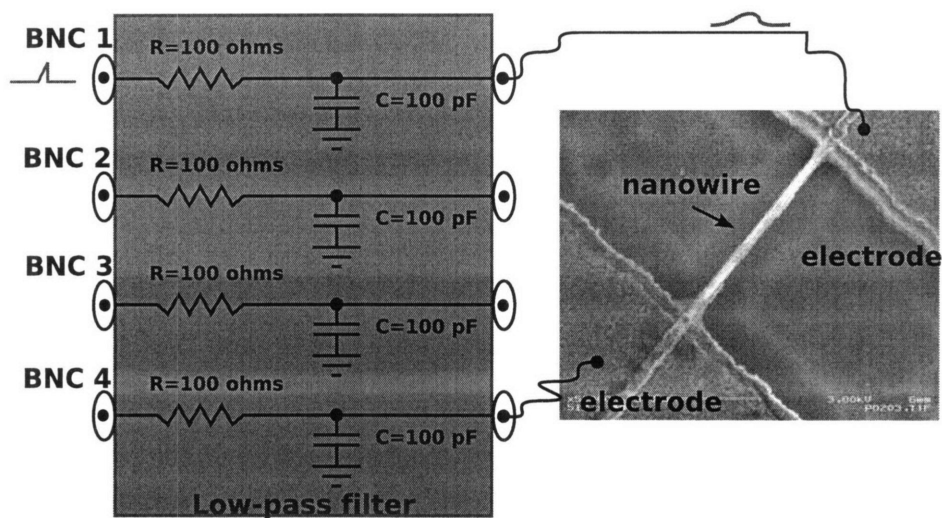


Figure 3-17: Schematic diagram of a low-pass filter attached to the sample.

Chapter 4

Measurements on a Nanowire Field Effect Transistor

4.1 Introduction

The field of nanotechnology has been born out of the need to make electronic and optoelectronic devices smaller and more densely packed. The main interest of nanotechnology research lies in the discovery of novel phenomena and the possibility of improvements in device performance. A top-down approach has been successfully implemented in the microelectronic industry to produce ever-shrinking devices. However, because of the economic burden and scientific difficulties associated with the top-down approach, an alternative approach, known as a bottom-up approach, has been sought after. The bottom-up approach relies on chemical synthesis to build functional electronic structures such as nanowires and this is the approach taken by this work.

The material of our interest is GaN. GaN is a wide band-gap (3.4 eV at 300°K) semiconductor with the wurtzite crystal structure. Wide band-gap semiconductors are needed for short wavelength optoelectronic devices and high-power/-temperature devices. Characterization of the material is essential for successful device applications. However, the conventional methods of characterization are hardly suitable for nanowires due to their extremely small size and shape. Therefore, it is important to

find suitable characterization methods for nanowires. In this work, GaN nanowires are grown by HVPE or CVD, and characterized using a field effect transistor (FET) geometry. The background material on FET device physics is given in section 2.2. By forming metal electrode contacts to a nanowire and capacitively coupling the nanowire to a gate electrode, the electrical properties of the nanowires have been measured.

4.2 Experimental Details

GaN nanowires were grown by chemical vapor deposition (CVD) on sapphire substrates using nickel nanoparticles as a catalyst. The CVD reactor consists of a 25 mm quartz tube, placed in a hot-zone horizontal furnace. Prior to the growth, the system was pumped down to 2×10^{-5} torr and filled with ultra-high purity Ar gas (purity 99.999 %). Both the Ga source and the substrate were introduced into the hot zone, preheated to 900°C, and maintained there for an hour with a 60:1 mixture of Ar:NH_3 at a flow rate of 30 sccm. After the growth, the nanowires were harvested by ultrasonic agitation in ACS/USP grade ethyl alcohol and a drop of the resulting wires from this dispersion was transferred to degenerately doped p^{++} Si(100) wafers with 300 nm of thermally grown oxide on the surface. The p^{++}Si substrate was used as a global back-gate electrode. In some devices, a local top-gate electrode was fabricated as well to increase the capacitive coupling between the nanowire channel and the gate electrode. However, most of these top-gate devices became shorted to the top-gate before a gate bias high enough to deplete the nanowire could be applied. Electron-beam lithography was used to define multiple metal contacts on wires after suitable wires were located using a field emission scanning electron microscope (FE-SEM). "Blind" Photolithography (see section 3.2.6) was also used to increase the yield rate of devices. Metal contacts, typically Ti/Au , were deposited by thermal evaporation. Right before the deposition of the metal contacts, samples were exposed to a 50 W O_2 plasma for 60 seconds to remove any residual polymer left from the lithographic procedure and the samples were then dipped in 1:7 HF:NH_4F for 3 seconds to etch

away any residual oxide layer from the contact area of the wires. The latter step was essential for achieving Ohmic contact to the wires. The nanowire FET devices were imaged again with an FE-SEM to determine the length and diameter of the nanowire. Figure 4-1 shows an FE-SEM image of a GaN nanowire field effect transistor (top) along with a schematic diagram (bottom) of such a device. The diameter of the particular wire in Figure 4-1 is 20 nm and the channel length is 2.6 μm. Field effect transistor (FET) measurements were performed at room temperature using a probe station with an Agilent 4156C semiconductor parameter analyzer. For cryogenic temperature measurements, FET devices were wire-bonded onto a 32-pin die and held in a cryogen by a homemade insert.

4.3 Results and Discussion

Ohmic contacts were achieved on most of the nanowires as is confirmed by linear $I_{SD} - V_{SD}$ curves (see Figure 4-2). The contact resistance, R_C , between the Ti contact layer of the electrodes and the GaN nanowire was determined using four-point measurements to be less than 2 % of the wire resistance in nearly all cases and therefore negligible. This justified the use of two-point contact schemes to carry out the measurements. In devices having more than two contacts, only a single measurement on an arbitrarily chosen adjacent pair of contacts was included in the statistics. The specific contact resistivity value, ρ_C , was calculated from the measured contact resistance, R_C , assuming a cylindrical wire using the relation $\rho_C = R_C \cdot A$, where A is the electrode covered surface area of the nanowire. The specific contact resistivity thus calculated was 1×10^{-5} $\Omega\cdot$ cm^2 , which is comparable to another published value for CVD grown GaN nanowires [75]. The histogram of the resistivity values from the 52 CVD grown nanowire devices is shown in Figure 4-3. A Gaussian fit is shown to fit 90% of the data, excluding outliers which clearly fall outside the main distribution. The Gaussian is centered at an average resistivity of 6.3 mΩ·cm with a standard deviation of 3.3 mΩ·cm. The nanowire resistivity value, ρ_{nw}, was calculated from the measured nanowire resistance, R_{nw}, assuming a cylindrical wire

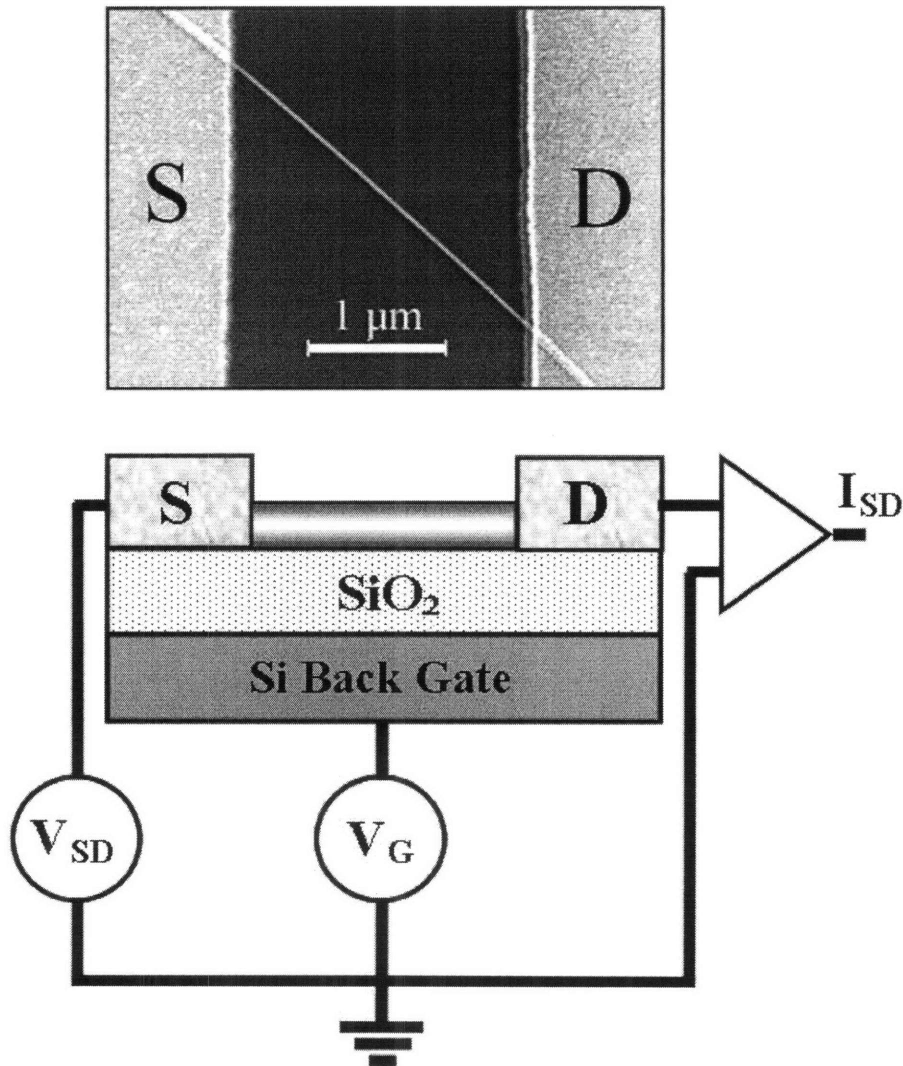


Figure 4-1: SEM image (top) and a schematic diagram (bottom) of a nanowire-channel field-effect transistor.

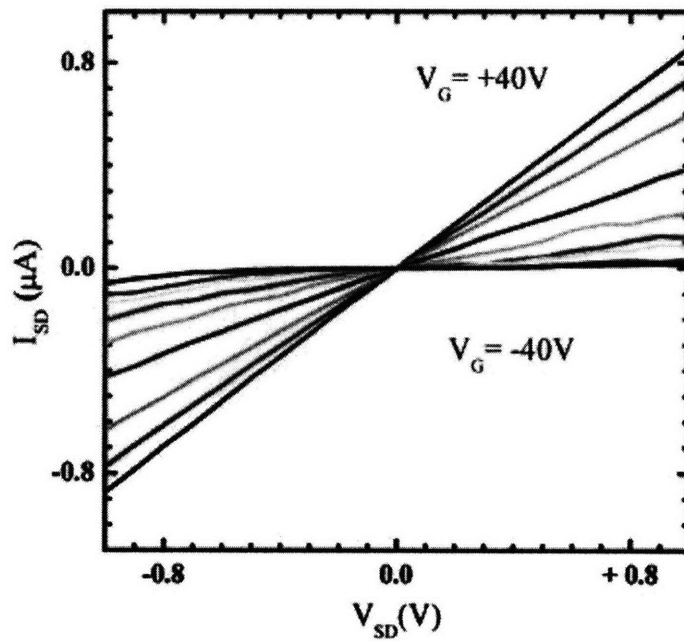


Figure 4-2: Current I_{SD} versus Voltage V_{SD} at gate biases from -40 to 40 V with 10 V increments. (color)

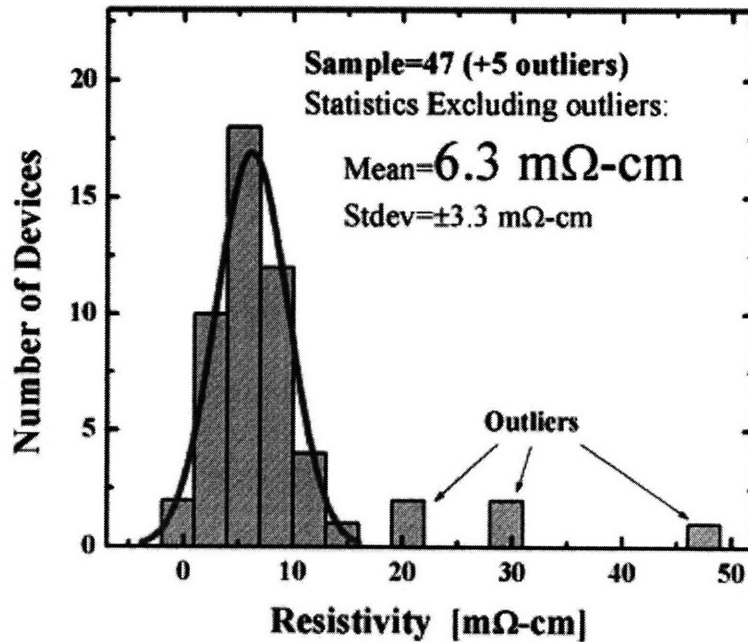


Figure 4-3: The resistivity distribution of a sample of 52 CVD-grown GaN nanowires.

with radius r and length l, and using the relation $\rho_{nw} = R_{nw} \cdot \pi r^2/l$. An average radius value was used for some nanowires with non-uniform cross section along the length. The largest source of error in determining the nanowire resistivity is from the determination of the radius. We used SEM (Scanning electron microscopy) or AFM (Atomic force microscopy) to measure the radius of a nanowire. The typical upper bound of the uncertainty in the measured radius was about 10 % and therefore the expected upper bound in the measured resistivity is about 20 %. This upper bound error was estimated for the nanowire with radius of 10 nm and the error is expected to be much smaller for the nanowire with larger radius.

Transconductance measurements at a series of source-drain voltages, V_{SD} , from 0.1V to 1V in increments of 0.1 V are shown in Figure 4-4. The curves show a gate threshold voltage, V_{th} , of around 30 V, and a switching ratio, I_{on}/I_{off}, of over 100 is deduced from the curve for a source-drain voltage of 1 V. Once the threshold gate voltage and the dimensions for a particular nanowire are known, the equilibrium

carrier concentration, n_e , can be calculated as follows, based on a wire-on-plane capacitor model,

$$n_e = V_{th}C/(e\pi R^2 L), \tag{4.1}$$

where R is the wire radius, and L is the length of the active nanowire channel between the source and drain contacts. The capacitance between the wire and substrate is given by [76]

$$C \approx \frac{2\pi\kappa_i\varepsilon_0 L}{\ln[2(h/R+1)]}, \tag{4.2}$$

where κ_i and h are respectively the dielectric constant and thickness of the insulator between the wire and the substrate. From Eq 4.1, the carrier concentration is estimated to be around $4 \times 10^{19}\text{cm}^{-3}$ for our GaN nanowires. The electron mobility μ for a nanowire field effect transistor can be extracted from the transconductance value in the linear regime above the threshold bias using the expression

$$\frac{dI_{SD}}{dV_G} = \frac{C\mu V_{SD}}{L^2}. \tag{4.3}$$

The mobility μ thus calculated from Figure 4-4 for a source-drain voltage of 1V is found to be ~18 $\text{cm}^2/(\text{V}\cdot\text{s})$, neglecting the voltage drop across the contacts. Most of our GaN nanowire FET devices displayed almost no carrier modulation due to an unintentionally high carrier concentration, which is a common observation for GaN nanowire growth [77, 78, 79]. The most probable sources for this high carrier concentration are believed to be nitrogen vacancies, and oxygen or silicon growth contamination [80, 81, 82, 83]. A gate-modulated switching behavior was only observed for the thinnest of our GaN wires.

For comparison, we also studied HVPE grown GaN nanowires. Figure 4-5 shows a histogram of the resistivity values from the 37 HVPE grown GaN nanowires. A similar average resistivity value of 8.1 mΩ·cm was found, compared to the CVD value of 6.3 mΩ·cm. The carrier modulation could not be achieved up to a gate bias of -40 V since our HVPE grown GaN wires are typically several times thicker than the CVD grown wires [2] and require a higher gate bias to deplete carriers from HVPE

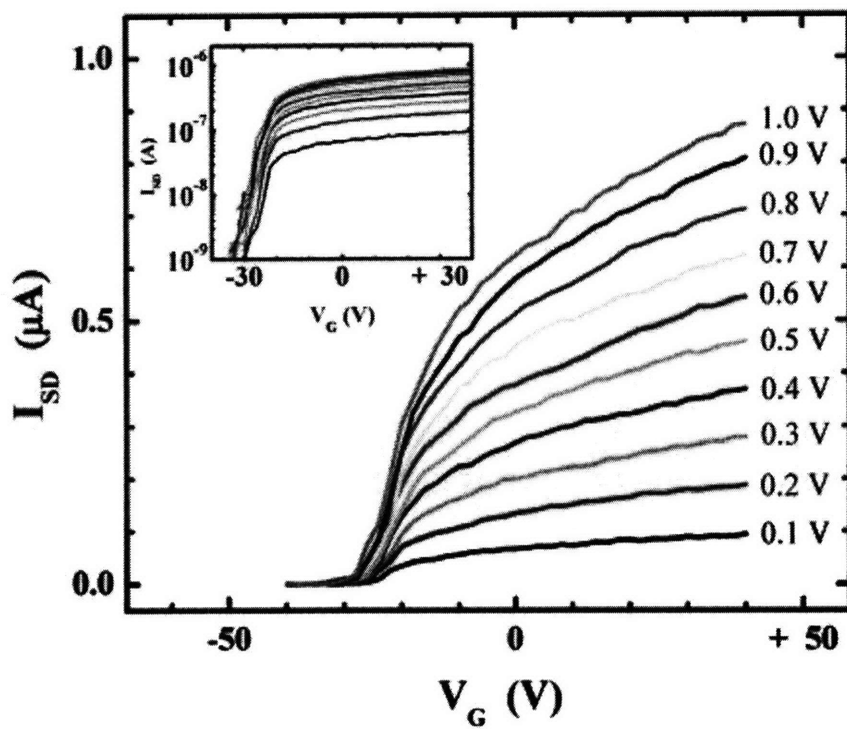


Figure 4-4: A plot of the source-drain current, I_{SD}, versus gate voltage, V_G, for source-drain voltages from 0.1 to 1 V in 0.1 V increments. The inset shows the same data in a log plot. (color)

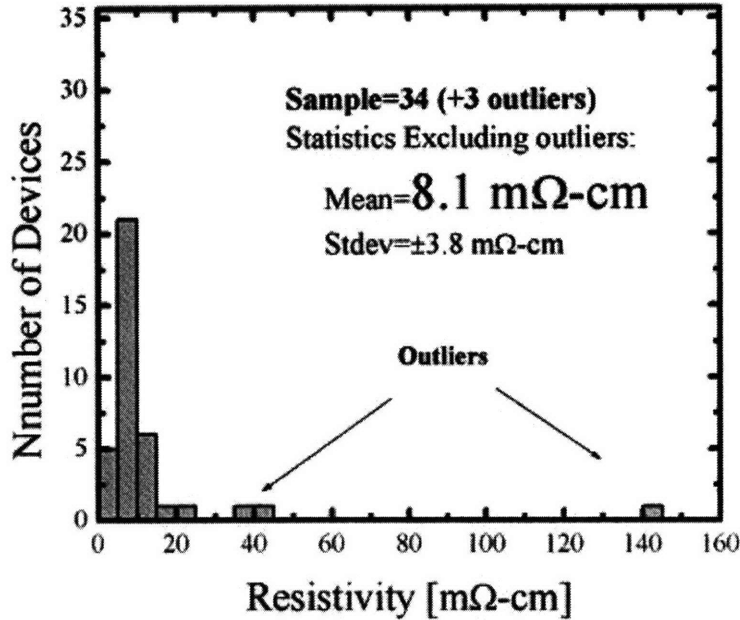


Figure 4-5: The resistivity distribution of a sample of 37 HVPE-grown GaN nanowires.

wires. Important electrical properties are summarized in table 4.1.

4.4 Conclusions

Nanowire FET devices were fabricated from GaN nanowires grown by CVD or HVPE and characterized by transconductance measurements at room temperature and temperature-dependent conductance measurements from 300°K to 4.2°K. Resistivity, carrier density, mobility and thermal activation energy have been estimated for our nanowires. Transconductance measurements indicated our CVD grown wires to be a degenerately doped n-type semiconductor with an electron concentration of 4×10^{19} cm^{-3}. Despite the high doping level, thin nanowires showed a switching ratio of over 100 and an electron mobility of 18 cm^2/V·s.

Table 4.1: Electrical Data for HVPE and CVD Nanowire FETs. There are missing values for some parameters for HVPE wires because even the thinnest of HVPE wires was too thick to reach a complete depletion of the carriers, which is needed for some of the characterizations.

	HVPE	CVD
Carrier Type	n	n
Carrier Density [cm^{-3}]	-	$4 \cdot 10^{19}$
Mobility [$cm^2/v{\cdot}s$]	-	~18
On-off ratio	-	> 100
Mean Resistivity [$m\Omega{\cdot}cm$]	8.1	6.3
Contact Resistivity [$\Omega{\cdot}cm^2$]	$1{\cdot}10^{-6}$	$1{\cdot}10^{-5}$

Chapter 5

Transport Properties of GaN Nanowires

5.1 Introduction

Interest in reduced dimensional systems is motivated by the novel physics that is revealed in nanoscale structures. The recent success of vapor-liquid-solid (VLS) [25] and other growth mechanisms [84, 85] have opened up this new exciting field of research for semiconductor nanowires as examples of one-dimensional systems. The field of semiconductor nanowire applications has been expanding quickly due to the ease of transferring existing semiconductor technology to nanowires. The unwavering flourish of the semiconductor field is largely due to the readily tunable optical and electrical properties of semiconductors. The optical and electrical properties depend on the number of carriers available in a semiconductor. This applies to semiconducting nanowires also. The capability to dope nanowires with impurities allows the control of their electrical properties, together with the selective growth of various semiconductor materials, which has resulted in sophisticated heterostructure devices [86, 87, 88, 89]. Moreover, the novel aspect of semiconductor nanowires over bulk semiconductors comes from their reduced size and enhanced ratio of surface area to the volume [71, 90, 91]. These particular characteristics of semiconductor nanowires have resulted in many applications, such as optical sensors, detectors, and chemical sensors [92, 93].

The size of a semiconductor nanowire can play a key role in the electrical properties through confinement effects in two different size regimes. The quantum confinement effect results in an enhancement of the ionization energy for impurities when the diameter of the nanowire is of the same order as the impurity Bohr radius [57, 58]. This size range, however, is rarely seen in nanowires, probably for thermodynamic reasons associated with the growth [94]. For diameters much larger than the impurity Bohr radius, the "dielectric confinement" effect increases the ionization energy significantly when there is a dielectric mismatch between the wire and the surrounding medium [59, 60]. This effect has been proposed theoretically [60] but has never been reported through electrical measurements. Herein, we report electrical transport studies of GaN nanowires and examine the "dielectric confinement" effect through the size-dependence of the impurity ionization energy observed in GaN nanowires. The background material on the dielectric confinement effect was previously provided in section 2.3.

Two different sets of donor levels were identified through a determination of the activation energies in the temperature dependent conductivity. The first set of impurity levels is quite shallow (< 5 meV) and doesn't seem to depend much on the radius of the nanowire. The second set of impurity levels is somewhat deep (> 40 meV) and depends on the radius of the nanowire.

We also observed variable-range hopping conduction in highly doped GaN nanowires and we attribute this behavior to the defective layer near the surface of the nanowire. We believe that this observation has not been reported so far in nanowires without focused-ion-beam (FIB) induced damage [95, 96].

5.2 Experiments

5.2.1 Nanowires on a SiO_2/Si substrate

A detailed description of the experimental aspects is given in section 4.2. To recap

in one line, nanowires were placed on a SiO_2 coated Si substrate and 80nm Ti/80nm Au electrical contacts were made on the nanowires.

5.2.2 Suspended Nanowire over a trench

Electrical measurements on nanowires are usually done with nanowires lying on a SiO_2/Si substrate as prepared in section 5.2.1. The pertinent question is then, "Does the dielectric environment around a nanowire affect the electrical properties of the nanowire ?" In order to preclude a possible effect from the substrate, we fabricated devices with the suspended nanowire over a trench. GaN nanowires are transferred to a SiO_2/Si substrate and metal contacts were defined using e-beam lithography. 80 nm Cr and 80 nm Au are then evaporated thermally for the contacts. Trenches are defined by e-beam lithography. After the e-beam exposure and development in 1:3 MIBK:IPA, the chips are postbaked on a hot plate above the glass transition point at 130°C for 30 minutes to promote the better adhesion of the PMMA layer to the substrate and to remove any pinholes. Otherwise, the oxide etchant can creep under the patterned PMMA and create a broader etching area than the lithographic pattern. 1:7 HF:NH_4F_3 is used to etch SiO_2. The chips are dipped in BHF for 3 minutes, which is long enough to remove a 300 nm SiO_2 layer under the nanowire. After the etching step, special care needs to be taken to avoid the nanowires from being pulled down by the surface tension of DI (deionized) water and sticking to the Si substrate which results in a poor contact to the metal electrode. Since we want to remove the effect of the substrate on the nanowires, the part of the nanowire touching the substrate is not ideal for the proposed experiments. In order to reduce the surface tension from the DI water, the chips are transferred to acetone while still wet from DI water and transferred again to IPA and blow dried with a nitrogen gun. We found that this triple rinsing step in descending order of surface tension reduces the damage done by surface tension significantly. An SEM image shows that the nanowires are taut and free from touching the substrate below (figure 5-1). Alternately one can also use the critical drying furnace to dry off the DI water.

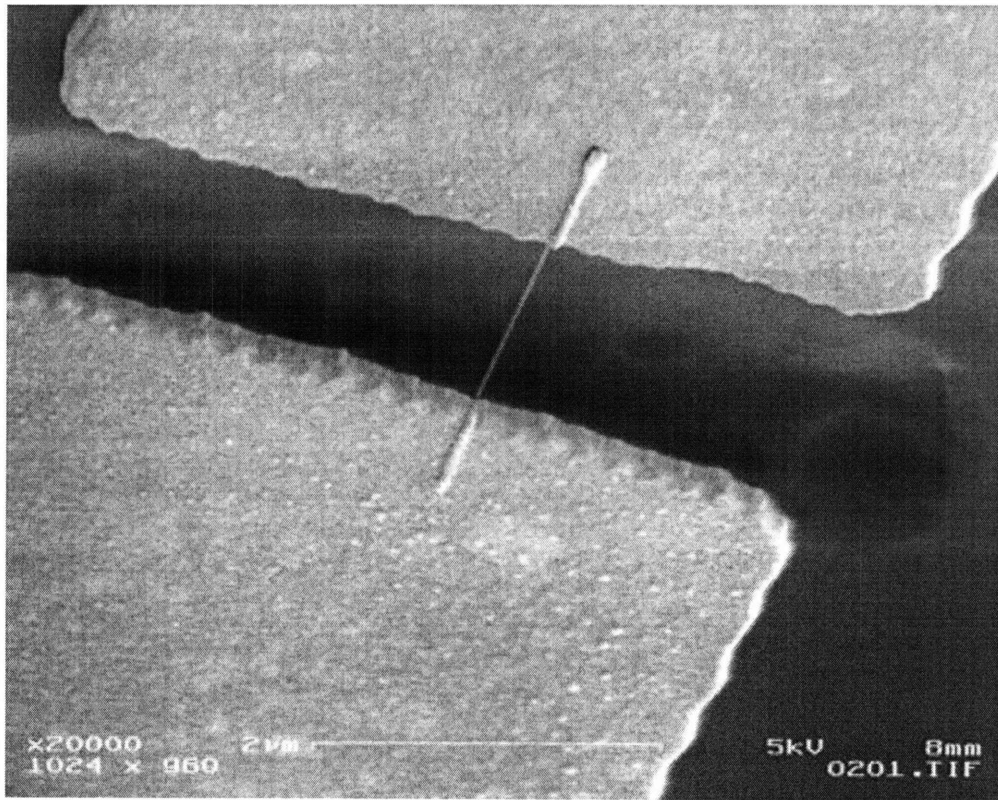


Figure 5-1: SEM image of a suspended GaN nanowire.

5.2.3 SiO_2 coated Nanowires

In the section 5.2.2 we devised an experiment to test the effect of the dielectric environment on nanowires by suspending a nanowire over a trench, where a nanowire is free standing without touching the substrate. In this section we coat nanowires with SiO_2. SiO_2 is either deposited by an RF sputtering method or grown by a plasma-enhanced chemical vapor deposition (PECVD) method. We give a detailed description of the PECVD process here. PECVD uses a plasma to promote the chemical reaction of the precursors, which react and decompose to deposit the desired dielectric material on the desired substrate. PECVD processing facilitates deposition at a lower temperature compared to regular CVD processing. We use a NEXX Cirrus 150 PECVD system, which is an ECR (electron cyclotron resonance) plasma-enhanced CVD system. ECR technology produces a high plasma density and low ion energy at a low chamber pressure, allowing the deposition of high quality films at relatively low temperature.The system is equipped with a load-lock wafer transporter, allowing fast system pump-down and a low base pressure of 10^{-6} to 10^{-7} torr.

We use silane (SiH_4) and oxygen (O_2) as the precursors to deposit SiO_2. The substrate temperature is kept at around 20°C, cooled by helium gas and water. The pertinent reaction is as follows:

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H. \tag{5.1}$$

First, nanowire devices are prepared as described in section 3.2.4. After the lift-off step, the chip with a patterned structure is transferred to the PECVD chamber for the deposition of SiO_2. Prior to the actual deposition, the PECVD chamber is pre-baked and cleaned with an oxygen plasma. After the initial cleaning, a 300 nm-thick film of SiO_2 is deposited on the sample for more than 30 minutes. Since the deposited film is everywhere on the chip, bonding pads need to be exposed by etching away the area above the bonding pads, facilitating a wire bonding process later; a quick photolithography and BHF (buffered hydrofluoric) acid etching step is applied to the chip. Figure 5-2 shows a GaN nanowire buried under PECVD grown SiO_2.

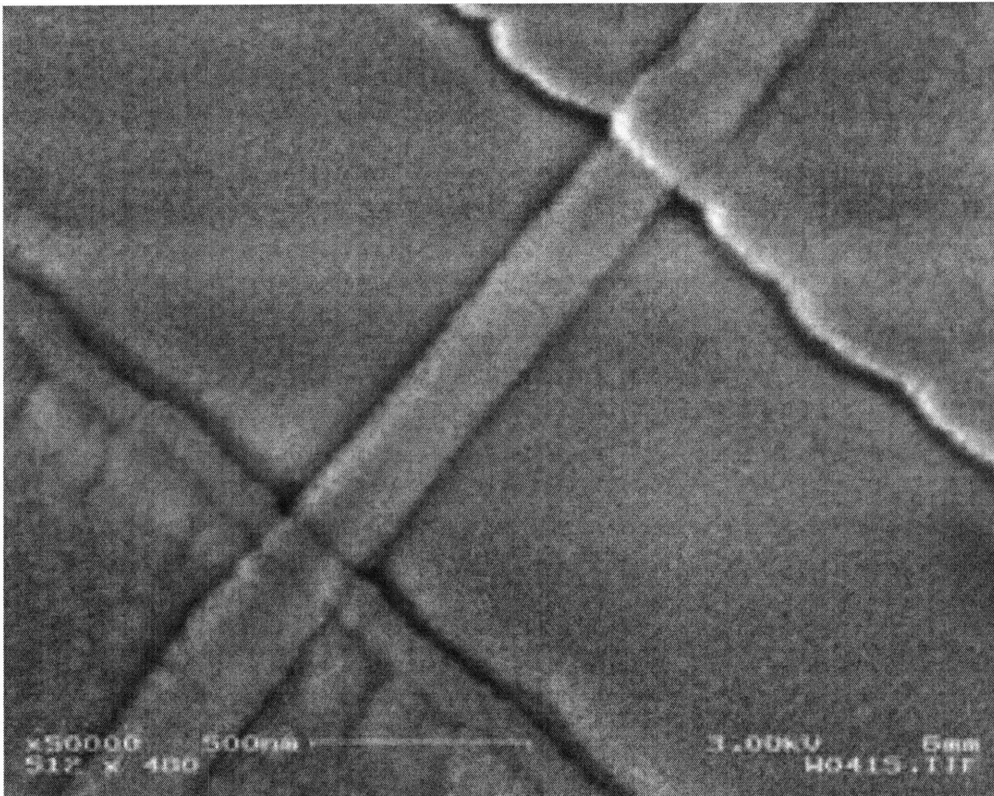


Figure 5-2: SEM image of a GaN nanowire coated with PECVD SiO_2.

5.3 Results and Discussion

We first analyze in detail the data for the case of a nanowire on a SiO_2/Si substrate and show the size-dependent transport in GaN nanowires in section 5.3.1, and then we present supporting experiments from the configurations with suspended nanowires and from SiO_2 coated nanowires in section 5.3.2 to remove any uncertainty from the first configuration with a nanowire on SiO_2/Si substrate.

5.3.1 Size-dependent Ionization Energy in GaN Nanowires

The temperature-dependent conductivity in the nanowires was measured to gain insight into the mechanisms involved in carrier transport. The conductivity as a function of temperature is plotted in Figure 5-3 for four CVD grown wires with 15, 25, 45, and 60 nm diameters. The donor thermal activation energies, E_{ai} , were estimated by fitting the experimental data in Figure 5-3 to

$$\begin{aligned} \sigma &= \sigma_s + \sigma_c, \\ \sigma_s &= \sigma_{so} + C_s T^{(\beta_s/2-\alpha_s)} \exp[-E_{a1}/(k_B T)], \\ \sigma_c &= C_c T^{(\beta_c/2-\alpha_c)} \exp[-E_{a2}/(2k_B T)], \end{aligned} \tag{5.2}$$

where $\beta_{s,c} = 1/2, 1, 3/2$ for 1D, 2D, and 3D transport [97], respectively, σ_{S0} is the temperature independent impurity band conduction at the surface of a nanowire, and $(-\alpha_{s,c})$ comes from the temperature dependence of mobility. We assume that the mobility in the surface of the nanowire is mainly determined by phonon scattering processes (α_s=3/2) rather than by ionized-impurity scattering processes [77], and therefore the net power dependence on temperature is negligible. For the core of the nanowire, we assume a weak compensation ($N_D \gg n \gg N_A$), and an exponential temperature dependence dominates the transport process. We simplified the fitting by neglecting the power law behavior in Eq. (5.2). we model our nanowire to have two conduction channels, one for the core of the nanowire and the other for the surface

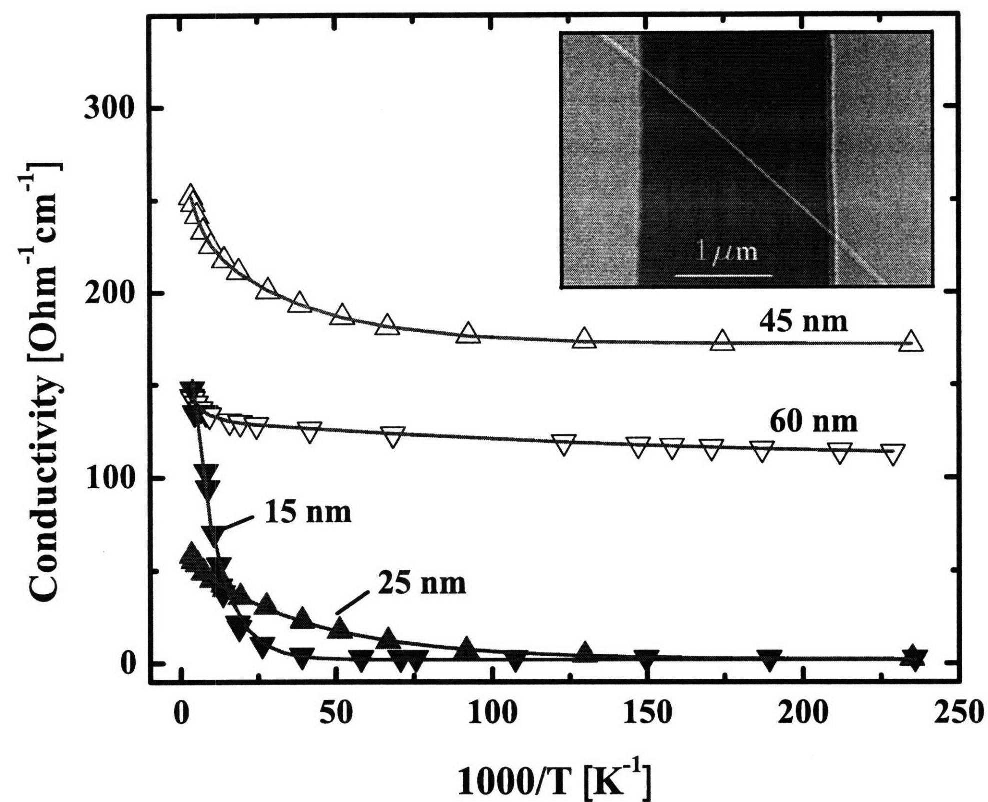


Figure 5-3: The conductivity versus 1000/T for 15, 25, 45, and 60 nm diameter wires. The points represent experimental data while the lines represent fits over the entire temperature range. The donor activation energy and other fitting parameters are reported in Table 5.1. The inset shows a scanning electron micrograph of an actual nanowire device described in the text.

of the nanowire. We suspect that surface segregation of impurities is taking place in the nanowire system, resulting in a degenerately doped surface and a non-degenerate core.

The fitting parameters in Table 5.1 show that our GaN nanowires with diameters of 25, 45, and 60 nm have two donor levels, one shallow (0.6 - 10.8 meV) and one relatively deep (42 - 73 meV). We attribute shallow levels to the impurities segregated to the surface and relatively deep levels to the impurities in the core of the nanowires. During a high temperature growth of the nanowires, most of the impurities segregate to the surface, where impurities find energetically favorable sites, and form an impurity band.

The temperature dependent conductivity was measured for nanowires with 4 different diameters and the activation energies were extracted by fitting Eq. 5.2. Each nanowire produced 2 sets of activation energies except for the 15 nm nanowire, which has a large fitting error (see $\tilde{\chi}^2$ in Table 5.1). So we excluded the data point for the 15 nm nanowire and plotted the activation energy versus radius in Figure 5-4 for the other three nanowires. The thermal activation energy for the impurity increases substantially as the diameter of the nanowires decreases, which could be attributed to the dielectric confinement [59, 60].

Table 5.1: The fitting parameters for the conductivity as a function of temperature given in Eq. (5.2) for nanowires with four different diameters. The 15nm nanowire has a large $\tilde{\chi}^2$ value because the curve fitting is poor in the low temperature region. The deviation of the fitting curve from the experimental data points is not noticeable in the provided linear plot (Figure 5-3). We also didn't find two values for the ionization energy for the 15 nm nanowire and therefore excluded the data point for the 15 nm nanowire in Figure 5-4.

D [nm]	C_s [$(\Omega\text{cm})^{-1}$]	E_{a1} [meV]	C_c [$(\Omega\text{cm})^{-1}$]	E_{a2} [meV]	σ_{so} [$(\Omega\text{cm})^{-1}$]	$\tilde{\chi}^2$
60	23.9±0.8	0.6±0.1	30.4±1.2	41.8±1.9	108.1±0.9	0.04
45	67.3±0.9	2.6±0.1	47.5±1.9	44.7±2.8	171.7±0.2	0.09
25	55.5±2.1	2.2±0.1	20.6±14.3	73.2±37.9	2.1±0.6	0.56
15	240.8±12.0	10.8±0.7	0	N/A	1.9±2.1	38

* Note: The chi-square is defined as $\chi^2 \equiv \sum_{i=1}^{N} \left(\frac{y_i - f(x_i)}{\sigma_i}\right)^2$, where y_i is the mea-

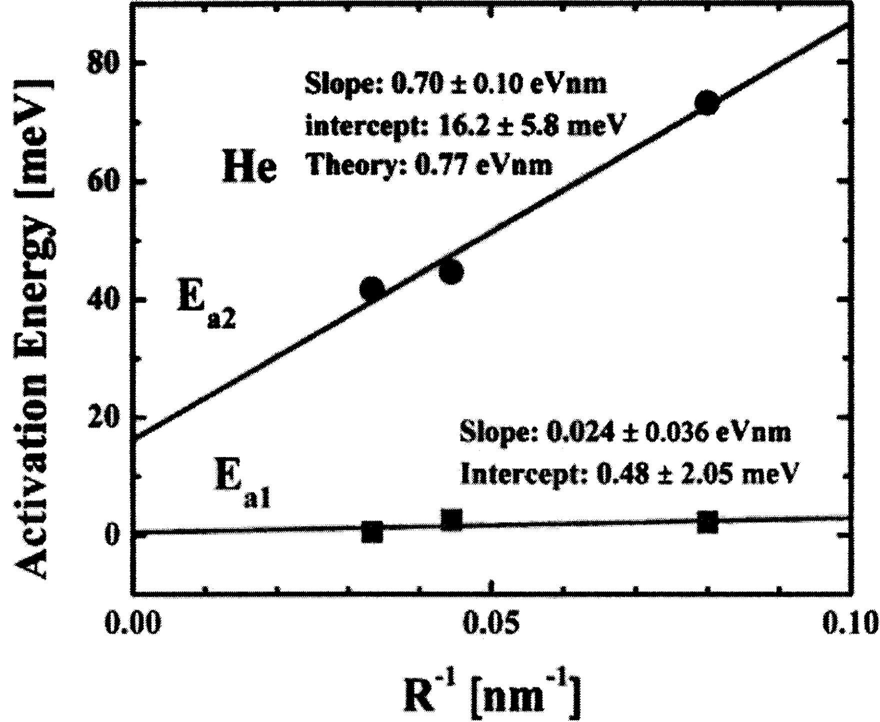


Figure 5-4: Activation energies from the fit of the data given in Figure 5-3 as a function of inverse wire radius. The lines are linear fits to the experimental data.

sured data point, $f(x_i)$ is the fitting value and σ_i^2 is the variance in the measured data. The reduced chi-square, $\tilde{\chi}^2$, is given as χ^2/ν, where $\nu = N - p - 1$, N is the number of observations and p is the number of fitting parameters. The good fit is said to be achieved when $\tilde{\chi}^2$ is close to one.

This self-energy effect arises via the interaction between the electrons bound to the donors and the surface polarization charges induced by the donor nucleus when there is a significant dielectric mismatch between the nanoscale system and its surroundings. For typical nanowires with a diameter larger than 10 nm, the shift of the conduction band edge due to quantum confinement is much smaller than the dielectric confinement effect. The shift in donor binding energy due to the dielectric confinement is calculated using [59, 60]

$$\Delta E = E_I - E_{I0} \approx \frac{2}{\varepsilon_{in} R} \frac{\varepsilon_{in} - \varepsilon_{out}}{\varepsilon_{in} + \varepsilon_{out}} F(\frac{\varepsilon_{in}}{\varepsilon_{out}}) = \frac{\gamma}{R} \quad [\text{eV}], \tag{5.3}$$

in which γ is the slope of ΔE vs. $1/R$ and

$$F(x) \approx \frac{0.0949x^3 + 17.395x^2 + 175.739x + 200.674}{x^2 + 50.841x + 219.091} \quad [\text{eV}\cdot\text{nm}]. \tag{5.4}$$

In Eq. (5.3), the self-energy correction to the impurity ionization energy is given. The slope γ depends on the dielectric constants of the nanowires and of their surroundings. E_{I0} is the ionization energy of impurities in bulk GaN, which is independent of the radius. Figure 5-4 shows the radius-dependent ionization energy for CVD grown GaN nanowires. The value of the slope obtained from the fit to the radius dependent ionization energy data (E_{a2} in Figure 5-4) is 0.7 ± 0.1 eV·nm. The value of γ, calculated from Eq. (5.3) assuming GaN nanowires were surrounded by helium gas, is 0.77 eV·nm and is within our fitting error. Since the nanowires are lying on a SiO_2 surface, we might expect to see some dielectric effect from the SiO_2 as well. However, given that the contact area to the SiO_2 substrate is fairly limited, the effect of the SiO_2 on the E_{a2} states was not observed. The E_{a1} states are fairly shallow and did not seem to display a strong dependence on the radius of the nanowires that were studied. We think it might be that E_{a1} is coming from the impurity band formed near the surface based on the shallow ionization values of 0.6 - 2.6 meV (see Table 5.1).

The bulk ionization energy, E_{I0} , is estimated to be 16.2 ± 5.8 meV by fitting the equation $E = \frac{\gamma}{R} + E_{I0}$ to the E_{a2} values in Figure 5-4. The activation energy of 16.2 meV is within the range for the donor ionization energy of either Si or O impurities or N vacancies [80, 81, 82, 83]. An alternative method such as a local electrode atom probe [70] or secondary ion mass spectrometry (SIMS) [69] is needed to identify the impurities present in these semiconductor nanowires.

In the low temperature region of Figure 5-3, a shallow impurity band at the surface of the GaN nanowire dominates the conduction behavior. All four nanowires displayed a minimal temperature-dependence of the conductivity with almost no activation in the low temperature region, which indicates the formation of an impurity band a few degrees above the Mott limit [98]. The transition from the localized impurity state to the delocalized impurity band occurs when $d/a_B < 2.5$, where $d = [3/(4\pi N_d)]^{1/3}$ and

$a_B = 0.53(m_0/m^*)(\varepsilon/\varepsilon_0)$ [Å] is the impurity Bohr radius. Using $m^*/m_0 = 0.22$ and $\varepsilon/\varepsilon_0 = 8.9$, the bulk values for Wurtzite GaN, the impurity Bohr radius is calculated to be around 21 Å. From the impurity Bohr radius, we can deduce the critical donor concentration to be $\sim 1.6 \times 10^{18}$ cm^{-3} , which is one order lower than the donor density predicted for our GaN nanowires by the simple calculation using Eq. (4.1). This back-of-the-envelope type calculation suggests that the donor concentration in our nanowire is high enough for an impurity band to form, even though a new criterion for the critical donor concentration may be necessary in nanoscale systems [60].

5.3.2 Confirmation of a Size-dependent Ionization Energy in GaN Nanowires

In section 5.3.1, a nanowire lying on a SiO_2/Si substrate is discussed. In this configuration, a nanowire experiences an inhomogeneous surrounding dielectric and this dielectric inhomogeneity might create uncertainty in interpreting the dielectric effect. In order to confirm the size-dependent behavior observed in section 5.3.1, a suspended nanowire structure and SiO_2 coated nanowire structure are fabricated as described in sections 5.2.2 and 5.2.3, respectively.

The conductivity as a function of temperature is measured for these two different configurations, suspended and SiO_2 coated, each with three different diameter nanowires. This conductivity vs. temperature plot for the suspended nanowire is shown in Figure 5-5 and the plot for the SiO_2 coated nanowire is shown in Figure 5-7. These conductivity data points are fitted with Eq. (5.2) as described in section 5.3.1 and activation energies are extracted. The resulting plots of activation energy vs. inverse radius are shown in Figures 5-6 and 5-8, respectively for the suspended nanowires and for the SiO_2 coated nanowires.

First, we discuss the size-dependent transport data. In Figure 5-6, the activation energy, E_{a2}, is inversely proportional to the nanowire radius with the slope $\gamma = 0.70 \pm 0.07$ eV·nm. This determined value agrees well with the theory which predicts $\gamma = 0.77$ eV·nm for a freely suspended nanowire configuration with relative dielectric

constants 8.9 and 1, respectively for GaN and helium gas. We further tested the surrounding dielectric effect on nanowires by coating nanowires with SiO_2 as described in section 5.2.3. The theory predicts $\gamma = 0.18$ eV·nm assuming a relative dielectric constant value of 3.9 for SiO_2. The experimental value, shown in Figure 5-8, is $\gamma = 0.310 \pm 0.083$ eV·nm, which is larger than the calculated value of 0.18 eV·nm. This disagreement might be due to the quality of the SiO_2 coating around the nanowire and its relative dielectric constant value. However, the trend of decreasing γ slope with decreasing dielectric mismatch between the nanowire and the surrounding dielectric is correct. We can predict what the dielectric constant of the surrounding dielectric should be, assuming that the fitting to the experimental data is reliable and the theory is correct. The fitting value, $\gamma = 0.310$ eV·nm, corresponds to the dielectric constant value of about 2.6. This low dielectric constant value indicates that the SiO_2 coating around the nanowire is not very dense.

We now discuss the size-independent transport data. Both the suspended nanowire and the SiO_2 coated nanowire seem to have a second transport channel independent of the nanowire radius. The activation energy, E_{a1}, is independent of the nanowire radius as shown in Figures 5-6 and 5-8, respectively, for the suspended nanowire and SiO_2 coated nanowire. We attribute this behavior to the impurity band conduction in which carriers conduct within the impurity band without being ionized into the conduction band.

5.3.3 Hopping Conduction in GaN Nanowires

There have been a few reports of variable-range hopping conduction in the nanowires contacted with the focused-ion-beam (FIB) technique [95, 96]. The FIB-induced amorphization in the nanowires was shown as the cause of the variable-range hopping conduction in references [95, 96]. Here we present results showing that nanowires without any apparent damage to the crystalline structure also display variable-range hopping. We speculate that the random distribution of impurity atoms in the semiconductor nanowire creates an effect related to a disordered crystal. In a disordered crystal, the energy of localized states is spread over a wide range. The nearest neigh-

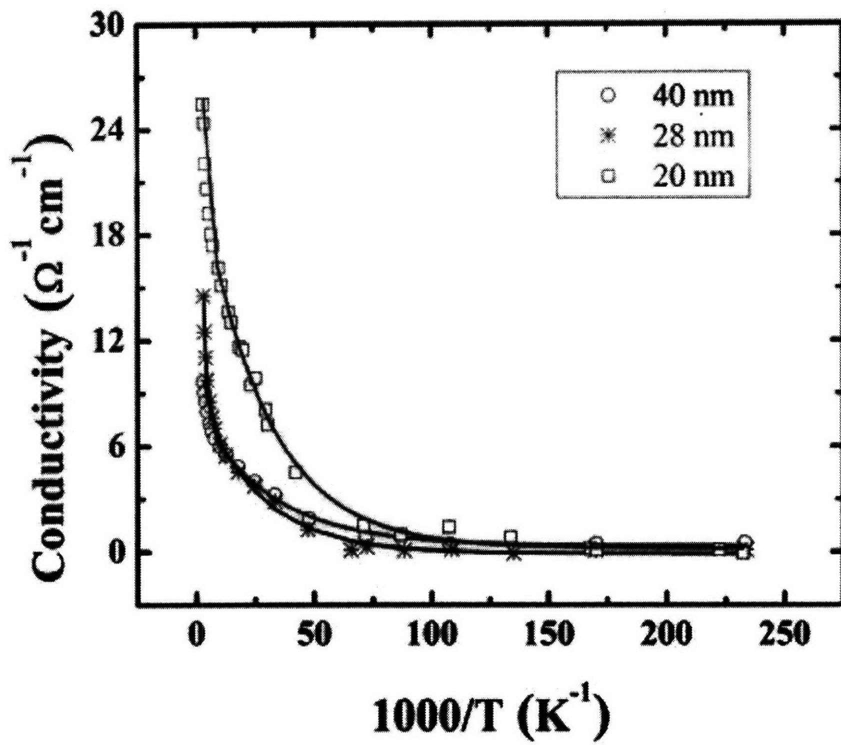


Figure 5-5: The conductivity versus 1000/T for suspended nanowires with 20, 28, and 40 nm diameters. The points represent experimental data while the lines represent fits over the entire temperature range.

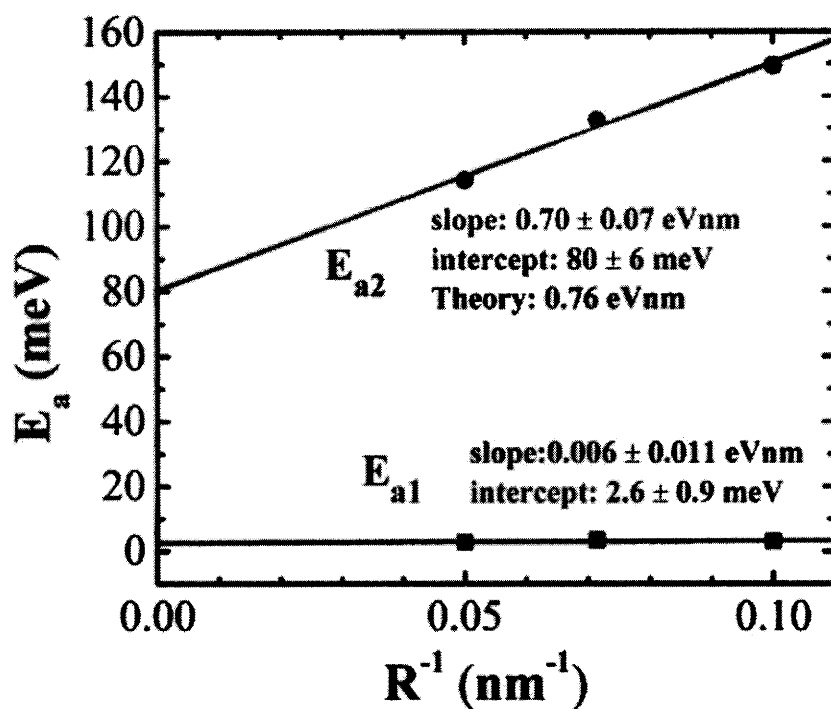


Figure 5-6: Activation energies for the suspended nanowires from the fit of the data given in Figure 5-5 as a function of inverse wire radius. The lines are linear fits to the experimental data.

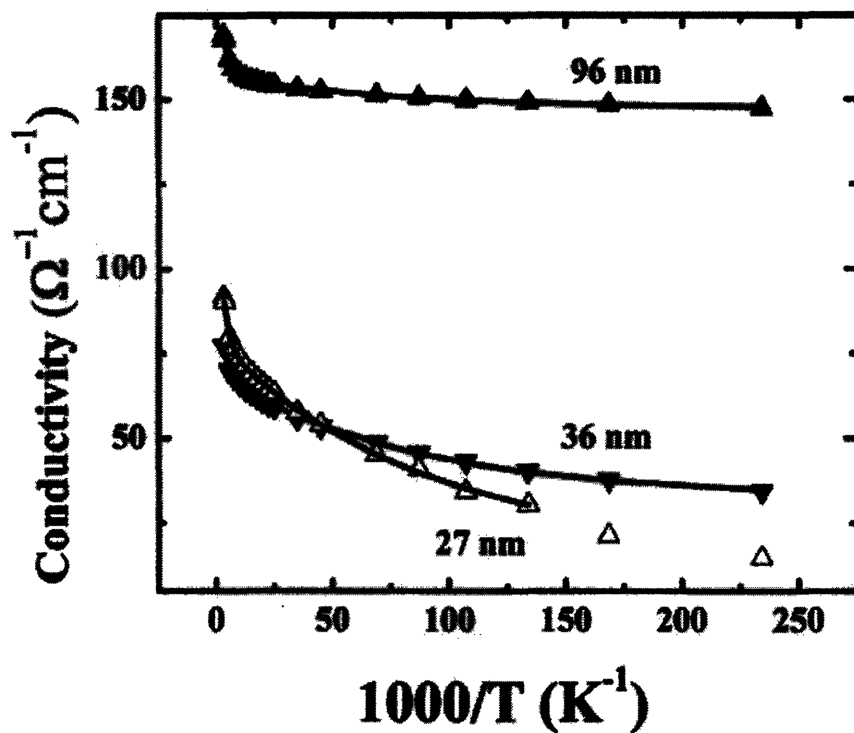


Figure 5-7: The conductivity versus 1000/T for the SiO_2 coated nanowires with 27, 36, and 96 nm diameters. The points represent experimental data while the lines represent fits over the entire temperature range. For the 27 nm diameter nanowire, the fitting does not include the last two data points because at these low temperature points a gap structure developed for this nanowire.

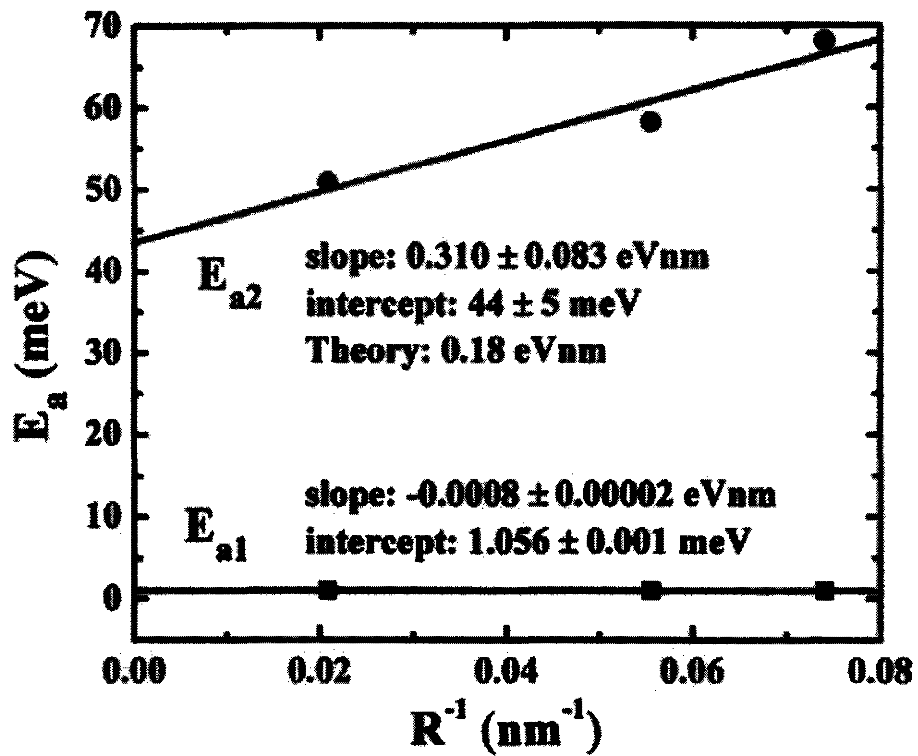


Figure 5-8: Activation energies for the SiO_2 coated nanowires from the fit of the data given in Figure 5-7 as a function of inverse wire radius. The lines are linear fits to the experimental data.

bor localized states can have widely different energy levels and the hopping to the nearest neighbors becomes costly and less likely. Thus hopping to further away but less energy-costly localized states dominates at low temperatures. In the case of Mott's variable-range hopping model, the low-temperature conductivity can be expressed as

$$\sigma = \sigma_0 \exp[-(T^*/T)^\nu] \tag{5.5}$$

where $T^* \approx 1/[\lambda^3 N(E_F) k_B]$ is Mott's characteristic temperature, with $\nu = 1/2$, $1/3$, or $1/4$ for 1D, 2D, or 3D hopping conduction, respectively. Here λ is the localization length, and $N(E_F)$ is the density of localized states at the Fermi level. The conductivity of the 60 nm diameter nanowire in the low temperature regime displayed a temperature dependence which can be described by the variable-range hopping conduction process. Fitting the low-temperature part of the 60 nm nanowire curve in Figure 5-9 to Eq. (5.5) yielded $\nu = 0.52 \pm 0.17$ as shown in Table 5.2. This value for ν is comparable to Mott's 1D variable-range hopping model. Our fitting result can also be explained by the possible existence of a soft Coulomb gap in the density of localized states near the Fermi level due to the long-range Coulomb interaction of the localized electrons as proposed by Efros and Shklovskii [99]. However, our low-temperature conductivity data did not corroborate the formation of the gap structure. The localization length can be estimated from the Mott's characteristic temperature, T^* , which was fitted to be 0.15±0.08°K as reported in Table 5.2. A plausible value for $N(E_F) = 7 \times 10^{20}$ eV$^{-1}\cdot$ cm^{-3} yielded an extremely large value, 50 nm, for the localization length, which is approximately the diameter of the nanowire, suggesting the occurrence of 1D hopping conduction in our nanowires.

Table 5.2: The fitting parameters to Eq.(5.5) for the nanowire with a diameter of 60 nm. Other nanowires did not display the clear characteristics of the variable-range hopping conduction.

T^*	ν	$\ln \sigma_0$	$\tilde{\chi}^2$
0.15±0.08	0.52±0.17	4.90±0.05	$4.3 \cdot 10^{-7}$

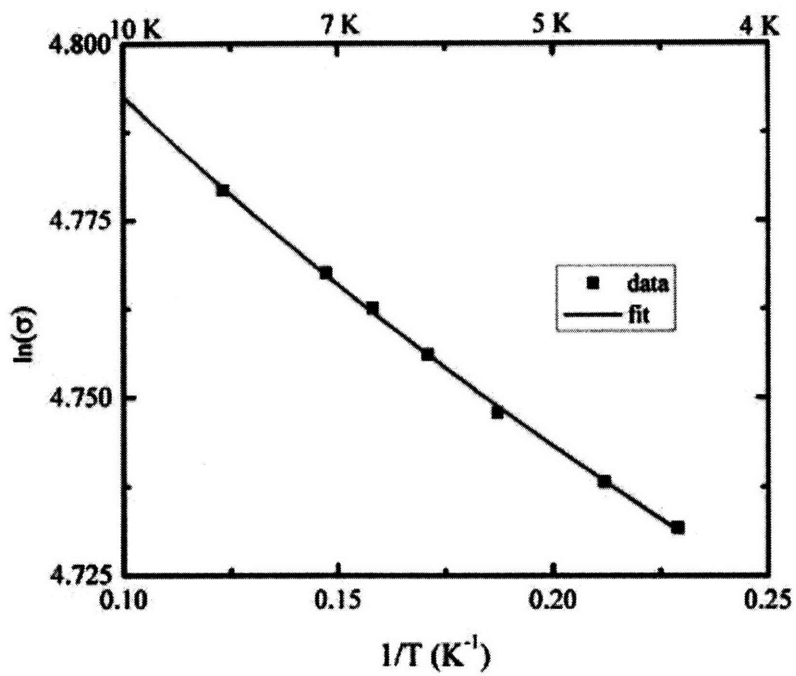


Figure 5-9: A plot of $\ln \sigma$ versus inverse temperature in the low temperature region for the 60 nm nanowire. The fitting parameters for the Mott hopping conduction are reported in Table 5.2.

5.4 Conclusions

We have studied the transport properties of GaN nanowires surrounded by a dielectric medium. In traditional bulk semiconductor based devices, electrical transport properties are not determined by the surrounding dielectric medium or the size of the device. However, in semiconducting nanowire devices, we found that the electrical transport properties are significantly modified by the presence of the surrounding dielectric medium and the size of the nanowire. Two sets of impurity ionization energies were found. The first impurity ionization energy was shallow and did not depend on the radius of the nanowires measured, while the second impurity ionization energy displayed the inverse radius dependence. We speculate that there exist two conduction paths for the nanowires, namely the core and the surface of the nanowires. Since impurities tend to segregate to the surface of the nanowire [100], we imagine that the impurities form an impurity band at the surface of the nanowire and charge carriers conduct within the impurity band without being ionized into the conduction band, and therefore the conductivity activation energy is shallow and independent of the nanowire radius. On the other hand, the impurities at the core of the nanowire do not form an impurity band and supply the carriers into the conduction band and this process requires an ionization energy, which is enhanced by the dielectric confinement and depends on the nanowire radius. This new observation suggests that, when designing nanoscale devices, special attention should be paid to the dielectric medium since the electrical properties can be modified significantly by the surrounding dielectric. We also found that nanowires can be used to study transport phenomena in a one-dimensional disordered system since variable-range hopping conduction was observed in our nanowires.

Chapter 6

Conclusions and Future Directions

6.1 Conclusions

Surfaces are often ignored in modeling the physical properties of bulk solids but play a major role in explaining the physical properties of nanostructures. Therefore a detailed and systematic investigation of the role of surfaces in determining the electrical properties of nanowires is essential for nanowire devices. This thesis presents a systematic experimental study of the significant role surfaces play in the electrical properties of GaN nanowires and provides the theoretical background to understand our results.

GaN nanowires were grown in house by the hydride vapor phase epitaxy (HVPE) or the chemical vapor deposition (CVD) methods. Both HVPE and CVD methods exploited the vapor-liquid-solid (VLS) growth mechanism [25] using Ni catalyst nanoparticles. TEM and XRD studies indicate that both HVPE and CVD grown GaN nanowires exhibit the wurtzite single crystal structure, which is the more common crystal structure for GaN than the zincblende crystal structure. We tried both nickel and gold nanoparticles as catalysts in both the HVPE and CVD growth methods and found that only Ni catalyst nanoparticles promoted GaN nanowire growth, possibly due to the low solubility of both Ga and N in gold. We were able to grow the HVPE GaN nanowires epitaxially on a c-plane sapphire substrate. Control over the nanowire growth is important because many materials characteristics depend on the

crystal orientation. Ni catalyst nanoparticles were rarely found at the tip of either the HVPE or CVD grown nanowires. This absence of a catalyst nanoparticle remaining at the tip of our nanowires contradicts the VLS growth mechanism and might indicate the incorporation of Ni in our nanowires. All the GaN nanowires that were grown were n-type semiconductors and had a considerable amount of impurities in them as indicated by transconductance measurements. In order to identify the impurities and defects in our GaN nanowires, we tried energy-dispersive x-ray spectroscopy (EDS) on both the HVPE and the CVD grown GaN nanowires. Within the detection limit of EDS (0.5 *at.* %), we did not find any particular foreign element, such as Ni, in our nanowires. These characterization results justified the important fundamental assumptions and provided valuable information for modeling and understanding the electrical transport properties of GaN nanowires.

GaN nanowire field-effect transistors (FET) were fabricated on top of a dielectric insulator (Figure 2-2(b)) to study the device characteristics along with the materials characteristics. The fabrication of nanowire FETs requires many steps of carefully designed semiconductor processing. Once the nanowire devices were fabricated, the devices were handled with care to prevent the destruction of the nanowire devices due to electrostatic discharge. A method and a procedure for preventing the burnout of nanowires by electrostatic discharge was developed. These fabrication techniques and the methods developed in this thesis are general and applicable to any nanostructured devices.

We were able to form ohmic contacts to GaN nanowires by removing both the polymers left from the lithographic process and the amorphous oxide layer. A Schottky barrier normally forms at the metal-semiconductor interface. However, the high doping level ($\sim 10^{19}$ cm^{-3}) present in our nanowires reduces the space charge region and allows the carriers to tunnel through a thin barrier and thus ohmic contact is formed. An average specific contact resistivity value of $1{\cdot}10^{-5}$ $\Omega{\cdot}$cm^2 was achieved for CVD grown GaN nanowires. Our contact resistivity value is a several times better than the values reported by others [75]. The capability to form ohmic contacts to nanowires is essential not only for the performance of nanoelectronic devices but also

for obtaining the electrical properties of nanowires.

A field effect mobility value of $\sim$ 18 cm^2/V-s was measured for the CVD GaN nanowire. This value is one order of magnitude smaller than the reported electron Hall mobility value of 140 cm^2/V-s obtained for bulk GaN with a similar doping concentration [101]. We note here that the field effect mobility is supposed to be a few times smaller than the Hall mobility because of the extra scattering from the surface conduction channel in FET devices. This reduced mobility for our GaN nanowire is most likely due to the reduced mobility in impurity band conduction at the surface of our GaN nanowires under an applied gate bias. Photoluminescence measurements were performed on both HVPE and CVD grown GaN nanowires at room temperature. A redshift of the near-band-edge emission was observed in both HVPE and CVD grown GaN nanowires. This redshift indicated that a band renormalization was taking place, due to heavy concentration of impurities in our GaN nanowires. An enhanced relative intensity of the broadband yellow luminescence has been also observed in CVD grown GaN nanowires which have a smaller average diameter than the HVPE grown nanowires. This PL data supports the model of deep-level luminescence originating from surface states because an enhanced surface-to-volume ratio in smaller diameter nanowires would increase the relative intensity of the emission from surface states [71]. Insights gained from these experiments can provide new ideas on how to improve the performance of nanoelectronic devices and and eventually lead to a new breed of devices.

Systematic transport measurements were carried out for CVD grown GaN nanowires as a function of temperature, wire radius, and surrounding dielectric. In order to test the effect of the surrounding dielectric medium, nanowires with three different surrounding configurations were prepared. Nanowires are either lying on the SiO_2/Si substrate, freely suspended between the metal contacts, or embedded in SiO_2. Conductivity measurements identified two separate electrical conduction channels in our CVD grown GaN nanowires. Two conduction channels are due to the core and the surface of the nanowire. The conduction in the core of the nanowire depends on the nanowire radius and the conduction in the surface of the nanowire does not show a

radius dependence. The observed size-dependent conduction is shown to be due to the mismatch between the dielectric constants of the nanowire and its surroundings. As we increase the dielectric mismatch between the nanowire and the surrounding dielectric, an increasing dependence of the donor ionization energy on the inverse radius is observed. The dependence coefficient γ increases from 0.31 ± 0.08 eV·nm to 0.70 ± 0.07 eV·nm as the surrounding dielectric constant decreases from 3.9 (SiO_2) to 1 (He gas). The size-independent conduction is attributed to impurity band conduction at the surface of GaN nanowires. We speculate that the surface of the nanowire is degenerately doped with impurities because impurities tend to segregate to the surface [100]. These impurities at the surface form an impurity band which provides a channel for impurity band conduction. This impurity band conduction does not need carriers to be ionized into the conduction band and is therefore independent of the nanowire radius. On the other hand, the impurities in the core of our nanowires contribute to the conduction by donating carriers to the conduction band. Therefore the impurity ionization energy depends on nanowire radius.

Recently, semiconducting nanowires are being considered for a wide range of applications and have been drawing considerable research interest. Therefore a detailed study of the electrical properties of nanowires are timely and important. Furthermore, analysis of the surrounding dielectric effect on the transport properties of GaN nanowires is very much relevant because any nanowire-based device would typically have a dielectric mismatch with its surrounding medium. Our work is the first experimental research to report on a size-dependent conductivity due to the dielectric confinement effect.

6.2 Future Directions

An accurate chemical analysis of grown nanowires would immensely benefit the growth quality of nanowires paying attention to the specific growth mechanism that was used. For bulk materials, secondary ion mass spectrometry (SIMS) is typically used to identify the impurities in the materials, and there exists a report of applying this

technique to identify the impurities in semiconducting nanowires [69]. The drawback of this measurement method is that it requires a high concentration of nanowires and has a poor spatial resolution. An alternative method is the LEAPT (local electrode atom probe tomography) which tears atoms away from the length of the nanowire starting from the tip of the nanowire to the base of the nanowire to construct a 3-dimensional chemical analysis of the nanowire [70, 102]. However, the difficulty with this method is that this technique requires a certain alignment of the nanowires, an array of the nanowires which are well separated from each other and vertically planted on the substrate. The as-grown GaN nanowires usually tend to grow densely over the entire region of the growth substrate, and this alignment is not suitable for the LEAPT technique. Also for device applications of the nanowires, the capability to grow a regular array of nanowires would be very useful for device integration. Alternatively a post-growth assembly technique can be used for the device integration of the nanowires. These techniques include the dielectrophoretic method [20], the fluidic method [103], and the Langmuir-Blodgett method [104].

As we have seen in this thesis, the surface plays an increasingly important role as the surface-to-volume ratio becomes significant in our nanowires. Therefore an experimental tool to monitor the electronic states at the surface of nanostructures would be necessary to study nanostructures. Electron spin resonance (ESR) spectroscopy can detect chemical species with one or more unpaired electrons and could be useful for studying the surface states of GaN nanowires. Recently there has been a report of applying ESR techniques to study defects in Si nanowires [105]. These defects, which are identified at the Si/SiO_2 interface and the SiO_2 shell, are shown to be eliminated by hydrogen passivation. ESR measurements can also be used to study the dielectric confinement or quantum confinement effect since it can measure the hyperfine splitting, which is proportional to the modulus squared of the ground state wavefunction on the impurity atom, and is therefore expected to be enhanced as the ground state wavefunction is confined dielectrically. Our initial photoluminescence measurements have indicated the presence of a broad sub-bandgap luminescence associated with defect states. The further systematic study of the photoluminescence as a function

of wire diameter would be of great interest.

In order to improve the nanostructured device performance, we need to consider the effect from the surrounding dielectric, surface states, and impurites. Semiconducting nanowires can be embedded in the dielectric material rather than be on top of a dielectric insulator. The embedded-nanowire is expected to show an increase in capacitance by about a factor of two compared to twice that of the non-embedded nanowire. The electric field distribution around the nanowire is also more favorable for the embedded-nanowire configuration than that of the non-embedded nanowire configuration since the breakdown field of the gate oxide is reached at a much lower gate bias for the non-embedded-nanowire configuration than for the embedded-nanowire configuration. Therefore, the embedded-nanowire configuration enhances the gate control of the carrier density inside the nanowire. Lowering the background doping level during the growth step will also result in a reduced scattering of the carriers from the charged donors. Impurities are expected to segregate to the surface of the nanowire and to form a complex with the dangling bonds at the surface [100]. The passivation of the surface can neutralize the impurities and reduce the scattering from the surface.

Core/shell heterostructures should be an important direction of future study. It has been reported that core/shell heterostructures can be exploited to enhance the mobility of carriers in nanowires by reducing the scattering from the charged impurities [106]. The core/shell heterostructure consists of a narrow band gap semiconducting nanowire for the core and a wide band gap material as the cladding layer which is epitaxially grown on the core. This heterostructure reduces the electron scattering from the surface by confining the electrons in the core and also by passivating the dangling bonds at the surface of the core. This type of core/shell structure should find applications not only for use in high mobility FETs but also in high efficiency light-emitting devices.

Bibliography

[1] Olaf Wunnicke. Gate capacitance of back-gated nanowire field-effect transistors. *Applied Physics Letters*, 89(8):083102, 2006.

[2] G. Seryogin, I. Shalish, W. Moberlychan, and V. Narayanamurti. Catalytic hydride vapour phase epitaxy growth of GaN nanowires. *Nanotechnology*, 16(10):2342–2345, 2005.

[3] Hiroshi Harima. Properties of GaN and related compounds studied by means of raman scattering. *Journal of Physics: Condensed Matter*, 14(38):R967–R993, 2002.

[4] J. Petalas, S. Logothetidis, S. Boultadakis, M. Alouani, and J. M. Wills. Optical and electronic-structure study of cubic and hexagonal GaN thin films. *Phys. Rev. B*, 52(11):8082–8091, Sep 1995.

[5] K. v. Klitzing, G. Dorda, and M. Pepper. New method for high-accuracy determination of the fine-structure constant based on quantized hall resistance. *Phys. Rev. Lett.*, 45(6):494–497, Aug 1980.

[6] Mark A. Reed. Quantum dots: nanotechnologists can now confine electrons to pointlike structures, such designer atoms may lead to new electronic and optical devices. *Scientific American*, 268(1):118–123, 1993.

[7] M. A. Kastner. Artificial atoms. *Physics Today*, 46:24, 1993.

[8] R. C. Ashoori. Electrons in artificial atoms. *Nature*, 379(6564):413–419, 1996.

[9] Sander J. Tans, Michel H. Devoret, Hongjie Dai, Andreas Thess, Richard E. Smalley, L. J. Geerligs, and Cees Dekker. Individual single-wall carbon nanotubes as quantum wires. *Nature*, 386(6624):474–477, 1997.

[10] Marc Bockrath, David H. Cobden, Paul L. McEuen, Nasreen G. Chopra, A. Zettl, Andreas Thess, and R. E. Smalley. Single-Electron Transport in Ropes of Carbon Nanotubes. *Science*, 275(5308):1922–1925, 1997.

[11] Danny Porath and Oded Millo. Single electron tunneling and level spectroscopy of isolated c[sub 60] molecules. *Journal of Applied Physics*, 81(5):2241–2244, 1997.

[12] Sumio Iijima. Helical microtubules of graphitic carbon. *Nature*, 354(6348):56–58, 1991.

[13] Wenjie Liang, Marc Bockrath, Dolores Bozovic, Jason H. Hafner, M. Tinkham, and Hongkun Park. Fabry - perot interference in a nanotube electron waveguide. *Nature*, 411(6838):665–669, 2001.

[14] Jing Kong, Erhan Yenilmez, Thomas W. Tombler, Woong Kim, Hongjie Dai, Robert B. Laughlin, Lei Liu, C. S. Jayanthi, and S. Y. Wu. Quantum interference and ballistic transmission in nanotube electron waveguides. *Phys. Rev. Lett.*, 87(10):106801, Aug 2001.

[15] Marc Bockrath, David H. Cobden, Jia Lu, Andrew G. Rinzler, Richard E. Smalley, Leon Balents, and Paul L. McEuen. Luttinger-liquid behaviour in carbon nanotubes. *Nature*, 397(6720):598–601, 1999.

[16] Teri Wang Odom, Jin-Lin Huang, Philip Kim, and Charles M. Lieber. Atomic structure and electronic properties of single-walled carbon nanotubes. *Nature*, 391(6662):62–64, 1998.

[17] Jeroen W. G. Wilder, Liesbeth C. Venema, Andrew G. Rinzler, Richard E. Smalley, and Cees Dekker. Electronic structure of atomically resolved carbon nanotubes. *Nature*, 391(6662):59–62, 1998.

[18] Y. Cui, X. Duan, J. Hu, and C.M. Lieber. Doping and electrical transport in silicon nanowires. *Journal of Physical Chemistry B*, 104(22):5213–5216, 2000.

[19] Eric W. Wong, Paul E. Sheehan, and Charles M. Lieber. Nanobeam mechanics: Elasticity, strength, and toughness of nanorods and nanotubes. *Science*, 277(5334):1971–1975, 1997.

[20] Xiangfeng Duan, Yu Huang, Yi Cui, Jianfang Wang, and Charles M. Lieber. Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices. *Nature*, 409(6816):66–69, 2001.

[21] Michael H. Huang, Samuel Mao, Henning Feick, Haoquan Yan, Yiying Wu, Hannes Kind, Eicke Weber, Richard Russo, and Peidong Yang. Room-temperature ultraviolet nanowire nanolasers. *Science*, 292(5523):1897–1899, 2001.

[22] J. Heremans and C. M. Thrush. Thermoelectric power of bismuth nanowires. *Phys. Rev. B*, 59(19):12579–12583, May 1999.

[23] Yu-Ming Lin, Xiangzhong Sun, and M. S. Dresselhaus1, 2. Theoretical investigation of thermoelectric transport properties of cylindrical Bi nanowires. *Phys. Rev. B*, 62(7):4610–4623, Aug 2000.

[24] Joseph P. Heremans, Christopher M. Thrush, Donald T. Morelli, and Ming-Cheng Wu. Thermoelectric power of bismuth nanocomposites. *Phys. Rev. Lett.*, 88(21):216801, May 2002.

[25] R. S. Wagner and W. C. ellis. Vapor-solid-growth mechanism of single crystal growth. *Applied Physics Letters*, 4:89, 1964.

[26] R. S. Wagner. *Whisker Technology.* Wiley, New York, 1970.

[27] E. I. Givargizov. Fundamental aspects of vls growth. *Journal of Crystal Growth*, 31:20–30, 1975.

[28] J. Kikkawa, Y. Ohno, and S. Takeda. Growth rate of silicon nanowires. *Applied Physics Letters*, 86(12):123109, 2005.

[29] Teh Y. Tan, Na Li, and Ulrich Gosele. Is there a thermodynamic size limit of nanowires grown by the vapor-liquid-solid process? *Applied Physics Letters*, 83(6):1199–1201, 2003.

[30] Y. Wu, Y. Cui, L. Huynh, C.J. Barrelet, D.C. Bell, and C.M. Lieber. Controlled growth and structures of molecular-scale silicon nanowires. *Nano Letters*, 4(3):433–436, 2004.

[31] S. Kodambaka, J. Tersoff, M. C. Reuter, and F. M. Ross. Germanium Nanowire Growth Below the Eutectic Temperature. *Science*, 316(5825):729–732, 2007.

[32] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and P. Avouris. Single- and multi-wall carbon nanotube field-effect transistors. *Applied Physics Letters*, 73(17):2447–2449, 1998. charge transfer model.

[33] Y. Huang, X. F. Duan, Y. Cui, and C. M. Lieber. Gallium nitride nanowire nanodevices. *Nano Letters*, 2(2):101–104, 2002.

[34] Maja Krcmar, Wayne M. Saslow, and Andrew Zangwill. Electrostatics of conducting nanocylinders. *Journal of Applied Physics*, 93(6):3495–3500, 2003.

[35] D. Vashaee, A. Shakouri, J. Goldberger, T. Kuykendall, P. Pauzauskie, and P. D. Yang. Electrostatics of nanowire transistors with triangular cross sections. *Journal of Applied Physics*, 99(5), 2006.

[36] M Buttiker. Capacitance, admittance, and rectification properties of small conductors. *Journal of Physics: Condensed Matter*, 5(50):9361–9378, 1993.

[37] Kenji Natori. The capacitance of microstructures. *Journal of Applied Physics*, 78(7):4543–4551, 1995.

[38] M. Lannoo. C. Delerue. *Nanostructures: theory and modelling.* Berlin ; New York : Springer, 2004.

[39] L. V. Keldysh. Excitons and polaritons in semiconductor/insulator quantum wells and superlattices. *Superlattices and Microstructures*, 4(4-5):637–642, 1988.

[40] C. Delerue, M. Lannoo, and G. Allan. Concept of dielectric constant for nanosized systems. *Phys. Rev. B*, 68(11):115411, Sep 2003.

[41] John David Jackson. *Classical Electrodynamics.* New York, Wiley, 1962.

[42] Masami Kumagai and Toshihide Takagahara. Excitonic and nonlinear-optical properties of dielectric quantum-well structures. *Phys. Rev. B*, 40(18):12359–12381, Dec 1989.

[43] C. J. F. B´ottcher. *Theory of Electric Polarization.* Amsterdam, New York, Elsevier Scientific Pub. Co., 1973.

[44] D. G. Thomas and J. J. Hopfield. Exciton spectrum of cadmium sulfide. *Phys. Rev.*, 116(3):573–582, Nov 1959.

[45] J. J. Hopfdeld. Fine structure in the optical absorption edge of anisotropic crystals. *Journal of Physics and Chemistry of Solids*, 15(1-2):97–107, 1960.

[46] G. Ramirez-Flores, H. Navarro-Contreras, A. Lastras-Martínez, R. C. Powell, and J. E. Greene. Temperature-dependent optical band gap of the metastable zinc-blende structure β-GaN. *Phys. Rev. B*, 50(12):8433–8438, Sep 1994.

[47] H. Okumura, S. Yoshida, and T. Okahisa. Optical properties near the band gap on hexagonal and cubic GaN. *Applied Physics Letters*, 64(22):2997–2999, 1994.

[48] R. C. Powell, N.-E. Lee, Y.-W. Kim, and J. E. Greene. Heteroepitaxial wurtzite and zinc-blende structure GaN grown by reactive-ion molecular-beam epitaxy: Growth kinetics, microstructure, and properties. *Journal of Applied Physics*, 73(1):189–204, 1993.

[49] Z. Sitar, M. J. Paisley, J. Ruan, J. W. Choyke, and R. F. Davis. Luminescence and lattice parameter of cubic gallium nitride. *Journal of Materials Science Letters*, 11(5):261–262, 1992.

[50] S. Strite, J. Ruan, Z. Li, A. Salvador, H. Chen, David J. Smith, W. J. Choyke, and H. Morkoc. An investigation of the properties of cubic GaN grown on GaAs by plasma-assisted molecular-beam epitaxy. *Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures*, 9(4):1924–1929, 1991.

[51] Gerhard Fasol Shuji Nakamura, Stephen Pearton. *The blue laser diode: the complete story.* Berlin; New York: Springer, 2000.

[52] D. Volm, K. Oettinger, T. Streibl, D. Kovalev, M. Ben-Chorin, J. Diener, B. K. Meyer, J. Majewski, L. Eckey, A. Hoffmann, H. Amano, I. Akasaki, K. Hiramatsu, and T. Detchprohm. Exciton fine structure in undoped GaN epitaxial films. *Phys. Rev. B*, 53(24):16543–16550, Jun 1996.

[53] R. Dingle, D. D. Sell, S. E. Stokowski, and M. Ilegems. Absorption, reflectance, and luminescence of GaN epitaxial layers. *Phys. Rev. B*, 4(4):1211–1218, Aug 1971.

[54] B. Monemar. Fundamental energy gap of GaN from photoluminescence excitation spectra. *Phys. Rev. B*, 10(2):676–681, Jul 1974.

[55] K. Pakula, A. Wysmolek, K. P. Korona, J. M. Baranowski, R. Stepniewski, I. Grzegory, M. Bockowski, J. Jun, S. Krukowski, M. Wroblewski, and S. Porowski. Luminescence and reflectivity in the exciton region of homoepitaxial GaN layers grown on GaN substrates. *Solid State Communications*, 97(11):919–922, 1996.

[56] J. A. Majewski, M. Städele, and P. Vogl. Electronic structure of biaxially strained wurtzite crystals GaN, AlN, and InN. *MRS Internet Journal on Nitride Semiconductor Research*, 1(30), 1996.

[57] Rodney Loudon. One-dimensional hydrogen atom. *American Journal of Physics*, 27(9):649–655, 1959.

[58] Garnett W. Bryant. Hydrogenic impurity states in quantum-well wires. *Phys. Rev. B*, 29(12):6632–6639, Jun 1984.

[59] Y. M. Niquet, A. Lherbier, N. H. Quang, M. V. Fernandez-Serra, X. Blase, and C. Delerue. Electronic structure of semiconductor nanowires. *Physical Review B (Condensed Matter and Materials Physics)*, 73(16):165319, 2006.

[60] Mamadou Diarra, Yann-Michel Niquet, Christophe Delerue, and Guy Allan. Ionization energy of donor and acceptor impurities in semiconductor nanowires: Importance of dielectric confinement. *Physical Review B (Condensed Matter and Materials Physics)*, 75(4):045301, 2007.

[61] Thaddeus B. Massalski, editor. *Binary Alloy Phase Diagrams*, volume 1. ASM International, Materials Park, Ohio, 1990.

[62] P. L. Llewellyn, V. Chevrot, J. Ragai, O. Cerclier, J. Estienne, and F. Rouquerol. Preparation of reactive nickel oxide by the controlled thermolysis of hexahydrated nickel nitrate. *Solid State Ionics*, 101-103(Part 2):1293–1298, 1997.

[63] Tevye Kuykendall, Peter J. Pauzauskie, Yanfeng Zhang, Joshua Goldberger, Donald Sirbuly, Jonathan Denlinger, and Peidong Yang. Crystallographic alignment of high-density gallium nitride nanowire arrays. *Nat Mater*, 3(8):524–528, 2004.

[64] Y. Cao Y. Lan H. Li M. He C. Wang Z. Zhang Z. Qiao X. Chen, J. Li. Straight and smooth GaN nanowires. *Advanced Materials*, 12(19):1432–1434, 2000.

[65] D. Tham, C. Y. Nam, K. Byon, J. Kim, and J. E. Fischer. Applications of electron microscopy to the characterization of semiconductor nanowires. *Applied Physics A: Materials Science & Processing*, 85(3):227–231, 2006.

[66] J. C. Wang, S. Q. Feng, and D. P. Yu. High-quality GaN nanowires synthesized using a CVD approach. *Applied Physics A: Materials Science & Processing*, 75(6):691–693, 2002.

[67] H. Li, A. H. Chin, and M. K. Sunkara. Direction-dependent homoepitaxial growth of GaN nanowires. *Advanced Materials*, 18(2):216–220, 2006.

[68] N.J. Watkins and G.W. Wicks. Oxidation study of GaN using x-ray photoemission spectroscopy. *Applied Physics Letters*, 75(17):p2602 –, 19991025.

[69] Kok-Keong Lew, Ling Pan, Timothy E. Bogart, Sarah M. Dilts, Elizabeth C. Dickey, Joan M. Redwing, Yanfeng Wang, Marco Cabassi, Theresa S. Mayer, and Steven W. Novak. Structural and electrical properties of trimethylboron-doped silicon nanowires. *Applied Physics Letters*, 85(15):3101–3103, 2004.

[70] D.E. Perea, J.E. Allen, S.J. May, B.W. Wessels, D.N. Seidman, and L.J. Lauhon. Three-dimensional nanoscale composition mapping of semiconductor nanowires. *Nano Letters*, 6(2):181–185, 2006.

[71] Ilan Shalish, Henryk Temkin, and Venkatesh Narayanamurti. Size-dependent surface luminescence in ZnO nanowires. *Physical Review B (Condensed Matter and Materials Physics)*, 69(24):245401, 2004.

[72] J. M. Graybeal and M. R. Beasley. Localization and interaction effects in ultrathin amorphous superconducting films. *Phys. Rev. B*, 29(7):4167–4169, Apr 1984.

[73] M. Asif Khan Q. Chen J. W. Yang A. C. Schmitz, A. T. Ping and I. Adesida. Schottky barrier properties of various metals on n-type GaN. *Semicond. Sci. Technol.*, 11:1464–1467, 1996.

[74] A. LeR. Dawson and D. H. Ryan. Heat capacity of silver paint. *Review of Scientific Instruments*, 67(7):2648–2649, 1996.

[75] E. Stern, G. Cheng, M. P. Young, and M. A. Reed. Specific contact resistivity of nanowire devices. *Applied Physics Letters*, 88(5):053106–3, 2006.

[76] Philip McCord Morse and Herman Feshbach. *Methods of theoretical physics.* International series in pure and applied physics. McGraw-Hill, New York,, 1953. [by] Philip M. Morse [and] Herman Feshbach. illus. 24 cm.

[77] E. Stern, G. Cheng, E. Cimpoiasu, R. Klie, S. Guthrie, J. Klemic, I. Kretzschmar, E. Steinlauf, D. Turner-Evans, E. Broomfield, J. Hyland, R. Koudelka, T. Boone, M. Young, A. Sanders, R. Munden, T. Lee, D. Routenberg, and M. A. Reed. Electrical characterization of single GaN nanowires. *Nanotechnology*, 16(12):2941–2953, 2005.

[78] B. S. Simpkins, P. E. Pehrsson, and A. R. Laracuente. Electronic conduction in GaN nanowires. *Applied Physics Letters*, 88(7), 2006.

[79] J. Y. Li, L. An, C. G. Lu, and J. Liu. Conversion between hexagonal GaN and beta-Ga_2O_3 nanowires and their electrical transport properties. *Nano Letters*, 6(2):148–152, 2006.

[80] W. Gotz, N. M. Johnson, C. Chen, H. Liu, C. Kuo, and W. Imler. Activation energies of si donors in GaN. *Applied Physics Letters*, 68(22):3144–3146, 1996.

[81] B. C. Chung and M. Gershenzon. The influence of oxygen on the electrical and optical-properties of GaN crystals grown by metalorganic vapor-phase epitaxy. *Journal of Applied Physics*, 72(2):651–659, 1992.

[82] T. Mattila and R. M. Nieminen. Ab initio study of oxygen point defects in GaAs, GaN, and AlN. *Physical Review B*, 54(23):16676–16682, 1996.

[83] Jörg Neugebauer and Chris G. Van de Walle. Atomic geometry and electronic structure of native defects in GaN. *Phys. Rev. B*, 50(11):8067–8070, Sep 1994.

[84] Ann I. Persson, Magnus W. Larsson, Stig Stenstrom, B. Jonas Ohlsson, Lars Samuelson, and L. Reine Wallenberg. Solid-phase diffusion mechanism for GaAs nanowire growth. *Nat Mater*, 3(10):677–681, 2004.

[85] Justin D. Holmes, Keith P. Johnston, R. Christopher Doty, and Brian A. Korgel. Control of thickness and orientation of solution-grown silicon nanowires. *Science*, 287(5457):1471–1473, 2000.

[86] C. Thelander, T. Mrtensson, M. T. Bjork, B. J. Ohlsson, M. W. Larsson, L. R. Wallenberg, and L. Samuelson. Single-electron transistors in heterostructure nanowires. *Applied Physics Letters*, 83(10):2052–2054, 2003.

[87] C P T Svensson, W Seifert, M W Larsson, L R Wallenberg, J Stangl, G Bauer, and L Samuelson. Epitaxially grown GaP/$GaAs_{1-x}P_x$ / GaP double heterostructure nanowires for optical applications. *Nanotechnology*, 16(6):936–939, 2005.

[88] Lincoln J. Lauhon, Mark S. Gudiksen, Deli Wang, and Charles M. Lieber. Epitaxial core-shell and core-multishell nanowire heterostructures. *Nature*, 420(6911):57–61, 2002.

[89] Y. Li, J. Xiang, F. Qian, S. Gradecak, Y. Wu, H. Yan, D.A. Blom, and C.M. Lieber. Dopant-free GaN/AlN/AlGaN radial nanowire heterostructures as high electron mobility transistors. *Nano Letters*, 6(7):1468–1473, 2006.

[90] R. Calarco, M. Marso, T. Richter, A.I. Aykanat, R. Meijers, A. v.d.Hart, T. Stoica, and H. Luth. Size-dependent photoconductivity in mbe-grown GaN-nanowires. *Nano Letters*, 5(5):981–984, 2005.

[91] Chun-Wei Chen, Kuei-Hsien Chen, Ching-Hsing Shen, Abhijit Ganguly, Li-Chyong Chen, Jih-Jen Wu, Hui-I Wen, and Way-Faung Pong. Anomalous blueshift in emission spectra of ZnO nanorods with sizes beyond quantum confinement regime. *Applied Physics Letters*, 88(24):241905, 2006.

[92] Jing Kong, Nathan R. Franklin, Chongwu Zhou, Michael G. Chapline, Shu Peng, Kyeongjae Cho, and Hongjie Dai. Nanotube molecular wires as chemical sensors. *Science*, 287(5453):622–625, 2000.

[93] Fernando Patolsky, Gengfeng Zheng, Oliver Hayden, Melike Lakadamyali, Xiaowei Zhuang, and Charles M. Lieber. Electrical detection of single viruses. *PNAS*, 101(39):14017–14022, 2004.

[94] C.-X. Wang, B. Wang, Y.-H. Yang, and G.-W. Yang. Thermodynamic and kinetic size limit of nanowire growth. *Journal of Physical Chemistry B*, 109(20):9966–9969, 2005.

[95] C.Y. Nam, D. Tham, and J.E. Fischer. Disorder effects in focused-ion-beam-deposited Pt contacts on GaN nanowires. *Nano Letters*, 5(10):2029–2033, 2005.

[96] Yong-Jun Ma, Ze Zhang, Feng Zhou, Li Lu, Aizi Jin, and Changzhi Gu. Hopping conduction in single ZnO nanowires. *Nanotechnology*, 16(6):746–749, 2005.

[97] Karlheinz Seeger. *Semiconductor Physics*. Springer-Verlag, Berlin, Heidelberg, New York, 8th edition, 2002.

[98] Sir Nevill Mott. *Conduction in Non-Crystalline Materials*. Clarendon, Oxford, 1993.

[99] A L Efros and B I Shklovskii. Coulomb gap and low temperature conductivity of disordered systems. *Journal of Physics C: Solid State Physics*, 8(4):L49–L51, 1975.

[100] M. V. Fernandez-Serra, Ch. Adessi, and X. Blase. Surface segregation and backscattering in doped silicon nanowires. *Physical Review Letters*, 96(16):166805, 2006.

[101] D. L. Rode and D. K. Gaskill. Electron hall mobility of n-GaN. *Applied Physics Letters*, 66(15):1972–1973, 1995.

[102] D. E. Perea, J. L. Lensch, S. J. May, B. W. Wessels, and L. J. Lauhon. Composition analysis of single semiconductor nanowires using pulsed-laser atom probe tomography. *Applied Physics A: Materials Science & Processing*, 85(3):271–275, 2006.

[103] Y. Huang, X. F. Duan, Q. Q. Wei, and C. M. Lieber. Directed assembly of one-dimensional nanostructures into functional networks. *SCIENCE*, 291(5504):630–633, Jan 2001.

[104] D. Whang, S. Jin, Y. Wu, and C. M. Lieber. Large-scale hierarchical organization of nanowire arrays for integrated nanosystems. *NANO LETTERS*, 3(9):1255–1259, Sep 2003.

[105] A. Baumer, M. Stutzmann, M. S. Brandt, F. C.K. Au, and S. T. Lee. Paramagnetic defects of silicon nanowires. *Applied Physics Letters*, 85(6):943–945, 2004.

[106] Jie Xiang, Wei Lu, Yongjie Hu, Yue Wu, Hao Yan, and Charles M. Lieber. Ge/Si nanowire heterostructures as high-performance field-effect transistors. *Nature*, 441(7092):489–493, 2006.