An All-Digital Transmitter for Pulsed Ultra-Wideband Communication

by

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Abstract

Applications like sensor networks, medical monitoring, and asset tracking have led to a demand for energy-efficient and low-cost wireless transceivers. These types of applications typically require low effective data rates, thus providing an opportunity to employ simple modulation schemes and aggressive duty-cycling. Due to their inherently duty-cycled nature, pulse-based Ultra-Wideband (UWB) systems are amenable to low-power operation by shutting off circuitry during idle mode between pulses. Furthermore, the use of non-coherent UWB signaling greatly simplifies both transmitter and receiver implementations, offering additional energy savings.

This thesis presents an all-digital transmitter designed for a non-coherent pulsed-UWB system. By exploiting relaxed center frequency tolerances in non-coherent wideband communication, the transmitter synthesizes UWB pulses from an energy-efficient, single-ended digital ring oscillator. Dual capacitively-coupled digital power amplifiers (PAs) are used in tandem to generate bipolar phase modulated pulses for spectral scrambling purposes. By maintaining opposite common modes at the output of these PAs during idle mode (i.e. when no pulses are being transmitted), low frequency turn-on and turn-off transients typically associated with single-ended digital circuits driving single-ended antennas are attenuated by up to 12dB. Furthermore, four level digital pulse shaping is employed to attenuate RF sidelobes by up to 20dB. The resulting dual power amplifiers achieve FCC compliant operation in the 3.5, 4.0, and 4.5GHz IEEE 802.15.4a bands without the use of any off-chip filters or large passive components. The transmitter is fabricated in a 90nm CMOS process and requires a core area of $0.07mm^2$. The entirely digital architecture consumes zero static bias current, resulting in an energy efficiency of 17.5pJ/pulse at data rates up to 15.6Mbps.

Thesis Supervisor: Anantha P. Chandrakasan
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Chapter 1

Introduction

1.1 Background

The world-wide use of portable electronics has never been more prevalent than in today's society. With the consumer semiconductor market expected to grow from $58 billion in 2007 to $100 billion in 2012 at a compound annual growth rate (CAGR) of 12% [13], it is increasingly important to design portable electronics to have high performance, small form factors, and long battery life in order to stay competitive. As a result, much research and development efforts have been spent maximizing the performance and integration of portable electronics in power-constrained environments. However, for applications such as wireless sensor networks, medical monitoring, and asset tracking, the ultimate goal of maximizing performance is superseded by minimizing energy consumption, area, and cost [14, 15]. Typically in these types of energy-starved applications, the radio-frequency (RF) circuits dominate the overall energy budget. In order to maximize battery lifetime or minimize the required amount of energy harvesting, new and innovative design techniques are required to reduce the RF circuitry energy burden.

In 2002, the United States Federal Communications Commission (FCC) issued a First Order and Report permitting the development and operation of ultra-wideband (UWB) wireless communication devices operating in the 3.1-to-10.6 GHz range [16, 17]. According to the FCC, a signal is considered ultra-wideband if it has a -10dB

bandwidth 20% larger than its own center frequency. Alternatively, the signal's bandwidth must be greater than or equal to 500MHz. Since the Shannon channel capacity is directly related to bandwidth, UWB communication has the potential to acheive very high data rates.

Ultra-wideband is commissioned to be an overlay technology, such that it will not disrupt the operation of narrowband devices operating in the same frequency span. In fact, the average power spectral density (PSD) in the 3.1-to-10.6GHz UWB band is restricted to be less than -41.3dBm/MHz; this is equivalent to the FCC Part 15 limit for unintentional radiators such as personal computers. Due to concerns about interference with low signal-to-noise ratio (SNR) devices such as the global positioning system (GPS), the average PSD limit is further reduced in other frequency ranges, as shown in Figure 1-1.

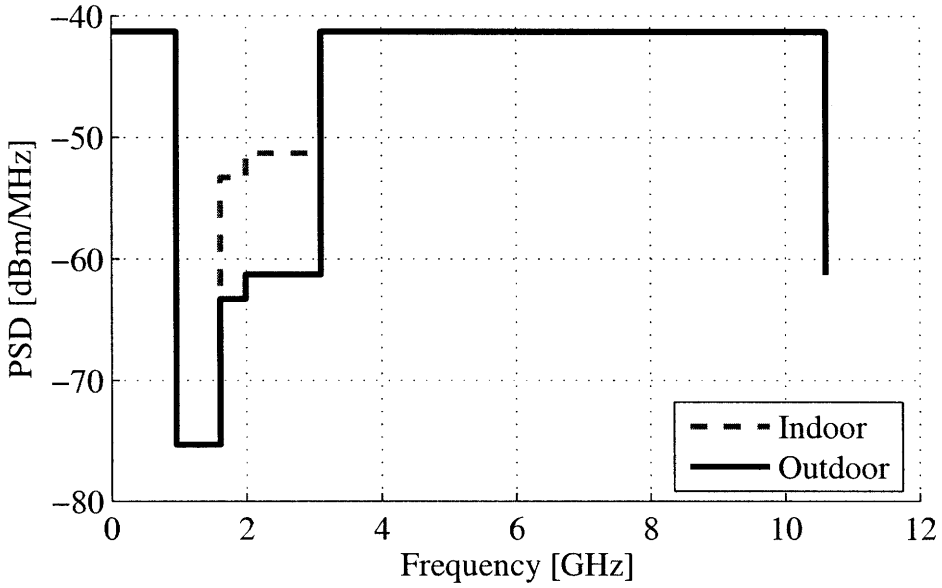


Figure 1-1: FCC mask restricting power spectral densities from 0-to-10.6GHz.

The resulting power limit constrains high data rate communication to a range of approximately 1-to-10m, which is appropriate for Wireless Personal Area Network (WPAN) and Body Area Network (BAN) applications. It is possible, however, to trade-off data rate and/or spectral efficiency for increased transmit distance and/or energy efficiency, which opens up UWB to several exciting potential applications.

For instance, applications such as miniaturized flying vehicles require communication distances upwards of 100m, while minimizing both energy consumption and weight due to limited payload carrying capacities [18]. As discussed throughout this thesis, leveraging the wide available bandwidth of UWB signaling can lead to the possibility of achieving small, energy efficient radios which can communicate at distances up to 100m.

1.2 UWB Standards, Proposals, and Communication Schemes

Since the 2002 FCC report did not restrict UWB signaling to any particular scheme, circuit and systems designers have the freedom to choose any type of implementation, provided the spectral masks are met. As a result, several very different techniques were proposed for standardization in the Institute of Electrical and Electronics Engineers (IEEE) 802.15.3a task group. After much deliberation, the task group consolidated the many submitted proposals into two separate proposals: one relying on Orthogonal Frequency Division Multiplexing (OFDM), and the other relying on pulse-based communication. Since the parties could not agree to further consolidation, the 802.15.3a task group was disbanded in 2006 and each technology sought standardization and development elsewhere.

1.2.1 MB-OFDM

The OFDM-based technology utilizes a carrier-based approach by modulating information onto 128 separate sub-carriers which, added together, create an ultra-wideband signal. Termed Multi-Band OFDM (MB-OFDM), this approach is spearheaded for standardization by the WiMedia Alliance, an International Organization for Standardization (ISO)-published offshoot of the disbanded IEEE 802.15.3a task group. The frequency plan consists of fourteen channels spaced by 528MHz and grouped into five separate subgroups, as shown in Figure 1-2. Channel hopping over

the three channels in each subgroup is implemented for robustness to narrowband interferers.

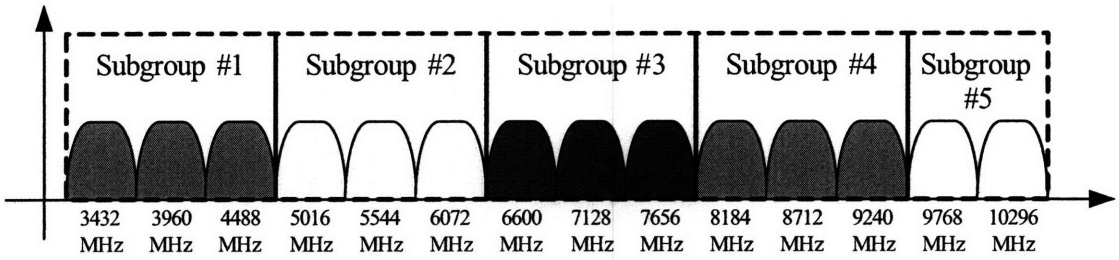


Figure 1-2: Frequency plan of the WiMedia Alliance MB-OFDM proposal.

WiMedia's promise of high transfer rates of at least 480Mbps has prompted the Bluetooth Special Interest Group (SIG) to select MB-OFDM as its next generation standard for sub-10m communication. With the Bluetooth market expected to break 1 billion products shipped by 2009 while growing at a CAGR of 40% up to 2011 [19], the future of MB-OFDM UWB technology appears to be bright.

One of the first published MB-OFDM RF transceivers was considered in 2005 [20]. Fabricated in a 0.13μm Complimentary Metal Oxide Semiconductor (CMOS) technology, it required three separate phase-locked loops in order to meet frequency hopping specifications. The chip achieved an overall power consumption of 105mW. Improvements in linearity, frequency switching times, and the of inclusions digital basebands were shown in [21, 22, 23, 24], though no significant improvements in power consumption were reported.

From these test chips, it is clear that the considerable complexity of MB-OFDM systems leads to power consumptions that are larger than desirable for most energy starved electronics. For this reason, MB-OFDM techniques are not given any further consideration in this thesis.[1]

[1]This is not to say MB-OFDM techniques are not amenable to low power solutions through clever implementation strategies. Rather, other UWB techniques (namely, pulsed-UWB) are inherently suited to fast duty cycling and low complexity architectures, as will be shown throughout this thesis.

1.2.2 IR-UWB

A promising alternative to MB-OFDM for implementing low-power UWB communication involves a time-domain Impulse Radio UWB (IR-UWB) approach [25]. With this technique, pulses of very short duration (on the order of 200ps to 2ns) are used to create inherently wideband signals capable of both transmitting digital data and providing ranging and localization information [26]. These wideband signals can be generated to lie directly in the band of interest, or can be generated at baseband and subsequently mixed-up to RF frequencies. Since the radiated pulse power is relatively low due to FCC regulations, IR-UWB receivers must operate at very low signal-to-noise ratios. Correlation and comparison operations are typically required to separate signal information from noise, even at low-to-medium transmission distances.

Although IR-UWB has a lower maximum anticipated data throughput and is often less robust to multi-path compared to MB-OFDM, the transmitter and receiver complexity can be decreased, thus allowing a significant reduction in energy consumption [27]. The lower anticipated power makes IR-UWB particularly suited for portable or energy-starved applications where battery life is of paramount importance. For instance, one of the first publications proposing a pulse-based UWB architecture which included modern semiconductor circuit-level considerations was presented in 2002 [28]. In stark contrast to MB-OFDM transceivers, this architecture targeted a 100kbps data rate with a 1mW power budget when duty-cycling most circuits between pulses.

IR-UWB is currently in the process of being standardized by the IEEE 802.15.4a group, specifically targeted for low data rate WPANs [29]. Touted as a potential next-generation physical (PHY) layer for Zigbee, IR-UWB can be seen as a complimentary technology to MB-OFDM UWB, where longer communication distances, lower power consumption, or ranging are key. Zigbee revenues amounted to $11 million in 2005, yet the market is expected to increase exponentially at a CAGR of 190% to reach $800 million by 2009 [30].

The frequency plan of the 802.15.4a proposal is split up into three main groups:

sub-GHz, low-band, and high-band. A compliant device should be capable of operating in at least one of the three bands. The sub-GHz band consists of only one channel centered at 499.2MHz, while the low- and high-bands contain three and eight channels, respectively. If operating in the low- or high-bands, the device must support the mandatory channel, as shown in Figure 1-3. The remaining channels are optional.

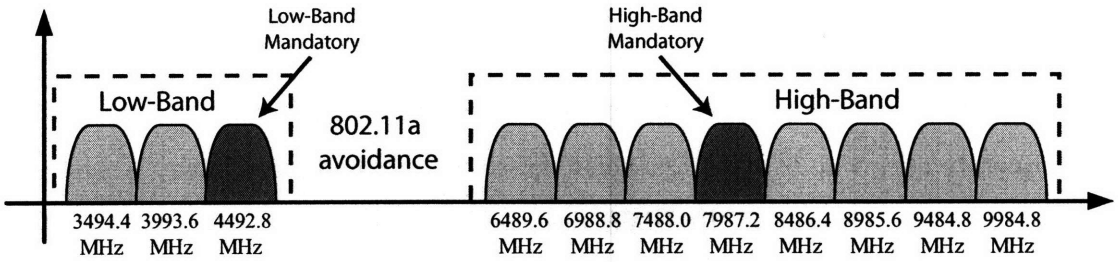


Figure 1-3: Frequency plan of the low- and upper-bands of the 802.15.4a task group proposal.

Note that there are no channels in the 5-to-6GHz range to avoid interference with the 802.11a/U-NII band. It should also be noted that the channel frequencies and spacings are different than those proposed in the WiMedia standard. In this case, the channels are spaced at integer multiples of 499.2MHz.

1.2.3 Coherency

There are two fundamentally different ways to demodulate data in carrier-based communication systems: coherent versus non-coherent demodulation. Coherent receivers typically lock the incoming carrier phase with a locally generated carrier or pilot tone, whereas non-coherent receivers discard phase information. For example, consider the non-coherent receiver shown in Figure 1-4. The incoming signal is amplified, squared, then integrated over a set window of time. The squaring and integrating operation does not consider phase, and is in fact equivalent to finding the *energy* of a signal in a given window of time. For this reason, this type of non-coherent receiver is called an energy-detecting receiver.

Non-coherent systems have a lower effective data rate for a given bit error rate (BER) compared to the coherent case, since the loss of phase information reduces the

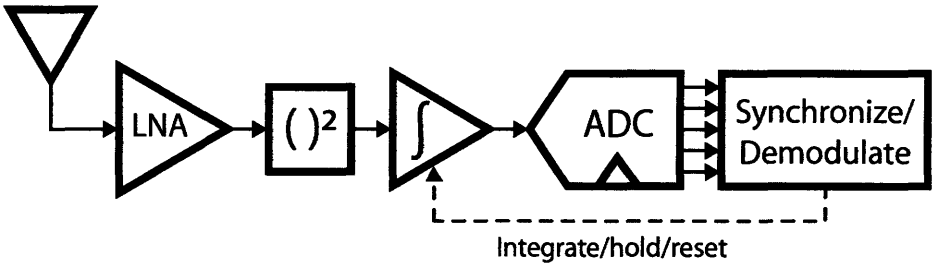


Figure 1-4: Block diagram of a non-coherent energy-detecting receiver.

number of potential signaling dimensions by one. This limits the types of modulation that can be used, and may result in decreased symbol distances in the constellation diagram.

However, since phase information is discarded, non-coherent systems do not require phase alignment between the transmitter and receiver. Thus, non-coherent receivers are only sensitive to variations in the transmitted *frequency*. If the fractional bandwidth of a system is large (as is the case for UWB), then the *absolute* transmitted frequency accuracy can be relatively low compared to narrowband systems. For this reason, non-coherent systems can employ simple architectures with relaxed frequency requirements, and often do not require the use of phase-locked loops (PLLs) or cordic blocks. If the decrease in performance can trade-off favorably with a decrease in energy consumption versus the coherent case, then a net improvement in energy efficiency is possible.

1.3 Previous Work

Since this thesis discusses the implementation of a pulse-based UWB transmitter, the scope of this section is limited to UWB pulse generators.

Ultra-wideband pulse generators can typically be distinguished using two sets of criteria:

1. *RF generation*: There are two different techniques used to synthesize UWB pulses at RF frequencies. The first technique involves mixing a baseband pulse with a local oscillator (LO) running at the desired RF center frequency. The

second technique involves generating UWB pulses to lie directly at the desired RF center frequency. In other words, the second technique does not use a local oscillator.

2. *Power amplification*: There are two different techniques used to amplify and interface pulsed signals with an antenna. The first technique involves using analog circuits biased in their linear region for small-signal amplification and balanced conversions. The second technique uses digital circuits to buffer pulses at the interface to the antenna.

1.3.1 Coherent Pulsed-UWB

This section will classify transmitter architectures into four different categories, using the aforementioned criteria as a guide. As a forewarning, it should be mentioned that it is sometimes difficult to make clear classifications, as some pulse generators use a combination of different techniques.

Traditional Small-Signal, Mixer-based Transmitters

In these types of architectures, baseband data is typically converted from the digital to analog domain and subsequently mixed with an LO. The output of the LO is then amplified by an analog power amplifier (PA), often biased as class A or class AB in order to meet linearity requirements. A simplified example architecture can be seen in Figure 1-5. The initial popularity of this technique stemmed mainly from the fact that similar techniques are well established in traditional narrowband radio design.

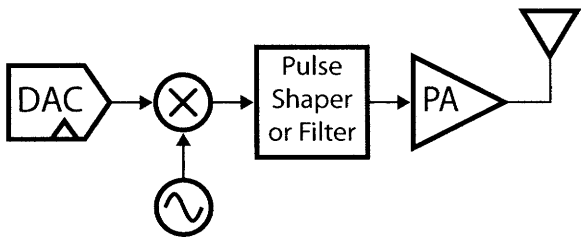


Figure 1-5: A traditional small-signal, mixer-based pulse generator architecture.

From a signaling point of view, this type of architecture is the most robust, as both phase and amplitude modulation are possible.[2] Pulse shaping, used to attenuate RF sidelobes in order to meet FCC spectral masks, is also easily achieved in these types of architectures by either shaping the baseband data, or the RF data before the PA. For instance, the transmitter considered in [4] employed approximate Gaussian pulse shaping in the mixer by utilizing the exponential response of bipolar transistors.

The transmitter considered in [31] operates in dual bands by simultaneously up-converting two data streams onto two separate RF carriers. This is made possible by a wide bandwidth power amplifier employing shunt peaking and inductive feedback. A similar design is shown in [32], however only one band is operated in at a time. The transmitter supports all of the 802.15.4a specifications and reduces the power consumption over [31] by aggressively duty-cycling the class A power amplifier.

LC-based Transmitters

LC-based transmitters use an LO to generate RF content, yet an explicit mixer is not necessarily required. For instance, a simple switch can either pass or block the LO output, thus effectively mixing the RF signal with a rectangular baseband pulse. As an example, the transmitter considered in [2] operates in a similar fashion to a superregenerative receiver; that is, the output of an LC oscillator is the transmitter output itself. A schematic is shown in Figure 1-6.

In this case a rectangular quenching pulse train acts as the baseband mixing signal. Like most oscillators, this circuit can be modeled as a second order system with poles in the right half portion of the s-plane.[3] It is well known that the oscillatory output of such systems grow exponentially in time until circuit non-linearities limit the output swing. This oscillation growth can be leveraged to employ simple pulse shaping.

[2]Note that in-phase and quadrature paths are often used to enable Quadrature Amplitude Modulation (QAM) for high data-rate communication.

[3]The s-plane is sometimes called the Laplace plane.

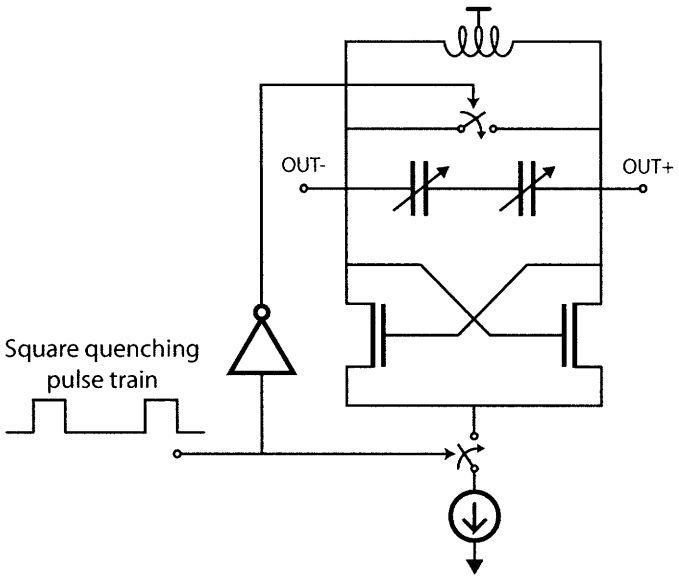


Figure 1-6: An LC-based transmitter.

Carrier-Less Transmitters

Carrier-less transmitters do not have an explicit local oscillator to mix baseband data up to RF. Instead, baseband data typically triggers a pulse generator to synthesize a pulse directly in the RF band of interest. One advantage over traditional mixer-based architectures is that the carrier frequency generation is inherently duty cycled; that is, RF energy is only generated when it is required. A disadvantage of this approach is that an integrated downconverting receiver typically cannot share the RF generation circuits and therefore must have a separate LO.

Implementation strategies typically involve generating pulses by combining edges of various delay elements, then amplifying the result using a power amplifier [5, 8]. Architectures that use delay lines to synthesize RF frequencies typically have half-RF cycles available at the output of each delay cell. By exploiting the fact that each half-RF cycle can be manipulated, simple pulse shaping schemes and differential-to-single-ended conversions are possible [6, 7, 33]. A popular architecture involves feeding half-RF cycles to alternating sides of a wideband balun, as shown in Figure 1-7. This architecture ensures there is close to zero DC content at the transmitter output, thus enabling clean Binary Phase-Shift Keying (BPSK) modulation.

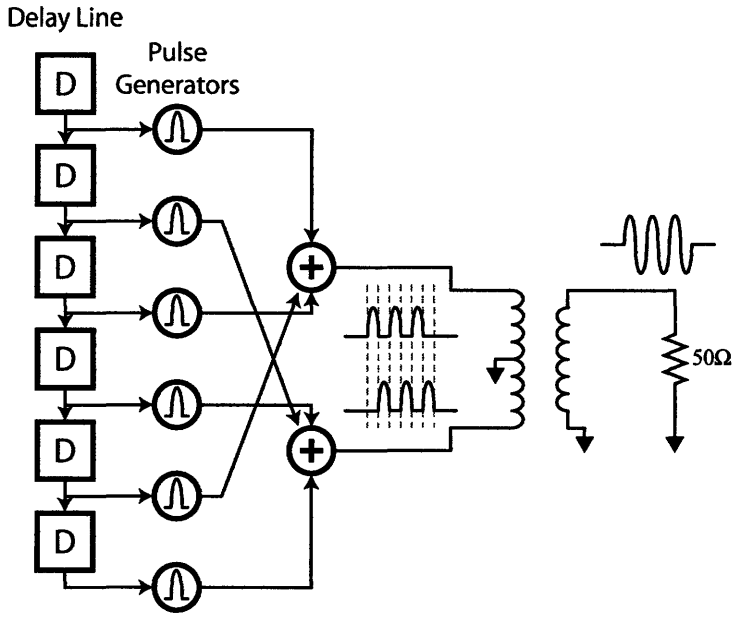


Figure 1-7: A carrier-less architecture employing a balun for zero-DC voltage pulse generation.

All-Digital Transmitters

All-digital pulse generators attempt to reduce the power consumption over their analog counterparts by eliminating large static currents required to bias transistors in their linear regions. Instead, digital static CMOS gates are used to generate high frequency rail-to-rail voltage swings. These digital architecture dissipate only CV^2f switching power and subthreshold leakage power.

A similar technique is popular in narrowband radio design, where linear power amplifiers are replaced by switched-mode power amplifiers. A major drawback of this approach is that constant-envelope modulation schemes must often be used, as switched-mode PAs have poor linearity and thus cannot support amplitude modulation techniques. Similarly, all-digital UWB transmitters are often restricted to phase and position modulations schemes only.

Pulses in all-digital transmitters can either be synthesized using carrier-less techniques, or by modulating the output of a digitally controlled oscillator (DCO). Examples of carrier-less techniques include the transmitters presented in [11, 34]. In these examples, UWB pulses are generated directly in the band of interest by NOR-

ing two delayed edges together, converting from single-to-differential, and applying the differential signal to a dipole antenna. Similarly, the transmitter considered in [35] generates pulses by combining inverter gate delays using NOR and NAND structures. Relying on uncalibrated gate delays, however, leads to significant deviations in frequency and bandwidth targets over process voltage and temperature (PVT) variation.

The transmitter considered in [10] generates pulses in a carrier-less fashion by combining output edges from a delay line. BPSK modulation is achieved by applying full-swing pulses to either input of a balun, as illustrated in Figure 1-8. However, a bandpass filter is required to reduce the low-frequency content typically associated with digital pulse generation driving a single-ended antenna. This issue is discussed further in Chapter 2.

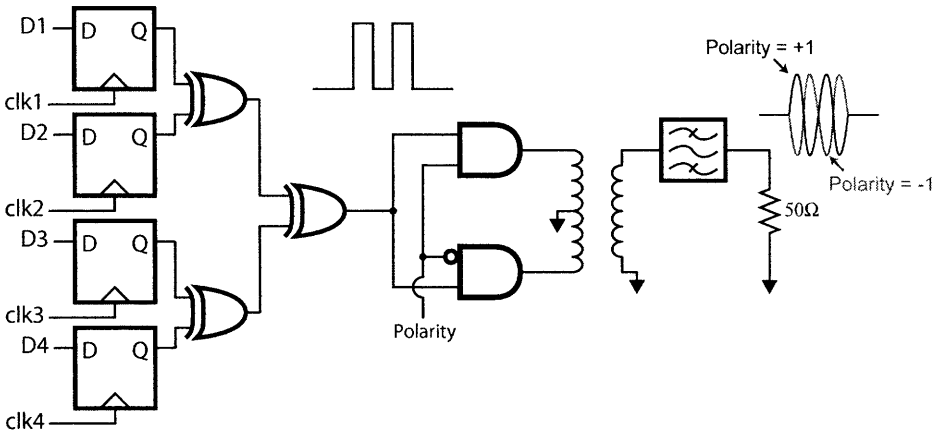


Figure 1-8: An all-digital architecture employing a balun for BPSK modulation.

The other technique to generate UWB pulses digitally is to modulate the output of a DCO. For instance, the transmitter considered in [36] generates pulses by directly modulating the output of a three-stage inverter-based ring oscillator. By utilizing the phases of an on-chip frequency divider, discrete two-level pulse shaping is employed. Since digital circuits are used in this architecture, reconfigurability and calibration are easily implemented.

1.3.2 Non-coherent Pulsed-UWB

It is well known that coherent IR-UWB systems suffer from significant multi-path fading. One method to capture and utilize many propagation paths is to include RAKE-based techniques [27]. This, however, requires high speed and power-hungry clocking, which is not suitable for energy-starved applications. An alternative approach to capturing multi-path effects is to use a non-coherent, energy-detection architecture [37]. In this technique, the incoming signal is squared, then integrated over a set window of time as discussed in section 1.2.3. If the integration time window is set to be larger than the width of the pulse, the energy of several propagation paths will be collected. Furthermore, the shape of the received pulse is no longer of concern to the receiver.[4]

Some of the first published non-coherent UWB transceivers incorporating energy detection techniques were presented in [38] and [39]. Pulses were generated by utilizing static digital logic similar to the technique found in [11], however, with the advantage of amplitude and phase control via an analog power amplifier. The receiver architecture included a digital baseband and is very similar to that shown in Figure 1-4, with eight integrators operating in parallel to shorten synchronization times. Measured results were shown in [40], and a total pulse generator power consumption of 12.9mW was reported.

One of the most common multiple access and modulation schemes for energy-detection-based IR-UWB is time-hopped (TH) Pulse Position Modulation (PPM), where logical values are indicated by the presence of pulses in user-specific windows of time. For deeply duty-cycled transceivers, it is often most convenient and energy-efficient to align PPM intervals closely in time. Unfortunately, this creates large spectral lines at integer multiples of the pulse repetition frequency (PRF), which can adversely affect the ability to meet FCC spectral masks without significant power backoff [41]. Although phase information is meaningless to energy-detection receivers, one method to eliminate such lines is to include random phase scrambling, typically

[4]The transmitter must still adhere to any pulse shape regulations to be standards-compliant.

in the form of BPSK.[5] This is discussed in further detail in Chapter 2.

The transmitter considered in [12] proposes a new phase modulation technique termed delay-based BPSK (DB-BPSK). Rather than using an area-expensive balun to invert pulses, a digitally-generated pulse is simply delayed by half of an RF cycle to create a pseudo 180° phase shift. It has been shown that DB-BPSK has the same spectral smoothing effect as pure BPSK in the frequency range of interest [42]. The non-coherent operation relaxes center frequency tolerances, lending this technique to a purely digital implementation employing digital delay lines. The transmitter achieves an excellent energy efficiency of 47pJ/bit; however, an off-chip filter is required for FCC compliance. A corresponding energy-detection receiver considered in [43] utilizes simple analog integration of charge onto capacitors to achieve a low energy consumption of 2.5nJ/bit up to data rates of 16.7Mbps.

As an alternative to energy detection, the non-coherent transceiver considered in [3] eliminated the need for synchronization and correlation by modulating data using On-Off Keying (OOK) and recovering the digital signal through envelope detection. A RAKE-based technique to improve the BER and multi-path fading of such OOK techniques was discussed in [44], though at a cost of increased hardware complexity and power consumption.

The transmitter presented in this thesis utilizes non-coherent pulsed-UWB signaling to relax frequency tolerances. This enables an all digital architecture where pulses are synthesized by directly modulating the output of a single-ended DCO. In this manner, the DCO is shared with an integrated downconverting receiver.

[5] In fact, the IEEE 802.15.4a proposal mandates that all transmitters *must* be capable of including phase information as a means of data modulation; low-power receivers can opt to ignore this information.

1.3.3 Summary

A summary of recently published UWB transmitters is shown in Table 1.1.

Table 1.1: Previously Published UWB Transmitters.

Ref.	Process	Vdd [V]	Symbol Rate [MHz]	Power [mW]	E/pulse [pJ]	Modulation
[1]	65nm	1.2	1(×8†)	0.3	37.5	PPM/BPSK
[2]	0.18μm	1.5	200	3.4	16.8	OOK
[3]	0.18μm	1.8	50	12.6	252	OOK
[4]	0.18μm	1.8	100	31.3	313	BPSK
[5]	0.18μm	1.8	400	76	190	PPM
[6]	0.18μm	2.2	36	29.7	825	BPSK
[7]	0.18μm	*	1000	50	50	OOK
[8]	0.18μm	1.8	750	9	12	BPSK
[9]	90nm	1.0	1(×16†)	0.65	40	PPM/BPSK
[10]	0.13μm	1.2	160	10	62.5	PPM/BPSK
[11]	0.18μm	2.5	1	0.7	700	OOK
[12]	90nm	1.0	10	0.47	47	PPM/DB-BPSK
This Work	90nm	1.0	15.6(×16†)	4.4	17.5	PPM/BPSK

* No VDD was specified.

† These transmitters burst multiple pulses back-to-back. The quoted energy per pulse numbers are for a single pulse within a burst.

1.4 Thesis Contributions

This thesis explores pulse-based ultra-wideband transmitters designed for highly energy and area constrained applications. Due to their relaxed center frequency tolerances, non-coherent UWB systems offer the opportunity to simplify transmitter architectures and increase energy efficiency. This enables the design of an all-digital UWB transmitter. However, all-digital UWB transmitters driving single-ended antennas typically produce undesired low-frequency content which violate FCC spectral masks. This low-frequency content is most often attenuated using large passive components, resulting in a severe area penalty.

The main contribution of this thesis is the design and implementation of an all-digital UWB transmitter which achieves FCC compliant operation without the use of

large passive components. Area and energy efficient FCC compliance is accomplished by using a combination of two techniques:

1. Low frequency content is attenuated up to 12dB by capacitively combining two paths which have in-phase RF components, yet have opposite common-modes which are canceled. This technique is realized in an energy efficient manner by dual capacitively coupled digital power amplifiers.

2. The dual power amplifiers each consist of a number of tri-state inverters. Four-level discrete pulse shaping is employed by dynamically enabling and disabling these inverters during pulse generation, resulting in up to 20dB of RF sidelobe attenuation.

The transmitter is implemented in 90nm CMOS and requires a core area of $0.07mm^2$. The all-digital architecture consumes 17.5pJ/pulse, which is among the most energy efficient UWB pulse generators reported in the literature.

This thesis also presents mathematical models used to predict measured spectral results of ultra-wideband pulse bursts. A technique to maximize communication distance of low-rate systems under peak and average power constraints is contributed as a result of this modeling.

Chapter 2

Pulsed-UWB Signaling

The 2002 FCC first order and report placed limits on both the peak and average isotropic radiated power from a UWB device over the 3.1-to-10.6GHz band. Since medium-to-high data rate transmitters are typically average power limited, there has been much effort spent trying to meet average spectral mask requirements while minimizing both energy consumption and implementation area. This chapter analyzes several different pulse shaping implementation strategies and offers a particular strategy that uses both minimal power and chip area. Also explored in this chapter are mathematical models to predict spectral measurements, which leads to a technique used to maximize communication distance for low-rate systems under both peak and average power constraints.

2.1 Generating UWB Pulses Digitally

As Moore's law continues to march down its path of ever-increasing transistor speed and density, it becomes more and more appealing to move previously analog dominated functions and circuits over to digital-oriented algorithms and circuits. This move away from analog structures is seen time and time again in examples such as PLLs [45], switched-capacitor circuits [46], and even entire Analog to Digital Converters (ADCs) [47]. The advantages of digital structures are plentiful, including

continued density scaling, zero static bias currents[1], and noise immunity.

Assuming, for the moment, that everything that can be done in digital CMOS *should* be and *will* be done in digital CMOS[2], it is worthwhile to investigate how UWB pulse generation can be done using entirely singled-ended digital circuits. Section 2.2 and Chapter 4 will discuss some results of this claim in more detail. For now, it does not take much effort to design a very simple all-digital pulse generator. As an example, consider the transmitter shown in Figure 2-1. Data in this transmitter can be modulated using OOK, or PPM, as illustrated in Figure 2-2.

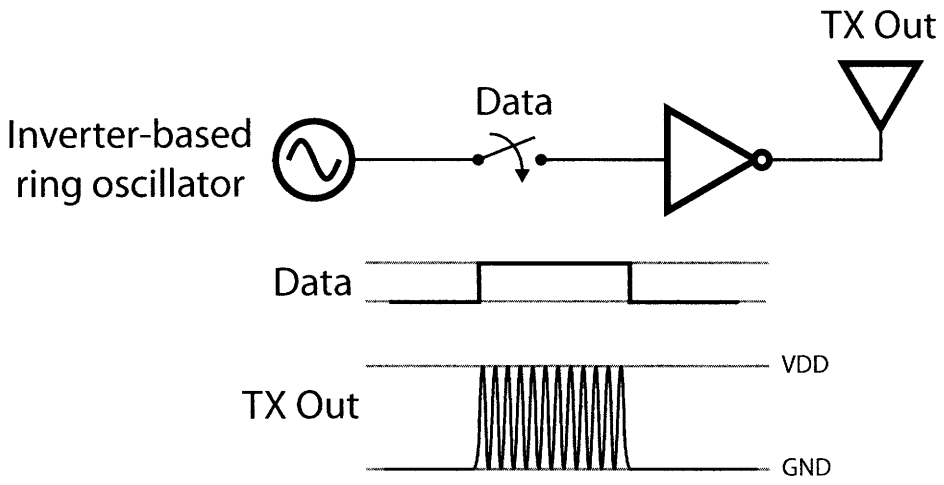


Figure 2-1: A simple way to generate UWB pulses using all-digital circuits.

This transmitter can be designed using only standard cells in a digital CMOS process. For instance, the oscillator can be implemented as three inverters in a ring, the switch can be implemented as a 2-to-1 multiplexer with one input connected to the output of the ring and the other to ground, and the power amplifier can simply be a large inverter. Since only standard cells are used, it should be possible to synthesize and auto-layout this transmitter architecture using digital Computer Aided Design (CAD) tools.

Of course, this architecture suffers from several drawbacks. Several notable omis-

[1]Note that subthreshold leakage currents of large digital designs are fast approaching the levels of static bias currents. However, the recent introduction of low-leakage processes specifically produced for low-power circuits are helping to mitigate this problem.

[2]...with or without you, as Professor Ali Hajimiri might say. In other words, if you don't do it in digital CMOS, somebody else will, as the cost advantages over other technologies are indisputable.

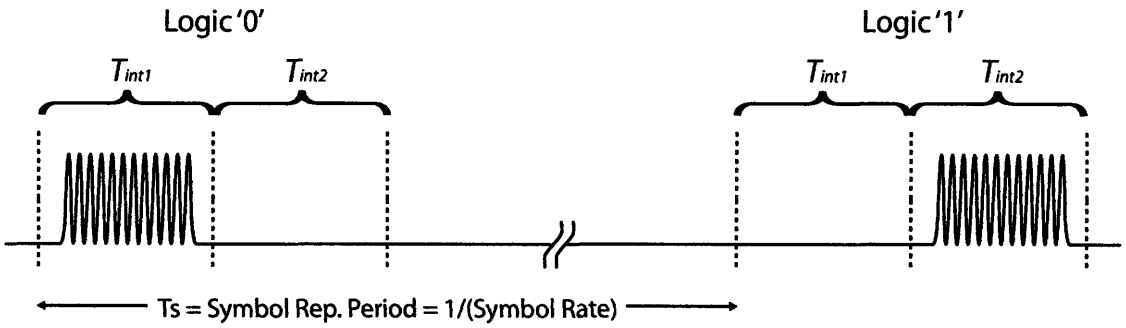


Figure 2-2: Pulse position modulation represents data by the presence of a pulse in a particular window in time.

sions are the lack of programmability, calibration, and carrier phase lock. Programmability can be achieved in the hand-designed oscillator by using binary-weighted capacitive loads which can programmed through digital logic. In the synthesized circuits, similar programmability can be achieved by inserting several tri-state inverters in parallel, thereby effectively changing each stage of the ring oscillator's drive strength and capacitive load. Similar techniques can by applied to the power amplifier for gain control. Carrier frequency calibration can be achieved using a combination of divider, counter, and phase detector circuits. Carrier phase lock is in fact not necessary if the receiver is non-coherent, since the phase is discarded anyways. Otherwise, a PLL may be used for coherent systems.

Another major problem with this architecture is found in the spectral characteristics of the generated pulses. The output spectrum of a PPM-modulated pulse train is given by equation 2.1 [41, 42].

$$P_{PPM}(f) = \frac{1}{4T_s^2} \cdot \sum_{n=-\infty}^{\infty} \left| S\left(\frac{n}{T_s}\right)\left(1 + e^{-j2\pi \frac{nT_{PPM}}{T_s}}\right)\right|^2 \delta(f - \frac{n}{T_s}) + \frac{1}{T_s}|S(f)|^2 - \frac{1}{4T_s}\left|S(f)(1 + e^{-j2\pi f T_{PPM}})\right|^2 \quad (2.1)$$

Here, $S(f)$ is the Fourier transform of the reference pulse, T_{PPM} is the PPM delay, and T_s is the symbol repetition period. The resulting power spectral density of a square pulse train with non-zero DC content centered at 4GHz (as in Figure 2-2)

is superimposed over the FCC indoor mask in Figure 2-3.

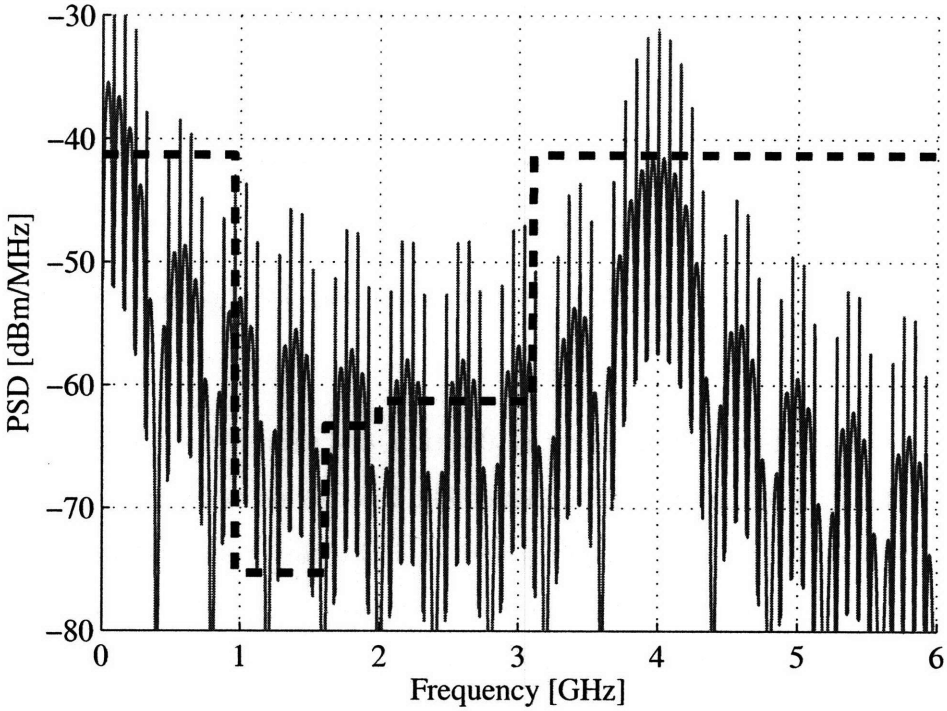


Figure 2-3: Power spectral density of a train of PPM-modulated square UWB pulses.

The resulting spectrum has an underlying shape of a $sinc(x)$ (or $sin(x)/x$) envelope centered at the carrier frequency. This makes sense, since the Fourier transform of a rectangular pulse in the time domain leads to a $sinc(x)$ function in the frequency domain. However, due to several reasons this spectrum is not FCC compliant. Section 2.2 will attempt to fix the compliance issue while adding as little circuit area and energy overhead as possible.

2.2 Achieving Spectral Compliance

The time and frequency domain views of a PPM-modulated square UWB pulse train are shown in Figures 2-2 and 2-3, respectively. There are three main problems with this resulting spectrum, all three of which must be addressed in order to meet the FCC spectral mask:

1. Large spectral lines spaced at integer multiples of the pulse repetition frequency.

2. Sidelobes centered at the carrier frequency.

3. Sidelobes centered at DC.

2.2.1 Spectral Lines

The problem of spectral lines is conceptually easy to fix. If the UWB pulses were phase modulated with random (or pseudo-random) data during transmissions, the tones would be scrambled out. This effect is most easily achieved by implementing a BPSK scrambler or modulator. The resulting power spectral density is given by equation 2.2, and is illustrated in Figure 2-4.

$$P_{BPSK}(f) = \frac{1}{T_s} |S(f)|^2 \tag{2.2}$$

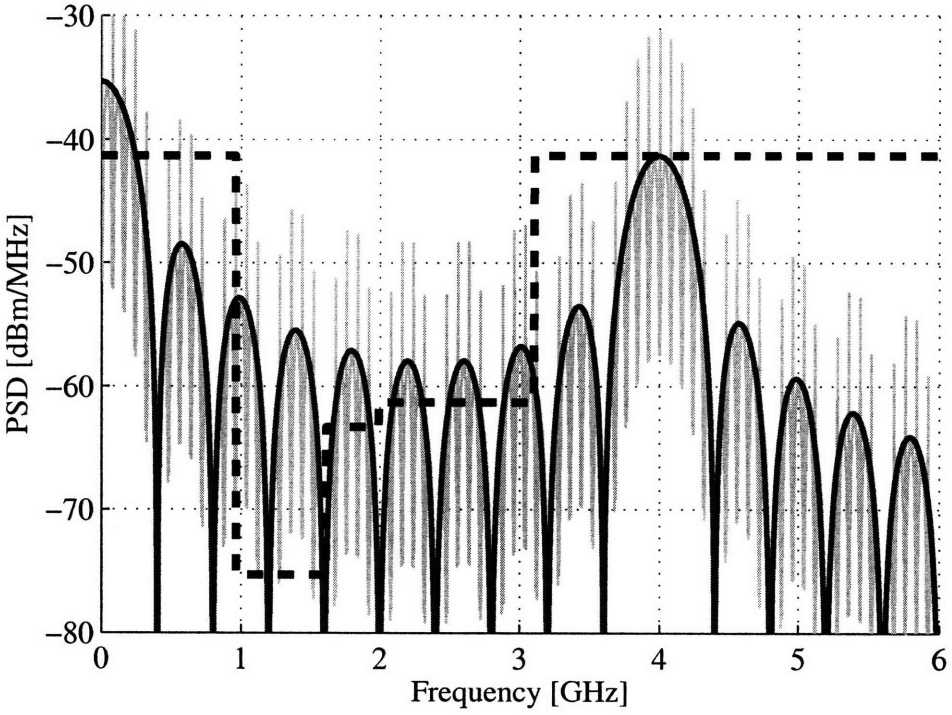


Figure 2-4: Power spectral density of a train of PPM-modulated, BPSK-scrambled, square UWB pulses overlaid on top of the non-BPSK-scrambled case.

2.2.2 RF Sidelobes

This spectrum of Figure 2-4 still suffers from drawbacks two and three: namely, it contains undesired sidelobes centered at both RF and DC. Although these sidelobes can easily be eliminated by bandpass or highpass filters, the area penalty of this approach is significant. For instance, this particular example would require at least a fourth order passive filter to ensure the necessary roll-off of roughly 20dB in 0.29 decades (from the 1.61GHz to 3.1GHz mask boundaries). A fourth order passive filter requires several inductors and capacitors, which are not only lossy in modern semiconductor technologies, but also consume significant area.[3] One can also engineer an antenna to have the desired bandpass properties, however since the UWB band is so large (3.1-to-10.6GHz), it may be difficult to achieve the required selectivity. Also, for system robustness it is generally desirable to design circuits to be compatible with a variety of different peripheral devices, such as antennas in this case.

An alternative to filtering is to employ pulse shaping to reduce the sidelobes centered at RF. As demonstrated in [6, 7, 48, 49, 50], and many other designs, pulse shaping is a very good method for obtaining high-order roll-off without the use of large passive filters. An excellent overview of several popular pulse shapes can be found in [51].

To illustrate the virtues of pulse shaping, consider shaping a pulse with a raised-cosine envelope, as illustrated in Figure 2-5. The resulting spectrum achieves up to 17dB of sidelobe rejection, as shown in Figure 2-6.

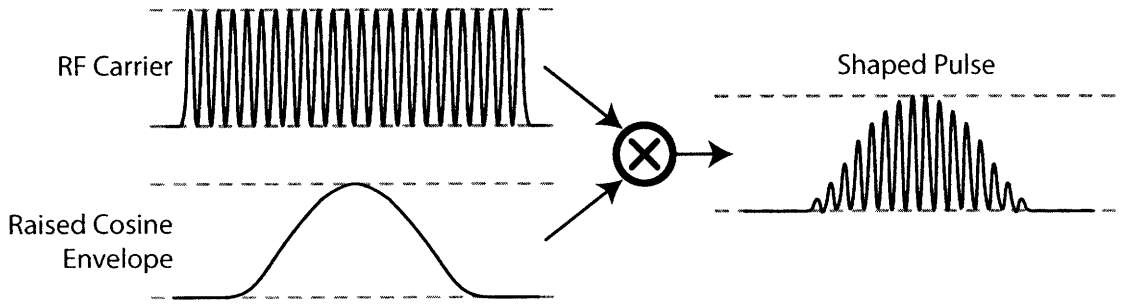


Figure 2-5: Time domain view illustrating how to generate a raised-cosine pulse.

[3]The option of an off-chip filter is far worse in terms of an area trade-off, although they do tend to have much better characteristics than their on-chip counterparts.

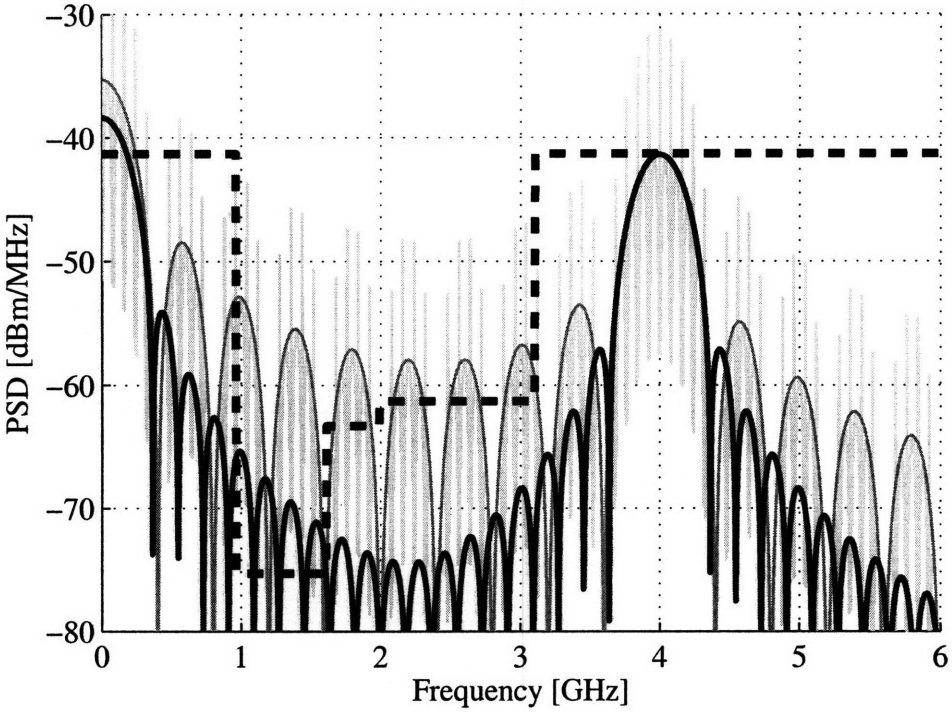


Figure 2-6: Power spectral density of a train of PPM-modulated, BPSK-scrambled, raised-cosine UWB pulses overlaid on top of the spectrum in Figure 2-4.

2.2.3 Low Frequency Sidelobes

The raised cosine envelope greatly suppresses the sidelobes centered around the carrier frequency. However, the sidelobes centered at DC remain. This problem does not depend on pulse shape, but is rather fundamentally related to the method in which the digital pulses are synthesized. The issue stems from the fact that single ended digital circuits have only two stable operating points: the lowest and highest potentials in the circuits (typically GND and VDD). To eliminate the DC content and its associated sidelobes, the generated pulses must have *three* effective levels: GND, +V, and -V, as illustrated in Figure 2-7.

For continuous wave systems, this is a relatively easy problem: simply insert an AC-coupling capacitor[4] before the antenna, as illustrated in Figure 2-8. This solution is not ideal for pulses of short duration, the reason for which will become clear momentarily. Digitally generated pulses with two reference voltage levels (e.g.

[4]Otherwise known as an DC-blocking capacitor.

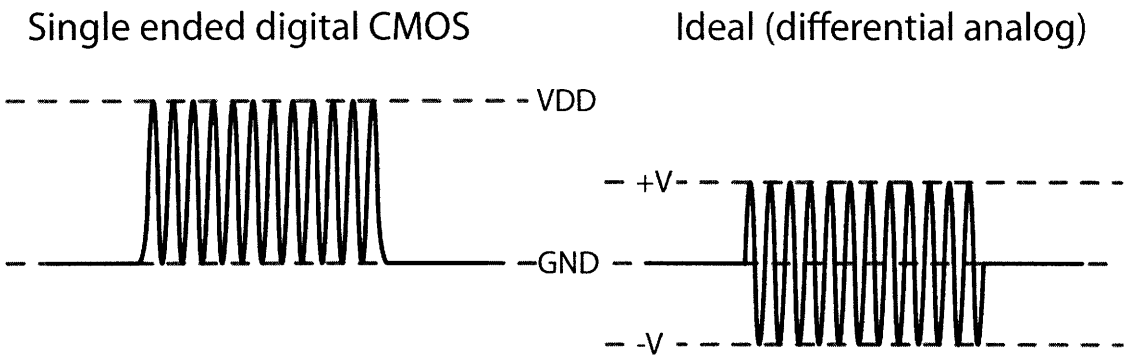


Figure 2-7: Digital CMOS circuits can only generate one of two different reference levels. On the other hand, differential analog circuits can generate multiple reference levels at different bias voltages.

GND and VDD), can be decomposed into an RF carrier and a baseband pulse, as illustrated in Figure 2-5. The baseband pulse will require a finite amount of time to charge and discharge the voltage across the capacitor, as shown in Figure 2-9. The time required to charge and discharge, given by t_{charge} and $t_{discharge}$ respectively, is proportional to the $1/RC$ time constant of the circuit.

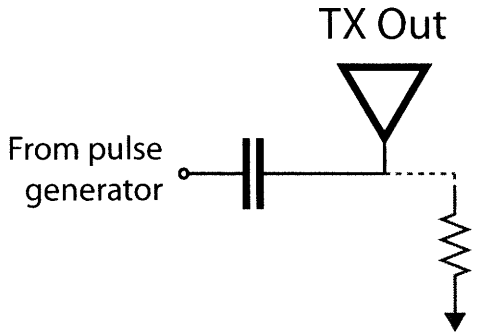


Figure 2-8: A coupling capacitor providing a DC block to a wideband antenna. A large resistor may be connected from the output to ground in order to provide a stable DC voltage to the antenna if necessary.

The effect of finite low frequency capacitor charging and discharging times when AC-coupling UWB pulses is illustrated through a time-domain simulation of a square pulse in Figure 2-10. It can be noted here that the AC-coupled pulse has a non-zero DC value, as well as some low-frequency turn-on and turn-off transients. The power spectral density of a train of BPSK-scrambled raised-cosine UWB pulses before and after the AC-coupling filter is shown in Figure 2-11. The AC-coupled spectrum

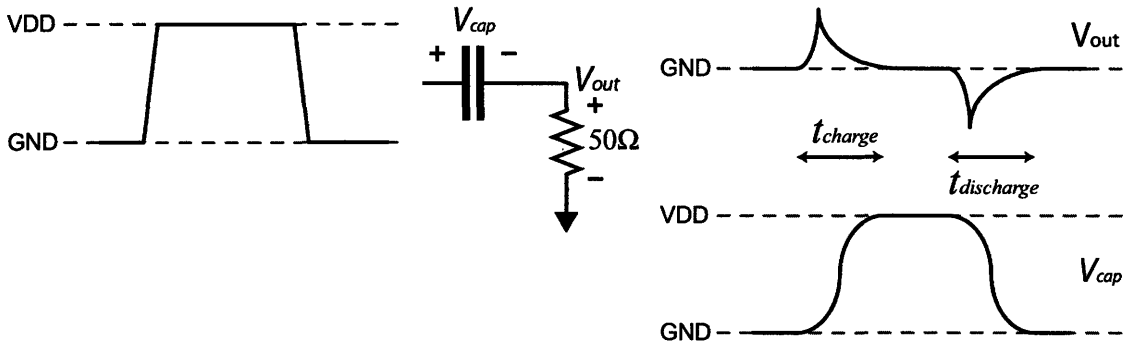
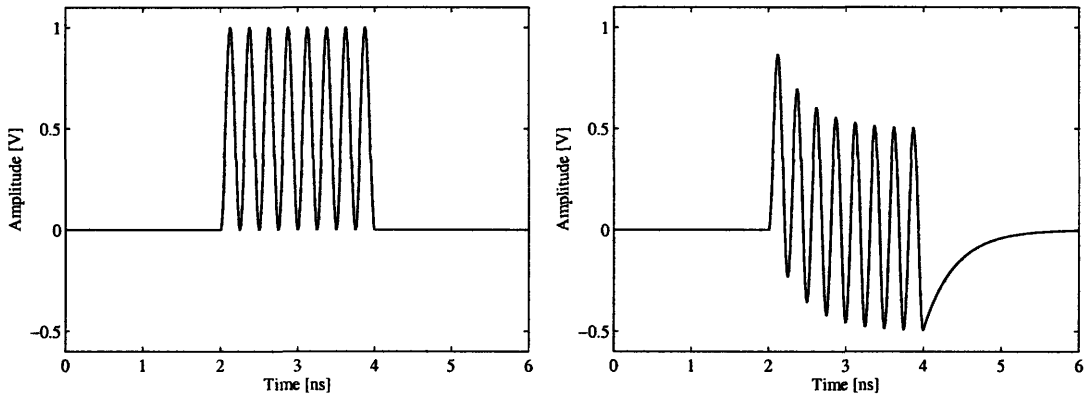


Figure 2-9: A baseband pulse requires a finite amount of time to charge and discharge a coupling capacitor.



(a) Digitally generated pulse

(b) After AC-coupling filter

Figure 2-10: The effect of passing a UWB pulse through an AC-coupling capacitor.

does not comply with the FCC mask, since the first order roll off is not sufficient to eliminate all of the low frequency sidelobes.

There are several techniques to reduce or even eliminate the low frequency-content of digitally generated UWB pulses. The most common technique relies on generating individual half-RF cycles and applying them differentially to a wideband balun, as discussed in section 1.3.1 [6]. This technique produces excellent spectral results, however it does not fit in with the spirit of designing scalable architectures with minimal area, since inductors are relatively large and do not scale very well in advanced

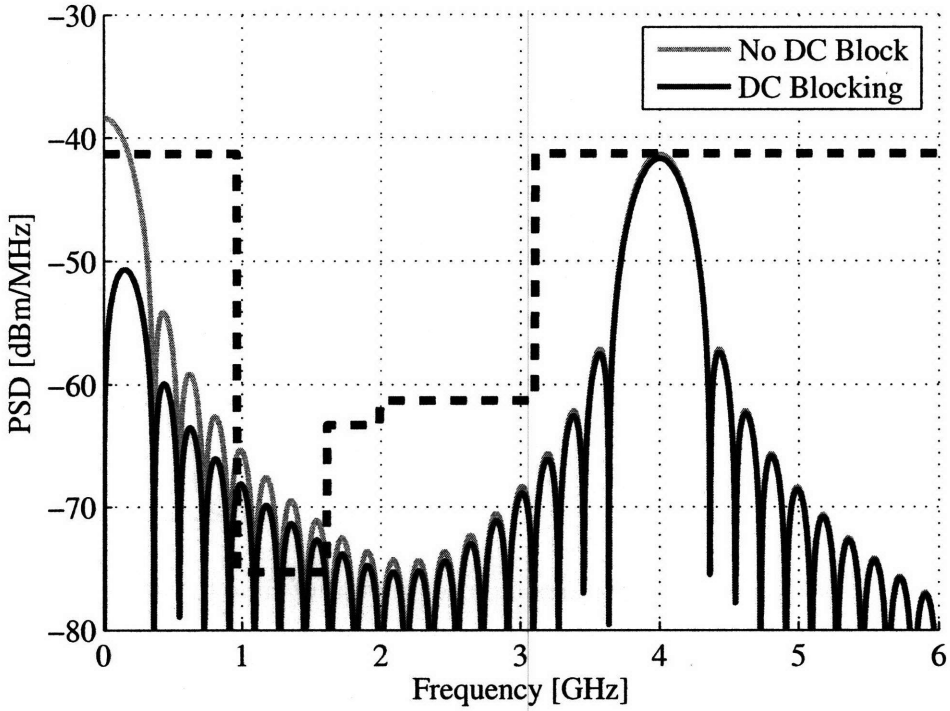


Figure 2-11: Power spectral densities of raised-cosine pulses before and after an AC-coupling filter.

CMOS technologies.[5] Another potential drawback of this type of architecture is that the half-RF cycles are generated from a delay line instead of a free-running ring oscillator. This can be seen as a benefit if the designed system is only a transmitter which generates a single pulse, then immediately turns off for a period of time. If, instead the designed system is a transceiver that transmits multiple pulses back-to-back, it is beneficial to design a single oscillator which is shared between the receiver and transmitter, as shown in Figure 2-12.

The proposed solution to attenuating the low frequency content using scalable digital structures involves capacitively coupling two paths which have differential baseband signals, yet contain in-phase RF tones. To elaborate, consider the network shown in Figure 2-13(a), where the two capacitors nominally have opposite DC voltages across them (GND and VDD, generated from digital logic). If they are driven

[5]That is, they do not scale as well as capacitors in terms of area density. This is because inductors are typically implemented in the topmost metal layers (which have not been scaling very quickly), whereas capacitors are scaling somewhat more rapidly with advancements in dielectrics and/or increases in lower-metal layer densities (for metal-oxide-metal capacitors).

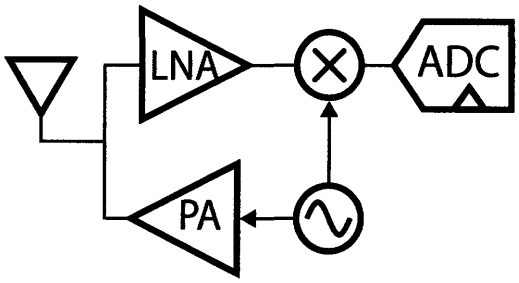


Figure 2-12: A simple transceiver system sharing a single oscillator.

with a differential baseband pulse, the upper capacitor will ideally charge at the same rate that the lower capacitor is discharging, thereby inducing zero voltage at the output.

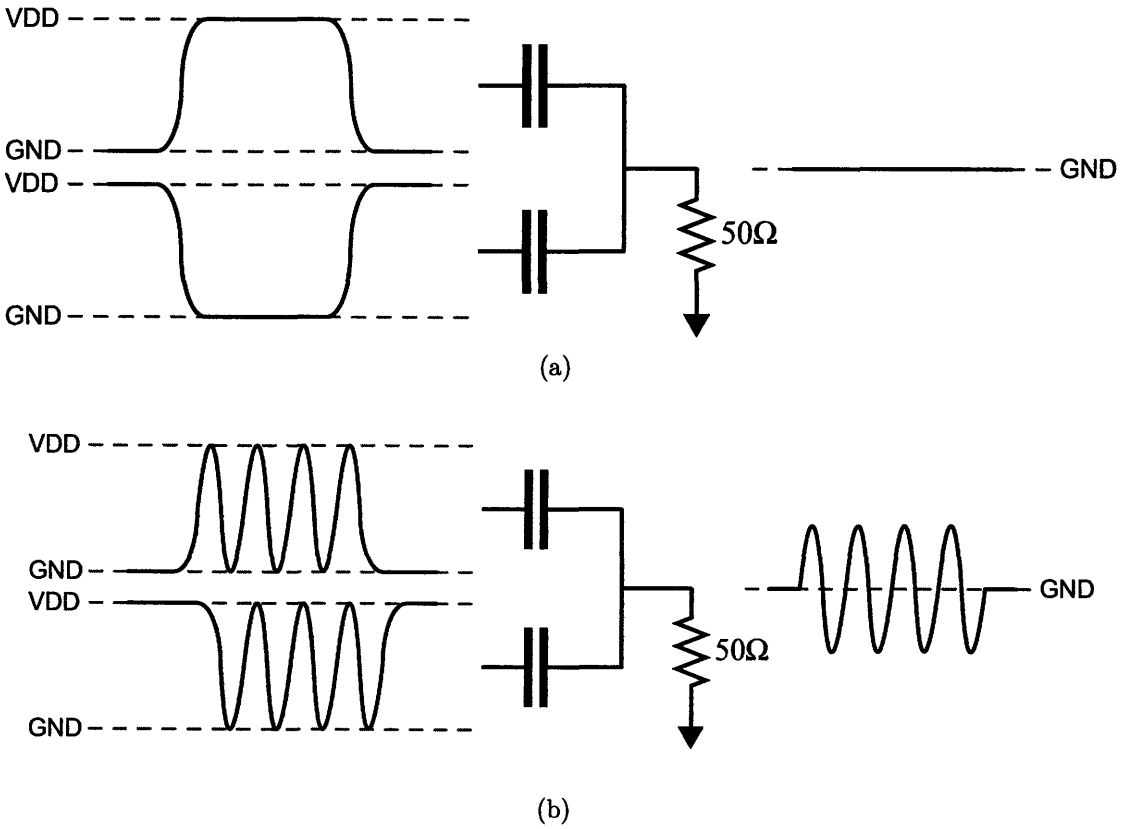


Figure 2-13: Differential baseband pulses cancel as shown in (a), while in-phase RF signals propagate relatively undisturbed to the output, as shown in (b).

If the low frequency baseband pulses are multiplied with in-phase RF tones as illustrated in Figure 2-13(b), then the low frequency common-modes will cancel, and the in-phase RF components will propagate to the output.

Since the two inputs into the capacitive combination network start off with opposite common modes, there is an inherent half RF cycle delay between the start of the effective baseband pulses shown in Figure 2-13(b). This, combined with circuits mismatches, will create non-idealities including turn-on and turn-off transients leading to spectral impurities. Ideally, the output spectrum will contain zero low frequency content, as illustrated by the spectrum of ideal raised cosine pulses in Figure 2-14. In practice, the output spectrum will have an appreciable amount of low-frequency content. This is discussed using mismatch analysis of the designed circuits in Chapter 3. The measurement results in Chapter 4 will indicate that there is sufficient low frequency attenuation to meet the FCC spectral mask.

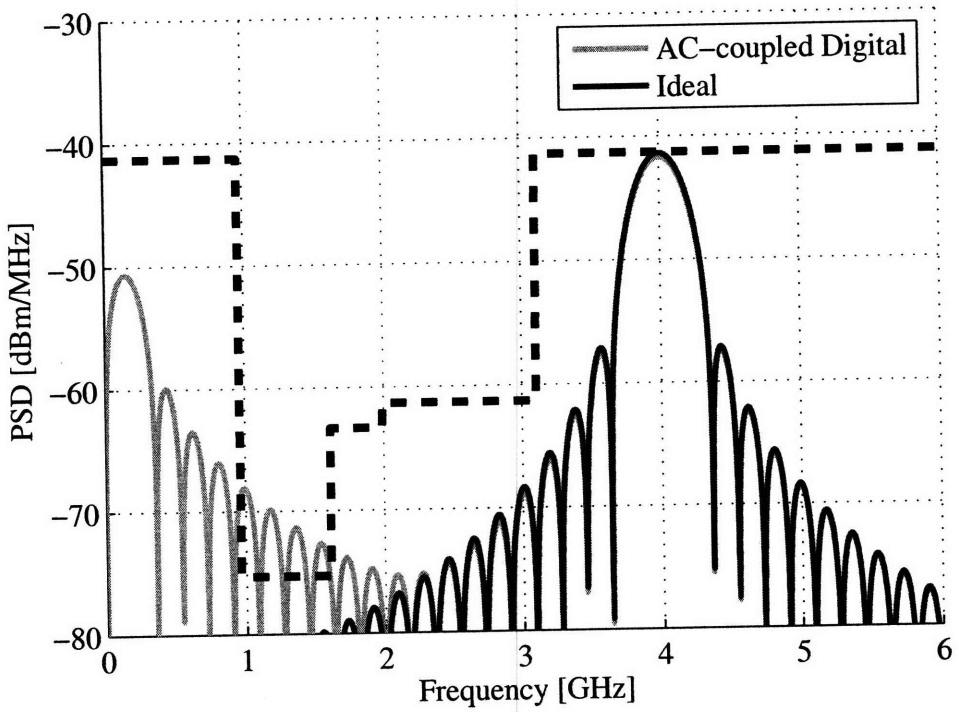


Figure 2-14: Power spectral densities of ideal raised-cosine pulses and AC-coupled digitally generated raised cosine pulses.

2.3 Predicting Measurement Results

The goal of this section is to provide a mathematical framework for predicting the measurement results of pulsed-UWB signals using a spectrum analyzer (SA). Before getting into the details it is worthwhile to review the FCC regulations and introduce the concept of pulse bursting, all while introducing some notation.

2.3.1 FCC Regulations

Recall that the FCC places limits on both the peak and average radiated output power in the 3.1-to-10.6GHz UWB band. For the sake of completeness, the two key FCC regulations are as follows [16]:

1. The *average* PSD must be less than or equal to -41.3dBm in the 3.1-to-10.6GHz band. This corresponds to a theoretical maximum total power of -14.3dBm for a 500MHz bandwidth signal. In practice this number is reduced by 2-to-4dB via pulse generation constraints. Table 2.1 shows the maximum PSDs in other frequency ranges.

2. The *peak* power may not exceed 0dBm at the UWB signal's center frequency in a 50MHz resolution bandwidth (RBW). Since most spectrum analyzers are not equipped with a 50MHz intermediate frequency (IF) filter, the peak power measurement is typically performed at a lower RBW and the limit is conservatively set to be $P_{pk} \leq 20log_{10}(\text{RBW}/50\text{MHz})$.

It should be noted that although measurements to confirm FCC compliance are typically done with a spectrum analyzer, alternative techniques exist [52].

2.3.2 Pulse Bursting

For long range and/or reliable communication, it is often necessary to transmit multiple pulses per bit of information. The extra pulse information allows the receiver to perform averaging, thereby increasing the effective signal to noise ratio and thus

Table 2.1: FCC Mask Limits

Frequency Range $[MHz]$	Indoor Limit $[dBm/MHz]$	Outdoor Limit $[dBm/MHz]$
Below 960	FCC 15.209	
960-1610	-75.3	-75.3
1610-1990	-53.3	-63.3
1990-31000	-51.3	-61.3
31000-10600	-41.3	-41.3
Above 10600	-51.3	-61.3

decreasing the bit error rate. The number of pulses per bit is typically called the *spreading factor.*

In the interest of duty cycling, it is generally advantageous to process information using many bits at a time, then subsequently shutting circuitry off. This minimizes the energy overhead of having to turn on and off the circuits performing the information processing. For example, if a system operates at an effective data rate of 100kbps and requires a spreading factor of 10 for reliable communication, the PRF would have to be 1Mpulse/s. Instead of representing a symbol with a single pulse, it is alternatively possible to burst several pulses together and transmit them at once. For instance, if a burst of ten pulses constituted a symbol, then a symbol repetition frequency (SRF) of 100kSymbols/s would still have an effective PRF of 1Mpulse/s, yet there is a 10x reduction in the turn-on/turn-off energy overhead, as illustrated in Figure 2-15. Pulse bursting is especially beneficial to non-coherent system implementations, as the

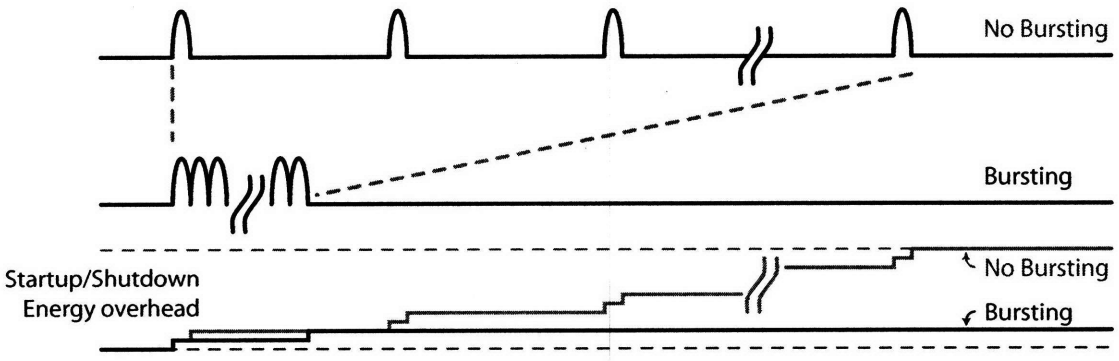


Figure 2-15: Turn-on/turn-off energy overhead reduction when applying pulse bursting.

integration period often determines the maximum symbol rate, which is typically the same as the baseband clocking frequency. Thus a low symbol rate leads to a low clock rate, which simplifies digital implementations and improves energy efficiency.

Figure 2-16 illustrates the concept of pulse bursting by showing two groups of five individually BPSK modulated pulses. Some notation is also introduced here. For instance, in communication theory the individual pulse width is typically called the chip period, indicated by τ_c. N_c is the number of chips per burst, and V_{pk} is the peak voltage of the waveform. It should be noted that the IEEE 802.15.4a standardization committee incorporates pulse bursting into the UWB PHY layer [29].

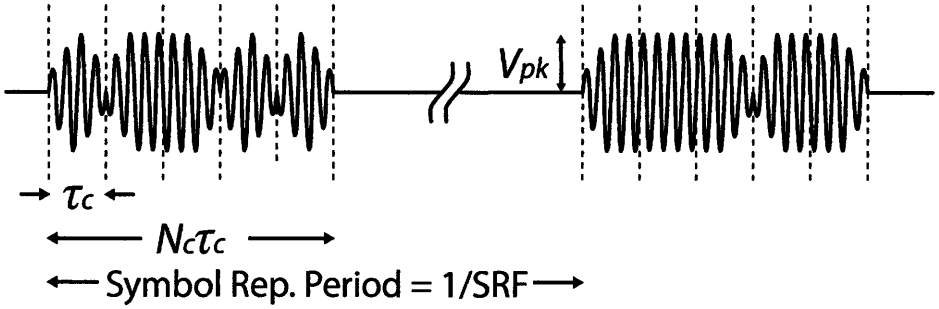


Figure 2-16: Two bursts of five individually BPSK modulated pulses (i.e. $N_c = 5$).

2.3.3 Mathematical Modeling

Most UWB pulses have a narrow pulse width $\tau_c < 0.1/\text{RBW}$ relative to the intermediate frequency of an SA. Thus, the SA measures the impulse response of its own IF filter, rather than the response of the UWB pulse. To predict certain measured results from an SA, a pulse desensitization correction factor (PDCF) will be introduced [4, 53].

Ideally, the spectral response of a periodic BPSK-modulated pulse (or burst) train should contain spectral lines at integer multiples of the SRF.[6] This effect will be observed on an SA if its RBW if less than the SRF, since the SA will have sufficient resolution to display the spectral lines. This measurement regime is called the *high-SRF region*, and occurs when RBW/SRF < 0.3. If, on the other hand, the RBW

[6]These lines are different than the undesired spectral lines produced by non-phase-scrambled, PPM-modulated pulse trains.

is greater than the SRF, the SA does not have sufficient resolution and individual spectral lines are blended together. This measurement regime is called the *low-SRF region*, and occurs when RBW/SRF > 1.7. The peak and average powers in these two regions can be predicted using the equations derived below. Unfortunately, measurements in the region around SRF≈RBW depend heavily on modulation statistics and is much more difficult to predict [54].

For both low and high symbol-repetition frequency BPSK-modulated signals, the the average power can be found by using Equation 2.3.

$$P_{avg} = 10\log\left(\frac{V_{pk}^2}{Z_0}\right) + 20\log(\tau_{eff}) + 10\log(\mathrm{PRF}_{eff} \cdot \mathrm{RBW}) \tag{2.3}$$

Here, V_{pk} is the peak voltage of the pulse, Z_0 is the characteristic impedance, and PRF_{eff} is the effective *pulse* repetition frequency (i.e. for bursting, $\mathrm{PRF}_{eff} = \mathrm{SRF} \times N_c$). τ_{eff} is the effective individual pulse width, as illustrated by Figure 2-17 and given by Equation 2.4.

$$\tau_{eff} = \int_0^{\tau_c} \frac{p(t)}{V_{pk}} dt \tag{2.4}$$

Here, $p(t)$ is a single pulse, and τ_c is the time interval which contains all the energy of $p(t)$.

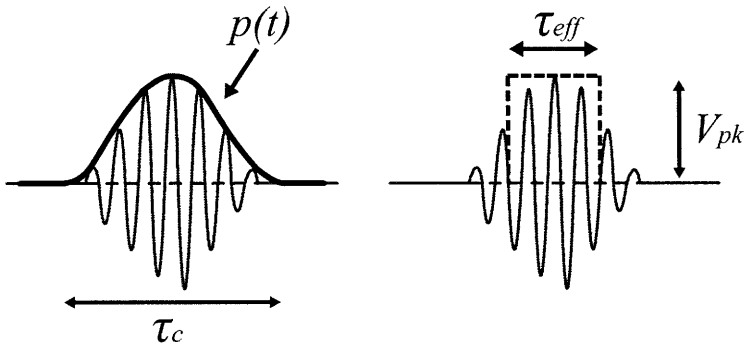


Figure 2-17: Effective pulse width of a non-rectangular pulse envelope.

The peak power in the high-SRF region is given by Equation 2.5

$$P_{pk,h} = P_{avg} + P_{m,h} \tag{2.5}$$

Here, $P_{m,h}$ typically ranges from 7dB to 11dB, and depends on both the modulation statistics and the length of time the peak measurement is taken over [53].

The peak power in the low-SRF region is given by Equation 2.6.

$$P_{pk,l} = 10\log\left(\frac{V_{pk}^2}{Z_0}\right) + \text{PDCF} + P_{m,l} \tag{2.6}$$

Here, $P_{m,l}$ is a fitting factor based on modulation statistics and typically varies from -3dB to +3dB. The pulse desensitization correction factor is given by Equation 2.7.

$$\text{PDCF} = 20\log(\tau_{b,max} \cdot \text{RBW} \cdot k_{pulse}) \tag{2.7}$$

k_{pulse} relates the RBW frequency to an effective IF bandwidth for pulsed signals. It depends on the SA used and typically varies from 1.5 to 1.617 [53]. $\tau_{b,max}$ is the worst-case effective burst width and is given by Equation 2.8:

$$\tau_{b,max} = \left| \int_0^{\frac{1}{SRF}} \frac{p_{b,max}(t)}{V_{pk}} dt \right| \tag{2.8}$$

Here, $p_{b,max}$ is the inter-burst chip sequence with the worst-case peak power, which occurs when the chip sequence contains a minimum number of phase inversions. For single-pulse transmissions, $p_{b,max} = p(t)$.

Although there is a small degree of uncertainty to these models (typically depending on modulation statistics), section 2.3.4 shows that system level insight can be gained regardless.[7]

[7]This is not unlike the reason students learn the zero-th order transistor models - although they are no longer accurate in deep submicron CMOS, they still provide the tools to understand what trade-offs can be made when chasing specific design goals.

2.3.4 Extending Communication Distance

Communication distance in a non-coherent energy-detecting UWB system is maximized when the SNR seen at the receiver during the integration period is maximized. This occurs when the transmitter generates maximum total output power under regulatory limits. Since sensor networks typically communicate at low data rates, large amplitude pulses transmitted at the data rate are required to maximize power under FCC spectral masks. For example, a peak-to-peak voltage swing of 19.3V is required to maximally satisfy FCC spectral masks at a PRF of 10kHz (when the spreading factor is zero). This is clearly impractical in deep sub-micron CMOS where supply voltages are on the order of 1V.[8] An alternative approach to generating large-swing pulses while maximizing total power under FCC masks is to reduce output voltage swings and increase the spreading factor.

High data rate pulsed-UWB transmitters are typically average power limited, while low data rate transmitters are typically peak power limited [4]. Low data rate systems can thus forsake a considerable amount of total power in order to remain peak power compliant. In other words, the peak-to-average power ratio (PAPR) of low pulse rate transmitters is generally large and thus violates the FCC peak power limit well before the average power limit.

Since the average power of low-SRF transmitters has a $10log()$ dependence on SRF while the peak power does not depend on SRF, the PAPR can be reduced by decreasing the peak-to-peak voltage swing and increasing the SRF. This increases the number of receiver integrations required per bit as a trade-off for enhanced communication distance. This can alternatively be thought of as increasing the spreading factor to approach the spectral behavior of a high-SRF transmitter.

An additional method to reduce PAPR is by introducing run length limits (RLLs) in the transmitter phase modulator to prohibit long bursts of pulses with no phase inversions [55]. In other words, the peak power may be reduced by lowering $\tau_{b,max}$, which ideally leaves the average power unaffected. For example, a linear feedback shift register (LFSR) based scrambler may output a run of eight '+1' phase bits at

[8] Not to mention this scheme would likely also violate peak power regulations.

some point in its sequence. This results in $\tau_{b,max} = 8\tau_c$. A run length limit of three would ensure that the fourth and eighth phase bits are inverted, as illustrated in Fig. 2-18. This results in $\tau_{b,max} = 4\tau_c$, giving a 2x (or 3dB) reduction in peak power over the non-RLL case.

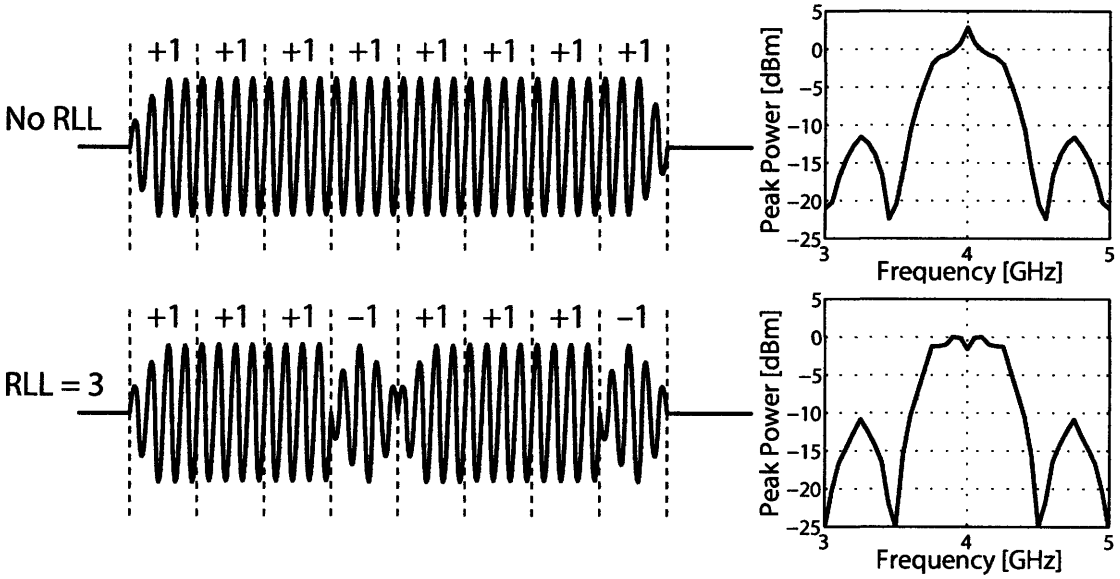


Figure 2-18: Example of run-length limiting. The simulated peak PSDs emulate the results of a spectrum analyzer operating in peak-hold mode.

This technique spreads *peak* power away from the carrier frequency while leaving the average PSD undisturbed for reasonable RLLs. However, small-valued RLLs (such as run-length limits of three when a burst contains sixteen pulses) can distort the average PSD by spreading a significant amount of energy away from the carrier frequency.

Figure 2-19 illustrates the reduction of peak power by decreasing voltage swings, increasing SRF, and applying run-length limiting. The maximum average PSD is fixed at -41.3dBm/MHz across all voltages and SRFs. In the case of a data rate of 10kbps, the communication distance is maximized under FCC constraints without run length limiting at $V_{pk-pk} = 0.26$V and SRF = 3.3MHz. Sixteen pulses are generated per burst and 330 burst-repetitions are required per bit, resulting in an overall spreading factor of 5280. Applying an RLL of 4 reduces peak power by approximately 3dB, giving $V_{pk-pk} = 0.37$V, SRF = 1.7MHz, and 170 burst-repetitions per bit, resulting

in an overall spreading factor of 2720. This represents a 1.9x improvement in receiver energy efficiency over the non-RLL case.

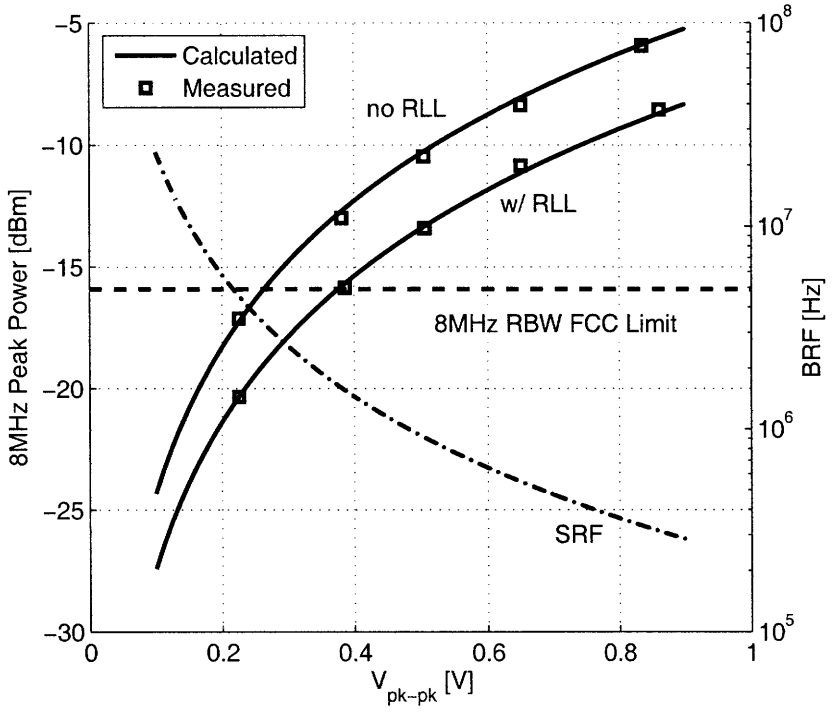


Figure 2-19: Peak power versus V_{pk-pk} with $P_{avg} = -41.3$dBm/MHz fixed. Here, $R_{nom} = 10$kbps, RBW = 8MHz, $\tau_c = 2$ns, $N_c = 16$, and RLL = 4 (when used). $P_{m,l}$ is -3dB and -2dB for no RLL and RLL = 4, respectively. The measured results are from the transmitter proposed in Chapter 3.

Although receiver implementation details and link budget analysis are outside the scope of this thesis, applying run length limiting in combination with a low effective data rate and large spreading factor can lead to an ultra-wideband system capable of reliable communication up to 100m. The transmitter discussed in Chapter 3 implements run length limiting to help achieve this communication distance goal.

2.4 Summary

This chapter explored the use of single-ended digital circuits for UWB pulse generation. It was shown that having only two stable operating points in digital static CMOS circuits can lead to undesired low-frequency spectral content at the transmit-

ter output. This low-frequency content may compromise FCC compliance, especially in the GPS notch from 960MHz-to-1.61GHz. The proposed solution to attenuating this low-frequency content involves capacitively combining paths which are in-phase at RF, yet have counter-phase common-mode components that are canceled. The common-mode cancellation ideally leads to zero low-frequency content at the transmitter output. Additionally, by shaping the output pulses, it was shown that FCC compliant operation could ideally be achieved without requiring the use of explicit passive filters.

This chapter also presented mathematical models for predicting spectrum analyzer measurement results of pulsed-UWB signals. It was shown that peak power could be reduced in pulse-bursting communication schemes without compromising the average power. This can be achieved if the worst-case effective burst length, $\tau_{b,max}$, can be reduced. It was shown that applying run length limits to the output of a phase-scrambling LFSR achieves this goal. Since low data rate pulsed-UWB systems are typically peak power limited, any amount of peak-power reduction helps in maximizing communication distance under FCC regulations.

Chapter 3

Transmitter Design

3.1 Architecture

A block diagram of the proposed transmitter is shown in Figure 3-1 [56]. The transmitter is designed to operate in all three channels of the low-band group of the 802.15.4a proposal. As per the 802.15.4a specifications, payload data is modulated using TH-PPM, where a PPM symbol is represented by a burst of several back-to-back pulses contained in a fixed window of time [1]. In idle mode between bursts, all transmitter circuits are off and the transmitter consumes only leakage power.

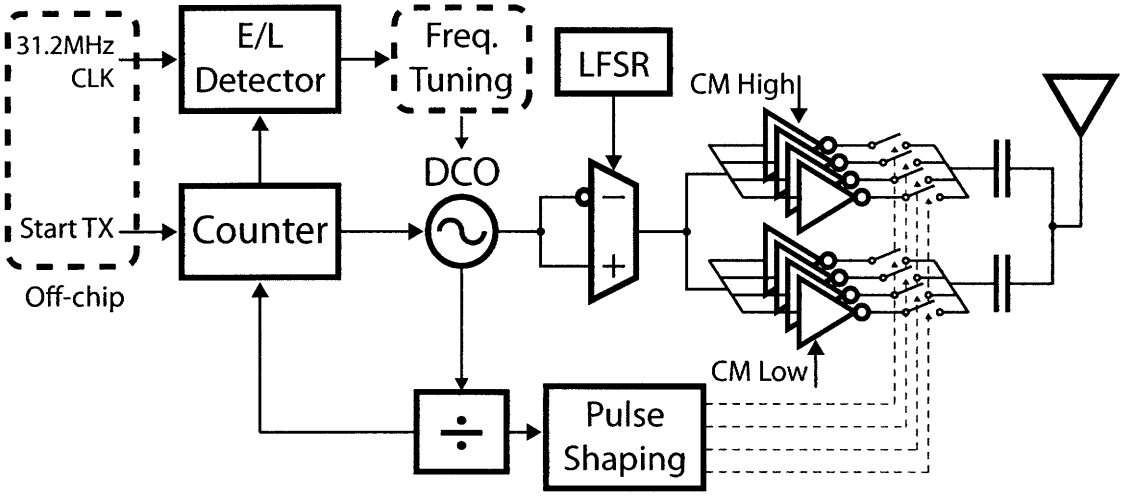


Figure 3-1: Transmitter block diagram.

Pulse bursts are generated on the rising edge of the off-chip *Start-TX* signal. This

edge enables a DCO, whose output is BPSK-scrambled via an LFSR and subsequently buffered through dual single-ended digital PAs employing capacitive combination.

The DCO output frequency is calibrated and dynamically adjusted using an early-late detector in a digital frequency-locked loop (FLL). The DCO output is also synchronously divided to a 499.2MHz clock as specified by the 802.15.4a standard [29]. Several phases of the divided clock are used by pulse shaping circuitry to dynamically shape the PA envelope to one of four discrete levels. The 499.2MHz clock sets the PRF within a burst, and is also used in conjunction with a counter to program the number of pulses transmitted per burst.

All programmable digital bits are configured by an on-chip shift register. The shift register was coded in Verilog, synthesized, and imported into the layout by Denis Daly.

The remainder of this chapter will discuss the implementation strategies of each block in more detail.

3.2 Dual Digital Power Amplifiers

A key challenge in pulsed-UWB power amplifier design is how to achieve energy efficiency and spectral compliance while requiring as little chip and circuit board area as possible. Traditional differential analog power amplifiers operating in their linear region can easily achieve spectral compliance, but typically have poor power efficiency [4]. Digital and switched-mode PA implementation offer superior energy efficiency compared to their analog counterparts [57], yet as discussed in Chapter 2, digital power amplifiers typically require high order off-chip filters and/or baluns to achieve spectral compliance [6, 10, 12]. An added benefit of digital power amplifiers is that they are far more amenable to continued scaling in advanced CMOS processes.

It should be noted that a *digital power amplifier* does not necessarily refer to a *switched-mode power amplifier*. Switched mode PAs, such as class F amplifiers, are typically narrowband in nature. That is, although they utilize transistors as digital switches, the output is shaped by a tank circuit to only contain the primary sinusoidal

harmonics. In the context of this thesis, a digital power amplifier will accept full swing digital signals as inputs, and output digital signals with no explicit filtering.

As discussed in section 2.2.3, one technique to reduce low frequency content generated from single-ended digital power amplifiers involves capacitively combining two paths which have in-phase RF components, yet have counter-phase common-mode components which are canceled. The circuit shown in Figure 3-2 achieves this goal by driving two 2pF coupling capacitors with two separate digital PAs.

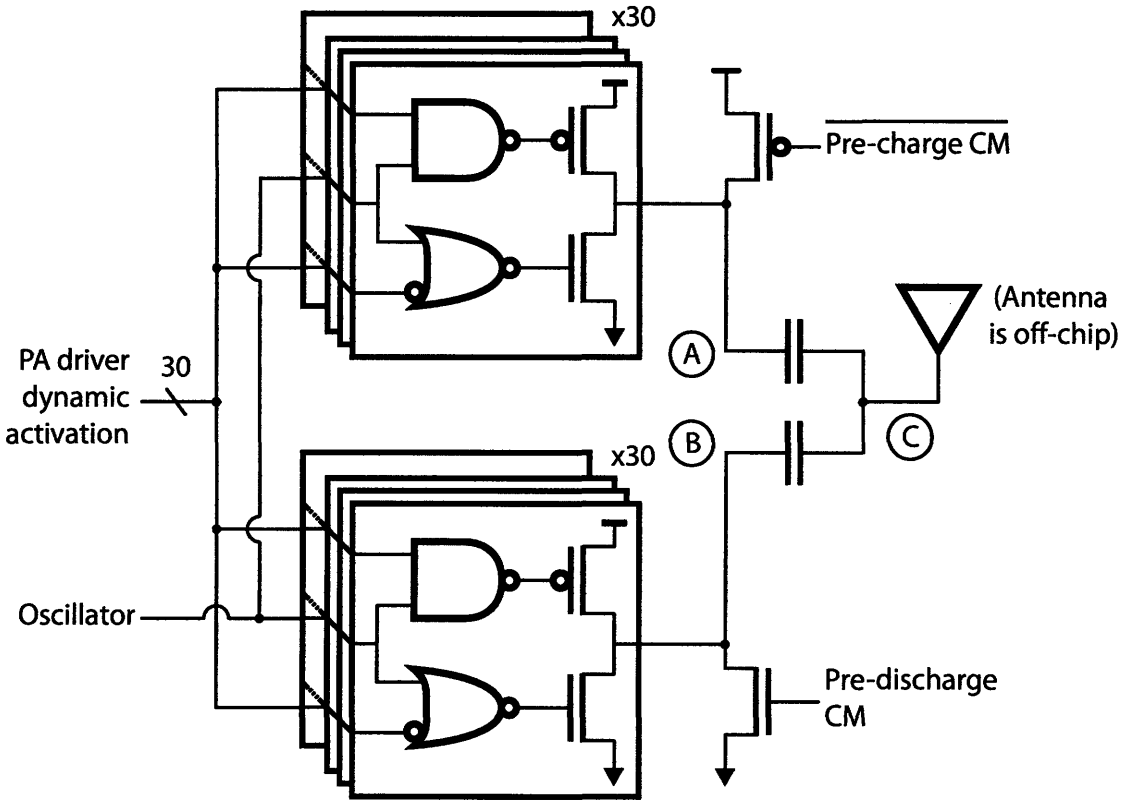


Figure 3-2: Dual digital power amplifiers.

Each PA consists of 30 tri-state inverters. A single oscillator signal is fed as an input to all 60 tri-state inverters, thus ensuring both paths receive in-phase RF signals. Each tri-state inverter is sized such that all 60 inverters operating in parallel can drive the antenna and associated parasitics up to 800mV when switching at 4GHz. Output power control can be configured by programming the number of tri-state inverters enabled at a given time. Furthermore, by dynamically adjusting the number of enabled tri-state inverters during pulse transmission, pulse shaping can be

realized. Section 3.5 discusses the implementation details of the pulse shaping logic.

The differential baseband pulses (i.e. opposite common mode low-frequency pulses) are generated by ensuring that the outputs of the two PAs are at opposite supply rails immediately before and after pulse generation. Thus, during pulse generation the two capacitively coupled paths begin to charge and discharge low-frequency content at the same rate, resulting in close to zero low-frequency content on the output.

The opposite common modes for the two PA outputs are set by pre-charge and pre-discharge transistors during idle mode between pulses (i.e. when the PA outputs are tri-stated). The dynamic PA control logic should ensure that the pre-charge and pre-discharge transistors are never turned on during pulse generation in order to avoid static power dissipation. Although not shown in Figure 3-2, each input into the capacitive combination network has both pre-charge and pre-discharge transistors that can be optionally enabled for testing purposes. It should also be mentioned that since the PA outputs can be tri-stated, the transmitter can easily share the antenna with an integrated receiver without requiring an explicit transmit/receive switch. If required, the DC voltage of node C can be set with a large resistance or inductor to GND in order to eliminate any potential build up of charge.

Figure 3-3 shows a representative timing diagram of the dual digital power amplifiers with pulse shaping applied. Since the coupling capacitors are charging and discharging at roughly the same rate, the average voltage of nodes A and B approach the same value (ideally VDD/2) during pulse generation. For this reason, a very visible low-frequency transient is seen on nodes A and B at the end of pulse generation when the pre-charge/discharge devices are turned on. If the two paths are matched and the pre-charging and pre-discharging begin at the same voltage on nodes A and B, this low-frequency transient will not be seen at the output (node C).

However, if the two paths are not matched, nodes A and B will discharge with different initial conditions, thus leading to some low-frequency content on output node C. For example, Figure 3-4(a) shows the simulated output spectrum of the dual PAs with ideally-matched paths overlaid on top of spectra generated with coupling capacitor mismatches of 20% and 30%. Even with an extreme mismatch of 30%, there

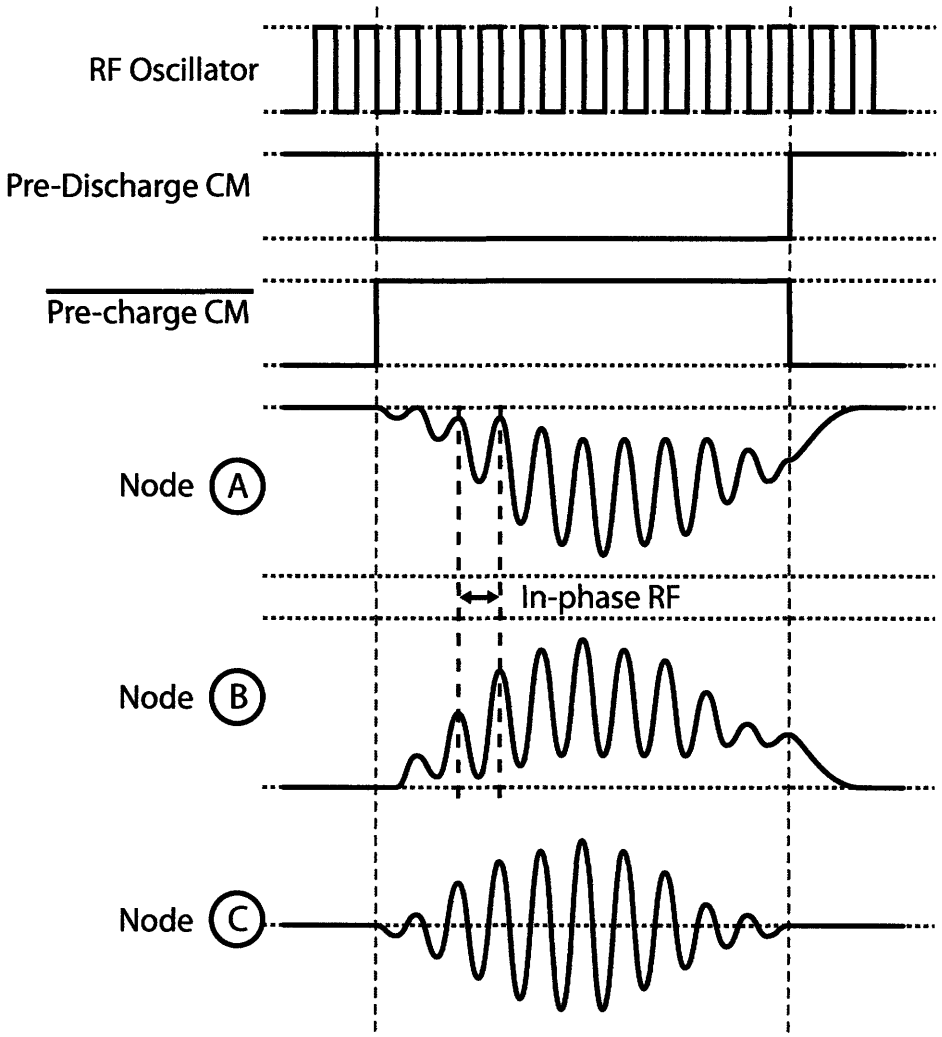
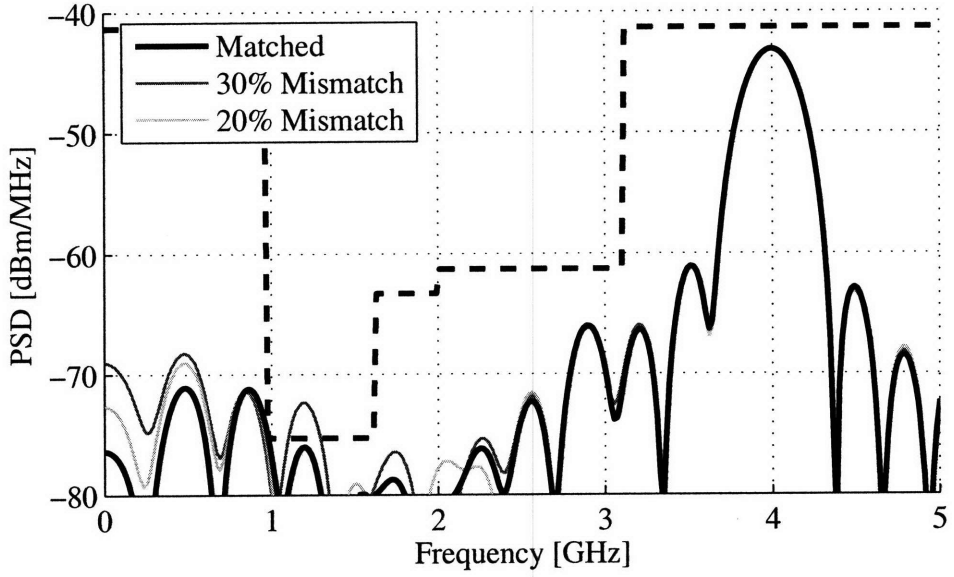


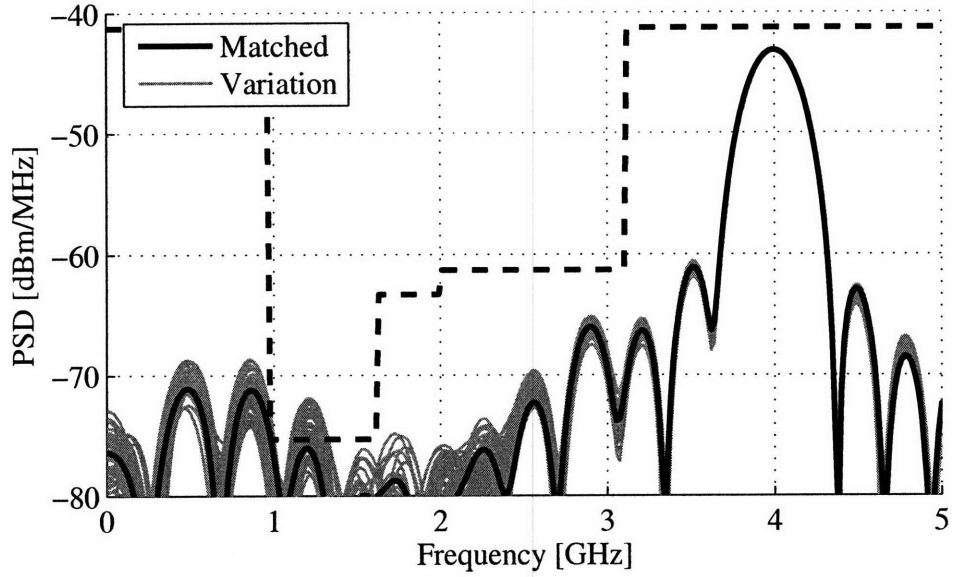
Figure 3-3: Timing diagram for the dual digital power amplifiers.

is only an 8dB degradation at DC and a 4dB degradation at 1.2GHz. A mismatch of 20% results in a 4dB degradation at DC and zero degradation at 1.2GHz. Figure 3-4(b) shows the spectra resulting from a Monte Carlo simulation of process variation and transistor mismatch. There is up to a 4dB degradation at both DC and 1.2GHz.

These simulation results are dependent on what pulse shape is used. For instance, in some cases a particular pulse shape would not meet the FCC mask under perfect matching conditions. However, after mismatch and process variation, that same pulse shape configuration was able to meet the FCC mask. Since there are relatively small spectral differences across process variation and device mismatches, a large number of pulse shape configurations should be able to guarantee, with a reasonable degree



(a)



(b)

Figure 3-4: Simulated output spectra with (a) coupling capacitor mismatch and (b) Monte Carlo process variation.

of confidence, that the FCC mask will be met. This idea of implementing *redundancy* in order to guarantee desired operation is almost necessary in high density memory design, and is becoming more popular for other types of circuits such as ADCs [47, 58]. Section 3.5 discusses pulse shaping implementation strategies.

3.3 Digitally Controlled Oscillator

Since non-coherent pulsed-UWB receivers have large input bandwidths *and* discard phase information, precise transmitter frequency tolerances are not necessarily required. To quantify this claim, consider a UWB transmitter with a 6000ppm accuracy. At a 4GHz center frequency, this corresponds to a maximum frequency error of ±12MHz. If an ideal receiver with a 500MHz brick wall input filter received a 500MHz input signal offset by 12MHz, a loss of only 0.1dB would be incurred. The situation typically improves when dealing with non-ideal signal bandwidths and filters. As an example, the system presented in [59] has a transmitter center frequency accuracy of 6000ppm. While unacceptably large for coherent and/or narrowband systems, the receiver still achieves a sensitivity of -99dBm at a BER of 10^{-3} and a data rate of 100kbps. As a result, the transmitter oscillator design requirements can be relaxed considerably with the ultimate goal of improving energy efficiency.

The proposed DCO is a three stage ring oscillator designed by Denis Daly. A schematic is shown in Figure 3-5.

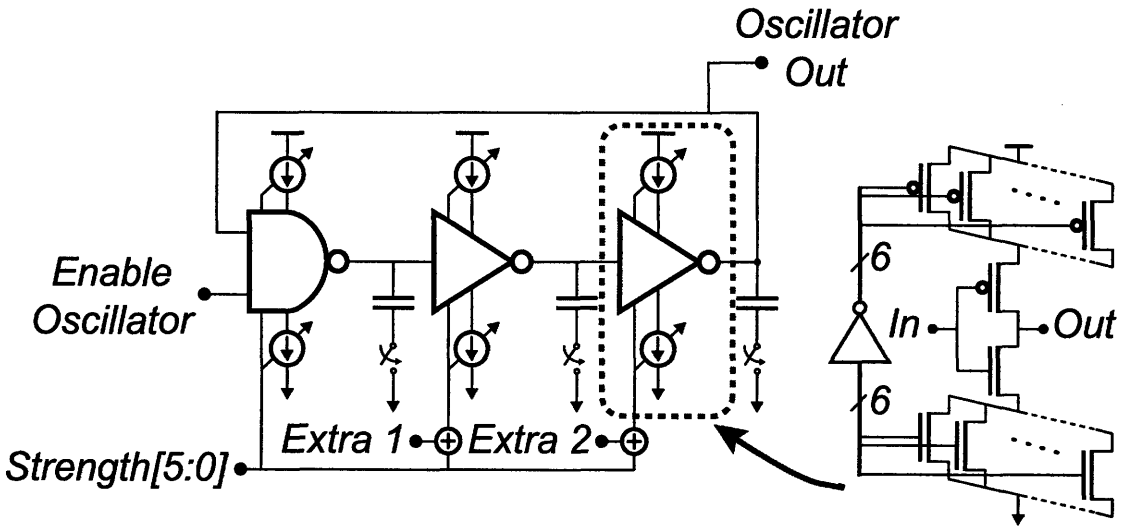


Figure 3-5: Digitally controlled oscillator.

The highly digital structure is designed to have a fast turn-on time on the order of 2ns to reduce energy consumption in duty-cycled operation. Furthermore, the delay elements are all single-ended to further reduce energy consumption over a differential

structure. Although single-ended structures are more susceptible to power supply noise compared to their differential counterparts, the resulting increase in phase noise is of negligible concern to a non-coherent energy-detecting receiver.

Coarse frequency tuning is provided by switchable load capacitors, while fine frequency tuning is provided with NMOS and PMOS current starving Digital to Analog Converters (DACs). To simplify the frequency locking algorithm, all three current starving DACs are set to the same digital value, except that the second and third stage DACs can be individually incremented by one for increased resolution. This technique results in a resolution of 7.5 bits from the DACs and 2 bits from the 3 thermometer encoded capacitors, totaling 9.5 bits.

In order to guarantee operation at the 3.5, 4.0, and 4.5GHz channels of the 802.15.4a proposal, the DCO must be over-designed to account for process variation. In this manner, the DCO targets a tuning range of 2.2-to-6.0GHz in the typical corner. Figure 3-6 shows the simulated tuning curve of the DCO at over the slow, typical, and fast design corner.

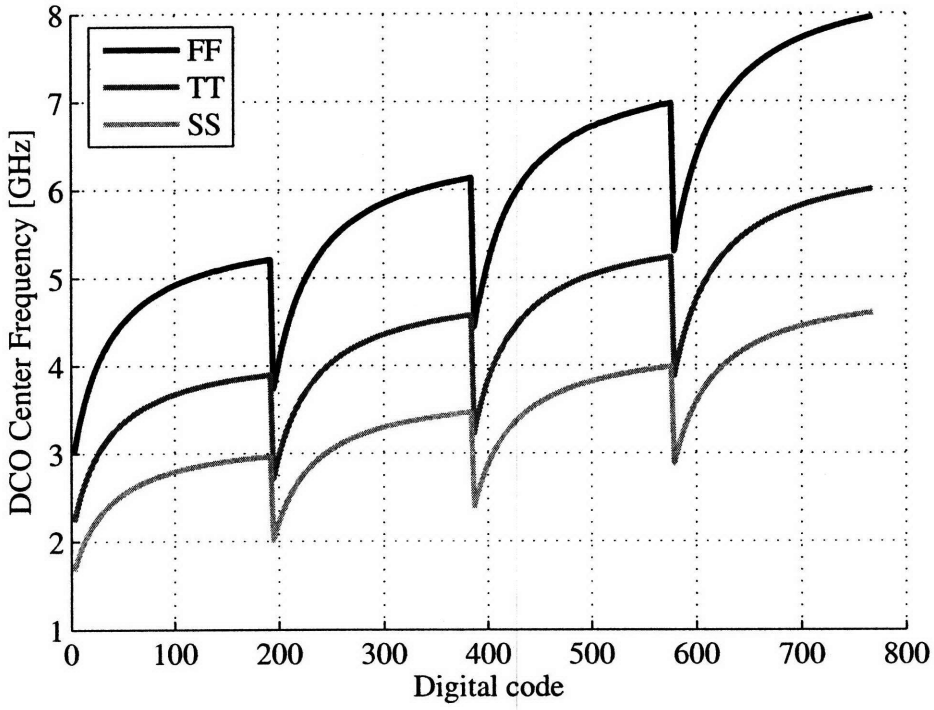


Figure 3-6: Simulated DCO output frequency versus digital code over process variation.

It is observed that all three channel frequencies are met, even under extreme process variation. The slow and fast corners achieve tuning ranges of 1.7-to-4.6GHz and 3.0-to-8.0GHz, respectively. The four regions of the tuning curves represent the four possible capacitor bank permutations.

3.4 Frequency Divider

The output of the DCO is fed to a programmable synchronous frequency divider. The divider is realized using true single-phase clock (TSPC) logic [60] in order to accommodate inputs up to 6GHz. The divider consists of fourteen half-transparent latchs (HTLs) which can be individually bypassed, thus allowing a programmable divide ratio of up to fourteen. A block diagram of the divider is shown in Figure 3-7. The design is based on the work presented in [36] and [61].

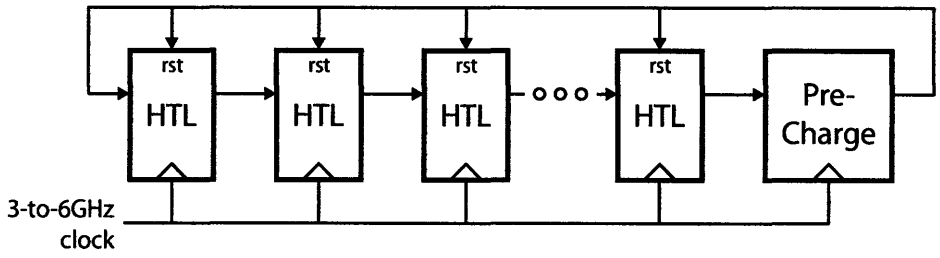


Figure 3-7: TSPC frequency divider.

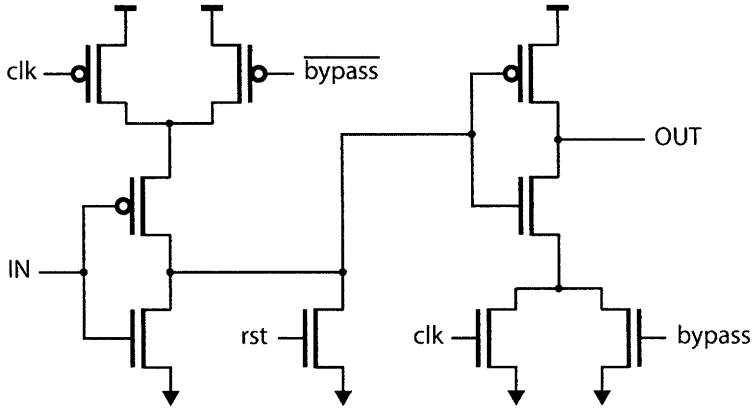
The output of the divider drives the pulse shaping circuitry, which in turn determines the effective transmitted pulse width (and thus the bandwidth). To comply with 802.15.4a standards, the transmitted pulse width is maximally set to one over the 499.2MHz PRF within a burst (i.e. 2ns). If the DCO frequency is set to one of the 802.15.4a channels, an integer division will always yield the required 499.2MHz clock. Division values for each channel in the sub-GHz and low-bands can be found in Table 3.1.

A schematic of the implemented HTL is shown in Figure 3-8(a). In bypass mode, the HTL simply behaves as two inverters. When the *bypass* input is set to logic 0, the HTL is transparent to high inputs and will only latch low inputs after a clock

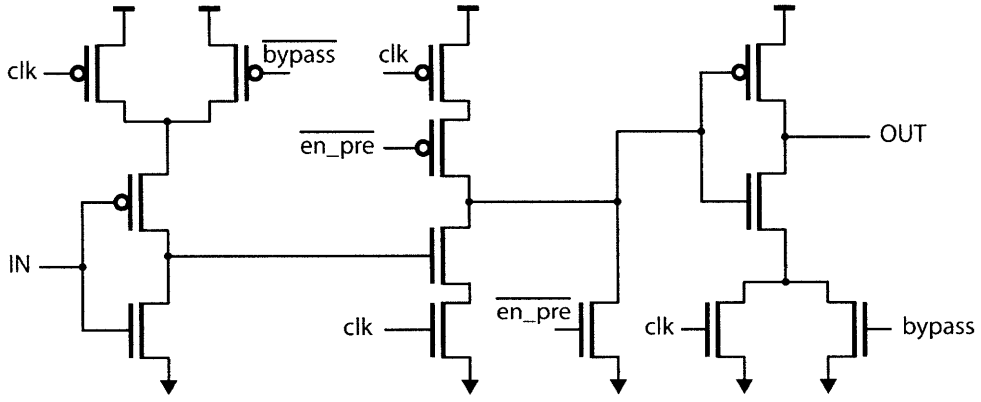
Table 3.1: Division values to obtain a 499.2MHz PRF for the sub-GHz and low-band 802.15.4a channels.

Channel	Frequency [MHz]	Divisor
0	499.2	0
1	3494.4	7
2	3993.6	8
3	4492.8	9

period delay. Therefore, if all HTLs are enabled and set to be in their transparent state (output is high), a falling edge will propagate through the network on rising edges of the clock input.



(a) Half transparent latch



(b) Pre-charge unit

Figure 3-8: Half transparent latch and pre-charge schematics.

The *rst* signal may be asserted in order to reset the HTLs back to their transparent

state. This reset sequence is performed at the start of every divide cycle by a pre-charge unit, whose schematic is shown in Figure 3-8(b). The pre-charge unit also generates the initial falling edge which propagates through the network. Since the *rst* signal is asynchronously applied to all HTLs at once, the internal divider phases do not necessarily have a 50% duty cycle, as illustrated by the simulation results in Figure 3-9. This property will be exploited in the design of the pulse shaping logic.

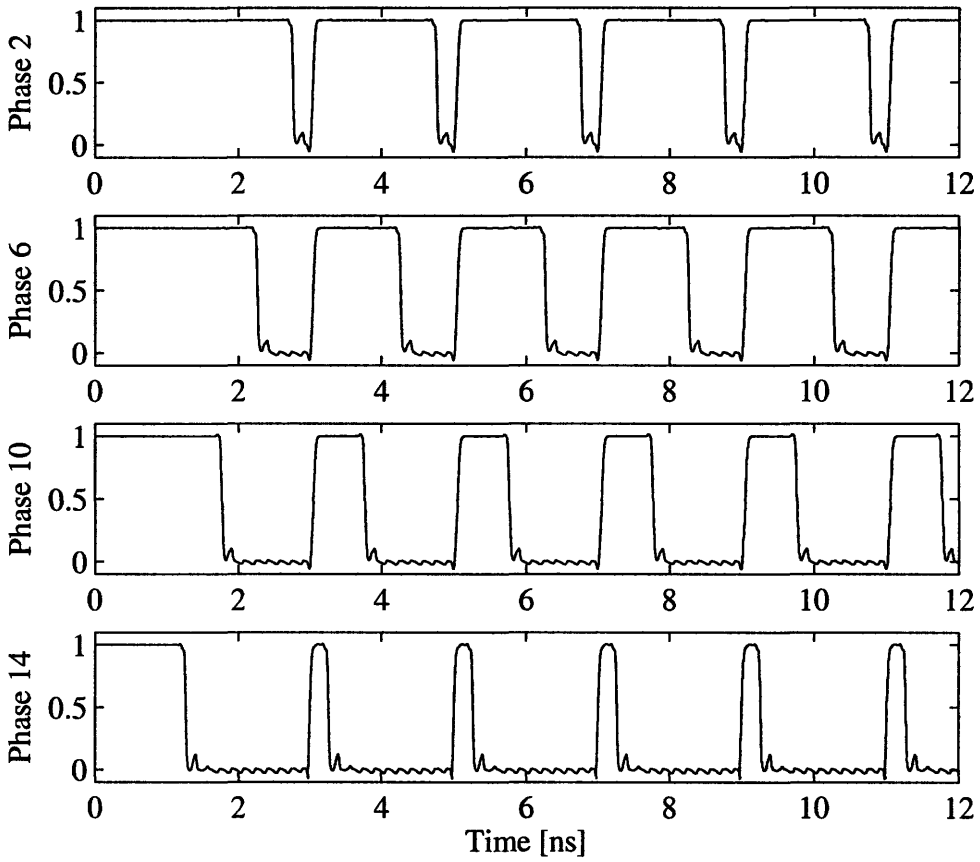


Figure 3-9: Simulations of selected phases of the frequency divider.

3.5 Pulse Shaping Logic

As described in section 3.4, the output phases of the frequency divider do not necessarily have 50% duty cycles. In fact, the duty cycles of the internal phases vary approximately linearly from 10% to 90%, depending on the divide ratio. Since the period of each phase is set to be equal to the pulse width of 2ns, it is possible to

combine several of these phases in order to generate the timing required for pulse shaping. This is illustrated in Figure 3-10, where signals Φ_{1-4} are appropriately chosen to have duty cycles of approximately 20%, 40%, 60%, and 80%, based on which HTLs are enabled or disabled.

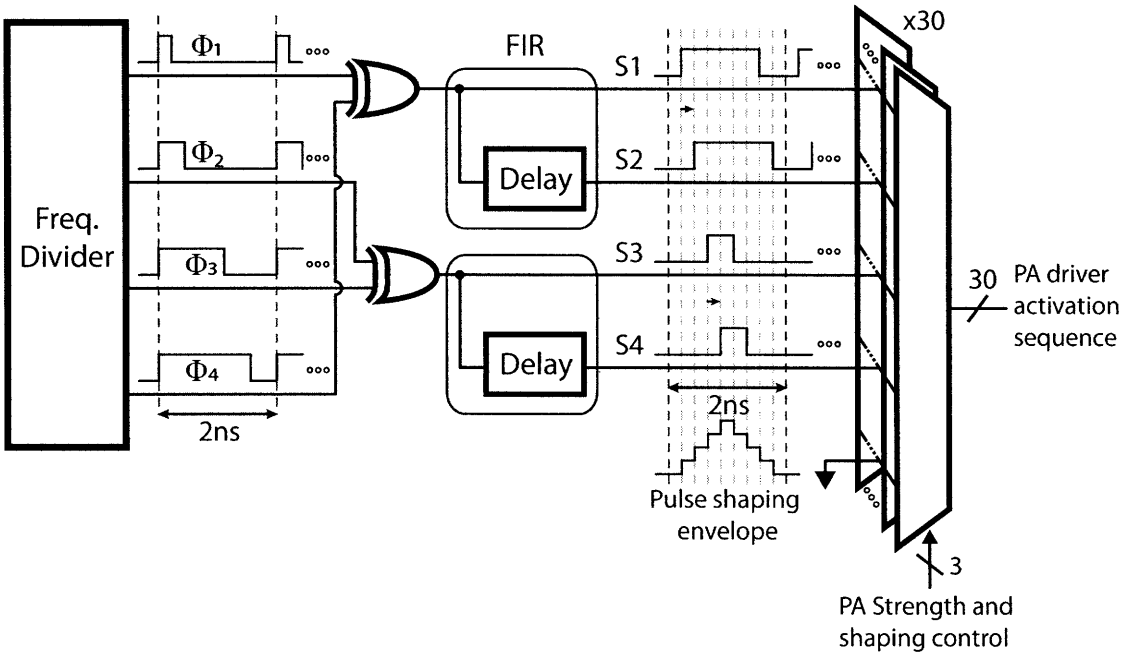


Figure 3-10: Pulse shaping logic.

By XOR-ing Φ_1 with Φ_4 and Φ_2 with Φ_3, two pulse shaping signals are generated. These two pulse shaping signals are each passed through simple one-tap finite impulse response (FIR) filters to increase the number of pulse shaping signals to four (signal S1-S4). The delay elements of the FIR filters are simply comprised of a programmable number of inverter-based buffers.

Each tri-state inverter of the dual PAs is individually programmed through a five-input multiplexer network to receive one of the four pulse shaping signals as a dynamic activation input. The fifth multiplexer input is grounded in order to allow statically disabled tri-state inverters, as the inverters are typically disabled to perform gain control. The four pulse shaping signals can be thought of as the output of FIR filter taps which are added together at the input of the coupling capacitors via the parallel combination of PA tri-state inverters. Maximum PA output swing is achieved when

all four pulse shaping signals are high, i.e. the maximum number of PA inverters are enabled in parallel simultaneously. This pulse shaping configuration also ensures that the output signal amplitude is zero during BPSK phase transitions in order to avoid common-mode glitching and inter-pulse interference.

The actual pulse shape can be modified through two different methods. One method involves changing the relative times at which the shaping signals arrive. This can be accomplished by selecting different frequency divider phases or changing the FIR filter delay element. This does not typically produce a desired pulse shape; an example is shown in Figure 3-11(a). The FIR filter delays have $2^3 = 8$ possible permutations. The second method involves changing how many tri-state inverters

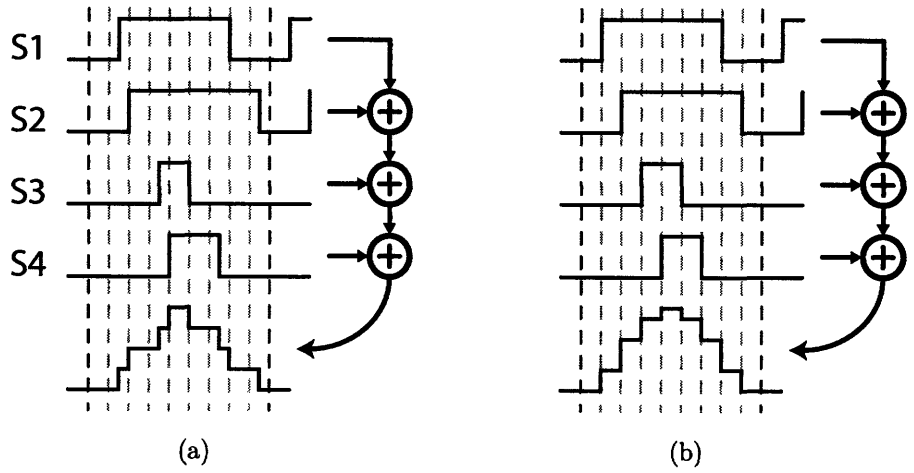


Figure 3-11: Modifying pulse shapes by changing (a) delays and (b) weights.

receive a particular pulse shaping signal. This is similar to choosing the weights of the FIR tap coefficients, and can be used to more closely approximate a raised-cosine shape [48]. An example pulse shape is shown in Figure 3-11(b). There are approximately $2^{30} \approx 10^9$ total pulse shape strength permutations. Many of these permutations are not practically useful, however as discussed in section 3.2, there are more than enough possible configurations to guarantee FCC spectral compliance with a reasonable degree of confidence.

3.6 Frequency Calibration

The transmitter contains an early/late detector which can be used for periodic frequency calibration in a frequency locked loop. An ideal early/late detector receives two edges as inputs; depending on which edge arrives first, the output is declared to be either early or late.[1] In order to calibrate the DCO center frequency using such a detector, there must be a reference input available to compare to the edges generated by the DCO. If the output edge of the DCO arrives before the reference edge, the DCO center frequency is deemed to be early and must be reduced to more closely match the reference. On the other hand, if the output edge of the DCO arrives after the reference edge, the DCO center frequency is deemed to be late and must be increased to more closely match the reference.

This sounds very much like the operation of an elementary PLL. The key difference is that the early/late detector only produces one bit of *edge difference* information, whereas PLLs typically generate several bits (or an analog value) of *phase and frequency* information. Thus, an integer-N PLL can achieve phase and frequency lock, whereas an FLL using an early/late detector can never achieve true lock, as the edges will still always be either early or late.[2] However, at the cost of reduced frequency resolution, early/late detector implementations for periodic frequency calibration are typically much simpler than their PLL counterparts. For non-coherent systems where a precise phase and frequency are not critical, this is a worthwhile trade-off.

It should be noted that it is in fact possible to use an FLL for coherent systems where precise phase and frequency are very important. This is accomplished by ensuring the oscillator startup sequence is identical at each activation. In this manner the phase is aligned to the reference clock at the start of transmission. If the accumulated jitter over the course of transmission is low[3], then only the frequency needs to

[1]This describes a 1-bit early/late detector. It is possible to increase the resolution and create multi-bit early/late detectors, though these are often grouped into the area of time-to-digital converters.

[2]Depending on the circuit implementation, if two edges arrive at exactly the same time the early/late detector may enter metastability, thus potentially providing a "locked" condition. It is not recommended to pursue this strategy.

[3]This is often the case for duty-cycled pulsed-UWB.

be compensated by the loop. Such systems are called phase-aligned frequency-locked loops (PA-FLLs) [36].

As is the case with PLLs, it is beneficial in an early/late detector loop to divide the local oscillator signal and compare it with a low frequency reference. In this manner, the low frequency reference can be very precise without dissipating a large amount of switching power. In the designed transmitter, the low frequency reference is the off-chip *Start-TX* signal. A simplified schematic and timing diagram of the early/late sensing scheme is shown in Figure 3-12.

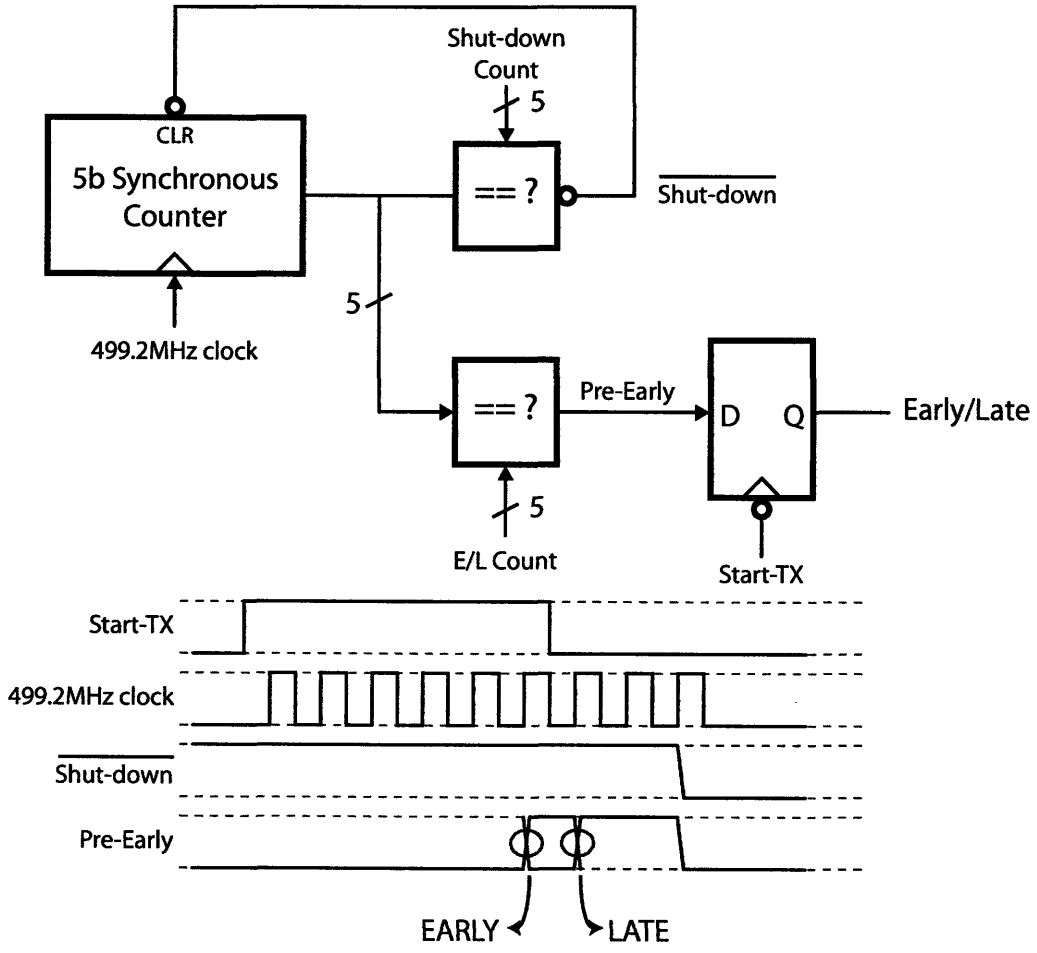


Figure 3-12: Early-late and counting logic used for frequency calibration.

As described in section 3.1, the rising edge of *Start-TX* triggers pulse generation by first enabling the DCO. The DCO drives a frequency divider which should ideally generate a 499.2MHz signal. This divided frequency output drives a 5-bit synchronous

counter, which can also be thought of as a frequency divider programmable to divide by integer values 1 through 32. The 5-bit output of the synchronous counter is compared to a programmable *E/L Count* register. When the two values are equal, the *Pre-Early* output latches high. If this occurs before the falling edge of *Start-TX*, the DCO is considered to be early. Otherwise, the DCO is considered to be late. When transmitting data at symbol rates of 15.6MHz, an *E/L Count* value of 16 will ideally trigger a transition at the same time as the falling edge of *Start-TX*, assuming a 50% duty cycle.[4]

The output of the synchronous counter is also compared to a programmable *Shut-down Count* register. Once the two values are equal, the *Shut-down* signal is asserted and all blocks are reset. For proper operation, *Shut-down Count* must always be greater or equal to *E/L Count*. The purpose of having a *Shut-down Count* is to give circuitry in other parts of the system time to finish their operations. The timing diagram of Figure 3-12 has *E/L Count* equal to six or seven, and *Shut-down Count* is set to nine.

3.7 Linear Feedback Shift Register

The transmitter employs BPSK scrambling in order to smooth out spectral lines associated with non-phase modulated PPM signaling. The scrambling output is generated by a 15-bit pseudo-random sequence, defined by the following generator polynomial:

$$g(D) = 1 + D^{14} + D^{15}, \tag{3.1}$$

where D is a unit delay element. The lower block in Figure 3-13 shows the implementation of this generator polynomial. If the initial condition of the scrambler is set to the sequence $(s_0, s_1, ...s_{14}) = 0011111111111111$, then the LFSR output complies with the 802.15.4a spreading sequence [29].

As discussed in section 2.3.4, the attainable communication distance of low-rate

[4]This is also assuming the DCO starts up instantaneously. In reality, a few cycles are added on to accomodate for the DCO turn-on time.

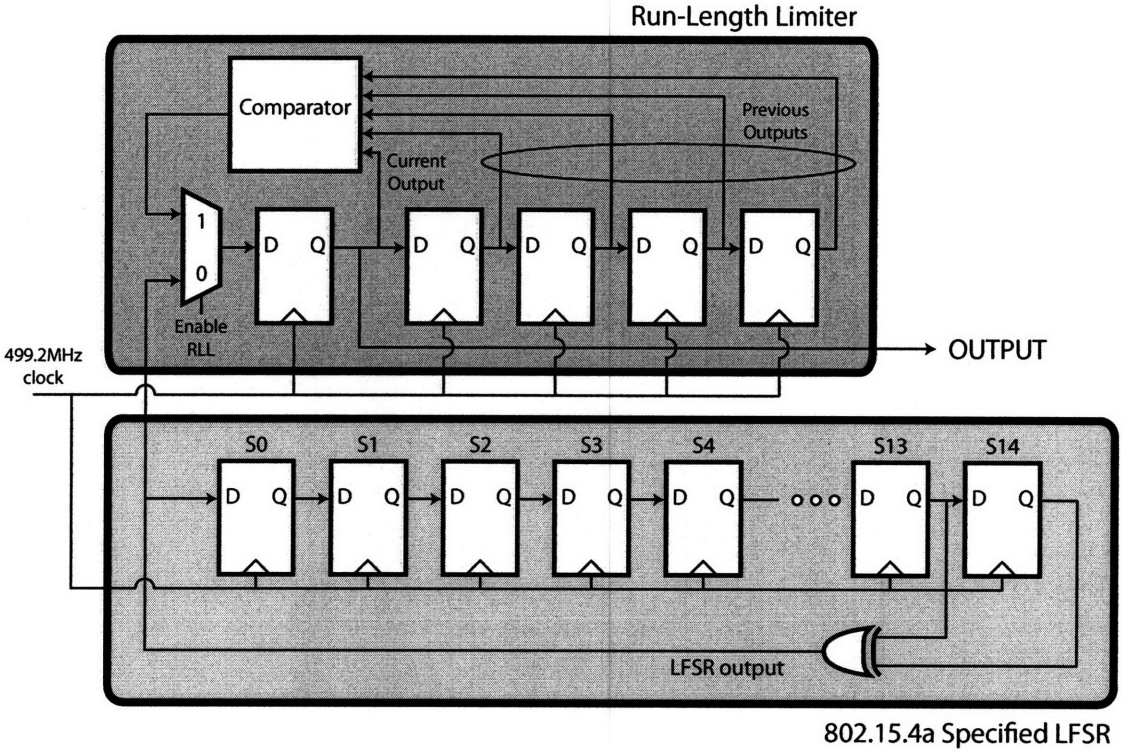


Figure 3-13: LFSR scrambler with run length limiting for peak power reduction.

UWB systems can be extended under FCC limits by reducing the peak power. This can be accomplished by applying run length limits on the phase modulation sequences. Run length limits can be introduced in the scrambler by monitoring current and previous output values. If a run of a pre-programmed length is detected, the run length limiter can intentionally introduce an output of opposite value to that particular run. The proposed transmitter includes support for maintaining run length limits of three, four, and five. Alternatively, there is an option to disable run length limiting altogether. A circuit used to detect and correct run lengths is shown in the upper block of Figure 3-13.

The scrambler is clocked at the transmitted pulse rate of 499.2MHz. Each register can be programmed to have a specific initial condition. Note that since the output of the scrambler is one cycle delayed from the output of the LFSR, a different initial condition is required if the scrambler is to follow the 802.15.4a spreading sequence. Alternatively, the first output from the scrambler can simply be discarded.

Chapter 4

Measurement Results

4.1 Overview

The transmitter was fabricated in a 90nm CMOS process by STMicroelectronics. The design uses a combination of foundry-supplied standard cells and full custom layout. The chip was packaged in a 40-lead, wirebonded QFN package; all measurement results were taken from the packaged chip. A die photograph is shown in Figure 4-1. Note that there is also a receiver designed by Denis Daly integrated on the same chip. The highlighted areas on the die photograph show the transmitter core, and the DCO and shift register which are shared between the transmitter and receiver. The transmitter core and DCO consume an area of $0.07mm^2$.

The transmitter was tested using a Field Programmable Gate Array (FPGA) to generate digital inputs. Synthesized on the FPGA were code modules used to generate *Start-TX* edges, perform frequency calibration, and program shift register bits. The FPGA is clocked by a high accuracy crystal for precise baseband timing. To facilitate easy human interaction for testing, the FPGA was interfaced with Matlab and a custom graphical user interface was designed.

The transmitter operates at data rates from 0-to-15.6Mbps on a 1V power supply. It has a quick turn-on time of 7.2ns, measured as the time it takes pulses to appear at the output of the dual PAs after the rising edge of *Start-TX* has arrived.

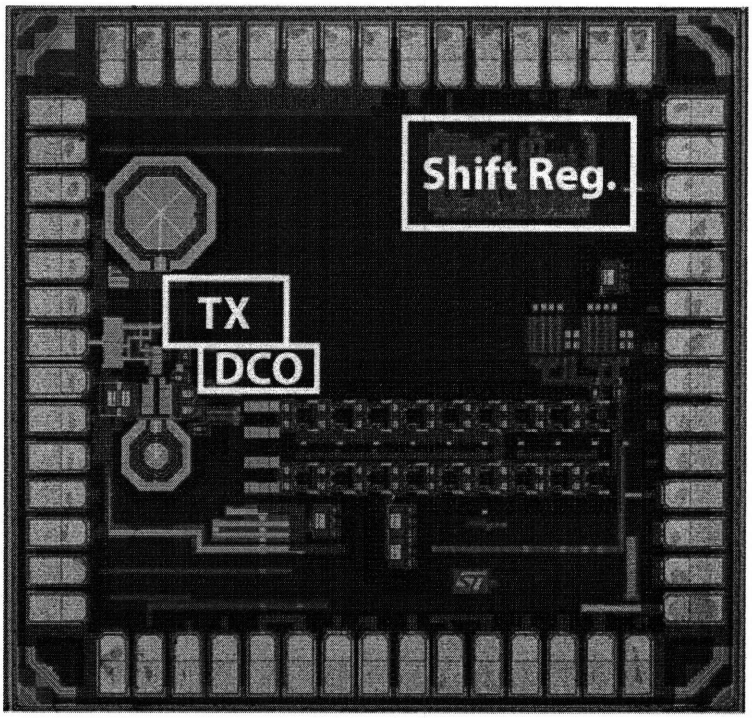


Figure 4-1: Die photo of fabricated transmitter.

The following sections detail the measured results of several key blocks in the transmitter.

4.2 Dual Digital Power Amplifiers

4.2.1 Transient Results

Time domain measurements of the output of the capacitive combination network were taken using a Tektronix TDS 8000 Sampling Oscilloscope with an 80E04 sampling module.

Figure 4-2 shows the output when the transmitter is configured to generate one pulse at a time. Figure 4-3 shows the output when the transmitter is configured to generate a burst of five individually BPSK-modulated pulses at a time. In this particular example, the BPSK modulation code sequence is $(+1, -1, -1, +1, -1)$. Note that there are no large low-frequency turn-on transients for either the single pulse or pulse burst cases. However, it appears there is a very small turn-off transient

for both cases. This is most likely due to the fact that the pre-charging and pre-discharging rates and initial conditions are not matched between the two capacitively coupled paths. Still, the transient content is much smaller than the result of simply capacitively coupling a single-ended digital circuit to the output. It is of course difficult to quantify the effects of these turn-off transients in the time domain. Section 4.2.2 offers a frequency-domain perspective of these (or similar) pulses.

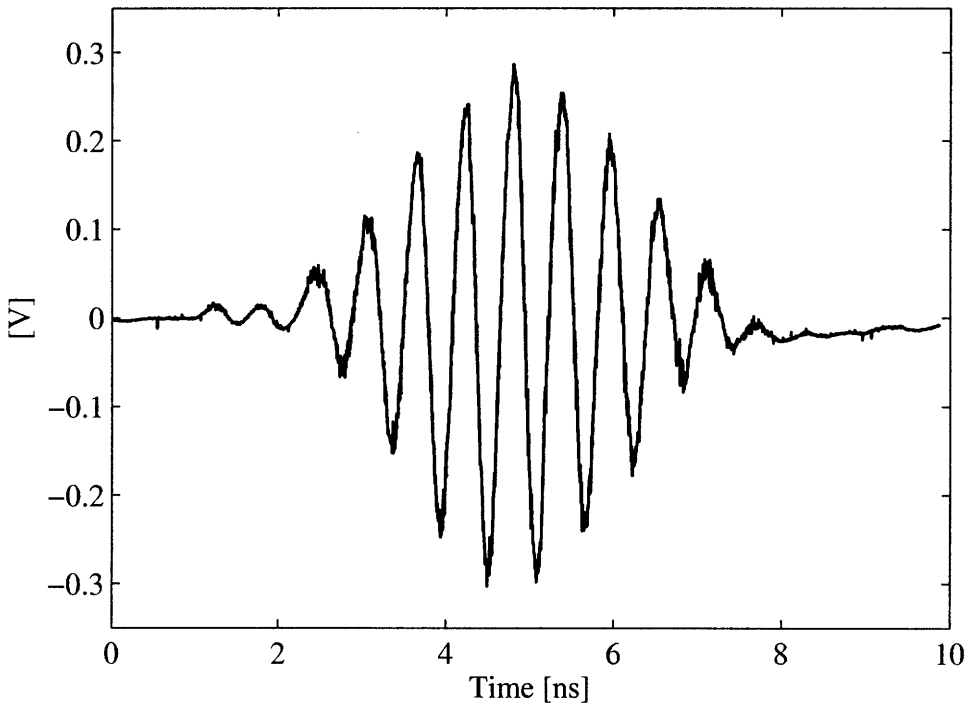


Figure 4-2: Measured transient waveform of a single pulse.

Figure 4-4 shows the output of the dual PAs when the TDS 8000 is in envelope detect mode. From this plot, it is possible to view the four discrete pulse shaping levels. Note that the BPSK modulation code sequence is different than in Figure 4-3. In this case it is $(+1, +1, -1, +1, -1)$.

The dual PAs were measured to have an output voltage swing range from 160-to-710mV, resulting in an output power control range of 13dB.

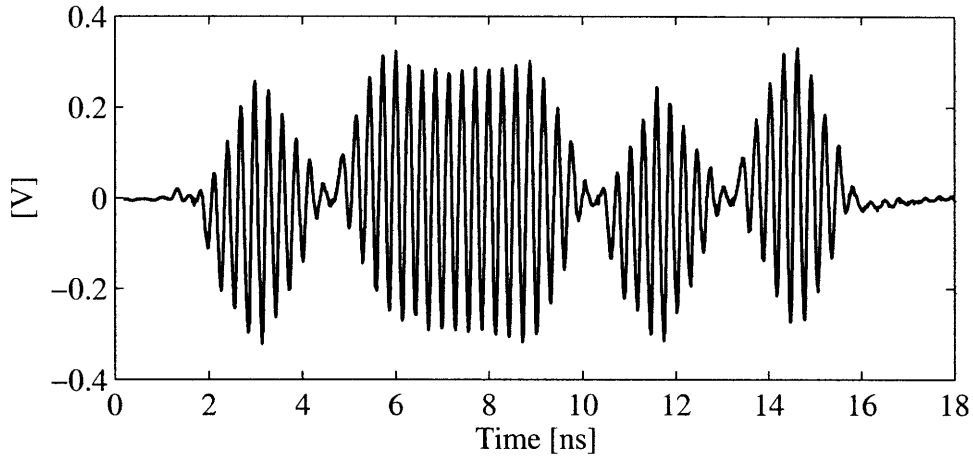


Figure 4-3: Measured transient waveform of a burst of five individually BPSK-modulated pulses.

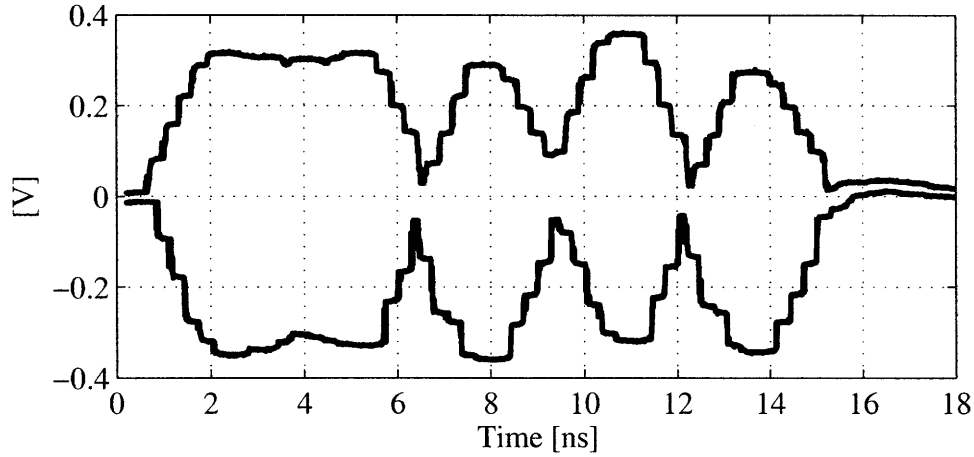


Figure 4-4: Measured envelope of a burst of five individually BPSK-modulated pulses.

4.2.2 Spectral Results

Frequency domain measurements were taken at the output of the capacitive combination network using an Agilent MXA N9020A Spectrum Analyzer. Unless otherwise noted, the resolution bandwidth was set to 1MHz to generate the correct units of dBm/MHz for comparison to the FCC spectral mask. Also, the SA detector was typically set to Root Mean Square (RMS) averaging mode.[1]

[1]Slightly older spectrum analyzers, such as the Agilent 8564EC, often used a logarithmic averaging detector instead of an RMS detector. This is troublesome when measuring very low duty-cycled pulses, as the logarithmic detector places more weight on the long zero-input signal, thus severely underestimating the actual average power spectral density.

During normal operation, the proposed transmitter achieves both indoor and outdoor FCC spectral compliance in all three channels comprising the low-band of the 802.15.4a proposal. The resulting spectra for sixteen-pulse bursts are superimposed together over the FCC spectral mask in Figure 4-5. Note that no off-chip filters were used to make this measurement.

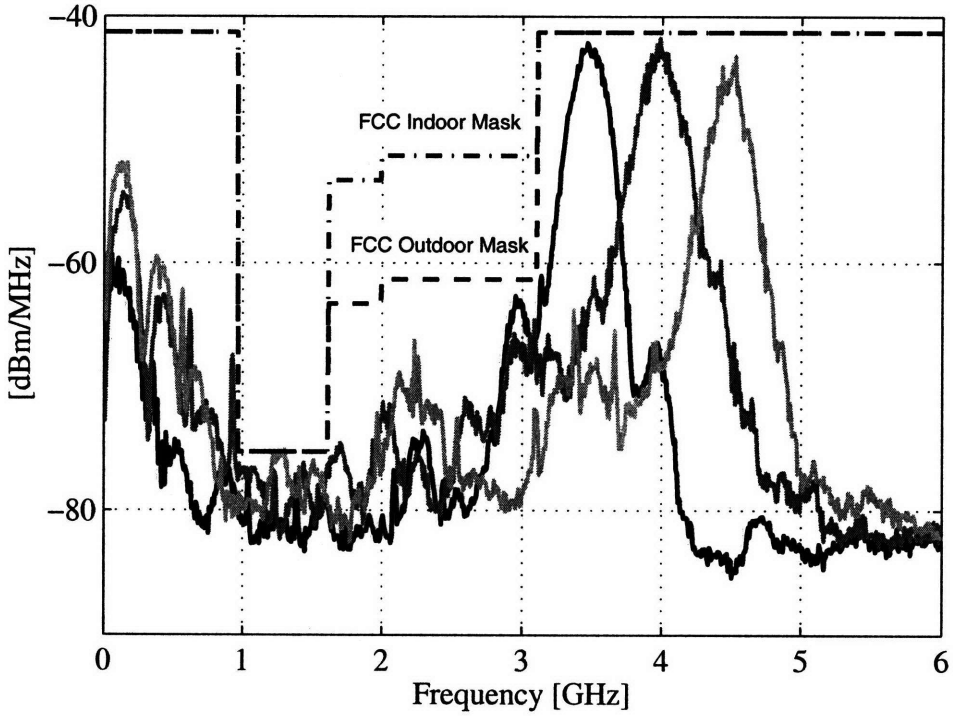


Figure 4-5: Overlaid power spectral densities of the three channels in the low-band of the 802.15.4a proposal.

As suspected in section 4.2.1, it is observed that some low-frequency content does make it to the output of the capacitive combination network. The low-frequency content is, however, sufficiently attenuated to meet the FCC spectral mask. To determine how effective capacitive combining and pulse shaping are at reducing both low frequency content as well as RF sidelobes, Figure 4-6 shows the output power spectral density of two-pulse bursts with:

- capacitive combining and no pulse shaping,
- pulse shaping and no capacitive combining, and

- capacitive combining and pulse shaping.

Note that disabling capacitive combining can be achieved by simply pre-charging (or dis-charging) the inputs of the capacitive combination networks to the same voltage during idle mode between pulses. This way, the low-frequency baseband pulses are in-phase instead of differential. Alternatively, only a single PA driver can be enabled.

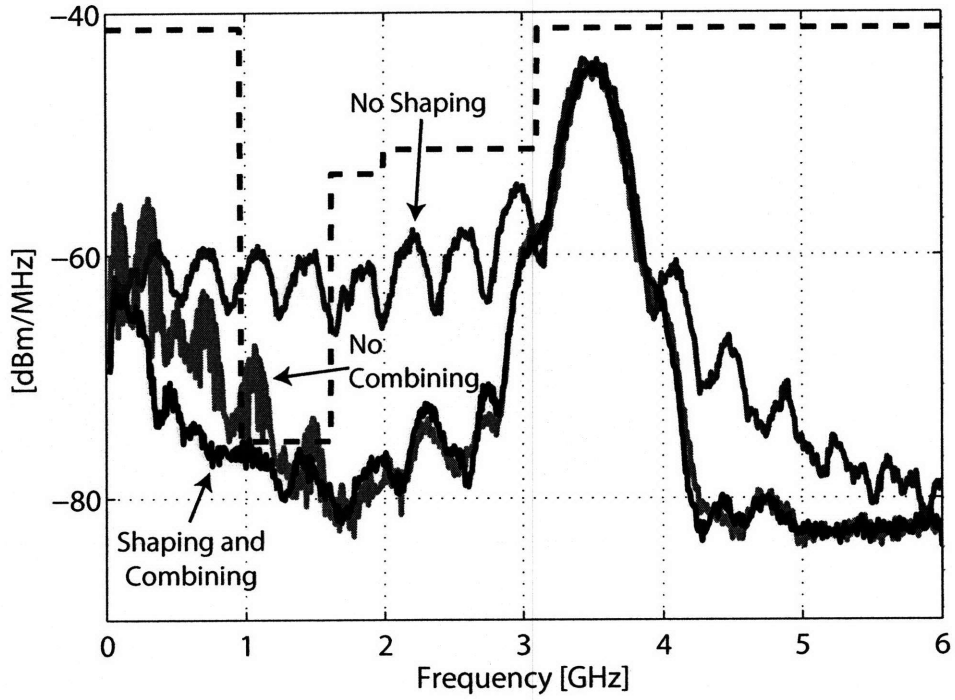


Figure 4-6: Overlaid power spectral densities with shaping disabled, combining disabled, and normal operation.

It can be seen here that capacitive combination achieves up to 12dB of low-frequency attenuation. Furthermore, pulse shaping achieves 15-to-20dB of sidelobe rejection.

It should be noted that the effect of capacitive combination is more pronounced for bursts containing few pulses. Since bursts with many pulses have more time to settle the average DC voltage across the coupling capacitors, the power around the carrier frequency increases in proportion to the low frequency content. In other words, every time pulse generation begins and ends, low-frequency content is generated by charg-

ing and discharging the average DC voltage across the coupling capacitors. When transmitting a single pulse at a time, there is an overhead cost for every pulse. When bursting several pulses at a time, there is only an overhead cost for the entire burst. Thus, for an equivalent output power around the carrier, bursting many pulses will always result in less low frequency content.

That being said, it is still beneficial to support single pulse transmission, as a non-coherent receiver may be designed with a short integration window in order to provide increased ranging resolution. Furthermore, in extreme multi-path environments it is often beneficial to transmit only a few pulses at once, as the channel may spread a considerable amount of energy over the receiver's entire integration window.

Figure 4-7 shows six of the sixteen programmable gain settings in the 3.5GHz channel, resulting in 13dB of output power scaling. Since all tri-state inverters were sized to have the same drive strength, the increase in gain through parallel combination is linear.

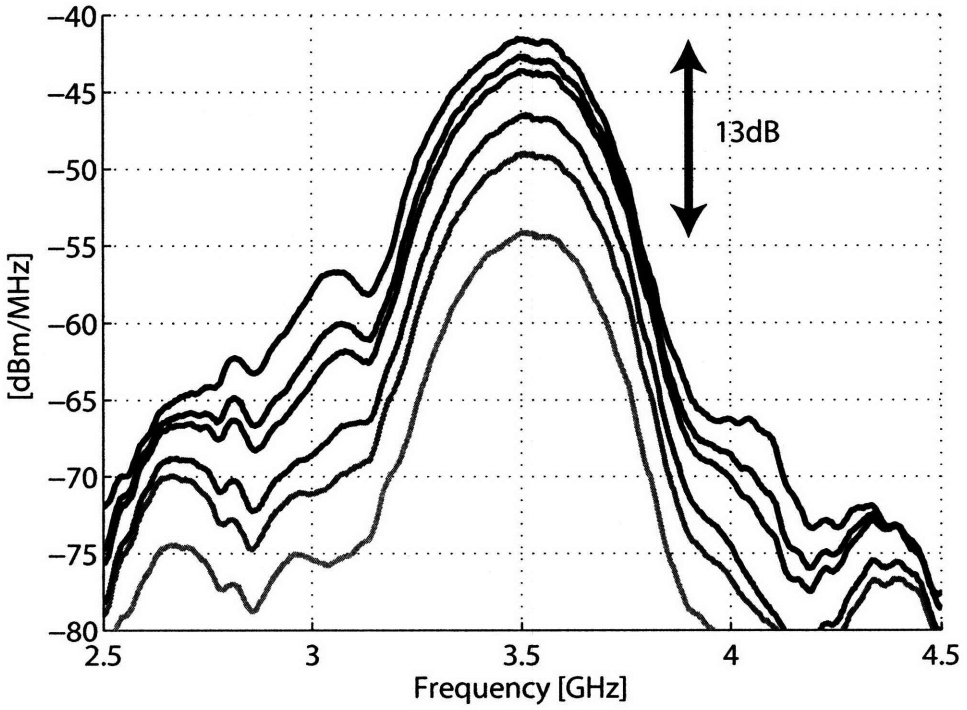


Figure 4-7: Power spectral densities of six of the sixteen gain settings in the 3.5GHz channel.

The effects of run length limiting on peak power can be seen for bursts of 16 pulses in Figure 4-8. For this measurement the spectrum analyzers RBW should ideally be set to 50MHz in order to comply with FCC regulations. However, the maximum RBW on the N9020A (with no extra options) is 8MHz. In this case, the FCC recommends measuring peak power in the highest RBW available. Then, the maximum output value is set using the conservative formula shown in section 2.3.1. The limit for an 8MHz RBW is $20log$(8MHz/50MHz) = -15.9dBm.

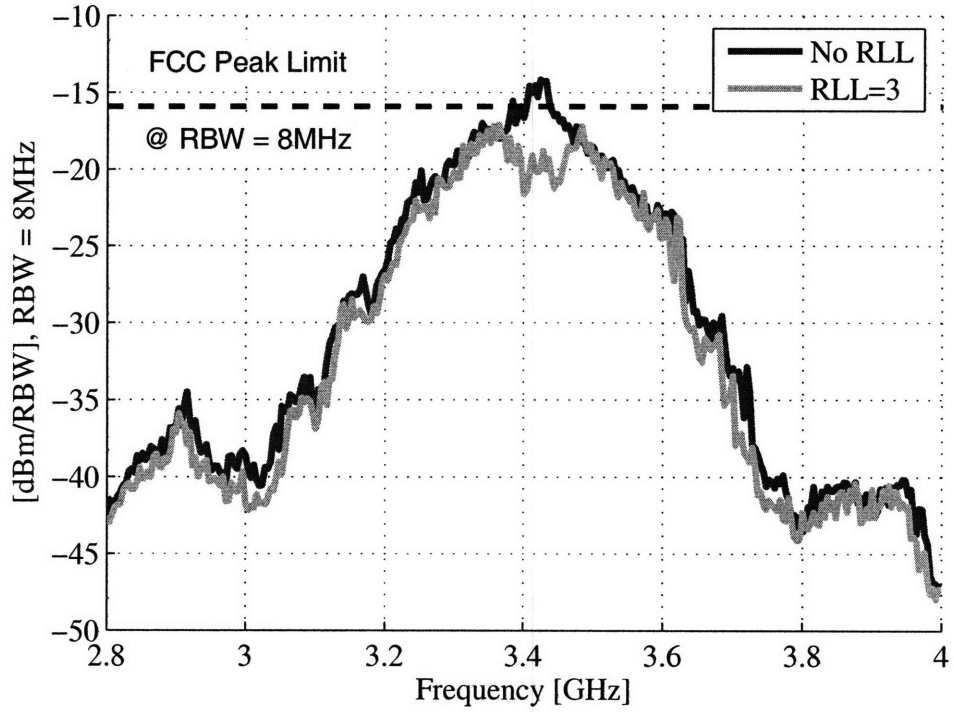


Figure 4-8: The effects on peak power when setting RLL=3 for bursts of 16 pulses.

In this measurement, the spectrum analyzers RBW is set to 8MHz, and the detector is set to peak-hold mode. The output is fed to the SA for several minutes to ensure the maximum peak powers in each frequency bin are observed. It is shown that a run length limit of three for sixteen-pulse bursts reduces the peak power by 3dB. This occurs by spreading peak power away from the carrier frequency. This result is in good agreement with the theory presented in section 2.3.3, as a length-sixteen burst has $\tau_{b,max} = 16\tau_c$ without run length limiting, yet has $\tau_{b,max} = 8\tau_c$ when RLL=3, representing a 3dB decrease in peak power.

4.3 Digitally Controlled Oscillator

The digitally controlled oscillator exhibited a tuning range from 2.1GHz to 5.7GHz, which is more than sufficient to cover the three low-band channels of the 802.15.4a proposal. The measured and simulated tuning curves are shown in Figure 4-9. It can be seen that the fabricated chip is closest to the typical corner.

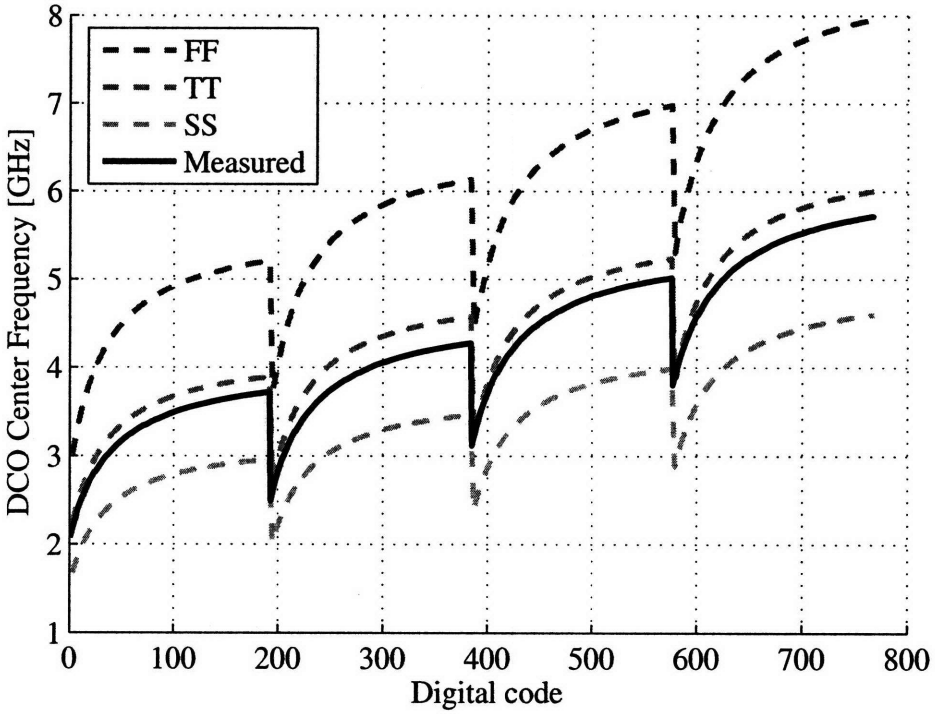


Figure 4-9: Measured DCO tuning curves compared to simulated results.

The available step sizes for each attainable frequency are shown in Figure 4-10. The maximum step size is 15MHz at a carrier frequency of 4.313GHz. The worst-case tuning accuracy is measured to be 2300ppm.

A successive approximation algorithm for frequency calibration was implemented on the FPGA. The algorithm converges in 12 cycles, or 0.77μs when operating at 15.6MHz. Since only an early/late detector is used, obtaining the exact DCO frequency cannot be guaranteed after calibration. Instead, the algorithm converges to within one digital code of the desired frequency. As discussed in section 3.3, this is more than sufficient for non-coherent UWB systems.

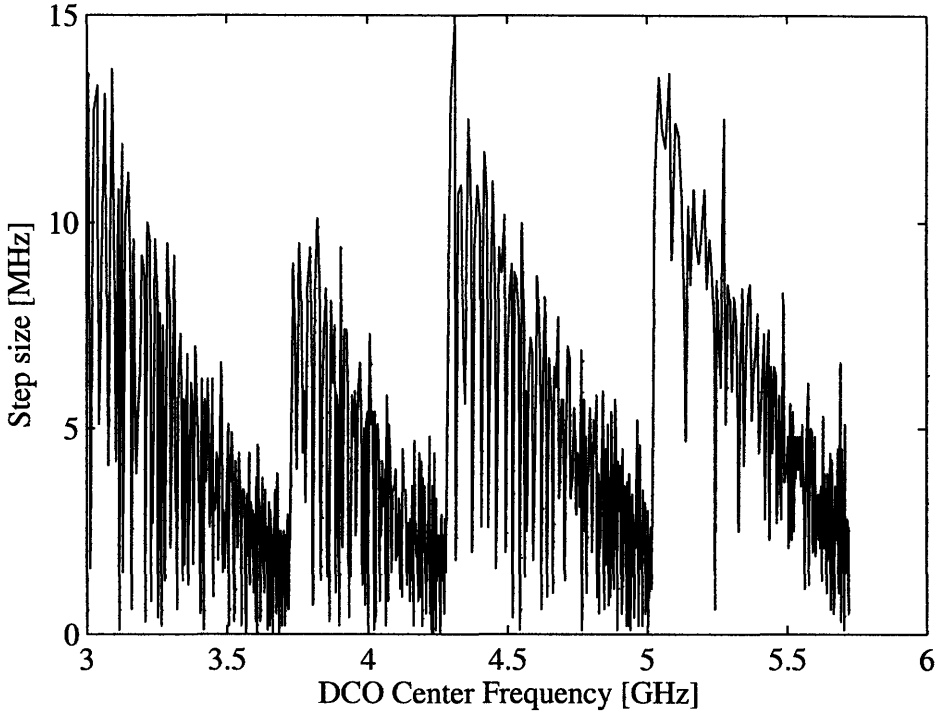


Figure 4-10: Measured DCO step sizes for center frequencies from 3-to-5.7GHz.

4.4 Summary of Results

Operating on a 1V supply, the transmitter draws 4.36mW when generating 16-pulse bursts at an SRF of 15.6MHz. The total output in this configuration is -16.4dBm. This results in an energy efficiency of 280pJ/burst, or 17.5pJ/pulse. Since all transmitter circuits are inherently off between pulse transmissions, the power consumption scales with data rate. However, the impact of leakage power becomes significant at symbol rates below 1MHz. The standby (i.e. idle-mode) leakage power is 123μW. Table 4.1 summarizes the transmitter's performance.

It should be noted that since the transmitter is integrated with an on-chip receiver, several of the power domains are shared. Thus, the leakage of the PA, DCO, and shift register power domains includes leakage from several receiver blocks.

The DCO, clock distribution, and control power domain consumed roughly 88% of the active energy in the transmitter. This power domain included the DCO, frequency divider, early/late loop, pulse shaping logic, LFSR, and some miscellaneous control

Table 4.1: Transmitter Performance Summary

Specification	Value	
Process	90nm CMOS	
Active Die Area	0.07mm^2	
Modulation	PPM+BPSK	
SRF Range	0-to-15.6MHz	
Supply	1V	
	Standby Power	Active E/pulse
Power Amplifier	22μW	2pJ
DCO/Clock/Control	83μW	15pJ
Shift Register	11μW	-
I/O and ESD	7μW	<1pJ
Total	123μW	17pJ
Output Voltage Swing	165mV-to-710mV	
DCO Frequency Range	2.1GHz-to-5.7GHz	
Turn-on Time	7.2ns	
Symbol Rate (SRF)	100kHz	15.6MHz
Energy/16-pulse-burst	1.6nJ	280pJ
Energy/pulse	103pJ	17.5pJ
Total power	164μW	4.36mW
Output power	-25dBm	-16.4dBm

logic. These blocks constitue the majority of the transmitter, thus accounting for the large active energy consumption. Furthermore, sharing the DCO with the on-chip receiver increased the overall wire lengths of high speed signals, which adds extra CV^2f power in addition to requiring extra buffer insertion.

4.5 Comparisons to Other Works

The proposed transmitter compares favorably to other published works in terms of energy consumption and power dissipation. Figure 4-11 illustrates the energy per pulse of the transmitter compared to other recently published work.

It should be noted that the total output power of the transmitter was set to be as close as possible to -16dBm for all measurements in order to obtain maximum output power under FCC limits. Due to the limited output swing of the dual power

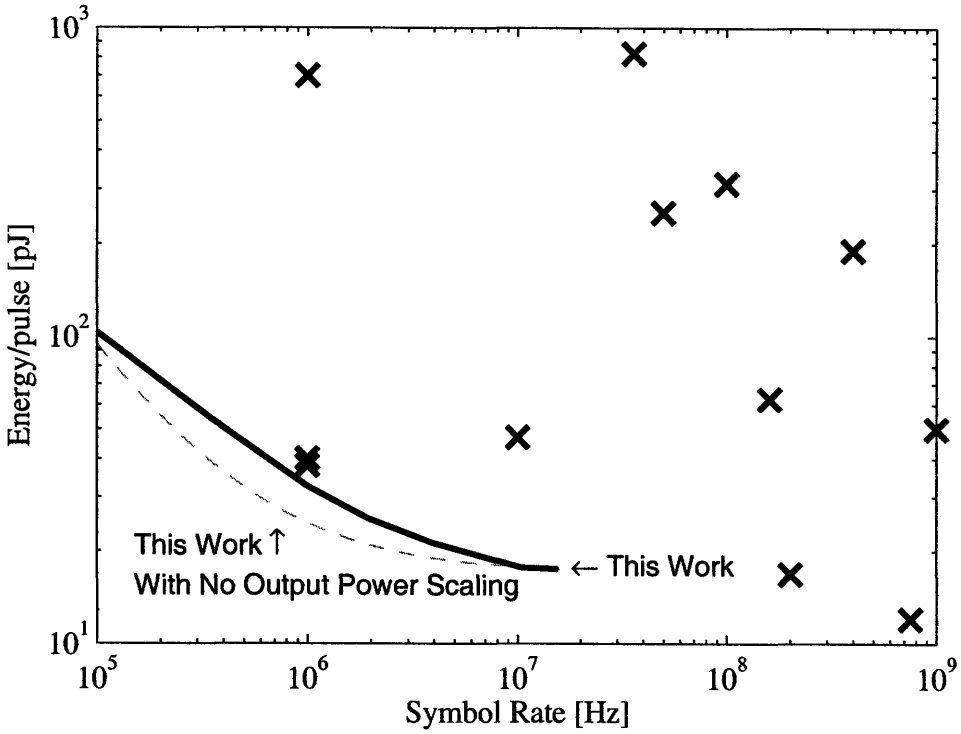


Figure 4-11: Energy per pulse for the proposed transmitter compared to the transmitters described in [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12].

amplifiers, -16dBm total output power could not be reached for symbol rates under 500kHz. For these measurements, the maximum PA gain was chosen.

The dashed line in Figure 4-11 illustrates the effective energy per pulse if the transmitter output power was not scaled with symbol rate, but instead retained the PA gain settings of the 15.6MHz symbol rate measurement. The two curves converge asymptotically as the symbol rate scales downwards; this occurs because average active power approaches zero and leakage power remains unchanged. Note that if power gating were applied, the knees of the energy per pulse curves would occur at much smaller symbol rates due to reduced idle-mode leakage currents. This would result in a power consumption that scales close to linearly with symbol rate. However, the overhead associated with charging and discharging the power-gated supply rails could be significant and would thus have to be taken into account.

Chapter 5

Conclusion

5.1 Thesis Summary

Ultra-wideband systems are uniquely positioned to explore trade-offs not typically available in narrowband design. For instance, the enormous bandwidth available to UWB systems combined with non-coherent signaling relaxes center frequency tolerances and enables the design of highly digital architectures. These architectures have the potential to offer superior energy efficiency at the cost of reduced receiver SNR. For low-rate, short-range, and energy-starved applications such as sensor networks and medical monitoring, the increased energy efficiency is a welcome trade-off compared to maximizing spectral efficiency. Furthermore, these highly-digital architectures enjoy the advantage of being more amenable to scaling in deep submicron CMOS technologies compared to their analog counterparts. This promises to be a significant advantage moving forward, especially in terms of cost certainty.

This thesis presented arguments for why digitally-based UWB pulse generators are excellent architectures to choose when the minimization of area and energy consumption is important. It was shown why pulse shaping is important for spectral compliance reasons, and methods to reduce low-frequency content generated by digitally-synthesized pulses were presented. Mathematical tools were introduced and used to predict spectral measurements for pulsed-UWB signals. Applying these tools led to a technique which can reduce peak power emissions and extend communication distance

for low-rate UWB systems.

To demonstrate these ideas, this thesis presented the design and implementation of an all-digital ultra-wideband transmitter for non-coherent communication. Fabricated in 90nm CMOS, the transmitter consumed zero static bias current and achieved an energy efficiency of 17.5pJ/pulse at symbol rates up to 15.6MHz. The transmitter communicates in the 3-to-5GHz low-band as specified by the IEEE 802.15.4a standard proposal. Dual digital power amplifiers feeding a capacitive combination network resulted in the attenuation of low-frequency content typically associated with digitally generated UWB pulses. Combined with discrete four-level pulse shaping, the resulting power amplifiers achieved both indoor and outdoor FCC compliant operation without requiring the use of off-chip filters. The lack of large passive filters or baluns in addition to the all-digital architecture led to an extremely compact and cost effective design; the transmitter core and DCO consumed an on-chip area of $0.07mm^2$.

5.2 Future Work

In today's ultra-competitive consumer, medical, and industrial electronics sectors, time-to-market of working silicon chips can often be the primary determining factor in the success of entire companies. To this end, engineers and designers are always searching for techniques to shorten design times. For example, digital circuit design has seen tremendous growth over the past two decades in the development of better CAD tools. These tools can synthesize and layout high performance digital systems in orders of magnitude less time than equivalent hand design. Since the transmitter described in this thesis is comprised of entirely digital circuits, it is worthwhile investigating the use of digital CAD tools combined with hardware description languages (i.e. Verilog) to synthesize an entire UWB transmitter. This becomes increasingly more viable in deeply scaled digital CMOS where transistor switching speeds are increasing dramatically.

If the transmitter were to be commercialized, it would have to be 802.15.4a compliant in order to operate with other pulse-based UWB receivers. In this case, the

transmitter must support coherent communication. This would be possible if the DCO performance was enhanced by adding additional tuning bits and reducing its sensitivity to supply noise coupling. Furthermore, a PLL or PA-FLL would likely be necessary to meet frequency stability requirements. For added robustness to narrow-band interferers, it would be beneficial to increase the DCO range to cover the entire 3.1-to-10.6GHz UWB band.

The transmitter proposed in this thesis was designed to operate at distances up to 100m by supporting pulse bursting, high output voltage swings, and run-length limiting. However, applications such as medical monitoring would typically only use UWB as a last-meter communication link, thus significantly reducing the required range. Additionally, these type of systems often employ unidirectional links that push the communication complexity out of the transmitting sensor node where energy is extremely limited, and into the basestation receiver where energy is abundant. In this manner, future work could involve investigating what transmitter features can be eliminated and/or streamlined to further reduce the energy burden. Future work could also involve investigating what features can be *added* to the transmitter in order to improve overall communication reliability, thus decreasing the absolute number of bits which must be transmitted. As a simple example, convolutional encoders are low-complexity blocks which can easily be implemented on an energy-starved sensor node, whereas the high complexity decoder can be implemented on the basestation receiver. A system-level view is required to find optimal solutions to these types of problems, with the ultimate goal of minimizing the energy consumed per *useful* bit of transmitted information.

Finally, techniques to reduce the peak power consumption of the transmitter should be investigated if the transmitter is to be utilized in self-powered sensor nodes. Such systems typically employ integrated energy harvesters, which can often sustain large power draws for only very short periods of time.

Appendix A

List of Acronyms

AC alternating current

ADC Analog to Digital Converter

BAN Body Area Network

BER bit error rate

BPSK Binary Phase-Shift Keying

CAD Computer Aided Design

CAGR compound annual growth rate

CMOS Complimentary Metal Oxide Semiconductor

DB-BPSK delay-based BPSK

DAC Digital to Analog Converter

DC direct current

DCO digitally controlled oscillator

FCC Federal Communications Commission

FIR finite impulse response

FLL frequency-locked loop

FPGA Field Programmable Gate Array

GPS global positioning system

HTL half-transparent latch

IEEE Institute of Electrical and Electronics Engineers

IF intermediate frequency

IR-UWB Impulse Radio UWB

ISM Industrial, Scientific and Medical

ISO International Organization for Standardization

LO local oscillator

LNA Low Noise Amplifier

LFSR linear feedback shift register

MAC Medium Access Control

MB-OFDM Multi-Band OFDM

MOS Metal Oxide Semiconductor

OFDM Orthogonal Frequency Division Multiplexing

OOK On-Off Keying

QAM Quadrature Amplitude Modulation

PA power amplifier

PA-FLL phase-aligned frequency-locked loop

PAPR peak-to-average power ratio

PDCF pulse desensitization correction factor

PHY physical

PLL phase-locked loop

PPM Pulse Position Modulation

PRF pulse repetition frequency

PSD power spectral density

PVT process voltage and temperature

RBW resolution bandwidth

RLL run length limit

RMS Root Mean Square

RF radio-frequency

SIG Special Interest Group

SA spectrum analyzer

SAW Surface Acoustic Wave

SNR signal-to-noise ratio

SRF symbol repetition frequency

TSPC true single-phase clock

TH time-hopped

U-NII Unlicensed National Information Infrastructure

UWB ultra-wideband

WLAN Wireless Local Area Network

WPAN Wireless Personal Area Network

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