A High Performance Zero-Crossing Based Pipelined Analog-to-Digital Converter

by

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Abstract

In this thesis, I describe a zero-crossing based pipelined ADC. Unlike traditional pipelined ADCs, this work does not use any op-amps in the signal path. The use of zero-crossing based circuits made it possible to achieve a much better figure of merit. The ADC is design to operate at 200MS/s with a resolution of 12 bits. The simulated results suggest that the target performance is achievable with less than 10 mW of power. This design's figure of merit is at least an order of magnitude better than any existing designs that have comparable speed and accuracy performance. The design will be fabricated later to be tested in silicon.

Thesis Supervisor: Hae-Seung Lee
Title: Professor of Electrical Engineering

Acknowledgments

I would like to thank my parents for their support and guidance. I couldn't have come this far without them. They taught me a lot of math and physics when I was younger. That laid out the foundation for me to succeed later on in high school, college, and beyond.

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Chapter 1

Introduction

As CMOS processes continue to scale to smaller dimensions, the increased f_T of the devices and smaller parasitic capacitance allow for more power efficient, and faster digital circuits to be made. But at the same time, output impedance of transistors has gone down, as have the power supply voltages, and leakage currents have increased. These changes in the technology have made analog design more difficult. More specifically, the design of a high gain op-amp, a fundamental analog building block, has become more difficult in scaled processes.

The objective of this work is to demonstrate that zero-crossing based circuits (ZCBC) are a much more power efficient method to build switched-capacitor circuits.

1.1 Motivations

In traditional pipelined ADC designs, op-amps are used in the switched-capacitor circuit to transfer charge between capacitors. The accuracy and speed of the charge transfer operation is often limited by the accuracy and speed of the op-amp used.

As technology continues to scale, the supply voltage has reduced. This reduces the amount of available signal range. To maintain the same amount of SNR in analog circuits, the noise must be reduced correspondingly. This usually involves using bigger capacitors and burning more power. In addition, the reduced intrinsic gain of devices makes op-amp design in scaled CMOS processes especially challenging.

The accuracy of the charge transfer operation is limited by the open-loop gain of the op-amp. Thus, a high gain op-amp is needed for high resolution ADCs. It's possible to increase the op-amp gain by using cascoded devices, but this takes up more headroom and further reduces the signal range. Cascading multiple stages can increase the gain, but it introduces stability issues.

An alternative approach, the Comparator Based Switched-Capacitor (CBSC) circuits, has been demonstrated in [3]. A comparator and a current source are used to replace the op-amp in switched-capacitor circuits. By using this structure, the high-gain op-amp is no longer required in switched-capacitor circuits. Also, the comparator based circuits are more amenable to scaling. A more detailed description will be given in chapter 3.

The CBSC technique is not limited to ADCs. It can be applied to many different switched-capacitor circuits including filters, integrators in sigma-delta converters, and switched-capacitor DACs.

1.2 Prior Work

The first prototype of the Comparator Based Switched-Capacitor circuit was demonstrated in a 8 MHz , 10b pipelined ADC in a 0.18μm process [3]. The ADC consumed 2.5 mW and achieved 8.6 effective number of bits (ENOB).

In a later design, a more power efficient zero-crossing detector was used to replace the comparator in the original CBSC design. This resulted in a 200MS/s 8b pipelined ADC which consumed 4.5 mW [4]. Although the ADC was designed for a higher resolution, the substrate noise from the IO drivers limited the ENOB to 6.4b at 200 MS/s.

To improve the circuit's robustness against substrate, power supply, and common mode noises, a differential structure was used in the subsequent design [5].

Chapter 2

Traditional Pipelined ADC

There are numerous types of analog-to-digital converters. The performance space of various ADC architectures is shown in figure 2-1. Each architecture is best suited for a specific range of resolution and speed. The Pipelined ADC is well suited for medium to high resolution and high speed applications. There are a few clock cycles of latency due to the pipelined nature of this structure. However, in many applications, the latency is well tolerated.

2.1 Operation and Architecture

The Pipelined ADC is made up of many identical stages that are cascaded together. The operation is pipelined. When the input signal enters the first stage, it is quantized by the first stage's flash ADC. This is shown in figure 2-3. The decision bits are used by the DAC, whose output value is subtracted from the signal and amplified. The amplification factor is usually 2^n where n is the number of bits being resolved by the flash ADC. The resulting residue is passed onto the next stage where the same operation is performed during the next cycle.

The digital output bits from each sub-ADC are then re-aligned in a digital buffer before the resulting word is passed to the output.

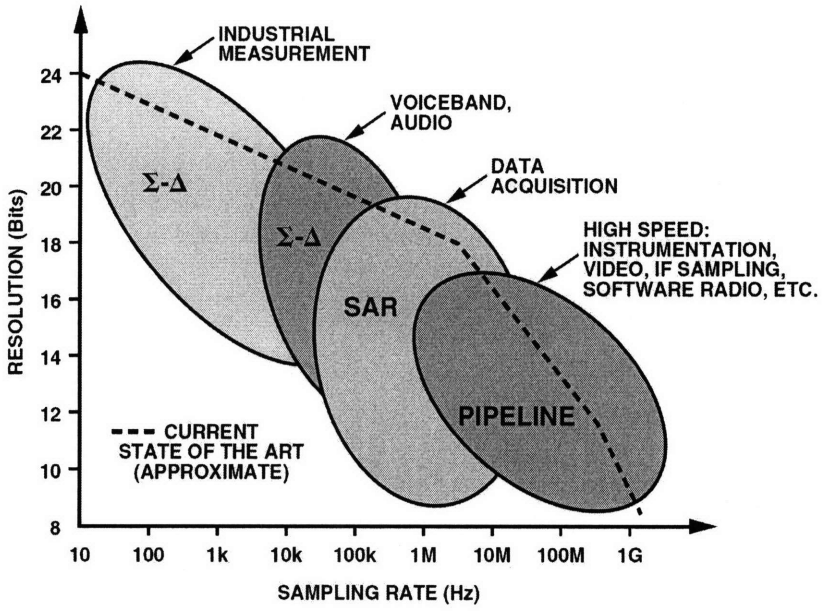

Figure 2-1: ADC architectures [1]

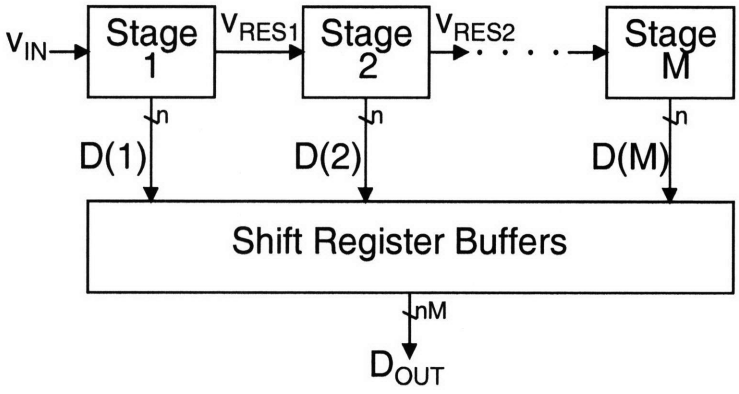

Figure 2-2: Pipelined ADC architecture [2]

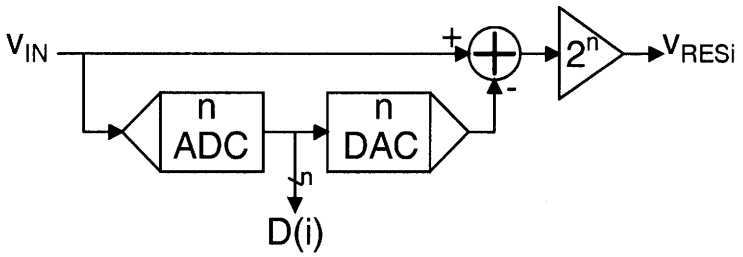

Figure 2-3: Pipelined ADC stage [2]

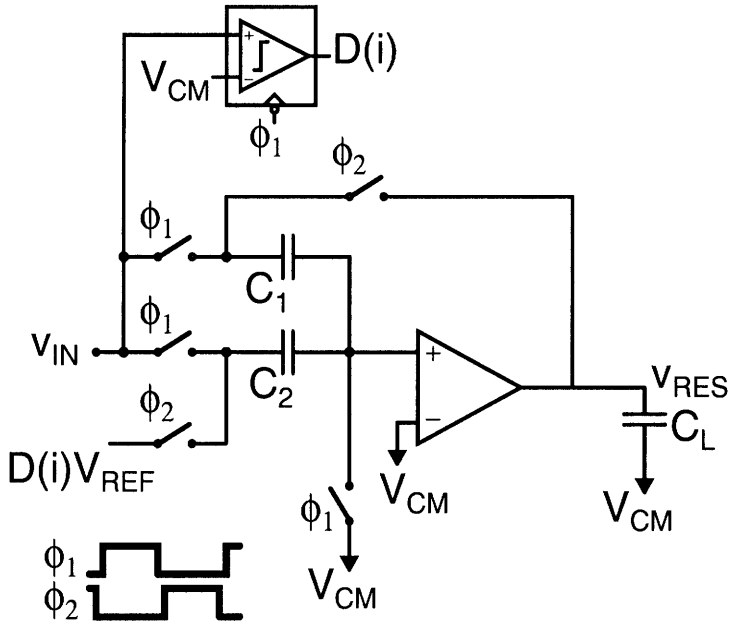

Figure 2-4: Traditional op-amp based 1 bit per stage pipelined ADC stage [2]

2.2 Op-Amp Based Switched Capacitor Circuit Structure

The DAC, the subtraction block, and the amplification circuit is usually formed with one block as shown in figure 2-4, which shows a 1 bit/stage example. This structure is referred to as the multiplying digital-to-analog converter (MDAC).

This circuit operates in two phases. In the first phase, the input is sampled onto C1 and C2. In addition, the 1 bit flash ADC's decision is latched at the end of the first phase, Φ_1. During the second phase, when Φ_2 is high, the op-amp forces the voltage on its non-inverting input to equal to the voltage on its inverting input. When this

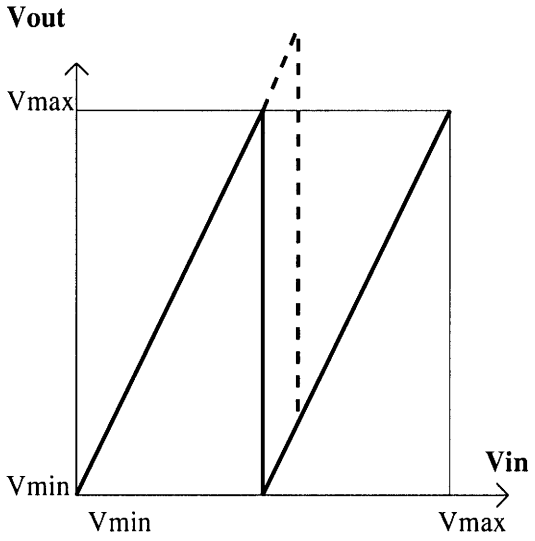

Figure 2-5: Residue plot of a single stage of a 1 bit per stage Pipelined ADC.

condition is reached, the output of the op-amp settles to the residue of the stage. For a 1 bit per stage implementation, the residue voltage settles to

$$v_{RES} = \frac{C_2 + C_1}{C_1} v_{IN} - D(i)\frac{C_2}{C_1} V_{REF} \tag{2.1}$$

where $D(i)$ is either +1 or -1 depending on the bit decision from the flash ADC. If there is an offset in the bit decision, as shown in the dotted line in figure 2-5, the output residue exceeds the maximum range of subsequent stages. The subsequent stages will then be saturated and information about the signal will be lost. This results in wide codes in the ADC.

A popular way to protect the ADC from bit decision offsets is to use redundancy. Extra bit decision comparators are used in the flash ADC to chop the residue into smaller pieces. This prevents the residue from going out of range when there is a limited amount offset in the bit decisions. The 1.5b per stage algorithm uses two bit decision comparators in the flash ADC [6, 7, 8]. The redundancy allows the circuit to correct for bit decision offsets up to 1/8 of the input range. A more detailed description of the general pipelined ADC structure can be found in Abo's thesis. [9].

Chapter 3

Comparator Based Switched-Capacitor Design

In CBSC pipelined ADCs, the op-amp can be replaced with a comparator and a current source. Although the transient behavior is different, the final voltage sampled is the same. Analysis shows that using the comparator-based technique is more power efficient compared to the traditional op-amp based design [3].

3.1 The Original CBSC design

A schematic diagram of the CBSC MDAC is shown in figure 3-1. The CBSC circuit is operated in a similar fashion to the op-amp based designs. During the first phase, the input signal is sampled on C_{1a} and C_{1b}. There is a preset phase at the beginning of phase 2. This ensures that the input to the comparator starts out below its tripping threshold. When the preset phase ends, the course phase begins. The current source I1 charges the output node. This fast ramp is design to charge the output node to approximately the right level. Then the coarse current source is turned off and the fine current source I2 is turned on. This is a smaller current source that charges the output node to its final value. When the threshold of the comparator has been reached, the comparator turns off the sampling switch and the current sources. This completes the charge transfer.

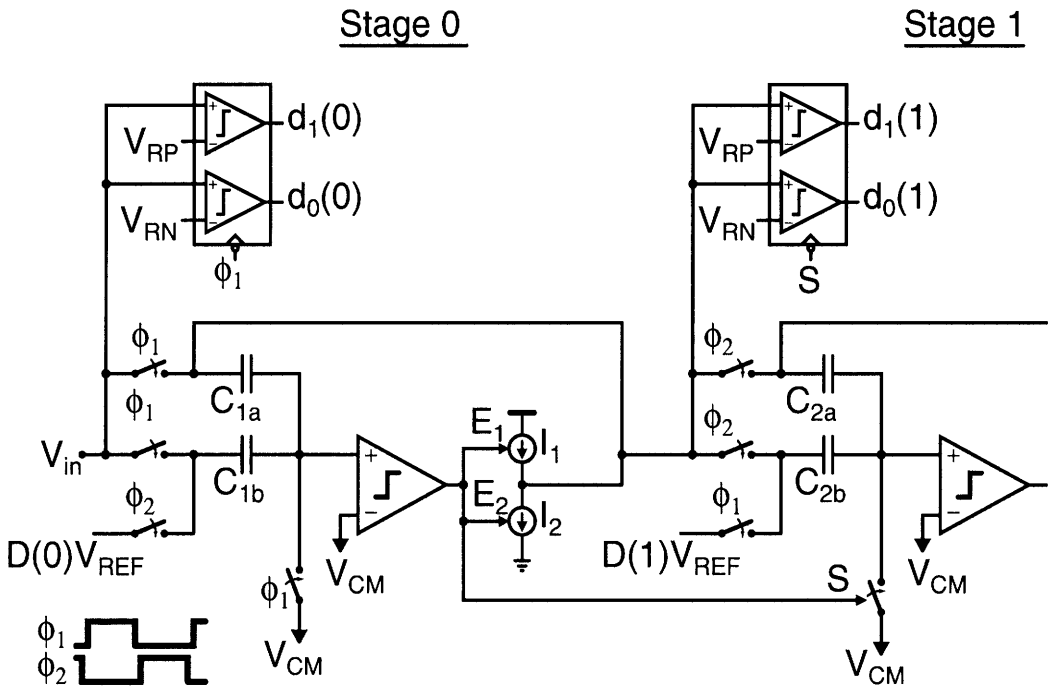

Figure 3-1: First two stages of the CBSC Pipelined ADC.

The same operation is repeated in the following stage to pass its residue onwards. There are also bit decision comparators attached to the output node. These comparators quantize the input signal and determine the DAC voltage that is applied to the top plate of C_{2b} during the following phase.

3.1.1 Accuracy Limitations

Since the comparator has finite delay, it will not be able to sample the output at the exact moment when its input crosses the threshold. This results in an overshoot. The amount of overshoot is constant if the current source is perfectly linear. But due to finite output impedance and parasitic junction capacitance, the current source's current level is not constant. Its variation causes the amount of overshoot to vary. This ultimately increases the amount of DNL and INL of the ADC.

Unlike op-amp based circuits, switches in the CBSC structure that connect various node still conduct current when the sample is taken. The amount of voltage dropped across the switches depends on their resistance. If the resistance is a non-linear

function of its input voltage, the voltage drop will also be non-linear. This can further degrade the linearity of the ADC. However, there is some cancellation between this non-linearity and the non-linearity caused by the current source. [2].

3.1.2 Noise Performance

In CBSC circuits, the current source, the switches, and the comparator all contribute noise to the system. It has been shown that the dominant noise source is the comparator [10]. One advantage of CBSC designs over traditional op-amp based designs is that the noise spectral density of the comparator can be made to be much lower than the noise spectral density of an op-amp. [10]. This is because it is possible to make a comparator with less active devices. In addition, the output swing on the pre-amp of the comparator does not need to be very large. In addition, the comparator is not connected in feedback. This removes the stability issue faced in op-amp based designs. These facts ease the design constraints of comparator considerably and allow for a more power efficient design.

3.2 Zero-Crossing Based Circuits

It was soon realized that a general purpose comparator is not needed in the CBSC design. In CBSC, the function of the comparator is to make a zero-crossing detection. Thus it's possible to use a zero-crossing detector instead of a general purpose comparator in the design. The difference is that a general purpose comparator must be able to compare two arbitrary voltages. However, in CBSC circuits, the input to the comparator is always a voltage ramp that approaches from one direction. Thus, the comparator can be replaced with a more power efficient zero-crossing detector.

It is possible to build the zero-crossing detector with a single transistor [4]. In ??, a single transistor is used as the zero-crossing detector. It only consumed power during the zero-crossing detection. This allowed the ADC to operate without any static power dissipation. A 200MS/s 8b ADC was produced. The ADC was designed for a higher resolution, but substrate noise coupled in from I/O drivers limited its

performance. The single ended zero-crossing detector was very sensitive to substrate noise and thus the SNR of the converter was limited to 6.4b at 200 MHz.

In this work, a differential structure is used to improve the circuit's robustness against power supply and substrate noise.

Chapter 4

High Performance Differential Zero-Crossing Based ADC

In this work, a high performance pipelined ADC is designed using the zero-crossing detection technique [4]. To improve its robustness against power supply and substrate noise, a differential topology is used. The converter's power efficiency is also improved by using a differential structure because it increases the input signal range by 2x. This allows the signal power to be increased by the factor of 4, while the power consumption only needs to increase by approximately a factor 2. To improve the current source's linearity, a dynamic biasing scheme is employed to compensate for its finite output impedance.

4.1 Sampling Network

The front end of the ADC consists of boot-strapped switches and capacitors as shown in Fig. 4-1. The boot-strapped switches help to lower the on resistance of the switches [11]. In addition, they also help to maintain a more linear resistance over the signal range. The capacitors are sized based on $\frac{KT}{C}$ sampling noise requirements. In this design, 1 pF capacitors are used to sample the input on both sides. The resulting differential RMS noise due to sampling is 91 μV. Cross coupled dummy switches are added to reduce the feed-through from the switches at high frequencies [12].

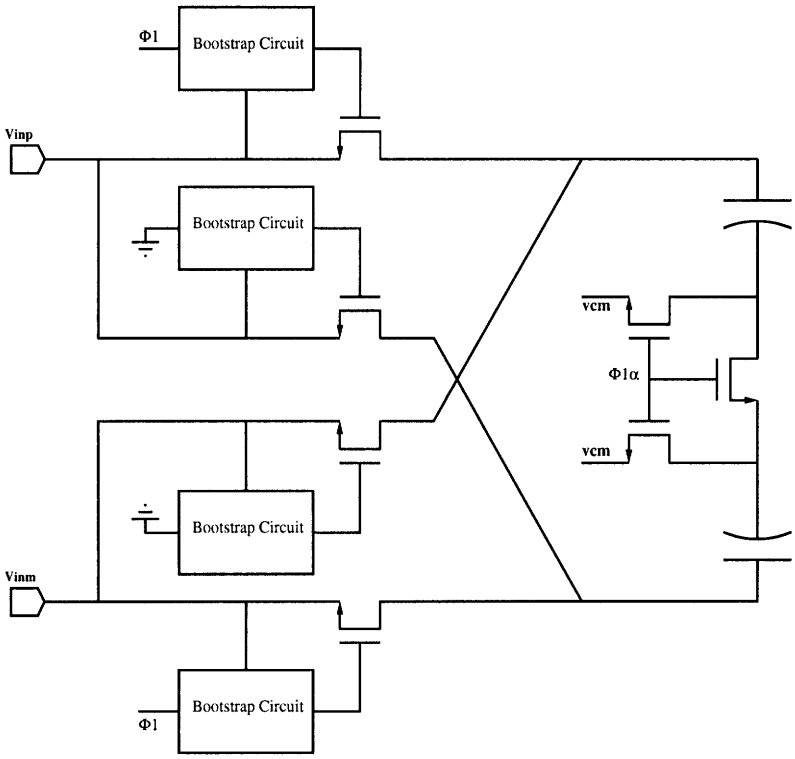

Figure 4-1: Differential sampling network

In this design, bottom plate sampling is used to reduce the effect of signal dependent charge injection. Even with bottom plate sampling, the bottom plate switch's charge injection is still not constant. Impedance mismatch at the top plate of the capacitors causes the the charge on the bottom plate to distribute unevenly. Fortunately, this error is small enough for our desired resolution.

During the sampling phase, a shorting switch connects the bottom plates of the two sampling capacitors. The middle part of the channel of the shorting switch can be considered to be virtual ground. Thus, the shorting switch can be represented using two transistors with length L/2, where L is the length of the shorting switch. As a result of using the shorting switch, the effective conductance to the virtual ground node is increased by a factor of 2 compared to using a single switch of the same width. In addition, area is reduced by a factor of 2. In terms of conductance/area ratio, the shorting switch is 4 times as efficient as using a switch to connect directly to the common mode voltage. Since charge injection is proportional to the area of the device, charge injection from the bottom plate switch is reduced by using a shorting switch.

There are also two switches connecting the bottom plate to the common mode voltage. These two switches are used to prevent the common mode level from drifting too far from the desired voltage.

4.2 Flash ADCs

In a pipelined ADC designs, flash ADCs are used in each stage to make bit decisions. The bit decisions are also passed onto the next stage to be used during the charge transfer phase of the following stage. In this pipelined ADC, the structure shown in Fig. 4-2 is used as the flash ADC.

In this design, the input signal is sampled onto capacitors of the flash ADC during the first phase. Once the sampling phase finishes, two reference voltages, which are generated from a resistor string, are applied to the top plates of the capacitors. After approximately 100 ps, the latch is enabled and a digital decision is made. The

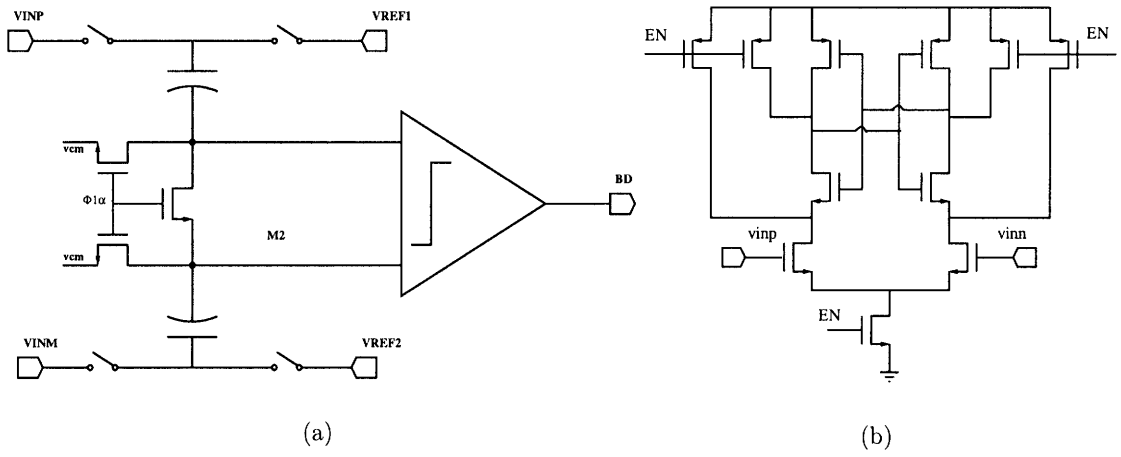

Figure 4-2: Flash ADC building blocks
(a) Comparator structure used to generate bit decisions. (b) Circuit implementation for the latch used in Fig. 4-2(a).

sampling switches and the capacitors in the flash ADC are designed to match the input path to minimize the difference between the flash ADC's input and the actual value sampled. Any mismatch between the flash ADC and the main path will cut into the amount of over range protection gained through using redundant bit decision comparators.

The latch used in the flash ADC is shown in Fig. 4-2(b). It consists of a differential pair with two cross coupled inverters. PMOS switches are used to reset the latch. When the EN signal is low, the latch is turned off and the internal nodes are preset to VDD. When EN turns on, depending on which input transistor has a higher gate voltage, the cross coupled inverters will latch in one direction.

The speed of the comparator is directly proportional to its $\frac{gm}{C}$ ratio [13]. Thus, from a speed perspective, it is desirable to use the minimum channel length in order to minimize capacitance and maximize gm.

However, as the area of the transistor becomes smaller, mismatch increases. Mismatch of the transistors causes offset in the comparator. Although the over-range protection in this design allows for up to 50 mV of offset, the performance of the system will be less than optimal if the offset is large. Large offsets can cause the

output voltage to get closer to the supply rails, causing the output impedance of the current sources to drop.

To improve matching between the devices, the channel length is made 25% larger than the minimum channel length. In addition, the width is also made larger. The layout of the device is made to be as symmetrical as possible. The simulated RMS offset voltage is less than 1 mV from Monte Carlo simulations.

As EN rises, it pulls the middle node towards ground. The rapid voltage change on this middle node couples to both input nodes. If the impedances of the reference switches are mismatched, the input voltages will move by different amounts and cause an offset in the latch. If the impedances of the switches connecting the reference voltages to the top plate of the capacitors are close enough, the kick-back error from the latch will affect the input voltages equally. Since the two reference voltages are different, it is difficult to guarantee that the impedance of switches is well matched under process and temperature variations. To avoid this issue, the switches should be sized to have low enough impedance such that the reference voltages on the top plates of the capacitors are held close to their ideal value when the latch is enabled. This will ensure that the coupling to the two input terminals is equal.

In order to minimize the offset, the layout of the latch comparator is made to be as symmetric as possible. A triple well is used to isolate the noise generated by this block from the substrate. There are two strips of dummy poly-silicon blocks attached on the edge of the cell. These dummy poly lines increases the nearby poly density, which helps to reduce mismatch in gate lengths due to etching variation [14].

4.3 Multi-bit Differential MDAC

Component matching requirements and other design requirements of the later stages are significantly reduced by using a multi-bit MDAC in the first stage. The This reduces the DNL caused by capacitor mismatch [15]. In this design, the first stage resolves 3.3 bits by using nine bit-decision comparators and the residue is amplified by a factor of 4. This residue scheme is demonstrated in previous work [5]. The following

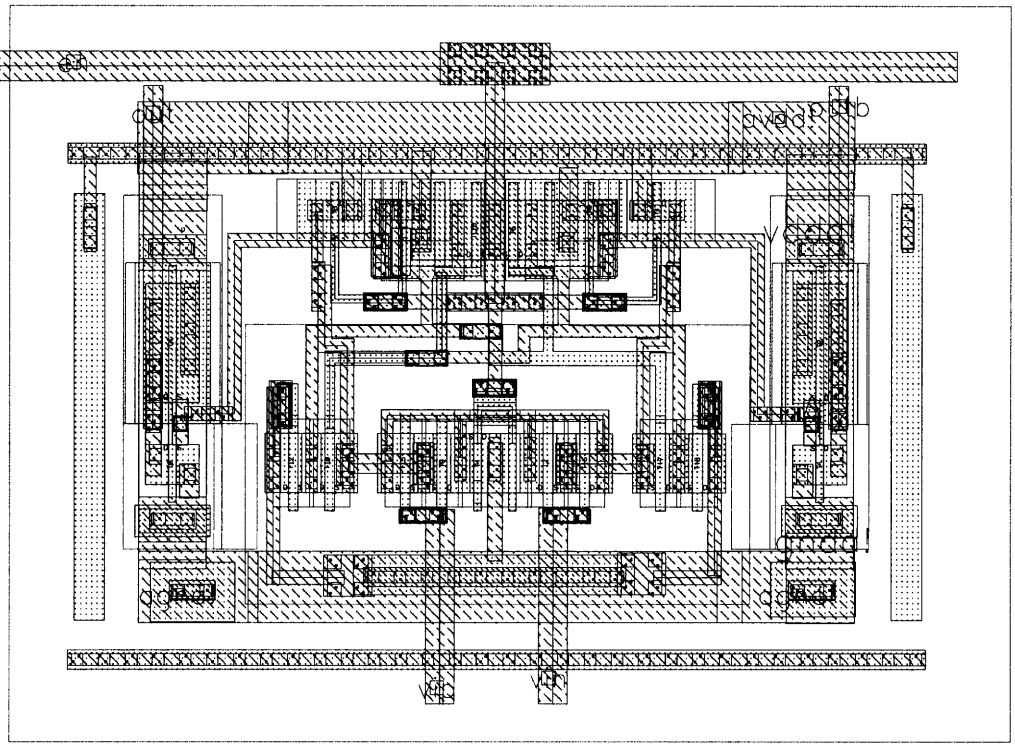

Figure 4-3: Layout of the latch comparator

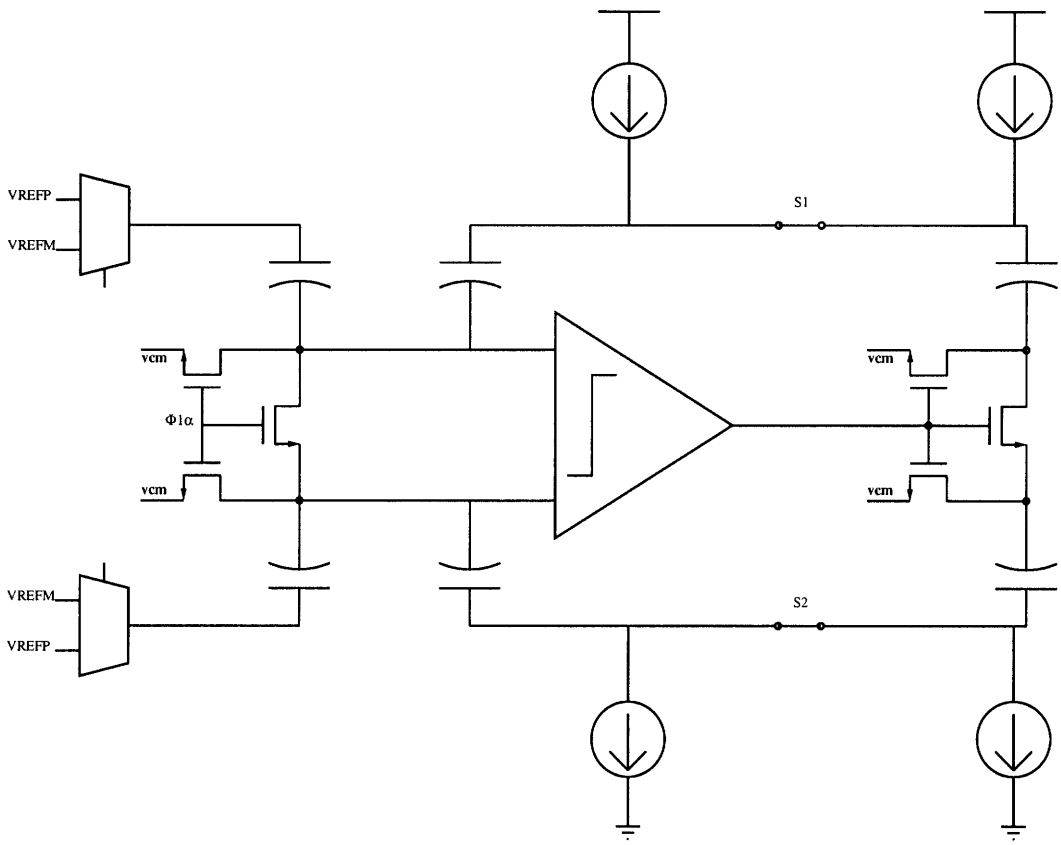

Figure 4-4: ZCBC differential MDAC stage

stages use five bit-decision comparators. The two bit decision comparators on the edge are redundant comparators used for over-range protection. The inter-stage gain of the following stages is also 4. The use of redundant bit decision comparators allows the input signal to be divided into smaller pieces. This limits the output range to values where the current source behaves linearly. In addition, the extra bit decision comparators in the first stage help to expand the input signal range.

4.3.1 Dynamically Biased Current Source

The linearity of the current sources used in ZCBC directly affects the linearity of the system. To the first order, the non-linearity comes from the finite output impedance

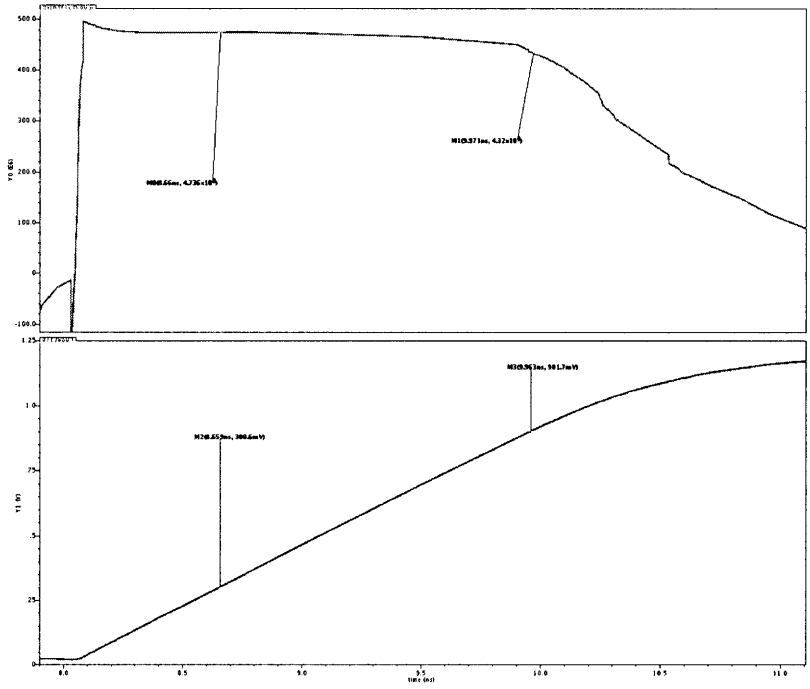

Figure 4-5: Ramp linearity of a cascoded PMOS current source

of the transistors.

$$r_o = \frac{1}{\lambda I_{ds}} \tag{4.1}$$

The output impedance r_o is inversely proportional to the product of the drain to source current and λ, which is the inverse of the Early Voltage. For high speed designs, the linearity problem is worsened due to the higher ramp rate required to reach the entire output range. If the delay of the zero-crossing detector remains appoximately fixed, then the over-shoot will be larger. The non-linearty of the over-shoot will increase proportionally. This degrades the linearity of the system.

In this process, the PMOS device has much lower output impedance compared to its NMOS counter part. Thus, the linearity of the system is limited by the PMOS current source. In figure 4-5 , the output $\frac{dV}{dt}$ is plotted as a function of time in the top graph. The bottom graph shows the output voltage as a function of time.

In addition, non-linear junction capacitance worsens the situation. In a pmos current source, the drain is made up of P+ silicon and the bulk is N-type silicon. As

the output voltage rises, this PN junction becomes less reverse biased. The depletion region shrinks, causing the junction capacitance to rise. The increase in capacitance on this node further reduces the ramp rate.

For the simulation results shown in figure 4-5, the PMOS current source is implemented using a cascoded current source. The ramp rate varies by approximately 8.5% in the allowable output range. From simulation results, approximately 5% of the variation is due to finite output impedance of the current source and 3.5% of the variation is due to the non-linear increase in parasitic junction capacitance.

The design of the current sources for ZCBC becomes increasingly more challenging as the speed of operation is increased. This is because for higher speeds, the ramp rate needs to increase. This causes more overshoot, given that the delay stays fixed. The larger overshoot requires the design to have a more linear ramp. In addition, device size will need to be increased to accommodate for larger current levels. This increases the amount of non-linear junction capacitance attached to the output node. These effects ultimately degrade the DNL and INL of the ADC.

A new type of current source is explored in this work to achieve the desired ramp linearity at an operating frequency of 200 MHz. The devices M2 and M3 shown in figure 4-6 form the core part of the current source. M3 acts as a cascode device, which helps to improve the output impedance by a factor of gm_3ro_3, where gm_3 and ro_3 are the transconductance and output impedance of M3.

The observation is that the ramp rate always slows as the output voltage rises. Instead of biasing the gate of M2 with a static voltage from a current mirror, a dynamic bias voltage is generated on the gate of M2 to compensate for the decreasing ramp rate at the output node. As the output voltage rises, the bias voltage on the gate of M2 is reduced. This increases the amount of current sourced by M2 and compensates for the reduction in the ramp rate.

The dynamically biased current source (DBCS) operates in two phases. During the first phase, ϕ_2 is low. The bias voltage on the gate of M2 settles exponentially back to its initial value, which is set by the Iref current and the size of the diode connected pmos transistor. The initial voltage is set at $VDD - (V_t + V_{dsat})$. During

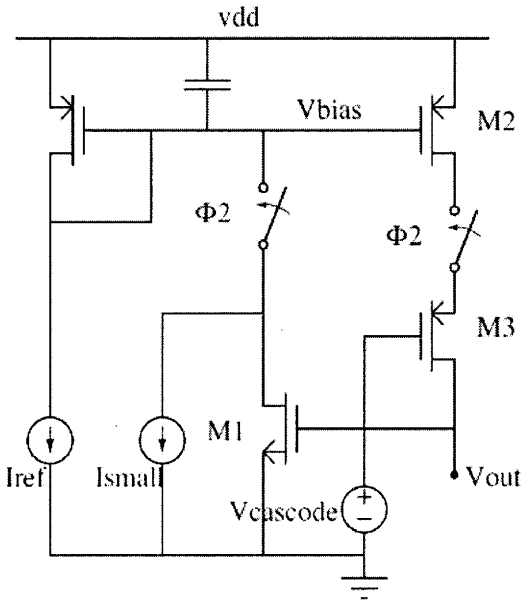

Figure 4-6: Dynamically Biased Current Source (DBCS)

this phase, the current source is disabled by turning the middle switch off. The recovery time constant is set by the ratio between the capacitance on the Vbias node to the transconductance of the diode-connected pmos device.

During the following phase, ϕ_2 turns high, activating the current source. The Vbias voltage will gradually decrease with time due to the additional current drawn by Ismall. The decreasing Vbias voltage will help to compensate for the reduction in ramp rate. The value of Ismall needed for optimal correction is dependent on process and temperature variation. Thus, to use this scheme effectively, a calibration step needs to be run periodically to ensure that value of Ismall is optimal. In this design, a 4 bit current DAC is used to calibrate Ismall digitally.

Dummy current sources are attached at the output of each current source to match the two differential paths [5]. These permanently disabled dummy current sources help to reject power supply and substrate noise by moving them to the common mode domain. Also, the dummy current source has a PN junction of an opposite polarity from the PN junction of the main current source. This helps to reduce the effect of non-linear junction capacitance on the ramp rate. For example, as the output voltage

rises, the pmos current source's junction capacitance increases while the dummy nmos current source's junction capacitance decreases. Although these two effects will not perfectly cancel, there is a fair amount of cancellation which helps to improve the ramp rate linearity.

4.3.2 Zero-Crossing Detector

The zero-crossing detector forms the core part of the MDAC. Its output voltage controls the sampling switch in the next stage. During the beginning of each charge transfer phase, a preset phase is used to ensure that the inputs to the zero-crossing detector start out below its tripping threshold. As soon as the preset phase ends, the output voltages start to ramp. The output ramp rate is given by $\frac{I}{C}$ where I is the current from the current sources and C is the total effective capacitance.

As the input to the zero-crossing detector crosses its threshold, it will trip and turn off the sampling switch in the next stage. The output of the zero-crossing detector is labeled as the sample_on signal in figure 4-7. As soon as the sample_on signal falls, charge is locked onto the next stage's input capacitors and the charge transfer operation is complete. A delayed version of the sample_on signal from the zero-crossing detector is then used to turn off all the current sources.

The zero-crossing detector's delay directly affects the linearity of the circuit. Let t_d be the delay of the zero-crossing detector. After the zero-crossing condition happens, the zero-crossing detector does not turn off the sampling switch until t_d later. During this time, the output continues to ramp at the same rate. The resulting overshoot can be expressed as the product of the delay with the ramp rate at the output.

$$V_{overshoot} = t_d \frac{dV}{dt} \tag{4.2}$$

If the output ramp rate is always constant, the resulting overshoot term will be constant. The resulting overshoot term will result in a constant input referred offset error, which can be corrected by an offset cancellation circuit. However, due to non-linearities in the ramp rate, this overshoot term will vary with input voltage, and

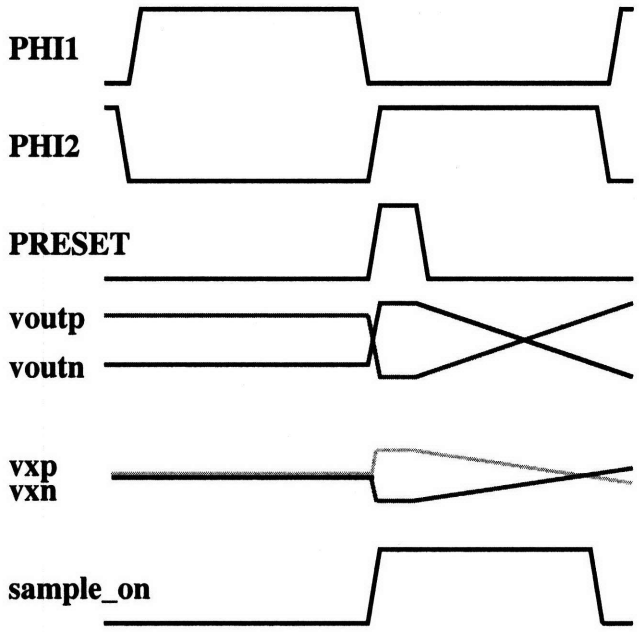

Figure 4-7: MDAC transient behavior

thus cause non-linearity. In this design, the non-linearity in the ramp rate is the main source of distortion in the ADC.

$$\Delta V_{overshoot} = t_d \Delta \frac{dV}{dt} \tag{4.3}$$

This $\Delta V_{overshoot}$ causes non-linearity and its contribution should be limited to less than 1 LSB. Although remaining stages also exhibit the same type of non-linear behavior, their non-linear contributions are divided by the interstage gain. In this design, the inter-stage is gain is 4. This increased inter-stage gain reduces the input-referred non-linearities of the later stages. This allows for a slightly higher amount of distortion in the first stage. For a given non-linearity specification, we can use the previous equations to calculate the delay and ramp linearity requirements. For example, if we want the non-linearity to be less than 1/2 an LSB, then $\Delta V_{overshoot}$ should be restricted to be smaller than that value.

The zero-crossing detector is implemented using a differential pre-amp followed by digital logic. The pre-amp is comprised of a differential pair as shown in figure 4-8.

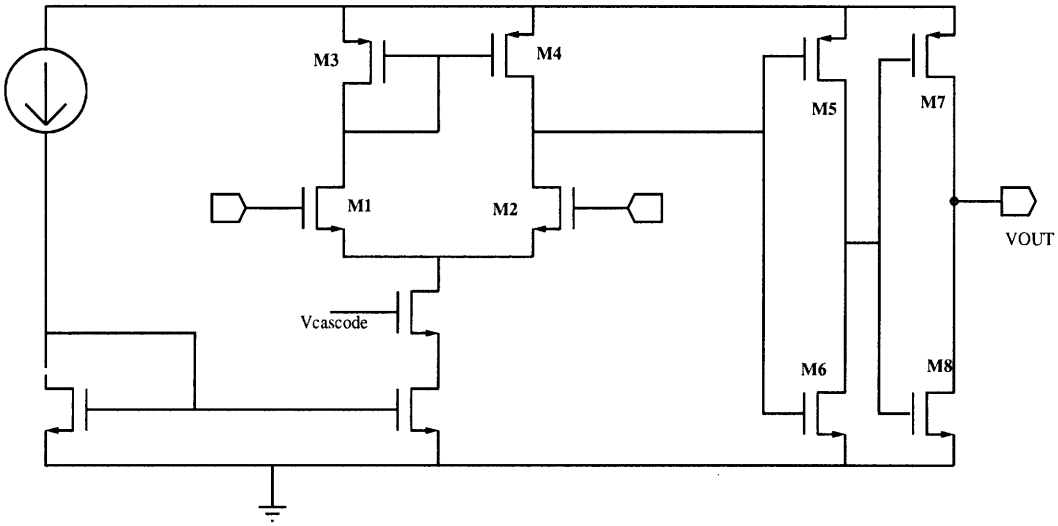

Figure 4-8: Zero-Crossing Detector

The input pair M1 and M2 is made wide to maximize their transconductance so that the input referred noise of the circuit is minimized. The devices M3 and M4 have smaller W/L ratios, which limits their transconductance values. This helps to reduce the input referred noise that they contribute. The pre-amp's tail current source is cascoded to improve its common mode rejection [16].

There are two inverters following the preamp that are used to amplify the pre-amp's output voltage to a full rail-to-rail signal. Since the input to the zero-crossing detector always moves in the same direction, the inverters are heavily skewed to minimize the delay in one direction. In this design, the W/L ratio of M5 is made to be 20x larger than that of M6 and the W/L ratio of M8 is made to be 28x larger than that of M7. There are additional switches (not shown) used in the preset phase to preset the zero-crossing detector's output to high, which turns on the sampling switch in the following stage.

The layout of the zero-crossing detector is made as symmetric as possible to minimize offset and improve common mode rejection. The input diff pair is laid out using a Common Centroid scheme. To isolate it from substrate noise, the zero-crossing detector sits in its own well. The nmos devices sit inside a pwell which is inside the nwell. Also, a P+ guard ring surrounds the zero-crossing detector's nwell to shield it

from unwanted disturbances in the substrate.

4.3.3 Switches

For switches, their on-resistance can be expressed by the following formula.

$$R_{on} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_t)} \tag{4.4}$$

The μ_n, V_t, and C_{ox} are process dependent parameters. The channel length is typically chosen to be the minimum size to minimize the on-resistance. The design parameters are W, the width and V_{gs} . Increasing the width increases the amount of parasitic junction capacitance which increases the amount of coupling from the clock signal. In addition, larger W will cause more charge injection when the switch is turned off. Another way to lower a switch's on-resistance is by increasing its gate to source voltage through boot-strapping [11]. This technique has become very common in scaled CMOS processes for low resistance switches.

For the sampling network, boot-strapping is used to lower the on-resistance and to improve the linearity of the switch. This is done in a way such that the gate oxide voltages do not exceed VDD. This ensures that there is no reliability problem.

The common mode voltage in this design is set at mid rail. At this voltage, the nmos conductance is much better than the pmos conductance. Thus, nmos switches are used for the switches that connect the bottom plates of capacitors to the common mode voltage.

The series switches that connect one stage to the following stage also use boot-strapping to improve their linearity. The current source splitting technique [4] is used to reduce the non-linear effects from these switches. A plot of various switch on-resistance characteristics is shown in figure 4-9 .

As shown in 4-9, the NMOS boot-strapped switch's resistance is the most linear. However, there is still a gradual increase in the resistance value as the output voltage rises due to the back gate effect. As the output voltage rises, the source-to-bulk potential increases, causing the threshold of the device to rise. This causes an increase

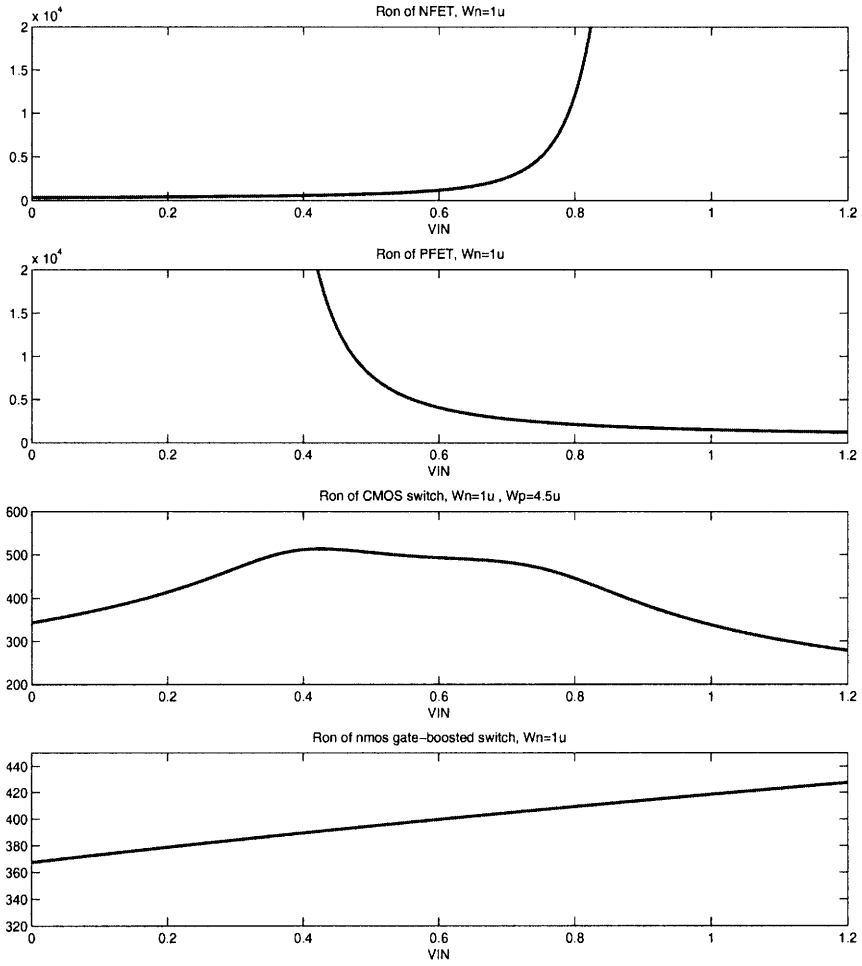

Figure 4-9: On-resistance plots of various switches

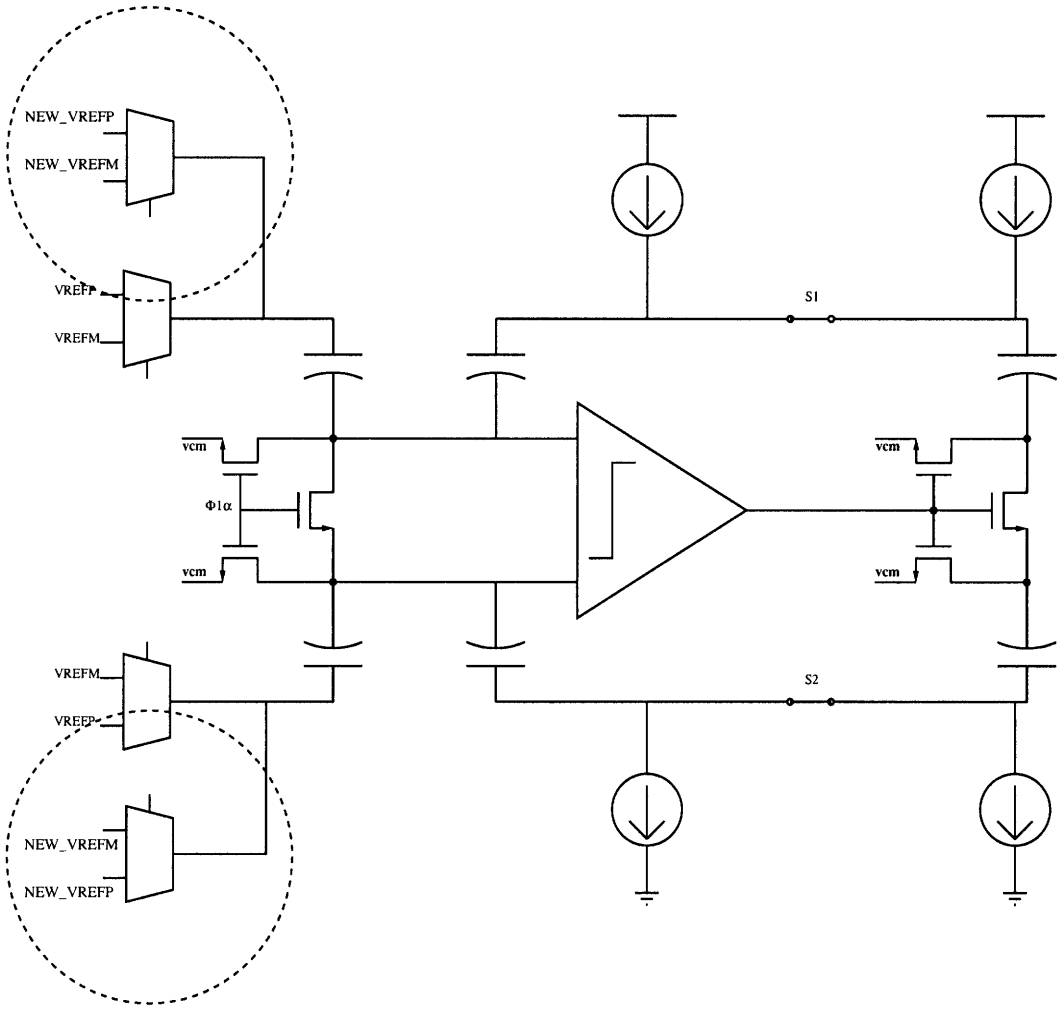

Figure 4-10: MDAC with reference pre-charge circuit

the differential nature of the design. However, a differential error on the reference remains.

In this design, a coarse pre-charge phase is inserted in the first stage, where accuracy matters most. This stage would have caused the most disturbance on the reference nodes because its capacitors are the biggest. The new reference pre-charge circuit is attached in parallel to the regular analog mux circuits used in the DAC as shown in figure 4-10. The pre-charge reference circuit is only used in the first stage because there is extra time that can be allocated for this operation in the first stage. The time is borrowed from the sampling time. In addition, two additional pins are

in on-resistance. In a triple-well process, it's possible to isolate the bulk of the boosted switch from the global substrate and tie its bulk to the source during the phase when the switch is turned on. The resulting on-resistance becomes much more linear. At the 12-bit resolution level, the body-effect does not introduce excessive non-linearity in boot-strapped switches.

4.3.4 Reference Ripple Reduction Technique

After the flash ADC makes its bit decisions, these digital values are passed into the DAC. Depending on the value of the bit decision, either vrefp or vrefm is driven onto the top plate of the capacitor during the charge transfer phase, as shown in 4-4.

For op-amp based designs, the output voltage is always sampled at the end of the phase, giving the vrefp and vrefm voltages the entire period to settle. However, for zero-crossing based ADCs, the charge transfer can finish before half of the cycle is completed. If the reference voltage is not settled, its deviation from the ideal value will add an error term at the output. In this aspect, ZCBC is at a disadvantage compared to op-amp based designs. Care must be taken to ensure that the reference voltages are sufficiently settled by the earliest possible end time of the charge transfer operation. If needed, it is possible to increase this time by increasing the time of the preset phase. However, the system will need a faster ramp for a given ADC operating speed.

In this design, Vrefp and Vrefm are not generated on-chip. They are connect through a bond wire to the external pins of the package. The reference voltages Vrefp and Vrefm suffer the most disturbance during the preset phase. This is because a large amount of current is drawn to preset the top plates of the sampling capacitors to either Vrefp or Vrefm, depending on the bit decision from the flash ADC. And since the inductor voltage $V = L\frac{dI}{dt}$, a large voltage drop shows up across the inductive bond wire during this time. Once the reference voltages are disturbed, they continue to ring but the amplitude of the ringing gradually dies down.

By inserting a large decoupling capacitor between the Vrefp and Vrefm node, the ringing is mostly limited to a common mode disturbance, which is rejected by

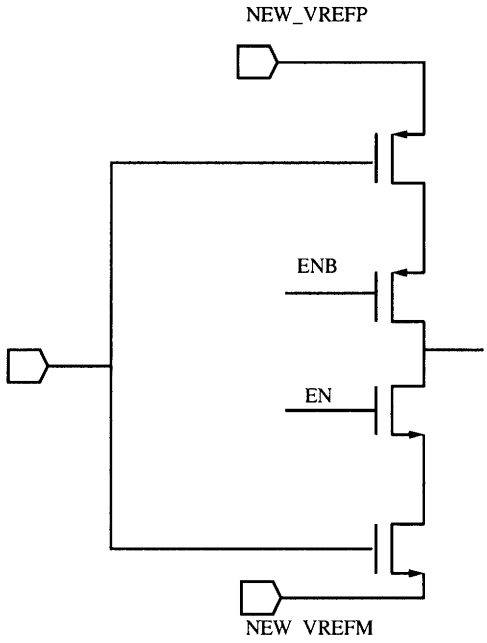

Figure 4-11: Reference Pre-charge Circuit implementation

used to connect two separate voltages to the additional reference pre-charge circuit. The pre-charge reference circuit drives the nodes that need to be driven by vrefp and vrefm to within tens of mili-volts before the actual vrefp and vrefm are connected. This greatly reduces the disturbance on the reference nodes and allows the system to meet its accuracy requirement. In this design, the voltages attached to the pre-charge circuit are at the same potential as vrefp and vrefm.

After the input voltage is sampled, there is some time given for the flash ADCs to generate the bit decisions. Once the bit decisions are ready, the reference pre-charge circuit is enabled. The top plates of the capacitors are pulled toward either VDD or GND. During the preset time of the following phase, the reference pre-charge circuit is disabled. The EN and ENB signal isolates the pre-charge voltages from the output node and the actual reference voltage is then applied to the top plates of the capacitors.

The pre-charge circuit significantly reduces the bounce on the vrefp and vrefm nodes. This helps to ensure that the ADC's performance is not limited by the settling of the reference voltages.

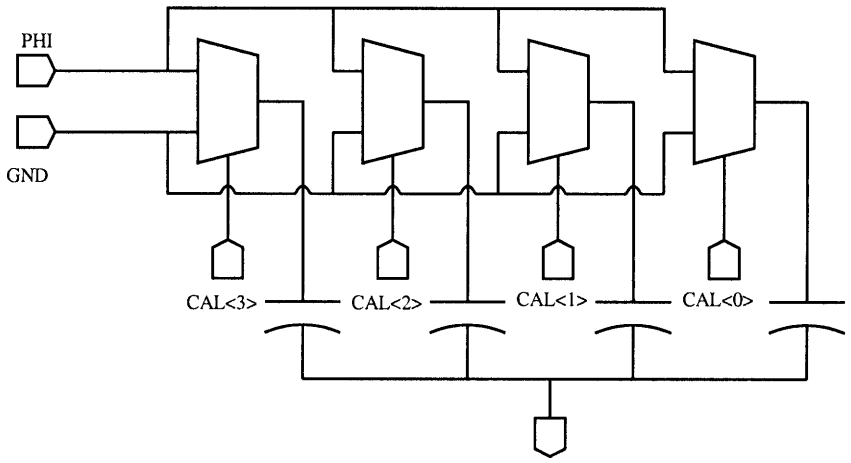

Figure 4-12: Offset Correction Circuit

4.4 Offset Cancellation

Due to the finite delay of the zero-crossing detector, the ADC inherently has offset. If left alone, this offset will reduce the effective input range. In this design, offset correction blocks have been added to the MDAC to help correct for offset as shown in figure 4-12.

The output node of this block is attached to the virtual ground Vx node of the MDAC. This is where the charge is locked after the input from the previous stage is sampled. Based the value of the digital calibration bits $CAL < 3 : 0 >$, some amount of charge is added or subtracted from the Vx node during the charge transfer phase. The offset of the ADC is adjusted based on the amount of charge injected. The capacitors are binary weighted. The calibration bits control whether or not a particular capacitor will add its charge to Vx node. The capacitors used in this block make up approximate 1% of the total capacitance attached to the node. Thus, their presence does not significantly impact the normal mode of operation.

Calibration is required to correct for the offset. If the input signal's statistics are known, it may be possible to do background calibration.

If the statistic of the input signal is unknown,foreground calibration needs to be applied. Since this offset is mainly due to the delay of the zero-crossing detector,

which varies with temperature, the ADC needs to be calibrated periodically.

4.5 Other optimizations

The analog power and ground are completely separated on-chip from the digital power and ground by using triple wells. The substrate is tied to its own ground pin, which is electrically isolated from the other power nets on-chip. This helps to limit the effect of substrate noise and power supply noise.

A SRAM block is included on chip to store the output data. The I/O drivers operating at 200 MHz could potentially inject substantial amounts of substrate noise. The use of the SRAM blocks allows the I/O drivers to be disabled while data is collected in the SRAM. The controller for the SRAM has three states: read, write, and idle. During the idle state, the SRAM circuit is turned off to save power.

The layout is made as symmetric as possible to improve the circuit's robustness against common mode noise.

Chapter 5

Simulation Results

This design will be fabricated during Fall 2008. The results presented in this section are obtained from simulators Eldo and Spectre.

5.1 Sampling Network

The sampling network operates at 200 MHz. A 2V, peak-to-peak near Nyquist sinusoid is used as the input signal. The input signal can be expressed as $Sin(2\pi ft)$ where f is approximately 90 MHz. The input frequency and the sampling frequency are chosen such that the signal is coherently sampled [17]. Given the limited number of samples, it is usually best to use coherent sampling to get a clean DFT plot[1] There are 2048 samples used to create the plot shown in figure 5-1. Our overall design target for the ADC is 11 ENOBs. Based on the simulated data, the sampling network's performance should have sufficient margin.

[1]This plot is commonly referred to as the FFT plot. However, it would be more accurate to call figure 5-1 a DFT plot. To get the plot, the Discrete Fourier Transform is performed. The Fast Fourier Transform (FFT) is class of algorithms that are used to perform the DFT operation. The same plot can be produced with any other implementation of the DFT operation without using the FFT algorithm.

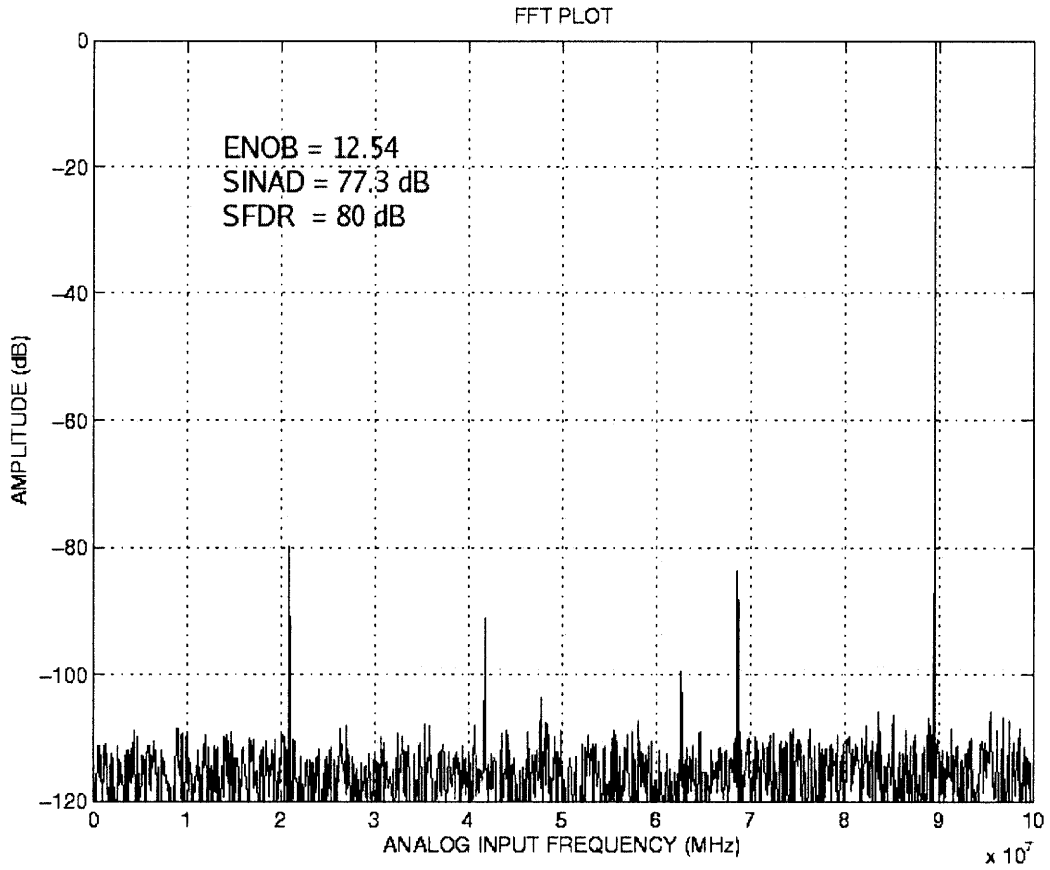

Figure 5-1: DFT of the sampled values

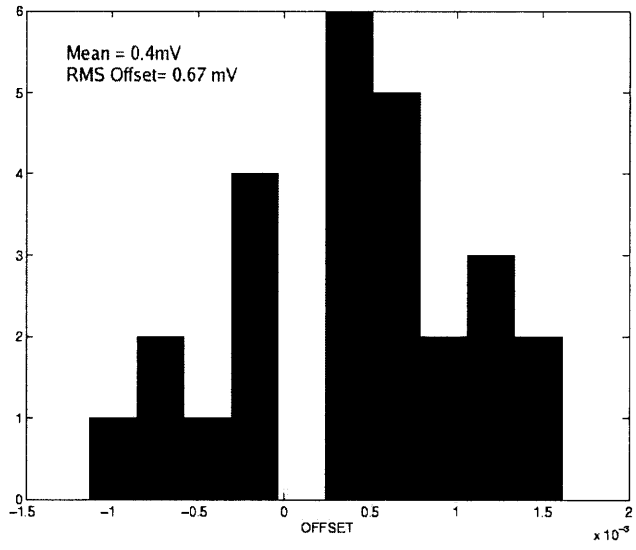

Figure 5-2: Bit decision comparator offset simulation

5.2 Flash ADC

To measure the offset of the bit decision comparators, a slow ramp near the threshold is applied to the input. The actual trip point of the comparator is measured. A Monte Carlo simulation is performed on an extracted net-list, which includes parasitic capacitances and resistances from layout.

25 data points were taken. The mean is at 0.4 mV. And the standard deviation is 0.67 mV. In this design, the over-range protection allows up to 50 mV of offset.

5.3 Dynamically Biased Current Source

There are four bits used to calibrate the current source. Without calibration, the ramp rate generated by the PMOS current source varies by approximately 9% in the range of interest. With calibration, this variation is reduced to less than 2%. Assuming a delay of 100 pS in the zero-crossing detector, the PMOS current source contributes 450 μV of input referred non-linearity. This error is partially cancel by the series resistance in the sampling switch [2]. In addition, part of this variation is canceled out by the change in delay in the zero-crossing detector [2]. The resulting

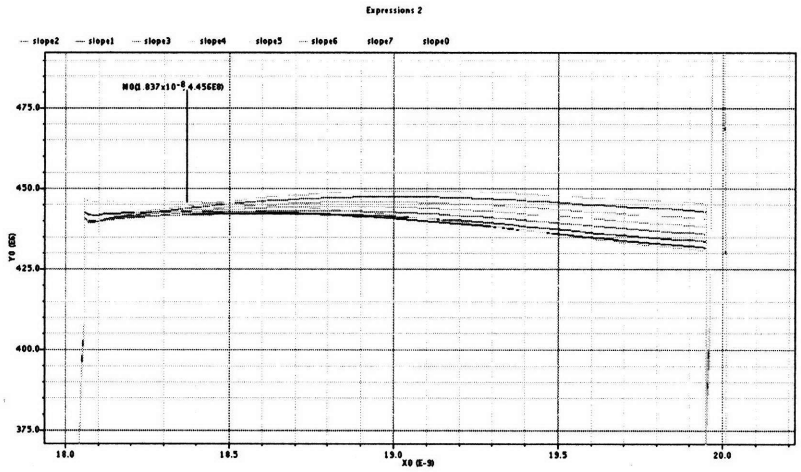

Figure 5-3: Dynamic Biasing: ramp rate plots

input-referred error observed in simulation is approximately $250\mu V$.

A plot of the different ramp rates is shown in figure 5-3.

5.4 Zero-Crossing Detector

In the original CBSC design, the main noise contributor is the comparator [10]. In ZCBC, the zero-crossing detector, which replaces the comparator in CBSC, is the main source of noise [4]. The pre-amplifier dominates the noise contributions in the zero-crossing detector design. When noise from the later stages is input-referred, it is attenuated by the gain of the pre-amp.

Since a high speed pre-amp is used in this design, it is approximately in steady-state during the zero-crossing detection. In this case, we estimate the noise by using the traditional method by integrating the pre-amp's noise spectral density. The noise spectral density of the pre-amp structure shown in figure 4-8 is $\frac{4kT\gamma}{gm}2(1+\beta)$ where β is the ratio between the gm in the PMOS load to the gm of the input pair. The β used in this design is approximately 1/4. The bandwidth is determined by the RC time constant at the output node. From simulation, the RMS input-referred noise is 110 μV. The LSB size is 488 μV.

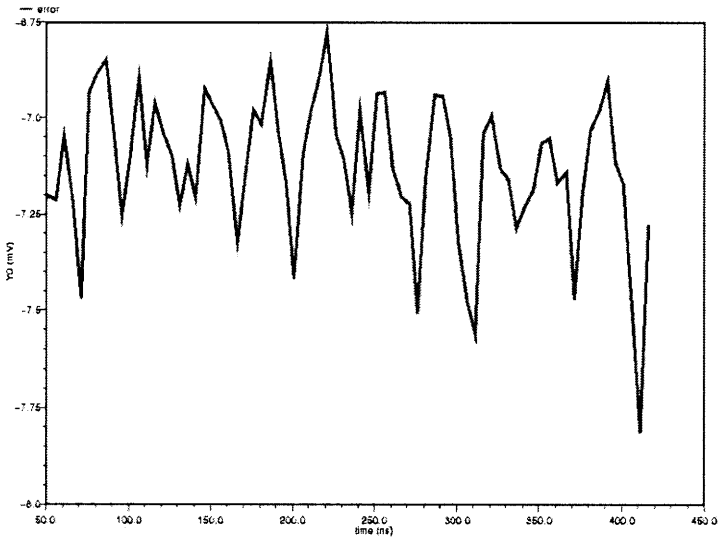

Figure 5-4: Residue error from stage 1

5.5 System Accuracy Estimate

To estimate the accuracy of our system, a linear ramp is applied at the input and the output residue of the first stage is sampled 72 times. The sampled residue is compared to the ideal residue, and their difference is plotted in figure 5-4. The ideal residue is computed in a verilogA block which calculates the residue based on the ideal input to output relation. In the error plot shown in figure 5-4, there is approximately 7mV of offset.

The non-linear contribution is approximately 1mV. Since the MDAC has a gain of 4, this is equivalent to 250μV of input-referred non-linearity. Since the input range is 2V, the LSB size is $\frac{2V}{2^{12}} = 488\mu V$. 250$\mu$V is approximately 1/2 of an LSB. The 2nd stage's linearity performance is comparable to the first stage. But its input-referred non-linearity contribution is 1/4 that of the first stage because there is an additional gain of 4 in the signal path.

Chapter 6

Conclusion

As described in this thesis, zero-crossing based circuits have a different set of design constraints compared to traditional op-amp based circuits. A great advantage of ZCBC is that the feedback and stability concerns associated with op-amp based designs are removed from the system. A high gain op-amp is no longer needed to achieve high resolution. Although the current source linearity is a bottle neck in ZCBC in terms of achieving high resolution, it is easier to generate linear ramps than to create high gain op-amps because there are fewer design constraints.

6.1 Thesis Contributions

This thesis describes a design for a 200 MHz, 12b differential pipelined ADC. The target for the power consumption is less than 5 mW. The target figure of merit, using the formula, $FOM = \frac{Power}{2^{ENOB} f_s}$, is 10 fJ per conversion step. This figure of merit is approximately 50 to 100 times better than any existing designs that operate in this frequency and resolution range. Our simulation results indicate that this is an achievable target. Results measured from the actual prototype circuit will be needed to verify the ADC's performance.

6.2 Future Work

Some possible directions for future work:

- Time interleave multiple zero-crossing based ADCs to achieve ultra high sampling rates.
- Various ramp rate linearization techniques
- On-chip reference voltage generators

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