Design, Fabrication, and Characterization of Germanium MOSFETs with High-k Gate Dielectric Stacks based on Nitride Interfacial Layers

by

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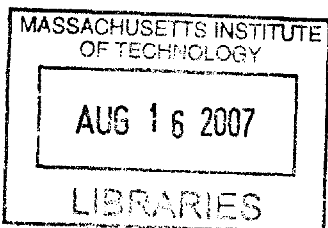

BARKER

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Abstract

To improve source injection velocity, and consequently MOSFET performance, high mobility semiconductors are being explored as possible replacements for silicon. Germanium offers enhanced electron mobility and superior hole mobility at high inversion charge density; however, the formation of a high quality germanium-dielectric interface remains a serious challenge. High-k dielectrics deposited directly on germanium exhibit poor physical and electrical properties so an interfacial layer is required. Proposed interlayers include GeON, Si, and metal nitrides such as AlN and Hf_3N_4.

This work focuses on the fabrication and characterization of germanium MOSFETs with GeON, Hf_3N_4, and AlN interlayers. WN/Al_2O_3/AlN gate stacks deposited by atomic layer deposition (ALD) were investigated in detail. The impact of AlN interlayer thickness and post-metal anneal conditions on the electrical properties of WN/Al_2O_3/AlN/Ge capacitors was determined. Optimal capacitance-voltage characteristics were achieved for an AlN thickness of 2.5 nm and 450-500 °C post-metal annealing. Ge n- and p-MOSFETs were fabricated with GeON, AlN, and Hf_3N_4 interlayers. The hole mobility of these devices generally matched or exceeded silicon universal hole mobility; however, Ge n-FETs showed poor electron mobility (50-100 cm^2/Vs).

Many theories have been proposed to explain the low carrier mobility of Ge n-FETs. These theories were investigated and it was found that an asymmetric distribution of interface states in the bandgap is the primary cause of low electron mobility for germanium-AlN interfaces. The interface state density near the conduction band edge approaches $6x10^{13}$ cm^{-2} eV^{-1}, approximately 5x higher than near the valence band edge. Low temperature characterization of n-FETs revealed degraded electron mobility due to carrier trapping and coulomb scattering from charged interface states. To reduce the interaction of carriers with interface states, n- and p-MOSFETs with reduced vertical effective field were fabricated using ion implantation. Devices exhibiting buried channel behavior showed electron and hole mobilities of 600 and 300 cm^2/Vs respectively, confirming that mobility degradation is caused by interface states. Evidence for phosphorus passivation of the germanium-AlN interface is also presented.

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Chapter 1

Introduction

1.1 Historical MOSFET Trends

Since its inception, the integrated circuit (IC) industry has been able to maintain an impressive set of trends governing device density and performance. Silicon-based MOSFET technology has provided an enabling platform for continuous improvement in density, switching speed, and cost per transistor. Since the 1970s, transistor density has doubled every 18 months. Dubbed Moore's Law, this trend reflects the tremendous impact of continuously reducing transistor dimensions and adjusting circuit parameters in a coordinated manner. In addition to gains in transistor density, the intrinsic switching delay for high-performance logic has historically decreased 17% per year [1]. The international semiconductor industry has developed a roadmap (*International Technology Roadmap for Semiconductors*) for extending these trends through 2020. Ultimately, technology R&D within the international semiconductor industry is geared towards maintaining these trends for as long as possible.

1.2 MOSFET Performance

Following the analysis of Antoniadis et al. [2], the intrinsic MOSFET switching delay, τ, is described by:

$$\tau = \frac{\Delta Q_G}{I_{eff}} \tag{1.1}$$

where ΔQ_G is the charge difference between logic states and I_{eff} is the effective switching current. The switching delay is inversely proportional to the *effective* virtual source velocity, v, which is defined as the effective carrier velocity at the virtual source. The virtual source is defined as the point at the top of the source-to-channel potential barrier where

carriers are injected into the channel. The effective virtual source velocity may be extracted using a simple model that accurately describes the drain saturation current, I_D, of state-of-the-art MOSFETs [2]:

$$\frac{I_D}{W} = C'_{oxinv}(V_G - V_t)v = q \cdot n_{inv} \cdot v \tag{1.2}$$

where W is the device width, C'_{oxinv} is the inversion capacitance per unit area, n_{inv} is the inversion layer carrier concentration per unit area, V_G is the applied gate voltage, and V_t is the threshold voltage determined by linear extrapolation of the I_D-V_G curve in saturation. Due to series resistance between the source contact and virtual source, equation 1.2 only provides the effective source velocity. The *actual* virtual source velocity, v_{xo}, is related to the effective velocity through the following expression [2]:

$$v_{xo} = \frac{v}{[1 - C'_{oxinv}R_sW(1 + 2\delta)v]} \tag{1.3}$$

where R_s is the parasitic access resistance between the source contact and virtual source and δ is the drain induced barrier lowering (DIBL) coefficient.

Antoniadis et al. extracted v_{xo} for bulk Si MOSFETs with gate lengths (L_G) ranging from 480 nm to 35 nm and the results are shown in Figure 1.1.

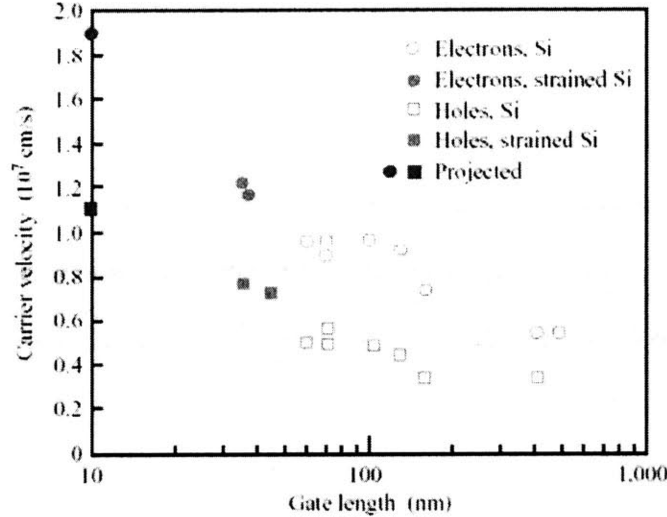


Figure 1.1: Actual virtual source velocity, v_{xo}, for commercial CMOS technologies with gate lengths ranging from 480 nm to 35 nm. Source velocities required to maintain historical performance trends at 10 nm gate length are also shown (from [2]).

Figure 1.1 shows that source velocities have been increasing for recent MOSFET technology generations. It is clear that continuous improvement in source velocity has played a large role in maintaining the historical reduction in intrinsic MOSFET delay.

Lundstrom has developed a theory that relates v_{xo} to backscattering near the virtual source through the following expression [3]:

$$v_{xo} = v_T\left(\frac{1 - r_c}{1 + r_c}\right) \tag{1.4}$$

where r_c is the backscattering coefficient and v_T is the thermal velocity. Lundstrom showed that backscattering is reduced by increasing low-field carrier mobility or increasing the lateral electric field at the channel-side of the virtual source. Simple backscattering theory can be used to explain the source velocity trend shown in Figure 1.1. In this figure, three separate regimes can be identified: $L_G > 130$ nm, 60 nm $< L_G <$ 130 nm, and $L_G <$

60 nm [2]. For L_G greater than 130 nm, low-field carrier mobility remained constant at the unstrained bulk Si value so v_{xo} improvement was due to the increased lateral source field produced by device scaling. From 130 nm to 60 nm, v_{xo} saturated due to increased coulomb scattering from the high doping concentrations required to maintain electrostatic integrity. From 60 nm onwards, process-induced strain has boosted low-field mobility and consequently v_{xo}. Recent work has shown that the correlation ratio between virtual source velocity and low-field mobility is 0.85 [4]. As shown in Figure 1.1, very high source injection velocities will be required to maintain historical performance trends for future technology generations. Given the direct relationship between low-field mobility and v_{xo}, high mobility semiconductors show promise for future CMOS devices.

1.3 The Advantages of Germanium

As shown in Table 1.1, germanium offers superior bulk hole mobility (approximately 4x enhancement relative to Si) while still offering 2.4x enhancement in electron mobility [5].

Semiconductor	Mobility at 300K (cm^2/Vs)	
	Electrons	Holes
Si	1500	450
Ge	3900	1900
GaAs	8500	400
InAs	33000	460

Table 1.1: Bulk carrier mobility for Si, Ge, GaAs, and InAs at 300K [5].

Additional advantages of germanium include high density of states (DOS) in the conduction band and relatively simple integration with silicon. Section 1.3.1 reviews the band structure of germanium and its relationship to DOS, inversion charge density, and mobility, Section 1.3.2 summarizes recent published simulation results comparing saturation drive current for germanium and III-V n-MOSFETs, and Section 1.3.3 briefly discusses

practical issues related to incorporating new semiconductor materials into CMOS manufacturing.

1.3.1 Band Structure

Carrier mobility and inversion charge density are intimately linked to semiconductor band structure. Semiconductors with diamond and zincblende crystal structures are characterized by the representative band structure and Brillouin zone shown in Figures 1.2 and 1.3, respectively [6]. Conduction band minima occur at the center of the Brillouin zone (Γ point), at the zone edge along the <111> direction (L point), and near the zone edge along the <100> direction (Δ point). The band structure depicted in Figure 1.2 corresponds to Ge (conduction band minimum at the L point). Diamond and zincblende semiconductors have three valence bands, two of which are degenerate at the Γ point.

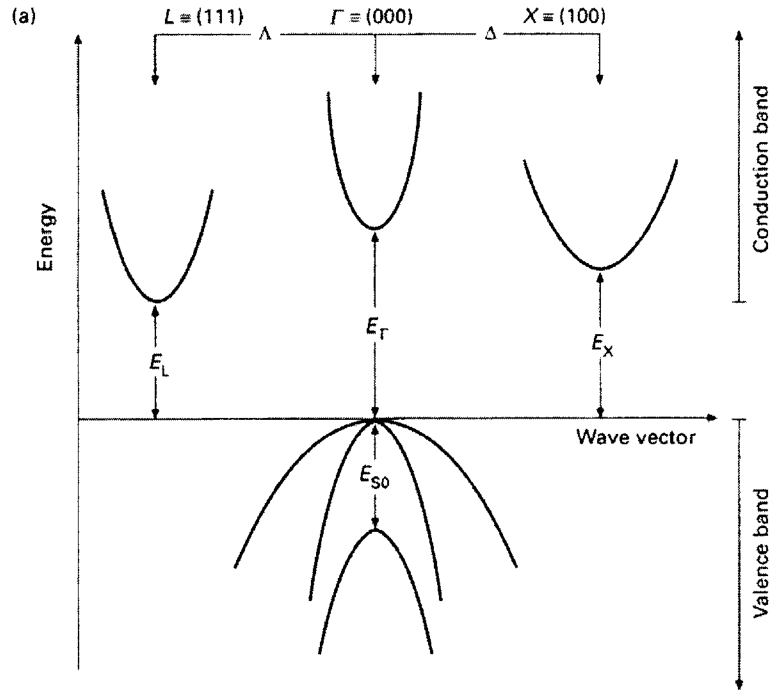


Figure 1.2: Representative band structure for diamond and zincblende semiconductors (from [6]). The band structure depicted in this figure corresponds to Ge (conduction band minimum at the L point).

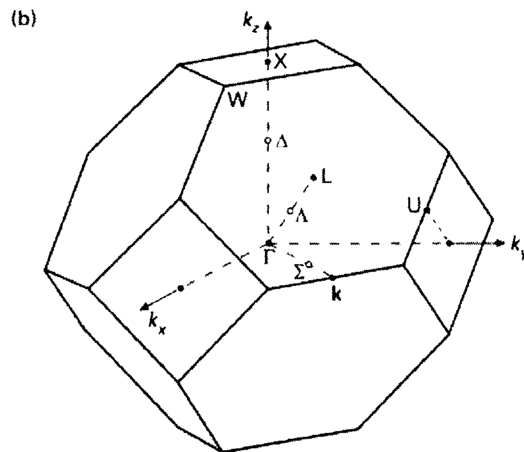


Figure 1.3: Brillouin zone for diamond (C, Si, Ge) and zincblende semiconductors (GaAs). Conduction band minima for Si, Ge, and GaAs occur at Δ, L, and Γ points, respectively (from [6]).

1.3.2 Conduction Band

As described above, diamond and zincblende semiconductors have conduction band minima at the Γ, L, and Δ points in the Brillouin zone. At low electric field and in the absence of a confining potential well, carriers populate the lowest energy valley. At high electric field and/or in the presence of a confining potential well, energy separation between valleys and quantization effective mass determine the carrier population distribution. The conduction band minimum for III-V semiconductors occurs at the Γ point which is characterized by isotropic effective mass (m^*). Germanium and silicon have conduction band minima at the L and Δ points, respectively. The effective mass in these valleys is anisotropic and may be characterized by an ellipsoidal constant energy surface with transverse (perpendicular to long axis) effective mass (m_t) and longitudinal (parallel to long axis) effective mass (m_l). The DOS, conductivity, and quantization effective masses are functions of m_t and m_l, or just m^* for the Γ valley. For maximum drive current, low conductivity effective mass (high mobility), high DOS in the low effective mass valley (high n_{inv}), and high quantization mass (high n_{inv}) are desirable. Inversion charge density is a critical parameter for determining MOSFET performance and is related to both DOS and inversion layer thickness through the equivalent circuit shown in Figure 1.4 [7].

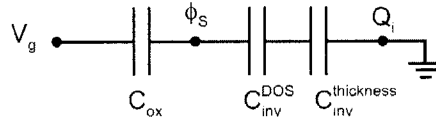


Figure 1.4: Equivalent circuit model for MOS inversion layer. Inversion layer capacitance (C_{inv}) is dominated by DOS at low inversion charge density and inversion layer thickness at high inversion charge density (adapted from [7]).

Inversion charge density is dominated by conduction band DOS at low charge density and inversion layer thickness at high charge density [7]. The crossover point occurs at a charge

density of approximately 1×10^{12} cm^{-2}. Inversion layer thickness is partly determined by energy level quantization in the 2D electron gas. Lower quantization mass translates into higher energy levels within the inversion layer potential well and consequently increased inversion layer thickness and decreased charge density.

The anisotropic effective mass of the Δ and L valleys in Si and Ge results in low conductivity effective mass and high DOS and quantization effective masses. Table 1.2 lists the transverse and longitudinal effective masses for the Δ and L valleys in Si and Ge [8]. Table 1.3 shows the effective mass in the x, y, and z directions (m_x, m_y, m_z) as a function of m_l and m_t for common substrate orientations [8]. As shown in Figure 1.5, the x-axis is oriented in the transport direction, the y-axis is oriented in the width direction, and the z-axis is oriented perpendicular to the wafer surface. Thus the conductivity, DOS, and quantization effective masses are given by m_x, $\sqrt{m_x m_y}$, and m_z, respectively [8]. The anisotropic effective mass in Si and Ge leads to high DOS and quantization masses which gives them a substantial advantage over III-V semiconductors.

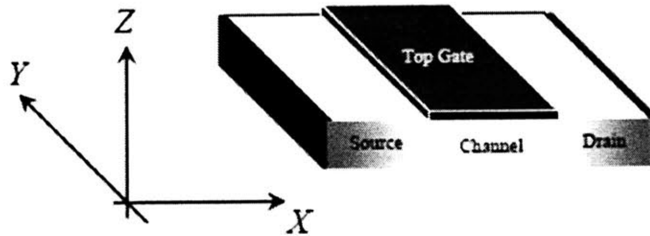


Figure 1.5: Definition of axes for m_x, m_y, and m_z effective masses. The x-axis is oriented in the transport direction, the y-axis is oriented in the width direction, and the z-axis is oriented perpendicular to the wafer surface (from [8]).

Material	Valley	m_l	m_t
Si	Δ	0.91	0.19
	L	1.70	0.12
Ge	Δ	0.95	0.20
	L	1.64	0.08

Table 1.2: Longitudinal and transverse effective masses for Δ and L valleys of Si and Ge (adapted from [8]).

(Wafer)/[transport] /[width]	Valley	m_x	m_y	m_z	Degeneracy
$(001)/[100]/[010]$	Δ	m_t	m_t	m_l	2
		m_l	m_t	m_t	2
		m_t	m_l		2
	Λ	$m_t\frac{(2m_l+m_t)}{(m_l+2m_t)}$	$\frac{(m_l+2m_t)}{3}$	$\frac{3m_lm_t}{(2m_l+m_t)}$	4
$(111)/[\bar{2}11]/[0\bar{1}1]$	Δ	$\frac{(2m_l+m_t)}{3}$	m_t	$\frac{3m_lm_t}{(2m_l+m_t)}$	2
		$\frac{2}{3}m_t\frac{(2m_l+m_t)}{(m_l+m_t)}$	$\frac{(m_l+m_t)}{2}$	$\frac{3m_lm_t}{(2m_l+m_t)}$	4
	Λ	m_t	m_t	m_l	1
		$\frac{(8m_l+m_t)}{9}$	m_t	$\frac{9m_lm_t}{(8m_l+m_t)}$	1
		$\frac{m_t}{3}\frac{(8m_l+m_t)}{(2m_l+m_t)}$	$\frac{(2m_l+m_t)}{3}$		2
$(110)/[001]/[0\bar{1}0]$	Δ	m_t	$\frac{(m_l+m_t)}{2}$	$\frac{2m_lm_t}{(m_l+m_t)}$	4
		m_l	m_t	m_t	2
	Λ	$\frac{(m_l+2m_t)}{3}$	m_t	$\frac{3m_lm_t}{(m_l+2m_t)}$	2
		$\frac{3m_lm_t}{(2m_l+m_t)}$	$\frac{(2m_l+m_t)}{3}$	m_t	2

Table 1.3: Conductivity (m_x), quantization (m_z), and width (m_y) effective masses of Δ and L valleys for (100), (111), and (110) substrate orientations (from [8]).

1.3.3 Valence Band

As shown in Figure 1.2, diamond and zincblende semiconductors have three valence bands. Two are degenerate at the Γ point but have different curvatures and effective masses and are thus termed the light (upper) and heavy (lower) hole bands. The third band is split-off and lies at higher energy. Strong interaction between the light and heavy hole bands leads to non-parabolicity; therefore, simple parabolic band models fail to accurately describe hole transport [6] and the concept of effective mass is less straightforward [9]. Theoretical studies have shown that the germanium hole DOS effective mass is approximately half that of silicon [10]. Germanium also has a lower optical phonon energy than silicon (37 meV compared to 62 meV [11]) which limits carrier scattering to subbands within a narrower energy range [9]. Even without a simple effective mass model to describe hole transport in semiconductors, it is clear that germanium has superior hole mobility relative to other elemental and III-V semiconductors, and consequently is well-suited for complementary logic.

1.3.4 Simulation Studies of Ge n-MOSFET Performance

Simulation studies of both bulk and double-gate ultra-thin body (DG UTB) n-MOSFETs with high mobility channels have recently been published [12], [13]. Ballistic drive current was compared for Si, Ge, GaAs, and other high electron mobility III-V semiconductors. The performance of III-V MOSFETs is limited by low inversion charge density and population of the lower mobility L valley [12]. The effects of low inversion layer capacitance are more pronounced for low equivalent oxide thickness (EOT). In general, germanium matches or outperforms III-V n-MOSFETs for EOT less than 1.5 nm for both bulk and DG UTB device geometries. In addition, Ge MOSFETs fabricated on (111) substrates always outperform silicon MOSFETs [12]. The combination of improved mobility and high inversion charge density results in superior drive current and makes Ge MOSFETs an ideal candidate for future CMOS technologies.

1.3.5 Practical Considerations

In addition to matching or exceeding the device performance of III-V semiconductors, germanium also has practical advantages over these materials. Germanium is an elemental semiconductor and is processed similarly to silicon so existing infrastructure is well-suited for germanium device fabrication. Silicon and germanium use similar dopants and dopant activation methods and both form silicides/germanides which enables self-aligned device structures. Crystal growth techniques for germanium are also well established and large-diameter germanium wafers are starting to become available; however, the world-wide supply of germanium is limited so germanium-on-insulator (GOI) is the most practical implementation. Any high mobility semiconductor will likely be integrated on a silicon platform so compatibility is an important consideration. Epitaxial growth of germanium on silicon results in a high quality interface without the risk of autodoping and cross-contamination that occurs when integrating III-V materials with Si or Ge. Furthermore, with the introduction of SiGe into the source-drain regions of Si p-MOSFETs, successful integration of germanium into high-volume CMOS manufacturing has already been demonstrated [14]. Unlike III-V semiconductors, germanium offers an evolutionary pathway to Ge CMOS, first as a source-drain material, and then perhaps as a buried-channel layer in p-FETs and finally a surface-channel layer for both n-FETs and p-FETs.

1.4 The Challenges of Germanium

In addition to the potential for improved drive current relative to silicon, germanium also presents new challenges due to differences in key material properties. Table 1.4 shows the bandgap and dielectric constant of Si and Ge [5].

Material Property	Si	Ge
Bandgap (eV)	1.12	0.66
Dielectric constant (ε_0)	11.9	16

Table 1.4: Bandgap at 300K and dielectric constant of Si and Ge.

The narrow bandgap of germanium results in increased source-drain (S/D) junction leakage while its higher dielectric constant degrades electrostatic integrity. In addition, compared to Si, n-type dopants have lower solid solubilities and diffuse rapidly in germanium making it difficult to achieve shallow junctions with sufficiently low sheet resistance. But most importantly, native insulators on germanium (GeO_2 and GeO_xN_y) do not offer the same high quality interface provided by SiO_2 on Si. For CMOS applications, the success of any alternative semiconductor requires the development of a semiconductor-dielectric interface that matches the quality of the Si-SiO_2 interface.

1.4.1 Junction Leakage

The narrow bandgap of germanium leads to increased leakage in reverse-biased p-n junctions. Under low-field reverse bias, the large minority carrier concentration of germanium results in increased minority carrier drift current across the space charge region. Under high-field conditions, occupied states in the p-Ge valence band become energetically aligned with unoccupied states in the n-Ge conduction band. As shown schematically in Figure 1.6 [15], this condition allows electrons to tunnel from the p-side to the n-side, and hence is termed band-to-band tunneling.

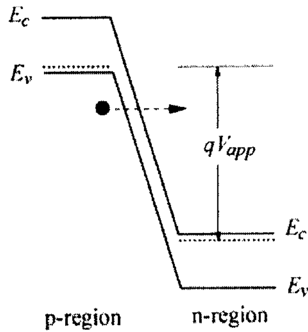


Figure 1.6: Schematic representation of band-to-band tunneling for a reverse-biased p-n junction (from [15]).

Tunneling may either be direct or indirect depending on whether the conduction and valence band minima are aligned in k-space. The magnitude of the tunneling current is determined by the efficiency of the tunneling process, which is related to the carrier effective mass, barrier width, and density of states in each band. Germanium has both a narrower bandgap and smaller effective mass than silicon, and thus a larger band-to-band tunneling current (I_{BTBT}). I_{BTBT} is highly dependent on device geometry (channel and gate oxide thickness, gate configuration, etc.). Recent simulations have shown that I_{BTBT} for Ge MOSFETs is on the order of 0.1-1 μA/μm [16], [17], which is at least several orders of magnitude higher than silicon but still comparable to the ITRS source-drain leakage target of 0.1-0.3 μA/μm [1]. Furthermore, it has been suggested that band-to-band tunneling in germanium channel devices can be reduced through the use of strained Si/Ge heterostructures [16].

1.4.2 Electrostatic Integrity

Many narrow bandgap semiconductors, including germanium and most III-Vs, also have a higher dielectric constant than silicon which contributes to reduced electrostatic integrity in short-channel devices. Ultra-thin body and double-gate device geometries may be used

to reduce the impact of dielectric constant on short-channel electrostatics and thus improve scalability. For double-gate MOSFETs with reasonable geometry (15 nm gate length, 5-10 nm channel thickness, and 1 nm oxide thickness), the subthreshold swing of a germanium device is predicted to be 10-15% larger than a corresponding silicon device [17]. The degree of electrostatic degradation ultimately depends on the specific 3D device geometry; therefore, it is difficult to simply and universally speculate whether the higher dielectric constant of germanium will be a limiting factor for short-channel devices.

1.4.3 Dopant Diffusion and Activation

Dopant diffusion and activation also play a critical role in device performance, both in terms of electrostatic integrity and S/D series resistance (R_{SD}). Dopant diffusion must be controlled in order to reduce S/D junction depth and maintain sharp doping profiles. In addition, a high electrically-active dopant concentration is required to meet future R_{SD} requirements. Any new semiconductor must be capable of achieving R_{SD} values equal to or better than silicon (currently ~180 Ω-μm [1]).

Boron and phosphorus are the most common dopants used for germanium. While the solid solubility of boron in germanium is reportedly low (5.5×10^{18} cm^{-3}), active concentrations greater than 10^{20} cm^{-3} have been achieved [18]. Due to the low diffusivity of boron in germanium, as-implanted and post-anneal profiles match very closely enabling shallow junction formation. N-type dopants, on the other hand, exhibit higher diffusivity and lower peak active concentration. Phosphorus, the most promising n-type dopant in germanium, has a solid solubility of 2×10^{20} cm^{-3}; however, to date, only peak active concentrations of 5×10^{19} cm^{-3} have been achieved [18]. Concentration-dependent diffusion and activation have also been reported for phosphorus activation at 600 °C [19]. At concentrations above 2×10^{19} cm^{-3}, a box-like profile is observed and 20-50% of phosphorus atoms are electrically active. At concentrations below 2×10^{19} cm^{-3}, no diffusion is

observed and 100% of phosphorus atoms are electrically active. Clustering is likely playing a role in the observed activation and diffusion behavior of phosphorus in germanium [18]. Table 1.5 shows state-of-the-art sheet resistance values for boron and phosphorus in Ge [18].

Dopant	Sheet Resistance (Ω/sq)	Junction Depth, x_j (nm)
B	85	70
P	75	92

Table 1.5: State-of-the-art sheet resistance values for boron- and phosphorus-implanted germanium [18].

1.5 The Germanium-Dielectric Interface

Whether junction leakage, dopant activation, or electrostatic integrity ultimately limits germanium devices strongly depends on the specific device geometry and implementation. In contrast, a high quality germanium-dielectric interface is a fundamental requirement that is independent of device implementation. Despite the challenges associated with junction leakage, dopant activation, and electrostatic integrity, *the germanium-dielectric interface remains both the most important and most challenging aspect of germanium device engineering.*

1.5.1 Germanium Surface Preparation and GeO_2

Unlike SiO_2 on silicon, germanium oxide does not provide a stable, high quality passivation on germanium. Germanium oxide exists in a number of stoichiometries (GeO_x) and crystal structures (amorphous, hexagonal, tetragonal) depending on oxidation conditions and processing history [20], [21]. Germanium oxide commonly exists as a mixture of these various forms and interconversion is possible during processing or exposure to ambient conditions [21], [22]. Hexagonal and amorphous germanium oxides are water soluble while the tetragonal form is insoluble. Because of the inherent instability of GeO_x,

controlling the stoichiometry and phase is challenging. Attempts to control the properties of GeO_2 films have resulted in reasonable quality Ge-GeO_2 interfaces (reported D_{it} ~$5x10^{11}$ cm^{-2}). However, these interfaces are still far from Si-SiO_2 interfaces in terms of quality and the proposed techniques are mainly applicable to thick dielectrics (greater than 10 nm) [20], [23]. Given the challenges associated with germanium oxide, a dielectric solution not relying on native oxide is preferable.

Due to the requirement of subnanometer EOT for future ultra-scaled MOSFETs [1], germanium oxide (or oxynitride) could only be used in a subnanometer interfacial layer between germanium and a high-k dielectric such as HfO_2. Control of ultra-thin germanium oxide layers is complicated by the lack of a stable surface termination. Unlike silicon, hydrogen-terminated germanium is not stable and is oxidized by exposure to ambient conditions [24]. Other surface terminations have been proposed (-S, -Cl, -Br, -I); however, they are also not completely stable against oxidation [24], [25] and have unknown consequences on the electrical properties of the germanium-dielectric interface.

1.5.2 High-k Dielectrics

To meet the EOT requirements for future MOSFETs, dielectrics with low permittivity (e.g. $SiO_2 \sim 3.9\varepsilon_0$) would need to be extremely thin (< 1 nm) and consequently would suffer from severe gate leakage due to direct tunneling [1]. For upcoming technology generations, the ITRS Roadmap calls for a maximum gate leakage of ~$1x10^3$ A/cm^2 for an EOT of ~1 nm. Both of these specifications cannot be simultaneously achieved with SiO_2 or SiON, therefore high-k dielectrics are required [1]. A high dielectric constant allows low EOT with a physically thicker film, thus maintaining acceptable gate leakage. Of course, incorporating high-k dielectrics into CMOS devices also presents many challenges. These materials must be thermally stable in contact with the semiconductor and gate electrode, have large band offsets (> 1.0 eV) with respect to the semiconductor, and form a high

quality interface that does not degrade carrier mobility [74], [75]. To date, Hf-based materials have proven to be the most viable option [75]. HfSiO and HfSiON exhibit reduced remote phonon scattering and improved thermal stability (including reduced interfacial SiO_2 formation) compared to HfO_2 and are the leading candidates to replace SiO_2 [75]. However, an interfacial SiO_2 or SiON layer is still required to achieve a high quality semiconductor-dielectric interface. This layer may be purposefully introduced or can be an unintentional consequence of high-k deposition on silicon. SiON has several important advantages over SiO_2 including higher dielectric constant and improved thermal stability; however, the presence of nitrogen also introduces fixed charge that can degrade carrier mobility [75]. These issues have largely been resolved [75], and companies have recently announced the use of high-k dielectrics in production [76].

1.5.3 High-k Dielectrics Directly on Germanium

The development of deposited high-k gate dielectrics for silicon CMOS devices has fueled renewed interest in semiconductors like germanium that lack a high quality native insulator. Ideally, the high-k dielectric should be deposited directly on germanium without an interfacial layer; however, a thin GeO_x layer is often present due to incomplete oxide removal during cleaning, oxidation after cleaning, or oxidation during high-k dielectric deposition. The deposition of common high-k dielectrics such as HfO_2 and ZrO_2 on cleaned germanium results in a thinner interfacial oxide layer than on silicon due to the volatility of germanium oxide [26]. For atomic layer deposition (ALD) of HfO_2 on HF-last germanium, the resulting interfacial germanium oxide layer is approximately 0.3 nm [27]. To date, high-k dielectrics deposited directly on germanium have produced interfaces with very poor electrical characteristics including large hysteresis and frequency dispersion as well as degraded mobility [28], [29], [30]. In the case of HfO_2, severe interfacial reactions [26] and germanium diffusion into the dielectric [28] have been observed during

subsequent thermal processing. For ZrO_2, the interfacial layer disappears during annealing due to germanium diffusion into the dielectric layer [26]. Interfacial reactions, interdiffusion, and the presence of germanium oxide at the interface appear to be fundamental problems for HfO_2 and ZrO_2 deposited directly on cleaned germanium surfaces. Improved device characteristics have been reported for Ge MOSFETs with ZrSiO rather than ZrO_2 [30]; however, at present, incorporating an interfacial layer between the high-k dielectric and germanium is the most promising approach for achieving a high quality germanium-dielectric interface.

1.5.4 Interfacial Layers

The interlayer must address the shortcomings of Ge-GeO_2 and Ge-(HfO_2, ZrO_2) interfaces. More specifically, the interlayer should:

- reduce interface state density,
- mitigate problems associated with interfacial GeO_x,
- prevent reactions and interdiffusion at the germanium-dielectric interface, and
- separate the inversion layer from the high-k dielectric to reduce remote coulomb and phonon scattering [31], [32].

Since it is difficult to passivate germanium surfaces against oxidation, a subnanometer layer of GeO_x is usually present on the surface prior to gate stack processing [25]. Furthermore, even if the initial surface is oxide-free, interfacial GeO_x can be formed during dielectric deposition or subsequent processing. To address the problems caused by interfacial GeO_x, the interlayer should:

- prevent GeO_x formation during processing,
- stabilize GeO_x, or
- chemically reduce GeO_x.

To date, germanium oxynitride (GeO_xN_y) [29], [33] and silicon [34] have been the most widely studied interlayers. In the case of GeON, nitrogen stabilizes the film making it

water insoluble and improving its electrical properties [35]. The use of a silicon capping layer effectively prevents GeO_x formation at the semiconductor-dielectric interface. Deposited nitrides (AlN and Hf_3N_4) and monolayer surface terminations (phosphorus and sulfur) have also been proposed as interlayers. Deposited nitride layers prevent oxidation during subsequent processing [36] but may also stabilize pre-existing oxide through nitrogen bonding. Monolayer surface treatments attempt to terminate all of the germanium surface bonds to prevent oxidation. The primary disadvantage of interlayers is the reduced EOT scalability of the dielectric stack. Aggressive EOT scaling will require reduction of the interlayer thickness and/or improved dielectric constant. GeON, silicon, metal nitride, and monolayer interlayers are discussed in detail in the following sections.

GeON

Thick germanium oxynitride was originally investigated as a standalone dielectric for germanium MOSFETs before EOT scaling demanded higher dielectric constant materials [35], [37]. More recently thin (~1 nm) GeON films have been used as interlayers between germanium and high-k dielectrics such as HfO_2 [33], [38]. Interfacial GeON improves both the physical and electrical properties of high-k dielectric stacks on germanium. HfO_2 deposited on HF-last germanium grows epitaxially and is polycrystalline while HfO_2 deposited on nitrided germanium yields an amorphous film [29]. Dielectric crystallization leads to increased gate leakage and is generally avoided. In addition, germanium oxynitride acts as a diffusion barrier and reduces germanium diffusion into the high-k dielectric [28]. MOS capacitors with GeON interfacial layers have shown significantly reduced leakage and more ideal C-V characteristics [29], [39]. Interface state densities as low as 5×10^{11} cm^{-2} have been reported for Ge-GeON interfaces [40]. It has been shown, however, that dielectric stacks with GeON interlayers are not thermally stable and suffer from a large increase in gate leakage after annealing at temperatures above 500 °C [36]. This is

particularly a problem for Ge n-FETs since the minimum activation temperature for n-type dopants is 500 °C. Furthermore, germanium oxynitride layers are not effective at preventing interfacial GeO_x formation during subsequent HfO_2 deposition [36].

Deposited Metal Nitrides

While nitridation of germanium results in a reasonable quality GeON native insulator, these films are still based on GeO_2 and suffer from poor thermal stability. As a consequence, deposited interlayers such as AlN [36], [41] and Hf_3N_4 [41] are being investigated. In principle, the composition of a deposited layer may be closely controlled and tailored to provide optimal interface characteristics. Metal nitride layers prevent oxidation during subsequent processing [36] and may also stabilize or chemically reduce pre-existing oxide. Like GeON, these interlayers suppress crystallization of the overlying high-k dielectric, reduce germanium in-diffusion, improve capacitor C-V characteristics, and reduce midgap D_{it} to reasonable levels (~1×10^{12} cm^{-2} eV^{-1} [41]). However, metal nitrides also offer advantages over GeON, namely, higher dielectric constant, improved thermal stability, and reduced formation of interfacial germanium oxide during subsequent processing [36]. It has been shown that AlN interlayers are partially oxidized during subsequent high-k deposition but are still effective at reducing GeO_x formation at the interface [36]. The higher dielectric constant of metal nitrides, especially Hf_3N_4 (ε_r~ 10) [42], enables EOT scaling while enhanced thermal stability allows higher temperature n-type S/D activation. AlN interlayers are stable to 600 °C while GeON starts to deteriorate at 500 °C [36]. However, as with Si_3N_4, AlN contains bulk traps and fixed charge that contribute to hysteresis and coulomb scattering [43], [77].

Silicon

In order to avoid the problems associated with germanium-dielectric interfaces, silicon capping layers have also been investigated [34], [44]. Very thin (~0.5 nm) silicon layers

may be epitaxially grown on germanium resulting in a high quality semiconductor-semiconductor interface. The large valence band offset (+0.51 eV [16]) between germanium and silicon forces the hole inversion layer into the underlying germanium. The conduction band edges of germanium and silicon are closely aligned (+0.05 eV [16]) so electron inversion is not confined to the underlying germanium. Silicon interlayers have several significant disadvantages. First, if inversion *does not* occur in the silicon layer it effectively acts as a dielectric and increases the effective oxide thickness. Second, if inversion *does* occur in the silicon layer, the structure does not take full advantage of germanium carrier mobility, and in the case of electrons, may suffer from intervalley scattering between the Si Δ and Ge L valleys [45]. Third, device performance will be very sensitive to small variations in silicon thickness so the manufacturability of this structure is questionable. Nevertheless, strained Si/Ge heterostructures show impressive electron and hole mobility enhancement [45] and are one of the primary options being considered for future CMOS devices.

Monolayer Surface Terminations

In an ideal germanium-dielectric interface, all germanium surface atoms are unperturbed and all bonds are properly terminated. In an attempt to achieve this ideal surface, monolayer surface terminations have been proposed for surface passivation prior to high-k dielectric deposition. It has been demonstrated that a few monolayers of sulfur terminate clean germanium surfaces and that these sulfur layers are stable up to ~200 °C [46]. Sulfur incorporation into germanium oxide has recently been reported [47]. Phosphorus-based surface treatments have also been investigated [48]. It was shown that phosphine plasma treatment at 400 °C provided similar benefits to AlN interfacial layers: suppression of germanium oxide formation, germanium in-diffusion, and high-k crystallization as well as improved thermal stability and carrier mobility. Nonetheless, monolayer termination

approaches are highly speculative and it is unclear what effect they have on the electronic properties of germanium-dielectric interfaces.

1.6 Historical Germanium MOSFET Performance

While MOS C-V characteristics are important for evaluating germanium-dielectric interfaces, device performance is the ultimate metric for assessing Ge MOSFETs. Efforts to develop germanium MOSFETs with high-k gate dielectrics started in 2002. Figure 1.7 shows electron and hole mobility at constant vertical effective field for bulk germanium MOSFETs reported since that time. Silicon universal electron and hole mobility are shown for reference. Results that have been difficult to reproduce and are not consistent with other published data are denoted by black circles. These results are not included in the discussion that follows. Table 1.6 provides a more detailed description of the data points in Figure 1.7, including the gate stack materials and dielectric deposition method.

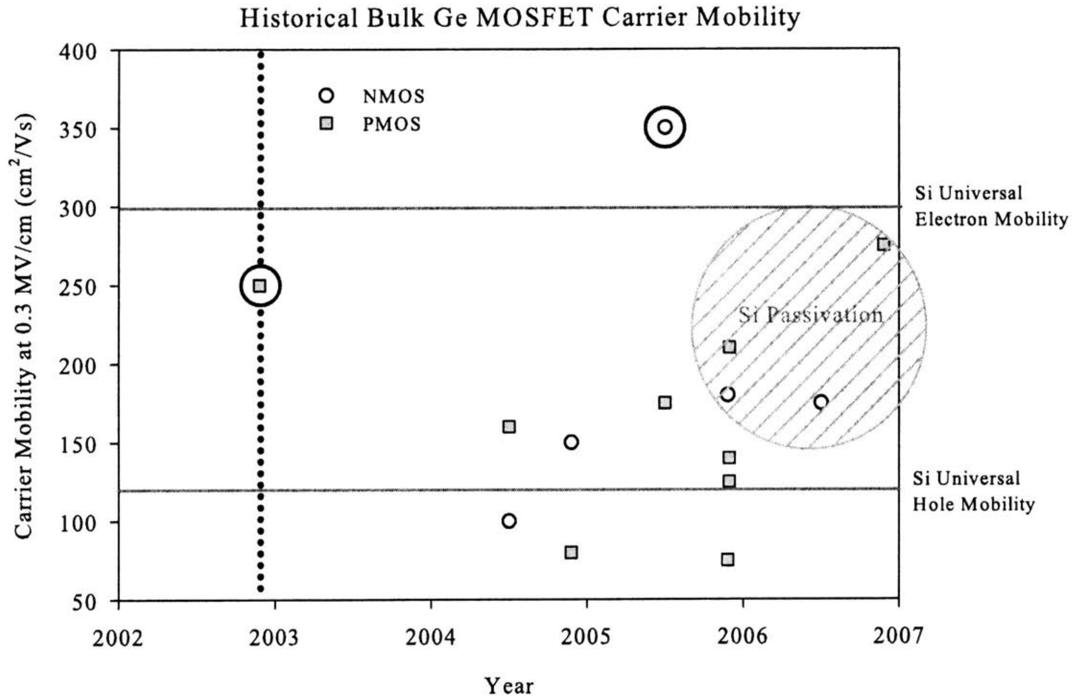


Figure 1.7: Carrier mobility at 0.3 MV/cm for Ge MOSFETs reported since 2002. Silicon universal electron and hole mobility are shown for reference. Results that have been difficult to reproduce and are not consistent with other published data are denoted by black circles. Results from silicon interlayers are denoted by the cross-hatched circle.

Year	Gate Stack Description (Dielectric Deposition Method)	Carrier Mobility at 0.3 MV/cm		Reference
		NMOS	PMOS	
2002	Pt/ZrO_2/Ge (PVD followed by UV ozone oxidation)	-	250	[49]
2004	Al/SiO_2/GeON/Ge (thermal oxidation followed by nitridation)	100	160	[40], [50]
2004	TaN/HfO_2/(AlN or PH_3 treatment)/Ge (MOCVD and ALD)	150	80	[48]
2005	(IrO_2 or IrO_2/Hf)/$LaAlO_3$/Ge (PVD)	350	175	[51]

Table 1.6: Gate stack materials and deposition method for mobility results summarized in Figure 1.7.

Year	Gate Stack Description (Dielectric Deposition Method)	Carrier Mobility at 0.3 MV/cm		Reference
		NMOS	PMOS	
2005	Mo/ZrO_2/Ge (PVD)	-	75	[30]
2005	Mo/ZrSiO/Ge (PVD)	-	125	[30]
2005	TaN/HfO_2/GeON/Ge (thermal nitridation followed by MOCVD)	-	140	[44]
2005	TaN/HfO_2/Si/Ge (MOCVD)	180	210	[44]
2006	TaN/HfO_2/Si/Ge (MOCVD)	175	-	[52]
2006	TiN/HfO_2/Si/Ge (ALD)	-	275	[34]

Table 1.6: Gate stack materials and deposition method for mobility results summarized in Figure 1.7.

As shown in Figure 1.7, enhanced hole mobility in Ge MOSFETs has been demonstrated by a number of groups. The best results have been achieved with thin (~0.5 nm) silicon interlayers with 3x enhancement recently being demonstrated [34]. Silicon capping avoids the germanium-dielectric interface problem and the large valence band offset between germanium and silicon effectively results in a buried-channel device. Manufacturability and EOT scalability are major drawbacks of this approach. Surface-channel p-FETs with high-k dielectrics have shown a much less impressive average enhancement of 0.4x. In contrast to the success of Ge p-FETs, n-FETs have shown mobilities far below silicon universal electron mobility, independent of gate stack composition and deposition method. Even n-FETs with silicon interlayers have shown disappointing results. The inversion layer in these devices is not buried due to the small conduction band offset and intervalley scattering may be occurring at the heterointerface [45].

While hole mobility enhancement has been seen for a wide variety of gate dielectric materials and processes, electron mobility has been universally poor. Successful demonstration of Ge n-MOSFETs will require better understanding of electron transport at germanium-dielectric interfaces and the development of new methods to passivate the interface.

1.7 Goals of Thesis

As demonstrated by recent published data, much progress has been made on Ge MOSFETs, particularly p-FETs. Nonetheless, passivation of the germanium-dielectric interface remains a serious challenge and the low mobility observed in Ge n-FETs is poorly understood. In this work, the device characteristics of Ge MOSFETs with nitride interlayers are evaluated. ALD metal nitrides (AlN and Hf_3N_4) are the primary focus; however, germanium oxynitride is also investigated. The specific goals of this thesis are to:

- develop, optimize, and characterize AlN interlayer gate stacks,
- assess the device performance of Ge MOSFETs with nitride interlayers, and
- understand the impact of the germanium-dielectric interface on carrier transport.

1.8 Organization of Thesis

The remainder of this thesis is organized into four chapters. Chapter 2 reviews atomic layer deposition and describes the development of ALD gate stacks based on AlN interlayers. Optimization and characterization of $WN/Al_2O_3/AlN$ gate stacks are discussed. Chapter 3 presents the device characteristics of Ge n- and p-MOSFETs with AlN, Hf_3N_4, and GeON interlayers. Carrier mobility is extracted for each interlayer and summarized at the end of the chapter. Chapter 4 discusses the impact of interface states on carrier transport in $WN/Al_2O_3/AlN$ Ge MOSFETs. Low temperature device characterization is used to examine the temperature dependence of mobility and also extract interface state density near the band edge. Buried-channel MOSFETs are used to reduce the interaction of carri-

ers with interface states. Chapter 4 also presents evidence of phosphorus passivation of the germanium-dielectric interface. And last, Chapter 5 summarizes the conclusions and contributions of this thesis, and discusses opportunities for future work.

Chapter 2

Atomic Layer Deposition of High-k Dielectric Stacks on Germanium

2.1 Introduction

Atomic layer deposition (ALD) allows a wide variety of materials to be deposited with layer-by-layer precision. This exquisite control over thickness and composition makes ALD particularly well-suited for the deposition of thin interfacial layers (0.5-2.0 nm) and high-k dielectrics for MOSFET applications. A model dielectric stack process consisting of an RCA-based clean followed by an aluminum nitride (AlN) interfacial layer and aluminum oxide (Al_2O_3) capping layer was selected for this work. AlN is one of only a few dielectric layers (GeON [50], AlN [48], Hf_3N_4 [41], $LaAlO_3$ [51]) that have produced functional Ge n-MOSFETs. In addition to reducing Ge diffusion into the high-k dielectric and suppressing interfacial GeO_x formation [36]), AlN also has a medium dielectric constant (ε_r~ 7-10) which makes it suitable for use as an interlayer in scaled dielectric stacks. Al_2O_3 was chosen as a capping layer for practical reasons. It is easily deposited using the same precursor and substrate temperature as AlN, and also exhibits low leakage at the thicknesses used in this work (3.5- 6 nm). To achieve low EOT, the Al_2O_3 capping layer could be replaced by a high dielectric constant material such as HfO_2. This chapter describes the optimization and characterization of Al_2O_3/AlN dielectric stacks on germanium with particular focus on AlN thickness and post-metal anneal (PMA) optimization, and interface state density (D_{it}) characterization. The purpose of this study was to understand the basic properties of Al_2O_3/AlN dielectric stacks, including thermal stability, while developing a gate stack suitable for investigating carrier transport in Ge MOSFETs. This chapter begins with a brief review of atomic layer deposition and then presents the

results of the Al_2O_3/AlN study. The conclusions drawn in this chapter are specific to the model dielectric stack process described above. Surface preparation and interfacial layer formation are tightly coupled, dependent processes. Recent evidence that will be discussed at the end of this chapter suggests that alternative surface preparations may be superior to the preparation used in this work, and that the optimal dielectric stack for these surfaces may be different than for RCA-cleaned surfaces.

2.2 Brief Review of Atomic Layer Deposition

Atomic layer deposition utilizes alternating pulses of precursors that undergo self-limiting reactions with the substrate and each other. Unlike chemical vapor deposition (CVD), the precursors are introduced into the chamber sequentially rather than simultaneously [53]. Atomic layer deposition occurs in four distinct steps which together are called an *ALD cycle* [54]:

1. Reactant A is pulsed into the chamber and chemisorbs on the surface forming a monolayer (ideal case).
2. Unreacted molecules of reactant A and by-products are removed from the chamber.
3. Reactant B is pulsed into the chamber and undergoes a self-limiting reaction with the chemisorbed molecules of reactant A.
4. Unreacted molecules of reactant B and by-products are removed from the chamber.

Figure 2.1 shows a schematic representation of the ALD reaction between trimethylaluminum (TMA) and water to form Al_2O_3 [55]. ALD processes typically begin with a hydroxyl (-OH) terminated surface as shown Figure 2.1a. Figures 2.1b and 2.1c show TMA undergoing a self-limiting reaction with surface hydroxyl groups followed by the removal of excess TMA and reaction by-products (CH_4). Figures 2.1d and 2.1e show water reacting with the remaining methyl groups on the chemisorbed TMA molecules followed by the removal of excess water and reaction by-products (CH_4). Note that at the end of the cycle, the surface is again hydroxyl terminated.

Substrate temperature affects substrate-precursor interactions as well as precursor stability and reactivity [53]. The substrate temperature range over which surface-limited ALD growth occurs is referred to as the *ALD window.* An ideal ALD process should be independent of precursor dose and exhibit a linear growth rate. Further information on ALD may be found in references 53 and 54.

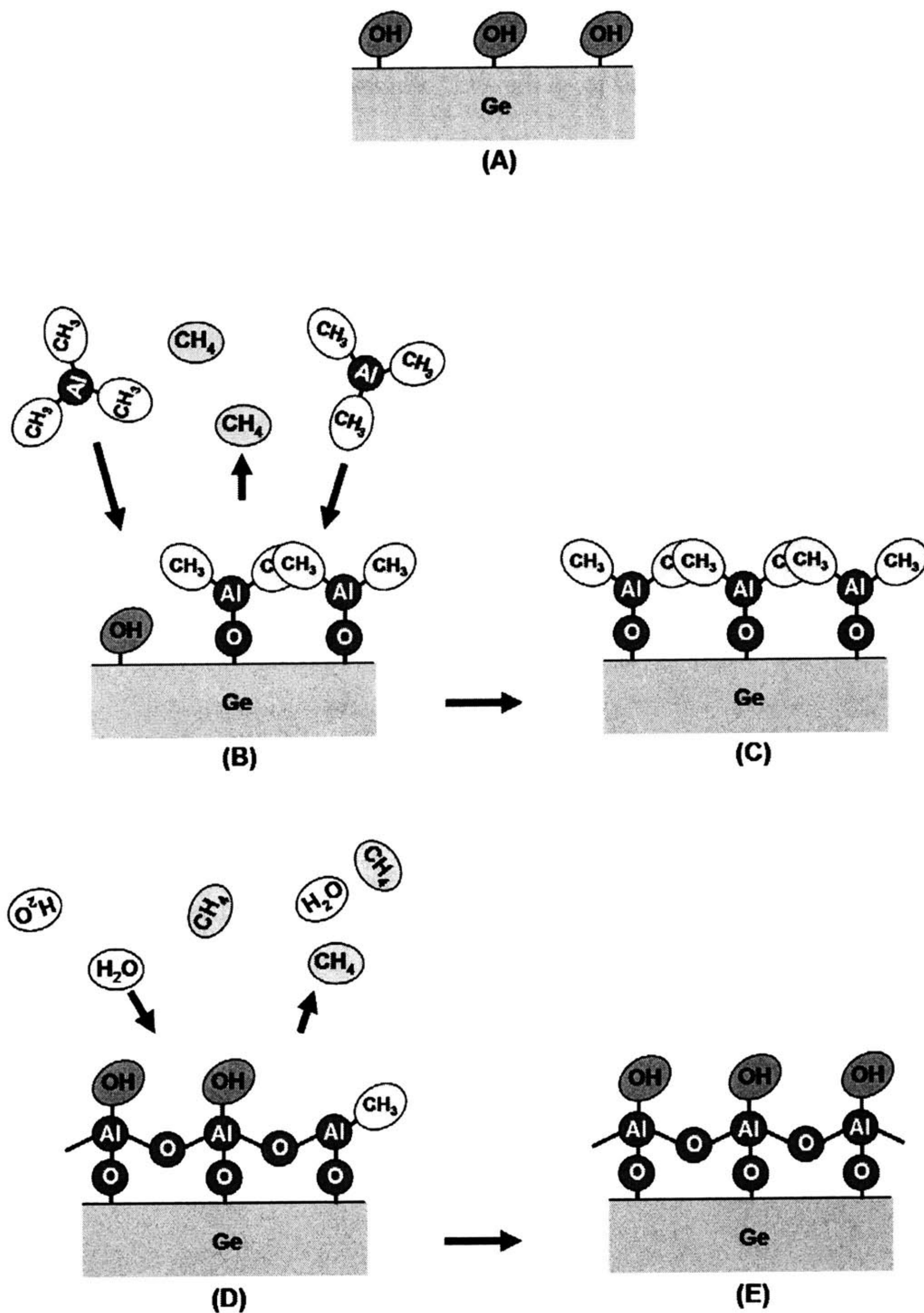


Figure 2.1: Schematic representation of reactions that comprise an ALD cycle. The reaction between trimethylaluminum (TMA) and water to form Al_2O_3 is used as an example (adapted from [55]).

2.3 ALD Gate Stack Films

The ALD gate stacks in this work consisted primarily of Al_2O_3/AlN dielectric stacks capped with a tungsten nitride (WN) electrode. The majority of the these films were deposited using a Cambridge NanoTech Savannah 200 ALD reactor installed in the Microsystems Technology Laboratory at MIT. Other high-k dielectrics (Hf_3N_4, $GdScO_3$, $LaAlO_3$) were deposited by K. Kim and R. Gordon at Harvard University.

2.3.1 Atomic Layer Deposition of AlN and Al_2O_3

AlN and Al_2O_3 were deposited using tris(dimethylamido)aluminum (TDMAA) and either ammonia or water as the co-reactant, respectively [41], [56]. The TDMAA bubbler temperature was 115 °C and a nitrogen carrier stream delivered the reactants from the precursor manifold to the chamber. The substrate temperature was 200 °C. Detailed process parameters are contained in Appendix A. SIMS analysis of a thick (50 nm) AlN film was performed to quantify the carbon and oxygen concentration in the film. The carbon and oxygen concentrations were 3.8×10^{20} cm^{-3} and 4.5×10^{20} cm^{-3}, respectively, or 0.8% and 0.9% assuming an atomic density of 5×10^{22} cm^{-3}. The growth rate of AlN and Al_2O_3 was 0.9-1.0 Å/cycle, as measured by spectroscopic ellipsometry.

2.3.2 Atomic Layer Deposition of WN

WN was deposited using bis(tertbutylimido)-bis(dimethylamido)tungsten with ammonia as the co-reactant [57]. The tungsten bubbler temperature was 90 °C and a nitrogen carrier stream delivered the reactants from the precursor manifold to the chamber. The substrate temperature was 340-375 °C. Detailed process parameters are contained in Appendix A. WN resistivity was measured using the four-point probe technique and was consistent with values reported in the literature (1.5×10^{-3}- 4.0×10^{-3} Ω-cm [57]). The WN growth rate was approximately 0.5 Å/cycle.

2.4 Review of MOS Capacitor Electrical Characterization

Impedance analysis is the most common method for evaluating the electrical properties of semiconductor-dielectric interfaces. The impedance of an MOS capacitor is typically measured as a function of gate bias and frequency. Measurement frequencies range from DC (quasistatic) to 1 MHz. Using an appropriate equivalent circuit model, relevant parameters of the device under test (e.g. capacitance, conductance, etc.) can be extracted. Imperfect semiconductor-dielectric interfaces require a more complex equivalent circuit to capture the effects of interface states and other non-idealities. Figure 2.2 shows the small-signal equivalent circuit model for an MOS capacitor with interface states [59]. The interface state capacitance is represented by C_{it} while R_{it} models losses due to the interface states' inability to respond in-phase with the applied signal. The time constant of the states, τ_{it}, is simply $C_{it}R_{it}$. C_{ox} and C_s represent the oxide and semiconductor capacitance, respectively.

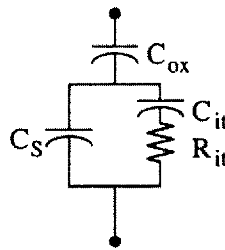


Figure 2.2: Small-signal equivalent circuit model for MOS capacitor with interface states (from [59]).

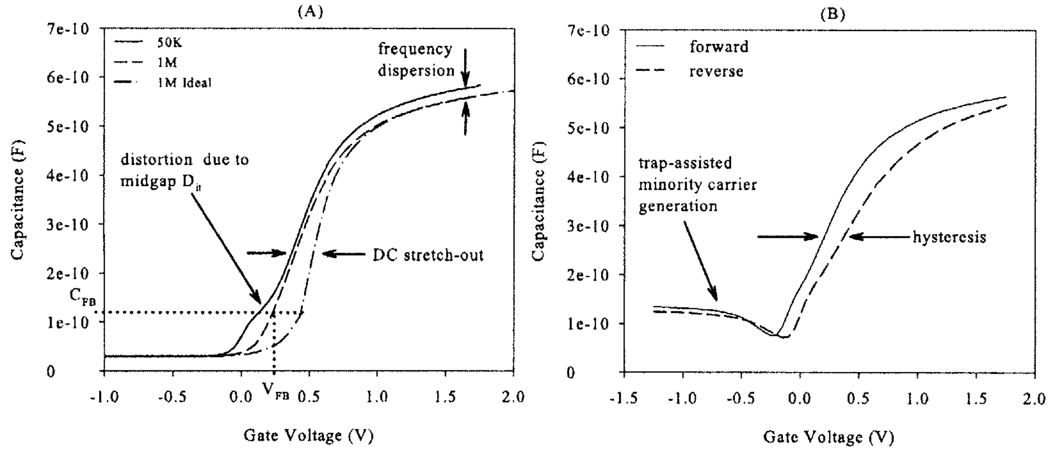


Figure 2.3: Common non-idealities observed in MOS capacitors. (A) Midgap D_{it} distortion, DC stretch-out, V_{FB} shift, and frequency dispersion. (B) Hysteresis and trap-assisted minority carrier generation.

At low frequency ($f < (2\pi\tau_{it})^{-1}$), distortion of the C-V characteristics is typically observed due to interface states that are able to respond at that frequency. Figure 2.3a shows 50 kHz and 1 MHz C-V characteristics for an MOS capacitor with midgap interface states. An ideal simulated 1 MHz curve without interface states is included for reference. This curve was generated using MISFIT, a C-V simulation program for Si and Ge MIS structures [72]. At 50 kHz, C-V distortion is clearly visible however at 1 MHz the interface states are unable to respond and do not contribute to the measured capacitance. In addition to C-V distortion, interface states also produce DC "stretch-out". Interface states must be filled as the Fermi level is swept through the bandgap thus requiring a larger voltage sweep to go from depletion to accumulation. This also produces a shift in flatband voltage (V_{FB}). The capacitance corresponding to the flatband condition (C_{FB}) can be determined from simulation, and thus V_{FB} is simply the voltage at which the measured capacitance equals C_{FB}. Figure 2.3a also shows frequency dispersion (frequency dependence of capacitance) in accumulation. This can be caused by problems intrinsic to the dielectric and semiconduc-

tor-dielectric interface as well as external parasitics (e.g. series resistance due to the gate and/or substrate). Another common problem in MOS capacitors is C-V hysteresis which is shown in Figure 2.3b. This plot shows both forward (depletion to accumulation) and reverse (accumulation to depletion) voltage sweeps. During measurement, charge can be injected into bulk traps in the dielectric or stored in slow interface states which produces a flatband voltage shift. This shift is clearly evident during the reverse voltage sweep. Figure 2.3b also shows the effect of minority carrier generation. At typical measurement frequencies (10 kHz to 1 MHz), inversion capacitance increase is not observed in MOS capacitors due to the low generation/recombination rate of minority carriers that prevents them from responding at these frequencies. However, for narrow bandgap semiconductors or in the case of significant trap-assisted generation/recombination, some level of capacitance increase in inversion can be observed in MOS capacitor C-V characteristics as shown in Figure 2.3b. For Si-SiO_2 interfaces, minority carrier generation has been observed due to bulk trap states in the semiconductor [73].

Since many of the non-idealities described above are very sensitive to sweep conditions, it is important to perform the measurements in a consistent manner. In this work, all C-V characteristics were measured using an Agilent IBASIC program that holds the gate voltage at the first sweep point for 1 s before starting the forward and reverse sweeps. Also, the maximum bandwidth setting of the Agilent 4294A Impedance Analyzer was used to minimize measurement time (1-10 ms/point) thereby capturing transient effects. By holding the forward and reverse sweep start voltage for 1 s and minimizing total measurement time, the measured hysteresis is "worst case" because the interface has little time to relax. In addition, the use of an automated program ensures that measurements are repeatable and allows fair comparison across different samples. The Agilent IBASIC program is listed in Appendix B.

2.5 ALD Gate Stack Capacitor Fabrication and Characterization

Germanium capacitors were fabricated to optimize and characterize Al_2O_3/AlN dielectric stacks. Initial experiments used an *ex-situ* sputtered aluminum gate electrode while later experiments used an *in-situ* ALD WN gate electrode. Al electrode capacitors were used to verify the film growth mechanism and also to estimate the dielectric constant of ALD AlN and Al_2O_3. Gate stack optimization and interface state characterization were performed on WN electrode capacitors. From a process integration perspective, aluminum is not a practical gate material because of its low melting point and poor chemical resistance, so WN was used in MOSFET fabrication. In addition, Al-gated MOS capacitors exhibited poor thermal stability characterized by a large increase in hysteresis during 400- 500 °C anneals. WN-gated capacitors were stable up to 500 °C and in general, the electrical characteristics improved with increasing PMA temperature from 350 to 500 °C.

2.5.1 Al/Al_2O_3/AlN/Ge capacitors

Experimental Description

Capacitors were fabricated on (100) Ga-doped p-type substrates with resistivity of 0.12-0.17 Ω-cm and (100) Sb-doped n-type substrates with resistivity of 0.13-0.16 Ω-cm. The wafers were cleaned using the modified RCA clean described in Appendix A. The dielectric stacks shown in Table 2.1 were deposited on both n- and p-Ge followed by *ex-situ* Al sputtering (200 nm) on the frontside of the wafer and Ti/Au sputtering (50 nm/ 200 nm) on the backside of the wafer. The aluminum gate electrodes were patterned using photolithography and wet etching. In this document, Al_2O_3/AlN dielectric stacks are denoted by the number of Al_2O_3 cycles followed by the number of AlN cycles (e.g. 50/20).

ALD Run No.	Al_2O_3 cycles/AlN cycles
41	50/20
42	50/30
43	100/30
44	50/10

Table 2.1: Dielectric stack splits for Al/Al_2O_3/AlN/Ge capacitors. Stacks are defined by number of Al_2O_3 cycles and number of AlN cycles (Al_2O_3 cycles/ AlN cycles)

Electrical Results

The first step in characterizing any ALD process is to verify that surface-limited ALD growth is actually occurring. In the case of a dielectric, this can be accomplished by measuring capacitance as a function of the number of ALD cycles. Table 2.2 summarizes the capacitance equivalent thickness (CET) for n- and p-Ge capacitors after 350 °C 30 min. N_2 post-metal annealing. CET is simply the equivalent SiO_2 thickness corresponding to the peak measured capacitance. Figure 2.4 shows CET vs. total number of ALD cycles for the p-Ge capacitors in Table 2.2. The linear relationship between CET and total number of cycles verifies ALD deposition and also suggests that the deposition rate and dielectric constant of AlN and Al_2O_3 result in similar effective thickness per cycle. Since the deposition rates are similar (0.9-1.0 Å/cycle), the relative dielectric constants are also similar (ε_r ~6-7 for both films). The y-intercept in Figure 2.4 at zero cycles indicates the presence of an ultra-thin (0.38 nm CET) interfacial oxide. The composition of this layer is a matter of speculation but likely includes Ge, Al, O, and N.

These capacitors exhibited poor thermal stability, as evidenced by a large increase in hysteresis, at post-metal anneal temperatures above 350 °C. Furthermore, aluminum is not suitable for use as a MOSFET gate electrode and *ex-situ* gate electrode deposition exposes the gate dielectric to ambient conditions after deposition. For these reasons, most optimi-

zation and characterization was performed on WN electrode capacitors, and is discussed in the following sections. C-V characteristics of the Al-gated capacitors are summarized in Appendix C.

Dielectric Stack	n-Ge CET (nm)	p-Ge CET (nm)
10/50	3.97	3.82
20/50	4.45	4.40
30/50	4.65	4.91
30/100	7.63	7.81

Table 2.2: Capacitance equivalent thickness for Al/Al_2O_3/AlN/Ge capacitors.

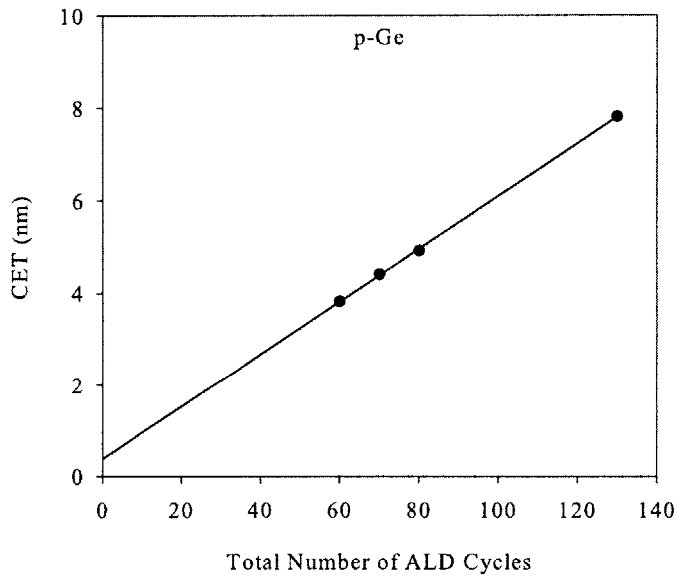


Figure 2.4: CET of Al/Al_2O_3/AlN/p-Ge capacitors vs. total number of ALD cycles. Y-intercept of 0.38 nm indicates the presence of an ultra-thin interfacial oxide.

2.5.2 WN/(Al_2O_3,AlN)/Ge Capacitors

Al_2O_3/AlN dielectric stacks were primarily evaluated using *in-situ* ALD WN gate electrodes. *In-situ* gate electrode deposition prevents the dielectric from being exposed to ambient conditions and the thermal stability of WN allows higher temperature post-metal annealing. In this section, the C-V characteristics of Al_2O_3/AlN stacks are compared to pure Al_2O_3 and AlN films to clearly demonstrate the benefits of thin (~2 nm) AlN interlayers. The impact of post-metal annealing on capacitors with 1.5 nm and 2.5 nm AlN interlayers is then discussed. And finally, the results of interface state characterization are presented.

Experimental Description

Capacitors were fabricated on (100) Ga-doped p-type substrates with resistivity of 0.12-0.17 Ω-cm and (100) Sb-doped n-type substrates with resistivity of 0.13-0.16 Ω-cm. The wafers were cleaned using the modified RCA clean described in Appendix A. The WN/(Al_2O_3,AlN) gate stacks shown in Table 2.3 were deposited on both n- and p-Ge followed by *ex-situ* Al sputtering (250 nm) on the frontside of the wafer and Ti/Al sputtering (20 nm/ 1 μm) on the backside of the wafer. The aluminum metallization was patterned using photolithography and wet etching. Using the same resist mask, the WN gate electrode was etched using CF_4 RIE. The capacitors were then annealed as shown in Table 2.4. The "as-deposited" samples did not receive a post-metal anneal but did receive the thermal budget associated with WN deposition (approximately 350 °C for 6 hrs. in N_2).

ALD Run No.	Al_2O_3 cycles/AlN cycles
104	45/15
105	35/25
111	60/00
113	00/60

Table 2.3: Dielectric stack splits for WN/(Al_2O_3, AlN)/Ge capacitors. Stacks are defined by number of Al_2O_3 cycles and number of AlN cycles (Al_2O_3 cycles/ AlN cycles).

Temperature (°C)	Time (min.)	Ambient
as-deposited	-	-
350	30	FG
400	1	N_2
450	30	FG
450	1	N_2
500	30	FG
500	1	N_2
550	30	FG
550	1	N_2

Table 2.4: Post-metal anneal splits for WN/Al_2O_3/AlN/Ge capacitors. FG= 8:1 N_2:H_2.

Impact of AlN Interlayer Thickness on C-V Characteristics

Figure 2.5 shows C-V characteristics at 50 kHz, 100 kHz, and 1MHz for as-deposited gate stacks. The left column shows p-Ge while the right column shows n-Ge. The CET for these capacitors is approximately 3 nm with p-Ge having slightly higher peak capacitance than n-Ge. This CET corresponds to an average relative dielectric constant of 7-8. This value is slightly higher than for Al-gated capacitors, probably due to the enhanced stability of WN/Al_2O_3 interfaces compared to Al/Al_2O_3 interfaces. Figures 2.5a and 2.5d show results from gate dielectric stacks consisting of pure Al_2O_3 and AlN, respectively. Al_2O_3 directly on germanium produces significant hysteresis for both p- and n-Ge (250 mV and 500 mV). DC stretch-out and distortion due to interface states are also evident. AlN directly on germanium produces poor C-V characteristics for both p- and n-Ge and large hysteresis for n-Ge. The WN/AlN/p-Ge capacitor shows inversion behavior due to trap-assisted minority carrier generation. The WN/AlN/n-Ge capacitor shows severe distortion, particularly near accumulation. In contrast, the capacitors in Figures 2.5b and 2.5c with WN/Al_2O_3/AlN gate stacks show significantly improved C-V characteristics with reduced stretch-out, distortion, and hysteresis. In addition to better-behaved C-V characteristics, WN/Al_2O_3/AlN stacks also exhibit low gate leakage ($< 10^{-6}$ A/cm^2) as shown in Figure 2.6. These results clearly demonstrate the benefit of using thin (1.5- 2.5 nm) AlN interlayers.

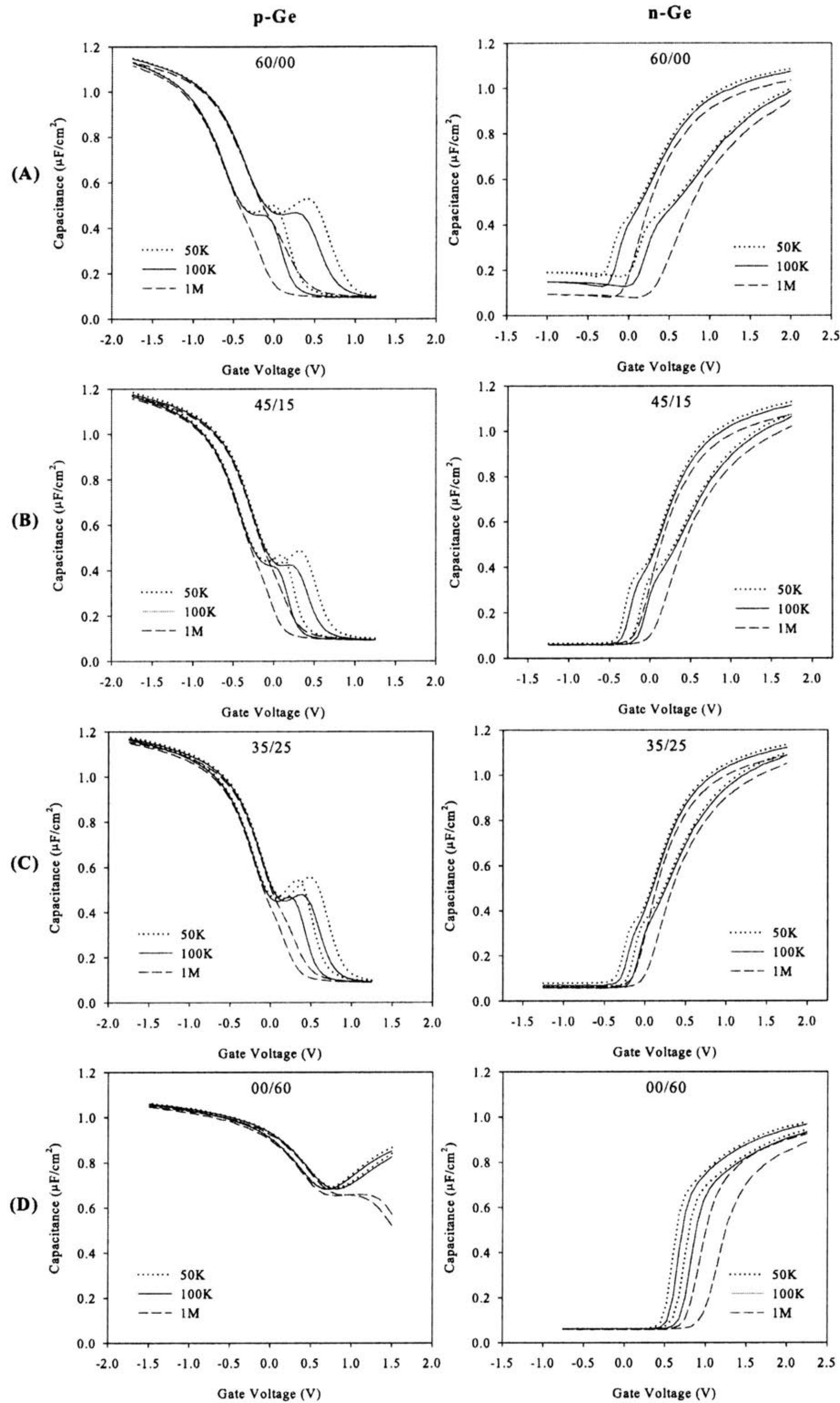


Figure 2.5: Forward and reverse sweep C-V characteristics of as-deposited WN/(Al_2O_3, AlN)/Ge capacitors at 50 kHz, 100 kHz, and 1 MHz. (A) 60/00 Al_2O_3/AlN (B) 45/15 Al_2O_3/AlN (C) 35/25 Al_2O_3/AlN (D) 00/60 Al_2O_3/AlN.

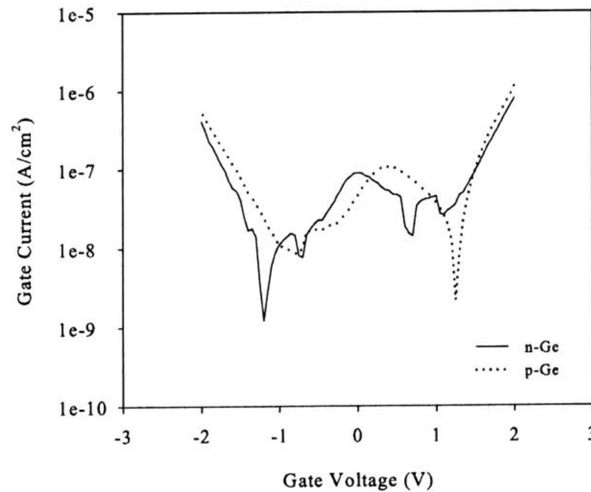


Figure 2.6: Gate leakage for WN/ 35 cycle Al_2O_3/ 25 cycle AlN gate stacks on n- and p-Ge.

Impact of Post-Metal Annealing on C-V Characteristics

Post-metal annealing is a critical step for high-k dielectrics, particularly ALD films deposited at low temperature (200 °C), that is used to improve the electrical properties of as-deposited gate stacks. However, degradation of germanium-dielectric interfaces has also been observed during subsequent thermal processing. The purpose of this experiment was to determine the optimal post-metal anneal and investigate the thermal stability of these gate stacks at n-type S/D activation temperatures (500- 550 °C).

Due to the large number of unique samples (approximately forty), several simple metrics were developed to facilitate sample comparison. Hysteresis is a common metric for C-V characteristics; however, some capacitors in this work exhibit variable hysteresis depending on the magnitude of the capacitance, so a single value does not sufficiently describe the hysteretic behavior. To address this issue, hysteresis values were extracted at 20% (H-20) and 80% (H-80) of peak normalized capacitance as demonstrated in Figure 2.7a. The difference between these two hysteresis values can also provide useful information. For example, slow detrapping of charge trapped during accumulation will result in

larger hysteresis at 80% C/C_{max} than at 20% C/C_{max}. This difference provides insight into the severity and time constant of interface trapping.

In addition to hysteresis, C-V distortion due to midgap interface states is also a useful metric for comparing C-V characteristics. While hysteresis provides information on charge injection and trapping, C-V distortion provides complementary information on midgap D_{it}. In this work, the area difference between the 50 kHz and 1 MHz curves (shown in Figure 2.7b as ΔQ) serves as the quantitative metric for midgap D_{it}. 50 kHz and 1 MHz curves sometimes show frequency dispersion in accumulation so each curve is normalized separately to ensure that ΔQ is due to midgap D_{it} and not to frequency dispersion in accumulation. Trap-assisted minority carrier generation can also produce a deviation in low and high frequency C-V characteristics in the depletion/inversion regime. While this effect is not due to midgap interface states [73], it is still undesirable and will get included in the ΔQ metric. Thus for samples with high ΔQ, the C-V characteristics must be examined to determine whether it results from minority carrier generation or midgap D_{it}.

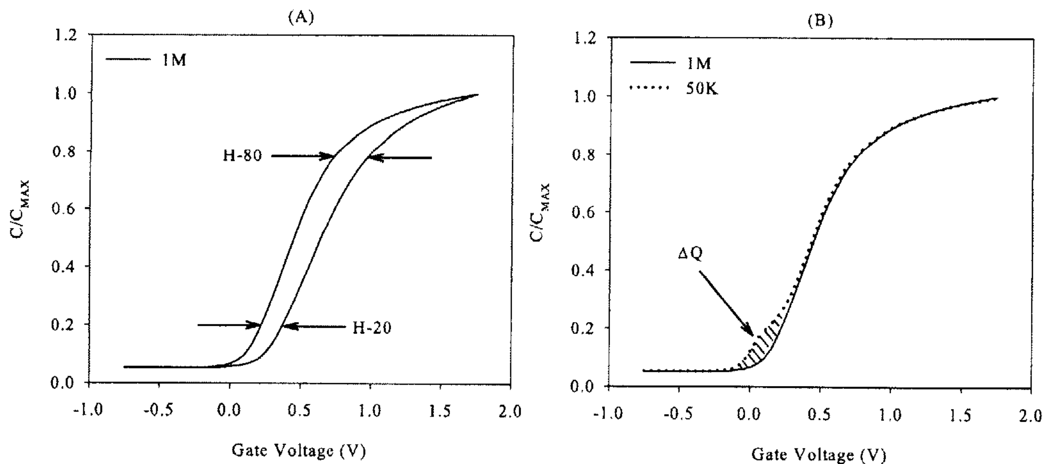


Figure 2.7: Metrics used to compare C-V characteristics of MOS capacitors. (A) Hysteresis extracted at 20% (H-20) and 80% (H-80) of C/C_{max} and (B) ΔQ extracted from separately normalized 50 kHz and 1 MHz forward-sweep C-V characteristics.

Since dielectric stacks with AlN interlayers exhibit the most promising as-deposited electrical characteristics, these samples were used to study the impact of post-metal annealing. The WN/45 cycle Al_2O_3/15 cycle AlN and WN/35 cycle Al_2O_3/25 cycle AlN gate stacks will simply be denoted by their AlN thickness (1.5 nm and 2.5 nm, respectively). Both stacks have similar total thickness and peak capacitance, so AlN thickness is the differentiating parameter for these stacks. These capacitors were subjected to the post-metal annealing conditions listed in Table 2.4.

Figure 2.8 shows ΔQ vs. anneal temperature for (A) 60 s N_2 and (B) 30 min. FG annealing. As will be the case for all plots in this section, n-Ge and p-Ge capacitors are denoted by closed and open symbols, respectively. Additionally, 1.5 nm and 2.5 nm AlN interlayer thicknesses are indicated by circles and squares, respectively. The actual C-V characteristics used to extract ΔQ and hysteresis are shown in Appendix D. For most samples, ΔQ decreases with increasing anneal temperature. For 60 s N_2 annealing, reduction in ΔQ is seen up to 550 °C. For 30 min. FG annealing, ΔQ decreases up to 450 °C but no additional reduction is observed at 500 and 550 °C. The ultimate reduction in ΔQ is similar for 60 s 550 °C N_2 and 30 min. 450 °C FG annealing suggesting that thermal budget, rather than anneal ambient, is responsible for the decrease in midgap D_{it}. Most samples followed the general trends outlined above, however, there was one notable exception. The 2.5 nm AlN n-Ge capacitor shows a large increase in ΔQ when annealed in nitrogen. Examination of the C-V characteristics for this sample (see Appendix D) shows trap-assisted minority carrier generation. The precise physical mechanism responsible for enhanced minority carrier generation in these samples is not known; however, similar behavior in Si MOS capacitors has been attributed to bulk semiconductor traps [73].

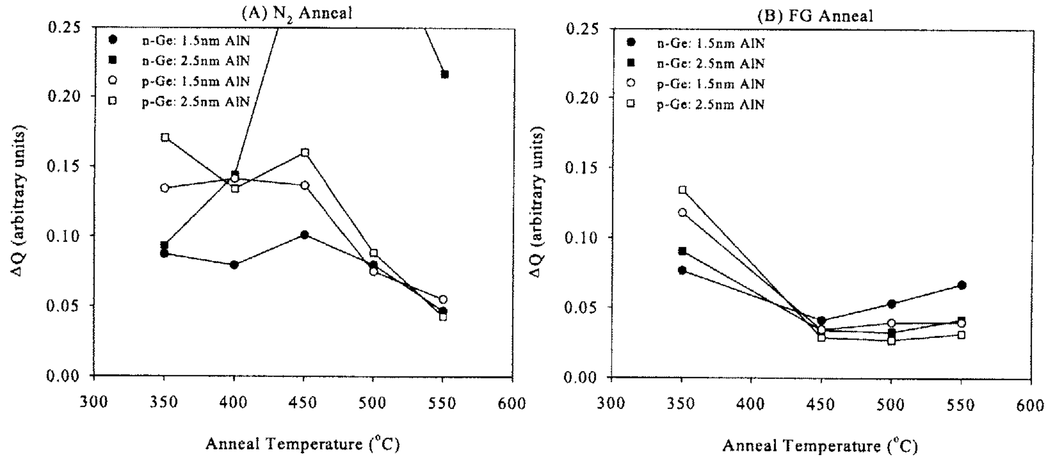


Figure 2.8: ΔQ vs. anneal temperature for n- and p-Ge capacitors with 1.5 and 2.5 nm AlN interlayers. (A) 60 s N_2 annealing. (B) 30 min. FG annealing. n-Ge and p-Ge capacitors are denoted by closed and open symbols, respectively. 1.5 nm and 2.5 nm AlN interlayer thicknesses are indicated by circles and squares, respectively. The N_2 anneal data point at 350 °C is from the as-deposited sample.

Figure 2.9 shows hysteresis at 20% C/C_{max} vs. anneal temperature for (A) 60 s N_2 and (B) 30 min. FG annealing. At temperatures below 500 °C, 1.5 nm and 2.5 nm AlN interlayers show hysteresis values of 150- 225 mV and 100- 150 mV, respectively. For N_2 annealing, hysteresis reaches a minimum at 500 °C before increasing slightly for p-Ge and rapidly for n-Ge at 550 °C. For FG annealing, n-Ge hysteresis reaches a minimum at 400-450 °C before increasing rapidly at 500 and 550 °C while p-Ge reaches a minimum at 500 °C and increases rapidly at 550 °C. Again, differences between N_2 and FG annealing appear to be due to thermal budget (i.e. anneal time and temperature) rather than anneal ambient. In general, n-Ge capacitors exhibit less thermal stability than p-Ge capacitors. In N_2, both are stable up to 500 °C, however hysteresis increases more rapidly in n-Ge at 550 °C, and in FG, n-Ge is stable to 450 °C while p-Ge is stable to 500 °C. It is interesting to note that n- and p-Ge have similar H-20 values before degradation at high temperature. Capacitors with 2.5 nm interlayers also tend to have lower hysteresis than capacitors with

1.5 nm interlayers. Since the interfacial region is quite complex, this observation is difficult to rationalize with simple bulk/interface trap theory.

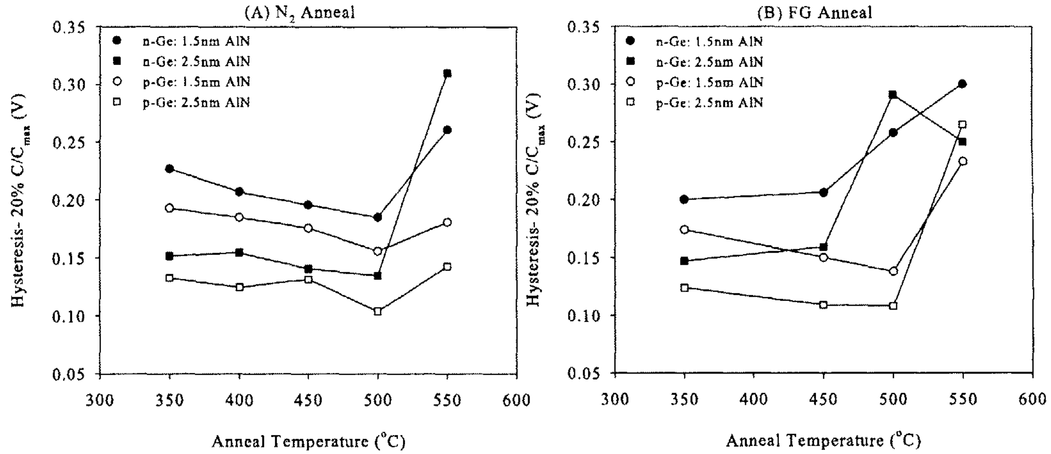


Figure 2.9: Hysteresis at 20% C/C_{max} vs. anneal temperature for n- and p-Ge capacitors with 1.5 and 2.5 nm AlN interlayers. (A) 60 s N_2 annealing. (B) 30 min. FG annealing. n-Ge and p-Ge capacitors are denoted by closed and open symbols, respectively. 1.5 nm and 2.5 nm AlN interlayer thicknesses are indicated by circles and squares, respectively. The N_2 anneal data point at 350 °C is from the as-deposited sample.

Figure 2.10 shows hysteresis at 80% C/C_{max} vs. anneal temperature for (A) 60 s N_2 and (B) 30 min. FG annealing. The values generally range from 300- 450 mV for n-Ge and 100- 200 mV for p-Ge. In contrast to the similar hysteresis values at 20% C/C_{max} for n- and p-Ge, n-Ge shows much larger hysteresis at 80% C/C_{max} due to greater trapping of carriers in slow states during accumulation. This trapping results in a large flatband shift for the reverse C-V characteristic. However, some carriers detrap during the reverse sweep time (~0.5 s for 50 bias points and measurement time of 10 ms/point). This effectively results in a time-dependent flatband shift that causes C-V hysteresis to decrease during the reverse sweep. By 20% C/C_{max}, most electrons have detrapped, therefore, 20% hysteresis is similar for n- and p-Ge. Hysteresis at 20% C/C_{max} is probably determined by bulk trapping in the AlN interlayer and hence less dependent on substrate type, while hysteresis at

80% C/C_{max} depends on carrier trapping near the conduction and valence band edges of n- and p-Ge, respectively. For n-Ge, hysteresis at 80% C/C_{max} shows clear minima at 500 °C and 450 °C for N_2 and FG annealing, respectively. In addition, n-Ge capacitors with 2.5 nm interlayer show significantly less hysteresis than capacitors with 1.5 nm interlayer. For p-Ge, hysteresis at 80% C/C_{max} is relatively independent of anneal temperature but does increase at 550 °C.

The difference between hysteresis at 80% and 20% C/C_{max} is shown in Figure 2.11. p-Ge samples exhibit constant hysteresis, so as expected, the difference is approximately zero. The difference for n-Ge decreases at high anneal temperature partly due to reduced hysteresis at 80% C/C_{max} but also because of increased hysteresis at 20% C/C_{max}. Thus while the difference in hysteresis decreases at 550 °C, the average hysteresis increases substantially.

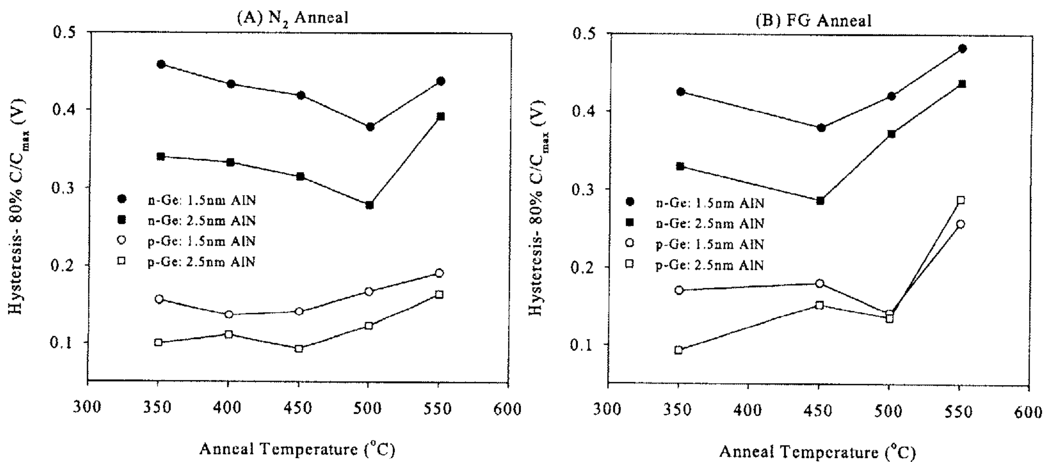


Figure 2.10: Hysteresis at 80% C/C_{max} vs. anneal temperature for n- and p-Ge capacitors with 1.5 and 2.5 nm AlN interlayers. (A) 60 s N_2 annealing. (B) 30 min. FG annealing. n-Ge and p-Ge capacitors are denoted by closed and open symbols, respectively. 1.5 nm and 2.5 nm AlN interlayer thicknesses are indicated by circles and squares, respectively. The N_2 anneal data point at 350 °C is from the as-deposited sample.

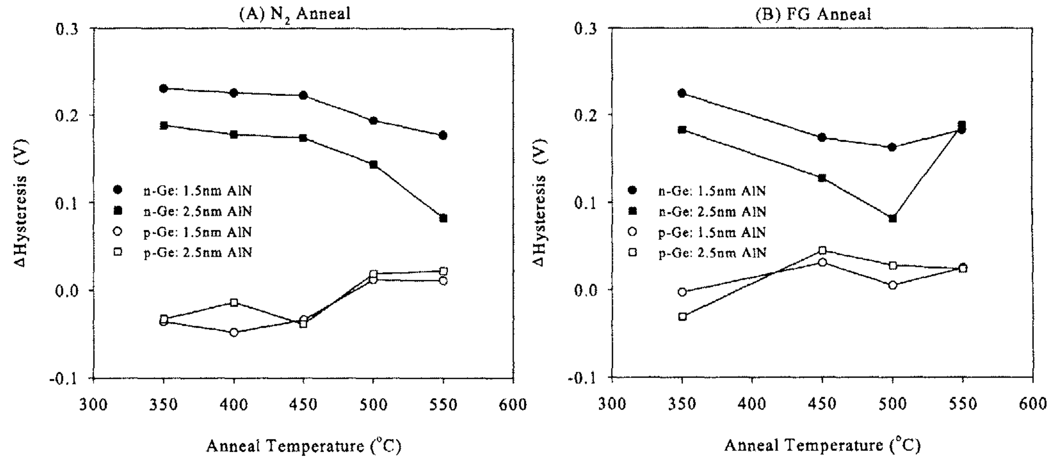
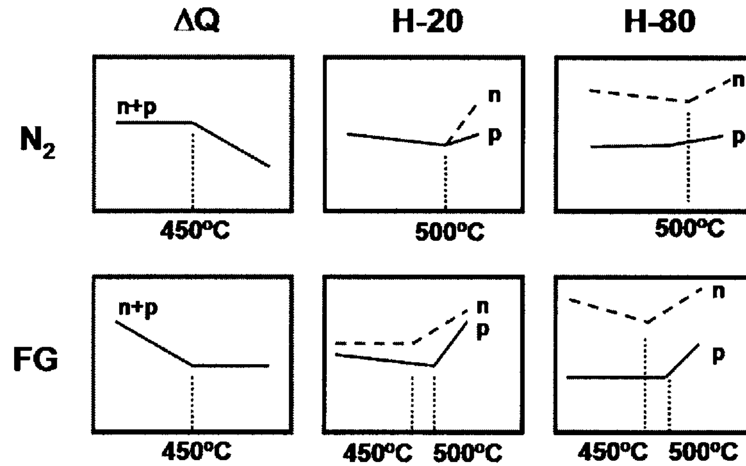


Figure 2.11: Difference in hysteresis at 80% and 20% C/C_{max} vs. anneal temperature for n- and p-Ge capacitors with 1.5 and 2.5 nm AlN interlayers. (A) 60 s N_2 annealing. (B) 30 min. FG annealing. n-Ge and p-Ge capacitors are denoted by closed and open symbols, respectively. 1.5 nm and 2.5 nm AlN interlayer thicknesses are indicated by circles and squares, respectively. The N_2 anneal data point at 350 °C is from the as-deposited sample.

Summary of AlN Thickness and PMA Optimization

N- and p-Ge capacitors were fabricated with Al_2O_3, Al_2O_3/AlN, and AlN gate dielectrics. Al_2O_3/AlN dielectric stacks showed superior characteristics compared to pure Al_2O_3 and AlN. The impact of post-metal annealing on WN/Al_2O_3/AlN/Ge capacitors with 1.5 nm and 2.5 nm AlN interlayers was investigated for 60 s N_2 and 30 min. FG annealing at 350-550 °C. The C-V characteristics were compared using several simple metrics: area difference between 50 khz and 1 Mhz curves (ΔQ), hysteresis at 20% C/C_{max} (H-20), and hysteresis at 80% C/C_{max} (H-80). Figure 2.12 summarizes important trends from the post-metal annealing study on n- and p-Ge capacitors with 1.5 and 2.5 nm interlayers. Each column shows the results for a particular metric while row 1 and row 2 summarize the results for N_2 and FG annealing, respectively. The third row summarizes the impact of AlN thickness on the given metric.



AlN Interlayer Thickness Effect:

- Similar in N_2
- 2.5nm IL shows lower ΔQ in FG

- 2.5nm IL shows lower H-20

- 2.5nm IL shows lower H-80, esp. for n-Ge

Figure 2.12: Summary of important trends from PMA study on n- and p-Ge capacitors with 1.5 and 2.5 nm AlN interlayers. Metrics are shown in each column while row 1 and 2 summarize the results for N_2 and FG annealing, respectively. The impact of AlN interlayer (IL) thickness on the given metric is shown in the third row.

By examining the temperature dependence of these three metrics, it is clear that n- and p-Ge capacitors are both stable to 500 °C for short anneal times (60 s). At longer anneal times (30 min.), or higher temperature (550 °C), n-Ge C-V characteristics start to degrade more severely than p-Ge. For all of the data, the observed trends correlate with thermal budget rather than anneal ambient. It does not appear that hydrogen passivation plays the same role at germanium-AlN interfaces that it does for Si-SiO_2 interfaces, possibly due to lower Ge-H bond strength and the position of hydrogen energy levels in germanium [58]. Hysteresis at 20% and 80% C/C_{max} also shows an important trend. While hysteresis at 20% C/C_{max} is similar for n- and p-Ge, hysteresis at 80% C/C_{max} is much higher for n-Ge indicating greater carrier trapping. Less trapping occurs in capacitors with 2.5 nm interlay-

ers and in general, these capacitors outperform those with 1.5 nm interlayers. In this gate stack, the thicker AlN interlayer is probably more effective at reducing or stabilizing interfacial GeO_x. For the process space explored in this work, 2.5 nm AlN interlayers annealed at 500 °C in N_2 or 450 °C in FG produced the best C-V characteristics (see Figure 2.13). In the next section, interface state characterization is performed on 2.5 nm AlN interlayer capacitors annealed at 450 °C in FG.

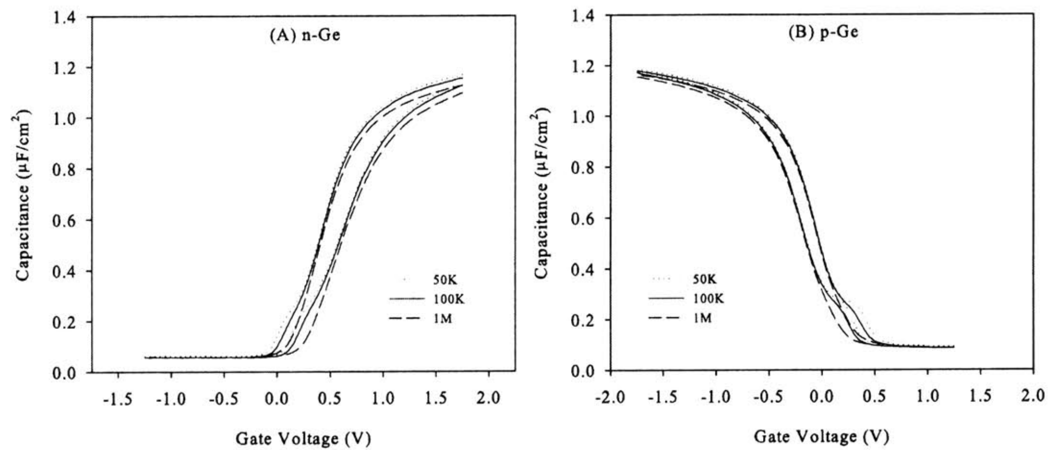


Figure 2.13: C-V characteristics for WN/3.5nm Al_2O_3/2.5 nm AlN/Ge capacitors annealed at 450 °C for 30 min. in FG.

2.5.3 Interface State Characterization of $WN/Al_2O_3/AlN/Ge$ Capacitors

Common capacitor-based techniques for extracting D_{it} include the conductance, quasistatic, and Gray-Brown methods [59]. MOSFET-based techniques include charge pumping [59] and V_t temperature dependence [79]. Challenges in measuring interface state density include: precise determination of D_{it} distribution (due to uncertainty in surface potential), measurement of D_{it} near the band edges, and limitations imposed by severely distorted C-V characteristics. The conductance and charge pumping methods rely on direct measurement of dynamic charge exchange with the interface states. These techniques are not affected by C-V distortion but do require low minority carrier generation in the depletion regime (conductance method) and low gate leakage (conductance and charge pumping methods). For charge pumping, band edge states are difficult to detect and without the use of more complex procedures this technique yields an average D_{it} value rather than the distribution [59]. The conductance method is also inaccurate near the band edges and determination of the surface potential, and hence D_{it} distribution, is complicated by the presence of interface states. In contrast to the conductance and charge pumping methods, the quasistatic technique utilizes both low-frequency (quasistatic) and high-frequency C-V characteristics. In principle, this technique allows the D_{it} distribution to determined across the bandgap; however, interfaces with a high density of states may exhibit severe C-V distortion making it difficult to obtain true quasistatic and high frequency C-V characteristics [59]. Temperature-based techniques, such as the Gray-Brown method (temperature dependence of V_{FB}) and MOSFET V_t temperature dependence, offer several advantages over the techniques discussed thus far. First, flatband and threshold voltage shifts are easily measured. Second, for both the flatband and threshold voltage, the corresponding surface potential is known from basic theory which allows the D_{it} distribution to be determined. And third, temperature-based techniques are effective at measuring D_{it} near the band

edges. The Gray-Brown and low temperature MOSFET V_t methods also have important drawbacks that must be considered when using these techniques. The primary disadvantage of the Gray-Brown technique is that high measurement frequencies are required to ensure that the flatband shift is only due to the temperature dependence of the Fermi level and not trap freeze out at low temperature [73]. Additional flatband shift due to decreased trap response results in an overestimation of D_{it} [73]. The measurement frequency required to ensure true high-frequency C-V characteristics (i.e. no contribution from interface states) is sample specific; therefore, this technique is best suited for qualitative sample comparison [73]. To the best knowledge of the author, the accuracy of the low temperature MOSFET V_t method has not been studied in detail. This method relies heavily on the definitions used for threshold voltage and inversion, as well as the model used to determine the ideal V_t shift (i.e. without interface states). It assumes that any additional observed V_t shift is due to interface states.

In this work, interface state characterization was performed using the conductance, Gray-Brown, and MOSFET V_t (discussed in Chapter 4) methods. The conductance method allows rapid determination of midgap D_{it} while the temperature-based techniques measure near-band-edge D_{it}. This section discusses the characterization of WN/Al_2O_3/AlN capacitors using the conductance and Gray-Brown methods.

Interface state characterization was performed on n- and p-Ge capacitors with 2.5 nm AlN interlayer. The post-metal anneal condition for these samples was 450 °C for 30 min. in FG. The conductance method is accurate from flatband to weak inversion [59], so n-Ge and p-Ge were used to extract D_{it} in the lower and upper halves of the bandgap, respectively. The surface potential, ϕ_s, was determined by integrating same-device quasistatic C-V characteristics according to the following relation [59]:

$$\phi_s = \int_{V_{G1}}^{V_{G2}} \left(1 - \frac{C_{lf}}{C_{ox}}\right) dV_G + \Delta \tag{2.1}$$

where C_{lf} is the quasistatic capacitance and C_{ox} is the peak oxide capacitance. Integration was carried out from strong inversion to strong accumulation yielding a total change in surface potential of 0.70 V. This approximately matches the bandgap of germanium (0.66 eV) indicating that the method is valid [59]. In strong inversion (accumulation), the Fermi level for an n-Ge (p-Ge) capacitor is near the valence band edge, so the valence band edge is taken as the surface potential reference and Δ is assumed to be zero in equation 2.1. Figure 2.14 shows the resulting D_{it} distribution referenced to the intrinsic Fermi level. Midgap D_{it} is approximately 2×10^{12} cm^{-2} eV^{-1} and is slightly higher in the upper half of the bandgap. For comparison, midgap D_{it} of Si-SiO_2 interfaces is typically on the order of 10^{10} cm^{-2} eV^{-1}.

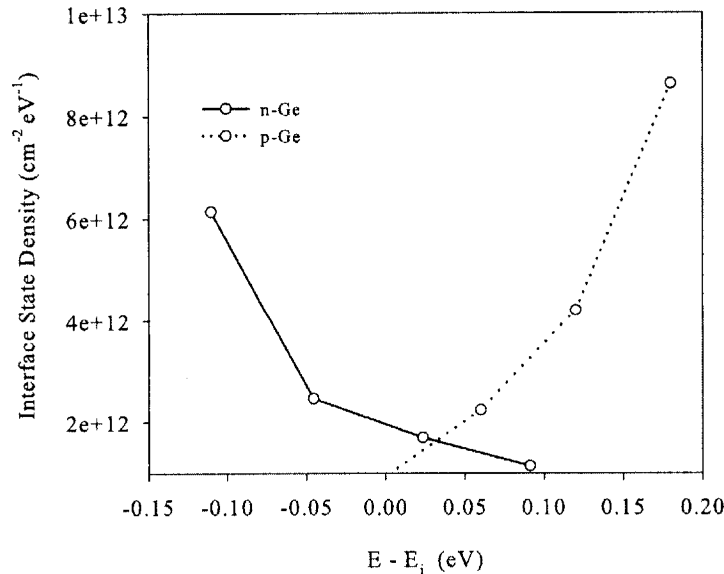


Figure 2.14: Interface state density (D_{it}) determined using the conductance method for WN/ 3.5 nm Al_2O_3/ 2.5 nm AlN/Ge gate capacitors that received a 30 min. 450 °C FG anneal. This method is accurate from flatband to weak inversion, so n-Ge and p-Ge were used to extract D_{it} in the lower and upper halves of the bandgap, respectively. The energy position in the bandgap is referenced to the intrinsic Fermi level.

In addition to the conductance method, the Gray-Brown method was also used in order to extract D_{it} closer to the band edges [60]. In this method, the temperature dependence of the Fermi level is used to sweep the Fermi level position within the upper and lower halves of the bandgap in n-Ge and p-Ge, respectively. The corresponding change in flat-band voltage is directly related to the interface state density within the energy range swept out by the Fermi level. At flatband, the surface potential is zero so the region of the band-gap swept out by the Fermi level position is easily calculated from basic theory thus allowing the D_{it} distribution to be determined. This technique assumes that true high-frequency curves (i.e. no contribution from interface states) are measured at each temperature [73]. This is most likely to be true at lower measurement temperatures due to trap freeze out [73]. Figure 2.15 shows forward sweep 1 MHz C-V characteristics as a function of temperature for n- and p-Ge. The flatband capacitance shown on each plot was determined by simulating an ideal germanium capacitor with similar substrate doping and CET. The flatband voltage is simply the voltage at which the capacitance equals the flatband capacitance. The n-Ge capacitor shows a larger flatband shift, qualitatively indicating a higher density of states in the upper half of the bandgap. Making the assumptions discussed above, the extracted D_{it} distribution is shown in Figure 2.16. D_{it} extracted from the conductance method has also been included for reference. This plot shows an asymmetric interface state distribution that rises more quickly near the conduction band edge. At $E- E_i = 0.3$ eV, D_{it} is approximately $3.5x10^{13}$ cm^{-2} eV^{-1}. The D_{it} values extracted using the two techniques appear to be consistent.

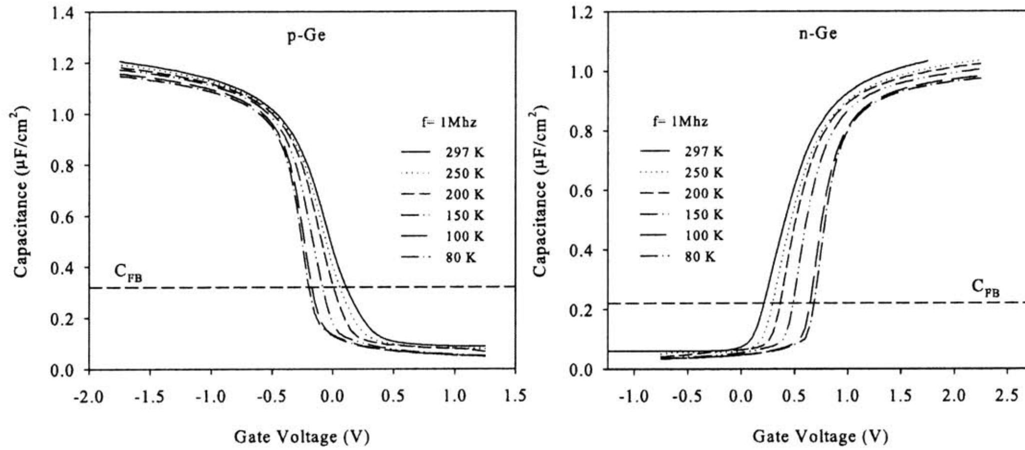


Figure 2.15: Forward sweep 1 MHz C-V characteristics as a function of temperature for WN/ 3.5 nm Al_2O_3/ 2.5 nm AlN gate stack on p- and n-Ge. The n-Ge capacitor shows a larger flatband shift indicating a higher density of states in the upper half of the bandgap.

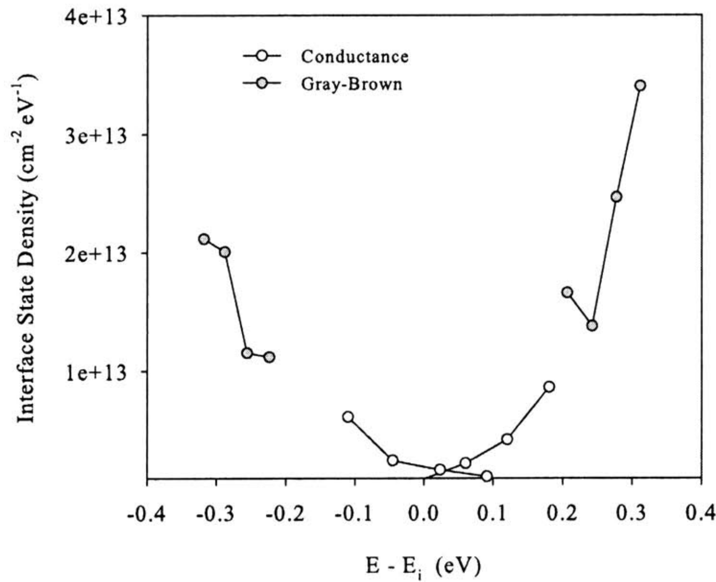


Figure 2.16: D_{it} distribution for WN/ 3.5 nm Al_2O_3/ 2.5 nm AlN/Ge capacitors extracted using conductance and Gray-Brown methods. The energy position in the bandgap is referenced to the intrinsic Fermi level.

In addition to extracting D_{it} from flatband shift, simple examination of the low temperature C-V characteristics also provides insight into the germanium-AlN interface. Figure 2.17 shows n-Ge C-V characteristics at 297, 250, 200, 150, 100, and 80 K. As discussed previously, and as shown at 297 K, hysteresis decreases during the reverse voltage sweep. The peak capacitance also decreases at high frequency and/or low-temperature which points to a large density of "trapped" electrons in accumulation. At high frequency, the trap time constant, τ_{it}, is long relative to the small-signal period and the trapped carriers cannot respond. At low temperature the trap emission time, and consequently τ_{it}, increase [73], thus producing the same effect. At 297 K and 10 kHz, n- and p-Ge have similar peak capacitance; however, at high frequency or low temperature, the "trapped" electrons do not contribute to small-signal AC capacitance. This frequency dispersion is not consistent with other possible explanations such as series resistance or capacitor perimeter effects. In addition to reduced peak capacitance, the hysteresis of n-Ge capacitors also changes significantly from 297 to 80 K. At low temperature, the emission time of trapped carriers becomes long resulting in constant hysteresis over the reverse sweep. For comparison, the low temperature C-V characteristics of p-Ge capacitors are shown in Figure 2.18. As expected, midgap interface states freeze out at low temperature producing more-ideal C-V characteristics [73]. A direct comparison of n- and p-Ge C-V characteristics at 297, 250, and 200 K is shown in Figure 2.19. From this data, it is very clear that carrier trapping severely impacts electrons at the germanium-AlN interface. The percentage of trapped electrons can be estimated by comparing the integrated charge from the 50 kHz and 1 MHz curves at 297 K. This estimate is most accurate at high inversion charge density. At low inversion charge density, small differences in integrated charge caused by factors not related to trapping may result in an inaccurate estimate. Figure 2.20 shows the integrated charge of both curves (secondary axis) along with the percentage of trapped charge (pri-

mary axis). For electron accumulation charge densities approaching $1x10^{13}$ cm^{-2}, approximately 15% of the carriers appear to be trapped. In contrast, p-Ge does not show evidence of significant charge trapping.

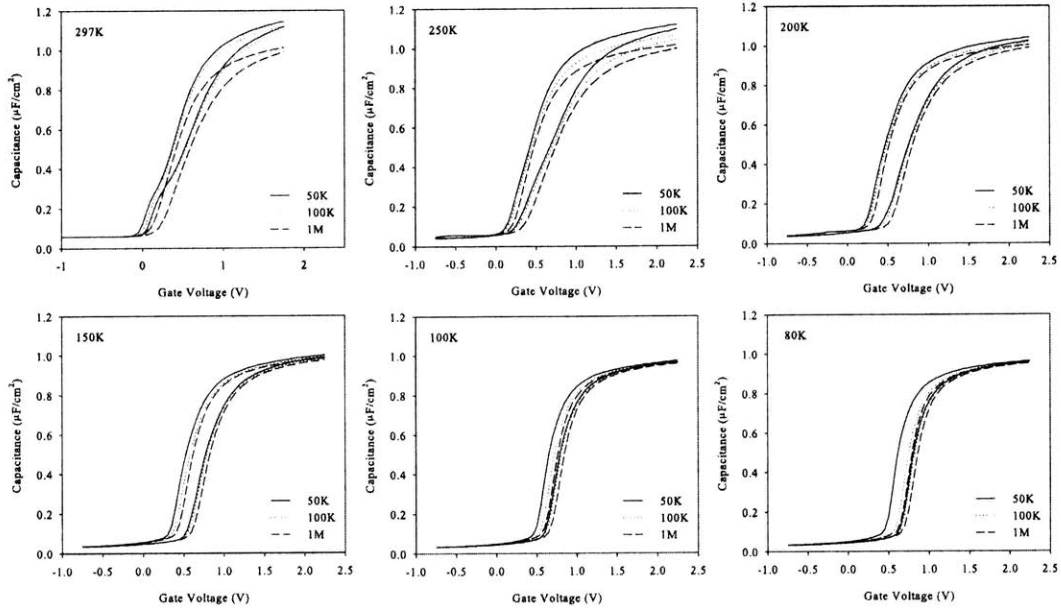


Figure 2.17: C-V characteristics of WN/ 3.5 nm Al_2O_3/ 2.5 nm AlN/n-Ge capacitors at 297, 250, 200, 150, 100, and 80 K. Forward and reverse sweeps are shown at frequencies of 50 kHz, 100 kHz, and 1 MHz

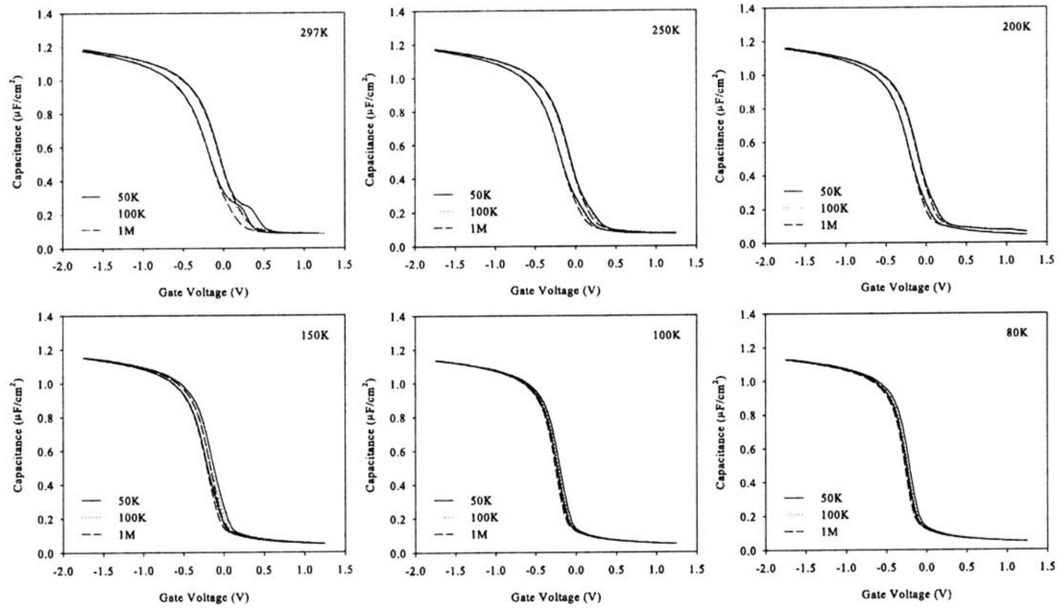


Figure 2.18: C-V characteristics of WN/ 3.5 nm Al_2O_3/ 2.5 nm AlN/p-Ge capacitors at 297, 250, 200, 150, 100, and 80 K. Forward and reverse sweeps are shown at frequencies of 50 kHz, 100 kHz, and 1 MHz.

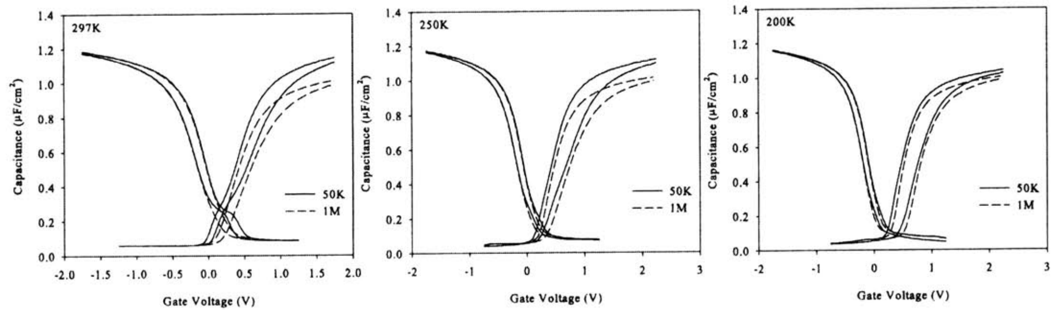


Figure 2.19: Direct comparison of low temperature C-V characteristics of WN/ 3.5 nm Al_2O_3/ 2.5 nm AlN gate stack on n- and p-Ge at 297, 250, and 200 K. n-Ge shows a significant reduction in peak capacitance at high frequency and/or low temperature due to trapping.

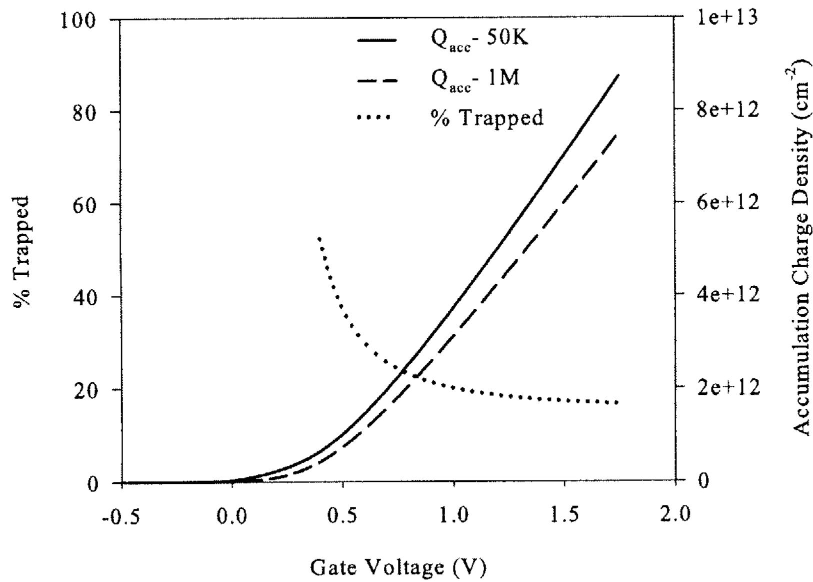


Figure 2.20: Integrated charge from 297 K 50 kHz and 1 MHz C-V characteristics of WN/ 3.5 nm Al_2O_3/ 2.5 nm AlN/n-Ge capacitors. The charge difference is attributed to carrier trapping. The percentage of trapped charge is plotted on the primary axis while integrated charge is plotted on the secondary axis.

To further investigate the reduced small-signal capacitance in n-Ge, quasistatic C-V measurements were performed to compare the peak DC capacitance of n- and p-Ge capacitors. Figure 2.21 shows quasistatic and high-frequency data for n- and p-Ge. The quasistatic and high-frequency data show better agreement for hole accumulation than for electron accumulation. Furthermore, the peak DC electron capacitance is always higher than the peak DC hole capacitance suggesting that the reduction in n-Ge small-signal capacitance is significant and that electron trapping is occurring at the interface.

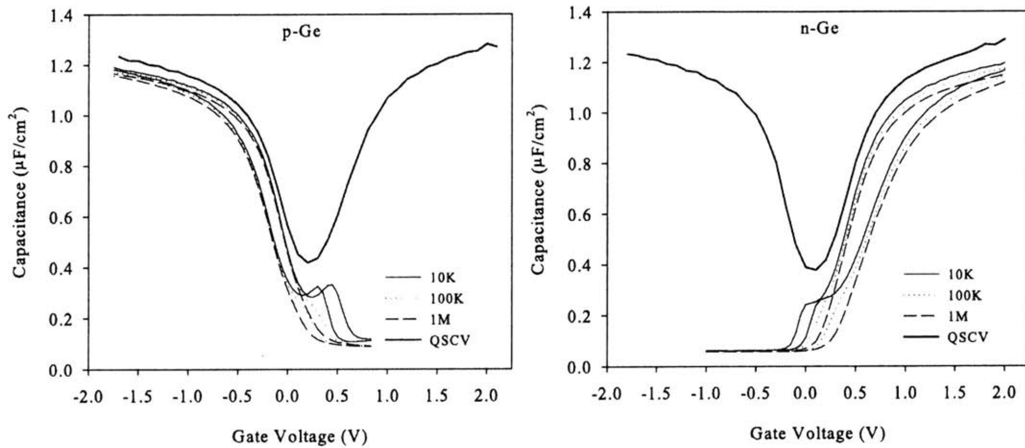


Figure 2.21: Quasistatic and high-frequency C-V data for WN/ 3.5 nm Al_2O_3/ 2.5 nm AlN gate stack on n- and p-Ge.

2.6 Summary

AlN is one of only a few dielectric layers that have produced functional Ge n-MOSFETs; however, AlN interlayers have yet to be studied in detail. In this study, the effects of AlN thickness and PMA conditions on Al_2O_3/AlN dielectric stacks were investigated. Interface state characterization was performed on Ge capacitors fabricated using an optimized gate stack and post-metal anneal.

Optimal C-V characteristics were achieved for an AlN interlayer thickness of 2.5 nm and either a 500 °C 60 s N_2 or 450 °C 30 min. FG anneal. As shown in Figure 2.13, these capacitors are still far from ideal with hysteresis values ranging from 100- 300 mV, mid-gap distortion for p-Ge, and evidence of electron trapping in n-Ge. Gate stacks annealed in N_2 were stable up to 500 °C with noticeable degradation observed at 550 °C. Interface state density was extracted for capacitors with 2.5 nm AlN interlayers using both the conductance and Gray-Brown methods. D_{it} was approximately $2x10^{12}$ cm^{-2} eV^{-1} near midgap and increased to $2x10^{13}$ and $3.5x10^{13}$ cm^{-2} eV^{-1} near the valence and conduction band

edges, respectively. Low temperature C-V measurements also revealed a decrease in peak capacitance at low temperature and/or high measurement frequency for n-Ge capacitors. This behavior was attributed to electron trapping at the interface, and based on the observed frequency dispersion, the percentage of trapped carriers at high accumulation charge density was estimated to be approximately 15%.

Despite the non-idealities of the Al_2O_3/AlN dielectric stack, its properties are sufficient for fabricating functional Ge MOSFETs. Furthermore, additional optimization of this gate stack may be possible. The process space investigated in this work was limited to RCA-based cleaning followed by ALD deposition and post metal annealing in either N_2 for 60 s or 8:1 N_2:H_2 for 30 min. Each of these steps could be investigated in more detail. Other surface preparation techniques and more complex interlayers (e.g. AlON, HfON, HfAlON) could certainly be explored. As has been observed with silicon [75], interlayers with reduced nitrogen content may improve carrier mobility. Recent evidence also suggests that alternative surface preparations may be superior to the RCA-based cleans used in this work. Surface preparation and interlayer formation are dependent processes that must be co-optimized. It was recently discovered that dielectric stacks deposited on as-received wafers from the supplier (Umicore) exhibit better electrical properties than on RCA-cleaned wafers. Furthermore, for as-received wafers, pure Al_2O_3 appears to perform better than Al_2O_3/AlN stacks. Since the supplier's surface preparation technique is proprietary, it is difficult to speculate why this may be the case; however, it seems likely that pre-existing germanium oxide is acting as an interlayer. The thermal stability of this apparent interlayer is unknown. Despite these new results, AlN interlayers are still a promising approach for improving the germanium-dielectric interface. In the next chapter, the electrical characteristics of surface-channel Ge MOSFETs with AlN interlayers are discussed.

Chapter 3

Surface-Channel Ge MOSFETs

3.1 Introduction

To evaluate device performance, Ge MOSFETs were fabricated with the optimized WN/ Al_2O_3/AlN gate stack described in Chapter 2. n-FETs were fabricated on both (100) and (111) bulk germanium substrates to examine the impact of substrate orientation on electron mobility. Ge MOSFETs with Hf_3N_4 and GeON interlayers were also investigated through collaborations with Harvard University [41], the University of Texas at Austin [33], [61], and the National Center for Scientific Research (NCSR) Demokritos in Athens, Greece [62].

Section 3.2 provides detailed electrical characteristics for devices with AlN interlayers. Sections 3.3, 3.4, and 3.5 describe device results for Hf_3N_4, RTP GeON, and MBD GeON interlayers, respectively. In addition to bulk germanium, epitaxial strained germanium p-MOSFETs were also fabricated with RTP GeON interlayers and are described in Section 3.4. Lastly, Section 3.6 summarizes the carrier mobility for Ge MOSFETs fabricated at MIT with nitride-based interlayers.

3.2 AlN Interlayer MOSFETs

3.2.1 Fabrication Process

n- and p-MOSFETs were fabricated using a standard process that is summarized in Table 3.1. A detailed process description may be found in Appendix A. Annular devices were fabricated on bulk (100) Ge substrates (Ga: 0.12-0.17 Ω-cm, Sb: 0.13-0.16 Ω-cm). n-FETs were also fabricated on bulk (111) Ge substrates (Ga: 0.084-0.130 Ω-cm). The pre-gate stack cleaning procedure consisted of three steps: (1) 10 min. 6:1 DI:HCl followed by DI rinse, (2) 2 min. 5:1:1 DI: NH_4OH: H_2O_2 followed by DI rinse, and (3) 10 min. 6:1 DI:HCl followed by DI rinse. The first step removes native oxide, the second step etches germanium to provide a fresh surface prior to gate dielectric deposition, and the third step removes chemical oxide and chlorine-terminates the surface to reduce subsequent GeO_x formation [24]. Chlorine termination is not perfectly stable [24] so some oxide forms on the surface prior to gate stack deposition. The *in-situ* ALD gate stack consisted of a 2.5 nm AlN interlayer, 3.5 nm Al_2O_3 capping layer, and 40 nm WN gate electrode. The gate electrode was etched using CF_4-based reactive ion etching. Next S/D implantation was performed (P: 5×10^{14} cm^{-2}, 25 keV; BF_2: 1×10^{15} cm^{-2}, 40 keV), followed by PECVD oxide deposition, S/D activation, and contact photolithography and etching. Ti/Al was used for the metallization. S/D anneal conditions for p- and n-FETs were 450°C 60 s N_2 and 500°C 60 s N_2, respectively. The S/D anneal also served as the post-metallization anneal (PMA) for the gate stack.

Step	Process	Description
1	Pre-gate stack clean	Modified RCA clean: dilute HCl + SC1 (RT) + dilute HCl (DI rinse after each step)
2	ALD gate stack deposition	40 nm WN/3.5 nm Al_2O_3/2.5 nm AlN
3	Gate electrode patterning	CF_4 RIE
4	S/D ion implantation	PMOS: BF_2, $1x10^{15}$ cm^{-2}, 40 keV NMOS: P, $5x10^{14}$ cm^{-2}, 25 keV
5	PECVD SiO_2 deposition	200 nm
6	S/D activation	PMOS: 450 °C, N_2, 60 s NMOS: 500 °C, N_2, 60 s
7	Contact hole patterning	3:1 DI: BOE followed by 4:1 DI:HCl to insure high-k dielectric removal
8	Metal deposition	Frontside: 50nm Ti/ 400 nm Al Backside: 50nm Ti/ 2 μm Al
9	Metal patterning	Al: Al etchant Ti: dilute BOE

Table 3.1: Fabrication process summary for AlN interlayer Ge MOSFETs. Detailed process description may be found in Appendix A.

3.2.2 Device Characterization and Results

(100) p- and n-FETs

Typical as-measured p- and n-FET I_S-V_G and I_S-V_D characteristics are shown in Figures 3.1 and 3.2. Source current is measured to eliminate the effect of drain junction leakage to the substrate.

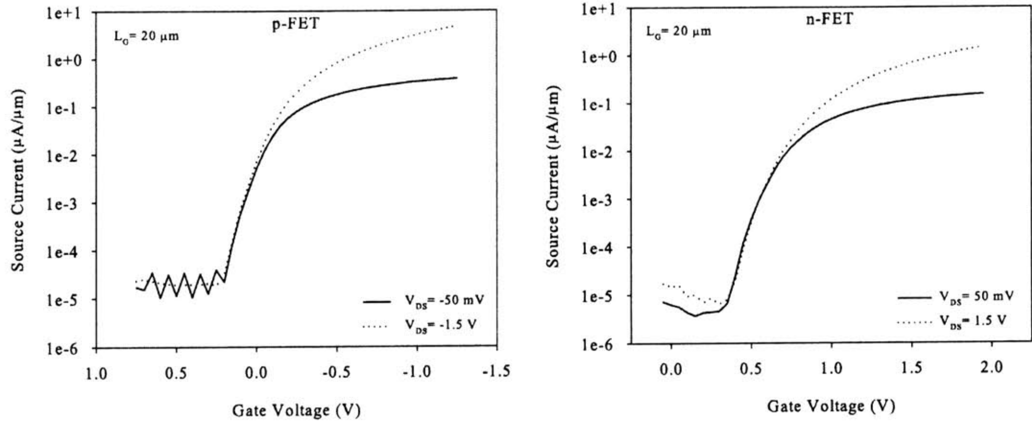


Figure 3.1: Typical as-measured I_S-V_G characteristics for Ge p- and n-MOSFETs with 40 nm WN/3.5 nm Al_2O_3/2.5 nm AlN gate stack. p-FETs exhibited a 95 mV/decade subthreshold swing and V_t of –0.05 V. n-FETs exhibited a V_t of +0.7 V, gradual roll-off of the I_S-V_G characteristic in the subthreshold regime, and increased device-to-device variability.

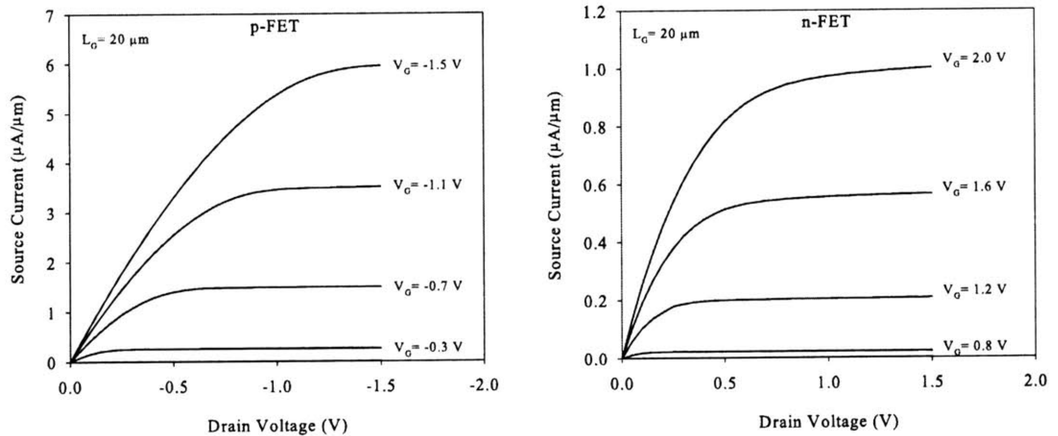


Figure 3.2: Typical as-measured I_S-V_D characteristics for Ge p- and n-MOSFETs with 40 nm WN/3.5 nm Al_2O_3/2.5 nm AlN gate stack.

The Ge p-FETs exhibited a 95 mV/decade subthreshold swing and –0.05 V threshold voltage (V_t). Device characteristics (V_t, source current, carrier mobility) were uniform across the wafer. The n-FETs exhibited a V_t of +0.7 V, gradual roll-off of the I_S-V_G characteris-

tics in the subthreshold regime, and increased device-to-device variability. The work function of WN is 4.6 eV [63], which approximately aligns with the germanium valence band edge. The ideal threshold voltage (i.e. assuming zero fixed and interface state charge) for these devices is approximately +0.05 V for the p-FET and +0.5 V for the n-FET. The measured p-FET V_t is higher by |0.1 V| while the n-FET V_t is higher by |0.2 V|. These shifts are due to both fixed charge and interface states in the upper and lower halves of the bandgap for n- and p-FETs, respectively. The n-FET V_t shift combined with I_S-V_G subthreshold distortion suggests a higher interface state density in the upper half of the bandgap. Figure 3.3 shows the inversion-side split C-V characteristics (C_{GSD}) at low frequency (10 kHz). The forward sweep is from depletion to inversion, and vice versa for the reverse sweep. The peak inversion capacitance corresponds to a capacitance equivalent thickness (CET) of approximately 3 nm and is similar for both the n- and p-FET. Not surprisingly, the n- and p-FET inversion-side split C-V characteristics are similar to the n- and p-Ge MOSCAP results in Chapter 2. The p-FET C_{GSD} shows low hysteresis and slight distortion at midgap due to interface states. The n-FET C_{GSD} shows large hysteresis, distortion near inversion, and slow detrapping on the reverse sweep. The effective carrier mobility for these devices was extracted from same-device I_S-V_G and C_{GSD} characteristics and is shown in Figure 3.4. Silicon universal hole mobility at similar substrate doping ($5x10^{16}$ cm^{-3}) is included for reference. Silicon universal mobility is typically defined in terms of vertical effective field, which is calculated using empirically determined multiplying factors for electron and hole inversion charge density (1/2 and 1/3, respectively). These factors have not been verified for germanium, so germanium carrier mobility is often plotted versus inversion charge density. As was done for the silicon universal reference curve in Figure 3.4, vertical effective field can easily be translated into inversion charge density for a given substrate doping.

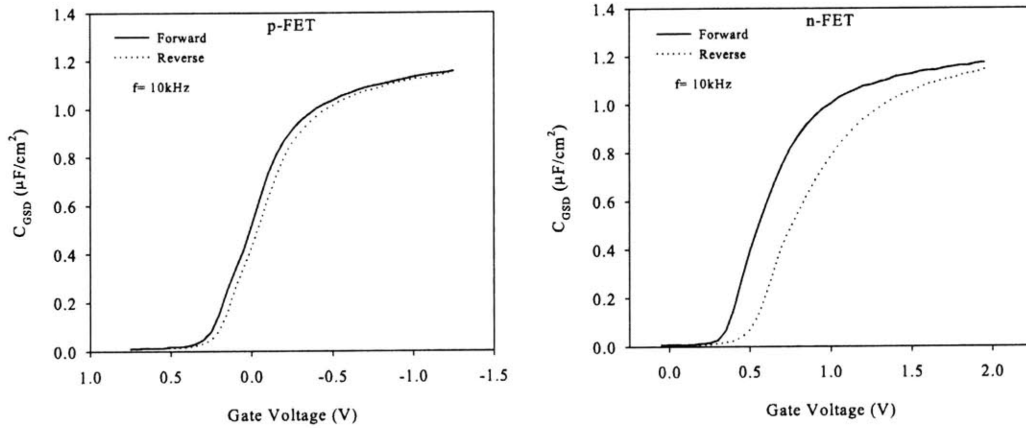


Figure 3.3: Typical as-measured inversion-side split C-V characteristics for Ge p- and n-MOSFETs with 40 nm WN/3.5 nm Al_2O_3/2.5 nm AlN gate stack. The peak inversion capacitance corresponds to a capacitance equivalent thickness (CET) of approximately 3 nm and is similar for both the n-FET and p-FET.

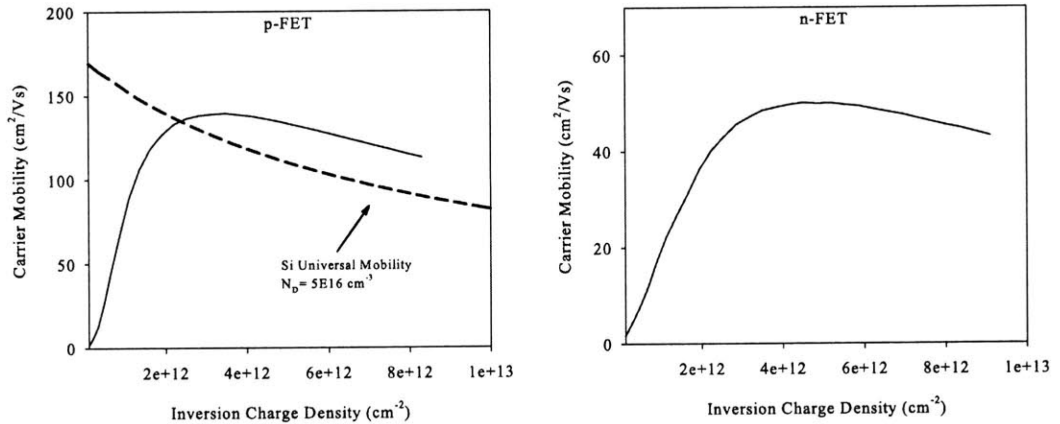


Figure 3.4: Effective carrier mobility for Ge p- and n-MOSFETs with 40 nm WN/3.5 nm Al_2O_3/2.5 nm AlN gate stack. p-FETs show slight enhancement compared to silicon universal while n-FETs show peak mobility of only 50 cm^2/Vs.

The Ge p-FETs show a peak mobility of 140 cm^2/Vs and slight enhancement over silicon universal hole mobility. Given the 4x difference in bulk hole mobility, larger enhancement is expected. The bulk mobility enhancement factor is not realized in inversion layer mobil-

ity due to the non-ideal germanium-dielectric interface. Nonetheless, this result is still impressive given the early stage of this work. Mobility enhancement of up to 40% is typically reported for surface-channel Ge MOSFETs with high-k gate dielectrics and no silicon interlayer. In contrast, Ge n-FETs show a disappointing peak mobility of 50 cm^2/Vs which is far below silicon universal electron mobility. The mobility peak is also pushed out to high inversion charge density due to coulomb scattering from charged interface states. The gradual roll-off of the I_S-V_G characteristics, early saturation behavior of the I_S-V_D characteristics, C-V distortion and hysteresis, and poor mobility all point toward problems with the germanium-dielectric interface that impact electrons more severely than holes. Chapter 4 investigates this topic in detail.

(111) n-FETs

Ge n-FETs were also simultaneously fabricated on (111) substrates to determine whether band structure was playing a significant role in the observed electron mobility. Figure 3.5 shows a comparison between the effective electron mobility for (100) and (111) Ge n-FETs. Because of high device-to-device variability, mobility from five devices is shown for each substrate orientation.

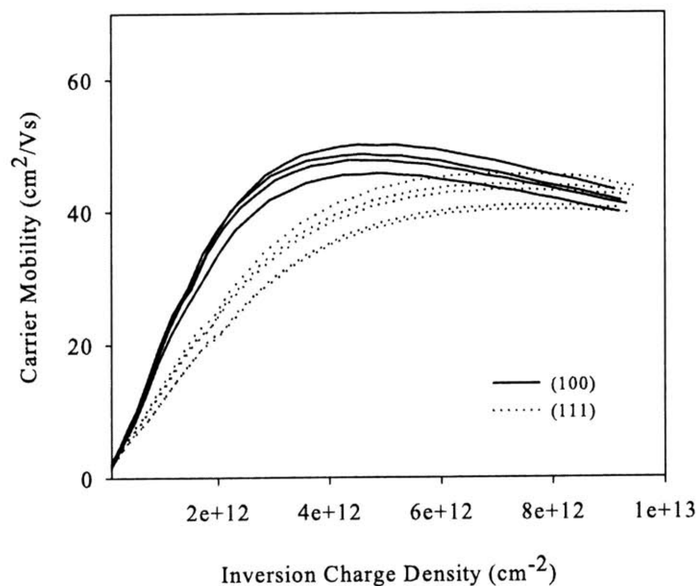


Figure 3.5: Comparison of effective electron mobility for (100) and (111) Ge n-MOSFETs with 40 nm WN/3.5 nm Al_2O_3/2.5 nm AlN gate stack. Mobility from five devices is shown for each substrate orientation.

Ge (111) n-FETs show slightly lower mobility than (100) devices and the peak occurs at higher inversion charge density. As with silicon, the (111) plane has a higher density of atoms, and thus a larger number of bonds that must be terminated, so it is not surprising that (111) devices show degraded mobility relative to (100). While band structure certainly plays an important role in electron transport in germanium, the observed mobility in these devices is clearly limited by the germanium-dielectric interface.

3.3 Hf_3N_4 Interlayer MOSFETs

Hf_3N_4 interlayers were explored through a collaboration with K. Kim and R. Gordon of Harvard University. Gate stack deposition and post-metal annealing were performed at Harvard, and device fabrication was completed at MIT. Device results from this collaboration are published in reference 62.

3.3.1 Fabrication Process

Annular Ge n- and p-MOSFETs were fabricated on bulk (100) Ge substrates (Ga: 0.2-0.4 Ω-cm, Sb: 0.025-0.04 Ω-cm). The substrates were cleaned in dilute HF (10%) for 5 min. and rinsed in DI water for 30 s. The *in-situ* ALD gate stack consisted of a 1.5 nm Hf_3N_4 interfacial layer, 2.5 nm $GdScO_3$ capping layer, and 40 nm WN gate electrode [62]. $GdScO_3$ has shown promise as a high-k dielectric on silicon and thus was used in this work [80]. After gate stack deposition, post-metal annealing was performed at 420°C for 90 s in 10:1 He:H_2 (10 torr). The gate electrode was then etched using CF_4-based reactive ion etching. Next S/D implantation was performed (P: 5×10^{14} cm^{-2}, 15 keV; BF_2: 1×10^{15} cm^{-2}, 24 keV), followed by PECVD oxide deposition, S/D activation, and contact photolithography and etching. Ti/Al was used for the metallization. S/D anneal conditions for n- and p-FETs were 500°C 60 s N_2 and 400°C 60 s N_2, respectively.

3.3.2 Device Characterization and Results

Typical as-measured p- and n-FET I_S-V_G characteristics are shown in Figure 3.6. The p-FETs exhibited a 114 mV/decade subthreshold swing and –0.65 V threshold voltage. The ideal p-FET threshold voltage is +0.0 V. The gradual I_S-V_G roll-off and high $|V_t|$ indicate a large density of states in the lower half of the bandgap. The n-FETs exhibited a V_t of +0.45 V and steeper subthreshold swing of 103 mV/decade. The ideal n-FET threshold voltage is approximately +0.5 V. The agreement between measured and ideal V_t is better than for $WN/Al_2O_3/AlN$ Ge n-FETs, suggesting lower D_{it} in the upper half of the bandgap for Hf_3N_4 interlayers.

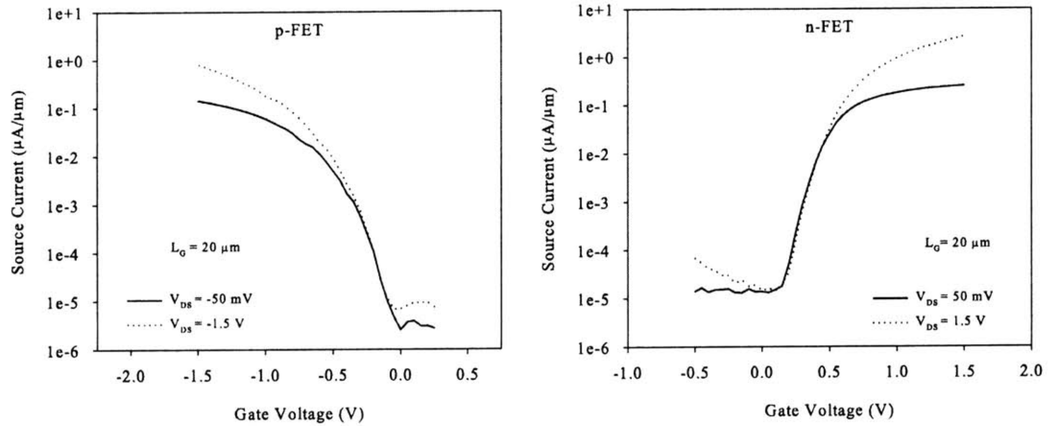


Figure 3.6: Typical as-measured I_S-V_G characteristics for Ge p- and n-MOSFETs with 40 nm WN/2.5 nm $GdScO_3$/1.5 nm Hf_3N_4 gate stack. p-FETs exhibited a 114 mV/decade subthreshold swing and –0.65 V threshold voltage (V_t). The gradual I_S-V_G roll-off and high V_t indicate a large density of states in the lower half of the bandgap. The n-FETs exhibited a V_t of +0.45 V and steeper subthreshold swing of 103 mV/decade.

Figure 3.7 shows inversion-side split C-V characteristics (C_{GSD}) at low frequency (10 kHz). The peak inversion capacitance corresponds to a capacitance equivalent thickness (CET) of approximately 1.5 nm and is similar for both the n-FET and p-FET. As expected from the I_S-V_G characteristics, the n-FET C_{GSD} characteristics shows less distortion and hysteresis. The effective carrier mobility for these devices is shown in Figure 3.8. Peak electron and hole mobilities are 90 and 17 cm^2/Vs, respectively. While the electron mobility is promising, the hole mobility for Hf_3N_4 is significantly lower than for alternative interlayers such as GeON and AlN. It is certainly possible that gate stacks for Ge n- and p-FETs will need to be optimized separately.

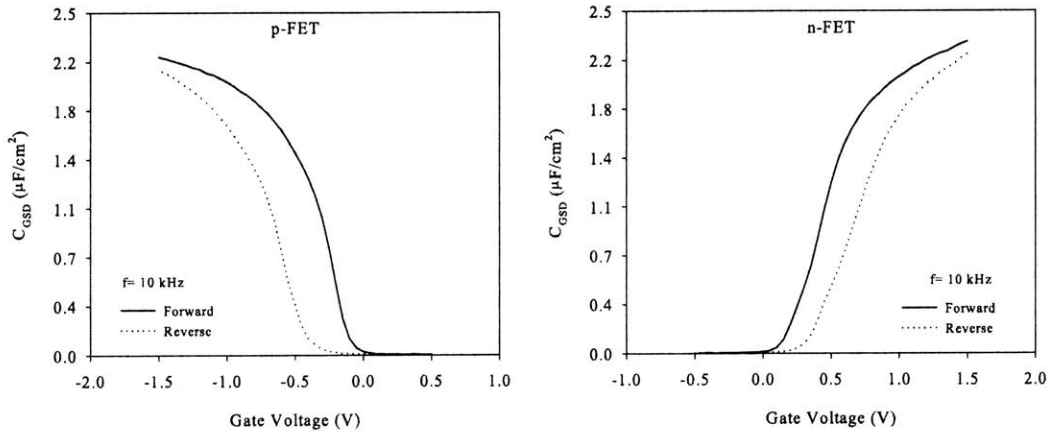


Figure 3.7: Typical as-measured split C-V characteristics at 10 kHz for Ge p- and n-MOSFETs with 40 nm WN/2.5 nm $GdScO_3$/1.5 nm Hf_3N_4 gate stack. The peak inversion capacitance corresponds to a capacitance equivalent thickness (CET) of approximately 1.5 nm and is similar for both the n-FET and p-FET.

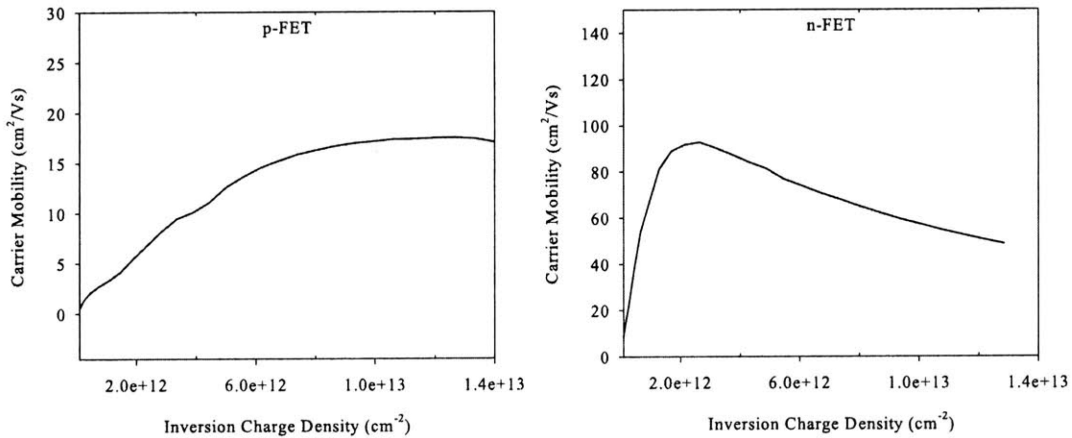


Figure 3.8: Effective carrier mobility for Ge p- and n-MOSFETs with 40 nm WN/2.5 nm $GdScO_3$/1.5 nm Hf_3N_4 gate stack. n-FETs show promising peak electron mobility of 90 cm^2/Vs while p-FETs show severely degraded hole mobility.

3.4 RTP GeON Interlayer MOSFETs

Gate stacks with RTP GeON interlayers were explored through a collaboration with D.L. Kwong at the University of Texas at Austin. TaN/HfO_2/GeON gate stack deposition was performed at the University of Texas at Austin, and device fabrication was completed at MIT. In addition to bulk germanium substrates, p-FETs were also fabricated on epitaxial strained germanium. GeON interlayer p-FETs showed reasonable performance; however, n-FETs showed very low drive current (0.01 μA/μm) and are not discussed further in this section. Device results from this collaboration are published in reference 61.

3.4.1 Strained Germanium Heterostructure

Figure 3.9 describes the Ge/SiGe heterostructure and Figure 3.10a shows an XTEM micrograph of the structure. The strained Ge channel is approximately 55 nm thick. This layer was intentionally grown thicker than its critical thickness (h_c~ 12 nm) to withstand pre-gate cleaning steps. While the compressive strain is partially relaxed by misfit dislocations at the heterointerface, the strained Ge maintains approximately 0.8% elastic strain after device processing (the lattice mismatch between Ge and $Si_{0.3}Ge_{0.7}$ is 1.3%). Device fabrication on strained germanium virtual substrates was performed at reduced temperature compared to bulk germanium substrates to prevent strain relaxation and interdiffusion.

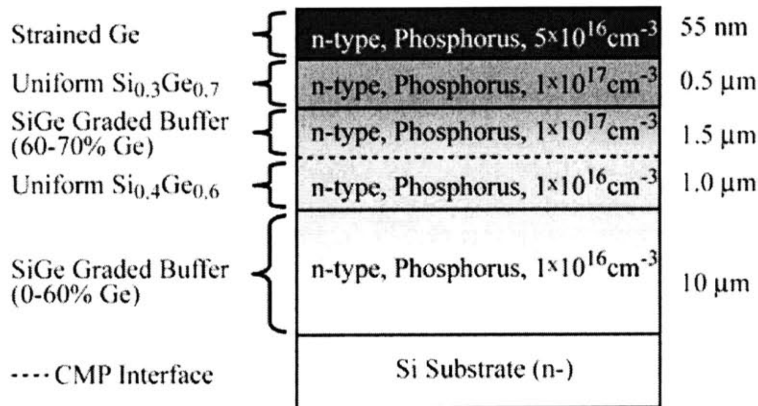


Figure 3.9: Schematic of Ge/SiGe heterostructure grown using UHVCVD. The strained germanium layer is approximately 55 nm thick. All SiGe layers are relaxed. After growing the 0-60% SiGe graded buffer, the wafers were polished using CMP to remove the cross-hatch that arises during growth (from [61]).

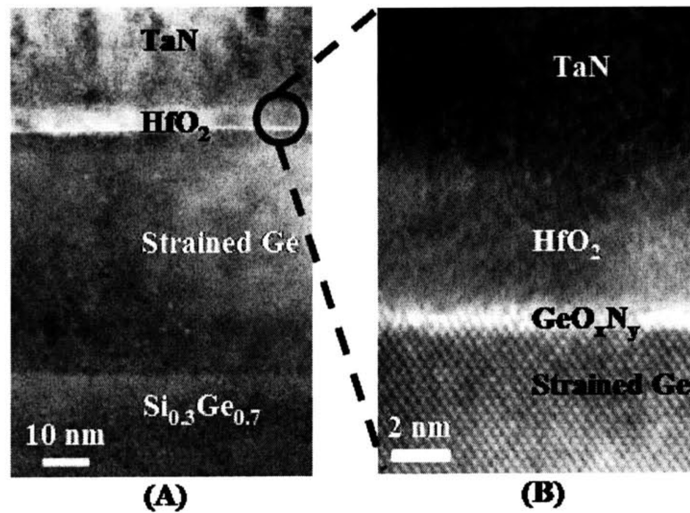


Figure 3.10: (A) XTEM of strained Ge after processing. The strain present in the film may be estimated from the dislocation density as seen in XTEM micrographs [64]. Applying this technique yields a strain of 0.8% in the germanium channel layer. (B) XTEM of gate stack on strained Ge after processing. The HfO_2 layer is approximately 5 nm thick. The germanium oxynitride interfacial layer is clearly visible (from [61]).

3.4.2 Fabrication Process

Long-channel annular p-MOSFETs were fabricated on bulk (100) Ge substrates (Sb: 0.05-0.3 Ω-cm) and epitaxial strained Ge on $Si_{0.3}Ge_{0.7}$ virtual substrates. The substrates were cleaned using cyclic 50:1 DI:HF [33]. The GeON interlayer was then formed by rapid thermal annealing in ammonia (NH_3) at 600 °C for 2 min. for bulk Ge and 500 °C for 2 min. for strained Ge. This process forms a thin (~0.7 nm) germanium oxynitride layer [33]. Next, 5 nm of HfO_2 was deposited by MOCVD followed by 140 nm of reactively sputtered TaN as the gate electrode. Figure 3.10b shows an XTEM micrograph of the gate stack. The gate electrode was etched using CF_4-based reactive ion etching (RIE). Following gate patterning, HfO_2 was removed from the S/D regions using CF_4 RIE. Next S/D implantation was performed (BF_2: 1×10^{16} cm^{-2}, 35 keV), followed by PECVD oxide deposition, S/D activation, and contact photolithography and etching. Ti/Al was used for the metallization. S/D anneal conditions for the bulk and strained Ge p-FETs were 450 °C for 30 min. in N_2 followed by 600 °C for 2 min. in N_2, and 450 °C for 30 min. in N_2, respectively.

3.4.3 Device Characterization and Results

Figures 3.11 and 3.12 show I_S-V_G and split C-V characteristics for the bulk Ge p-MOSFETs. These devices have a –0.19 V threshold voltage, 80 mV/decade subthreshold swing, and 1.8 nm CET. I_S-V_G and split C-V characteristics for the strained Ge p-MOSFETs are shown in Figures 3.13 and 3.14. The strained Ge devices have a –0.23 V threshold voltage, 90 mV/decade subthreshold swing, and 1.6 nm CET.

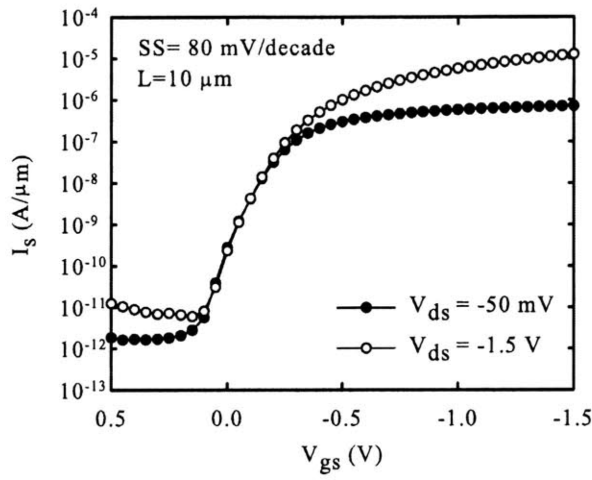


Figure 3.11: Typical as-measured I_S-V_G characteristics for bulk Ge p-MOSFETs with 140 nm TaN/5 nm HfO_2/0.7 nm GeON gate stack. These devices exhibited a –0.19 V threshold voltage and 80 mV/decade subthreshold swing (from [61]).

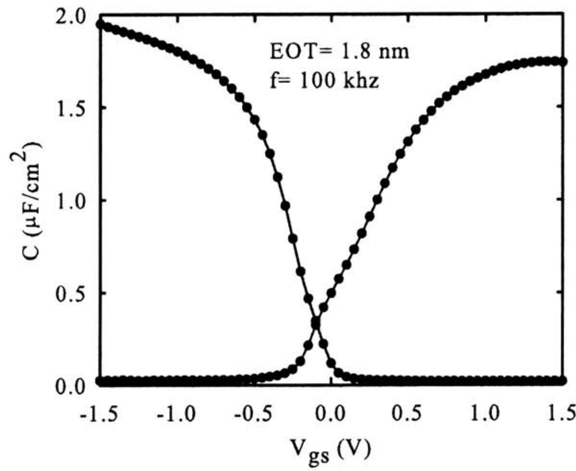


Figure 3.12: Typical as-measured split C-V characteristics for bulk Ge p-MOSFETs with 140 nm TaN/5 nm HfO_2/0.7 nm GeON gate stack. The inversion-side capacitance corresponds to a CET of 1.8 nm (from [61]).

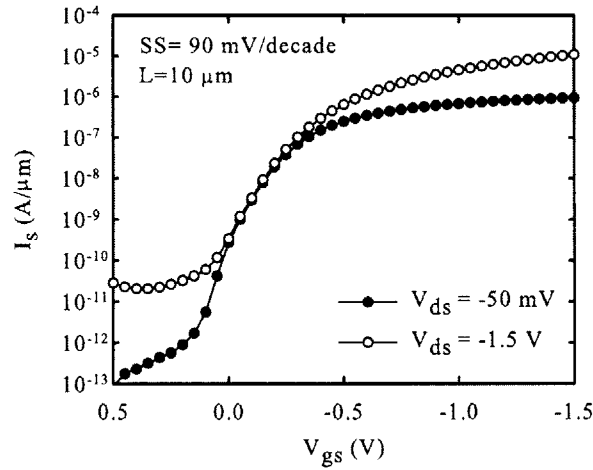


Figure 3.13: Typical as-measured I_S-V_G characteristics for strained Ge p-MOSFETs with 140 nm TaN/5 nm HfO_2/0.7 nm GeON gate stack. These devices have a –0.23 V threshold voltage and 90 mV/decade subthreshold swing (from [61]).

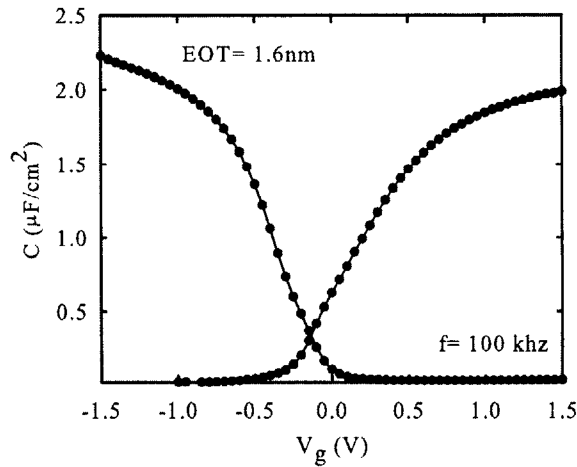


Figure 3.14: Typical as-measured split C-V characteristics for strained Ge p-MOSFETs with 140 nm TaN/5 nm HfO_2/0.7 nm GeON gate stack. The inversion-side capacitance corresponds to a CET of 1.6 nm (from [61]).

The bulk Ge devices exhibit slightly lower subthreshold swing than the strained Ge devices. This is not surprising since the bulk Ge nitridation was performed at 600 °C (vs. 500 °C for strained Ge) which results in a better interface with fewer traps [33]. Figure 3.15 compares the effective hole mobility for bulk and strained Ge p-FETs. The strained Ge devices show a 35% increase in hole mobility at high vertical effective field compared to bulk Ge devices. This enhancement is encouraging given the low level of strain present in the germanium channel and the imperfect germanium-dielectric interface.

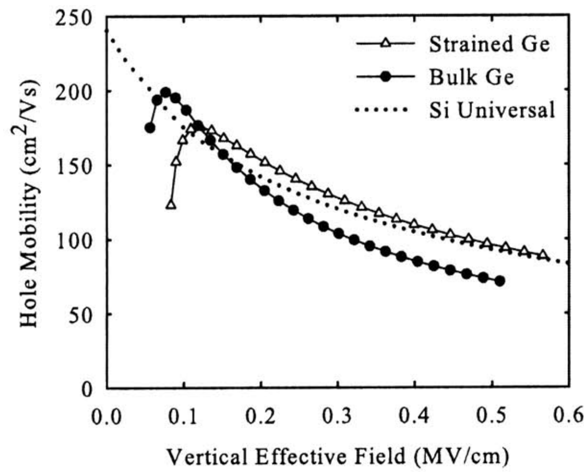


Figure 3.15: Comparison of effective hole mobility for bulk and strained Ge p-MOSFETs with 140 nm TaN/5 nm HfO_2/0.7 nm GeON gate stack. At high vertical effective field, strained Ge p-FETs show a 35% increase in mobility compared to the bulk Ge devices (adapted from [61]).

3.5 MBE GeON Interlayer MOSFETs

In addition to RTP GeON, GeON interlayers deposited by molecular beam deposition (MBD) were also explored through a collaboration with A. Dimoulas of NCSR Demokritos in Athens, Greece. TaN/HfO_2/GeON gate stack deposition was performed at NCSR, and device fabrication was completed at MIT. MBD offers a completely different approach to surface preparation prior to gate stack deposition. Rather than *ex-situ* wet cleaning, MBD allows *in-situ* desorption of germanium surface oxides under UHV conditions immediately prior to gate stack deposition. In this work, native germanium oxide was desorbed at 360 °C for 15 min. while monitoring the RHEED surface reconstruction pattern [65]. The surface was then exposed to nitrogen and oxygen atomic beams while evaporating germanium at 0.05 Å/s to form an ultra-thin (less than 0.5 nm) GeON interlayer. The gate stack was completed by *in-situ* deposition of 5 nm HfO_2 and 70 nm TaN. Molecular beam deposition of the GeON interlayer allows precise thickness control and consequently, very thin interlayers. In this work, an equivalent oxide thickness of 0.7 nm was demonstrated indicating that aggressive EOT scaling is possible for gate stacks on germanium. In general, germanium forms thinner interfacial layers than silicon for high-k deposition directly on cleaned substrates and this is perhaps one benefit of GeO_x volatility [26]. As with RTP GeON, the p-FETs showed reasonable device characteristics with carrier mobility similar to silicon universal hole mobility while the n-FETs were essentially non-functional. Device results from this collaboration are published in reference 62.

3.6 Summary of MIT Ge MOSFET Mobility

Ge n- and p-MOSFETs were fabricated with GeON, AlN, and Hf_3N_4 interlayers that were formed using techniques ranging from thermal nitridation to atomic layer deposition and molecular beam deposition. Despite the range of materials and deposition methods investigated, device performance was relatively consistent indicating a degree of commonality

in nitride-germanium interfaces. Figure 3.16 shows representative carrier mobility data for nitride interlayer Ge MOSFETs fabricated at MIT. p- and n-FET data are shown by open and closed symbols, respectively.

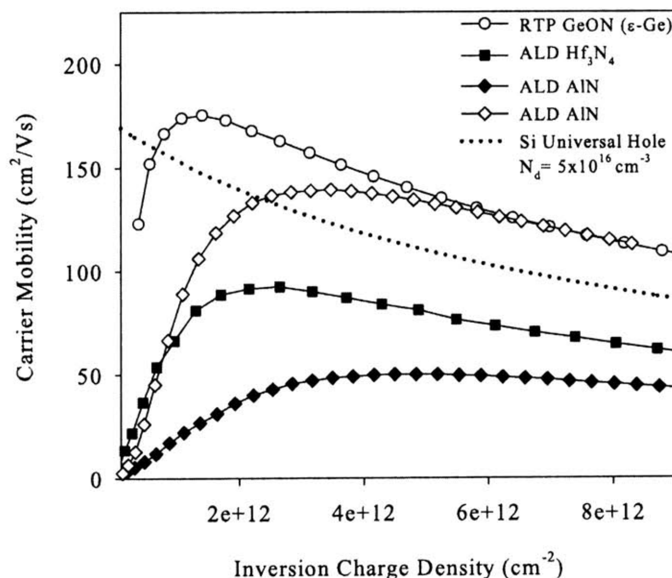


Figure 3.16: Summary of carrier mobility for nitride interlayer Ge MOSFETs fabricated at MIT. Representative data shown for p-FETs (open symbols) and n-FETs (closed symbols).

As shown in the figure, hole mobility generally matches or exceeds silicon universal hole mobility. In addition, p-FET device characteristics were generally distortion-free with subthreshold swing less than 100 mV/decade and reasonable C-V hysteresis (~100 mV). In contrast, ALD nitride interlayer n-FETs show poor mobility (typically 50-100 cm^2/Vs), distorted device characteristics, and larger C-V hysteresis (~200 mV). n-FETs based on GeON interlayers were essentially non-functional. Amongst ALD interlayers, Hf_3N_4 produced higher electron mobility (100 cm^2/Vs) while AlN produced higher hole mobility (150 cm^2/Vs). The mobilities observed in this work are consistent with other published

reports for surface-channel Ge MOSFETs with high-k dielectrics and no silicon interlayer. Based on all of the published data, the path towards high-mobility Ge p-FETs is clear; however, the same cannot be concluded for Ge n-FETs. To date, Ge n-FET device characteristics have been extremely disappointing and have contributed to renewed interest in III-V n-FETs. While many theories have been proposed to explain poor Ge n-FET performance, careful examination of carrier transport in surface-channel Ge MOSFETs has yet to be performed. In Chapter 4, carrier transport in Ge MOSFETs with WN/Al_2O_3/AlN gate stacks is experimentally investigated through low-temperature device characterization and the analysis of both surface-channel and buried-channel MOSFETs.

Chapter 4

Investigation of Carrier Transport in Ge MOSFETs with AlN Interlayers

4.1 The Ge NMOS Problem

As shown in Chapters 1 and 3, Ge MOSFETs show promising hole mobility but very poor electron mobility. Many theories have been proposed to explain poor Ge n-FET performance:

- high series resistance due to inadequate n-type activation in the S/D regions [78],
- electrochemical difference between dielectric formation on n- an p-Ge [66],
- poor thermal stability of the germanium-dielectric interface at n-type S/D activation temperatures [50],
- fundamental band structure issue (e.g. L-Δ intervalley electron scattering), and
- asymmetric distribution of interface states [38].

Although commonly cited as a reason for poor Ge n-FET performance, series resistance should not impact mobility extraction from long-channel (L_G= 20- 100 μm) devices. Active n-type dopant concentrations of $5x10^{19}$ cm^{-3} and sheet resistance values of 75 Ω/ sq. (x_j= 100 nm) have been demonstrated [18] and are more than adequate for mobility extraction from long-channel devices.

An electrochemical effect related to the presence of dopants in germanium substrates has also been suggested as a cause for poor n-FET performance. It has been theorized that Ga and Sb (common dopants in Ge wafers) affect interfacial layer formation, and thus CET, for identical gate stacks deposited on n- and p-Ge [66]. In this work, gate stacks deposited on n- and p-Ge exhibited similar CET. Furthermore, as shown in Figure 4.1, electron inversion on p-Ge (inversion-side of MOSFET split C-V characteristics) produces similar C-V characteristics to electron accumulation on n-Ge (MOSCAP C-V characteristics). The MOSFET split C-V characteristics show higher baseline capacitance due

to parasitic probe pad capacitance that is not modulated by the gate. At least for dielectric stacks with AlN interlayers, dielectric formation on n- and p-Ge does not produce significantly different C-V characteristics.

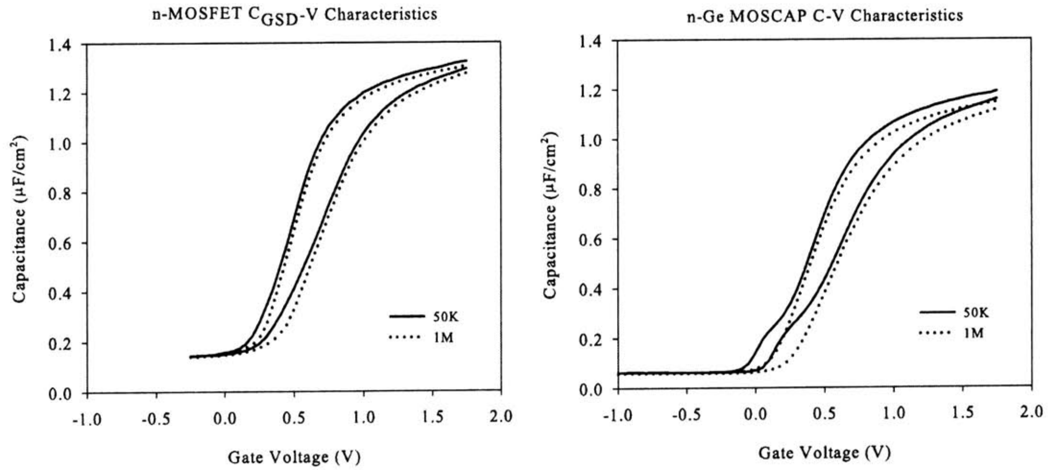


Figure 4.1: Comparison of C-V characteristics for electron inversion on p-Ge (MOSFET) and electron accumulation on n-Ge (MOSCAP). Both devices had WN/3.5 nm Al_2O_3/2.5 nm AlN gate stacks. MOSFET split C-V characteristics show higher baseline capacitance (dashed line) due to parasitic probe pad capacitance that is not modulated by the gate.

Poor gate stack thermal stability at n-type dopant activation temperatures (500- 600 °C) does affect interfacial quality and likely contributes to poor NMOS performance for some dielectrics. For example, GeON layers are known to exhibit poor thermal stability which likely degrades device performance [50]. AlN interlayers, however, exhibit stability up to at least 500 °C. In Chapter 2, the impact of post-metal annealing at 350-550 °C was explored and no significant change in C-V properties was observed at the n-type S/D activation temperature used in this work (500 °C).

Band structure related phenomena such as L-Δ intervalley scattering have also been proposed to explain the observed electron mobility in Ge n-FETs. In early published reports of high electron mobility in Ge n-FETs [e.g. 37], devices were often fabricated on

(111) substrates. In addition, recent simulations have shown that Ge n-FETs on (111) substrates should outperform those fabricated on (100) substrates [67]. However as discussed in Chapter 3, Ge n-FETs with $WN/Al_2O_3/AlN$ gate stacks were fabricated on both (111) and (100) substrates and similar mobility was observed. This suggests that substrate orientation and consequently band structure are not responsible for the degraded mobility observed in AlN interlayer Ge n-FETs.

The last and most plausible explanation for poor n-FET mobility is the germanium-dielectric interface. More specifically, an asymmetric distribution of interface states with high density near the conduction band edge will result in severely degraded electron mobility while having less impact on hole mobility. Interface states in the upper half of the bandgap are acceptor-like (neutral when empty, negatively charged when filled) and therefore act as coulomb scattering sites in n-FETs but remain uncharged in p-FETs. Interestingly, an asymmetric D_{it} distribution resulting in electron mobility degradation was also observed during early work on $HfO_2/SiON/Si$ gate stacks [68]. In the remainder of this chapter, the impact of interface states on carrier transport in Ge MOSFETs with $WN/Al_2O_3/AlN$ gate stacks is investigated. First, the interface state distribution within the bandgap is discussed. Second, the impact of this distribution on carrier mobility is determined through low-temperature device characterization and the analysis of both surface-channel and buried-channel MOSFETs.

4.2 Interface Distribution for Germanium-AlN Interfaces

The interface state distribution for $WN/Al_2O_3/AlN/Ge$ capacitors was extracted over most of the bandgap using the conductance and Gray-Brown methods as described in Chapter 2. The temperature dependence of MOSFET threshold voltage can be used to determine D_{it} even closer to the band edge (within 0.05 eV). At low temperature, the Fermi-Dirac distribution becomes more abrupt and consequently the Fermi level must move closer to the

conduction band edge for the same inversion charge density. This results in the filling of additional interface states which produces a threshold voltage shift. In the ideal case of zero interface states, the temperature dependence of the threshold voltage is given by:

$$\frac{dV_t}{dT} = -\frac{1}{2q}\frac{dE_g}{dT} + (2m-1)\frac{d\psi_B}{dT} \tag{4.1}$$

where m is the MOSFET body-effect coefficient and ψ_B is the difference between the Fermi level and intrinsic level in the bulk of the semiconductor [15]. Any additional shift that is observed can be attributed to interface state charging. In this case, the interface density is simply:

$$D_{it} = \frac{(\Delta V_{t,\,meas} - \Delta V_{t,\,ideal}) \cdot C_{ox}}{q} \tag{4.2}$$

where $\Delta V_{t,meas}$ is the observed V_t shift and $\Delta V_{t,ideal}$ is the V_t shift in the absence of interface states. V_t was extracted at each temperature by linear extrapolation of the I_S-V_G characteristic at low $|V_{DS}|$ (50 mV). Using the popular definition for inversion, $\phi_s = 2\psi_B$, and knowing the temperature dependence of ψ_B, the position of the Fermi level relative to the intrinsic level is known at inversion. Accounting for the temperature dependence of E_g, the position of the Fermi level with respect to the band edge (E_c) can then be calculated at each temperature. Thus the V_t shift that occurs between temperatures T_1 and T_2 can be attributed to interface states between $(E_c - E_{F,i})_{T_1}$ and $(E_c - E_{F,i})_{T_2}$ where $E_{F,i}$ is the Fermi level position at inversion.

Low temperature measurements on Ge MOSFETs with 40 nm WN/3.5 nm Al_2O_3/2.5 nm AlN gate stacks were performed using a standard liquid nitrogen cryostat at temperatures of 297, 250, 200, 150, 100, and 80 K. The V_t shift at low temperature is qualitatively shown by the shift of the I_S-V_G and inversion-side split C-V characteristics in Figures 4.2 and 4.3, respectively. The positive threshold voltage shift for n-FETs and negative shift for

p-FETs confirms the acceptor-like nature of states in the upper half of the bandgap and donor-like nature of interface states in the lower half of the bandgap [60]. The large shift for n-FETs relative to p-FETs indicates a gross asymmetry in the interface state distribution near the band edge. Figure 4.4 shows the D_{it} distribution extracted from the temperature dependence of threshold voltage. D_{it} values extracted using the conductance and Gray-Brown methods are included for reference. As shown in the figure, the interface state density is clearly asymmetric. D_{it} near the valence band edge (VBE) rises slowly and saturates at approximately $1x10^{13}$ cm^{-2} eV^{-1}. In contrast, D_{it} rises very rapidly near the conduction band edge (CBE) and approaches $6x10^{13}$ cm^{-2} eV^{-1}. The number of additional interface states near the CBE relative to the VBE (indicated by dotted triangle in Figure 4.4) is approximately $2x10^{12}$ cm^{-2} which is similar to the trapped charge density estimated from the low temperature MOSCAP measurements in Chapter 2. The clear asymmetry in near-band-edge D_{it} suggests that interface states are the principal cause of poor n-FET performance.

The next section discusses carrier transport in Ge MOSFETs with AlN interlayers. Low temperature mobility measurements were performed to better understand the mobility degradation mechanism. In addition, buried-channel MOSFETs were fabricated to investigate transport in devices with reduced interaction between carriers and interface states.

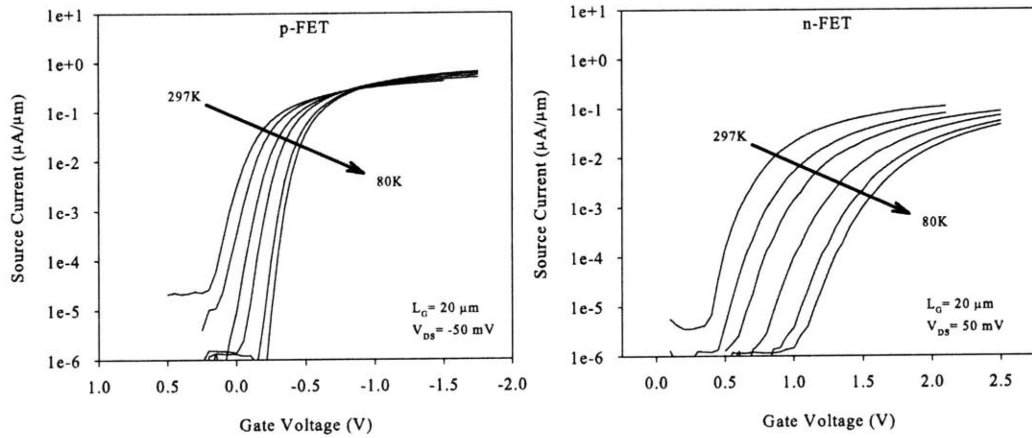


Figure 4.2: I_S-V_G characteristics as a function of temperature (297, 250, 200, 150, 100, and 80 K) for Ge p- and n-FETs with 40 nm WN/3.5 nm Al_2O_3/2.5 nm AlN gate stack. The large V_t shift for n-FETs relative to p-FETs suggests higher D_{it} in the upper half of the bandgap, particularly near the conduction band edge.

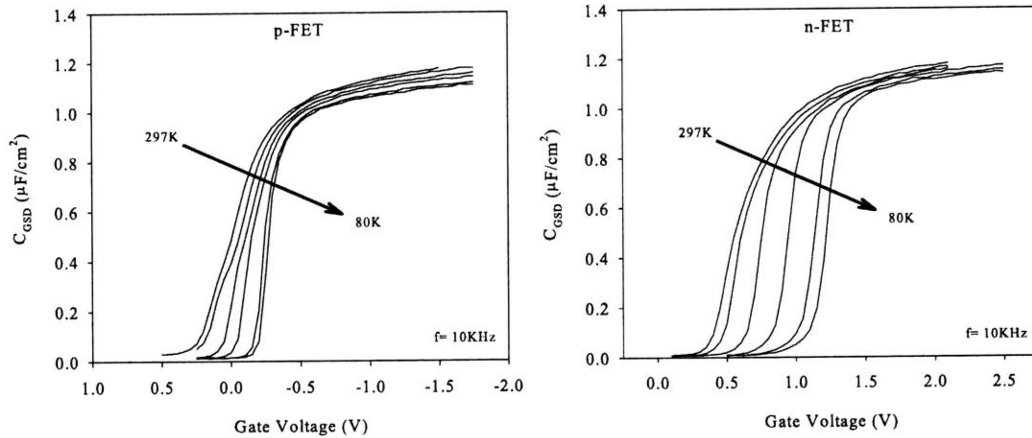


Figure 4.3: Inversion-side split C-V characteristics (C_{GSD}) as a function of temperature (297, 250, 200, 150, 100, and 80 K) for Ge p- and n-FETs with 40 nm WN/3.5 nm Al_2O_3/ 2.5 nm AlN gate stack.

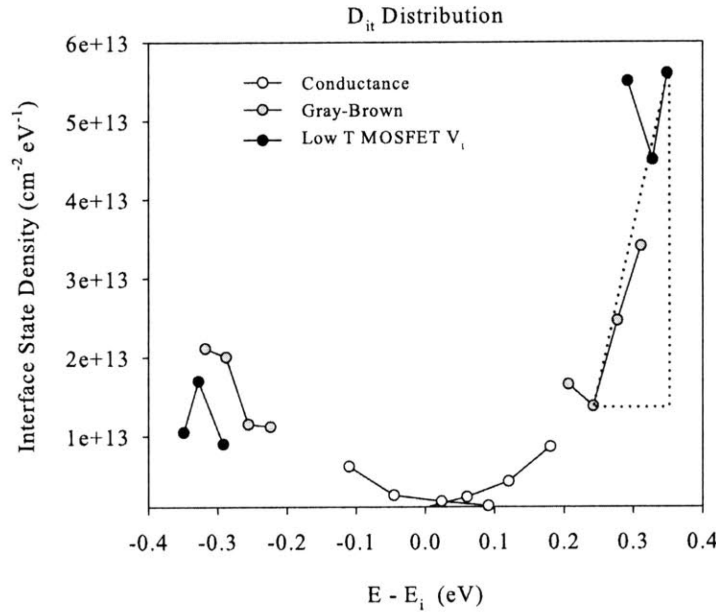


Figure 4.4: Interface state distribution for WN/3.5 nm Al_2O_3/2.5 nm AlN gate stack on germanium. Conductance, Gray-Brown, and temperature dependence of MOSFET V_t were used to map D_{it} across the bandgap. D_{it} rises rapidly near the conduction band edge and approaches $6x10^{13}$ cm^{-2} eV^{-1}. The number of additional interface states near the CBE relative to the VBE (indicated by dotted triangle) is approximately $2x10^{12}$ cm^{-2} which is similar to the trapped charge density estimated from the low temperature MOSCAP measurements in Chapter 2.

4.3 Low Temperature Mobility Characterization

As described in the previous section, low temperature measurements were performed on Ge MOSFETs with 40 nm WN/3.5 nm Al_2O_3/2.5 nm AlN gate stacks. Effective mobility was extracted from the same-device I_S-V_G and split C-V data shown in Figures 4.2 and 4.3, respectively. Figure 4.5 shows the effective electron and hole mobility as a function of temperature.

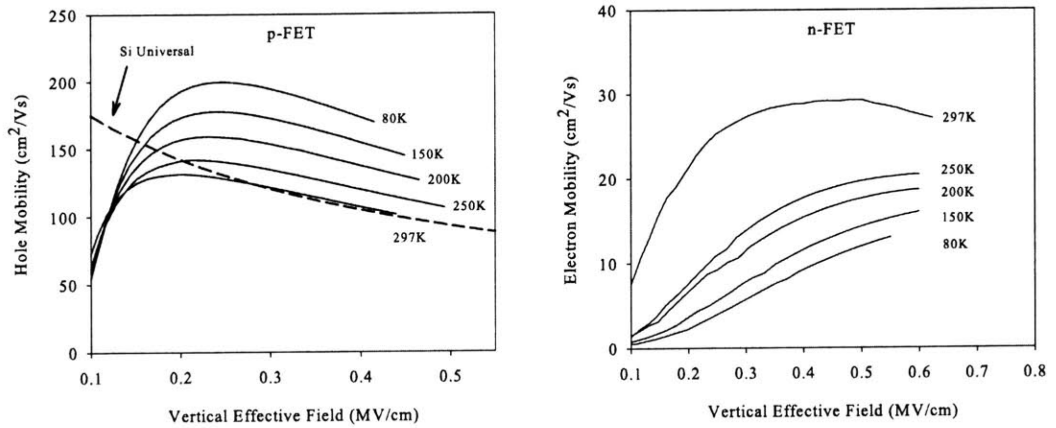


Figure 4.5: Carrier mobility as a function of temperature (297, 250, 200, 150, 100, and 80 K) for Ge p- and n-FETs with 40 nm WN/3.5 nm Al_2O_3/2.5 nm AlN gate stack. Electron mobility decreased with decreasing temperature indicating significant charge trapping in interface states near the conduction band edge. Distortion of the electron mobility curves can be attributed to coulomb scattering from charged interface states.

As expected, hole mobility increased with decreasing temperature due to reduced phonon scattering. In contrast, electron mobility decreased with decreasing temperature indicating significant charge trapping in interface states near the conduction band edge [69]. The low temperature n-FET mobility curves also show severe distortion due to coulomb scattering from charged interface states. This data shows that the degraded mobility of Ge n-MOS-FETs with AlN interfacial layers, and possibly Ge n-MOSFETs in general, is due to a large number of interface states near the conduction band edge that trap carriers and act as coulomb scattering sites. Trapping of carriers results in an overestimation of mobile charge and consequently the extracted mobility is lower than the true mobility. However, for small fractions of trapped charge (0.1- 0.2), the effective mobility (particularly at high inversion charge density) will only be reduced by a similar fraction. Assuming that the surface mobility ratio between germanium and silicon should be similar to the bulk mobility ratio, the best surface-channel electron mobility achieved in this work (160 cm^2/Vs) is

still approximately 4x lower than expected. This severe reduction cannot be explained by carrier trapping and therefore must be due to carrier scattering (e.g. coulomb scattering from charged interface states and fixed charge). Published data on SiGe surface-channel p-MOSFETs with ALD $TiN/Al_2O_3/HfAlO_x/Al_2O_3$ gate stacks illustrates the relative impact of trapping and coulomb scattering on carrier mobility [70]. Figure 4.6 shows the mobility correction due to 1×10^{12} cm^{-2} trapped carriers as well as coulomb scattering from 1×10^{12} cm^{-2} and 4×10^{12} cm^{-2} charged interface states. To correct for carrier trapping, mobile charge rather than total inversion charge is used for mobility extraction. To correct for coulomb scattering, the coulomb limited mobility (μ_{Cit}) is first estimated from:

$$\mu_{Cit} = 1.47 \times 10^{18} \frac{\sqrt{Q_i}}{N_{it,C}} \tag{4.3}$$

where Q_i is the mobile inversion charge density and $N_{it,C}$ is the density of charged interface states [70]. The corrected mobility (μ_{corr}) is then obtained from Mathiessen's Rule using the following expression:

$$\frac{1}{\mu_{corr}} = \frac{1}{\mu_{corr,Qi}} - \frac{1}{\mu_{Cit}} \tag{4.4}$$

where $\mu_{corr,\,Qi}$ is the mobility corrected only for trapped inversion charge [70].

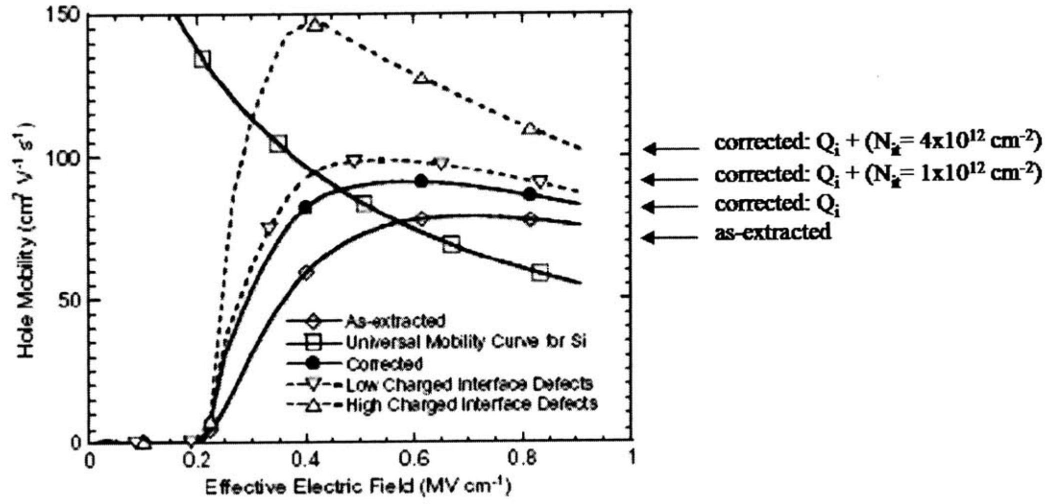


Figure 4.6: Hole mobility for SiGe surface-channel p-MOSFETs with ALD TiN/Al_2O_3/ $HfAlO_x/Al_2O_3$ gate stack. As-extracted mobility is compared with mobility corrected for carrier trapping (Q_i), carrier trapping plus coulomb scattering from $1x10^{12}$ cm^{-2} interface states, and carrier trapping plus coulomb scattering from $4x10^{12}$ cm^{-2} interface states (from [70]).

As can be seen in the figure, the correction for trapped carriers is relatively small while coulomb scattering accounts for the majority of the observed mobility degradation. To confirm that interfacial trapping and scattering are primarily responsible for mobility degradation in Ge n-FETs with $WN/Al_2O_3/AlN$ gate stacks, buried-channel devices were fabricated to reduce the interaction of carriers with the germanium-AlN interface.

4.4 Buried-Channel MOSFETs

4.4.1 Device Fabrication

Long-channel annular Ge p- and n-MOSFETs were fabricated on bulk (100) Ge substrates (Sb: 0.13-0.16 Ω-cm, Ga: 0.16-0.47 Ω-cm). First, an 11 nm SiO_2 screen oxide was deposited by low-temperature CVD followed by channel implantation. The n-FETs received phosphorus implants of 1×10^{12} cm^{-2} at 10 keV, and 2×10^{12}, 4×10^{12}, and 1×10^{13} cm^{-2} at 15 keV while the p-FETs received BF_2 implants of 1×10^{12} cm^{-2} at 16 keV, and 2×10^{12},

4×10^{12}, and 1×10^{13} cm^{-2} at 24 keV. Doses were chosen to be similar to typical MOSFET inversion charge densities. Dose and energy were also selected to ensure that some of the devices could be completely shutoff with gate bias. Table 4.1 shows the simulated implant depth and peak concentration for each of the doses. The depth is given with respect to the germanium surface. The P and BF_2 implant energies were adjusted to give the same implant depth.

Implant Dose (cm^{-2})	N_{peak} (cm^{-3})	Depth (nm)
$1x10^{12}$	$6x10^{17}$	at Ge-SiO_2 interface
$2x10^{12}$	$9x10^{17}$	6
$4x10^{12}$	$2x10^{18}$	6
$1x10^{13}$	$4x10^{18}$	6

Table 4.1: Simulated depth and peak concentration for buried-channel implants. Depth is given with respect to the germanium surface. P and BF_2 implant energies were adjusted to give the same depth.

The BF_2 and P implants were activated at 400 °C and 500 °C, respectively, for 60 s in N_2. Following channel implant activation, the screen oxide was removed in 50:1 DI:HF and the wafers were then immersed in 6:1 DI:HCl for 5 min. and rinsed in DI water in preparation for gate stack deposition. An *in-situ* ALD WN/3.5 nm Al_2O_3/ 2.5 nm AlN gate stack was then deposited on all wafers [41]. After gate etching, S/D implantation was performed (BF_2: 1×10^{15} cm^{-2}, 40 keV; P: 1×10^{15} cm^{-2}, 25 keV), followed by PECVD oxide deposition, S/D activation, and contact patterning. Ti/Al was used for the metallization. S/D anneal conditions for the p- and n-FETs were 450 °C for 30 min. in forming gas and 500 °C for 60 s in N_2, respectively.

4.4.2 Experimental Results

Figure 4.7 shows I_S-V_G characteristics, Figure 4.8 shows inversion-side split C-V charac-

teristics (C_{GSD}), and Figure 4.9 shows effective carrier mobility, measured from the same p-FET or n-FET for each dose.

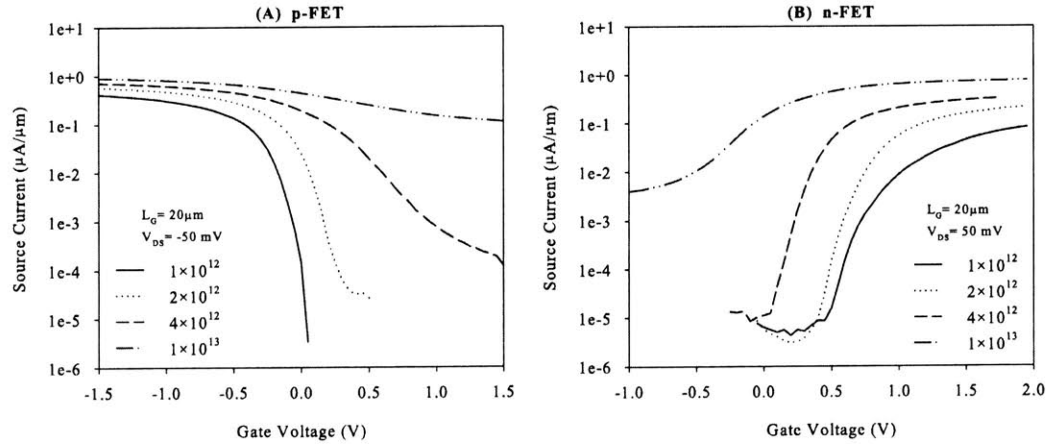


Figure 4.7: Measured I_S-V_G characteristics for long-channel Ge p-FETs (a) and n-FETs (b) that received 1×10^{12}, 2×10^{12}, 4×10^{12}, and 1×10^{13} cm^{-2} channel implants. In contrast to p-FETs, n-FETs show decreasing subthreshold swing as implant dose increases from 1×10^{12} to 4×10^{12} cm^{-2}

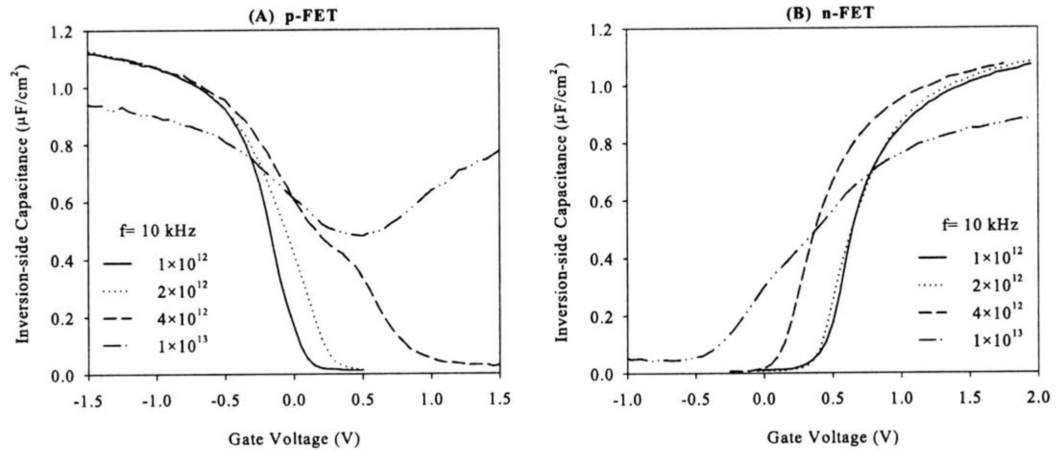


Figure 4.8: Measured inversion-side split C-V characteristics (C_{GSD}) for Ge p-FETs (a) and n-FETs (b) that received 1×10^{12}, 2×10^{12}, 4×10^{12}, and 1×10^{13} cm^{-2} channel implants. p-FETs show C-V stretch-out associated with transition from surface-channel to buried-channel operation as implant dose increases from 1×10^{12} to 1×10^{13} cm^{-2}. In contrast, n-FETs show a simple shift of C_{GSD} characteristics for low implant doses (1×10^{12}- 4×10^{12} cm^{-2}) with only the highest implant dose (1×10^{13} cm^{-2}) showing evidence of buried-channel operation.

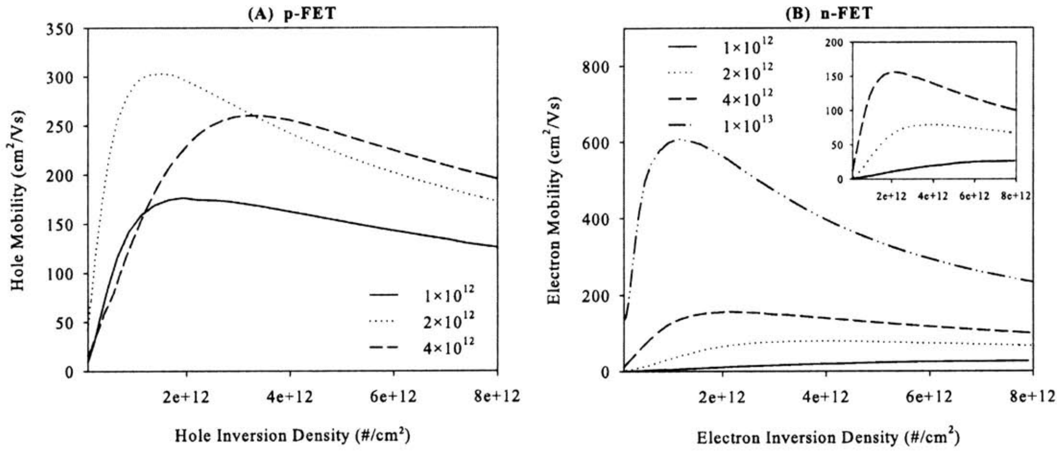


Figure 4.9: Effective carrier mobility for Ge p-FETs (a) and n-FETs (b) that received 1×10^{12}, 2×10^{12}, 4×10^{12}, and 1×10^{13} cm^{-2} channel implants. Peak mobilities of 300 and 600 cm^2/Vs were observed for p- and n-FETs, respectively. Inset of (b) shows electron mobility on reduced vertical scale to provide a better view of carrier mobility in Ge n-FETs with 1×10^{12}- 4×10^{12} cm^{-2} channel implants. Mobility was extracted using the standard split C-V method for devices that could be sufficiently turned off with gate bias.

The p-FET device characteristics show expected behavior as the devices transition from surface-channel to buried-channel operation with increasing channel implant dose. Figures 4.7a and 4.8a show increasing subthreshold swing and increased C-V stretch-out for higher implant doses. For implant doses up to 4×10^{12} cm^{-2}, the devices operate at reduced vertical effective field (E_{eff}) while the device that received the 1×10^{13} cm^{-2} dose shows buried-channel behavior and significantly reduced capacitance equivalent oxide thickness (CET). Figure 4.9a shows the effective hole mobility as a function of implant dose. As expected, reduced E_{eff} and buried-channel operation results in increased mobility due to reduced interaction with interface states. These devices exhibit peak mobility of 300 cm^2/Vs and 2-3x improvement over Si universal hole mobility. At a dose of 4×10^{12} cm^{-2}, ionized impurity scattering starts to become significant and mobility improvement saturates. Figures 4.7b and 4.8b show the n-FET I_S-V_G and split C-V characteristics. n-FETs that

received the highest dose (1×10^{13} cm^{-2}) show clear buried-channel behavior and peak mobility of 600 cm^2/Vs (Figure 4.8b). The 1×10^{12} cm^{-2} dose devices show a distorted mobility curve with a peak value of 26 cm^2/Vs (inset Figure 4.9b). While both n- and p-FETs show substantial mobility improvement for reduced E_{eff} and/or buried-channel operation, the impact on electron mobility is dramatic. This difference is due to the asymmetric distribution of interface states within the bandgap. Since the peak mobilities extracted in this work correspond to carriers in doped buried channels with low vertical effective field, these results are best compared against the bulk conductivity mobility of similarly doped n- and p-Ge. From resistivity data [5], the electron and hole mobility for a given doping concentration can easily be calculated. The buried-channel implants resulted in peak concentrations of 1- 4×10^{18} cm^{-3} (Table 4.1), so bulk electron and hole mobility were calculated assuming a doping level of 2×10^{18} cm^{-3}. Table 4.2 compares the measured and calculated carrier mobilities. Given the assumptions involved in this comparison, the agreement is reasonable. The buried channel mobility is expected to be lower than the bulk conductivity mobility since the carriers are not completely isolated from the interface. Furthermore, the active doping concentration/profile is not precisely known which adds additional uncertainty to this comparison.

Parameter	Measured Values	Calculated Values (assuming doping of 2×10^{18} cm^{-3})
Electron mobility (cm^2/Vs)	600	781
Hole mobility (cm^2/Vs)	300	481
Mobility ratio (μ_e/μ_h)	2.0	1.6

Table 4.2: Comparison of peak electron and hole mobility measured in buried-channel MOSFETs with bulk conductivity mobility of n- and p-Ge. Bulk conductivity mobility was calculated assuming a doping of 2×10^{18} cm^{-3}.

Due to process variation, some 1×10^{13} cm^{-2} dose n-FETs exhibited different degrees of buried-channel operation as evidenced by differences in peak CET. Figure 4.10 shows effective mobility for 1×10^{13} cm^{-2} dose n-FETs with peak CETs of 4.5 and 6 nm (mobility for 1×10^{12} cm^{-2} dose device with peak CET of 3 nm is shown for comparison). As expected, devices that are "more buried" show higher CET, higher mobility, and cannot be shutoff with gate bias. For the 6 nm CET device, inversion charge was determined using both split C-V and Hall measurements. At an inversion charge density of $8x10^{12}$ cm^{-2}, this device shows an effective mobility of approximately ~350 cm^2/Vs. Buried-channel p-FETs show a mobility of ~200 cm^2/Vs at similar charge density. The buried-channel hole mobility observed in this work closely agrees with recently published data for Ge p-FETs with 0.5 nm silicon interlayers [34] which suggests that 2-3x enhancement over silicon universal could be achieved for surface-channel devices with a high quality germanium-dielectric interface.

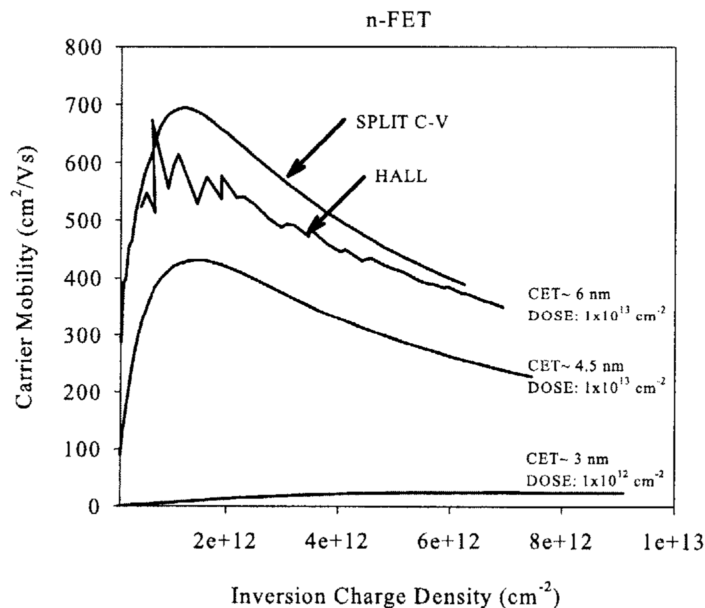


Figure 4.10: Effective mobility for 1×10^{13} cm^{-2} dose buried-channel n-FETs with peak CETs of 4.5 and 6 nm. Mobility for 1×10^{12} cm^{-2} dose n-FET with peak CET of 3 nm is shown for reference. For n-FET with 6 nm CET, inversion charge was determined using both split C-V and Hall measurements.

4.4.3 Phosphorus Passivation Effect

Interestingly, n-FETs that received lower implant doses (1×10^{12}- 4×10^{12} cm^{-2}) *do not* exhibit the signature behavior of reduced E_{eff} and/or buried-channel operation. The sub-threshold swing of these devices decreases for doses up to 4×10^{12} cm^{-2} and the split C-V characteristics exhibit a simple shift rather than the expected stretch-out that was observed for p-FETs. In addition to reduced subthreshold swing, the I_S-V_G characteristics also show less distortion for doses up to 4×10^{12} cm^{-2}. Fig. 4.11 shows CET vs. inversion charge (CET-n_{inv}) for both n- and p-FETs. By definition, reduced E_{eff} is manifested by increased CET for a given amount of inversion charge. As shown in Fig. 4.11, p-FETs clearly show this behavior for each of the implant conditions. In contrast, n-FETs that received 1×10^{12}- 4×10^{12} cm^{-2} doses show nearly identical CET-n_{inv} characteristics, which implies that they are not operating under reduced E_{eff} or as buried-channel devices.

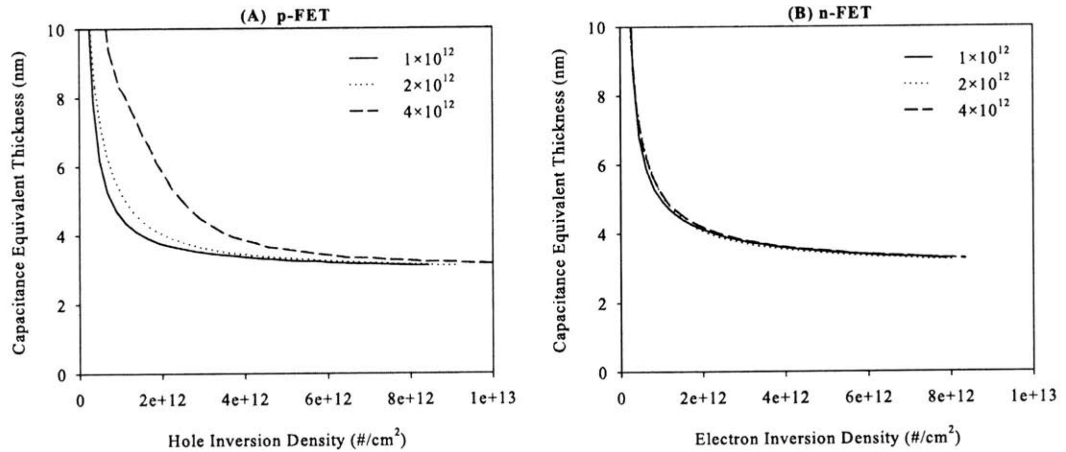


Figure 4.11: Capacitance equivalent thickness (CET) vs. inversion charge density for Ge p-FETs (a) and n-FETs (b) that received 1×10^{12}, 2×10^{12}, and 4×10^{12} cm^{-2} channel implants. p-FETs show evidence of reduced E_{eff} and/or buried-channel operation while n-FETs appear to be surface-channel devices. Plots were obtained by integrating the split C-V characteristics.

Despite this fact, the 2×10^{12} and 4×10^{12} cm^{-2} dose devices still show substantially increased mobility accompanied by reduced subthreshold swing. The 4×10^{12} cm^{-2} dose device has a peak electron mobility of 150 cm^2/Vs and 6x increase at high field relative to the 1×10^{12} cm^{-2} dose device. Since this improvement is not obviously explained by reduced E_{eff}, it is possible that phosphorus accumulates at the interface and either passivates interface states or prevents them by altering or suppressing GeO_x [48], [71]. Both lower subthreshold swing and reduced distortion of the I_S-V_G characteristics suggest a reduction in interface state density. Furthermore, the threshold voltage of the 4×10^{12} cm^{-2} dose device is shifted closer to the ideal value of +0.5 V which also suggests that interface states have been passivated. This theory is consistent with published diffusion studies of phosphorus-implanted germanium in which out-diffusion and segregation of phosphorus at the germanium-dielectric interface was observed [19]. In addition, plasma PH_3 treatment [48] and AlP_xO_y dielectrics [71] have previously been reported to improve the electrical characteristics of Ge MOS devices.

4.5 Summary

Carrier transport in Ge n-MOSFETs with WN/3.5 nm Al_2O_3/2.5 nm AlN gate stacks was investigated through low temperature device characterization and buried-channel device operation. Low temperature characterization showed significant electron trapping and a high density of interface states within 0.05 eV of the conduction band edge. The density of states near the conduction band edge approached 6×10^{13} cm^{-2} eV^{-1}, approximately 5x higher than near the valence band edge. Buried-channel Ge n- and p-FETs were fabricated and peak mobilities of 600 cm^2/Vs and 300 cm^2/Vs were observed, respectively. These values agree reasonably well with the bulk conductivity mobility of similarly doped n- and p-Ge and demonstrate that surface-channel mobility is limited by the quality of the germanium-dielectric interface. In contrast to buried-channel p-FETs, n-FETs that received phosphorus implants ranging from 1×10^{12}- 4×10^{12} cm^{-2} did not exhibit reduced E_{eff}/ buried-channel behavior but still showed mobility improvement. Given previously published results, it seems plausible that phosphorus is accumulating at the germanium-dielectric interface and either passivating near-band-edge interface states or preventing interface state formation by altering or suppressing GeO_x formation. These results provide the first direct evidence that phosphorus incorporation at the interface leads to improved mobility and suggest that it is possible to achieve reasonable electron mobility with high-k dielectrics directly on germanium. Furthermore, phosphorus-based passivation techniques may be useful in improving other germanium-dielectric interfaces.

Chapter 5

Conclusions

5.1 Summary

Recent analysis has shown a strong correlation between intrinsic transistor delay, source injection velocity, and low-field carrier mobility. To maintain historical performance trends for ultra-scaled (L_G= 10 nm) CMOS devices, significant improvement in source injection velocity is required. Replacing silicon with a higher mobility semiconductor is one potential solution. Of the high mobility semiconductors, only germanium offers significant improvement in both electron (~2.4x) and hole (~4x) mobility. In addition, the band structure of germanium results in low transport effective mass and high inversion charge density for electrons on (111)-oriented substrates. High inversion charge density allows (111) Ge n-MOSFETs to match or exceed the performance of III-V MOSFETs for devices with aggressively scaled equivalent oxide thickness (0.5- 1.0 nm). However, formation of a high quality germanium-dielectric interface remains a serious challenge that threatens to limit the ultimate performance of these devices. High-k dielectrics (HfO_2, ZrO_2) deposited directly on cleaned germanium result in a poor quality interface due to germanium in-diffusion, interfacial reactions, crystallization of the high-k dielectric, and GeO_x formation at the interface. Inserting an interfacial layer between the high-k dielectric and germanium surface mitigates these problems. To date, germanium oxide has been unable to provide a high quality, thermally stable interface with germanium, so alternative interlayers must be considered. Proposed interlayers include GeON, Si, and metal nitrides such as AlN and Hf_3N_4, with this work focusing on nitride-based interlayers.

A model dielectric stack process consisting of RCA-based surface preparation followed by ALD deposition of an aluminum nitride (AlN) interfacial layer and aluminum

oxide (Al_2O_3) capping layer was studied in detail. Despite its limitations (bulk traps and fixed charge), AlN is one of only a few dielectric layers (GeON, AlN, Hf_3N_4, $LaAlO_3$) that have produced functional Ge n-MOSFETs. In this study, the effects of AlN thickness and PMA conditions on the electrical properties of Al_2O_3/AlN dielectric stacks were investigated. Interface state characterization was performed on Ge capacitors fabricated using an optimized gate stack and post-metal anneal. Optimal C-V characteristics were achieved for an AlN interlayer thickness of 2.5 nm and either a 500 °C 60 s N_2 or 450 °C 30 min. FG anneal. Gate stacks annealed in N_2 were stable up to 500 °C with noticeable degradation observed at 550 °C. Low temperature C-V measurements revealed a decrease in peak capacitance at low temperature and/or high measurement frequency for n-Ge capacitors. This behavior was attributed to electron trapping at the interface, and based on the observed frequency dispersion, the percentage of trapped carriers at high accumulation charge density was estimated to be approximately 15%.

Ge n- and p-MOSFETs were fabricated with GeON, AlN, and Hf_3N_4 interlayers deposited using techniques ranging from thermal nitridation to atomic layer deposition and molecular beam deposition. Surface preparation methods included standard wet cleans (dilute HF, modified RCA clean) as well as *in-situ* GeO_x desorption under UHV conditions. Despite the range of materials and methods investigated, device performance was relatively consistent indicating a degree of commonality in nitride-germanium interfaces. Hole mobility generally matched or exceeded silicon universal hole mobility. In addition, p-FET device characteristics were relatively distortion-free with subthreshold swing less than 100 mV/decade and reasonable C-V hysteresis (~100 mV). In contrast, ALD nitride interlayer n-FETs showed poor mobility (typically 50-100 cm^2/Vs), distorted device characteristics, and larger C-V hysteresis (~200 mV). n-FETs based on GeON interlayers were essentially non-functional, probably due to poor thermal stability at the n-

type S/D activation temperature used in this work (500 °C). Amongst ALD interlayers, Hf_3N_4 produced higher electron mobility (100 cm^2/Vs) while AlN produced higher hole mobility (150 cm^2/Vs). Based on these and other published results, a clear path towards high-mobility Ge p-FETs is apparent; however, the same cannot be concluded for Ge n-FETs. To date, Ge n-FET device characteristics have been extremely disappointing and have contributed to renewed interest in III-V n-FETs.

Many theories have been proposed to explain poor Ge n-FET performance. These theories were investigated and it was found that an asymmetric distribution of interface states in the bandgap is the primary cause of low electron mobility in AlN interlayer n-FETs. For germanium-AlN interfaces, the interface state density near the conduction band edge approaches $6x10^{13}$ cm^{-2} eV^{-1}, approximately 5x higher than near the valence band edge.

Carrier transport in Ge n-MOSFETs with WN/3.5 nm Al_2O_3/2.5 nm AlN gate stacks was investigated through low temperature device characterization and buried-channel device operation. Low temperature mobility characterization showed significant electron trapping at the germanium-dielectric interface. To reduce the interaction of carriers with interface states, buried-channel Ge n- and p-FETs were fabricated and peak mobilities of 600 cm^2/Vs and 300 cm^2/Vs were observed, respectively. These values agree reasonably well with the bulk conductivity mobility of similarly doped n- and p-Ge and demonstrate that surface-channel mobility is limited by the quality of the germanium-dielectric interface. In contrast to buried-channel p-FETs, n-FETs that received phosphorus implants ranging from 1×10^{12}- 4×10^{12} cm^{-2} did not exhibit reduced E_{eff}/ buried-channel behavior but still showed mobility improvement. These experiments provide the first direct evidence that phosphorus incorporation at the interface leads to improved mobility in Ge n-FETs.

In summary, the specific contributions of this work include:

- development and optimization of AlN interlayer MOS gate stacks,
- determination of the interface state distribution for WN/Al_2O_3/AlN gate stacks on germanium,
- performance evaluation of Ge MOSFETs with AlN, Hf_3N_4, and GeON interlayers prepared using atomic layer deposition, rapid thermal nitridation, and molecular beam deposition
- investigation of limiting factors in Ge n-FET surface mobility including an evaluation of carrier transport in surface-channel and buried-channel MOSFETs with WN/ Al_2O_3/AlN gate stacks, and
- discovery of a novel phosphorus-based passivation technique that significantly improves Ge n-FET device performance.

5.2 Future Work

Additional optimization of AlN and Hf_3N_4 interlayer gate stacks may be possible. The process space investigated in this work was limited to RCA-based cleaning followed by ALD deposition and post metal annealing in either N_2 for 60 s or 8:1 N_2:H_2 for 30 min. Each of these steps could be investigated in more detail. Other surface preparation techniques and more complex interlayers (e.g. AlON, HfON, HfAlON) could certainly be explored. As has been observed with silicon [75], interlayers with reduced nitrogen content may improve carrier mobility. Recent evidence also suggests that alternative surface preparations may be superior to the RCA-based cleans used in this work. Surface preparation and interlayer formation are dependent processes that must be co-optimized. It was recently discovered that dielectric stacks deposited on as-received wafers from the supplier (Umicore) exhibit better electrical properties than on RCA-cleaned wafers. Furthermore, for as-received wafers, pure Al_2O_3 appears to perform better than Al_2O_3/AlN stacks. Since the supplier's surface preparation technique is proprietary, it is difficult to speculate why this may be the case; however, it seems likely that pre-existing germanium oxide is acting as an interlayer. The thermal stability of this apparent interlayer is unknown. Understanding the conditions under which this layer forms and being able to

controllably form this layer prior to high-k deposition are critical first steps. If the thermal stability of this layer is poor, nitrogen or other stabilizing elements (e.g. Si) could be added [75]. This thesis also provides a detailed description of symptoms associated with degraded NMOS mobility so rapid screening of new gate stack processes should be possible. Furthermore, phosphorus-based passivation techniques are a promising new direction for improving Ge n-FET performance.

Appendix A

MOSFET Process Flow

The process flow described in this appendix includes optional process modules for LTO device isolation and buried-channel MOSFETs.

Device Isolation Process Module (optional)

1. RCA Clean
   Machine: TRL RCA
   Recipe: see notes
   Notes: (1) 6:1 DI:HCl 10 min.
   (2) Rinser 1
   (3) 5:1:1 DI:NH_4OH:H_2O_2 30 s
   (4) Rinser 1
   (5) 6:1 DI:HCl 10 min.
   (6) Rinser 2
   (7) Dry with N_2 gun

2. LTO- Active Area- 130 nm
   Machine: ICL Tube 6C
   Recipe: "LTO 400C 53A SPK", ~30.6 Å/min., 43 min.
   Notes:

3. Photo- Active Area
   Machine: TRL HMDS, Coater, and EV1
   Recipe: HMDS Setting 5, 4 s dispense, 4 KRPM 40 s, Expose 3.0 s, Develop 45 s
   Notes:

4. Etch- Active Area
   Machine: TRL Acidhood2
   Recipe: 3:1 DI:BOE 80 s
   Notes: Etch rate~ 25 Å/s

5. Ash- Active Area
   Machine: TRL Asher
   Recipe: 1 hr. 15 min.
   Notes:

Buried-Channel Implant Module (optional)

6. RCA Clean
   Machine: TRL RCA
   Recipe: see notes
   Notes: (1) 6:1 DI:HCl 10 min.
   (2) Rinser 1
   (3) 5:1:1 DI:NH_4OH:H_2O_2 *10 s* to minimize etching of germanium
   (4) Rinser 1
   (5) 6:1 DI:HCl 10 min.
   (6) Rinser 2
   (7) Dry with N_2 gun

7. LTO- Implant Screen Oxide- 10 nm
   Machine: ICL Tube 6C
   Recipe: "LTO-GATE1", ~5.25 Å/min., 21 min.
   Notes: Wafers loaded in 4" boat between 4" dummy wafers

8. Buried Channel Implant
   Machine: Innovion
   Recipe: variable
   Notes:

9. Post Implant Clean
   Machine: TRL Acidhood2
   Recipe: 5 min. Nanostrip
   Notes:

10. RCA Clean
    Machine: TRL RCA
    Recipe: see below
    Notes: (1) 6:1 DI:HCl 10 min.
    (2) Rinser 1
    (3) 5:1:1 DI:NH_4OH:H_2O_2 30 s
    (4) Rinser 1
    (5) 6:1 DI:HCl 10 min.
    (6) Rinser 2
    (7) Dry with N_2 gun

11. Buried Channel Implant Activation
    Machine: ICL RTA2
    Recipe: N_2 setpoint= 25, Emissivity= 55, TC control
    Notes: PMOS: 400 °C 60 s (APR400.rcp)
    NMOS: 500 °C 60 s (APR500.rcp)

Annular MOSFET Process Module

12. RCA Clean

For Surface-Channel MOSFETs:
Machine: TRL RCA
Recipe: see notes
Notes: (1) 6:1 DI:HCl 10 min.
(2) Rinser 1
(3) 5:1:1 DI:NH_4OH:H_2O_2 30 s
(4) Rinser 1
(5) 6:1 DI:HCl 10 min.
(6) Rinser 2
(7) Dry with N_2 gun

For Buried-Channel MOSFETs:
Machine: TRL Acidhood2
Recipe: clean + target 20 nm oxide removal
Notes: (1) 5:1:1 DI:NH_4OH:H_2O_2 30 s
(2) Rinse in labware
(3) 50 s 50:1 DI:HF, etch rate~ 4.0 Å/s
(4) Rinse in labware
(5) 6:1 DI:HCl 10 min.
(6) Rinse in labware
(7) Dry with N_2 gun

13. ALD Gate Stack

Machine: ALD reactor
Recipe: WN/Al_2O_3/AlN stack (see below)
Notes:

Film: AlN
Cycles: 25
Carrier: 10 sccm
Substrate T: 200 °C

Precursor	Precursor T	Pulse (s)	Expo (s)	Pump (s)
TDMAA	110 °C	0.2	0	8
NH_3	N/A	0.1	0.1	12

Film: Al_2O_3
Cycles: 35
Carrier: 10 sccm
Substrate T: 200 °C

Precursor	Precursor T	Pulse (s)	Expo (s)	Pump (s)
TDMAA	110 °C	0.2	0	8
H_2O	N/A	0.015	0	8

Film: WN
Cycles: 1000
Carrier: 10 sccm
Substrate T: 375 °C

Precursor	Precursor T	Pulse (s)	Expo (s)	Pump (s)
N_2 ASSIST	N/A	0.015	0	1
W	90 °C	0.1	0	8
NH_3	N/A	0.2	0.2	12

14. Photo- Gate
    Machine: TRL HMDS, Coater, and EV1
    Recipe: HMDS Setting 5, 4 s dispense, 4 KRPM 40 s, Expose 3.0 s, Develop 45 s
    Notes:

15. Etch- Gate
    Machine: TRL Plasmaquest
    Recipe: TANETCH.rcp, 60 s (see below)
    Notes: (A) Before etching, run ETCHCLN.rcp for 10 min., TANETCH for 10 min.
    (B) Reflected power: 22-24 W
    (C) Wafers clear after 40-50 s of etching so 10-20 s of overetch

Etch recipes:

TANETCH.RCP

	Step 1	Step 2
CF_4 (sccm)	40	40
ECR (W)	0	300
RF (W)	0	25
Pressure (mT)	15	15
Time (s)	30	VAR

ETCHCLN.RCP

	Step 1	Step 2
O_2 (sccm)	15	15
He (sccm)	15	15
CF_4 (sccm)	40	40
ECR (W)	0	300
RF (W)	0	50
Pressure (mT)	15	15
Time (s)	30	VAR

16. S/D Implant
    Machine: Innovion
    Recipe: see below
    Notes: PMOS= BF_2,40 keV,$1x10^{15}$ cm^{-2}, 7 deg.
    NMOS= P, 25 keV, $1x10^{15}$ cm^{-2}, 7 deg.

17. Post Implant Clean
    Machine: TRL Photowet
    Recipe: IPA rinse
    Notes:

18. Ash- Gate
    Machine: TRL Asher
    Recipe: 1 hr. 15 min.
    Notes:

19. PECVD SiO_2- Interlevel Dielectric- 200 nm
    Machine: TRL STSCVD
    Recipe: HFSIO, 4 min. 20 s
    Notes:

    Recipe:
    Pressure (mT): 900
    Platen T (°C): 300
    Showerhead T (°C): 250
    N_2O (sccm): 1420
    N_2 (sccm): 392
    SIH_4 (sccm): 10
    RF: 30 W, 13.56 Mhz on showerhead only

20. S/D Implant Activation
    Machine: TRL RTA35, Tube B1
    Recipe: N_2 setpoint= 30, Emissivity= 55, TC control
    Notes: PMOS: 450 °C 8:1 N_2:H_2 30 min.
    NMOS: 500 °C N_2 60 s (GE500.RCP with Ge TC wafer)

21. Photo- Via
    Machine: TRL HMDS, Coater, and EV1
    Recipe: HMDS Setting 5, 4 s dispense, 4 KRPM 40 s, Expose 3.0 s, Develop 45 s
    Notes:

22. Etch- Via
    Machine: TRL Acidhood
    Recipe: 3:1 DI:BOE, 60 s
    Notes: Etch rate~ 50 Å/s

23. Etch- High-k Dielectric
    Machine: TRL Acidhood
    Recipe: 4:1 DI:HCL 2 min.
    Notes:

24. Ash- Via
    Machine: TRL Asher
    Recipe: 1 hr. 15 min.
    Notes:

25. Pre-metal Clean
    Machine: TRL Acidhood
    Recipe: 50:1 DI:HF 15s
    Notes:

26. Metallization- Frontside and Backside
    Machine: TRL Perkin Elmer
    Recipe: see below
    Notes: Frontside= 50 nm Ti/ 400 nm Al
    Backside= 50 nm Ti/ 2μm Al

27. Photo- Metal
    Machine: TRL HMDS, Coater, and EV1
    Recipe: HMDS Setting 5, 4 s dispense, 4 KRPM 40 s, Expose 3.0 s, Develop 45 s
    Notes:

28. Etch- Metal
    Machine: TRL Acidhood
    Recipe: Al Etchant 50 s followed by Ti Etchant 90s
    Notes: Al Etchant: 55 °C
    Ti Etchant: 1000:15 DI:BOE

29. Ash- Metal
    Machine: TRL Asher
    Recipe: 1 hr. 15 min.
    Notes:

Appendix B

Agilent 4294A IBASIC C-V Measurement Program

The IBASIC program listed below performs forward and reverse C-V sweeps at the frequency specified in line 50. The sweep start voltage is held for 1 s before starting the forward and reverse sweeps. The DC bias sweep range is specified in line 210.

```
10 DIM Buff$[9],Command$[9]
20 REAL Freq(1:4)
30 ASSIGN @Agt4294 TO 800
40!
50Freq(1)=50000
60!
70 PRINT "Input file name (without Extension)"
80 INPUT "Name?",Inp_char$
90 File$=UPC$(Inp_char$)
100 !
110 PRINT "Input measurement number"
120 INPUT "Number?",Inp_char2$
130 Num$=UPC$(Inp_char2$)
140 !
150 File1$=File$&Num$
160 !
170 OUTPUT @Agt4294;";MEAS CPD"
180 OUTPUT @Agt4294;";SPLD OFF"
190 OUTPUT @Agt4294;";ACCUD OFF"
200 OUTPUT @Agt4294;";ACCUD ON"
210 OUTPUT @Agt4294;";STAR -1;STOP 1"
220 ! Set hold time before sweep to 1s
230 OUTPUT @Agt4294;";SDELT 1"
240 OUTPUT @Agt4294;";TRGS INT"
250 !
260 ! Start Measurement
270 !
280 OUTPUT @Agt4294;";CWFREQ ";Freq(1)
290 OUTPUT @Agt4294;";SWED UP"
300 OUTPUT @Agt4294;";DCO ON"
310 OUTPUT @Agt4294;";SING"
320 !
```

```
330 ! Wait for measurement to finish
340 PRINT "Waiting..."
350 OUTPUT @Agt4294;"*OPC?"
360 ENTER @Agt4294;Buff$
370 PRINT "Sweep complete"
380 !
390 ! Write data to memory
400 OUTPUT @Agt4294;";DATMEM"
410 !
420 ! Prepare for next sweep
430 OUTPUT @Agt4294;";SWED DOWN"
440 OUTPUT @Agt4294;";SING"
450 !
460 ! Wait for measurement to finish
470 PRINT "Waiting..."
480 OUTPUT @Agt4294;"*OPC?"
490 ENTER @Agt4294;Buff$
500 PRINT "Sweep complete"
510 !
520 OUTPUT @Agt4294;";DCO OFF"
530 OUTPUT @Agt4294;";STOD DISK"
540 OUTPUT @Agt4294;";SAVDTRC ON"
550 OUTPUT @Agt4294;";SAVCAL OFF"
560 OUTPUT @Agt4294;";SAVDAT OFF"
570 OUTPUT @Agt4294;";SAVMEM OFF"
580 OUTPUT @Agt4294;";SAVMTRC ON"
590 Command$="SAVDASC"
600 OUTPUT @Agt4294;"*CLS"
610OUTPUT @Agt4294;Command$&" """&File1$&""""
620 !
630 !END
```

Appendix C

C-V Characteristics of $Al/Al_2O_3/AlN/Ge$ Capacitors

Experimental Description

Capacitors were fabricated on (100) Ga-doped p-type substrates with resistivity of 0.12-0.17 Ω-cm and (100) Sb-doped n-type substrates with resistivity of 0.13-0.16 Ω-cm. The wafers were cleaned using the modified RCA clean described in Appendix A. The dielectric stacks shown in Table C.1 were deposited on both n- and p-Ge followed by *ex-situ* Al sputtering (200 nm) on the frontside of the wafer and Ti/Au sputtering (50 nm/ 200 nm) on the backside of the wafer. The aluminum gate electrodes were patterned using photolithography and wet etching. Capacitors were then annealed as shown in Table C.2. In this document, Al_2O_3/AlN dielectric stacks are denoted by the number of Al_2O_3 cycles followed by the number of AlN cycles (e.g. 50/20).

ALD Run No.	Al_2O_3 cycles/AlN cycles
41	50/20
42	50/30
43	100/30
44	50/10

Table C.1: Dielectric stack splits for $Al/Al_2O_3/AlN/Ge$ capacitors. Stacks are defined by number of Al_2O_3 cycles and number of AlN cycles (Al_2O_3 cycles/ AlN cycles)

Temperature (°C)	Time (min.)	Ambient
no anneal	-	-
350	30	FG
350	30	N_2
400	1	N_2
500	1	N_2

Table C.2: Post-metal anneal splits for Al/Al_2O_3/AlN/Ge capacitors. FG= 8:1 N_2:H_2.

Electrical Results

Using these capacitors, the impact of AlN thickness was examined. Figure C.1 shows C-V characteristics for 50/10, 50/20, and 50/30 Al_2O_3/AlN stacks on p-Ge at 100 kHz and 1 MHz. The left column shows as-deposited characteristics while the right column shows the characteristics after 350 °C 30 min. forming gas (FG) annealing. In this work, the forming gas composition was 8:1 N_2:H_2. The forward sweep is from depletion to accumulation, and vice versa for the reverse sweep.

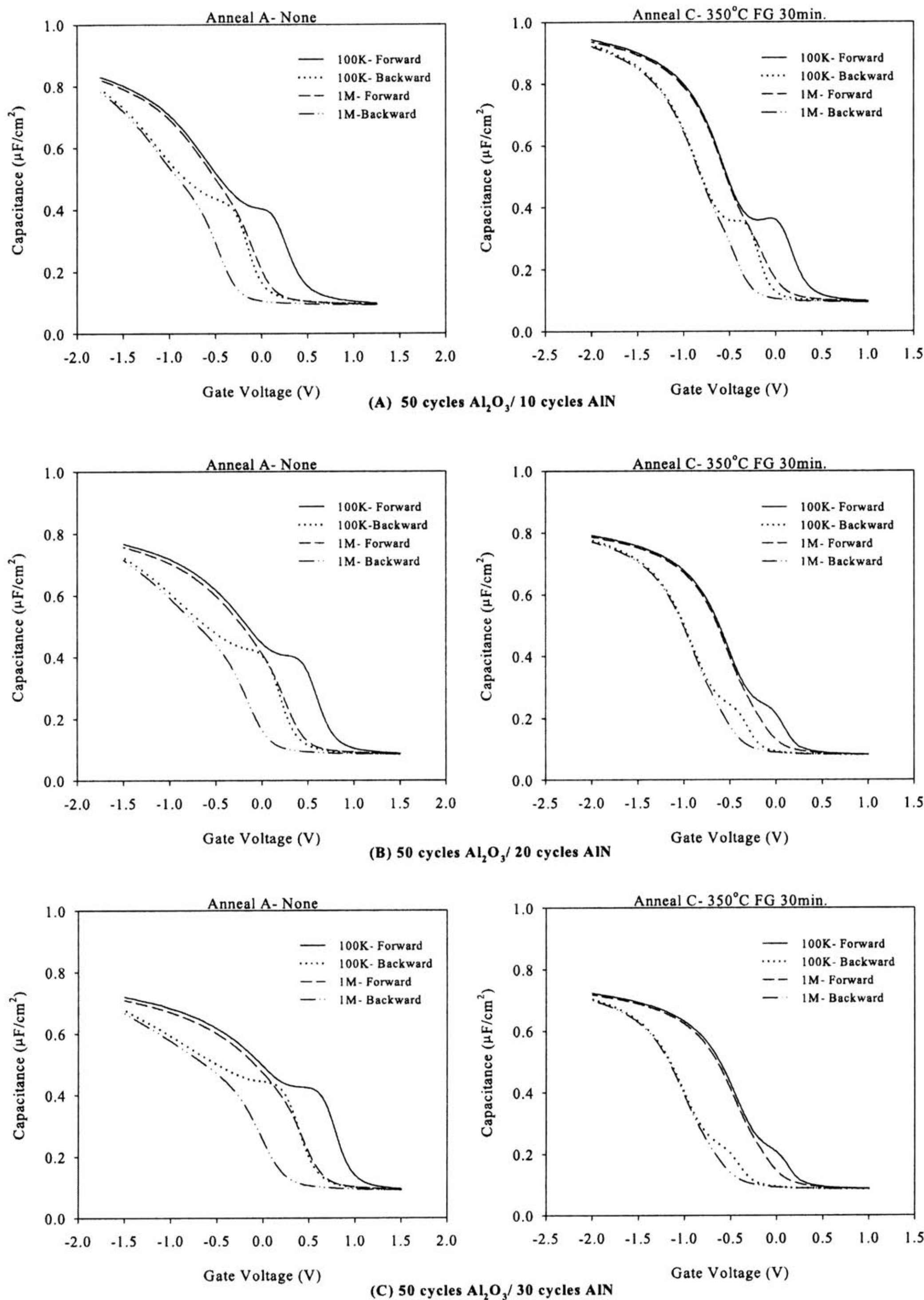


Figure C.1: C-V characteristics for (A) 50/10, (B) 50/20, and (C) 50/30 Al_2O_3/AlN stacks on p-Ge at 100 kHz and 1MHz. Left column shows as-deposited characteristics while right column shows characteristics after 350 °C 30 min. FG annealing.

Other than variation in peak capacitance due to varying AlN thickness, the as-deposited samples all exhibit similar behavior. The capacitance due to midgap interface states (C_{it}) features prominently in the as-deposited samples. For all three AlN interlayer thicknesses, post-metal annealing reduces interface state capacitance. Increasing AlN thickness, particularly from 10 to 20 cycles (approximately 1 nm to 2 nm), also reduces C_{it}; however, less improvement is seen for the 30 cycle AlN interlayer. Like Si_3N_4, AlN contains bulk traps that lead to C-V hysteresis [43]. As seen in Figure C.1, thicker AlN interlayers result in larger hysteresis in the PMA samples. Therefore, a trade-off between reduced C_{it} and increased hysteresis determines the optimal AlN thickness. From the data in Figure C.1, the optimal AlN thickness is 20 cycles or equivalently 2 nm.

The corresponding data for n-Ge is shown in Figure C.2. The trends are qualitatively similar to p-Ge; however, there are a few differences. The n-Ge C-V characteristics show more distortion near accumulation and also exhibit decreasing hysteresis during the reverse sweep. Both of these observations suggest a high density of interface states near the conduction band edge. Like p-Ge, the optimal AlN thickness for n-Ge is approximately 2 nm.

In addition to the 350 °C FG anneal, n and p-Ge capacitors were also annealed at 350 °C in N_2 (Table C.2). Figure C.3 shows the C-V characteristics for 50/20 n-Ge capacitors after nitrogen and forming gas annealing. The effect of anneal ambient on C-V characteristics was minimal. From this data, and the data presented in Chapter 2, it does not appear that hydrogen passivation plays the same role at germanium-dielectric interfaces that it does for Si-SiO_2 interfaces.

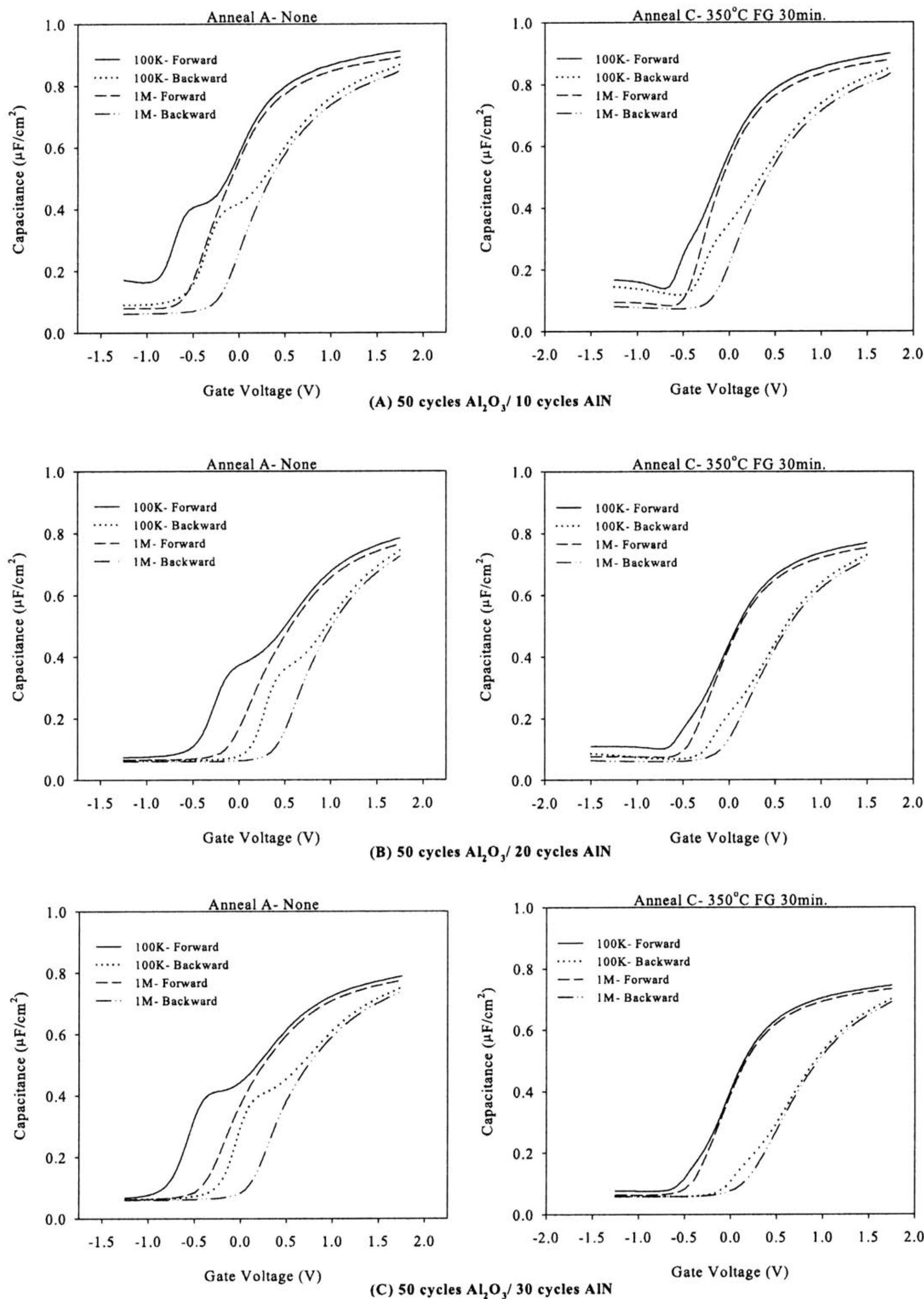


Figure C.2: C-V characteristics for (A) 50/10, (B) 50/20, and (C) 50/30 Al_2O_3/AlN stacks on n-Ge at 100 kHz and 1MHz. Left column shows as-deposited characteristics while right column shows characteristics after 350 °C 30 min. FG annealing.

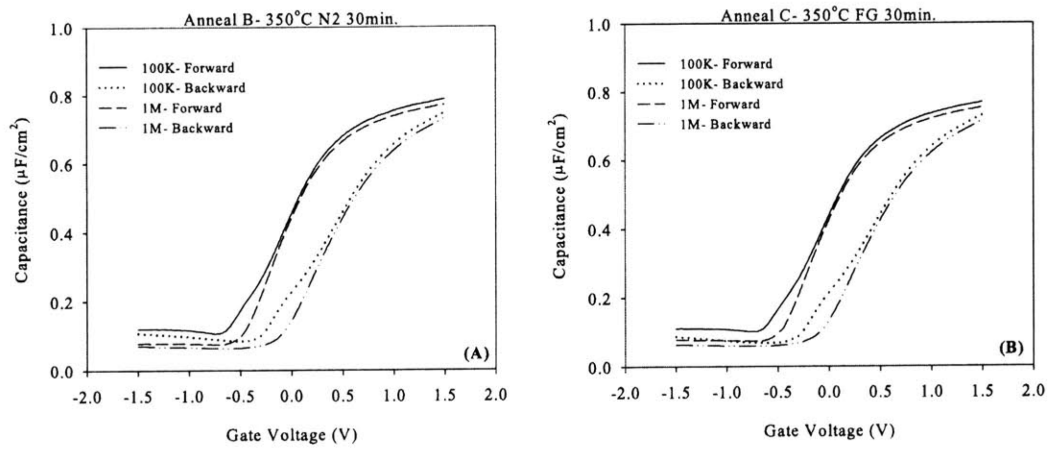


Figure C.3: C-V characteristics of 50/20 n-Ge capacitors after (A) nitrogen and (B) forming gas annealing at 350 °C for 30 min.

Appendix D

C-V Characteristics of $WN/Al_2O_3/AlN/Ge$ Capacitors

Experimental Description

Capacitors were fabricated on (100) Ga-doped p-type substrates with resistivity of 0.12 - 0.17 Ω-cm and (100) Sb-doped n-type substrates with resistivity of 0.13 to 0.16 Ω-cm. The wafers were cleaned using the modified RCA clean described in Appendix A. The $WN/(Al_2O_3,AlN)$ gate stacks shown in Table D.1 were deposited on both n- and p-Ge followed by *ex-situ* Al sputtering (250 nm) on the frontside of the wafer and Ti/Al sputtering (20 nm/ 1 μm) on the backside of the wafer. The aluminum metallization was patterned using photolithography and wet etching. Using the same resist mask, the WN gate electrode was etched using CF_4 RIE. The capacitors were then annealed as shown in Table D.2. The "as-deposited" samples did not receive a post-metal anneal but did receive the thermal budget associated with WN deposition (approximately 350 °C for 6 hrs. in N_2).

ALD Run No.	Al_2O_3 cycles/AlN cycles
104	45/15
105	35/25
111	60/00
113	00/60

Table D.1: Dielectric stack splits for $WN/(Al_2O_3, AlN)/Ge$ capacitors. Stacks are defined by number of Al_2O_3 cycles and number of AlN cycles (Al_2O_3 cycles/ AlN cycles).

Temperature (°C)	Time (min.)	Ambient
as-deposited	-	-
350	30	FG
400	1	N_2
450	30	FG
450	1	N_2
500	30	FG
500	1	N_2
550	30	FG
550	1	N_2

Table D.2: Post-metal anneal splits for WN/Al_2O_3/AlN/Ge capacitors. FG= 8:1 N_2:H_2.

Impact of Post-Metal Annealing on C-V Characteristics

Post-metal annealing is a critical step for high-k dielectrics, particularly ALD films deposited at low temperature (200 °C), that is used to improve the electrical properties of as-deposited gate stacks. However, degradation of germanium-dielectric interfaces has also been observed during subsequent thermal processing. The purpose of this experiment was to determine the optimal anneal and also investigate the thermal stability of these gate stacks at n-type S/D activation temperatures (500- 550 °C).

WN/45 cycle Al_2O_3/15 cycle AlN/Ge (45/15) and WN/35 cycle Al_2O_3/25 cycle AlN/Ge (35/25) capacitors were subjected to the post-metal annealing conditions listed in Table D.2. Figures D.1 and D.2 show the effect of 450 °C and 550 °C annealing in both N_2 and forming gas (FG) for p-Ge capacitors with 45/15 (Figure D.1) and 35/25 (Figure D.2) gate stacks. The corresponding data for 45/15 and 35/25 n-Ge capacitors is shown in Figures D.3 and D.4.

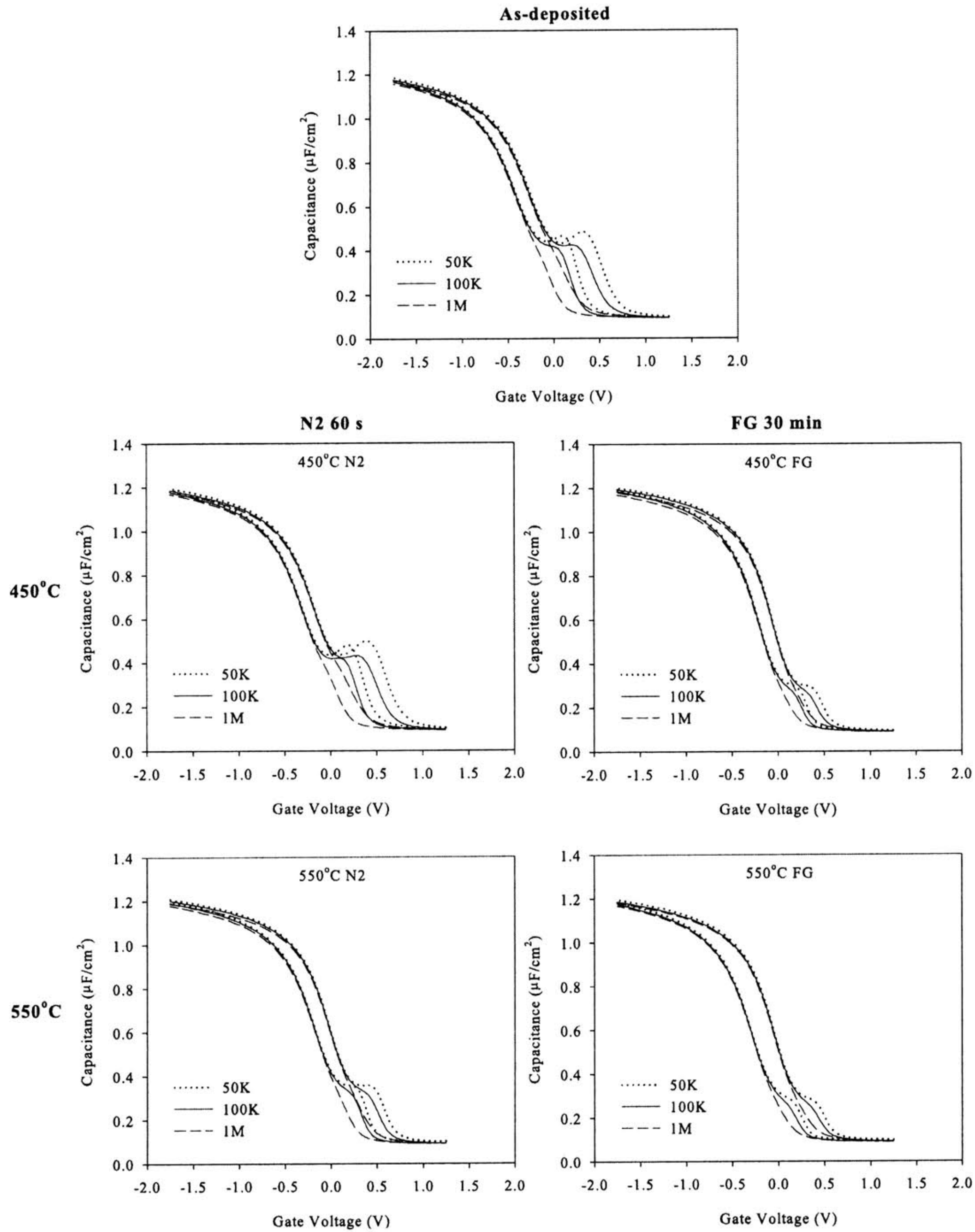


Figure D.1: Impact of PMA on C-V characteristics of WN/45 cycle Al_2O_3/15 cycle AlN/ p-Ge capacitors. From top to bottom, characteristics from as-deposited, 450 °C, and 550 °C samples are shown. Left column shows characteristics from 60 s N_2 anneal while right column shows 30 min. FG anneal.

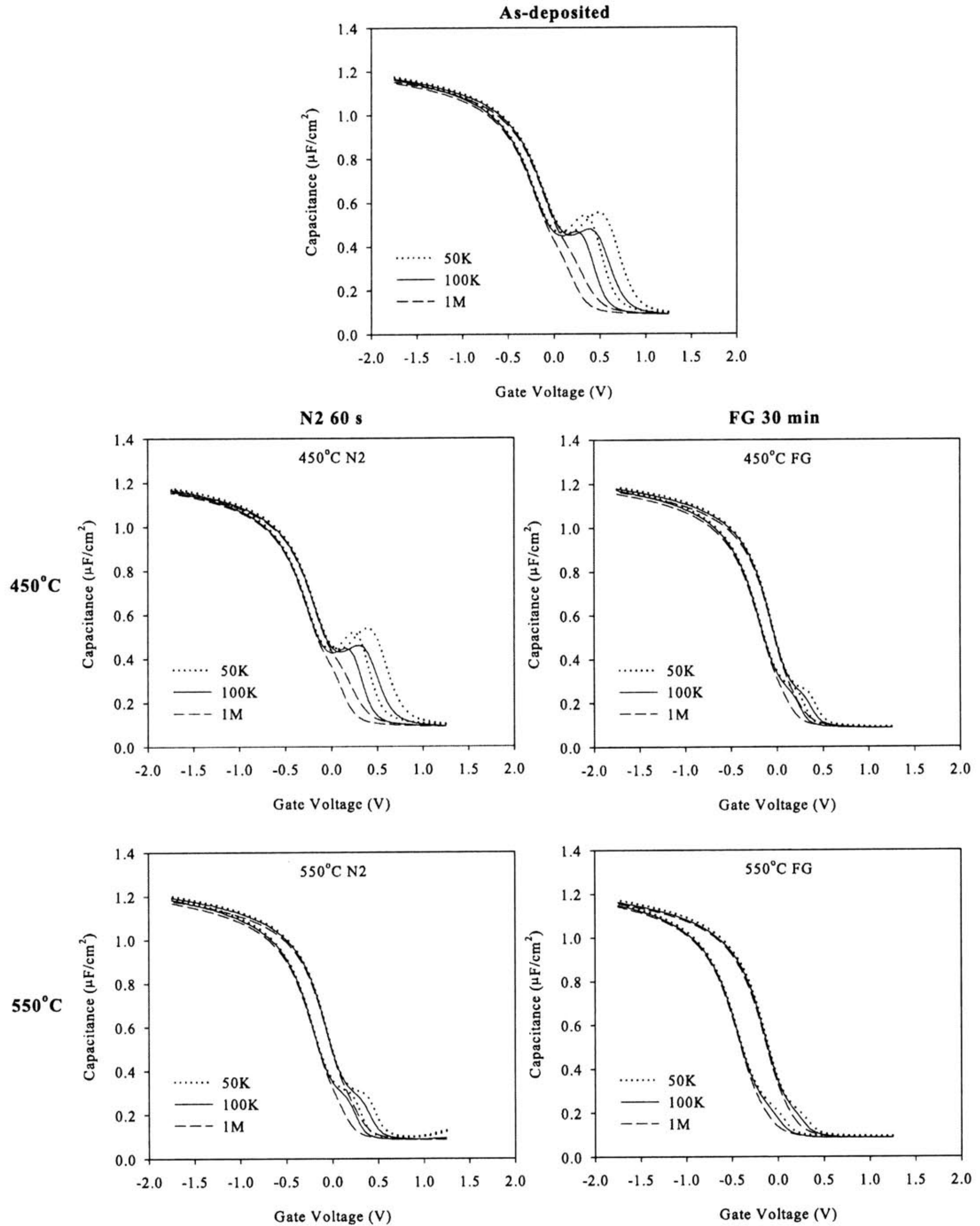


Figure D.2: Impact of PMA on C-V characteristics of WN/35 cycle Al_2O_3/25 cycle AlN/ p-Ge capacitors. From top to bottom, characteristics from as-deposited, 450 °C, and 550 °C samples are shown. Left column shows characteristics from 60 s N_2 anneal while right column shows 30 min. FG anneal.

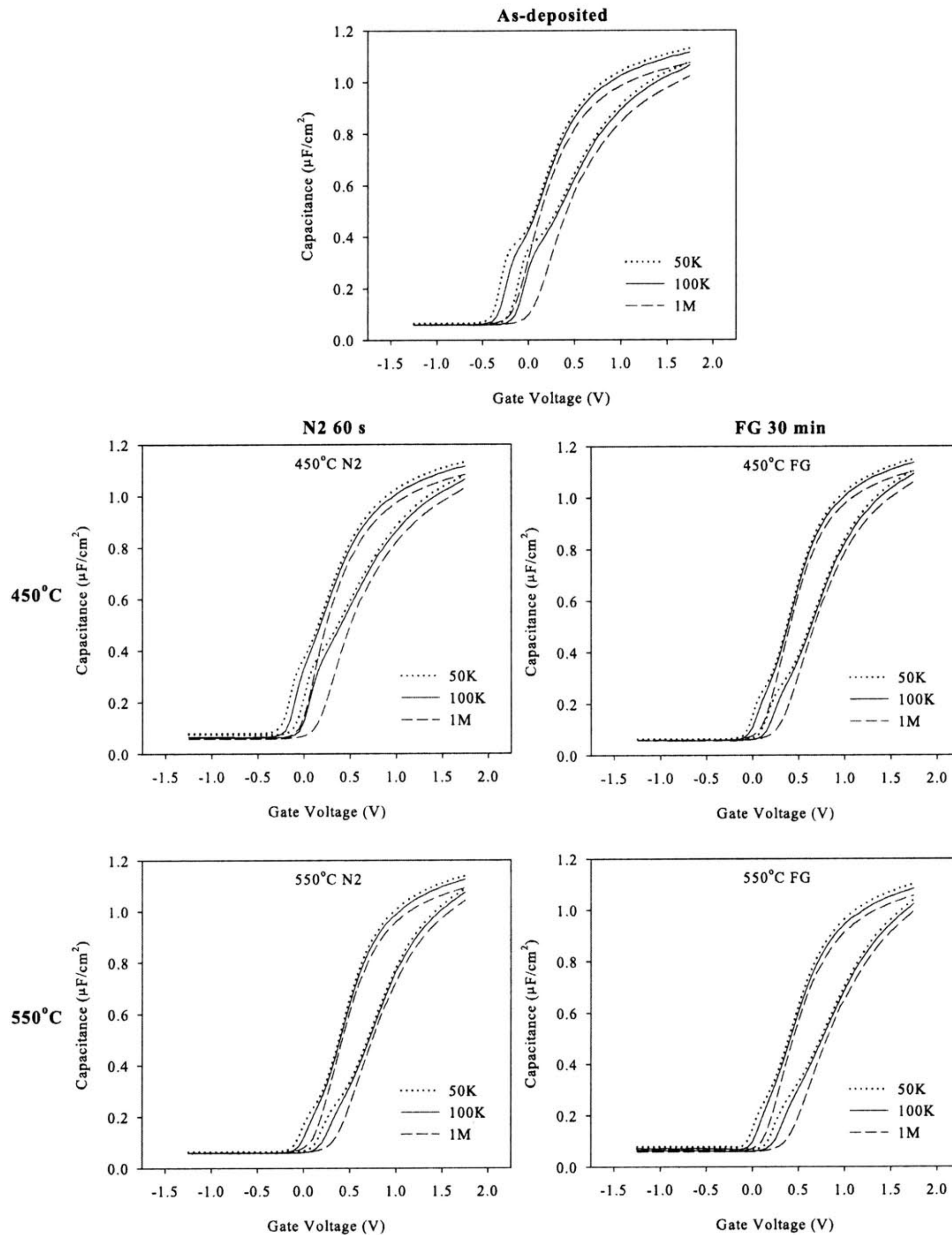


Figure D.3: Impact of PMA on C-V characteristics of WN/45 cycle Al_2O_3/15 cycle AlN/ n-Ge capacitors. From top to bottom, characteristics from as-deposited, 450 °C, and 550 °C samples are shown. Left column shows characteristics from 60 s N_2 anneal while right column shows 30 min. FG anneal.

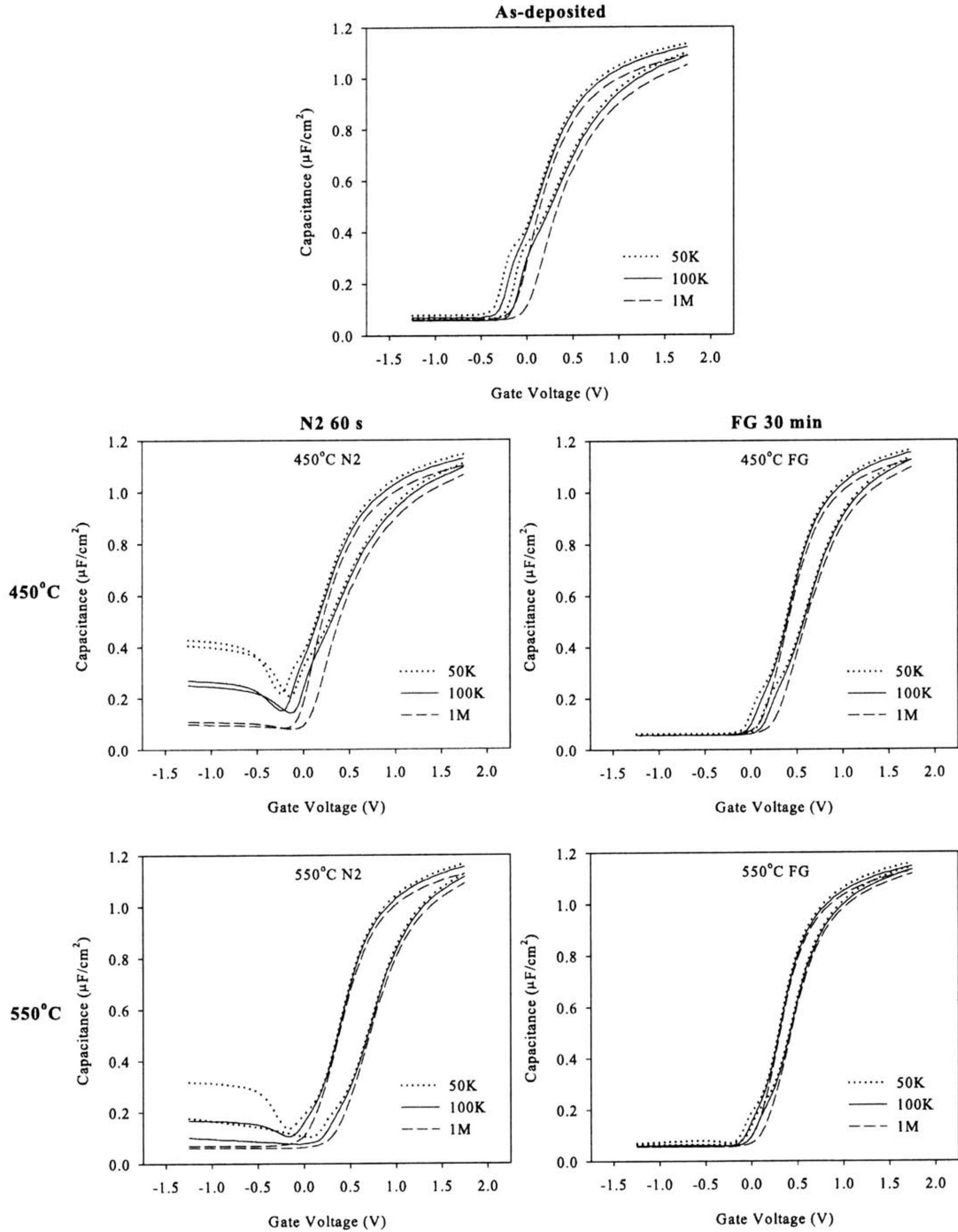


Figure D.4: Impact of PMA on C-V characteristics of WN/35 cycle Al_2O_3/25 cycle AlN/ n-Ge capacitors. From top to bottom, characteristics from as-deposited, 450 °C, and 550 °C samples are shown. Left column shows characteristics from 60 s N_2 anneal while right column shows 30 min. FG anneal.

Appendix E

C-V Characteristics of $WN/GdScO_3/Hf_3N_4/Ge$ Capacitors

Experimental Description

In addition to AlN, Hf_3N_4 interlayers were also explored through a collaboration with Harvard University [41]. ALD Hf_3N_4 layers were deposited using tetrakis-(ethylmethylamido)hafnium (TEMA-Hf) and NH_3 as reactants. The TEMA-Hf bubbler temperature was 80 °C and the substrate temperature was 200- 250 °C. ALD $GdScO_3$ was used as the dielectric capping layer and ALD WN was used as the gate electrode, both deposited *in-situ*. In general, MOS capacitors with Hf_3N_4 behaved similarly to those with AlN. Figure E.1 shows measured quasistatic and high frequency C-V characteristics for a WN/8 nm $GdScO_3$/1.5 nm Hf_3N_4 /p-Ge capacitor [41]. Interface state density was extracted using both the quasistatic and conductance methods. Figure E.2 shows the resulting D_{it} distribution [41]. Midgap D_{it} for this gate stack was approximately $1x10^{12}$ cm^{-2} eV^{-1} which is slightly lower than the value obtained for AlN interfacial layers.

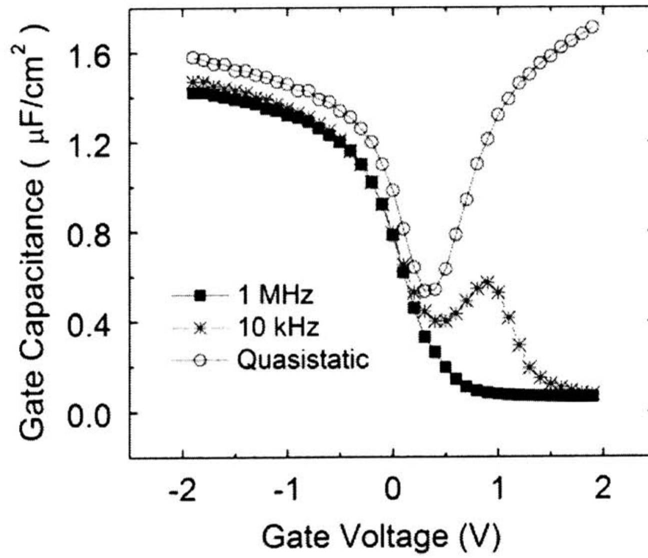


Figure E.1: Quasistatic, 10 kHz, and 1 MHz C-V characteristics for WN/8 nm $GdScO_3$/ 1.5 nm Hf_3N_4 /p-Ge capacitor (from [41]).

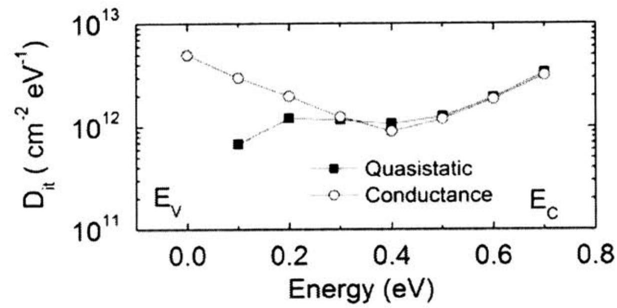


Figure E.2: D_{it} extracted using both the conductance and quasistatic methods [59] for a WN/8 nm $GdScO_3$/1.4 nm Hf_3N_4/p-Ge capacitor (from [41]).

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