RELIABILITY OF COPPER INTERCONNECTS IN INTEGRATED CIRCUITS

by

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B.S. Materials Science and Engineering
Cornell University, 2000

Submitted to the Department of Materials Science and Engineering in Partial Fulfillment of the Requirements for the Degree of

DOCTOR OF PHILOSOPHY

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2007

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To Jungsuk Han, Myounghee Lee and Hyunjoon Cho
Whose prayers led me to complete this work

ABSTRACT

As dimensions shrink and current densities increase, the reliability of metal interconnects becomes a serious concern. In copper interconnects, the dominant diffusion path is along the interface between the copper and the top passivation layer (usually Si_3N_4). One of the predominant failure mechanisms in Cu has been open-circuit failure due to electromigration-induced void nucleation and growth near the cathode ends of interconnect segments. However, results from accelerated electromigration tests show that the simple failure analyses based on simple void nucleation and growth can not explain the wide range of times-to-failure that are observed, suggesting that other types of failure mechanisms are present. In this thesis, by devising and performing unique experiments through the development of an electromigration simulation tool, unexpected complex failure mechanisms have been identified that have significant effects on the reliability of copper interconnects.

A simulation tool was developed by implementing the one-dimensional non-linear differential equation model first described by Korhonen *et al.* By applying an implicit method (Backward Euler method), the calculation time was significantly reduced, and stability increased, compared to previous tools based on explicit methods (Forward Euler method). The tool was crosschecked with experimental results by comparing void growth rates in simulations and experiments. Using this tool, one can simulate stress and atomic concentration states over the entire length of an interconnect segment or throughout a multi-segment interconnect tree, to identify analyze possible failure locations and mechanisms.

Experiments were carried out on dotted-i structures, where two 25μm-lomg segments were connected by a via in the middle. Electrical currents were applied to the two segments independently, and lifetime effects of adjacent segments were determined. Using the simulation tool and calculations, it was shown that adjacent segments have a significant effect on a segment's stress state, even if the adjacent segment has no electrical current. This explains experimental observations. This also suggests that for reliability analyses to be accurate, the states of all adjacent segments must be considered, including the ones without electrical current.

In a second set of experiments, the importance of pre-existing voids was investigated. Using in-situ scanning electron microscopy, voids away from the cathode were observed. These voids grew and drifted toward the cathode and the shape of the voids were found to be closely related to the texture and stress state of individual grains in the interconnect. The drift velocity of voids was shown to be directly proportional to

surface diffusivity. Electromigration tests on unpassivated samples were performed under vacuum to obtain the surface diffusivity of copper and its dependence on texture orientations.

Simulation results show that pre-existing voids cause void growth away from the cathode. Subsequent failure mechanisms differ depending on the location of the pre-existing void and the critical void volume for de-pinning from grain boundaries. If pre-existing voids are present, void-growth-limited failure is expected in interconnects at low current densities, due to growth of pre-existing void, and the lifetimes are expected to scale inversely with j. However, at higher current densities (typical for accelerated testing), failure can occur through nucleation of new voids at the cathode (so that lifetimes scale inversely with j^2), or through a mixture of nucleation of new voids and growth of pre-existing voids. These effects must be taken into account to accurately project the reliability of interconnects under service conditions, based on experiments carried out under accelerated conditions.

Acknowledgements

I have been blessed with numerous people that I have known during the course of my Ph.D. work at MIT. There is no doubt that this thesis could not have been completed without them.

I first would like to thank Prof. Thompson. He has been a great advisor. There is no question that his intellectual insights were critical to this thesis, but I also like to thank him for shaping my presentation, writing, and communication skills.

I thank the committee members of my thesis, Prof. Allen and Prof. Fitzgerald for their helpful discussion and comments.

The research in this thesis was supported by the Semiconductor Research Corporation, Intel Corp., and AMD. Most of the samples were provided by Sematech Inc. Fabrication work was done at Microsystems Technology Laboratories (MTL) at MIT and I would especially like to thank Kurt Broderick for his help with all the equipments.

Most of sample characterization and analysis was done at Center for Nanoscale Systems (CNS) at Harvard. I especially like to thank David Lange and Richard Schalek. I also thank Rowland Institute at Harvard and Michael Burns for letting me to use their SEM and providing me with necessary components to do in-situ experiment.

I thank Reiner Mönig for his excellent advices on designing and building test equipments that could not have been done correctly without him. I thank Junghoon Lee for helping me to construct xSim, the simulation tool. I thank the EM colleagues, Frank Wei, Cheelip Gan, Choonwai Chang, Prof. Pey, and Prof. Choi for their helpful discussions and some EM runs and failure analysis. Colleagues in Prof. Thompson's group have been great; discussions, helps, hangouts, lunches, etc.

My friends at MIT/Boston; Jihun, Woosik, Wonjoon, Byungwoo, Kwan, Jason, etc. And my friends around the globe; Saejin, Andrew, Mune, Suk, Andy, Dongwoo, Hojun, Sheeyoung, Kijoon, Q, Minsik, etc. I would like to thank them for removing my stresses and teaching me all the fun stuffs.

My deepest thanks to my family – grandmother, mother, uncles, aunts, brother and cousins. Lastly, I thank God for giving me a chance to meet all these great people. Amen.

Table of Contents

	Page
Figure and Table Captions	xi
Chapter 1: Introduction	1
1.1 Advances in Semiconductor Industry	2
1.1.1 Moore's Law	
1.1.2 Technical Challenges in Back-End Technology	
1.1.3 Challenges in Reducing RC Delay	
1.2 Failures by Electromigration	4
1.2.1 Fundamentals of Electromigration	
1.2.2 Back Stress Effect	
1.2.3 Steady State with Force Balances	
1.2.4 Compressive Stress/Extrusion Failures	
1.2.5 Tensile Stress/Voiding Failures	
1.2.6 Black's Equation	
1.3 Aluminum Interconnect Technology	14
1.3.1 Advantages of Al	
1.3.2 Fabrication Processes	
1.3.3 Electromigration in Al	
1.3.4 Improvements in Al Interconnect Reliability	
1.3.5 Reliability of Al Interconnect Trees	
1.4 Copper Interconnect Technology	24
1.4.1 Advantages and Disadvantages of Cu	
1.4.2 Cu Interconnect Fabrication	
1.4.3 Electromigration in Cu Interconnects	
1.4.4 Improvements in Cu Interconnect Reliability	
1.4.5 Voids in M1 and M2 of Cu Interconnects and Their Roles in Reliability	
1.4.6 Liners	
1.4.7 The Reliability of Cu Interconnect Trees	
1.5 Scope of the Thesis	32
Chapter 2: Numerical Simulation Tool for Observing Atomic Concentration and stress in Metal Interconnect During Electromigration	37

2.1 Introduction 39
2.2 Simulation Approach 42
2.2.1 Atom Conservation
2.2.2 The Finite Volume Method for Spatial Discretization
2.2.3 Time Integration
2.3 Numerical Experiments 51
2.4 Simulation Tool Capabilities 54
2.4.1 Simulation of Stress Evolution in Interconnect Trees
2.4.2 Void Nucleation/Growth, Pre-existing Voids
2.4.3 Diffusivity Variations Along the Interconnect
2.5 Conclusion 59

Chapter 3: Fatal Void Size Comparison in Via-Below and Via-Above Copper Dual-Damascene Interconnects 63

3.1 Introduction 65
3.2 Numerical Simulation 70
3.3 Analysis and Discussion 70
3.3.1 Analysis with Simulation
3.3.2 Comparison Between Simulated and Experimental Results
3.4 Conclusion 77
3.5 Acknowledgements 79

Chapter 4: Electromigration Resistance in a Short Three-Contact Interconnect Tree 81

4.1 Introduction 82
4.2 Experiments 85
4.3 Experimental Results 87
4.4 Discussion 93
4.4.1 Active and Passive Reservoirs
4.4.2 Failures at Low $(jL)_{eff}$ with Inactive Segment
4.4.3 Accounting for the Effects of Inactive Segment
4.4.4 Failures at Low $(jL)_{eff}$ with Liner Failure
4.4.5 Unexpected Failures
4.5 Conclusions 102

4.6 Acknowledgement 102
4.7 Appendices for Chapter 4 103
4.7.1 Maximum Stress at Steady State
4.7.2 Maximum Void Length at Steady State

Chapter 5: Effects of Texture on the Formation, Shape, and Motion of Voids During Electromigration in Passivated Copper Interconnects 108

5.1 Introduction 109
5.2 Experimental Procedure 111
5.2.1 Test Structure
5.2.2 Thinning Passivation
5.2.3 In-Situ SEM
5.2.4 EBSD
5.3 Results 115
5.3.1 Void Drifting in 1.0μm and 2.25μm Width Samples
5.3.2 Void Drifting in 0.3μm Width Samples
5.3.3 Void Drift Velocity
5.3.4 Grain Orientation Dependence on Voids
5.3.5 Void Elongation and Residues
5.4 Discussion 128
5.4.1 Failure by Voids Away from Cathode
5.4.2 Effect of Grains on Void Growth
5.4.3 Effect of Grains on Void Drift
5.4.4 Effect of Grains on Void Shape
5.4.5 Width Dependence on Void Drift Velocity
5.4.6 Difference in Grain Orientation Before and After Void Drift
5.4.7 Criteria for Void Growth Away from the Cathode
5.5 Conclusion 137

Chapter 6a: Activation Energy and Pre-Factor of Surface Electromigration in Copper interconnects 143

6a.1 Introduction 144
6a.2 Experimental Procedures 147

6a.3 Results and Discussion 148
6a.4 Conclusion 154

Chapter 6b: Dependence of the Electromigration Flux on the Crystallographic Orientation of Different Grains in Polycrystalline Copper Interconnects 157

6b.1 Introduction 158
6b.2 Experimental Procedures 160
6b.3 Results and Discussion 161
6b.3.1 Voids in Flux Divergence Sites
6b.3.2 Relative Diffusivities in Different Grain Orientations
6b.4 Conclusion 169

Chapter 7: Void Dynamics in Copper-Based Interconnects 171

7.1 Introduction 173
7.2 Modeling and Simulation 181
7.3 Results 184
7.3.1 Conditions for Void Nucleation at Grain Boundaries
7.3.2 Effects of Pre-Existing Voids
7.3.2.1 Void Nucleation at the Cathode
7.3.2.2 Void Growth Near the Anode Via
7.3.2.3 Void Growth Far from the Vias
7.3.2.4 Void Growth Near the Cathode Via
7.4 Discussion and Conclusions 200
7.5 Summary 205

Chapter 8: Conclusions and Future Works 208

8.1 Summary 209
8.1.1 xSim
8.1.2 Effect of Adjacent Segments
8.1.3 Dynamics of Voids Away from the Cathode
8.1.3.1 Accelerated EM Tests with In-Situ SEM
8.1.3.2 Vacuum EM Tests

8.1.3.3 Effect of the Stress State Around a Pre-Existing Void
8.1.4 Effect of Pre-Existing Voids on Current Density Exponent
8.1.4.1 Low Current Density
8.1.4.2 High Current Density
8.2 Conclusions 216
8.3 Proposed Future Works 217

Appendix A: Monolayer on Unpassivated Copper Interconnect Surface for Reducing Diffusion 220

A.1 Introduction 221
A.2 Experimental Procedures 222
A.3 Results 223
A.4 Discussion 225
A.5 Conclusion 228

Appendix B: Setup for Vacuum Electromigration Station 231

Appendix C: Manual for Running xSim 237

FIGURE AND TABLE CAPTIONS

Chapter 1

Figure 1.1 Schematic diagram of interconnects in first **(a)** and second **(b)** metallization. Stress gradient ($\partial\sigma/\partial x$) opposes e- force.

Figure 1.2 Stress profile with time increments along the length (20μm) of the interconnect with electrons flowing left to right. Note that void is forced not to nucleate. Magnitudes of maximum tensile stress at cathode end and maximum compressive stress at anode end are identical at steady state.

Figure 1.3 Stress profile with time increments along the length (20μm) of the interconnect with electrons flowing left to right. Void nucleates once stress reaches 40MPa. Steady state is reached with stress at cathode end fixed at zero.

Figure 1.4 Atomic concentration with time at the cathode end of the interconnect. The rate of change decreases as the steady state is reached. The size of the void can be calculated by subtracting the value in this graph from the initial concentration state.

Figure 1.5 Aluminum fabrication process. **(a)** Al and shunt layer are deposited using PVD. **(b)** Metals are patterned and etched with RIE. **(c)** Dielectric material is deposited with CVD. **(d)** CMP dielectric material **(e)** Dielectric material is patterned and etched with RIE. **(f)** Via material is filled for next metallization.

Figure 1.6 (a) Void nucleating at grain boundary site, **(b)** Void spans through thickness and width of the interconnect to cause failure by high resistance.

Figure 1.7 (a) Polycrystalline Al **(b)** Polycrystalline Al with large grains **(c)** Bamboo Al.

Figure 1.8 (a) Schematic of Al interconnect tree **(b)** Separating interconnect tree into individual segments for reliability estimation.

Figure 1.9 Copper fabrication process. **(a)** ILD is patterned and etched with RIE. **(b)**

Diffusion barrier layer and Cu seed layer is sputter deposited. **(c)** Cu is electroplated **(d)** Over-burden Cu is polished with CMP, and diffusion barrier passivation layer is deposited.

Figure 1.10 Void nucleation site in Cu interconnect. Void nucleates at the Cu/Si_3N_4 interface near cathode end.

Chapter 2

Figure 2.1 Sketch of an interconnect segment: **a)** side view, **b)** top view.

Figure 2.2 Discretization of an interconnect segment into individual cells. The stress and atom concentration is tracked for each cell. The atomic flux between cells is calculated by using a staggered grid system, which can be envisioned as corresponding to cell boundaries.

Figure 2.3 Stress profile with Δt larger than the stability limit in forward-Euler method (low-order explicit method). Notice that the stress profile shows random behavior. Simulations conditions : 50 cells of 1.0μm length, total length = 50μm, j = 2.5MA/cm^2, T = 623K, D = 4.5x10^{-16} m^2/s.

Figure 2.4 Calculation time comparison for explicit-based and implicit-based methods. Simulations conditions: **(a)** 100 cells of 1.0μm length, total length = 100μm, j = 2.5MA/cm^2, T = 623K, D = 4.5x10^{-16} m^2/s; **(b)** 200 cells of 1.0μm length, total length = 200μm, j = 2.5MA/cm^2, T = 623K, D = 4.5x10^{-16} m^2/s. **(c)** is the close up region of (b).

Figure 2.5 Schematic diagram of an interconnect tree where two segments are connected with a via in the middle. Current density (j) of the left segment is fixed while j in the right segment is varied. T=350°C, j_L=0, ±0.5, ±1.5, ±2.5 (MA/cm^2), two 25μm segments for total 50μm in length. Detailed analysis is in chapter 4.

Figure 2.6 Stress evolution before and after nucleation of a void at the cathode. **(a)** Stress profiles at 1 hour intervals of simulated time. A void nucleates when the stress reaches the critical value σ_{crit}=40MPa. **(b)** Concentration vs. time in the first cell where the void nucleates. Note that there is a sudden increase in the rate of depletion of atoms

when void nucleation occurs, due to the sudden change in the stress gradient, both in magnitude and sign. Simulation conditions: 50 cells of 1.0μm length, total length = 50μm, j = 0.5MA/cm^2, T = 623K.

Figure 2.7 Stress profiles at 1 hour intervals of simulated times for an interconnect segment with a pre-existing void 5μm away from the cathode. **(b)** Volume of pre-existing void vs. time. Simulation conditions: 50 cells of 1.0μm length, total length = 50μm, j = 0.5MA/cm^2, T = 623K.

Figure 2.8 Stress profiles at 1 hour intervals of simulated time for an interconnect segment with diffusivity variations of the type expected in polycrystalline segments. Note that the diffusivity effect decreases as the stress approaches a steady state. Simulation conditions: 30 cells of 1.0μm length, total length = 30μm, j = 0.5MA/cm^2, T = 623K, D varied between $0.5D_{eff}$ to $2D_{eff}$.

Chapter 3

Figure 3.1 Schematic diagram of M1 and M2 structures.

Figure 3.2 Preferential void nucleation and growth at the Cu/Si_3N_4 interface in **(a)** M1 and **(b)** M2 structures.

Figure 3.3 The number of atoms removed from a void nucleation site vs. time in **(a)** 50μm, **(b)** 100μm, and **(c)** 800μm lines, as determined through simulations.

Figure 3.4 (a) M2 L=800μm, w=0.28μm, current terminated after 312 hours.
(b) M2 L=800μm, w=1.00μm, current terminated after 55 hours.
(c) M1 L=100μm, w=0.28μm, current terminated after 192 hours.

Figure 3.5 f=atomic flux **(a)** Void nucleation and growth away from the cathode in M2. **(b)** Void nucleation and growth at the end of the cathode in M2.

Figure 3.6 (a) Cathode of M2 interconnect, L = 800μm, w = 0.28μm, STTF at j = 2.5MA/cm^2. **(b)** Cathode of M2 interconnect, L = 100μm, w = 0.28μm, STTF at j = 2.5MA/cm^2.

Table 3.I t_{50}'s and STTFs The widths of all lines are 0.28μm; All lines are single via terminated; the thickness of M1 is 0.34μm and of M2 is 0.24μm. All tests were done at T = 350 °C Assumed failure when resistance increases more than 30% of the initial resistance [Gan 2001]. j=current density, L=length

Table 3.II number of removed atoms and void volumes j=current density, N=number of atoms removed, V=void volume, L=length of the interconnect

Table 3.III void volume comparisons The error range of measured void volumes is within 0.4 $x10^{-20}$ m^3. V_{Ex}/V_{Sim} corresponds to ratio of the voids between experiment and simulation.

Chapter 4

Figure 4.1 (a) Top and **(b)** cross-sectional view of the dotted-I test structure. The arrows indicate the directions of the electron flow.

Figure 4.2 (a) Plot of the percentages of samples in which the right segment failed, as a function of the current density in the left segment, j_L. **(b)** Plot of the percentage of the samples that failed with failure occurring first in the left or right segments, or with failure occurring simultaneously in both segments.

Figure 4.3 SEM images for the voids formed in the right segments either **(a)** at the cathode or **(b)** at region close to the central via, though the left segments had higher current densities. The arrows indicate the directions of electron flow.

Figure 4.4 TEM image of the central via for the failed sample where j_L = -0.5 MA/cm^2.

Figure 4.5 SEM image for the large volume void in the left segment for j_L = -1.5 MA/cm^2 where the right segment first failed.

Figure 4.6 (a) SEM image of a failure site near the central via in the right segment for j_L = -1.5 MA/cm^2. The arrows indicate the directions of the electron flow. **(b)** SEM image of the trace of metal extrusion at the Cu/Si_3N_4 interface parallel to the test line. The arrows indicate the extruded metal with clear dielectric cracks, while the dashed-circle is the erupted failure site in (a). The M2 test line is not visible as it had been over-cut.

Figure 4.7 Plot of the overall failure percentage of the tested structures for tests carried out under conditions leading to different values of $(jL)_{eff}$. Absolute immortality was obtained from 10μm-segment dotted-I with [0 ←0.5 MA/cm^2] test configuration.

Figure 4.8 Simulated stress evolution for various test.

Figure 4.9 Schematic illustration of the balanced stress distribution with and without a passive segment for the cases **(a)** when void nucleation does not occur (the peak tensile stress is higher when there is a passive reservoir) and **(b)** when void growth saturates (the void length at saturation is larger when there is a passive reservoir).

Table 4.I Percentages of the 50μm-long dotted-I (25μm segment) that failed, for individual segments and for the overall structure. The arrows indicate the electron flow directions. R denotes the right segment and L the left segment. Also shown are the percentage of the failures that occurred first in the right or left segments, and the percentage of the samples that failed simultaneously in both the right and left segments.

Table 4.II Failure percentages for the 20μm-long dotted-I (10μm segment).

Chapter 5

Figure 5.1 Si_3N_4 passivation layer thinning process using focused ion beam (FIB). Thinning process enables to see Cu/Si_3N_4 interface more clearly using SEM.

Figure 5.2(a) In-situ SEM images of the voids from the top view with out of plane orientation of the tested samples and resistance during the test. The width of the test structure is 0.3μm.

Figure 5.2(b) In-situ SEM images of the voids from the top view with out of plane orientation of the tested samples and resistance during the test. The width of the test structure is 0.3μm.

Figure 5.2(c) In-situ SEM images of the voids from the top view with out of plane orientation of the tested samples and resistance during the test. Width of the test structure is 1.0μm.

Figure 5.2(d) In-situ SEM images of the voids from the top view with out of plane orientation of the tested samples and resistance during the test. Width of the test structure is 1.0μm.

Figure 5.2(e) In-situ SEM images of the voids from the top view with out of plane orientation of the tested samples and resistance during the test. Width of the test structure is 2.25μm.

Figure 5.3 Void drift velocities at various line widths. Average drift velocities are 3.31nm/min (0.3μm), 7.62nm/min (1.0μm), and 46.22nm/min (2.25μm).

Figure 5.4 Shape of the void drifting in a single grain region is well maintained until the void reaches to the different grain.

Figure 5.5 (a) First void passing through a circled region of the grain and **(b)** second void passing through a circled region of the grain. Cathode edge of the second void has the same shape as the grain, but the shape of the first void is different, suggesting that the grain has changed in the circled region after the first void drifted.

Figure 5.6 (a) First void passing through a circled region of the grain and **(b)** second void passing through a circled region of the grain. Both cathode edges of first and second void have similar angle, suggesting that the grain in that region has not changed.

Figure 5.7 Length of the void vs. location of the void for the voids that nucleated away from the cathode. 1.0μm width samples.

Figure 5.8 Void residues are observed that are left behind by the first void.

Figure 5.9 A cartoon shows the case in which void may nucleate and grow. e- is electrons, and blue arrow indicates the direction of electrons. The void is at a grain boundary, between grain a and b where diffusivity of Cu/Si_3N_4 passivation interface in grain a ($D_{int(SiN)\_a}$) is larger than that of grain b ($D_{int(SiN)\_b}$). Thick red arrow in grain a indicates large atomic flux and thinner red arrow in grain b indicates smaller atomic flux.

Figure 5.10 A cartoon shows the case in which void drifts in a single grain. D_s is the surface diffusivity of the exposed surface at the void, which is much larger than interface diffusivity ($D_{int(SiN)}$) around the void, as indicated by the thickness of the red arrow. The overall direction of the void drift, then, is against the direction of the electrons, shown by black arrow.

Figure 5.11 A cartoon shows the case in which the existing or incoming void shrinks and possibly disappears. Similarly as in Figure 5.9, void is between grain a and b, but in this case, $D_{int(SiN)\_a}$ is lower than $D\text{-}_{int(SiN)\_b}$, leading to smaller outgoing flux from the void, than the incoming flux to the void.

Table 5.I Summary of Experimental Results

Table 5.II Out of plane crystallographic orientations of grains at anode and cathode edges of the void as voids nucleate away from the cathode end of the interconnect.

Chapter 6a

Figure 6a.1 Surface z*D at Various Temperatures.

Figure 6.2 Average Surface z*D at Various Temperatures.

Figure 6.3 $(z^*D)_s$ of three different values. Note that z^* for Bradshaw was set to 1 [Hu 1999].

Table 6a.I Reported E_s and D_o values obtained experimentally. Note that values obtained through EM test (first four rows) are $(z^*D)_s$ rather than D_s.

Table 6a.II Average void drift velocity obtained from in-situ EM testing [Choi Ch.5] and drift velocity obtained by using surface diffusivity. $T = 370^{o}C$, $j = 3.0MA/cm^2$.

Chapter 6b

Figure 6b.1 One of immobile voids in the middle of the line, anode edge of the void has faster diffusivity than the cathode edge of the void.

Figure 6b.2 Inverse pole figures of the cathode edge **(a)** and anode edge **(b)** of the immobile voids in the tested samples.

Figure 6b.3(a) Inverse pole figure of the untested sample with 0.3μm width, 1000μm length. Circled regions show (1 1 1) and its first (1 1 5) and second (7 5 13), (11 1 11) twin orientations.

Figure 6b.3(b) Mackenzie plot of randomly oriented sample (gray) versus untested sample (red).

Table 6b.I Volume fractions of orientations within 9^{o} of (1 1 1), its first and second generation twins, and the rest of the orientation of untested sample.

Table 6b.II Number of grains observed in cathode and anode edges of the voids, within 9^{o} of (1 1 1), its first and second generation twins, and the rest of the orientation of untested sample.

Table 6b.III Number of grain orientation pairs in each individual voids.

Chapter 7

Figure 7.1 Voids in an interconnect segment terminating in a cathode via *below* the segment. **(a)** Voids most readily nucleate at the Cu-cap interface, and grow at the site where the electromigration-induced tensile stress is highest. **(b)** Voids are sometimes

observed at the base of vias, where they may have nucleated or where they may have drifted from other locations. Voids are sometimes observed at locations other than directly at the cathode via. These voids can drift toward the via **(c)** or grow in place **(d)** to cause failure.

Figure 7.2 Voids in an interconnect segment terminating in a cathode via *above* the test segment. **(a)** Voids most readily nucleate at the Cu-cap interface, and grow where the electromigration-induced tensile stress is highest. Voids are sometimes observed at locations other than directly at the cathode via. These voids can drift toward **(b)** the via or grow in place **(c)** to cause failure.

Figure 7.3 **(a)** Void nucleation and growth at boundaries is favored when the atomic interfac diffusivity at the Cu-cap interface of the cathode-side grain is lower than the diffusivity of the anode-side grain. **(b)** Once voids have grown to a critical size they can de-pin from boundaries and drift toward the cathode. The drift rate is determined by the magnitude of the diffusivity on the surface of the void relative to the interface diffusivity.

Figure 7.4 Stress-profiles along a 50μm-long line after four 100-minute steps and after the last step at 10000min., when the evolution stops due to a balance of the electron wind force and the back stress (j=0.5MA/cm^2, T=350°C, σ_{nuc}=40MPa). **(a)** uniform diffusivity of D_0=4.5x10-16m^2/s throughout the line. **(b)** diffusivities of either $D_0/2$, D_0, or $2D_0$ randomly assigned to 50 1μm-long grains (so that the average diffusivity is D_0.

Figure 7.5 Stress profiles after 2-minute intervals, with a 2μm-long grain 20μm away from the cathode via with a diffusivity of $100D_0$ (with a diffusivity of D_0 everywhere else along the line). (j=0.5MA/cm^2, T=350°C, σ_{nuc}=40MPa) Notice that the cathode edge of the grain quickly reaches a local maximum stress that is initially higher than the stress at the cathode via, but that the stress at the cathode via eventually exceeds this local maximum stress.

Figure 7.6 Stress profiles after four 2 minute intervals for an interconnect segment with a 5μm-long cluster of grains with a high diffusivity, with the diffusivity elsewhere set at D_0. (j=3.0MA/cm^2, T=350°C, σ_{nuc}=40MPa.) The high-diffusivity grain cluster is 3μm away from cathode via in the 50μm-long interconnect segment. The diffusivity in the

high-diffusivity cluster is $11D_0$ in **(a)** and $5D_0$ in **(b)**. The tensile stress reaches σ_{nuc} (40MPa) first at the cathode edge of the cluster in (a) and first at the cathode via in (b).

Figure 7.7 Stress profiles at the cathode end of an interconnect segment after five 1-minute time intervals with a pre-existing void **(a)** 5μm and **(b)** 2μm away from the cathode via. ($j=3.0MA/cm^2$, $T=370^oC$, $\sigma_{nuc}=40MPa$) In case (a) the stress at the cathode via reaches σ_{nuc} and the stress in the region between the void and the cathode via quickly relaxes to zero. In case (b) the stress stops evolving when a force balance develops, and a void does not nucleate at the cathode via.

Figure 7.8 (a) Stress profiles after five 1-minute. intervals at the anode end of an interconnect segment with a pre-existing void 5μm away from the anode. **(b)** Change in void volume of a pre-existing void as a function of time for voids at different distances La from the anode via. (Segment length = 1000μm, $j=3.0MA/cm^2$, $T=370^oC$, $D=D_0$ everywhere a long the segment.)

Figure 7.9 Change in the volume with time for a pre-existing void in the middle of a 50μm-long interconnect segment. The grain on the anode side of the void is 0.6μm long , with a diffusivity varied from $D_0/2$ to $2D_0$, while all other regions have diffusivity D_0 ($j = 3.0MA/cm^2$, $T = 370^oC$).

Figure 7.10 Change in void volume as a function of time for pre-existing voids at different distances from the cathode via L_c ($j = 3.0MA/cm^2$, $T = 370^oC$, $\sigma_{nuc}=40MPa$, $D=D_0$ everywhere). **(a)** When $L_c>L_{c,cr}$, void growth saturates. **(b)** Only when $L_c<L_{c,cr}$ do voids continue to grow.

Figure 7.11 Change in the volume with time of a pre-existing void 2mm away from cathode via with an anode-side 0.6μm-long grain with diffusivities $D_0/2$, D_0, and $2D_0$, with the diffusivity set to D_0 everywhere else ($j = 3.0MA/cm^2$, $T = 370^oC$).

Table 7.1 Parameters used for simulations.

Chapter 8

Figure 8.1 (a) Unpassivated test structure with strips of passivation of desired material.

(b) Assuming surface diffusion is higher than the interface diffusion, voids will grow at the edges of the passivation.

Appendix A

Figure a.1 TTF of unpassivated and monolayer deposited samples. **(a)** 0.3μm width and **(b)** 1.0μm width samples.

Figure a.2 Monolayer deposited samples after EM tests. **(a)** shows precipitate-like spots in extrusion monitor righ and test line. **(b)** Region showing nanowire growth **(c)** Region with clean surface.

Figure a.3 (a) Thiol group of diacetylene adheres to Cu surface. **(b)** UV light turns triple bonds in diacetylene to cross-linked double bonds with other molecules.

Figure a.4 Other monolayer candidates:
(a) COOH terminated of diacetylene
(b) Mercaptopropyltrimethoxylsilane
(c) Aminopropyltriethoxylsilane

Table a.I MTTF of samples with different monolayers. *Note that a.4(a), a.4(b), and a.4(c) are monolayers described in figure a.4; very limited number of samples are tested.

Appendix B

Figure b.1(a) A schematic diagram of vacuum electromigration test chamber setup.

Figure b.1(b) A photograph of actual vacuum electromigration test chamber.

Figure b.2 A photograph of actual socket with wires, ceramic package, and halogen lamp heater.

Figure b.3 Transistor regulates current by difference in resistance of the potentiometer.

Figure b.4 It can be controlled with a accuracy with variable resistance in the configuration shown in the left.

CHAPTER 1

INTRODUCTION

1.1 ADVANCES IN SEMICONDUCTOR INDUSTRY

1.1.1 Moore's Law

Since the introduction of Intel 4004 4-bit central processing unit (CPU) in 1971, microprocessors have become an essential part of living. Microprocessors are used in virtually all electronics that people use, from sophisticated state-of-the-art supercomputers to everyday gadgets such as cell phones and personal MP3 players. Because of benefits that microprocessors have provided, pursuit of improving capability and speed have been at the center of electronics industry's interest. Following Moore's Law, the density of the transistors in a microprocessor has been doubling about every 2 years, now counting about 600 million transistors in a single chip as of 2007 [Moore 1971]. Moreover, the switching speed of transistors is also steadily rising to decrease computational time, where the clock speed is over 3.0GHz as of 2006. There have been many technical challenges to attempts to increase transistor density and the switching speed.

1.1.2 Technical Challenges in Back-End Technology

Some of these challenges arise from concerns with metal interconnects, which are fabricated late, or in the 'back-end', of the microprocessor fabrication process.

Interconnects in a microprocessor are electrically conductive wires that connect transistors to transistors or other parts of the system. These metal interconnects in the back-end are surrounded by inter-level dielectric (ILD) layers to prevent electrical shorts and to provide mechanical stability for the wiring. In order to keep up with increasing transistor density, the total length of interconnects and the current density in a single interconnect structure need to increase and the spacing between interconnects (metal 1 wiring pitch) needs to decrease. Currently, as of 2007, the total interconnect length in a microprocessor is over 1.2km/cm^2, with the smallest width interconnects reaching 150nm, and the current density as high as 1.37x10^{6}A/cm^2 [ITRS]. With longer total length and higher current density, ensuring interconnect reliability becomes more challenging.

1.1.3 Challenges in Reducing RC Delay

With increasing interconnect length, delay associated with the interconnect and the ILD becomes a more serious concern, as the resistance-capacitance (RC) delay time starts to exceed the gate delay time for CMOS, leading to an overall increase in calculation time [ITRS]. From the 1960's to the mid 1990's, the materials for the interconnect and ILD remained the same, aluminum (Al) and SiO_2, respectively.

However, both the resistance of the interconnect and the dielectric constant of the ILD need to decrease in order to minimize RC delay.

For lowering the dielectric constant of the ILD, a broad range of research is being conducted using various low-k materials, such as doped SiO_2, polymers, porous materials and air gaps [Ho 2003] [Hu 1998a]. Beyond manufacturability, the primary concern is the reliability of low-k dielectric materials, both electrically and mechanically. It has been observed that as the dielectric constant decreases, young's modulus and rigidity also decrease, resulting in easy mechanical failure of the dielectric, which can lead to electrical shorts by extrusion of interconnect material [S.Hau-Riege 2000b].

To reduce resistance, lower resistance Cu is replacing Al. Due to intrinsic differences between Al and Cu, significant changes have been made in terms of fabrication processes as well as reliability analysis.

1.2 FAILURES BY ELECTROMIGRATION

1.2.1 Fundamentals of Electromigration

One of the main reliability issues for metal interconnects is due to a phenomenon called electromigration (EM). Electromigration occurs when electrical current is applied to a electrically conductive material; electrons transfer momentum to

the conductor atoms and cause the atoms to drift in the direction of the electron 'wind' (opposite to the direction of current). The atomic flux, J_a, due to the electron current in a one dimensional system is given by: [Lloyd 1999]

$$J_a = -\frac{D_{eff} C_a}{kT} Eq^* = -\frac{D_{eff} C_a}{kT} j\rho z^*_{eff} e \quad , \tag{1.1}$$

where D_{eff} is the effective diffusivity of conductor atoms in the interconnect, C_a is atomic concentration, E is the electric field that drives the current, q* is the effective charge, k is Boltzmann's constant, and T is the temperature. The electric field can be written as the product of the resistivity, ρ, and the current density, j. Effective charge can also be written as the product of the effective charge number, z^*_{eff}, and the electron charge, e.

1.2.2 Back Stress Effect

Interconnects in an actual device are usually fully surrounded and confined by ILD, and vias block the diffusion of atoms between interconnects. In this confined interconnect, electromigration causes atoms to accumulate at the anode which leads to

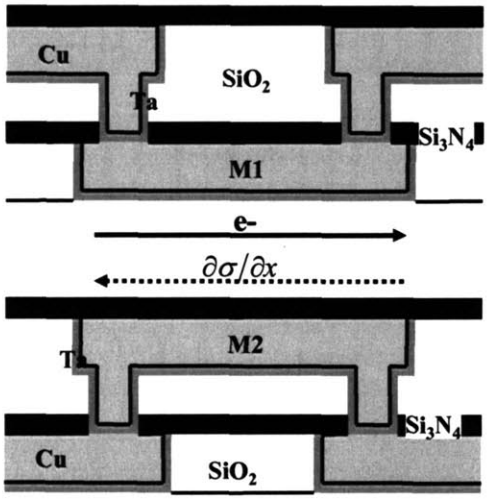

Figure 1.1 Schematic diagram of interconnects in first **(a)** and second **(b)** metallization. Stress gradient ($\partial\sigma/\partial x$) opposes e- force.

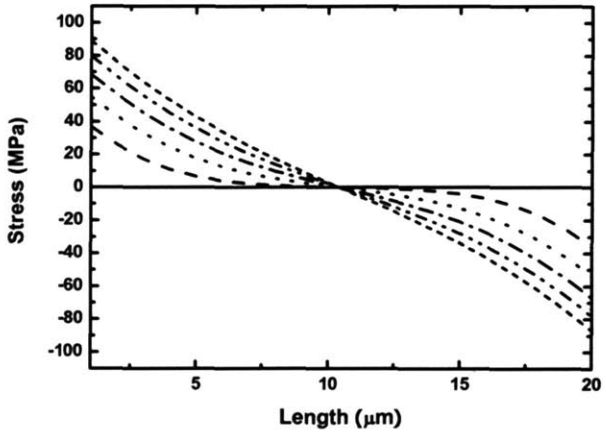

Figure 1.2 Stress profile with time increments along the length (20μm) of the interconnect with electrons flowing left to right. Magnitudes of maximum tensile stress at cathode end and maximum compressive stress at anode end are identical at steady state.

compressive stress and deplete from the cathode which leads to tensile stress (Figures 1.1, 1.2) [Blech 1976]. The net atomic flux is also affected by the magnitude of the stress gradient that opposes the electron wind force. The atomic flux and stress gradient relationship is given as: [Clement 1995]

$$J_a = \frac{D_{eff} C_a}{kT} \Omega \frac{\partial \sigma}{\partial x}, \tag{1.2}$$

where Ω is the atomic volume and $\partial\sigma/\partial x$ is the stress gradient along the length of the interconnect. Putting Eq. 1.1 and Eq. 1.2 into one equation,

$$J_a = -\frac{D_{eff} C_a}{kT} \left(j \rho z^*_{eff} e - \Omega \frac{\partial \sigma}{\partial x} \right). \tag{1.3}$$

Thus, typically in interconnects the atomic flux is dominated by two types of driving forces, electron wind force and the 'back-stress' force due to the stress gradient. Stress is also related to the atomic concentration through an effective modulus, B, by: [Korhonen 1993]

$$\sigma = -B \ln\left(\frac{C_a}{C_{ao}}\right), \tag{1.4}$$

where C_{ao} is the atomic concentration at zero stress. Figure 1.2 shows the stress evolution in a one-dimensional (1D) interconnect at given time intervals. This plot was generated using an electromigration simulation tool developed by Zung-Sun Choi and Jung Hoon Lee called xSIM, which will be described in Chapter 2.

1.2.3 Steady State with Force Balances

At early times, the magnitude of the stress gradient, which is the slope of the line in the figure 1.2, is maximum at both ends of the interconnect, and the magnitude decreases with increasing distance away from both ends. However, the stress gradient becomes more uniform as time elapses, and the stress state of the interconnect eventually comes to a steady state with a linear stress gradient along the length of the interconnect. At steady state, the force due to the stress gradient balances the electron wind force [Blech 1976]. This leads to net atomic flux of zero. The magnitude of the stress gradient at steady state is:

$$\frac{\partial \sigma}{\partial x} = -\frac{j\rho z_{eff}^{*} e}{\Omega}. \qquad (1.5)$$

Also, at steady state, both the compressive and tensile stresses at the ends of the interconnect are at their maximum, where the maximum magnitude of the stress is given as:

$$\sigma_{\max} = \frac{j\rho z_{eff}^{*} e}{2\Omega} L, \qquad (1.6)$$

where L is the length of the interconnect. According to equation (1.6), σ_{max} varies with j and L, but it is independent of both the diffusivity and temperature.

1.2.4 Compressive Stress/Extrusion Failures

Many failures of interconnects are related to the development of stress. A compressive stress at the anode can cause extrusion of atoms from the interconnect when the liner and passivation layer mechanically fail. Atoms may diffuse or extrude through the ILD and bridge to other isolated interconnects; causing electrical shorts between interconnects. Failure due to extrusion, therefore, is closely related to the mechanical characteristics of surrounding ILD, liner, and passivation layer materials

[Morgen 2000] [C.Hau-Riege 2004]. The materials industry is seeking with lower dielectric constants to reduce RC delay usually exhibit lower Young's moduli and toughness, which can reduce the compressive stress required to cause an extrusion failure. The maximum compressive stress occurs at the end of the anode, which means that failure due to extrusion is more probable near the anode. Thus, it is important to consider ILDs with low dielectric constants that also have a relatively small loss in mechanical strength.

1.2.5 Tensile Stress/Voiding Failures

Another type of failure occurs at the cathode. Electromigration leads to a tensile stress at the cathode, and if the tensile stress reaches a certain critical stress σ_{crit}, a void nucleates [Rosenberg 1971] [Korhonen 1993] (σ_{crit} for Al: [Greenebaum 1991] [Park 1999], for Cu: [S. Hau-Riege 2002] [C. Hau-Riege 2002]). Similarly to the anode end where the maximum compressive stress is obtained, the maximum tensile stress occurs at the cathode end [Blech 1976]. Thus, it is most likely to observe voids close to the end of the cathode. After the void nucleates, the stress around the void quickly drops to zero by releasing energy and creating a free surface on the void, and the tensile stress region gradually relaxes as shown in figure 1.3, with stress at the void

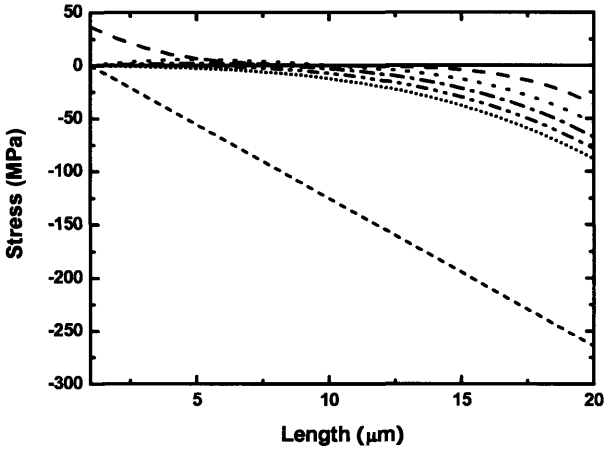

Figure 1.3 Stress profile with time increments along the length (20μm) of the interconnect with electrons flowing left to right. Void nucleates once stress reaches 40MPa. Steady state is reached with stress at cathode end fixed at zero.

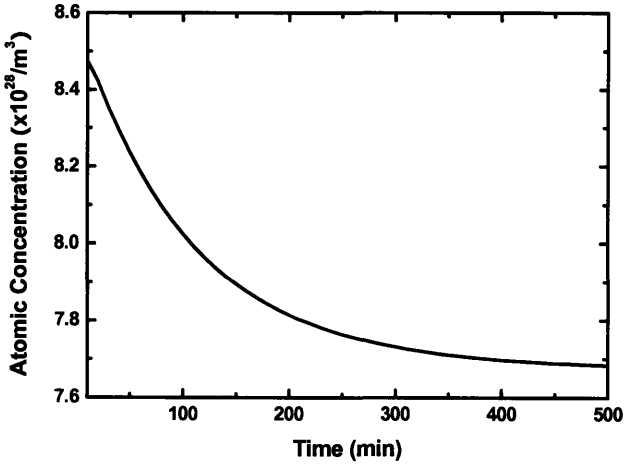

Figure 1.4 Atomic concentration with time at the cathode end of the interconnect. The rate of change decreases as the steady state is reached. The size of the void can be calculated by subtracting the value in this graph from the initial concentration state.

fixed at zero. A different steady state is reached with a void present. If the same magnitude of current density is applied, the difference in stresses between the cathode and anode ends of the interconnect with the void at the cathode end is identical to that of the interconnect without a void, because in both cases the magnitude of the stress gradient at steady state is the same. However, in the interconnect without a void, magnitudes of tensile and compressive stresses at each are equal (but opposite, assuming an initial stress state of zero) at steady state, whereas in the interconnect with a void, the stress is zero at the cathode end and the magnitude of the compressive stress at the anode end is twice the magnitude of the compressive stress at the anode of the interconnect without a void.

After the void nucleates near the cathode end, it grows until the interconnect reaches steady state, because the net atomic flux prior to achieving the steady state always depletes atoms from the cathode. The rate of depletion decreases as it reaches the steady state, which leads to a decrease in the void growth rate (Figure 1.4). Thus, the maximum void volume is obtained at steady state.

Depending on the location of void nucleation, failure can occur in the interconnect at any time during the void growth. The failure can occur almost immediately after the time taken to nucleate a void in a specific location, or failure may

never occur if the maximum void volume at steady state does not span the width and thickness of the interconnect or if current can shunt around the void through the conductive liner. Criteria for these cases are described in chapter 3.

1.2.6 Black's Equation

Because the failure types and times even at identical test conditions may be different, several tens of identical samples or more are tested under the same accelerated conditions, with temperature and current density used to accelerate EM-induced failure, to obtain statistical results. Failure times (times-to-failure; TTFs) are fit to a distribution function (mostly either lognormal or Weibull distribution function). The temperature and current density dependence of the median time to failure, t_{50}, can then be analyzed using Black's empirical equation [Black 1967]:

$$t_{50} = Aj^{-n} \exp\left(\frac{Q}{kT}\right), \tag{1.7}$$

where A is a constant, Q is the activation energy, and n is the current density exponent factor (n). With A, Q, and n obtained from accelerated EM tests, Black's equation can be used to extrapolate failure times of interconnects in actual operating conditions in

integrated circuit. The exponent factor n is observed to range roughly from 1 to 2. It has been demonstrated to have a value close to 1 for failures occurring due to void growth (void-growth-limited failure), and close to 2 for failure occurring due to void nucleation at specific locations (void-nucleation-limited failure) [Lloyd 1991] [Park 1999] [Andleigh 1999].

However, it is possible to have both void-growth and nucleation-limited failures in a single set of nominally identical samples under identical test conditions. Furthermore, there may be other kinetic processes that affect n, such as void drift and pinning. All failure mechanisms are therefore represented in the obtained current density exponent and activation energy determined through the process described above. It has also been demonstrated that under some circumstances, the exponent factor is different between operating condition and accelerated EM testing conditions [Andleigh 1998]. These problems can lead to extrapolations that can be different by orders of magnitude compared to actual behavior in real operating conditions. Therefore, an improved fundamental understanding of different failure mechanisms of interconnects is needed in order to ensure accurate predictions of the lifetimes interconnects.

1.3 ALUMINUM INTERCONNECT TECHNOLOGY

1.3.1 Advantages of Al

From 1960's until relatively recently, aluminum (Al) was the metal chosen for interconnects [Wolf 1990]. Al has several advantages over other materials for interconnect materials.

First, Al has a relatively low electrical resistivity compared to most other metals. Its resistivity is 2.65μΩ-cm at room temperature. Second, Al does not contaminate silicon-based devices in the same way that metals such as gold and copper do, which diffuse rapidly into Si and form intermediate states in a silicon bandgap to cause a reduction in the minority carrier lifetime and a degradation of device performance. Therefore, Al can be deposited and handled with other silicon-based device fabrication tools without concern with contamination problems. Third, Al adheres very well to dielectrics, giving it mechanical stability. Fourth, Al forms an ohmic contact with Si. Fifth, Al forms a very stable self-passivating oxide layer where the oxide acts as a diffusion barrier layer which prevents Al atoms from diffusing into the ILD. Lastly, it has a well-developed fabrication processes that has proven to be manufacturable and cost effective [Luce 1992].

1.3.2 Fabrication Processes

Figure 1.5 shows the fabrication process for Al-based interconnects in integrated circuits [Licata 1995]. Al and barrier layers are deposited using a physical vapor deposition (PVD) tool, generally a sputter deposition system. The Al films are polycrystalline in the as-deposited state (Figure 1.5(a)). Materials used for shunt layers are typically refractory metals or compounds, such as Ti, TiN, and TiW. The overlayer was introduced as an anti-reflection coating that was later found to provide electromigration resistance. The underlayer was initially included as a nucleation layer for W in the vias, and then also found to help suppress electromigration. (Note that there were never layers on the side of the Al).

These shunt-layer materials were chosen for the following characteristics: [Ramkumar 1993]

1. Not react excessively with Al so the interconnect resistance does not increase too much.
2. Resist electromigration.
3. Easily dry-etched along with Al.
4. Have deposition process that is compatible with other IC fabrication processes.
5. Have low stress.
6. Adhere well to both ILD/Si and Al.

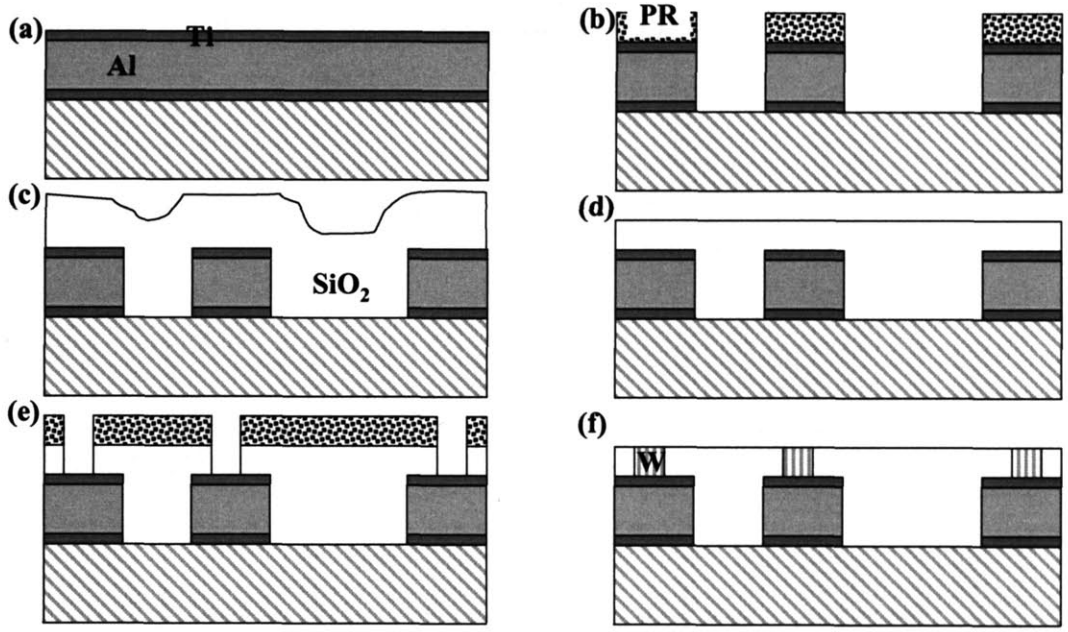

Figure 1.5 Aluminum fabrication process. **(a)** Al and shunt layer are deposited using PVD. **(b)** Metals are patterned and etched with RIE. **(c)** Dielectric material is deposited with CVD. **(d)** CMP dielectric material **(e)** Dielectric material is patterned and etched with RIE. **(f)** Via material is filled for next metallization.

After the film deposition, photolithography is used to pattern the film into appropriate dimensions for interconnects and is etched using reactive ion etching (RIE) (Figure 1.5(b)). The fabricated Al interconnect is then encapsulated by a dielectric material such as SiO_2 using plasma-enhanced a chemical vapor deposition (PECVD) tool, and planarized by chemical mechanical polishing (CMP) (Figure 1.5(c), (d)). Again using photolithography and RIE, vias are made and filled with tungsten (via CVD) to connect

Al interconnects in different layers of metallization (Figure 1.5(e), (f)).

1.3.3 Electromigration in Al

One of the drawbacks for use of Al for interconnection is its relatively poor resistance to electromigration due to the relativity high self-diffusivity of Al atoms. Improving reliability with respect to electromigration has been the central theme for research on Al interconnects for the past few decades. In Al interconnects, there are several diffusion paths: bulk (lattice), grain boundary (gb), and interfaces (Al/Al_2O_3, Al/SiO_2, Al/barriers, and Al/W). The effective diffusivity and effective charge product, $(z^*D)_{eff}$, of the interconnect has contributions from all possible diffusion paths, and can be described as: [Hu 1998]

$$\left(z^* D\right)_{eff} = z_B^* D_B (1 - \sum F_f) + \sum F_m z_m^* D_{fm} \quad , \qquad (1.8)$$

where the subscripts B and f refer to bulk and fast diffusion paths, respectively, and F_m is the fraction of atoms diffusing along the *m*th fast-diffusion path. For a thin film Al interconnect, the possible fast-diffusion paths could be along grain boundaries and interfaces. Assuming that the contribution from bulk diffusion is negligible, then

equation (1.8) can be simplified to:

$$\left(z^{*}D\right)_{eff} = \left(\frac{\delta_{gb}}{d}\right) z^{*}_{gb} D_{gb} + \left(\frac{2\delta_{is}}{h}\right) z^{*}_{is} D_{is} + \left(\frac{2\delta_{iILD}}{w}\right) z^{*}_{iILD} D_{iILD}, \qquad (1.9)$$

where the subscripts gb, is, and iILD refer to grain boundary, top and bottom interfaces between Al and the shunt/barrier layer, and side interfaces between Al and the ILD, respectively. δ is the grain boundary or interface width, d is grain size, w is interconnect width, and h is interconnect thickness.

It has been observed that the dominant diffusion path in wide Al interconnects is along grain boundaries [Vaidya 1980]. Not only do grain boundaries provide the fastest diffusion path, they also provide the most probable sites for the nucleation of voids. Voids nucleate and grow at grain boundaries [Borgesen 1992] (Figure 1.6). Thus, a grain boundary near the cathode end of an interconnect is the most likely location for void nucleation. It has been found that σ_{crit} for Al is about 400MPa [Greenebaum 1991] [Park 1999]. The nucleated void can grow to span the width and the thickness of the interconnect, forcing electron current to shunt through higher resistive barrier layers (Figure 1.6(b)). With the electron current shunting through barrier layers, the resistance may increase beyond the tolerable limit, thereby causing a

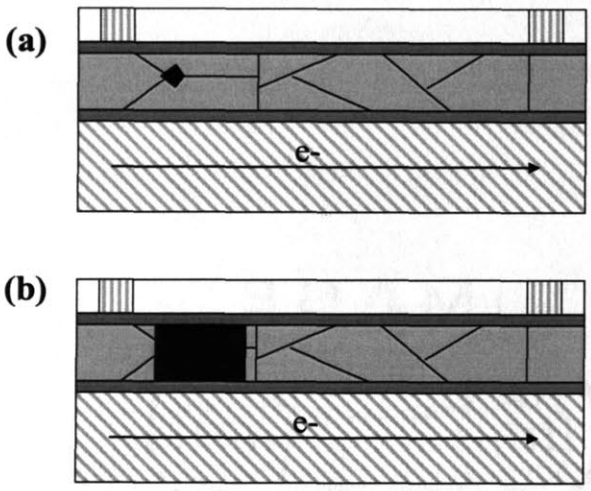

Figure 1.6 (a) Void nucleating at grain boundary site, **(b)** Void spans through thickness and width of the interconnect to cause failure by high resistance.

failure. Joule heating caused by current shunting can accelerate the diffusion and thus shorten the failure time or even cause a catastrophic failure. Therefore in Al interconnects, preventing or reducing electromigration along grain boundaries is the most important task in improving the overall reliability.

1.3.4 Improvements in Al Interconnect Reliability

One approach to improve the reliability of Al interconnects is to use an Al-Cu alloy by adding about 1 atomic percent of Cu [D'Heurle 1971]. It has been shown that the lifetime of Al-Cu interconnects increases by an order of magnitude compared to that of pure Al interconnect [Agarwala 1972]. It is believed that Cu atoms segregate to the

grain boundaries and occupy the Al vacancy sites. Cu atoms in the Al grain boundaries resist the diffusion of Al atoms [Blech 1977][Hu 1993]. Even though adding Cu improves the reliability of interconnects, the overall resistivity increases about 0.3μΩ-cm per % of Cu added, which is undesirable [Ramkumar 1993].

Secondly to improve reliability, it has been observed that Al interconnects with bamboo microstructures have significantly longer TTFs compared to interconnects with polygranular clusters. In bamboo microstructures, all grain boundaries lie in planes perpendicular to the axis of the length of the interconnect or the direction of the electron flow (Figure 1.7(c)). Therefore, atoms can no longer diffuse along fast grain boundary paths, but are forced to diffuse through slower interfacial paths, which significantly reduces the flux rate [Joo 1994]. The average grain size in 0.4μm-thick Al films is about 0.3μm, but bamboo structures are formed by intentionally growing large grains by annealing interconnects at elevated temperature. Grains can grow to larger than 100μm when annealed at 550°C [Cho 1989]. As interconnect dimensions shrink in order to increase the density of ICs, widths and thicknesses of interconnects become smaller than the average Al grain size at room temperature, causing interconnects to form near bamboo structures - mixtures of bamboo structures and polygranular clusters. Reliability of near bamboo structures highly depends on the detailed microstructure of

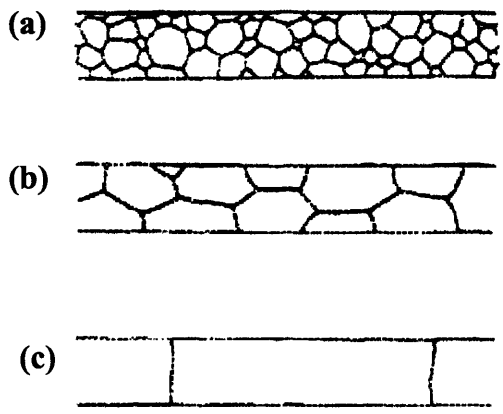

Figure 1.7 (a) Polycrystalline Al **(b)** Polycrystalline Al with large grains **(c)** Bamboo Al.

the interconnect, as flux divergences in boundaries between bamboo and polygranular clusters serve as high tensile stress and void nucleation sites (Figure 1.7(b)) [Cho 1989] [Thompson 1993] [Joo 1994]. Again, the reliability can by significantly improved by removing polygranular clusters from near bamboo structures by carrying out a post-patterning anneal [Walton 1992].

1.3.5 Reliability of Al Interconnect Trees

Most test structures usually terminate with vias at each end, at the cathode and anode, giving straight interconnects with specific lengths. However, in real ICs, interconnects of different dimensions are all connected with each other in the same or different metallization levels, as shown schematically in Figure 1.8(a). These groups

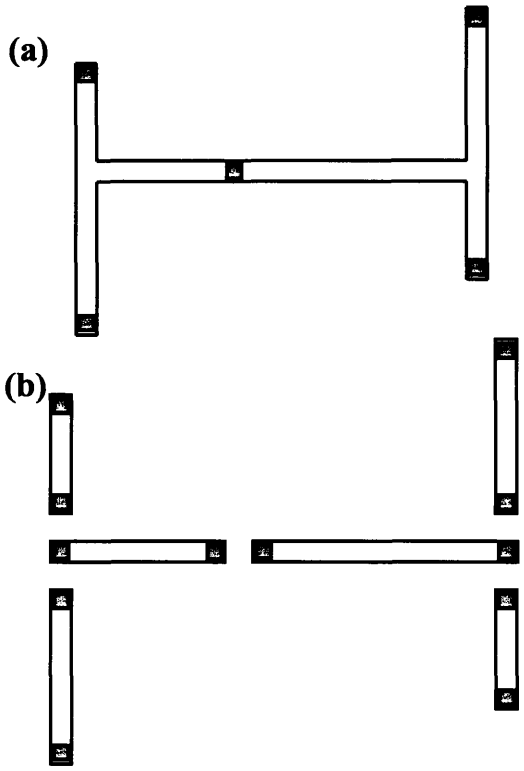

Figure 1.8 (a) Schematic of Al interconnect tree **(b)** Separating interconnect tree into individual segments for reliability estimation.

of linked interconnects are called "interconnect trees." Conventionally, when performing a reliability analysis of a certain IC, interconnect trees in the IC are separated into straight segments and the lifetimes of individual straight segments are used to predict the lifetime of the IC (Figure 1.8(b)). The predicted lifetimes of the straight segments are obtained by performing accelerated EM tests on straight test structures and applying Black's equation to predict TTF at service conditions. However, accelerated EM tests on simple Al interconnect trees show that reliability of

each segment in the tree is not independent of the reliability of other segments [S.Hau-Riege 2000]. Therefore, the conventional method for predicting the reliability of ICs can lead to a conclusion that is likely to deviate from the actual behavior.

To make a predictions with better accuracy, each interconnect tree should be considered as one reliability unit, or Fundamental Reliability Unit (FRU) [S.Hau-Riege 1998]. The failure time of an FRU depends on the path between any two vias that has the highest product of current density and length, $\left(\sum_i j_i L_i\right)_{\max}$, and this can be written as:

$$(jL)_{eff} \equiv \left(\sum_i j_i L_i\right)_{\max}, \tag{1.10}$$

where $(jL)_{eff}$ determines the failure time of the FRU. Accelerated EM tests on simple interconnect trees confirm that the method using trees as FRUs has better accuracy than the conventional method. Therefore, with the proper FRU and data on the microstructure of interconnects, one can carry out a reliability estimation of actual ICs with good accuracy in Al interconnect technology.

1.4 COPPER INTERCONNECT TECHNOLOGY

1.4.1 Advantages and Disadvantages of Cu

As mentioned earlier in this chapter, due to the unavoidable requirement to lower the resistivity of interconnects to minimize RC delay, lower resistance Cu has been introduced to replace Al. However, integrating Cu interconnects in ULSI systems requires completely different fabrication processes compared to Al. Because of the need to have sub-micron-scale interconnects and high thickness-to-width ratio structures, RIE is used in Al interconnect fabrication instead of wet etching, for its fine scale etch capability and anisotropic etching. However, RIE of Cu is not practical because of the lack of volatile Cu compound formation at low temperature [Howard 1991]. Also, because Cu diffuses through SiO_2 and creates mid-gap energy levels in the Si band gap, which degrades the electronic properties of Si, diffusion barrier layers are needed to encapsulate Cu [Sze 1981]. The only known process that can meet these requirements is use of the damascene technique with CMP [Kaanta 1991].

1.4.2 Cu Interconnect Fabrication

The Cu metallization fabrication sequence using the dual-damascene method is described in figure 1.9. The ILD is first etched, then a diffusion barrier layer and Cu seed layer are deposited using sputter deposition. Cu is then electroplated, and

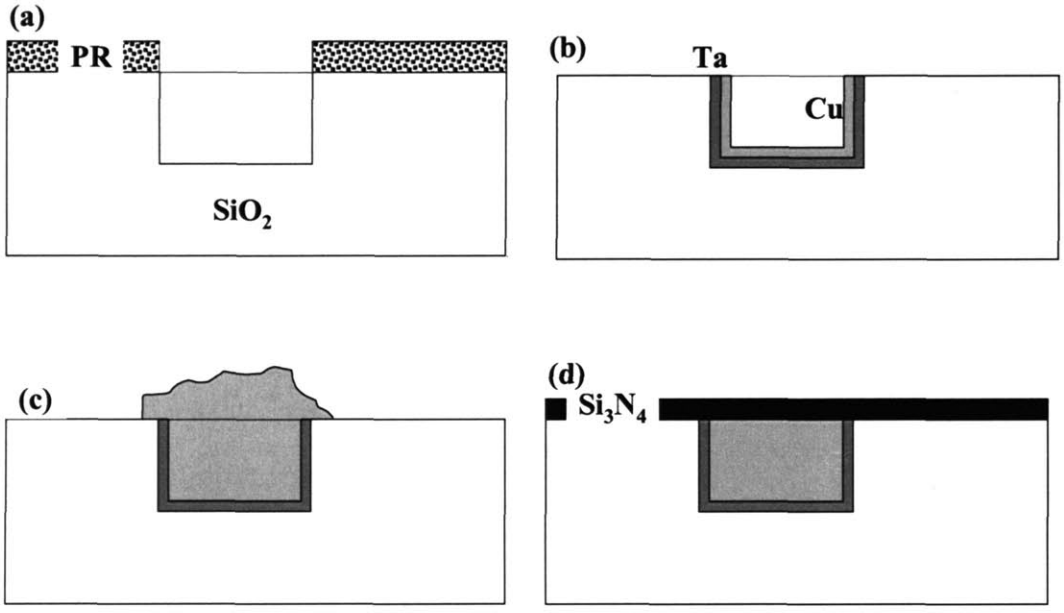

Figure 1.9 Copper fabrication process. **(a)** ILD is patterned and etched with RIE. **(b)** Diffusion barrier layer and Cu seed layer is sputter deposited. **(c)** Cu is electroplated **(d)** Over-burden Cu is polished with CMP, and diffusion barrier passivation layer is deposited.

planarized using CMP. Finally, diffusion-barrier capping layer, which has been typically Si_3N_4, is deposited to completely encapsulate the Cu interconnects.

1.4.3 Electromigration in Cu Interconnects

With the transition from Al to Cu, the reliability of interconnects also changes, due to the differences of the intrinsic properties between Al and Cu. First, due to changes in the surrounding materials and geometry for Cu interconnects, $(z^* D)_{eff}$ is calculated differently compared to that of Al, which was given in equation (1.9).

Using equation (1.8), [Hu 1997]

$$\left(z^{*}D\right)_{eff} = z_{B}^{*}D_{B}n_{B} + z_{icl}^{*}D_{icl}\delta_{icl}\left(\frac{1}{h}+\frac{2}{w}\right) + z_{icp}^{*}D_{icp}\delta_{icp}\left(\frac{1}{h}\right) + \sum z_{gb}^{*}D_{gb}\left(\frac{\delta_{gb}}{d}\right), \quad (1.11)$$

where subscripts icl and icp are interfaces between Cu and liner material and interfaces between Cu and the passivation layer, respectively. Other notations are described earlier. With a higher melting point than Al, Cu is expected to have lower self diffusion. Therefore, assuming similar failure mechanisms, Cu should have much better electromigration resistance, especially in bamboo structures. However, experimental results show that Cu-based interconnects do not exhibit superior reliability as expected [C. Hau-Riege 2004].

In Al interconnects the dominant diffusion path is along grain boundaries, and the grain boundary paths are effectively reduced by forming bamboo structures, or by inclusion of impurity materials (such as copper) into the grain boundaries. However, in Cu interconnects, grain boundary paths are not the dominant diffusion paths. The dominant diffusion path is reported to be along the interface, especially between Cu and the top passivation layer (Cu/passivation) [Hu 1997]. The Cu/passivation interface is also most prone to void nucleation due to its weak bonding nature, especially with Si_3N_4.

It has been found that σ_{crit} for a Cu interconnect is about an order lower than that for Al, at around 40MPa [S. Hau-Riege 2002][C. Hau-Riege 2002]. Therefore, unlike Al interconnects, forming a bamboo structure in Cu interconnects does not effectively reduce the overall diffusivity or improve reliability. In order for Cu interconnects to have significantly superior reliability compared to that of Al, diffusion along Cu/passivation interface must be effectively suppressed.

1.4.4 Improvements in Cu Interconnect Reliability

For Cu interconnects, enhancing the bonding energy or reducing the diffusion at Cu/passivation interface are key to overall improvement of reliability. The procedure or the material that can reduce the diffusion at this interface should also be simple and able to be integrated into a current technology process. Hu *et al.* used materials that preferentially deposited only onto the Cu surface and showed the increase in lifetime [Hu 1998a] [Hu 2002]. One of the materials used was cobalt tungsten phosphate (CoWP). After CMP, CoWP was selectively deposited only onto Cu surface using electroless deposition. By having a selective deposition, an extra photolithography step is avoided, thus reducing the time and cost of the overall fabrication process. However, so far, yield for this process has been poor, which has prevented its use in

actual production [Rosenberg 2005]. AMD has a process in which Al is included in the seed layer, so that when the interconnect is annealed it segregates to the top surface and suppresses diffusion, and greatly enhances reliability. Unfortunately, this comes with the cost of increased resistivity. Also, there have been general process improvements that have lead to better interfaces, involving cleaning a surface. While more research is in progress to find an effective solution to reduce the Cu/passivation interface diffusivity, there has been no significant integration process for actual production to date.

1.4.5 Voids in M1 and M2 of Cu Interconnects and Their Roles in Reliability

Another critical factor to reliability of Cu interconnects is the characterization of void dynamics, which is also significantly different from that of Al. As described earlier (Figure 1.6), the most likely site for void nucleation in Al interconnects is at grain boundaries. In Cu interconnects, the Cu/passivation interface is the site most prone to void nucleation. Because of this, the main difference in Cu interconnects compared to that of Al is that the void mostly nucleates at the upper side of the cathode end (Figure 1.10). This leads to differences in failure times with the level of metallization in Cu interconnect [Gan 2003, C. Hau-Riege 2002, Lee 2001, Alam 2004].

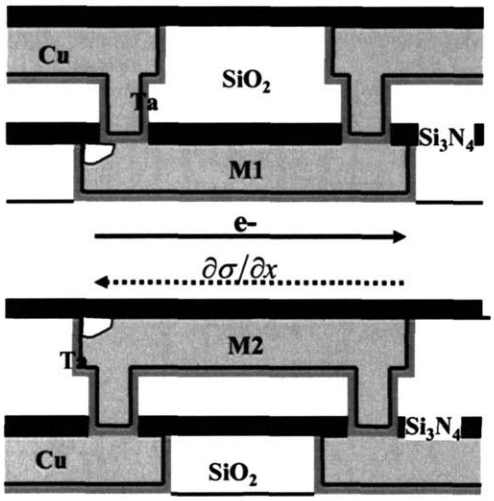

Figure 1.10 Void nucleation site in Cu interconnect. Void nucleates at the Cu/Si_3N_4 interface near cathode end.

If the interconnect is in the first level of metallization (M1) (Figure 1.10(a)), or the via is above the interconnect, a void will be likely to nucleate near the base of the via. Because the passivation layer is insulating (in contrast with Al technology), if the void fully covers the base of the via, an open circuit failure occurs. The void volume required to cause open-circuit failure in M1 or via-above structures can be small [S. Hau-Riege 2002].

On the other hand, if the interconnect is in the second metallization layer (M2) (Figure 1.10(b)), or the via is below the interconnect, the nucleated void at the Cu/passivation layer interface needs to span the thickness and width of the interconnect in order to cover the via. Therefore, a larger void volume than that required in M1

structures is required to cause the failure [Gan 2003]. This is described in detail in chapter 3. Thus, in M1 or via-above structures, failure occurs at or shortly after void nucleation, which is regarded as void-nucleation-limited failure. As described earlier, this gives a current density exponent value of 2 in Black's equation. In M2 structures, failure occurs after the void grows to a critical size, and this is regarded as void-growth-limited failure. This gives a current density exponent value of 1. However, Rosenberg *et al.* observed that the current density exponent in M1 structures is close to 1 only at low current densities, and changes to 2 at higher current densities [Rosenberg 2000]. Also in M2 structures, a current density exponent of 1 is observed at low current densities, but the value changes to around 1.6 at high current densities [Padhi 2003] [Vairagar 2004]. These phenomena have so far not been clearly understood, and are the subject of chapter 7.

1.4.6 Liners

With industry pushing toward higher IC density, the dimension of the Cu interconnect *as well as the liners* must shrink. Currently, Ta, Ta based alloys, or Ti-based alloys are used as liners in Cu interconnects [Hu 1998a]. As described earlier, liners need to provide good adhesion between Cu and the ILD, and also prevent Cu

diffusion into the ILD. Liners are already expected to be reduced to a few atomic layers [ITRS] [Hu 1998a]. This is another reliability concern because having a continuous, reliable liner is critical.

1.4.7 The Reliability of Cu Interconnect Trees

As with Al interconnects, the reliability of individual segments in a Cu interconnect tree behave differently compared to similar single interconnect segments in isolation [Gan 2003]. The reliability of Cu must also be treated with trees serving as FRUs and by using $(jL)_{eff}$. Moreover, $(jL)_{eff}$ of M1 and M2 structures must be treated separately for Cu interconnects [Alam 2004]. More detailed analyses of Cu interconnect trees are described in chapter 4.

1.5 SCOPE OF THE THESIS

Many of the failure mechanisms found in Al interconnects are not be directly relevant to Cu interconnects. Thus, it is important to understand the phenomena that are unique to Cu interconnects. The scope of this thesis is to observe and analyze the failure mechanisms of Cu interconnects, especially mechanisms that involve voids, using new techniques and simulations. Information obtained on failure mechanisms

can be applied to development of more accurate reliability predictions for Cu interconnect technology.

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CHAPTER 2

NUMERICAL SIMULATION TOOL FOR OBSERVING ATOMIC CONCENTRATION AND STRESS IN METAL INTERCONNECT DURING ELECTROMIGRATION

ABSTRACT

A new technique for simulation of electromigration-induced atom diffusion and stress evolution in a confined metal interconnect has been developed. The Korhonen model for stress evolution was used. In this model, diffusion is driven by both a momentum transfer from the electron 'wind' and by the gradient in chemical potential that results from stress gradients and opposes the electron wind force. This model results in a differential equation that describes the evolution of stress as a function of time and location along the length of an interconnect. However, because the diffusivity of electromigrating atoms in a confined interconnect is dependent on stress, the differential equation is non-linear. It is shown that high-order implicit time integration methods result in stable simulations and much shorter simulation times than the low-order explicit schemes, such as, the forward-Euler technique, used in earlier work. A simulation tool based on implicit methods was constructed to allow investigation of the conditions leading to void nucleation and growth in both single interconnect segments and complex multi-segment interconnect trees. This tool allows mechanistic analyses of accelerated test results, as well as extension of these analyses to the much long times expected under service conditions.

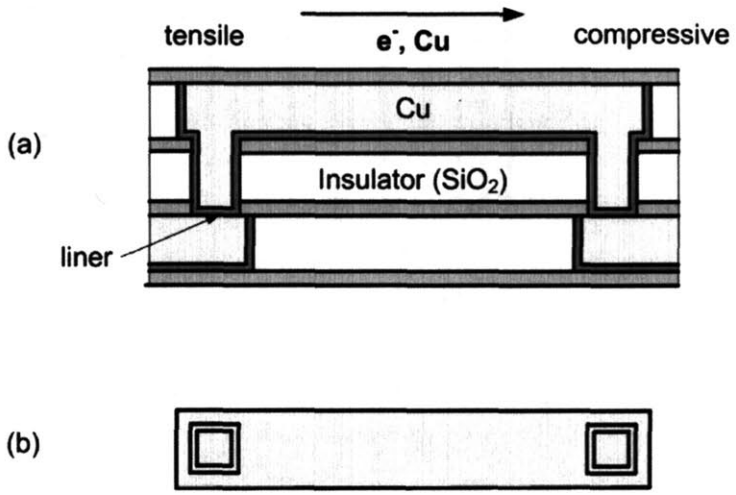

Figure 2.1 Sketch of an interconnect segment: **a)** side view, **b)** top view.

2.1 INTRODUCTION

Electromigration is one of the main causes of failures in metal lines that are used to interconnect devices in integrated circuits [Blech 1967]. When electrical current is applied to a metal interconnect, electrons transfer momentum to metal atoms and cause them to diffuse in the same direction as the direction of electron motion. The rate of electromigration scales with the diffusivity of the conducting metal, so that, at a given temperature, electromigration rates in materials like Cu are much higher than electromigration rates in the materials used as liners and diffusion barriers in Cu-based interconnect metallization schemes, such as Ta, TaN, and TiN. These liner materials are present at the 'vias' that connect different levels of metallization, and partition the interconnect network into segments and trees (Figure 2.1). As atoms electromigrate

they accumulate at anode vias and deplete at cathode vias. Because interconnects are confined, both by liners and insulating materials such as silicon dioxide, a compressive stresses build up at the anode vias and tensile stresses build up at the cathode vias. A compressive stress at an anode via can cause the mechanical failure of the surrounding materials, which leads to leakage or extrusion of metal atoms to cause short-circuit electrical failures. A tensile stress at a cathode via can cause nucleation and growth of a void, which can lead to an open-circuit failure. Therefore, understanding electromigration-induced stress evolution is critical for understanding the failure rates and mechanisms of interconnects.

Korhonen *et al.* proposed an equation describing the electromigration-induced evolution of the hydrostatic stress σ along the length x of a confined conductor [Korhonen 1993]

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\frac{D_{eff} B}{kT}\left(\Omega \frac{\partial \sigma}{\partial x} + Z^{*}_{eff} e \rho j\right)\right], \tag{2.1}$$

where t is time, D_{eff} is the effective atomic diffusivity, Ω is the atomic volume, k is Boltzmann's constant, T is the temperature, Z^{*}_{eff} is the effective charge number for the electromigrating atoms, e is the fundamental electron charge, ρ is the electrical

resistivity of the conducting material, and j is the current density. B is an effective modulus that describes the composite elastic response of the materials surrounding the conductor, to changes in the volume of the conductor due to atom accumulation or depletion. The effective atomic diffusivity is expressed as [Clement 1995]

$$D_{eff} = D_o \exp\left(-\frac{\Delta H}{kT}\right)\exp\left[\left(\frac{\Omega}{kT}+\frac{1}{B}\right)\sigma\right], \tag{2.2}$$

where ΔH is the activation energy for diffusion and D_o is a temperature independent constant. As shown in equation (2.2), D_{eff} is stress dependent, so that when equation (2.2) substituted into equation (2.1), the differential equation becomes highly non-linear. There is no known analytic solution for this equation, so that it must be solved numerically. In the past this has been done using low-order explicit schemes, such as the forward-Euler technique [Park 1997]. However, this approach often leads to long computation times and time-domain instabilities that can result in solution failures due to the strong nonlinearity and stiffness of the Korhonen's model in equation (2.1) [Ascher 1998]. In this paper we develop a solution approach based high-order implicit time integration methods, and use this approach in a tool that allows analysis of stress evolution, and the conditions leading to compressive or tensile failures, in both

individual interconnect segments and multi-segment interconnect tress.

2.2 SIMULATION APPROACH

2.2.1 Atom Conservation

Equation (2.1) can be reformulated into the form of a conservation law. Because the total number of metal atoms in a confined interconnect is conserved [Korhonen 1993],

$$\frac{\partial C_a}{\partial t} + \frac{\partial J_a}{\partial x} = 0, \tag{2.3}$$

where C_a is the atomic concentration (number per volume) and J_a is the atomic flux. Also,

$$C_a = C_l - C_v, \tag{2.4}$$

where C_l is the concentration of lattice sites and C_v is vacancy concentration, and where C_l and C_v vary with σ according to:

$$C_l = C_{lo} \exp\left(-\frac{\sigma}{B}\right) \tag{2.5}$$

and

$$C_v = C_{vo} \exp\left(\frac{\Omega\sigma}{kT}\right). \tag{2.6}$$

Furthermore, the atomic flux, J_a, is given by:

$$J_a = -\frac{D_{eff} C_a}{kT}\left(Z^*_{eff} e\rho j - \Omega\frac{\partial\sigma}{\partial x}\right), \tag{2.7}$$

where the effective atomic diffusivity D_{eff} is given as [Clement 1995]:

$$D_{eff} = D_v \frac{C_v}{C_l} \tag{2.8}$$

and

$$D_v = D_{vo} \exp\left(-\frac{\Delta H}{kT}\right). \tag{2.9}$$

Equations (2.5) through (2.8) combine to give equation (2.3), with

$$D_o = D_{vo} \frac{C_{vo}}{C_{lo}}. \tag{2.10}$$

Equations (2.3) through (2.10) provide the basis for our simulation approach.

2.2.2 The Finite Volume Method for Spatial Discretization

Finite-volume methods constitute a class of methods developed primarily for computational fluid mechanics, to (a) satisfy the conservation law; and (b) capture shock effects accurately [LeVeque 2006]. The reformulation of equation (2.1) as a conservation law allows application of these methods as described in the following.

An interconnect of length L is discretized into a number of cells N_c, each with length Δx, so that :

$$L = N_c \Delta x. \tag{2.11}$$

The atomic concentration, stress, and *state* value of each cell are tracked. The state values distinguish cells filled with conductor from cells that represent voids. The atomic concentration and stress in conductor cells are related by equations (2.4) through (2.6). However, in voided cells, the atomic concentration is allowed to change even

though the stressed is fixed at zero. Cells share boundaries with adjacent cells at which the atomic flux is defined, as shown in Figure 2.2. Following the usual staggered grid convention [Legeque 2006], cells have integer indices from 1 to N_c and the cell boundaries have half integer indices, e.g. 1/2, 3/2, 5/2 etc., up to N_c+1/2.

The atomic flux defined by equation (2.7), is approximated as:

$$J_{a(i-1/2)} = -\frac{\left(D_{eff\,(i-1)} + D_{eff\,(i)}\right)\left(C_{a(i-1)} + C_{a(i)}\right)}{4kT}\left(Z^*_{eff} e\rho j - \Omega\frac{\sigma_i - \sigma_{i-1}}{\Delta x}\right). \tag{2.12}$$

Linearly interpolated values are used for D_{eff} and C_a at the half-integer indices, resulting in a first-order accurate approximation. Finally, the conservation law in equation (2.3) is approximated as:

$$\frac{\partial C_{a(i)}}{\partial t} = -\frac{J_{a(i+1/2)} - J_{a(i-1/2)}}{\Delta x} = \frac{J_{a(i-1/2)} - J_{a(i+1/2)}}{\Delta x}. \tag{2.13}$$

Once the atomic concentration C_a is found from equation (2.13), σ can be evaluated either by using equations (2.4), (2.5), and (2.6), or it can be forced to zero, depending on the state of the cell.

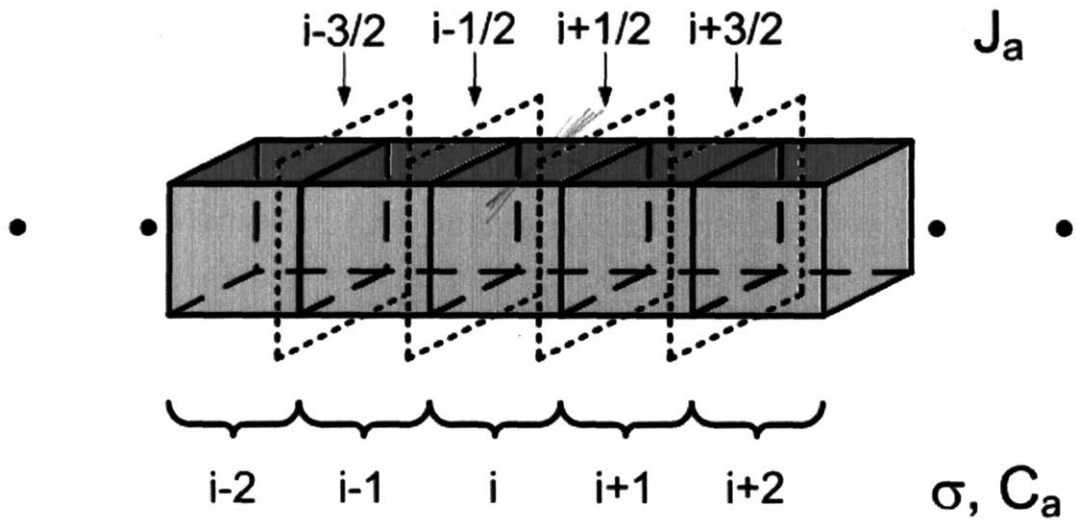

Figure 2.2 Discretization of an interconnect segment into individual cells. The stress and atom concentration is tracked for each cell. The atomic flux between cells is calculated by using a staggered grid system, which can be envisioned as corresponding to cell boundaries.

2.2.3 Time Integration

Consider an ordinary differential equation,

$$\frac{dC_a}{dt} = f(C_a) \tag{2.14}$$

where C_a can be treated as a vector of dimension N and f is a vector-valued function that maps an N dimensional vector to an N dimensional vector. Such an abstraction applies to equation (2.13) if f evaluates the net atomic influx from C_a, based on the right-hand side of equation (2.13). The problem is to find C_a at

time t^{k+1}, denoted C_a^{k+1}, from the known sampled values $C_a^0, C_a^1, \ldots, C_a^k$. Different time integration methods are classified based on where and how many points are used to approximate $\frac{dC_a}{dt}$ [Ascher 1998]. The derivative at either t^k or t^{k+1} is approximated by a weighted sum of $C_a^0, C_a^1, \ldots, C_a^{k+1}$ as

$$\frac{dC_a}{dt} = \sum_{j=0}^{k+1} \alpha_i C_a^j . \tag{2.15}$$

The accuracy of this approximation tells the order of the numerical integration and approximating $\frac{dC_a}{dt}$ at t^k or t^{k+1} determines whether the method is explicit or implicit.

A straightforward and simple method is to utilize a low-order explicit method. One such method is the forward Euler method, which discretizes equation (2.14) into

$$\frac{C_a^{k+1} - C_a^k}{\Delta t} = f\left(C_a^k\right) \tag{2.16a}$$

or

$$C_a^{k+1} = C_a^k + \Delta t f\left(C_a^k\right) \tag{2.16b}$$

The method is widely used in practice since each update is a simple function evaluation. But, the simplicity comes with a price; the time step Δt is limited by both the accuracy requirement given by the user and the stability requirement imposed by the equation itself [Ascher 1998]. This can be shown with a linear example. Suppose equation (2.16) is linearized around C_a^k,

$$\frac{C_a^{k+1} - C_a^k}{\Delta t} = A^k C_a^k, \tag{2.17}$$

where A^k is an N-by-N matrix and diagonalizable. $A^k = V^k \Lambda^k V^{-k}$ for some V^k where Λ^k is a diagonal matrix of eigenvalues λ_i^k and V^k is an invertible matrix of eigenvectors. In this case, $\tilde{C}_a^k = V^{-k} C_a^k$ satisfies

$$\tilde{C}_a^{k+1} = \left(1 + \Delta t \Lambda^k\right) \tilde{C}_a^k \tag{2.18}$$

and for each scalar equation of (2.18) to be stable,

$$\left|1 + \Delta t \lambda_i^k\right| < 1 \tag{2.19}$$

must be satisfied. This leads to the time step size limit:

$$\Delta t_{\max} < \frac{2}{\min\left|\lambda_i^k\right|} . \tag{2.20}$$

A differential equation is called stiff if the largest Δt to meet the stability requirement is much smaller than that to meet the accuracy requirement. For such equations, explicit methods usually perform poorly especially if moderate accuracy is required. The discretized Korhonon model in equation (2.13) falls into this category. The problem of explicit methods can be mitigated if higher order approximation is used. In addition, an adaptive algorithm to adjust the order or approximation and Δt can help improve the algorithm for nonlinear ordinary differential equations, like equation (2.13), since the stability requirements for nonlinear equations are different for different t's.

The number of calculations can be significantly reduced by an implicit method. An example is the backward Euler method, which discretizes equation (2.14) into

$$\frac{C_a^{k+1} - C_a^k}{\Delta t} = f\left(C_a^{k+1}\right) \tag{2.21}$$

Obtaining C_a^{k+1} requires solution of a nonlinear equation, making each step considerably more computationally expensive. However, this method guarantees stability for all positive time step sizes, so that larger time steps can be used. To see this, equation (2.21) is again linearlized,

$$C_a^{k+1} - C_a^k = \Delta t A^{k+1} C_a^{k+1}, \tag{2.22}$$

where A^{k+1} is assumed diagonalizable, and the difference equation for each component is

$$\widetilde{C}_a^{k+1} = \left(I - \Delta t \Lambda^{k+1}\right)^{-1} \widetilde{C}_a^k \tag{2.23}$$

All the scalar equations are stable for all positive Δt. Note that, we have used the assumption that all λ_i^{k+1} are negative to arrive at this stability result, which means that the linearized systems in equation (2.14) are stable for all values of t.

Implicit methods enable us to take large time steps even for stiff problems. As

a result, fewer steps are necessary to reach t_{final}, especially if the accuracy requirement is not stringent, the overall cost is less compared to an explicit method even though each step is more expensive.

2.3 NUMERICAL EXPERIMENTS

In the final implementation of the numerical method, the ode23s function in Matlab, an adaptive semi-implicit time integration scheme, is used to shorten simulation time and improve stability since equation (2.13) is highly stiff. In this section, the performance of such time integration scheme is compared with two other methods: the forward Euler method and an adaptive explicit scheme.

For the simulations, values for Cu-based interconnects with SiO_2 dielectric insulators have been used, and simulations have been carried out for a temperature of 350°C, to correspond to electromigration experiments carried out by the authors [Chang 2006]. The following values were used for the simulations: σ_{crit} = 40MPa [C.Hau-Riege 2002]; Z^*_{eff} = 1 [Hu 1999]; B = 28GPa [S.Hau_Riege 2000]; $\Omega = 1.18 \times 10^{-29}$ m^3; $\rho = 4.1 \times 10^{-8}$ Ω-m (at 350°C); ΔH = 0.8eV [Hu 1997].

The importance of meeting the stability requirement is shown by forcing the forward Euler method to take Δt larger than the stability limit. As shown in Figure 2.3,

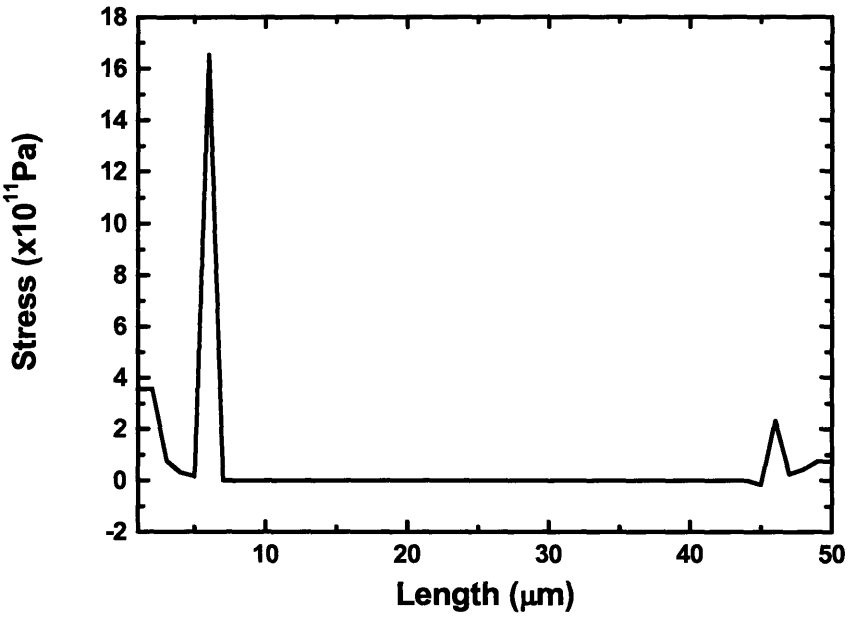

Figure 2.3 Stress profile with Δt larger than the stability limit in forward-Euler method (low-order explicit method). Notice that the stress profile shows random behavior. Simulations conditions : 50 cells of 1.0μm length, total length = 50μm, j = 2.5MA/cm^2, T = 623K, D = 4.5x10^{-16} m^2/s.

the stress profile shows random behavior.

Comparison of the adaptive implicit and explicit methods has been carried out using the ode23 function in Matlab, an adaptive explicit numerical. The order of approximation and Δt's for both ode23 and ode23s are optimized internally by Matlab.

The results of this comparison are shown in Figure 2.4. The calculation time increases linearly with the simulated time when ode23 is used since Δt is limited by the stability of equation (2.13). The rate of increase of the calculation time depends on a

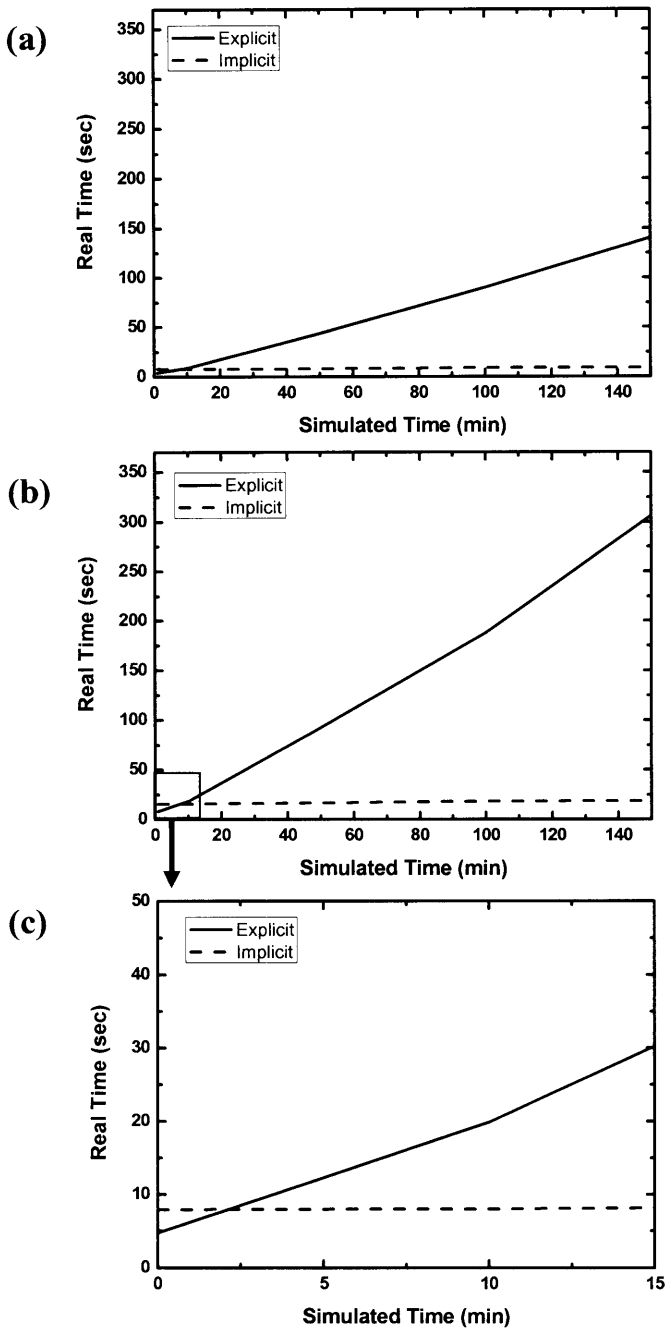

Figure 2.4 Calculation time comparison for explicit-based and implicit-based methods. Simulations conditions: **(a)** 100 cells of 1.0μm length, total length = 100μm, j = 2.5MA/cm^2, T = 623K, D = 4.5x10^{-16} m^2/s; **(b)** 200 cells of 1.0μm length, total length = 200μm, j = 2.5MA/cm^2, T = 623K, D = 4.5x10^{-16} m^2/s. **(c)** is the close up region of (b).

number of factors, including the diffusivity, the temperature, and the number of cells. Using ode23s, the calculation time at short simulated times (<10minutes) is longer than when ode23 is used since each time step for ode23s is more expensive than that of ode23. However, the calculation time using ode23s increases very slowly with increasing simulated time since Δt is no longer limited by stability requirements. Figure 4b shows that at a simulated time of 150 minutes, ode23 is 16 times slower than ode23s (ode23s – 18.71 seconds, ode23 – 306.57 seconds).

A typical failure time for interconnects under accelerated electromigration testing is 100 hours. At this simulation time, the calculation time is about factor of 600 times longer for explicit-based (12000 seconds) than implicit-based (19 seconds) methods. The difference is greater as the simulated time increases, making the use of implicit methods mandatory for simulations of failure mechanisms operating at the times expected under actual service conditions.

2.4 SIMULATION TOOL CAPABILITIES

Input variables for the tool include: j, T, D_{eff}, ρ, B, Ω, and ΔH. Along with the ability to investigate the impact of adjustment of these input parameters, three main additional capabilities were implemented.

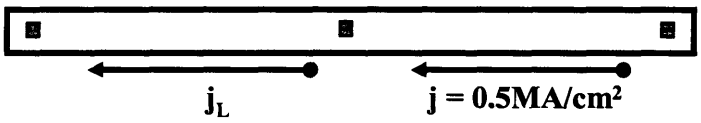

Figure 2.5 Schematic diagram of an interconnect tree where two segments are connected with a via in the middle. Current density (j) of the left segment is fixed while j in the right segment is varied. T=350°C, j_L=0, ±0.5, ±1.5, ±2.5 (MA/cm^2), two 25μm segments for total 50μm in length. Detailed analysis is in chapter 4.

2.4.1 Simulation of Stress Evolution in Interconnect Trees

An interconnect tree is defined as a group of interconnect segments that are connected without electromigration barriers, such as liners, between them. This usually means segments connected within one layer of metallization, since liners in vias block electromigration between layers of metallization. In our simulation tool, interconnect trees are defined by the length of all of the segments within a tree, where each segment terminates at a node, either defined by a via or a connection to one or more other segments. Currents can be applied independently in each tree segment, as long as Kirchoff's laws are obeyed. An example is shown in Figure 2.5, in which two interconnect segments are connected with a via in the middle. Current densities are applied to each of two segments independently and observed the stress profiles with time increments (refer to Figure 4.8 in chapter 4). Experimental results by Chang *et al.*

showed the reliability of the two adjacent segments depend on each other [Chang 2006] which were clearly shown through the simulation tool by observing the sites of void nucleation. More complex interconnect tree structures can also be designed and simulated.

2.4.2 Void Nucleation/Growth, Pre-existing Voids

The simulation tool can be used to treat void nucleation and growth. Void nucleation is assumed to occur if the stress at any point exceeds the critical stress for void nucleation, σ_{crit}. Once a void nucleates, the stress in the cell with a void is assume to relax to zero. Rather than requiring that voids nucleate, pre-existing voids can also be placed anywhere in the segments of a tree, by changing a cell state to indicate a void, and setting the stress in that cell to zero. Figure 2.6 shows an example of stress evolution leading to nucleation and growth of a void and Figure 2.7 shows the effects of a pre-existing void in an otherwise identical simulation. Number of vacant sites is calculated by subtracting the number of atoms in each cell from the initial number of atoms. Then, the void volume is approximated by volume of the vacant site (which is approximated as atomic volume) multiplied by the number of vacant sites.

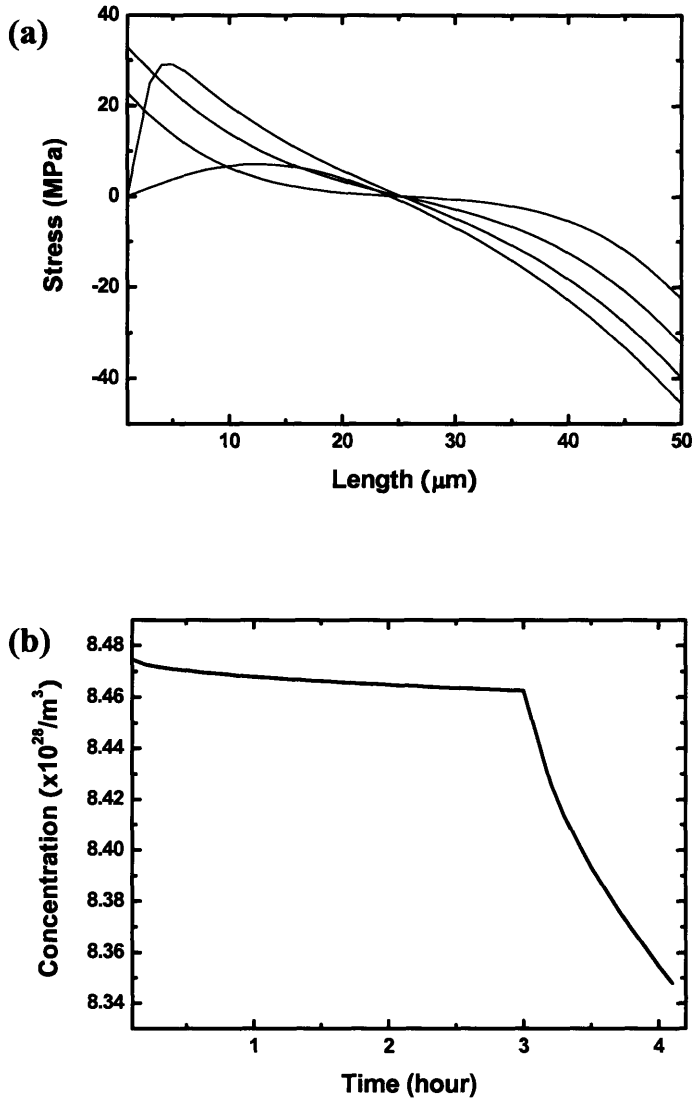

Figure 2.6 Stress evolution before and after nucleation of a void at the cathode. **(a)** Stress profiles at 1 hour intervals of simulated time. A void nucleates when the stress reaches the critical value σ_{crit}=40MPa. **(b)** Concentration vs. time in the first cell where the void nucleates. Note that there is a sudden increase in the rate of depletion of atoms when void nucleation occurs, due to the sudden change in the stress gradient, both in magnitude and sign. Simulation conditions: 50 cells of 1.0μm length, total length = 50μm, j = 0.5MA/cm^2, T = 623K.

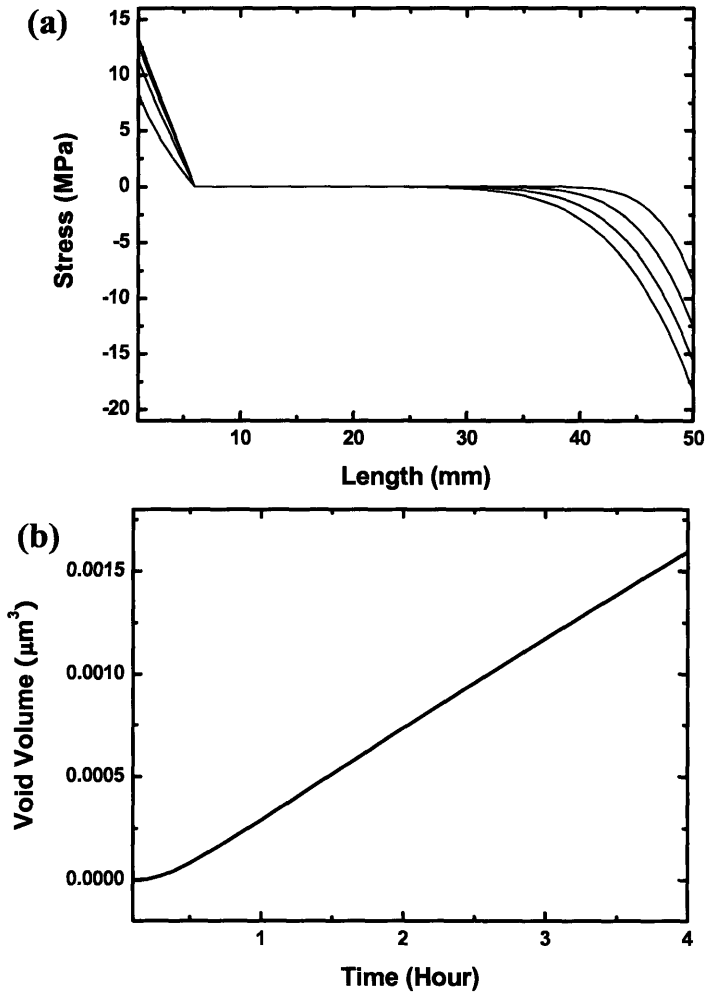

Figure 2.7 Stress profiles at 1 hour intervals of simulated times for an interconnect segment with a pre-existing void 5μm away from the cathode. **(b)** Volume of pre-existing void vs. time. Simulation conditions: 50 cells of 1.0μm length, total length = 50μm, j = 0.5MA/cm^2, T = 623K.

2.4.3 Diffusivity Variations Along the Interconnect

It has been reported that the diffusivity varies with change in crystallographic orientations of grains along the length of polycrystalline interconnect segments [Choi Ch.6b]. Using the approach described above, the effects of diffusivity variations can be readily simulated by varying the diffusivities associated with individual or groups of cells. Figure 2.8 shows the effects of diffusivities varying randomly between $0.5D_{eff}$ and $2D_{eff}$, for an average diffusivity D_{eff}, every 1μm along the length of a segment. These values were chosen to simulate the effects of known diffusivity variations. The simulation shows that, in this case, effects are limited. However, the effects of diffusivity variations on void growth are more profound, and are described in chapter 7.

2.5 CONCLUSION

A simulation tool based on the Korhonen model for electromigration-induced stress evolution along the length of confined metal interconnect has been developed for simulation of various effects of electromigration within interconnect segments and within multi-segment interconnect trees. The tool is based on the use of implicit methods rather than the explicit methods used in earlier studies. Implicit methods lead to stable calculations that allow much reduced calculation times for phenomena

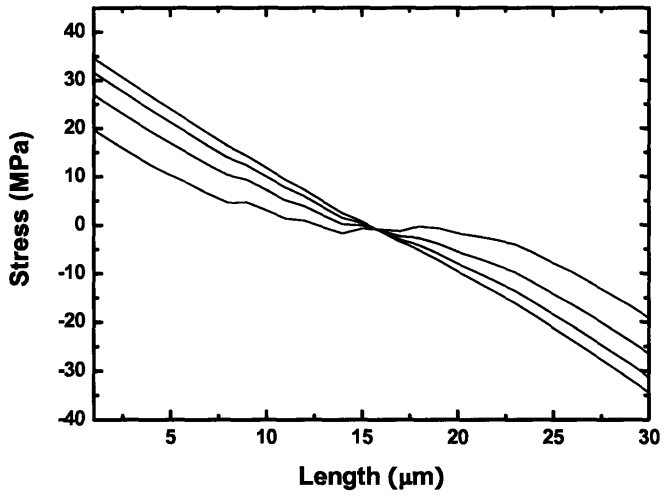

Figure 2.8 Stress profiles at 1 hour intervals of simulated time for an interconnect segment with diffusivity variations of the type expected in polycrystalline segments. Note that the diffusivity effect decreases as the stress approaches a steady state. Simulation conditions: 30 cells of 1.0μm length, total length = 30μm, j = 0.5MA/cm^2, T = 623K, D varied between 0.5D_{eff} to 2D_{eff}.

occuring at long simulation times. It was demonstrated that using implicit method, the calculation time was 19 seconds for a specific conditions described in figure 3b with 100 hours of simulation time, where simulation based on explicit method resulted 12000 seconds of calculation time. The difference in calculation times further increases as the simulated time increases. A new tool, based on use of implicit methods, was constructed to allow simulation of stress-evolution everywhere within a multi-segment interconnect tree, simulation of the conditions leading to nucleation of voids, the effects

of pre-existing voids, the rate of void growth as a function of time and location, and the effects of diffusivity variations along the length of individual interconnect segments. All of these phenomena are know from experiments to occur during electromigration. The simulation approach described above provides a much improved tool for mechanistic investigation of phenomenology observed in accelerated lifetime testing. Moreover, this new approach allows analysis of the effects of these mechanisms at the much longer times for which interconnects are expected to survive in service.

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CHAPTER 3

FATAL VOID SIZE COMPARISON IN VIA-BELOW AND VIA-ABOVE COPPER DUAL-DAMASCENE INTERCONNECTS

ABSTRACT

The median-times-to-failure (t_{50}'s) for straight dual-damascene via-terminated copper interconnect structures, tested under the same conditions, depend on whether the vias connect down to underlaying leads (metal 2, M2, or via-below structures) or connect up to overlaying leads (metal 1, M1, or via-above structures). Experimental results for a variety of line lengths, widths, and numbers of vias show higher t_{50}'s for M2 structures than for analogous M1 structures. It has been shown that despite this asymmetry in lifetimes, the electromigration drift velocity is the same for these two types of structures, suggesting that fatal void volumes are different in these two cases. A numerical simulation tool based on the Korhonen model has been developed and used to simulate the conditions for void growth and correlate fatal void sizes with lifetimes. These simulations suggest that the average fatal void size for M2 structures is more than twice the size of that of M1 structures. This result supports an earlier suggestion that preferential nucleation at the Cu/Si_3N_4 interface in both M1 and M2 structures leads to different fatal void sizes, because larger voids are required to span the line thickness in M2 structures while smaller voids at the base of vias can cause failures in M1 structures. However, it is also found that the fatal void sizes corresponding to the shortest-times-to-failure (STTF's) are similar for M1 and M2, suggesting that the voids that lead to the

shortest lifetimes occur at or in the vias in both cases, where a void need only span the via to cause failure. Correlation of lifetimes and critical void volumes provides a useful tool for distinguishing failure mechanisms.

3.1 INTRODUCTION

As described in chapter 1, it is well understood that electromigration, atomic diffusion driven by a momentum transfer from conducting electrons, leads to serious reliability concerns for integrated circuits. The failure mechanisms due to electromigration are well characterized in aluminum (Al) interconnect technology [Hu 1993][S.Hau-Riege 2000][Wang 1998]. As industry migrates to lower resistance copper (Cu), different failure mechanisms have been discovered, due to different material properties and processes.

One of the failure characteristics in Cu interconnects that differs from that of Al is the asymmetry of the median-times-to-failure (t_{50}'s) in M1 and M2 structures, terminating in vias to upper levels (via-above) and vias to lower levels (via-below), respectively. The terminating vias for these two types of dual-damascene copper interconnects, are illustrated in Figure 3.1. In earlier studies [Gan 2001], it has been shown that the t_{50} for M2 structures of various lengths, widths, and numbers of vias are

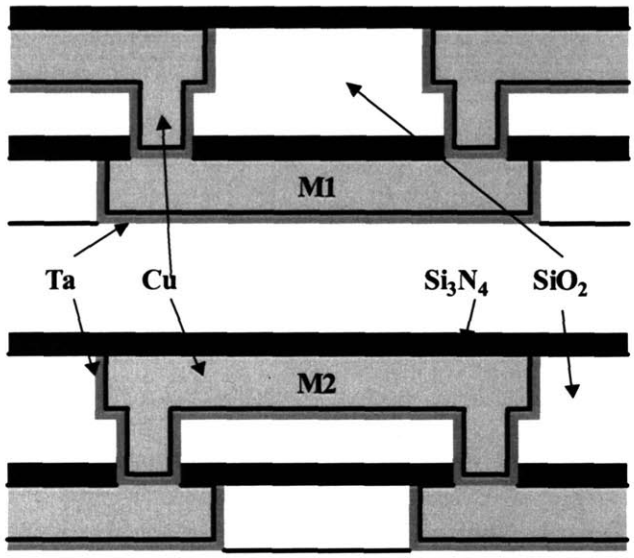

Figure 3.1 Schematic diagram of M1 and M2 structures.

higher than those of analogous M1 structures tested under the same current density and temperature conditions (Table 3.I). It has been proposed that the cause of this asymmetry in lifetimes is due to the preferential nucleation of void at the Cu/passivation layer (Si_3N_4) interface [Gan 2001]. The critical tensile stress for the void nucleation at the Cu/ Si_3N_4 interface is reported to be about 40MPa [S.Hau-Riege 2002]. The stress in an interconnect evolves non-uniformly when it is subjected to continuous electromigration stressing. The critical tensile stress for void nucleation will first be reached at the cathode end of the line [Filipi 1995].

While for M2 structures, the maximum tensile stress is expected to develop at the base of the Cu-filled via, if the critical stress required for void nucleation at the

Table 3.I

t_{50}'s and STTFs

L (μm)	Type/j ($x10^6$ A/cm^2)	MTTF / STTF (hours)
50	M1 / 2.3	20.8 / 1.38
50	M2 / 3.6	68.7 / 3.13
100	M1 / 2.3	25.2 / 4.53
100	M2 / 3.6	116 / 5.73
100	M1 / 2.5	20.5 / 7.33
100	M2 / 2.5	122.8 / 10.01
800	M1 / 2.3	14.5 / 7.36
800	M2 / 3.6	48.5 / 11.67
800	M1 / 2.5	28.7 / 4.44
800	M2 / 2.5	107 / 3.98

The widths of all lines are 0.28μm; All lines are single via terminated; the thickness of M1 is 0.34μm and of M2 is 0.24μm. All tests were done at T = 350 °C Assumed failure when resistance increases more than 30% of the initial resistance [Gan 2001]. j=current density, L=length

Cu/S_3N_4 interface is significantly lower than that of the Cu-liner (Ta) interface, a void will nucleate and grow on the Cu/ Si_3N_4. To cause failure, a void that nucleates at the Cu/Si_3N_4 interface in M2 structures must span the width and thickness of the line to cause failure (Figure 3.2(b)). Once current must shunt through the thin Ta liner, it is assumed that Joule heating rapidly leads to failure.

In M1 structures, voids that nucleate at the Cu/Si_3N_4 interface need only grow to span the base of the via to cause failure [Gan 2001][S.Hau-Riege 2002], because of

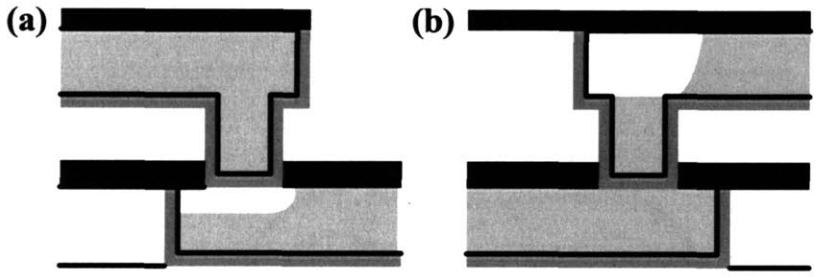

Figure 3.2 Preferential void nucleation and growth at the Cu/Si_3N_4 interface in **(a)** M1 and **(b)** M2 structures.

the Si_3N_4 passivation layers do not provide a shunting path for current as TiN anti-reflection coating (ARC) layers did in Al technology (Figure 3.2(a)). In this paper, the critical void sizes at the TTFs of M1 and M2 structures are calculated using a numerical simulation tool.

The experimental results reported earlier for failure times for straight Cu dual-damascene lines of type M1 and M2 are listed in Table 3.I [Gan 2001]. The median time to failure (t_{50}) and shortest time to failure (STTF) are listed for each test population. These Cu test structures were fabricated by IME in Singapore and had Ta liners and Si_3N_4 passivation layers. The lengths for both M1 and M2 lines are 50μm, 100μm, and 800μm. The thicknesses for M1 and M2 line are 0.36μm and 0.24μm, respectively. The width of all lines is 0.28μm and the cylindrically shaped vias have diameters of 0.26μm. For the analysis, only data for lines terminated with a single via

was used. The wafers were diced and packaged in ceramic packages. Gold wires were used to connect the bond pads to package lead frames. The structures were stressed in an electromigration test system at various current densities and a temperature of 350°C.

In a separate set of studies [Wei 2002], we have investigated the electromigration drift velocities as measured in M1 (via-above) and M2 (via-below structures) prior to failure. After voids have nucleated, but before they grow large enough to cause failure, their growth often leads to a steady resistance increase. Characterization of this resistance increase can be related to the rate of void growth, which is also often referred to electromigration drift, in which the rate of drift of the void edge is related to the drift velocity, which can, in turn be related to the effective electromigration induced diffusivity, or more specifically the effective z*D product, where z* and D are the effective charge and diffusivity, respectively, that characterize electromigration. The values of drift velocity, v_d, obtained using the M1 interconnects are in agreement with the value measured using the M2 interconnects, even among the samples fabricated by different organizations. Therefore, the median lifetimes are significantly different in M1 and M2 structures, but the drift velocity is not. This

indicates that electromigration in these two types can be modeled using the same effective z*D product.

3.2 NUMERICAL SIMULATION

Assuming each atom has the atomic volume $\Omega = 1.18 \times 10^{-29} m^3$ the size of the void is estimated as the total volume of the atoms removed from the void nucleation site. D_{eff} was calculated to be 2.99×10^{-16} m^2/s for M1 structure and 4.23×10^{-16} m^2/s for M2 structure at T = 350°C and σ=0, which is the diffusivity at the Cu/Si_3N_4 interface, the dominant diffusion path for Cu interconnects [Gan 2003]. The following values were used for the simulation: σ_{crit} = 40MPa [S.Hau-Riege 2002]; Z_{eff}^* = 1 [Hu 1999]; B = 28GPa; $\Omega = 1.18 \times 10^{-29}$ m^3; $\rho = 4.1 \times 10^{-8}$ Ω-m; ΔH = 0.8eV.

3.3 ANALYSIS AND DISCUSSION

3.3.1 Analysis with Simulation

The number of atoms removed from the void nucleation site for each structure was simulated as shown in Figure 3.3. The numbers of atoms removed at t_{50} and at the shortest-times-to-failure (STTFs) of each structure have been determined and are shown in Table 3.II. The critical void volumes for failure were calculated at each t_{50} and the

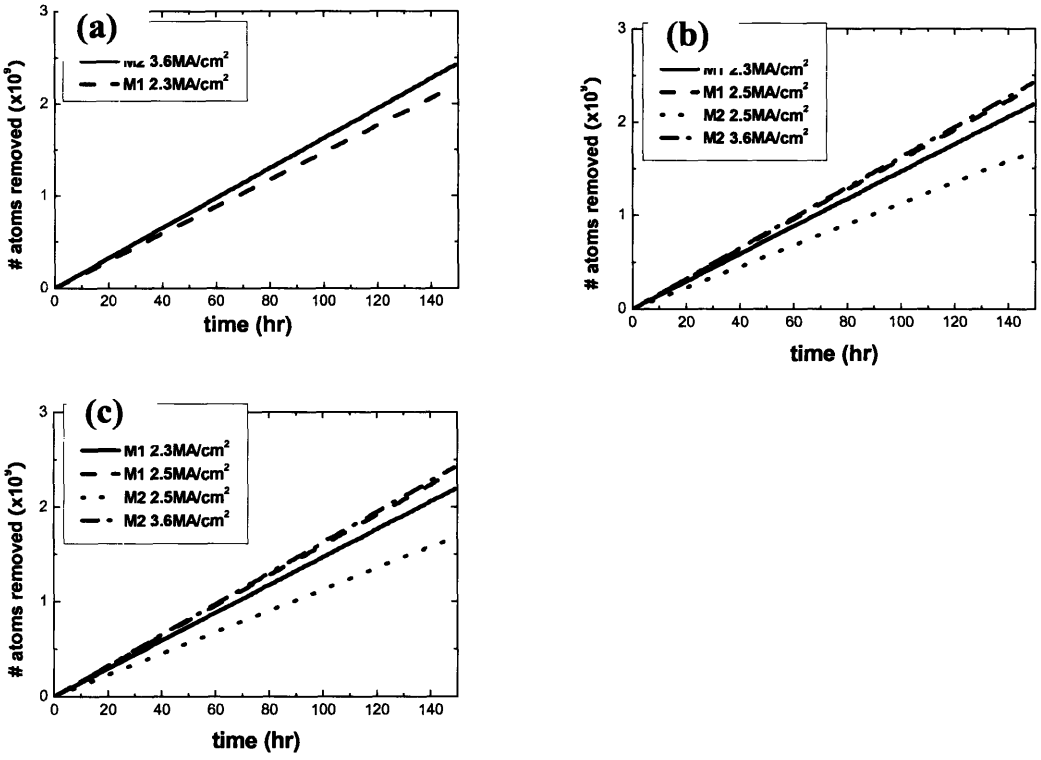

Figure 3.3 The number of atoms removed from a void nucleation site vs. time in **(a)** 50μm, **(b)** 100μm, and **(c)** 800μm lines, as determined through simulations.

STTF and are also shown in Table 3.II.

From the calculated critical void sizes, it is clear that the M2 structures require larger void sizes for failure than the M1 structures. This supports the earlier conclusion that the reason for the difference in void sizes is due to preferential void nucleation at the Cu/ Si_3N_4 interface which causes the void size required for failure in M2 to be larger than that of M1, as shown in Figure 3.2. The void in M2 must fully span in the line in order to cause an open circuit failure, where as only partially

Table 3.II

number of removed atoms and void volumes

L (μm)	Type/j ($x10^6$ A/cm^2)	N($x10^8$) /V(μm^3) (t_{50})	N ($x10^8$) /V(μm^3) (STTF)
50	M1 / 2.3	3.05 / 0.0052	0.20 / 0.0003
50	M2 / 3.6	11.1 / 0.0190	0.51 / 0.0009
100	M1 / 2.3	3.69 / 0.0063	0.67 / 0.0011
100	M2 / 3.6	11.9 / 0.0203	0.93 / 0.0016
100	M1 / 2.5	3.27 / 0.0056	1.17 / 0.0020
100	M2 / 2.5	11.4 / 0.0195	1.13 / 0.0019
800	M1 / 2.3	2.13 / 0.0036	1.08 / 0.0018
800	M2 / 3.6	5.47 / 0.0094	1.90 / 0.0032
800	M1 / 2.5	4.58 / 0.0078	0.71 / 0.0012
800	M2 / 2.5	12.1 / 0.0207	0.45 / 0.0007

j=current density, N=number of atoms removed, V=void volume, L=length of the interconnect

spanning voids directly below the via can cause failure in M1 structures. It is important to note that the thickness of M2 is smaller than that of M1. If the thickness of M2 is increased to that of M1, the t_{50} of M2 should also increase. This will result in an even larger difference in fatal void sizes.

When comparing the critical void sizes at the STTF, however, it can be seen that failure of M2 structures does not *necessarily* require a larger void than for failure of M1 structures. We predict that the reason for the similarity in critical void sizes for failure at the STTF is due to the void forming near in the via in M2 structures and at the base of

the vias in M1 structures. If the void forms right in the via in M2 structures, even a small void size can lead to a fatal failure.

Also, it will be shown in chapter 5 that the void formed at the Cu/passivation layer interface can drift into the via to cause the failure, which does not require a large void. In the case of M1, as shown in Figure 3.2, if a void nucleates at the end of the line it must grow first to the via, and then across it to cause failure. If the void nucleates "downwind" of the via, it must grow to span the line width and thickness, as in the case of M2 structures, the void can grow towards the via and cover the bottom of the via to cause an open circuit failure at relatively small volume.

Fatal void volumes depend critically on the site for void nucleation, so that critical void volumes and lifetimes can vary over broad ranges for both M1 and M2 structures. While the Cu/Si_3N_4 interface is the most probable site for void nucleation in M2 structures, it is possible to have a defect inside the via, such as a pre-existing void present before the test, that can lead to void growth and the resulting line failure, which are described in later chapters of this thesis.

3.3.2 Comparison between Simulated and Experimental Results

In order to verify that the void volumes simulated are fair representation of the

actual void volumes created in the electromigration experiments, the two void volumes were compared. Several cross-sectional images of failed interconnects have been obtained using focused ion beam/scanning electron microscopy as shown in Figure 3.4. The void volumes were measured based on the voids seen from the cross-sectional images. Interconnects terminated with 4 vias (Figures 3.4(a), (b)) were also included. Voids were assumed to span across the width of the interconnects. The void volumes between the simulation and the experiment match reasonably well (Table 3.III). The discrepancies in void volumes, especially for cases in Figures 3.4(b) and 3.4(c), could be the fact that the voids formed away from the cathode. In the simulation, voids form at the end of the cathode because it is the location where the critical stress for the void nucleation is first reached in the straight line interconnect structures. In Figures 3.4(b) and 3.4(c), pre-existing voids away from the cathode may have been present before the

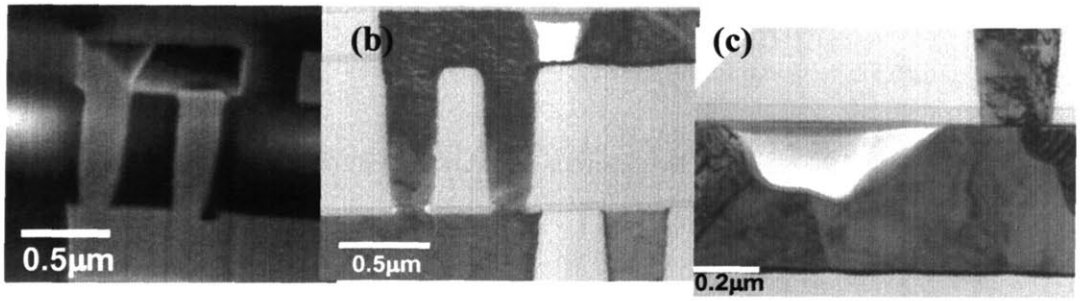

Figure 3.4 (a) M2 L=800μm, w=0.28μm, current terminated after 312 hours.
(b) M2 L=800μm, w=1.00μm, current terminated after 55 hours.
(c) M1 L=100μm, w=0.28μm, current terminated after 192 hours.

Table 3.III

void volume comparisons

Figure	Simulation (x 10^{-20} m^3)	Experiment (x 10^{-20} m^3)	V_{ex}/V_{sim}
4(a)	4.12	3.73	~ 90%
4(b)	9.31	6.44	~ 69%
4(c)	3.61	1.92	~ 53%

The error range of measured void volumes is within 0.4 x10^{-20} m^3.

V_{Ex}/V_{Sim} corresponds to ratio of the voids between experiment and simulation.

current was applied for the electromigration test, which led to a growth as current was applied in the interconnect. The growth rate of the voids away from the cathode is expected to be lower than that of voids at the cathode. This is because while an atomic flux is only going out from the void that forms at the end of the cathode (Figure 3.5(b)), there is an additional atomic flux which goes in to the void when the void is away from the cathode (Figure 3.5(a)). The imbalance of fluxes going out from and into the void may lead to the drift of the void towards the cathode as well as the growth of the void. This is also described in more detail in chapters 5 and 7.

To observe the void volume and the location for the STTF samples, cross-sectional images of 800μm and 100μm length M2 lines at 2.5MA/cm^2 have been obtained (Figure 3.6). In both cases, the location of the failures was at the via, which

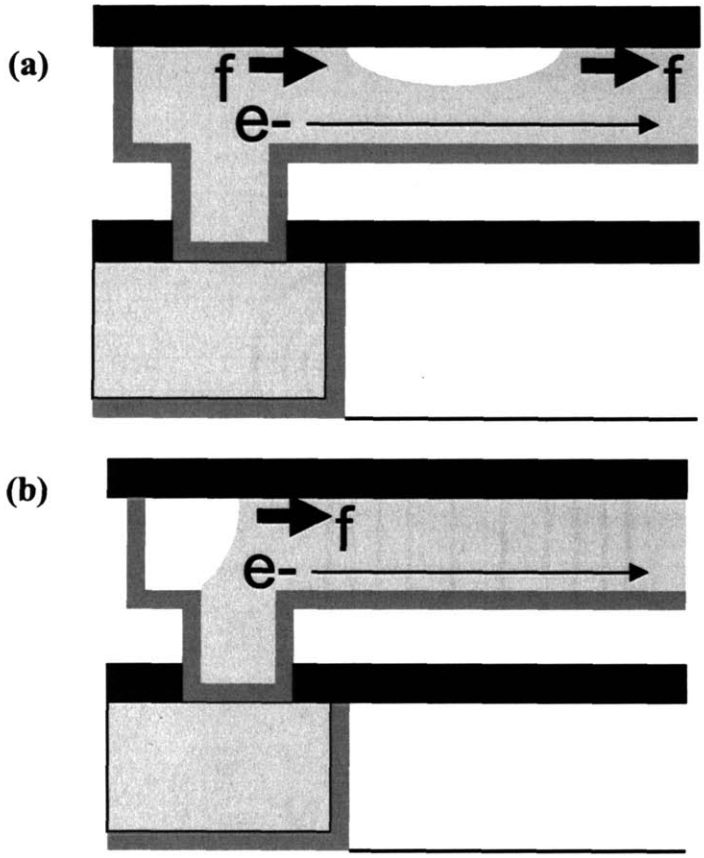

Figure 3.5 f=atomic flux **(a)** Void nucleation and growth away from the cathode in M2. **(b)** Void nucleation and growth at the end of the cathode in M2.

was as expected. However, the failure sites seem to show poor integrity of the shape of the failed vias. The failure criterion of the interconnects is a 30% increase of the initial resistance. However, the current is set to flow until the interconnects become completely open circuit. Therefore, the voids seen in Figure 3.6 represent the voids after the open circuit of the interconnects, which occurred later than STTF. Moreover, the shunted current through a high resistance Ta layer causes the local joule heating, which

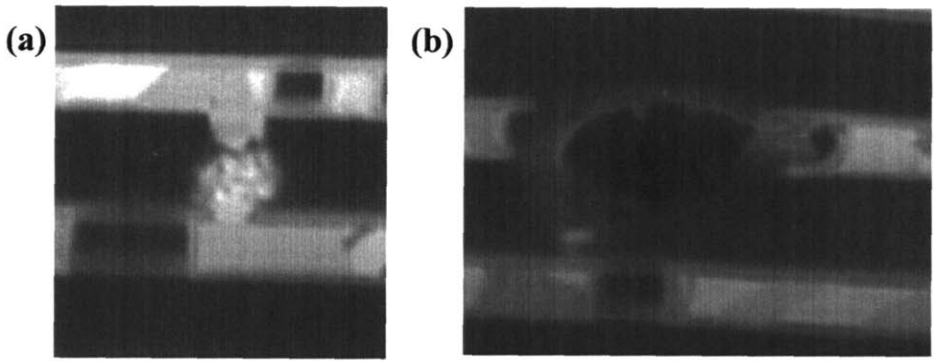

Figure 3.6 (a) Cathode of M2 interconnect, L = 800μm, w = 0.28μm, STTF at j = 2.5MA/cm^2. **(b)** Cathode of M2 interconnect, L = 100μm, w = 0.28μm, STTF at j = 2.5MA/cm^2.

can result in melting or eruption of the interconnects, which might be the case in the poor integrity of the shape as seen in Figure 3.6.

3.4 CONCLUSION

We have developed a simulation tool for electromigration modeling. The tool was utilized to simulate the number of atoms removed from the site of void nucleation. The number of atoms removed was used to estimate the fatal void size. The void volume simulated matches well with the void volume obtained experimentally. The simulation results corresponding to observed t_{50}'s of straight M1 and M2 lines confirm that the average void sizes required for failure in M2 structures is larger than for M1

structures. This is due to the preferential nucleation of voids at the Cu/Si_3N_4 interface. On the other hand, the simulation results for STTFs show that the fatal void sizes for M1 and M2 do not show asymmetric behavior. The similarity in void sizes suggests that the minimum fatal void sizes correspond to nucleation in the via in M2 structures, and at the base of the voids in M1 structures. The nucleation in the via is confirmed with cross-sectional images in figure 3.6. The simulation suggests that while in most cases M2 structures are more reliable than M1 structures, the minimum lifetimes for the two structures might generally be similar if a few flaws exist in the vias. These results show that the variations in the location of void nucleation lead to large variations in the lifetimes of Cu-based interconnects, not only from line-to-line, but from structure-to-structure. This is different from that of Al-based interconnects, where the void nucleates at a grain boundary and is not sensitive to metallization levels [Borgesen 1992]. Therefore, the lifetimes for different metallizations in Al-based interconnects should be similar. These variations in Cu-based interconnects are larger than in the case of Al, and complicate the task of accurate reliability projections for large populations of interconnects. These results also demonstrate the usefulness of simulations, in combination with experimental data, in differentiating complex variations in failure mechanisms.

3.5 ACKNOWLEDGEMENTS

This research was supported by the Singapore-MIT Alliance (SMA) and the Semiconductor Research Corporation. The authors would like to thank Institute of Microelectronics DSIC Cu BEOL for processing the test samples, and Prof. J. White for assistance in development of the numerical simulation tool.

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CHAPTER 4

ELECTROMIGRATION RESISTANCE IN A SHORT THREE-CONTACT INTERCONNECT TREE

ABSTRACT

Electromigration has been characterized in via-terminated interconnect lines with additional vias in the middle, creating two adjacent segments that can be stressed independently. The mortality of a segment was found to depend on the direction and magnitude of the current in the adjacent segment, confirming that there is not a fixed value of the product of the current-density and segment-length, jL, that defines immortality in individual segments that are part of a multi-segment interconnect tree. Instead, it is found that the probability of failure of a multi-segment tree increases with the increasing value of an *effective* jL product defined in earlier work. However, contrary to expectations, the failures were still observed when $(jL)_{eff}$ was less than the critical jL product for which lines were found to be immortal in single-segment test structures. It is argued that this is due to reservoir effects associated with unstressed segments, or due to liner failure at the central via. Multi-segment test structures are therefore shown to reveal more types of failure mechanisms and mortality conditions that are not found in tests with single-segment structures.

4.1 INTRODUCTION

As described in chapter 1, the net atomic electromigration flux, J_a, results from

an electron wind force which is countered by a force caused by the resulting mechanical stress gradient:

$$J_a = -\frac{D_a C}{kT}\left(Z^* e\rho j - \Omega\frac{\partial\sigma}{\partial x}\right), \tag{4.1}$$

where D_a is the atomic diffusivity, C is the concentration of diffusing species, kT is the thermal energy, Z^* is the effective charge number, e is the elementary charge, ρ is the resistivity, j is the current density, Ω is the atomic volume, and σ is the hydrostatic stress along the length x of the interconnect. For short lines bound by zero-flux boundaries that are electrically stressed at low current densities, a steady state will be reached when the stress along the line evolves to a uniform stress gradient, so that the back force due to the stress gradient is balanced by the electron wind force [Blech 1976]. If the stresses remain low enough that void nucleation or metal extrusion does not occur, the back stress will balance the electron wind force and J_a will go to zero. In this case the metal line will be immortal, i.e. immune to electromigration-induced failure. For zero net atomic flux, Equation (4.1) can be rearranged to give:

$$(jL)_{crit} = \frac{\Omega\Delta\sigma}{Z^* e\rho}, \tag{4.2}$$

where $(jL)_{crit}$ is the critical product of current density, j, and the line length, L, for which the forces balance and $\Delta\sigma$ is the difference in the hydrostatic stress between the anode and the cathode.

If a void nucleates, it will grow until failure occurs or until the forces balance. The latter can occur if the void does not cause an open circuit failure or if it causes a resistance increase less than the increase defined as unacceptable, ΔR_{fail}. In this case, the line will be immortal as long as

$$jL < (jL)_{sat} = \frac{(\rho / A)}{(\rho / A)_l} \frac{\Delta R_{fail}}{R} \frac{2\Omega B}{Z^* e \rho}, \tag{4.3}$$

where (ρ/A) and $(\rho/A)_l$ are the ratio of the resistivity and the cross-sectional area of the primary conductor and the liner, respectively, and R is the resistance of the line without a void [Suo 1998].

$(jL)_{crit}$ and $(jL)_{sat}$ are important parameters in IC interconnect layout design as they determine the line length beyond which electromigration would be a concern. It also serves as an important input in circuit-level reliability analysis tools in defining the overall reliability of the IC metallization. While immortality has been demonstrated for

straight via-to-via Cu interconnects [Wang 2001][Lee 2001][C.Hau-Riege 2002], a range of jL values, from 1500 A/cm to 3700 A/cm, have been reported. This is mainly due to the asymmetrical EM behavior for the via-above (M1) and via-below (M2) of Cu interconnects [Gan 2001], and the sensitivity of the interconnects to the location of voids formation [S.Hau-Riege 2002]. Moreover, the reliability of a segment in a Cu-based interconnect tree has been reported to depend on the stress conditions of adjoining segments [Gan 2002][Gan 2003], where an "interconnect tree" has been defined as a unit of continuously connected high conductivity metal lying within one layer of metallization [S.Hau-Riege 2000]. In this paper, the reliability of the segments in the interconnect trees is further investigated to validate the applicability of the immortality criteria, $(jL)_{crit}$, determined in single-segment trees, for segments within multi-segment interconnect trees.

4.2 EXPERIMENTS

Experiments were performed by Choon-Wai Chang, a student from Singapore-MIT Alliance. Chang carried out the experiments at National University of Singapore. Package-level electromigration tests were carried out on simple two-segment interconnect trees consisting of straight via-terminated lines with an additional via in the

middle that creates two segments ('dotted-I' structures). Most experiments were carried out in lines with two 25μm-long segments each, and unless otherwise noted, it should be assumed that the segments were 25μm-long. In some cases the lines had a total length of 20μm with two segments of length 10μm each. Via-below (M2-type) dotted-I structures were 0.28μm-wide test structures in the metal-2 layer connected to wide leads in the metal-1 layer (Figure 4.1). The inter-level dielectric (ILD) was SiO_2, with Ta as the diffusion barrier and silicon nitride as the capping dielectric. The current density in the right segment was kept constant at 0.5 MA/cm^2 with the electrons flowing from the right via towards the middle via, while the current density in the left segment was varied, with values of 0, 0.5, 1.5 or 2.5 MA/cm^2, and with electrons flowing either into or out of the central via. The current density in the left segment (j_L) was defined to be positive if the electron flow direction was the same as in the right segment (see Figure 4.1(a)).

There were 16 samples in the population for each of the test condition. All the samples were stressed at 350°C in the EM tester. The samples were stressed for 780 hours until a failure criterion of a 30% resistance increase was met. Failure sites of

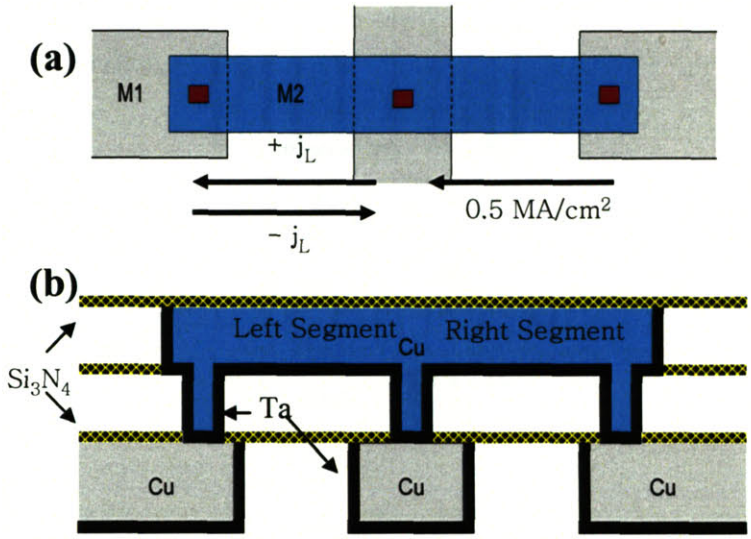

Figure 4.1 (a) Top and **(b)** cross-sectional view of the dotted-I test structure. The arrows indicate the directions of the electron flow.

selected samples were characterized using focused ion beam (FIB) milling with scanning or transmission electron microscopy.

4.3 EXPERIMENTAL RESULTS

Tests were carried out at a current density in the right segment that was not expected to cause failure in an individual isolated segment of 25μm length. Due to the small number of failures in some of the test configurations, the percentages (or fractions) of the population that had failed at the end of the experiments are used for comparison instead of the median-time-to-failure. The percentages of the population

Table 4.I

Percentages of the 50μm-long dotted-I (25μm segment) that failed, for individual segments and for the overall structure. The arrows indicate the electron flow directions. R denotes the right segment and L the left segment. Also shown are the percentage of the failures that occurred first in the right or left segments, and the percentage of the samples that failed simultaneously in both the right and left segments.

Test Configuration (MA/cm^2)	**Total Failed** (% of population)			**Failure Sequence** (% of total failed)		
	R	**L**	**Overall**	**R first**	**L first**	**R = L**
2.5 ← ← 0.5	68.8	68.8	81.2	46.2	38.5	15.4
1.5 ← ← 0.5	62.5	43.8	62.5	80	10	10
0.5 ← ← 0.5	37.5	12.5	37.5	100	0	0
0 ← 0.5	18.5	0	18.5	100	0	0
0.5 → ← 0.5	14	14	20	40	40	20
1.5 → ← 0.5	46.2	46.2	53.8	75	25	0
2.5 → ← 0.5	35.7	50	57.1	20	80	0

Table 4.II

Failure percentages for the 20μm-long dotted-I (10μm segment).

Test Configuration (MA/cm^2)	**Total Failed** (% of population)			**Failure Sequence** (% of total failed)		
	R	**L**	**Overall**	**R first**	**L first**	**R = L**
0.5 ← ← 0.5	12.5	6.2	12.5	100	0	50
0 ← 0.5	0	0	0	0	0	0

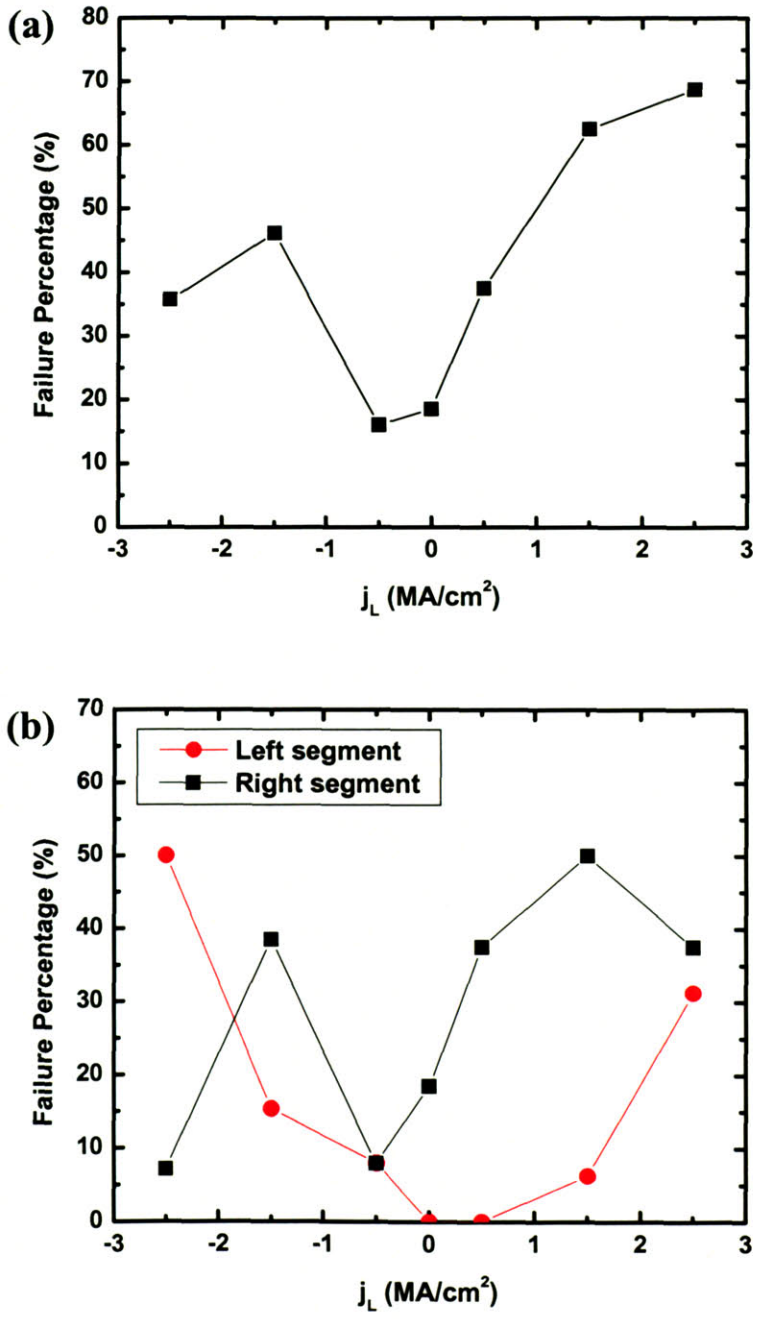

Figure 4.2 (a) Plot of the percentages of samples in which the right segment failed, as a function of the current density in the left segment, j_L. **(b)** Plot of the percentage of the samples that failed with failure occurring first in the left or right segments, or with failure occurring simultaneously in both segments.

that failed in the left segments, right segments, and anywhere in the overall structure (where the dotted-I was considered failed when either the left or right segment had failed) for all the test conditions on 50μm-long (25μm segment) lines are tabulated in Table 4.I. Also given in the table is the percentage of the lines that either failed first in the left segment, failed first in the right segment, or that failed in both the left and right segments simultaneously. Table 4.II shows data for the 20μm-long lines (10μm-long segments). The percentage of the samples that failed in the right segment and the percentage of the samples that failed *first* in either the left or right segment, are plotted for the 50μm-long (25μm-long segment) lines as a function of the current density in the left segment (j_L) in Figure 4.2.

Results from focused ion milling and electron microscopy are shown in Figures 4.3 through 4.6. Figure 4.3 shows scanning electron micrographs of typical samples that failed in the right segment, either at the cathode end (Figure 4.3(a)) or near the anode or central via. Figure 4.4 shows a transmission electron micrograph of an unusual failure indicating liner failure at the central via. Figure 4.5 shows a scanning electron micrograph of a typical sample that failed at the cathode of the left segment, where failure in the right segment was detected earlier. Figure 4.6 shows unusual

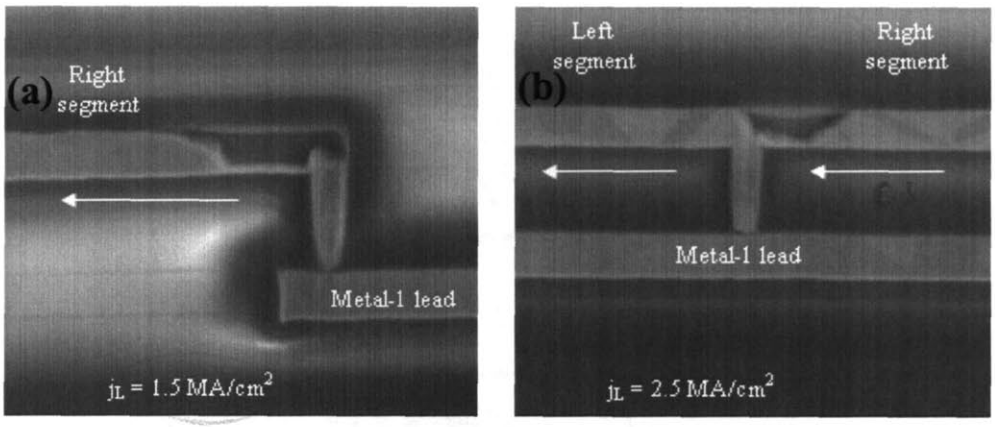

Figure 4.3 SEM images for the voids formed in the right segments either **(a)** at the cathode or **(b)** at region close to the central via, though the left segments had higher current densities. The arrows indicate the directions of electron flow.

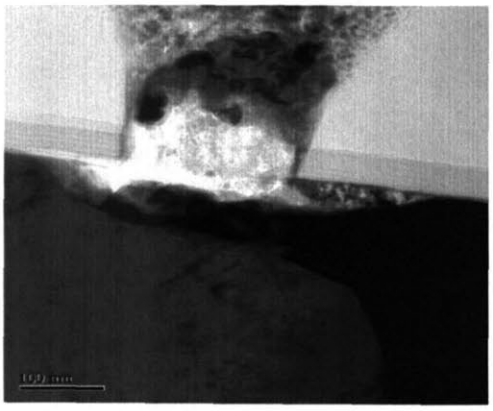

Figure 4.4 TEM image of the central via for the failed sample where j_L = -0.5 MA/cm^2.

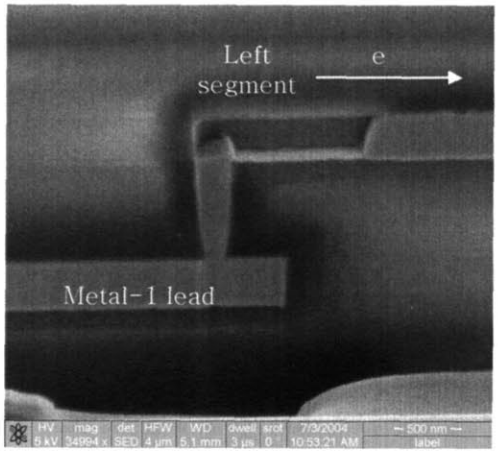

Figure 4.5 SEM image for the large volume void in the left segment for j_L = -1.5 MA/cm^2 where the right segment first failed.

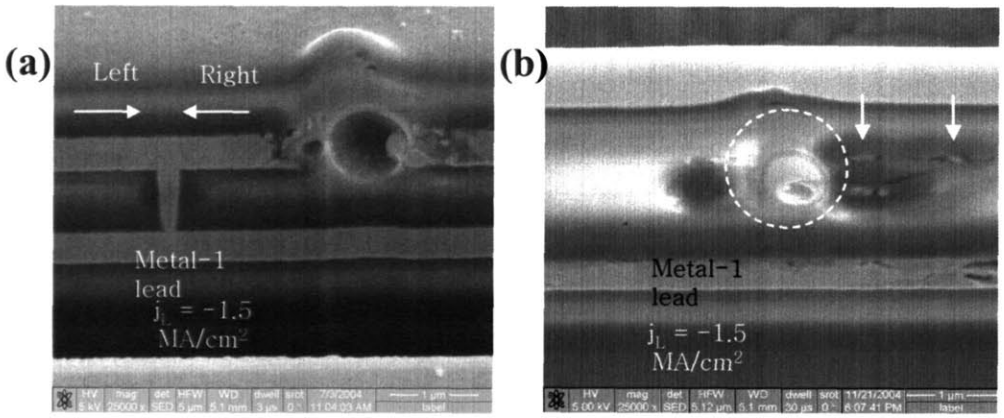

Figure 4.6 (a) SEM image of a failure site near the central via in the right segment for j_L = -1.5 MA/cm^2. The arrows indicate the directions of the electron flow. **(b)** SEM image of the trace of metal extrusion at the Cu/Si_3N_4 interface parallel to the test line. The arrows indicate the extruded metal with clear dielectric cracks, while the dashed-circle is the erupted failure site in (a). The M2 test line is not visible as it had been over-cut.

failures of the same sample in Figure 4.5, in which the right segment failed catastrophically, despite a higher opposing current in the left segment.

4.4 DISCUSSION

In all experiments, the *jL* product in the 25μm-long right segment was 1250 A/cm, which is below the values of 3700 A/cm and 1500 A/cm at which EM-induced failure is reported to occur for similar M2 structures [Lee 2001] and M1 (via-above) structures [C.Hau-Riege 2002], respectively. Despite this, complete immortality (0% failed) was not found in our experiments on 25μm-long segments, even when the current density in the left segment was zero. Moreover, the mortality (percent that failed) of the right segment in the dotted-I structure was found to depend on the direction and magnitude of the current in the adjacent left segment. Riege and Thompson [Riege 1998] and Clement *et al.* [Clement 1999] recognized these effects as being due to interacting segments acting as sinks or reservoirs for diffusing atoms, and suggested that immortality of a multi-segment interconnect tree can be determined through calculation of an *effective jL* product, $(jL)_{eff}$ given by

$$(jL)_{eff} = \left(\sum_i j_i L_i \right)_{\max}, \tag{4.4}$$

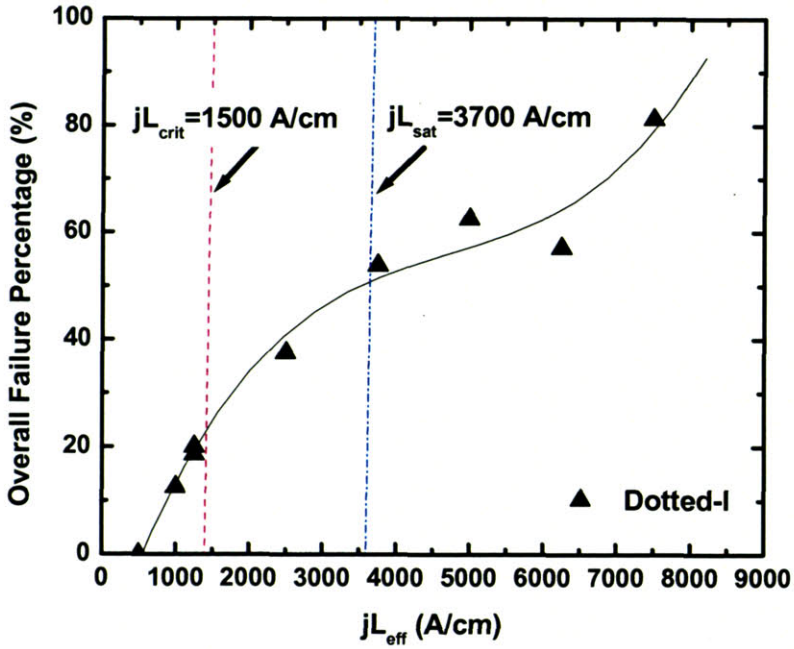

Figure 4.7 Plot of the overall failure percentage of the tested structures for tests carried out under conditions leading to different values of $(jL)_{eff}$. Absolute immortality was obtained from 10μm-segment dotted-I with [0 ←0.5 MA/cm^2] test configuration.

where j_i and L_i are the current density and length of individual segments and the sum is taken over all possible paths through the tree, with $(jL)_{eff}$ given as the maximum of these sums. Figure 4.7 shows the overall failure percentages of the dotted-I as a function of $(jL)_{eff}$. Also shown in Figure 4.7 are the expected failed percentage for $(jL)_{crit}$ = 1500 A/cm and $(jL)_{sat}$ = 3700 A/cm.

It can be seen that the failure percentage decreases monotonically with decreasing $(jL)_{eff}$ and goes to zero at finite $(jL)_{eff}$. However, the transition to full immortality is not sharp, with some lines with high $(jL)_{eff}$ proving to be immortal, and some lines with low $(jL)_{eff}$ proving to be mortal. The rest of this discussion will focus on these differences from expected behavior.

4.4.1 Active and Passive Reservoirs

A reservoir can be defined as the extension of an electrically stressed line either at the cathode or the anode side. A reservoir at the cathode end can be treated as an atomic source for the test line, while it is an atomic sink at the anode end. A reservoir is considered as 'active' when it carries electrical current and 'passive' if there is no current in it.

The failed population of the right segments was observed to increase with increasing current density in the left segment for electron flow in and out of the central via, with the smallest percent failing when j_L = -0.5 MA/cm^2, the case for which the atomic fluxes into the central via was counter-balanced in the two segments. For the cases of j_L = 0.5, 1.5 and 2.5 MA/cm^2, for which the electron flows of the two segments were in the same direction, over one third of the samples' right segments failed earlier

than the left segments, even though the current densities in the left segments were higher. This is due to the right segment serving as an active atomic source for the left segment in these cases. The atomic flux from the right segment to the left segment relaxes the tensile stress built-up in the left segment at the central via, and accelerates the build-up of tensile stress at the cathode-end of the right segment. Voids can form either near the cathode via of the right segment for moderate current density in the left segment (j_L = 1.5 MA/cm^2), or in a region close to the middle via for a large current density in the left segment (j_L = 2.5 MA/cm^2), as shown in figure 4.3.

4.4.2 Failures at Low $(jL)_{eff}$ with Inactive Segment

To gain insight into the interactions of the interconnect segments, stress evolution was simulated using the 1-D electromigration finite-differential equation solver [Choi 2004] for all the test conditions. The increased mortality of the right segment with increasing j_L was found to match with the simulated results as shown in Figures 4.8(a)-(d). The simulations show that when electrons flowed in the same direction in both segments, the time to reach the critical tensile stress for void nucleation of 40 MPa [S.Hau-Riege 2002] at the cathode of the right segment reduced with increasing current density in the left segment. Void nucleation in the right

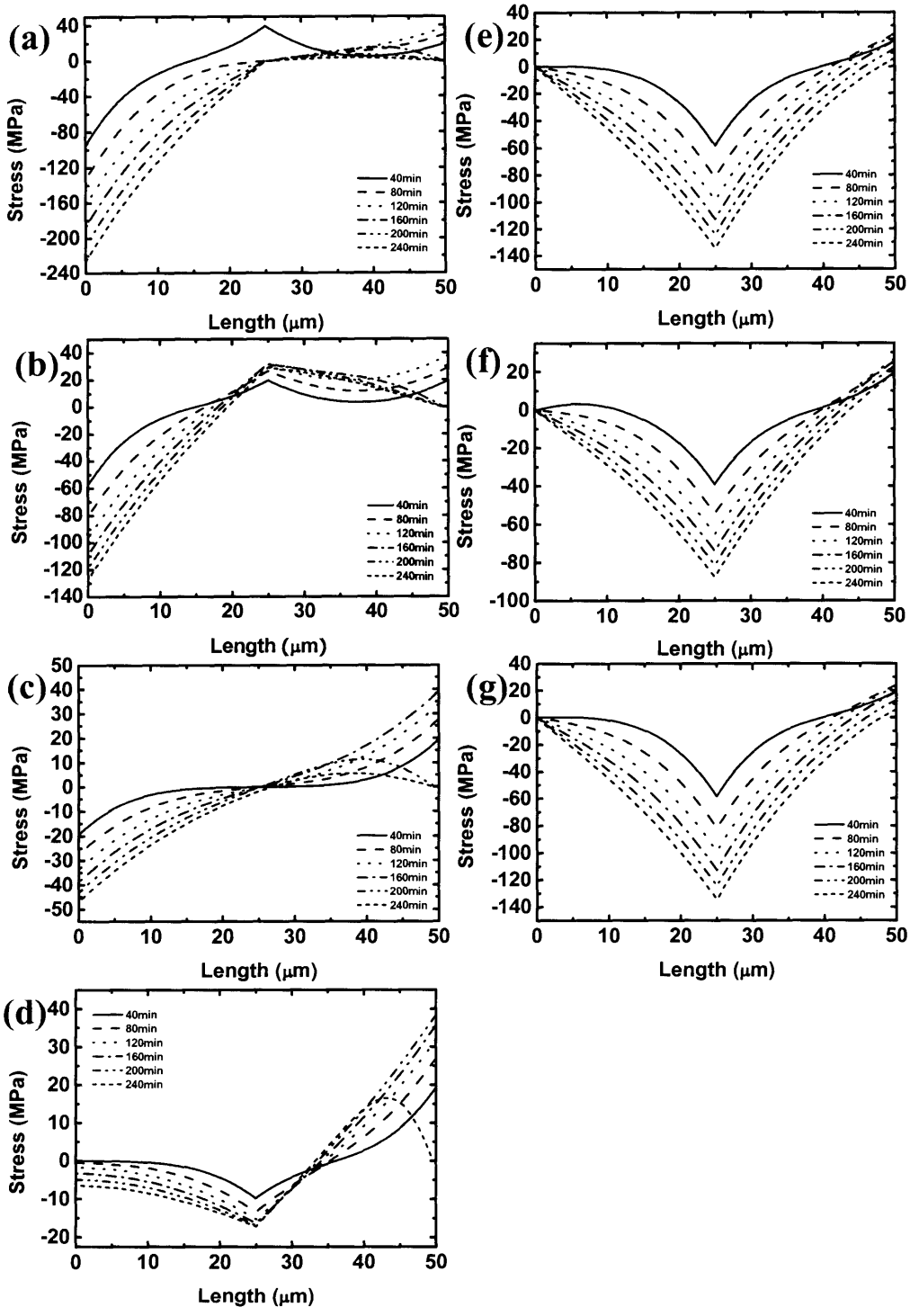

Figure 4.8 Simulated stress evolution for various test. conditions shown in Table 4.I.

segment is also predicted when the left segment is inactive (j_L = 0), since even in this case the left segment serves as an inactive sink for atoms from the right segment. The effects of inactive segments are not accounted for in the definition of $(jL)_{eff}$. This causes the unexpected mortality observed at low $(jL)_{eff}$ shown in Figure 4.7, for j_L = 0 and segment length equal to 25μm.

The segment that failed earlier could also serve as an inactive sink for the other surviving adjacent segment. For example in the case where j_L = -2.5 MA/cm^2, most of the left segment failed earlier than the right segment as shown in Figure 4.2(b). The segment with higher current density fails first and becomes an inactive segment while the adjacent right segment is still active. This causes the failure percentage of the right segment to increase with the current density in the left segment as well when the electron flow was in the opposite direction.

4.4.3 Accounting for the Effects of Inactive Segment

Consider the cases shown in figure 4.9, which compares the steady state stress distribution in an isolated active segment of length a, with the case in which the active segment is connected to a passive segment of length p. In the case that void nucleation does not occur, the peak tensile stress is higher when there is a passive reservoir. The

presence of a passive reservoir therefore makes void nucleation (and failure) more likely.

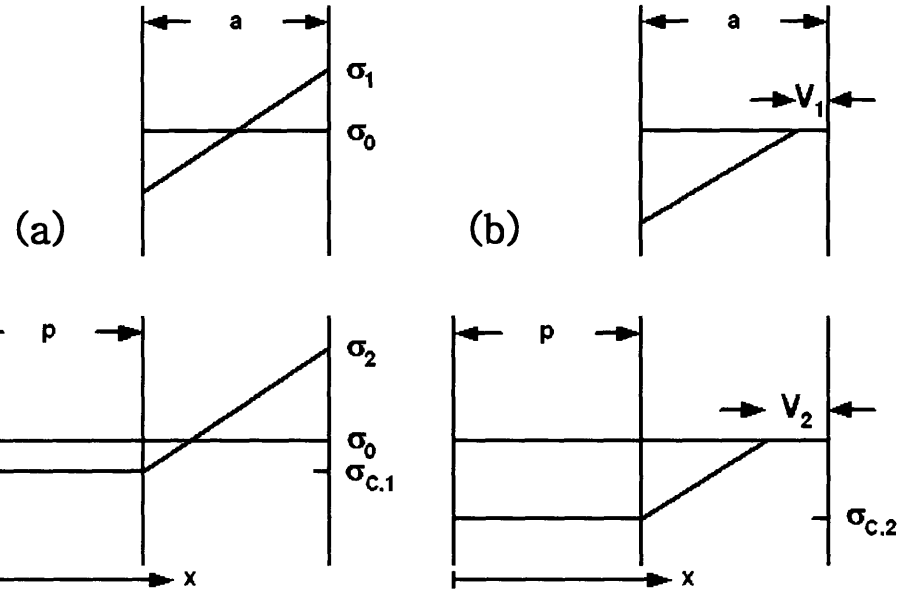

Figure 4.9 Schematic illustration of the balanced stress distribution with and without a passive segment for the cases **(a)** when void nucleation does not occur (the peak tensile stress is higher when there is a passive reservoir) and **(b)** when void growth saturates (the void length at saturation is larger when there is a passive reservoir).

The stress is related to the atomic concentration by $C=C_0\exp(-\sigma/B)$, or for small σ, $C \approx C_0[1-(\sigma/2B)]$. If σ_0 is the equilibrium stress, it can be shown that mass conservation requires that

$$\sigma_{\max} = \sigma_2 = \frac{Z^* \rho j e}{2\Omega}\left(\frac{2ap + a^2}{a + p}\right). \tag{4.5}$$

The criterion for immortality is therefore that $(jL)_{eff} < (jL)_{crit}$ *and* $\sigma_{max} < \sigma_{nuc}$, where σ_{nuc} is the stress required for void nucleation.

If a void nucleates, but its growth saturates before leading to failure, the steady state stress distribution will be as shown in figure 4.9(b). The presence of a passive segment leads to a higher void size at saturation, and is therefore more likely to lead to failure. It can be shown that:

$$V_{\max} = wh\left\{a + p - \frac{2B}{K}\left[\sqrt{\left(\frac{Kp}{2B} + 1\right)^2 + \frac{aK}{B}} - 1\right]\right\}, \tag{4.6}$$

where w is the segment width, h is the segment thickness, and $K = Z^* \rho j e/\Omega$. The criterion for immortality is therefore that $(jL)_{eff} < (jL)_{sat}$ and $V_{max} < V_{fail}$, where V_{max} is the maximum void volume and V_{fail} is the void volume that leads to failure. Equations (4.5) and (4.6) are derived in the appendixes.

4.4.4 Failures at Low $(jL)_{eff}$ with Liner Failure

The other case in which unexpected high failure rates occurred at low $(jL)_{eff}$ is when $j_R = |-j_L|$. In this case, as shown in figure 4.8(e), a compressive stress is expected to develop at the central via. However, in some cases the liner at the central via was found to have been non-blocking (as shown in Figure 4.4). This could be the result of a discontinuous liner in the as-fabricated structure or could have resulted from rupture of the liner caused by the compressive stress. In either case, a non-blocking liner at the central via allows the wide metal-1 lead to serve as an active sink for electromigrating atoms from the metal-2 segments, and will lead to continued build-up of tensile stresses in these segments and eventually to their failures.

4.4.5 Unexplained Failures

When the electron flow direction is toward the central via in both segments, and the left segment had higher current, failure is expected to occur first at the cathode of the left segment. However, this was not always observed in our experiments especially when $j_L = -1.5 A/cm^2$, where very long void can be formed in the left segment. Figures 4.5 and 4.6 show failure sites for such samples. Not only did the right segments fail first, but they failed catastrophically near the central via rather than at the cathode end of the right segment. These results are difficult to explain. However, the micrograph

in figure 4.6(b) suggests that failure is associated with compressive decohesion at the Cu-silicon nitride interface. This would result in Cu extrusion and copious Cu voiding near the extrusion site.

4.5 CONCLUSIONS

The mortality of a multi-segment interconnect tree is governed by interactions among the segments, not by the stress conditions in individual segments. The existence of an active or passive reservoir causes the electromigration behavior of an interconnect tree to be very different compared to straight via-to-via lines, which was confirmed through experiments and simulations. The probability of failure was shown to depend on the *effective jL* product, $(jL)_{eff}$, with immortality occurring when $(jL)_{eff}$ was sufficiently low. However, the effects of inactive segments must be accounted for in order to predict immortality based on $(jL)_{eff}$. It was also shown that failures can occur for low values of $(jL)_{eff}$ when liners are missing or ruptured. Testing of multi-segment trees allows greater flexibility in testing to reveal different failure mechanisms, and different constraints on immortality.

4.6 ACKNOWLEDGEMENTS

The research was funded by the Singapore-MIT Alliance and the Semiconductor Research Corporation. The authors would like to thank C. K. Cheng (JK) from the Institute of Microelectronics Singapore for his support and fruitful discussion of the experimental results.

4.7 APPENDICES FOR CHAPTER 4

4.7.1 Maximum Stress at Steady State

Consider an interconnect tree in steady state as shown in figure 4.9(a). The stress along the direction x in the right segment is given by

$$\sigma(x) = \frac{Z^* \rho j e (x - p)}{\Omega} + \sigma_{C,1}, \tag{4.A1}$$

where $\sigma_{C,1}$ is the steady stress in the left segment. Since mass is conserved, by approximating $C = C_o \exp(-\sigma_{C,1}/B) \approx C_o[1-(\sigma_{C,1}/2B)]$,

$$C_o A(a+p) = C_o A\left[\int_0^p (1 - \frac{\sigma_{C,1}}{2B})dx + \int_p^{a+p} (1 - \frac{K(x-p)+\sigma_{C,1}}{2B})dx\right], \tag{4.A2}$$

where A is the cross-sectional area of the line and $K = Z^* \rho j e/\Omega$. Solving for $\sigma_{C,1}$,

$$\sigma_{C,1} = \frac{K(ap - \frac{a^2 + 2ap}{2})}{a+p} = \frac{-Ka^2}{2(a+p)} \qquad (4.A3)$$

For a single segment of line length a in steady state with $\sigma_o = 0$, the maximum tensile stress is given by

$$\sigma_1 = \frac{Z^* \rho j e a}{2\Omega}. \qquad (4.A4)$$

When an adjacent segment is present, the same stress gradient develops in the right hand segment (when the same current density is used), but in the steady state the compressive stresses at the end of the segment is reduced. The new stress at the compressive end is given by

$$\sigma_{C,1} = \sigma_{max} - \frac{Z^* \rho j e a}{\Omega} = \sigma_{max} - Ka. \qquad (4.A5)$$

Combination of equations (4.A3) and (4.A5) gives

$$\sigma_{max} = \sigma_2 = \frac{Z^* \rho j e}{2\Omega}\left(\frac{2ap + a^2}{a + p}\right). \qquad (4.A6)$$

4.7.2 Maximum Void Length at Steady State

If a void nucleates but its growth saturates before leading to failure, the steady state stress distribution will be as shown in figure 4.9(b). The presence of a passive segment leads to a larger void size at saturation, and is therefore more likely to lead to failure. If we assume that the void spans the width w and thickness h of the segment, mass conservation requires that for a void volume at saturation of V_2,

$$C_o A(a + p) = C_o A\left[\int_0^p (1 - \frac{\sigma_{C,2}}{2B})dx + \int_p^{d+p} (1 - \frac{K(x - p) + \sigma_{C,2}}{2B})dx\right], \qquad (4.A7)$$

where $d = a\text{-}(V_2/wh)$. Hence,

$$a + p = p - \frac{\sigma_{C,2}}{2B} p + d - \frac{K(d^2 + 2dp)}{4B} + \frac{Kdp}{2B} - \frac{d\sigma_{C,2}}{2B} \qquad (4.A8)$$

Since $\sigma_{C,2} = -Z^* \rho j e d/\Omega = -Kd$,

$$d = \frac{2B}{K}\left[\sqrt{\left(\frac{Kp}{2B}+1\right)^2 + \frac{aK}{B}} - 1\right] - p \qquad (4.A9)$$

The maximum void size at saturation V_{max} is then given by

$$V_{max}/wh = V_2/wh = a - d = a + p - \frac{2B}{K}\left[\sqrt{\left(\frac{Kp}{2B}+1\right)^2 + \frac{aK}{B}} - 1\right] \qquad (4.A10)$$

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CHAPTER 5

EFFECTS OF TEXTURE ON THE FORMATION, SHAPE, AND MOTION OF VOIDS DURING ELECTROMIGRATION IN PASSIVATED COPPER INTERCONNECTS

ABSTRACT

In-situ scanning electron microscope (SEM) observations have been performed on passivated damascene Cu interconnect segments of different widths during accelerated electromigration (EM) tests. In some cases, voids form and grow at the cathode. However, an alternative failure mode is also observed, during which voids form distant from the cathode end of the interconnect segment and drift toward the cathode where they eventually lead to failure. The number of observations of this failure mode increased with increasing line width. During void motion, the shape and the velocity of the drifting voids vary significantly. Post-mortem electron back-scattered diffraction (EBSD) analysis was performed after in-situ testing and a correlation of EBSD data with the in-situ observations reveals that locations at which voids form, their shape evolution, and their motion all strongly depend on the locations of grain boundaries and the crystallographic orientations of neighboring grains.

5.1 INTRODUCTION

It is well established that electromigration in confined metal interconnects can lead to tensile stresses that can cause void nucleation and growth [[Korhonen 1993]. In via-terminated interconnect segments, electromigration is usually blocked by

refractory metal liners found at the base of the vias. Therefore, when an electrical current is applied, electromigration leads to stress evolution such that a maximum tensile stress occurs at the cathode-end via. This via is therefore generally expected to be the most probable location for the nucleation of a void. More specifically, for the case of Cu-based interconnects, voids are typically located at the interface between Cu and the top passivation layer, very close to the via at the cathode. This preferred site for nucleation is due to the weak Cu/Si_3N_4 interface, which has a poor adhesion [Lloyd 1995] and a high diffusivity [Hu 1997, Arnaud 1999]. The dominant failure mechanism of interconnects in metallization segments with vias below the interconnects is reported to be void growth above the via at the cathode end [Lee 2001], which eventually causes an electrical open circuit.

Recent failure analysis and in-situ scanning electron microscopy (SEM) experiments show that voids can not only nucleate at the cathode, but often also form away from the cathode, and then drift toward the cathode to cause open circuit failure by diving into the via [Meyer 2002, Zschech 2004, Choi 2006]. The behavior of a void as it drifts can lead to critical variations in the failure characteristics and failure time. In order to estimate or improve reliability it is therefore important to better understand void motion and determine factors influencing it. In this study, accelerated in-situ

electromigration tests were performed in an SEM. Post-failure Electron Backscatter Diffraction (EBSD) analysis was carried out to correlate behavior observed during testing with miocrostructural features and characteristics.

5.2 EXPERIMENTAL PROCEDURE

5.2.1 Test Structure

Nucleation, growth and motion of voids were observed by performing accelerated electromigration (EM) tests in an SEM at elevated temperatures and current densities. The orientations of grains at the Cu/Si_3N_4 passivation-layer interface were identified after the tests using back-scattered diffraction (EBSD) analysis. By observing the location, drift rate, and size of the voids, we investigated the relationship between diffusivities at the Cu-capping layer interface for Cu grains of different orientations. In this experiment, we used interconnects that were fabricated by Sematech Inc, in which the test structures were located in the second metallization layer (M2). The test structures were 1000μm long, 0.45μm thick and had a width of either 0.3μm, 1.0μm or 2.25μm. The interlayer dielectric (ILD) was SiO_2 and the passivation layer was a 200nm-thick layer of Si_3N_4. The Cu was lined on both sides and the bottom with a 25nm-thick Ta layer.

5.2.2 Thinning Passivation

Before testing we used a focus ion beam (FIB) Microscope to reduce the thickness of the Si_3N_4 to roughly 100nm to be able to obtain SEM images of good quality of the underlying metal (Figure 5.1). The FIB can mill material through bombardment and sputtering with Ga ions. Thus, the material that is used in an FIB is typically doped by trapped Ga ions. Ion beam current of 300pA and accelerating voltage of 30kV were used for milling. Depending on the material and Ga ion energy, the penetration depths of Ga ions vary. In our case the penetration depth of Ga ions in Si_3N_4 was estimated using the simulation with SRIM [SRIM], which indicated that a negligible number of Ga ions came to rest at depths of 50nm or more in Si_3N_4. Thus, when we milled the Si_3N_4 with roughly 100nm remaining thickness, it can be safely assumed that Ga did not affect the Cu/passivation layer interface or any of the observed in-situ phenomenology. The FIB used was an FEI Strada DB235 located at Center for Nanoscale Systems (CNS) at Harvard University. A 5μm x 10μm window was milled at a rate of 10nm/min. After this treatment the quality of SEM images showing voids underneath the 100nm-thick passivation was significantly improved.

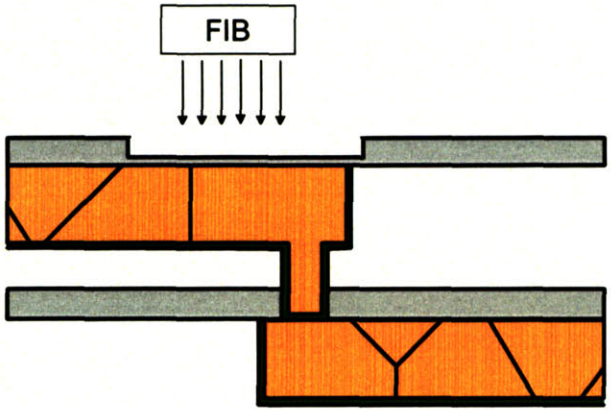


Figure 5.1 Si_3N_4 passivation layer thinning process using focused ion beam (FIB). Thinning process enables to see Cu/Si_3N_4 interface more clearly using SEM.

5.2.3 In-Situ SEM

After the FIB sample preparation, samples were mounted and gold-wire bonded onto a commercial 24-pin ceramic package. The sample was attached using Duralco 124 silver filled epoxy to withstand the elevated temperature of the accelerated electromigration test. The epoxy was cured prior to wire bonding at 120°C in a furnace for 50 minutes. The package was then mounted onto a custom-made SEM sample holder which was connected to an electrical feed-through for application of electrical current to the test structures and the resistive heater. The SEM sample holder with the ceramic package was inserted into the SEM. We used a JEOL 450 tungsten filament SEM which was located at the Rowland Institute at Harvard. The sample was heated to the desired temperature of 370°C and the temperature was measured using a

thermocouple that was securely attached to the heated ceramic package. There was severe image drift caused by thermal expansion during heating, therefore the sample was heated at the same electrical power for at least 10 hours prior to starting the tests, to avoid sample drift during the SEM observation. Accelerated EM tests were then performed using a current density of 3.0 MA/cm^2. The base pressure of the chamber was $1x10^{-6}$ torr during the tests. The tests were terminated when the sample met the failure criterion of an open circuit. SEM images of the Cu /passivation interface around the thinned Si_3N_4 region of the sample were taken in top view and were automatically recorded every 165 seconds using a computer and custom-written software. The beam current was 1 nA, the accelerating voltage was 20 kV, and the working distance was chosen to be 20mm to reduce heat transfer from the hot stage to the SEM column. The resistance of the samples was recorded throughout all experiments.

5.2.4 EBSD

After the tests, the samples were carefully removed from the ceramic package, and the remaining passivation layers were fully removed using the FIB. EBSD analysis was used to map the crystallographic orientations of the grains in the region that had been observed during the in-situ experiments. EBSD analysis was performed with a

system from HKL using a Channel 5 detector that was mounted to a SEM with a Schottky Emitter (Leo 982) at CNS at Harvard University. For EBSD measurements, the sample was tilted at 70° with working distance of 8mm, and an accelerating voltage of 19kV was used.

5.3 RESULTS

Out of ten 0.3μm-wide samples, two samples formed voids away from the cathode. In the 1.0μm-wide samples, three out of seven samples formed voids away from the cathode and all four of the samples that were 2.25μm-wide formed voids distant from the cathode. A summary of these and other observations is given in Table 5.I. For all samples in which voids formed at a distance from the cathode, voids were never subsequently observed to form at the end of the cathode.

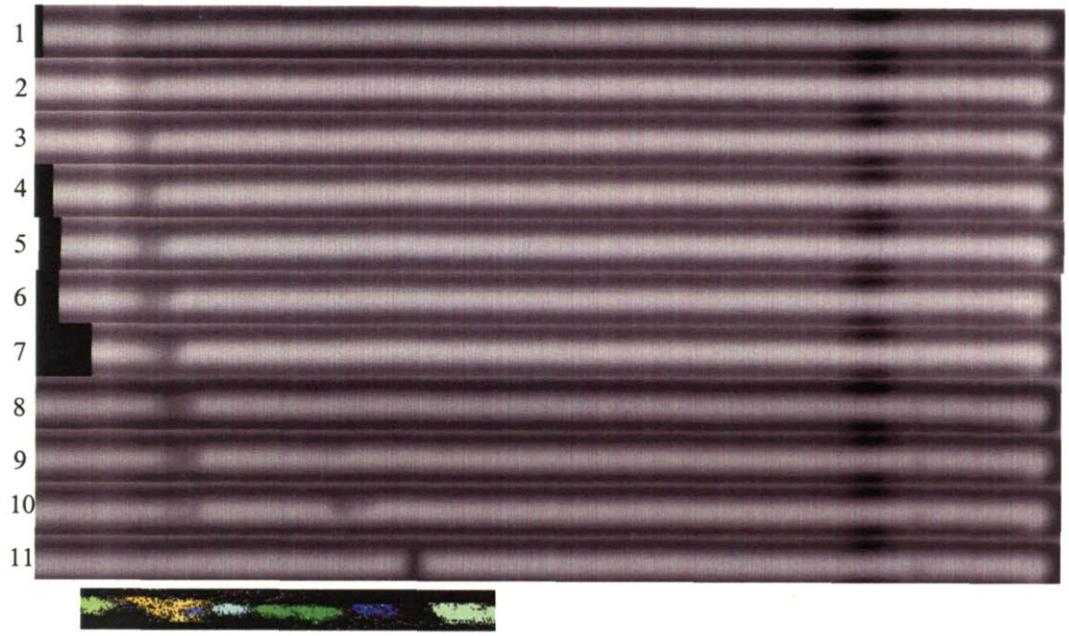
Table 5.I

Summary of Experimental Results

	Grains per width	Likely to form voids away from cathode	Number of voids away from cathode	Location of first void away from cathode	Distance void drifted	Void drift velocity (nm/min)	TTF of samples with void away from cathode
0.3μm	Mostly 1	Low (2 out of 9)	1 or 2	12~13μm away	1~2μm	3.31	~1000min
1.0μm	1~3	Intermediate (3 out of 7)	1 or 2	More than 13μm away	To or close to cathode end	7.62	1000~2750min
2.25μm	2~5	High (4 out of 4)	3 to 7	Within 3μm away	To cathode end	46.22	Less than 300min

5.3.1 Void Drifting in 1.0μm and 2.25μm Width Samples

For the samples with 1.0μm and 2.25μm widths, voids that had formed away from the cathode drifted toward the cathode. In one case, a 1.0μm-wide line failed when a void grew to span the width and thickness of the interconnect after drifting close to, but not all the way to, the end of the cathode (Figure 5.2(c)). In all other 1.0μm and 2.25μm-wide samples, open circuit failures were detected after the voids reached the end of the cathode.



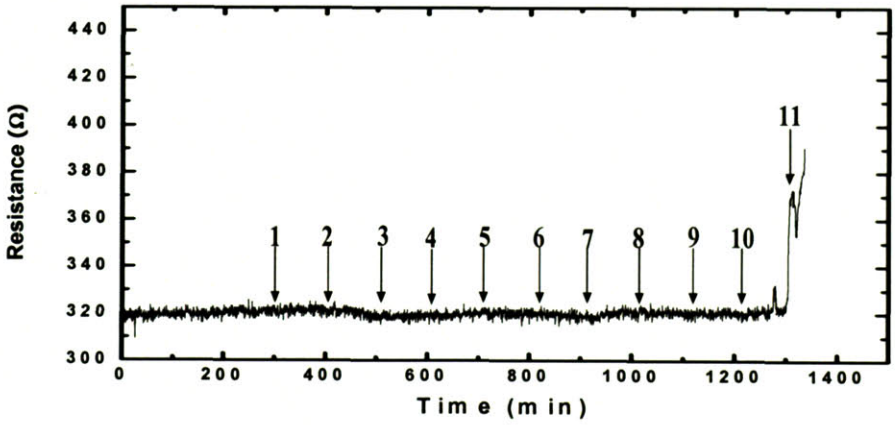


Figure 5.2(a) In-situ SEM images of the voids from the top view with out of plane orientation of the tested samples and resistance during the test. The width of the test structure is 0.3μm.

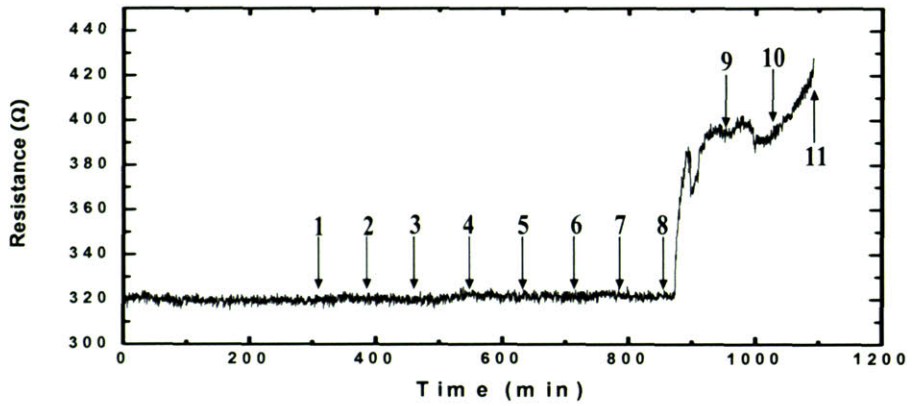


Figure 5.2(b) In-situ SEM images of the voids from the top view with out of plane orientation of the tested samples and resistance during the test. The width of the test structure is 0.3μm.

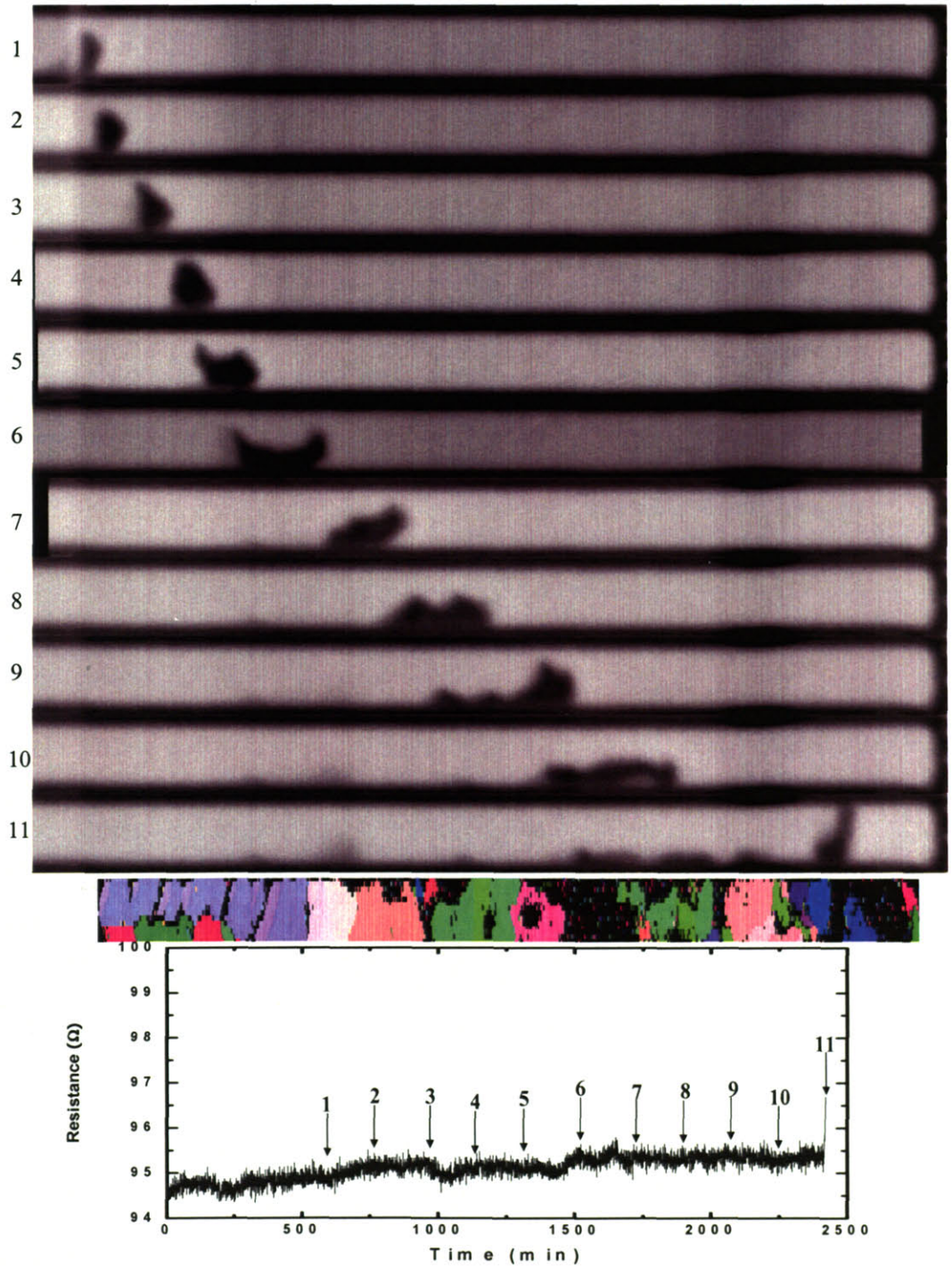


Figure 5.2(c) In-situ SEM images of the voids from the top view with out of plane orientation of the tested samples and resistance during the test. Width of the test structure is 1.0μm.

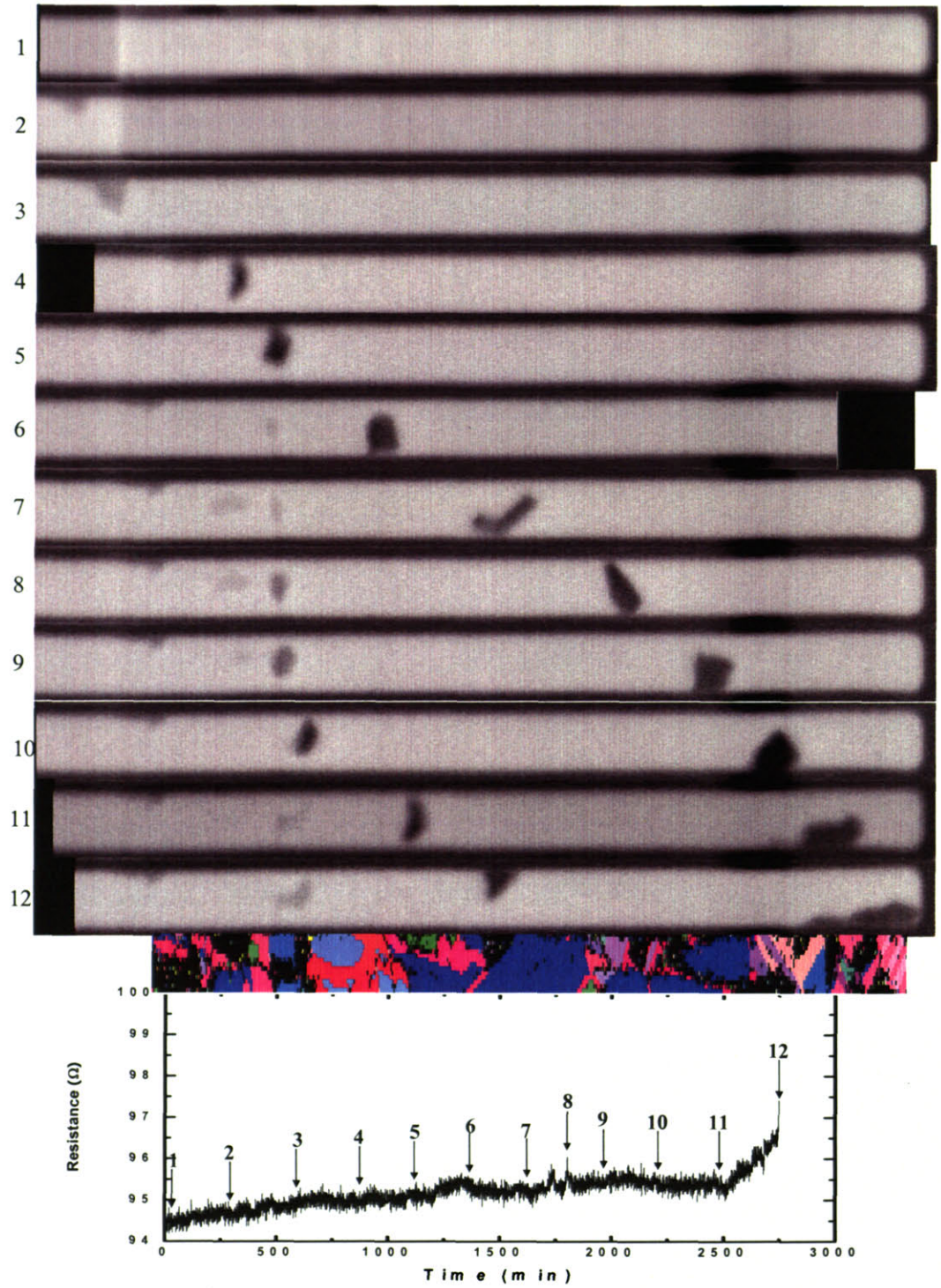


Figure 5.2(d) In-situ SEM images of the voids from the top view with out of plane orientation of the tested samples and resistance during the test. Width of the test structure is 1.0μm.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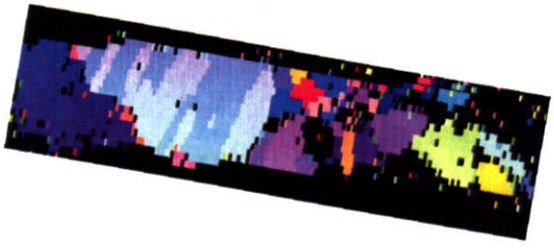

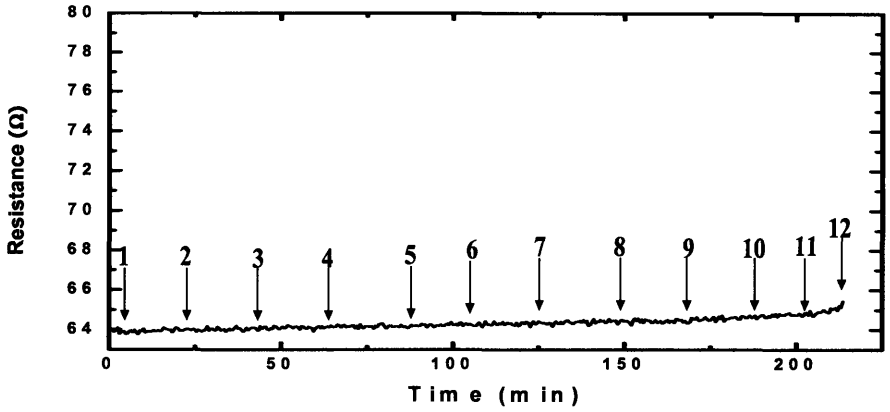

Figure 5.2(e) In-situ SEM images of the voids from the top view with out of plane orientation of the tested samples and resistance during the test. Width of the test structure is 2.25μm.

5.3.2 Void Drifting in 0.3μm Width Samples

In the case of the 0.3μm-wide interconnects, voids that formed away from the cathode did not drift all the way to the end of the cathode. Instead, after drifting for only one or two micrometers, the voids grew to span the width and thickness of the line and caused failure (Figures 5.2(a) and (b)). Very close to the time of failure it was observed that when the void nearly spanned the line, both the anode and cathode edges of the void still propagated slowly toward the cathode end of the interconnect. Once the void fully spanned the line, both edges of the void instantly changed their direction of motion and propagated away from the cathode end.

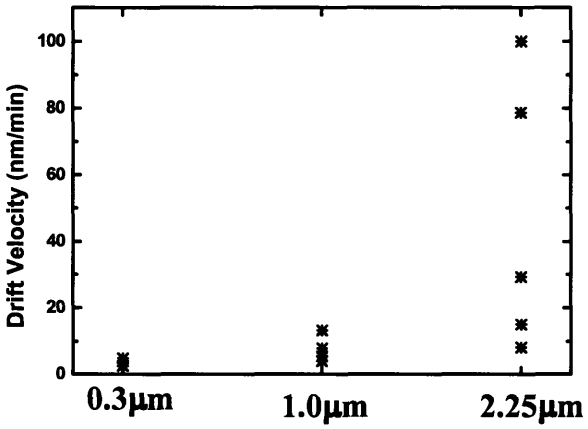

Figure 5.3 Void drift velocities at various line widths. Average drift velocities are 3.31nm/min (0.3μm), 7.62nm/min (1.0μm), and 46.22nm/min (2.25μm).

5.3.3 Void Drift Velocity

The void drift velocity changed substantially as voids drifted toward the cathode during all observations. Averaged drift velocities of individual voids are plotted in figure 5.3. D_s was extracted from the drift velocity and is compared and analyzed in a separate study [Choi Ch.6a]. Voids in 2.25μm-wide samples drift significantly faster than voids in 1.0μm and 0.3μm-wide samples. Drift velocities for 2.25μm-wide samples also have a very wide range, from 8.1nm/min to 100nm/min.

Table 5.II

Anode and cathode edges of the void as voids nucleate away from the cathode end of the interconnect.

Sample	Anode/Cathode
2.25μm wide	(2 4 7)/(10 13 21)
2.25μm wide	(3 2 6)/(18 19 27)
1.0μm wide	(2 3 12)/(8 11 12)
0.3μm wide	(1 0 1)/(15 13 18)

5.3.4 Grain Orientation Dependence on Voids

The EBSD data for the interconnects showed that in the wider lines there were more grain boundaries per length of the interconnect than in the narrower lines. In particular there were more grain boundaries oriented along the length of the interconnect in the wider samples. From the EBSD measurements, we also were able to locate the sites at which voids appeared in four samples including all widths. The orientations of the grains at the anode and cathode edge of the void are listed in Table 5.II.

In the 1.0μm-wide lines, the changes in size and shape of drifting voids were

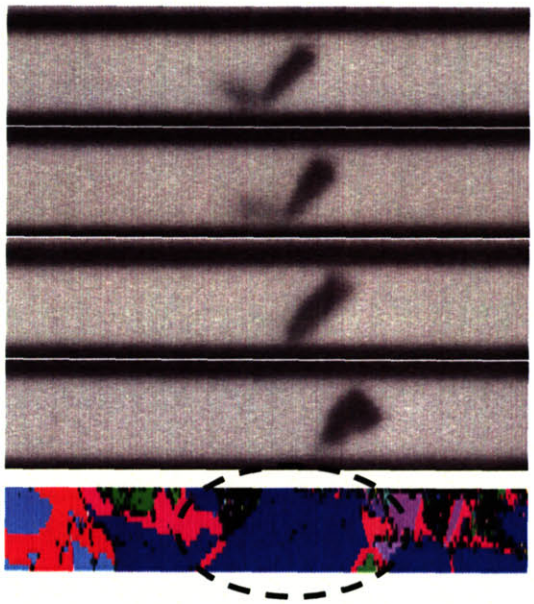

Figure 5.4 Shape of the void drifting in a single grain region is well maintained until the void reaches to the different grain.

observed in detail. EBSD results on these test lines also show that the shape of a void changed as it passed through or along grains with different orientations (Figures 5.2 (c),(d)). When a void moves within a single grain, the shape of the void is fixed as shown in Figure 5.4. The shape of the void changes drastically once the void moves into a different grain which can be also seen in Figure 5.4. In a few cases it was observed that the void shape within certain regions was different for different voids. Examples are shown in Figures 5.5 and Figure 5.6.

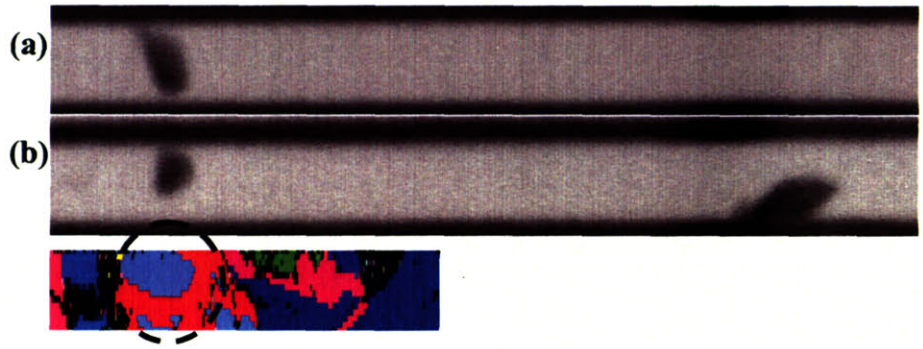

Figure 5.5 (a) First void passing through a circled region of the grain and **(b)** second void passing through a circled region of the grain. Cathode edge of the second void has the same shape as the grain, but the shape of the first void is different, suggesting that the grain has changed in the circled region after the first void drifted.

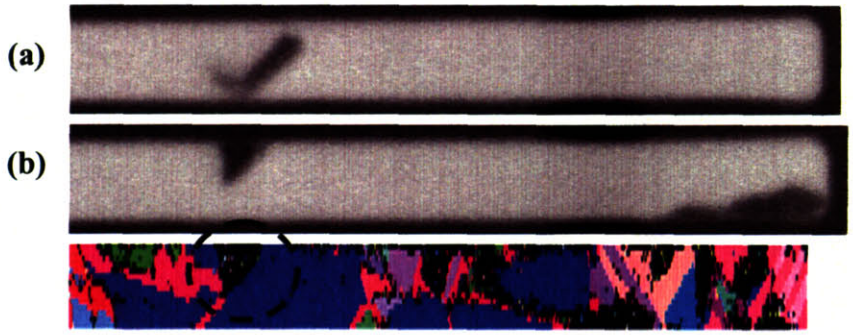

Figure 5.6 (a) First void passing through a circled region of the grain and **(b)** second void passing through a circled region of the grain. Both cathode edges of first and second void have similar angle, suggesting that the grain in that region has not changed.

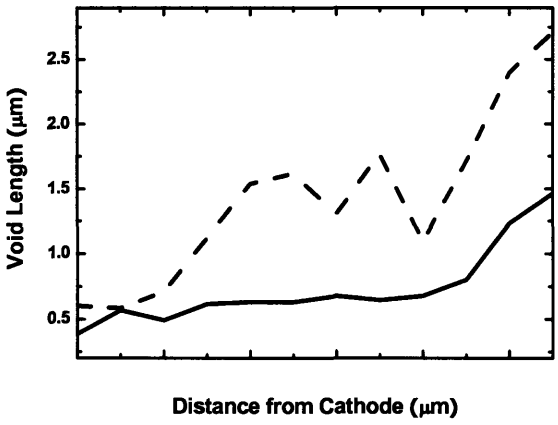

Figure 5.7 Length of the void vs. location of the void for the voids that nucleated away from the cathode. 1.0μm width samples.

5.3.5 Void Elongation and Residues

In general, the length of voids increased as the voids drifted closer to the end of the cathode and the increase was especially pronounced near the end of the cathode (Figure 5.7). Some voids left small residual voids behind, as can be seen in figure 5.8. For all samples with voids distant from the cathode, no void at the end of the cathode was observed. These observations will be analyzed in detail and discussed by Choi *et al* [chapter 7]. Residual voids sometimes grow and drift as shown in figure 5.2(d).

Figure 5.8 Void residues are observed that are left behind by the first void.

5.4 DISCUSSION

5.4.1 Failure by Voids Away from Cathode

The results of our in situ EM observations clearly show that two different failure modes exist in interconnects. EM failure mostly occurs by voids causing an electrical open at the cathode via, as has been found in numerous lifetime tests [Hu 1995, S. Hau-Riege 2002, C.Hau-Riege 2002, Ogawa 2002, Hauschildt 2006]. Our observations show that there are two modes that can lead to this failure. One is the formation of a void at or in the via, as has been discussed before, and is growth of voids at a distance from the via and their subsequent motion toward the cathode via. The failures observed in Figures 5.2(d) and (e) can be explained by voids diving into the via to cause failure at the bottom, as has also been observed in cross-sectional view in-situ SEM studies [Meyer 2002].

5.4.2 Effect of Grains on Void Growth

Voids initially grow in the locations at which they first appeared, before de-pinning and drifting toward the cathode. The locations of void appearance and initial growth were found to correlate with the locations of grain boundaries. The activation energies for diffusion of Cu atoms on Cu surfaces are known to vary on surfaces with different crystallographic orientations of the surface [Karimi 1995]. It is reasonable to expect that this will also be true for Cu/passivation-layer interfaces. Therefore, as illustrated in figure 5.9, assuming a bamboo structure, if a void is pinned at a grain boundary and the grain on the anode side of the void has a higher diffusivity than that on the cathode side of the void, the void will grow in size due to the flux divergence. After growing to a certain size, the void may de-pin from the grain boundary and drift toward the cathode [Borgesen 1992].

As a void drifts it can become pinned at another grain boundary. The grain size for the Cu used in this study was about 0.6μm, so that a void can become pinned or change velocity frequently as it drifts toward the cathode. Once a void is pinned at a new grain boundary it can continue to grow and eventually again de-pin. However, the flux divergence at the new boundary might also cause the void to shrink and eventually disappear (Figure 5.2(a)).

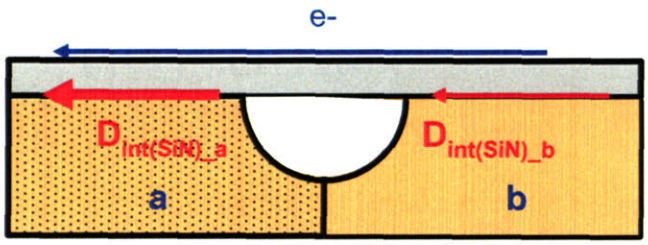

Figure 5.9 A cartoon shows the case in which void may nucleate and grow. e- is electrons, and blue arrow indicates the direction of electrons. The void is at a grain boundary, between grain a and b where diffusivity of Cu/Si_3N_4 passivation interface in grain a ($D_{int(SiN)\_a}$) is larger than that of grain b ($D_{int(SiN)\_b}$). Thick red arrow in grain a indicates large atomic flux and thinner red arrow in grain b indicates smaller atomic flux.

5.4.3 Effect of Grains on Void Drift

Voids drift because of to the difference in diffusivities on the void's surface and in the Cu/passivation-layer interface next to the void. The Cu surface diffusivity is a few orders magnitude larger than the diffusivity in the interface [Hu 1997, 1997a]. Thus, at the cathode edge of the void there is a local flux divergence between the Cu surface of the void and the Cu/passivation-layer interface next to the void, where the outgoing flux on the surface is larger than the incoming flux in the interface (Figure 5.10). At the anode edge of the void, a flux divergence of opposite sign exists and the outgoing flux through the interface is smaller than the incoming flux on the surface. These flux

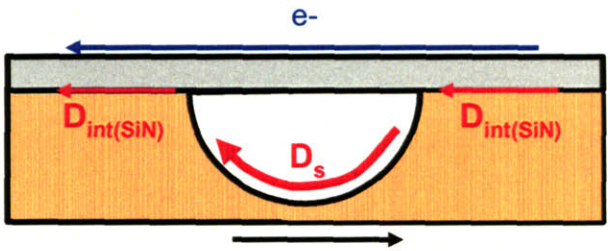

Figure 5.10 A cartoon shows the case in which void drifts in a single grain. D_s is the surface diffusivity of the exposed surface at the void, which is much larger than interface diffusivity ($D_{int(SiN)}$) around the void, as indicated by the thickness of the red arrow. The overall direction of the void drift, then, is against the direction of the electrons, shown by black arrow.

divergencies lead to gain (loss) of Cu on the anode (cathode) side of the void and therefore to a motion towards the cathode end.

By these arguments, the drift rate of the void should be directly proportional to the differences between the diffusivities of the surface and the Cu/Si_3N_4 interface. Since the stress is effectively reduced to zero around the void, the atomic flux J_a is given by [Korhonen 1993]

$$J_a = -\frac{D_{eff} C_a}{kT} j \rho z^*_{eff} e, \tag{5.1}$$

so that the flux difference on the anode side of the void is:

$$\Delta J_a = -\frac{\{\delta_s (z^* D)_s - \delta_i (z^* D)_i\} C_a}{hkT} j\rho e, \tag{5.2}$$

where the subscript s indicates the Cu surface of the void, i indicates the Cu/passivation-layer interface, ΔJ is the net flux that is accumulated/removed from the edges of the void, z* is the effective charge, D is the diffusivity around the void, C_a is the atomic concentration of Cu, k is Boltzmann's constant, T is the temperature, j is the current density, e is the fundamental charge, δ is the surface (interface) thickness, h is the thickness of the Cu interconnect and ρ is the resistivity. It can be seen then that the void will then drift with a velocity v_{void} given by:

$$v_{void} = -\left(\frac{A_{\text{int}}}{A_{void}}\right) \frac{\{\delta_s (z^* D)_s - \delta_i (z^* D)_i\}}{hkT} j\rho e, \tag{5.3}$$

where A_{int} is the cross-sectional area of the interconnect, A_{void} is the cross-sectional area of the void, assuming a fully spanning void through the width and thickness, (A_{int}/A_{void}) is 1. Also, since $\delta_s(z^*D)_s$ is much greater than $\delta_i(z^*D)_i$, the equation can be further simplified to:

$$v_{void} \cong -\frac{\delta_s (z^* D)_s}{hkT} j\rho e. \tag{5.4}$$

Equation (5.4) shows that the void drift velocity is directly proportional to the surface diffusivity, D_s. Since D_s depends on the crystallographic orientation of the surrounding grain the velocity of a void will vary with the crystallographic orientation of the grains it passes through. Therefore, the substantial variation of the drift velocity observed for drifting voids is likely due to changes in the diffusivities on different exposed grain surfaces as the voids moved from grain to grain. A quantitative analysis of relationship between drift velocity and grain orientation of the exposed void surface could not be obtained from in-situ SEM experiment because it is not possible to observe grain orientations of the exposed void surface while performing EM tests. However, the observed range of drift velocities suggests that surface diffusivities vary over a range of a factor of about 4.

The fact that the overall velocity of voids is higher in wider lines could be due to preferential motion of voids along grain boundaries that are oriented parallel to the direction of the electron wind, as predicted by Borgesen [Borgesen 1992].

5.4.4 Effect of Grains on Void Shape

After the electroplating and annealing steps, the average grain size of the Cu in

the interconnect was 0.6μm. Thus, if a void drifts for more than 0.6μm and hits a grain boundary, and if the interface diffusivity of the cathode-side grain is larger than that of the anode-side grain, the void will shrink or even disappear. Such a scenario could explain the observation shown in Figure 5.11. According to these simplified considerations, one expects that the size of the void depends on the interface diffusion at both edges of the void and the drift velocity of the void depends on the surface diffusion within the void. The fact that the voids that were drifting grew on their way to the cathode suggests that during EM the cathode edge of the voids tends to propagate faster than the anode edge.

Table 5.II contains some information about the individual diffusivities of the different grains. Unfortunately it is difficult to draw a conclusion with such a small number of data points. These results are compared with results that were obtained with better statistics using a different method by Choi *et al* [Choi Ch.6].

5.4.5 Width Dependence on Void Drift Velocity

The fact that the overall velocity of voids is higher in wider lines could be due to voids preferentially moving along grain boundaries that are oriented parallel to the direction of the electron wind, as predicted by Borgesen [Borgesen 1992].

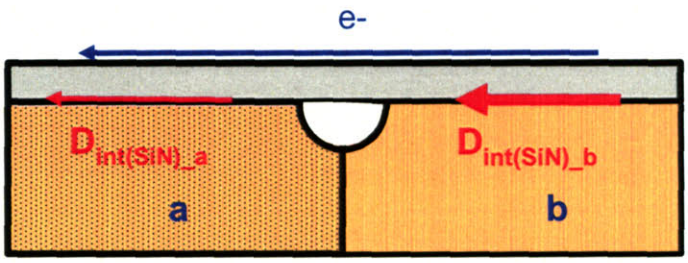

Figure 5.11 A cartoon shows the case in which the existing or incoming void shrinks and possibly disappears. Similarly as in Figure 5.9, void is between grain a and b, but in this case, $D_{int(SiN)\_a}$ is lower than $D_{-int(SiN)\_b}$, leading to smaller outgoing flux from the void, than the incoming flux to the void.

5.4.6 Difference in Grain Orientation Before and After Void Drift

Since all EBSD measurements were performed after the in-situ experiments, there is the chance that the region through which a void has passed might have an orientation other than the initial orientation. Indications for this are the observations shown in figure 5.5, where the first void seemed to be unaffected by one particular grain, but when the second void drifted through this region the shape of the void closely matched the shape of the grain. This indicates that this particular region in figure 5.5 had a different orientation after the first void had passed through. Some regions seemed to maintain their orientations as shown in figure 5.6, where the cathode edges of both voids are aligned at a very similar angle. From the small number of observations we made it is not clear what distinguishes the reconstruction of a grain with same

orientation from a grain with different orientations.

5.4.7 Criteria for Void Growth Away from the Cathode

When performing experiments in an SEM, only one sample could be imaged at a time. Therefore, only a limited number of samples could be tested in this study and therefore statistical analyses are not possible. However, the numbers in Table 5.I *suggest* that more voids form away from the cathode as the width of the line increases. Considering that the density of grain boundaries was higher in the wider lines this supports the idea that voids preferentially nucleate at grain boundaries or grain boundary triple junctions. [Korhonen 1993a]. However, even given defects such as grain boundaries that catalyze void nucleation, significant stresses are still required for nucleation. For electromigration-induced void formation, in Cu, stresses develop due to differences in diffusivities in the Cu/passivaition-layer interfaces. Stress can therefore develop at grain boundaries, for the reasons dicussed earlier. Crystallographic differences in the the surface diffusivity for Cu have been estimated to range up to a factor of 4 [Choi Ch.6b]. While these differences are large and would be expected to lead to large electromigration flux divergences and associated stresses, the electromigration flux divergence at vias will always be higher. The flux through the

liner is zero, while the flux at the Cu/passivation-layer will always be finite. In a separate analysis, we have shown that it is therefore very unlikely that the critical stress for void nucleation will be reached at a grain boundary before it is reached at the cathode [Choi Ch.7]. These results therefore suggest that voids observed to grow away from the cathode pre-existed, and did not nucleate because of the electromigration flux. There was no SEM evidence of pre-existing voids. However, the critical size for void nucleation is of order 1nm, so that voids as small as 1nm could grow due to an electromigration flux divergence, without the requirement that new voids be nucleated. Such small pre-existing voids, or void 'embryos' would generally be hard to detect. It should be noted that the increasing lifetime with decreasing linewidth observed in the current study is consistent with a recent study in which voids were known to exist before electromigration began [Chang 2005].

5.5 CONCLUSION

In situ observations of electromigration-induced failure of passivated interconnects demonstrate that there are at least two distinct failure modes, involving formation and growth of voids directly at the cathode via, and formation and growth of voids at significant distances (many line-widths) away from the cathode via. In the

latter case, voids generally drift toward the cathode and continue to grow to cause failure, either before or after arriving at the cathode.

Observations of void drift showed that voids first grew in place, and then de-pinned to drift toward the cathode, with velocities that frequently varied significantly until the void reached the cathode. Drifting voids sometimes became pinned again at grain boundaries. Post-failure EBSD analysis allowed association of all of these effects with grain boundaries.

The voids first appeared and grew at grain boundaries, presumably due to the difference in the electromigration flux at grain boundaries, arising from differences in interface diffusivities for grains with different crystallographic orientations. Drifting voids sometimes became pinned at boundaries again. In this case they sometimes shrank and disappeared instead of growing larger. This can also be understood to be associated with electromigration flux differences at grain boundaries. Data from experiments of this type, can, in principle, allow determination of relative values for the diffusivities between grains with different crystallographic orientations. We were able to obtain such data in only a few cases in the current study. However, in a related study on unpassivated interconnects [Choi Ch.6b], it was confirmed that voids that grow tend to have grains with similar orientations on their anode side (presumably

orientations with low diffusivities), and grains with a different set of similar orientations on the cathode side (presumably orientations with high diffusivities).

As voids drifted, their shape and drift velocity constantly changed, depending on the grains that the voids were passing next to or through. The drift rate of a void is determined by the diffusivity of Cu on the surface of the void. This is also expected to vary with the crystallographic orientations of grains. The jerky motion of 'voids' was clearly correlated with the grain structure revealed by EBSD analyses. When voids drift through large grains, their velocity, volume and shape remained fixed. However, as voids drifted from grain to grain, their shape and drift velocity usually changed radically.

All voids drifted toward the cathode and the voids in wider interconnects reached the cathode via. However, voids in narrower interconnects typically drifted shorter distances, presumably because the volume required for de-pinning was not reached before the void spanned the width and thickness of the interconnect. Void drift velocities were also higher in wider lines than in narrow lines, presumably because voids tended to drift faster along grain boundaries that had components parallel to the length of the interconnect. This type of grain boundary was observed more frequently in wider lines.

The overall kinetics of failure will be influenced by the mode of void formation

that ultimately leads to failure. Voids that form at the cathode via need only grow to cause failure. The time required for void nucleation is thought to scale with j^{-2} [Lloyd 1991] and the rate of void growth scales with j^{1} [Kircheim 1991]. Voids that form away from the cathode generally form at grain boundaries, from which they de-pin at a volume that scales as $j^{-1/2}$ [Borgesen 1992], drift at a rate that varies dramatically with the grain structure, but should scale as j within a single grain, and continue to grow or shrink (at a rate that also scales with j), depending on subsequent microstructural interactions. It is therefore reasonable to expect that the operation of both of these failure modes in a single test population (void formation away from and at the cathode) will affect the way in which reliability test data should be properly interpreted, and how the test results should be scaled to predict in-service lifetimes. These issues will be quantitatively treated in chapter 7.

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CHAPTER 6A

ACTIVATION ENERGY AND PRE-FACTOR OF SURFACE ELECTROMIGRATION IN COPPER INTERCONNECTS

ABSTRACT

Dual-damascene Cu interconnect segments were without passivation layers were subjected to electromigration testing in vacuum after removal of the native copper oxide on their top surfaces. Electromigration-induced voids grew at the cathode end of the segments due to a flux divergence at refractory-metal -lined vias to the lead lines below the test segment. The diffusivity of the clean Cu surface was determined by measuring the size of the voids as a function of time and test temperature, at a fixed current. An activation energy of 0.45±0.11eV, and a pre-factor of 3.35×10^{-12} m^2/s was found fro the product of the effective charge z* and the surface diffusivity D_s. This result is shown to be consistent with void drift rates measured in passivated interconnects.

6a.1 INTRODUCTION

Electromigration-induced failures in interconnect segments usually occurs by the nucleation and growth of voids at or near the cathode end via. In Cu interconnects, void nucleation usually occurs at the Cu/passivation layer-interface since this interface, since this interface provides the dominant diffusion path (Hu) and because adhesion is poor at this interface [Lloyd 1995].

In recent in-situ scanning electron microscope (SEM) experiments on passivated

interconnects, voids have been observed to often form at significant distances away from the cathode (many line-widths away) [Zschech 2004, Choi Ch.5]. When voids are found at a distance from the cathode, they typically grow to a certain size, then de-pin from their original location, and later drift toward the cathode end, against the direction of the electron and atom flow, where they either grow or coalesce with other voids to cause failure. These observations demonstrate that not only are the kinetics of void nucleation and growth important factors that influence the reliability of interconnects, but that rate of void motion is an important factor as well.

The motion of a void against the direction of electron current is the result of the difference in diffusivities between the Cu on the surface inside the void (D_s), and the Cu/passivation-layer interface (D_i) surrounding the void [Choi Ch.5]. At the anode side edge of the void, the flux out of void's edge is governed by D_i and the flux into the edge is governed by D_s, and because $D_i<D_s$ [Lloyd 1995] [Hu 1997] atoms accumulate at the anode edge, which results in the propagation of the anode edge against the direction of the electrons. A similar analysis applies for the edge at the cathode side of the void, so that the void moves against the direction of the electrons due to the flux divergences at both edges of the void.

The flux into and out of the void edge is given by

$$J_a = -\frac{(z^* D_{eff})_s - (z^* D_{eff})_i C_a}{kT} j\rho e, \qquad (6a.1)$$

where z^* is the effective charge, j is the current density, ρ is the resistivity of the conducting metal, e is the electron charge, k is the Boltzmann's constant, T is the temperature, C_a is the volumetric concentration of atoms, D_{eff} is the effective diffusivity, and the subscripts s and i refer to the surface of the void and Cu/passivation-layer interface, respectively. For Cu, the effective diffusivity is given by the surface or interface diffusivity D, times the surface interface thickness d and divided by the thickness of line (at the edges of the void) h [Hu 1997] so that,

$$\Delta J_a = -\frac{\{\delta_s (z^* D)_s - \delta_i (z^* D)_i\} C_a}{hkT} j\rho e, \qquad (6a.2)$$

or because $D_s >> D_i$

$$\Delta J_a = -\frac{\delta_s (z^* D)_s C_a}{hkT} j\rho e \qquad (6a.3)$$

The velocity of the void can be by applying the Nernst-Einstein equation to give

$$v_{void} = -\frac{\delta_s}{h}\frac{(z^* D)_s}{kT} j\rho e, \qquad (6a.4)$$

If the void forms at a distance from the cathode end of the interconnect and then drifts toward the cathode to cause failure, the time to failure (TTF) of the interconnect is governed by the initial location of void formation and the value of $(z^*D)_s$, which determines the drift velocity of the void in a passivated interconnect, as well as the time for void nucleation, growth and de-pinning. For an accurate lifetime analysis it is therefore critical to have reliable data for the electromigration-induced diffusivity on the free Cu surface. In this paper, we have performed experiments to obtain values for $(z^*D)_s$ on clean Cu surfaces.

6a.2 EXPERIMENTAL PROCEDURES

In this experiment, we used interconnects that were fabricated by Sematech Inc, in which the test structures were located in the second metallization layer (M2). The test structures were 1000μm in length, 0.45μm in thickness and 0.3μm in width. The interlayer dielectric (ILD) was SiO_2. However, for the samples used in this experiment, they were only processed up to chemical mechanical polishing (CMP) of second metallization, which means before deposition of the passivation layer on the second metallization. Thus, the top copper surface is exposed in these samples. The samples

were mounted on 24-pin ceramic package using the silver epoxy, as in the previous chapter, but unlike in previous chapter, while curing the epoxy at 120°C, H_2 gas was flown to prevent Cu oxidation. Then the sample was gold wire-bonded, and the package was inserted into the self-made vacuum electromigration test chamber. After pressure reaches below $1x10^{-7}$ torr, 5% hydrogen and 95% nitrogen forming gas was flown with 500sccm/min at $1x10^{-3}$torr and 250°C for 5 minutes to reduce the residual copper oxides on the top surface of the interconnect [Y.Hu 2001] [Rodriguez 2003]. Then temperature was raised to an accelerated testing condition and the chamber was remained undisturbed until the pressure reached $2.5x10^{-8}$ torr. After the base pressure of $2.5x10^{-8}$ torr or below was reached, accelerated electromigration test was performed by applying a current density of $1.852x10^{6}A/cm^{2}$. Detailed setup of vacuum electromigration station is described in Appendix B. After the accelerated electromigration test, the sample was removed from the ceramic package, and the void volumes at the cathode end were obtained using scanning electron microscope (SEM).

6a.3 RESULTS AND DISCUSSION

Voids were observed at the end of the cathode in all samples. This was expected since there is no incoming flux from the blocking via due to the refractory

metal liner. Voids were often observed elsewhere, but were not the focus of the current study [Choi, Ch.6b]. By measuring the volume of the cathode void and correlating this volume with the time a particular line was subjected to current, one can calculate $(z^*D)_s$ using equation (6a.4). The drift velocity v_{void} is the length L_v of the void when fully spanning the line divided by the time t_{test}

$$\left(z^* D\right)_s = -\frac{h}{\delta_s}\frac{L_v kT}{t_{test} j\rho e}, \qquad (6a.5)$$

For the evaluation of z^*D_s, 0.5nm was used for δ_s [Hu 1999]. Values for $(z^*D)_s$ were obtained at three different temperatures, 261°C, 281°C, and 320°C, and are plotted in figure 6a.1. An average of 17 measurements was made at each temperature. The activation energy E_s extracted from a $\ln((z^*D)_s)$ vs. 1/T is 0.45±0.11eV (Figure 6a.2). E_s is the activation energy for surface self diffusion of Cu, where

$$(z^* D)_s = [z^* D_0 \exp(\frac{-E_s}{kT})]_s = (z^* D_0)_s \exp\left(\frac{-E_s}{kT}\right) \qquad (6a.6)$$

The pre-exponential factor in equation (6a.6), $(z^*D_0)_s$, was found to be 3.35×10^{-12} m^2/s.

Values for E_s determined by other groups are given in table 6a.I. Hu extracted E_s

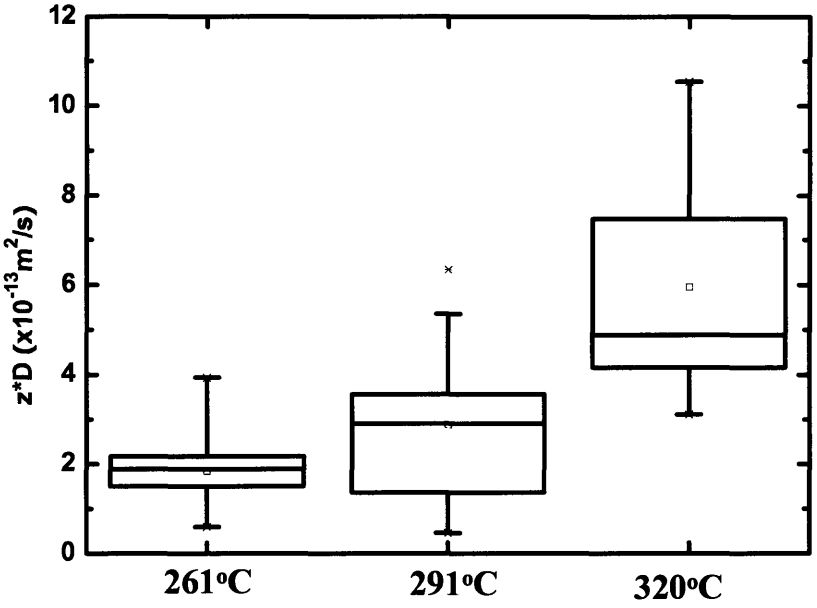

Figure 6a.1 Surface z*D at Various Temperatures.

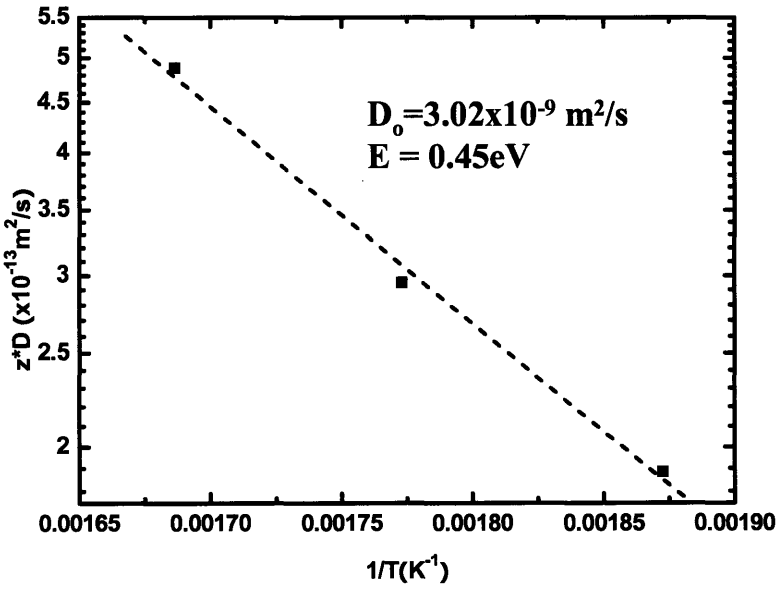

Figure 6a.2 Average Surface z*D at Various Temperatures.

Table 6a.I

Reported E_s and $(z^*D_0)_s$, $D_{o,s}$ values determined in various studies.

	E_S (eV)	$(z^*D_0)_s$ (m^2/s)	Experimental Method	Surface Condition
This study	0.45±0.11	3.35×10^{-12} m^2/s	vacuum EM test	clean
Park[Park1991]	0.79±0.02	not known	vacuum EM test	oxidized
Hu [Hu1991]	0.9	7.39×10^{-6}	EM test	exposed to air
Liniger [Liniger 2002]	0.89	not know	vacuum EM test	exposed to air
		$D_{0,s}$ (m^2/s)		
Jo [Jo1995]	0.47±0.03	not known	vacuum EM test	clean
Ernst [Ernst1992]	0.35±0.06	not known	He beam scattering	clean
Breeman [Breeman1992]	0.39	not known	Low Energy Ion Scattering	clean
Bradshaw [Bradshaw1967]	0.824	7×10^{-6}	grain boundary grooving	clean

values from electromigration-induced drift of unpassivated Cu strips on refractory metal conducting underlayers. The value of E_s are around 0.9eV [Hu 1999]. Liniger et al observed the void growth rate of dual-damascene unpassivated Cu interconnects using in-situ SEM and extracted E_s which has similar value to that of Hu [Liniger 2002]. The main difference between this study and the procedures of Hu and Liniger is that in their studies, the Cu surfaces had been exposed to air and no further treatment was used

to remove the native oxide prior to electromigration (EM) tests. Jo and Vook created Cu strips in vacuum chamber using shadow mask, and performed EM tests without breaking a vacuum, so that Cu strips remain oxide free. Their value was 0.47±0.03eV which closely matches with the value obtained here. However, $(z^*D_0)_s$ was not reported. Other values of E_s obtained on clean Cu surfaces using different techniques are generally similar, except for the work of Bradshaw *et al*, in which the kinetics of grain boundary grooving was characterized to extract the Cu surface diffusivity [Bradshaw 1967].

To our knowledge, only Hu has reported a measured values of $(z^*D_0)_s$ (Table 6a.I) However, because this value applies for Cu coated with a native oxide, it is not surprising that, as in the case E_s, the value for $(z^*D_0)_s$ reported here differs significantly form the value reported by Hu. Figure 6a.3 shows values of $(z^*D_0)_s$ plotted vs. 1/T, based on the values of $(z^*D_0)_s$ and E_s reported by Hu, Bradshaw and reported here. At a typical integrated circuit temperature of operation, 100°C, $(z^*D)_s$ for oxide-free Cu is more than three orders of magnitude higher than values found by Hu for native-oxide-coated Cu.

When a void nucleates in a passivated interconnect, the exposed surface of the void is likely to be free of oxide, due to the complete encapsulation of the Cu.

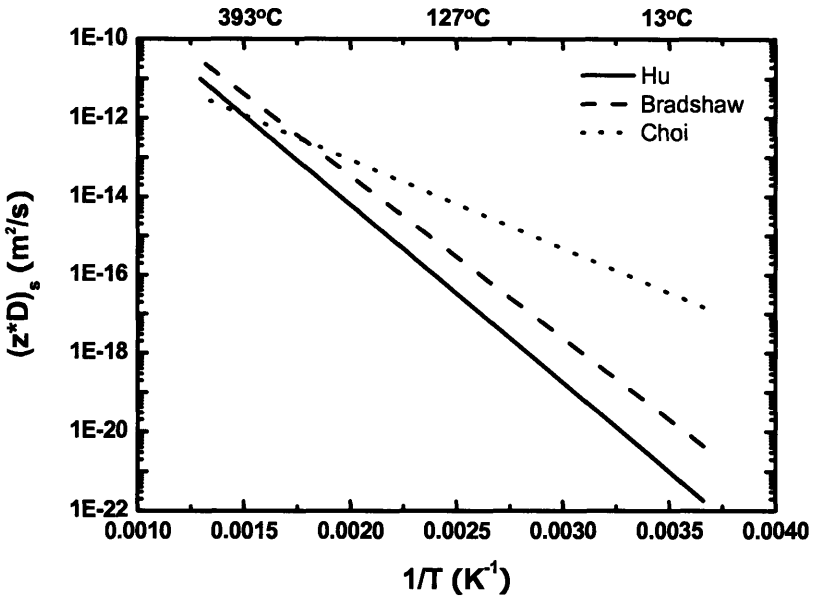

Figure 6a.3 $(z^*D)_s$ of three different values. Note that z^* for Bradshaw was set to 1 [Hu 1999].

Therefore, the D_s for an oxide-free Cu surface is more relevant to void dynamics than the D_s for Cu coated with a native oxide.

To test this conclusion, the drift velocity of voids was calculated using equation (6a.4) and the experimentally determined values of $(z^*D_0)_s$ and Es and was compared with the void drift velocities measured by Choi *et al.* during SEM *in-situ* electromigration studies [Choi Ch.5] (Table 6a.II). Void drift rates were measured in lines of three different widths, and the drift velocity was found to increase with increasing line width. Drift velocity values calculated for oxide-free surfaces, rather

Table 6a.II

Average void drift velocity obtained from in-situ EM testing [Choi Ch.5] and drift velocity obtained by using surface diffusivity. $T = 370^{\circ}C$, $j = 3.0MA/cm^2$.

Interconnect width	Average Drift Velocity
2.25μm	0.0462μm/min
1.0μm	0.0076μm/min
0.3μm	0.0031μm/min
Extracted from z^*D_s	
Choi	0.0013μm/min
Hu	0.00096μm/min

than oxidized surfaces, are in the best agreement with measured drift rates for all three line widths. The agreement is best in the narrowest lines, which had the most bamboo-like grain structures. The wider lines had more grain boundaries and grain boundary networks lining along the length of the lines. In the widest lines, these grain boundary networks were clearly observed to provide preferred paths for void migration. We therefore conclude that in lines with near-bamboo grain structures, the rate of void migration is set by the Cu diffusivity on the clean oxide-free surfaces of the void.

6a.4 CONCLUSION

Using accelerated electromigration tests on unpassivated interconnects in vacuums, we were able to obtain temperature dependent data for electromigration-

induced surface diffusivity, $(z^*D)_s$, on clean oxide-free Cu embedded in damascene structures. When this data is used calculate void drift velocities in passivated interconnects, reasonable agreement is found with void drift rates observed in SEM *in-situ* experiments on passivated interconnects, especially in narrow lines with near-bamboo grain structures. When voids first form at a distance from the cathode and drift toward and to the cathode to cause failure, the temperature dependence of rate of void drift plays an important role interpretation of test results and in accurate reliability projections.

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CHAPTER 6B

DEPENDENCE OF THE ELECTROMIGRATION FLUX ON THE CRYSTALLOGRAPHIC ORIENTATIONS OF DIFFERENT GRAINS IN POLYCRYSTALLINE COPPER INTERCONNECTS

ABSTRACT

Dual-damascene Cu electromigration test structures with unpassivated segments in the second level of metallization were tested under vacuum. About 20 immobile voids formed along 1000μm-long structures. Crystallographic orientations of grains on anode and cathode sides of 158 voids were obtained. It is shown that electromigration diffusivities vary with crystallographic orientations of the grains, increasing in the order (1 1 1), (1 1 5), (7 5 13), (11 1 11), and other orientations not twin-related to (1 1 1). Data of this type provides an improved basis for process-development for optimized reliability and for extrapolation of test results for reliability projections.

6b.1 INTRODUCTION

One very important factor influencing the reliability of interconnects carrying such high current densities is electromigration (EM). Different mechanisms for EM-induced failure of Cu-based interconnects have been proposed and a wide range of activation energies for failure have been reported [Lloyd 1999, C.Hau-Riege 2004]. There is evidence that nucleation, growth, motion, and coalescence of voids may all play roles in EM-induced failure [Gan 2001, S.Hau-Riege 2002]. EM leads to tensile

and compressive stresses where there are divergences in the atomic flux, and voids are expected to nucleate in regions with high tensile stresses [Korhonen 1993, C.Hau-Riege 2004a]. The highest tensile stress in an interconnect segment is expected to develop at the cathode-end via, where the Cu that electromigrates away from the via can not be replaced because the refractory-metal liners at the base of the via blocks migration. However, in-situ side-view observations of EM-induced void dynamics indicate that voids often form away from the cathode and then drift toward the cathode [Meyer 2002, Zschech 2004, Choi Ch.5]. Because the product of the effective charge and diffusivity (z*D) on the surface of a grain depends on the crystallographic orientation of the grain relative to the surface, there can be flux divergence sites where grain boundaries that span the width of a line meet the Cu/passivation-layer interface. Voids can therefore nucleate at grain boundaries away from the cathode [Borgesen 1992, Sekiguchi 2003], however, Choi et al [Choi Ch.7] showed that it is very unlikely for voids to nucleate away from the cathode. There can be pre-existing voids that result from processing-induced stresses. These pre-existing voids can also grow due to the electromigration flux divergence at a grain boundary, if the diffusive flux of copper out of the void is higher than the flux into the void. Because of the higher z*D of Cu along the free surface within a void compared to the z*D of Cu along the Cu/passivation-layer

interface, atoms tend to move from the cathode side to the anode side of a void, leading to motion of the void toward the cathode end of the interconnect [Choi Ch.7]. This occurs after a void reaches a critical size that allows it to become de-pinned from a boundary [Borgesen 1992a]. Drifting voids can become trapped at other boundaries where they can either grow or shrink, depending on the sign of the flux divergence. Generally, though, they drift to the cathode where they coalesce to form a fatal void. If EM-induced failure occurs due to these dynamic void phenomena, it is clear that the crystallographic texture of the copper has an important role in governing reliability [Zschech 2004]. The purpose of this work is to correlate texture and EM reliability by observing the texture-dependence of void growth and drift in interconnects.

6b.2 EXPERIMENTAL PROCEDURES

Experimental procedures and conditions are identical to that of chapter 6a and appendix B. In this experiment, we used interconnects that were fabricated by Sematech Inc, in which the test structures were located in the second metallization layer (M2). The test structures were 1000μm in length, 0.45μm in thickness and 0.3μm in width. The interlayer dielectric (ILD) was SiO_2. However, for the samples used in this experiment, they were only processed up to chemical mechanical polishing (CMP) of the second

metallization, which means before deposition of the passivation layer on the second metallization. Thus, the top copper surface is exposed in these samples.

The samples were mounted on 24-pin ceramic package using the silver epoxy, as in the previous chapter, but unlike in previous chapter, while curing the epoxy at 120°C, H_2 gas was flowed over the specimen to prevent Cu oxidation. Then the sample was gold wire-bonded, and the package was inserted into the self-made vacuum electromigration test chamber. After pressure reaches below $1x10^{-7}$ torr, 5% hydrogen and 95% nitrogen forming gas was flown with 500sccm/min at $1x10^{-3}$torr and 250°C for 5 minutes to reduce the residual copper oxides on the top surface of the interconnect. Then temperature was raised to a testing condition of 320°C and the chamber was remained undisturbed until the pressure reached $2.5x10^{-8}$ torr. After the base pressure of $2.5x10^{-8}$ torr was reached, accelerated electromigration test was performed by applying a current density of $1.852x10^{6}A/cm^{2}$.

After the accelerated electromigration test, the sample was removed from the ceramic package and the grain orientation of the exposed copper surface was obtained using EBSD.

6b.3 RESULTS AND DISCUSSION

6b.3.1 Voids in Flux Divergence Sites

While voids in fully-processed passivated interconnects drifted toward the cathode, no drift was observed in in-situ SEM observations of unpassivated samples. In the latter case, the z*D within the void and along the surfaces next to the voids are similar so the void becomes immobile. SEM observations revealed that there were typically about 20 to 30 evenly distributed voids along the length of one 1000μm-long test sample. The voids are assumed to form and grow due to the divergence in the z*D of the surface at grain boundaries. The surface z*D of the grain at the anode edge of the void has to be higher than that of the cathode edge for a void to grow (Figure 6b.1). Therefore, by obtaining grain orientation data at the cathode and anode edges of the voids, one can determine the relative diffusivities of grains.

6b.3.2 Relative Diffusivities in Different Grain Orientations

A direct comparison of this type is only possible if there is only one grain across the width of the interconnect (a bamboo or near bamboo structure). This was the case for the 0.3μm wide interconnects that were used. Figure 6b.2 shows the inverse pole figure for grains on the cathode side (figure 6b.2(a)) and anode side (figure 6b.2(b)) of the voids after the EM tests. For grains on both the cathode and anode edges of the

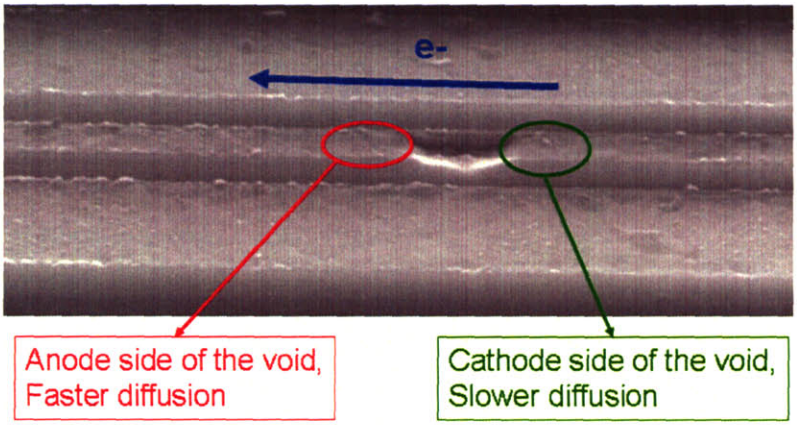

Figure 6b.1 One of immobile voids in the middle of the line, anode edge of the void has faster diffusivity than the cathode edge of the void.

voids, there is a frequent occurrence of three orientations. The out of plane orientations are (1 1 1), (1 1 5), and (7 5 13). (1 1 5) is the first generation twin orientation for the (1 1 1) grains and (7 5 13) and (11 1 11) are the second generation twins of (1 1 1) grains. We observed a relatively small population of (11 1 11) oriented grains compared to the three orientations as expected from twinning. We also determined grain orientations of 0.3μm-wide samples that had not been subjected to EM testing and found that they also showed frequent occurrence of these three twin related orientations (Table 6b.I, Figure 6b.3). Others have observed similar textures in interconnects with dimensions that are smaller than the size of the grains [Hu 1997]. Table 6b.II shows the number of grains found for cathode and anode edges that are within 9° of (a) (1 1 1), (b) (1 1 5), (c) (7 5 13), and (d) (11 1 11). Also shown in Table

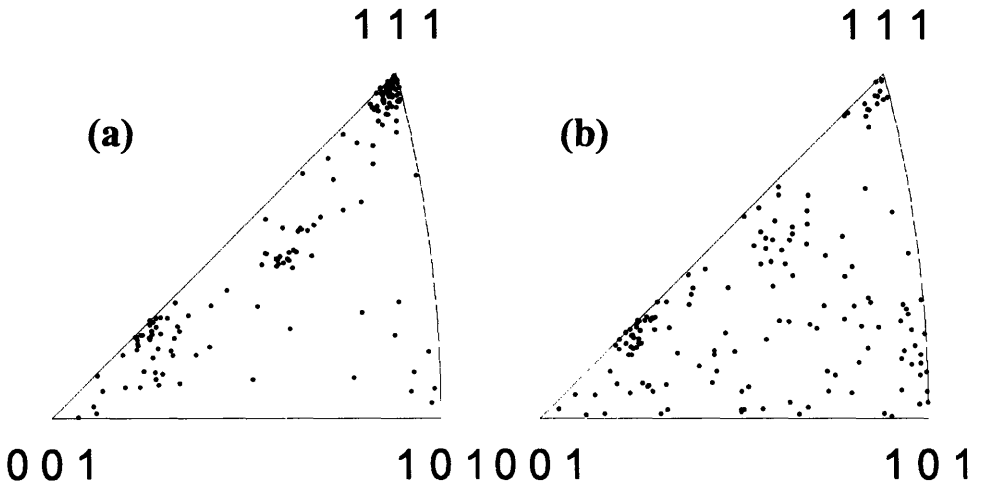

Figure 6b.2 Inverse pole figures of the cathode edge **(a)** and anode edge **(b)** of the immobile voids in the tested samples.

Table 6b.I

Volume fractions of orientations within 9° of (1 1 1), its first and second generation twins, and the rest of the orientation of untested sample.

	Volume Fractions
(1 1 1)	18.89
(1 1 5)	19.22
(7 5 13)	23.32
(11 1 11)	13.09
Rest	25.48

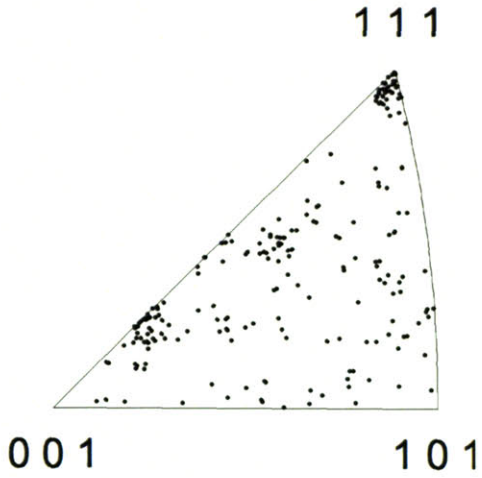

Figure 6b.3(a) Inverse pole figure of the untested sample with 0.3μm width, 1000μm length. Circled regions show (1 1 1) and its first (1 1 5) and second (7 5 13), (11 1 11) twin orientations.

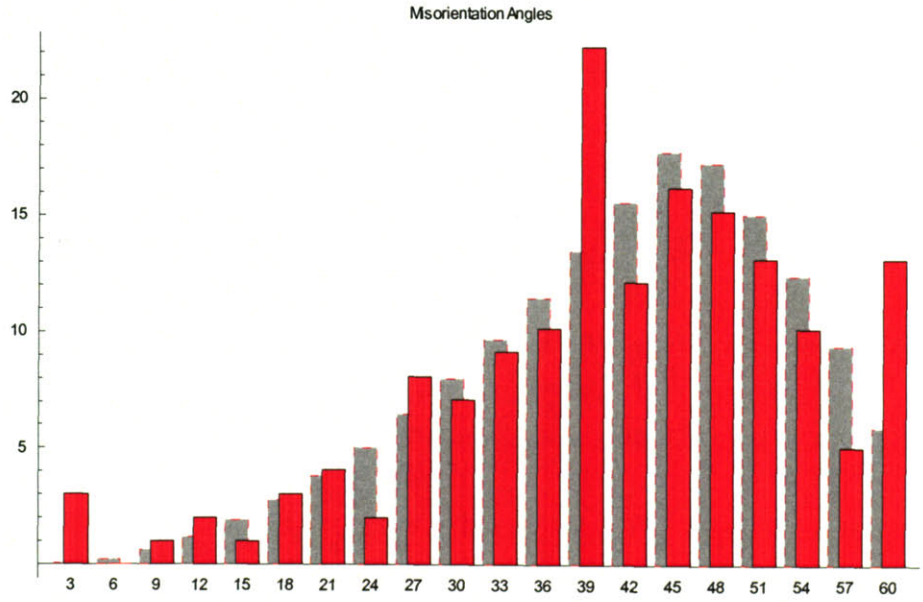

Figure 6b.3(b) Mackenzie plot of randomly oriented sample (gray) versus untested sample (red).

Table 6b.II

Number of grains observed in cathode and anode edges of the voids, within 9° of (1 1 1), its first and second generation twins, and the rest of the orientation of untested sample.

	Cathode (slow)	Anode (fast)	total
(1 1 1)	64	16	80
(1 1 5)	45	46	91
(7 5 13)	30	31	61
(11 1 11)	7	26	33
High	11	38	49

6b.II are the number of grains that are not in one of these four orientations (Table 6b.II(e)). As seen in table 6b.II, (1 1 1) grains are most common at the cathode edge, (1 1 5) and (7 5 13) are evenly distributed between the two edges, and the grains with random orientations (not twin related) have higher populations at anode edge. Assuming that voids can only grow when there are flux divergencies, this suggests that the z*D increases from (1 1 1) to (1 1 5) and (7 5 13) to (11 1 11). The z*D is still higher for grains with other orientations. No significant trend for preferred crystallographic orientations along the interconnect line has been found. Table 6b.III shows the number of grain pairs (on either side of a void) of each crystallographic type

Table 6b.III

Number of grain orientation pairs in each individual voids.

Anode / Cathode	(1 1 1)	(1 1 5)	(14 10 26)	(11 1 11)	Rest
(1 1 1)	8	17	9	11	19
(1 1 5)	3	14	11	8	9
(7 5 13)	2	10	7	5	6
(11 1 11)	2	2	2	0	1
Rest	1	3	2	2	3

and allows direct comparison between two different orientations at two edges of each void. Table 6b.III clearly shows that most of the grains around the void follow the proposed behavior noted earlier, i.e. that the diffusivity increases in the order of (1 1 1), (1 1 5) and (7 5 13), (11 1 11) and the rest of the orientations. A percentage of about 12% of all voids were found that did not follow this behavior. There are a few possible explanations. First, in some cases, there can be more than one grain through the thickness of the interconnect, so that if the upper grain is the faster diffusing grain, the grain can be completely removed when the current is applied, leaving the slower grain exposed in the bottom. In this case, a slow-diffusion grain would be observed at the anode edge of the void. Second, the edge of the void can sometimes be difficult to

Table 6.IV

$(z^*D)_s$ of various grain orientations

	z*D (at 320°C) ($x10^{-13}m^2/s$)
(1 1 1)	**2.84**
(1 1 5)	**4.61**
(7 5 13)	**5.94**
(11 1 11)	**7.06**
Rest	**8.65**

identify and can lead to indexing with an incorrect grain orientation. Third, while no strong correlation with in-plane orientations was observed, weak dependencies may contribute to deviations from the observed trend. Given the strength of the observed trend, even in the presence of these sources for deviations, we are able to identify relative z*D in different grain orientations. Using the $(z^*D)_s$ distribution at 320°C [Choi Ch.6a] and volume fraction of grains in an untested sample, absolute values of $(z^*D)_s$ in various orientation can be extracted (Table 6.IV). Diffusivity at 320°C shows that slowest diffusing (1 1 1) grain is about four times slower than that of fastest diffusing grains of orientations unrelated to (1 1 1) and its twins.

6b.4 CONCLUSION

It seems likely that the trend in crystallographic-orientation-dependent surface z*D observed here is preserved in passivated lines. This is the subject of on-going research. If this is the case, z*D values between neighboring grains at the Cu/passivation-layer interfaces can be used to predict the rate of void growth or shrinkage at grain boundaries, while measurements of the z*D at free surfaces allows prediction of the rates of void drift. Together, this information provides an improved basis for understanding the impact of texture control on reliability improvement, and for development of improved models for relating failure rates observed at test conditions to those expected at service conditions.

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CHAPTER 7

VOID DYNAMICS IN COPPER-BASED INTERCONNECTS

ABSTRACT

The electromigration lifetimes of Cu-based interconnects are strongly influenced by whether voids are present before electromigration, and by where fatal voids initially form and grow. Modeling, simulations, and comparisons with in-situ experiments are used to establish criteria for void formation away from the cathode end of a copper interconnect. It is shown that observation of voids at locations other than the cathode strongly suggests that the voids grew from pre-existing voids. When pre-existing voids are within a current-density-dependent critical length of the cathode, new voids are unlikely to nucleate at the cathode and failure occurs only when the pre-existing voids grow. For voids to grow they must be at grain boundaries and the diffusivity on the anode side of the void must be higher than on the cathode side. As these voids grow, they will either lead directly to open-circuit failure or, once they reach a critical size, they will de-pin from grain boundaries and drift toward the cathode. In the latter case, multiple voids might accumulate and coalesce to cause failure. This mechanism has been observed in both side-view and top-down in-situ accelerated life-time testing. It is shown that the relative importance of these various void-induced failure mechanisms depends on the current density, and is different under typical accelerated test conditions from what is expected at service conditions.

7.1 INTRODUCTION

A divergence in the electromigration flux leads to local evolution in the stress state of encapsulated metal interconnects. In via-terminated Cu-based interconnect segments, an electromigration flux divergence will usually occur at the base of vias where there is a refractory metal liner (e.g. Ta). The electromigration flux at a given current density scales with the atomic self-diffusivity of a conducting material. Due to their much different self-diffusivities, electromigration will occur in Cu at much lower current densities and temperatures than in liner materials. Therefore, the liner at the base of a cathode via will prevent replacement of Cu electromigrating away from the via, resulting in development of a tensile hydrostatic stress. When the tensile stress reaches the critical value, the stored strain energy will drive nucleation of voids. In a via-terminated interconnect segment, the critical stress reaches its highest value at the cathode via [Korhonen 1993]. It is therefore generally expected that void nucleation will occur at the cathode. However, recent in-situ experiments on electromigration-induced voiding in encapsulated interconnects have revealed that while voids do sometimes first appear at cathode vias, voiding often is first detected at significant distances away from the cathode [Meyer 2002, Zschech 2004, Choi Ch.5]. Moreover, these voids can grow in-place to cause failure or de-pin from grain boundaries and drift

toward the cathode where they can grow or coalesce with other voids to cause failure. It is the purpose of this paper to explore the origin, consequences, and implications of this varied behavior. This will be done through development of simple models and simulations that have been developed through direct quantitative comparisons with experimental data.

Several different mechanisms for void-induced failure will be considered, as illustrated in figures 7.1 and 7.2. First, for cathode vias in via-below interconnect segments, voids can nucleate and grow to cause failure above the via (Figure 7.1(a)) or nucleate and grow to cause failure at the base of the via (Figure 7.1(b)). The former case is generally expected to be more likely because void nucleation is expected to be easier at the Cu-cap interface [Lane 2003, Lloyd 1999], and growth should be faster because of higher diffusivities along the Cu-cap interface [Rosenberg 2000, C.Hau-Riege 2001]. However, failure analysis often reveals voids at the base of vias [Lee 2001]. Voids away from the cathode have also been observed both in in-situ studies [Meyer 2002, Zschech 2004, Choi Ch.5] and in failure analyses [S.Hau-Riege 2002, Chang 2007]. These voids can migrate to the cathode to contribute to failure (Figure 7.1(c)), or can grow in place to cause failure (Figure 7.1(d)). Both mechanisms have been observed in in-situ experiments. It also important to note that voids have been

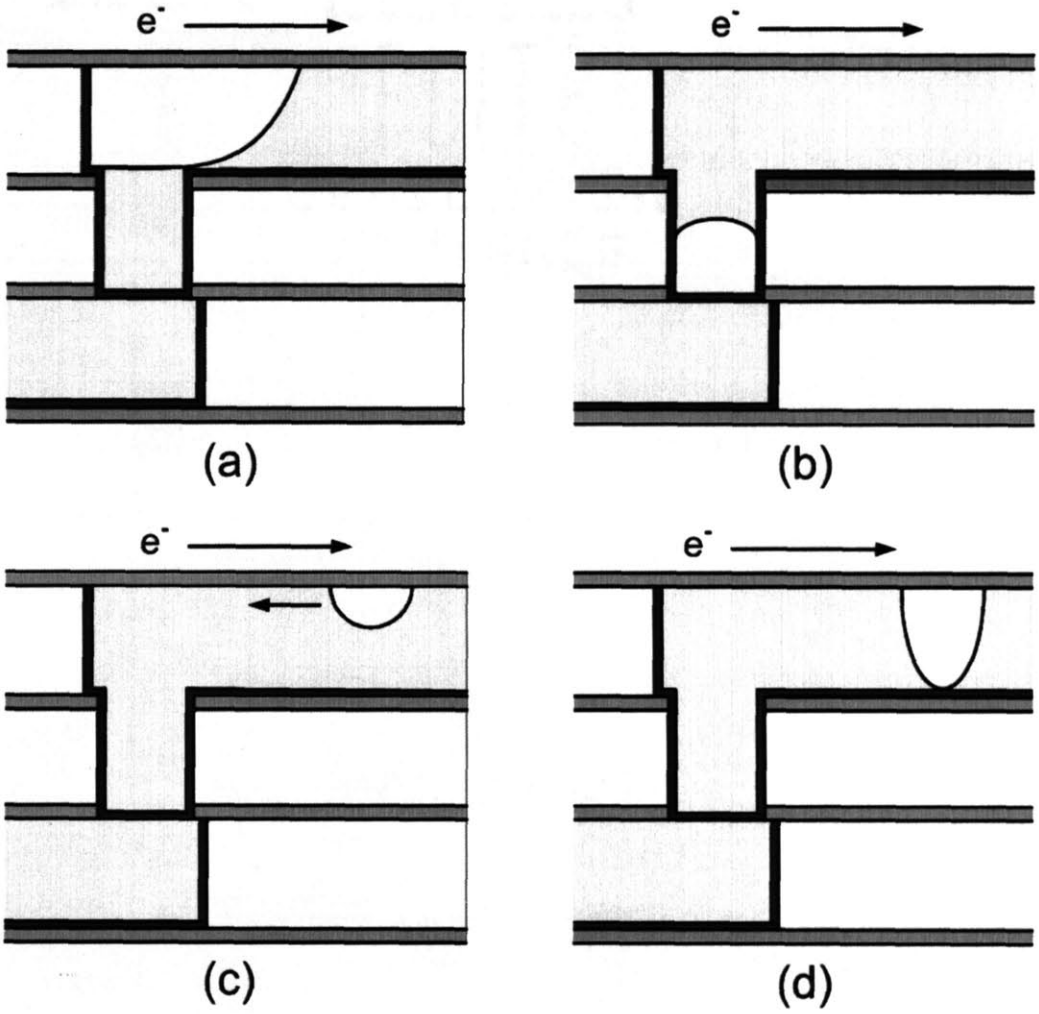

Figure 7.1 Voids in an interconnect segment terminating in a cathode via *below* the segment. **(a)** Voids most readily nucleate at the Cu-cap interface, and grow at the site where the electromigration-induced tensile stress is highest. **(b)** Voids are sometimes observed at the base of vias, where they may have nucleated or where they may have drifted from other locations. Voids are sometimes observed at locations other than directly at the cathode via. These voids can drift toward the via **(c)** or grow in place **(d)** to cause failure.

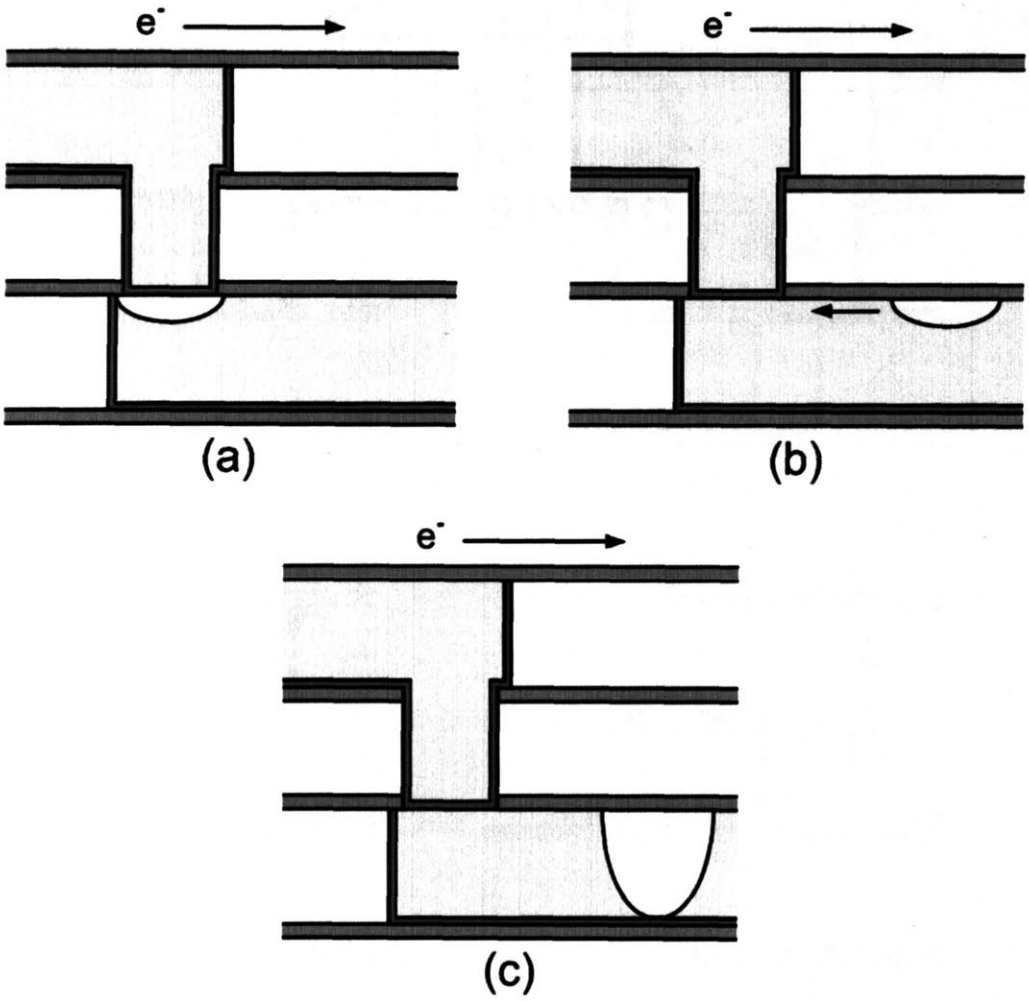

Figure 7.2 Voids in an interconnect segment terminating in a cathode via *above* the test segment. **(a)** Voids most readily nucleate at the Cu-cap interface, and grow where the electromigration-induced tensile stress is highest. Voids are sometimes observed at locations other than directly at the cathode via. These voids can drift toward **(b)** the via or grow in place **(c)** to cause failure.

observed to grow or coalesce at the cap above the via, before abruptly 'diving' into the via to cause failure at the base [Meyer 2002]. In this case, post-testing failure analysis

might incorrectly lead to the conclusion that the void formed at the base of the via.

The scenario is somewhat different for cathode vias in via above configurations. A void that nucleates and grows directly under a via (Figure 7.2(a)) can cause failure even when the void is quite small, because of the absence of a cap layer that can shunt current [S.Hau-Riege 2002]. A void that forms away from the via can drift to the via to cause failure (Figure 7.2(b)), again at a small void size, or grow in place to cause failure (Figure 7.2(c)). The difference in the fatal void size in via-above and via-below structures is thought to be the cause of the different lifetimes and critical lengths measured in these different types of structures [Gan 2001]. It should be noted that failure analyses suggest the case illustrated in figure 7.2(a) is rare, and also shows examples of the failure mode illustrated in figure 7.2(c) [S.Hau-Riege 2002].

If only one of the mechanisms discussed above dominates (e.g. Figure 7.1(a) or Figure 7.2(a)), failure-time distributions would be expected to be monomodal. Also, if the mechanisms of figures 7.1(a) and 7.2(a) were the only mechanisms, for example, the current density scaling of lifetimes should be the same for both types of vias. However, when mechanisms of type 7.1(a) and 7.1(b) are mixed, failure can be affected by void nucleation ($t_{50} \propto j^{-2}$) [Shatzkes 1986, Korhonen 1993] or void-growth ($t_{50} \propto j^{-1}$) [Lloyd 1991], as well as void de-pinning and drift. TTF data from copper

interconnect reliability tests often show complex behavior suggestive of the operation of multiple failure mechanisms [Hu 1998] [Lloyd 1999] [C.Hau-Riege 2004].

Likely sites for void nucleation and growth away from the cathode are associated with grain boundaries, either at locations where single boundaries contact the capping layer (Figure 7.3(a)) or at grain boundary triple junctions at the capping layer. The former is more likely in narrow lines with near-bamboo structures. If we consider the case illustrated in figure 7.3, if the diffusivity at the Cu-cap interface for grain 2 (the anode-side grain) is higher than for grain 1, the electromigration flux divergence will lead to a tensile stress that might lead to void nucleation. Once a void is present at such a boundary, it will grow at a rate proportional to the difference in the cap-liner interface diffusivities ($D_{1,int}$-$D_{2,int}$) for the two grains and the current density j, and will continue to grow at the boundary until, or unless, it de-pins from the boundary [Borgenson 1992]. Both in-place growth and growth to de-pinning behavior have been observed in in-situ experiments [Mayer 2002, Zschech 2004, Choi Ch.5] as well as in simulations [Zaporozhets 2005].

Voids can be pinned at grain boundaries because of the energetic cost associated with replacement of the grain boundary once the void has moved away (Figure 7.3(a)).

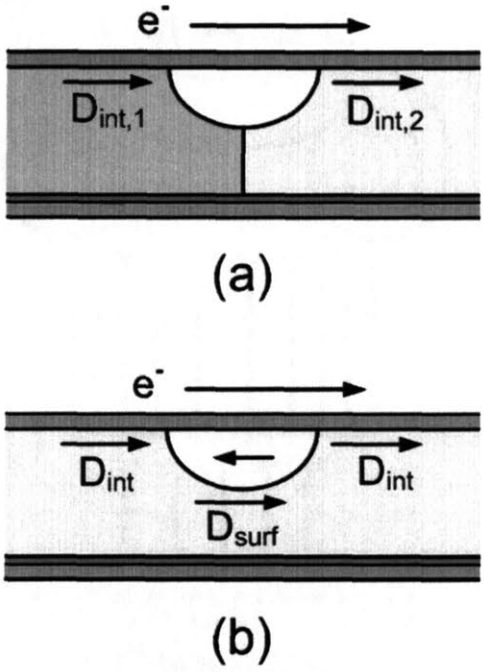

Figure 7.3 **(a)** Void nucleation and growth at boundaries is favored when the atomic interfac diffusivity at the Cu-cap interface of the cathode-side grain is lower than the diffusivity of the anode-side grain. **(b)** Once voids have grown to a critical size they can de-pin from boundaries and drift toward the cathode. The drift rate is determined by the magnitude of the diffusivity on the surface of the void relative to the interface diffusivity.

The magnitude of this energy, relative to the energy associated with the electron-wind force that would be released once the void drifts away, increases with increasing void size. Borgesen *et al.* [Borgesen 1992] have argued that for hemi-cylindrical voids, this leads to a critical void radius for de-pinning R_d that depends on the current density according to

$$R_d = \sqrt{\frac{3\gamma_{gb}\Omega}{4qz^*\rho j}}, \qquad (7.1)$$

where Ω is the atomic volume of the conductor, q is the fundamental charge, z* is the effective charge for electromigration, ρ is the resistivity, and γ_{gb} is the grain boundary energy.

Once a void de-pins, it will drift due to electromigration on the free surface of the Cu inside the void. The rate of drift (or drift velocity v) will scale with the current density and the Cu self diffusivity on this surface, (D_{surf}). The void will not grow when it drifts through a grain because there will not be a difference in D_{int} on either side of the void. The drifting void may subsequently be pinned at a higher energy boundary, or grow while it passes through boundaries.

Choi *et al.* [Choi Ch.6b] characterized the crystallographic texture of anode-side grains and cathode-side grains in unpassivated lines (in which voids do not de-pin), and to a more limited extent, passivated lines. By tracking the growth rates of pinned voids, they were able to determine $D_{1,int}$-$D_{2,int}$ for a large range of different boundary types. From growth rates measured for voids at the cathode vias of lines, they were also able to determine the magnitude of the average interface diffusivity, $\overline{D}_{int}$. Their results indicate that D_{int} varies among different individual grains only up to a factor of 4

[Choi Ch.6].

7.2 MODELING AND SIMULATION

An understanding of stress evolution during electromigration is critical to understanding void nucleation, growth, and drift. We will employ the simple 1D model of Korhonen *et al* [Korhonen 1993] to discuss and analyze these phenomena. In this model, the rate of evolution of the hydrostatic stress σ at any position x along the length of an interconnect segment is given by

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\frac{DB}{kT}\left(\Omega \frac{\partial \sigma}{\partial x} + z^* q\ \rho\ j\right)\right], \tag{7.2}$$

where D is the relevant diffusivity (D_{int} for Cu) and B is a modulus that accounts for the elastic response of the material around the conductor to volume changes of the conductor resulting from electromigration-induced mass transport. 'B' therefore defines the relationship between mass transport and the resulting hydrostatic stress in the interconnect. 'B' can be determined from finite element analyses that include the complex elastic interactions of the various materials surrounding the Cu [S. Hau_Riege 2002, Lee 2003].

Equation (7.2) can be used to calculate σ everywhere along an interconnect segment. In a via-terminated segment, stress at the cathode via increases at a rate that scales with j^{-2}. It is typically assumed that once this stress reaches the critical value required for void nucleation, σ_{nuc}, a void will nucleate and the local stress will drop to zero. However, in the absence of void nucleation (or metal extrusion), stress evolution can reach a steady state in which the tensile stress is at a maximum at the cathode, σ_{max}, and a minimum σ_{min} at the anode. Reaching a steady state requires that $\sigma_{max} < \sigma_{nuc}$, and $|\sigma_{min}| < |\sigma_{comp}|$, where σ_{comp} is the critical stress for compressive failure (e.g., for dielectric cracking an metal extrusion). For a segment that is initially at zero stress, this condition will be met when the product of the segment length L and current density j fall below a critical value,

$$(jL)_{crit} < \left(\frac{\Omega \Delta\sigma_{crit}}{z^* q \rho j} \right), \tag{7.3}$$

where $\Delta\sigma_{crit} = \sigma_{nuc} - \sigma_{comp}$

The Korhonen model has been successfully used to explain a wide range of experimental behavior [Korhonen 1993a, Brown 1995, Knowlton 1997&1998].

Table 7.1

Parameters used for simulations.

Parameter	Value
σ_{nuc}	40 MPa [C.Hau-Riege 2002]
z*	1 [Hu 1999]
B	28 GPa [S.Hau_Riege 2000]
Ω	1.18×10^{-29} m^3
D_o	1.25×10^{-9} m^2/s
ρ	4.1 mΩ-cm (at 370°C)
ΔH_{eff}	0.8eV [Hu 1997]

Unfortunately, because D depends on σ, equation (7.2) can not be solved analytically. We have recently developed a numerical solver based on use of a reverse Euler technique that allows use of equation (7.2) for simulation of stress evolution leading to void nucleation, and stress evolution and mass transport in the presence of voids. A detailed description of this solver is given elsewhere [Choi Ch.2]. Here we report analyses based on the use of this tool to investigate the implications of the location of voids in interconnects.

In using equation (7.2) for the simulations described below, we have, unless otherwise noted, used the experimental values indicated in Table 7.I. D_0 is the average interfacial diffusivity determined from observations of voids growing at the cathode end

in-situ experiments fully passivated via-terminated interconnect segments [Choi Ch.6a]. In a study reported elsewhere, we have characterized the crystallographic orientations of grains on the anode-side and cathode-side of stationary voids in both passivated and unpassivated Cu damascene lines. We found that while certain grain orientations have high diffusivities and others have low diffusivities, these two extremes differ only by a factor of about 4 [Choi Ch.6b]. This variation will be used in a number of the simulations described below.

7.3 RESULTS

7.3.1 Conditions for Void Nucleation at Grain Boundaries

We will first consider whether or not void nucleation at grain boundaries is likely. We consider a simplified scenario illustrated in figure 7.3(a), which would be expected in a narrow line with bamboo or near-bamboo grain structures. As discussed above, interface diffusivities vary with the crystallographic orientations of grains, causing an electromigration flux divergence at grain boundaries.

In order to assess the effects of different diffusivities in various grains on stress evolution, we have simulated behavior in a 50μm-long via-terminated interconnect segment with and without 1μm-long grains, with a randomly assigned diffusivity for

each grain of $0.5D_0$, D_0, or $2D_0$, where D_0 is the average diffusivity (with $0.5D_0$ to $2D_0$ represents the range of diffusivity variations suggested by experimental measurements). The first grain was manually set to have a diffusivity of D_0. This simulation was compared with simulation of stress evolution in a 50μm-long interconnect segment with uniform diffusivity of D_0.

Figure 7.4 shows the results from these two simulations. In the case of uniform diffusivity (Figure 7.4(a)), the stress rises to that required for void nucleation, σ_{nuc}, at the cathode via. Once this occurs it is assumed that the stress adjacent to the void falls immediately to zero, so that over time, the tensile stress everywhere along the line drops to, or below, zero, and the compressive stress continues to increase at the anode. Eventually the electron wind force is balanced by the back-stress force and electromigration stops with the cathode stress at zero the anode stress at a fixed value $\sigma_{comp,max}$ (assumed to be less than the critical stress required to cause compressive failure, σ_{comp}). At this point there is a constant stress gradient between the vias and both the magnitude of $\sigma_{comp,max}$ and the stress gradient scale with j.

Figure 7.4(b) shows the results for a segment with varying interface diffusivities. The differences in diffusivities at grain boundaries initially lead to mass accumulation (compressive stress) or depletion (tensile stress) at the boundaries, and stress gradients

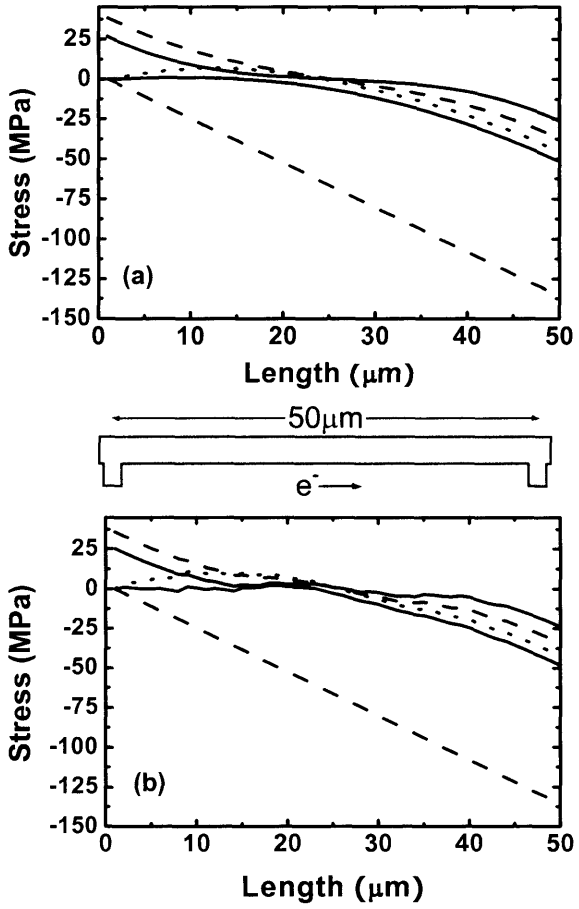

Figure 7.4 Stress-profiles along a 50μm-long line after four 100-minute steps and after the last step at 10000min., when the evolution stops due to a balance of the electron wind force and the back stress (j=0.5MA/cm^2, T=350°C, σ_{nuc}=40MPa). **(a)** uniform diffusivity of D_0=4.5x10-16m^2/s throughout the line. **(b)** diffusivities of either $D_0/2$, D_0, or $2D_0$ randomly assigned to 50 1μm-long grains (so that the average diffusivity is D_0.

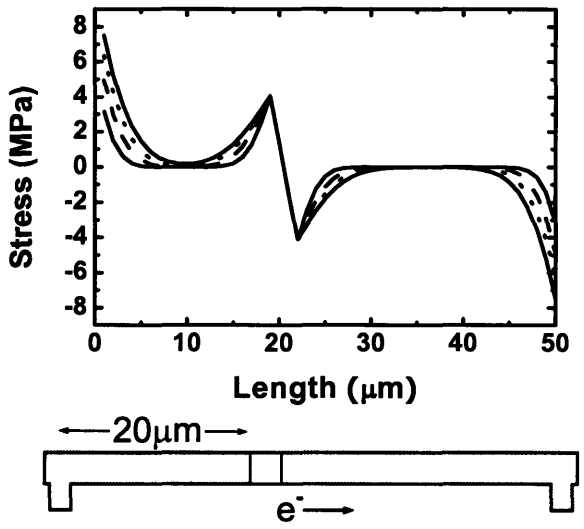

Figure 7.5 Stress profiles after 2-minute intervals, with a 2μm-long grain 20μm away from the cathode via with a diffusivity of $100D_0$ (with a diffusivity of D_0 everywhere else along the line). ($j=0.5MA/cm^2$, $T=350^oC$, $\sigma_{nuc}=40MPa$) Notice that the cathode edge of the grain quickly reaches a local maximum stress that is initially higher than the stress at the cathode via, but that the stress at the cathode via eventually exceeds this local maximum stress.

along grain lengths. However, these effects are always small compared to those found at the vias and even the small gradients within grains or grain clusters are 'washed out' near the vias. By comparing the results in figures 7.4(a) and 7.4(b), we see that both the time and location for void nucleation are unchanged by the grain-by-grain diffusivity variations expected in narrow copper interconnects.

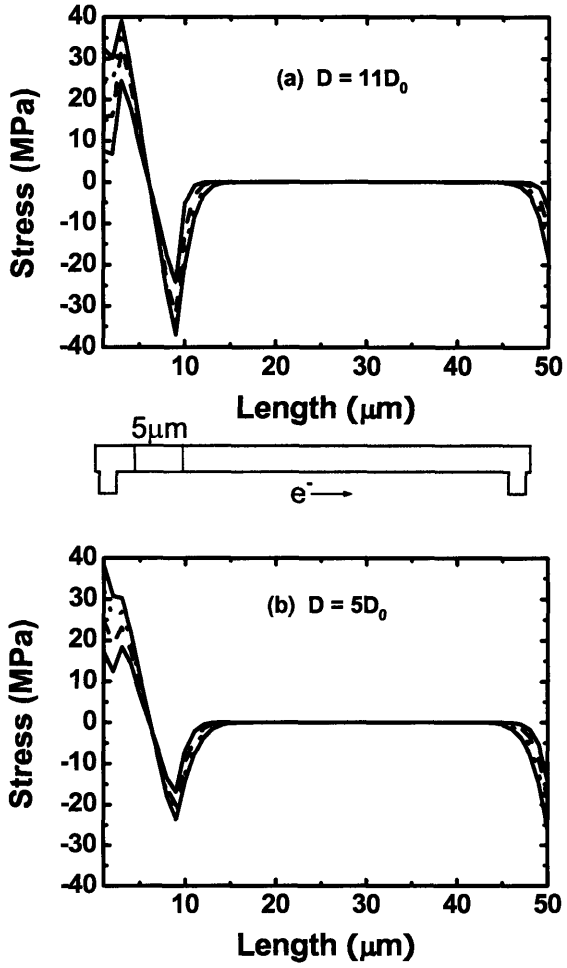

Figure 7.6 Stress profiles after four 2 minute intervals for an interconnect segment with a 5μm-long cluster of grains with a high diffusivity, with the diffusivity elsewhere set at D_0. (j=3.0MA/cm^2, T=350°C, σ_{nuc}=40MPa.) The high-diffusivity grain cluster is 3μm away from cathode via in the 50μm-long interconnect segment. The diffusivity in the high-diffusivity cluster is $11D_0$ in **(a)** and $5D_0$ in **(b)**. The tensile stress reaches σ_{nuc} (40MPa) first at the cathode edge of the cluster in (a) and first at the cathode via in (b).

Next consider the existence of a single grain with a diffusivity 100 times the average value ($100D_0$). Figure 7.5 shows results for a 2μm long grain located 20μms away from the cathode ($j = 0.5 \times 10^6$ A/cm^2). The stress within the grain quickly evolves until the electron wind and back-stress forces are balanced. The tensile stress at the cathode end of the grain then stops increasing, and the critical stress for void nucleation is again first reached at the cathode. The magnitude of the tensile stress reached at the cathode side of the high diffusivity grain is determined by its length (according to a relationship of the type given by equation (7.3)). If we assume that there was a cluster of high diffusivity grains in a segment composed otherwise of grains with average diffusivities, we find that the cluster would have to be 28μm long (~28 or more high-diffusivity grains in a row) for the stress to reach the critical value at the cathode-end grain boundary before it is reached at the cathode via. Assuming the actual current density of a service condition is around 0.1×10^6 A/cm^2, the length of the cluster needs to be 140μm. This is unlikely.

We next consider the effects of a 5μm-long high-diffusivity grain cluster 3μm from the cathode. Here we have used a higher current density (3×10^6 A/cm^2) to amplify the effects of the high-diffusivity segment. Results from two cases are shown in figure 7.6, with the magnitude of the diffusivity in the high-diffusivity segment of set

at $5D_0$ (Figure 7.6(a)) or $11D_0$ (Figure 7.6(b)). Only in the later case (and higher diffusivities) is the critical stress first reached at the grain boundary instead of the cathode via. For this to happen at 0.5×10^6 A/cm^2, the diffusivity in the 28μm long high diffusivity segment would have to be more than $70D_0$.

It can be seen then that the only scenarios that lead to void nucleation at grain boundaries are very unlikely, and that the probability of void nucleation at a grain boundary decreases with decreasing current density.

7.3.2 Effects of Pre-Existing Voids

Pre-existing voids, which are believed to be present due to tensile stresses associated with differential thermal expansion [Ogawa 2002], have been observed in untested Cu interconnects [Nucci 1995] [Sekiguchi 2001] [Sekiguchi 2003] [Chang 2007]. As argued above, the observation of voids at locations other than the cathode via strongly suggests that they have grown from pre-existing voids. Voids that have grown to cause failure away from the cathode via are commonly observed in failure analyses after accelerated lifetime testing [S.Hau-Riege 2002, Chang 2007]. Also void growth and drift at locations away from the cathode have been observed through in situ observations in fully passivated copper interconnects [Meyer 2002, Zsechech 2004,

Choi Ch.5]. Pre-existing voids may therefore be common.

In this section we will investigate the effects of pre-existing voids on void nucleation at the cathode and the conditions that lead to the growth of pre-existing voids. The void divides the line into a cathode-side region (region 1) and an anode side region 2. To simplify the discussion, we will in most cases assume that the diffusivity is uniform along the line in these two regions, and consider the effects of pre-existing voids at different locations along a 1000μm-long via-terminated line. We assume that the void does not fully span the line and that remains pinned at fixed location (e.g., at a grain boundary). We also assume the current crowding and joule heating effects near the void are negligible. We have picked simulation conditions that match those under which voids have been observed to grow in in-situ experiments [Choi Ch.5], and have chosen kinetic parameters that match observed void growth rates.

7.3.2.1 Void Nucleation at the Cathode

We first consider the case when a void is at a significant distance from the cathode via, L_c. Figure 7.7(a) shows stress evolution in the presence of a void at L_c=5μm. The stress between the void and the cathode via evolves in the same way it evolves without a void, up to the time at which the critical stress for void nucleation at the cathode via is reached. Pre-existing voids that are at this distance from the cathode

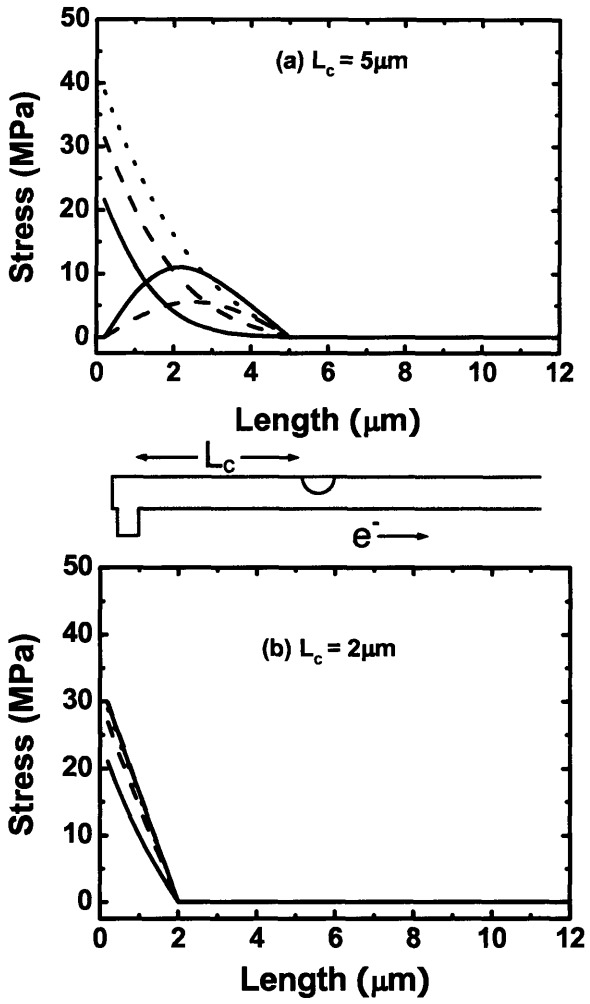

Figure 7.7 Stress profiles at the cathode end of an interconnect segment after five 1-minute time intervals with a pre-existing void **(a)** 5μm and **(b)** 2μm away from the cathode via. (j=3.0MA/cm^2, T=370°C, σ_{nuc}=40MPa) In case (a) the stress at the cathode via reaches σ_{nuc} and the stress in the region between the void and the cathode via quickly relaxes to zero. In case (b) the stress stops evolving when a force balance develops, and a void does not nucleate at the cathode via.

are therefore not expected to affect void nucleation at the cathode.

When a pre-existing void is placed closer to the cathode its effects can be much different, as can be seen in figure 7.7(b) for L_c=2μm. In this case, the stress in the segment between the void and the cathode via quickly reaches the condition in which there is a balance between the electron-wind force and the back-stress, and the stress at the cathode does not reach σ_{nuc}. Therefore, when pre-existing voids lie within a critical distance $L_{c,crit}$ from the cathode they are expected to prevent nucleation of voids at the cathode. This critical distance can be determined by recognizing that the stress at the cathode will reach σ_{nuc} only when

$$jqz^*\rho < \Omega\frac{\sigma_{nuc}-\sigma_0}{L_c} \tag{7.4}$$

so that

$$L_{c,crit} = \frac{\Omega(\sigma_{nuc}-\sigma_0)}{jqz^*\rho}, \tag{7.5}$$

where σ_0 is the initial stress, here taken to be zero. It should be noted that as j is decreased, $L_{c,cr}$ increases, so that when pre-existing voids are present the probability that

a void will nucleate at the cathode decreases as j is decreased.

7.3.2.2 Void Growth Near the Anode Via

Figure 7.8(a) shows stress evolution when a void is present at a distance L_a=5μm from the anode via. Here we have assumed that the critical stress for compressive failure, σ_{comp}, is large. In analogy with the results shown in figure 7.7(b), the affect of the void is to cause the segment between it and the anode via to quickly reach a force balance, so that the stress at the anode via approaches a fixed value that may be less than σ_{comp}. As this is happening, the void will grow or shrink at a rate dictated by the difference in the diffusivities for the anode-side and cathode-side grains. However, as back-stress forces become important near the void it will always shrink. The rate at which the void will shrink (even when the diffusivities are the same in regions 1 and 2) depends on the distance of the void from the cathode via, as shown in figure 7.8(b). It should be noted that in all cases the same steady state growth rate is reached. What changes is the time it takes to reach this steady state, which increases as the distance from the anode via, L_a, increases. It should also be noted that the steady state growth rate scales with j.

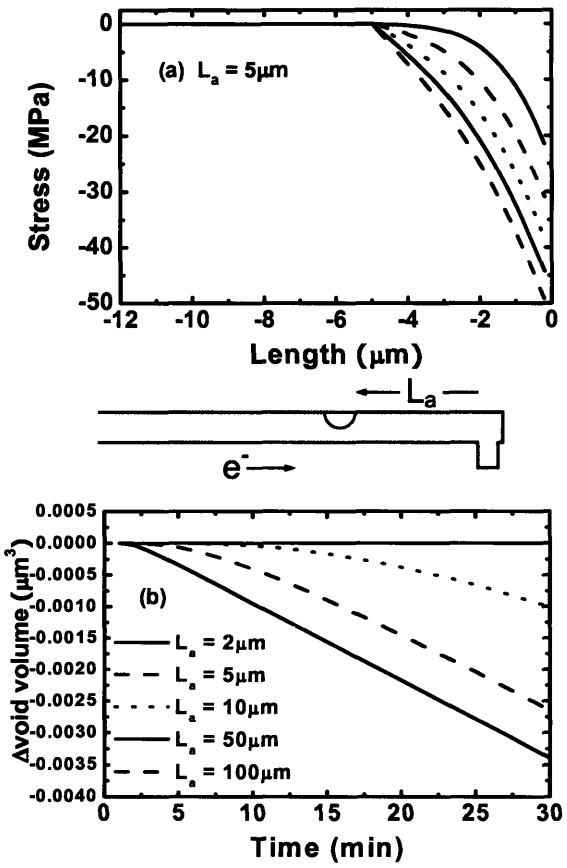

Figure 7.8 (a) Stress profiles after five 1-minute. intervals at the anode end of an interconnect segment with a pre-existing void 5μm away from the anode. **(b)** Change in void volume of a pre-existing void as a function of time for voids at different distances La from the anode via. (Segment length = 1000μm, j=3.0MA/cm^2, T=370°C, D=D_0 everywhere a long the segment.)

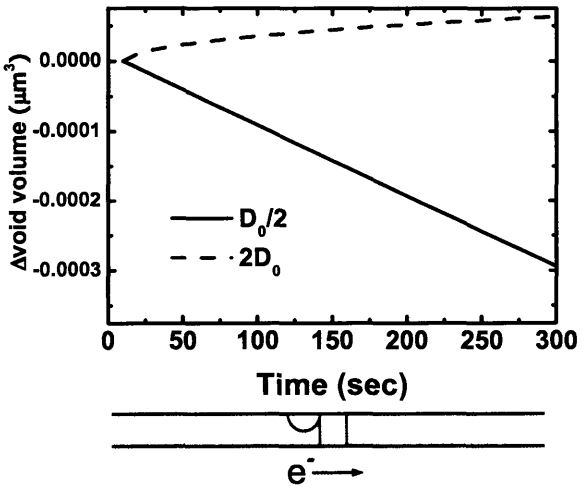

Figure 7.9 Change in the volume with time for a pre-existing void in the middle of a 50μm-long interconnect segment. The grain on the anode side of the void is 0.6μm long , with a diffusivity varied from $D_0/2$ to $2D_0$, while all other regions have diffusivity D_0 (j = 3.0MA/cm^2, T = 370°C).

7.3.2.3 Void Growth Far from the Vias

If a pre-existing void lies at a distance greater than $L_{c,cr}$ from the cathode and $\sigma_{nuc} << \sigma_{comp}$, whether or not it will grow or shrink depends on the diffusivity of the anode-side grain relative to the diffusivity of the cathode-side grain. This is illustrated in figure 7.9 for a simple case in which the diffusivity on the anode-side grain is either $D_0/2$ or $2D_0$, and the diffusivity is D_0 everywhere else. When the diffusivity of the anode-side grain is smaller than D_0 the void will shrink at a constant rate that scales with j. When the diffusivity in the anode-side grain is smaller than D_0, the void will

grow. However, the rate of void growth diminishes over time. This effect is explored in more detail in the next section.

7.3.2.4 Void Growth Near the Cathode Via

Figure 7.10(a) shows the change in void volume as a function of time for a void located near the cathode but still at a distance L_c greater than $L_{c,cr}$. In this case, we have assumed that there is no difference in diffusivity in either region, so that void growth results from effects associated with stress evolution alone. It can be seen that while voids at $L_c > L_{c,cr}$ grow, their growth saturates. The voids first grow because a stress gradient between the void and the cathode via develops and drives a flux of atoms out of the void, while no stress gradient exists on the anode side. When $L_c > L_{c,cr}$, a void will eventually nucleate and grow at the cathode. This lowers the stress between the cathode via and the pre-existing void until no gradient exists, and the void stops growing. This happens more quickly and leads to a larger final void size the closer L_c is to $L_{c,cr}$. Therefore, for $L_c > L_{c,cr}$ continued void growth occurs only due to differences in diffusivities in the anode-side and cathode-side grains, However, even in this case local force balances within grains will lead to a zero net growth so that growth will still saturate at a size that depends on the probability of finding long clusters of high-

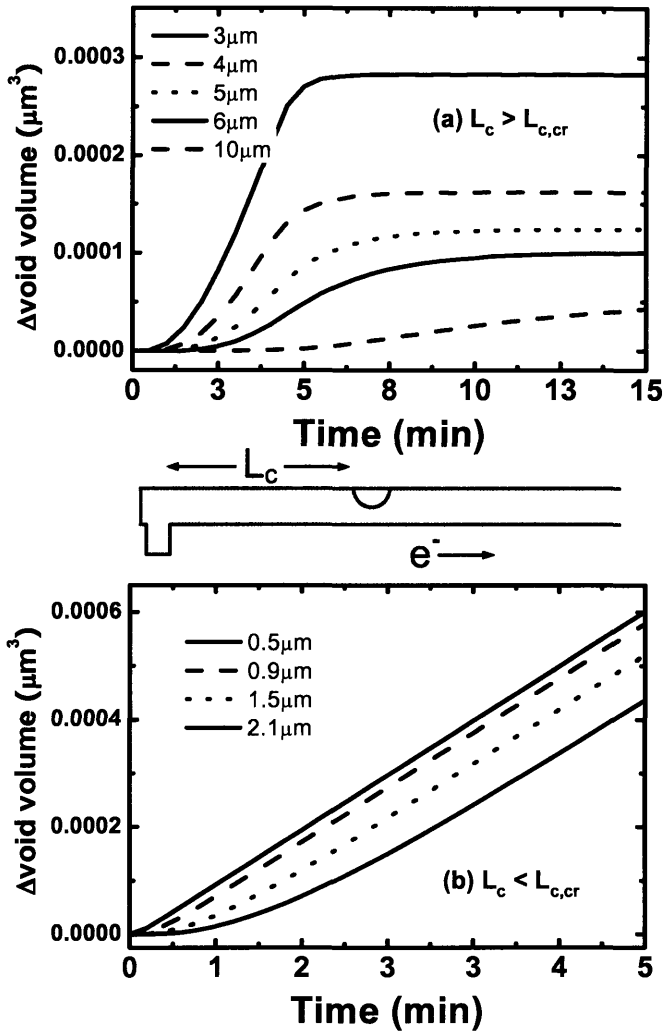

Figure 7.10 Change in void volume as a function of time for pre-existing voids at different distances from the cathode via L_c (j = 3.0MA/cm^2, T = 370°C, σ_{nuc}=40MPa, D=D_0 everywhere). **(a)** When $L_c > L_{c,cr}$, void growth saturates. **(b)** Only when $L_c < L_{c,cr}$ do voids continue to grow.

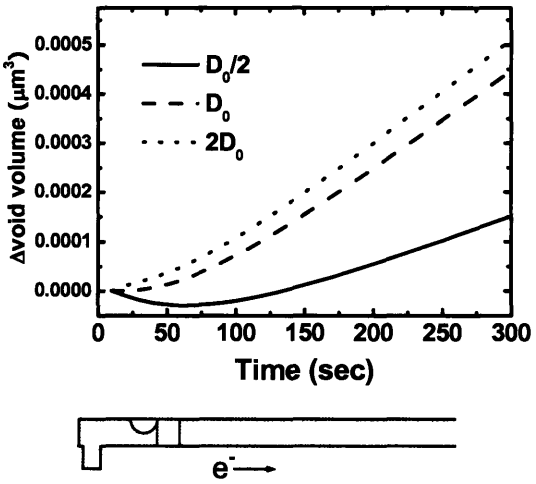

Figure 7.11 Change in the volume with time of a pre-existing void 2mm away from cathode via with an anode-side 0.6μm-long grain with diffusivities $D_0/2$, D_0, and $2D_0$, with the diffusivity set to D_0 everywhere else ($j = 3.0MA/cm^2$, $T = 370°C$).

diffusivity and low-diffusivity grains. It should be noted that in all cases these voids will eventually shrink when the effects of the flux divergence at the anode via leads to stress gradients on the anode side of the voids.

When a pre-existing void is at a distance L_c that is less than $L_{c,cr}$ its growth is much different. Figure 7.10(b) shows the change in volume with time for voids at different distances L_c less than $L_{c,cr}$. In all cases, the void grows without limit (even without diffusivity variations). Referring back to figure 7.7(b), recall that in this case a force balance develops and a constant stress gradient develops between the void and the cathode via. Once this happens there is a driving force for a flux of atoms out of the

void, toward the cathode, while at the same time there is no stress-related driving for a flux of atoms into the void. When this happens the void grows at a constant rate. It should be noted that this constant rate is not a function of L_c, and that the constant growth rate scales with j. L_c affects the time required to reach a constant growth rate, with this time increasing toward infinity a L_c approaches $L_{c,cr}$.

Figure 7.11 illustrates the effects of diffusivity variations on growth of voids closer than $L_{c,cr}$ to the cathode via. In this case we let a grain on the on the anode side of the void have different diffusivities D_a, while the diffusivity is fixed at D_0 every where else. The case that $D_a=D_0$ is the same as illustrated above in figure 7.10(b). When $D_a>D_0$, the steady state growth rate is reached earlier and when $D_a<D_0$, the void initially shrinks, but if it does not first disappear it will eventually grow at a rate limited by the steady state growth rate associated with stress effects. If the same void (with $D_a<D_0$) pre-existed at a distance $L_c>L_{c,cr}$, it would shrink and disappear.

7.4 DISCUSSION AND CONCLUIONS:

From the forgoing analyses we conclude that:

1) Observations of voids at locations at locations other than the cathode via strongly suggest that these voids pre-existed before electromigration began.

2) Pre-existing voids that are at a distance from the cathode L_c less than a critical distance $L_{c,cr}$ will prevent nucleation of voids at the cathode via (where $L_{c,cr}$ scales with j).

3) Pre-existing voids at $L_c < L_{c,cr}$ will prevent nucleation at the cathode via and will grow at a rate limited only by a steady state value $\dot{V}$, where $\dot{V}$ scales with the current density, $\dot{V} \propto j$.

4) Pre-existing voids at distances $L_c > L_{c,cr}$ may grow, but their size will be limited and they will eventually shrink and disappear. Such voids will not affect either the probability or time for void nucleation at the cathode via.

First, it is important to recall that in the absence of pre-existing voids, the time required to reach the critical stress for void nucleation at the cathode scales with j^{-2}, while, because $\dot{V} \propto j$, the time required for a pre-existing void to grow to a size that will cause failure scales with j^{-1}. Therefore if an interconnect segment has pre-existing voids within $L_{c,cr}$, void growth will lead to failure at lifetimes that will scale with j^{-1}. If there are no pre-existing voids within $L_{c,cr}$, both nucleation and growth are required for failure and the time for failure will have a current density dependence that can range from j^{-2} scaling if failure is nucleation limited to j^{-1} scaling if failure is growth limited. Therefore, if there is a low density of pre-existing voids, some lines will fail

due to growth of pre-existing voids and some will not. This creates two populations of segments failing with very different mechanisms which have different current density dependencies. This will lead to multimodal failure time distributions, and will greatly complicate life-time projections, not only because the different failure mechanisms must be separated in statistical analyses, but also because lifetime projections will require different current density scaling.

It should be further noted that $L_{c,cr}$ itself scales inversely with j, so that for a fixed density of pre-existing voids, the fraction of a test population of segments that will fail due to growth of pre-existing voids will be higher at low current densities (service conditions) than at high current densities (test conditions). This also greatly complicates scaling of test results to service conditions. At high current densities, void nucleation is expected, so that in this regime, j^{-2} scaling is expected, even though at lower currents, where most lines fail due to the growth of preexisting voids, j^{-1} scaling might be found. This might explain why Rosenberg *et al* [Rosenberg 2000] observed both j^{-2} scaling at high current densities and j^{-1} scaling at lower current densities in a single set of experiments. It may also explain why there are reports of both approximately j^{-2} [Padhi 2003] and j^{-1} scaling [Wei 2003, Vairagar 2004] found elsewhere in the literature. If results from populations with a mixture of modes are fit to

a j^{-n} scaling relationship, it would be expected that values *between* 1 and 2 would be expected, which might also explain values of n=1.5 found by Padhi *et al* [Padhi 2003]. Proper scaling would require isolation and characterization of results for growth of pre-existing voids (if they exist), either by testing at low current densities or through use of special test structures. Alternatively, scaling can be conservatively carried out by assuming j^{-2} scaling.

In the forgoing analyses we have not considered the effects of void drift. As discussed in the introduction, voids can be pinned at grain boundaries, due to the energy required to replace the grain boundary once a void drifts away. However, void drift has been observed in in-situ experiments in which it is usually observed that voids usually grow in place before drifting toward the cathode. As also outlined in the introduction, this is consistent with the expectation that a void must grow to a critical size V_{crit} before it can de-pin from a boundary. The magnitude of this critical size scales inversely with the square root of the current density.

As discussed above, pre-existing voids at $L_c<L_{cr}$ might be expected to rapidly reach the critical size for de-pinning, and drift to the cathode where they either continue to grow or coalesce with other voids to cause failure. The overall rate of failure will not be greatly affected by de-pinning in this case. As also discussed above, pre-

existing voids at $L_c > L_{c,cr}$ will grow only if the anode-side grain has a diffusivity higher than the cathode-side grain, and even then the growth rate will saturate and eventually become negative. However, it is still possible that pre-existing voids at $L_c > L_{c,cr}$ might drift to locations for which $L_c < L_{c,cr}$, and then more rapidly grow, drift, and/or coalesce to contribute to failure. It should be noted though that this possibility becomes even less likely at lower current densities, as the critical size for de-pinning is larger and the rate of void growth is smaller. Void drift is therefore considered to not affect the conclusions discussed above.

Finally, the forgoing discussion has focused on the case in which the vias lie below the test segment (Figure 7.1). Similar effects are expected in when vias lie above the test segments (Figure 7.2). However, tests of lines in these two configurations generally lead to different lifetimes [Gan 2001, Padhi 2003], because the fatal void volume is higher for via-below test structures [S.Hau-Riege 2002, Gan 2001]. This may also lead to a greater sensitivity to nucleation of voids at or near the via for via-above than for via below configurations, and an associated difference in fitted current density scaling exponents for these to types of configurations, as observed by Padhi *et al.* [Padhi 2003].

7.5 SUMMARY

Electromigration-induced tensile stresses in void-free via-terminated interconnect segments are expected to first reach the magnitude required for void nucleation at the cathode via. However, in both post-testing failure analysis and in in-situ electromigration testing, voids are often observed at locations other than the cathode via. We have shown that observations of such voids strongly suggest that they have grown from voids (perhaps quite small voids) that existed before electromigration testing was started. Such voids have often been observed and usually are the results of tensile stresses associated with differential thermal expansion during interconnect fabrication.

It is also shown that the existence and frequency of occurrence of pre-existing voids will significantly affect the mechanism of failure, including the current density dependence of the time to failure. It is further argued that the effects of pre-existing voids become more important at lower current densities compared to the higher current densities used in lifetime testing. The consequence is that scaling of test results to service conditions is complicated not only by the presence of multiple failure modes with different current density scaling, but also by a change in the mode frequency as test results are scaled to service conditions.

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CHAPTER 8

CONCLUSIONS AND FUTURE WORK

8.1 SUMMARY

Previously, reliability assessment of copper interconnects has been carried out with under assumptions that a specific limited number of failure mechanisms operate, which can lead to an inaccurate extrapolations of tests results to operating conditions. By introducing new experimental techniques and a new simulation tool, a number of additional failure mechanisms were identified and analyzed in this thesis

8.1.1 xSim

A simulation tool based on the one-dimensional Korhonen model was developed to assist in identification and analysis of failure mechanisms. The new simulation tool, xSim, has most of the features from the previous version by V. Andleigh (called EmSim), plus an improvement listed in 1. Following key features are:

1. Implemented implicit method to reduce calculation time and improve stability.

2. Able to construct more complex interconnect trees, with application of independent current densities in each segment, to allow analysis of stress/atomic concentration interactions between segments.

3. Able to change current densities of the segment while running the simulation.

4. Able to obtain void volume as a function of time.

5. Set different values of failure criteria by changing σ_{crit} or the critical void volume for failure.

6. Manually insert pre-existing voids at desired locations.

7. Manually vary diffusivities of individual grains.

8. Able to simulate the conditions for liner ruptures.

8.1.2 Effect of Adjacent Segments

Dotted-i structures, in which is two 25μm-long segments are connected with a via in the middle, were tested to observe the stress interactions between two segments. We observed that the stress state of a segment strongly depends on the state of the adjacent segment. Therefore, even though the product of current density and length (jL) of the segment is lower than $(jL)_{crit}$, failure can still occur, depending on the state of the adjacent segment. Moreover, even if the adjacent segment has no electrical current, it acts as a passive reservoir, and leads to a different stress state than that of the segment without an adjacent segment. More specifically, if the inactive segment is adjacent to the anode side of the active segment, the maximum tensile stress, σ_{max}, at the cathode is given as:

$$\sigma_{max} = \frac{Z^* \rho j e}{2\Omega}\left(\frac{2ap + a^2}{a + p}\right), \tag{4.5}$$

where a is the length of active segment, p is the length of inactive segment. From this, σ_{max} of a segment with an adjacent inactive segment can be as much as twice that of a segment without the adjacent segment. Similarly, the maximum void volume with an adjacent segment is significantly larger than that of a segment without an adjacent segment. Therefore, it is important to consider even the inactive segments in interconnect trees to accurately locate the most probable location for failure and to also correctly predict failure times.

8.1.3 Dynamics of Voids Away from the Cathode

8.1.3.1 Accelerated EM Tests with In-Situ SEM

Accelerated electromigration (EM) tests were performed while top-view imaging of the cathode region of the interconnect, using scanning electron microscopy (SEM). The tests revealed that the failures not only occur by void nucleation and growth at the cathode but voids also grow away from the cathode to cause failure. They grow at a junction between copper/passivation-layer interface and a grain boundary. These voids away from the cathode grow to a certain size, de-pin from the grain boundary, and drift

to the cathode, some times diving into the bottom of the via (in M2) to cause the failure. With simple analyses, the drift velocity is found to be directly proportional to the surface diffusivity of the void surface. Some voids also grow to span the width and thickness of the interconnect at the initial location and cause the failure by shunting current through higher resistance liner material.

After in-situ tests, the top passivation layer was removed and grain texture/orientation mapping carried out using an electron backscatter diffraction (EBSD) tool. The shape and drift velocity of voids away from the cathode depend on the crystallographic texture of the grains in the interconnect.

8.1.3.2 Vacuum EM Tests

A separate set of experiments was carried out to measure average surface diffusivities for copper and relative diffusivities for grains with different orientations. Unpassivated test structures were tested in a home made vacuum EM station to obtain these results. Using measurements of the void volume at the end of the cathode as a function of test time, the average surface diffusivity for copper was extracted. The activation energy was found to be 0.45±0.11eV, and the pre-factor, D_o, was found to be 3.35×10^{-12} m^2/s. Without passivation, voids also grew at flux divergence sites such as

grain boundaries, but they did not drift, due to the relatively high surface diffusivity compared to copper/passivation-layer. We expect that the source for a flux divergence is the differences in diffusivities for different grain orientations. The diffusivities increase in the order (1 1 1), (1 1 5), (7 5 13), and higher out of plane orientations. Note that (1 1 5) is the first generation twin and (7 5 13) is the second generation twin orientation of (1 1 1). These results from unpassivated samples are consistent with limited results from passivated samples observed from in-situ SEM and post-testing EBSD experiments.

8.1.3.3 Effect of the Stress State Around a Pre-Existing Void

Simulation results show that it is very unlikely for a void to nucleate at locations other than at the cathode end of an interconnect segment. Thus, those voids observed away from the cathode in-situ SEM experiment must be due to defects or pre-existing voids. Using the simulation tool, the behavior of pre-existing voids was analyzed. Pre-existing voids were manually inserted in various locations in the interconnect and changes in the void volume, which depends on the stress state around the void, were observed. We found that voids near the anode are likely to shrink and disappear, so that an insignificant contribution to fatal is expected. However, voids near

the cathode may cause a failure. We predict that if the pre-existing voids are within a certain length, $L_{c,crit}$, from the cathode end, they are likely to grow to cause failure, while also preventing a void nucleation at the cathode end. However, if the pre-existing void is further away than $L_{c,crit}$, its growth saturates, and the failure is governed by void nucleation and growth at the cathode end. $L_{c,crit}$ is defined by:

$$L_{c,crit} = \frac{\Omega(\sigma_{nuc} - \sigma_0)}{jqz^*\rho}, \tag{7.5}$$

where σ_{nuc} is the critical stress for the void nucleation and σ_0 is the initial stress. From equation (7.5) we observe that $L_{c,crit}$ increases with decreasing current density, j. Thus, at low current densities, there is a higher probability of having pre-existing voids within $L_{c,crit}$, leading to more fatal failures due to pre-existing voids.

8.1.4 Effect of Pre-Existing Voids on Current Density Exponent

8.1.4.1 Low Current Density

A current density exponent close to 1 is observed at low current densities. We suspect that this is due to two effects. First, as explained above, low current densities lead to longer $L_{c,crit}$, causing more failures due to pre-existing void. Secondly, the

critical void volume required to de-pin from the grain boundary increases with decreasing current density, according to:

$$R_d = \sqrt{\frac{3\gamma_{gb}\Omega}{4qz^*\rho j}}, \tag{7.1}$$

where R_d is the radius of the void required to de-pin from the grain boundary. Thus, especially in interconnects with small dimensions, pre-existing voids are likely to grow to span the width and thickness of the interconnect before it de-pins and drifts toward the cathode. This may cause failure by electrical shunting through higher resistant liner material.

Combining the above two effects, the failure at low current densities may be predominantly by growth of the pre-existing void, leading to a current density exponent of 1 (void-growth-limited failure).

8.1.4.2 High Current Density

At high current densities, voids are likely to nucleate at the cathode end, which can lead to void-nucleation-limited failure or mixture of void-nucleation-limited and void-growth-limited failures. This can lead to a current density exponent that is greater

than 1 (up to 2).

8.2 CONCLUSIONS

By introducing new experimental techniques and utilizing an internally developed simulation tool, new Cu-interconnect reliability issues have been identified.

First, by testing and analyzing dotted "i" interconnect trees, inactive segments are shown to be as critical as active segments for reliability of interconnect trees. Therefore, a current method of identifying $(jL)_{eff}$ must be modified to include the contribution from the inactive segment for more accurate reliability assessment of both Cu-based and Al-based interconnects. Also, process defects, such as discontinuous liner at the bottom of the via, can lead to a variation in lifetime of the interconnect.

Second, EM tests with in-situ SEM show that open circuit failures are not only by the void nucleation and growth at the cathode end of the interconnect. Pre-existing voids that are away from the cathode can also cause the failure. Pre-existing voids can either grow to span the thickness and width of the via or drift into the bottom of the via to cause the open circuit failure. We have also observed the effect of crystallographic orientation of copper grains on motion and shape of the voids that can lead to variations in lifetime of the interconnects.

We have shown that at low current densities, a failure by growth of a pre-existing void may be more likely to occur than a failure by void nucleation and growth at the cathode end. This leads to current density exponent (n) value close to 1 at low current densities while n is close to 2 at high current densities. This is critical because most accelerated EM tests are performed at much higher current densities than that of the service conditions. Thus, using values obtained from EM tests (with n close to 2) to extrapolate lifetimes at service conditions can be too conservative.

Studies in this thesis can lead to better understanding of reliability of metal interconnects especially Cu-based interconnects. We have shown that it is critical to understand detailed geometry of the interconnect trees (both active and inactive segments) as well as fabrication defects (missing liners or pre-existing voids) in order to correctly assess the reliability of the interconnect.

8.3 PROPOSED FUTURE WORKS

There are a few experiments that can be carried out to further clarify the phenomena described in this thesis.

A. With unpassivated samples, one can have various surface treatments before

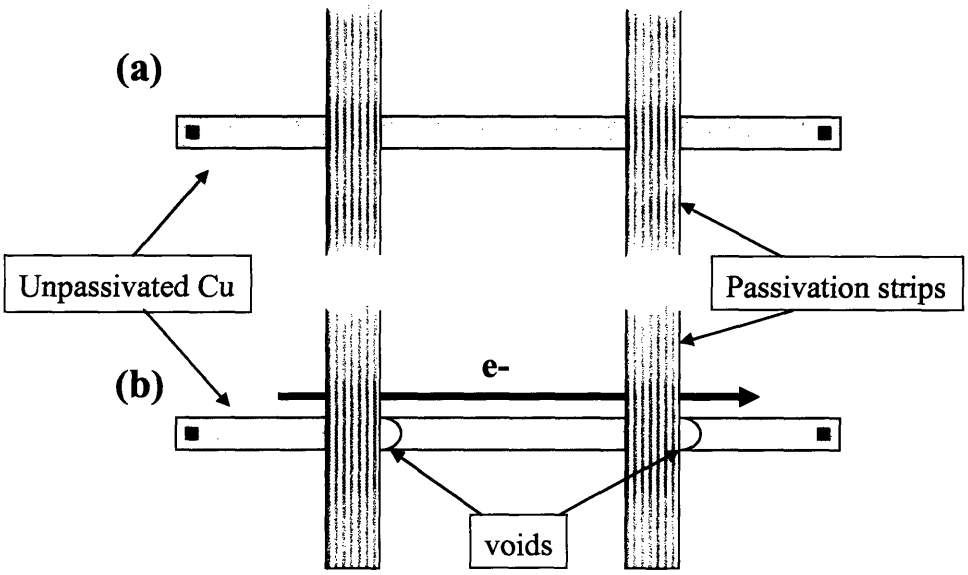

Figure 8.1 **(a)** Unpassivated test structure with strips of passivation of desired material. **(b)** Assuming surface diffusion is higher than the interface diffusion, voids will grow at the edges of the passivation.

passivation and compare the diffusivities of untreated and treated samples. Preliminary results with self-assembled monolayer (SAM) deposition onto Cu surface are described in appendix A. Various intermediate layers can be deposited between Cu and the passivation layer.

B. By depositing strips of materials perpendicular to the length of the interconnect as shown in figure 8.1, one can obtain the relative diffusivities between surface and Cu/material interface. For example, by depositing strips of Si_3N_4, a void is expected to grow at the boundary between the Cu/Si_3N_4 interface and the Cu surface

(figure 8.1(b)). By obtaining the void volume as a function of test time, the relative diffusivities of the Cu surface and Cu/Si_3N_4 interface can be determined.

C. The current density in fully processed samples can be varied to confirm the proposed failure mechanism by pre-existing void growth with extensive failure analysis.

D. Using in-situ SEM, void pinning at the cathode end can be observed. In teh second metallization (M2) layer, the void is expected to nucleate at the cathode end of the Cu/passivation interface. Some voids grow to a certain size and dive into the via to cause the. There seems to be a critical void volume required for the void to transfer from the Cu/passivation interface to Cu/liner interface. One may identify factors leading to the critical void volume for de-pinning at this location.

E. Quantitatively obtain the relationship between pre-existing void initiated failure and the width of interconnects.

F. Manually insert defects at various locations prior to passivation and observe the failure characteristics.

APPENDIX A

MONOLAYER ON UNPASSIVATED COPPER INTERCONNECT SURFACE FOR REDUCING ATOMIC DIFFUSION

A.1 INTRODUCTION

Electromigration (EM) has been one of the major factors for reliability of metal interconnects. EM is a diffusion of metal atoms induced by momentum from applied electron current. In order to minimize failures due to EM, diffusion of metal atoms must be effectively suppressed. In copper interconnects, dominant or fastest diffusion path is along the interface between copper and top passivation layer (Cu/passivation). Si_3N_4 has been the choice of material for passivation layer. Therefore, suppressing diffusion in Cu/passivation interface is the key to reliability improvement in copper interconnects. Also, it is important that the method that can suppress the interface diffusion should be simple and low cost process in order to be implemented in an actual production fabrication procedure.

A number of attempts have been made to suppress the interface diffusion. One of them is alloying Cu with elements such as Al, Cr, Mg, Pd, Sn, and Zr [C.Hau-Riege 2004]. Alloying with these materials has shown improvements in lifetime of the interconnect, however, it was difficult to prevent resistivity increase of the interconnect.

Second method involves depositing a thin metal cap layer between copper and passivation layer. CoWP, CoSnP, and Pd have been selected as a metal cap [Hu 1998]. Using electroless deposition, these metals selectively deposit on copper surface. Thus, it

does not require an extra lithography step. Also, unlike alloying method, resistance increase is negligible. A number of them showed significant improvements in lifetime. However, one of the problems is having a uniform deposition across the wafer that is as large as 12 inches in diameter.

Third method is depositing organic monolayer between copper and passivation layer. It has been shown that a thiol-terminated monolayers selectively adhere onto only copper surface which may pin the surface atoms and reduce diffusion [Ganesan 2005]. However, one of the main issues with organic monolayers is their thermal resistance. Some of the back-end fabrication processes require temperatures up to 400°C and most of organic monolayers can not resist this temperature. Thus, selecting a monolayer that can withstand high temperatures is the key to this process.

In this paper, we select thiol-terminated diacetylene for suppressing diffusion of copper atoms. We deposited this monolayer onto surface of the copper interconnect and performed accelerated EM tests to observe effect of the monolayer on suppressing diffusion of copper atoms.

A.2 EXPERIMENTAL PROCEDURES

Samples used for this experiment are identical to that of the samples in chapter 6 and appendix B. The samples that were used in this experiment are 1000μm long and either 0.3μm or 1.0μm wide. Monolayer was deposited by Xiaogang Liu. Detailed synthesis of thiol-terminated diacetylene salt is described by Kim *et al* [Kim 1994]. 10^{-4} mol of prepared salt is dissolved in 100mL of $CHCl_3$ to make a 1mM solution. Unpassivated samples were immersed into the monomer solution for 3 hours. The monolayer is cross-linked by exposing 254nm wavelength light from Hg(Ar) UV pen lamp (UV Products Ltd.) for 5 minutes with nominal power of 4.75mW/cm^2. Si_3N_4 passivation layer was not deposited. The samples were mounted to 24-pin ceramic package and wire-boned using Au wires. The package was inserted into the vacuum EM station for accelerated EM test at a temperature of 320°C and 1.85MA/cm^2. Again more detailed procedure of accelerated EM tests in vacuum are described in chapter 6 and appendix B. Tested samples were observed using secondary electron microscopy (SEM) for further analysis.

A.3 RESULTS

Figure a.1 shows the time-to-failure (TTF) results of untreated and SAM treated

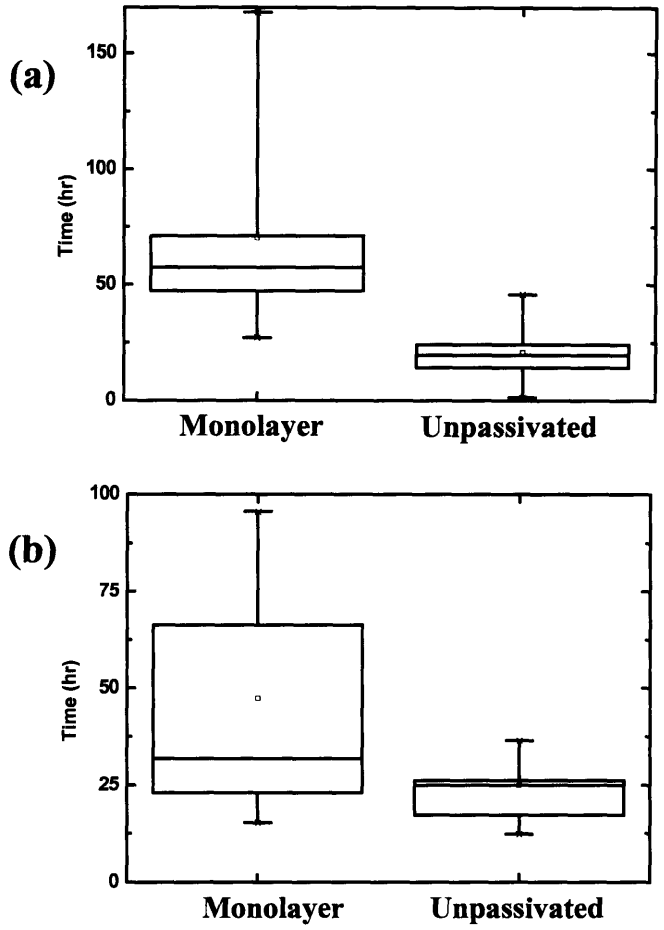

Figure a.1 TTF of unpassivated and monolayer deposited samples. **(a)** 0.3μm width and **(b)** 1.0μm width samples.

samples. The result shows that TTF of the SAM treated samples is two to three times longer than that of the untreated samples. SEM images of the tested samples show inconsistent surface morphology (Figure a.2). There were regions where surface looks contaminated and shows precipitates of some kind (Figure a.2(a),(b)), while some

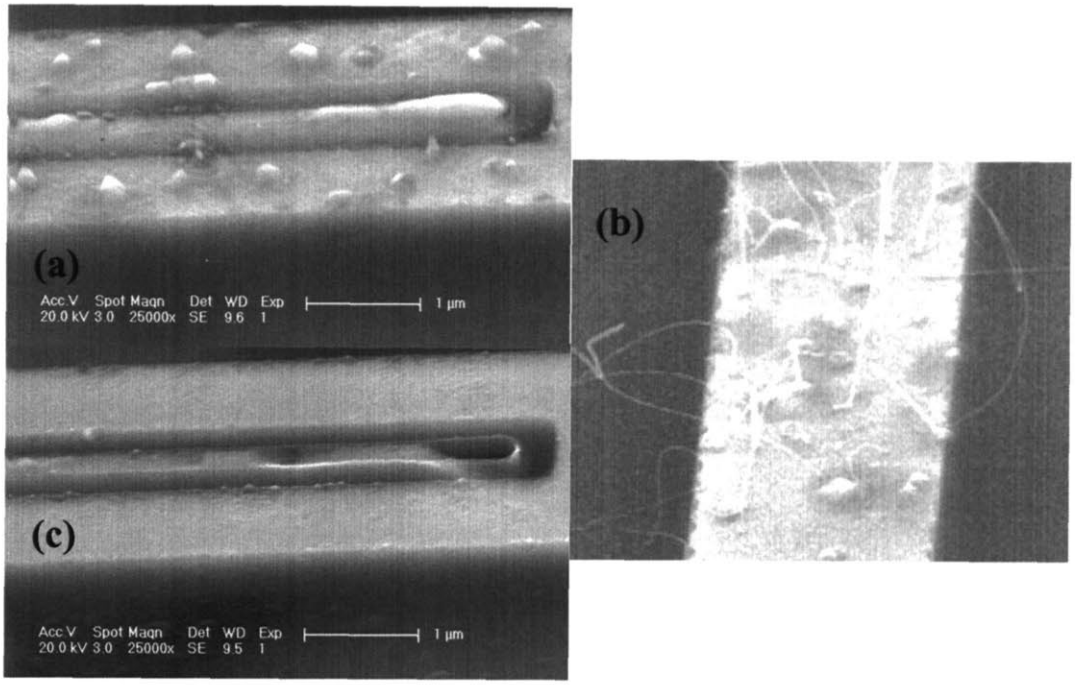

Figure a.2 Monolayer deposited samples after EM tests. **(a)** shows precipitate-like spots in extrusion monitor righ and test line. **(b)** Region showing nanowire growth **(c)** Region with clean surface.

regions show no signs of any disturbance (Figure a.2(c)). However, TTFs showed no dependence on these different regions.

A.4 DISCUSSION

A molecular structure of thiol-terminated diacetylene is shown in figure a.3 [Kim 1994]. It is well known that thiol end of the molecule selectively adheres to the gold surface [Batchelder 1994], behaving as a self-assembled monolayer (SAM). Since Cu-S [Gimarc 1983] and Au-S [Kim 1994] have similar bonding energies, thiol-

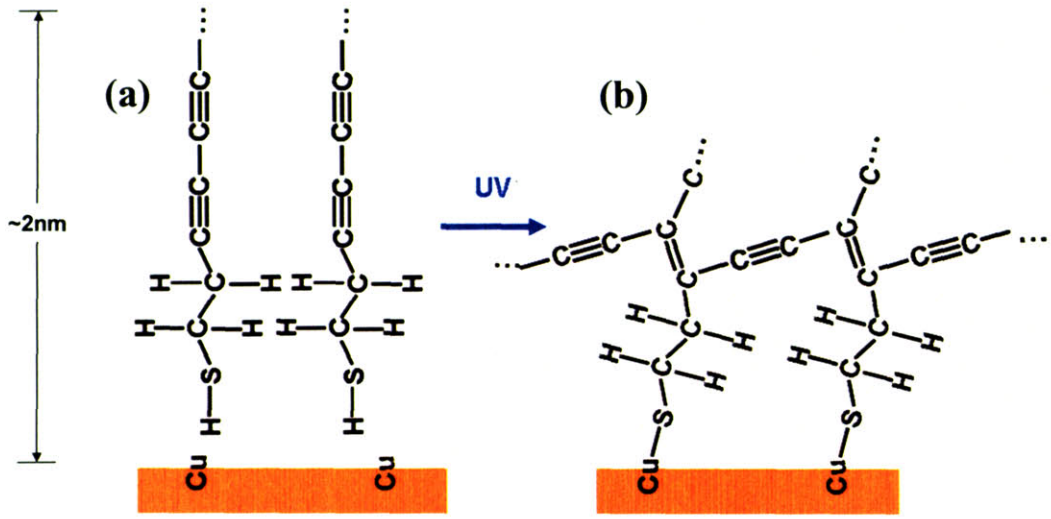

Figure a.3 (a) Thiol group of diacetylene adheres to Cu surface. **(b)** UV light turns triple bonds in diacetylene to cross-linked double bonds with other molecules.

terminated diacetylene is expected to adhere on copper surface as well as on gold surface. Then with ultraviolet light, triple carbon bonds in diacetylene break into double bonds and the remaining bond cross-links with the neighboring molecule, as shown in figure a.3(b) [Wegner 1969]. The cross-linked monolayer is known to resist elevated temperature condition [Kim 1996]. Thus, the monolayer may be able to withstand the later process of Si_3N_4 passivation, which is usually done with PECVD at 400°C.

The thickness of the monomer on copper surface is obtained by ellipsometry [Kim 1996], however, this technique alone does not guarantee the uniform deposition of the monolayer onto the entire surface of the substrate. From the observed SEM images after the EM tests (Figure a.2), it is evident that the monolayer was not uniformly

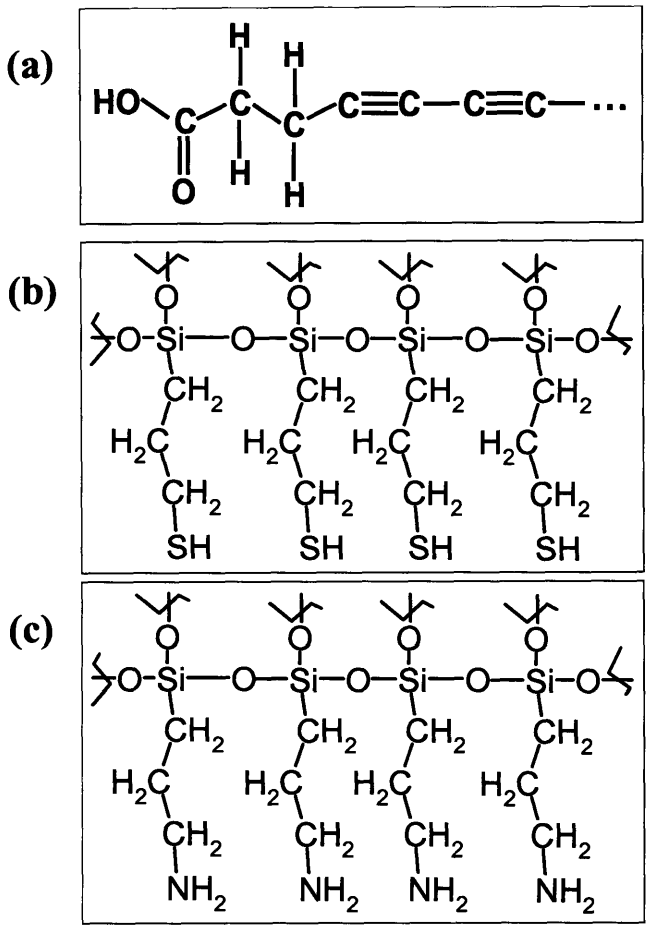

Figure a.4 Other monolayer candidates:
(a) COOH terminated of diacetylene
(b) Mercaptopropyltrimethoxylsilane
(c) Aminopropyltriethoxylsilane

deposited throughout the surface. The monolayer deposition needs to be optimized to give more uniform deposition. Samples with SAM showed an increased TTF compared to unpassivated samples with clean copper surface, but TTF of passivated samples is

Table a.I

MTTF of samples with different monolayers. *Note that a.4(a), a.4(b), and a.4(c) are monolayers described in figure a.4; very limited number of samples are tested.

Samples --- widths	Untreated	Thiol terminated dicetylene	a.4(a)*	a.4(b)*	a.4(c)*
0.3μm	20.56hrs	70.24hrs	19.15hrs	26.38hrs	40.92hrs
1.0μm	25.09hrs	47.48hrs	44.85hrs	63.90hrs	62.88hrs

significantly longer (~460 hours in identical conditions). To make a fair comparison with passivated samples, samples with SAM should also be passivated.

There are other SAM candidates as shown in figure a.4, which are also known to withstand high temperatures by forming cross-links. Preliminary results of these monolayers were also obtained (Table a.I). However, due to low number of tested samples, it is difficult to draw any conclusion.

A.5 CONCLUSION

Thiol-terminated monomers only adhere onto Cu surface, which leads to a very simple process integration – immersing the sample into the monomer solution for self-assembled monolayer (SAM). With a strong bond between Cu and S, the mobility of the Cu atoms at the surface should be well reduced, which can lead to overall improvement

in reliability of Cu interconnects. Thiol-terminated dicetylene was selected because it is resistant to elevated temperature when cross-linked. Preliminary EM tests were performed and showed improvements in TTF compared to unpassivated samples, however, further experiments need to be done for more quantitative and in-depth analysis.

Reference: Appendix A

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APPENDIX B

SETUP FOR VACUUM ELECTROMIGRATION STATION

Vacuum Electromigration Setup

At an elevated temperature, copper oxidizes and continuously forms unstable oxide. Oxidation of copper leads to degradation of copper interconnects. In fully a processed copper interconnect test structure, oxidation is not an issue because copper is surrounded by interlevel dielectric (ILD) and passivation layer. However, test structures we used in chapter 6 and appendix A are structures without top Si_3N_4 passivation layers. Thus, top copper surface of the test structure is exposed. In order to perform accelerated electromigration (EM) test on these samples, high vacuum environment is necessary to minimize the oxidation. Furthermore, native oxide must be removed prior to EM test for accurate observation of copper surface.

Vacuum electromigration station is designed and constructed by Zung-Sun Choi and Reiner Mönig. The samples were mounted on 24-pin ceramic package using the silver epoxy, and the epoxy was cured at 120°C with H_2 gas flow to prevent the Cu from oxidation. Then the sample was gold wire-bonded, and the package was inserted into a vacuum electromigration test chamber (Figure b.1). Main body of the test chamber is a 304L stainless steel five-way cross tube with 6-inch diameter CF flange connections purchased from Kurt J. Lesker Company. One of the five connections leads to TCU-170 turbo pump by Pfeiffer Vacuum Co. with Duo 2.5 rotary vane pump also by Pfeiffer Vacuum Co. A *Micromaze Foreline trap* by Kurt J. Lesker Co. is used between the turbo and rotary pump to prevent turbo pump from oil contamination by the rotary pump. Both pumps are controlled by TCP-300 controller by Pfeiffer. The pressure is measured by an ion gauge and the connection is shown in figure b.1.

A socket made of alumina (received from a courtesy of Chang, Choonwai at

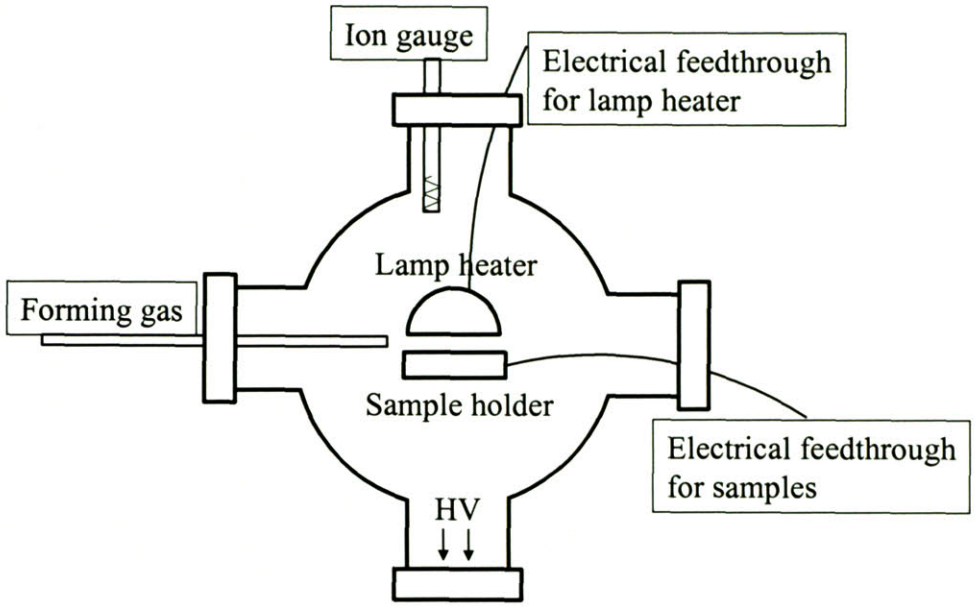

Figure b.1(a) A schematic diagram of vacuum electromigration test chamber setup.

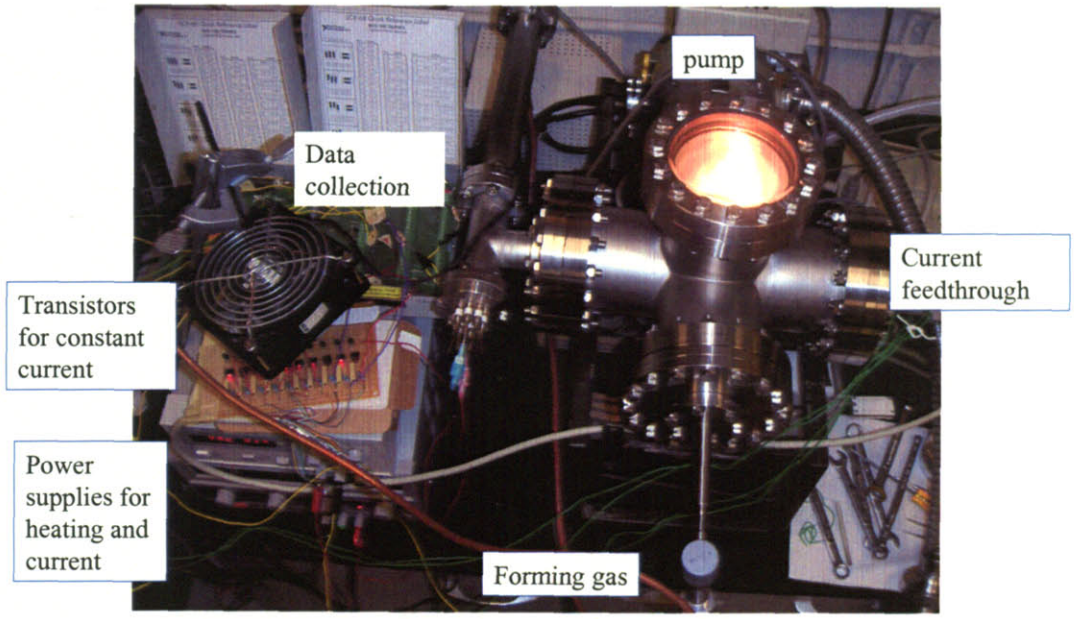

Figure b.1(b) A photograph of actual vacuum electromigration test chamber.

Singapore-MIT Alliance) connects 24-pin ceramic packages via electrical feedthroughs to the outside of the vacuum chamber (Figure b.2). For wiring inside the vacuum chamber, 1mm diameter bare copper wires surrounded with alumina tubes for isolation are used to be compatible with high vacuum and temperature.

Wires for sample testing and heating are separated. For heating, the radiation of a MR-16 24 V halogen lamp is used. The lamp is connected to an adjustable voltage source that allows the adjustment of the sample temperature by manually adjusting the lamp's voltage. Temperatures on the order of 400°C can be achieved with this setup (Figure b.2). The sample temperature is measured by a thermocouple that is attached to the ceramic package which is in good thermal contact with the interconnects.

For the electrical current supply for the test samples, another power supply is connected to eleven LM334 3 terminal transistors which supply adjustable constant current depending on the amount of the resistance connected to the transistor, as shown in figure b.3. To effectively adjust the amount of current, potentiometers, are used to regulate the resistance in each transistor. (Figure b.4) With this setup, 11 samples can be tested simultaneously only using one main power supply and adjusting the current densities for individual samples with the potentiometers.

With constant currents, voltages of individual samples are recorded then converted to resistance using a SCB-68 collector block attached to a National Instruments A/D card in a computer running a Labview program (Figure b.1(b)). The vacuum system is equipped with a gas feedthrough for flowing forming gas in order to reduce oxides on the sample's surface. The Time for the chamber to reach pressures below $1x10^{-7}$ torr is about 5 hours. After the pressure reached below $1x10^{-7}$ torr, 5% hydrogen and 95% nitrogen forming gas was flowed with 500sccm/min at $1x10^{-3}$torr

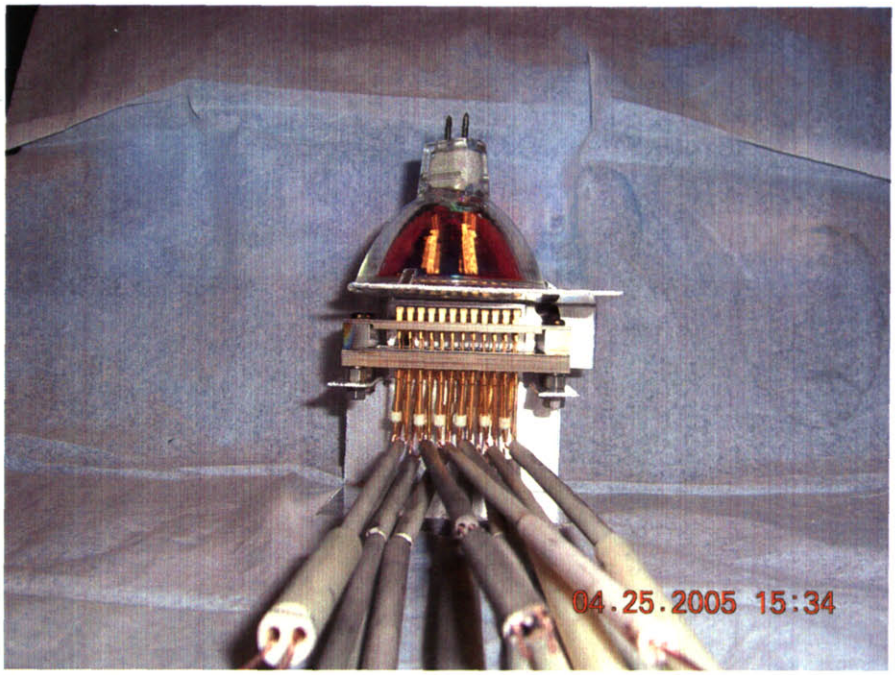

Figure b.2 A photograph of actual socket with wires, ceramic package, and halogen lamp heater.

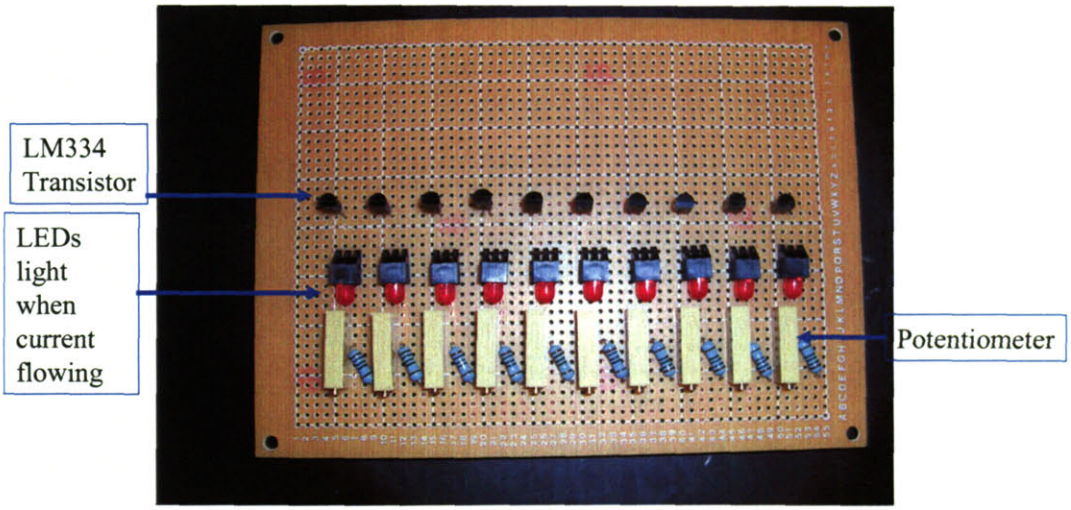

Figure b.3 Transistor regulates current by difference in resistance of the potentiometer.

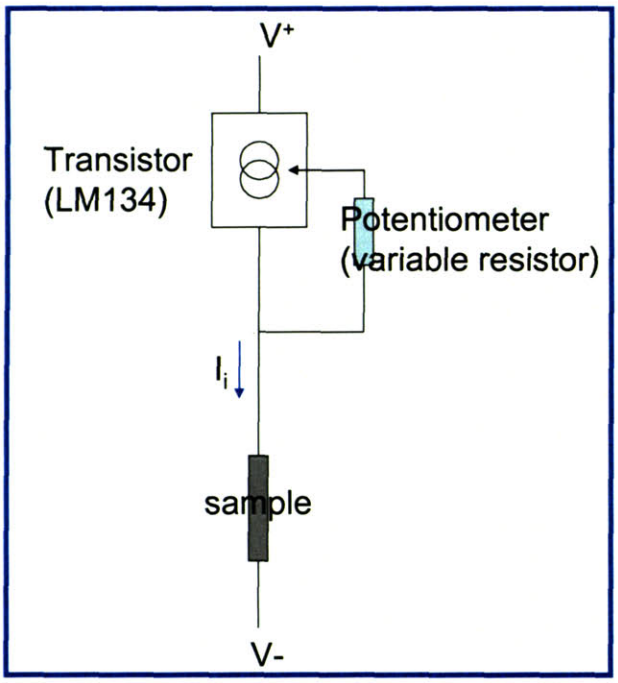

Figure b.4 It can be controlled with a accuracy with variable resistance in the configuration shown in the left.

and 250°C for 5 minutes to reduce the residual copper oxides on the top surface of the interconnect. [Y.Hu 2001] [Rodriguez 2003]. Then temperature was raised to the testing condition while the system was pumping. After about 12 hours the pressure was below 2.5×10^{-8} torr and accelerated electromigration tests were performed by applying a desired current density to the interconnects.

Reference: Appendix B

[Rodriguez 2003] Jose´ A. Rodriguez, Jae Y. Kim, Jonathan C. Hanson, Manuel Pe´rez, and Anatoly I. Frenkel, Catalysis Letters, **85**, p247 (2003)

[Y.Hu 2001] Yao Zhi Hu, Rahul Sharangpani, and Sing-Pin Tay, J. Electrochem. Soc, **148,** G669-G675 (2001)

APPENDIX C

MANUAL FOR RUNNING XSIM

The code is in a folder named "xsim" in an attached DVD with the thesis. The code requires Matlab software to run the simulation.

1. After opening a Matlab software, go to "command window" and type "cd xsim" or the name of the folder where xSim code is. Then the "current directory" will show this folder.
2. Go to file and select "open file"
3. select one of the *.m file

For single interconnect terminated with two vias.

4. select "sim_one_interconnect.m"

5. in the file "sim_one_interconnect.m", some of the fundamentals constants are in lines 9 through 20. q = fundamental charge (C), B = effective modulus (Pa), omega = atomic volume (m^3), Cl0 = lattice concentration at zero stress (m^{-3}), Cv0 = vacancy concentration at zero stress (m^{-3}), EtDa = diffusion activation energy (Joule), EtCv = vacancy activation energy (Joule), sigmac = critical stress for void nucleation (Pa), efactor = void propagation factor.
6. line 21 "lc" sets the number of cells in the interconnect, currently set to 25 cells (lc = 25)
7. line 25 sets status of the cell, set to zero, which is initial condition
8. lines 26 to 34 are user defined conditions. Da0 = diffusivity pre-factor of individual cells (m^2/s), Dac = surface diffusivity pre-factor at voided region of individual cells(m^2/s), T =temperature (K), dx=cell length (m), A=cross-sectional area (m^2), E = electric field (j (A/m^2)*ρ(Ωm))
9. lines 37 and 38 initialize atomic concentration of each cells.
10. line 45 is the time step of each integration, assign desired time steps you wish to output
11. line 46 is the number of time steps, assign desired number of time steps you wish to output
12. lines 47 and 48 output the results.
13. once user defined values are inserted, go back to "command window" and type "sim_one_interconnect" which will run the simulation
14. after the simulation, go to "Desktop" menu and check "workspace"
15. click on either "sigma" or "Ca" and you will see the spreadsheet with simulated

results of stress and concentration profiles

16. Type plot(sigma) or plot(Ca) in "command window" to see the plots

For interconnect with two segments.

1. open "sim_two_interconnect.m" file
2. lines 8 and 9 assign the number of cells for two interconnects, num_cell1, and num_cell2.
3. lines 11 to 22 are material parameters described in "sim_one_interconnect.m"
4. lines 25 to 42 are user input values for the first interconnect, definitions and parameters are described in "sim_one_interconnect.m"
5. line 41, "NETLIST" combines all interconnects into one structure. First interconnect is assigned as "i1" and cells of "i1" occupies from cell 1 of NETLIST.
6. lines 45 to 60 are user input values for the second interconnect.
7. line 59, Second interconnect is assigned as "i2" and cells of "i2" occupies from cell (num_cell1 + 2)
8. lines 64 to 84 are user input values for a junction connecting two interconnects.
9. lines 64 to 72 are assigned values for junction cell, similar to that of interconnect assignment.
10. line 75 connects a junction to the first interconnect (inter_num1). "is_blocked" means there is a block between a junction and interconnect to prevent atomic diffusion. It is marked "0" for false, so atoms are diffusing. "is_end" means junction is connected to the last cell of the interconnect, which is marked "1" for true.
11. line 76 connects a junction to the second interconnect. "is_end" is marked "0" meaning junction is connected to the first cell of the second interconnect.
12. line 83 junction cell is assigned as "j1" and occupies cell (num_cell1+1)
13. lines 89 to 92 are for simulation output, described in "sim_one_interconnect.m."