A Low Power Digitizer for Precision Carrier Band Measurements

by

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Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of

Master of Engineering in Electrical Engineering and Computer Science

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Abstract

It has been found that the amplitude of the 20kHz harmonic at the output of a particular third order $\Sigma\Delta$ analog to digital converter drifts significantly as the temperature fluctuates. In this document, both methods of ascertaining the source of this drift and ways to reduce it are discussed. First, the settling time of the circuit is explored by analyzing the design of the transmission gates used to implement the switched capacitor integrators in the $\Sigma\Delta$. Next, the effects of op amp transistor mismatch is considered via simulations which introduce small random offsets to the widths and lengths in the transistors of each op amp. Finally, a calibration scheme which can be used to eliminate the AC gain variation of the $\Sigma\Delta$ at 20kHz is analyzed, and simulation results of the circuit used to perform the calibration are portrayed.

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Keith R. Santarelli

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Chapter 1

Introduction

1.1 Motivation

In many applications today involving the use of electronic circuits, there is a need to convert analog waveforms into a digital form. In my group at the Charles Stark Draper Laboratory, we wish to digitize a signal which has a power spectrum that is depicted in Figure 1-1. The fundamental harmonic of the spectrum, denoted in the figure by f_0 = 10kHz, has amplitude that is roughly 40dB higher than the amplitudes of the higher order harmonics shown in the picture which all have roughly the same amplitude (up to about 80kHz). The information of interest in this signal is the amplitude of the second harmonic. Analog circuits can be used to extract this information, but significant error can be introduced by the DC bias drift of analog circuitry. Digital processing of the signal can avoid this problem.

Given the above information about the input spectrum to the converter, two requirements for the design of an analog to digital converter circuit become apparent:

- The second harmonic distortion of the converter must be very low to prevent distortion due to the fundamental frequency from significantly affecting the amplitude of the second harmonic.

- The noise floor of the analog to digital converter must be very low in the vicinity of $2f_0$ to reduce the error in the measurement of the second harmonic's

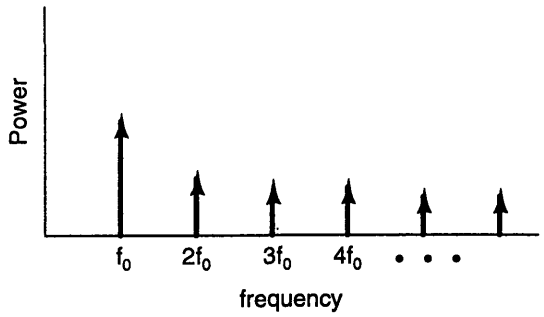

Figure 1-1: Power spectrum of an analog signal that we wish to digitize.

amplitude.

The particular type of analog to digital converter which has been chosen to digitize the given spectrum is a third order, one bit $\Sigma\Delta$ converter. The primary reasons why this type of converter was chosen over other converter architectures are that it is an easy converter to make in a CMOS process, and it is a fast converter (e.g., compared to an integrating converter). Furthermore, $\Sigma\Delta$ converters reduce the stringency on the requirements for analog anti-aliasing filters which precede the actual converter [7]. Also, the static power dissipation of these converters can be made very low without degrading the performance of a $\Sigma\Delta$ converter. The $\Sigma\Delta$ that was designed for processing the input signal spectrum of Figure 1-1 consumes only 30mW of static power.

The third order $\Sigma\Delta$ circuit that has been designed has already been fabricated. Table 1.1 summarizes the major specifications of the third order $\Sigma\Delta$ along with the results measured in the laboratory (when applicable). The nominal power supplies for the circuit are V_{CC}=5V, V_{EE}=0V, MID=2.5V. All tests were performed using a 2.0V peak-to-peak, 20kHz sine wave as an input. The resulting output spectrum of the $\Sigma\Delta$ is depicted in Figure 1-2.

Examining Table 1.1, we find that the noise specification has not been satisfied;

Characteristic	Specification	Measured Result
Clock Frequency	5.12MHz	—
Input Range	±1V Full scale about MID	—
Noise	100nV/rtHz within 20kHz±100Hz	140nV/rtHz
AC Gain Stability at 20kHz	0.1% over temperature	1.5% over temperature
Spurious Tones	< -80dBcFS at 20±4kHz	No tones in output spectrum
Second Harmonic Distortion	< -80dBcFS (after digital filtration)	-82dBcFS

Table 1.1: Major specifications of third order $\Sigma\Delta$ circuit. The temperatures at which the circuit was tested range from -40C to 85C.

however, the measured noise level should not impede the performance of the circuit significantly since the original design specification for the noise level is tighter than currently necessary.

Also, we find that the second harmonic distortion of the output spectrum meets the specified level shown in Table 1.1. Note that all tests were performed using a 20kHz sine wave input, so the second harmonic distortion is measured at 40kHz for convenience. When the input for this application is applied to the $\Sigma\Delta$, the second harmonic will lie at 20kHz as indicated previously.

While both the noise level and second harmonic distortion meet the desired specifications, the gain stability of the circuit is currently unacceptable for use with the current application. As the Table 1.1 clearly indicates, the amplitude of the 20kHz harmonic varies by more than an order of magnitude higher than the specified level as the temperature changes from -40C to 85C. The AC gain at 20kHz must be made more stable over temperature in order to make precision measurements about the 20kHz carrier band.

1.2 Document Outline

The goal of this thesis is twofold. First, after a brief introduction to the operation of $\Sigma\Delta$ analog to digital converters, we discuss tests which were performed to attempt

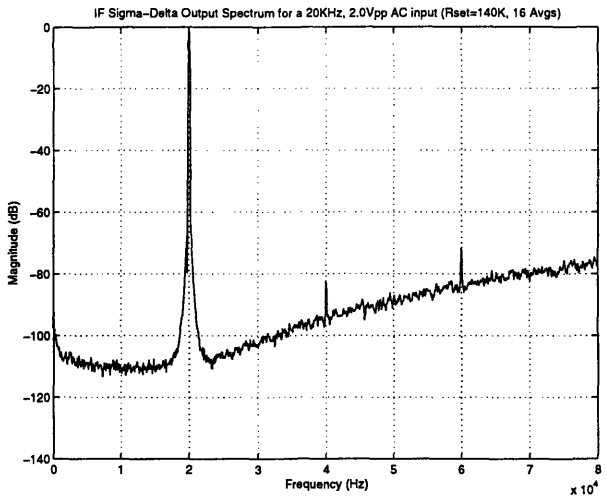

Figure 1-2: Output spectrum of $\Sigma\Delta$ circuit with a 2.0V peak-to-peak, 20kHz input. The resolution bandwidth for the noise floor is roughly 80Hz.

to discover the source of the error in the design and/or layout of the $\Sigma\Delta$ circuit that are causing the AC gain variations exhibited in the laboratory tests. Specifically, we explore issues related to the design of the transmission gates which are used in implementing the $\Sigma\Delta$, as well as issues related to mismatch errors in the widths and lengths of the transistors used to implement the op amps in the circuit. As we shall see, neither of these sets of analyses identify the source of the AC gain drift over temperature, but they do provide useful information for future $\Sigma\Delta$ designs and, in the case of the mismatched transistor widths and lengths, potentially point in the direction of the source of the AC gain drift.

After having analyzed the above issues, we then present a calibration scheme whereby the AC gain error may be reduced to within the specified tolerance. This calibration circuit is to be fabricated as a separate integrated circuit from the existing third order $\Sigma\Delta$ for purposes of test and will be integrated onto the same die as the $\Sigma\Delta$ once its performance has been verified. The basic operation of the calibration scheme is presented here, as well as the circuits used to implement this system, and HSPICE simulation results are presented to verify the theoretical performance of this calibration system.

Chapter 2

Fundamental Operation of the Sigma-Delta Analog to Digital Converter

In this chapter, the principles which govern the operation of one bit $\Sigma\Delta$ analog to digital converters is surveyed. First, we investigate the concept of noise shaping within the context of a simple first order lowpass $\Sigma\Delta$ converter, and then extend this idea to the operation of the hybrid third order lowpass/bandpass converter used in the current design. Once the system level operation of the third order converter has been explained, the current circuit-level implementation of the third order converter is discussed.

2.1 First order Lowpass $\Sigma\Delta$ Converters

The two techniques which allow a one bit $\Sigma\Delta$ converter to achieve high resolution are referred to as *oversampling* and *noise shaping*. In this section, we explain the operation of each of these two techniques in the context of a first order lowpass $\Sigma\Delta$ converter and discuss their merits.

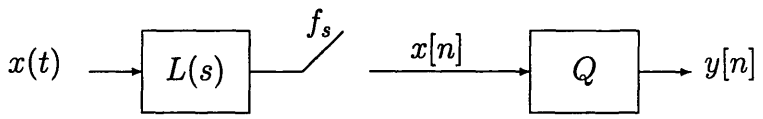

Figure 2-1: Block diagram of one bit oversampling converter.

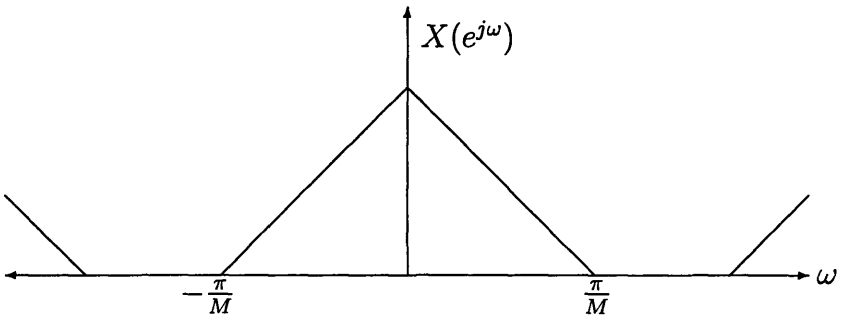

Figure 2-2: Spectrum of a band limited, sampled continuous-time waveform.

2.1.1 Oversampling

A particularly simple type of analog to digital converter which can achieve high resolution in the digital output waveform is a one bit oversampling converter. A block diagram of a one bit oversampling converter is depicted in Figure 2-1. Before sampling occurs, the analog waveform $x(t)$ is band limited by a lowpass filter $L(s)$ to have bandwidth Ω_b. The resulting signal is then sampled at a rate $f_s = 2Mf_b$ (or, equivalently $\Omega_s = 2M\Omega_b$), where M is called the *oversampling ratio*, as it is the ratio of the sampling rate Ω_s to the Nyquist rate. Thus, in the discrete-time domain, the sampled signal, $x[n]$, has a bandwidth $\omega_b = \frac{\Omega_b}{f_s} = \frac{\pi}{M}$ [10]. One possible example for the spectrum of $x[n]$ is depicted in Figure 2-2.

Once the signal has been band limited and sampled, it passes through a quantizer Q which outputs a value of $\frac{\Delta}{2}$ when $x[n] \geq 0$, and a value of $-\frac{\Delta}{2}$ when $x[n] < 0$, where Δ is a value determined by the supply rails of the circuit used to implement the quantizer. While it is easy to characterize the spectrum of $x[n]$ in terms of the spectrum of the continuous-time waveform $x(t)$, it is not very easy, in general,

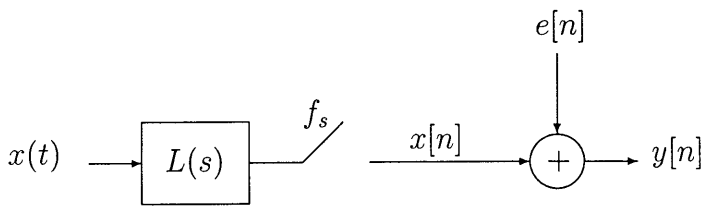

Figure 2-3: Block diagram of linearized one bit oversampling converter.

to determine the spectrum of $y[n]$, the quantized version of the sampled signal, as quantization is a nonlinear operation. However, as is described in [10], it is often the case that one can approximate the quantizer as an additive noise source that is uncorrelated with the input $x[n]$. There is no theoretical basis for this result; it is only based on empirical evidence which shows that the error sequence $e[n] = y[n] - x[n]$ (commonly referred to as *quantization noise*) often has a small correlation with $x[n]$. Furthermore, it is a fair approximation to assume that the probability density of $e[n]$ is uniform between $-\frac{\Delta}{2}$ and $\frac{\Delta}{2}$ and, also, that $e[n]$ is wide-sense stationary white noise (i.e., $e[n]$ has samples which are uncorrelated with one another and whose variance is independent of time) [10, 2, 6]. A block diagram of a one bit oversampling converter which includes this linearized model of the quantizer is depicted in Figure 2-3.

Using these approximations, we find that the power spectral density of $e[n]$ is equal to σ_e^2, the variance of $e[n]$, over the range $[-\pi,\pi]$. Since the approximate system is linear and since $e[n]$ and $x[n]$ are assumed to be uncorrelated, the power spectrum of $y[n]$, $S_{yy}(e^{j\omega})$, is equal to the sum of the power spectrums of $x[n]$ and $e[n]$.

In order to measure the performance of the oversampling converter, we define a metric commonly referred to as the signal to quantization noise ratio (abbr. SQNR), defined as

$$SQNR = \frac{P_x}{P_e} \tag{2.1}$$

where P_x is the energy in $y[n]$ due to the input $x[n]$, and P_e is the expected energy[1] in $y[n]$ due to the portion of $e[n]$ that lies within the range $[-\frac{\pi}{M}, \frac{\pi}{M}]$. Note that

[1] $e[n]$ is a random process, so the energy in $e[n]$ is also random. We, therefore, look at the *expected* energy to obtain a measure of the system performance.

the portion of $e[n]$ which lies outside of this bandwidth is irrelevant since it can be removed with a lowpass filter without affecting the portion of $y[n]$ due to the input $x[n]$ [10]. A typical sketch of the power spectrum of $y[n]$ on $[-\frac{\pi}{M},\frac{\pi}{M}]$ (which has been broken down into the components due to the $x[n]$ of Figure 2-2 and $e[n]$) is shown in Figure 2-4.

It should be clear that P_x is independent of the sampling frequency. In the discrete-time domain, P_x is given by

$$P_x = \frac{1}{2\pi}\int_{-\frac{\pi}{M}}^{\frac{\pi}{M}} S_{xx}(e^{j\omega})d\omega. \tag{2.2}$$

By the sampling theorem, we have that $S_{xx}(e^{j\omega}) = f_s S_{xx}(j\Omega)|_{\Omega=\omega f_s}$ for ω on the interval $[-\pi,\pi]$ where $S_{xx}(j\Omega)$ is the power spectral density of $x(t)$. Thus,

$$P_x = \frac{1}{2\pi}\int_{-\frac{\pi}{M}}^{\frac{\pi}{M}} f_s S_{xx}(j\Omega)|_{\Omega=\omega f_s}d\omega = \frac{1}{2\pi}\int_{-\frac{\pi f_s}{M}}^{\frac{\pi f_s}{M}} S_{xx}(j\Omega)d\Omega = \frac{1}{2\pi}\int_{-\Omega_b}^{\Omega_b} S_{xx}(j\Omega)d\Omega. \tag{2.3}$$

Because the power spectrum of $e[n]$ is constant, $P_e = \frac{1}{2\pi}(\frac{2\pi}{M})\sigma_e^2 = \frac{1}{M}\sigma_e^2$. Thus, the SQNR=$\frac{P_x}{\sigma_e^2}M$. To see how the oversampling ratio M relates to the resolution of this one bit converter, consider a standard multi bit converter with B bits of resolution or, equivalently, 2^B quantization levels which are evenly distributed between two values $\pm X_m$. It can be shown that the variance σ_e^2 is given by $\frac{X_m^2}{12(2^{2B})}$ [10]. Thus, the SQNR for a standard multi bit converter is given by $\frac{12P_x(2^{2B})}{X_m^2}$. Comparing this to the SQNR of an oversampled converter, if we let $M = 2^{2B}$ and keep all other parameters fixed, we see that every factor of 4 increase in M is equivalent to adding 1 extra bit to a multistage quantizer. Thus, every factor of 4 increase in M increases the output resolution of an oversampling converter by 1 bit [10, 2, 6].

2.1.2 Noise Shaping

While oversampling is a simple method of increasing the resolution of the digital output spectrum, one typically needs to sample *very* quickly to ensure that M is large enough for high-resolution applications. If $X_m = 1$, then, in order for a one bit

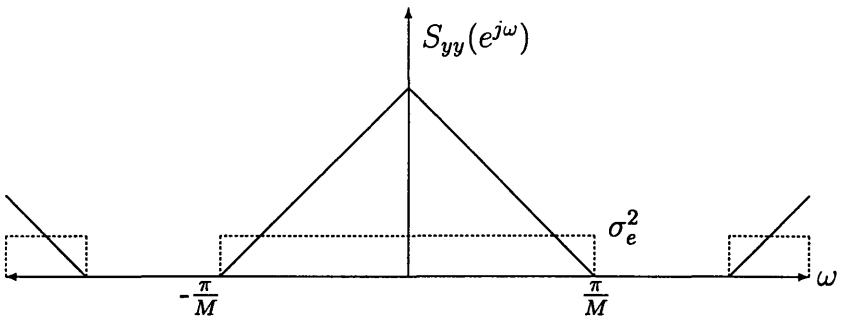

Figure 2-4: Power spectral density of the sampled, quantized input signal assuming an additive white noise model for $e[n]$.

oversampling converter to achieve the same resolution as a 10 bit multi bit converter, we must set M equal to 1,048,576. For a low frequency signal with a bandwidth of 1kHz, we require circuitry that can sample at a rate roughly equal to 2GHz! Having to sample at such a high rate will greatly increase both the complexity and cost of our system.

One way of helping to increase the resolution of a one bit converter without using extremely large values of M is to use a modification to the oversampling method known as *noise shaping.* The basic idea behind noise shaping is to design the system so that the noise seen at the output due to quantization noise is primarily pushed out of the frequency span of the input signal. If the input signal is baseband, then we wish to push the quantization noise out of the low frequency region. The system in Figure 2-5 carries out this task. This architecture, known as a first order, lowpass $\Sigma\Delta$ architecture, increases the SQNR by highpass filtering $e[n]$ to reduce the in-band quantization noise. The block denoted "DAC" the figure represents a digital to analog converter. In the case of a one bit converter, this block simply translates the digital 1 or 0 at the output of the quantizer into the corresponding analog voltage used to represent the corresponding state. Since we have assumed that the output of the quantizer is equal to $\pm\frac{\Delta}{2}$ where $\frac{\Delta}{2}$ represents the magnitude of the power supply rails, and since the output of the digital to analog converter will, also, be one of these two levels, the "DAC" block may simply be replaced by a gain of 1 [10, 2, 6].

If we replace the quantizer in Figure 2-5 with an additive noise source, and if we

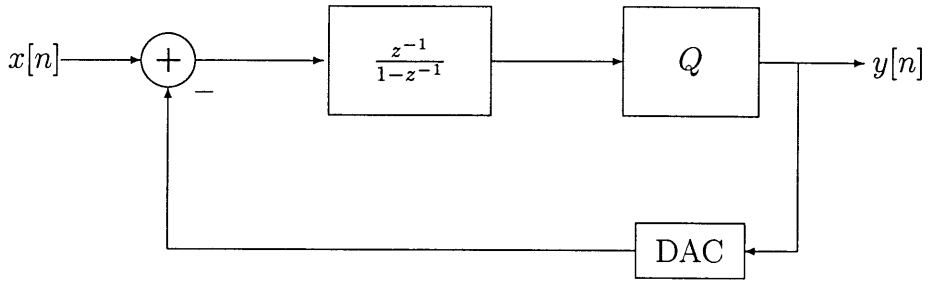

Figure 2-5: Block diagram for a lowpass, one bit quantizer $\Sigma\Delta$ analog to digital converter.

define $H_x(z)$ to be the transfer function from $x[n]$ to $y[n]$ (commonly referred to as the *signal transfer function*) and $H_e(z)$ to be the transfer function from $e[n]$ to $y[n]$ (commonly referred to as the *noise transfer function*), then it can be shown that

$$H_x(z) = z^{-1} \tag{2.4}$$

$$H_e(z) = (1 - z^{-1}) \tag{2.5}$$

The portion of the power spectrum of $y[n]$ due to the source $x[n]$ (denoted by $S_{yx}(e^{j\omega})$) and the portion due to $e[n]$ (denoted by $S_{ye}(e^{j\omega})$) are given by

$$S_{yx}(e^{j\omega}) = S_{xx}(e^{j\omega})|H_x(e^{j\omega})|^2 = S_{xx}(e^{j\omega}) \tag{2.6}$$

$$S_{ye}(e^{j\omega}) = S_{ee}(e^{j\omega})|H_e(e^{j\omega})|^2 = 4\sin^2(\frac{\omega}{2})S_{ee}(e^{j\omega}) \tag{2.7}$$

Assuming that $\Omega_b \ll \pi$, then we can use the approximation that $\sin x \approx x$ to calculate P_e:

$$P_e = \frac{\sigma_e^2}{2\pi}\int_{-\omega_b}^{\omega_b} 4\sin^2\left(\frac{\omega}{2}\right)d\omega \approx \frac{\sigma_e^2}{2\pi}\int_{-\omega_b}^{\omega_b}\omega^2 d\omega = \frac{\sigma_e^2}{3\pi}\Omega_b^3 = \frac{\sigma_e^2\pi^2}{3M^3} \tag{2.8}$$

Because P_x remains unchanged, the SQNR is now given by $\frac{3P_x}{\pi^2\sigma_e^2}M^3$. If we once again let $M = 2^{2B}$, then we see that for each factor of 4 increase in M, we increase the SQNR by 3 bits instead of only 1. Thus, in order to achieve roughly the same

SQNR as a 10 bit converter for a low frequency signal with bandwidth of 1kHz, we only need to use a value of M on the order of 100, thus reducing the sampling rate to 200kHz instead of 2GHz. This immensely reduces both the complexity and cost of our system [10, 2, 6].

2.2 A Third Order Hybrid $\Sigma\Delta$ Topology

2.2.1 Operation Fundamentals

While the above first order architecture works well for baseband signals, it will not work well for the current application since the signal of interest is centered at 20kHz. In order to be able to use a first order $\Sigma\Delta$ converter effectively in this scenario, the oversampling ratio still needs to be rather high in order to push enough of the quantization noise beyond 20kHz so that the measurement of the 20kHz harmonic is accurate. This requirement is demonstrated in Figure 2-6 which depicts the magnitude of the frequency response of the noise transfer function governed by Equation 2.5 at a sampling rate of 5.12MHz. If we consider our example from the last section where we were interested in converting a baseband signal with a bandwidth of 1kHz, we see that a rough upper bound on the magnitude of the noise transfer function in this region is -60dB. If, instead, we consider converting a 1kHz region about 20kHz, we see that the magnitude of the noise transfer function in this region is roughly -32dB. Thus, the SNRs of each of region differ by at *least* 28dB! Indeed, the difference is probably greater since the magnitude of the noise transfer function is much smaller than -60dB for the entire frequency range between DC and 1kHz. If we increase the sampling rate, then we essentially will "push" the 20kHz region closer to the zero notch of the noise transfer function. But we see, based upon Figure 2-6 that we need to increase the sampling rate by at least a factor of 20 to get the quantization noise level to lie below -60dB for the 1kHz region about 20kHz. Indeed, in order to achieve the same SQNR as the 1kHz baseband signal sampled at 5.12MHz, we would need to increase the sampling rate by much more than a factor of 20 to get the region

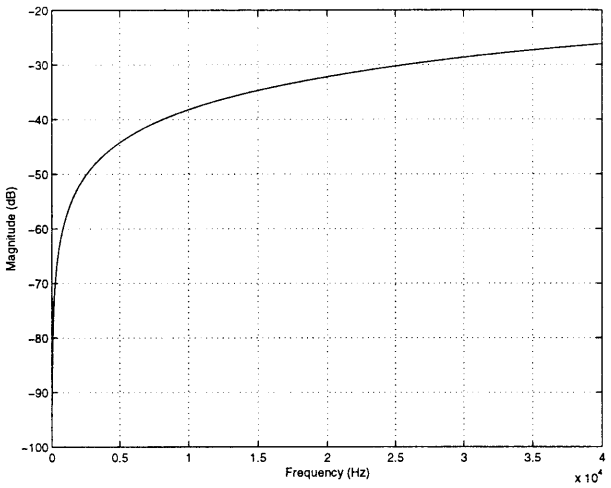

Figure 2-6: Magnitude of $H_e(z)$ of Equation 2.5.

about 20kHz as close to the zero notch as possible.

From the above, we see that noise shaping is most efficient when the signal of interest is centered at the frequency of the zero notch. Another way to reduce the in-band quantization noise energy without significantly increasing the oversampling ratio is to obtain a noise transfer function with a zero notch that is located at the center of the frequency span of interest. A different architecture which achieves this objective, the one that has already been fabricated for the current application, is a third order *hybrid* design. A block diagram of a basic third order topology is shown in Figure 2-7, where a_i, b_i, and c_i are constants. While the first order lowpass design has only one zero at DC in the noise transfer function, the third order bandpass design adds two complex-conjugate zeros at 20kHz (assuming a sampling frequency of 5.12MHz) in addition to the one zero at DC. Thus, since there are two zeroes immediately within the bandwidth of the carrier signal (20kHz$\pm$100Hz), the quantization noise can be greatly suppressed without requiring an extremely large oversampling ratio [2].

If we replace the quantizer in Figure 2-7 with the linear noise model and the

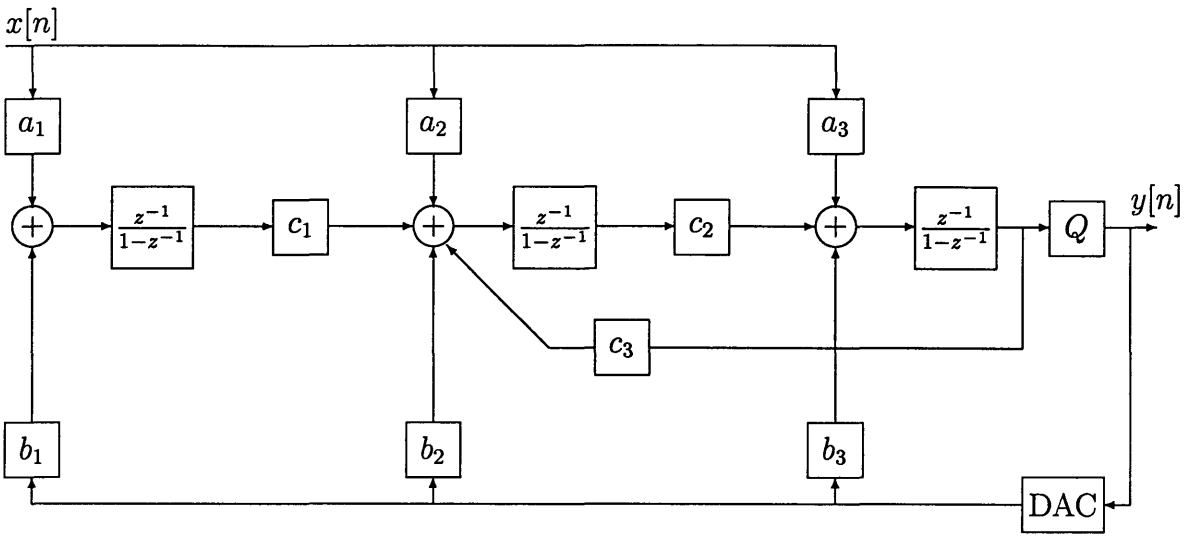

Figure 2-7: Block diagram of third order $\Sigma\Delta$ circuit.

"DAC" block with a gain of 1, we can calculate $H_x(z)$ to be

$$\frac{(a_1c_1c_2 - a_2c_2 + a_3)z^{-3} + (a_2c_2 - 2a_3)z^{-2} + a_3z^{-1}}{(-1 - b_3 + (b_2 + c_3)c_2 - b_1c_1c_2)z^{-3} + (3 - c_2(c_3 + b_2) + 2b_3)z^{-2} + (-3 - b_3)z^{-1} + 1} \tag{2.9}$$

and $H_e(z)$ to be

$$\frac{(1 - z^{-1})(1 - 2z^{-1} + (1 - c_2c_3)z^{-2})}{(-1 - b_3 + (b_2 + c_3)c_2 - b_1c_1c_2)z^{-3} + (3 - c_2(c_3 + b_2) + 2b_3)z^{-2} + (-3 - b_3)z^{-1} + 1}. \tag{2.10}$$

For the values of the constants a_i, b_i, and c_i used in this design, 2.9 and 2.10 reduce to

$$H_x(z) = \frac{0.2161z^{-3} - 0.5107z^{-2} + 0.3125z^{-1}}{-0.7844z^{-3} + 2.4898z^{-2} - 2.6875z^{-1} + 1} \tag{2.11}$$

$$H_e(z) = \frac{(1 - z^{-1})(1 - 2z^{-1} + 1.0006z^{-2})}{-0.7844z^{-3} + 2.4898z^{-2} - 2.6875z^{-1} + 1} \tag{2.12}$$

To illustrate the reduction in required oversampling ratio of this hybrid converter as compared to a simple lowpass converter, consider rewriting the noise transfer func-

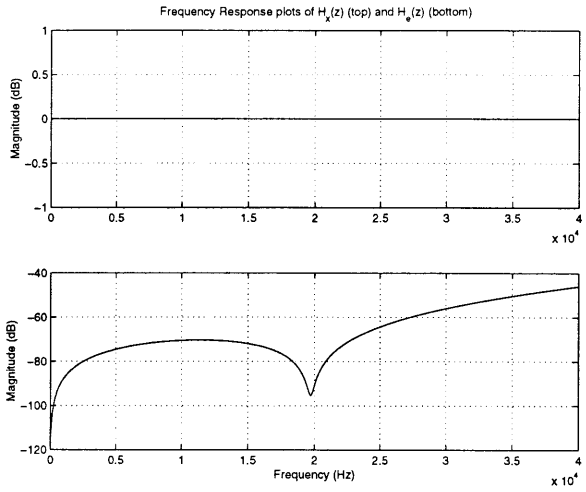

Figure 2-8: Frequency response of signal and noise transfer functions from DC to 40kHz

tion in the following form:

$$H_e(z) = H_1(z)(z - e^{j\omega_0}) \tag{2.13}$$

where ω_0 is the frequency of the notch, and $H_1(z)$ represents all other terms. Within a small bandwidth of the notch frequency, we can approximate the noise transfer function as

$$H_e(z) \approx H_1(e^{j\omega_0})(z - e^{j\omega_0}.) \tag{2.14}$$

If we consider computing the quantization noise energy in a small bandwidth $\Delta\Omega$ about the continuous-time carrier frequency, we may write the equivalent discrete-time bandwidth $\Delta\omega$ as some constant α times the discrete-time signal bandwidth, $\omega_b = \frac{\pi}{M}$. Thus, the in-band quantization noise energy is given by

$$\frac{1}{2\pi}\int_{\omega_0-\Delta\omega}^{\omega_0+\Delta\omega} |H_e(e^{j\omega})|^2\sigma_e^2 d\omega \approx \frac{\sigma_e^2}{2\pi}|H_1(e^{j\omega_0})|^2 \int_{\omega_0-\Delta\omega}^{\omega_0+\Delta\omega} 4\sin\left(\frac{\omega-\omega_0}{2}\right)^2 d\omega. \tag{2.15}$$

If we make the substitution $\omega' = \omega - \omega_0$ and, again, the approximation that

$\sin x \approx x$ for small x, then 2.15 reduces to

$$\frac{\sigma_e^2}{2\pi}|H_1(e^{j\omega_0})|^2 \int_{-\Delta\omega}^{\Delta\omega} (\omega')^2 d\omega' = \alpha^3 |H_1(e^{j\omega_0})|^2 \frac{\sigma_e^2 \pi^2}{3M^3} \tag{2.16}$$

Ignoring the additional constants, we see that Equation 2.16 has the same functional form as Equation 2.8. Therefore, if we once again let $M = 2^{2B}$, then for each power of 4 increase in M, we achieve three extra bits of resolution. Thus, a third order $\Sigma\Delta$ converter can achieve similar resolution in a carrier band as a lowpass converter can achieve at baseband for similar values of M. Indeed, one may even be able to lower the value of M for a given quantization noise energy specification as the values of α and $|H_1(e^{j\omega_0})|$ are typically quite small (0.05 and 0.07, respectively, for the current design).

2.2.2 Noise Transfer Function Non-idealities

The pole zero diagrams of both the signal and noise transfer function magnitudes are depicted in Figures 2-9 and 2-10 respectively. Note that the notch in the noise transfer function frequency response due to the complex conjugate zeroes does not appear to drop to 0 (or, in the case of this plot -∞ dB), nor does the notch occur exactly at 20kHz. Two reasons account for these facts. First, if we analyze the structure of the quadratic in the numerator of Equation 2.10, we see that the complex conjugate zeroes will occur at $1 \pm \sqrt{c_2 c_3}$. Thus, the only value of the product $c_2 c_3$ which will result in complex frequencies on the unit circle is $c_2 c_3 = 0$. For $c_2 c_3 < 0$, the zeroes will occur in complex conjugate pairs with real part equal to 1, while with $c_2 c_3 > 0$, the zeroes will lie on the real axis. In our case, the zeroes lie at roughly $1 \pm j0.0245$ which lie extremely close to the unit circle (0.0003 units away). Thus, even though the zeroes do not lie exactly on the unit circle and, consequently, cannot fully attenuate any frequency along the unit circle, they will create a very notch-like structure in the frequency response because of their close proximity. Why do we not simply change the structure of the system to be able to achieve zeroes on the unit circle? To achieve this, we would require the quadratic in the numerator of 2.10 to

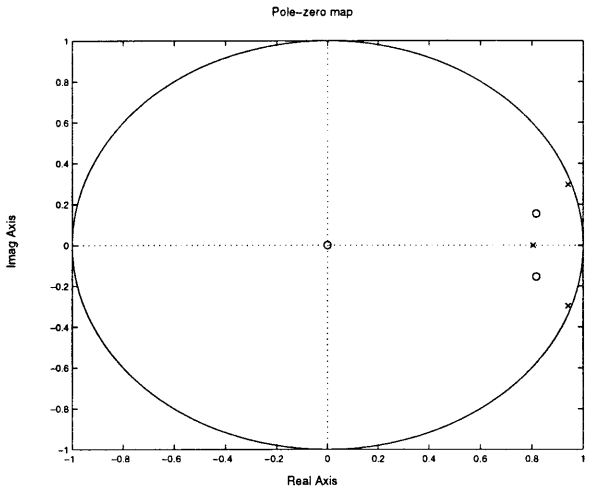

Figure 2-9: Pole zero diagram of signal transfer function. Coefficients are quantized to the ratios determined by the capacitor values used in the current design.

be of the form $1 - (2 + c_2c_3)z^{-1} + z^{-2}$. While the analysis will not be carried out here, it can be shown that, to achieve such a quadratic, one of either the second or third accumulators depicted in Figure 2-7 must be *delayless*; that is, one of the integrators must have a transfer function of the form $\frac{1}{1-z^{-1}}$. As will become apparent when the circuit topology of the current third order $\Sigma\Delta$ is discussed, using delayless accumulators adds the potential problem of increased circuit noise.

The reason as to why the notch does not occur exactly at 20kHz is primarily due to coefficient quantization. In theory, we can choose values of c_2 and c_3 with infinite precision that will create a notch arbitrarily close to 20kHz, but, in practice, this is impossible. Each of the a_i, b_i, and c_i depicted in Figure 2-7 are implemented as the ratio of two capacitors. Each individual capacitor is composed of a series or parallel combination of smaller "unit" capacitors. The size of the unit capacitor depends upon the process used to lay out the integrated circuit, but, in this design, a value of 100fF was assumed. The maximum capacitor size used in this design is 5pF, so we see that, for this maximum size capacitor, if we wish to slightly increase or decrease the capacitance, we must do so by at least $\pm 2\%$. For smaller size capacitors, the percentage quantization is larger. Thus, the ratios of the capacitor sizes are heavily quantized, so, as is illustrated in Figure 2-8, we cannot achieve a noise transfer

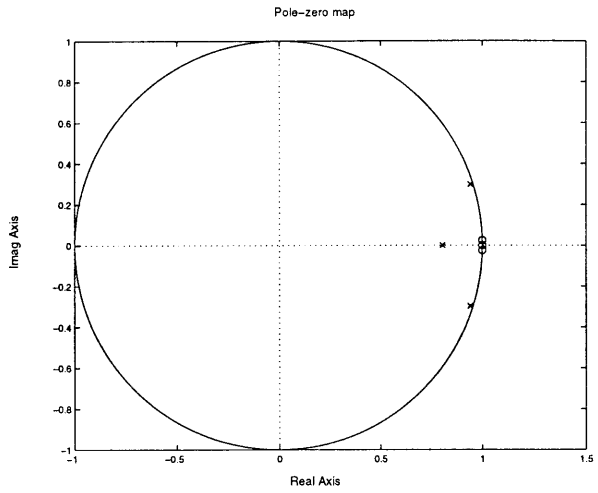

Figure 2-10: Pole zero diagram of noise transfer function. Coefficients are quantized to the ratios determined by the capacitor values used in the current design.

function zero arbitrarily close to 20kHz.

Another reason why the notch due to the complex conjugate zeroes does not occur exactly at 20kHz is due to mismatch in capacitor values. No integrated circuit process is perfect, so when a capacitor is laid out, imperfections in the layout process as well as stray capacitance associated with fringing effects will alter the actual capacitance from the desired value. Consequently, the capacitor ratios will be altered by this phenomenon, as well. Ergo, even if we were able to layout capacitors with infinite precision, the mismatch would perturb the capacitor ratios and, subsequently, the notch frequency.

Even though the designed noise transfer function characteristics are not perfect, these imperfections are small enough that they should not affect the performance of the circuit. All analysis up to this point has assumed that the only source of noise in a $\Sigma\Delta$ converter is quantization noise. In reality, the individual circuit components add noise to the output spectrum of the $\Sigma\Delta$, as well. If the $\Sigma\Delta$ is well designed, then, in the frequency region of interest, the circuit noise should dominate the quantization noise. In the current design, the noise due to the circuit lies at a level of about -140dBcFS while the quantization noise is attenuated by roughly 180dB within 100Hz of either side of the carrier frequency. Thus, the signal to noise ratio (abbr. SNR),

defined as the signal power with a given bandwidth to the *total* noise power within the same bandwidth, will be dominated by the circuit noise, so small imperfections in the quantization noise transfer function are insignificant in the end. The reader may ask why we go to such pain-staking efforts to place a notch at 20kHz if, in the end, the system performance is dominated by another noise source. If we do *not* attempt to place a notch in the noise transfer function at 20kHz, then the quantization noise will dominate (typically by at least an order of magnitude higher than the circuit noise) which is obviously undesirable. The other option discussed at the beginning of this section is to build faster circuits that can sample at a much higher rate, but this is a much more difficult and costly task. Note, also, that the $\Sigma\Delta$ power consumption is minimized when the circuit noise dominates the quantization noise.

2.3 Third Order $\Sigma\Delta$ Circuit Topology

In this section, we discuss the circuits which implement the $\Sigma\Delta$ converter presented in the previous section. Most of the circuit is composed of three switched-capacitor integrators, so a large part of this section addresses the configuration of these switched-capacitor integrators. In addition to this discussion, the circuit implementation of the quantizer and the digital to analog converter are also briefly mentioned.

2.3.1 Switched-Capacitor Op Amp Configuration

Due to the dynamics of the device which produces the input signal, the input to the $\Sigma\Delta$ converter is fully differential; that is, the input to the circuit is a pair of inputs whose AC components[2] have equal magnitude but are 180° out of phase. Rather than convert this differential signal into a single-ended signal and perform the remainder of the processing with conventional single-ended op amps, a class of op amps known as fully differential op amps is used. These op amps differ from single-ended op amps

[2]Both inputs have a DC component of zero with respect to the virtual ground of the op amp.

in that their output is read as a differential voltage between two individual outputs. Also, because both of the traditional op amp input terminals must be used to perform feedback from one of the outputs to one of the inputs, a third input is added to the op amp which is used to control the common mode voltage of the two outputs. For a complete discussion of the structure and operation of fully differential op amps, please refer to Chapter 6 of [7].

Some advantages are gained in using a fully differential structure that are unobtainable with single-ended op amps. First, so long as the differential output gain is stable (with respect to process, temperature, etc.), then the common mode output voltage can vary significantly without degrading performance as the output of a fully differential op amp is independent of the common mode voltage within the linear range of the amplifier (adding a DC voltage to each output does not affect the difference between the two outputs). Furthermore, any common mode offset voltage at the output of one stage will be cancelled by the next stage due to the high common mode rejection ratio of each of the amplifiers and of the quantizer.

The schematic of the fully differential switched-capacitor circuit which implements the first integrator in the converter is depicted in Figure 2-11. The op amp used in the figure is a fully differential operational transconductance amplifier (abbr. OTA) with a programmable bias current that is set via an external resistor. The pin labeled "MID" in the diagram is used to set the common mode output voltage to approximately 2.5V (the value of MID). This voltage is considered the AC "ground" of the circuit as it lies in the middle of the dynamic range (0V to 5V). Thus, all voltages are referred to MID instead of 0V. The pins labeled IN+ and IN- represent the two inputs to the $\Sigma\Delta$, while the pins F+ and F- represent the feedback voltages produced by the DAC.

Because we are referencing all voltages to MID, it will be implicitly assumed that all voltages to which we henceforth refer will have a DC component of 2.5V. If we define $v_i[n]$ as IN+ – IN-, $f[n]$ as F+ – F-, and $v_o[n]$ as OUT+ – OUT-, then, using the principle of superposition , and assuming that the output is sampled on clock phase ϕ_1, we can derive the z-domain output $V_0(z)$ for an op amp with infinite gain

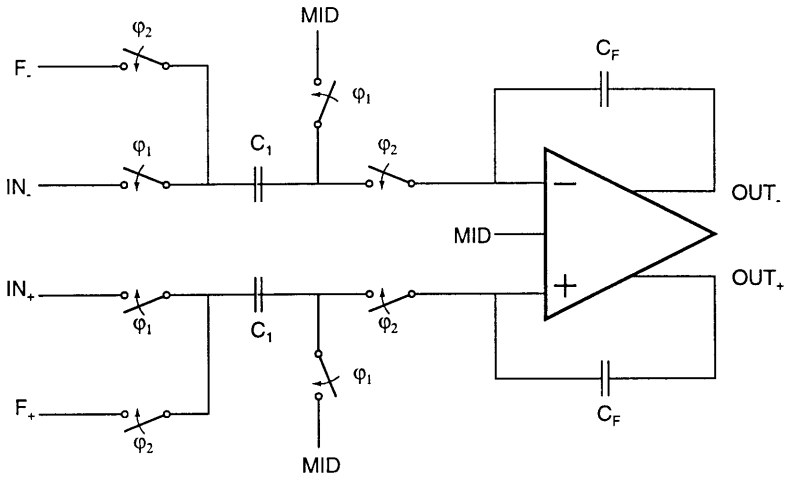

Figure 2-11: Fully differential switched-capacitor integrator architecture used in the currently fabricated third order $\Sigma\Delta$.

and bandwidth as [7]

$$V_o(z) = \frac{\frac{C_1}{C_F}z^{-1}}{1-z^{-1}}(V_i(z) - F(z)). \tag{2.17}$$

Referring to the block diagram of Figure 2-7, we see that when this integrator is used in the front end, it implements both integration and the summation of the input and feedback state with $a_1 = -b_1 = \frac{C1}{CF}$.

An alternative implementation for a switched capacitor integrator (drawn as single-ended for convenience) is depicted in Figure 2-12. In this case, the z-domain representation of OUT can be written as

$$V_o(z) = \frac{\frac{C_1}{C_F}z^{-1}}{1-z^{-1}}(V_i(z) + F(z)) \tag{2.18}$$

Note the sign inversion in 2.18 for the input $F(z)$ as compared to Equation 2.17. This sign inversion can be removed by inverting the sense of the feedback (i.e., by interchanging F- and F+). Thus, in terms of their ideal transfer functions, each of these configurations can be made identical by setting $C_2 = C_1$. Yet, each configuration has distinct advantages over the other.

The configuration of Figure 2-11 was chosen over that of Figure 2-12 primarily

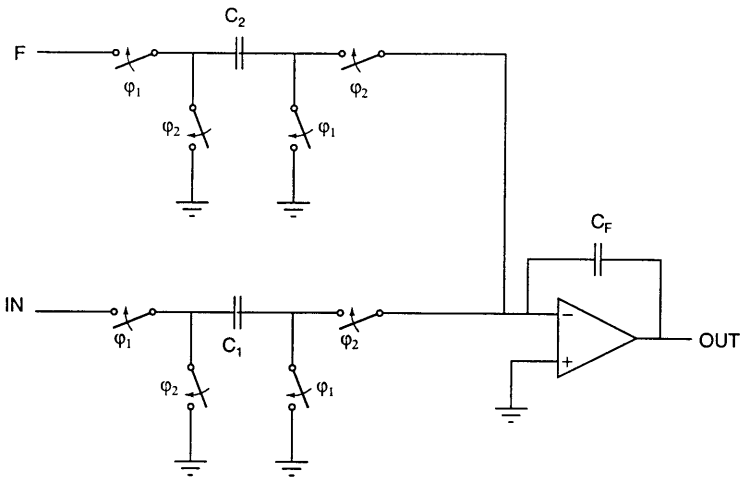

Figure 2-12: Alternative switched-capacitor integrator architecture.

because 2-11 halves the amount of noise sampled from the input and the DAC power supplies. The total thermal noise energy which a capacitor can sample is given by kT/C where k is Boltzmann's constant, T is the absolute temperature, and C is the capacitance [7]. Thus, by employing two sampling capacitors instead of one, we increase the total sampled thermal noise. Another advantage of Figure 2-11 over 2-12 lies in the issue of capacitor mismatch. The implementation in Figure 2-12 cannot ensure that a_1 can exactly equal $-b_1$ as any capacitor mismatch thwarts the coefficient values as discussed previously. Thus, perfect subtraction of $f[n]$ from $v_{in}[n]$ is impossible with the structure of Figure 2-12.

The major advantage of the configuration is Figure 2-12 over that of 2-11 lies in an issue referred to as data dependency. Examining the structure of Figure 2-11 during phase ϕ_2, we see that the amount of charge supplied by the DAC reference supplies is a function of the sampled input voltage. Thus, the loading on the supplies is also a function of the input voltage. This signal-dependent loading has been shown to be a major source of quantization noise aliasing in systems with poor DAC voltage supplies. The DAC supplies of the circuit in Figure 2-12 supply an amount of charge that is independent of the sampled input voltage and, therefore, mitigate this effect [3].

Another potential advantage of the circuit in Figure 2-12 is that, if we properly adjust the switch phases, it may be used to implement a delayless integrator [7]. As mentioned in the previous section, a delayless integrator must be used in either the second or third integrator in the chain to be able to place zeroes on the unit circle; however, we see that this sacrifices the noise performance of the circuit, so we allow the zeroes to travel slightly off the unit circle to allow for a decrease in noise energy.

2.3.2 Quantizer and Digital to Analog Converter

A diagram depicting the quantizer and digital to analog converter is depicted in Figure 2-13. The quantizer in Figure 2-7 is implemented via a comparator. The DAC is implemented via four voltage controlled switches and two stable power supplies: NREF, which is simply 0V, and PREF, which is a 4.25V source derived from a bandgap reference. If we denote the logical output of the quantizer as Q, then we see that, when Q is high, F+ is connected to PREF while F- is connected to NREF. On the other hand, when Q is low, we see that F+ is connected to NREF while F- is connected to PREF. If we view PREF as a logic 1 and NREF as a logic 0, then we see that F+ is logically equivalent to Q while F- is logically equivalent to $\bar{Q}$. Choosing the logic levels as such ensures that we provide the inputs to the integrators with negative feedback.

Note that we choose to use a separate bandgap reference voltage to implement the feedback instead of using the +5V power supply. We do this simply because the power supply voltage is derived from a battery, so it is very susceptible to fluctuation over both time and temperature, whereas the 4.25V bandgap reference eliminates both of these dependencies to first order [7].

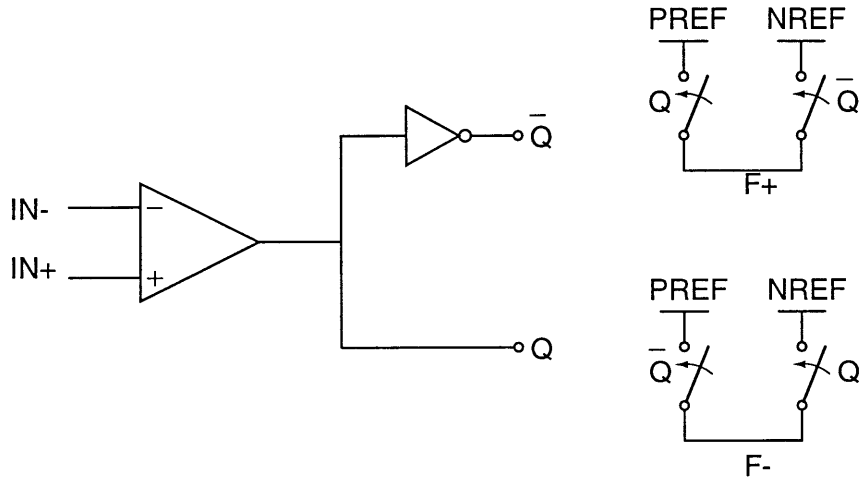

Figure 2-13: Circuit implementation of quantizer and DAC.

Chapter 3

Settling Time Issues: Switches

In the previous chapter, the ideal behavior of a third order $\Sigma\Delta$ was outlined. In this chapter, we explore one of the potential reasons as to why the gain of the 20kHz harmonic fluctuates over temperature: the settling time of the capacitor voltages. In a system with ideal voltage sources, switches, and op amps, the voltage across each capacitor changes instantaneously when a voltage is applied across its terminals; however, due to finite switch resistance, finite bandwidth and slew rate of op amps, and the finite series resistance of each voltage source, the voltage across each capacitor changes continuously and requires time to settle to the applied voltage. As we will see, if a poorly designed switch is used to implement a switched capacitor integrator, the output may require a much longer time to settle than is permitted by the clock frequency. Furthermore, the settling time may become very temperature sensitive, which can cause variation in the amplitude of the 20kHz harmonic on the order of 1%.

Unfortunately, at the time that this issue was being investigated, the wrong switches were being used to carry out simulations. When simulations were run using the switches that were actually laid out in the existing circuit, they indicated that settling time should not be an issue. However, the results that were discovered are of general use in designing switches for any switched-capacitor circuit and are presented here for general knowledge.

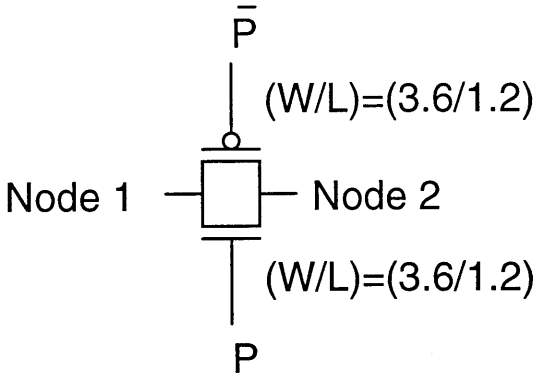

Figure 3-1: Schematic of bidirectional transmission gate. The on/off state of the switch is controlled by P and $\bar{P}$.

3.1 Switch Structure: Simple Transmission Gates

A schematic of the simple transmission gate which was originally assumed to have been laid out in the current third order $\Sigma\Delta$ is depicted in Figure 3-1. When P is low, both transistors are in cutoff and the switch is open. When P is high, the PMOS and NMOS devices begin to conduct. Unless the voltage driving one side of the switch is close to either the positive or negative rail, both devices enter conduction; however, if the driving voltage is higher than one NMOS threshold voltage away from the positive supply, the NMOS device enters subthreshold while the PMOS device conducts in strong inversion. Likewise, if the driving voltage is less than one PMOS threshold voltage away from the negative supply, the PMOS device enters subthreshold while the NMOS device conducts in strong inversion [7].

Simple transmission gates are highly nonlinear devices; however, once all large-signal transients have passed and the voltage difference between Node 1 and Node 2 in Figure 3-1 is small (usually on the order of 0.2V or less), each of the transistors in the transmission gate enters the triode region of operation (assuming that the driving voltage is not too high or too low to put either the PMOS or the NMOS device in subthreshold). In this mode of operation, each transistor approximately acts as a

resistor with resistance given by

$$R = \frac{1}{\frac{W}{L}\mu_n C_{ox}(V_{GS} - V_{Tn})} \tag{3.1}$$

for an NMOS device and

$$R = \frac{1}{\frac{W}{L}\mu_p C_{ox}(V_{SG} + V_{Tp})} \tag{3.2}$$

for a PMOS device [7].

Of all the parameters involved in the above expressions for resistance, the one which is most sensitive to temperature is the carrier mobility, μ. The value of μ for both PMOS and NMOS devices is approximately inversely proportional to $T^{2.5}$ where T is the absolute temperature [9]. As the temperature changes from -40C to 85C, the value of μ decreases by a little more than a factor of 2, which, consequently, implies that the value of the resistance of a single device increases by more than a factor of 2.

Let us consider how this factor of two change in resistance affects the settling of capacitor voltages. Consider a simple RC circuit with $R = C = 1$ where a unit step voltage is applied and the output voltage is read across the capacitor. Then the output voltage as a function of time is given by

$$v_o(t) = (1 - e^{-t})u(t) \tag{3.3}$$

where $u(t)$ denotes the unit step function. If we wish the circuit to settle within 0.01% of its final value, we must wait 9.2 seconds.

Now consider the same RC circuit as above, except now let $R = 2$. In this case, we must wait 18.4 seconds in order for the circuit to settle to 0.01% precision. If we only wait 9.2 seconds as before, we find that the circuit settles to within only 1% of it's final value, a stark contrast.

Extending these results to simple transmission gates, we see that, if the equivalent resistance of each NMOS and PMOS device operating in the triode region doubles as the temperature increases from -40C to 85C (thus doubling the resistance of the

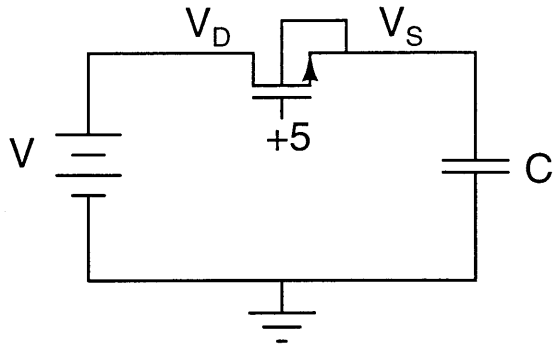

Figure 3-2: Circuit in which an NMOS switch connects a DC voltage of value V to a capacitor C charged initially to 0V. The voltage +5V is applied to the gate of the NMOS transistors at $t = 0$.

switch since it is the parallel combination of the NMOS and PMOS resistances), the amount of settling may fluctuate greatly within the allowed settling time. Because the $\Sigma\Delta$ for our application is clocked at a rate of 5.12MHz, the permissible settling time is one-half clock period, or approximately 95ns.

The above analysis points us in the direction of a potential problem. It is useful to analyze the system in its true nonlinear fashion to gain more insight as to where a potential settling problem in the circuit may exist. Consider the circuit depicted in Figure 3-2. To simplify the analysis, the PMOS device has been removed. In this circuit, a voltage source of value V drives a capacitor C which has 0V across it at the time that the NMOS switch is turned on. If we assume that V is less than one NMOS threshold voltage away from 5V, then, after turn on, the NMOS device will be conducting in the triode region with drain-to-source current given by

$$I_D = k'(V_{GS} - V_{Tn} - \frac{V_{DS}}{2})V_{DS} \tag{3.4}$$

where $k' = \frac{W}{L}\mu_n C_{ox}$ and V_G is the 5 volt supply [7]. By Kirchoff's Current Law, the drain-to-source current I_D must be equal to the current flowing through the capacitor which is given by $C\frac{dV_S}{dt}$. Setting equal the two constraint equations on I_D

and rearranging terms, we find that

$$\frac{dV_S}{(4-\frac{V}{2}-\frac{V_S}{2})(V-V_S)} = \frac{k'}{C}dt \tag{3.5}$$

for $V_G = 5V$ and $V_{Tn} = 1V$. Performing a partial fraction expansion on the left-hand side and integrating both sides of the equation, we obtain (after some algebra) that the voltage across the capacitor, $V_S(t)$, is given by

$$V_S(t) = \left(4-\frac{V}{2}\right)\frac{1-e^{(4-V)\frac{k'}{C}t}}{\frac{1}{2}-(\frac{4}{V}-\frac{1}{2})e^{(4-V)\frac{k'}{C}t}}u(t) \tag{3.6}$$

While the expression in Equation 3.6 may appear complicated, it does offer us some valuable insight. First, as a double-check, note that $\lim_{t\to\infty} V_S(t) = V$. In other words, in the steady state, the capacitor charges up to the applied input voltage, which is expected. Second, note that the rate of increase of the exponentials is proportional to the applied input voltage V. Specifically, the higher V, the slower the rate of increase. Thus, large input voltages have a longer settling time than small input voltages. This information immediately points us in the direction of the switches associated with the digital to analog converter as a potential source of settling time error. While the voltages at the input to the $\Sigma\Delta$ normally lie within 1V of MID, the DAC voltage is always either 0V or 4.25V. Thus, if settling is an issue over the full temperature range, we would expect that this phenomenon would be most apparent with respect to the settling of the DAC reference voltages.

Simulations were run which applied DC voltages of 0V and 4.25V as inputs to the discrete-time integrator depicted in Figure 2-11, but the settling of the the capacitors did not vary significantly over temperature (<0.1%). However, it was then realized that the reference voltages of the DAC are connected to the sampling capacitors via *two* transmission gates. A MATLAB simulation comparing the relative settling times of a switch composed of (i) one NMOS device and (ii) two NMOS devices is depicted in Figure 3-3. It is apparent from these plots that, when two NMOS devices are connected in series, the settling time increases.

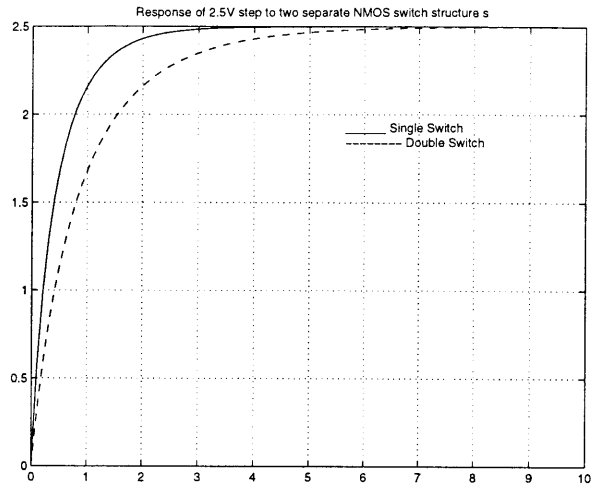

Figure 3-3: MATLAB simulation comparing the step response of a 2.5V step for $k'/C = 1$ using switches composed of (i) a single NMOS transistor (solid line) and (ii) two NMOS transistors in series (dotted line). The time scale is in seconds.

A schematic that was used to simulate the settling time of the front-end switched-capacitor integrator is shown in Figure 3-4. The op amp used in the simulation was single-ended and had infinite slew rate and bandwidth in order to isolate the settling issues due solely to the transmission gates. The clocks labeled ϕ_{1d} and ϕ_{2d} are slightly delayed versions of the clocks ϕ_1 and ϕ_2. The purpose of these delayed clocks is to ensure that the right node of the capacitor connects to a stable voltage reference (or, in the case of phase ϕ_2, to a stable virtual voltage reference) before any input and/or DAC feedback voltages are applied. This aids in reducing voltage glitches across the feedback capacitor [7].

The resulting output waveforms for nodes IN2 and OUT for temperatures at -40C and 85C are depicted in Figure 3-5. Assuming an ideal op amp, then the increment in the output voltage each clock cycle should equal -0.4 times the input voltage applied on the previous clock cycle. Thus, when 4.25V is applied to the sampling capacitor, the output voltage should decrease by 0.7V on the next clock cycle.

Examining the plots for IN2 at both temperatures, we see that there is a definite settling time issue with respect to the 2pF sampling capacitor as the waveforms at both temperatures appear to approach there steady-state values in a very slow man-

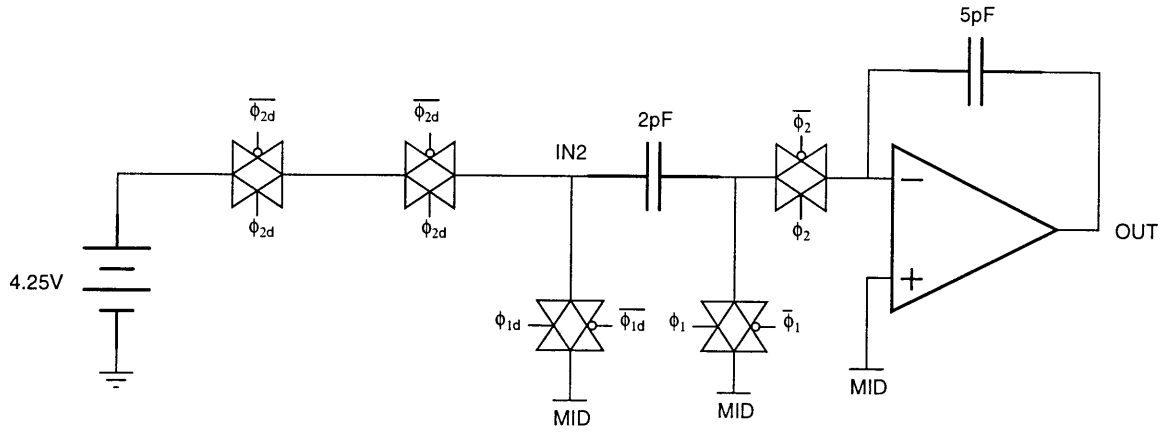

Figure 3-4: Schematic used to simulate settling time of DAC voltage on the sampling capacitor and the feedback capacitor of a switched-capacitor integrator.

ner. Indeed, when we measure the percentage error in the output voltage increment from 0.7V at the end of each clock cycle, we find that the output voltage only settles to within 0.8% of 0.7V at -40C and settles only to within 5% of 0.7V at 85C. Thus, the variation in settling over temperature of this configuration is 4.2%.

A MATLAB simulation of a block diagram description of the third order $\Sigma\Delta$ was then run incorporating a settling error of 1% in the front end integrator, and the resulting output spectrum magnitude at 20kHz also changed by roughly 1%. Thus, the settling of the DAC voltage references is highly correlated within the amplitude of the 20kHz harmonic in the output spectrum, and, therefore, measures had to be taken to reduce the settling time of the output spectrum.

Returning to our linear model of the switches, we see that if we double the width-to-length ratio of each MOSFET, the resistance should divide in half. Consequently, the settling time of the capacitors should decrease and the settling error over temperature should decrease greatly.

Figure 3-6 shows the results of doubling the length of each transistor in all transmission gates. It should immediately become apparent that the settling time of the sampling capacitors has decreased as the waveforms for IN2 at both temperatures appear to approach their steady-state values more quickly than for the waveforms of

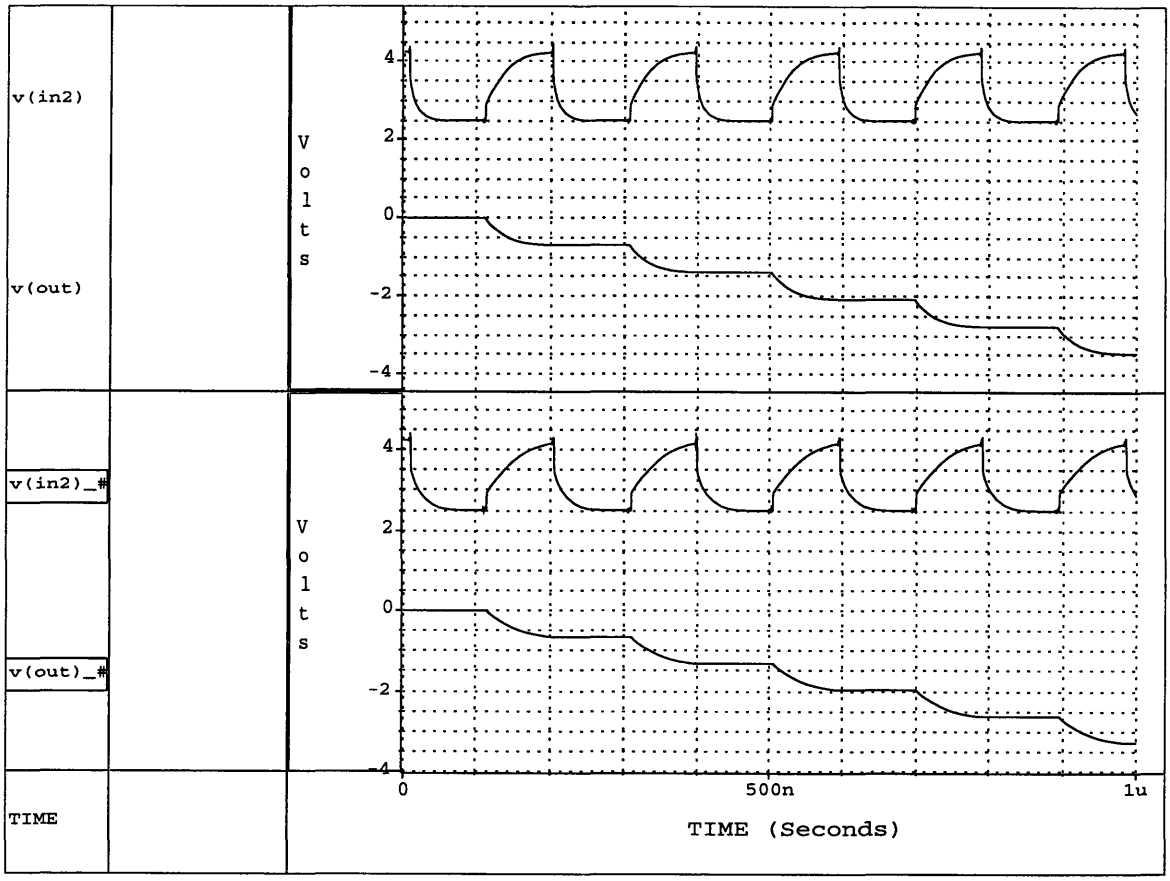

Figure 3-5: Output waveforms for circuit of Figure 3-4 for temperatures of -40C (top) and 85C (bottom). The settling of node OUT over the full temperature range varies by 4.2%

Figure 3-5; however, the output voltage at -40C settles to within 0.02% of its steady-state value, while at 85C it only settles to within 0.5% of it's final value. Figure 3-7 shows the results with the length of each PMOS device quadrupled and the length of each NMOS device doubled. We see that the waveforms for IN2 approach steady-state even faster than in the previous configuration. In this configuration, the output voltages reach within 0.01% of their steady-state output voltages at both temperatures which meets the stability specification of 0.1% error over the full temperature range.

3.2 Charge-Injection Compensated Switches

Unfortunately, the simple transmission gates which were used in the above simulations were not actually laid out in the existing third order $\Sigma\Delta$. A schematic of the switches that were laid out for use in implementing the switched-capacitor integrators is portrayed in Figure 3-8. The intention of this more complicated switch structure is to reduce the effects of charge injection. The central pair of PMOS transistors dispels a charge Q to both node 1 and node 2 when they turn off; however, at the same time that these PMOS devices are turning off, the dummy PMOS devices to the left and right are turning on, and, thus, should absorb this dispelled charge so long as the area of each dummy device is half the total area of the two PMOS devices. In this design, all of the width-to-length ratios for the transistors depicted in Figure 3-8 are (23.6/0.6), so the dummy devices should absorb all of the charge injected by the central pair of PMOS devices. A similar analysis can be performed for the NMOS devices to show that the two NMOS dummy devices cancel the charge injection of the central pair of NMOS devices. In reality, the charge injection of the central MOSFET devices does not usually split perfectly evenly between both nodes, but even with this asymmetry, the presence of the dummy devices often mitigates the effects of charge injection by at least a factor 5 [8].

In addition to charge injection compensation, the transmission gate of Figure 3-8 uses devices with a *much* higher width-to-length ratio than the transistors of the

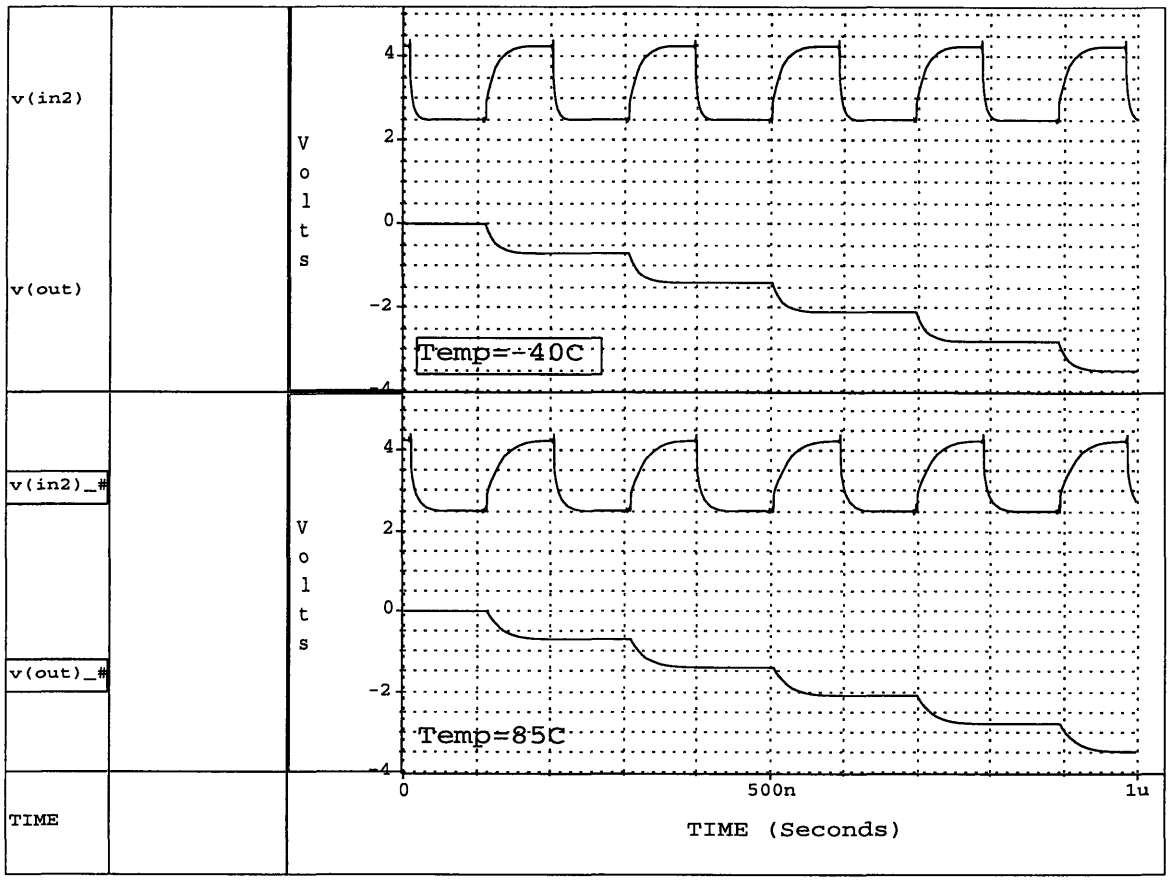

Figure 3-6: Output waveforms for circuit of Figure 3-4 with the length of each MOSFET doubled at temperatures of -40C (top) and 85C (bottom). The settling of node OUT over the full temperature range varies by 0.48%

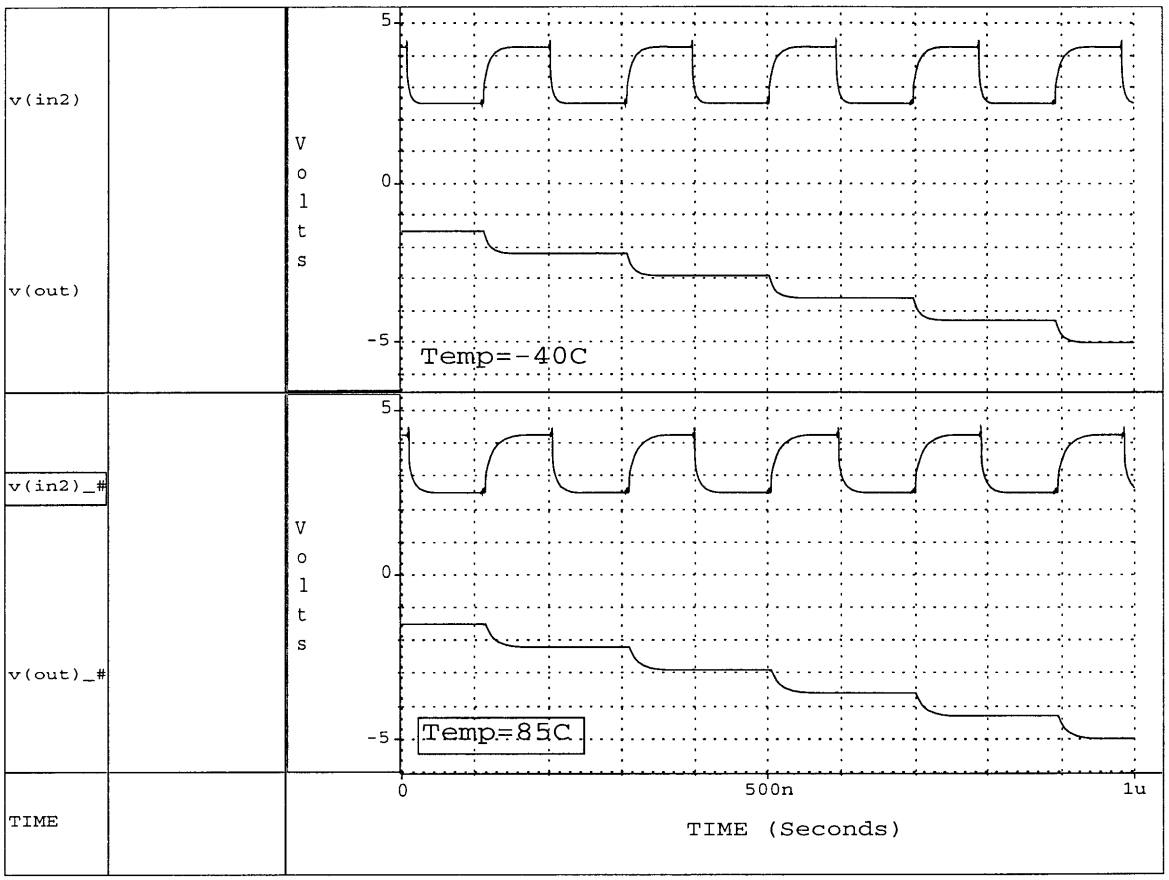

Figure 3-7: Output waveforms for circuit of Figure 3-4 with the length of each PMOS device quadrupled and the length of each NMOS device doubled at temperatures of -40C (top) and 85C (bottom) . The settling of node OUT over the full temperature range varies by less than 0.1%

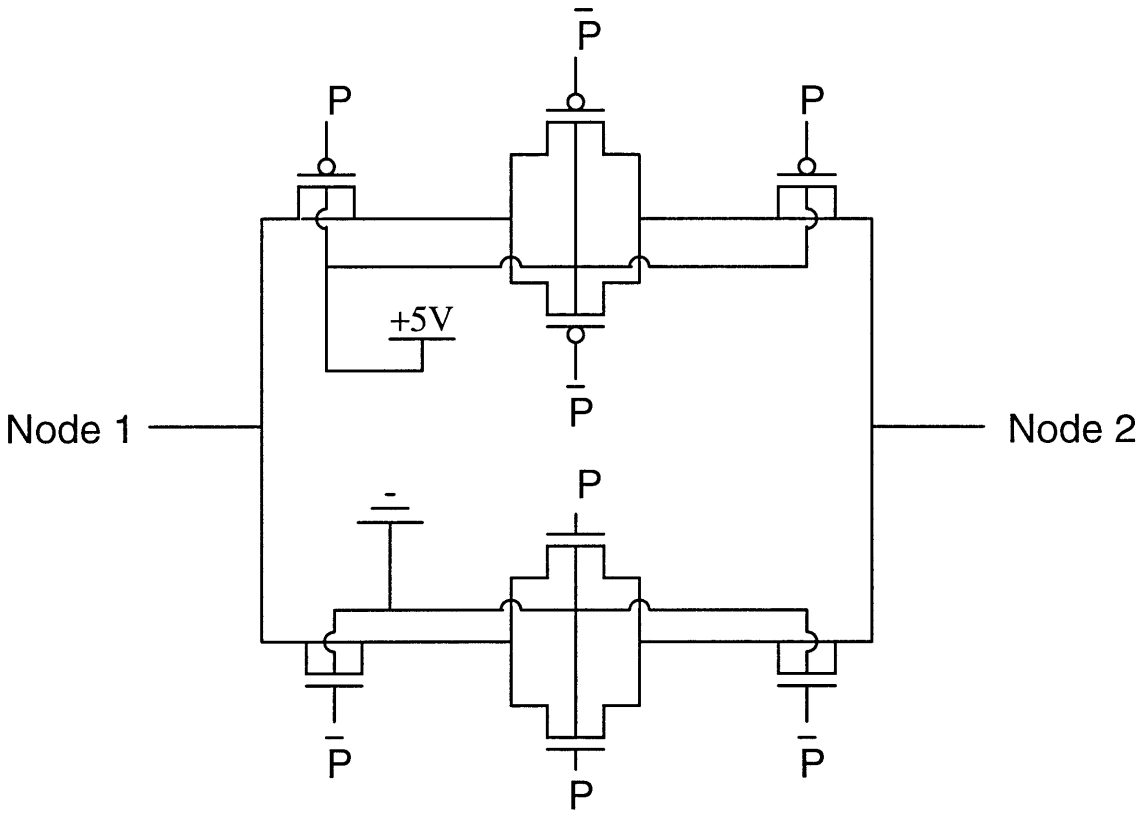

Figure 3-8: Transmission gates laid out in the third order $\Sigma\Delta$. The size of all transistors is $\left(\frac{W}{L}\right) = \left(\frac{23.6}{0.6}\right)$.

simple transmission gate—there is a factor of 13 difference between the two. Consequently, the drain to source resistance of the transistors is a factor of 13 smaller for this configuration, and we would expect that settling would not be an issue. Indeed, when simulations were run using the charge injection compensated transmission gates, the output waveforms of the op amps settled to well within 0.01% of their final value.

Even though the size of the transistors in the transmission gates did not turn out to be a problem, a valuable lesson was learned: make sure to size devices properly. As we have seen here, devices with too small a width-to-length ratio can cause severe settling issues.

Chapter 4

Op Amp Transistor Mismatch

In this chapter, we discuss issues relating to errors in the dimensions of the op amp transistors due to imperfections in the fabrication process. These errors can have severe repercussions, particularly in a differential circuit such as an op amp whose operation depends heavily on the fact that the transistors in each differential half circuit are perfectly matched. Because, in reality, our circuit will never have perfectly matched transistors, it is important to be able to quantify the sensitivity of the circuit performance to mismatch conditions. HSPICE offers an option in which it will randomly vary a given parameter given enough information (probability density function, mean, and variance) and simulate the circuit with the randomly varied parameter in place of the ideal parameter. This option, known as a *monte carlo* simulation, can be used to randomly vary the dimensions of the transistors, as well as other parameters such as resistance and capacitance, and run simulations on the resulting circuits.

The results of this chapter briefly outline some of the basic monte carlo simulations that were performed. Due to time constraints, work on these simulations has currently come to a halt but will resume in the future. The results from these simulations are currently both perplexing and inconclusive, but they are presented as a basis for work with future monte carlo simulations on this $\Sigma\Delta$ circuit.

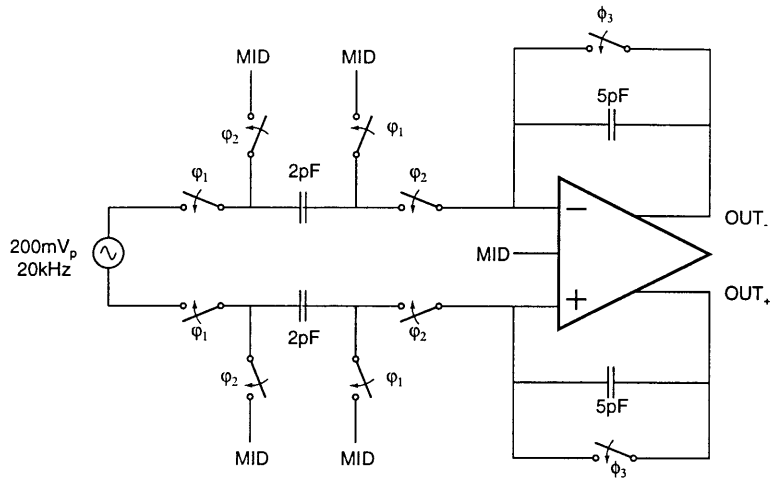

Figure 4-1: Switched-capacitor circuit used for monte carlo simulations.

4.1 Monte Carlo Simulation Results

All monte carlo simulations were performed on a fully differential switched-capacitor integrator and, as a comparison, a fully differential continuous-time integrator. Both integrators were configured in the same manner as in Figure 2-11 with three exceptions. First, F- and F+ were set to MID. Second, for the continuous-time integrator, the switched capacitor network was replaced by a single resistor of value 100K. Finally, for the switched-capacitor integrator, a voltage controlled switch was placed in parallel with each feedback capacitor which is controlled by phase ϕ_3. For the first 200ns of the simulation, these switches were turned on and had a resistance of 1Ω. After the first 200ns had expired, the switches were turned off and maintained a resistance of 1TΩ to simulate an open circuit. Schematics of both the switched-capacitor and continuous time integrators are depicted in Figures 4-1 and 4-2 respectively.

The results of simulating each of these circuits are plotted in Figures 4-3 (switched-capacitor) and 4-4 (continuous). All op amp transistors had widths and lengths which were perturbed by a Gaussian random variable with mean 0 and variance 0.1667μm. Different outcomes of the probability density function (abbr. PDF) were obtained via the HSPICE simulator and were added to the nominal transistor widths and lengths of the op amp model to obtain the transistor widths and lengths used in each monte

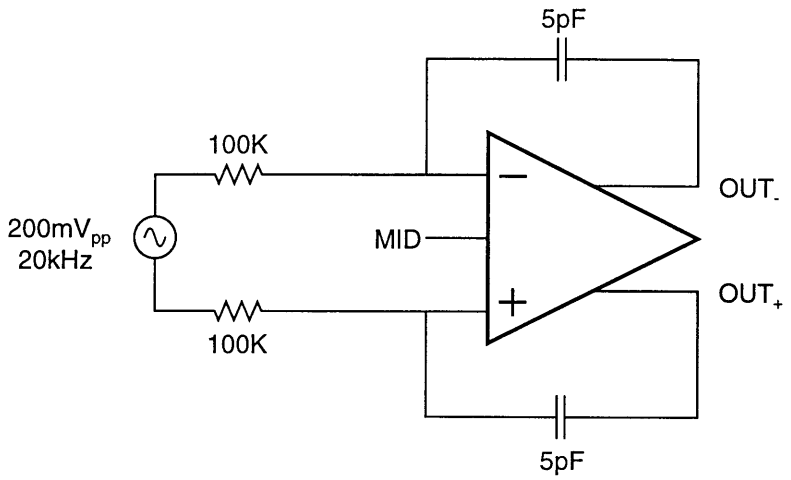

Figure 4-2: Continuous time integrator used for monte carlo simulations.

carlo trial. In cases where minimum length transistors were used, the absolute value of the PDF outcome was added to the minimum length (0.6μm) since HSPICE will not simulate MOSFETS with lengths less than 0.6μm due to model constraints.

For the first 10μs of each simulation, the sine wave generator was shut off; therefore, the voltage ramps which are visible in both the discrete- and continuous-time plots for the first 10 microseconds are due to the offset voltage of the op amps. As is apparent from these results, the offset voltage can become quite large since some of the ramps have a large slope. In order to measure the peak-to-peak amplitude of the sine waves, we need to measure this offset ramp so that we can obtain an accurate measurement.

The algorithm for cancelling the offset voltage in sine wave amplitude measurements is as follows. We know the frequency of the sine wave is 20kHz. Therefore, the maximum and minimum values of the sine wave occur at one-quarter of a cycle and three-quarters of a cycle, or at 22.5μs and 47.5μs (recall the 10μs delay). The first step is to make voltage measurements of OUT+ and OUT- at these times. Next, we measure the slope of the corresponding offset ramp. Using this slope, we estimate the value of the voltage at the offset ramp at 22.5μs and 47.5μs as the measured slope multiplied by the corresponding time. These offset voltages can then be subtracted

Switched-Capacitor	Continuous
3.26283V	3.19298V
3.15414V	3.16989V
3.35575V	3.19360V

Table 4.1: Peak output amplitudes for three different discrete- and continuous-time monte carlo simulations of the circuits depicted in Figures 4-1 and 4-2 for a 20kHz, 200mV peak differential input sine wave at -40C.

from the corresponding measured voltages, and the peak amplitude of the sine wave can subsequently be determined.

Table 4.1 lists the peak amplitudes of the output sine waves for a 20kHz, 200mV peak fully differential input sine wave for three different monte carlo simulations at -40C. All amplitudes listed in the table include offset correction. An ideal version of the switched-capacitor integrator depicted in Figure 4-1 should yield a peak output amplitude of 3.25958V, while an ideal version of the continuous-time integrator of Figure 4-2 should yield a peak amplitude of 3.18310V. The above data shows that the switched-capacitor integrator is much more sensitive to transistor mismatch than is the continuous-time integrator. The amplitude of the switched-capacitor integrator varies by as much as 3.2% from the ideal value, while the continuous-time integrator varies by no more than 0.5%. Granted that much more data is required if we wish to state results of any statistical significance, but the data for the switched-capacitor integrator structure is alarming nonetheless.

Additionally, it has been noticed that the deviation from the ideal amplitude is highly correlated with the offset voltage. That is, large offset voltages lead to large amplitude deviations, *even when the offset is measured and subtracted out.* This very peculiar behavior is currently inexplicable.

Even more alarming, there are some additional simulations which indicate that the amplitude variation over temperature can reach as high as 0.9% when the peak amplitude of the sine wave deviates from the ideal amplitude by a large amount (3.61254V peak at -40C and 3.64473V peak at 85C, for instance); however, the data

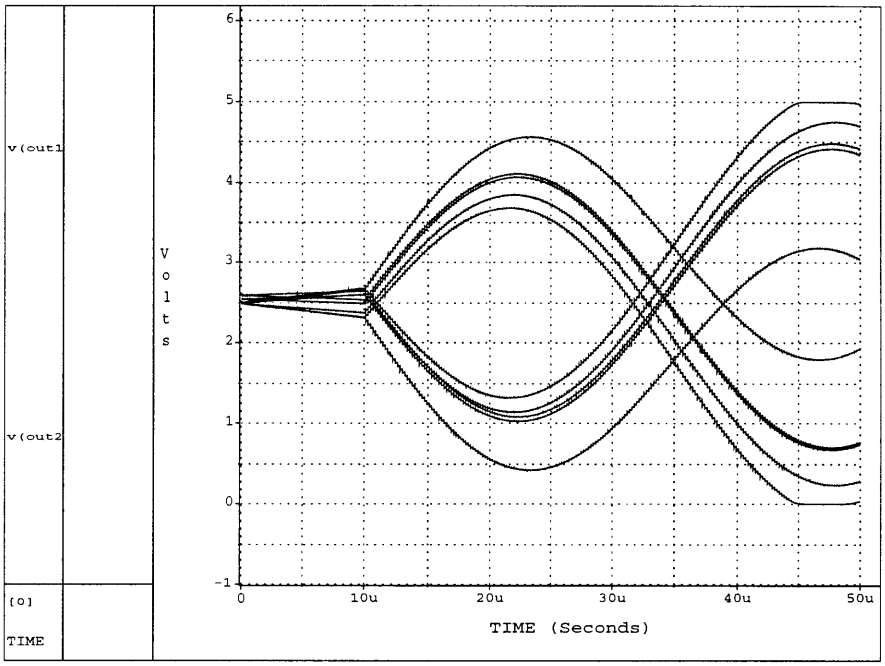

Figure 4-3: Monte carlo simulations for switched-capacitor integrator circuit.

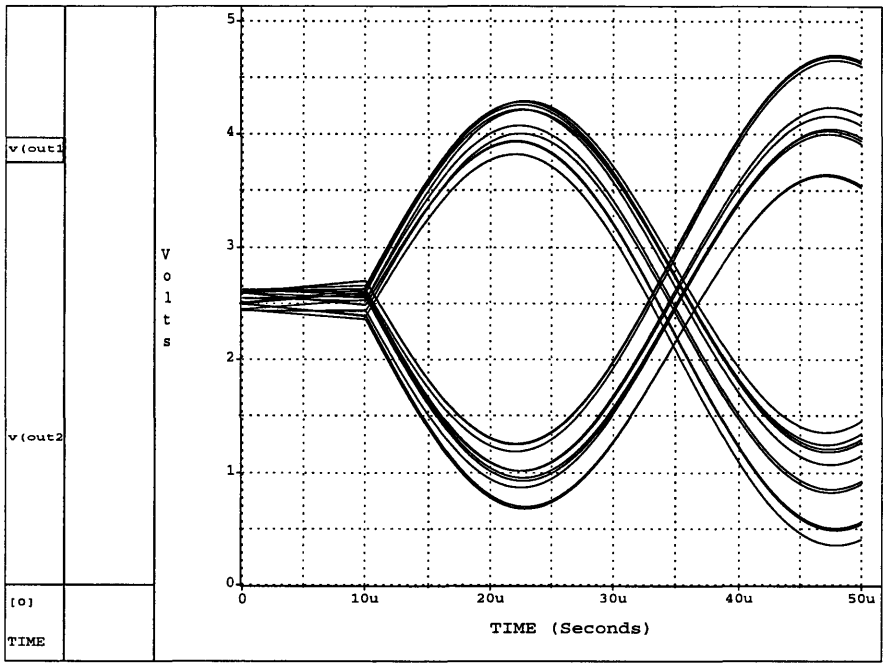

Figure 4-4: Monte carlo simulations for continuous time integrator circuit.

which support this hypothesis are currently in question as it is possible that the peak amplitudes measured in this simulation were not corrected for the output-referred offset ramps. Thus, the 0.9% change in temperature could be due to a change in offset over temperature and may have nothing to do with the structure of the switched-capacitor configuration at all. Nevertheless, this issue is still a serious one and should be investigated in the future.

4.2 Recommendations

It is likely that the effects demonstrated here are merely artifacts of the HSPICE simulator (i.e., the effect seen here will not actually occur in the fabricated circuit). Nevertheless, these simulations should be investigated further to determine whether the switched-capacitor architecture proposed in Figure 4-1 is inherently flawed. Care should be taken, however, only to simulate scenarios which are well thought-out; in general, to obtain one run of a monte carlo simulation at -40C and 85C takes roughly four to five hours if fairly high accuracy is desired in the simulated waveforms, so it is difficult to obtain information in a speedy manner (If accuracy is sacrificed somewhat, the length of the simulation can be reduced to about two hours). Consequently, running simulations which will provide little to no information can waste a large amount of time.

If it is determined that the switched-capacitor structure is the source of the AC gain error over the full temperature range, then it may well be worthwhile to investigate using continuous-time integrators instead, as it appears that their performance is much more stable with respect to transistor mismatch.

Chapter 5

Calibration

As none of the routes that I had investigated determined the source of the 20kHz gain error of the $\Sigma\Delta$ converter at hand, the next logical step was to try to see if the problem could be fixed *without* altering the existing $\Sigma\Delta$ circuitry. While this option is less desirable in that whatever phenomenon is causing the current gain error could cause problems in separate future circuits, it will at least allow us to meet the given gain drift specification. Fortunately, I discovered that such a calibration circuit can be implemented, at least in simulation. This chapter outlines the basic principles behind the calibration scheme and then describes the circuitry used to implement this system.

5.1 Calibration Scheme

The basic idea behind the calibration scheme is to compare the amplitude of the 20kHz harmonic with the amplitude of another periodic waveform that has been processed by the $\Sigma\Delta$, whose fundamental harmonic lies close to 20kHz and whose amplitude is fixed and known. If the amplitude of this waveform (referred to here as a *pilot tone*) is truly independent of temperature, then any fluctuations in the amplitude of its fundamental harmonic as seen at the output of the $\Sigma\Delta$ are due to the temperature drift of the $\Sigma\Delta$ itself. Furthermore, assuming the fundamental period of the pilot tone is sufficiently close to 20kHz, the drift of the pilot tone's fundamental

amplitude at any given temperature should be equal to the drift of the input signal at that same temperature. Thus, by examining the drift in this amplitude, we can compensate for the drift in the amplitude of the 20kHz harmonic.

Once the pilot tone has passed through the $\Sigma\Delta$, we can compute its amplitude via digital signal processing. Once we have this quantity, we can digitally divide the $\Sigma\Delta$ output bit stream by the AC gain error of the pilot tone's fundamental frequency. Since the AC gain error of both the pilot tone and the 20kHz harmonic should be the same, this division will exactly cancel the error, ignoring effects due to quantization.

A block diagram of the calibration scheme used in this application is depicted in Figure 5-1 while a block diagram of the digital processing is depicted in Figure 5-2. A 16kHz square wave which is approximately 100mV in amplitude was chosen as the pilot tone. The frequency was chosen on the basis that 16kHz lies in a low-noise region of the third order $\Sigma\Delta$'s noise transfer function and is very close to the frequency which we wish to calibrate (the 4kHz frequency difference between 16kHz and 20kHz is less than 0.1% of the sampling rate), and because the harmonics of the 16kHz square wave will not interfere with harmonics of the 20kHz waveform until 80kHz. Since 80kHz is heavily suppressed by the digital signal processing, we do not care about distortion of the 80kHz harmonic. Also, 16kHz is an integer division of the 5.12MHz clock which, as we will see, is important. The amplitude of this pilot tone was chosen to lower the harmonics produced by any intermodulation distortion below the thermal noise floor of the $\Sigma\Delta$'s output.

The digital processing first decimates the input bit stream by a factor of 64 since most of the input spectrum is quantization noise, and since decimation reduces the speed at which the DSP must carry out computations. The resulting signal is then passed through a constant gain to normalize the amplitude of the pilot tone's fundamental harmonic to 1 at room temperature. This signal is then demodulated by a digital sine wave of frequency 250Hz (the fundamental frequency of the pilot tone after decimation by 64) and lowpass filtered to obtain the instantaneous amplitude of the fundamental frequency of the pilot tone. The resulting amplitude is then divided into the decimated bit stream to produce a temperature-compensated waveform. This

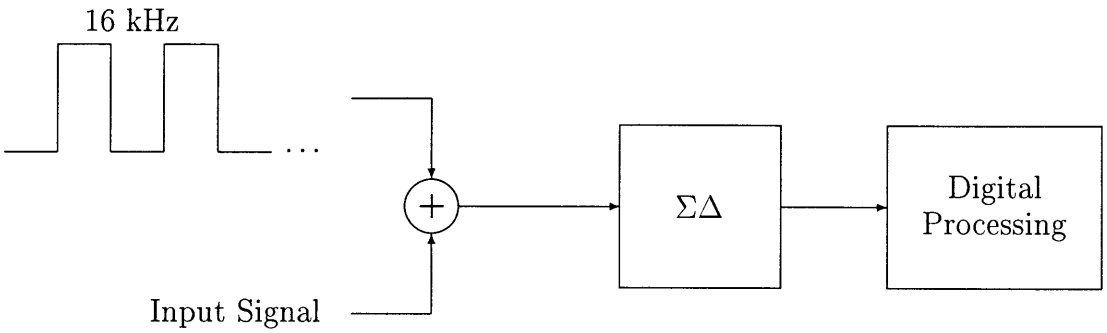

Figure 5-1: Block diagram of AC gain calibration scheme

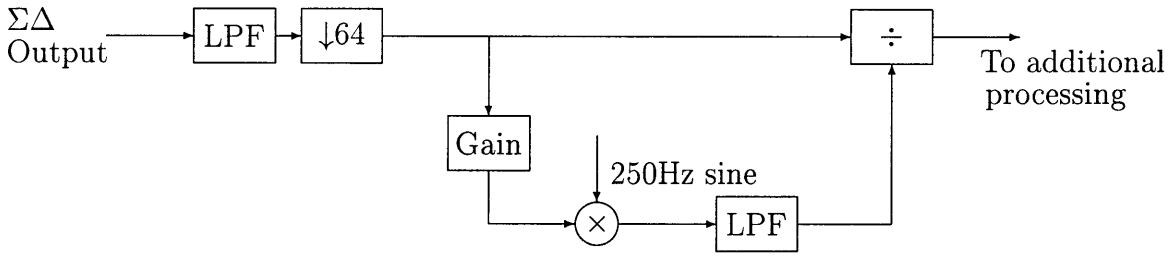

Figure 5-2: Digital Signal Processing of Figure 5-1.

waveform is further digitally processed to produce the desired output information.

All digital processing will be designed at some future time. The work that is presented here relates entirely to the analog circuitry used to create the pilot tone and adder depicted in Figure 5-1. The circuits used to accomplish these two tasks is described next.

5.2 Pilot Tone Circuitry

5.2.1 16kHz Clock Generator

Creating a square wave requires two components: a clock that oscillates at the frequency of the square wave, and a method of switching between two stable reference voltages to produce the square wave voltages. The first of these requirements is the topic of this section. It is imperative that the 16kHz waveform be derived from the same clock that is tied to both the 20kHz spectrum and the 5.12MHz clock which is used to operate the $\Sigma\Delta$. This will ensure that, in the discrete-time domain, both the 16kHz and 20kHz waveforms will be locked at their corresponding discrete-time frequencies.

As mentioned previously, 16kHz was chosen as the frequency of the pilot tone as it is an integer division of the 5.12MHz clock (specifically, it is 5.12MHz divided by 320). As it turns out, frequency division by an integer amount can be carried out in a relatively straightforward manner via digital circuits.

The simplest frequency divider circuit is a divide-by-2 circuit, depicted in Figure 5-3. In this figure, the DQ flip-flop triggers on the positive rising edge of CLKIN, as the timing diagram of Figure 5-4 indicates. Whenever CLKIN hits a rising edge, then Q follows D. In our case, D is equal to $\bar{Q}$. Thus, if Q is initially 0, then on the first rising of CLKIN, Q will toggle to 1. On the second rising edge, since D is now 0, Q will fall to 0. On the third rising edge, Q will toggle back to 1, and so on and so forth. Because it takes two rising edges of the clock to return the value of Q back to its original value, the frequency of the output square wave is exactly equal to half

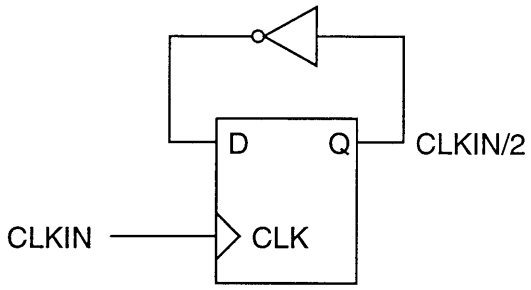

Figure 5-3: Frequency divide-by-2 circuit.

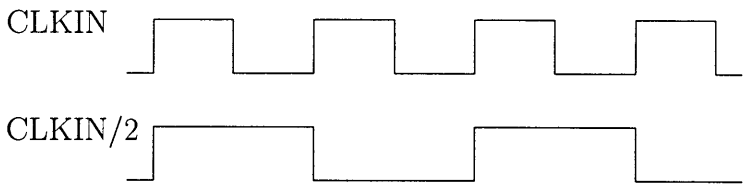

Figure 5-4: Timing diagram for frequency divide-by-2 circuit.

the clock frequency.

If we wish to divide a clock frequency by a power of 2, it follows that we can simply cascade as many divide-by-2 circuits as we need to achieve the appropriate frequency division. Unfortunately, we wish to divide the clock frequency by 320, which is not a power of 2. Thus, we need to resort to more exotic methods. First, note that 320 can be written as the product of 64 and 5. We know how to implement a divide-by-64 circuit, so all that remains to achieve the desired frequency division is to design a divide-by-5 circuit.

The circuit in Figure 5-5 performs the required division by 5 [1]. As is illustrated by the timing diagram of Figure 5-6, QD (also denoted as CLKIN/5) produces a pulse on every fifth falling edge of the clock. Note that QB, QC, and QD need not be initialized to particular values in order for the circuit to perform as intended. Examining the truth table of Table 5.1, we see that the circuit toggles through five of the eight possible combinations of QD, QC, and QB. Thus, if the initial state is

QD	QC	QB
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0

Table 5.1: Truth Table for frequency divide-by-5 circuit

one of the states listed in the truth table, the circuit will follow the timing diagram of Figure 5-6 starting from the initial state. For instance, if the initial state is $QD = 0$, $QC = 1$, $QB = 0$, the circuit would start following the timing diagram of Figure 5-6 on the rising edge of the third CLK pulse and continue on. But what if the initial state is *not* one of the states listed in the truth table? This corresponds to the case where $QD = 1$, and one or possibly both of QC and QB are 1. If this occurs, the output of NAND gate 1 will always output a 1 since the input due to $\bar{QD}$ is 0. Thus, neither QB or QC can toggle. At the same time, because $\bar{QD} = 1$, the output of NAND gates 2 and 3 is 1, which means that the output of the NOR gate is 0. Consequently, the value of TD is equal to the inverse of CLKIN. Thus, as CLKIN toggles, TD toggles as well, which further means that QD will eventually toggle to 0. When this happens, the state of the circuit will enter one of the states listed in Table 5.1 and will simply follow the timing diagram.

The composite divide-by-320 circuit is depicted in Figure 5-7. We cascade the output of the divide-by-5 circuit with six divide-by-2 circuits which, together, achieve an effective frequency division of 64.

5.3 Square Wave Generator

The basic schematic of the circuit used to create the square wave and add it to the input signal is depicted in Figure 5-8. Since the amplitude of the square wave is to be small, we first create a stable voltage reference VREF via a resistive divider between

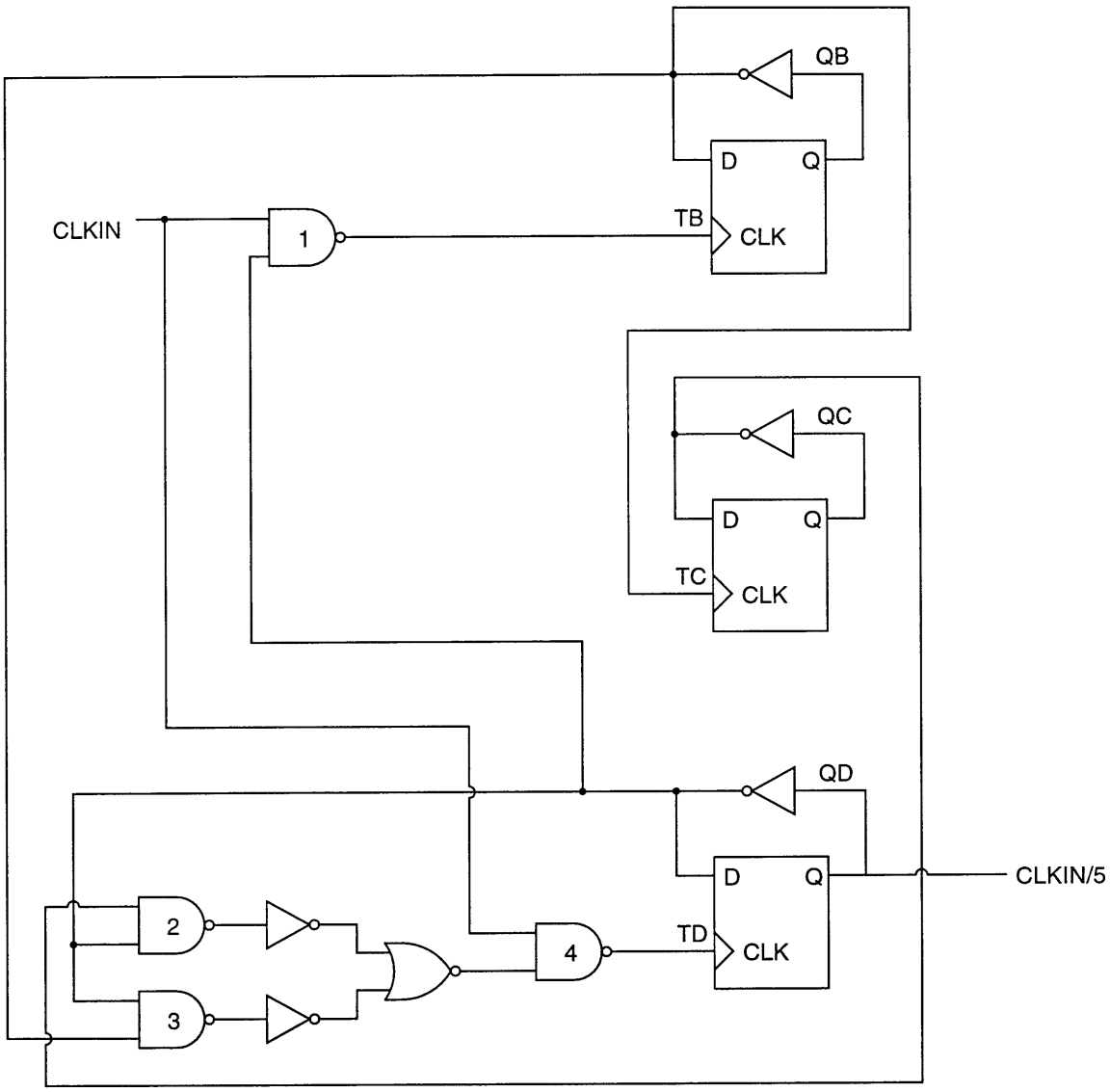

Figure 5-5: Frequency divide-by-5 circuit.

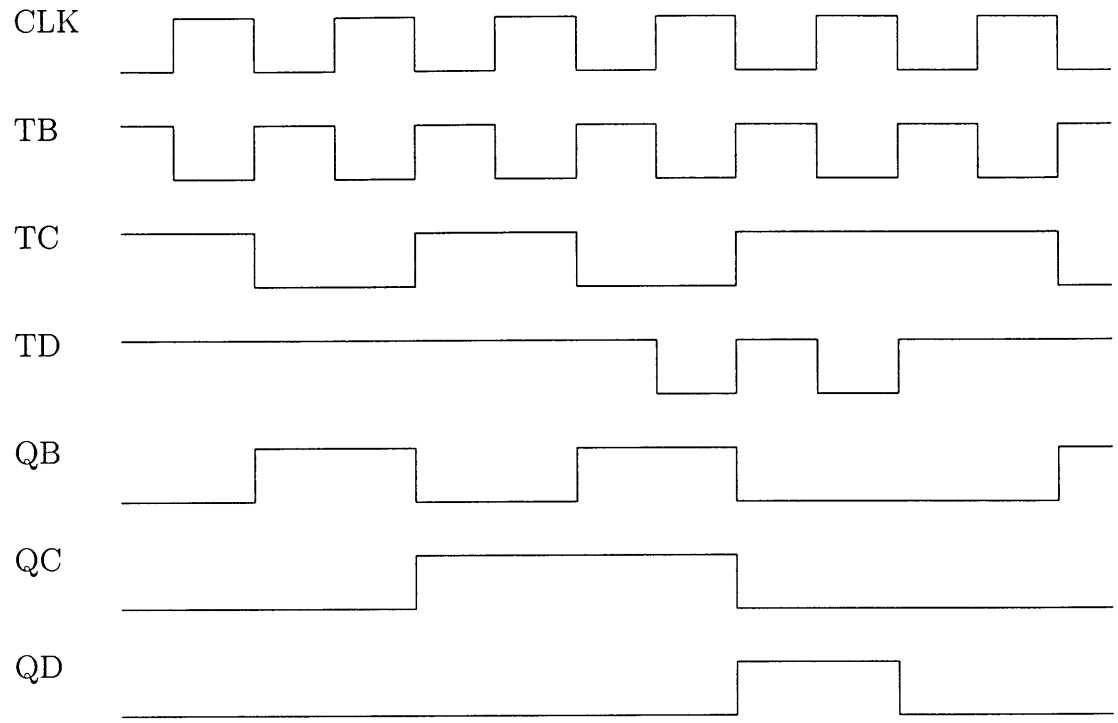

Figure 5-6: Timing diagrams for frequency divide-by-5 circuit.

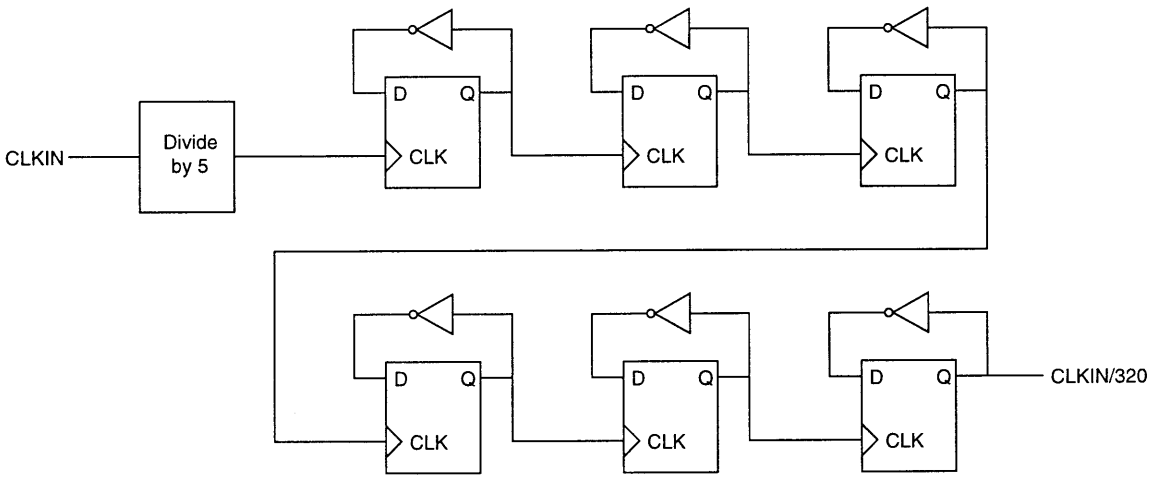

Figure 5-7: Frequency divide-by-320 circuit.

PREF and MID. To create the square wave, we then take two single-ended op amps connected in a unity gain configuration and connect each of them to a set of two switches, one of which connects to MID, the other of which connects to VREF. The logic levels S1 and S2 are non-overlapping clock signals with a frequency of 16kHz which control the state of the switches. When S1 is high and S2 is low, op amp 1 will output a voltage roughly 56mV above MID, while op amp 2 will output MID. When S1 is low and S2 is high, op amp 2 will output 56mV above MID while op amp 1 will output MID. Thus, viewing the output of these two op amps as the output of op amp 1 minus the output of op amp 2, we see that this portion of the circuit creates a fully differential square wave with a peak-to-peak amplitude of approximately 112mV. This output is then input to an inverting adder circuit which adds the input voltages of the third order $\Sigma\Delta$ to the 16kHz square wave. The output of this inverting adder circuit is then input to the $\Sigma\Delta$ for processing.

While this calibration circuit appears fairly simple, there is much "behind-the-scenes" information about the circuitry which allows it to successfully carry out its task. We now explore each of the important details of this design in turn.

5.3.1 Operational Amplifiers

The operational amplifiers chosen to implement this design is key to its success. In order to be able to reduce the temperature-induced AC gain error to within 0.1%, the amplitude of the square wave used to calibrate the rest of the circuit must remain stable to within this precision. The use of the single-ended buffer circuits in Figure 5-8 eliminates many sources of temperature-induced error. One major source of temperature error which we have already seen can reek havoc upon circuits is the change in the resistance of the transmission gates (which are implemented using the charge injection compensated version of Figure 3-8) over temperature. Were the switches in this circuit connecting two finite impedance nodes, the change in the switch resistance would change the Thèvenin resistance seen by node VREF and, consequently, change the voltage at this node; however, all op amps in the figure are entirely CMOS, so the input stage of each op amp has roughly an infinite impedance when compared to

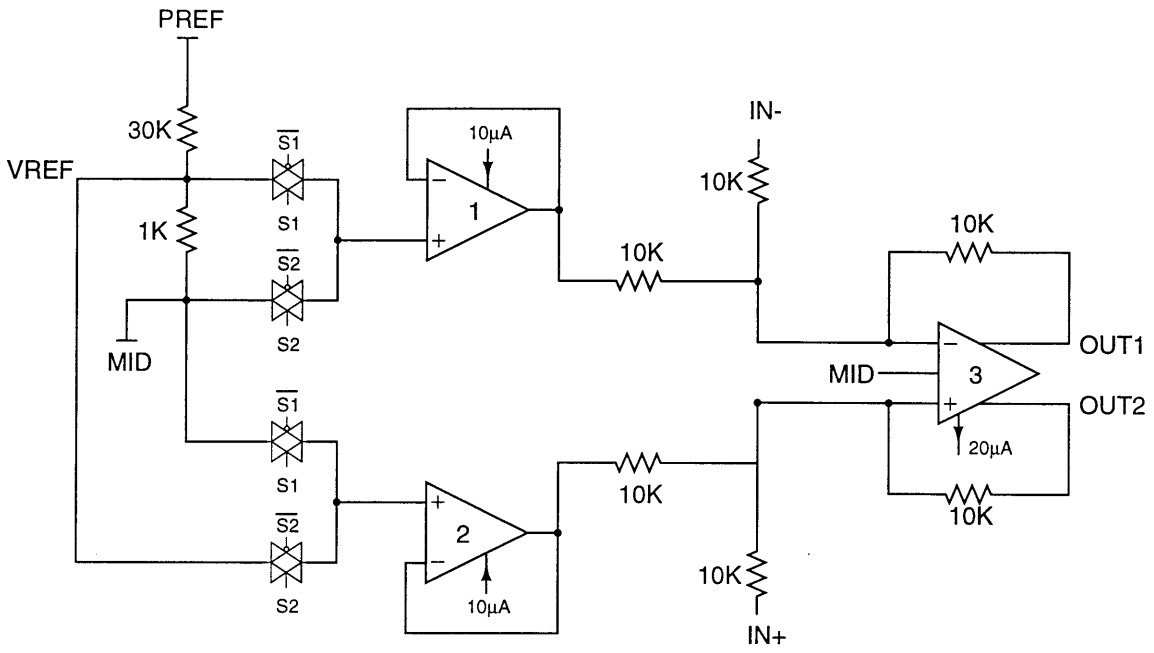

Figure 5-8: Square wave generator and inverting adder.

the impedances of the resistors and switches used in this circuit. Thus, VREF sees an open circuit to the right of the resistor string regardless of the resistance of the switches.

Another potential source of temperature-induced error is the error in the resistance of the resistors themselves. While the value of each resistor may vary absolutely by as much as 10-20%, any pair of resistors is generally matched to within 0.05%, so the value of VREF should not deviate too much from the ideal value of 56mV at room temperature. Additionally, because the resistance of each resistor will vary by the same factor as the temperature changes, the value of VREF should not change over temperature since it is derived via the ratio of two resistances. Indeed, simulations indicate that, over the full temperature range, the amplitude of the square wave as seen at both the input to the summing op amp and at the outputs OUT1 and OUT2 changes by less than 0.01%[1].

[1]It is possible that the simulations may have indicated an even smaller percentage drift over temperature, but the number of digits for each voltage recorded by the simulator is quantized to 10μV which is 0.01% of the square wave's amplitude.

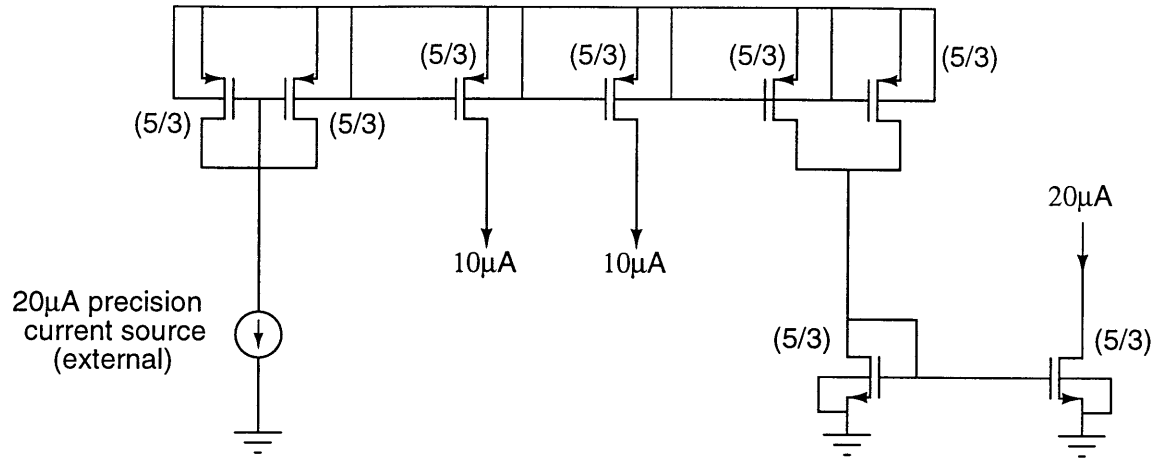

Figure 5-9: Current mirror used to generate op amp bias currents. The two 10μA sources bias op amps 1 and 2, while the 20μA sink biases op amp 3.

5.3.2 Current Sources

As indicated by Figure 5-8, each of the op amps used in the circuit has a programmable bias current. The current mirror used to produce each of these bias currents is shown in Figure 5-9. The two 10μA sources are used to bias op amps 1 and 2, while the 20μA sink biases op amp 3. The value of the currents used to bias the two single-ended op amps was chosen simply because the performance of this op amp at 10μA set current had been measured in the past, and the results indicated that the performance would be acceptable for this application in terms of settling time and offset voltage. The bias current of the fully differential op amp was chosen for similar reasons, but also because a 20μA set current allows the adder circuit to act as an anti-aliasing filter, as well. A 20μA set current band limits the output of op amp 3 to roughly 4MHz$\pm$1MHz which has been deemed sufficient anti-aliasing for the current application of the third order $\Sigma\Delta$.

5.3.3 Timing Circuitry

In addition to the required analog circuitry, a large amount of digital circuitry is necessary to control the transmission gates. A schematic of this control circuitry

is depicted in Figure 5-10. The ENABLE logic input allows the user to turn off the square wave generator. When ENABLE is low, the divide by 320 circuit is disactivated. This is important as it ensures that no unwanted AC components will accidentally feed through to the input of the $\Sigma\Delta$. Also, the additional NAND and inverter at the output of the DQ flip-flop are used to ensure that the values of S1 and S2 will be the same every time the divide-by-320 circuit is disabled. This ensures that the output voltages of op amps 1 and 2 will not depend on the output value of the DQ flip-flop just before the divide-by-320 circuit was turned off. Thus, the differential output of op amps 1 and 2 is now a small (56mV) DC voltage which should not affect the performance of the $\Sigma\Delta$. Adding the extra NAND and inverter guarantees that the polarity of this DC voltage will not change if we turn the square wave generator back on and then shut it off again. This feature is added primarily to aid in debugging the entire calibration circuit. If we need to perform tests on this circuit with the square wave generator shut off, we would like to make sure that the output of op amps 1 and 2 remain in the same state every time we run a particular test so that the results will be repeatable. If the polarity of the differential output voltage between the two op amps changes, we cannot guarantee this.

The circuits labeled BBML ("Break before make logic") are used to generate non-overlapping complementary clock waveforms. This is necessary to ensure that VREF is not temporarily shorted to MID as S1 and S2 transition between states. A schematic of a BBML is depicted in Figure 5-11, and a timing diagram is shown in Figure 5-12. From the timing diagram, we see that MK and BKP form a set of non-overlapping clocks (note that the delay due to the NAND gates and inverters is exaggerated to make this explicit). So, if we choose S1 to be MK and S2 to be BKP, both switches in each pair should never conduct at the same time.

When used in conjunction with a BBML, the block labeled "Switch Logic" can be used to create the necessary clock phases to run the switched capacitor integrators. A schematic of the switch logic block is depicted in Figure 5-13. The blocks labeled "Dig. Dly." (see Figure 5-14) are used to add delay between ϕ_1, ϕ_2 and ϕ_{1d}, ϕ_{2d}. When D2 is high, the delay is longer than when D2 is low. This can be seen from the

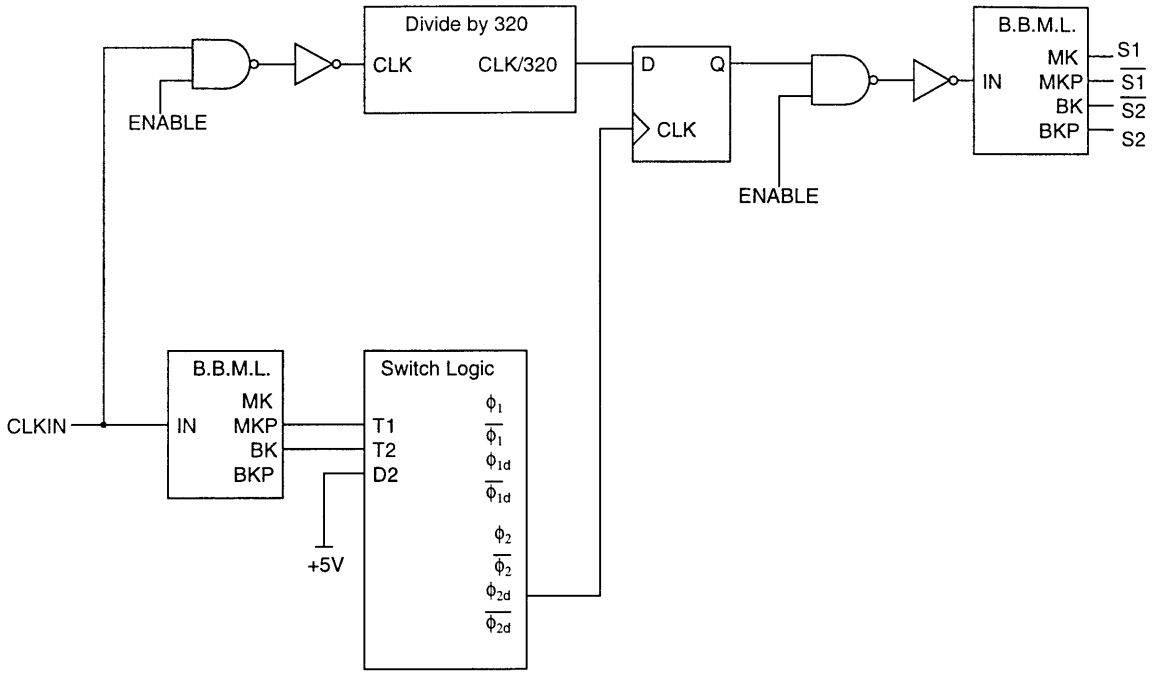

Figure 5-10: Digital circuitry used to implement S1 and S2 of Figure 5-8.

fact that, when CNTL is high, IN must propagate through two NAND gates and two inverters before reaching OUT, whereas, when CNTL is low, IN need only propagate through two NAND gates.

While the calibration circuit to be fabricated is a separate chip that is to interface the $\Sigma\Delta$ and, thus, contains no switched-capacitor integrator circuits, we still need to reproduce the clock phase ϕ_{2d} in order to make the S1 and S2 transition periods occur when the input to the $\Sigma\Delta$ is *not* in the sampling mode. As Figure 2-11 suggests, this occurs during phase ϕ_2. Thus, we wish to lock the transitions of S1 and S2 as close as possible to the beginning of phase ϕ_2 to maximize the amount of time the op amps have to settle before the input to the $\Sigma\Delta$ begins to sample. Applying the output of the divide-by-320 circuit to a DQ flip-flop which is clocked by ϕ_{2d} accomplishes this task. Note that ϕ_{2d} was chosen in lieu of ϕ_2 to avoid any glitches that may occur if ϕ_{1d} is still high when ϕ_2 transitions high[2].

[2]The BBML circuit should prevent this from happening. Choosing ϕ_{2d} over ϕ_2 is merely an extra precaution.

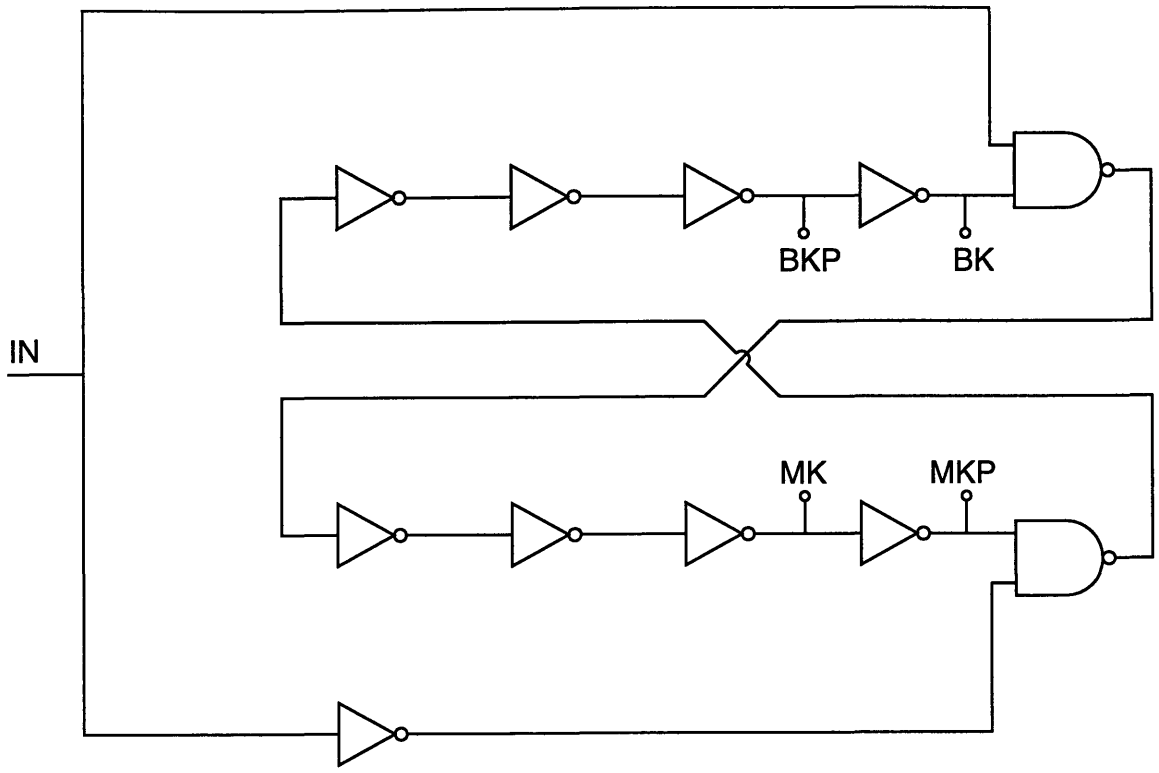

Figure 5-11: BBML circuit used to generate non-overlapping complementary clocks.

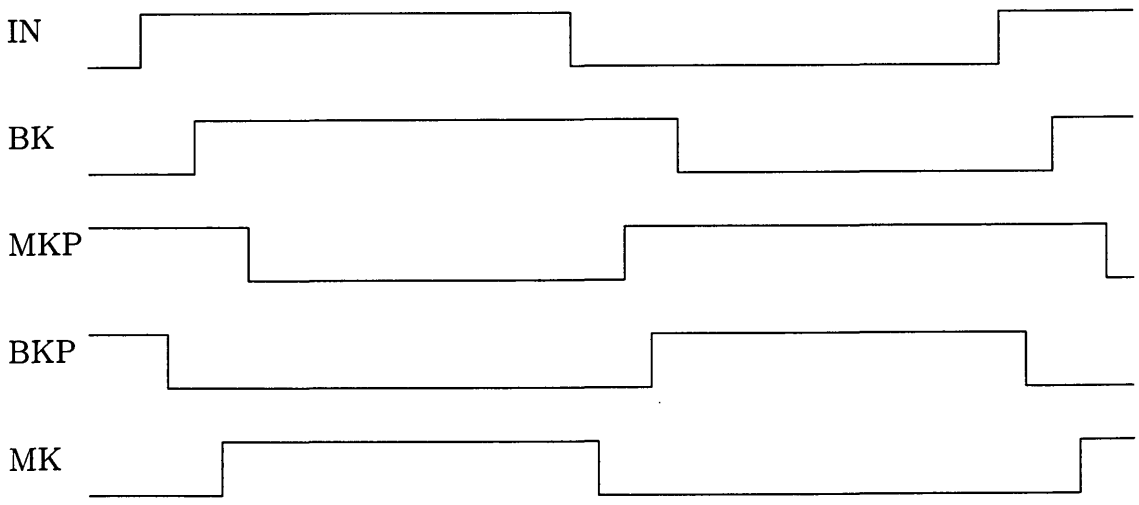

Figure 5-12: Timing diagram for break before make logic (not drawn to scale).

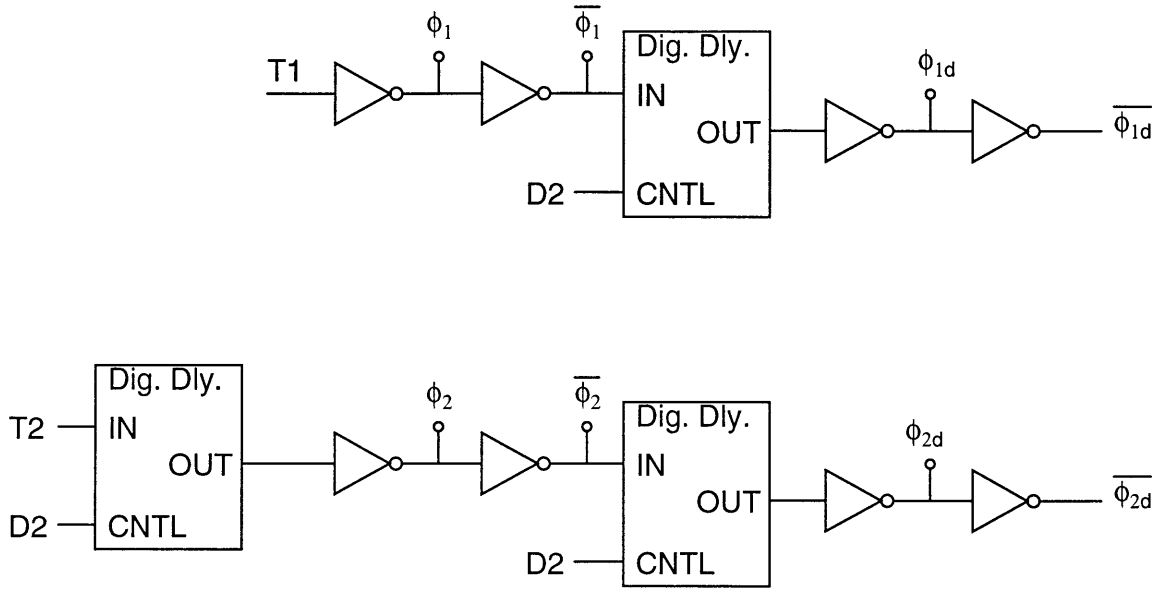

Figure 5-13: Switch logic circuit.

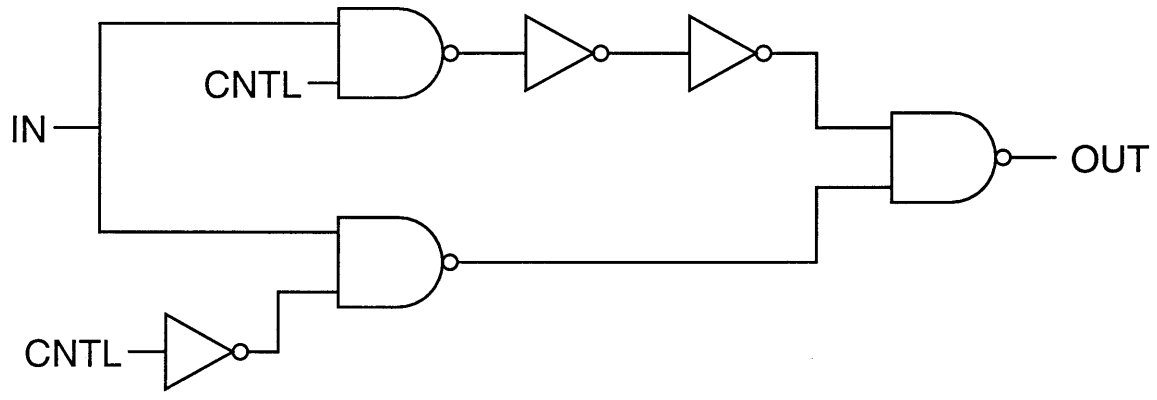

Figure 5-14: Digital Delay circuit.

5.4 Results

Figures 5-15 and 5-16 show the output waveforms of the calibration circuit near a transition in the square wave at temperatures of -40C and 85C, respectively, when the inputs IN+ and IN- are both set to MID. The DC offset from MID apparent in both OUT1 and OUT2 is due to the common mode offset of op amp3 of Figure 5-8. Notice that the OUT1 and OUT2 waveforms due not appear to settle until 250 to 300ns after they initially begin to transition. Consequently, when OUT1 and OUT2 are subsequently sampled onto the input sampling capacitors of the $\Sigma\Delta$, the square wave voltages will not have fully settled. This incomplete settling, however, does not affect the performance of the calibration system in an ill manner. Incomplete settling will cause small even harmonics to appear in the output spectrum (recall that an ideal square wave is composed entirely of odd harmonics), but the output amplitude of the fundamental 16kHz frequency will be virtually unaffected. As mentioned previously, the output amplitude of the square wave measured with respect to the output terminals OUT1 and OUT2 varies by less than 0.02% over temperature (0.01% variation for each output), so the amplitude of the 16kHz harmonic should remain stable to within this amount, as well.

Figures 5-17 and 5-18 also show the output waveforms of the calibration circuit at -40C and 85C, except, in this case, random variations have been added to the widths and lengths of the HSPICE models for both the single-ended and fully differential op amps of Figure 5-8. Note at -85C, the DC values between which OUT1 and OUT2 toggle are different for each of OUT1 and OUT2 (OUT1 toggles between roughly 2.64V and 2.695V while OUT2 toggles between approximately 2.635V and 2.69V). This implies that a DC differential voltage induced by the mismatched transistors has been added to the differential output voltage. Because this component is common to both OUT1 and OUT2, it does not affect the amplitude of the square wave. Measurements of the amplitude of the square wave in this scenario still indicate that the amplitude of the square wave is stable to within 0.02%. Moreover, because this additional component lies at DC, it will not affect the amplitude of the 16kHz

harmonic.

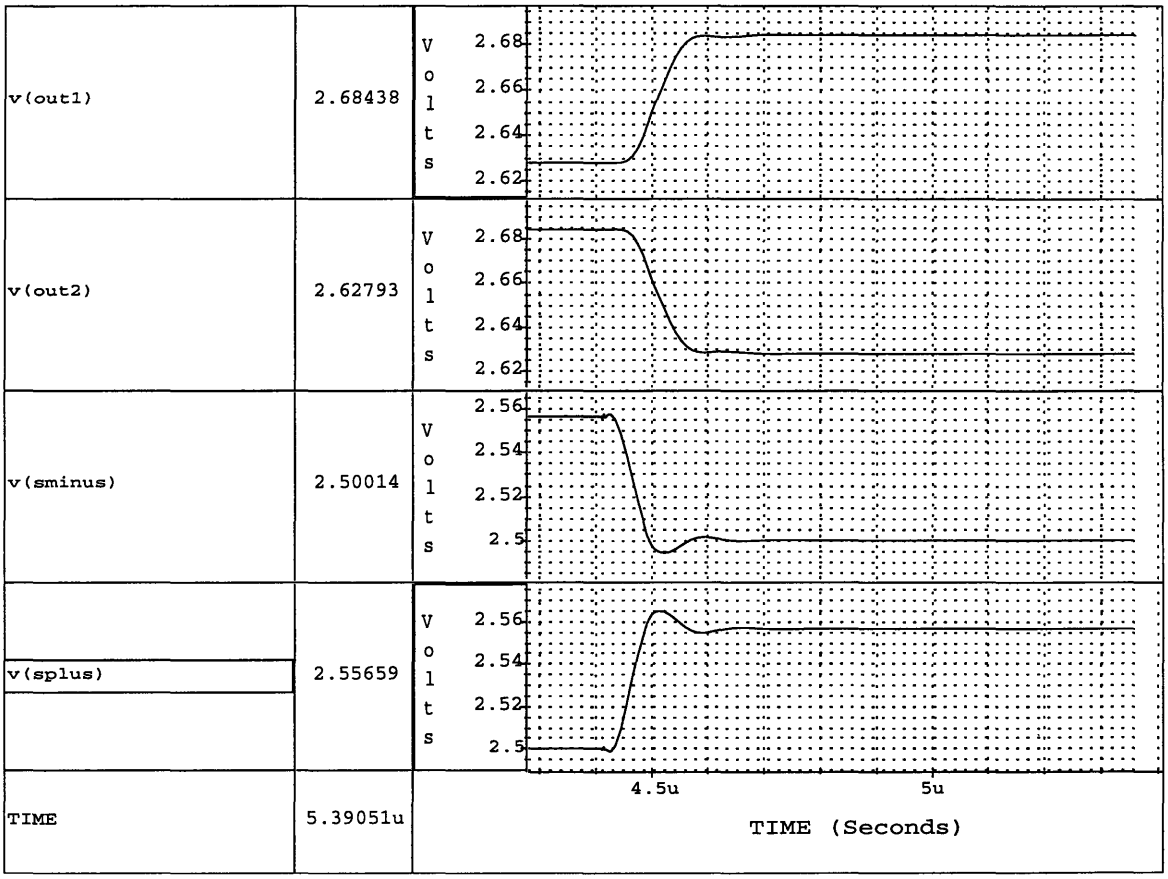

Figure 5-15: Output waveforms of calibration circuit at -40C.

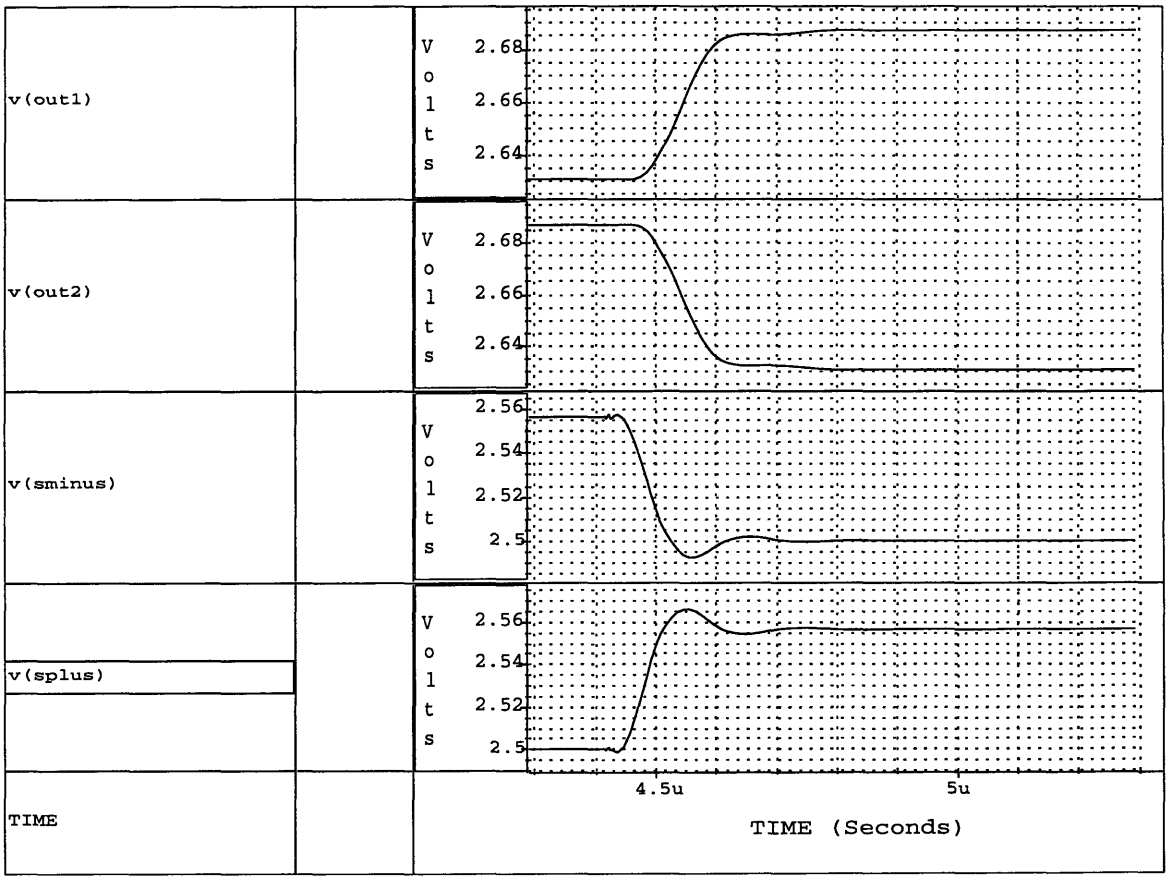

Figure 5-16: Output waveforms of calibration circuit at 85C.

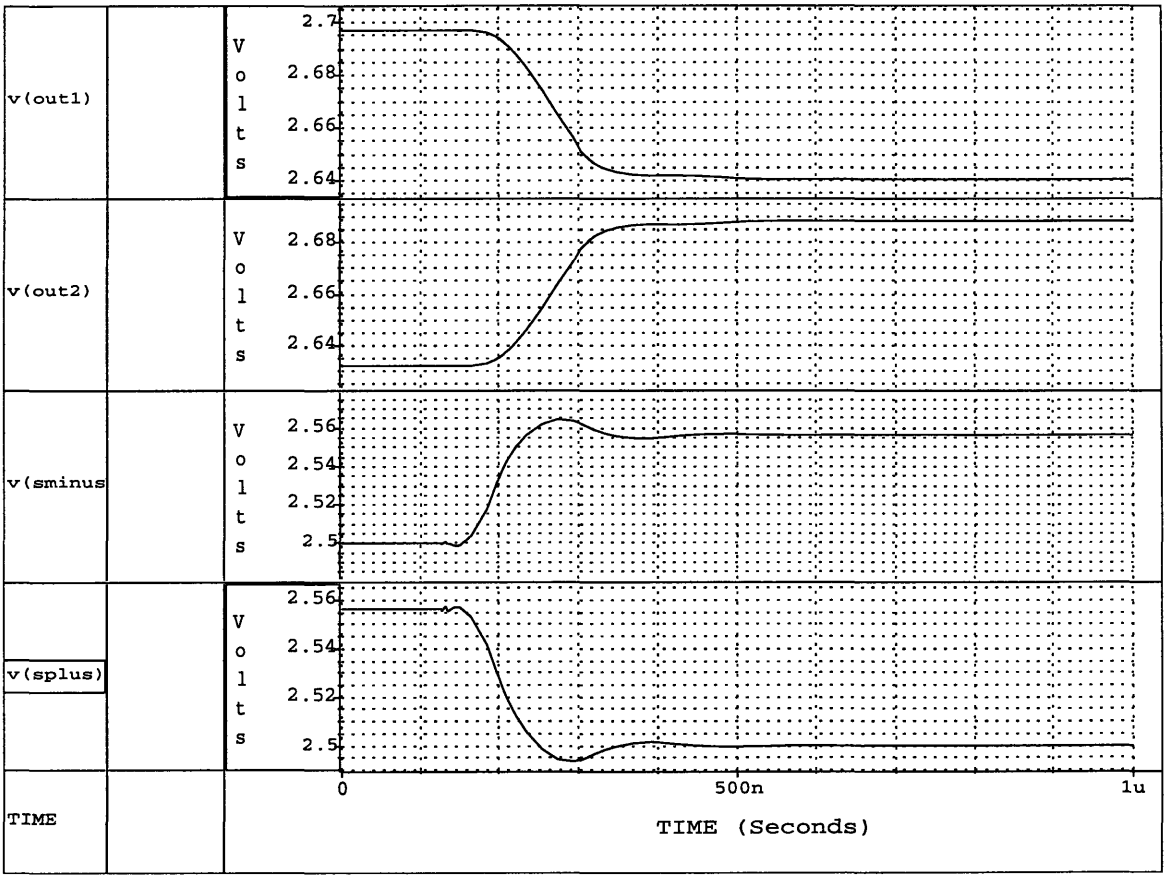

Figure 5-17: Output waveforms of calibration circuit at -40C with random width and length variations added to the transistors in each of the op amp models.

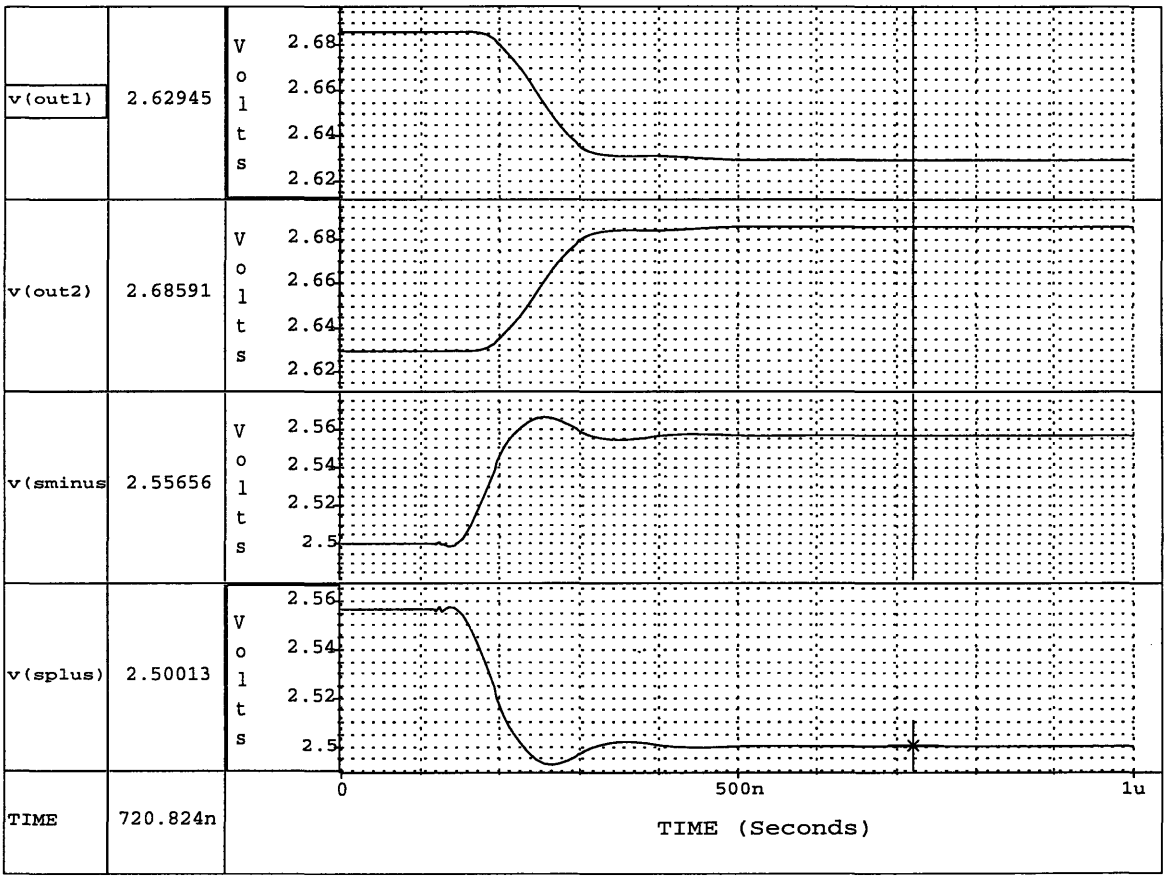

Figure 5-18: Output waveforms of calibration circuit at -40C with random width and length variations added to the transistors in each of the op amp models.

Chapter 6

Conclusion

In this document, we have analyzed potential sources of temperature-induced gain variation in the 20kHz harmonic of a third order $\Sigma\Delta$ analog to digital converter, and have offered a potential solution to fixing this problem. While neither of the potential sources of error which were analyzed determined the flaw in the existing $\Sigma\Delta$ circuit which causes the AC gain drift, they both provided some useful information. In the case of the transmission gate structure analysis, we now know that the structure currently implemented in the third order $\Sigma\Delta$ is *not* the source of the problem. Also, we know for future circuit designs that the width-to-length ratios of the transmission gates can only be made so small before causing detrimental effects. In the case of the monte carlo simulations used to model transistor width and length mismatch, the direct information we obtained was even less than that which we learned from the transmission gate analysis; however, these tests do naturally lead us to question both the structure and utility of switched-capacitor integrators as opposed to continuous-time integrators. Further tests involving monte carlo simulations of both types of integrators will be conducted in the future, and plans to investigate the possible advantages of using continuous-time integrators in place of switched-capacitor integrators will soon go underway, as well.

Nevertheless, while the source of the AC gain drift has not been identified, the calibration circuit which is to be cascaded with the input of the $\Sigma\Delta$ should eliminate this drift. The simulations show that, even when random offsets are added to

the widths and lengths of the op amp transistors, the amplitude of the calibration waveform remains extremely stable over temperature variations, so the digital signal processing which follows the $\Sigma\Delta$ should be able to eliminate the AC gain drift almost entirely. At this time, the calibration circuit has yet to be fabricated so actual measurements of its performance are not yet available; however, given the robustness of the performance demonstrated in the simulation, I am confident that the calibration circuit will perform as intended.

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