Fabrication and Measurement of Lateral-Surface-Superlattice Devices

by

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Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

September 1997

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Abstract

A novel nanostructured device, the lateral-surface-superlattice device (LSSL), has been fabricated and the transport properties measured. The LSSL is similar to a conventional high-electron-mobility transistor (HEMT) with the continuous metallic gate replaced by a periodic metallic gate. The fine pitched (150nm-400nm period) grid-gates, are fabricated using x-ray lithography. New techniques were implemented for contact x-ray lithography and ohmic contact fabrication.

Thesis Supervisor: Terry P. Orlando
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Acknowledgments

I have enjoyed the good fortune of working with many terrific faculty members at MIT. Professor Terry Orlando provided me with my first opportunity at MIT as a TA. Terry has taught me, by his example, the value of professionalism, strong ethics, and consideration of others. Professor Hank Smith introduced me to nanolithography and provided outstanding facilities for me to work in. Hank is a constant source of enthusiasm and motivation, even when the chips are down. Professor Dimitri Antoniadis provided insight, clear thought, and plans of action when needed.

Many of my fellow NSL members have gone beyond the call of duty in assisting me. Anne Pepin graciously introduced me to this project and started me on my way. David Carter has been truly exceptional in answering my barrage of questions and showing me the QEE group's fabrication steps. Tim Savas, Mike Lim, and Juan Ferrera have provided me with constant support and camaraderie. I would also like to thank Jimmy Carter, James Dailey, and Mark Mondol for their assistance.

My officemate, Amy Duwel, has been very supportive, helpful and tolerant. Enrique Trias and Chagarn Whan have offered many insights and enjoyable conversations.

Many people outside of MIT had an important role in this work. I am very grateful for all their help, services, and support. Professor Michael Melloch of Purdue University provided our group with high-quality heterostructures. The wonderful e-beam writing of the mother mask was done by Dr. K. Rhee and Dr. C. Marrian of the Naval Research Laboratory in Washington, D.C. The work presented in this thesis was sponsored by the Air Force Office of Scientific Research.

During the course of my research, I have used an abundance of Gnu Public Licensed (GPL) or otherwise free software. I would like to thank all of the authors for providing such high quality software for free. In particular, I would like to thank Linus Torvalds for the Linux kernel, Richard Stallman founder of the GNU Project and author of Emacs, Donald Knuth for TEX, and Leslie Lamport for LATEX.

I would like to thank my family for their support and understanding. My parents worked hard to raise me well; I have worked hard to show they succeeded. To my family-in-law, the Ellisons, I thank you for accepting me and supporting me along the way.

Finally, I thank my wife, Dana, for her unending love and support. Dana has selflessly sacrificed much of her time and some of her own goals so that I could concentrate my efforts on this work.

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Chapter 1

Introduction

Critical dimensions for VLSI circuits continue to decrease at an amazing rate. The much-celebrated Moore's law observes that the densities of chips have grown exponentially in time. This growth indicates that minimum feature sizes have decreased exponentially; linewidths have been reduced by a factor of two every three years. Figure 1-1 displays this trend. If we are to continue on this path, minimum feature sizes will be below 100 nm by the year 2003.

At these smaller dimensions, there are major obstacles for VLSI technology. The reduced channel length causes short-channel effects, as well high-field effect problems. Other problems arise from the associated problem of ultra-high densities of devices. At these dimensions, an integrated circuit of 1 cm^2 area would contain 50–100 million transistors! The active power of current devices is 10–20 W. As the clock rates increase, and the switching capacitance increases, the active powers will further increase. Besides the active power, each device in a digital system loses some power even when the transistor is in the "off state" due to sub-threshold leakage current. At present circuit densities, the I^2R heating from power losses can be dealt with, but at higher future densities, the heating could become problematic. The ultra-high density issue also poses problems for interconnection of devices. The high density demands extra metalization levels to achieve the interconnects, and the RC delays of long-routed interconnects become a great concern. One trade-off to alleviate the active power problem is to reduce V_{dd}, the power supply voltage, but this further increases the gate delay. For a review of CMOS scaling issues, see Ref. [1]. The ideal solution to these problems is to find a device that operates better at small feature sizes, does not produce large power losses in the "off state", and alleviates the interconnect problem.

One possible alternative to conventional circuits is quantum-effect electronics(QEE). In

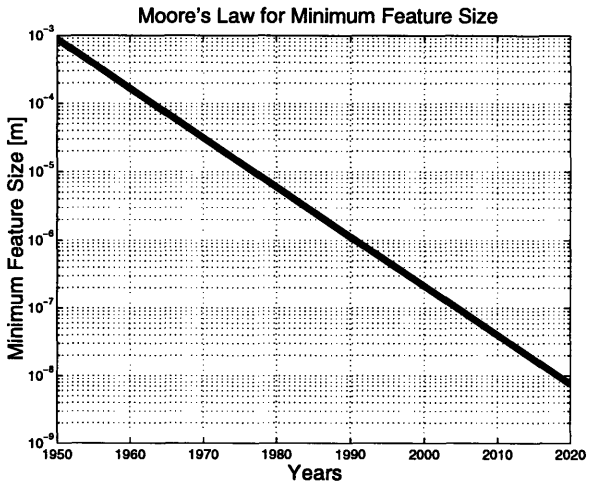

Figure 1-1: Gordon Moore's law shows the exponential decrease in minimum feature size.

general, QEE devices operate on principles based on the quantum nature of matter. The two most important examples are designs which take advantage of charge quantization and the wave property of the electron. Coulomb blockade devices[2] (quantum dot system) rely on charge quantization. Superlattice devices rely on the wave-like nature of the electron. Both types of devices should improve in operations with smaller dimensions. Furthermore, quantum dots can be created in arrays where each dot "communicates" with its neighbors via coulomb interactions. This communication may provide an alternative to metallic interconnects. The lateral-surface-superlattice device (LSSL) can be viewed as a very large array of quantum dots.

Many different quantum-effect computational architectures have been proposed[3]. A common basis for these computational paradigms is that a computation is performed by a large array of interacting quantum dots. In order to design computationally useful quantum dot systems which will have an arbitrary interaction geometry, we have to be able to understand the basic physics of the systems with regular interaction geometry, e.g. the LSSL device.

1.1 Superlattice Devices

The concept of a superlattice was first proposed by Esaki and Tsu[4]. A superlattice device in its simplest configuration is a two-terminal (source and drain) device. While traveling from source to drain, electrons traverse a periodic potential. This periodic potential can be created electrostaticly, by material differences, or via localized persistent photoconductivity

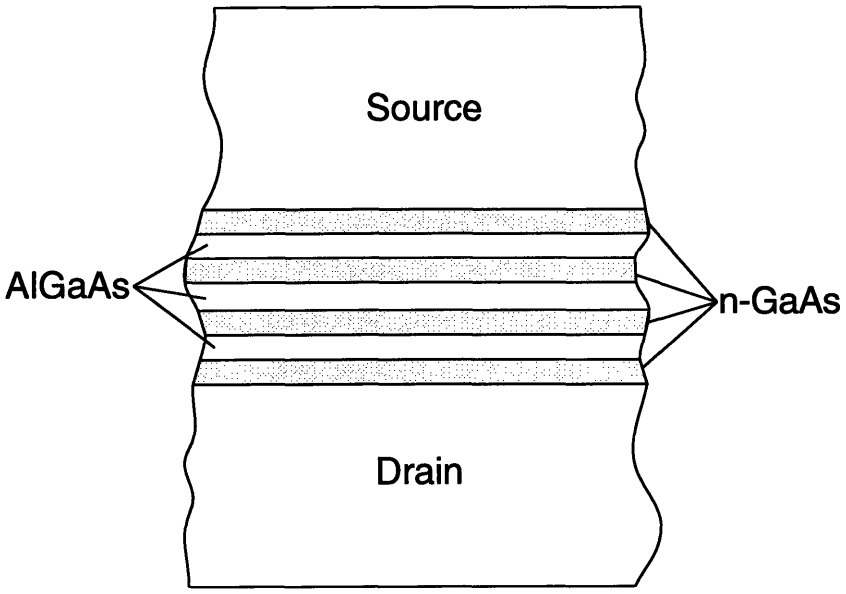

Figure 1-2: Example of a fixed-potential vertical superlattice device.

(PPC) effects. The superlattice device can also be categorized by the direction of transport. In vertical superlattice devices, the transport is normal to the substrate plane. Lateral superlattice devices have transport parallel to the substrate plane, as is common with today's planar fabricated transistors.

The thickness of grown materials can be controlled much better than our ability to pattern lateral dimensions with standard lithographic techniques. Because of this, the first superlattice devices were made using different materials grown in a layered fashion to form a periodic potential[5]. Figure 1-2 shows an example of this device. Although the layer thickness can be controlled very well, there are many disadvantages to this device. First, the strength of the potential modulation is fixed by the materials chosen. For this reason, these types of devices are often called fixed-potential superlattices. Secondly, the vertical growth required to make this device is incompatible with today's planar fabrication technology. Finally, this structure creates only a one-dimensional periodic potential, which is less desirable than a two-dimensional periodic potential as will be explained in Section 1.2.

A lateral-surface-superlattice (LSSL), independently proposed by Sakaki[6] and Bate[7], is created with a periodic potential applied in the plane of the device. These devices have been made in both Si[8] and GaAs/AlGaAs[9] heterostructures. The gate-controlled LSSL device has two distinct advantages over grown superlattices. First, the potential modulation is tunable. If the LSSL is viewed as an array of quantum dots, then this has the effect of

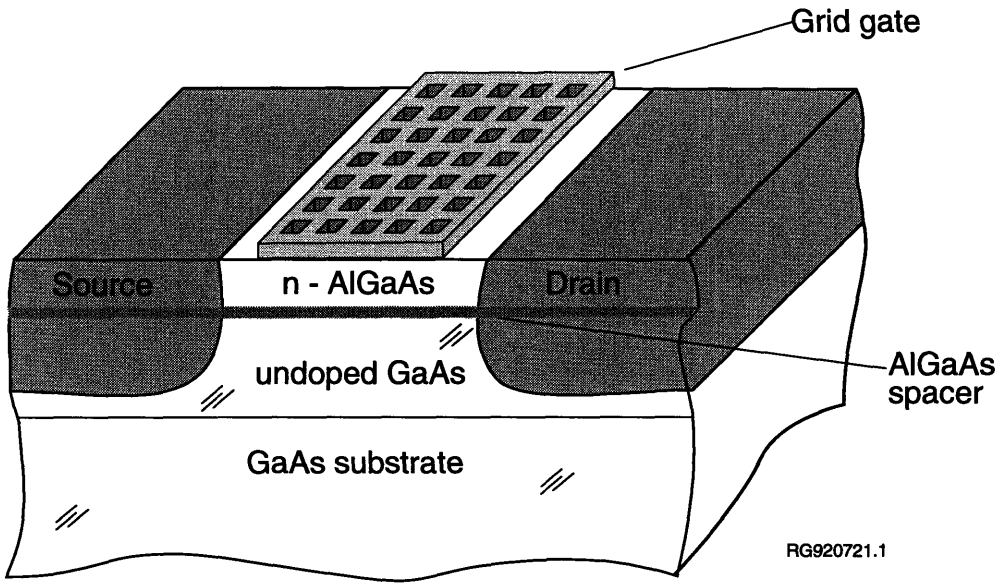

Figure 1-3: Schematic of a lateral surface superlattice device created with a gate over a 2DEG.

controlling the coupling between dots. Second, it is possible to create a two-dimensional periodic potential in the lateral device, compared to the one-dimensional potential of the grown vertical superlattice. By creating the potential in the second direction, the effects of electron back-diffraction are greatly enhanced.

The periodic potential can also be created by etching the heterostructure to form potential modulation. Like the vertically-grown superlattice, this structure has the disadvantage that the strength of the modulation is not tunable. Another alternative is to spatially modulate the electron density by using the PPC effect[10]. The Si dopant in the heterostructure creates some deep donor levels. These levels trap electrons from the 2DEG at low temperatures. The trapped donors can be ionized by the presence of light, and once ionized, they remain ionized. By using holographic illumination techniques, a spatially modulated photon flux can create a periodic potential. The disadvantages of this method are the need for *in situ* holographic illumination techniques and the weak potential modulation (at best, around 1meV [11]).

1.2 Superlattice Physics

The period of the imposed potential is large compared to atomic distances so we may employ the effective mass theorem[12] to determine the effects of the applied potential. We need to

solve the Schrödinger equation for the applied periodic potential. The well-known result to this problem is the formation of bands and band gaps. Because we have used the effective mass theorem, these bands and bandgaps are superimposed on the band structure of the material.

The effect of these mini-bandgaps depends on the dimensionality of the system. The electrons are confined in the z-direction because of the heterostructure (see Section 2.1), leaving 2 degrees of freedom. In the case of a one-dimensional applied potential, there are no true bandgaps in a two-dimensional system because at all energies there are some available states. Having a two-dimensional applied potential allows for, but is not sufficient to cause, true bandgaps. The applied potential must be strong enough to open the bands for all k. Figure 1-4 shows $E(k)$ for a weak and strong two-dimensional potential. Note that in the case of the weak potential, states exist at all energies, although there is a decreasing density of states near the region where the expected band gap would be. In contrast, the strong potential has a true bandgap where no states exist for a range of energies. It can be shown that the n^{th} band opens up only if

$$V > \left(\frac{\hbar\pi n}{P}\right)^2 \frac{1}{4m^*e}$$

where V is the applied potential and P is the period of the grid[13].

The novel properties expected in this device arise from these mini-bandgaps. If we picture the gate bias as raising the Fermi level, then when the Fermi energy reaches one of the mini-bandgaps, conduction should go to zero. Furthermore, if the source drain bias is made large, theory predicts Bloch oscillations[14]. However, this theory assumes that the electrons stay within one band, and that the scattering time is much longer than the time required for the elctron to traverse the full range of k_x-space (i.e. a full cycle of back-diffractions.)

1.3 Review of LSSL Experimental Results

The LSSL has shown many novel features. Electron back-diffraction has clearly been seen in the low-field (low source-to-drain bias) regime[8, 9, 15]. However, others have attempted to make LSSL devices and have not seen electron back-diffraction effects[16, 17].

In the high-field regime (high source-to-drain bias), negative differential conductance (NDC) has also been seen. Negative differential conductance has many possible sources: Bloch oscillations, Gunn effect, real space transfer, and sequential resonant tunneling.

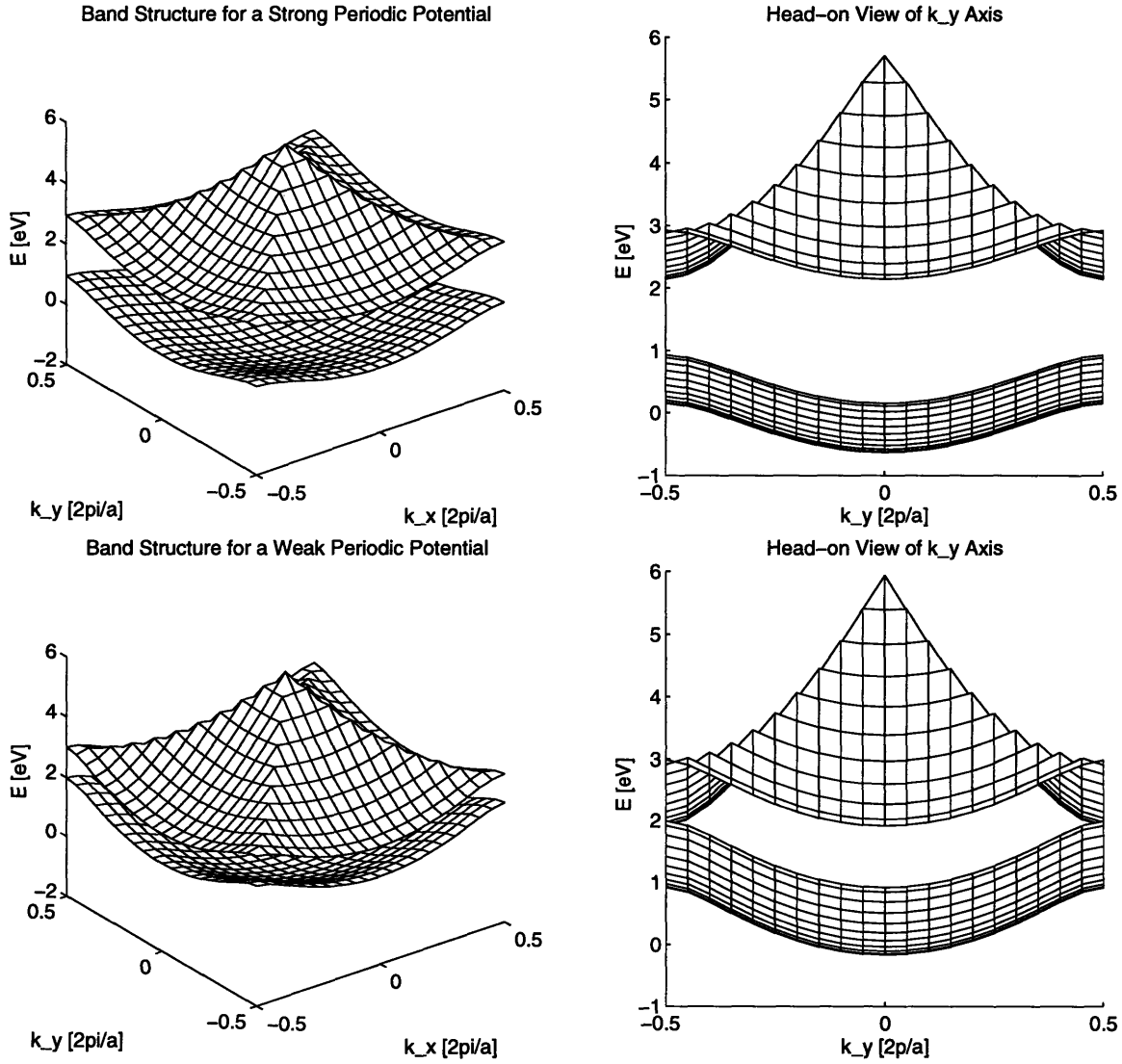

Figure 1-4: Example of the mini-bandgaps created by a strong (top pair) and weak (bottom pair) two-dimensional periodic potential. The head-on view of the k_y axis shows that there is a true gap only for the strong potential band structure.

Ismail[9] has seen NDC in a regime where Bloch oscillations were possible, and the fields were such that the Gunn effect and real space transfer are not possible. Due to the extreme sensitivity of the NDC to the gate bias, Ismail explained the results in terms of sequential resonant tunneling. Bernstein and Ferry[18] also reported NDC and attributed it to Bloch oscillations, but the fields used in their measurements were high enough to possibly allow interband transitions and real space transfer. Recent reports[16] have challenged the existence of NDC. The wide range of reports and explanations indicate that more research needs to be conducted in this area to gain greater understanding of this phenomena.

Chapter 2

Fabrication

The challenges of making LSSL devices are numerous. The first challenge is to obtain suitable material. The LSSL device depends directly on the wave-like properties of the electron. To see the predicted effects, the electron waves must remain coherent over several periods of the LSSL. If the length of the device is greater than the inelastic scattering length, device operations will be degraded by energy broadening[19].

The second challenge involves the stringent requirements on lithography. For the device to operate properly, the period of the potential must be small so that thermal smearing does not dominate the sought-after effects[19]. Even at 4 K, this requires periods below 400 nm. In our design, we have chosen periods as small as 150 nm. To fabricate these devices, we have used x-ray lithography because of its ability to produce fine dimensions and because of its robustness.

2.1 Device Material

The LSSL devices are made on a GaAs/AlGaAs heterostructure grown by Professor M. Melloch at Purdue University. The heterostructure is shown schematically in Figure 2-1.

Ignoring the AlGaAs spacer and GaAs cap for the moment, the heterostructure is n-AlGaAs grown on top of nominally undoped GaAs. The n-AlGaAs layer is a doped, wide-bandgap material. The bulk GaAs layer is undoped and small bandgap. Growing these materials on top of each other causes a conduction-band discontinuity between the wide and narrow bandgap materials. Electrons from the doped material diffuse to the undoped material until the resulting field retards further diffusion. This results in a "sheet" of electrons underneath the doped material. These electrons "see" a nearly-triangular potential

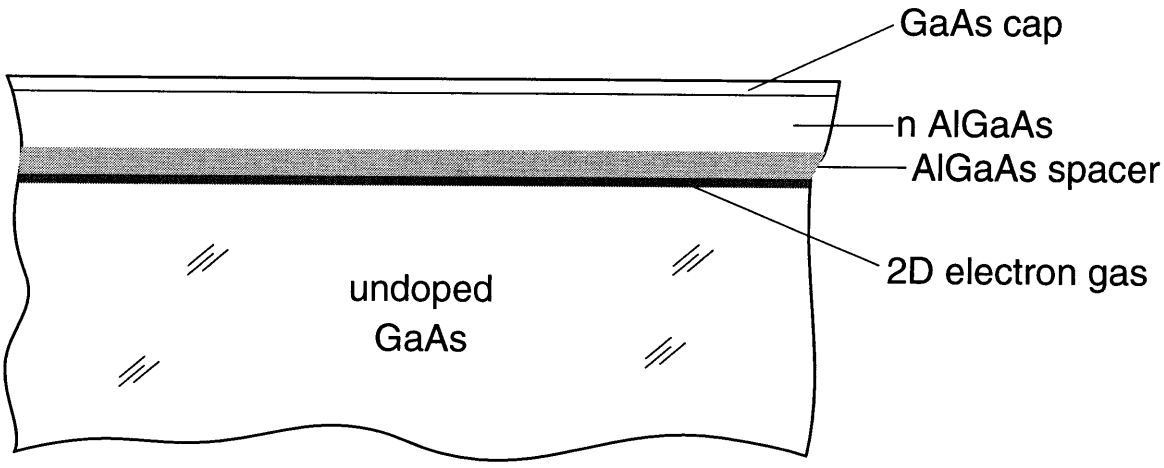

Figure 2-1: Schematic of the MBE-grown GaAs/AlGaAs heterostructure used.

well. At low temperatures, the electrons are in the ground state of this triangular well, however the tails of their wave functions do extend into the doped AlGaAs region. This allows the electron wave functions to scatter off the dopant impurities. In order to reduce this scattering, an undoped AlGaAs "spacer" layer is placed between the AlGaAs layer and the GaAs layer.

Although the spacer layer improves mobility, there is an important trade-off. The 2-DEG must be close to the surface of the wafer so that the potential from the gate is not smeared out. At the same time, we want the 2-DEG to be located far from the doped layer to reduce scattering. The material we used had a 15nm spacer layer and the 2-DEG was approximately 55 nm below the surface.

By numerically solving Poisson's equation, the conduction band edge relative to the Fermi level can be found for the heterostructure. Figure 2-2 shows the results of using a two-dimensional Poisson solver developed by Arvind Kumar to simulate the heterostructure. For this heterostructure (label MBE33), the 2-DEG is 55nm below the surface of the wafer.

2.2 Ohmic Contacts

In past efforts, our group has had inconsistent results with ohmic contacts. It is believed that the poor ohmic contacts resulted from electron induced damage during electron-beam evaporation of metals. To reduce this damage, we have switched our metalization process to a thermal evaporater.

The thermal evaporater was modified to allow a third source in order to make ohmic

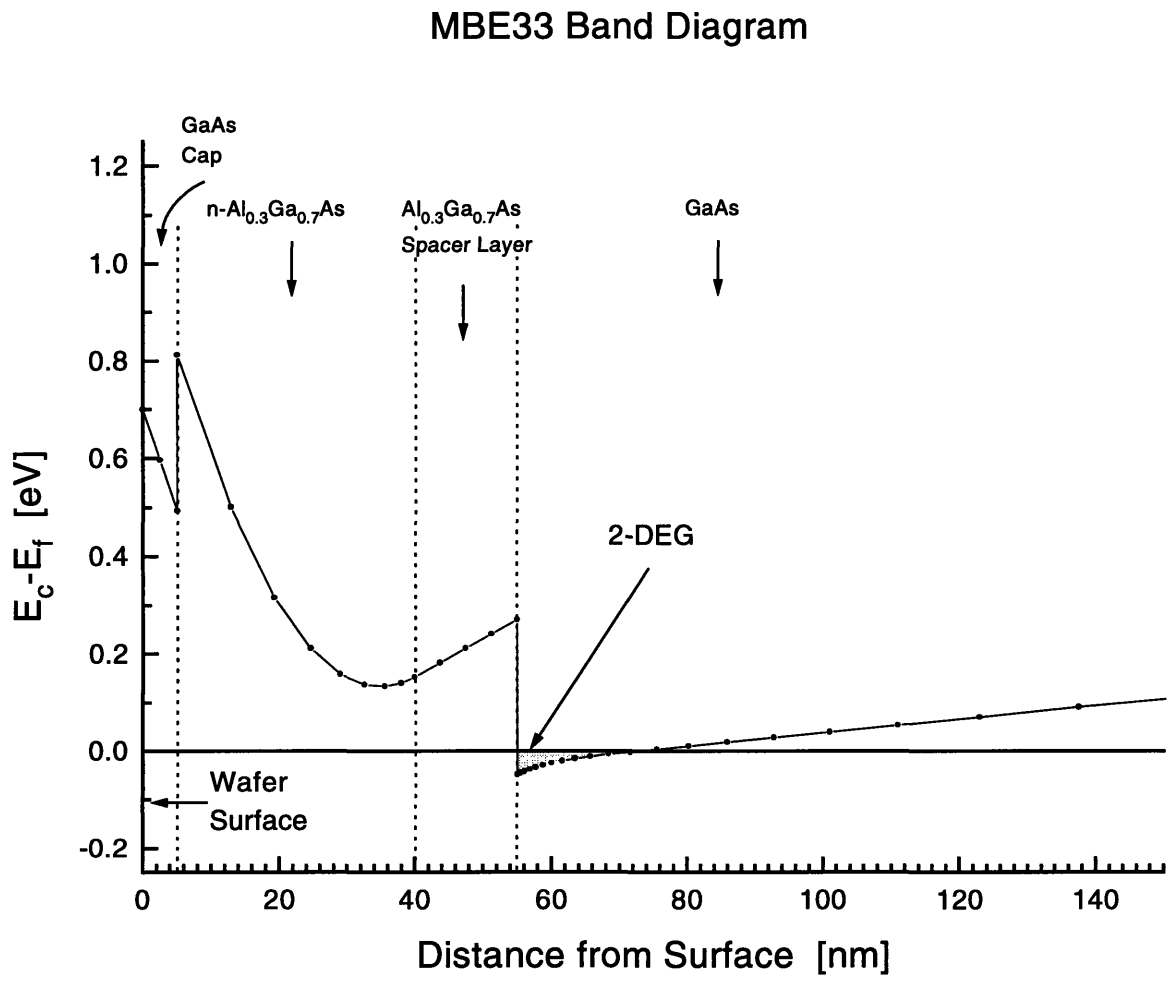

Figure 2-2: Conduction band edge relative to the Fermi level for the heterostructure used. Note the area under the abscissa is populated by free electrons.

contacts. Our ohmic contacts are made of the following metal layers: Ni/Ge/Au/Ni/Au (5/60/120/30/30 nm). Each source has a stainless steel barrier between it and its neighbor to prevent cross-contamination of the evaporants. A double-shielded shutter was installed to reduce radiative heating of the substrate.

Thermal evaporation for ohmic contacts presents a few difficulties. First, it is very difficult to evaporate nickel. In a thermal evaporater, the metal to be evaporated is placed in a "boat". The boat is a metal, either tungsten or molybdenum, with a recessed cavity to hold the sample. The boat is heated by applying a current through it. Nickel is quite corrosive and readily destroys both tungsten and molybdenum boats. For this reason, it is necessary to use boats that have an Al_2O_3 barrier in the recessed areas that hold the molten nickel. Unfortunately, this barrier also reduces thermal conductivity, thus increasing the power required to melt the Ni. The high temperature needed to evaporate nickel demands that a double-shutter system be used to reduce radiative heating of the substrate.

In the case of gold and germanium, once molten, the metal tends to spread out "wetting" the entire boat. In order to lift-off the metal, it is highly desirable to have a point source for the evaporation. Using an Al_2O_3 covered boat solves this problem as well. The evaporant tends to ball up, rather than "wet", on an Al_2O_3 surface, thus providing a very small source size.

Occasional boat breakage was also a problem with thermal evaporation. A standard boat is only reliable for one run. Upon cooling, the boat would usually break. This can be alleviated by using boats that have small, rippled folds in them[1]. The folds allow for expansion and contraction during temperature changes and reduce the likelihood of the boat breaking.

After the material was deposited for the ohmic contacts, the samples were annealed on a strip heater at 425 °C for 30 s. in "forming gas" (97% N_2, 3%H_2.) Details of the new strip heater and its usage can be found in Appendix B.

2.3 X-ray Lithography

In order to produce the fine lines required for the LSSL device, advanced lithographic techniques were required. Only electron-beam, x-ray, and ion-beam lithography are capable of producing the required feature sizes. Electron-beam and ion-beam lithography increase the risk of damaging the substrate. Furthermore, direct write e-beam lithography suffers from

[1]R. D. Mathis boat #S35B-AO-W modified to 4.5" overall-length works well.

feature broadening due to backscattered electrons and proximity effects. x-ray lithography has been shown not to induce any damage to the substrate[20], is very robust, and provides a large process latitude.

In our experiments, Cu_L x-rays with wavelength of 1.3 nm were used. This wavelength is sufficiently small compared to our desired feature size to allow faithful replication. The limiting factor for resolution is diffraction in the mask—sample gap. The maximum gap that can be tolerated is given by

$$G \leq \alpha W^2/\lambda$$

where G is the gap, α is a scaling factor, W is the minimum linewidth desired, and λ is the radiation wavelength. As an example, to print 25 nm lines with $\lambda = 1.3$ nm and $\alpha \approx 1$, the gap must be less than 480 nm. In some case, α can be as large as 1.5 or even 2.

2.3.1 Mother Mask

In x-ray lithography, a parallel process, one must use a mask to allow x-ray irradiation only in the desired areas. An x-ray mask is shown schematically in Figure 2-3. The materials used in the mask are chosen based on their x-ray absorbency. SiN_X has very low x-ray attenuation ($\approx 3\,dB/\mu m$) and Au has a very high attenuation ($\approx 50\,dB/\mu m$), at $\lambda = 1.3$ nm. The absorber pattern in Au, plated to a thickness of 200 nm, provides a contrast of 10 dB or 100:1 in transmitted power. In addition, 200 nm of Au provides nearly a π phase shift in the transmitted radiation at 1.2 nm. This has the advantage of reducing diffraction effects and improving the edge slope of the aerial image.

The original mask must be patterned by one of the other possible technologies (e-beam or ion-beam lithography). Electron-beam lithography is an ideal candidate. Because the mask is a thin (1 μm) SiN_X membrane, there is very little pattern widening from back-scattered electrons. Electron-beam lithography is a serial process requiring very long writing times. In order to reduce the writing time, the mask is written in reverse polarity so that only the features themselves are written. The large blank areas can be skipped, yielding a "clear-field" mask. The polarity of the mask is switched during the "daughtering" process (i.e., copying the clear field mask onto a second mask.)

To create the original mask, plating base is evaporated on the SiN_X membrane. This allows the features to be electroplated on the mask after patterning. Polymethylmethacrylate (PMMA) is then spun on the mask. The mask is sent to the Naval Research Laboratory electron-beam lithography facility where the pattern is written on the mask. Upon completion, the mask is returned, the PMMA is developed, and the Au absorber is electroplated

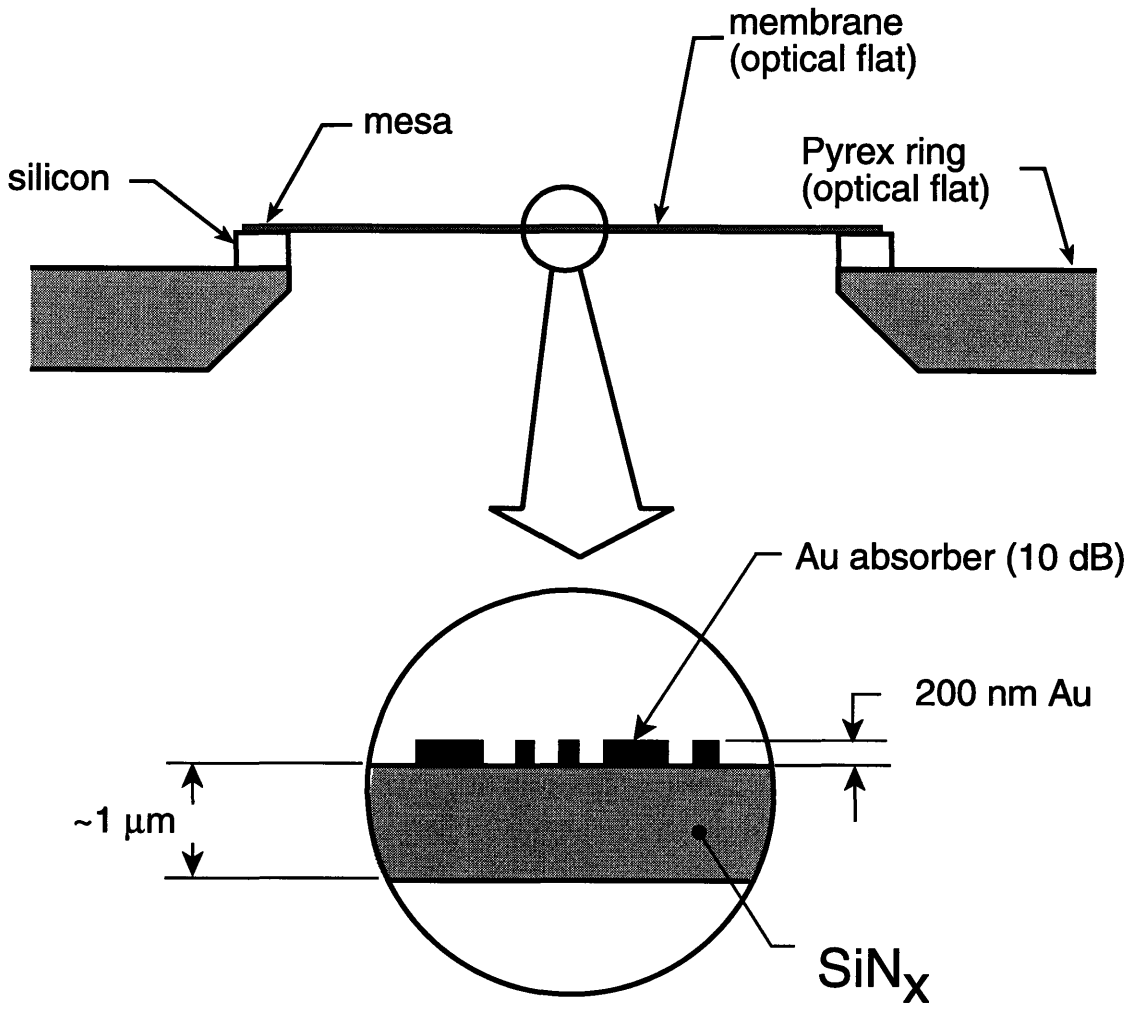

Figure 2-3: Schematic of the MIT mask used for x-ray lithography.

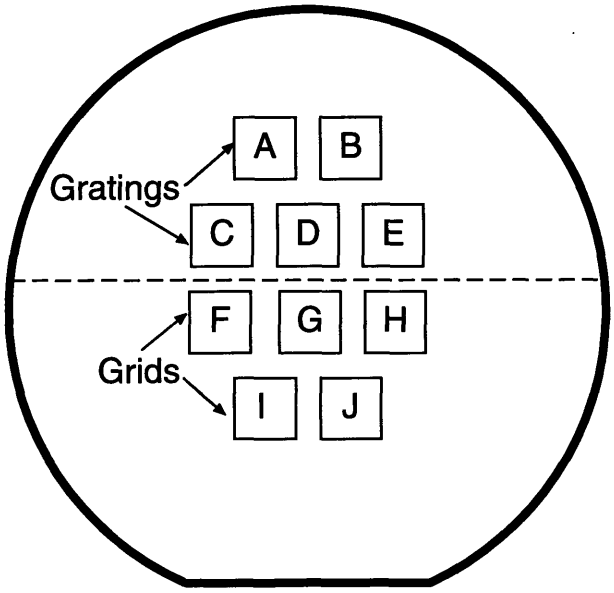

Figure 2-4: Diagram of the location of dies on the mother mask. Letters correspond to doses in Table 2.1.

(see Appendix A for details).

The fine lines creating the grids are written in a single pass to produce the narrowest possible lines. This makes development difficult: underdevelopment will result in no lines, overdevelopment will result in a solid gate. To remedy this difficulty, each die is written at five different doses. Development is then performed for a fixed amount of time. The die that comes out the best is used for actual device fabrication. The die/dose pattern on the mask is shown in Figure 2-4. Figure 2-5 shows the layout of an individual die.

The linewidths achieved for various doses are shown in Table 2.1. In general, smaller doses produce finer patterns. However, some of the smallest doses were insufficient to clear the pattern. The general trend also shows, for a given dose, the linewidths are smaller for larger period grids and gratings. This result is caused by proximity effects from back-scattered electrons when writing the mask. Regions of higher pattern density receive a greater contribution of back-scattered electrons than sparse areas. Although this is undesirable, the effects from writing on a thin membrane are much less than the effects from directly writing on a thick substrate. There are some inconsistencies from the general trend noticed, and for the grating devices these seem to be related to whether the device was oriented horizontally or vertically. This indicates that there may have been a slight astigmatism in the beam. The fine-line patterns are written at a current of 15 pA with a corresponding beam diameter of ≈ 10 nm.

Die Number	Period nm	Dose nC/cm	Linewidth nm
Grating B	150	1	61
Grating B	300	1	40
Grating C	150	1.5	68
Grating C	200	1.5	56
Grating C	300	1.5	59
Grating C	400	1.5	51
Grating D	150	2	74
Grating D	200	2	73
Grating D	300	2	65
Grating D	400	2	77
Grating E	150	2.5	73
Grating E	200	2.5	82
Grating E	300	2.5	56
Grating E	400	2.5	56
Grid F	200	2.5	50
Grid F	300	2.5	45
Grid F	400	2.5	55
Grid G	150	2	60
Grid G	200	2	50
Grid G	300	2	42
Grid G	400	2	50
Grid H	150	1.5	50
Grid H	200	1.5	38
Grid H	300	1.5	35
Grid H	400	1.5	33
Grid I	150	1	25

Table 2.1: Linewidths achieved on a daughter mask given the mother masks's e-beam dose.

Note that this data was actually taken by measuring the daughter mask. The mother mask was slightly overplated by about 10 nm. Once the Au was plated above the height of the PMMA, it is no longer confined to the PMMA mold. This causes the tops of the features to "mushroom." Because of the "mushroom" caps, it was not possible to directly measure the linewidths on the mother mask. Although the caps extend the feature size on the mother mask, the caps are thin ($\approx$10 nm), and do not significantly change the aerial dose when daughtering. Therefore, the caps are not imaged in the replication process.

The grid devices are achieved by writing a series of lines in one direction, then writing the perpendicular series. This causes the area of intersection to receive twice the dose of the normal line. Thus, the grid has rounded corners (see Figure 2-9). To avoid this effect, the

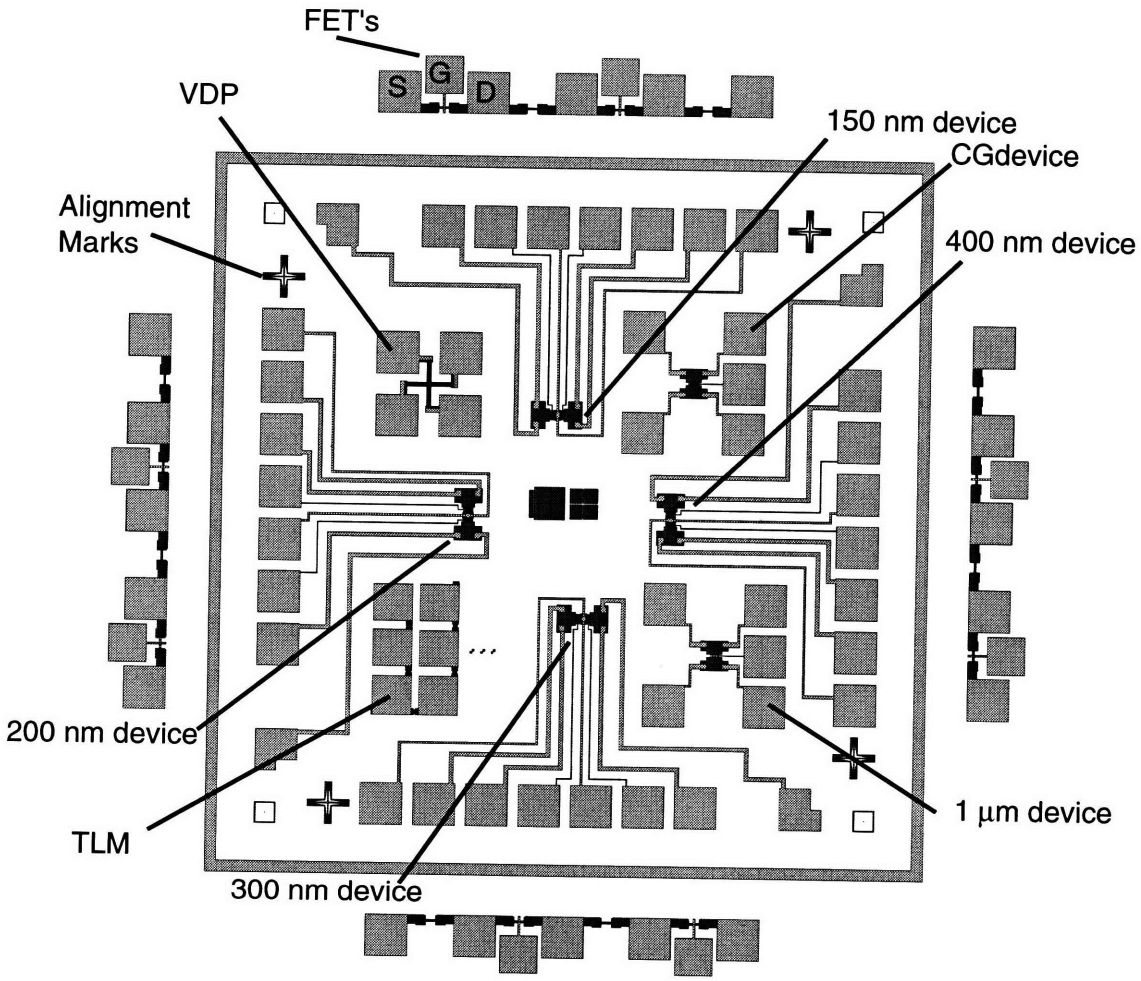

Figure 2-5: Pattern for a single die. Four devices with periods of 150, 200, 300, and 400nm periods are at the center. Test devices with 1μm and continuous gates are to the right. VDP and TLM structures are on the left.

overlap region should only be written once, thus one of the lines should be broken. The size of the break depends on the beam diameter and proximity effects. A program to generate a `Kic` file for experimentally determining the optimum break size and orientation is presented in Appendix C.

2.3.2 Daughter Mask

The use of a daughter mask is desirable for two reasons. First, as discussed above, the mother mask is written in reverse polarity to reduce writing time. Second, in the event that a mask is damaged during device processing, another mask can be made quickly if the mother mask is available. This is a considerable advantage; shipping, writing, and receiving an e-beam written mask takes approximately one week, whereas daughtering a mother mask via x-ray lithography takes approximately one day.

The process of daughtering masks has been successfully performed by our group for many years without noticeable problems. However, as the minimum feature size has been shrinking, we have noticed significant problems with daughtering. Figure 2-6 shows a schematic of the observed undercut in the PMMA profile. Once the mask is electroplated, the undercut PMMA feature becomes a protrusion in the gold patterns. The undercut can be attributed to two separate mechanisms. Figure 2-6 shows the one-dimensional effect. Here, the absorber material is not perfect, and some radiation passes through. The photons absorbed by the plating base (Au) emit many photoelectrons. These photoelectrons dose the PMMA near the substrate. Overdevelopment allows lateral development of the PMMA along this thin layer of exposed PMMA.

Even if the absorber perfectly attenuates the radiation, we will still have an undercut near the pattern edge. Figure 2-7 shows the two-dimensional photoelectron effect. Here, the absorber is assumed perfect. Radiation that is absorbed in the plating-base gives off photoelectrons. For the x-ray spectrum used in our experiments, the range of these photoelectrons in PMMA is around 40nm. Therefore, x-rays absorbed near the pattern edge emit photoelectrons into the dark region, thereby exposing the PMMA. The range of exposed PMMA is nearly the same as the range of the photoelectrons.

In either case, after gold electroplating, the desired features we expected had a "foot" added to them. This foot arises from the gold electroplating into this undercut region. In the case of very finely-pitched features, it is possible that the PMMA feature could be completely undercut. This allows for complete electroplating underneath the feature, and the result is a solid Au pattern. Figure 2-8 shows an example of an unsuccessful daughtering

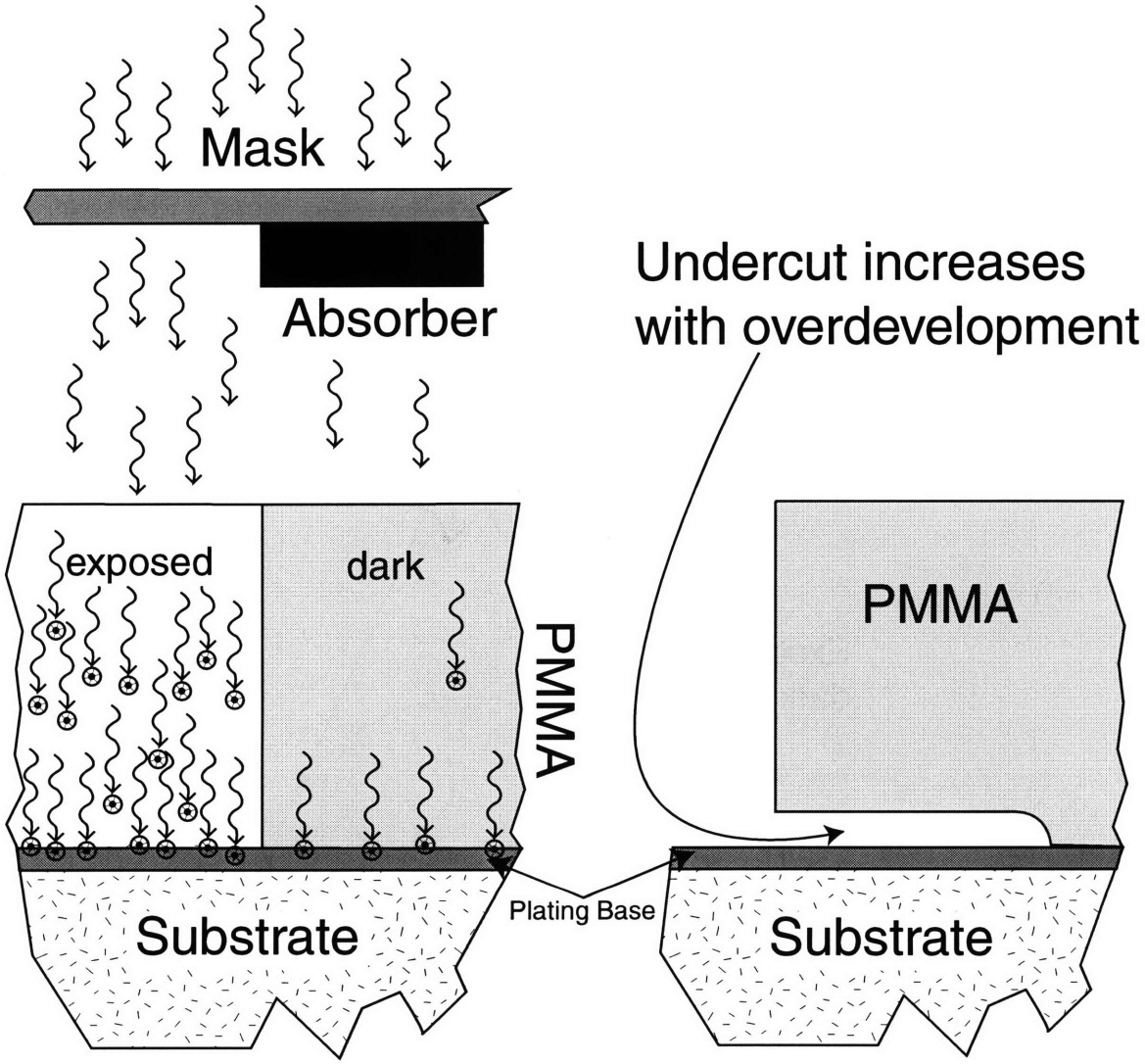

Figure 2-6: The one-dimensional foot problem. A thin sheet of PMMA near the substrate is exposed under the absorber pattern

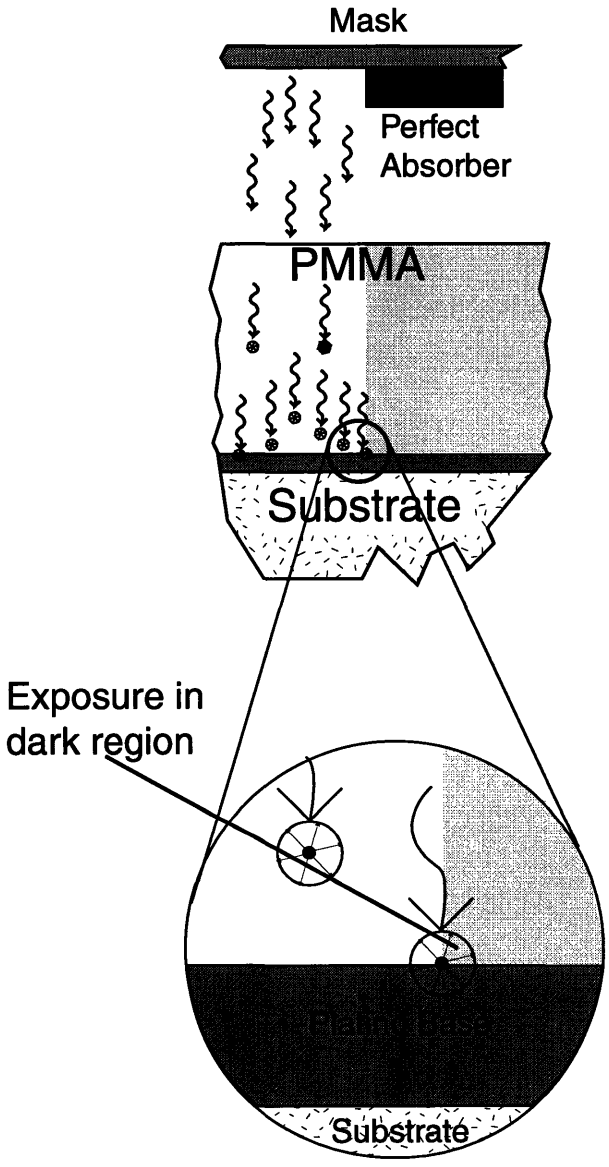

Figure 2-7: The two-dimensional foot problem. The finite range of the photoelectrons near the pattern boundary expose the resist in the dark region.

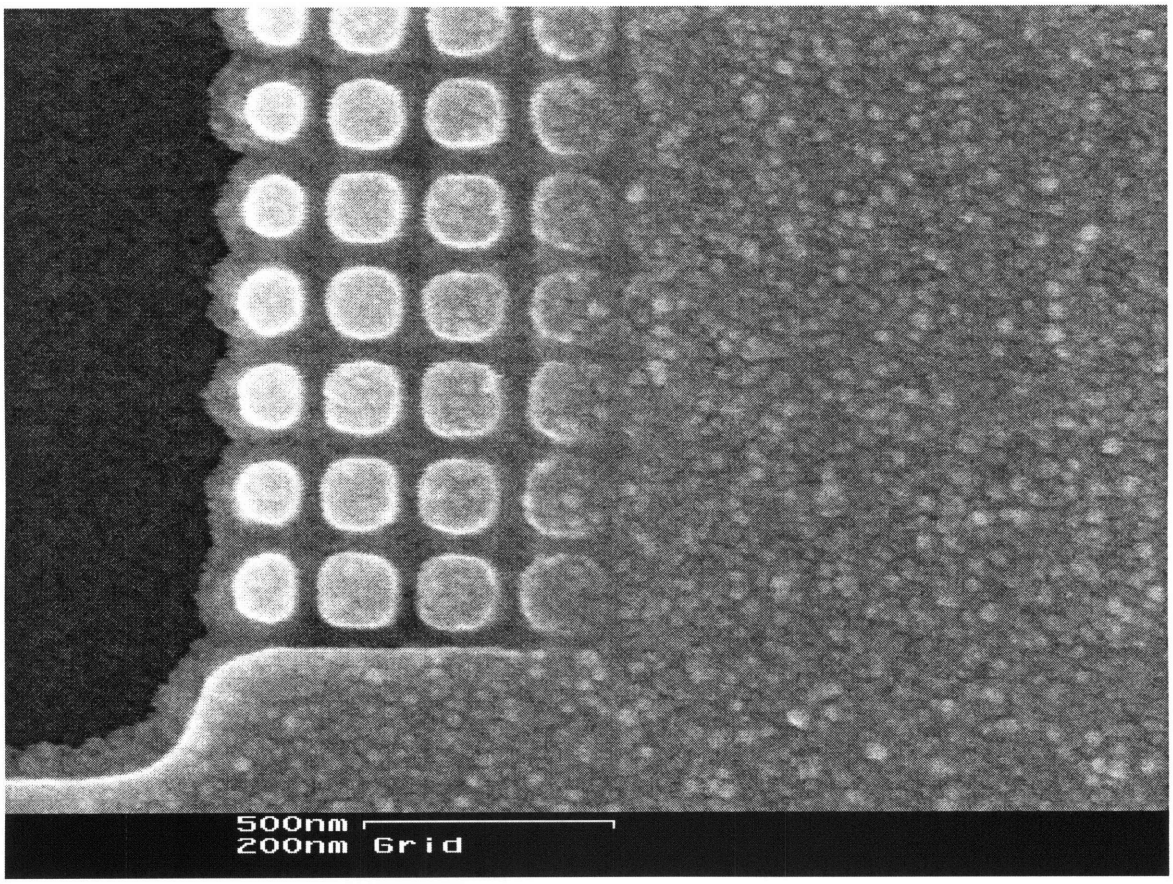

Figure 2-8: Daughter mask showing a "foot." The entire area to the right should be a grid. It has been plated solid because the PMMA mold was completely undercut.

attempt where the foot has destroyed the grid entirely.

Similar exposure experiments by David Carter[21] on Si substrates rather than on another x-ray mask did not reproduce the observed foot. This indicated the problem was substrate specific. The gold plating base has much stronger absorption of x-rays than does a silicon substrate. Correspondingly, the plating base dumps many more photoelectrons into the PMMA.

The solution to this problem was to reduce the thickness of the gold plating base. Since the photoelectrons have a finite range in the gold plating base, changing to a thicknesses of Au above this range will not effect the resulting undercuts to the PMMA. Therefore, we had to reduce the thickness significantly below this range to reduce the effects of photoelectrons. By switching from 10 nm to 1.7 nm of gold, the problem is eliminated. Figure 2-9 shows a successful daughtering of the same mother mask using the thin plating base.

2.3.3 Contact Daughtering

As mentioned in Section 2.3, to replicate 25 nm lines, the mask-to-substrate gap has to be less then 500 nm. One way to control gap is to evaporate studs onto the mask to provide spacing between the mask and substrate. In order to adjust the gap, and to monitor its stability, one can measure the capacitance between the mother and daughter masks. This can then be used as a feedback to control the vacuum between the masks. In practice however, this proved difficult because the masks would often electrically short, removing the feedback control. Furthermore, the gap at the center of the membrane differs from the gap at the edges, reducing the gap uniformity across the entire mask.

To minimize the gap and to simplify control, the mother mask can be placed in intimate contact with the daughter mask. Because PMMA outgasses during exposure, a gas-relief structure must be provided. This was done by patterning a thin layer of polyimide on the mother mask. A two-layer coating was used. The first layer of polyimide, approximately 250 nm thick, was used to protect the mother mask and cover the absorber pattern. A second layer, approximately 70 nm thick, was patterned with a 20 μm-period grid to provide gas relief channels.

The masks were then placed into a vacuum contact fixture. This fixture allows a vacuum to be pulled in the volume between the mother and daughter mask membranes. Vacuum is applied to the inlet to pull the masks in contact, and is continuously applied during the exposure to ensure they stay in contact. Typical pressures used were 4–5 in. Hg. As the needle valve is opened, nothing noticeable happens until the gauge reads approximately

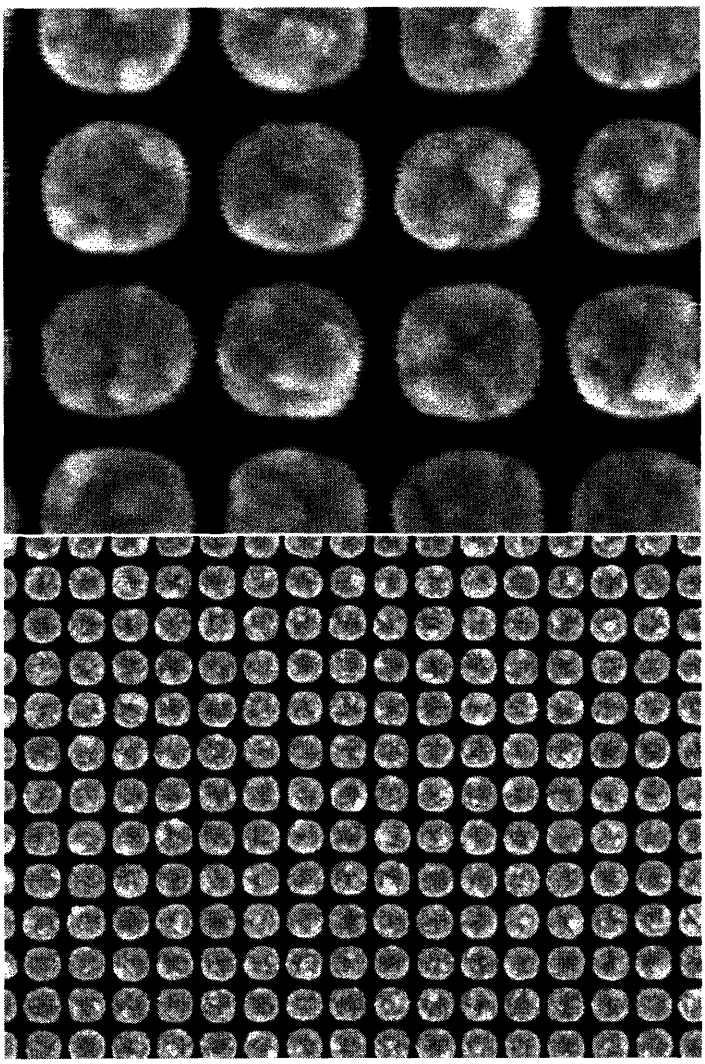

Figure 2-9: SEM of a successful daughtering attempt with thin plating base. The period of the grid is 150 nm. The spacing between gold posts is 25 nm. The top figures shows a magnified view of the fine features. The bottom figure shows a large-area view of the same grid.

1.6; then the masks quickly begin to come into contact. It is very important to use a monochromatic light source, which reflects from the two mask surfaces, to examine the interference fringes and ensure they are not wedged. Wedging may overstress one of the membranes. After the exposure, the masks are removed from contact by applying N_2 to the inlet. The use of a nitrogen gun, with the pressure set to 8–10 PSI, worked successfully in all cases.

2.4 Device Exposure

Once a suitable daughter mask has been made, the device itself must be fabricated. As explained in Section 2.3, we require a very small gap to replicate the fine lines. As with daughtering the mask, this is accomplished with contact exposure. Because of the high cost of the heterostructures, we break the original wafer into small pieces, $\approx 4\,\text{mm} \times 4\,\text{mm}$, about the size of a single die. The small dies size precludes using the vacuum techniques for putting the chip in contact with the mask. Instead, the chip is brought into loose contact by physically pressing it against the mask. An electrostatic potential is then applied to draw the mask and chip into intimate contact. The bias needed to achieve contact varies greatly. The two most important factors are the resistivity of the substrate material, and how level the mask is to the chip. Once in contact, the potential can be removed and the substrate stays in contact with the mask, presumably due to van der Waals force and possibly residual electrostatic forces.

2.5 Metalization

After the exposure, the PMMA is developed and monitored via AFM measurements. One difficulty is that monitoring large-area pads is not indicative of the development of small area features. There are several possible explanations of why this is so. First, the dose may not be the same in large areas as small areas. This might occur if there is a large amount of ultraviolet (UV) radiation produced by the x-ray source. Another possibility is that the development process itself is not uniform with varying pattern density. It is suspected that in very small features (sub 50 nm), development is limited by transport of the solvent and solutes into and out of the fine channels. Experimental observation also indicates that dose and development time can not be traded off as one might expect. In trying to obtain suitable PMMA profiles for lift-off, it was discovered that overdosing the sample and shortening the exposure time produced better results.

The sample is mounted in the thermal evaporater, and AuPd is evaporated onto it, typically to a thickness 60 nm. Lift-off is performed in hot 1-Methyl-2-Pyrrolidinone (NMP) ($\approx$ 90 °C.) Although lift-off is possible in acetone, and has been the primary lift-off solvent used in our group, hot NMP produced remarkably-better results. It was also found that ultrasonic agitation was necessary to complete the lift-off of fine features (caution is warranted here since extended ultrasonic agitation can rip fine features off the substrate completely.) Another method that works well is to use an air-brush filled with acetone. The acetone is sprayed onto the sample at high velocities (extreme caution is warranted here since a solvent spray can be explosive.) It is imperative that the sample never be allowed to dry during this technique. As with ultrasonic agitation, over-vigorous use can rip fine features from the substrate.

Chapter 3

Device Measurements

3.1 TLM Measurements

Since we had developed a new procedure for fabricating ohmic contacts, it was important to be able to measure the quality of the contacts. To do this, transfer-length-method (TLM) structures were fabricated on the heterostructure. The TLM structure is shown in Figure 3-1. This structure allows one to measure the resistance between two ohmic contacts, with a variable length (l) of 2-DEG in between. Our TLM structure provides $l = 5, 8, 10, 12,$ and $15\,\mu$m. Assuming that the resistance from the contacts is the same for all contacts, the only difference is the resistance due to the length of 2-DEG. We can simply model the resistance between two adjacent pads as:

$$R_t = 2R_C + \frac{l\,\rho_s}{W}$$

Where R_t is the total resistance between pads, R_C is the resistance of a single ohmic contact, ρ_s is the sheet resistance of the material, l is the length of 2-DEG, and W is the width of the mesa structure. With this linear model, the contact resistance can easily be found from the y-intercept of R_t versus l, and the sheet resistance can be found from the slope.

The QEE group's past experience with ohmic contacts showed that some would freeze-out at 4K. In general, if the contact resistance looked good at 77K, it was also fine at 4K. The value of contact resistance is not of paramount importance as long as it is not prohibitively large. Table 3.1 shows the results of these measurements.

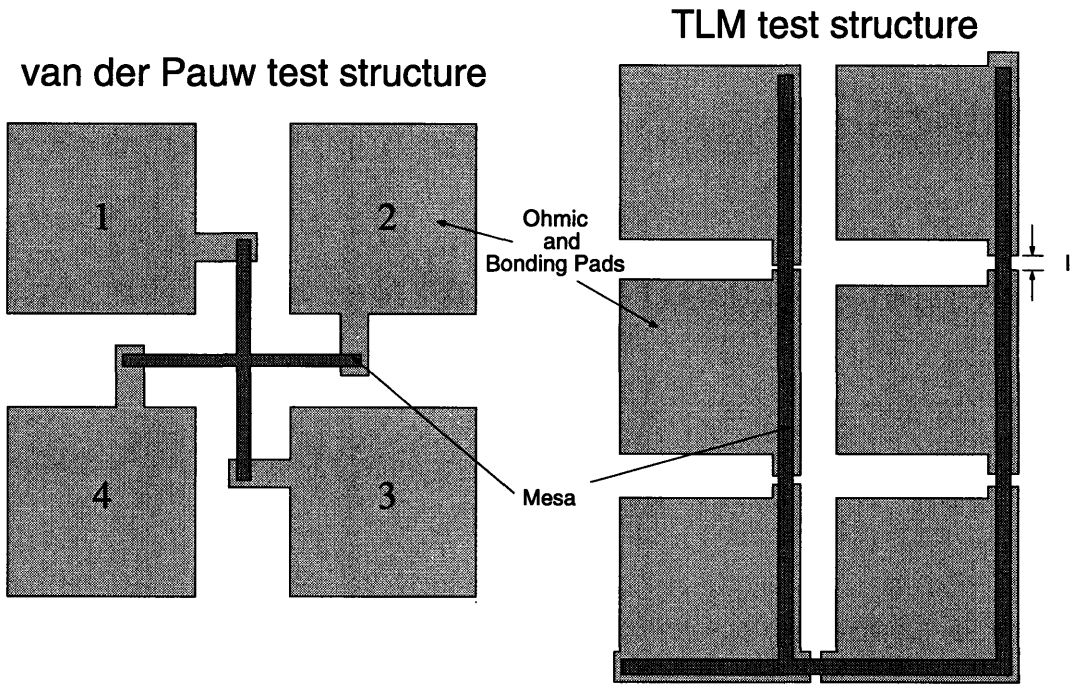

Figure 3-1: Transfer length method (TLM) test structure used to measure contact resistance and sheet resistance. Also shown is a van der Pauw structure for measuring resistivity, carrier concentration and mobility of a 2-DEG.

Heterostructure	Temperature K	R_C $\Omega \cdot$ mm	ρ_S $\Omega/\square$
MBE 33	295.0	1.45	1936
MBE 33	4.2	1.83	39
MBE 30	295.0	1.27	1628
MBE 30	90.0	0.55	193

Table 3.1: Contact resistance (R_C) and sheet resistance (ρ_S) for heterostructures MBE 33 and MBE 30.

3.2 Hall Measurements

Because the LSSL devices require phase coherence across the channel, it is important to know the inelastic scattering length in the material. The van der Pauw(VDP) test structure allows measurement of resistivity, carrier concentration, and mobility. From these measurements, the elastic scattering length (mean-free-path) can be calculated, placing a lower bound on the inelastic scattering length.

The sheet resistance is calculated in the absence of a magnetic field and is given by[22]:

$$\rho_s = \frac{\pi}{\ln(2)} \frac{R_{12,34} + R_{23,41}}{2} F$$

where $R_{12,34}$ is defined as V_{34}/I_{12} (see Figure 3-1 for the contact numbering) and F is a geometrical scaling factor. For symmetrical VDP structure, $R_{12,34} = R_{23,41}$ and $F = 1$. The sheet resistance is then simplified to:

$$\rho_s = \frac{\pi}{\ln(2)} R_{12,34}$$

In order to reduce errors and account for slight asymmetries, the measurement should be performed twice, permuting the sets of contacts. Furthermore, our measurements average the results from the use of two different currents, $I_1 = 50\,\mu$A and $I_2 = 100\,\mu$A. The results of these measurements one MBE 33 yield a sheet resistance $\rho_s = 49\Omega/\square$, slightly higher than the TLM results.

To find the Hall mobility, a magnetic field is applied perpendicular to the plane of the test structure. The Hall mobility for symmetrical VDP structures is then defined as[23]:

$$\mu_h = \frac{V_{42}}{\rho_s B I_{31}}$$

As in the measurement of sheet resistance, multiple currents were used, and each measurement was repeated for the two permutations of contacts. The mobility was found to be $\mu_H = 4.1 \times 10^5 \mathrm{cm}^2/\mathrm{V\,s}$.

The carrier density can be calculated from the above values. In general,

$$n_s = \frac{r}{q \rho_s \mu_H}$$

where r is the Hall scattering factor[23]. The Hall scattering factor depends on the dominate scattering mechanism in the material. Its value ranges between 1 and 2, where a value of

1 corresponds to neutral impurity scattering. Assuming $r = 1$, the calculated density is $n_s = 3.1 \times 10^{11}\text{cm}^{-2}$.

The elastic mean free path can be calculated as:

$$l = \frac{\hbar \mu_H}{e} \sqrt{2\pi n_s}$$

Computed values for MBE 33 yield $l = 3.8$ um. Note that the inelastic mean free path is larger than this value and hence much larger than the period of our LSSL devices, as required. In order to have phase-coherence, we require that our sample be smaller than the *inelastic* mean free path[24]. Unfortunately, we did not directly measure this quantity.

3.3 LSSL Measurements

All measurements on the LSSL devices were performed in a ^{3}He cryostat at 4.2 K and 300 mK. Details of the cryostat operations can be found in References [25, 26]. The measurement electronics consisted of an HP function generator, a low-noise current preamplifier, and several HP digital multimeters.

The simplest measurement to perform on the LSSL device is to apply a small bias across the source and drain of the device and sweep the gate voltage. As the gate is swept more negative, carriers are depleted under the gate and consequently the Fermi level drops. It is anticipated that when the Fermi level is swept through a mini-bandgap, conduction will decrease, ideally to zero. A plot of the typical data is shown in Figure 3-2. This plot is for a device with a 150 nm period and linewidths of about 55 nm. In this device, and the others measured, there is no sign of the expected conductance modulation.

The lack of conductance modulation implies that the mini-bandgaps are not present, or that the conduction is occuring from multiple bands. A micrograph of the device confirmed the presence of a periodic metallic gate. One possible explanation is that there is mobile surface charge that effectively makes the device a continuous-gate MODFET. With this hypothesis in mind, experiments were done with the gate bias modulated quickly (70 Hz) with the hope that the surface charge mobility was low. However, no noticeable difference was seen.

Another possible explanation is that there are long-range potentials present from the random impurity doping of the n-AlGaAs layer. Nixon and Davies[27] have shown the standard deviation of potential fluctuation is 18 mV over a 100 μm^2 area at low densities. In the case of our LSSL device, we expect to see the conductance modulation near the

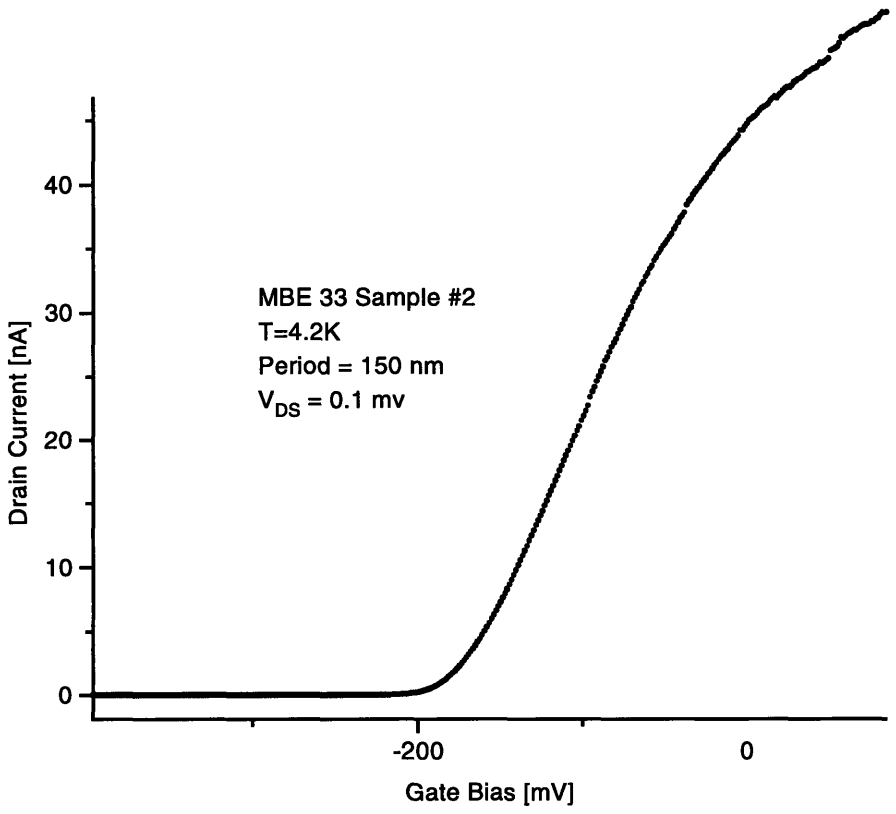

Figure 3-2: Representative I-V curve for the 150 nm period device.

pinch-off voltage. In this regime, the density of electrons is very low. Furthermore, the study of a 400 nm wire near pinch-off revealed even more dramatic effects than the $100\,\mu m^2$ area. When modeled with random impurity doping, the wire became discontinuous at $V_g = -2.65\,V$, approximately 150 mV greater than without the random impurities! In the case of the LSSL device, we expect the mini-bandgaps to be on the order of 10 meV, less than that of the standard deviation of potential fluctuations found by Nixon and Davies. It is therefore possible that the 2-DEG does not see a periodic potential. Alternatively, we could view the periodic potential as being unaffected, retaining the mini-bandgaps, and assume the long range potential fluctuations cause local changes in E_f. This implies that at a suitable bias, some regions of the device have energies in the gap, while other regions are in the bands. The conductance then would be averaged over these values. Although this explanation is plausible, further experiments are needed to validate it.

Chapter 4

Conclusions

4.1 Summary

Several innovations in the fabrication of nano-scaled devices have been made. A reliable process for ohmic contact generation has been developed and tested. The contacts did not freeze out at low temperatures and showed a good nominal contact resistance of $\approx 1\Omega \cdot mm$. New techniques for contact x-ray lithography have been used to reproduce feature sizes down to 25 nm. LSSL devices have been fabricated and measured. A hypothesis for why the device failed has been formulated, and experiments for future work are proposed.

4.2 Future Work

The major question with regard to the LSSL device is the cause of failure reported by our group and others. In order to eliminate the possibility of surface charge effects, a fixed-potential device should be made by etching the grid pattern into the heterostructure. Our current x-ray mask has both the fine period gates and the general metalization layers on the same mask. In order to switch to an etched grid, a new x-ray mask must be written with just the grid patterns. A corresponding optical mask needs to be made to complete the metalization layers.

In order to examine the possibilities of long-range potential fluctuations, one could examine a device with only a few periods of the grid. By reducing the overall size, the potential fluctuations should be reduced. Another possibility is to create a narrow quantum wire. If the long-range potential fluctuations exist, the wire should become discontinuous near pinch-off. If it becomes multiply disconnected, it will look like a quantum dot, and may show signs of coulomb blockade.

Appendix A

Fabrication Sequence

This appendix covers in detail all of the fabrication steps used to create both the masks and devices used in this work.

A.1 Mask Fabrication

A.1.1 Development and Electroplating

1. Turn on the pump for the plating system and the temperature controller for the water bath. The plating system needs some time to stabilize to the desired bath temperature (33 °C). Adjust the bath flow for a rate of 2.5 LPM. Add water to the bath if needed.
2. Setup the OAI (optical aligner) for 220 nm operation and turn on.
3. Place mask under the "enterprise hat" to cover the membrane area. Flood expose the outer area for 30 minutes.
4. Start a "dsclean" run on the RIE to clean the chamber if the last RIE process run used gases other than oxygen.
5. Characterize the plating bath.
   (a) Check the temperature and conductivity. The conductivity is normally around 74 mS/cm.
   (b) UV ozone an old plating monitor (resist stripped) for 30 s.
   (c) Load the monitor in the plating system. Place the saturated Calomel electrode (SCE) in the bath.
   (d) Start the plating power supply.
   (e) Change the current sequentially through 35, 25, 15, then 35 mA. At each current, note the supply bias and the SCE voltage.

(f) One benchmark for the plating solution is the SCE voltage reading at 35mA. Plating is good if this voltage is under 0.6V. If it is not, add 5-10ml of brightener. Wait for the bath to stabilize, and re-characterize.

(g) Remove the plating monitor. Rinse monitor and mounting ring.

6. Mix the developer (1:2 MIBK:IPA) in a 1 liter beaker. The desired temperature for the developer of 21 °C can be achieved by warming it with the hands on the outside of the beaker.

7. Once the developer temperature has settled to 21 ^{o}C, develop the mask. Mother masks with patterns written at multiple doses are developed for a fixed time of 90 seconds. Daughter masks are developed in multiple steps, with inspection between each step indicating when to stop. Try 15 seconds as an initial time for daughter masks.

8. Immediately rinse the mask with IPA using the squirt bottle.

9. Blow the sample dry with the filtered N_2 gun. Use caution not to apply too much pressure to the membrane.

10. If this is a daughter mask, measure the step height in the AFM. If the step height is not the same as the PMMA height, further development is needed. Repeat the previous steps. Note: If the mother mask had a PI_{2610} gas relief channel on it, you will be able to see that grid pattern in the daughter mask. Once the pattern can not be seen, the development is complete.

11. Load the sample into the RIE for "descum". Run the descum program. Keep the sample under vacuum in the RIE until you are ready to plate.

12. Electroplate 200 nm of gold. For good plating, you want a current density of 0.4 mA/cm^2. At this density, the plating rate is 25 nm/minute.

13. Measure the step height from PMMA to Au to verify the proper thickness. For a mask spun with 250 nm of PMMA, the step height should be 50 nm.

14. Strip the PMMA by rinsing in acetone and methanol and plasma ashing.

15. For mother masks, remove the thick Au fingers near the mesa. If you do not remove them, they tend to curl up and stick out of the mask. If the mask is used for contact daughtering, the fingers will poke through the daughter mask!

(a) Spin Shipley 1813 photo resist at 4kRPM for 30 seconds over the whole mask.

(b) Using the xenon lamp for the optical microscope, expose the fingers and any suspicious particles in the optical microscope with maximum white light intensity. Using the 50x objective, it takes a dose of approximately 5 seconds to clear using 30 s development time.

(c) Develop the resist in 351:H_2O 5:1.

(d) Use an eye dropper to put drops of gold etch on the openings in the resist. The etch of the largest particles should be completed in about 15 minutes.

(e) Strip resist by rinsing in acetone and methanol. Plasma ash if necessary.

A.1.2 Removing Plating Base in Alignment Areas

If the mask is to be used for aligned exposure, the plating base needs to be removed from the alignment marks. By exposing through the membrane, the thick Au patterns will still be covered by unexposed resist and only the resist over the plating base will be exposed.

1. Spin photoresist Shipley 1813 at 4.5 kRPM for 30 sec. Bake for 30 minutes at 90°C.
2. Place xenon lamp on the microscope and power on.
3. Place mask in bottom part of flouroware so that the mask can be placed pattern-side down on the microscope stage.
4. Using the 50x objective, carefully bring the backside of the mask into focus. Be very careful not to let the objective hit the Pyrex mask ring!
5. Expose the alignment mark regions for 30 seconds each.
6. Develop with Shipley 351 (1:5 351:DI) developer for about 30 sec.
7. Plasma ash the sample in He/O_2 for 6 seconds at about 60 W power.
8. Etch the gold in 10:1 dilute gold etchant for 10 seconds (this is assuming the plating base is thin, i.e. 20ÅAu).
9. Etch the Ti in 55°C Ti etchant for 5 sec.

A.1.3 Polyimide Gas Relief Channels

If the mask is to be used for exposures in intimate contact with the substrate or blank mask, a polyimide corrugation grating is necessary for outgassing of the resist.

1. Spin about 300 nm of PI_{2610}, use 3:2 PI_{2610}:NMP at 3.6 kRPM for 60 sec.
2. If this is a daughter mask, clean off the polyimide at the edges of the mask with a swab soaked in NMP. This ensures good electrical contact with the mask holder.
3. Softbake the polyimide. Bake at 140 °C for 30 minutes.
4. If the polyimide should be stripped in the alignment mark area, spin photoresist, bake, expose, develop, and strip resist. The developer (351) will remove the softbaked polyimide from the exposed regions.
5. Hardbake the polyimide. Bake 250 °C for 30 minutes.
6. Spin on 1:3 PI_{2610}:NMP at 3.1 kRPM for 60 sec to get roughly 70 nm of polyimide.
7. Bake at 180 °C for 30 min.
8. Immediately spin on photoresist (4.5kRPM, 30 sec.) and bake at 90°C for 20 minutes.
9. If there are alignments marks, expose them in the optical microscope as before.

10. Expose with a grid flex mask in the Tamarak ($\lambda = 400\,\text{nm}$). Use $20\,\mu$m-period for mother masks, and $100\,\mu$m-period for daughter masks.

11. Develop in 5:1 DI:351 developer. Carefully monitor the development. Overdevelopment will remove all of the polyimide.

12. Strip the remaining resist using acetone and methanol.

13. Bake at $200\,^{o}$C for 1 hour.

A.2 Device Fabrication

A.2.1 Mesa Isolation

1. Solvent Cleaning of Sample and Surface Clean.

   (a) Prerinse beakers with solvent.

   (b) Rinse sample in TCA.

   (c) Boil in TCA for 10 min (hotplate designation $\approx 90\,^{\circ}$C.)

   (d) Ultrasonicate in acetone for 10 min.

   (e) Ultrasonicate in methanol for 10 min.

2. Photolithography and Development:

   (a) Expose resist with mesa mask for 3.7 sec, using OAI.

   (b) Develop exposed resist for 30 s with straight Shipley CD-30 developer. Use a dipper. Follow by 1 min. rinse in DI. Transfer to running DI.

   (c) Inspect in microscope.

   (d) Continue developing in 10—15 second increments until pattern clears. Total development time should be $\approx$45—60 sec. Pay attention to corners where resist is thickest.

   (e) Spray mask with acetone/methanol.

   (f) Blow dry mask.

3. Etch AlGaAs – RUN MONITOR SAMPLE FIRST:

   (a) Ammonium hydroxide/hydrogen peroxide etch: 500:10:3 DI:NH_4OH:H_2O_2 in large RCA beaker (put H_2O_2 last); mix well and put small amount into a beaker. Run a monitor sample first to calibrate etch rate. Etch $\approx$17 s (=600-750Å).

   (b) Rinse in DI for 2 min. Transfer directly to running DI water in sink if possible.

   (c) Blow dry.

   (d) Inspect in microscope.

4. Strip resist:

(a) Spray with acetone.
(b) Spray with methanol.
(c) Blow dry.
(d) Inspect in microscope.
(e) Measure mesa height in Alpha-Step.

A.2.2 Ohmic Contacts

It's a good idea to run a bare Si monitor with the evaporation in case you might need to analyze the films later.

1. Solvent clean (same as above).
2. Spin and bake photoresist (same as above).
3. Expose sample (same as above)
4. Develop (≈45—60 sec total) and rinse 1 min in DI. Try to clear corners, but not overdevelop center features.
5. Inspect in microscope.
6. Spray mask with acetone/methanol.
7. Blow dry mask.
8. UV ozone for 15 s (run UV ozone for 30 s before putting samples).
9. Rinse in DI water for 1 min.
10. Rinse in 5% NH_4OH for 15 sec. 5% NH_4OH is mixed 5:1 H_2O:NH_4OH(30%)
11. Blow dry.
12. Thermal evaporate ohmic contacts: 5 nm Ni/60 nm Ge/120 nm Au/30 nm Ni/30 nm Au.
13. Liftoff by soaking for ≈10 minutes in acetone. Then place beaker in ultrasound for ≈10 sec for full liftoff. Do not use a dipper for this step. Quickly remove sample from first beaker and transfer to a second beaker (also filled with acetone), spraying with acetone in between. Remove from second beaker at your leisure, spray with acetone, then methanol, then blow dry.
14. Solvent clean the sample.
15. Transport to Rm. 13-2111 in a vacuum container.
16. Anneal in the strip heater in forming gas at 420 °C for 30 sec. Place sample face up on the resistive heating element. Place a solvent-cleaned piece of semi-insulating (SI) GaAs face down onto the sample.
17. Check TLM resistances, should be $\approx 1\Omega \cdot$ mm, using program POHMIC3 (2 probe) or PMBOHM or PAKOHM (4 probe). Verify sheet resistance using 4-point VDP.

A.3 Gates

1. Solvent clean (same as above).
2. Spin 3% 950K PMMA at 2.9 kRPM for 60 seconds for ≈220 nm of PMMA.
3. Bake at 180 °C for 1 hour.
4. Place samples face down on a clean-wipe. Place under the OAI. Flood expose backside of chips at 220 nm for 30 min.
5. Use a swab soaked in 3:2 IPA:MIBK to remove PMMA from the backside of the sample.
6. Rinse sample in IPA for 30 seconds. Dry with N_2.
7. Place small-sample chuck on top of pin-chuck in Head 5.
8. Place sample on chuck. Apply vacuum.
9. Place mask in holder.
10. Raise sample to mask. Watch as the corners come into contact with the mask. Lower sample, and adjust leveling until all four corners come into contact at the same time.
11. Raise sample again. Examine alignment in microscope. Lower sample, adjust, raise. Repeat until the sample and mask are aligned. After aligned, keep sample in physical contact with mask.
12. Remove vacuum to the sample.
13. Apply voltage between mask and sample. Watch for intimate contact. The voltage needed varies greatly with the resistivity of the substrate.
14. Lower stage. Remove mask/sample and load into Head 1.
15. Expose sample.
16. To remove sample from mask, put mask back in Head 5 holder. (make sure chuck is lowered).
17. Apply vacuum to chuck. Raise chuck until the vacuum pulls the chip off the mask. Lower chuck.
18. Develop
    (a) Mix new 2:3 MIBK:IPA, and warm to 21 °C.
    (b) Develop sample in petri dish. Use the image of the mask's gas-relief channels to monitor development.
    (c) Squirt with MIBK:IPA as you pull out of developer and put into straight IPA.
    (d) Blow dry.

19. Descum sample
    (a) Put sample on top of the dummy mask or dummy wafer in the RIE.
    (b) Using the manual mode of operation flow 2.5 sccm O_2 and 10 sccm of He.
    (c) Adjust chamber pressure to 35 mTorr. Wait one minute.
    (d) Set to bias control mode. Set bias to 20 V.
    (e) Once plasma sparks, allow to run for 15 seconds. Stop.
20. Rinse sample in running DI for 1 min.
21. Rinse in 5% NH_4OH (mixed as above) for 10 sec.
22. Blow dry and go directly into evaporater.
23. Evaporate gate material
24. Liftoff in hot NMP for 2 minutes.
25. Transfer to acetone. Spray during transfer.
26. Ultrasonicate for 20 seconds.
27. Place sample in small, shallow petri dish filled with acetone.
28. Using a *long focal length* objective (e.g. the 20h on Head 5), examine the lift-off.
29. Repeat above steps as necessary.
30. Rinse sample in acetone and methanol. Blow dry.

Appendix B

Strip Heater

This appendix describes the use and maintenance of the strip heater maintained by the Quantum Effects Electronics (QEE) group. The strip heater is designed for annealing ohmic contacts. It can easily attain temperatures of 500°C, and remains stable to ±1°C. It also has the ability to be programmed with eight ramp and soak sequences for complete process control.

B.1 Using the Strip Heater

B.1.1 Loading the sample.

1. Move the fan away from the strip heater.
2. Remove the three allen-screws holding the bell jar onto the strip heater frame.
3. Carefully remove the retainer ring and the bell jar.
4. Place the sample to be annealed on the center of the strip heater.
5. Replace the bell jar and retainer ring. Note: there is a chip on the edge of the bell jar. Position the bell jar *slightly* offset so that the chip is mostly on the outside of the O-ring.
6. Retain the bell jar with the allen-screws. Do not over-tighten!

B.1.2 Forming gas flow.

1. Open the main valve on the bottle of forming gas.
2. Open the gas valve on the strip heater.

3. Turn the needle valve counter-clockwise until gas just begins to flow. (This is indicated by the flow meter).

4. Check that the regulator on the bottle of gas is set near 20 PSI.

5. Adjust the needle valve until 3 "silver ball units" (sbu) of gas are flowing.

6. Start a timer or stop-watch. Forming gas must flow for at least five minutes before using the strip heater.

B.1.3 Programming the Process in the Eurotherm controller.

It is extremely important to only change the parameters listed below. Other changes could potentially damage the power supply.

The Eurotherm controller is controlled by a set of six buttons (three buttons are located behind the "door") on the front panel.

The buttons have the following functions:

[⇑] increases the value of the current parameter.

[⇓] decreases the value of the current parameter.

[℗] scrolls through the menu selections. Pressing the button once at a time scrolls through the temperature set point (Sp), the output power (Op), and the time remaining in the current step if a program is running. You may also hold the scroll button down, without releasing it. This causes the menu to scroll through the above items, and then enter an extended menu so that you can change the programming of the controller.

[**Hand**] puts the controller in manual mode. You can directly control the power supplied to the strip heater. There should be no reason to select this.

[**Rem**] allows the set point to be controlled remotely. This feature is not setup for our strip heater. Do not press this button.

1. Press the menu scroll button ([℗]) until the set point (`Sp`) is displayed. Make sure that the main set point (`Sp`) is set to 0 °C. If it is not, use the decrease value key (⇓) to set it to zero.

2. Press and hold the menu scroll button until the display (`Pr1`) is shown. This is the ramp rate in °C/min for the first ramp interval. Set it appropriately. Default value is 400.

3. Press the scroll menu button again. The display reads `Pl1`. This is the desired temperature to ramp up to. Set it appropriately.

4. Press the scroll menu button again. The display reads `Pt1`. This is how long, in minutes, the controller maintains the temperature given by `Pl1`. Set it appropriately.

5. Press the scroll menu button again. The display reads `Pr2`. This is the ramp tate for the second ramp sequence. Continue program ramp and soak sequences until you are done. The last programmed ramp rate should be set to 400, the last level must be set to 0°C, and the last hold time should be set to `End`. (Note: `End` is found by pressing the down arrow button after zero is reached).

B.1.4 Running your process.

1. Turn on the power on the Sorenson power supply.
2. Set the coarse current control to the midpoint value (pointing straight up). Set the fine current control and both voltage controls fully counter-clockwise.
3. Turn on the power-strip to activate the fan and the strip-chart recorder. Move the fan so that it blows on the bell jar.
4. Set the strip-chart recorder to advance paper at 5 cm/min. Put pen 1 on the 0-10 V range and turn it on.
5. Press the run button on the Eurotherm controller.
6. You may press the scroll menu button to switch the display between temperature and time remaining (and output power).
7. When the run is ended, an `E` is displayed in the lower right corner of the Eurotherm.
8. Turn off the power to the Sorenson power supply.
9. Turn off the paper feed on the strip chart recorder (0 cm/min). Turn pen 1 off on the strip chart recorder. advance the paper as necessary and tear off the sheet. Tape it to the back of the run log you have filled out.
10. Wait for the temperature to fall below 80 °C.
11. Close the needle valve. Turn off the gas flow switch. Close the main valve on the forming gas bottle.
12. Remove the bell jar as described above, and remove your sample.
13. Replace the bell jar as described above.

B.2 Maintenance of the Strip Heater

The manuals involving the components of the strip heater can be found in Rm. 13-2111. They are in the top drawer of the filing cabinet near the door in a folder labeled "Strip heater". The following manuals are available:

- Eurotherm controller.

- Sorenson power supply. Note: This manual is for a different model power supply than the one used, but most functions are the same.
- Lein 24 strip chart recorder.

B.2.1 Routine maintenance and supplies.

The following items are expected to need routine replacement. The vendor and product descriptions are give.

Forming Gas The forming gas used is 95% N and 5% H. The tank is a 5 ft. tank size 200. It has approximately 200 $ft^3 \approx 5664L$. Assuming 10 minute runs at 2L/min, we should get 280 runs from a tank. The gas can be ordered from BOC for approximately $15.00.

Strip Chart Recorder Supplies There are extra pens and and paper stored in Rm. 13-2111. They can be found in a metal draw labeled "Strip chart recorder pens" on the bottom shelf of the shelving unit near the entrance to the lab.

If the pen quits moving, it is most likely due to the drive belt (an O-ring) breaking. If the second pen works, just switch the inputs to the second pen, otherwise belts will have to be ordered from Lein. All strip chart recorder parts can be ordered from Lein.

Thermocouples The strip heater uses type J thermocouples (Iron – Constanian). They can be ordered from Omega Engineering.

Appendix C

Electron Beam Lithography

The following file is the source code used to create a set of dose matrices. The dose matrix also contains patterns which can be used to determine the optimum way to write intersecting lines.

This code readily compiles under `gcc` and must be linked to the Kic file gencif.c. It also uses the header file `cd.h` available with the Kic source-code distribution. This program is guaranteed to produce valid Kic files because it is linked to the Kic program itself, rather than emulating these routines. Furthermore, if the Kic specifications change in the future, the program only needs to be re-linked to the new library. This allows easy upward migration for future revisions.

```
/* This program creates a kic file with grids suitable for dose
 * testing, astigmitism checking, and for optimizing the break size of
 * line intersections */

#include <stdio.h>
#include "cd.h"
#include <math.h>

#define LW 0
#define INTSCALE 100L                                                    10
#define MARGIN 100L
#define PIXEL_SZ .61035156250

void make_kic(FILE **FileDesc, char fname[]);
void close_kic(FILE *FileDesc);
void make_dbl_grid(FILE *fp, char layer[],
            long int x_off, long int y_off);
void make_grid(FILE *fp, long int period, int num_per,
            long int x_off, long int y_off);
void make_grid_doses(FILE *fp, long int period,                          20
```

```
                long int x_off, long int y_off);
void make_bracket(FILE *fp, long int period, int num_per, int start_sz,
                long int x_off, long int y_off);
void make_bracket_doses(FILE *fp, long int period,
                        long int x_off, long int y_off);
void make_abroken_grid(FILE *fp, long int period, int num_per, float break_sz,
                long int x_off, long int y_off);
void make_abroken_grid_doses(FILE *fp, long int period, float break_sz,
                        long int x_off, long int y_off);
void make_sbroken_grid(FILE *fp, long int period, int num_per, float break_sz,
                long int x_off, long int y_off);
void make_sbroken_grid_doses(FILE *fp, long int period, float break_sz,
                        long int x_off, long int y_off);

main()
{
  FILE *FileDesc;
  int     break_pix;
  float break_sz;
  long int y_off=40000;
  char fname[12]="d1.kic";

  /* Create a kic file and send out the intializing commands */

  make_kic(&FileDesc, "dall.kic");

  /* Generate standard dose matrix grids */
  GenComment(FileDesc,"Grid Dose Matrix");
  make_grid_doses(FileDesc, 15L, 0L+MARGIN,     0L+MARGIN);
  make_grid_doses(FileDesc, 20L, 0L+MARGIN, 10000L+MARGIN);
  make_grid_doses(FileDesc, 30L, 0L+MARGIN, 20000L+MARGIN);
  make_grid_doses(FileDesc, 40L, 0L+MARGIN, 30000L+MARGIN);

  /* Generate "angle brackets" to check astigmitisms */
  GenComment(FileDesc,"Bracket-Grid Dose Matrix");
  make_bracket_doses(FileDesc, 15L, 10000L+MARGIN,     0L+MARGIN);
  make_bracket_doses(FileDesc, 20L, 10000L+MARGIN, 10000L+MARGIN);
  make_bracket_doses(FileDesc, 30L, 10000L+MARGIN, 20000L+MARGIN);
  make_bracket_doses(FileDesc, 40L, 10000L+MARGIN, 30000L+MARGIN);

  /* Generate grids without overlaps at the intersections.  The break
     is only in one direction with varying size. */
  GenComment(FileDesc,"Asymmetrically Broke Grid Dose Matrix");
  y_off=40000;
  for (break_pix=1; break_pix<=11 ;break_pix+=2 ){
    break_sz=(break_pix)*PIXEL_SZ;
    make_abroken_grid_doses(FileDesc, 15L, break_sz,
                            0L+MARGIN, y_off+MARGIN);
    make_abroken_grid_doses(FileDesc, 20L, break_sz,
                            10000L+MARGIN, y_off+MARGIN);
    make_abroken_grid_doses(FileDesc, 30L, break_sz,
                            20000L+MARGIN, y_off+MARGIN);
    make_abroken_grid_doses(FileDesc, 40L, break_sz,
                            30000L+MARGIN, y_off+MARGIN);
    y_off=y_off+10000;
```

```
  }

  /* Generate grids without overlaps at the intersections.  The breaks
     are in both direction with varying sizes. */
  GenComment(FileDesc,"Symmetrically Broke Grid Dose Matrix");
  y_off=40000;
  for (break_pix=1; break_pix<=11 ;break_pix+=2 ){
    break_sz=break_pix*PIXEL_SZ;
    make_sbroken_grid_doses(FileDesc, 15L, break_sz,
                            40000L+MARGIN, y_off+MARGIN);
    make_sbroken_grid_doses(FileDesc, 20L, break_sz,
                            50000L+MARGIN, y_off+MARGIN);
    make_sbroken_grid_doses(FileDesc, 30L, break_sz,
                            60000L+MARGIN, y_off+MARGIN);
    make_sbroken_grid_doses(FileDesc, 40L, break_sz,
                            70000L+MARGIN, y_off+MARGIN);
    y_off=y_off+10000;
  }
  close_kic(FileDesc);
}

void make_kic(FILE **FileDesc, char fname[])
{
  *FileDesc = fopen(fname,"w");
  fprintf(*FileDesc,"(Symbol %s);\n",fname);
  fprintf(*FileDesc,"9 %s;\n",fname);
  GenBeginSymbol(*FileDesc,0,1,1);
}
void close_kic(FILE *FileDesc)
{
  GenEndSymbol(FileDesc);
  GenEnd(FileDesc);
  fclose(FileDesc);
}
/*
 * Routine to write a P=150nm and P=300nm grid beside each other
 * with 10 periods each.  1.5um between boxes.
 * With a 1um border around everything, the unit cell is 8umx8um
 *
 */

void make_dbl_grid(FILE *fp, char layer[],
                   long int x_off, long int y_off)
{

  /* 100 lambda = 1um for lambda =.01 um */

  char Tech='L';

  GenLayer(fp,Tech,layer);
  make_grid(fp, 15L, 10, x_off+MARGIN, y_off+MARGIN);
  make_grid(fp, 30L, 10, x_off+MARGIN+300L, y_off+MARGIN);
}
```

```
/*
 * Routine to write one period grid in 30 doses (3x10 array)
 *
 */
void make_grid_doses(FILE *fp, long int period,
                     long int x_off, long int y_off)
{

  int i,j,layer_num=0;
  char Layer[3]="1";                                                    140
  char Tech='L';


  /* Create 30 layers of arrays in a 10x3 array */

  for(j=0; j<3; j++)
    for(i=0; i<10; i++){
      layer_num++;
      sprintf(Layer,"%d",layer_num);
      GenLayer(fp,Tech,Layer);                                          150
      make_grid(fp, period , 10, x_off+i*700, y_off+j*700);
    }
}



/*
 * Routine to write one grid
 *
 */                                                                     160
void make_grid(FILE *fp, long int period, int num_per,
               long int x_off, long int y_off)
{


  struct p Start, End;
  long int Width = LW;
  int i;

  /* Intitialize a two element linked list */                           170
  Start.pSucc = &End;
  End.pSucc = NULL;


  /* Make Horizontal Lines */
  Start.pX = x_off*INTSCALE;
  End.pX = (x_off + num_per*period)*INTSCALE;
  for (i=0; i<=num_per; i++){
    Start.pY = (y_off + i*period)*INTSCALE;
    End.pY = Start.pY;                                                  180
    GenWire(fp, Width, &Start);
  }

  /* Now for the Vertical Lines */
  Start.pY = y_off*INTSCALE;
```

```
  End.pY = (y_off + num_per*period)*INTSCALE;
  for (i=0; i<=num_per; i++){
    Start.pX = (x_off + i*period)*INTSCALE;
    End.pX = Start.pX;
    GenWire(fp, Width, &Start);                                    190
  }
}


/*
 * Routine to write one period bracketed grid in 30 doses (3x10 array)
 *
 */
void make_bracket_doses(FILE *fp, long int period,
                        long int x_off, long int y_off)            200
{

  int i,j,layer_num=0;
  char Layer[3]="1";
  char Tech='L';


  /* Create 30 layers of arrays in a 10x3 array */

  for(j=0; j<3; j++)                                               210
    for(i=0; i<10; i++){
      layer_num++;
      sprintf(Layer,"%d",layer_num);
      GenLayer(fp,Tech,Layer);
      make_bracket(fp, period , 10, 500, x_off+i*1500, y_off+j*1500);
    }
}

/*
 * Routine to write bracketed-grid                                 220
 *
 */
void make_bracket(FILE *fp, long int period, int num_per, int start_sz,
                  long int x_off, long int y_off)
{


  struct p S,M,E;
  long int Width = LW;
  int i;                                                           230

  /* Intitialize a two element linked list */
  S.pSucc = &M;
  M.pSucc = &E;
  E.pSucc = NULL;

  for (i=0; i<=num_per; i++){
    S.pX = (x_off + i*period + start_sz)*INTSCALE;
    S.pY = y_off*INTSCALE;
                                                                   240
```

```
    M.pX = S.pX;
    M.pY = (y_off + i*period + start_sz)*INTSCALE;

    E.pX = x_off*INTSCALE;
    E.pY = M.pY;

    GenWire(fp, Width, &S);
  }
}

/*
 * Routine to write one period of assymetrically broken intersection
 * grids in 30 doses (3x10 array)
 *
 */
void make_abroken_grid_doses(FILE *fp, long int period, float break_sz,
                             long int x_off, long int y_off)
{

  int i,j,layer_num=0;
  char Layer[3]="1";
  char Tech='L';


  /* Create 30 layers of arrays in a 10x3 array */

  for(j=0; j<3; j++)
    for(i=0; i<10; i++){
      layer_num++;
      sprintf(Layer,"%d",layer_num);
      GenLayer(fp,Tech,Layer);
      make_abroken_grid(fp, period , 10, break_sz, x_off+i*700, y_off+j*700);
    }
}

/*
 * Routine to write one assymetrically broken intersection grid
 *
 */
void make_abroken_grid(FILE *fp, long int eperiod, int num_per, float break_sz,
                       long int ex_off, long int ey_off)
{


  struct p Start, End;
  long int Width = LW;
  int i, j;
  double period, x_off, y_off;

  /* Intitialize a two element linked list */
  Start.pSucc = &End;
  End.pSucc = NULL;

  /* Adjust to make it fit pixel size better */
```

```
  period = (PIXEL_SZ*ceil(eperiod/PIXEL_SZ));
  x_off = (PIXEL_SZ*ceil(ex_off/PIXEL_SZ));
  y_off = (PIXEL_SZ*ceil(ey_off/PIXEL_SZ));

  /* Make Horizontal Lines */                                          300
  Start.pX = x_off*INTSCALE;
  End.pX = (x_off + num_per*period)*INTSCALE;
  for (i=0; i<=num_per; i++){
    Start.pY = (y_off + i*period)*INTSCALE;
    End.pY = Start.pY;
    GenWire(fp, Width, &Start);
  }

  /* Now for the Vertical Lines */
  for (i=0; i<=num_per; i++){                                          310
    Start.pX = (long int)((x_off + i*period)*INTSCALE);
    End.pX = Start.pX;
    for (j=0; j<num_per; j++){
      Start.pY = (long int)((y_off + j*period + break_sz/2)*INTSCALE);
      End.pY = (long int)((period - break_sz)*INTSCALE) + Start.pY;
      GenWire(fp, Width, &Start);
    }
  }
}
                                                                       320

/*
 * Routine to write one period of symetrically broken intersection
 * grids in 30 doses (3x10 array)
 *
 */
void make_sbroken_grid_doses(FILE *fp, long int period, float break_sz,
                             long int x_off, long int y_off)
{
                                                                       330
  int i,j,layer_num=0;
  char Layer[3]="1";
  char Tech='L';


  /* Create 30 layers of arrays in a 10x3 array */

  for(j=0; j<3; j++)
    for(i=0; i<10; i++){
      layer_num++;                                                     340
      sprintf(Layer,"%d",layer_num);
      GenLayer(fp,Tech,Layer);
      make_sbroken_grid(fp, period , 10, break_sz, x_off+i*700, y_off+j*700);
    }
}

/*
 * Routine to write one symetrically broken intersection grid
 *
 */                                                                    350
```

```
void make_sbroken_grid(FILE *fp, long int eperiod, int num_per, float break_sz,
                       long int ex_off, long int ey_off)
{


  struct p Start, End;
  long int Width = LW;
  double period, x_off, y_off;
  int i, j;

  /* Intitialize a two element linked list */
  Start.pSucc = &End;
  End.pSucc = NULL;


  /* Adjust to make it fit pixel size better */
  period = (PIXEL_SZ*ceil(eperiod/PIXEL_SZ));
  x_off = (PIXEL_SZ*ceil(ex_off/PIXEL_SZ));
  y_off = (PIXEL_SZ*ceil(ey_off/PIXEL_SZ));

  /* Make Horizontal Lines */

  for (i=0; i<=num_per; i++){
    Start.pY = (long int)((y_off + i*period)*INTSCALE);
    End.pY = Start.pY;
    for (j=0; j<num_per; j++){
      Start.pX = (long int)((x_off + j*period + break_sz/2)*INTSCALE);
      End.pX = (long int)((period - break_sz)*INTSCALE) + Start.pX;
      GenWire(fp, Width, &Start);
    }
  }

  /* Now for the Vertical Lines */
  for (i=0; i<=num_per; i++){
    Start.pX = (long int)((x_off + i*period)*INTSCALE);
    End.pX = Start.pX;
    for (j=0; j<num_per; j++){
      Start.pY = (long int)((y_off + j*period + break_sz/2)*INTSCALE);
      End.pY = (long int)((period - break_sz)*INTSCALE) + Start.pY;
      GenWire(fp, Width, &Start);
    }
  }
}
```

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