Power Limiting Mechanisms in InP HEMTs

by

Christopher S. Putnam

Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degrees of

Bachelor of Science in Electrical Science and Engineering

and Master of Engineering in Electrical Engineering and Computer Science

at the Massachusetts Institute of Technology

June 6, 1997

Copyright Christopher S. Putnam. All Rights Reserved.

The author hereby grants to M.I.T. permission to reproduce and

disribute publicly paper and electronic copies of this thesis

and to grant others the right to do so.

Author___________________________

Department of Electrical Engineering and Computer Science

May 9, 1997

Certified by___________________________

Jesús A. del Alamo

Associate Professor of Electrical Engineering

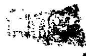
Thesis Supervisor

Accepted by___________________________

Arthur C. Smith

Chairman, Department Committee on Graduate Theses

2 5 1997



Power Limiting Mechanisms in InP HEMTs

by

Christopher S. Putnam

Submitted to the Department of Electrical Engineering and Computer Science

May 9, 1997

in Partial Fulfillment of the Requirements for the Degrees of
Bachelor of Science in Electrical Science and Engineering
and Master of Engineering in Electrical Engineering and Computer Science

Abstract

The InAlAs/InGaAs High Electron Mobility Transistor (HEMT) fabricated on InP has proven to be the fastest transistor ever produced. It also appears to be the best candidate for power amplification at mm-wave frequencies. To date, however, very good high-frequency power performance has not been realized in these devices, and the lack of a clear understanding of the power-limiting mechanisms has hampered success in pushing the devices farther. In an effort to understand the dominant power-limiting mechanisms in InAlAs/InGaAs HEMTs, we performed extensive electrical characterization including temperature-dependent measurements on state-of-the-art HEMTs fabricated by Lockheed Martin. Our experiments focused on the mechanisms determining the maximum drain current and the off-state breakdown voltage (BV) since these are the important parameters setting the power limits of a device. We conclude that the maximum current appears to be limited by velocity saturation in the extrinsic channel. We also find that the breakdown voltage primarily is set by tunneling and thermionic-field emission of electrons from the gate, and our findings are consistent with a new predictive model for the temperature dependence of BV based on this mechanism.

Thesis Supervisor: Jesús A. del Alamo
Title: Associate Professor of Electrical Engineering

Acknowledgments

The successful completion of this project would not have been possible without the help of my family, friends, and colleagues.

I would first like to thank my family for all of their support and encouragement throughout my career at MIT and the path leading to this institution. I would not be the man I am today without the Christian guidance and caring I received from my parents.

I also thank Professor Jesús del Alamo for his excellent leadership, insight, and unparalleled knowledge of device physics. He guided me throughout my research and was an excellent mentor.

Mark Somerville worked very closely with me in this entire project, and his collaboration is a significant part of this work. He was a constant source of help and information and was responsible for the model and theoretical calculations in the breakdown voltage section.

I would also like to recognize the other members of my research group. Roxann Blanchard, my officemate, put up with a lot of questions from me and was always willing to stop what she was doing to help me out. Alex, Ritwik, and Jim also provided assistance and diversions to keep our sanity.

My time at MIT would not have been complete without four years spent rowing with the heavyweight crew and the brotherhood and Christian fellowship I experienced as a member of the Beta Chapter of the Chi Phi fraternity.

Support for this work came from Lockheed Martin, who provided the devices for the research and funded the project as part of the MAFET program.

Table of Contents

Chapter 1: Introduction 8

1.1 Motivation 8

1.2 Device Description 11

1.3 Thesis Organization 14

Chapter 2: Maximum Drain Current 15

2.1 Introduction 15

2.2 Theoretical 16

2.3 Experimental 18

2.4 Discussion 25

2.5 Conclusion 28

Chapter 3: Breakdown Voltage 29

3.1 Introduction 29

3.2 Theoretical 30

3.3 Experimental 32

3.4 Discussion 37

3.5 Conclusion 44

Chapter 4: Implications to Device Design 46

4.1 Introduction 46

4.2 Optimization of Power Performance 48

4.3 Conclusion 52

Chapter 5: Conclusions and Suggestions for Future Work **53**

5.1 Conclusions 53

5.1.1 Maximum Drain Current 53

5.1.2 Breakdown Voltage 54

5.2 Suggestions for Future Work 54

References **57**

List of Figures

1.1 Power performance vs. frequency for various devices 9

1.2 Cross-section of the double heterostructure HEMTs under study 11

1.3 Conduction band diagram for a typical HEMT in this study 13

2.1 Current vs. field for a Transmission Line Model (TLM) test structure on Lockheed Martin sample 2721 17

2.2 Transfer characteristics for one of the devices measured 19

2.3 Results of simulations for sample 2723 20

2.4 Cross-section of HEMT detailing the small signal source resistance 21

2.5 Measurements for a typical TLM on wafer 2722 23

2.6 Source resistance vs. current 24

2.7 Measured transconductance and calculated intrinsic transconductance 26

2.8 Alternate approach for comparing g_m and g_{mo} 27

3.1 The three mechanisms investigated for breakdown voltage: (a) impact ionization; (b) tunneling/ thermionic-field emission; (c) a combination of the two 30

3.2 Two-terminal breakdown voltage measurement 33

3.3 Three-terminal breakdown voltage measurement 34

3.4 BV_{DG} vs. Temperature for one of the devices under study. Both two- and three-terminal measurements are plotted 35

3.5 BV_{DG} vs. $n_{s(extrinsic)}$ for several devices on each wafer in the sample set 36

3.6 Temperature dependence of BV_{DG} on three samples 37

3.7 BV_{DG} vs. $n_{s(extrinsic)}$ for devices in the literature 38

3.8 BV_{DG} vs. insulator thickness for four of the samples 39

3.9 Arrhenius plot of I_G across three samples showing universal behavior 40

3.10 Extraction of ϕ_B 42

3.11 Bias dependence of the gate current 43

3.12 BV_{DG} vs. Temperature for three samples: measurement and theory 44

4.1 Theoretical I_{dmax} for extrinsic region velocity saturation model 47

4.2 Theoretical breakdown voltage vs. $n_{s(extrinsic)}$ for tunneling/ TFE model 48

4.3 Breakdown voltage vs. maximum current for several devices in this sample set .. 49

4.4 $BV_{DG} \times I_{dmax}$ vs. $n_{s(extrinsic)}$ for devices in this sample set 50

List of Tables

1.1 Details of the structural parameters that varied across the sample set 12

Chapter 1

Introduction

1.1 Motivation

Continuing growth and advancement in communications technology is fueling an increasing need for systems that are capable of operating at extremely high frequencies so as to provide large bandwidth. Millimeter-wave devices are expected to gain demand in such markets as Local Area Networks (LAN), automobile communications, and toll debiting, to name a few [1]. In addition to high frequency capabilities, many applications demand devices that provide amplification at high power and power efficiency. This has sparked interest in new technologies across an expanded array of material systems.

Recent devices based on Indium Phosphide (InP) have exhibited very good high-frequency performance. Much of the research on devices in this family has focused on the Indium Aluminum Arsenide/ Indium Gallium Arsenide (InAlAs/InGaAs) High Electron Mobility Transistors (HEMTs) fabricated on an InP substrate (InP HEMTs, for short). Although originally investigated for high-speed low-noise applications, these devices show promise for millimeter wave power applications [1, 2]. InP-based HEMTs, in fact, exhibit record frequency performance, with results including a 600 GHz f_{max} [3] and 340 GHz f_t [4]. Also, designers have been able to produce impressive mm-wave systems using InAlAs/InGaAs HEMTs [5-7].

The outstanding frequency performance of InAlAs/InGaAs HEMTs arises from the intrinsic properties of the material system. The InGaAs channel has a high electron mobility and velocity, large conduction band discontinuity, and the heterojunction between

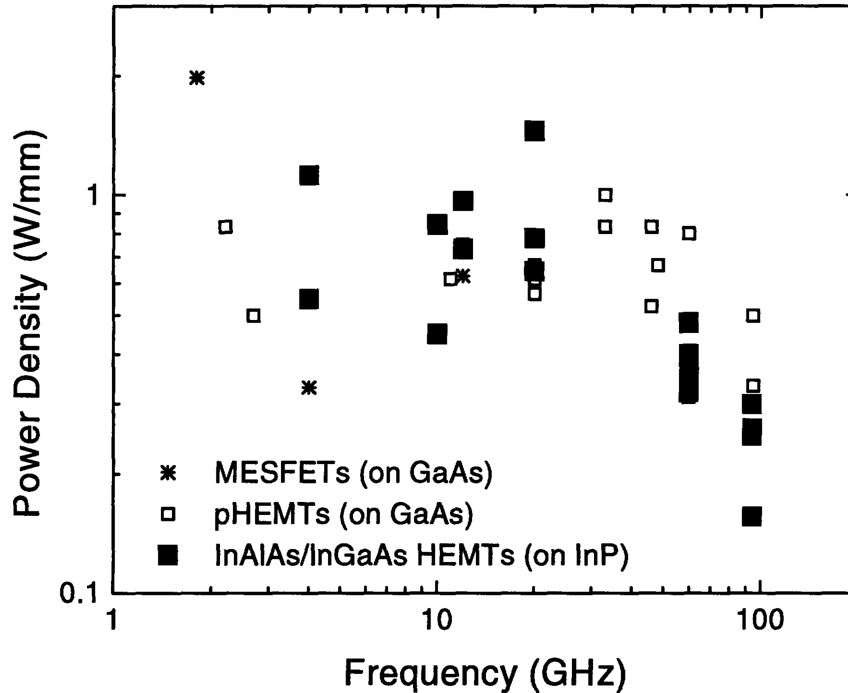


Figure 1.1: Power performance vs. frequency for various devices.

InGaAs and InAlAs provides for the formation of a dense two-dimensional electron gas in the channel [2]. These factors lead to large transconductance values, and this is key to the excellent frequency operation of the devices. Transconductances in 0.1 μm InAlAs/InGaAs HEMTs have been reported to be as high as 800 to 1000 mS/mm [2].

InP-based HEMTs have already proven their excellence as low-noise high-speed devices. At 60 GHz, they show impressive noise figures of 0.8 to 0.9 dB, about 0.7 dB better than devices in other leading millimeter wave technologies. At 95 GHz, they exhibit noise figures of 1.2 to 1.3 dB, beating the competition by about 0.9 dB [1].

Unfortunately, however, to date InAlAs/InGaAs HEMT have not fulfilled their promise as power devices. Fig. 1.1 shows a plot of reported power performance vs. frequency for millimeter-wave devices. We see that rather than dominating in high-power millimeter-wave performance, InP-based HEMTs in fact do not even achieve power performance as

high as is seen in AlGaAs/InGaAs pseudomorphic HEMTs (pHEMTs) fabricated on GaAs substrates. This is not what we expect, since devices in the InAlAs/InGaAs system should be able to beat other technologies in high-frequency power performance. Where is the problem? The biggest difficulty is that, as InAlAs/InGaAs HEMTs are an immature technology, issues critical to the power performance remain yet unresolved. Key understanding of the power-limiting mechanisms is lacking and, for the most part, no predictive models have been available. Conventional theories have been based substantially on knowledge of these mechanisms in MESFETs or GaAs pHEMTs but these theories have not been well-established in the InAlAs/InGaAs technology. This has hindered success in optimizing power performance.

How is the high-frequency power performance of a device assessed? Unfortunately, there is no unambiguous way. The ability of a device to deliver power depends strongly on the network in which the device is used and how the device is biased. Most commonly the power performance is quoted based on the power a device is able to deliver in Class A amplifier configuration. In this configuration, the maximum output power is related to the maximum current (I_{dmax}) and the drain-to-source breakdown voltage (BV_{DS}) by [8]

$$P_{MAX} \propto I_{dmax} BV_{DS}. \tag{1.1}$$

While this result is for Class A amplifier configuration, other configurations show similar dependence on I_{dmax} and BV_{DS}. Therefore, in order to understand the power limits of the device we must look at the mechanisms determining I_{dmax} and BV_{DS}.

In this work, we characterized state-of-the-art power millimeter-wave InAlAs/InGaAs HEMTs fabricated by Lockheed Martin to evaluate their power performance. We investigated the various theories for I_{dmax} and BV_{DS} and identified the dominant power-limiting mechanisms in these devices.

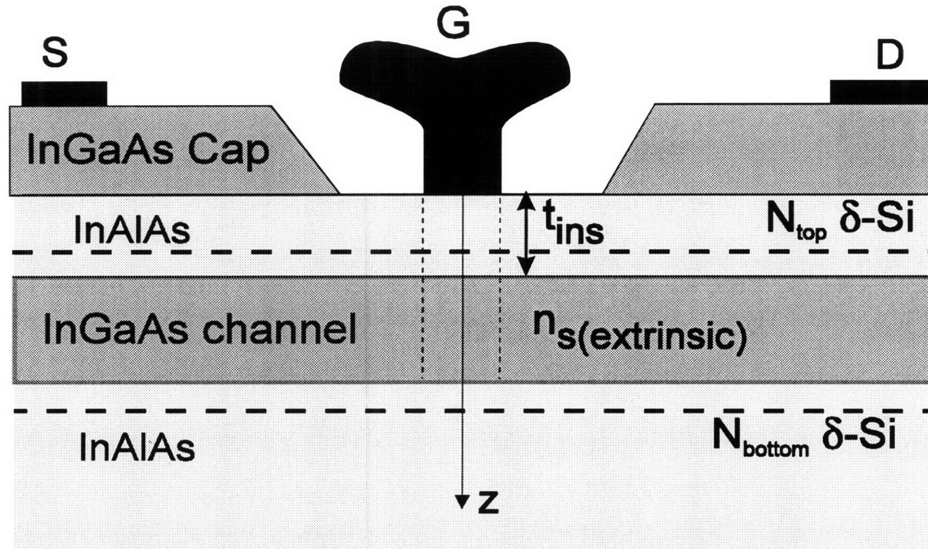


Figure 1.2: Cross-section of the double heterostructure HEMTs under study.

1.2 Device Description

HEMTs, which are also known as Modulation Doped Field Effect Transistors (MODFETs) and Two-dimensional Electron Gas Field Effect Transistors (TEGFETs or 2DEGFETs), differ from traditional Field Effect Transistors (FETs) in that the dopants are located in the insulator instead of the channel. A cross section of the HEMTs investigated in this study is shown in Fig. 1.2. InAlAs has a large bandgap and thus acts as an insulator, and InGaAs, which is a narrow bandgap material, is the conducting channel. The devices under study here are double heterostructure HEMTs, meaning that the n-type dopants (silicon atoms) are located in two delta doping layers, one above and one below the channel. These are labeled in Fig. 1.2 as N_{top} and N_{bottom}. The gate metal or metal alloy makes a Schottky (metal-semiconductor) junction at the InAlAs surface and the insulator is doped directly under the drain and source contacts to provide a good conducting path to the surface.

Table 1.1: Details of the structural parameters that varied across the sample set. All other parameters were constant across all of the wafers studied.

wafer number	$n_{s(extrinsic)}$ (T=300K) (x 10^{12} cm^{-2})	t_{ins} (Å)	top-to-bottom doping ratio
2720	3.35	190	3:2
2721	2.82	190	4:1
2722	3.06	190	4:1
2723	2.97	200	4:1
2724	3.15	210	4:1
2725	3.48	210	4:1
2726	3.23	200	4:1
2727	3.66	190	3:2

The sample set under study consisted of eight device wafers manufactured by Lockheed Martin. The fabrication process features a 0.1 μm gate length (L_G), thin undoped InGaAs cap, and a selective gate recess [9] which allows precise control of the threshold voltage (V_t) and the value of the sheet carrier concentration in the extrinsic channel ($n_{s(extrinsic)}$). The wafer set was designed specifically to test the effect of certain structural parameters on the power performance. These parameters are indicated in Fig. 1.2, and Table 1.1 enumerates the variations. $n_{s(extrinsic)}$ refers to the concentration of carriers in the capped InGaAs channel, that is, everywhere except directly beneath the gate. In this sample, $n_{s(extrinsic)}$ was experimentally varied between 2.82×10^{12} cm^{-2} and 3.66×10^{12} cm^{-2}. We refer to a sheet carrier concentration rather than a bulk concentration because the carriers ideally reside in a two-dimensional electron gas in the channel. Wafers in this sample were also made with different values of the insulator thickness (t_{ins}) and the top-to-bottom delta doping ratio was different on two of the wafers.

Fig. 1.3 shows two conduction band energy (E_C) diagrams detailing the operation of a typical device in this sample set. The diagrams are shown for a vertical cut through the gate as indicated in Fig. 1.2. These HEMTs are depletion-mode devices, meaning that at

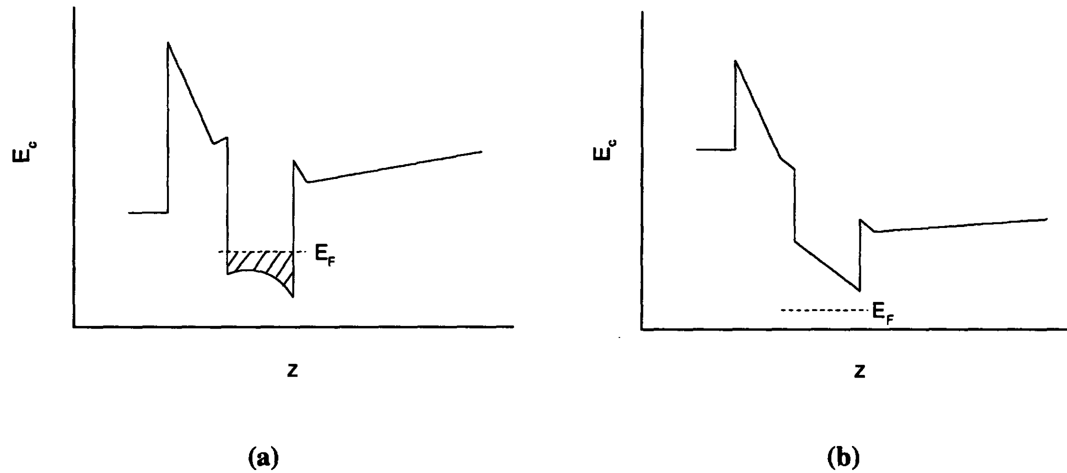


Figure 1.3: Conduction band diagram for a typical HEMT in this study. (a) The device is on and the channel is degenerate. (b) The device is off and the channel is depleted of electrons. The x-axis represents vertical distance into the HEMT from the gate to the substrate.

$V_{GS} = 0$ V the channel is on. At this bias, the carriers created in the doping layers reside in the InGaAs channel as a result of the energy configuration of the device. Looking vertically into the intrinsic device, we first notice the Schottky barrier at the gate-semiconductor interface. Looking specifically at Fig. 1.3(a) for the device in the on-state, the first well in the conduction band occurs at the location of the top delta doping layer. Next we observe the large conduction band discontinuity (ΔE_C) at the top InAlAs/InGaAs interface. Since the device is on, the channel is degenerate (E_C is below the Fermi level (E_F)), and there is band bending within the channel as a result of the electrons present there. We then see ΔE_C at the bottom InGaAs/InAlAs interface and the effect of the bottom delta doping.

When a sufficient negative voltage is applied to the gate, E_C is raised above E_F in the channel, it is depleted, and the device is therefore off. This is shown in Fig. 1.3(b).

1.3 Thesis Organization

Power performance is directly related to I_{dmax} and BV_{DS}. Thus, in Chapter 2 and 3 we discuss our investigation of these two parameters, respectively, in the devices in this sample set. In Chapter 2 we will see that the maximum current appears to be the result of velocity saturation in the extrinsic regime. In Chapter 3, a tunneling and thermionic field emission model will be shown to explain the BV and its temperature dependence. An important result of this work is developing design criteria for improving the power performance. Therefore, in Chapter 4, we look into the implications of our findings for device design to optimize power performance. Finally, in Chapter 5 we present the conclusions of this study and make suggestions for future research to deepen the understanding of the power limiting mechanisms in InAlAs/InGaAs HEMTs.

Chapter 2

Maximum Drain Current

2.1 Introduction

We first turn our attention to the maximum drain current a HEMT can support (I_{dmax}). In general, for a given drain-to-source voltage we expect to be able to drive more current as we increase the gate-to-source voltage (V_{GS}). However, experimentally it is found that there is an ultimate limit to the drain current. In Chapter 1 we showed that I_{dmax} is one of the critical parameters determining the maximum power handling. It is essential to understand the mechanisms resulting in I_{dmax} in order to optimize power performance in new designs.

Throughout our investigating the maximum drain current, a large focus will be on the transconductance, g_m, which is defined as

$$g_m = \left.\frac{dI_d}{dV_{GS}}\right|_{V_{DS}} . \tag{2.1}$$

Examining g_m will help us observe the details about how I_d responds to V_{GS}. In particular, we will define I_{dmax} at the point where g_m drops to zero. Additionally, however, the transconductance defines the power gain in the device, and thus it also of interest to us since the device is only useful in regimes where the gain is sufficiently high.

2.2 Theoretical

2.2.1 Conventional understanding

It is commonly believed that the drain current (I_d) in HEMTs is limited by turn-on of the parallel Metal Semiconductor FET (MESFET) in the top delta doped region in the intrinsic portion of the device. According to the theory, once V_{GS} becomes sufficiently positive the doped region becomes an alternative conduction path. This path has a much lower carrier mobility than the undoped channel, and therefore the current conducting through it is small compared to the current flowing in the channel. Additional V_{GS} modulates charge in the parallel MESFET rather than in the channel, and thus I_d reaches its maximum value [1 , 2].

2.2.2 An alternate theory: source resistance blow-up

The conventional understanding that the parallel MESFET mechanism is the cause of the drain current limit does not describe well what is seen in HEMTs designed for power applications. In order to explain results seen in power HEMTs, a more recent theory blames a different mechanism: source resistance blow-up [3 , 4].

The source resistance blow-up theory is based on the supposition that the carriers reach their saturation velocity (v_{sat}) in the extrinsic source region before the parallel MESFET turns on. In a HEMT designed for power applications, the extrinsic sheet carrier concentration ($n_{s(extrinsic)}$) is small and as a result the maximum current that this region can handle is not very large. The maximum current is set by v_{sat} and the carrier concentration. In particular, if these HEMTs are limited by velocity saturation in the extrinsic channel, the maximum I_d (per unit width) will be given by

$$I_{dmax} = qn_{s(extrinsic)}v_{sat}. \qquad (2.2)$$

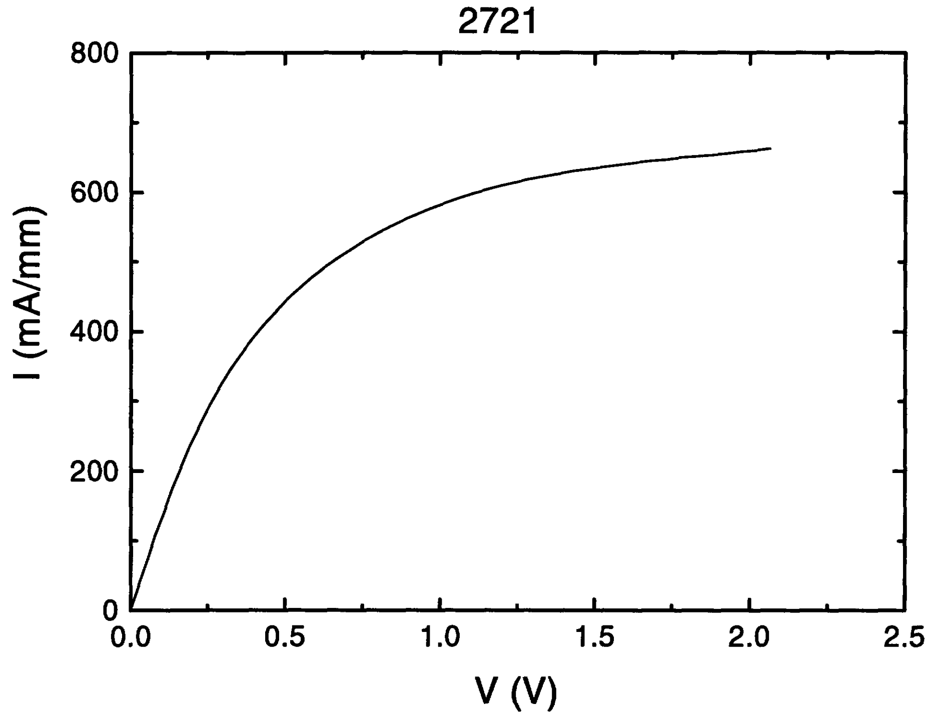


Figure 2.1: Current vs. field for a Transmission Line Model (TLM) test structure on Lockheed Martin sample 2721. Note the initial linear regime where the current is directly proportional to the field. At high fields, however, the current enters the saturation regime and becomes independent of applied voltage.

It is important to note that in discussing the source resistance blow-up, we are concerned with the small signal source resistance (r_s), which is described by

$$r_s = \frac{dV}{dI}. \tag{2.3}$$

In Fig. 2.1 we have plotted the current as a function of voltage for measurements on a Transmission Line Model (TLM) test structure (discussed later). Initially, transport takes place in the mobility-limited regime, and the current increases in direct proportion to the applied voltage. Because the velocity and the current increase linearly with the applied field, the small signal resistance (r) in this region is constant. However, as the carriers

begin to reach their saturation velocity, the current saturates to the value given by Eqn. 2.2. Correspondingly, r "blows-up" in this region.

Greenberg [4] showed that this source resistance blow-up results in a drop in the extrinsic transconductance of the device. The extrinsic transconductance (g_m) is related to the intrinsic transconductance (g_{mo}) and the source resistance by

$$g_m = \frac{g_{mo}}{1 + r_s g_{mo}}. \tag{2.4}$$

If r_s blow-up occurs at a low voltage, it can result in premature peaking of g_m followed by a rather steep drop. Of course, we will also observe a drop in the transconductance as a result of the parallel MESFET turning on. However, we can use the dependence of g_m on V_{GS} to understand which mechanism is responsible for limiting I_d, and see if in fact r_s blow-up is limiting the power gain in the devices.

2.3 Experimental

2.3.1 Transfer Characteristics

As a first investigation into the performance of the devices and the limits on I_{dmax}, the transfer characteristics were measured on several devices. Fig. 2.2 shows the transfer characteristics, $I_d(V_{gs})$ with V_{ds} as a parameter, for a typical device under study. As can be seen, the device turns on at a negative threshold voltage of about -1.3 V. The current initially grows fairly quickly as does its derivative, g_m. We notice that the current saturates to a value of about 900 mA/mm for V_{DS} = 2 V. We also notice that g_m peaks at -0.7 V. Similar results were seen across the sample set.

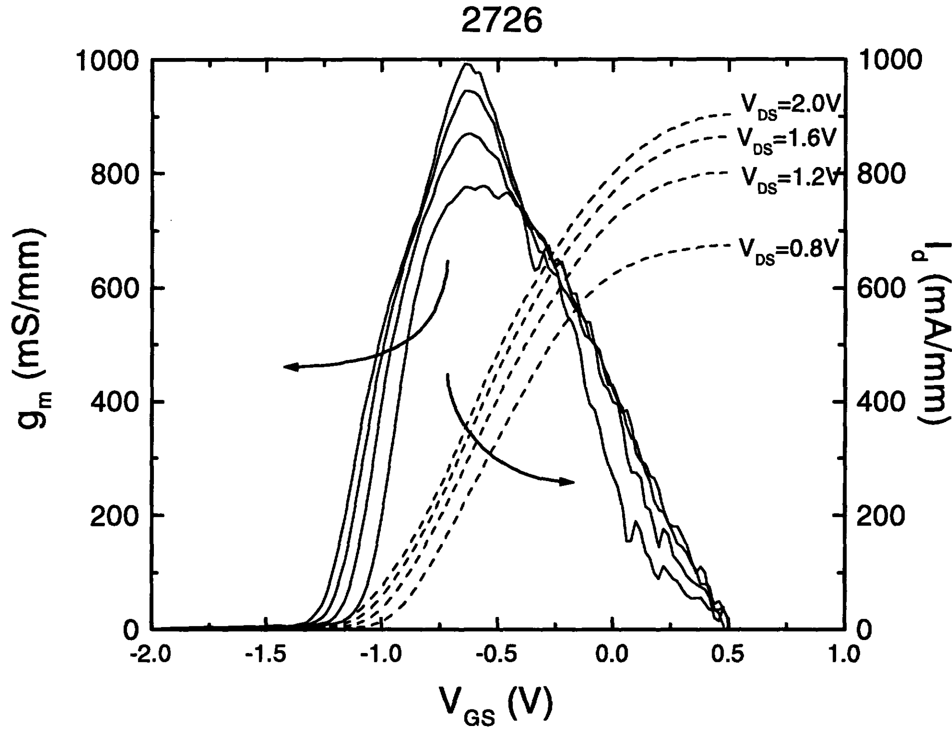


Figure 2.2: Transfer characteristics for one of the devices measured. Note that the extrinsic transconductance, g_m, peaks at $V_{GS} \approx -0.7$V, and I_d reaches a maximum at a low value of V_{GS}.

In order to investigate the expected intrinsic transconductance, we performed one-dimensional simulations of the device structure. These simulations take the parallel MESFET into account. The bias dependence of the sheet carrier concentration in the intrinsic channel was determined from quantum and classical simulations [5]. Then, assuming v_{sat} in the intrinsic channel as 2×10^7 cm/s, I_d and g_{mo} were calculated. Since these models are for the intrinsic transconductance, they do not take into account the current-limiting effects of velocity saturation in the extrinsic region.

In Fig. 2.3 we see g_{mo} theory lines generated from both models and g_m measured on one of the samples. We observe that g_{mo} rises quickly, flattens for a significant span of voltages, and then, at a V_{GS} significantly greater than 0 V, quickly drops due to the parallel MESFET. The two models agree fairly closely, but this is much different than the

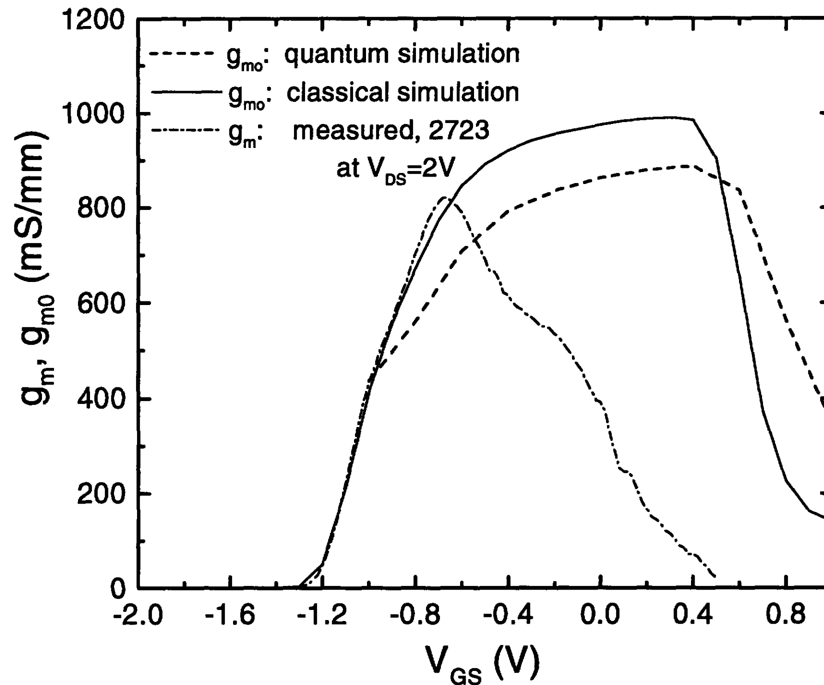


Figure 2.3: Results of simulations for sample 2723. Note that g_{mo} falls off at a larger voltage than is seen in the measured results.

measured transconductance. The measured g_m matches the theoretical g_{mo} in the initial stage, but then peaks and immediately falls off at a much smaller V_{GS}. Clearly, the parallel MESFET does not appear to be the dominant current-limiting mechanism in these HEMTs.

2.3.2 Determination of the source resistance (r_s)

Having concluded that the parallel MESFET theory is not appropriate for these devices, we turn our attention to velocity saturation. In order to investigate the impact of velocity saturation and r_s blow-up, we need to evaluate the current-voltage characteristics of the extrinsic source region. Unfortunately, it is difficult to isolate and measure this region or a similar region since it is only 0.7 μm long.

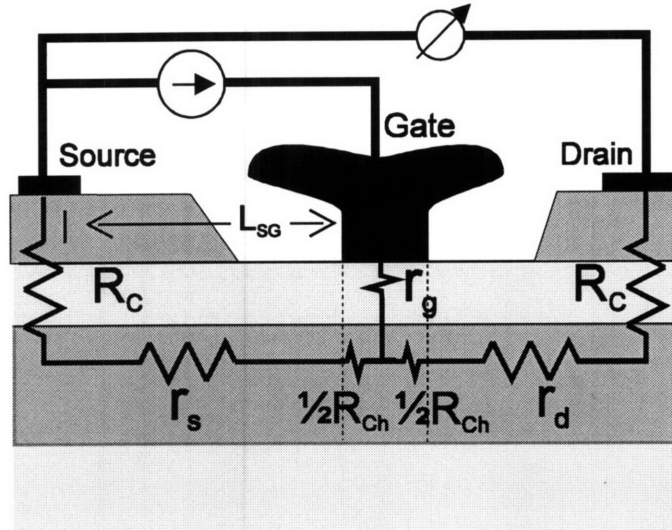


Figure 2.4: Cross-section of HEMT detailing the small signal source resistance.

Fig. 2.4 shows a cross section of our HEMT detailing the source resistance. The gate current injection technique can be used to measure r_s [6]. In this measurement, the source is grounded and the drain is left floating. A current source is placed between the gate and source, and we measure V_{DS}. As shown in Fig. 2.4, we now have a measurement of r_s, assuming we can independently measure the value of the contact resistance (R_C). However, we must note that at low currents there is also a contribution of $R_{ch}/2$, where R_{ch} is the intrinsic channel resistance. This contribution goes to zero at high currents when the gate is debiased [6].

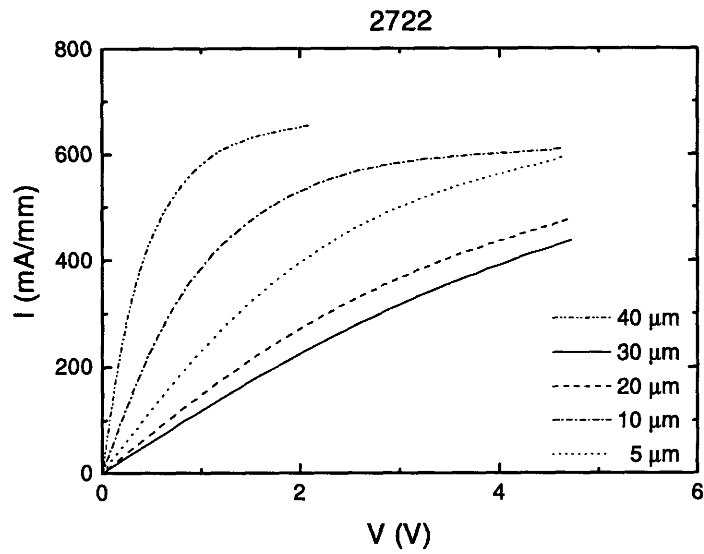
The gate current injection measurement was done on a few devices. Unfortunately, the gate can only a conduct a relatively small amount of current before it suffers catastrophic breakdown. Thus, the measurement does not give us a picture of what happens to the resistance at high currents, which is what is most important to this analysis.

Fortunately, there is another test structure on the wafer which we can use to extract current-voltage characteristics. The Transmission Line Model (TLM) test structure consists of a long region of semiconductor identical to the extrinsic regions of the devices. There are no gates, so the InGaAs cap extends across the entire TLM. At several points along the length of the TLM, contacts are made to the channel. The separation of these

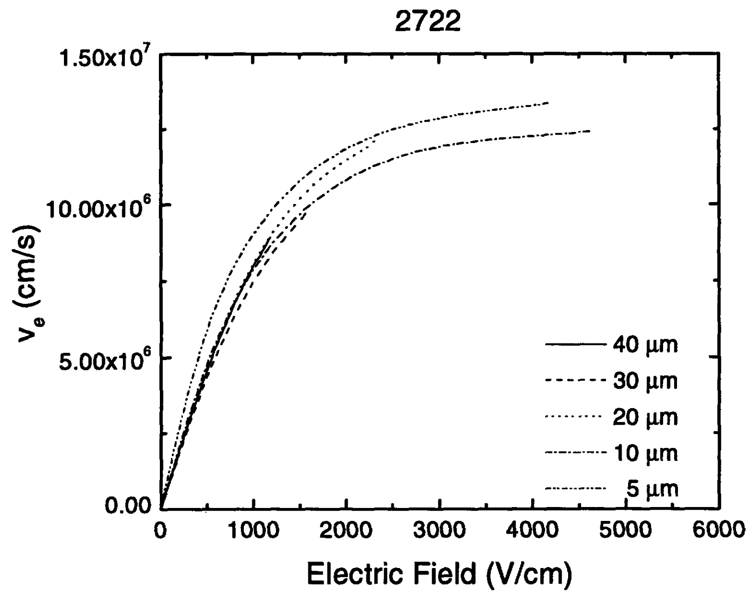
contacts steps though several values in order to allow the extraction of the specific contact resistance [7] and to identify the effects of changing length on the current-voltage characteristic of the channel. The measured current-voltage results can then be normalized to give the velocity-field (v-E) characteristics. Ideally, once the specific contact resistance has been eliminated, the v-E relation should be the same over any gap length since they should match the intrinsic characteristic of InGaAs. We can then use these results to determine the resistance characteristics of a region of any length.

Each die on the wafer included a TLM with five different separations ranging from 40 μm to 5 μm. Measurements were taken on many TLMs over the complete range of their lengths. Plotted in Fig. 2.5(a) are the I-V characteristics of a typical TLM. For low values, the current grows linearly with the voltage and this indeed is a mobility-limited regime. As the current increases, however, it begins to level off to its saturation value. After normalizing by the sheet carrier concentration ($n_{s(extrinsic)}$) and TLM lengths, we obtain the relationship between the carrier velocity and the electric field. The velocity-field characteristics for this TLM are seen in Fig. 2.5(b). Interestingly, the v-E characteristics are not entirely consistent across the different gap lengths. This is not what is expected from simple theory.

If the velocity-field characteristics were uniform across a gap of any length, it would be relatively simple to extract the current-dependent resistance characteristic of the short source-to-gate gap (denoted as L_{SG} in Fig. 2.4). Unfortunately, we do not have a single, clear picture of the v-E relation from the TLMs. Some of the error may be the result of imperfect pattern transfer which is inherent in processing. Such linewidth variation would be even more critical in the very short source-to-gate gap. A more critical non-ideality and one that is hard to include in modeling is the inconsistency in the saturation velocity. In fact, in previous work a higher v_{sat} has been observed in very short regions (on the order of 1 to 2 μm) than what is seen in large regions. This might be related to velocity overshoot at high electric fields over short distances [8].



(a)



(b)

Figure 2.5: Measurements for a typical TLM on wafer 2722. (a) Current-voltage characteristics. Note velocity saturation at a current level slightly greater than 600 mA/mm. (b) Velocity-field characteristics. Note that they do not overlap, and the saturation velocity does not appear to be consistent across the gaps.

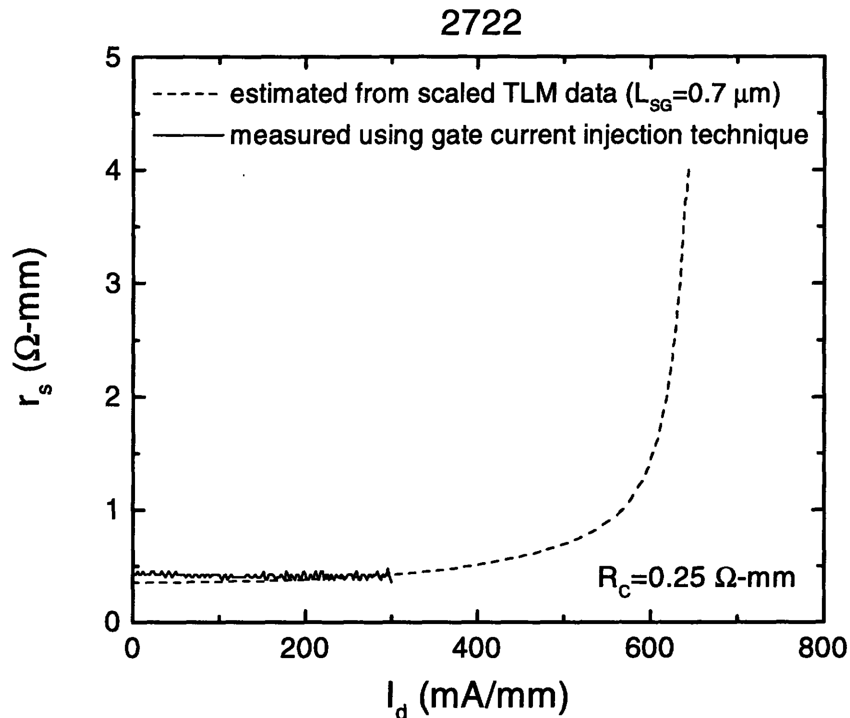


Figure 2.6: Source resistance vs. current: measured directly at low currents using the gate current injection technique; extrapolated from scaled TLM measurement at high currents.

In any case the TLM should give us a fair approximation to the v-E characteristic in the extrinsic source region. We will use measurements from the 5 μm TLM, as it is the shortest and closest to the L_{SG}, to extrapolate the current characteristic in that region.

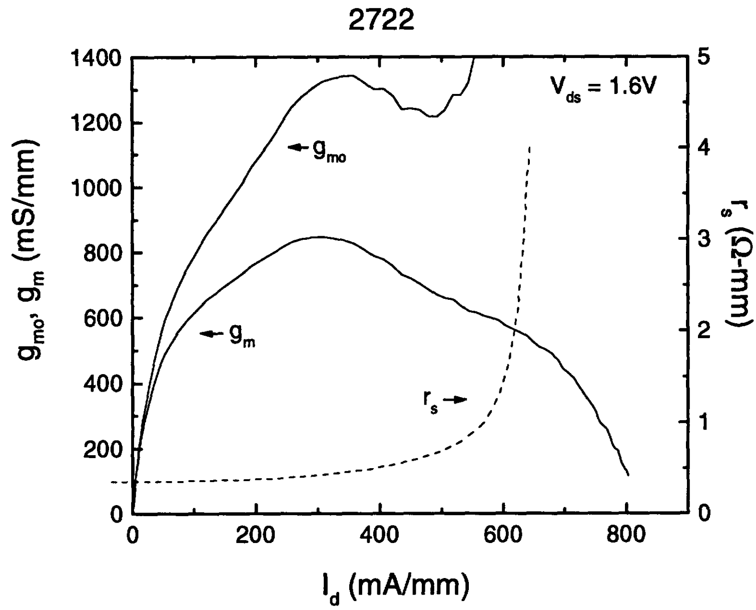
Shown in Fig. 2.6 is the extrapolated r_s as a function of current. The nominal value for L_{SG}, 0.7 μm, was used. We were not able to effectively extract R_C from the TLM measurements. So, we compared results for low currents from the gate current injection with the extrapolated 5 μm TLM measurement to determine R_C. To the first order, this should be a close approximation. A contact resistance of 0.25 Ω-mm provided a good match. We notice in Fig. 2.6 that for low currents r_s is constant at a low value. As the carriers begin to reach their saturation velocity, however, the resistance blows-up.

2.4 Discussion

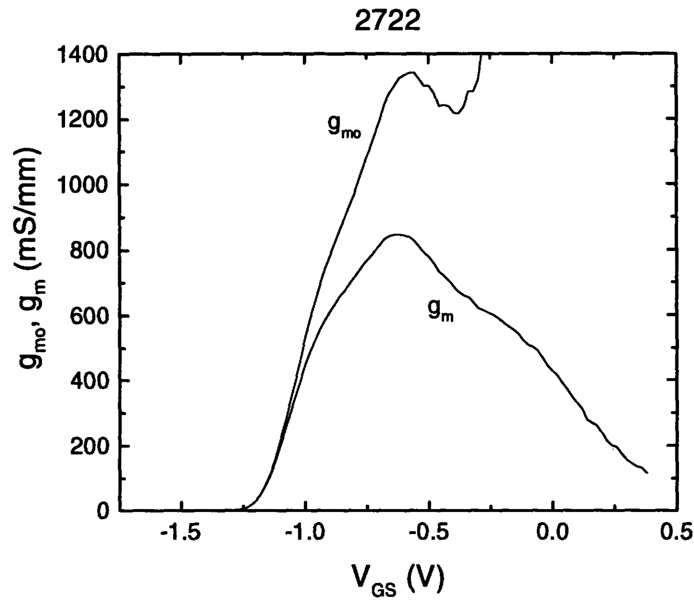
We have concluded that the parallel MESFET is not the dominant mechanism limiting the drain current in these devices. We have also taken measurements to examine the features of the current in the extrinsic source region. Here we evaluate the appropriateness of the model based on velocity saturation.

Unfortunately, we cannot directly measure the maximum current the extrinsic source region can handle. However, we can examine how the measured g_m deviates from the intrinsic g_{mo} to determine if this deviation corresponds to what we expect from source resistance blow-up.

In the first comparison, we use the extrapolated r_s and measured g_m to determine g_{mo} based on the r_s blow-up model [4]. We detail such a calculation in Fig. 2.7, where g_m is measured data, r_s is the extrapolated characteristic for $L_{SG} = 0.7$ μm, and g_{mo} is calculated based on Eqn. 2.4. The results are fairly good; for low currents, g_{mo} matches decently what would be expected in the intrinsic device where r_s blow-up has no impact. g_{mo} grows steadily and starts to flatten slightly in the area where the measured g_m starts to drop. Recall that simulations say that g_{mo} should be flat over a significant voltage range (Fig. 2.3). The model breaks down and results in unphysical values of g_{mo} above 500 mA/mm as r_s becomes too large. Note that the exact location of the blow-up in the source resistance critically impacts the calculated g_{mo} and remember that the extrapolated r_s is, of course, only an approximation. If v_{sat} is actually higher in the source-to-gate region, r_s blow-up would occur at a higher current. This actually is not an entirely unreasonable possibility when velocity overshoot is considered.



(a)



(b)

Figure 2.7 a and b: Measured transconductance and calculated intrinsic transconductance. The calculated data is a fair match to what is expected theoretically if source resistance blow-up were not occurring. The model breaks down at very high currents.

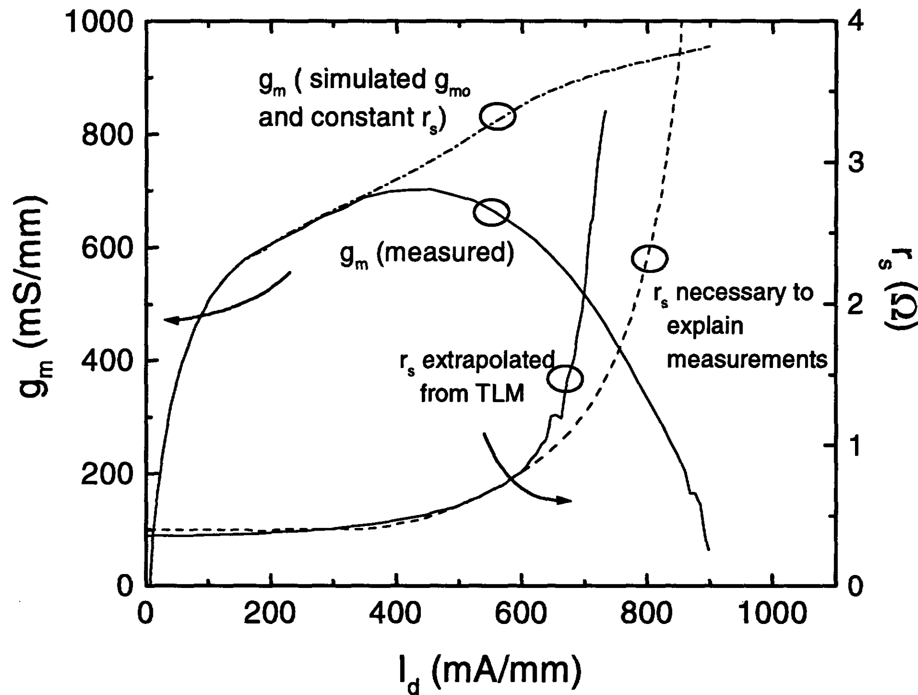


Figure 2.8: Alternative approach: g_m was calculated based on g_{mo} and a constant r_s; the r_s necessary to reconcile the newly calculated g_m and the measured g_m was then determined.

Approaching the problem from a different angle, we can use the measured g_m and simulated g_{mo} to calculate r_s. First, we assume that r_s remains constant at its low current value. We then use this r_s and g_{mo} from the classical simulations to determine the g_m that would be expected if r_s did not blow-up. Finally, we use Eqn. 2.4 to calculate the r_s curve that would be necessary to reconcile the calculated (theoretical) and measured g_m. This will show us the blow-up necessary to cause the drop we see in the measured g_m. Fig. 2.8 details this approach, showing the calculated and measured g_m curves along with the calculated r_s. We have also plotted the r_s we extrapolated from the TLM measurements for comparison purposes. The extrapolated and measured curves for r_s are indeed very close. We can see that the exact current where r_s blows up is critical in these calculations. In fact, the calculated r_s blows up at a slightly higher current than what we see in the

experimental extrapolation. This agrees with what would happen if the saturation velocity is higher in the very short source-to-gate region than in the 5 μm TLM.

2.5 Conclusion

We have found that velocity saturation in the extrinsic region appears to be the dominant current-limiting mechanism in Lockheed Martin's power HEMTs. Experimental results do not agree with what is expected from the parallel MESFET theory, but TLM measurements show that the maximum current that the extrinsic region can support is within the range of the maximum currents seen in the devices. Although we were unable to isolate the short source-to-gate region or another region of similar size to precisely determine its current characteristics, we were able to use scaled TLM measurements which provide a close approximation to r_s. The results agree very well with what is expected based on velocity saturation in the extrinsic channel.

Chapter 3

Breakdown Voltage

3.1 Introduction

We now turn our attention to the breakdown voltage. Breakdown can be understood several ways. Sometimes it refers to the voltage at which permanent damage is done to a device. In this research, we are not interested in catastrophic breakdown where the device is destroyed. Rather, our focus is on the voltage required to produce a certain gate current. Gate current should be nominally negligible, and designs assume this to be the case. If it becomes significant, charge storage capabilities degrade, the output conductance increases, and systems no longer operate as desired. We are interested in the off-state breakdown voltage since this breakdown voltage has the most direct effect on the power limits of a device. While there is no unambiguous definition for the off-state breakdown voltage, the criteria selected in this thesis is the standard gate current of 1 mA/mm.

Although the parameter of importance for determining the power performance of the transistor is the drain-to-source breakdown voltage (BV_{DS}), discussion of breakdown in this work will be primarily based on the drain-to-gate breakdown voltage (BV_{DG}). This is done because BV_{DG} is easier to measure. BV_{DS} represents the maximum voltage that can be applied to the output terminals of the device in the off-state with the gate current remaining below the defined breakdown level. The two breakdown voltages are related by

$$BV_{DS} = BV_{DG} + V_t. \qquad (2.1)$$

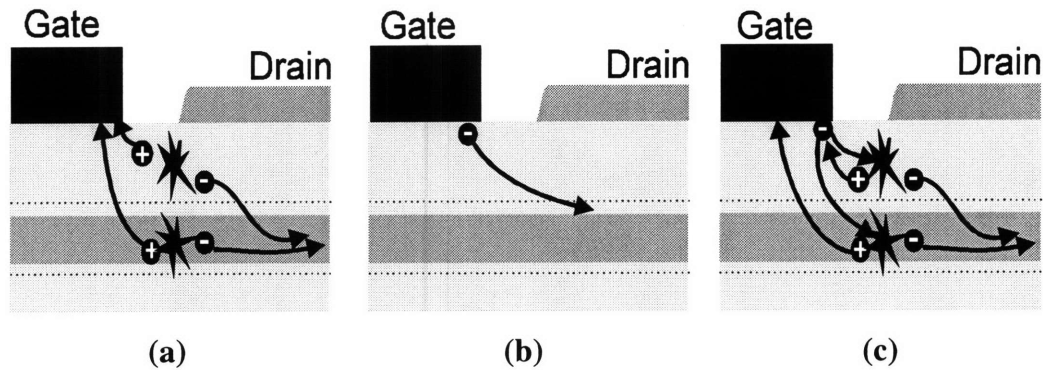


Figure 3.1: Investigations on breakdown have focused on three possible mechanisms: (a) impact ionization; (b) tunneling/ thermionic-field emission; (c) a combination of the two.

Thus, focusing on BV_{DG} is appropriate in evaluating the power performance of a device. In our devices, V_t is negative, so BV_{DS} will be less than BV_{DG}.

3.2 Theoretical

3.2.1 Conventional understanding

Originally, most understanding of breakdown in HEMTs was based on models developed for Metal Semiconductor FETs (MESFETs). Extensive research done into MESFET breakdown characteristics shows that impact ionization (as illustrated in Fig. 3.1(a)) is the dominant mechanism for breakdown, models based on this mechanism very well describe MESFET breakdown characteristics [1-3]. More recently, authors have appealed to a combination of tunneling and impact ionization with a fair bit of success (illustrated in Fig. 3.1(c)) [4].

3.2.2 New theory: tunneling/ thermionic-field emission

The applicability of MESFET models for breakdown to modern power HEMTs has recently come into doubt. Even before looking at the results of electrical measurements, we know that MESFETs have a significantly different structure and mode of operation than HEMTs. In contrast to HEMTs, there is no insulating layer in MESFETs. Also, the charge-control mechanism in a MESFET is the modulation of a depletion region formed at the metal-semiconductor junction. In a HEMT, the charge-control mechanism is the modulation of charge in an inversion layer formed in a channel that is separated from the metal-semiconductor junction by a wide bandgap material.

Additionally, experimental evidence reveals that the breakdown voltage in InAlAs/ InGaAs Heterostructure FETs (HFETs) has a negative temperature coefficient [4]. This would suggest that impact ionization cannot be involved in a significant way. However, there is some debate about the temperature dependence of impact ionization in the InGaAs system. The temperature coefficient (TC) of impact ionization in GaAs is known to be negative, while in InAs it is known to be positive [5, 6]. This leaves a large uncertainty in the expected TC of impact ionization in InGaAs. Recent measurements suggest that it is positive for InGaAs of a lattice-matched composition to InP [7].

A new theory has been recently introduced which explains experimental results and provides a good predictive model for the breakdown voltage in HEMTs. This theory, presented by Somerville and del Alamo, states that tunneling and thermionic-field emission (TFE) (illustrated in Fig. 3.1(b)) are the primary mechanisms responsible for breakdown gate current in HEMTs, not impact ionization [8].

Under this theory, the field configuration under the metal gate is the primary factor for determining current. Tunneling current is solely based on the field and therefore has no temperature activated component, while TFE depends on the field and T. This theory is consistent with the negative TC of BV. Evaluating the field configuration under the gate

is the first step in calculating the tunneling/ TFE current through the gate. As presented by Somerville, when the device approaches breakdown, the field under the gate is concentrated at the drain end of the gate. This occurs because a depletion region opens in the channel on the drain side of the gate after the channel has been completely depleted. The drain-end peak is the most important aspect of the field configuration for evaluating the current. Once the field in this region is known, and the value of the Schottky barrier height (ϕ_B) has been determined, calculating the gate current is a straightforward task [8].

In order to investigate the effects of various parameters on the field configuration under the gate, Somerville performed several two-dimensional simulations of various device structures. The sheet carrier concentration in the extrinsic region ($n_{s(extrinsic)}$) was found to be the only structural parameter that has a significant effect on the magnitude of the field underneath the gate. Other parameters, such as the insulator thickness, delta doping ratio, channel thickness, and gate length, have much less significant effects on the breakdown voltage [8].

Somerville's work very well explains the trends seen in experimental evidence for the many devices already in the literature. Measurements have been done on the Lockheed Martin sample set of this work to determine if, in fact, the tunneling/ TFE theory holds in these state-of-the-art devices.

3.3 Experimental

Extensive BV measurements have been carried out on our sample set. Breakdown measurements were made primarily by two methods: the two-terminal reverse diode measurement and the three-terminal drain current injection technique. Preliminary measurements were done at room temperature using a Karl Suss prober. Temperature dependence measurements were also carried out using a Cascade prober with Temptronix

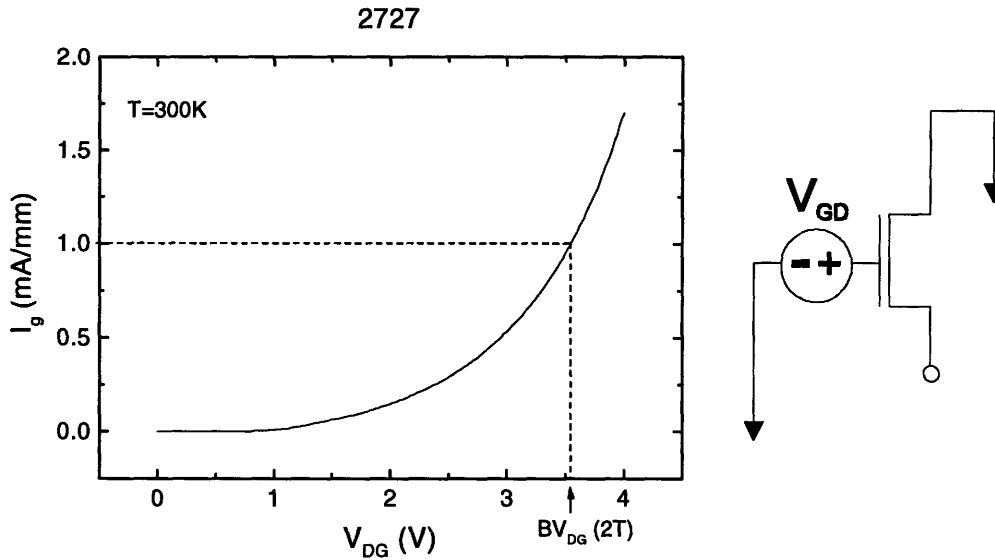


Figure 3.2: Two-terminal breakdown voltage measurement. The source floats and the reverse drain-gate diode I-V characteristics are found. $BV_{DG}(2T)$ is extracted at $I_g = 1$ mA/mm.

temperature controlling system. The system had the capabilities of measuring devices over a temperature range of -65°C to 200°C, but our measurements only went up to 95°C to ensure that the devices were not damaged since they were not passivated.

3.3.1 Two- and Three-terminal measurement techniques

The two-terminal reverse diode technique is the conventional method for determining breakdown in HEMTs. A schematic and typical result for this measurement are shown in Fig. 3.2. In this measurement test probes are placed on the drain and gate of the transistor and the source is left floating. In this way, the reverse diode characteristics of the drain-gate Schottky diode can be determined. The voltage corresponding to 1 mA/mm of gate current is chosen as the breakdown voltage of the device. Since this method only measures the reverse characteristics of the diode between the drain and the gate, it does not take into account any effects of the source or of breakdown in the channel.

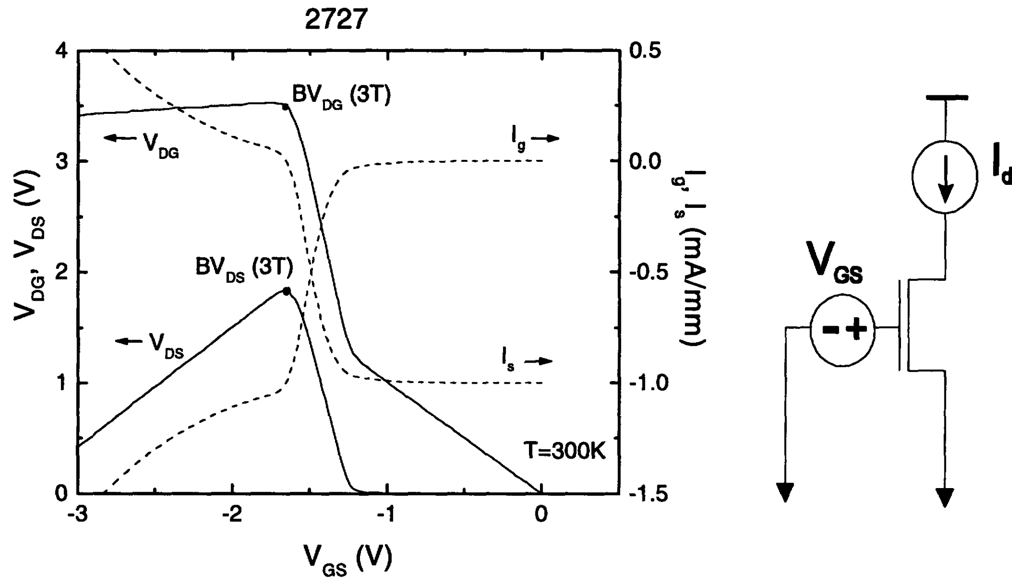


Figure 3.3: Three-terminal breakdown voltage measurement (drain current injection technique). 1 mA/mm is injected into the drain and V_{GS} is swept negative from 0V. BV_{DG}(3T) is extracted at the point where $I_S = 0$ and BV_{DS}(3T) is extracted at the peak of V_{DS}.

The three-terminal drain current injection technique provides a more complete determination of BV [9]. In this technique, as seen in Fig. 3.3, all three terminals of the device are probed, and 1 mA/mm is injected into the drain. Initially $V_{GS} = 0$ V. Since these HEMTs are depletion-mode devices, the channel is initially on. V_{GS} is then swept negatively well past the threshold voltage. The full 1 mA/mm initially flows through the channel and into the source, and the gate current (I_G) is negligible. As V_{GS} reaches V_t, the device turns off. The source current (I_S) drops and I_G increases correspondingly. Eventually, I_S drops to 0 and the entire 1 mA/mm flows through the gate. BV_{DG} is extracted at this point. BV_{DS} is extracted as the maximum value of V_{DS}.

Since the drain current injection technique makes use of all three terminals of the device, it takes into account the effect of the source in the measurement and the possibility of breakdown in the channel impacting BV.

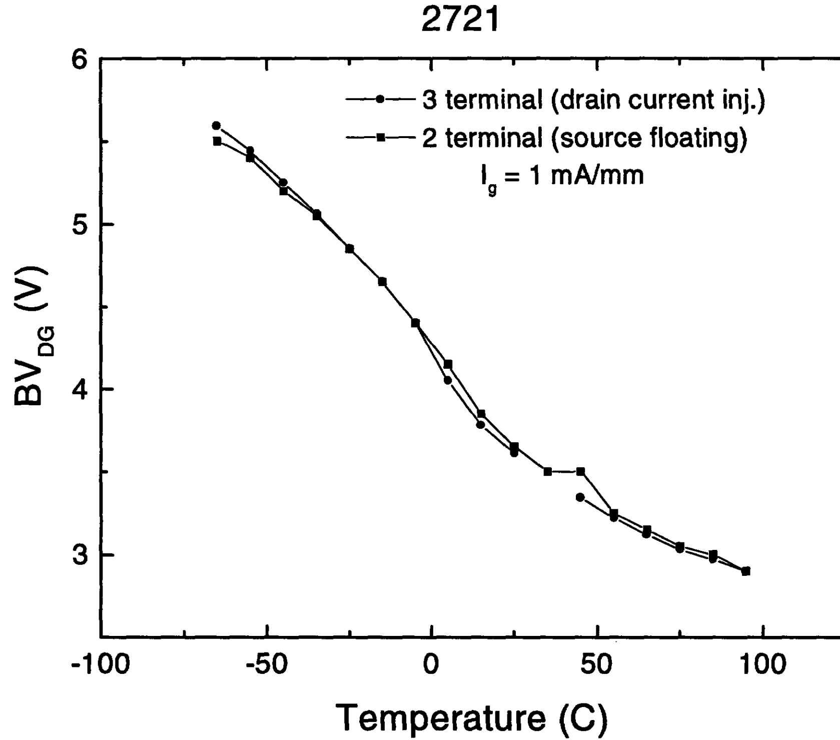


Figure 3.4: BV_{DG} vs. temperature for one of the devices under study. Both two- and three-terminal measurements are plotted. The correlation is excellent, indicating that breakdown is a drain-to-gate phenomenon.

Many devices in the sample set have been measured using both techniques. The correlation of the two is excellent, as seen plotted for one of the devices as a function of temperature in Fig. 3.4. Most significantly, this indicates that the breakdown path in these devices is strictly through the drain-to-gate diode, as has been noted in previous work [4]. Also, it validates that the two-terminal reverse diode measurement is appropriate to determine the breakdown voltage of the device. This is useful because it is a fast and simple measurement.

BV measurements were done on a large number of devices over the sample set. Fig 3.5 shows BV_{DG} vs. the extrinsic sheet carrier concentration ($n_{s(extrinsic)}$) for an investigation over our entire wafer set. Each point represents the average of a statistical measurement

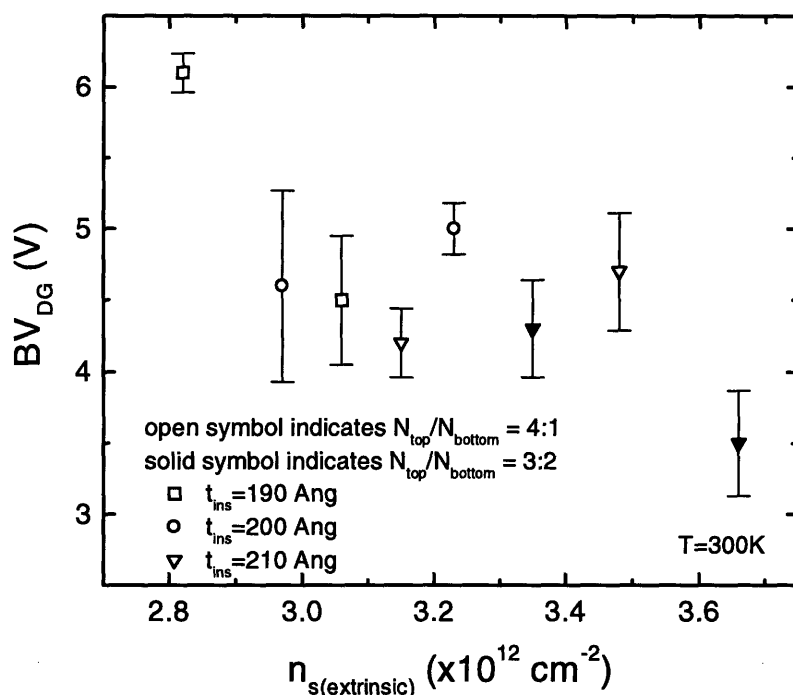


Figure 3.5: BV_{DG} vs. $n_{s(extrinsic)}$ for several devices on each wafer in the sample set. The trend toward an inverse relation is seen between BV and $n_{s(extrinsic)}$.

of devices on each wafer. The error bars denote the standard deviation across the set of measurements. Each of the points is also encoded to identify the other parameters that changed across the sample set.

3.3.2 Temperature Dependence

Temperature dependence measurements allowed the control and variation of a critical parameter in evaluating the thermionic-field emission portion of the gate current. Understanding the temperature dependence of breakdown is also important in itself since power HEMTs operate in significantly cold and hot environments.

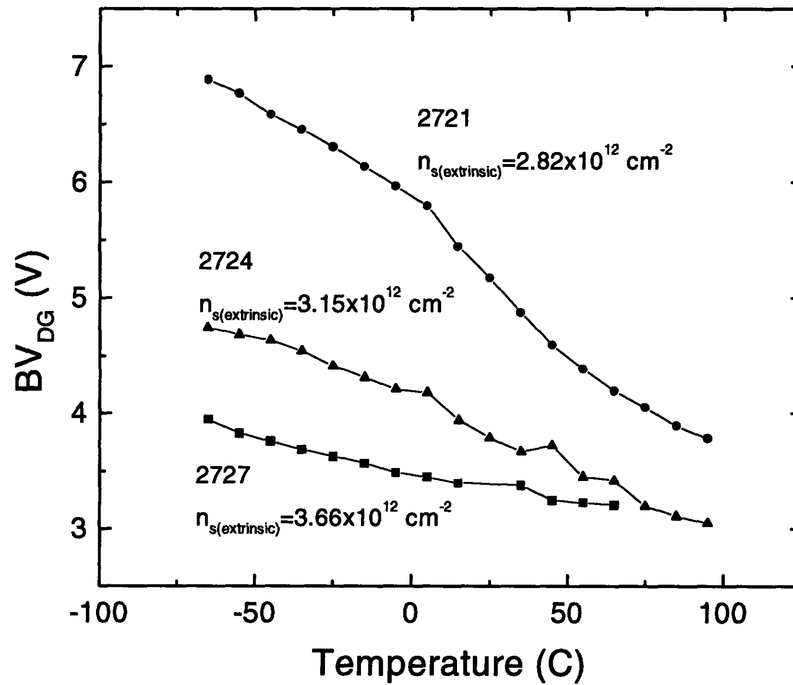


Figure 3.6: Temperature dependence of BV_{DG} on three samples.

Fig 3.6 shows the temperature dependence of devices on three of the wafers in our sample set. The selection corresponds to the lowest and highest values of $n_{s(extrinsic)}$ and one in between. BV has a negative temperature dependence, and the temperature coefficient increases for smaller values of $n_{s(extrinsic)}$.

3.4: Discussion

Several device structural parameters were varied over the sample set which provided many avenues of investigation. Most significantly, the extrinsic sheet carrier concentration varied over a significant range. The effects of changes in the insulator thickness, delta doping ratio, and recess etch time could also be investigated in our sample set.

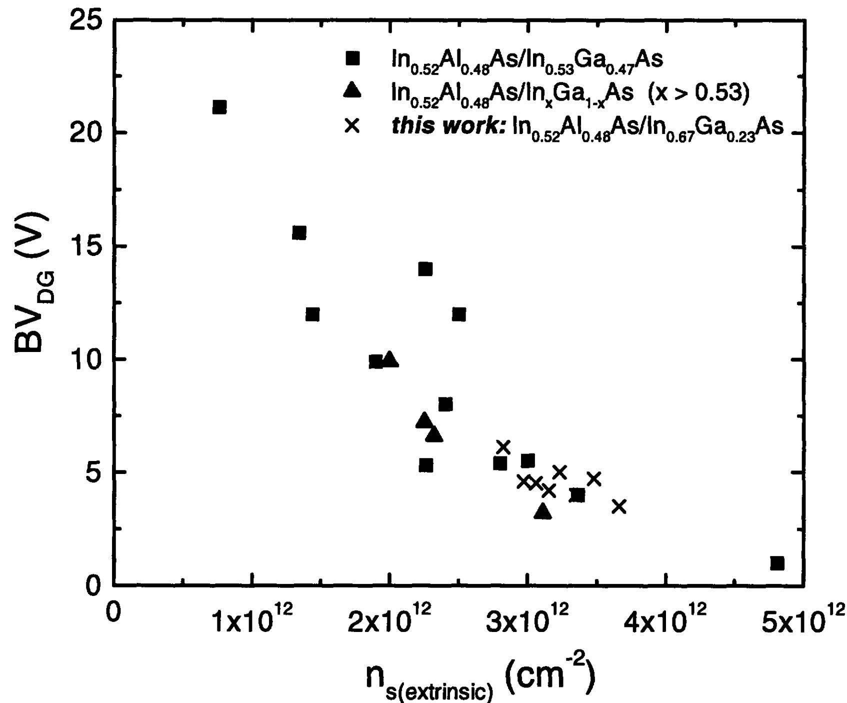


Figure 3.7: BV_{DG} vs. $n_{s(extrinsic)}$ for devices in the literature. A nearly universal inverse relationship between BV_{DG} and $n_{s(extrinsic)}$ emerges.

The tunneling/ TFE theory expects a nearly inverse relationship between the breakdown voltage and sheet carrier concentration, $n_{s(extrinsic)}$ [8]. Fig. 3.5 shows a plot of BV_{DG} vs. $n_{s(extrinsic)}$ for a large selection of devices measured at room temperature. The trend is toward an inverse relationship as expected.

If we compare the average BV_{DG} value versus $n_{s(extrinsic)}$ with a summary plot of devices seen in the literature, the Lockheed Martin samples fall very well into the greater trend seen in publication. Fig. 3.7 shows such a plot.

The points in Fig. 3.5 are coded to denote the various values of the insulator thickness and delta doping ratio. There does not appear to be any correlation between those parameters and the breakdown voltage. This can be seen more clearly with regard to the variation of the insulator thickness if we focus on four wafers with similar $n_{s(extrinsic)}$ values but different

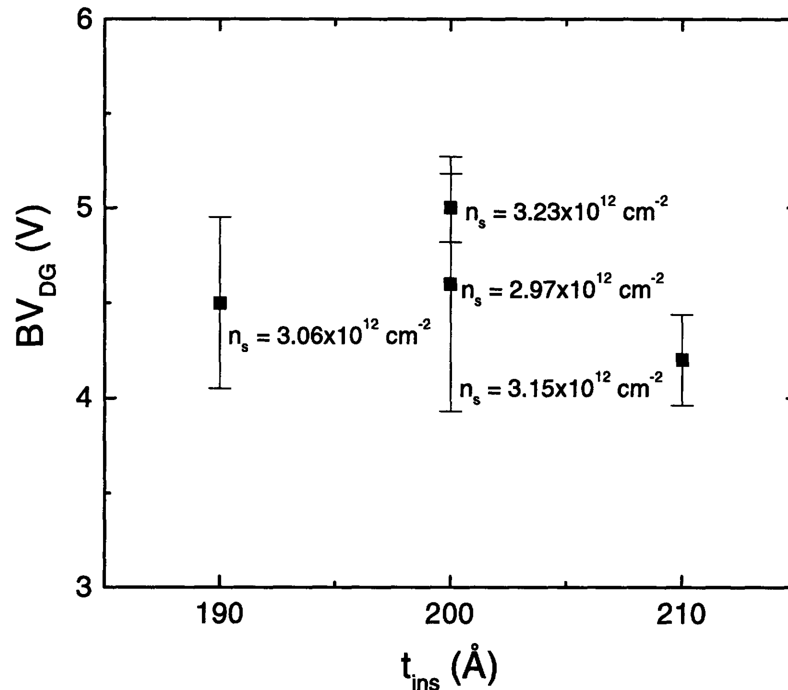


Figure 3.8: BV_{DG} vs. insulator thickness for four of the samples. No significant trend is seen.

values of t_{ins}. Unlike what was seen with $n_{s(extrinsic)}$, there does not appear to be a significant trend (Fig. 3.8).

Looking at the temperature dependence measurements gives us a more expanded understanding of the mechanisms responsible for breakdown in these HEMTs. In Fig. 3.6, we observed that BV_{DG} has a negative temperature coefficient (TC) and that the TC is smaller for higher values of $n_{s(extrinsic)}$. It is sensible at first sight that the temperature coefficient goes down for samples with a higher value of $n_{s(extrinsic)}$. In these HEMTs, tunneling, which is not thermally activated, plays a more significant role in the gate current and therefore the temperature effects are reduced.

As a further investigation of the tunneling/ TFE model, we looked at the evolution of I_G as a function of temperature at carefully chosen bias voltages on three of the wafers. Devices on all three wafers should have identical values of ϕ_B. If the gate current in these HEMTs

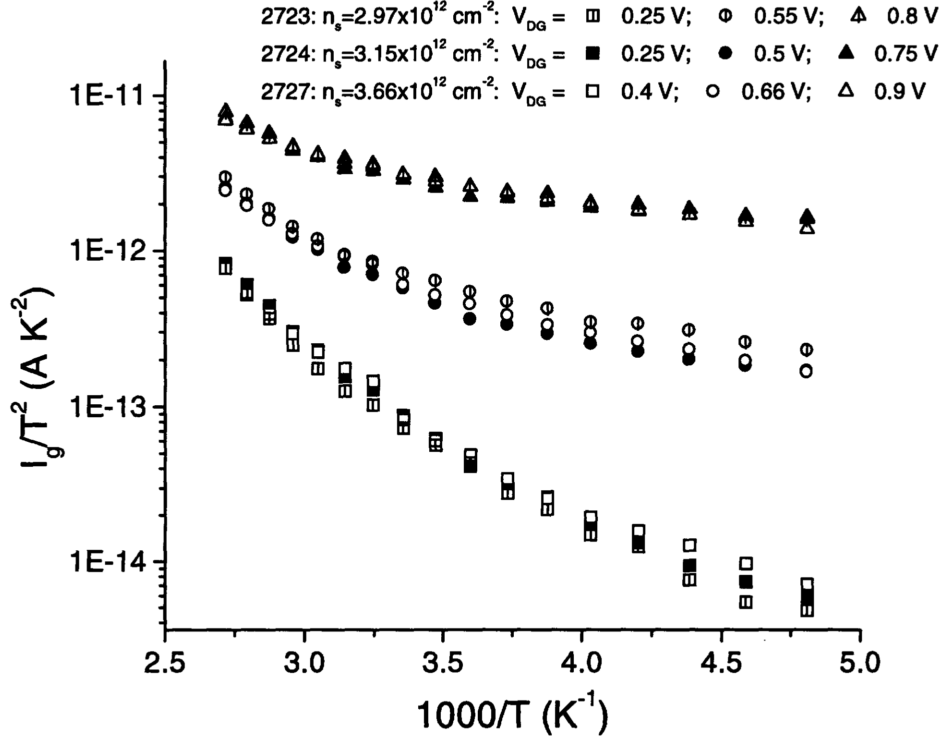


Figure 3.9: Arrhenius plot of I_G across three samples showing universal behavior. V_{DG} is chosen for matching the currents at room temperature. With the currents matched at one temperature, they stay matched at all temperatures.

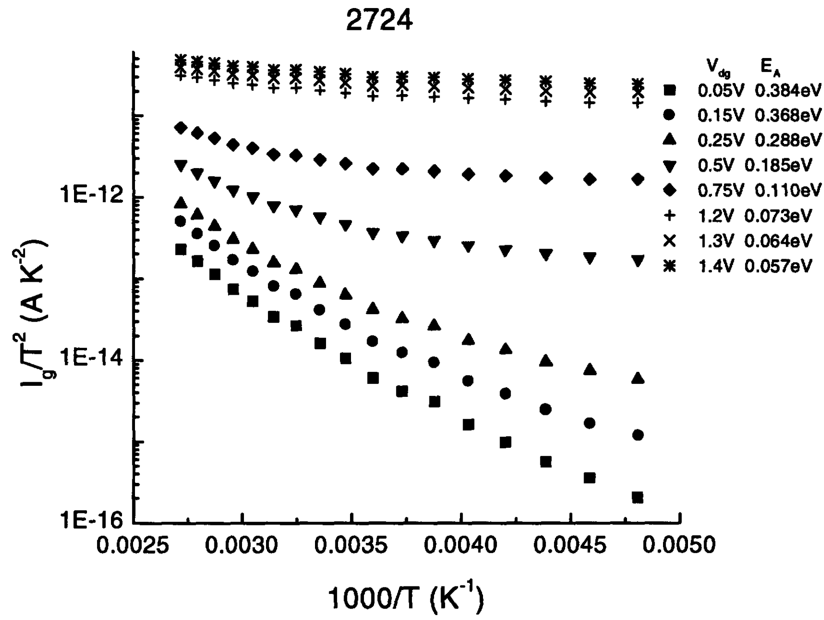
is determined primarily by tunneling and thermionic-field emission in the gate Schottky diode, I_G and its evolution with temperature should match across the samples if the field configuration under the gate is the same. We chose V_{DG} such that I_G matched across the different samples at a given temperature. This establishes that the field configuration under the gate is identical on the different devices. We then varied the temperature and found that the evolution of those gate currents with temperature also matched. This "universal" behavior is shown in Fig. 3.9.

All indications support that tunneling/ TFE is the dominant mechanism responsible for the gate current in the HEMTs being studied. But in order for the theory to be truly valid and

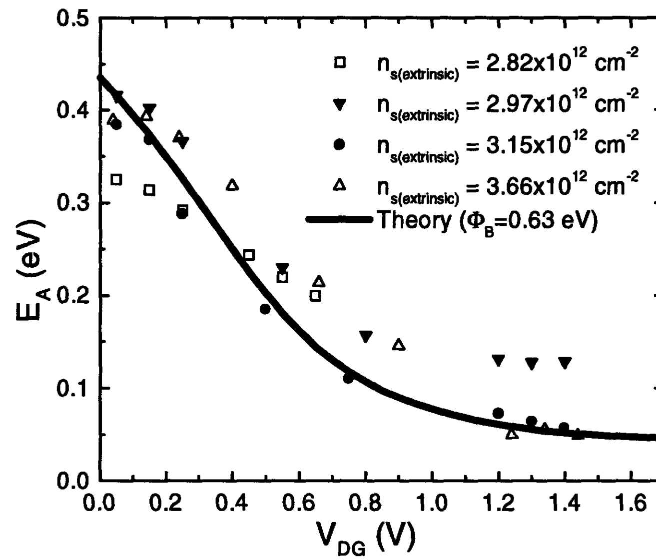
fill the needed gap in understanding of BV for design purposes, it is essential that a quantitative predictive model be developed based on this mechanism.

The model only needs two parameters in order to calculate the gate current, the Schottky barrier height, ϕ_B, and $n_{s(extrinsic)}$. The extrinsic sheet carrier concentration for each of the wafers is measured by the grower, but we need to determine ϕ_B for this gate metal-semiconductor junction. In order to extract ϕ_B for this system, measurements were done using Arrhenius plots of I_G such as the one seen in Fig. 3.10(a). The bias dependence of the effective activation energy (E_A) was determined for low values of V_{DG} where the channel is only partially depleted (the channel is in the "on" state). As illustrated in Fig. 3.10(b), we combine this with the bias dependence of E_A extracted from theoretical calculations and determine $\phi_B = 0.63$ eV. This is within a reasonable range for the materials used [10].

Now, with the extracted value of ϕ_B and the values of $n_{s(extrinsic)}$ known for each sample, the gate current can be predicted using the tunneling/ TFE model. Shown in Fig. 3.11 is the bias dependence of the gate current on one device near the two temperature extremes. We see that the theory almost perfectly predicts the gate current. Note that for low values of V_{DG}, the gate current increases with a large slope. As V_{DG} increases past the threshold voltage, the slope flattens because a portion of V_{DG} is used to open a depletion region in the channel on the drain side of the gate. The theory lines only begin to deviate at high currents. This may be due to the onset of impact ionization in the channel. This is, however, beyond the region we are mainly interested in since BV is defined at 1 mA/mm of gate current.



(a)



(b)

Figure 3.10: Extraction of ϕ_B: (a) Arrhenius plot of the gate current on one sample at various values of V_{DG} to extract bias dependence of effective activation energy; (b) bias dependence of activation energy over several samples used to determine Schottky barrier height.

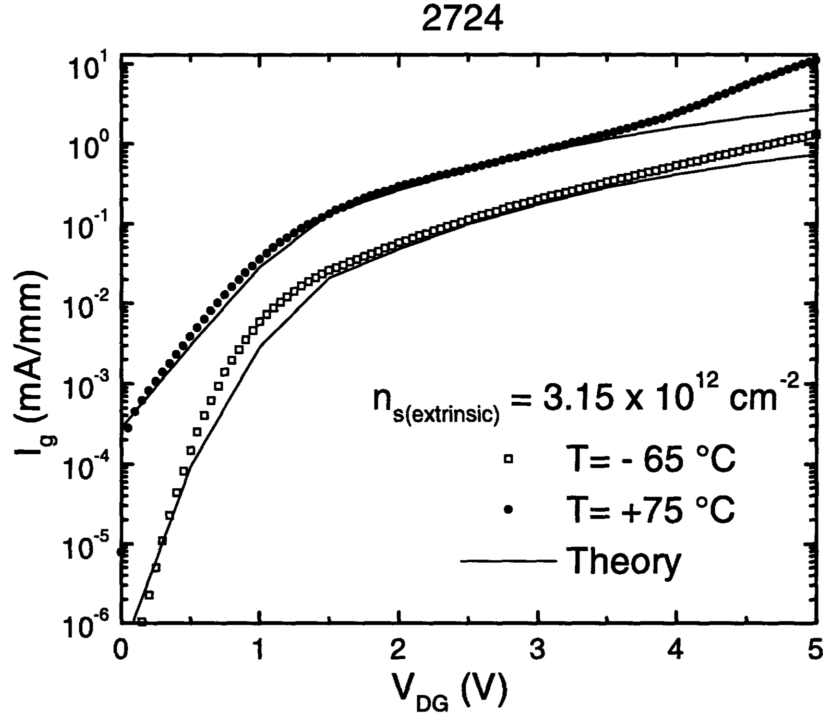


Figure 3.11: Bias dependence of gate current. Note excellent agreement between measurements and theory.

Finally, and most importantly, Fig. 3.12 shows a comparison between the measured BV and the prediction of the theory for three samples over the entire temperature range of the study. The theory correctly predicts the temperature dependence of BV, the reduction of the temperature coefficient with increasing $n_{s(extrinsic)}$, and even very closely predicts the actual values of the breakdown voltage. This is a significant result, especially considering that the only parameters are the Schottky barrier height and the sheet carrier concentration. No other device structural or fitting parameters are used in the calculations.

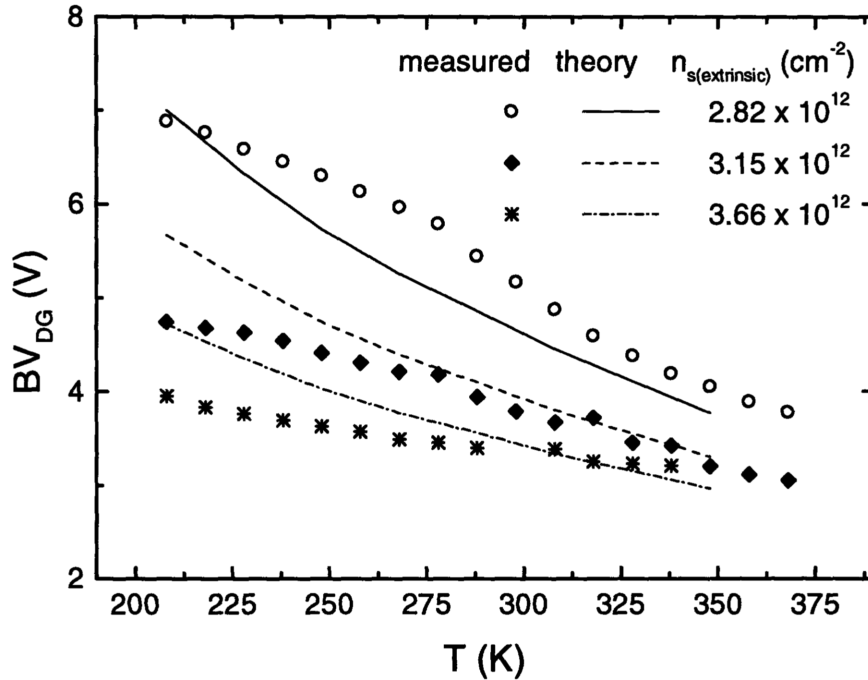


Figure 3.12: BV_{DG} vs. T for three samples: measurements and theory. Note theory correctly predicts temperature dependence and even fairly well predicts the actual values of BV_{DG}!

3.5 Conclusion

The experimental data collected over the sample set, which are also presented in [11], agree very closely with the new theory presented for the breakdown voltage. BV is inversely related to the value of the extrinsic sheet carrier concentration ($n_{s(extrinsic)}$) and other device structural parameters have little impact on BV. Breakdown has a negative temperature dependence and the absolute magnitude of the temperature coefficient increase for lower values of $n_{s(extrinsic)}$.

The theory also provides excellent quantitative predictive abilities. Calculations based on the theory very well predict the reverse diode current in the gate-drain diode over a large bias range and at the extremes of the temperature range investigated. The simple theory correctly predicts the temperature dependence of BV and the increase in the temperature

coefficient with smaller values of $n_{s(extrinsic)}$. Most importantly, it fairly well predicts actual values of the breakdown voltage.

Chapter 4

Implications to Device Design

4.1 Introduction

In the previous two chapters we presented our investigation of the two primary factors establishing power limits in our sample of Lockheed Martin HEMTs: the maximum drain current and the off-state breakdown voltage. Our research has given us a good understanding of the dominant mechanisms determining each of the parameters. Improving the power performance is essential to making InAlAs/InGaAs HEMTs a useful millimeter-wave device, and, as discussed in chapter 1, improving the power limit requires increasing both I_{dmax} and BV_{DS}. In this chapter we investigate the implications and applications of our conclusions on future device design.

We have found that I_{dmax} appears to be set by velocity saturation in the extrinsic region of the device. In Eqn. 2.2, we showed that the maximum current the extrinsic region is capable of conducting is proportional to the sheet carrier concentration and the electron saturation velocity. This result is shown graphically in Fig. 4.1. To improve I_{dmax}, we must increase either $n_{s(extrinsic)}$ or v_{sat}. Increasing $n_{s(extrinsic)}$ is feasible through enhanced doping of the delta doped layers. Increasing v_{sat} is not possible without altering the channel composition or using a different material.

As for breakdown, we concluded that BV_{DG} (and, equivalently, BV_{DS}) is determined primarily by tunneling and thermionic-field emission through the gate. According to the theory, $n_{s(extrinsic)}$ and the Schottky barrier height of the gate are the only structural device parameters that significantly impact the breakdown voltage. In Fig. 4.2 we have plotted

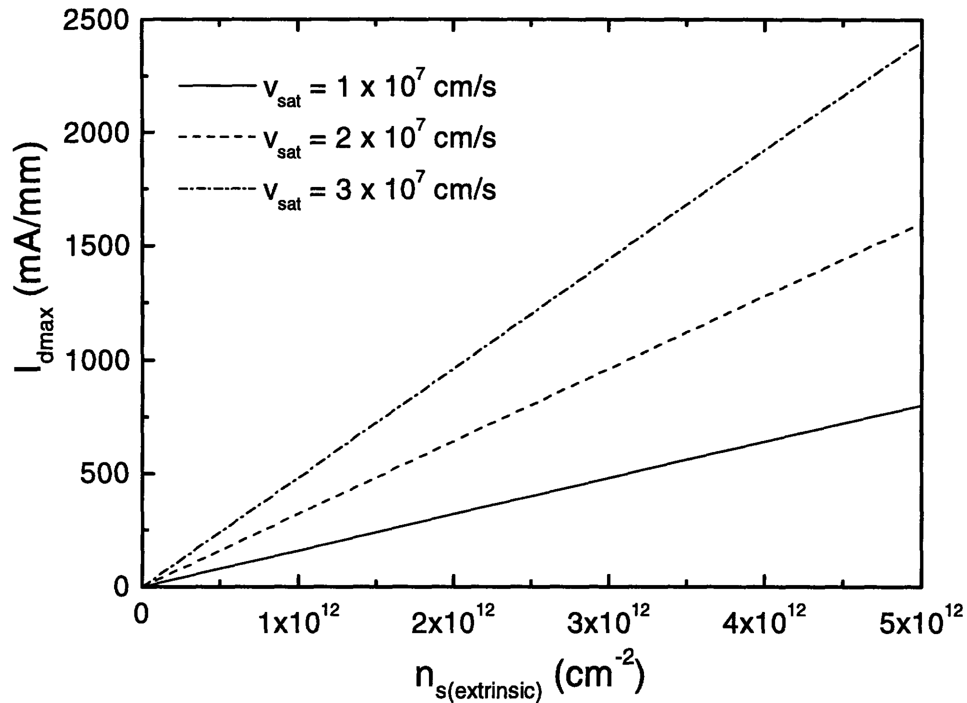


Figure 4.1: Theoretical I_{dmax} for extrinsic region velocity saturation model.

theoretical results of BV_{DG} vs. $n_{s(extrinsic)}$ at room temperature for various values of ϕ_B. BV_{DG} shows an inverse relationship to $n_{s(extrinsic)}$, but improves with a larger ϕ_B [1, 2]. In order to improve the breakdown voltage we need to decrease $n_{s(extrinsic)}$ or increase ϕ_B. Adjusting $n_{s(extrinsic)}$ is, once again, a straightforward design change. Engineering ϕ_B in a significant way is not easy as it is set to the first order by Fermi level pinning at the surface of the insulator. Careful selection of gate metal and insulator material is an option for changing ϕ_B, but it can not be changed much.

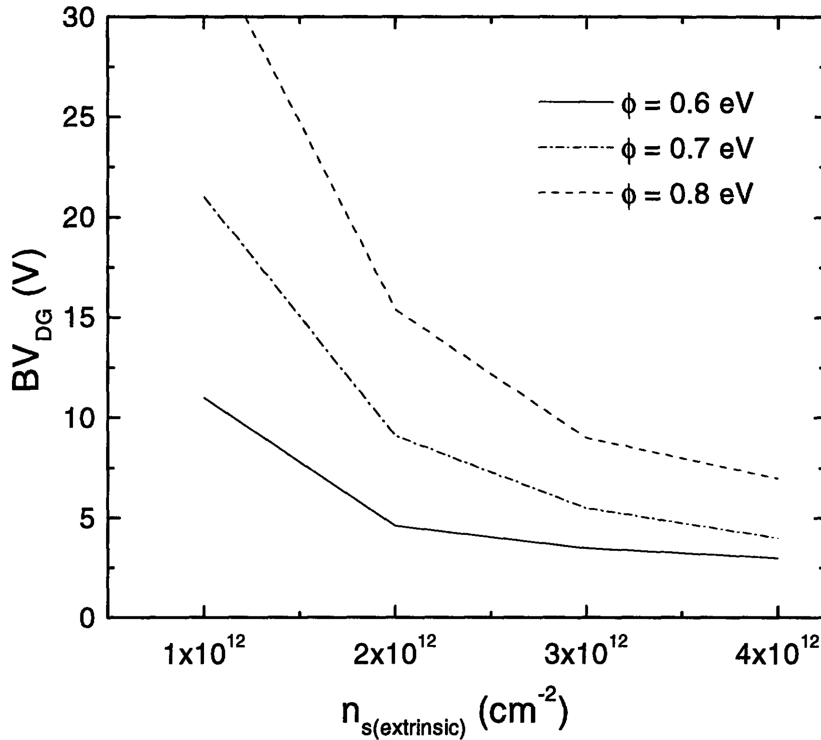


Figure 4.2: Theoretical breakdown voltage vs. $n_{s(extrinsic)}$ for the tunneling/ TFE model.

4.2 Optimization of Power Performance

4.2.1 Adjusting $n_{s(extrinsic)}$

Both I_{dmax} and BV_{DS} can be adjusted by the well-controlled value of $n_{s(extrinsic)}$. Unfortunately, as is evident in Figs. 4.1 and 4.2, they have opposite dependence on this parameter. If we increase BV_{DS} by decreasing the sheet carrier concentration, we will limit the ability of the device to handle current. But, if we increase $n_{s(extrinsic)}$ to improve I_{dmax}, the breakdown voltage will worsen. This is consistent with our findings in the Lockheed Martin HEMTs. Shown in Fig. 4.3 is a plot of BV_{DG} vs. I_{dmax} for devices across the sample set. The Schottky barrier height remains unchanged across all of the samples, but $n_{s(extrinsic)}$ is different for each wafer. An inverse relationship emerges between BV_{DG} and I_{dmax}. We see this even more clearly in Fig. 4.4. Here we have calculated the product

Figure 4.3: Breakdown voltage vs. maximum current for several devices in this sample set.

of BV_{DG} and I_{dmax} for the study shown in Fig. 4.3 and plot the results against $n_{s(extrinsic)}$. This product should have a strong relationship to the maximum output power. $BV_{DG} \times I_{dmax}$ is rather insensitive to the value of $n_{s(extrinsic)}$.

Although for a given v_{sat} and ϕ_B there will be an optimum $n_{s(extrinsic)}$, we clearly will not achieve a significant increase in the maximum power by changing the sheet carrier concentration. It may be possible, however, to improve devices with smart designs taking into account the $n_{s(extrinsic)}$ dependence. The double recess design [3] can enable the device to reach a higher useful I_{dmax}. An additional constraint on power devices is the need for a significant power gain in order the device to be useful. This requires a high g_m. In the double recess design, the gate is placed very close to the source and the cap is doped to provide a high carrier concentration close to the gate on the source side. This results in a low r_s. The double recess design effectively increases $n_{s(extrinsic)}$ where we want it to be high (at the source) while still maintaining its low value near the drain. While this will not

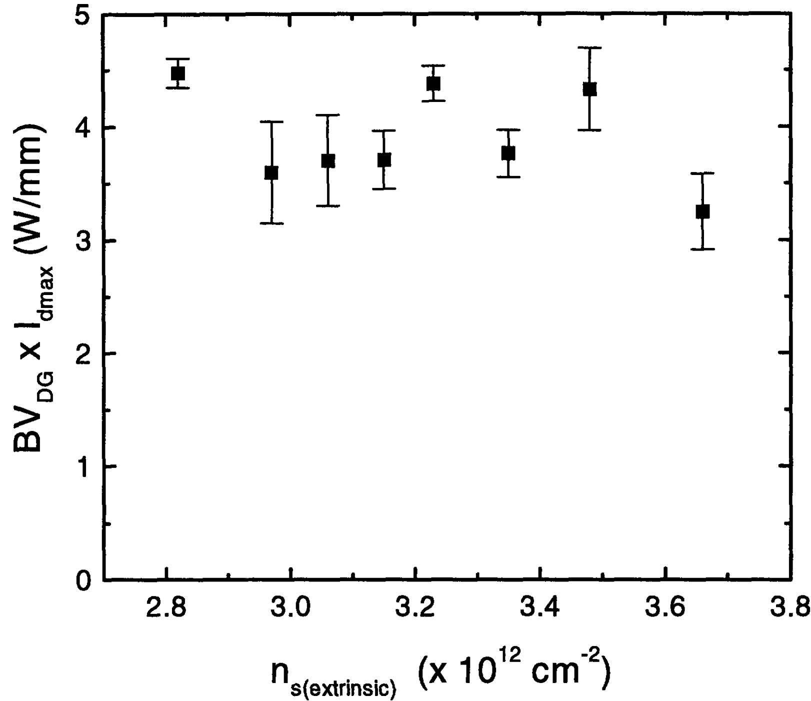


Figure 4.4: $BV_{DG} \times I_{dmax}$ vs. $n_{s(extrinsic)}$ for devices in this sample set.

actually increase I_{dmax}, the result is that g_m fall-off is pushed to a higher voltage, allowing a larger useful current range. An unfortunate side effect of this type of design is that the voltage on the source begins to have an effect on the breakdown voltage [4].

Recent investigations have also considered the use of parallel conduction in the cap over the extrinsic regions. The current handling capacity is increased with this modification since there is a parallel path for the current flow and therefore the bottleneck is reduced. Although this procedure has been used primarily in AlGaAs/InGaAs pHEMTs, and has recently shown some success in InAlAs/InGaAs HEMTs [5]. Similar to the double recess design, this will reduce the extrinsic source resistance and help to push the g_m peak to a higher current to provide a larger useful current range, but it is not clear that I_{dmax} would be affected. Unfortunately, however, it will also degrade BV and thus it might not be very effective for increasing power.

4.2.2 Increasing v_{sat}

Increasing the saturation velocity of the carriers shows promise for improving the power performance of the device. As shown in Fig. 4.1, the maximum drain current can be improved with either a higher $n_{s(extrinsic)}$ or a higher v_{sat}. We have already seen that it is ineffective to increase $n_{s(extrinsic)}$. However, a higher v_{sat} alone should not negatively affect the breakdown voltage. Unfortunately, this requires significant design modifications.

In order to get a higher v_{sat} we must alter the channel material. Increasing the InAs content of the channel has been shown to improve the electron mobility and v_{sat} in the channel. This yields a higher I_{dmax} and, since r_s is reduced, a larger current range with a useful power gain. Unfortunately, increasing the InAs content in the channel also leads to undesirable narrow bandgap effects in the channel. Specifically, impact ionization is known to increase when the InAs content is raised. This will lead to a lower on-state BV and could potentially affect the off-state BV [3, 8]

4.2.3 Raising ϕ_B

Raising the Schottky barrier height between the gate and the insulator also should be effective for improving the power performance of the device. A higher ϕ_B, like a lower $n_{s(extrinsic)}$, can significantly improve the breakdown voltage, but, unlike a lower $n_{s(extrinsic)}$, it will not degrade I_{dmax}. Unfortunately, engineering a change in the Schottky barrier height requires altering the materials used in the device structure.

One option is to alter the material structure of the metal gate. The gates of HEMTs are usually made of gold, but the Schottky contact is generally made through a barrier metal such as titanium (Ti). We are limited in selecting a material that will yield a higher ϕ_B by

constraints such as the adhesion of the metal to the InAlAs surface and process compatibility. Some experimentation has shown that it is beneficial to add platinum (Pt) to the gate structure to improve the Schottky contact [6].

The other choice is to alter the insulating layer in the HEMT. Increasing the aluminum composition of the InAlAs layer has been shown to increase the Schottky barrier height [7]. Unfortunately, this also is blamed for decreasing the reliability of the devices. Some researchers believe it may be advantageous to use a different material in the insulator. Recently, investigations into GaInP as a potential replacement for InAlAs have gained much attention [3].

4.3 Conclusion

It is clear from the results of this work that to substantially improve power performance we must focus on $n_{s(extrinsic)}$, ϕ_B, and v_{sat}. Other parameters, such as the insulator thickness and delta doping ratios, do not have a significant impact on I_{dmax} or BV. In fact, however, we actually cannot improve the power performance significantly by changing $n_{s(extrinsic)}$ either, since I_{dmax} and BV have opposite dependencies on this parameter. Thus, we must focus on increasing v_{sat} or ϕ_B. Changing these two parameters can significantly improve the power performance, and further research needs to focus on examining the various options for accomplishing this.

Chapter 5

Conclusions and Suggestions for Future Work

5.1 Conclusions

We have done extensive characterization on state-of-the-art devices provided by Lockheed-Martin in order to understand the power-limiting mechanisms in InAlAs/InGaAs HEMTs. Research focused on the two most important parameters for power, I_{dmax} and BV_{DS}. The experimental data, covering a range of temperatures and variation in device structural parameters, was compared with various theories for the mechanisms determining each of these parameters in HEMTs. From our results we have been able to draw significant conclusions on what appear to be the dominant power-limiting mechanisms in InAlAs/InGaAs HEMTs.

5.1.1 Maximum Drain Current

It appears that velocity saturation in the extrinsic source region is the dominant mechanism determining the maximum drain current. We observed the following:

- The conventional parallel MESFET theory does not describe what is seen in these HEMTs designed for power performance.
- Velocity saturation is seen in TLM test structures at currents similar to I_{dmax}.

- The source resistance blow-up theory, based on velocity saturation in the extrinsic source region, fairly well describes the behavior of the transconductance and the maximum current.
- Increasing I_{dmax} and reducing the undesirable effects of r_s blow-up requires increasing $n_{s(extrinsic)}$ or v_{sat}.

5.1.2 Breakdown Voltage

The results of this work conclusively show that the off-state breakdown voltage is determined by tunneling and thermionic-field emission of electrons from the gate. In particular, we saw the following:

- The off-state breakdown path is strictly in the drain-to-gate diode and the channel is not involved in off-state breakdown.
- BV_{DS} is inversely related to the $n_{s(extrinsic)}$, but other device parameters have little impact on breakdown.
- BV_{DS} exhibits a negative temperature dependence and the temperature coefficient decreases with increasing $n_{s(extrinsic)}$.
- Theoretical calculations based on the tunneling and thermionic-field emission model provide a good prediction of the gate current and the breakdown voltage in these devices.
- Increasing BV_{DS} requires decreasing $n_{s(extrinsic)}$ or increasing ϕ_B.

5.2 Suggestions for Future Work

While this research was able to provide important data to advance the understanding of state-of-the-art InAlAs/InGaAs HEMTs, and has fairly well established the dominant power-limiting mechanisms seen in these HEMTs, it is by no means a complete and

exhaustive study. It is essential to continue and extend the characterization done here to more devices over an expanded sample set and to have additional test structures on the wafer.

First, it would be very beneficial to investigate the breakdown voltage and maximum current on wafers with a much lower value of $n_{s(extrinsic)}$. This would allow for a good examination of the tunneling/ thermionic-field emission theory for breakdown, especially since the sheet carrier concentration values on this sample set were rather tightly clustered. It would also be useful to investigate such wafers to determine the impact on I_{dmax}. If our findings are correct, I_{dmax} should decrease proportionally to the change in $n_{s(extrinsic)}$.

This study was very much limited by the lack of a test structure appropriate for determining the current-voltage characteristics of the very short source-to-gate extrinsic region. Knowing this characteristic well is very important to determine the maximum current and r_s blow-up. A very short TLM-like structure is essential to determine this I-V characteristic since we are unable to get measurements from the gate current injection technique at the high currents that we are most interested in and it has previously been observed that the I-V characteristic changes for very short regions [1].

Another interesting experiment would be to investigate I_{dmax} and g_m characteristics on two wafers with matching $n_{s(extrinsic)}$ but different doping ratios. If indeed the current is being limited by saturation velocity and not the effect of the parallel MESFET, the two wafers should exhibit exactly the same I_{dmax} and g_m behavior. These characteristics will be different, however, if the parallel MESFET plays a role in determining I_{dmax}, since the MESFET turn-on voltage will shift.

According to our findings, the breakdown voltage is directly related to the Schottky barrier height. It is therefore essential to identify technologies that enable the enhancement of ϕ_B. In addition to the importance of enhancing ϕ_B to raise BV_{DS}, this would also enable verification of the dependence of BV_{DS} on ϕ_B.

Lastly, one aspect that was not investigated in this research is the effect of a passivation layer on the power performance. In this technology, passivation layers have been found significantly impact device performance because altering the surface conditions affects the carrier distribution in the channel [2]. Since commercial devices must be passivated, it is very important to know and understand the effects of this added process step.

References

Chapter 1

[1] S. Takamiya, N. Yoshida, N. Hayafuji, T. Sonoda, and S. Mitsui, "Overview of recent development of HEMTs in the mm-wave range", *Solid-State Electronics*, vol. 38, no. 9, p. 1581-1588, 1995.

[2] P.M. Smith, "Status of InP HEMT technology for microwave receiver applications", *IEEE MTT-S Digest*, p. 5-8, 1996.

[3] P.M. Smith, S.M.J. Liu, M.Y. Kao, P. Ho, S.C. Wang, K.H.G. Duh, S.T. Fuh, and P.C. Chau, "W-band high efficiency InP-based power HEMT with 600GHz f_{max}", *IEEE Microwave and Guided Wave Letters*, vol. 5, no. 7, p. 230-232, 1995.

[4] L.D. Nguyen, A.S. Brown, M.A. Thompson, and L.M. Jelloian, "50 nm self-aligned gate pseudomorphic AlInAs/GaInAs high electron mobility transistors", *IEEE Transactions on Electron Devices*, vol. 39, p. 2007-2014, 1992.

[5] J. Spicher, B.-U.H. Klepster, M. Beck, A. Rudra, R. Sachot, and M. Ilegems, "A 20 Gbit/s monolithic photoreceiver using InAlAs/InGaAs HEMTs and regrown p-i-n photodiode", *Proceedings of the IEEE International Conference on Indium Phosphide and Related Materials*, p. 439-442, 1996.

[6] R. Lai, *et al.*, "A high-efficiency 94GHz 0.15μm InGaAs/InAlAs/InP monolithic power HEMT amplifier", *IEEE Microwave and Guided Wave Letters*, vol. 6, no. 10, p. 366-368, 1996.

[7] T. Otsuji, "46 Gbit/s multiplexer and 40 Gbit/s demodulator IC modules using InAlAs/InGaAs/InP HEMTs", *Electronics Letters*, vol. 32, no. 7, p. 685-686, 1996.

[8] P.R. Gray and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 3rd ed., New York: Wiley, 1993 , p. 359-366 .

[9] M.H. Somerville, J.A. del Alamo, and W. Hoke, "A new physical model for the kink effect on InAlAs/InGaAs HEMTs", *IEEE IEDM Conference Proceedings*, p. 201-204, 1995.

Chapter 2

[1] M. Hirano, Y. Takanashi, and T. Sugeta, "Current-velocity characteristics of an AlGaAs/ GaAs heterostructure FET for high voltages", *IEEE Electron Device Letters*, vol. EDL-5, no. 11, p. 496-499, 1984.

[2] M.C. Foisy, P.J. Tasker, B. Hughes, and L.F. Eastman, "The role of inefficient charge modulation in limiting the current-gain cutoff frequency of the MODFET", *IEEE Transaction on Electron Devices*, vol. 35, no. 7, p. 871-878, 1988.

[3] H. Hida, T. Itoh, and K. Ohata, "A novel 2DEGFET model based on the parabolic velocity-field curve approximation", *IEEE Transactions on Electron Devices*, vol. ED-33, no. 10, p. 1580-1586, 1986.

[4] D.R. Greenberg and J.A. del Alamo, "Veocity saturation in the extrinsic device: a fundamental limit in HFETs", *IEEE Transaction on Electron Devices*, vol. 41, no. 8, p. 1334-1339, 1994.

[5]D.R. Greenberg, *The Physics and Technology of the InAlAs/n+-InP Heterostructure Field-Effect Transistor*, PhD thesis, MIT, 1995 .

[6] D.R. Greenberg and J.A. del Alamo, "The impact of electron transport regimes on the linearity of AlGaAs/n+-InGaAs HFETs", *Solid State Electronics*, vol. 36, no. 1, p. 53, 1993.

[7] G.K. Reeves and H.B. Harrison, "Obtaining the specific contact resistance from transmission line model measurements", *IEEE Electron Device Letters*, vol. EDL-3, no. 5, p. 111, 1982.

[8] S.M. Sze, *High-Speed Semiconductor Devices*, New York: Wiley, 1990 .

Chapter 3

[1] S.H. Wemple, W.C. Niehaus, H.M. Cox, J.V. Dilorenzo, and W.O. Schlosser, "Control of gate-drain avalanche in GaAs MESFETs", *IEEE Transactions on Electron Devices*, vol. ED-27, no. 6, p. 1013-1018, 1980.

[2] W.R. Frensley, "Power-limiting breakdown effects in GaAs MESFETs", *IEEE Transactions on Electron Devices*, vol. ED-28, no. 8, p. 962-970, 1981.

[3] C.-S. Chang and D.-Y.S. Day, "An analytical solution of the two-dimensional poission equation and a model of gate current and breakdown voltage for reverse gate-drain bias in GaAs MESFETs", *Solid State Electronics*, vol. 32, no. 11, p. 971-978, 1989.

[4] S.R. Bahl, J.A. del Alamo, J. Dickmann, and S. Schildberg, "Off-state breakdown in InAlAs/InGaAs MODFETs", *IEEE Transactions on Electron Devices*, vol. 42, no. 1, p. 15-22, 1995.

[5] G. Meneghesso, M. Matloubian, J. Brown, T. Liu, C. Canali, A. Mion, A. Neviani, and E. Zanoni, "Open channel impact-ionization effects in InP-based HEMT's and their dependence on channel quantization and temperature", *Proceedings of the 54th Device Research Conference*, p. 138, 1996.

[6]S.M. Sze, *Physics of Semiconductor Devices*, 2nd ed., New York: John Wiley, 1981 .

[7] G. Meneghesso, *et al.*, "Effects of channel quantization and temperature on off-state and on-state breakdown in composite channel and conventional InP-based HEMTs", *IEEE IEDM Conference Proceedings*, p. 43-46, 1996.

[8] M.H. Somerville and J.A. del Alamo, "A model for tunneling-limited breakdown in high-power HEMTs", *IEEE IEDM Conference Proceedings*, p. 35-38, 1996.

[9] S.R. Bahl and J.A. del Alamo, "A new drain-current injection technique for the measurement of off-state breakdown voltage in FETs", *IEEE Transactions on Electron Devices*, vol. 40, no. 8, p. 1558, 1993.

[10] P.M. Smith, "Status of InP HEMT technology for microwave receiver applications", *IEEE MTT-S Digest*, p. 5-8, 1996.

[11] C.S. Putnam, M.H. Somerville, J.A. del Alamo, P.C. Chao, and K.G. Duh, "Temperature dependence of breakdown voltage in InAlAs/InGaAs HEMTs: theory and experiments", *Proceedings of the International Conference on Indium Phosphide and Related Materials*, 1997.

Chapter 4

[1] S.R. Bahl, J.A. del Alamo, J. Dickmann, and S. Schildberg, "Off-state breakdown in InAlAs/InGaAs MODFETs", *IEEE Transactions on Electron Devices*, vol. 42, no. 1, p. 15-22, 1995.

[2] M.H. Somerville and J.A. del Alamo, "A model for tunneling-limited breakdown in high-power HEMTs", *IEEE IEDM Conference Proceedings*, p. 35-38, 1996.

[3] S. Takamiya, N. Yoshida, N. Hayafuji, T. Sonoda, and S. Mitsui, "Overview of recent development of HEMTs in the mm-wave range", *Solid-State Electronics*, vol. 38, no. 9, p. 1581-1588, 1995.

[4] M.H. Somerville, J.A. del Alamo, and P. Saunier, "Off-state breakdown in power pHEMTs: the impact of the source", *Proceedings of the 54th Device Research Conference*, p. 140, 1996.

[5] S. Kraus, H. Heib, D. Xu, M. Sexl, G. Bohm, G. Trankle, and G. Weimann, "InGaAs/InAlAs HEMTs with extremely low source and drain resistances", *Electronics Letters*, vol. 32, no. 17, p. 1619-1621, 1996.

[6] A. Mahajan, P. Fay, M. Arafa, G. Cueva, and I. Adesia, "Monolithic integration of InAlAs/InGaAs/InP enhancement- and depletion-mode high electron mobility transistors", *IEEE IEDM Conference Proceedings*, p. 51-54, 1996.

[7] M. Matloubian, L.M. Jelloian, M. Lui, T. Liu, and M.A. Thompson, "Ultra-high breakdown high-performance AlInAs/GaInAs/InP power HEMTs", *IEEE IEDM Conference Proceedings*, p. 915, 1993.

[8] P.M. Smith, "Status of InP HEMT technology for microwave receiver applications", *IEEE MTT-S Digest*, p. 5-8, 1996.

Chapter 5

[1] S.R. Bahl, *unpublished*, 1990.

[2] P.M. Smith, "Status of InP HEMT technology for microwave receiver applications", *IEEE MTT-S Digest*, p. 5-8, 1996.