A BANDPASS SIGMA DELTA MODULATOR IF RECEIVER

by

Emilija Simic

Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degrees of

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Author_____

Department of Electrical Engineering and Computer Science

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Certified by_____ 2/4/97

Hae Seung (Harry) Lee

Thesis Supervisor

Accepted by_____

F. R. Morgenthaler

Chairman, Department Committee on Graduate Theses

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ABSTRACT

Within the context of the wireless communication systems, there is a concrete commercial interest in A/D conversion at IF stage of the receiver because this allows digital channel-select filtering, gain control and demodulation. Apart from reducing the analog filtering and eliminating all the problems associated with analog I/Q demodulation and digitizing at 0 Hz, "digital receiver" has additional advantages of flexibility of digital programmability, as well as improved testability and yield. Unfortunately, the "digital receiver" places extremely high performance requirements on A/D converters, including high linearity to avoid interference, and high enough resolution to digitize large interferers so that final channel selection can be implemented on digital side. In a wideband systems, achieving necessary performance goals while still meeting the tight power constraints of mobile can ultimately set the limit to the application of this receiver architecture.

Motivated by the advantages of IF A/D conversion and the reported success of monolithic bandpass sigma-delta converters for narrowband applications, this thesis was set out to investigate whether the "digital receiver" architecture could be the architecture of choice for a wideband system, here for the CDMA path of the dual CDMA/analog mode phone receiver for the 1.23 MHz band of the North American cellular standard. The thesis answers this question by focusing on modeling, design and implementation of the critical component of "the digital receiver" for the CDMA system, namely 10.5 bit bandpass sigma-delta converter with the oversampling ratio of 16, sampling frequency of 39.36 MHz and a signal band of 1.23 MHz, and verifying through simulations whether it achieves the performance equivalent to the existing system in terms of the performance metric that was of crucial concern for this wideband system, namely power consumption. The results indeed compare favorably, verifying that the dual conversion "digital receiver" architecture with IF A/D conversion is a promising alternative to the existing dual conversion receiver with baseband A/D conversion for the CDMA system.

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Most of all, I thank my friend, Alex, for his love and companionship, my friend Jelena, for her humor and friendship, and my mother for her endless support.

This thesis is dedicated to my mother, Tamara, and the memory of my father, Milorad.

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.0 MOTIVATION AND GOAL

Within the context of communication systems, there is a concrete commercial interest in analog-to-digital (A/D) conversion at the intermediate-frequency (IF) stage of the receiver because this allows digital channel-select filtering, gain control and demodulation. Shifting in phase/quadrature (I/Q) demodulation on digital side is one of the key advantages because digital local oscillators can produce high precision quadrature waveforms, avoiding the problems of phase and gain mismatch present in analog system. Reduction of analog IF filtering is another key advantage because besides being large and costly, analog IF filters generally have poorly controlled phase performance and therefore can induce intersymbol interference, while digital filters can have exactly linear phase. More functionality implemented on digital side provides an additional advantage of improved testability. The robustness of digital circuitry also produces advantages in manufacturing; it decreases cost by decreasing yield loss. Digital implementation allows the use of sophisticated algorithms which are especially useful with digitally coded transmissions (e.g. CDMA) and where multiple transmission standards are in use. Digital programmability allows a change in function to be implemented by a simple software change. Unfortunately, the "digital receiver" places extremely high performance requirements on A/D converters. It is of prime importance to have linearity, or else strong interferers may intermodulate in the converter and mask the desired signal. The converter should have both high enough of a bandwidth to be able to convert the band of interest and high enough resolution (usually at least 10 bits) to be able to digitize large interferers, so that final channel selection can be performed on the digital side. To appreciate the issues involved, the past work on A/D converters has been consulted and Figure 1.1 summarizes the resolution and conversion rates of conventional lowpass Nyquist-rate and oversampled A/D converters

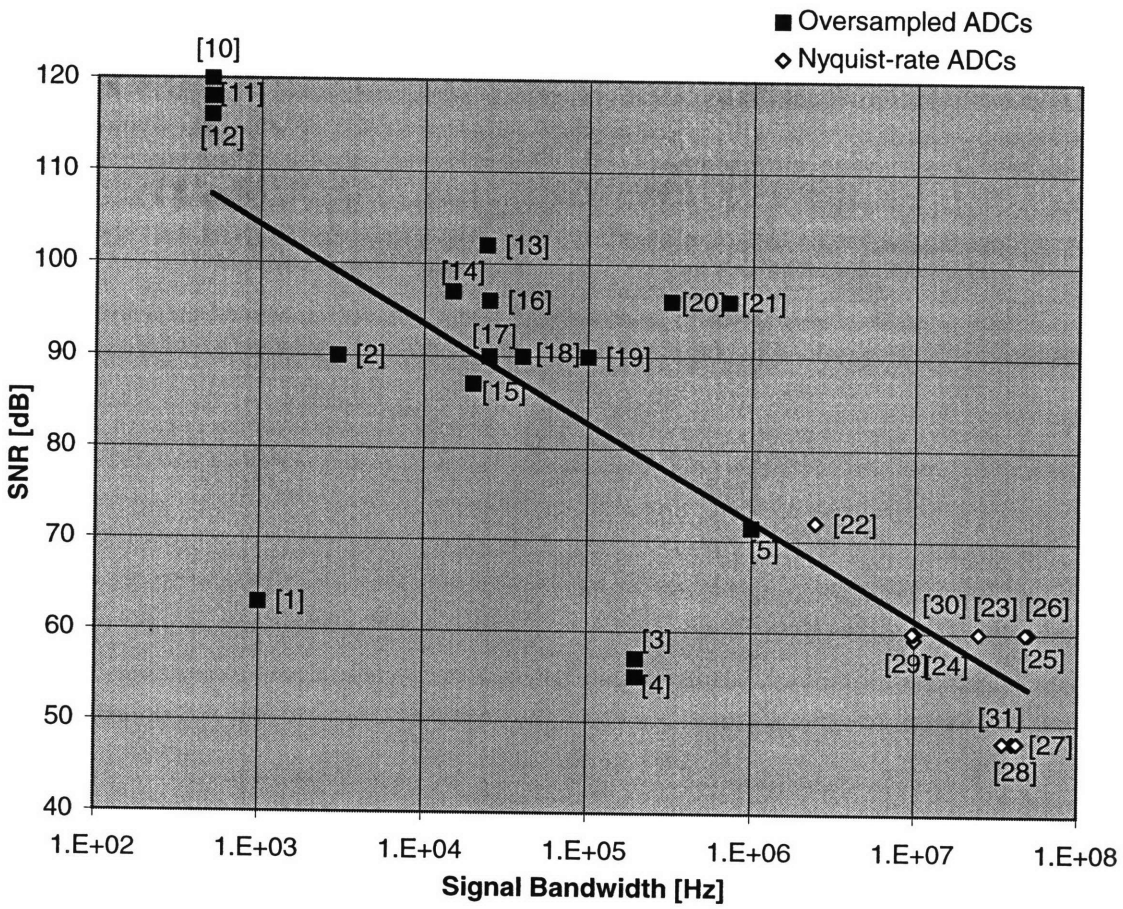


Figure 1.1 SNR and signal bandwidth for oversampled and Nyquist-rate A/D converters

published during recent years. There are several observations to be made from it as follows:

- There is a trade-off between the resolution in time and the resolution in amplitude inherent to A/D conversion.
- At low to medium conversion rates, oversampled A/D converters dominate the Nyquist rate converters in terms of achievable resolution.
- At higher channel bandwidths, Nyquist-rate converters dominate, but the achievable resolution is limited to below 70 dB due to component matching accuracy.

Due to an inherent trade-off between the conversion rate and the resolution of A/D converters, requirement of having both high resolution and bandwidth necessary can be readily obtained for narrow-band systems, such as voice AM, IS-54 and AMPS cellular telephony or even GSM telephony. At higher channel bandwidths, such as 1.23 MHz band of the North American cellular standard IS-95, achieving high enough precision may be a very difficult task

by itself, and doing so while still meeting the tight power constraints of mobile is what ultimately can set the limit to the application of this receiver architecture. Therefore, we conclude that the "digital receiver" could be a practical approach only for sufficiently narrowband signals. Consequently, we would expect oversampled A/D converters to be converters of choice for this application area. As already noted, oversampled A/D converters can achieve high resolution without calibration or trimming due to their tolerance to component mismatches and other circuit nonlinearities. They reduce the burden on analog circuitry, resulting in integration-friendly, simpler and more compact systems. Specifically, they don't require precision sample-and-hold circuitry and they relax performance requirements on the image rejection filter preceding the sampling. They have an inherent digital filtering capability and their resolution versus conversion rate is easily adjusted to allow the use of the same converter in variety of applications.

Sigma-delta oversampled A/D converters appear to be particularly suitable for the application area. They provide noise shaping that further attenuates the quantization noise in the band of interest, and as a result they require lower sampling frequency to achieve the same resolution as conventional oversampled A/D converters, potentially dissipating less power than conventional oversampled A/D converters.

The published work on bandpass converters verifies the conclusions drawn. Monolithic bandpass sigma-delta modulators have been reported [1]-[3] with center frequencies of 455 kHz, 1.8 kHz, 10.7 MHz, bandwidths of 10, 30, 200 kHz and resolutions of 10.5, 12.5 and 9.2 bits. These bandwidths are suitable for broadcast and voice AM, IS-54 cellular telephony, and GSM telephony, respectively. Another modulator obtained 9.2 bits of resolution with a 6.5 MHz center frequency and 200 kHz bandwidth using off-chip inductors as resonators [4]. There hasn't been any work reported on monolithic bandpass sigma-delta converters for higher channel bandwidths, although referring back to Figure 1.1, we notice that lowpass sigma-delta A/D converter designed by Brandt and Wooley in 1991 is a 12 bit converter for 1 MHz band [5].

Motivated by the prospects of a simpler, more robust and more flexible system, and inspired by the reported success of monolithic bandpass sigma-delta converters for similar applications (for narrower signals though), this work is intended to investigate whether the "digital receiver" architecture could be the architecture of choice for the CDMA path of the dual CDMA/analog mode phone receiver. In particular, the motivation is to

- avoid all the problems associated with analog I/Q demodulation, such as phase and gain mismatch among I and Q paths,
- avoid all the problems associated with digitizing at 0 Hz, such as DC-offsets,
- minimize the need for off-chip filtering,
- implement most of the selectivity processing on digital side, and
- minimize the area and power dissipation.

Since oversampling with wideband signals necessarily implies fast clocking, there is a question though whether it will be possible to meet the power budget. This thesis will attempt to answer this question by focusing on design and implementation of a bandpass sigma-delta A/D converter that would be able to convert an entire 1.23 MHz band of the North American cellular standard IS-95 and with enough resolution to do most of the channel selection on the digital side (here 10.5 bits). The results of this work will then serve as a benchmark in comparing performances of the existing and proposed architectures, with the immediate goal of achieving at least the same level of performance in terms of power consumption.

1.1 THESIS ORGANIZATION

This thesis is organized in six chapters. First chapter summarizes the main features of the existing dual conversion receiver architecture with baseband A/D conversion, briefly discussing some of its main advantages and disadvantages. It also presents new "digital receiver" architecture and discusses some of the system level decisions. The remainder of the thesis focuses on design of bandpass sigma-delta converter that is the heart of the new architecture, and will be used as a benchmark in comparing the performances of the existing and proposed architectures. Second chapter presents an overview of bandpass sigma-delta conversion, reviewing operation and performance modeling of two main converter architectural classes, single-loop and cascaded converters. Chapter 3 discusses the considerations in wide-bandwidth sigma-delta conversion, and presents the system level design in the ideal case. Chapter 4 identifies, discusses and quantifies relevant circuit non-idealities of the converter. Chapter 5 discusses the implementation of actual circuits that follows the design outlines arrived at in chapters 3 and 4, and presents the results of converter design. Finally, Chapter 6 draws the conclusions, comparing the performance of the new architecture to the existing one.

1.2 OVERVIEW OF EXISTING SYSTEM

Some of the system parameters for the physical layer of the communication link are given in Table 1-1. The portable operates in dual mode, providing CDMA or FM service, as indicated in column one. Column two indicates the frequency allocated to these bands - the first range is for the base to portable link (receive section of portable's integrated receiver/transmitter), while the second is for the portable to base link (transmit section of portable's integrated receiver). The third column provides the bandwidth of the channel. The modulation used for each of the modes is indicated in the forth column. This system employs full duplex (simultaneous transmission and reception), and shares a single antenna between the receiver and the transmitter through the use of duplex filters in a frequency-division duplex (FDD), as specified in column five. Finally, column six specifies the multiplex method used.

Service	Band	Channel BW	Modulation	Duplex Method	Multiplex Method
AMPS	Rx: 869-894Mhz Tx: 825-849MHz	30KHz	FM	FDD	FDMA
IS95/IS98	Rx: 869-894MHz Tx: 825-849MHz	1.23MHz	Spread Spectrum	FDD	CDMA

Table 1-1 System parameters for the physical layer of the communication link

The existing architecture of the portable's receiver is shown in Figure 1.2. It is a multiple conversion design that converts the incoming signal first to an IF, at a relatively high frequency of approximately 85 MHz, and then directly to baseband [54].

The received signal is passed through a preselect bandpass filter which is responsible for improving the dynamic range by rejecting out-of-band interferes. After preselection, a low noise amplifier (LNA) provides moderate gain to overcome losses in passive circuits up to the input of the first IF amplifier. This gain is needed to provide a good noise figure, but must be minimized to avoid degrading dynamic range. Next, another bandpass filter supplements the out-of-band attenuation provided by the preselect filter and serves as an image rejection filter by

attenuating any noise at the image frequency that would be translated to IF1 (and thus folded onto the desired signal) in the mixing process. The mixer LO1=RF+IF1 then converts the signal to the IF1 where additional levels of gain are provided. Thereafter, there are two SAW bandpass filters, one for CDMA and one for FM, that perform channel selection. Automatic gain control (AGC) IF amplification is then employed so that amplitude information is retained. The signal is then quadrature mixed with LO2 equal to the IF1, converting the signal directly to the baseband where final channel select filtering is performed with lowpass filter.

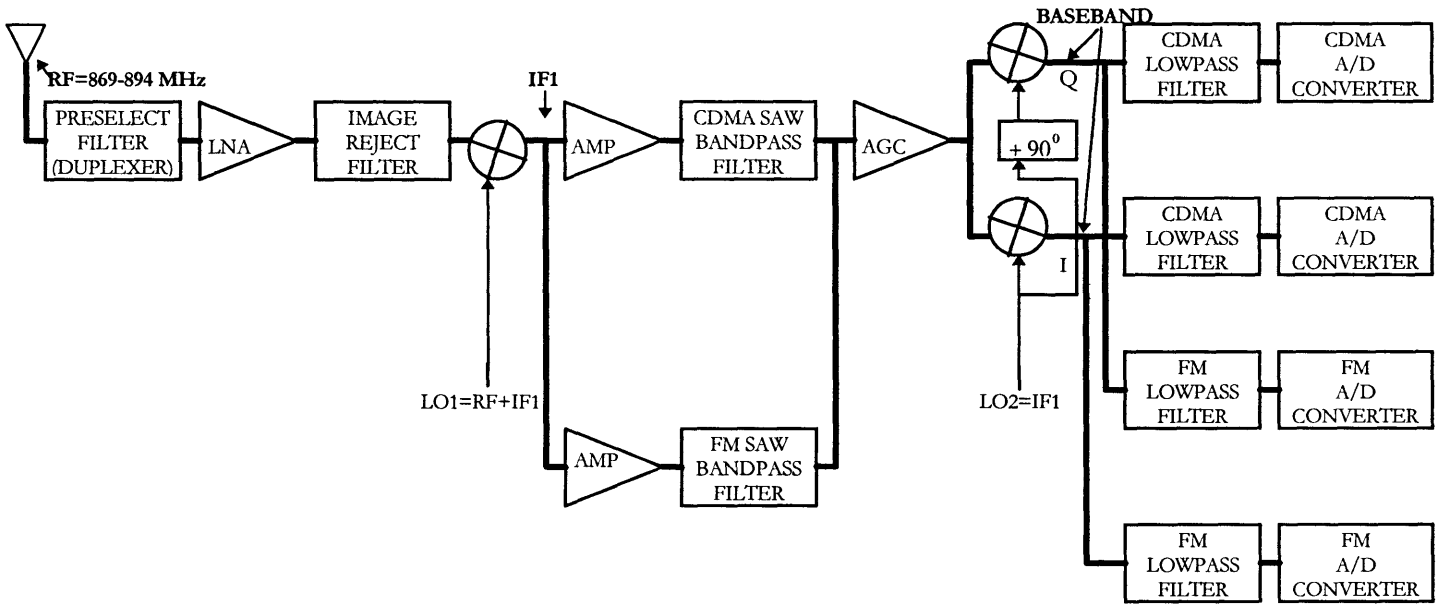


Figure 1.2 Block diagram of the existing receiver

This architecture has several important advantages over a single conversion super-heterodyne design. First, since preselect and image filters need to select band rather than channel, they will have wider bandwidth, lower Q and thus a smaller number of poles. Further, since the center of the second IF2 frequency is zero frequency, no image response is produced, and no image filtering is required for this second down-conversion. Signals above and below the desired signal frequency are translated into frequencies above or below DC, and are removed by lowpass filtering, rather than with a high-Q bandpass filter. As a result, this architecture benefits from low power A/D converters with small dynamic range and a small number of off-chip components.

There are several drawbacks to this architecture however, most of which stem from the fact that due to downconversion to baseband prior to A/D conversion, the in-phase/quadrature (I/Q) channel conversion had to be implemented on the analog side. First, this calls for two paths for each of the FM and CDMA signals, each path requiring a low pass filter and A/D converter, which increases the area. Second, it requires maintaining precision gain and phase matching between two paths in order to avoid image errors inside the path band. Next, DC-offsets voltages existing in active stages in the I and Q paths make the carrier components appear at 0 Hz or at output carrier frequency, requiring the employment of analog techniques for offset reduction, in order to prevent possible saturation of lowpass filters or A/D converters. Accordingly, there exists a need for an improved yet simpler receiver that would

- avoid the ambiguities, undesired signals and added noise caused by digitizing signals at 0 Hz, thus reducing the total area and power consumption.
- minimize the need for off-chip filtering, thus reducing cost.
- implement most of the selectivity processing on digital side, resulting in more robust and flexible system.

This thesis is intended as a proposal of such an alternate architecture for a CDMA path of a dual mode CDMA/FM receiver that will overcome the deficiencies of the existing system by minimizing the need for analog processing altogether.

1.3 OVERVIEW OF PROPOSED SYSTEM

A possible architecture to replace the dual conversion to analog baseband scheme is shown in Figure 1.3. Instead of mixing received signal from IF1 directly down to the baseband, the received signal is converted down to a non-zero lower IF2 where DC offsets cause no problem, and even-order distortion products have no effect, as is the case in any bandpass system [35]. As before, the quadrature analog IF mixers are used, but now as image reject mixer. The 27dB of image rejection does not necessitate high phase shift accuracy, so that matching between the I and Q branches is no longer a critical concern. Furthermore, now the front end CDMA SAW filter can have relaxed specifications, and therefore reduced size and cost. Received signal is then digitized directly at IF2 using a bandpass sigma-delta converter, shifting I/Q demodulation and the final channel-select filtering to the digital side, where the digital local oscillator can produce high precision quadrature waveforms and the benefits of

digital signal processing can be applied to realize channel selection filters with very high selectivity.

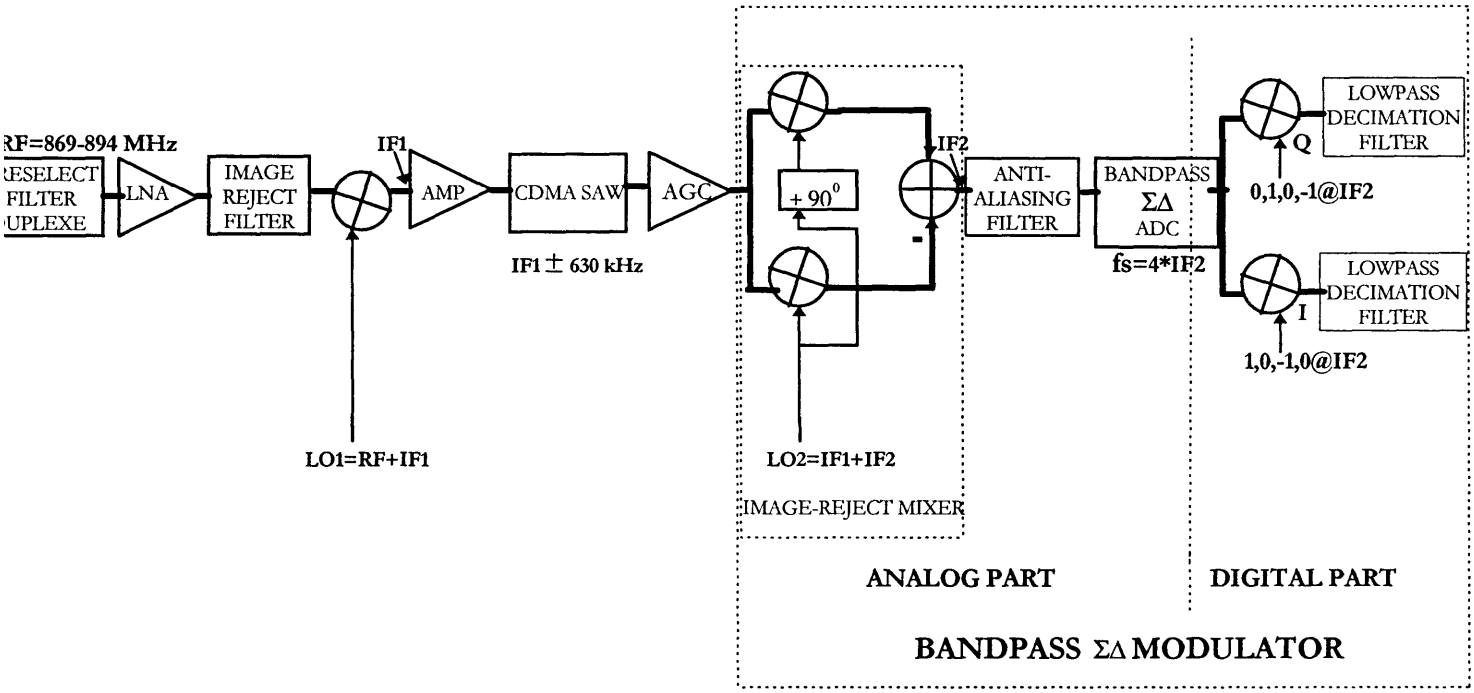


Figure 1.3 The architecture of the proposed system

1.4 BANDPASS SIGMA DELTA MODULATOR FOR CDMA SIGNAL PATH

Looking at Figure 1.3 we see that even though we relaxed specifications on SAW filter, we are still using analog image reject mixer to convert the signal down to IF2, whereas one of the original ideas was to minimize the need for analog processing. Couldn't we digitize the signal directly at IF1, and shift all of the processing to digital side, i.e. achieve a perfect "digital receiver"? Unfortunately not.

In order to meet power budget of the mobile receiver, we want A/D conversion to occur at as low of sampling frequency fs as possible, much lower than IF1. In this system, the proposed sampling frequency fs is 39.36 MHz and the proposed IF2 is 9.84 MHz, for reasons to be discussed briefly. Since the A/D converter is a sampled-data system, having fs lower then IF1 will automatically result in down-conversion of a signal from IF1 to some lower frequency IF1-fs, eliminating the need for analog mixers but still requiring elimination of image frequencies using analog image reject filter prior to sampling.

How close can we get to the perfect "digital receiver"? On the surface, the sampling approach has significant appeal, since it does not require the use of analog mixers. In reality, it is

implemented using "sub-sampling" approach to avoid the use of fast sampling clock which unfortunately poses high demands on image reject filter.

1.4.1 THE ANALOG PART

1.4.1.1 THE ALTERNATIVE MODULATOR: SUB-SAMPLING APPROACH

Conceptual block diagram of bandpass sigma delta modulator using sub-sampling techniques is given in Figure 1.4. Note that the sub-sampling stage is unnecessary, since the sampling operation in A/D conversion performs the same function. It is drawn as a separate stage for discussion purposes only. A/D converter and the digital part are the same regardless of which technique is used, and will therefore not be discussed in this section.

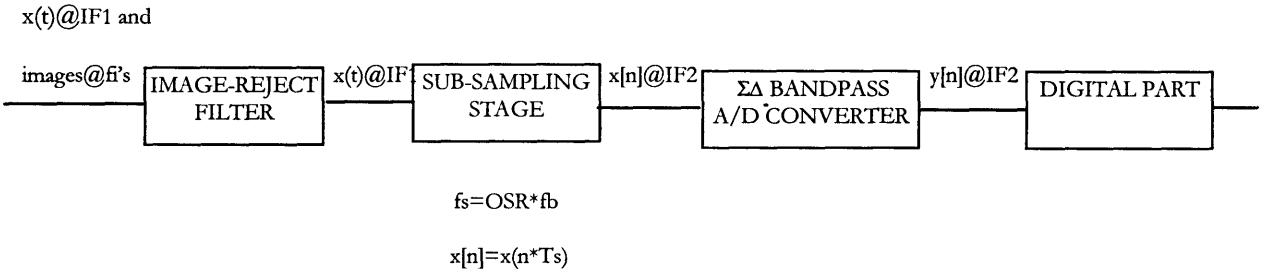


Figure 1.4 Block diagram of the bandpass $\Sigma\Delta$ modulator based on sub-sampling approach

1.4.1.1.1 SUB-SAMPLING STAGE

As already pointed out, in reality both fs and IF2 must be much lower than IF1 in order to meet the power budget of the mobile's receiver. In order to convert the received signal from IF1 to IF2 without using really fast sampling clock, designers take advantage of the concept of sub-sampling. Namely, the received signal is sampled at much slower fs, which is chosen such that

$$IF1 \pm N*fs = IF2$$

where N is an integer:

The principle of down-conversion using the idea of sub-sampling is illustrated in Figure 1.5.

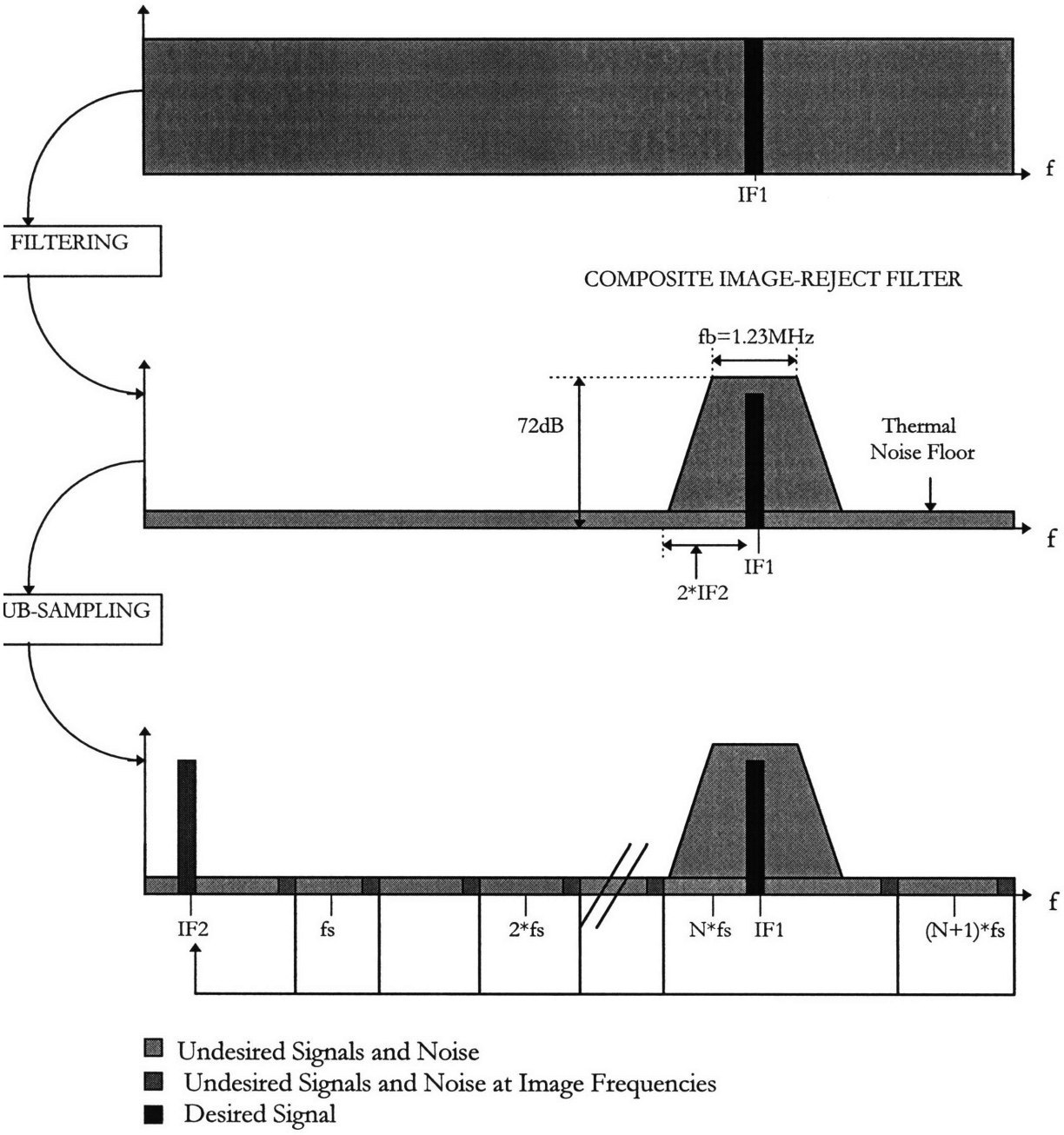


Figure 1.5 Down-conversion using sub-sampling

1.4.1.1.2 IMAGE-REJECT FILTER

Unfortunately, in the process of sub-sampling, both the desired signal at IF1 and all undesired signals at image frequencies fi such that fi ± n*fs=IF2 where n=1,2,3.... will be folded down to IF2. To solve this problem, an image-reject filter with bandwidth B<<2*IF2 and an attenuation on the order of 72 dB for this system would be needed preceding the sub-sampling

stage to reject the undesired signals at image frequencies. Since this is a relatively high-Q filter (i.e. $Q=\frac{85MHz}{1.23MHz}\approx 70$) it may still be potentially necessary to implement it as another off-chip SAW filter, which would be contrary to our goal of smaller size and cost-reduction!

There are several games we could play here to relax the requirements on this filter. Let us first note that image-reject filter does not perform any channel selection, it merely serves as an image reject for the conversion down to IF2. Any undesired signals at IF1 (e.g. the interferer in the adjacent channel) are converted and filtered out by digital filters. Consequently, we could relax some of the high selectivity requirement for the filter by allowing the passband bandwidth of filter to be larger, resulting in smaller fractional bandwidth (e.g., instead of $Q=\frac{85MHz}{1.23MHz}\approx 70$ we could require $Q=\frac{85MHz}{2.46MHz}\approx 35$). Unfortunately, this means that the number of poles required will go up too, resulting in increased filter order, which translates in bigger area and more power dissipated.

There are two ways to reduce the order of filter needed. Since the first image location is at 2*IF2 away from the desired signal, the image-reject filter would need to provide 72 dB of attenuation in 2*IF2-fb/2. Therefore, the choice of IF2 will determine how sharp the roll-of the image-reject filter need to be. It follows that we would like IF2 to be as large as possible in order to make the roll-of smoother, or equivalently relax the requirements on the filter in terms of the number of poles needed. This is contrary to our goals of minimizing power consumption. Choosing IF2 to be only large enough to place the undesired signal from nearest image frequency at the reject band of the other filters in the system, specifically of CDMA SAW filter and of front end image reject filter, we could relax the requirements on the off-chip filter even further, without compromising much of the performance! From the specifications of CDMA SAW filter we see that the choice of IF2 >9 MHz would place nearest image position in its ultimate rejection band, providing 45 dB of attenuation. In theory, we could choose IF2>17.5 MHz and such high IF2 would place the image position at the transition band of the front end image reject filter, providing additional 27 dB of attenuation in the worst case, and eliminating the need for the image-reject filter altogether! Unfortunately, this would result in sampling frequency of 70 MHz, which is likely to prevent us from achieving reasonable power consumption, even if it is possible to implement circuitry that can settle so fast. Thus we still need to provide the additional 27 dB of attenuation by the image-reject filter,

but with relaxed requirements, shown in Figure 6, we could use a cheap passive off-chip filter rather than an expensive SAW filter, or even implement it on chip.

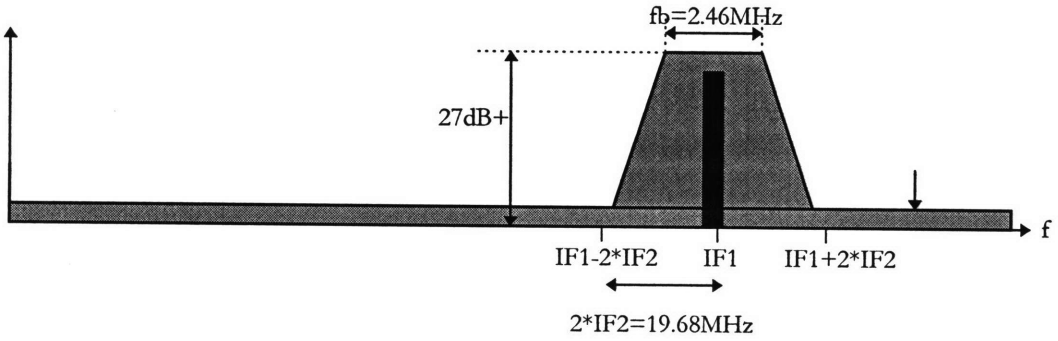


Figure 1.6 Performance requirements for the image-reject filter

1.4.1.2 THE MODULATOR OF CHOICE:ANALOG APPROACH

Instead of sub-sampling, the down-conversion can be performed using two quadrature analog mixers. The output of mixers could be summed together in quadrature to cancel the undesired image, eliminating the need for separate narrow bandpass image-reject filter. The conceptual block diagram is shown in Figure 1.7. More detailed block diagram has already been presented in Figure 1.3. Note that there still exists a need for analog filtering prior to sampling, in order to prevent all the signals produced by the mixer to fold down on the desired signal in the process of sampling.

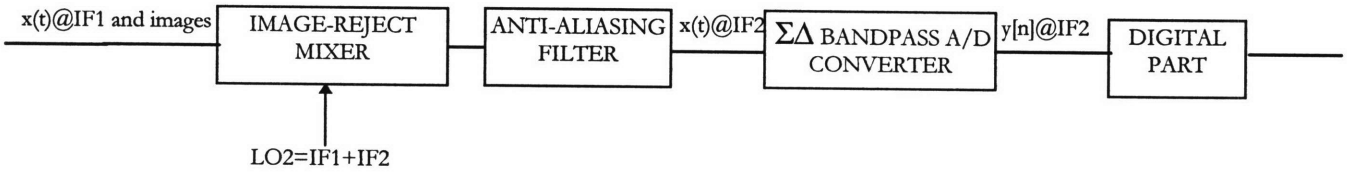
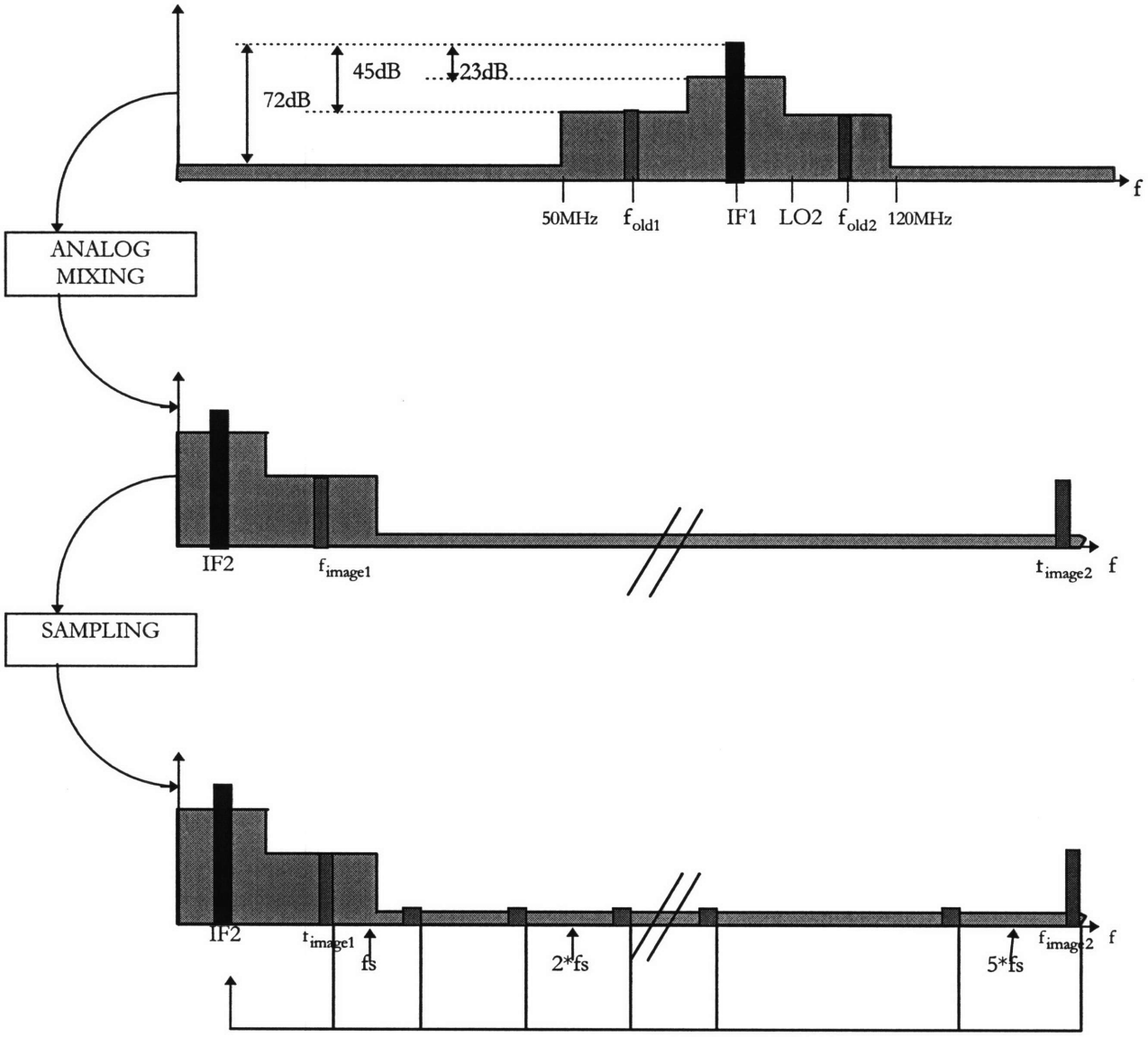


Figure 1.7 Block diagram of bandpass $\Sigma\Delta$ modulator based on the analog approach

1.4.1.2.1 IMAGE-REJECT MIXER

The image-reject mixer LO2 mixes the desired signal from IF1 to IF2, providing additional 27 dB of image rejection needed for this down-conversion. Unfortunately, it also creates some undesired signals at the image frequencies for subsequent sampling process. How does this happen? There is a range of frequencies (i.e. from 50 MHz to 120 MHz) at which the front-end filters (including CDMA SAW filter) did not provide the minimum required 72 dB of



$f_{old1} = 65.7$ MHz

$f_{old2} = 111.42$ MHz

$f_{image1} = 29.52\ \text{MHz} = (1 - \frac{1}{4}) \cdot fs$

$f_{image2} = 206.64\ \text{MHz} = (5 + \frac{1}{4}) \cdot fs$

Figure 1.8 Down-conversion using analog mixing

attenuation. In the process of mixing, all of these unfiltered signals will also get mixed from their original frequencies (call them f_{old}) to some new frequencies (call it f_{new}) according to the following equation: $f_{new} = f_{old} \pm LO2$. Some of the frequencies f_{old} will satisfy the following relation:

$$f_{image} = (n \pm \frac{1}{4}) \cdot fs = LO2 \pm f_{old} \qquad \ldots\ldots \quad n = \pm\ 1,2,3$$

The signals that were originally at these frequencies will get mixed down to the image frequencies for the sampling process and will mask the desired signal if not filtered out prior to sampling. The principle of down-conversion using the idea of image-reject mixer and the problem associated with the subsequent sampling are illustrated in Figure 1.8. Two undesired signals at $f_{old1} = 65.7$ MHz and $f_{old2} = 111.42$ MHz are shown explicitly to better illustrate the problem.

1.4.1.2.2 ANTI-ALIASING FILTER

To prevent these signals at image frequencies to mask the desired signal in the process of sampling, we still need to have an anti-aliasing filter. As illustrated in Figure 1.9, this filter only needs to provide 27 dB of rejection, starting at the first image frequency of 29.52 MHz. It can therefore be implemented with an on-chip lowpass filter.

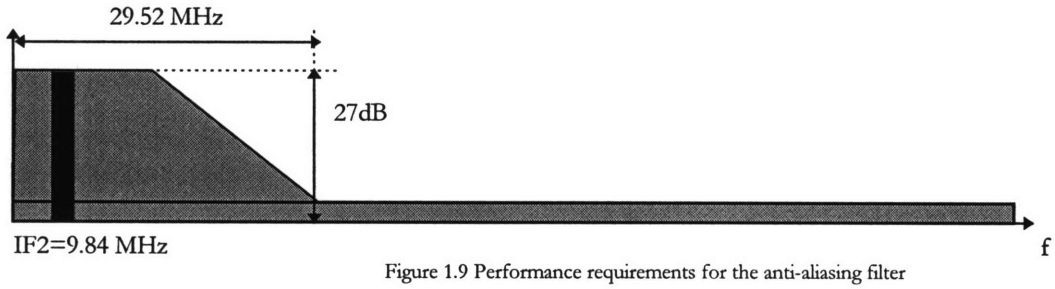


Figure 1.9 Performance requirements for the anti-aliasing filter

Comparing the two modulators, we notice that they trade-off the complexity of down-sampling stage (analog mixers vs. none) for complexity in image-reject filter (an additional adder and a small low pass filter vs. separate image-reject filter). Since the existing architecture already has two on-chip analog mixers, we have chosen the analog approach, since it buys us

image-reject mixer at virtually no extra cost. At the expense of the additional adder, the two analog mixers also provide the additional 27 dB of image rejection. In addition, a small lowpass filter is needed to prevent aliasing. Another reason for making this modulator the modulator of choice is the greater flexibility in terms of changing the frequency plan of the receiver. Sub-sampling approach requires that IF1 ± N*fs=IF2 be satisfied, so that any change in IF1 will require a change in choice of either fs or IF2. The analog approach requires only that LO2=IF1+IF2, so that change in IF1 requires a change of LO2 only.

1.4.2 THE DIGITAL PART

The digital part of the modulator consists of digital mixers and lowpass decimation filters, as shown in Figure 1.3. Digital mixers digitally mix the output from bandpass sigma-delta A/D converter from IF2 to digital baseband, producing I and Q components. The lowpass decimation filters then attenuate the out-of-band quantization noise produced by the A/D conversion and perform the final channel selection. Choosing the sampling frequency fs to be four times the IF2, the phase of the digital mixer can be chosen so that it has three convenient values: 0, -1, +1. That is, the I and Q components are obtained by multiplying the digitized modulator output by the periodic bit sequences {1,0,-1,0} and {0,1,0,-1}, that represent the cosine and sine carriers, respectively. This simplifies the digital quadrature mixer to a couple of exclusive-or gates. Observing that the inputs to two digital decimators are zero in alternate cycles allows these decimation filters to be implemented by multiplexing a single low pass filter, reducing the power consumption and area of decimators by approximately 50 % [6], [7], [8]. Brandt and Wooley have shown that decimation filters can be implemented at very low power of 6.5 mW for 11.3 MHz data with a word length of 16 bits at a 3 V power supply [9].

1.4.3 BANDPASS SIGMA-DELTA A/D CONVERTER

In the existing architecture, filtering of all undesired signals has been taken care of on the analog side prior to the A/D conversion, so that A/D converters needed to digitize only desired in-band signal. As a result, the A/D converters needed to have a resolution of only 4 bits. In the proposed receiver architecture, A/D conversion is performed early on, so that both desired and undesired in-band signals get digitized. How do we determine the required resolution of the new bandpass A/D converter? What are our design goals?

1.4.3.1 DESIGN GOALS

Smallest desired in-band signal the receiver must handle is specified at -104 dBm. The receiver also must be able to handle a single tone jammer at -32 dBm. This requires 72 dB of adjacent channel filtering. The CDMA SAW filter provides 33 dB of adjacent channel filtering , so that A/D converter needs to be able to digitize 38.8 dB of the jammer. From these and other related specifications, we can calculate that A/D converter should have maximum input referred signal-to-noise ratio (SNR) of 62dB in order to be able to digitize both the maximum signal and the jammer 38.8 dB above it. We can further calculate that the input referred signal-to-noise-plus-distortion-ratio (SNDR) of A/D converter should be 57.2 dB. The circuit is to operate from a single 3.3 V power supply.

An additional design goal was to dissipate at most as much power as the existing architecture. There is only one analog path now, so instead of two low-pass filters and two low-pass A/D converters that in current architecture dissipated approximately 50 mW, we now have one lowpass filter which will dissipate minimal power, the bandpass A/D converter and the digital part, whose power consumption is estimated to be around 6.5 mW. The resulting worst case target power dissipation for the converter is therefore approximately 40 mW. An additional potential source of power savings is the analog-to-digital interface in the proposed architecture. Using oversampled bandpass A/D converter reduces the number of bits between analog and digital interface, reducing the pin capacitance. The frequency at which the bits are transmitted is twice what it used to be though, allowing for power savings from the interface only if the number of bits used in A/D converter is less then four. For the worst case power dissipation calculation, it was assumed that there is no power savings here.

Referring back to Figure 1.2 and our introductory discussion, we reiterate that bandpass sigma-delta A/D converter is the converter of choice for the application. It can provide high resolution without imposing high performance requirements on the analog circuitry, which could translate in power savings needed. The design is flexible in a sense that the same converter can be easily tailored for change in oversampling ratio vs. resolution. The challenge is to meet power constraint for this wide-band system.

1.4.3.2 SWITCHED CAPACITOR IMPLEMENTATION

The most important circuit in the sigma-delta modulator is the first resonator in the loop filter. The effects of most of the nonidealities in the other circuits are attenuated by the noise shaping in the modulator. The nonidealities of the first resonator in the loop filter add directly to the input, and as such just get passed through, decreasing the total signal-to-noise ratio (SNR). This is why the first resonator needs to be approximately as linear as the overall resolution of the converter. This work focuses on switched capacitor technology because it has been proven for high resolution and linearity in design of the baseband sigma-delta A/D converters and because switched capacitor technology is also one of the rare monolithic technologies capable of delivering precision analog performance. Since in switched-capacitor implementation resonators need to settle within half of the clock cycles, they are expected to dominate only up to some upper bandwidth limit, dictated by technology used in circuit design. As reported in [5], this upper bandwidth limit is higher than 39.36 MHz needed for this application.

1.4.3.3 CHOICE OF BAND LOCATION

For a given input center frequency IF1 and bandwidth fb, a choice in the location of the band of interest IF2 (i.e. noise-shaping band center) with respect to fs involves various trade-offs among image reject filter requirements, sampling frequency and oversampling ratio. Placing the band low at frequency (making the fs/IF2 ratio large) increases the oversampling ratio and therefore improves the performance achievable for a given modulator order. Furthermore, since the first image frequencies that will alias into the signal band are further away, the requirements on the image-reject filter are relaxed. However, placing the band too low in the frequency can lead to unrealistically high clock rates. Moving the band closer to fs/2 may be necessary to reduce the clock rate to an acceptable level, but this puts increased demands on the image-reject filter. Other issues involve the impact of band location on the digital post filtering and decimation, as discussed in Section 1.4.2. The ratio of four was a choice for this application, mostly for reasons of power consumption savings in digital I/Q demodulation and post-digital filtering and decimation, and cost savings resulting from image-reject filter requirements.

1.4.3.4 CHOICE OF SAMPLING FREQUENCY

The lowest possible sampling frequency for target SNDR is 16*(2*BW)=39.36 MHz. The power dissipated in the sigma-delta modulator is dominated by static power dissipation in resonators, specifically the first resonator that needs to achieve the linearity of the overall system. The power dissipated in resonators is dominated by settling requirements imposed by the sampling frequency. Therefore, we would ideally like to use this minimal sampling frequency. Other requirements on sampling frequency discussed in previous sections include fs/4>9 MHz, imposed by image rejection needs. Finally, we would like fs to be a power of 2 multiple of the existing sampling frequency generator, so that the sampling frequency generation can be achieved by means of a PLL or doublers. The frequency of 39.36 MHz satisfies all the above mentioned requirements.

1.5 SUMMARY

An overview of a dual conversion receiver with baseband analog-to-digital (A/D) conversion for the North American cellular standard IS95 was presented, briefly discussing some of its main advantages and disadvantages. An alternate dual conversion "digital receiver" architecture with the intermediate frequency (IF) A/D conversion is further analyzed and compared to the first architecture. Some of the system level trade-offs for a bandpass modulator necessary for the "digital receiver" are discussed, such as sub-sampling versus analog mixing approach for the analog part, Nyquist-rate versus oversampled A/D conversion for the A/D part, and the impact of the frequency plans on design of the digital part of the modulator. The rest of thesis will focus on design of a bandpass sigma-delta A/D converter that would be able to convert an entire 1.23 MHz band of the North American cellular standard IS-95 and with enough resolution to do most of the channel selection on the digital side (here 10.5 bits). The results of this work will then serve as a benchmark in comparing performances of the existing and proposed architectures.

CHAPTER 2

BANDPASS SIGMA-DELTA ANALOG-TO-DIGITAL CONVERSION OVERVIEW

2.0 INTRODUCTION

Analog-to-digital (A/D) conversion is a process of transforming a continuous time and amplitude signal into a discrete time and amplitude signal. Sigma-delta A/D conversion is a type of analog-to-digital conversion that utilizes oversampling and noise shaping technique. Oversampling reduces the quantization noise power in the signal band by spreading a fixed quantization noise power over a bandwidth much larger than the signal band, and is achieved by conversion at a sampling frequency which is much higher than the Nyquist rate. Noise shaping further attenuates this noise in the signal band and amplifies it outside of the signal band, and is achieved through the use of feedback in the converter. Consequently, this process of oversampled noise shaping by sigma-delta converter can be viewed as pushing quantization noise power from the signal band to other frequencies. The output of converter is then filtered to remove the out-of-band quantization noise and is finally downsampled to the Nyqist rate, usually by a digital filter that also performs decimation.

In this work, we are interested in signal band centered at some intermediate-frequency (IF). The focus of this chapter is therefore on bandpass sigma-delta A/D conversion, where the basic principle of noise shaping is slightly modified to place the quantization noise nulls at the signal band center frequency, so that the quantization noise is pushed away from the signal band at the desired IF frequency. Moreover, since IF of choice in this work is fs/4, the bandpass sigma-delta converters discussed in this chapter are the converters with the quantization noise zeros at fs/4 and 3fs/4 frequencies. The fs/4 bandpass sigma-delta converters discussed in this chapter are obtained by performing lowpass to bandpass

transformation that maps the zeros of the lowpass converter from DC to ±fs/4, by the following change of variable,

$$z^{-1} \rightarrow -z^{-2}.$$

Equation 2-1

This is the simplest way to design fs/4 sigma-delta converters, since this transformation preserves the stability and SNR characteristics of the lowpass converter [8], which is better studied in previous literature.

Two main classes of sigma-delta converters, single-loop and cascaded converters, are reviewed, and their operation and performance modeled in sections 2.1 and 2.2, respectively.

2.1 SINGLE LOOP

2.1.1 OPERATION MODELING

Figure 2.1 shows the most general representation of a single-loop sigma-delta converter, consisting of a loop filter and an n-bit quantizer in its forward path, in series with a D/A converter enclosed in its feedback path. The z-transforms of the transfer function for the loop filter is A(z).

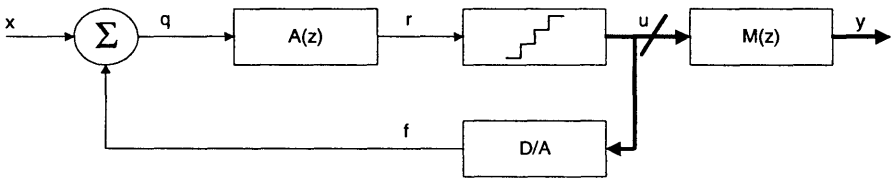


Figure 2.1 General representation of the sigma-delta converter

The quantizer and D/A converter in the sigma-delta converter are non-linear systems, and as such can be modeled only approximately. We will take time here to present the assumptions and describe the resulting models that will be used throughout the work.

The transfer function for a typical quantizer is illustrated in Figure 2.2. From a large scale perspective, the transfer function for moderate to high resolution appears to be a linear gain of

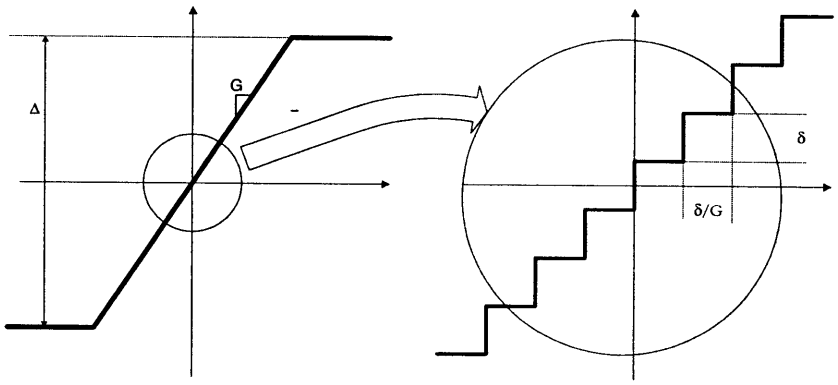


Figure 2.2 Quantizer transfer function

G that clips its output at $\pm\frac{\Delta}{2}$, where Δ is the maximum output range. On a smaller scale, the output is granular in that it is limited to a finite set of values; the separation between adjacent output levels, δ, is

$$\delta = \frac{\Delta}{2^N - 1},$$

Equation 2-2

where N is the quantizer resolution in bits. Combining the large and small perspectives, the quantizer output y[n] can be written as:

$$y[n] = G \cdot u[n] + E_Q[n],$$

Equation 2-3

where G is the effective linear gain of the quantizer, and $E_Q[n]$ is the additive error for the quantizer, shown in Figure 2.3.

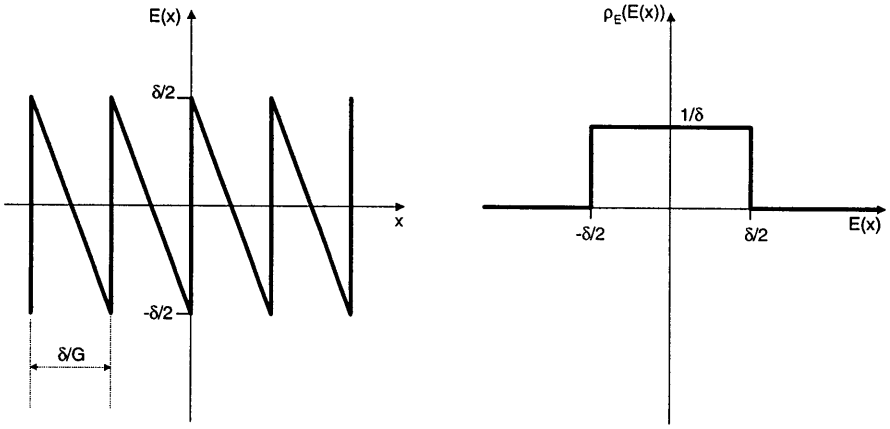


Figure 2.3 Quantizer error and its distribution

To further simplify the analysis of the nonlinear noise from the quantizer, the following assumptions are traditionally made:

- The error sequence, $E_Q[n]$, is a sample sequence of a stationary random process.
- $E_Q[n]$ is uncorrelated with the sequence x[n].
- The probability density function of the error process is uniform over the range of quantization error, i.e., over $\pm\frac{\delta}{2}$, as shown in Figure 2.3.
- The random variables of the error process are uncorrolated, i.e., the error is a white noise process.

Bennett has proven that these assumptions hold as reasonable under the following conditions [39]:

- the quantizer is not overloaded, i.e., the quantizer input does not exceed the signal range of the quantizer,
- the number of quantization levels, 2^N, is large,

- the quantizer level separation, δ, is small relative to the signal level, and
- the joint probability density of any two quantizer input samples is smooth, i.e., the successive signal values are not excessively correlated.

Under these conditions, the quantifier error can be modeled as an additive white noise term whose variance, σ_E^2, is

$$\sigma_E^2 = \int_{-\infty}^{\infty} E_Q^2 \cdot \rho_E(E_Q) dE_Q = \frac{\delta^2}{12}.$$

Equation 2-4

Bennett's noise model forms the basis of the analysis of the sigma-delta converters with quantizers that have large number of quantization levels, i.e. large N.

Unfortunately, many input signals and many systems fail to meet one or more of the conditions of Bennett's noise model. An example is given in [36], where it is noted that a pure sinusoidal quantizer input violates the smooth joint probability condition and produces a quantizer error that has a power spectrum comprising of discrete tones. Sigma-delta converter utilizing only one-bit quantizers violate most of the conditions of Bennett's noise model and thus the justification for Bennett's noise model appears to be much weaker. Nevertheless, it is still useful to define *white noise approximation* [36] in which the quantizer error, E_Q, is assumed to be

1. white with a variance given by Equation 2-4, and
2. uncorrelated with the input.

While loosely based on Bennett's white noise model, the justification for white noise approximation is the empirical evidence that supports the results obtained using this approximation.

An additional problem with modeling one-bit quantizers is the fact that the quantizer gain G is undefined. The output of the quantizer is determined based on the sign of the input signal, irrespective of its value. Nevertheless, if we model G such that

$$\prod_{i=1}^{L/2} K_i \cdot G = 1$$

Equation 2-5

is still satisfied, where K_i is the gain of the i-th resonator in the loop filter, we can still use our white noise approximation. In this way we also accurately model the situation, since the quantizer output signals appear to be independent of scaling coefficients, while the signals prior to quantizer are still scaled.

Similarly, we can model the D/A output, r[n], as

$$r[n] = y[n] + E_D[n].$$

Equation 2-6

Since any D/A gain could be modeled as a combination of quantizer gain and output gains, the D/A converter can be assumed to have a linear gain of one, at no loss in generality. Furthermore, since there is no additional quantization in D/A converter, it does not have an inherent noise component. In other words, the D/A error, E_D, results solely from implementation non-idealities.

The feedback converter measures the input x[n] while attenuating the quantization error, $E_Q[n]$, using the loop gain in the frequencies of interest. The modulator output is, using Equation 2-3 and Equation 2-6,

$$Y(z) = H_x(z) \cdot [X(z) - E_D(z)] + H_E(z) \cdot E_Q(z),$$

Equation 2-7

where $H_x(z)$ is the signal transfer function (STF) and is given by

$$H_x(z) = \frac{G \cdot A(z) \cdot M(z)}{1 + G \cdot A(z)},$$

Equation 2-8

and $H_E(z)$ is the quantization noise transfer function (NTF) and is given by

$$H\ \ (z) = \frac{1}{1 + G \cdot A(z)}.$$

Equation 2-9

The z-transform is related to frequency domain response with the following transformation:

$$z = e^{t \cdot \omega \cdot T} = e^{j\frac{2 \cdot \pi \cdot f}{f_s}}.$$

Equation 2-10

In a passband, $f \approx \frac{f_s}{4}$, so $z \approx j$. The loop gain T(z) is designed such that it satisfies the following conditions in the pass band:

$$|T(z)| = |G \cdot A(z)| >> 1 \text{ for } z \approx j,$$

Equation 2-11

so that STF and NTF in the pass band reduce to

$$H_x(z) \approx 1 \text{ and } H_E(z) \approx \frac{1}{G \cdot A(z)} \text{ for } z \approx j,$$

Equation 2-12

making the output of the modulator in the passband equal to

$$Y(z) \approx X(z) - E_D(z) + \frac{1}{G \cdot A(z)} \cdot E_Q(z) \text{ for } z \approx j.$$

Equation 2-13

If the forward gain, GA(z), is designed such that the error power in pass band is small relative to the signal power, and if the D/A error, $E_D(z)$ is small, the output will be approximately equal to the input, as desired.

Bandpass sigma-delta converter has a feedback gain equal to unity and the forward gain GA(z) much larger than one in the signal band. Since the feedback term is unity, the D/A error term is not amplified. Large forward gain reduces the quantization noise appearing in the signal band. In other words, not only does the bandpass sigma-delta converter reduces the quantization noise in the signal band by oversampling, i.e., by spreading a fixed quantization noise power over a bandwidth much larger than the signal band, but it also further attenuates this noise in the signal band, amplifying it outside of the signal band. This process is called the noise shaping, and it amounts to pushing quantization noise power from the signal band to other frequencies, as already discussed. The converter output can then be filtered to attenuate the out-of band quantization noise.

There are many transfer functions that could be used for the loop filter A(z) in a bandpass sigma-delta converter, i.e. that are high gain in the signal band. To implement desired fs/4 bandpass sigma-delta converter, a class of transfer functions that has been chosen for this work consists of a linear combination of N delaying fs/4 resonators that differentiate the

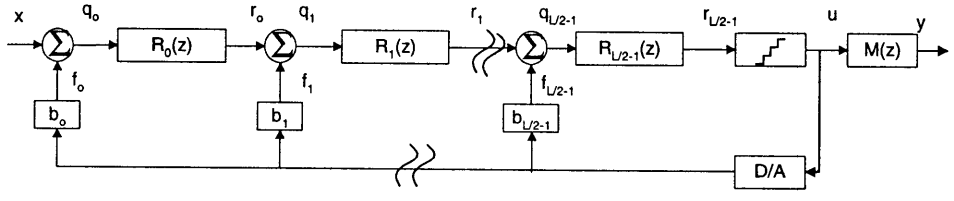


Figure 2.4 Single-loop sigma-delta converter

quantization noise. The input to each fs/4 resonator is the difference between the output of the previous resonator and a scaled version of the D/A converter output, as shown in Figure 2.4.

The transfer function for the i-th delaying resonator with gain K is

$$R_i(z) = -\frac{K_i \cdot z^{-2}}{1+z^{-2}}.$$

Equation 2-14

The order of the converter L is defined as twice the number of resonators in the forward path N. The transfer function of the loop filter of an L-th order converter is then given by

$$A(z) = \frac{U(z)}{Q(z)} = \frac{\prod_{i=0}^{L/2-1} R_i(z)}{1+G\cdot\sum_{i=1}^{L/2-1} b_i \cdot \prod_{j=i}^{L/2-1} R_j(z)}.$$

Equation 2-15

The feedback gain must be unity, so that

$$b_0 = 1,$$

Equation 2-16

and M(z) is given by

$$M(z) = (-1)^{L/2}.$$

Equation 2-17

Substituting these expressions for A(z) and M(z) back into the expressions for STF and NTF, i.e., Equation 2-8 and Equation 2-9, respectively, we get that

$$H_x(z) = \frac{G \cdot \prod_{i=0}^{L/2-1} K_i \cdot z^{-L}}{(1+z^{-2})^{L/2} + G \cdot \sum_{i=0}^{L/2-1} b_i \cdot (-1)^{L/2-i} \cdot z^{2 \cdot i-L} \cdot (1+z^{-2})^i \cdot \prod_{j=i}^{L/2-1} K_j}$$

Equation 2-18

and

$$H_E(z) = \frac{(1+z^{-2})^{L/2}}{(1+z^{-2})^{L/2} + G \cdot \sum_{i=0}^{L/2-1} b_i \cdot (-1)^{L/2-i} \cdot z^{2 \cdot i-L} \cdot (1+z^{-2})^i \cdot \prod_{j=i}^{L/2-1} K_j}.$$

Equation 2-19

Detailed derivation is given in Appendix A. For the converter to be stable, the poles of NTF and STF must be within the unit circle. For the low-order single-loop single-bit converters, this is always the case and they are therefore inherently stable. For higher order single-loop single-bit converters and any order single-loop multibit converters, the stability is conditional, limiting the quantization gain G, the resonator gains, K 's and the feedback coefficients, bi's [8].

Finally, it follows from Equation 2-11 that the in-band output for an L-th order single-loop noise-shaping bandpass sigma-delta modulator is, neglecting delays

$$Y(z) \approx X(z) - E_D(z) + \gamma \cdot (1+z^{-2})^{L/2} \cdot E_Q(z),$$

Equation 2-20

where γ is given by

$$\gamma = \frac{1}{G \cdot \prod_{i=0}^{L/2-1} K_i}.$$

Equation 2-21

For a single-bit single-loop converters, the Equation 2-20 reduces to

$$Y(z) \approx X(z) - E_D(z) + (1 + z^{-2})^{L/2} \cdot E_Q(z).$$

Equation 2-22

2.1.2 PERFORMANCE MODELING

To evaluate the performance of such a converter, we first need to define the performance metrics to be used in this work. There are three primary metrics used in evaluating sigma-delta converters. The first is the *signal-to-noise ratio, (*SNR), the second is the *signal-to-noise-and distortion ratio* (SNDR), and the third is *dynamic range* (DR).

- SNR is defined to be the ratio of the signal power at the output, S_{xx}, to the *total* noise power in the signal band at the output, S_{ee}, i.e.

$$SNR = \frac{S_{xx}}{S_{ee}}.$$

Equation 2-23

- SNDR is defined to be the ratio of the signal power at the output, S_{xx}, to the *total* noise power in the signal band at the output, S_{ee}, *plus* the distortion at the signal band at the output, S_{dd}, i.e.

$$SNDR = \frac{S_{xx}}{S_{ee} + S_{dd}}.$$

Equation 2-24

- DR is defined as the ratio of the full-scale signal power, $S_{xx_{full}}$, at the input to the signal power at the input for which the SNR is one, $S_{xx_{one}}$, i.e.

$$DR = \frac{S_{xx_{full}}}{S_{xx_{one}}}.$$

Equation 2-25

We are also going to introduce two other metric, that we will use as the primary metric throughout this work:

- SNR_{max}, or the maximum useful SNR, is defined as the ratio of the jammer power at the output, S_{jammer}, to the total noise power at the signal band at the output, S_{ee}, i.e.

$$SNR_{max} = \frac{S_{jammer}}{S_{ee}},$$

Equation 2-26

where the jammer is the maximum input signal (here interferer) that our modulator has to be able to handle.

- DR_{max}, or the maximum useful DR, is defined as the ratio of the jammer power at the output, S_{jammer}, to the signal power at the input for which the SNR is one, $S_{xx_{one}}$, i.e.

$$DR_{max} = \frac{S_{jammer}}{S_{xx_{one}}}.$$

Equation 2-27

where again the jammer is the maximum input signal (here interferer) that our converter has to be able to handle.

Note that DR_{max} is not necessarily equal to DR, since the full-scale input signal is usually chosen to be larger than the jammer, to allow for some margin.

For the discussion purposes, for the remainder of this section we will assume that the in-signal-band noise of the converter is dominated by the quantization noise, i.e. that

$$S_{ee} \approx S_{ee_{quantization}} .$$

Equation 2-28

Looking at Appendix A, we see that the signal power at the output of the converter, S_{xx}, is given by

$$S_{xx} = \frac{A_x^2}{2},$$

Equation 2-29

while the output quantizer noise power in the signal band, S_{ee}, is given by

$$S_{ee} = \gamma^2 \cdot \sigma_E^2 \cdot \frac{\pi^L}{(L+1) \cdot M^{L+1}} .$$

Equation 2-30

Using the expression for the variance of the quantization noise derived from white noise approximation, as given by the Equation 2-4 , we obtain that

$$S_{ee} = \gamma^2 \cdot \frac{\Delta^2}{12 \cdot (2^N - 1)^2} \cdot \frac{\pi^L}{(L+1) \cdot M^{L+1}} .$$

Equation 2-31

Finally, combining Equation 2-23, Equation 2-29 and Equation 2-31, we arrive at the expression for SNR to be

$$SNR = \frac{S_{xx}}{S_{ee}} = \frac{6 \cdot A_x^2}{\Delta^2} \cdot \frac{1}{\gamma^2} \cdot \frac{(L+1)}{\pi^L} \cdot (2^N - 1)^2 \cdot M^{L+1}.$$

Equation 2-32

Assuming that full-scale sinusoidal input has an amplitude of $A_{x\,full} = \frac{\Delta}{2}$, so that

$$S_{xx_{full}} = \frac{A_{x\,full}^2}{2} = \frac{\Delta^2}{8},$$

Equation 2-33

and calculating that

$$S_{xx_{one}} = \frac{A_{x_{one}}^2}{2} = \frac{\pi^L \cdot \gamma^2 \cdot \Delta^2}{12 \cdot (L+1) \cdot (2^N - 1)^2 \cdot M^{L+1}},$$

Equation 2-34

it follows that

$$DR = \frac{S_{xx_{full}}}{S_{xx_{one}}} = \frac{3}{2} \cdot \frac{1}{\gamma^2} \cdot \frac{(L+1)}{\pi^L} \cdot (2^N - 1)^2 \cdot M^{L+1}.$$

Equation 2-35

In contrast to the converters that utilize simple oversampling, where dynamic range is proportional to the oversampling ratio, M, the dynamic range of a bandpass sigma-delta is proportional to the (L+1) power of the oversampling ratio, M, due to its noise shaping action. Such a tremendous improvement in dynamic range due to noise shaping action allows sigma-delta converters to use substantially smaller number of bits then the Nyquist-rate converters with the same dynamic range. Figure 2.5 illustrates this point by plotting dynamic range, DR, versus oversampling ratio, M, for several different combinations of converter's order L, and the

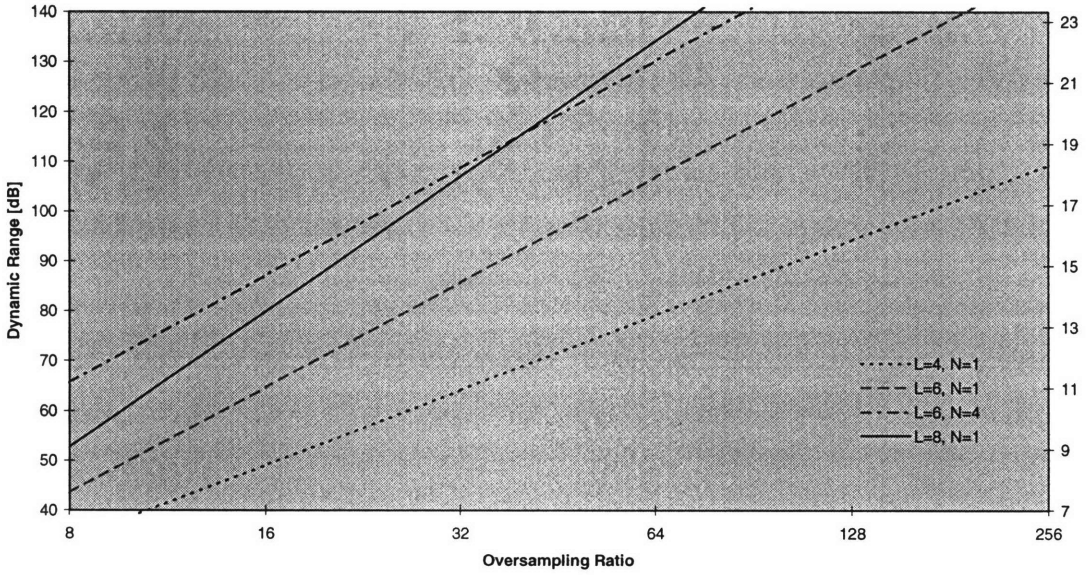


Figure 2.5 Calculated dynamic range vs. oversampling ratio

number of bits used in the quantizer, N, while the right-hand axis shows the number of bits that would be required from a Nyquist-rate converter in order to achieve equivalent dynamic range. The dynamic range is calculated for the ideal case, assuming γ is equal to 1. This assumption is for simplicity adopted in calculations throughout the remainder of the chapter.

2.2 MULTI-LOOP OR CASCADED BANDPASS SIGMA-DELTA CONVERTERS

In a multi-loop cascaded bandpass sigma-delta converters, each of the stages is itself a single-loop bandpass sigma-delta converter. The quantizer error of each stage serves as an input to the following stage, so that the output of each stage is then an approximate error from the previous stage. Error cancellation network performs subtraction of the approximate error from the output of the previous stage, so that most of the quantization error gets canceled. The generic multi-loop sigma-delta converter is illustrated in Figure 2.6.

In the ideal world, i.e., in the absence of mismatch, the performance of a cascaded converter is comparable to the ideal performance of the single-loop converter of the same order. The advantage of the multi-loop cascaded converter is that an inherently stable higher order converter can be achieved, since instability can be easily avoided by using only inherently stable second and fourth order single-loop single-bit bandpass sigma-delta converter as its stages.

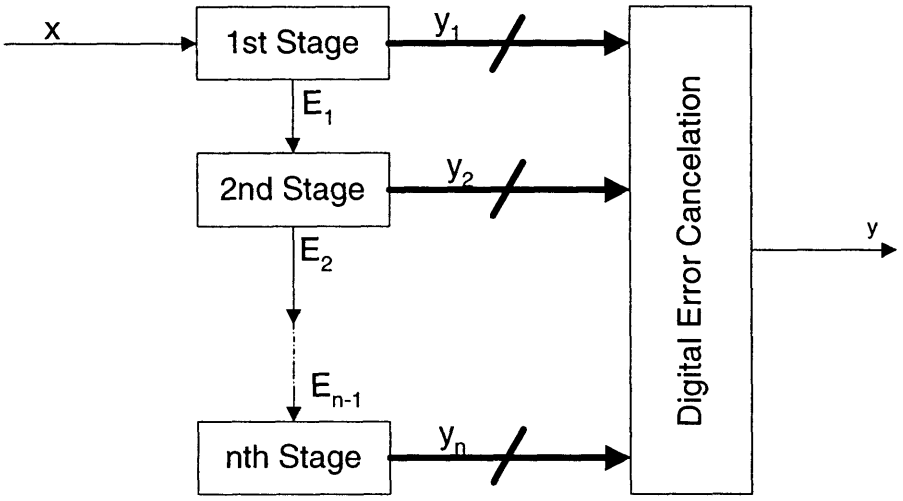


Figure 2.6 Multi-loop or cascaded sigma-delta converter.

The cascaded converters are referred to by the sequence of numbers that represent the order of the individual stage in the cascade. We will use a 4-2-2 cascade in this section to illustrate the operation and performance modeling for cascaded converters, from which we can then extrapolate the results to any arbitrary cascade of fourth and/or second/fourth order stages.

2.2.1 THE 4-2-2 ARCHITECTURE

2.2.1.1 OPERATION MODELING

A block diagram of the 4-2-2 architecture is shown in Figure 2.7. It is a cascade of a fourth-order stage followed by two second-order stages coupled through two error mixing networks formed by β_1, λ_1, β_2 and λ_2. The quantized output of each stage is combined in a digital filtering network designed to cancel the quantizer errors of the first two stages.

If the resonator transfer function is given by

$$R(z) = \frac{z^{-2}}{1+z^{-2}},$$

Equation 2-36

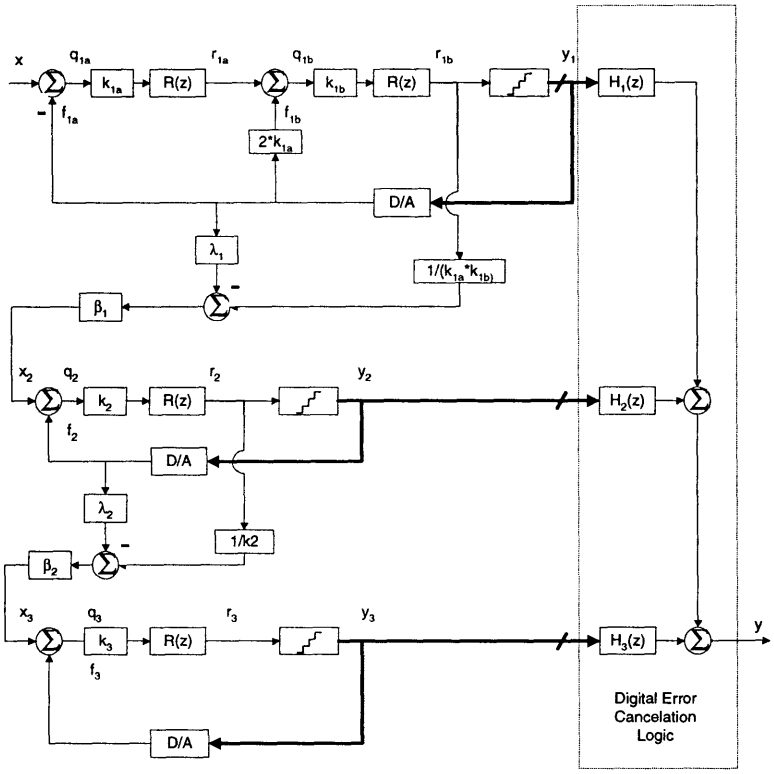


Figure 2.7 Block diagram of 4-2-2 architecture

and the quantizers and D/A converters are modeled as described in Section 2.1.1, it can easily be calculated that the outputs of each stage are given by following expressions:

$$Y_1(z) = z^{-4} \cdot (X(z) - E_{D1}(z)) + (1 + z^{-2})^2 \cdot E_1(z),$$

Equation 2-37

$$Y_2(z) = z^{-2} \cdot (X_2(z) - E_{D2}(z)) + (1 + z^{-2}) \cdot E_2(z) \text{ and}$$

Equation 2-38

$$Y_3(z) = z^{-2} \cdot (X_3(z) - E_{D3}(z)) + (1 + z^{-2}) \cdot E_3(z),$$

Equation 2-39

where $E_{D1}(z)$, $E_{D2}(z)$ and $E_{D3}(z)$ are z-transforms of the D/A errors, while $E_1(z)$, $E_2(z)$ and $E_3(z)$ are the quantizer errors for the first, second and the third stage, respectively. The inputs to the second and the third stages are

$$X_2(z) = \beta_1 \cdot \left[(1-\lambda_1)\cdot Y_1(z) - E_1(z)\right] \text{ and}$$

Equation 2-40

$$X_3(z) = \beta_2 \cdot \left[(1-\lambda_2)\cdot Y_2(z) - E_2(z)\right],$$

Equation 2-41

and the overall output of the 4-2-2 architecture, Y(z), is given by

$$Y(z) = H_1(z)\cdot Y_1(z) + H_2(z)\cdot Y_2(z) + H_3(z)\cdot Y_3(z),$$

Equation 2-42

where the transfer functions $H_1(z)$, $H_2(z)$ and $H_3(z)$ comprise the error cancellation logic. They are chosen so that the quantization error of the first and second stages, $E_1(z)$ and $E_2(z)$, are canceled, and are implemented digitally. The transfer functions that satisfy the requirement are

$$H_1(z) = z^{-4}\cdot(1+(\lambda_{1d}-1)\cdot(1+z^{-2})^2)\cdot(1+(\lambda_{2d}-1)\cdot(1+z^{-2})^3),$$

Equation 2-43

$$H_2(z) = \frac{1}{\beta_{1d}}\cdot(1+z^{-2})^2\cdot z^{-2}\cdot(1+(\lambda_{2d}-1)\cdot(1+z^{-2})^3) \text{ and}$$

Equation 2-44

$$H_3(z) = \frac{1}{\beta_{1d} \cdot \beta_{2d}} \cdot (1 + z^{-2})^3,$$

Equation 2-45

where β_{1d}, β_{2d}, λ_{1d} and λ_{2d} are digital coefficient that have the same values as the analog coefficients β_1, β_2, λ_1 and λ_2 in the absence of the mismatch.

The overall output of the 4-2-2 architecture, combining above equations and neglecting the higher order terms, is

$$\begin{aligned} Y(z) = {} & z^{-8} \cdot X(z) + \sigma_{\beta_1}^2 \cdot z^{-4} \cdot (1 + z^{-2})^2 \cdot E_1(z) + \sigma_{\beta_2}^2 \cdot \frac{1}{\beta_{1d}} \cdot z^{-2} \cdot (1 + z^{-2})^3 \cdot E_2(z) \\ & + \frac{1}{\beta_{1d} \cdot \beta_{2d}} \cdot (1 + z^{-2})^4 \cdot E_3(z) - z^{-8} \cdot E_{D1}(z) + \frac{1}{\beta_{1d}} \cdot z^{-4} \cdot (1 + z^{-2})^2 \cdot E_{D2}(z) \\ & + \frac{1}{\beta_{1d} \cdot \beta_{2d}} \cdot z^{-2} \cdot (1 + z^{-2})^3 \cdot E_{D3}(z). \end{aligned}$$

Equation 2-46

2.2.1.2 PERFORMANCE MODELING

In the presence of the mismatch, the analog coefficient will not match their exact values and will therefore not precisely match the digital coefficients. As a result, not all of the quantization error will get canceled, causing the quantization error from the first and the second stages to leak into the output, degrading the performance of the cascaded converter in comparison to the equivalent order single-loop converter. This section will quantify how much of the performance degradation can be expected for a given amount of mismatch.

The matching error is defined such that

$$\delta_{\beta_i} = \frac{\beta_{id} - \beta_i}{\beta_{id}}$$

Equation 2-47

and

$$\delta_{\lambda_i} = \frac{\lambda_{id} - \lambda_i}{\lambda_{id}}$$

Equation 2-48

for i=1 and 2.

Under the white noise approximation we can apply the formula for the quantization noise for a single-loop converter to each stage in 4-2-2 architecture. If in addition we assume that the three quantizer error terms are uncorrelated with each other, so that their power spectra add to obtain the total noise power, it follows from Equation 2-31 that the quantizer error in the signal band is

$$S_{ee} \approx \sigma_{\beta_1}^2 \frac{\pi^4}{5 \cdot M^5} \cdot \sigma_{E_1}^2 + \sigma_{\beta_2}^2 \cdot \frac{1}{\beta_{1d}^2} \cdot \frac{\pi^6}{7 \cdot M^7} \cdot \sigma_{E_2}^2 + \frac{1}{\beta_{1d}^2 \cdot \beta_{2d}^2} \cdot \frac{\pi^8}{9 \cdot M^9} \cdot \sigma_{E_3}^2,$$

Equation 2-49

where $\sigma_{\beta_1}^2$ and $\sigma_{\beta_2}^2$ are variances of δ_{β_1} and δ_{β_2}, and are given with the following expression:

$$\sigma_{\delta_{\beta_i}}^2 = \frac{\sigma_{\beta_i}^2}{\beta_{id}^2}$$

Equation 2-50

for i=1 and 2.

Using the expression for the variance of quantizer error as given by white noise approximation in Equation 2-4, we arrive at the following expression for the performance of 4-2-2 architecture

$$S_{ee} \approx \sigma^2_{\beta_1} \frac{\pi^4}{5 \cdot M^5} \cdot \frac{\Delta^2}{12 \cdot (2^{N1}-1)^2} + \sigma^2_{\beta_2} \cdot \frac{1}{\beta^2_{1d}} \cdot \frac{\pi^6}{7 \cdot M^7} \cdot \frac{\Delta^2}{12 \cdot (2^{N2}-1)^2} + \frac{1}{\beta^2_{1d} \cdot \beta^2_{2d}} \cdot \frac{\pi^8}{9 \cdot M^9} \cdot \frac{\Delta^2}{12 \cdot (2^{N3}-1)^2}.$$

Equation 2-51

In the ideal case, namely in the absence of the mismatch and for digital error gains, β_{1d} and β_{2d}, equal to one, the performance of 4-2-2 architecture is comparable to the ideal performance of the single-loop converter of the same order, since the output noise is then

$$S_{ee} \approx \frac{1}{\beta^2_{1d} \cdot \beta^2_{2d}} \cdot \frac{\pi^8}{9 \cdot M^9} \cdot \frac{\Delta^2}{12 \cdot (2^{N3}-1)^2}.$$

Equation 2-52

In the presence of the mismatch, the situation changes. The expressions for SNR and DR are as follows

$$SNR \approx \frac{\frac{A_x^2}{2}}{\sigma^2_{\beta_1} \frac{\pi^4}{5 \cdot M^5} \cdot \frac{\Delta^2}{12 \cdot (2^{N1}-1)^2} + \sigma^2_{\beta_2} \cdot \frac{1}{\beta^2_{1d}} \cdot \frac{\pi^6}{7 \cdot M^7} \cdot \frac{\Delta^2}{12 \cdot (2^{N2}-1)^2} + \frac{1}{\beta^2_{1d} \cdot \beta^2_{2d}} \cdot \frac{\pi^8}{9 \cdot M^9} \cdot \frac{\Delta^2}{12 \cdot (2^{N3}-1)^2}},$$

Equation 2-53

and

$$DR \approx \frac{\frac{\Delta^2}{8}}{\sigma^2_{\beta_1} \frac{\pi^4}{5 \cdot M^5} \cdot \frac{\Delta^2}{12 \cdot (2^{N1}-1)^2} + \sigma^2_{\beta_2} \cdot \frac{1}{\beta^2_{1d}} \cdot \frac{\pi^6}{7 \cdot M^7} \cdot \frac{\Delta^2}{12 \cdot (2^{N2}-1)^2} + \frac{1}{\beta^2_{1d} \cdot \beta^2_{2d}} \cdot \frac{\pi^8}{9 \cdot M^9} \cdot \frac{\Delta^2}{12 \cdot (2^{N3}-1)^2}}.$$

Equation 2-54

If we define ΔDR to be the fractional reduction in DR due to mismatch, we obtain that

$$\Delta DR = \frac{DR(\sigma_{\beta_{\beta_1}} = 0,\ \sigma_{\beta_{\beta_2}} = 0)}{DR(\sigma_{\beta_{\beta_1}} \neq 0,\ \sigma_{\beta_{\beta_2}} \neq 0)}$$

$$= 1 + \sigma^2_{\delta_{\beta_2}} \cdot \beta^2_{2d} \cdot \frac{9}{7} \cdot \left(\frac{M}{\pi}\right)^2 \cdot \left(\frac{2^{N3}-1}{2^{N2}-1}\right)^2 + \sigma^2_{\delta_{\beta_1}} \cdot \beta^2_{1d} \cdot \beta^2_{2d} \cdot \frac{9}{5} \cdot \left(\frac{M}{\pi}\right)^4 \cdot \left(\frac{2^{N3}-1}{2^{N1}-1}\right)^2 .$$

Equation 2-55

Note that if $\sigma_{\delta_{\beta_1}} \approx \sigma_{\delta_{\beta 2}}$, the $\sigma_{\delta_{\beta_1}}$ term will dominate, and the dynamic range loss is proportional to the fourth power of oversampling ratio. For small oversampling ratios, this results in a reasonable matching requirements. Figure 2.8 illustrates the dynamic range reduction for various values of matching errors and for several different values of N1, N2 and N3, under the assumptions that $\sigma_{\delta_{\beta_1}} \approx \sigma_{\delta_\beta}$, $\beta_{1d} = \beta_{2d} = 1$ and M=16. For a loss in dynamic range less than 1dB, the mismatch in a 4-2-2 architecture with N1=N2=N3=1 must be less than 1.5%.

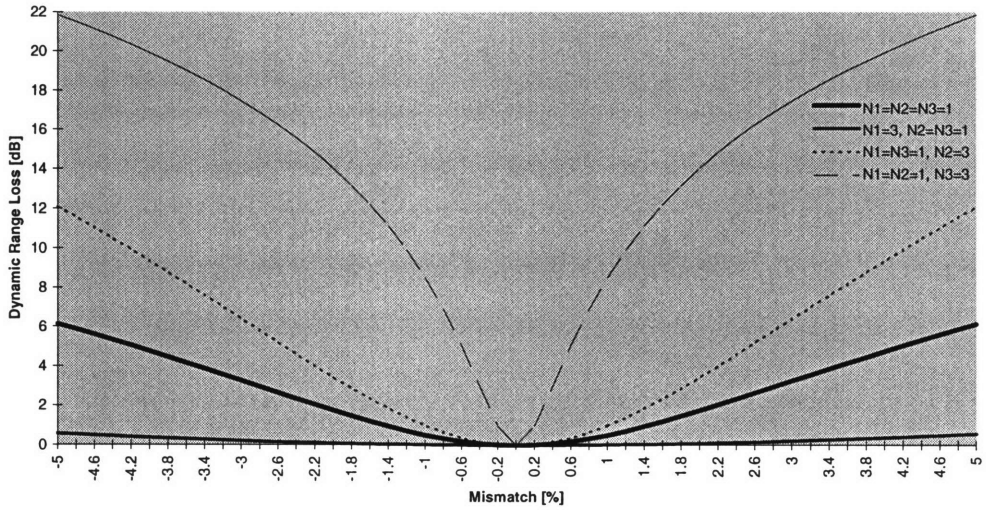


Figure 2.8 Effect of mismatch on dynamic range in the 4-2-2 architecture.

2.3 SUMMARY

Basic principles of bandpass sigma-delta conversion were reviewed. In particular, operation and performance modeling of two classes of sigma-delta converters, single-loop and cascaded converters, have been discussed. Modeling of single-loop converters has been discussed for a general case of an L-th order, N-bit converter, assuming Bennett's noise model. Model of L-th order, 1-bit converter has also been presented, assuming white noise approximation. Cascaded converters have been discussed by modeling operation and performance of a 4-2-2 architecture, that will prove to be useful for wide bandwidth systems in next chapter.

2.4 Appendix A

Looking at Figure 2.2, we see that we can express Y(z) as

$$Y(z) = G \cdot U(z),$$

and U(z) as

$$U(z) = (\cdots((Q \cdot R_0(z) - b_1 \cdot Y(z)) \cdot R_1(z) - b_2(z) \cdot Y(z)) \cdot R_2(z) - \cdots) \cdot R_{L/2-2} - b_{L/2-1} \cdot Y(z)) \cdot R_{L/2-1},$$

so that after rearranging the terms we get that

$$U(z) = Q(z) \cdot \prod_{i=0}^{L/2-1} R_i(z) - Y(z) \cdot \sum_{i=1}^{L/2-1} b_i \cdot \prod_{j=i}^{L/2-1} R_j(z).$$

Substituting for Y(z) and rearranging the terms further, we obtain that the transfer function of the loop filter is:

$$A(z) = \frac{U(z)}{Q(z)} = \frac{\prod_{i=0}^{L/2-1} R_i(z)}{1 + G \cdot \sum_{i=1}^{L/2-1} b_i \cdot \prod_{j=i}^{L/2-1} R_j(z)}.$$

Substituting the expression for A(z) back into Equation 2-8 and Equation 2-9, we obtain the expressions for STF and NTF to be

$$H_x(z) = \frac{G \cdot \prod_{i=0}^{L/2-1} R_i(z)}{1 + G \cdot \sum_{i=0}^{L/2-1} b_i \cdot \prod_{j=i}^{L/2-1} R_j(z)}$$

$$H_E(z) = \frac{1}{1 + G \cdot \sum_{i=0}^{L/2-1} b_i \cdot \prod_{j=i}^{L/2-1} R_j(z)}.$$

Substituting the expression for $R_i(z)$, Equation 2-14, into the above expressions, and further rearranging the terms, we finally obtain the following expressions for STF and NTF, respectively:

$$H_x(z) = \frac{G \cdot \prod_{i=0}^{L/2-1} K_i \cdot z^{-L}}{(1+z^{-2})^{L/2} + G \cdot \sum_{i=0}^{L/2-1} b_i \cdot (-1)^{L/2-i} \cdot z^{2 \cdot i - L} \cdot (1+z^{-2})^i \cdot \prod_{j=i}^{L/2-1} K_j}$$

$$H_E(z) = \frac{(1+z^{-2})^{L/2}}{(1+z^{-2})^{L/2} + G \cdot \sum_{i=0}^{L/2-1} b_i \cdot (-1)^{L/2-i} \cdot z^{2 \cdot i - L} \cdot (1+z^{-2})^i \cdot \prod_{j=i}^{L/2-1} K_j}.$$

Note that $(-z^{-2})^{L/2} = (-1)^{L/2} \cdot z^{-L}$ since by definition L is an even number.

Combining our results with the Equation 2-12, we have that in the signal band, i.e. for $z \approx j$,

$$H_x(z) \approx z^{-L} \text{ and } H_E(z) \approx \gamma \cdot (1+z^{-2}) \text{ for } z \approx j,$$

Equation 2-56

where $\gamma = \frac{1}{G \cdot \prod_{i=0}^{L/2-1} K_i}$. Thus we can write the output of the bandpass sigma-delta in the signal

band as

$$Y(z) \approx X(z) - E_D(z) + \gamma \cdot (1 + z^{-2})^{L/2} \cdot E_Q(z), \text{ where } \gamma = \frac{1}{G \cdot \prod_{i=0}^{L/2-1} K_i}.$$

To evaluate the performance of such a converter, we need to find the total signal and noise power at the output of the converter, S_{xx} and S_{ee} respectively. Given that

$$S_{xx} = 2 \cdot \int_{\frac{f_s}{4}-\frac{f_B}{2}}^{\frac{f_s}{4}+\frac{f_B}{2}} P_{xy(z)df}$$

and

$$S_{ee} = 2 \cdot \int_{\frac{f_s}{4}-\frac{f_B}{2}}^{\frac{f_s}{4}+\frac{f_B}{2}} P_{ey(z)df},$$

the first step is to evaluate the power spectral densities of the signal and noise at the output of the converter, $P_{xy}(f)$ and $P_{Ey}(f)$, based on the power spectral densities of the signal and noise at the input of the converter, $P_x(f)$ and $P_E(f)$. Using the fact that if a stationary random process with power spectral density P(f) is the input to a linear filter with transfer function H(f), the power spectral density of the output random process is $P_y(f) = P(f) \cdot |H(f)|^2$, and using the white noise approximation, we can write

$$P_{xy}(z) = P_x(z) \cdot |H_x(z)|^2$$

Equation 2-57

and

$$P_{Ey}(z) = P_E(z) \cdot \left|H_E(z)\right|^2 .$$

Equation 2-58

For a sinusoid input, $x(t) = A_x \cdot \sin(\omega_x \cdot t)$, the power spectral density is

$$P_x(z) = \frac{A_x^2}{2}.$$

Equation 2-59

Under the white noise approximation, the power spectral density of the noise at the input of the converter is

$$P_E(f) = \frac{\sigma_E^2}{f_s}.$$

Equation 2-60

It follows from the Equation 2-56 that

$$\left|H_x(z)\right|^2 = 1$$

Equation 2-61

and that

$$\left|H_E(z)\right| = \left|\gamma \cdot (1 + z^{-2})^{L/2}\right|.$$

Making the use of the transformation between the z-transform and the frequency domain response, i.e.

$$z = e^{t\cdot\omega\cdot T} = e^{j\frac{2\cdot\pi\cdot f}{f_s}},$$

we can write that

$$|H_E(z)| = \left|\gamma\cdot(1+e^{-2\frac{j\cdot 2\cdot\pi\cdot f}{f_s}})^{L/2}\right| = \gamma\cdot\left(\sqrt{\left(1+\cos(2\cdot\frac{2\cdot\pi\cdot f}{f_s})\right)^2+\sin^2(2\cdot\frac{2\cdot\pi\cdot f}{f_s})}\right)^{L/2} =$$

$$= \gamma\cdot\left(\sqrt{2\cdot(1+\cos(2\cdot\frac{2\cdot\pi\cdot f}{f_s}))}\right)^{L/2} = 2\cdot\gamma\cdot\left(\sqrt{\cos^2(\frac{2\cdot\pi\cdot f}{f_s})}\right)^{L/2}$$

$$= 2\cdot\gamma\cdot\cos^{L/2}(\frac{2\cdot\pi\cdot f}{f_s}).$$

Using the trigonometric identities, we obtain that

$$\cos(\frac{2\cdot\pi\cdot f}{f_s}) = -\sin(\frac{2\cdot\pi\cdot(f-\frac{f_s}{4})}{f_s}).$$

Using the approximation that

$$\sin(x) \approx x \text{ for } x << 1,$$

we can conclude that

$$\sin(\frac{2\cdot\pi\cdot(f-\frac{f_s}{4})}{f_s}) \approx 0 \text{ for } f \approx \frac{f_s}{4},$$

and it follows that

$$\cos(\frac{2\cdot\pi\cdot f}{f_s}) \approx \frac{2\cdot\pi\cdot(\frac{f_s}{4}-f)}{f_s} \text{ for } f \approx \frac{f_s}{4}.$$

Using this approximation, we can now write

$$\left|H_E(z)\right|^2 = 4\cdot\gamma^2\cdot\cos^L\left(\frac{2\cdot\pi\cdot f}{f_s}\right) = 4\cdot\gamma^2\cdot\left(\frac{2\cdot\pi\cdot\left(\frac{f_s}{4}-f\right)}{f_s}\right)^L.$$

Equation 2-62

Combining Equation 2-57, Equation 2-59 and Equation 2-61, we arrive at the following expression for S_{xx}:

$$S_{xx} = \frac{A_x^2}{2}.$$

Equation 2-63

Combining Equation 2-58, Equation 2-60 and Equation 2-62, we obtain the following expression for the output quantizer noise power, S_{ee}:

$$S_{ee} = 2\cdot\int_{\frac{f_s}{4}-\frac{f_B}{2}}^{\frac{f_s}{4}+\frac{f_B}{2}}\frac{\sigma_E^2}{f_s}\cdot 4\cdot\gamma^2\cdot\left(\frac{2\cdot\pi\cdot\left(\frac{f_s}{4}-f\right)}{f_s}\right)^L df = \gamma^2\cdot\sigma_E^2\cdot\frac{\pi^L}{(L+1)\cdot M^{L+1}}.$$

Using the expression for the variance of the quantization noise derived from white noise approximation, as given by the Equation 2-4 , we obtain that

$$S_{ee} = \gamma^2\cdot\frac{\Delta^2}{12\cdot(2^N-1)^2}\cdot\frac{\pi^L}{(L+1)\cdot M^{L+1}}.$$

Equation 2-64

Finally, combining Equation 2-63 and Equation 2-64, we arrive at the expression for SNR ,

$$SNR = \frac{S_{xx}}{S_{ee}} = \frac{6\cdot A_x^2}{\Delta^2}\cdot\frac{1}{\gamma^2}\cdot\frac{(L+1)}{\pi^L}\cdot(2^N-1)^2\cdot M^{L+1}.$$

Assuming that full-scale sinusoidal input has an amplitude of $A_{x\,max} = \frac{\Delta}{2}$, so that

$$S_{x\,max} = \frac{A_{x\,max}^2}{2} = \frac{\Delta^2}{8},$$

and calculating that

$$S_{x\,one} = \frac{A_{x\,one}^2}{2} = \frac{\pi^L \cdot \gamma^2 \cdot \Delta^2}{12 \cdot (L+1) \cdot (2^N - 1)^2 \cdot M^{L+1}},$$

it follows that

$$DR = \frac{S_{x\,max}}{S_{x\,one}} = \frac{3}{2} \cdot \frac{1}{\gamma^2} \cdot \frac{(L+1)}{\pi^L} \cdot (2^N - 1)^2 \cdot M^{L+1}.$$

CHAPTER 3

SYSTEM ARCHITECTURE

3.0 INTRODUCTION

The first step in designing a sigma-delta converter is choosing the system architecture that best suits the application in hand. The choice of system architecture includes the choice of converter architecture, oversampling ratio, the converter order and number of bits in quantizer. Two main architectural classes of sigma-delta converters, single-loop and cascaded architectures, are briefly reviewed in previous chapter, and their numerous topologies for multitude of different converter orders, number of bits employed, as well as oversampling ratios abundantly documented in previous literature for narrowband and medium bandwidth lowpass systems. The abundance of literature on narrowband and medium bandwidth lowpass sigma-delta converters stems from the fact that, due to the oversampling, the sampling rate of sigma-delta converters usually needs to be several orders of magnitude higher than the Nyquist rate, finding the sigma-delta converter best suited for relatively low bandwidth signals. Considerations for choosing the system architecture for sigma-delta conversion of wide bandwidth systems are somewhat different, and are not nearly as well researched in previous literature.

This chapter therefore starts the task of choosing the system architecture with the brief discussion in Section 3.1 of issues involved in sigma-delta conversion of wide-bandwidth systems, pointing out the major differences from narrowband design. Section 3.2 then discusses the system level design in the ideal case, for the architecture decided upon based on the considerations discussed in Section 3.1. This design is broken up in two parts. First part involves the choice of system parameters, such as D/A reference voltages, error gains, error

mixing coefficients and resonator gains. This part of design heavily relies on the behavioral simulations performed in MIDAS [55], since not all of the effects that system level parameters have on converter performance can easily be captured analytically. Second part consists of modeling the major converter building blocks in the ideal case, for the system parameters chosen.

3.1 CHOOSING THE ARCHITECTURE: CONSIDERATIONS IN SIGMA-DELTA CONVERSION OF WIDE-BANDWIDTH SYSTEMS

The main goals driving the choice of the architecture for the converter design in this work are summarized in Table 3.1.

PARAMETER	SPECIFICATION
SNR_{max}	> 62 dB
$SNDR_{max}$	> 57dB
Power Dissipation	< 50 mW
Bandwidth	1.23 MHz
Jammer	< 0.235 V_p
CDMA Signal	< 2.69 mV_p

Table 3-1 Summary of the performance goals

Equation 2-32 that describes the performance of both single- and multi-loop architectures in the ideal case indicate that the desired SNR_{max} can be achieved by

- increasing M,
- increasing L, and
- increasing N.

Unfortunately, increasing M and L results in increase in power consumption, while increasing N results in increased circuit complexity, as will be discussed next.

Increasing the oversampling ratio, M. The power dissipation in sigma-delta converter for low to medium bandwidth is proportional to sampling frequency, fs, and therefore the

oversampling ratio, M [40]. In sigma-delta converter for wide bandwidth signals, on the other hand, the power dissipation grows as the sampling frequency squared [40], i.e.

$$P \propto f_s^2$$

Equation 3-1

which translates to $P \propto M^2$. Since our system is wide bandwidth, it becomes crucial to choose minimal oversampling ratio that will still allow us to achieve the performance goals. Reducing the oversampling ratio will, on the other hand, increase both the in-signal-band quantization noise and the in-signal-band circuit noise produced by the resonator circuits. The point here is that the choice of M involves a compromise.

Increasing the converter order, L. Increasing L increases the number of amplifiers in the circuitry. As already discussed, the amplifiers are the single piece of circuitry in the analog part of the sigma-delta converter that consume the most power. At low oversampling ratios, the effectiveness of increasing the converter's order L is significantly diminished, as illustrated in Figure 2.5. Therefore, for wide bandwidth systems, L should be chosen as small as possible while still allowing the target performance.

Increasing the quantizer resolution, N. The effectiveness of increasing the quantizer resolution is independent of the oversampling ratio and is therefore particularly attractive in the wide bandwidth applications. While the single-loop converters based on multibit quantization are tolerant of nonlinearity in the quantizer thanks to the noise shaping, they impose stringent linearity requirement on D/A converter. This is due to the fact that any error due to N-bit D/A non-linearity will enter the converter at its input and will therefore not be attenuated by noise shaping. The D/A precision therefore limits the converter linearity and resolution. Self-calibration [17] or digital cancellation methods [12] are necessary to relax the requirements on N-bit D/A converter, which in turn complicates the circuitry and burns more power.

There are several ways of eliminating the dependence of the sigma-delta converter on the D/A linearity. The simplest way is to reduce its resolution to a single bit. Because there is only one comparison level and only two output levels , there can be no differential or integral non-linearity. The D/A error term will then at worst introduce a DC offset and gain error. The

penalty to pay for inherent linearity of a single bit D/A converter is the instability in the single-loop converters of order greater than two, due to its large quantization noise [43]. Architectural modifications typically employed to extend the input range for which stable operation is maintained in higher-order single-loop converters include, for lowpass case, limiting the magnitude of the error transfer function at out-of-band frequencies to less than 2 [41], placing limiters across each integrating capacitor to prevent large values from appearing at the integrator outputs [8], or resetting the integrators if it is detected that their values are becoming too large [42]. Unfortunately, they generally reduce the dynamic range below that predicted by Equation 2-35.

Using multi-loop architectures, the full dynamic range can be achieved for L>2 by cascading several first- or second-order single-bit stages. Such cascaded converters have two advantages over other high-order single-loop techniques. First, because stable first- and second-order single-bit converter stages can be used to compose a cascaded converter, no unstable oscillations will be excited in the converter as a whole, i.e. these converters are inherently stable. The second advantage involves noise tones at the output. In the error spectrum of a single-loop converter, discrete spectral tones can be generated. In the lowpass case, these tones are most evident in the first-order converters, have been demonstrated in the second- and fourth-order converters, and are believed to exist in all single-loop converters [36]. In a cascaded converter, the later stages tend to randomize the noise and eliminate these tones. The two motivating factors behind the study of the cascaded converters were therefore inherent stability and the improved suppression of the discrete noise tones. Cascaded converter that employs single-bit to eliminate the dependence on D/A linearity, was therefore the architecture of choice for this work.

It should be noted here for the future reference that the multibit D/A could be placed in the latter stages so that the noise shaping reduces the effect of multibit D/A nonlinearity [5]. This then becomes a viable approach for increasing DR at low oversampling ratios. The structure becomes extremely sensitive to mismatch, as illustrated in Figure 2.8, offsetting the advantage somewhat.

Now that we have decided on the basic architecture, we still need to decide on M and L. How low of M and L can we choose for our work?

Table 3.2 presents several combinations of the oversampling ratio and the converter's order capable of achieving the necessary SNRmax. The calculations are based on the performance modeling of cascaded converters in the ideal case, i.e. in the absence of mismatch and for

L	M	DR [dB]
4	16	49
4	32	64
4	64	79
6	16	64
6	32	86
8	8	53
8	16	80

Table 3-2 Required oversampling ration and converter order

digital error gains, β_{1d} and β_{2d}, equal to one, as given in Section 2.2.1.2, and for N=1. From both these calculations of the converter performance and the empirical evidence from the previously published works, a target oversampling ratio of M=16 and the converter order of L=8 have been chosen.

There are two basic topologies that could be used to implement the architecture of choice, 4-2-2 topology described in the previous section, and the 4-4 topology . The behavioral simulations done in [21] reveal that with the optimal loop coefficients, the two topologies have the same overloading input level, but the SNR of the former is about 8 dB better than the latter. This is mainly due to the higher overloading input level for a second-order bandpass sigma-delta converter than for a single-loop fourth-order one. The 4-2-2 topology therefore becomes the topology of choice.

3.2 THE ARCHITECTURE OF CHOICE: SYSTEM LEVEL DESIGN IN THE IDEAL CASE

Issues involved in sigma-delta conversion of wide bandwidth systems were discussed in previous section, leading to the choice of 4-2-2 single-bit cascaded converter as the architecture of choice. This section proceeds to further specify the architecture for the application in hand, by choosing the optimal architecture parameters, namely the error gains, error mixing coefficients, as well as the resonator gains.

3.2.1 CHOOSING THE SYSTEM PARAMETERS

The analysis of the basic operation and the performance modeling of 4-2-2 architecture is already presented in previous chapter, in Section 2.2.1. The block diagram of Figure 2.7 is for convenience repeated here in Figure 3.1, for the case where N1=N2=N3=1. The digital cancellation circuitry is included, while the quantizer and D/A converter of Figure 2.7 are replaced with the quantization function Q(x). The resonator transfer function is as given by Equation 2-36.

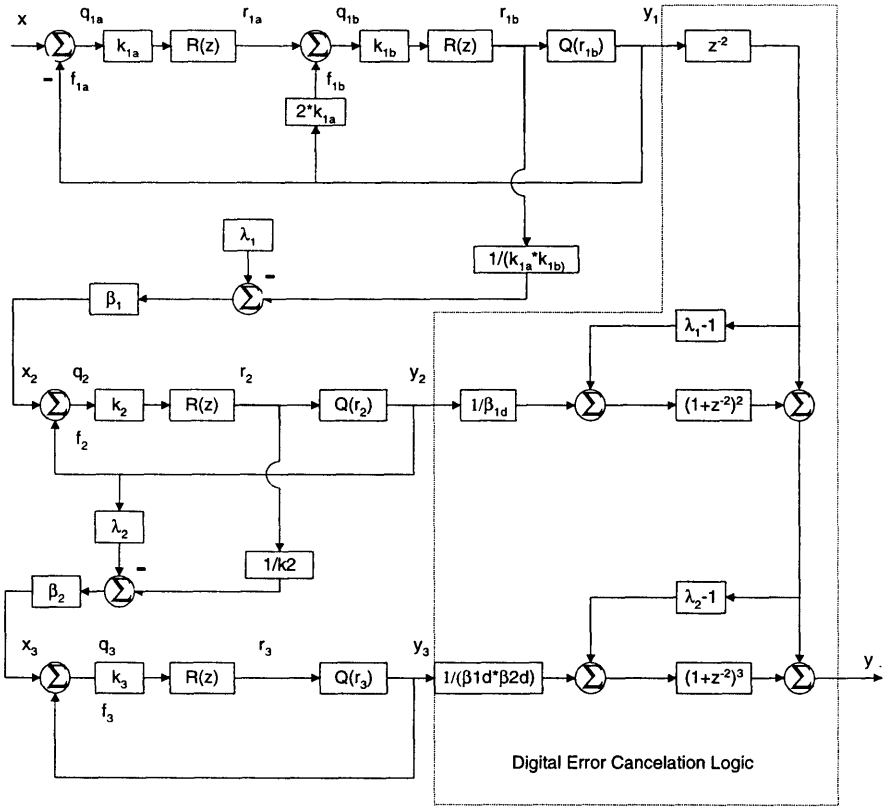


Figure 3.1 Flow diagram of the 4-2-2 Architecture

The performance modeling given in Section 2.2.1.2 provided useful insight in predicting many of the aspects of the converter performance, including for example the effect of the mismatch among stages. This insight was used in determining the values of M, L and N necessary to achieve the desired performance. Unfortunately, the performance modeling of Section 2.2.1.2 relies on the assumption that the effective gain of the quantizer and the noise power are constant with respect to the input amplitude, and independent of the system parameters such

as D/A reference voltage, V_{ref}, error gains β_1 and β_2, and the error mixing coefficients λ_1 and λ_2. Consequently, performance modeling cannot be used to choose optimal system parameters, but rather we must rely on the behavioral simulations.

For example, the expression for SNR and DR given in Equation 2-53 and Equation 2-54, respectively, appear to be independent of the error mixing coefficients, λ_1 and λ_2. As will be shown in the next section, the values of λ_1 and λ_2 do affect the converter performance, despite the predictions of these equations . Their values can be chosen to constraint the signal range at the inputs of the second and the third stage to allow the largest possible values of the error gains β_1 and β_2 for optimizing both the SNR_{max}, the overload point and the low-level SNR. For example, the maximum input to the third stage can be expressed as:

$$x_3 = \lambda_2 \cdot (x_2 + \frac{\Delta}{2} - \beta_2 \cdot \frac{\Delta}{2}).$$

Equation 3-2

Only if λ_2 is equal to one can the maximum value of β_2 be allowed for a given input level to the third stage. If β_2 is also equal to one, the third stage will not overload before the second stage does. We say that the converter is overloaded when its in-band noise starts to increase with the input level, as will be discussed shortly. These predictions are verified by the behavioral simulations in the next section.

3.2.1.1 BEHAVIORAL SIMULATIONS AND RESULTS

All the behavioral simulations were performed using MIDAS for the quantization limited system, with the oversampling ratio of 16. They were performed with the consideration that all the system parameters should be chosen in such a way as to maximize SNR_{max}, the input overload level and the low-level SNR, following the design guidelines for choosing the system level parameters outlined in [36]. All the digital coefficients are required to be powers of two in order to simplify the digital circuitry.

Choosing the D/A reference voltage, V_{ref}. The first set of behavioral simulations was done in order to determine the D/A reference voltage, V_{ref}, where $V_{ref}=\Delta/2$. The SNR was

measured versus input signal level for several different values of $V_{ref.}$. The results are shown in Figure 3.2.

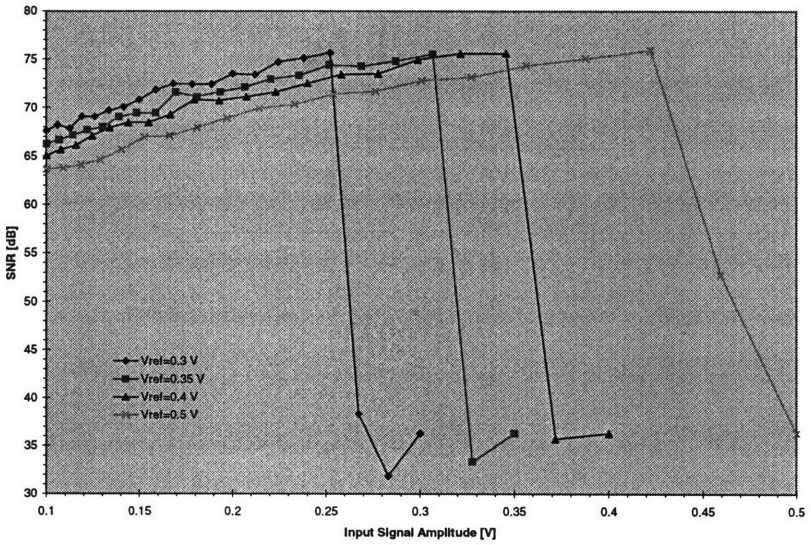


Figure 3.2 SNR vs. the input signal amplitude for various values of V_{ref}

Performance modeling of Section 2.2.1.2 tells us that SNR is inversely proportional to, and DR independent of Δ, as illustrated in Equation 2-53 and Equation 2-54, respectively. Therefore, we could conclude that Δ should be chosen to be as small as possible, i.e. $\Delta=2*A_{max}$. The results of this behavioral simulations reveal the first important characteristic of the sigma-delta conversion not predicted by the models developed in Section 2.2.1.2. Namely, the SNR peaks at an input level below the full scale, and then declines rapidly for input levels above this peak. The sigma-delta converter is said to overload at the high input levels, and the input level at which SNR peaks is called the overload level. Therefore, some margin is always necessary to account for the overload, and the full scale input level that sets the reference voltage of the D/A converter should always be designed to be higher than the minimal value of $\Delta=2*A_{max}$ predicted by the analysis of Section 2.2.1.2.

Figure 3.2 indicates that margin of at least 1.5 dB is necessary, since the overload level for this system is found to be 1.5 dB bellow the full scale. To allow for some additional margin, we

have chosen to place the maximum input signal at -3.46 dB bellow full scale, resulting in Vref=0.35 V.

Note that we should modify the definition of the useful signal range or dynamic range given by Equation 2-25 in Section 2.1.2. Hereafter, the dynamic range, DR, is defined as the ratio of the input overload power to the input power at which the SNR is one.

Choosing the first error mixing coefficient, λ_1. The next set of the behavioral simulations was done to determine the error mixing coefficient , λ_1. The SNR was measured versus input signal amplitude for several values of the first error mixing coefficient, λ_1, as shown in Figure 3.3.

Another important aspect of the sigma-delta performance exemplified in Figure 3.3 is the trade-off between the input overload level and low-level signal to noise ratio. This is further illustrated in Figure 3.4, where the input overload level and low-level SNR (SNR at Ax=-91dB) is plotted versus the first error mixing coefficient λ_1. Increasing λ_1 above approximately 1.6, the input overload level increases, while the low-level SNR decreases.

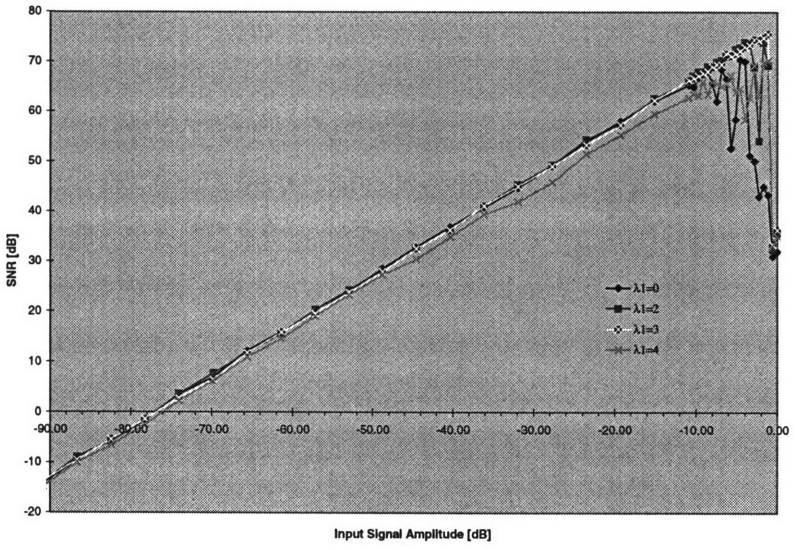


Figure 3.3 SNR vs. input signal amplitude for various values of λ_1

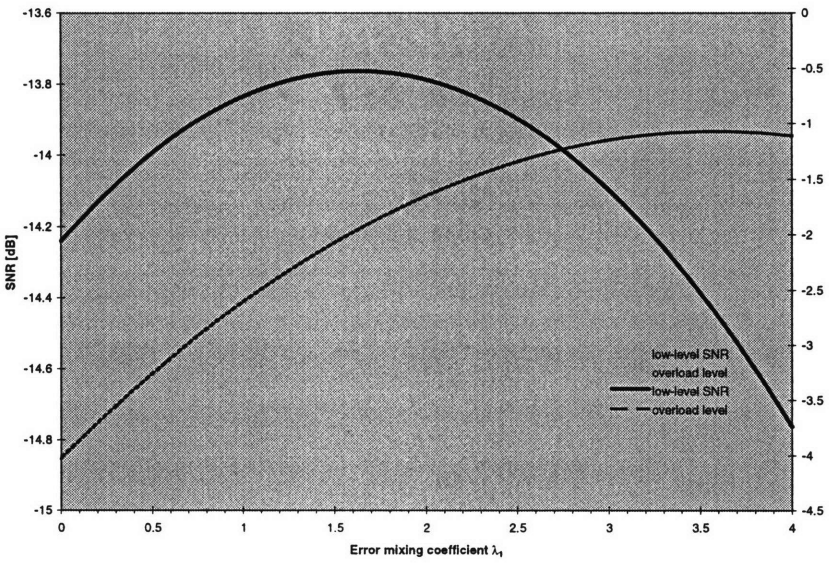


Figure 3.4. Low-level SNR and overload level trade-off

The optimum λ_1 is then the value that satisfies the following two conditions. First, it is the value of λ_1 that result in SNR_{max} that satisfies the target performance . Second, it is the value of λ_1 that maximizes the difference between the input overload level and the low-level noise. In other words, the optimum λ_1 is the value that results in SNR_{max} that satisfies the target performance, while still maximizing DR. An additional concern in choosing λ_1 is the fact that the digital coefficient λ_1-1 should be a power of 2, so that its digital implementation becomes straightforward. Figure 3.5 illustrates SNR_{max} and DR versus the first error mixing coefficient. There exist a definite peak in DR as a function of the λ_1 centered at approximately 3, and a peak in SNR_{max} of about 2.4. Since the value of SNRmax for λ_1=3 still satisfies the target performance, and makes the implementation of digital coefficient λ_1-1 easy, the value of 3 was chosen for the first error mixing coefficient.

It is important to note, that once again, the dependence of the sigma-delta performance on the first error mixing coefficient is not captured by the operation and performance modeling of Section 2.2. According to Equation 2-46, the value of λ_1 has no effect on the output of the converter. This is partly due to the fact that the higher order error terms have been neglected in

deriving this equation, and again partly due to the assumptions on which this analysis was based.

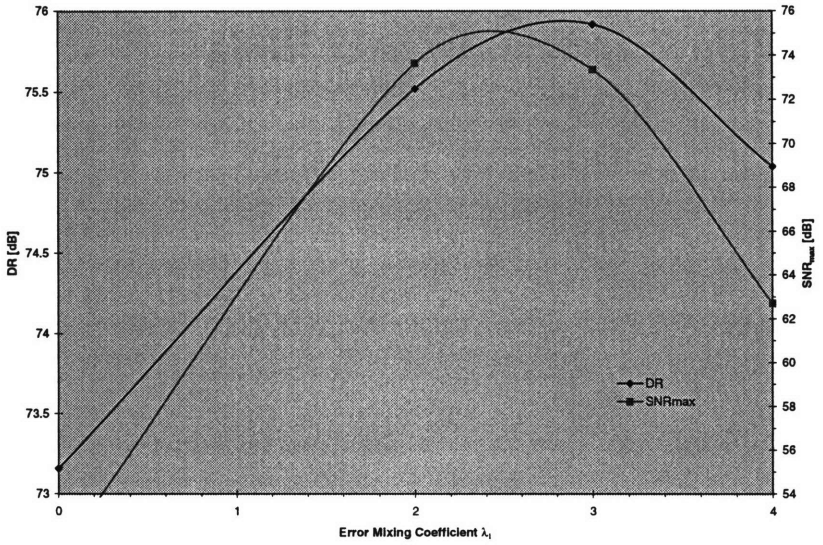


Figure 3.5 DR and SNR_{max} vs. the first error mixing coefficient

Choosing the first error gain β_1.In order to determine β_1, SNR is measured versus input signal level for several different values of this system parameter. The results are shown in Figure 3.6.

The trade-off between the low-level SNR and the overload point is evident again in Figure 3.6, and further illustrated in Figure 3.7. Here the input overload level and the low-level SNR (SNR at Ax=-91dB) are plotted versus the first error gain β_1. The overload input level increases but the low-level SNR decreases as we decrease β_1 below 1. For values of β_1 increasing above 1, both the input overload level and the low-level SNR decrease. The value of β_1 chosen as optimum was decided using the similar criteria applied to choosing the optimal λ_1 . We want the value that maximizes SNR_{max} and DR, while allowing the digital coefficient $1/\beta_1$ to be a power of 2 for easy digital implementation.

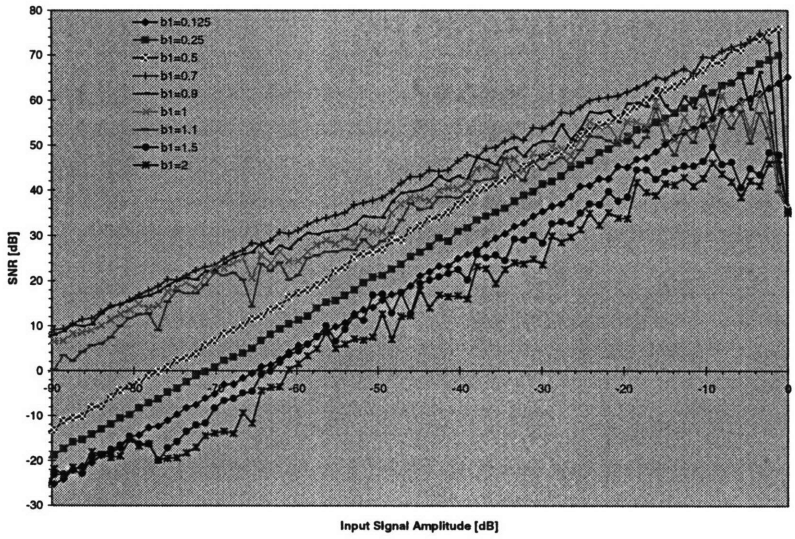


Figure 3.6 SNR vs. input signal amplitude for various values of β_1

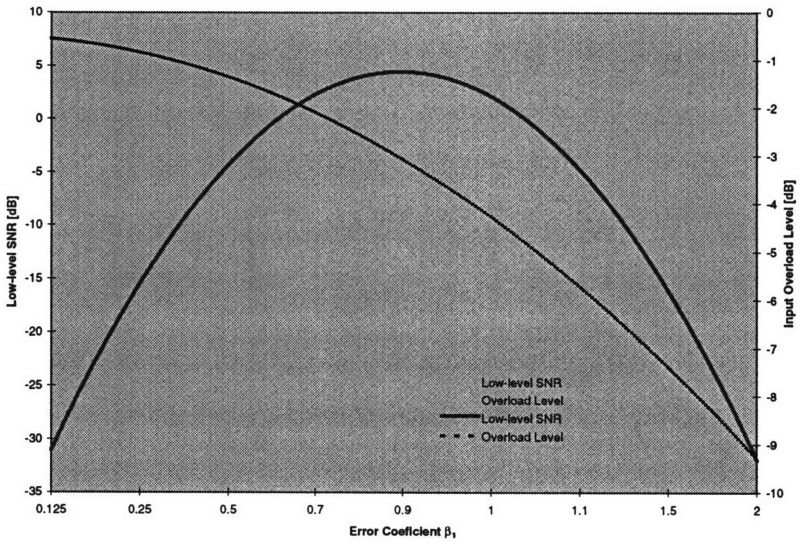


Figure 3.7 Low-level SNR and overload level trade-off

Figure 3.8 illustrates the effect of changing β_1 on SNR_{max} and the dynamic range. There is a definite peak both in the SNR_{max} and DR as a function of the first error gain, β_1, at approximately $\beta_1 \approx 0.5$ and $\beta_1 \approx 1$, respectively. The value of $\beta_1 = 0.5$ was chosen, since for $\beta_1 \approx 1$ SNR_{max} drops below the desired value.

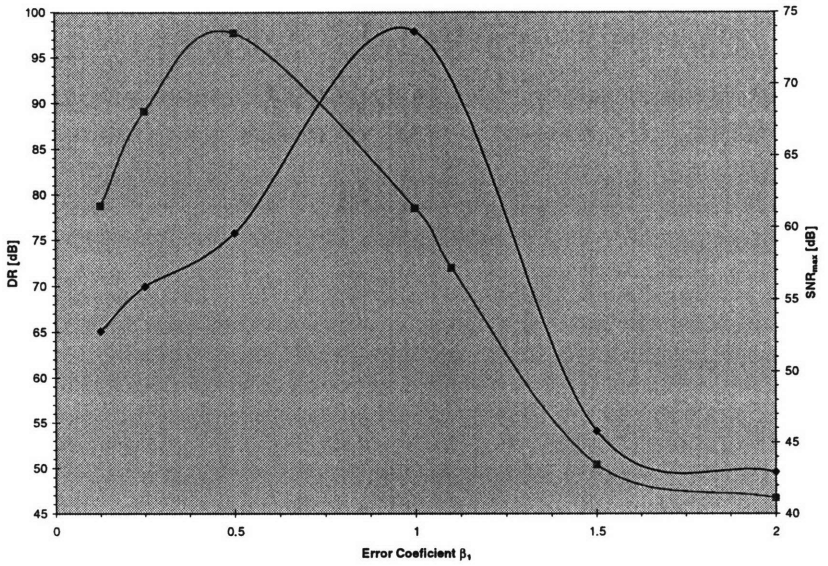


Figure 3.8 DR and SNR_{max} vs. the first error gain

Choosing the second error mixing coefficient, λ_2. The value of λ_2 was chosen in the similar manner. SNR was measured versus input signal level for several different values of this system parameter. The results are shown in Figure 3.9.

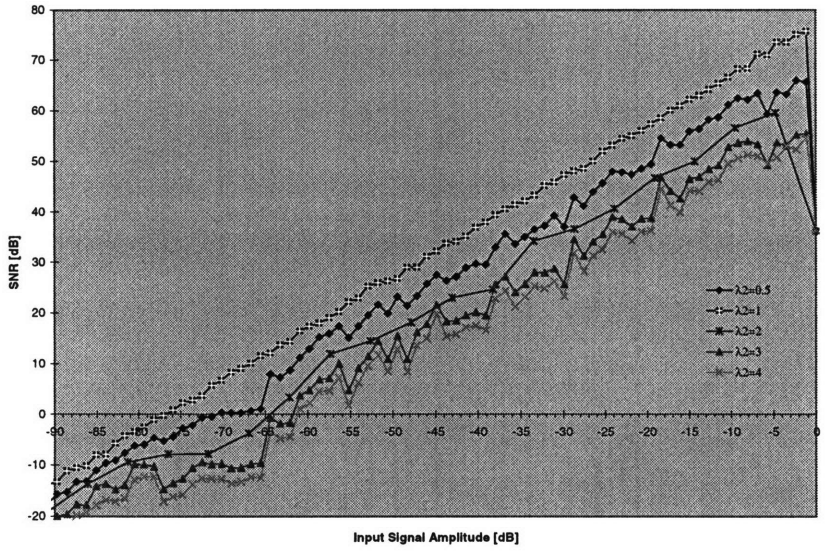


Figure 3.9 SNR vs. input signal amplitude for various values of λ_2

The data is replotted in Figure 3.10 to show SNR_{max} and DR for several different values of λ_2. Here we see a definite peak at both curves at approximately $\lambda_2 \approx 1$, and since this value also makes it easy to implement the digital coefficient $\lambda_2 - 1$, the value of $\lambda_2 = 1$ was chosen for this work.

Once again, the dependence of the sigma-delta performance on the second error mixing coefficient is not captured by the operation and performance modeling of Section 2.2, according to which the value of λ_2 have no effect either on the output of the converter, nor on the SNR or DR.

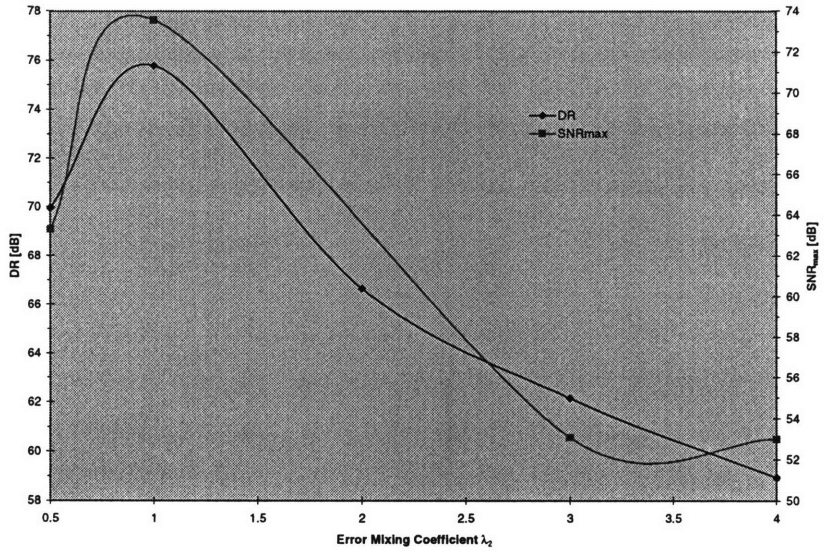


Figure 3.10 DR and SNR_{max} vs. the second error mixing coefficient

Choosing the second error gain β_2. The value of β_2 was chosen in the similar manner. SNR was measured versus input signal level for several different values of this system parameter. The results are shown in Figure 3.11. The data is replotted in Figure 3.12 to show SNR_{max} and DR versus β_2.

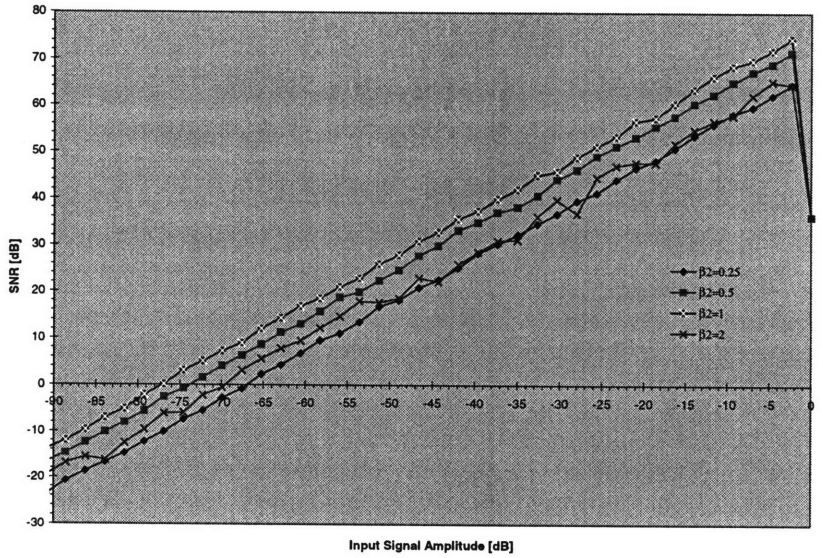


Figure 3.11 SNR vs. input signal amplitude for various values of β_2

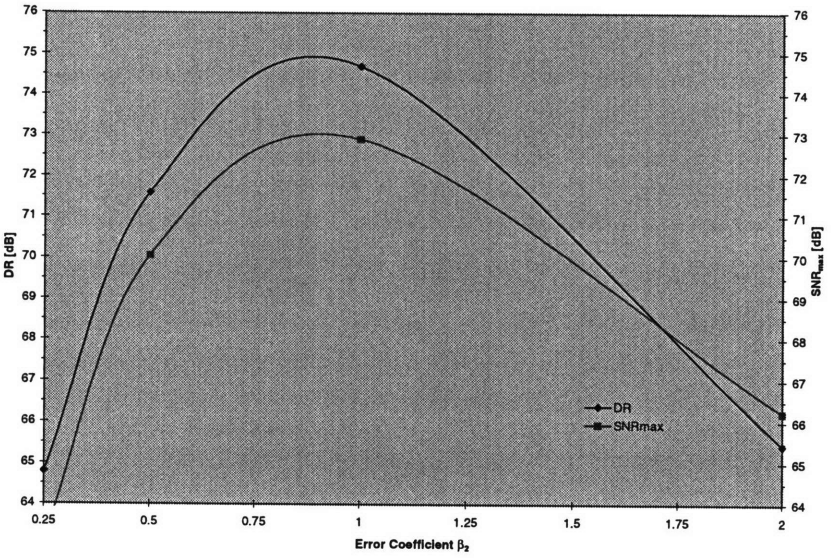


Figure 3.12 DR and SNR_{max} vs. the second error gain

Again we see a definite peak at both curves at approximately $\beta_2 \approx 1$, and since this value also makes it easy to implement the digital coefficient $1/\beta_1\beta_2$, the value of $\beta_2=1$ was chosen for this work.

Choosing the resonator gains k_{1a}, k_{1b}, k_2 and k_3. The behavioral simulations confirm that resonator gains can take any positive value without affecting the output of the modulator in each stage and the whole converter, as predicted by the Equation 2-46, but the required resonator output ranges are reduced with the resonator gain factors proportionally. The choice of the resonator gain factors k_{1a}, k_{1b}, k_2 and k_3 will therefore affect the required linear output range of the amplifiers, affecting the required maximum amplifier slew rate. We would therefore like these gains to be as small as possible. Increasing their value would, on the other hand, suppress the noise due to non-idealities from the later resonators and comparators seen at the input. The point here is that the choice of these parameters involves a trade-off and since it depends on the issues involving real circuits, its effect on the performance of the converter could have not been predicted by the performance modeling of the Section 2.2.1.2, since it is based on the ideal case.

3.2.2 MODELING THE BUILDING BLOCKS OF THE 4-2-2 ARCHITECTURE IN THE IDEAL CASE

Now that we have determined the system level parameters (besides the resonator gains, since they involve the real circuit issues), we can look little bit closer at how these system level parameters are really implemented. In order to do this, we must first model the resonator building blocks.

The most important building block of the analog part of the converter is the resonator. The resonator circuit is designed to implement the building block given in Figure 3.13.

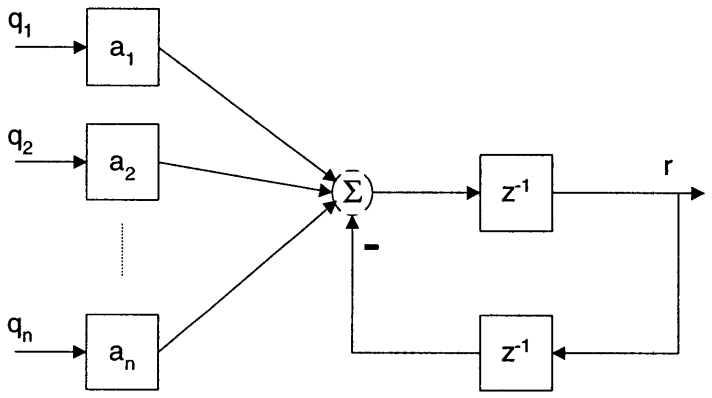


Figure 3.13 Resonator block diagram

In the time domain, the output is

$$r\big((n+1)T_s\big) = -r\big((n-1)T_s\big) + \sum_i a_i \cdot q_i(nT_s),$$

Equation 3-3

where Ts is the sampling period. The output can also be written in the z-transform domain,

$$R(z) = \frac{z^{-1}}{1+z^{-2}} \cdot \sum_i a_i \cdot Q_i(z).$$

Equation 3-4

The remaining building blocks in the analog portion of the converter are quantizers and 1 bit D/A converters. The quantizer acts as a 1-bit A/D converter that maps its analog inputs to one of the two digital output codes. The D/A converters then map these two digital codes back into analog levels, $\pm V_{ref}$. We could combine these two blocks into one represented by function Q(x) defined as

$$Q(x) = \begin{cases} V_{ref} & x \geq 0 \\ -V_{ref} & x < 0 \end{cases}$$

Equation 3-5

By combining four resonators with three quantizers and three 1-bit D/A converters, a 4-2-2 architecture can be modeled as shown in Figure 3.14.

This system produces the identical outputs as the 4-2-2 architecture shown in Figure 3.1, provided that

$$x = \frac{a_{i1}}{a_{f1}} \cdot x_1,$$

Equation 3-6

$$\beta_1 = \frac{a_{f1} \cdot a_{i2} \cdot a_{i3}}{a_{f3}}, \beta_2 = \frac{a_{f3} \cdot a_{i4}}{a_{f4}},$$

Equation 3-7

and

$$\lambda_1 = \frac{a_{u3}}{a_{f1} \cdot a_{i2} \cdot a_{i3}}, \lambda_2 = \frac{a_{u4}}{a_{i4} \cdot a_{f3}}.$$

Equation 3-8

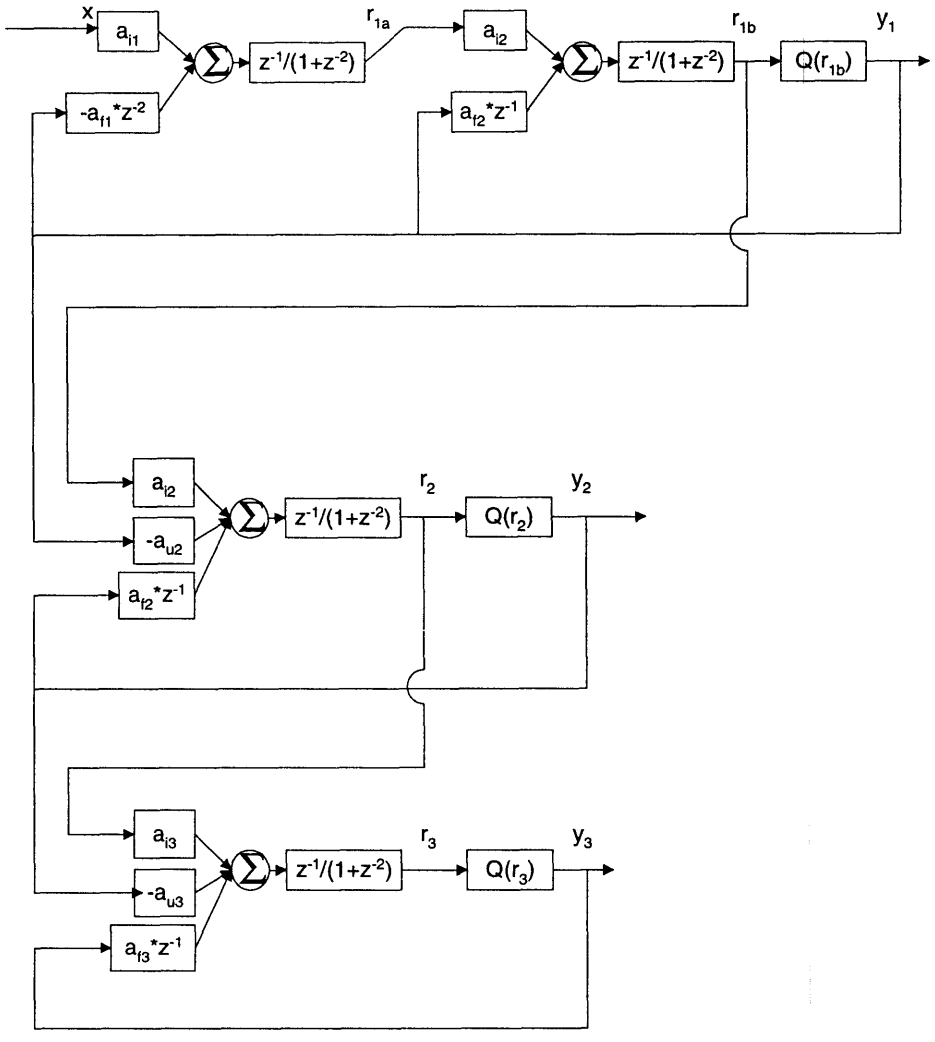


Figure 3.14 Block diagram of 4-2-2 architecture implementation

For our choice of the system parameters, we also have that

$$a_{i1} = a_{f1} = k_{1a},$$

Equation 3-9

$$a_{i2} = k_{1b},\ a_{f2} = 2 \cdot k_{1a} \cdot k_{1b},$$

Equation 3-10

$$a_{i3} = \frac{1}{2} \cdot \frac{k_2}{k_{1a} \cdot k_{1b}},\ a_{u3} = \frac{3}{2} \cdot k_2,\ a_{f3} = k_2,$$

Equation 3-11

and

$$a_{i4} = \frac{k_3}{k_2},\ a_{u4} = a_{f4} = k_3.$$

Equation 3-12

As it will be discussed in Chapter 5, the gains a_{ii}, a_{fi} and a_{ui} will be implemented using capacitors. In the interest of reducing the capacitor mismatch effects on the converter performance, it would be beneficial to implement the subtraction of pairs of inputs q_i in Figure 3.13 using only one capacitor, rather then two. Coupled with the considerations already discussed on choosing the resonator gains k_{1a}, k_{1b}, k_2 and k_3 in Section 3.2.1.1, following set of resonator gains was decided on: k1a=1/2, k1b=2/3, k2=1/3, and k3=1/6. These resonator gain values in turn result in following values for resonator gains of Figure 3.13: $a_{i1}=a_{i2}=1/2$, $a_{i2}=a_{f2}=2/3$, $a_{i3}=a_{u3}=1/2$, $a_{f3}=1/3$, $a_{i4}=1/2$ and $a_{u4}=a_{f4}=1/6$.

3.3 SUMMARY

Based on the brief discussion of considerations involved in wide-bandwidth sigma-delta design, presented in Section 3.1, cascaded 4-2-2 single-bit architecture was decided upon, as illustrated in Figure 3.14, for an oversampling ratio of 16. Behavioral simulations of the chosen architecture were run to determine the system level parameters, since not all of their effects on converters performance are easily captured analytically. Not even behavioral simulations were found useful in determining the resonator gains. Instead, they were chosen upon the considerations discussed at the end of Section 3.2.1.1 and Section 3.2.2. The results are summarized in Table 3-3.

While Figure 3.14 shows the basic form of the implementation of a 4-2-2 architecture, the real analog building blocks do not perform their functions ideally. The next chapter deals with studying the effects of non-idealities in the converter's building blocks in an effort to characterize the building blocks that will best meet the targeted performance of the converter.

PARAMETER	VALUE
ARCHITECTURE	4-2-2
CONVERTER ORDER, L	8
OVERSAMPLING RATIO, M	16
NUMBER OF BITS IN EACH STAGE	N1=N2=N3=1
β_1	½
β_2	1
λ_1	3
λ_2	1
k_{1a}	½
k_{1b}	2/3
k_2	1/3
k_3	1/6
$a_{i1}=a_{f1}$	½
$a_{i2}=a_{f2}$	2/3
$a_{i3}=a_{u3}$	½
a_{f3}	1/3
a_{i4}	½
$a_{u4}=a_{f4}$	1/6

Table 3-3 Summary of system parameters

CHAPTER 4

CONVERTER DESIGN

4.0 INTRODUCTION

Transferring the block diagram of the 4-2-2 architecture in Figure 3.14 to a device level description involves the design of circuits that implement resonators, comparators, digital flip-flops and D/A converters. Real circuits will have deficiencies such as finite speed, thermal noise and finite signal swing, that will limit the performance of the converter in comparison to the ideal case. The first step in designing converter circuits is therefore to identify, properly model and quantify the non-idealities of the building blocks.

Non-idealities to be analyzed, modeled and quantified in this chapter are as listed here.

- resonator non-idealities:

1. intrinsic circuit noise, including thermal noise of the switches, thermal and 1/f input referred op-amp noise.
2. incomplete settling of the resonator
3. finite dc gain of the resonator op-amps
4. non-linearity of the op-amp
5. finite on-resistance of the switches

- comparator non-idealities

6. comparator hysteresis

- D/A converter non-idealities

7. noise on the reference voltages

- sampling clock non-ideality

8. sampling clock jitter.

It should be mentioned that clock skew is another non-ideality that can have an adverse effect on the performance of the converter, by for example making the non-overlapping clocks semi over-lapping. This non-ideality is not modeled here.

The results of studying the effect of non-idealities in the converter building blocks then helped

a) characterize the building blocks

b) determine what circuit topologies would best meet the performance requirements of the converter.

Since the primary emphasis in this discussion is on the limitations in converter's performance imposed by the resonator , we will start the discussion by briefly discussing the choice of the high-pass pseudo two-path resonator and subsequently analyzing its ideal behavior in Section 4.1. Section 4.2 identifies and briefly discusses some of the key non-idealities of the generic resonator. Section 4.3 outlines the design procedure followed in this work. It quantifies the non-idealities introduced in Section 4.2, presenting the noise allocation budget for this design, and it addresses the issues involved in modeling these non-idealities in MIDAS. Section 4.4 presents and discusses the results of the behavioral simulations done in MIDAS, verifying that the noise allocation done in Section 4.3 indeed produces the converter with the desired performance.

4.1 FULLY DIFFERENTIAL PSEUDO TWO-PATH RESONATOR

The block diagram of Figure 3.13, representing fs/4 resonator, can be implemented in several different ways using switched-capacitor techniques. In previous literature, resonators have been implemented using Lossless Discrete Integrators (LDI) [3], Forward-Euler Integrators (FEI) [3], or by using two delay cells in a negative feedback loop, as in [2]. Another approach is to use high-pass pseudo N-path switched-capacitor filters with the out-of-band noise peaks, as described in [44]. The latter design is chosen here for the switched-capacitor implementation for three main reasons. First, the pseudo N-path filter requires only one op amp to implement the desired resonator transfer function, cutting the power dissipation by the factor of two in comparison to all other reported topologies that utilize two op amps to implement the same transfer function. Second, the center frequency of the passband is controlled only by the clock frequency [44], [45], provided op amp open loop DC gain is high enough. Finally, the structure has very low sensitivity to its component's non-idealities, including op amps and capacitors [44], [45].

The basic principle of pseudo-N-path filters have been reviewed by many authors [44], [45], [46]. In summary, pseudo N-path filters can be obtained by the use of the frequency transformations $z->z^N$ or $z->z^{-N}$. For the transformation $z->z^N$, the basic filter is of low-pass type, and is called low-pass N-path filter. For the $z->z^{-N}$ transformation, the basic filter is of high-pass type and is called high-pass N-path filter. High-pass N-path filters have same loss responses as low-pass N-path filters, but shifted by π/NT_s along the frequency axis, since

$$-z^N = e^{j(\omega NT_s+\pi)} = e^{jNT_s(\omega+\pi/NT_s)}.$$

Equation 4-1

Since the sampling theorem requires that the highest signal frequency be lower than the half of the sampling frequency, fs, it follows that the minimum N for low-pass N-path filters is 3. Otherwise, for low-pass pseudo two-path filters, the desired passband will be centered at the fs/2, and the signals in the upper half of the passband will alias in the lower half and vice versa. For high-pass pseudo N-path filters however, the desired passband is centered at fs/4 and the aliasing problem does not exist, allowing N=2 to be the minimum N.

The major problem in the pseudo N-path filters is the noise which appear inside the passbands, namely the clock feedthrough noise and the mirror frequency noise. The unwanted mirror frequency noise mainly results from mismatches between signal paths. Since the op amps are shared by different signal paths, the only source of mismatch will come from the capacitors, but the transfer function of the high pass pseudo N-path filter is to the first approximation independent of it, as long as the op amp gain is sufficiently high, as discussed in [45] and as will be discussed in Section 4.2.1. On the other hand, the mismatches of the switches in the feedback branches of the op amps can result in the clock feedthrough noise peaks at frequencies $k*f_s/N$, where k is an integer [47]. Several feedback branches that deal with this problem have been proposed in the literature [48], [49]. The circulating-delay-type approach [48] can completely eliminate the band-center clock feedthrough noise, since it only has one circulating loop for all charge packets. However, it is very slow, providing the output sample only in every N+1 clock phase, and is relatively sensitive to the finite op amp gain [47]. The hybrid-type approach [49] is both free of the clock feedthrough and faster, providing an output sample in every two clock phases, but the number of op amps needed is doubled to the same number in the approaches reported in [30] and [2], diminishing the number one advantage of the pseudo N-path filters over these approaches. The simplest and the fastest approach is the RAM-type one [47]. It provides an output sample every second clock phase, and is therefore as fast as the hybrid approach. However, since it contains N circulating loops for the charge packets, any asymmetry in the feedback switches of these loops introduces a noise peak at integer multiples of fs/N. If it is used in low-pass pseudo N-path filters, the clock feedthrough noise will appear at the center of the passbands, including the main one located at fs/N. This problem can be avoided in high-pass path filters, since the passbands have been shifted by π/NT_s, making the clock feedthrough peaks out-of-band noise. The only price paid here is that they require fully-balanced differential circuitry, which increases the overall complexity and chip area. Fully differential circuitry, on the other hand, has superior power supply noise rejection, as compared to a single-ended design, and also provides twice the output swing for a given supply voltage. Doubling the signal voltages increases the signal power by a factor of four, while the effective noise power is only doubled because of two independent signal paths, so that the net result is a 3 dB increase in the dynamic range of circuits. In addition, the symmetry of a fully differential circuit provides for cancellation of even-order distortion components, as well as immunity to switch charge injection, substrate noise, supply noise, and

other common-mode disturbances [50]. For these reasons, fully differential switched-capacitor circuits were used throughout this work, irrespective of the choice of the resonator topology.

Figure 4.1 shows the basic structure of the fully differential parasitic-insensitive high-pass pseudo two-path RAM-type filter used in this work and its timing diagram. The input sampling capacitor network is a typical inverting stray-insensitive network. For infinite op amp gain, the voltage transfer function of this resonator satisfies Equation 4-2,

$$\frac{\mathrm{Vout}(z)}{\mathrm{Vin}(z)} = \frac{\frac{C_s}{C_h} \cdot z^{-1}}{1 + z^{-2}}$$

Equation 4-2

provided that the appropriate capacitors are perfectly matched, and assuming that Ch=Ca=Cb.

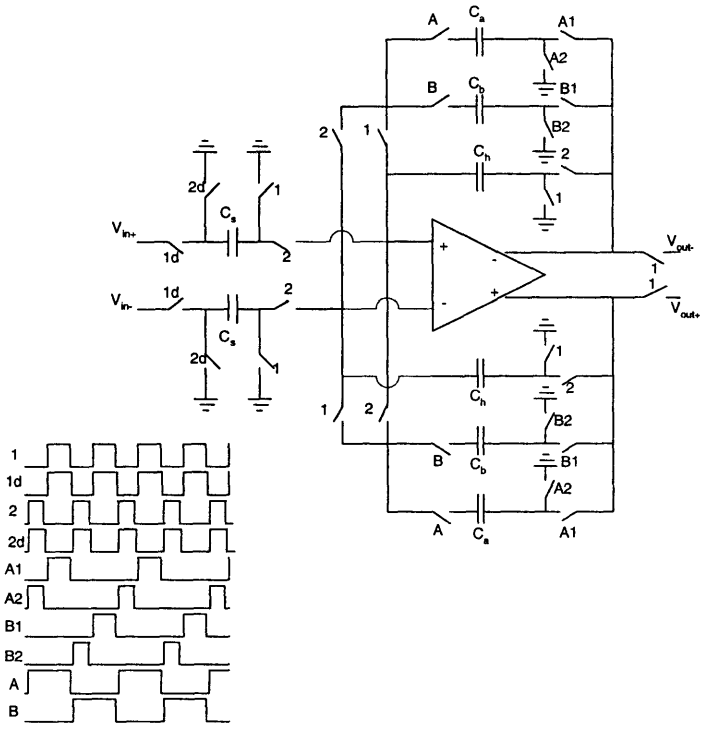


Figure 4.1 Pseudo two-path resonator

The passband centers of this filter are located at (2*k+1) multiples of the path clock frequency fs/4, where k is an integer. From the timing diagram and Figure 4.1 it can be seen that the circuit operation is as follows. During the time when clock phase A2, and hence clock phase 2 is high, the charge from the feedback capacitor C_a representing the path 1 signal, is transferred into the feedback capacitor C_h, where it is augmented by the input charge entered from the sampling capacitor C_s. The situation is illustrated in Figure 4.2. During the next clock phase, when clock phase A1, and therefore also clock phase 1, is high, the updated charge from C_h is transferred back into C_a, as illustrated in Figure 4.3, where it is stored for period of $2T_s$, until clock phase A2 occurs again. If the output voltage is looked at the beginning of the next clock phase, this circuitry implements the transfer function given by Equation 4-2.

The above description covers a full cycle (equal to $2T_s$) of operation for path 1. The route for the path 1 charge is given by C_a -> C_h -> C_a.

Similarly, the path 2 operation starts during the time when the clock phase B2, and hence also the clock phase 2, is high. The charge from the feedback capacitor C_b representing the path 2 signal gets transferred onto the feedback capacitor C_h, where it is augmented by the input charge entered from the sampling capacitor, C_s as shown in Figure 4.4. During the next clock phase, when clock phase B1, as well as clock phase 1, is high, the updated charge is transferred input charge from C_a back onto C_h, as shown in Figure 4.5, where it stays stored for a period of $2T_s$, until phase B2 occurs again. Again, if the output voltage is looked at the beginning of the next clock phase, this circuitry implements the transfer function given by Equation 4-2.

The above description covers a full cycle (equal to $2T_s$) of operation for path 2. The route for the path 2 charge is given by C_b->C_h->C_b.

Note that two feedback capacitors, C_a and C_b, are used so that charge could be stored away for 2 clock cycles, implementing the z^{-2} term. It should also be noted that the behavior of this circuit is time multiplexed, as the name "pseudo two-path resonator" indicates. During the clock phases n and n+1/2, it implements one transfer function utilizing capacitor C_a, while during clock phases n+1 and n+3/2 the same circuitry is used to implement another transfer function, utilizing capacitor C_b. In the absence of non-idealities, these two transfer functions are the same, as given by Equation 4-2. In the presence of non-idealitites, such as capacitor

mismatch, the two transfer functions are not exactly the same anymore. The analysis done in Section 4.2.1, as well as behavioral simulations discussed in Section 4.4 will show, however, that this structure is very insensitive to any non-idealities, as long as the op amp DC gain is sufficiently high.

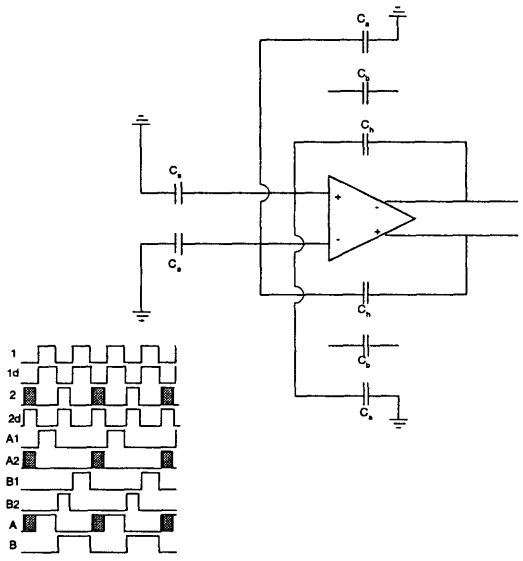


Figure 4.2 Pseudo two-path resonator during A2

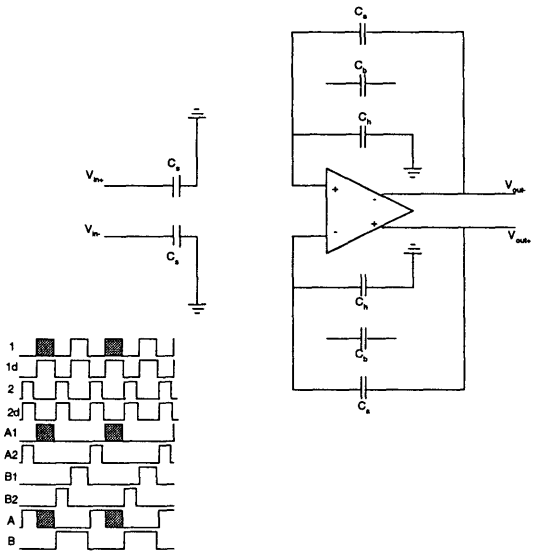


Figure 4.3 Pseudo two-path resonator during A1

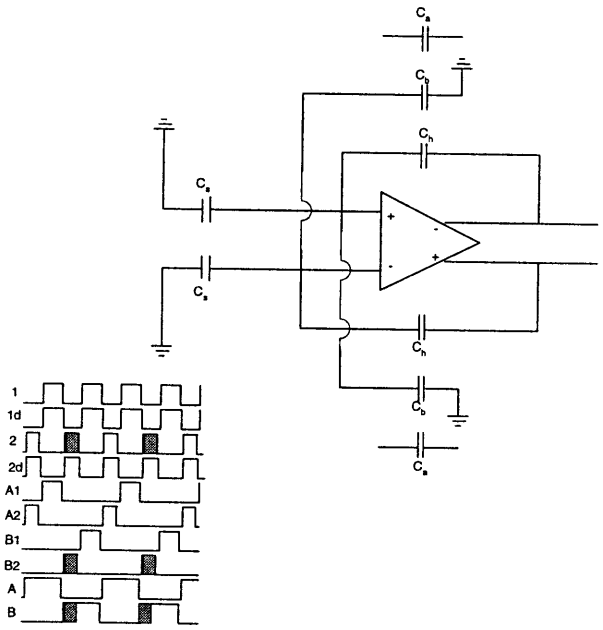


Figure 4.4 Pseudo two-path resonator during A2

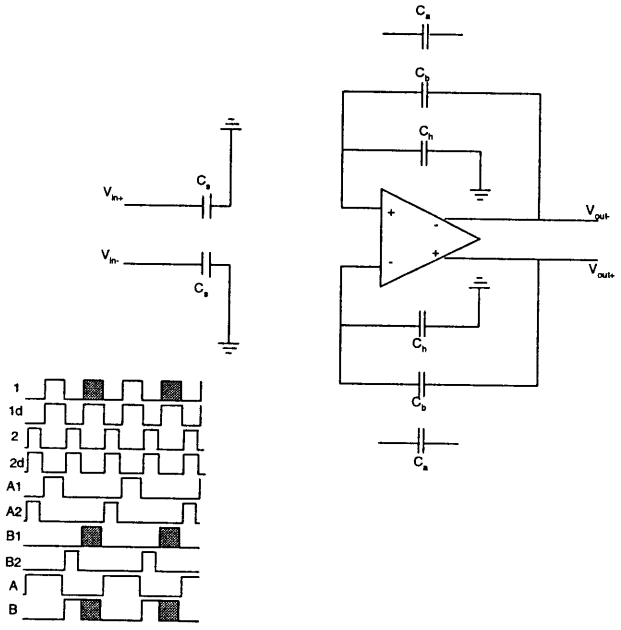


Figure 4.5 Pseudo two-path resonator during B1

4.1.1 AMPLIFIER DESIGN

Having analyzed a fully differential switched-capacitor resonator architecture consisting of MOSFET switches, integrated capacitors, and an amplifier, the next step is to discuss the design of the fully differential op-amp. In the sigma-delta converters and other capacitive load applications, several amplifier architectures have been typically used, including single-stage class A amplifiers, two-class stage A amplifiers, and a single stage class AB amplifiers. Among these, the single-stage class A amplifier has the highest bandwidth, and the single-stage class AB has the best slew rate.

The speed of the amplifier turns out to be of the primary interest in the sigma-delta applications. The SNR of any converter can be increased by increasing the oversampling ratio, making the speed of primary interest. Also, if the op-amp is fast enough to allow circuit to settle completely, the exact nature of settling becomes unimportant, i.e. slewing and voltage-dependent settling will not have any impact on the converter performance, as will be discussed shortly. In a wide-bandwidth systems, the speed becomes the most important and the most difficult thing to design for. Speed of the amplifiers is limited by the available technology and is what ultimately sets the limit on the applicability of the sigma-delta converters. Other criteria for choice of op amp includes reasonable amount of open-loop low-frequency gain and fairly linear open-loop transfer function, so that the distortion of the amplifier will be further reduced when placed in a closed-loop configuration.

The telescopic amplifier becomes the amplifier of choice for this work, since it is the fastest op amp, while its low-frequency open-loop gain is comparable to the gain of a two-stage class A amplifier.

The simplified circuit diagram of the telescopic op-amp, excluding the common-mode feedback and bias circuitry, is shown in Figure 4.6.

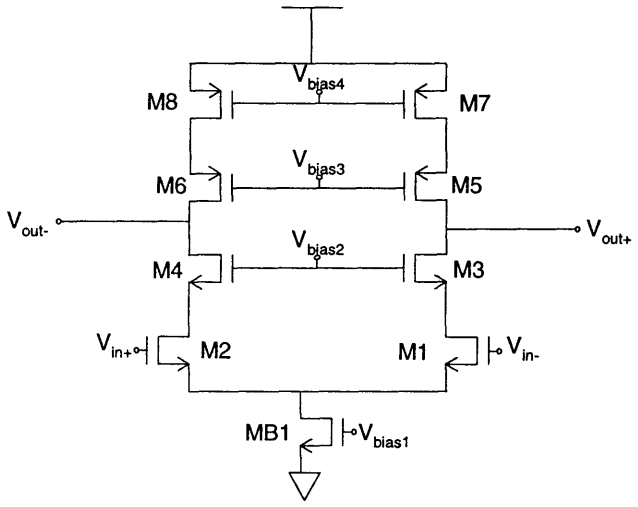


Figure 4.6 Telescopic op amp

The open-loop gain of the op-amp is given by the following expression

$$A_{dc} = g_{m_1} \cdot (g_{m_3} \cdot r_{o_3} \cdot r_{o_1} \| g_{m_5} \cdot r_{o_5} \cdot r_{o_7})$$

Equation 4-3

where g_{mi}, g_{oi}, r_{oi} are the transconductance, output conductance, and output resistance, respectively, of the transistor M_i. It is comparable to the open-loop gain of the folded-cascode amplifier and the basic two-stage class A amplifier.

The slew rate of the telescopic amplifier will be limited by the current available at the output, to drive the total capacitance loading the output node when the op amp is in the non-linear mode of operation (slewing), $C_{TL_{slew}}$. The maximum slew rate, ζ, will then be

$$\zeta = \frac{I_{D1}}{C_{TL_{slew}}},$$

Equation 4-4

where I_{D1} is the quiescent drain current of M1.

The op amp transfer function, A(s), can be modeled as

$$A(s) = \frac{\omega_{UG}}{(s+\omega_{-3dB})(s+\omega_{2nd})},$$

Equation 4-5

where the ω_{UG} is the unity gain frequency, ω_{-3dB} is the dominant pole frequency, and ω_{2nd} is the non-dominant pole frequency of the op amp.

The unity gain frequency of the telescopic amplifier, ω_{UG}, is given by

$$\omega_{UG} = \frac{2 \cdot \pi}{\tau_{UG}} = \frac{2 \cdot \pi \cdot g_{m_1}}{C_{TL_{settle}}},$$

Equation 4-6

where $C_{TL_{settle}}$ is the total load capacitance seen by the op amp when in linear mode of operation (settling).

The dominant pole frequency, ω_{-3dB}, is given by

$$\omega_{-3dB} = \frac{2 \cdot \pi}{\tau_A} = \frac{\omega_{UG}}{A_{DC}},$$

Equation 4-7

where τ_A is the open-loop time constant, and A_{DC} is the DC open-loop gain of the telescopic amplifier.

The strength of the telescopic amplifier is a high maximum non-dominant pole frequency. The non-dominant pole frequency, ω_{2nd}, is determined by g_{m3} and the parasitic capacitance at the source of M3, C_x, as given by

$$\omega_{nd} = \frac{g_{m_9}}{C_x}.$$

Equation 4-8

Compared with the folded-cascode amplifier, the non-dominant pole is at a considerably higher frequency because g_{m3} is relatively high, since M3 is NMOS, and the parasitic capacitance, C_x, is lower, since only two transistors are connected at the source of M3. This non-dominant pole can be near the unity gain frequency of M3, which is close to the upper limit of the speed of the technology.

The white noise coefficient of the input-referred noise voltage is

$$\zeta_{o_a} = 2 \cdot 4 \cdot \gamma \cdot k \cdot T \cdot \frac{1}{g_{m_1}} \cdot (1 + \frac{g_{m_3}}{g_{m_1}} + \frac{g_{m_7}}{g_{m_1}}),$$

Equation 4-9

where γ varies value of 1 at a zero drain-to-source voltage to a value of approximately 2/3 in saturation, and the factor of 2 is present since we have 2 devices in the differential pair.

Typically,

$$1 + \frac{g_{m_3}}{g_{m_1}} + \frac{g_{m_7}}{g_{m_1}} \approx 2 \text{ and } \gamma \approx \frac{2}{3},$$

Equation 4-10

so that Equation 4-9 becomes

$$\zeta_{o_a} = \frac{8 \cdot k \cdot T}{g_{m_1}}.$$

Equation 4-11

The noise is approximately bandlimited by single pole whose time constant is not the open-loop op amp time constant τ_A, but the closed-loop resonator time constant, τ.

In the resonator, the telescopic op amp is connected in one of the two negative feedback configurations illustrated in Figure 4.7, where Figure 4.7 (a) illustrates the situation during clock phase 1, while the situation during clock phase 2 is shown in Figure 4.7 (b). These negative feedback configurations can be modeled by block diagram illustrated in Figure 4.8.

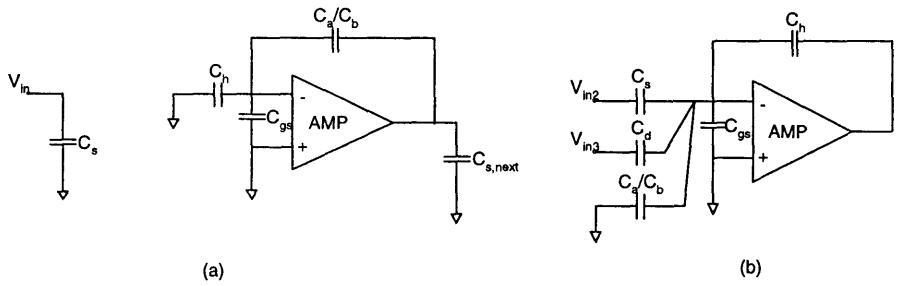


Figure 4.7 A single-ended equivalent circuit of resonator during (a) clock phase 1 and (b) clock phase 2

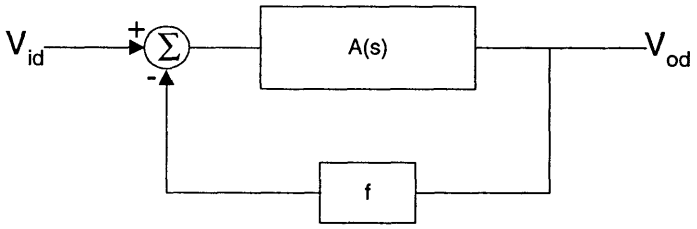


Figure 4.8 Model of op amp in the closed-loop configuration

Under the dominant pole approximation, we can model op amp transfer function, A(s) as

$$A(s) = \frac{\omega_{UG}}{s + \omega_{-3dB}},$$

Equation 4-12

where ω_{UG} and ω_{-3dB} are given by Equation 4-6 and Equation 4-7, respectively. The closed-loop resonator transfer function becomes

$$\frac{V_{od}}{V_{id}}(s) = \frac{A(s)}{1 + A(s) \cdot f} \approx \frac{\omega_{UG}}{s + f \cdot \omega_{UG}},$$

Equation 4-13

where f is the feedback factor and is given by

$$f_1 = \frac{C_{a,b}}{C_{a,b} + C_h + C_{gs_1}},$$

Equation 4-14

during clock phase 1, and by

$$f_2 = \frac{C_h}{C_h + C_s + C_d + C_{a,b} + C_{gs_1}}$$

Equation 4-15

during clock phase 2. The closed-loop time constant of the resonator, τ, is given by

$$\tau = \frac{\tau_{UG}}{f}.$$

Equation 4-16

Notice that the closed loop time constant depends on feedback factor, f, the amplifier transconductance, g_{m1}, and the total load capacitance seen by the amplifier while settling, $C_{TL_{settle}}$. The total capacitance seen by the amplifier depends on the mode the amplifier is operating at and the feedback configuration amplifier is in. The total load capacitance seen by the amplifier while settling during clock phase 1 is given by

$$C_{TL_{settle_1}} = (C_{s,next} + C_p) \cdot (1 + \frac{C_h + C_{gs_1}}{C_h}) + C_h + C_{gs_1},$$

Equation 4-17

and during clock phase 2 by

$$C_{TL_{settle_2}} = C_p \cdot (1 + \frac{C_s + C_d + C_{a,b} + C_{gs_1}}{C_h}) + C_s + C_d + C_{a,b} + C_{gs_1},$$

Equation 4-18

where C_p is the parasitic capacitance at the output of the op amp, Cgs1 is the gate-to-source capacitance of the input devices (it is assumed that this is the dominant capacitance at the input of the op amp), and $C_{s,next}$ is the sampling capacitor of the next resonator. The total load capacitance seen by the op amp when it is slewing is, during clock phase 1, given by

$$C_{TL_{slew_1}} = C_{s,next} + C_p + \frac{(C_h + C_{gs_1}) \cdot C_{a,b}}{C_h + C_{gs_1} + C_{a,b}},$$

Equation 4-19

and during clock phase 2 by

$$C_{TL_{slew_2}} = C_p + \frac{(C_s + C_d + C_{a,b} + C_{gs_1}) \cdot C_h}{C_s + C_d + C_{a,b} + C_{gs_1} + C_h}.$$

Equation 4-20

4.2 CIRCUIT NON-IDEALITIES

The ideal behavior of most important converter components was analyzed in previous section. A fully differential, switched-capacitor, parasitic-insensitive, pseudo two-path resonator was presented in Section 4.1, and Section 4.1.1 discussed a telescopic op-amp used in the resonator. In this section, relevant non-idealities of the converter circuits are identified and their effects on the performance of the converter analyzed. The implications of using non-ideal components for this design are quantified in the next section, detailing the allocation of the noise budget for each relevant non-ideality.

4.2.1 THE RESONATOR CIRCUIT NON-IDEALITITES

The relevant non-idealities, non-linearities and the intrinsic noise of the resonator are identified in three separate subsections, discussing briefly their effects on the resonator performance.

4.2.1.1 EFFECTS OF COMPONENT NON-IDEALITIES ON THE RESONATOR PERFORMANCE

The resonator transfer function will differ from the ideal because of the finite op-amp DC gain, finite op-amp bandwidth and nonzero switch resistance. For example, the finite DC op-amp gain will change the ideal transfer function given by Equation 4-2 to:

$$\text{for } t = (2\cdot n)\cdot\frac{T_s}{2}$$

$$V_{out_i}(z) = \frac{z^{-1}\cdot g\left(\sum_{j=1}^{n} a_{ij}\cdot x_{ji}(z)\right)}{1+\mu\cdot\left(1+\frac{1}{b_{b_i}}+a_{i1}\right)+\mu\cdot\frac{b_{a_i}+\mu\cdot(1+b_{a_i})}{1+\mu\cdot(1+b_{a_i})}\cdot z^{-1}+(1+\mu)\cdot\frac{1+\mu\cdot\left(1+\frac{1}{b_{b_i}}\right)}{1+\mu\cdot(1+b_{b_i})}\cdot z^{-2}}$$

$$\text{for } t = (2\cdot n+1)\cdot\frac{T_s}{2}$$

$$V_{out_i}(z) = \frac{z^{-1}\cdot g\left(\sum_{j=1}^{n} a_{ij}\cdot x_{ji}(z)\right)}{1+\mu\cdot\left(1+\frac{1}{b_{a_i}}+a_{i1}\right)+\mu\cdot\frac{b_{b_i}+\mu\cdot(1+b_{b_i})}{1+\mu\cdot(1+b_{b_i})}\cdot z^{-1}+(1+\mu)\cdot\frac{1+\mu\cdot\left(1+\frac{1}{b_{a_i}}\right)}{1+\mu\cdot(1+b_{a_i})}\cdot z^{-2}}$$

Equation 4-21

where $a_{i1} = a_{i2} = \frac{C_{s_i}}{C_{h_i}}$, $a_{i3} = \frac{C_{d_i}}{C_{h_i}}$, $b_{a_i} = \frac{C_{h_i}}{C_{a_i}}$, $b_{b_i} = \frac{C_{h_i}}{C_{b_i}}$ and $\mu = \frac{1}{A_{DC}}$ for i=1, 2, 3 and 4.

Similarly, we could derive the separate transfer function incorporating the effects of the finite op-amp bandwidth and the nonzero resistance of switches. These non-idealities will then also interact with each other.

The analysis indicates that these non-idealities affect the resonator performance in two ways, by introducing the gain error and by causing the pole error. The gain error affects the depth of the notch in the quantization noise transfer function (NTF), while the pole error affects the center frequency of the bandpass converter and the location of the zeros in the quantization noise transfer function. Total in-band quantization noise is much less sensitive to depth of notch compared with location of zeros, making the converter with minimal pole error particularly attractive for this application.

The gain error is the relative error in the value of the resonator gains. In the pseudo two-path resonator, it is caused by the capacitor mismatch and finite op-amp dc gain, as indicated in Equation 4-21, as well as by the incomplete resonator linear settling, caused either by nonzero switch resistance or finite op-amp bandwidth. Resonator pole error in pseudo two-path resonator is caused only be the finite DC op-amp gain, since it is only in the presence of the finite DC op-amp gain that the capacitor mismatch affects the location of NTF zeros. This is a very important feature when performing IF A/D conversion, since it means that the center frequency of the bandpass converter and the location of the zeros in the quantization noise transfer function are independent of the settling error and, to the first order, insensitive to the capacitor mismatch. This fact makes this resonator particularly attractive for the application in hand. One drawback in using the pseudo-two path resonator for this application is the fact that the resonator transfer function is implemented using two different capacitors for the two paths, resulting in the I/Q path mismatch in the presence of the capacitor mismatch. This drawback can easily be minimized by allowing the resonator amplifiers to have sufficiently high DC gains.

The next non-ideality we will discuss in this section is the resonator incomplete settling. Let us first remind ourselves that switched-capacitor circuits operate under the assumption that complete settling occurs during each time slot and therefore, unless the signal is used as a

continuos-time signal, the manner in which the circuit settles is unimportant. The only time the value of the voltages in the resonator outputs matters is at the end of each time slot. The only place where the continuos-time properties of the signal are important is at the input sampler.

Ideally, the input of a resonator gets completely integrated on the integrating capacitor during each time slot. In the clocking scheme shown in Figure 4.1, the length of the time slot is equal to one-half a clock period minus the delays put in for delayed clock phases, non-overlap time and charge injection reduction purposes, i.e.

$$T_{sett} = \frac{T_s}{2} - 4\text{ns} \approx 8.7\text{ns}.$$

Equation 4-22

In reality this never happens due to incomplete settling of the resonator. There are basically two factors that determine the settling time of the resonator, the RC time constant of the MOSFET input switches in series with the switched-capacitors, and the response time of the amplifiers. The response time of the operational amplifier is determined by the configuration in which it is placed, the slew rate and the unity-gain bandwidth.

The settling characteristics can be signal independent (linear settling) or signal dependent (non-linear settling). If the resonator does not settle fully but the settling process is linear, then the resultant error shows up as a gain error in the resonator (to be discussed in more detail briefly). A linear settling error has very little effect on the performance of the single-loop converter, and a linear settling to within 0.1% is more than adequate for most cascaded converters. A non-linear settling error, on the other hand, degrades the performance of both single-loop and cascaded converters. Non-linear settling may be due to the op-amp slewing, or the fact that the characteristics of the MOSFET devices will be operating point dependent. If the input capacitor does not charge completely and the degree of charging is signal dependent, the effect will be the same as if the capacitor was non-linear. The error due to nonlinear settling will show up as harmonic distortion and is independent of the oversampling ratio. Therefore, the non-linear settling is by far the more serious problem.

There are two ways to eliminate the effects of non-linear settling. The first is to design the resonator in a way that it never settles non-linearly. This may not always be possible, and the most straightforward solution for eliminating the effects of non-linear settling is then to make sure that the circuit settles completely enough so that the dynamic range requirements are satisfied no matter what the signal dependence may be. For example, if the circuit settles within 0.078% of final value, then a 62 dB dynamic range is guaranteed regardless of the nature of the settling.

Settling problems due to the RC time constants of the MOSFET input switches can be solved simply by decreasing the effective resistance by increasing the width of the switch. Care must be taken to ensure that the switches are not too big, since if the switch becomes comparable to the input capacitor, the effects due to channel charge injection and the parasitic junction capacitances will increase [8], degrading the performance.

The settling of the op-amp is a more involved problem to solve. As already pointed out, the settling of the op-amp depends on three factors: slew rate, the unity-gain bandwidth, and the gain configuration. The slew rate of the telescopic amplifier discussed in Section 4.1.1 is determined by the ratio of the current available at the output of the amplifier and the total load capacitance seen by the amplifier. The maximum slew rate is therefore limited by the bias current of the amplifier and the total load capacitance seen by the amplifier when in slewing mode of operation, as given by Equation 4-4. Since the capacitor sizes are ultimately set by the noise budget allocation considerations, such as maximum allowable kT/C noise and maximum allowable noise due to the capacitor mismatch, the slew rate can be increased only by increasing the bias current of the amplifier. There again is a limit, as dictated by a power budget allocation considerations. Unity gain bandwidth can be improved by increasing the gm of the input devices as given in the Equation 4-6, which is equivalent to increasing the bias current of the amplifier again, or increasing the width of the input devices. Increasing the width of the input devices also increases their Cgs, which has an adverse effect on unity gain frequency in two ways, by increasing the total load capacitance seen by the amplifier, and by reducing the feedback factor of the resonator, making the resonator overall response slower. To resolve this trade-off, spreadsheets were used to arrive at the optimal widths of the input transistors. Finally, it is also important to know the configuration in which the op-amp will be functioning in order to determine the feedback factor of the closed-loop resonator configuration, and

consequently the settling time constant of the overall resonator circuit. The feedback factor is inversely proportional to the resonator gains, as illustrated in Equation 4-14 and Equation 4-15, and the resonator closed-loop settling time constant is inversely proportional to the feedback factor, as given by Equation 4-16. It therefore follows that for the fastest settling op-amp the resonator gains should be made as small as possible, contrary to the requirement to make the resonator gains as large as possible in order to reduce the effects of the noise sources following the first resonator on the converters performance, illustrating another trade-off involved in the design process.

We noted that the finite on-resistance of the input switches can adversely affect the settling time of the resonator and consequently result in the gain error, but haven't yet discussed the effects that the finite on-resistance of the remaining switches can have on the resonator performance. High on-resistance of the feedback switches, for example, can make the closed-loop system poorly damped or unstable. In order to avoid this type of situation, low enough on-resistance of the switches is required, but using a too large of the switch can add significant amount of parasitic capacitance at the output reducing the overall bandwidth. The simulations should be performed to establish the best design compromise. Finally, the summing node switches can inject charge into the Cgs of the op amp input devices, changing the input common mode voltage by $\Delta Q/Cgs$. Since the op amp used in this design is telescopic op amp which has limited input common mode range, care must be taken to size the summing node switches such that this change in common-mode voltage does not change the bias condition of the input devices.

The final non-ideality we will consider in this section is the limited output swing of the resonator determined by the output range of the operational amplifier. When the resonator output exceeds this output range of the op-amp, the resonator will saturate and become very non-linear. As the output of the resonator approaches the upper or the lower bound of the op-amp output swing, it eventually clips, or hard-limits. In clip, the output of the resonator remains fixed, and the op-amp no longer has an effect on the circuit. The summing junction is no longer a virtual ground, but has a value determined by the input signal and by the passive RC equivalent formed by the switched input capacitor and the integrating capacitor.

Usually, the values of both the integrating capacitors and the input capacitor are scaled such that that the resonator outputs just saturate at the maximum allowed value of the input signal. Simulations are then performed to verify that the system operates to specifications with this scaling.

4.2.1.2 EFFECTS OF COMPONENT NON-LINEARITIES ON THE RESONATOR PERFORMANCE

The resonator non-linearity is caused by some non-ideal effects of the resonator components and can cause harmonic distortion that limits the SNR at large signal levels. Some of the non-ideal effects such as the signal dependent settling of the op-amp and the non-linear resistance of the MOSFET switches will only cause non-linearities if the settling is incomplete. Some of the non-ideal effects, such as the errors due to signal-dependent switch charge injection, voltage-dependent capacitors, or a non-linear op-amp DC transfer function will occur even if the settling time was infinite [8]. Signal-dependent switch-charge injection and incomplete linear settling due to the nonzero switch resistance have the same effect on a resonator performance as a non-linear switched capacitor, while non-linearities due to incomplete op-amp settling have a similar effect to a non-linear op-amp DC transfer function, but are more complex. For simplicity, only the effects of the non-linear capacitors and a non-linear op-amp DC transfer function will be considered here.

The charge-voltage relationship for the non-linear capacitor is given by

$$q = C_1 \cdot V + C_2 \cdot V^2 + C_3 \cdot V^3 + \ldots..$$

Equation 4-23

The non-linear transfer function of an amplifier is

$$V_o(t) = \alpha_o + \alpha_1 \cdot V_i(t) + \alpha_2 \cdot V_i^2(t) + \alpha_3 \cdot V_i^3(t) + \ldots.$$

Equation 4-24

where $\alpha_0 = V_{os}$ and $\alpha_1 = A_{DC}$.

One of the advantages in using fully differential circuits for high-performance switched-capacitors circuits is that all even-order distortion terms, regardless of the cause of the distortion, will be canceled. If we further assume that the power of harmonics decreases with increasing order, we can reduce the distortion analysis to considering only the third-order non-linear term.

The effect that a non-linear capacitor or non-linear op-amp have on the overall converter's performance depends on the placement within the converter. Because of the noise shaping, the non-linear effects are most important at the input. Let's assume that there are two capacitors at the input, the sampling capacitor and the D/A feedback capacitor. If a 1-bit D/A converter is used, the feedback capacitor is charged to only two distinct levels, so that the feedback becomes inherently linear and any non-linearity in the switched input capacitor does not cause any distortion at the output of the converter. A non-linearity in the input sampling capacitor will cause harmonic distortion in the output of the converter. For sinusoid input, the third order distortion factor will be

$$HD_{3_{cap}} = \frac{1}{4} \cdot \frac{C_3}{C_1} \cdot V_{iA}^2$$

Equation 4-25

where V_{iA} is the amplitude of he sinusoidal input signal.

The third harmonic distortion factor for the op-amp due to sinusoidal input signal is

$$HD_{3_{op-amp}} = \frac{1}{4} \cdot \frac{\alpha_3}{A_{DC}} \cdot V_{iA}^2 .$$

Equation 4-26

The third order harmonic distortion factor will be reduced by the feedback loop in which the amplifier is placed, but for the worst case analysis, we will use this open-loop distortion formula. It is useful to note here that increasing the open-loop DC gain of the amplifier will help reduce the distortion due to the amplifier.

The total harmonic distortion of the i-th resonator, THD_i, is then the sum of the harmonic distortions of the input sampling capacitor and of the amplifiers,

$$THD_i \approx HD3_{cap_i} + HD3_{opa-mp_i} .$$

Equation 4-27

The first resonator is the main source of nonlinearity because its harmonic distortion adds directly to the input signal. This requires the linearity of the first amplifier, at the maximum input level, i.e., jammer, to be the as good as the overall accuracy of the modulator. For example, our converter with 63 dB SNRmax would in this case require the first amplifier to have lower than 0.078% THD at the maximum input level.

In comparison to the harmonic distortion of the first resonator, the harmonic distortion of the following resonators is attenuated by the gain product of the resonator(s) before that resonator. Namely the harmonic distortion of the second resonator is attenuated by the gain of the first resonator. Similarly, the harmonic distortion of the third resonator is attenuated by the combined gain of the first and the second resonator, and the harmonic distortion of the fourth resonator is attenuated by the combined gain of the first, the second and the third resonator. The gain of the resonator is inversely proportional to the frequency, the harmonics above the signal bandwidth are suppressed by the decimation filter, and the harmonics of any subsequent resonator are minimally attenuated at $f = f_{worst} = \frac{f_s}{4} + \frac{f_B}{2}$, where

$$\left|H_i(f = f_{worst})\right| = a_{i_i} \cdot \frac{M}{\pi}$$

Equation 4-28

for i=1, 2, 3 and 4. Consequently, the linearity requirement for any subsequent resonator is relaxed for exactly this gain factor in comparison to the previous resonator.

The total harmonic distortion then becomes

$$THD = THD_1 + \frac{\pi}{a_{i1} \cdot M} \cdot THD_2 + \frac{\pi^2}{a_{i1} \cdot a_{i2} \cdot M^2} \cdot THD_3 + \frac{\pi^3}{a_{i1} \cdot a_{i2} \cdot a_{i3} \cdot M^3} \cdot THD_4 .$$

Equation 4-29

4.2.1.3 THE INTRINSIC RESONATOR CIRCUIT NOISE

The intrinsic resonator circuit noise is the noise generated in the devices that comprise the resonator. It is one of the intrinsic properties of the devices, as opposed to noise from some external source, and as such cannot be eliminated by the usual techniques such as filtering or the circuit layout. Its value however can be altered by the choice of circuit topology and component size. In this section, the two most important noise mechanisms in MOS devices, thermal noise and flicker, or 1/f noise, will be discussed.

Thermal noise is caused by the random fluctuation of the carriers due to thermal energy and is present even at equilibrium, e.g. even in a turned-on MOSFET with a zero current flow. Because of this, it needs to be taken into account for both switches and the op-amps in the resonator. Flicker noise is attributed to the variation in channel charge being captured and released by traps with a distribution of time constants. Since 1/f noise is caused by a fluctuation in the number of carriers in the channel, a device with no current flowing through it cannot have 1/f noise. This implies that switches that are fully "on", or fully "off" at the time of the sampling contribute no 1/f noise. Therefore, in a switched-capacitor resonator, 1/f noise is a concern only in the op-amps.

The section 4.2.1.4 discusses the thermal noise of the switches, while section 4.2.1.5 discusses both the thermal and the 1/f noise of the op-amps.

4.2.1.4 THE THERMAL NOISE OF THE SWITCHES

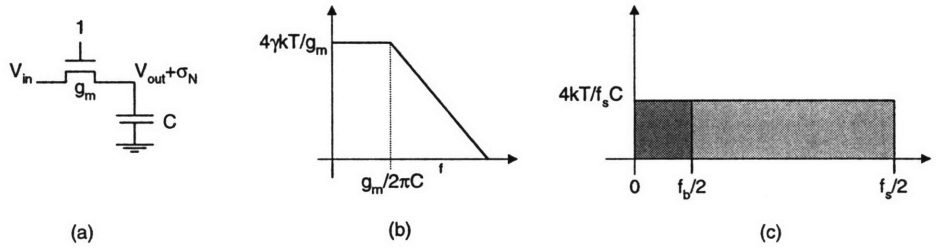


Figure 4.9 Switched capacitor noise subcircuit used to analyze $\frac{kT}{C}$ noise

The switched capacitor track and hold subcircuit shown in Figure 4.9 (a) is one of the main noise generators in a sampled-data analog MOS circuits. The MOS transistor is alternately switched between a high and low impedance state. In the low impedance state, the resistance of the switch generates noise. At the end of the low impedance portion of the cycle, the input and the switch noise are sampled onto the capacitor. The spectral density of the noise voltage sampled across the capacitor, $\zeta(f)$, can be written as

$$\zeta(f) = \frac{\zeta_o}{1+(2\cdot\pi\cdot\tau\cdot f)^2}.$$

Equation 4-30

ζ_o is a white noise coefficient given by

$$\zeta_o = 4\cdot k\cdot T\cdot\frac{1}{g_m},$$

Equation 4-31

where g_m is the transconductance of the switch transistor in the saturation and τ is the bandlimiting time constant of the circuit given by

$$\tau = \frac{C}{g_m}$$

Equation 4-32

This is illustrated in Figure 4.9 (b). Note that when the noise is sampled by a sigma-delta modulator, any noise components appearing at frequencies greater than half the converter's sampling frequency will be aliased or folded into the modulator sampling bandwidth. This is true for any noise, not only the thermal noise of the switches. The total noise power in the output signal's band, S_{tot}, is equal to the sum of the noise found within the signal-band-width windows centered about multiples of the sampling frequency. Expressed mathematically,

$$S_{tot} = \sigma_{tot}^2 = \sum_{n=-\infty}^{\infty} \int_{\frac{f_s}{4}-\frac{f_B}{2}}^{\frac{f_s}{4}+\frac{f_B}{2}} (\zeta|f - n \cdot f_s|) \cdot df .$$

Equation 4-33

Under the assumption that all the noise but the noise in the signal band has been filtered out as described in Chapter 1, this expression than reduces to

$$S_{tot} = \sigma_{tot}^2 = \int_{\frac{f_s}{4}-\frac{f_B}{2}}^{\frac{f_s}{4}+\frac{f_B}{2}} \zeta(f) \cdot df$$

Equation 4-34

This assumption will be used throughout this chapter, so that the noise we discuss here just means in-the-signal-band noise. Assuming that the bandwidth of the converter is sufficiently greater than the sampling frequency, we have that the total thermal noise power in the signal bandwidth, S_{tot}, is then given by

$$S_{tot} = \sigma_{tot}^2 = \frac{\zeta_o}{4 \cdot \tau} = \frac{k \cdot T}{C}.$$

Equation 4-35

It is interesting to note that while the thermal noise is generated in the resistor, the total noise power depends only on the capacitor. Once the output of the converter is digitally mixed down to baseband, all the noise is aliased down to the band from 0 to fs/2, and the final spectrum is white with the spectral density

$$S_{tot} = \sigma_{tot}^2 = \frac{2 \cdot k \cdot T}{f_s \cdot C}.$$

Equation 4-36

Since there are two samplings of thermal noise per clock period, the spectral density becomes

$$S_{tot} = \sigma_{tot}^2 = \frac{4 \cdot k \cdot T}{f_s \cdot C}.$$

Equation 4-37

This noise is then passed through a digital low-pass decimation filter, with the cut-off frequency of $f_c = \frac{f_B}{2}$. Since the thermal noise power is assumed to be white, the total power is reduced by the oversampling ratio M in the decimation process, as shown in Figure 4.9 (c), so that

$$S_{thermal} = \sigma_{thermal}^2 = \frac{k \cdot T}{M \cdot C}.$$

Equation 4-38

Note that the in-band thermal switch noise will decrease by 3 dB per octave of oversampling. Using the fully differential circuitry, an additional 3 dB improvement in the signal-to-thermal

noise ratio will be realized. This is due to the fact that the number of switches doubles, and since the noise is uncorrelated, the thermal switch noise power doubles, i.e.

$$S_{switch} = \sigma^2_{switch} = \frac{2 \cdot k \cdot T}{M \cdot C}.$$

Equation 4-39

A fully differential circuit also doubles the signal swing, which represents an increase in signal power of 6 dB. Hence, the fully differential circuitry increases the signal-to-switch noise ratio for 3 dB over the single-ended circuitry.

Now that we have the expression for the switch noise, we can derive the total switch noise for each of our four pseudo two-path resonators. In the following calculations, the switch noise will be estimated by assuming kT/MC contribution from each independent switch path. As we already noted, the switch noise will be doubled due to differential architecture used. Also, since all of the capacitors in the resonators use the two-phase switches, the noise sampled on capacitors in one clock cycle is effectively doubled again. Looking at the Figure 4.1 we see that total switch noise seen at the input of each resonator is:

$$\sigma^2_{switches-i} = 2 \cdot \left[\frac{2 \cdot k \cdot T}{M \cdot C_{s_i}} + \frac{2 \cdot k \cdot T}{M \cdot C_{s_{Di}}} + \frac{2 \cdot k \cdot T}{M \cdot C_{h_i}} + 2 \cdot \max\left[\frac{k \cdot T}{M \cdot C_{a_i}}; \frac{k \cdot T}{M \cdot C_{b_i}} \right] \right]$$

Equation 4-40

for i=1, 2, 3 and 4.

From the values of resonator gains given in Table 3-3 we know that

$$C_{s_1} = \frac{C_{h_1}}{2},\ C_{d_1} = 0 \text{ and } C_{h_1} = C_{a_1} = C_{b_1},$$

Equation 4-41

$$C_{s_2} = \frac{2}{3} \cdot C_{h_2},\ C_{d_2} = 0 \text{ and } C_{h_2} = C_{a_2} = C_{b_2},$$

Equation 4-42

$$C_{s_3} = \frac{C_{h_3}}{2},\ C_{d_3} = \frac{C_{h_3}}{3} \text{ and } C_{h_3} = C_{a_3} = C_{b_3},$$

Equation 4-43

and

$$C_{s_4} = \frac{C_{h_4}}{2},\ C_{d_4} = \frac{C_{h_4}}{6} \text{ and } C_{h_4} = C_{a_4} = C_{b_4},$$

Equation 4-44

so that the expressions for the switch noise of the first, second, third and fourth resonator become

$$\sigma^2_{\text{switches}_1} = \frac{8 \cdot k \cdot T}{M \cdot C_{s_1}},\ \sigma^2_{\text{switches}_2} = \frac{\frac{28}{3} \cdot k \cdot T}{M \cdot C_{s_2}},\ \sigma^2_{\text{switches}_3} = \frac{14 \cdot k \cdot T}{M \cdot C_{s_3}} \text{ and } \sigma^2_{\text{switches}_4} = \frac{16 \cdot k \cdot T}{M \cdot C_{s_4}}, \text{ respectively.}$$

It should be mentioned that, traditionally, 1/f noise of the switches is omitted and that the empirical evidence supports this omission, so that the same will be done here.

4.2.1.5 THE INPUT REFERRED NOISE OF THE OP-AMPS

The input referred noise of the op-amps has two components as already mentioned, one being the white noise and another being flicker, or 1/f noise. The total input-referred noise is, similarly to the switch noise, limited by the overall bandwidth of the circuit and can be expressed as

$$\zeta_a(f) = \frac{\zeta_{o_a} + \frac{K}{f}}{1 + (2 \cdot \pi \cdot \tau \cdot f)^2},$$

Equation 4-45

where ζ_{o_a} is the white noise density, K is the 1/f noise coefficient, and τ is the closed-loop resonator time constant of the single-pole band limit, given in Equation 4-15. The total in-band input-referred noise power is then calculated to be

$$S_a = \frac{\zeta_{o_a}}{4 \cdot M \cdot \tau} + K \cdot \ln \frac{\frac{f_s}{4} + \frac{f_B}{2}}{\frac{f_s}{4} - \frac{f_B}{2}}.$$

Equation 4-46

The white and 1/f noise coefficients of the input referred noise of the op-amps can be calculated only for a particular op-amp topology by input referring the noise of the individual transistors. The short analysis of the telescopic op amp topology decided on for this work is given in Section 4.1.1. The expression for the op-amp thermal noise coefficient is given in Equation 4-11, so that the expression for the total op-amp thermal noise becomes

$$S_{thermal} = \frac{2 \cdot k \cdot T}{M \cdot g_{m_1} \cdot \tau}.$$

Equation 4-47

Looking at Equation 4-15 and Equation 4-3, this expression reduces to

$$S_{thermal} = f \cdot \frac{2 \cdot k \cdot T}{M \cdot C_{TL_{settle}}}.$$

Equation 4-48

where $C_{TL_{settle}}$ is as given in Equation 4-18 and Equation 4-19, and f is as given in Equation 4-14 and Equation 4-15, for clock phases 1 and 2, respectively. It is interesting to note that the thermal noise depends only on the capacitances.

Experimental observations of various MOS transistors indicate that input-referred voltage in an MOS device has a 1/f power spectrum factor K_{MOS} that is roughly equal to

$$K_{MOS} = \frac{K_f}{C_{ox} \cdot W \cdot L}.$$

Equation 4-49

Under the assumption that the flicker noise due to two input transistors dominates, and plugging the results for the white noise and 1/f noise coefficients back into the Equation 4-46, we obtain the following expression for the 1/f noise of the op-amp to be

$$S_{1/f} = \frac{2 \cdot \ln 1.3 \cdot K_f}{C_{ox} \cdot (W \cdot L)_1}.$$

Equation 4-50

Equation 4-50 indicates one method for decreasing 1/f noise, namely increasing the gate area of the input MOSFET's. Flicker noise is predominant at the lower frequencies, and as such is not expected to be an issue in bandpass converters centered at a higher frequency.

Combining Equation 4-47 and Equation 4-50, the following expression is obtained for the input referred noise of the op-amp in the resonator:

$$S_{amps_i} = \sigma^2_{amps_i} = \frac{2 \cdot k \cdot T}{M \cdot g_{m_{1_i}} \cdot \tau_i} + \frac{2 \cdot \ln 1.3 \cdot K_f}{C_{ox} \cdot (W \cdot L)_{1_i}}.$$

Equation 4-51

for i=1, 2, 3 and 4.

4.2.2 THE QUANTIZER AND 1 BIT D/A NON-IDEALITIES

The quantizer appears after the loop gain block and before the output terminal, so that any non-idealities associated with it are shaped by the loop in the same way the quantization noise it produces is. This means that at the frequencies of the interest, the quantizer non-idealities are attenuated the most.

This is most easily illustrated by considering the offset of the quantizer, $V_{os,quantizer}$. In a forth-order loop, two resonators appear between the input terminal and the quantizer so that input referred offset becomes

$$V_{os,input} = \frac{V_{os_{quantizer}}}{A_{DC_1} \cdot A_{DC_2}},$$

Equation 4-52

where A_{DC1} and A_{DC2} are the open-loop DC gains of the first and second resonator, respectively.

Another quantizer non-ideality that can affect converter performance is the comparator hysteresis, since it can cause current comparator decisions to be dependent on the previous decisions. Memory in comparator can cause errors in both STF and NTF [8].

Any D/A non-ideality, on the other hand, can be modeled as an error source that adds directly to the input, and therefore does not benefit from the noise shaping property of the sigma-delta converter. The D/A converter of the first stage is required to be nearly as linear as the overall conversion resolution. 1 bit D/A converters are inherently linear, and as such are very attractive for this application. Since they are implemented as switches between two reference levels, Vref and -Vref, where Vref=$\frac{\Delta}{2}$, any noise on these reference voltages will add to the input. Care must be taken in the design of the reference supplies that their noise does not impact the modulator.

4.2.3 SAMPLING CLOCK JITTER

In sigma-delta converter, sampling clock jitter results in nonuniform sampling of input and increases the total error power in the quantizer output. The magnitude of this error increase is both a function of the statistical properties of the jitter and the input to the converter. An estimate is derived below.

The error resulting from sampling a sinusoidal signal with amplitude A and frequency f, at the instant that is in error for δ seconds is given by

$$\varepsilon = x(t+\delta) - x(t) \approx 2 \cdot \pi \cdot f \cdot \delta \cdot A \cdot \cos(2 \cdot \pi \cdot f \cdot t) .$$

Equation 4-53

Whether oversampling will help to reduce the output error caused by the jitter depends on the nature of the jitter. Assuming that the sampling uncertainty, δ, is an uncorrelated Gaussian random process with standard deviation Δt, the resultant error will have uniform power spectral density from 0 to fs/2, with a total power of

$$S_\varepsilon = \frac{(A \cdot 2 \cdot \pi \cdot f \cdot \Delta t)^2}{2}.$$

Equation 4-54

The decimation filter removes the content of this signal at frequencies above the baseband. Since the clock jitter δ is assumed to be white, the total power of the error is reduced by the oversampling ratio M in the decimation process. The in-band error power, $S_{\Delta t}$, is therefore

$$S_{\Delta t} \le \frac{(\Delta \cdot \pi \cdot 17 \cdot BW \cdot \Delta t)^2}{8 \cdot M}.$$

Equation 4-55

In this expression, the worst case amplitude ($A_{max}=\pm\Delta/2$) and signal frequency $f_{max}=f_c+BW/2=17/2$ have been used to establish the upper bound on the error power.

On the other hand, if the clock jitter has a 1/f characteristics, the error will have a spectrum that appears as a "skirt" on the spectral line of the fundamental. The oversampling will not reduce the in-band noise in this case, and a sigma-delta converter will have the same sensitivity to jitter as a Nyquist rate converter [8].

4.3 CONVERTER DESIGN

There are two major noise sources in the bandpass sigma-delta converter, the quantization noise, and the noise due to the non-idealities of the circuit blocks. The quantization noise is inherent to the A/D conversion, as discussed in Chapter 2, and it gets worse in the presence of the capacitor mismatch. The second noise source are the imperfections of the converter's building blocks, as discussed in Section 4.2. This section quantifies the quantization noise and noise due to non-idealites. It presents the noise allocation, i.e., how much noise budget was allocated to each type of the noise present, as well as how each of the allocated noise was modeled in MIDAS. Section 4.4 will then present the results of the MIDAS simulations, verifying that the noise allocation presented here indeed results in a converter that meets the desired specifications.

Our target is SNRmax of 62 dB, (for calculation purposes let SNRmax=63dB to allow for 1dB of margin) which equates to requiring S_N=1.38e-8 V^2_{rms}. Under the assumption that the random noise sources are statistically independent, so that their power spectra add, we can model the total noise in the circuit, S_N, as simply the sum of the noise sources power spectra, i.e.

$$S_N = S_{quantization} + S_{circuit} + S_{\Delta t_{max}},$$

Equation 4-56

where $S_{quantization}$, $S_{circuit}$ and $S_{\Delta tmax}$ are the power spectra of quantization noise, the noise due to the circuit non-idealities other than clock jitter, and the noise due to the clock jitter.

How do we allocate the noise budget to these noise sources?

Let us first note, that for our choice of error mixing coefficients, β_1 and β_2, of 1/2 and 1,

respectively, it can be calculated from Equation 2-52 that in the absence of the capacitor mismatch, $S_{quantizaton}$=2.5e-9 V^2_{rms}. To allow for additional loss of less than 2 dB in the presence of the resonator gain capacitor mismatch, we will allow 1.5e-9 V^2_{rms} of margin, allocating the total of 4e-9 V^2_{rms} to $S_{quantizaton}$. In order to relax the requirement on the clock jitter, we will allow

$$S_{\Delta t_{max}} \approx \frac{1}{2} \cdot S_N .$$

Equation 4-57

It follows that

$$S_{\Delta t_{max}} = 6.9e-9\ V^2_{rms},\ S_{quantization} = 4e-9\ V^2_{rms} \text{ and } S_{circuit} = 2.9e-9\ V^2_{rms}.$$

4.3.1 THE QUANTIZATION NOISE IN THE PRESENCE OF MISMATCH

The expression for the quantization noise in the presence of the mismatch has been derived in the Section 2.2.1.2, and is given in Equation 2-51. For the case when 1-bit D/A converters are used in each of the stages, this equation reduces to

$$S_{ee_{quantization}} \approx \sigma^2_{\beta_1} \frac{\pi^4}{5 \cdot M^5} \cdot \frac{\Delta^2}{12} + \sigma^2_{\beta_2} \cdot \frac{1}{\beta^2_{1d}} \cdot \frac{\pi^6}{7 \cdot M^7} \cdot \frac{\Delta^2}{12} + \frac{1}{\beta^2_{1d} \cdot \beta^2_{2d}} \cdot \frac{\pi^8}{9 \cdot M^9} \cdot \frac{\Delta^2}{12} .$$

Equation 4-58

The implementation of the coefficients β_1 and β_2 chosen in this work dictates the following expression for the mismatch variances $\sigma^2_{\delta\beta_1}$ and $\sigma^2_{\delta\beta_2}$:

$$\sigma^2_{\delta\beta_1} = \left(\frac{\sigma_{a_{i_1}}}{a_{i_1}}\right)^2 + \left(\frac{\sigma_{a_{i_2}}}{a_{i_2}}\right)^2 + \left(\frac{\sigma_{a_{i_3}}}{a_{i_3}}\right)^2 + \left(\frac{\sigma_{a_{f_3}}}{a_{f_3}}\right)^2 \text{ and}$$

$$\sigma^2_{\delta\beta_2} = \left(\frac{\sigma_{a_{f_3}}}{a_{f_3}}\right)^2 + \left(\frac{\sigma_{a_{i_4}}}{a_{i_4}}\right)^2 + \left(\frac{\sigma_{a_{u_4}}}{a_{u_4}}\right)^2 .$$

Equation 4-59

Here the advantage of implementing the difference of two input signals using only one sampling capacitor becomes evident; the operation of subtraction implemented in this way is insensitive to error from capacitor mismatch. Mathematically, there are less terms contributing in the above expressions for the error variance.

In order to quantify the effect of mismatch on the performance of the converter, we will make several assumption. First, let's assume we are using a process with oxide capacitance of 1.5 $fF/\mu m^2$. Second, let's assume that the capacitor mismatch is given by the following relation,

$$Mis = \sqrt{\frac{40^2}{W \cdot L} + \left(\frac{15}{W}\right)^2 + \left(\frac{15}{L}\right)^2}\ \%,$$

Equation 4-60

as a function of the capacitor width, W and length, L, where Mis is the $3-\sigma$ mismatch in %. There are various layout techniques that could improve the capacitor matching, but none of them are assumed here. The goal was to arrive at the worst case numbers for mismatch and use these estimate for the simulations. Mis is taken to be our worst case mismatch. Third, assume the capacitors are square, i.e. that W=L, to minimize the impact of the mismatch. With these assumptions and our capacitor values (the choice of capacitor values is discussed in Section 0), we arrive at the following numbers for mismatch

PARAMETER	C_S or C_D [pF]	L=W [μm]	M [%]
$a_{i1} = a_{f1}$	1.5	31.6	1.43
$a_{i2} = a_{f2}$	1.5	31.6	1.43
$a_{i3} = a_{u3}$	0.9	24.5	1.85
a_{f3}	0.6	20	2.26
a_{i4}	0.9	24.5	1.85
$a_{u4} = a_{f4}$	0.3	14.1	3.21

Table 4-1 The capacitor mismatch for 1.5 $fF/\mu m^2$ process

so that $\sigma^2_{\delta\beta_1}$ becomes 1.26e - 3 and $\sigma^2_{\delta\beta 2}$ becomes 1.88e - 3. Hence, it can be calculated that the incremental loss in SNR due to the resonator gain mismatch for the chosen capacitor sizes is less than 1.6 dB in a 1.5 $fF/\mu m^2$ process, resulting in the $S_{quantization}$=3.61e-9 V^2_{rms}, which

meets our noise budget. The calculated SNR is compared to the simulated one in Figure 4.14, where we see that the two follow closely, as expected. The only difference is that the real converter overloads at high input levels, as confirmed by the MIDAS simulations, while not accounted for in our calculations.

MODELING IN MIDAS: In order to model mismatch in MIDAS, each of the resonator gains were deliberately offset by the amounts given in Table 4-1.

COEFFICIENT	$a_i = a_f$	$a_{i2} = a_{f2}$	$a_i = a$	a_f	a_i	$a_i = a_f$
WORST CASE M [%]	+1.43	+1.43	+1.85	-2.26	+1.85	-3.21

Table 4-2 The worst case resonator gain mismatch

Simulations were done to establish the direction of the mismatch for each resonator gain that results in the biggest reduction of converter's SNR_{max}. The worst cases for each resonator gain, summarized in Table 4-2, were then stacked, and the resulting reduction in converter's performance recorder and compared to the calculated in Figure 4.14. The simulations results follow the predicted response closely and therefore verify that the quantization noise in the presence of the mismatch still meets the noise budget allocated to it.

4.3.2 THE CIRCUIT NOISE

Each of the circuit blocks contains components that generate the circuit noise. The most relevant sources of circuit noise were identified in Section 4.2, and are quantified in this section. Section 4.3.2.1 quantifies the resonator noise, while Section 4.3.2.2 quantifies quantizer and D/A noise. Both sections also briefly describe how each circuit noise source was modeled in MIDAS.

4.3.2.1 THE RESONATOR CIRCUIT NOISE

Three dominant types of circuit noise in the resonator were identified and discussed in Section 4.2.1: resonator intrinsic circuit noise, which includes the thermal noise of the resonator switches and the input referred noise of the resonator op-amps, the noise due to the incomplete settling of the resonator, and the noise due to the finite DC gain of the op-amps.

The noise generated in the resonators can be modeled with the input-referred noise generators

denoted n_{i1}, n_{i2}, n_{i3} and n_{i4} at the a_{i1}, a_{i2}, a_{i3} and a_{i4} inputs, respectively. These noise generators could equivalently be modeled as a single noise generator at the input x, denoted n. Neglecting delays, we would obtain the following relation between the two modeling approaches

$$n = n_{i1} + \frac{(1+z^{-2})}{a_{i1}} \cdot n_{i2} + \frac{(1+z^{-2})^2}{a_{i1} \cdot a_{i2}} \cdot n_{i3} + \frac{(1+z^{-2})^3}{a_{i1} \cdot a_{i2} \cdot a_{i3}} \cdot n_{i4} .$$

Equation 4-61

The noise generated in the second, third and the fourth resonator is shaped by the feedback loops of the converter. The noise in the second resonator is shaped by a second order NTF, the noise in the third resonator by a fourth order NTF and the noise in the fourth resonator is shaped by the eight order NTF. This means that the performance requirements on the subsequent resonators could be relaxed in order to achieve power savings necessary to meet the power budget.

The total in-band resonator circuit noise power, $S_{resonator}$, can then be expressed as

$$S_{resonator} \approx S_{res1} + \frac{1}{a_{i1}} \cdot \frac{\pi^2}{M^2} \cdot S_{res2} + \frac{1}{a_{i1} \cdot a_{i2}} \cdot \frac{\pi^4}{M^4} \cdot S_{res3} + \frac{1}{a_{i1} \cdot a_{i2} \cdot a_{i3}} \cdot \frac{\pi^6}{M^6} \cdot S_{res4} ,$$

Equation 4-62

where S_{res_1}, S_{res_2}, S_{res_3} and S_{res_4} are the in-band circuit power spectra of the first, second, third and forth resonator respectively.

There are three main conditions we will use in the allocation of the resonator circuit noise budget. First, let us note that in a well designed sigma-delta converter, the noise due to the resonator circuit non-idealites is the dominant source of circuit noise. Following this observation in our circuit noise allocation, we will make

$$S_{resonator} = \frac{2}{3} \cdot S_{circuit} = 2e-9\ V_{rms}^2 .$$

Equation 4-63

In other words, we expect maximum of 1.8 dB of additional loss in SNR due to the resonator circuit noise. Next, we know that from all resonators in a sigma-delta converter, the first resonator is the dominant source of noise, since its noise adds directly to the input and therefore does not undergo noise shaping. Therefore, we will make

$$\frac{1}{a_{i1}} \cdot \frac{\pi^2}{M^2} \cdot S_{res2} \approx \frac{1}{a_{i1} \cdot a_{i2}} \cdot \frac{\pi^4}{M^4} \cdot S_{res3} \approx \frac{1}{a_{i1} \cdot a_{i2} \cdot a_{i3}} \cdot \frac{\pi^6}{M^6} \cdot S_{res4} \approx \frac{S_{res1}}{10},$$

Equation 4-64

allocating the biggest amount of circuit noise to the first resonator, i.e.

$$S_{res1} = \frac{10}{13} \cdot S_{resonator} .$$

Equation 4-65

Final observation here is that the thermal noise of the resonator switches dominates the resonator circuit noise. Therefore we will impose

$$\frac{S_{switches_i}}{S_{amps_i} + S_{slew_i} + S_{DC_i}} \approx 10,$$

Equation 4-66

for i=1, 2, 3 and 4.

Finally, we obtain that

$$S_{switches_1} \approx 10 \cdot (S_{amps_1} + S_{slew_1} + S_{DC_1}) \approx 1.5e-9\ V_{rms}^2,$$
$$S_{switches_2} \approx 10 \cdot (S_{amps_2} + S_{slew_2} + S_{DC_2}) \approx 1.95e-9\ V_{rms}^2,$$
$$S_{switches_3} \approx 10 \cdot (S_{amps_3} + S_{slew_3} + S_{DC_3}) \approx 3.36e-8\ V_{rms}^2, \text{ and}$$
$$S_{switches_4} \approx 10 \cdot (S_{amps_4} + S_{slew_4} + S_{DC_4}) \approx 4.36e-7\ V_{rms}^2.$$

Equation 4-67

4.3.2.1.1 THE THERMAL NOISE OF THE SWITCHES

From the expressions for the switch noise of the resonator derived in section 4.2.1.4 and our switch noise budget given in Equation 4-67, it follows that $C_{s_{1min}} \approx 1.4$ pF, $C_{s_{2min}} \approx 1.2$ pF, $C_{s_{3min}} \approx 0.07$pF and $C_{s_{4min}} \approx 0.01$ pF. In order to minimize the power dissipated, we would like to use the minimum size sampling capacitors. In the presence of the capacitor mismatch, however, the converter performance degrades. Due to the resonator gain mismatch, the quantization noise increases, as already discussed in Section 4.3.1. Variation of the capacitor sizes may also increase the thermal noise of the switches. Smaller the capacitor, bigger the effect of the capacitor mismatch, as evident from Equation 4-60. Spreadsheet was used to establish the minimum capacitor sizes that would still result in the desired converter performance in the presence of the capacitor mismatch. The following capacitor sizes were chosen: $C_{s_1} = 1.5$ pF, $C_{s_2} = 1.5$ pF, $C_{s_3} = 0.9$ pF and $C_{s_4} = 0.9$ pF.

MODELING IN MIDAS: The switch noise generated in the resonators is modeled in MIDAS as input referred gaussian noise generators $n_{switches_1}$, $n_{switches_2}$, $n_{switches_3}$ and $n_{switches_4}$ at the a_{i1}, a_{i2}, a_{i3} and a_{i4} inputs. Using derivations of Section 4.3.2.1.1, we can model these gaussian noise generators have zero means and variances given by

$$\sigma^2_{n_{switches_1}} = \frac{8 \cdot k \cdot T}{C_{s1}},\ \sigma^2_{n_{switches_2}} = \frac{\frac{28}{3} \cdot k \cdot T}{C_{s2}},\ \sigma^2_{n_{switches_3}} = \frac{14 \cdot k \cdot T}{C_{s3}} \text{ and } \sigma^2_{n_{switches4}} = \frac{16 \cdot k \cdot T}{C_{s4}},$$

Equation 4-68

since the total power of the noise source will be reduced in the decimation process by the

oversampling ratio M. For the worst case switch thermal noise, the capacitor sizes were decreased for the maximum amount of mismatch.

4.3.2.1.2 THE INPUT REFERRED NOISE OF THE OP AMPS

The input referred noise of the op amps was identified, discussed and captured by the analytical expression in Section 4.2.1.3. Combined with the noise budget allocated to the input referred noise of the op amps in Section 4.3.2.1, as given in Equation 4-67, the expressions for the input referred op amp noise provide the minimum value for $(g_{m_i} \cdot \tau_i)$ and $(W \cdot L)_i$ for i=1, 2, 3 and 4. Other considerations set the tighter minimum design constraints for these parameters, however. The incomplete settling considerations in the next section, Section 4.3.2.1.3, set the design constraint on the resonator time constants, τ_i, as given by Equation 4-76. The transconductance of the amplifiers input devices, g_{m_i}, is then determined from Equation 4-16 and Equation 4-6 that link the resonator time constant to g_{m_i} and the $C_{TL_{settle}}$, since this design constraint happens to be tighter than the one imposed by the input referred op amp noise. 1/f noise turns out to have minimal effect on converter's performance, so that amplifiers input device lengths were kept technology minimum, for speed considerations, and the spreadsheet was used to arrive at the optimal width of the amplifiers input devices that resolves the following trade-off. For fixed g_{m_i}, increasing Wi is desirable, since it decreases the bias current needed, minimizing the power consumption. Increasing Wi, on another hand, decreases unity gain frequency, by increasing Cgs of the amplifier input devices, therefore increasing the total load capacitance, C_{TL} and decreasing the feedback factor, f. The resulting values of g_{m_i}, τ_i and $(W \cdot L)_{1_i}$ for i=1, 2, 3 and 4 are summarized in Table 4-3 at the end of chapter.

MODELING IN MIDAS:

The white and 1/f circuit noise generated in the resonator's amplifiers is modeled in MIDAS as input referred gaussian noise generators n_{amps_1}, n_{amps_2}, n_{amps_3} and n_{amps_4} at the a_{i1}, a_{i2}, a_{i3} and a_{i4} inputs. Using derivations of Section 4.2.1.5, we can model these gaussian noise generators as having zero means and variances given by

$$S_{m-amps_i} = \sigma^2_{m-amps_i} = \frac{2 \cdot k \cdot T}{g_{m_{1_i}} \cdot \tau_i} + M \cdot \frac{2 \cdot \ln 1.3 \cdot K_f}{C_{ox} \cdot (W \cdot L)_{1_i}}$$

Equation 4-69

for i=1, 2, 3 and 4, since the total power of the noise source will be reduced in the decimation process by the oversampling ratio M.

Spreadsheet was used to calculate that there is 1.65 dB of additional loss in SNR due to worst case resonator intrinsic circuit noise. In addition, the behavioral simulations were done to verify that the circuit noise budget is met for the worst case resonator intrinsic circuit noise, in the presence of the worst case circuit mismatch, by reducing all the capacitances in this model for the amount of offset specified in Table 4-1. The results are shown in Figure 4.15, where we see that the simulation results closely follow the predicted behavior, indicating an additional 1.65 dB of reduction in SNR due to the presence of the worst case resonator intrinsic circuit noise.

4.3.2.1.3 THE NOISE DUE TO THE FINITE RESONATOR SPEED

In modeling the finite resonator speed, several assumptions were made. First, it was assumed that the resonator settling speed is limited only by the amplifier finite settling, since the problems due to the speed limitation due to the RC constant of the resonator switches in series with the sampling capacitors can be easily solved by increasing the width of the switches, as already discussed in Section 4.2.1. Second, a first-order model of the settling characteristics of the generic resonator defined by Equation 3-3 is assumed, as given by the following expression.

$$r((n+1) \cdot T_s) = -r((n-1) \cdot T_s) + g\left(\sum_i a_i \cdot x_i(n \cdot T_s)\right)$$

Equation 4-70

where

$$g(x)=\begin{cases} x\cdot(1-e^{-\frac{T_{sett}}{\tau}}), & |x|<\tau\cdot\zeta \\ x-\mathrm{sgn}(x)\cdot\tau\cdot\zeta\cdot e^{(\frac{|x|}{\tau\cdot\zeta}-\frac{T_{sett}}{\tau}-1)}, & \tau\cdot\zeta<|x|<(\tau+T_{sett})\cdot\zeta \\ \mathrm{sgn}(x)\cdot\zeta\cdot T_{sett}, & (\tau+T_{sett})\cdot\zeta<|x| \end{cases}$$

Equation 4-71

and τ is the exponential settling time constant of the resonator, as given by Equation 4-16, and ζ is its maximum slope, i.e. the maximum slew rate of the amplifier, as given by the Equation 4-4.

The desired settling accuracy for each resonator is given by

$$\text{Sett. Acc.} = \frac{1}{2^{N_i}}$$

Equation 4-72

for i=1, 2, 3, and 4 and summarized in Table 4-3 at the end of the chapter. In order to meet the target settling accuracy, we need to decide on τ and ζ of each resonator. How do we do this?

Here we adopted the solution for eliminating the effects of non-linear settling by making the circuit settle completely enough so no matter what the signal dependence may be, the desired resolution is achieved, as discussed in section 4.2.1.

First we need to know what is the largest possible change in the input voltage to the resonator, $V_{step_{i_{max}}}$, for each resonator, i.e. for i=1, 2, 3 and 4, where

$$V_{step_{i_{max}}} = \left(\sum_n a_n \cdot x_n(z)\right)_{max}.$$

Equation 4-73

Looking at the block diagram of the converter, given in Figure 3.14, and applying Equation 4-73 to the values of resonator gains as given in Section 3.2.2, we see that

$$V_{step_{1_{max}}} = \frac{1}{2}\cdot(2\cdot V_{x_{max}}) + \frac{1}{2}\cdot(2\cdot V_{ref}) = 0.58\ V,$$
$$V_{step_{2_{max}}} = \frac{2}{3}\cdot V_{step_{1_{max}}} + \frac{2}{3}\cdot(2\cdot V_{ref}) = 0.85\ V,$$
$$V_{step_{3_{max}}} = \frac{1}{2}\cdot V_{step_2} + \frac{1}{2}\cdot(2\cdot V_{ref}) + \frac{1}{3}\cdot(2\cdot V_{ref}) = 1.01\ V,\ \text{and}$$
$$V_{step_{4_{max}}} = \frac{1}{2}\cdot V_{step_3} + \frac{1}{6}\cdot(2\cdot V_{ref}) + \frac{1}{6}\cdot(2\cdot V_{ref}) = 0.74\ V.$$

Equation 4-74

These are theoretical worst case resonator input steps. The behavioral simulations were run to verify the calculated results. The simulations results are given in Figure 4.10, and the worst case resonator input steps are established to be

$$V_{step1_{max}} = 0.58\ V,\ V_{step2_{max}} = 0.7\ V, V_{step3_{max}} = 0.6\ V \text{ and } V_{step4_{max}} = 0.26\ V.$$

Equation 4-75

The largest bandlimiting time constant of each resonator is the time constant with which the circuit settles if only linear settling occurs. Linear settling occurs for low to medium input resonator voltage changes, more precisely for $V_{step_i} < \tau\cdot\zeta$. In this case, the resonators settle without slew rate limiting from the amplifiers. Hence, the resonators settle to the same settling accuracy independent of the amplitude of the input signal. This is equivalent to reducing the resonator gain by a factor of $(1 - e^{-\frac{T_{sett}}{\tau}})$. For this gain error to be insignificant, we want to achieve the desired settling accuracy, so that

$$\tau_{max_i} = \frac{T_{sett}}{\ln 2^{N_i}}$$

Equation 4-76

for i=1, 2, 3 and 4, where N_i is the dynamic range of the i-th resonator in effective bits and is smaller for the subsequent resonators due to the noise shaping, and T_{sett} is the time available for the resonators to settle. It can quickly be calculated that

$$N_1 = 10.8 \text{ bits},\ N_2 = 9 \text{ bits},\ N_3 = 7 \text{ bits and } N_4 = 5.1 \text{ bits},$$

Equation 4-77

while

$$T_{sett} = \frac{T_s}{2} - 4\text{ns} \approx 8.7\text{ns};$$

Equation 4-78

as already discussed in section 4.2.1.1, so that

$$\tau_{1\,max} \approx 1.2\text{ns},\ \tau_{2\,max} \approx 1.4\text{ns},\ \tau_{3\,max} \approx 1.8\text{ns and } \tau_{4\,max} \approx 2.5\text{ns}.$$

Equation 4-79

For larger input resonator voltages, i.e. for $\tau \cdot \zeta < \left|V_{step_i}\right| < (\tau + T_{sett}) \cdot \zeta$, the non-linear settling occurs where the resonator is strongly slew-rate limited. The slew- rate limited resonators create harmonic distortion. If we design our amplifier fast enough, nonlinear effects of the slew rate limiting can be reduced to negligible levels, and we therefore choose the time constants given in Equation 4-79.

We also want to make sure that settling accuracy is met in this case too, so that the following relation is satisfied

$$\frac{1}{2^{N_i}} \approx \frac{\tau \cdot \zeta}{V_{step_i}} \cdot e^{\left(\frac{\left|V_{step_i}\right|}{\tau \cdot \zeta} - \frac{T_{sett}}{\tau} - 1\right)}.$$

Equation 4-80

Using the spreadsheet, we find that following slew-rates satisfy the relation

$$\zeta_1 = \zeta_2 = 160\ \frac{V}{\mu s},\ \zeta_3 = 130\ \frac{V}{\mu s} \text{ and } \zeta_4 = 80\ \frac{V}{\mu s}.$$

Equation 4-81

MODELING IN MIDAS: The z-transform of the resonator's transfer function now becomes $R(z) = \frac{z^{-1}}{1+z^{-2}} \cdot g\left(\sum_i a_i \cdot x_i(z)\right)$ instead of the ideal one given in Equation 3-4, with g(x) as given in the Equation 4-71. This is exactly how this resonator non-ideality is modeled in MIDAS, where function *slew(x)* implements function here given as g(x). Since any hand-calculating of the amount of the in-band noise and distortion generated by the incomplete settling proves to be tedious, the effect of settling process on the performance of the converter was determined by computer simulations. The results shown in Figure 4.16 verify that the finite resonator speed does not have any significant effect on the converter performance.

4.3.2.1.4 THE NOISE DUE TO THE FINITE AMPLIFIER'S DC GAIN

All practical amplifiers have a finite DC gain. It was calculated that a finite DC gain of the amplifier results in a resonator transfer function as given by Equation 4-21. Since any hand-calculating of the amount of the in-band noise generated by the finite DC gain of the amplifiers proves to be tedious, the effect of these amplifier non-idealities on the performance of the converter was determined by computer simulations. Figure 4.17 through 4.20 illustrate the effect of the op-amp DC gains on the converter's performance. These simulations verify that the finite DC gain equivalent to the desired resolution of the stage has minimal effect on the converter performance, as reported in previous literature [38]. Namely, if we choose the amplifier gains of

$$A1 \geq 63 \text{ dB},\ A2 \geq 54 \text{ dB},\ A3 \geq 42 \text{ dB and } A4 \geq 31 \text{ dB}.$$

Equation 4-82

there is no significant reduction in performance. Another set of simulations were done,

incorporating the effect of mismatch between feedback capacitors, verifying that the op amp gains chosen are sufficient to make these effects negligible.

MODELING IN MIDAS:

Since the time in MIDAS is implemented as a counter which gets incremented each clock cycle, it was necessary to write an user defined model that implements the function even?(x) that tests whether the argument x is even or not. If we apply even? function to the time counter, on each even clock cycle use the first equation, and on each odd clock cycle use the second equation in Equation 4-21 for resonator transfer function.

4.3.2.1.5 RESONATOR NONLINEARITY

From our requirements we see that at maximum input signal level $SNDR \approx SNR - 3dB$, which implies that $S_{ee} \approx 2 \cdot S_{dd}$, and SNDR becomes

$$SNDR \approx 20 \cdot \log(\frac{1}{2 \cdot THD}).$$

If we choose

$THD_1 \approx \frac{\pi}{a_{i1} \cdot M} \cdot THD_2 \approx \frac{\pi^2}{a_{i1} \cdot a_{i2} \cdot M^2} \cdot THD_3 \approx \frac{\pi^3}{a_{i1} \cdot a_{i2} \cdot a_{i3} \cdot M^3} \cdot THD_4 \approx \frac{THD}{4}$, we obtain the maximum values for the total harmonic distortion of each resonator, as given in Table 4-3. at the end of the chapter. Coupled with the minimal values for the DC gain of the amplifiers, we can also obtain the worst case values for α_3 coefficients for each of the four amplifiers, according to the worst case Equation 4-26 derived in Section 4.2.1.2. The effect of resonator non-linearity was not simulated in MIDAS, due tot he difficulty of modeling these very small effects.

4.3.2.2 THE NOISE DUE TO THE IMPERFECTIONS IN THE 1 BIT QUANTIZER AND 1 BIT D/A CONVERTER

Any nonlinearity in the comparator can be modeled as another source which adds to quantization noise, E[n]. Therefore, the noise from this extra source is, similarly to the quantization noise, subject to noise shaping by the converter and so its effect on SNR degradation is not considered significant [36].

Comparator hysteresis, however, can put memory in the comparator, creating unwanted system poles and causing errors in both STF and NTF [8]. The output of the comparator with hysteresis can be modeled by following expression:

$$y[n]=\begin{cases} 1 & x[n]\geq +V_{th} \\ -1 & x[n]\leq -V_{th} \\ y[n-1] & |x[n]|<V_{th} \end{cases}$$

Equation 4-83

where x[n] and y[n] are the input and the output of the comparator at time n, respectively, and $\pm V_{th}$ are the threshold levels determining the comparator hysteresis.

Any non-ideality of a 1 bit D/A converter, on the other hand, will show up as an error source at the input of the converter, and will therefore not be attenuated by converter's noise shaping. Since 1 bit D/A converters are inherently linear, the only non-ideality that we may see here is noise on its reference voltages. Here, this noise is modeled as an error source that adds directly to the input.

MODELING IN MIDAS:

The comparator and D/A converter are modeled with the *quantizer* function in MIDAS. This function also allows for modeling of hysteresis, as given by Equation 4-83. The noise on the reference voltages of 1 bit D/A converter is modeled as an additive gaussian noise source with zero mean and standard deviation given by Vrefnoise. The behavioral simulations were performed to establish the highest value of V_{th} and Vrefnoise for which there is still no significant degradation in performance. The threshold levels at $\pm V_{th}=\pm\frac{Vref}{35}$ and $Vrefnoise\leq\frac{Vref}{4000}\ V_{rms}$ were find to result in less than 1 dB of additional loss in SNR.

4.3.3 THE NOISE DUE TO THE SAMPLING CLOCK JITTER

As derived in Section 4.2.3, the in-band error power, $S_{\Delta t}$, is given by

$$S_{\Delta t} \le \frac{(\Delta \cdot \pi \cdot 17 \cdot BW \cdot \Delta t)^2}{8 \cdot M}$$

Equation 4-84

In this expression, the worst case amplitude ($A_{max} = \pm\frac{\Delta}{2}$) and signal frequency $f_{max} = f_c + \frac{BW}{2} = \frac{17}{2} \cdot BW$ have been used to establish the upper bound on the error power.

It follows that the upper limit for the tolerable sampling clock jitter is

$$\Delta t \le \frac{\sqrt{8 \cdot S_{\Delta t_{max}} \cdot M}}{\Delta \cdot \pi \cdot 17 \cdot BW}.$$

Equation 4-85

Following the noise budget allocated to the sampling clock jitter, as given by Equation 4-57, and under the white noise approximation,

$$S_{\Delta t_{max}} = \frac{1}{2} \cdot S_N = \frac{1}{2} \cdot \frac{1}{12} \cdot \left(\frac{\Delta}{2^N}\right)^2$$

Equation 4-86

where S_N is the total noise and Δ is the D/A swing, here equal to $\Delta = 2 \cdot V_{ref} = 0.7\ V$, and the number of effective bits, N, here equals to 10.5. The upper bound on sampling clock jitter for additional 3 dB of SNR reduction then reduces to

$$\Delta t \leq \frac{1}{17 \cdot \pi \cdot f_B \cdot 2^N} \cdot \sqrt{\frac{M}{3}} \approx 24.33\text{ps}.$$

Equation 4-87

MODELING IN MIDAS:

Given that the signal in-band transfer function equals unity, we can model the sampling clock jitter as an additive gaussian noise source at the input of the converter with the zero mean and the variance, S_{jitter}, given by

$$S_{jitter} = M \cdot S_{\Delta t_{max}}$$

Equation 4-88

since the total power of the noise source will be reduced in the decimation process by the oversampling ratio M.

4.4 SIMULATION RESULTS AND DISCUSSION

In this section we present and discuss the simulation results obtained from MIDAS using the models proposed in the previous section, with the values of each parameter simulated given in Table 4-3 at the end of the chapter. The simulations were done with the ideal elements first. In each section new non-ideality is added, so that the effect of each non-ideality on circuit performance can be monitored separately, and the incremental added loss in converter performance recorded. First, behavioral simulations were done on the ideal converter, whose block diagram is given in Figure 3.14, with the resonator gains and error mixing coefficients as given in Table 3-3, to establish the worst case resonator input voltage steps and the worst case resonator output swings. The output of resonators are then hard clipped to the established values of amplifier swings, in order to examine the effect of the amplifier saturation on the converter performance. Next, the resonator gains were offset by the worst case capacitor mismatch to examine the effect of capacitor mismatch in resonator gains on overall

performance. Next, the resonator intrinsic circuit noise generators were added, with the capacitor mismatch in them, to monitor further loss in SNR. Further, the effects of incomplete settling were incorporated in the converter model and the simulation results recorded. At this point, the resonator transfer function given by Equation 4-21 replaced the ideal resonator model, first without the mismatch between capacitors Ca, Cb and Ch, to allow us to investigate the effects of the finite op amp gains. Next the capacitor mismatch between capacitors Ca, Cb and Ch was added, to verify whether the chosen op amp gains were sufficient to reduce the effect of this mismatch to negligible levels. Then the comparator hysteresis, D/A reference voltage noise and clock jitter was added, and their individual effects on the converter performance examined and recorded.

Determining the worst case resonator input voltage steps. The worst case resonator input voltage step happens when the input is changing at the maximum rate, i.e. $f = f_{worst} = \frac{f_s}{4} + \frac{f_B}{2}$, and with a maximum input swing, i.e. $\Delta_{max} = 2 \cdot A_{max} = 2 \cdot A_{jammer}$. The converter is modeled as given by block diagram in Figure 3.14, and the results are shown in Figure 4.10.

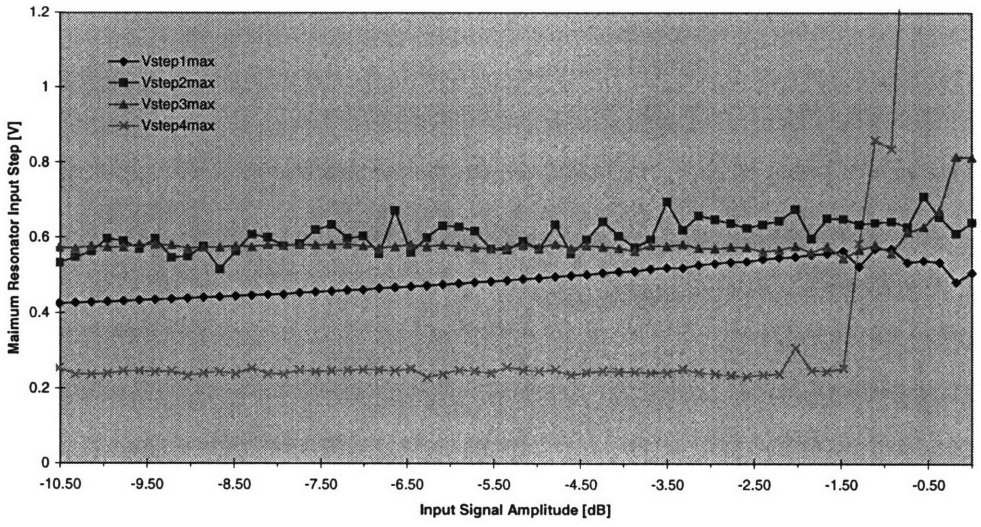


Figure 4.10 The worst case resonator's input voltage steps

We are interested in the values of the worst case resonator's input voltage steps at the maximum input signal level, i.e. -3.46dB below full scale. From Figure 4.10 we find that for

signal at -3.46 dB below the full scale, the maximum input resonator step voltages are $V_{step1_{max}} = 0.53$ V, $V_{step2_{max}} = 0.7$ V, $V_{step3_{max}} = 0.6$ V and $V_{step4_{max}} = 0.26$ V. These step voltages are somewhat smaller than the predicted values given in Equation 4-74 in Section 4.3.2.1.3. The predicted values are based on the absolute worst case scenario, where each of the involved signals steps maximally, which does not have to be and indeed according to the behavioral simulations is not the case, even under the worst case conditions.

Determining the worst case resonator output swing. The worst case resonator output swing happens when the worst case input resonator step happens, i.e. when the input is changing at the maximum rate, i.e. $f = f_{worst} = \frac{f_s}{4} + \frac{f_B}{2}$, and with a maximum input swing, i.e. $\Delta_{max} = 2 \cdot A_{max} = 2 \cdot A_{jammer}$. The converter is modeled as given by block diagram in Figure 3.14, and the results are shown in Figure 4.11

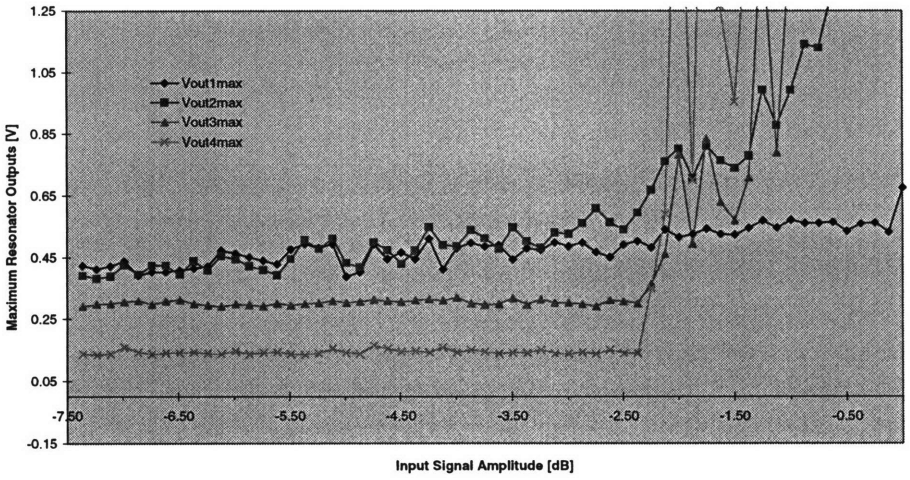


Figure 4.11 The maximum resonator outputs

Looking at the Figure 4.11, we notice several things, as follows. The output amplitude of the first resonator is well within 0.67 V for the entire range of the input signal amplitudes. The second resonator output exceeds this value for input amplitudes that are bigger than approximately -2.3 dB below full scale. The third and the fourth resonator output exceeds this value for the input signal amplitudes greater than -2 dB below full scale. Since we are interested in preserving the dynamic range for the input signal amplitudes that are -3.46 dB below the full

scale, we need only ensure that the resonator outputs are bound by certain value for the signals up until -3.46 dB below the full scale. The simulations indicate that this value is 0.5 V, 0.4 V, 0.3 V and 0.2 V for the first, second, third and fourth amplifier, respectively, indicating that we should let amplifiers saturate at $Vsat_1 = \pm 0.5$ V , $Vsat_2 = \pm 0.4$ V , $Vsat_3 = \pm 0.3$ V and $Vsat_4 = \pm 0.2$ V .

Figure 4.12 shows the histogram analysis for the output of each integrator for the input signal amplitude of -3.46 dB below the full scale, with our choice of k1a=1/2, k1b=2/3, k2=1/3 and k3=1/6. There we can see that the maximum recorded values at the output of each resonator for the input amplitude of -3.46 dB below full scale are indeed comfortably within the assigned full scale of range of operation of the op amps, never reaching the assigned saturation levels. In this way we ensure that the amplifier output range exceeds the range required by the converter dynamic range specifications, preventing the amplifier clipping and the resulting non-linearities, for the input signal range of interest.

Hard-clipping the resonator outputs in MIDAS at the given saturation levels is a way to model the resonator amplifiers saturation. Figure 4.13 illustrates the effect of the choice of the saturation voltage on the performance of the converter. We see that the chosen set of saturation voltages does not degrade converter performance.

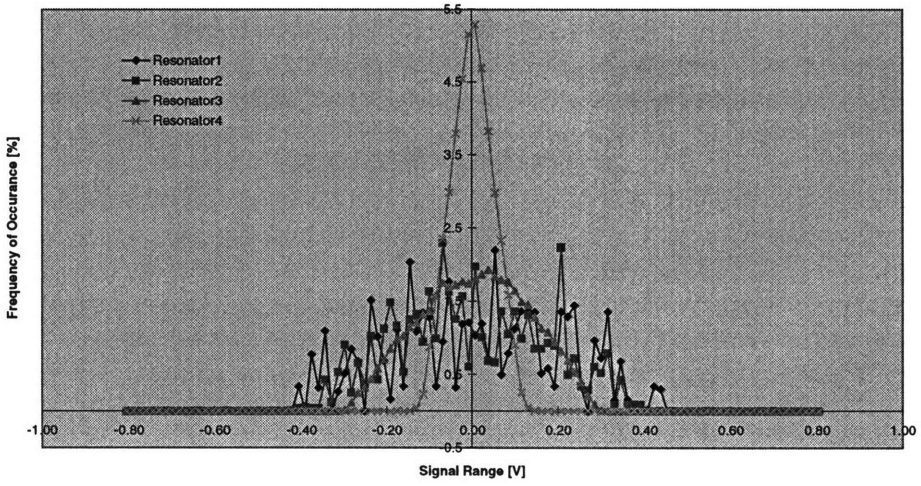


Figure 4.12 Histograms of the resonator outputs

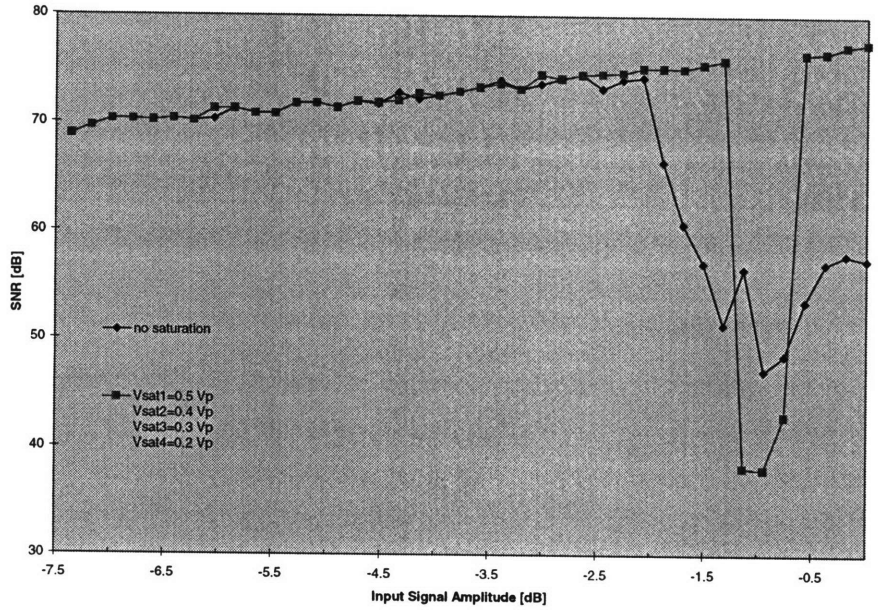


Figure 4.13 The effect of the amplifier saturation voltage on the performance of the converter

Effect of the capacitor mismatch. The simulations setup is as described in section 4.3.1. Behavioral simulations have been done on the converter of Figure 3.14, with the addition of hard clipping of the resonator outputs, as described in the previous section, in order to

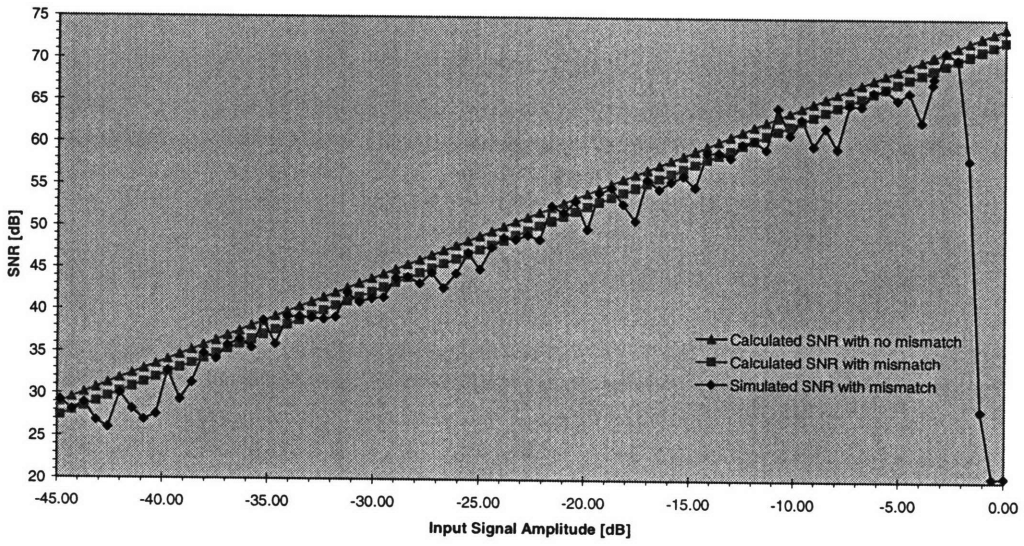


Figure 4.14 The effect of capacitor mismatch on quantization noise

establish the directions of the worst case resonator gain mismatch. The worst case resonator gain mismatches were then tabulated in Table 4-2, stacked and the circuit was resimulated. The results are summarized and compared to the calculated performance and calculated performance with no mismatch in Figure 4.14, to verify that the converter behaves as predicted. The incremental loss in SNR is approximately 1.6 dB, as predicted.

Effect of the circuit noise. In addition to all non-idealities added to the converter of block diagram shown in Figure 3.14, as described in previous simulation sets, the effects of the resonator intrinsic circuit noise were incorporated, in accordance with the models described in Section 4.3.2. The capacitors were reduced by the maximum amount of mismatch, as given in Table 4-1, to obtain the worst case resonator intrinsic circuit noise. The results, shown in Figure 4.15, closely follow predicted behavior. The additional loss in SNR is 1.65 dB, as predicted.

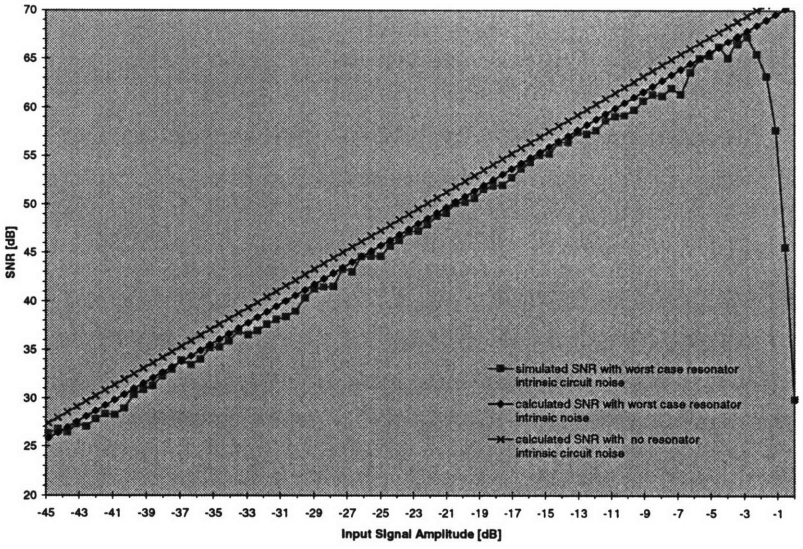


Figure 4.15 The effect of the circuit noise on the performance of the converter

The effect of the incomplete settling. The next non-ideality added is the incomplete settling, which is modeled as described in Section 4.3.2.1.3. The results, given in Figure 4.16, verify that for the chosen values of resonator time constant and amplifiers slew rates, there is no degradation in converter performance.

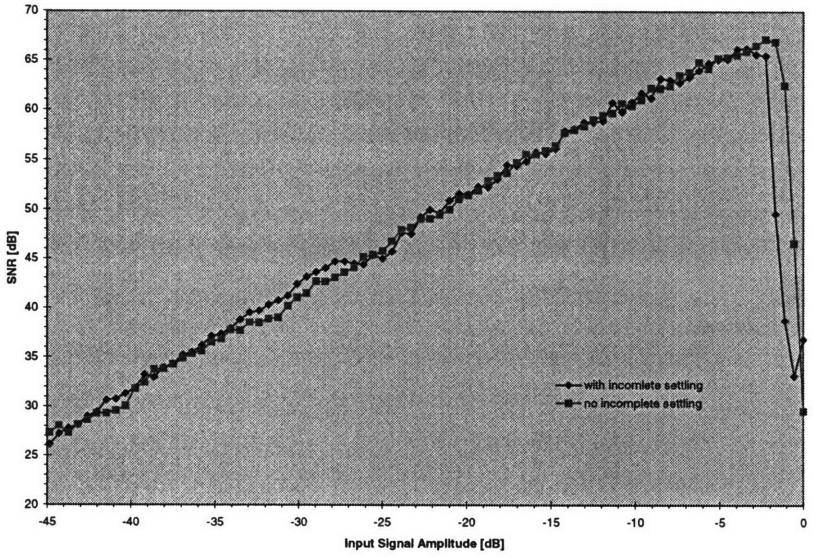


Figure 4.16 The effect of incomplete resonator settling on the performance of the converter

Effect of opamp finite DC gain. In this set of behavioral simulations, we investigate the effect of a non-infinite amplifier DC gain. The modeling is as described in the section 4.3.2.1.4 and the four simulations were set up. In each simulation, only the gain of one of the amplifiers was varied and the results are shown in Figure 4.17 through Figure 4.20.

The simulations clearly reinforce the previous evidence of the relative insensitivity to the amplifier DC gain, and the fact that the converter performance is less sensitive to the non-idealities, here the finite DC gain, of the amplifiers that are later in the chain. Even with the gain of the first amplifier of 500, the converter is capable of maintaining the target performance, although with some decrease in the SNR. It should be noted that, that in practice, higher amplifier DC gain are required to compensate for the non-linearity of these elements. Following the evidence in previous literature, the amplifier gains equal to the required stage resolution of 63 dB, 54 dB, 42 dB and 31 dB are chosen for the first, second, third and fourth amplifier, respectively.

Second set of simulation was run to determine the worst case mismatch between feedback capacitors, Ca, Cb and Ch. The worst cases were then stacked, and the simulation with the chosen amplifier gains was run to verify that no degradation in converter performance happens

in presence of mismatch, in accordance with the conclusions drawn from the analysis in Section 4.2.1.1.

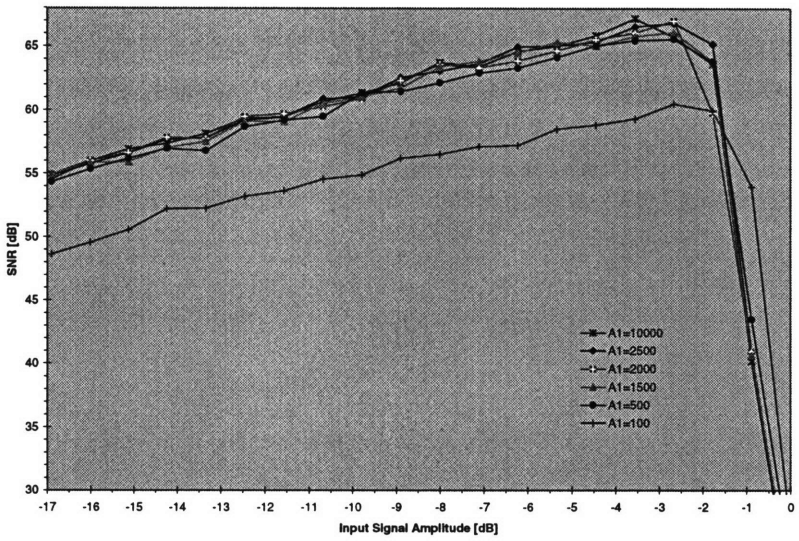


Figure 4.17 The effect of changing the dc gain of the first amplifier

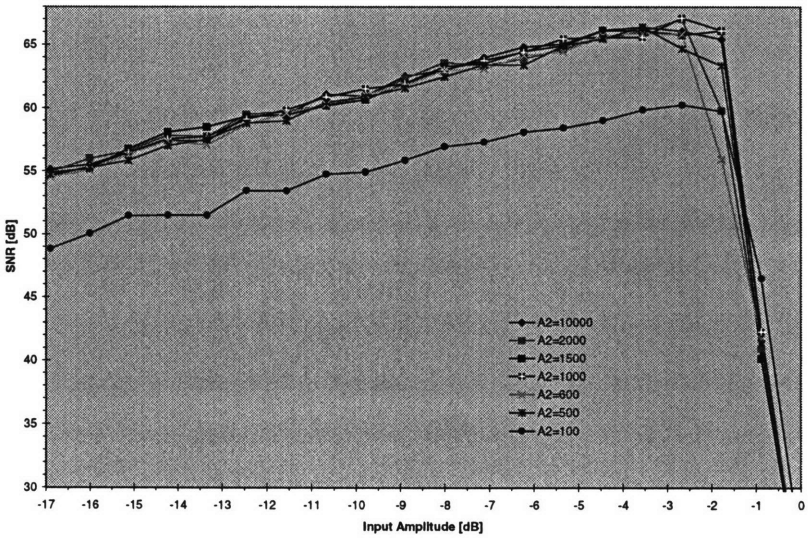


Figure 4.18 The effect of changing the dc gain of the second amplifier

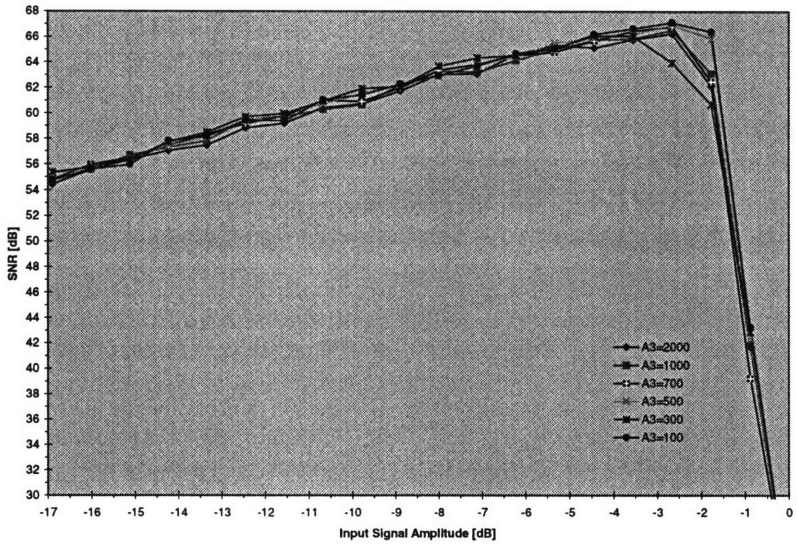


Figure 4.19 The effect of changing the dc gain of the third amplifier

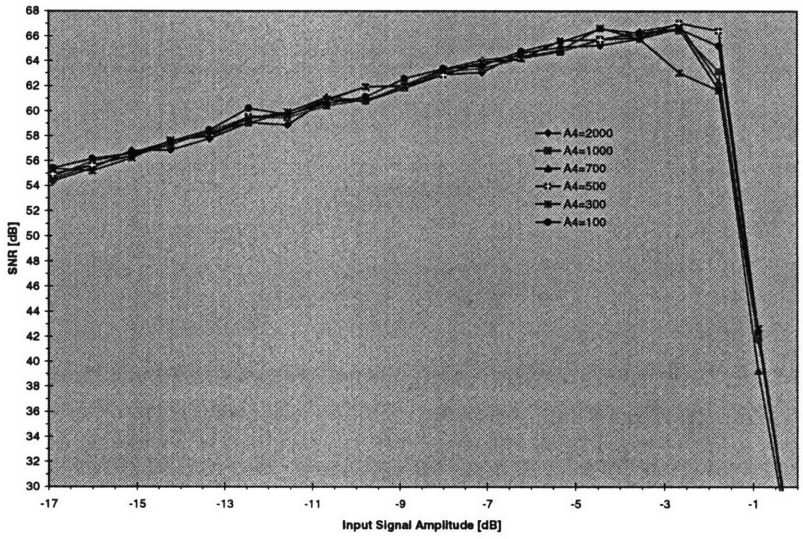


Figure 4.20 The effect of changing the dc gain of the fourth amplifier

The effect of the comparator hysteresis. Next non-ideality added was the comparator hysteresis, which was modeled as given in section 4.3.2.2. The circuit was then simulated for several of different values of hysteresis threshold levels, $\pm V_{th}$, and the results summarized in Figure 4.21.

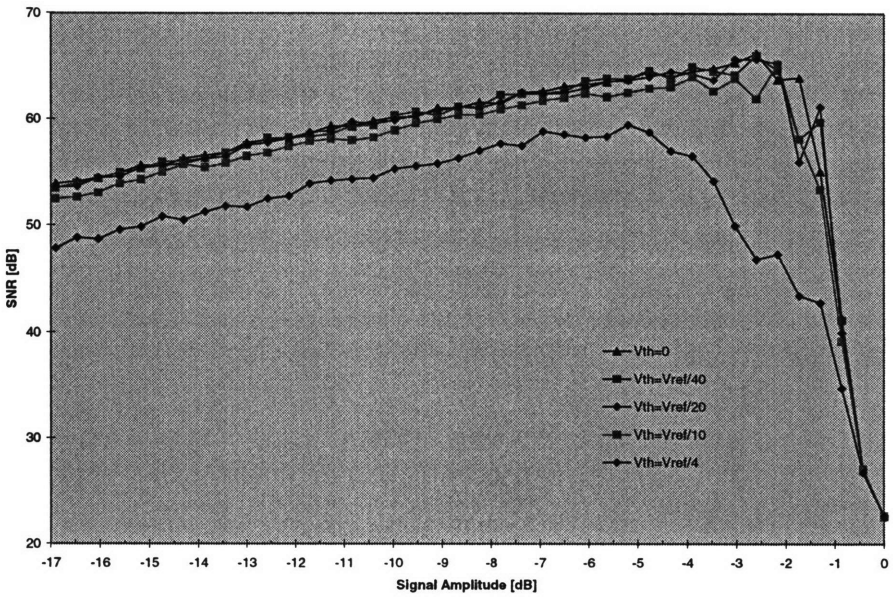


Figure 4.21 The effect of the comparator hysteresis

The values of hysteresis thresholds of ±Vth=±Vref/35 were taken as the maximum allowable hysteresis threshold levels for the comparators in this work, for ~0.5 dB of additional loss.

The effect of the noise on the D/A reference voltages. The noise on D/A reference voltages has been modeled as described in Section 4.3.2.2. The results, given in Figure 4.22,

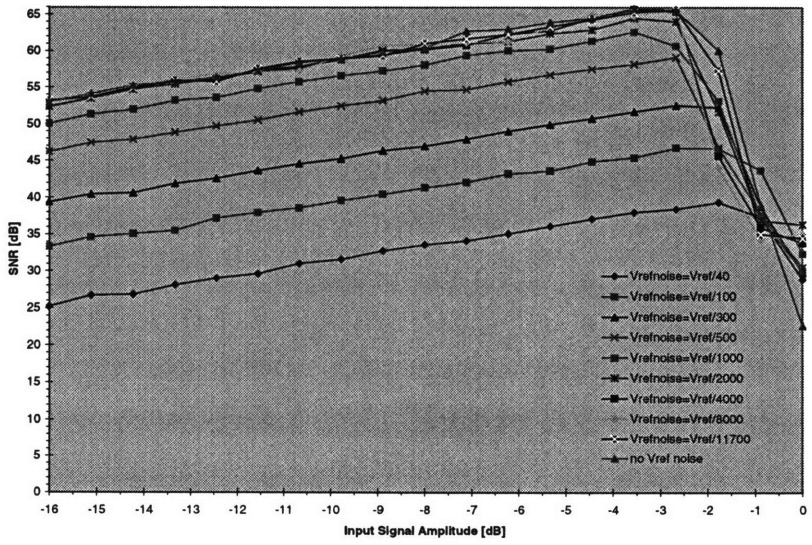


Figure 4.22 The effect of the noise on the D/A reference voltages.

reinforce the importance of clean D/A reference voltages. They also suggest that there is no significant loss in performance for $Vrefnoise \leq \frac{Vref}{4000}$. The maximum allowable noise on the D/A reference voltage is therefore taken to be Vrefnoise=Vref/4000.

Effect of the clock jitter. Using the modeling described in section 4.3.3, we simulated for three different values of the sampling clock jitter. The results support the previously discussed evidence of relatively high sensitivity to the jitter. Only if the clock jitter is constrained to be at the most Δt=24.23 ps can the converter meet the required specified target performance, as discussed in section 4.3.3 and illustrated in Figure 4.23.

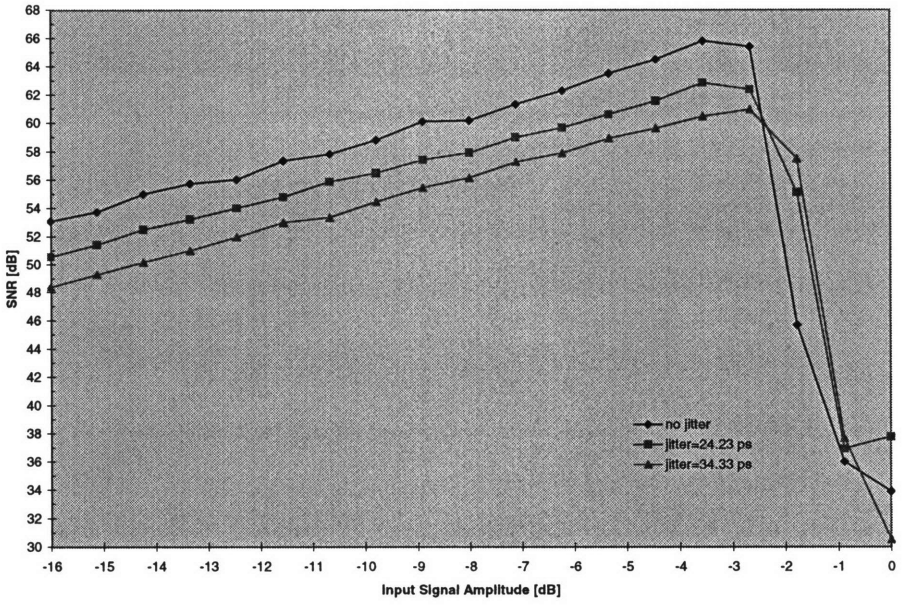


Figure 4.23 The effect of the sampling clock jitter on the performance of the converter

4.5 SUMMARY

In this chapter, several relevant non-idealities of sigma-delta converters were identified and studied, and then quantified for the design at hand. The behavioral simulations were then run in MIDAS to verify the converter design. The results are summarized below.

The ideal converter of Figure 3.14 with SNRmax of 76 dB was the starting point in noise budget allocation. Additional 6 dB was lost due to the choice of error mixing coefficient, β_1 and β_2, of ½ and 1, respectively. In the presence of resonators gains capacitor mismatch, there is an additional 1.6 dB of loss in SNR. Due to the resonator circuit noise, there is about 1.65 dB of additional loss in performance. Additional 1 dB of loss in SNR is allocated to comparator hysteresis and noise on the voltage references of 1 bit D/A converters, and 3 dB to sampling clock jitter. The resulting SNRmax is approximately 62.9 dB in the single-ended case, with additional 3 dB of improvement expected from using fully differential circuitry for the actual implementation. The output spectrum of the behavioral converter obtained from MIDAS is given in Figure 4.24.

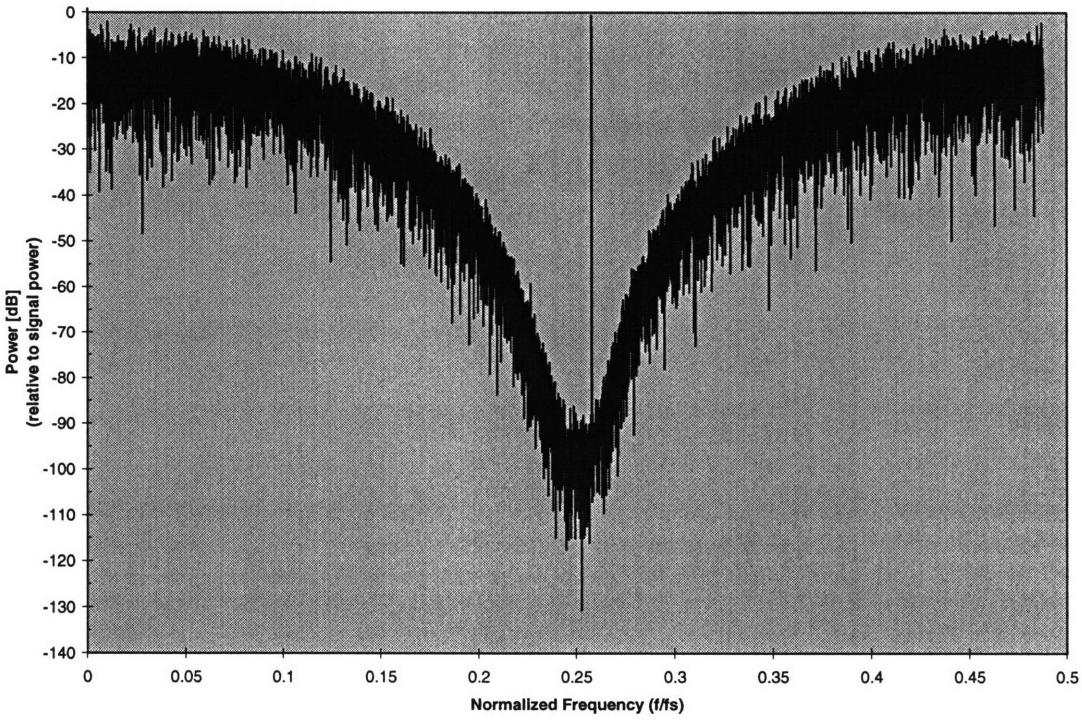


Figure 4.24 Output spectrum of a single-ended behavioral converter for signal -3.46 dB below the full scale

The actual circuit parameters needed to implement the designed behavioral converter were also quantified, and are summarized in Table 4-3.

PARAMETER	VALUE IN THE FIRST RESONATOR	VALUE IN THE SECOND RESONATOR	VALUE IN THE THIRD RESONATOR	VALUE IN THE FOURTH RESONATOR
Ca=Cb=Ch	3 pF	2.25 pF	1.8 pF	1.8 pF
Cs	1.5 pF	1.5 pF	0.9 pF	0.9 pF
Cd	0	0	0.6 pF	0.3 pF
τ	$\leq$ 1.2 ns	$\leq$ 1.4 ns	$\leq$ 1.8 ns	$\leq$2.5 ns
τ_A	$\leq$0.42 ns	$\leq$0.45 ns	$\leq$0.54 ns	$\leq$0.82 ns
ζ	$\geq$160 V/μs	$\geq$160 V/μs	$\geq$130 V/μs	$\geq$80 V/μs
g_m	$\geq$6.3 mhos	$\geq$11.3 mhos	$\geq$8.9 mhos	$\geq$5.24 mhos
W	1000 μm	1000 μm	900 μm	700 μm
A_{DC}	$\geq$63 dB	$\geq$54 dB	$\geq$42 dB	$\geq$31 dB
V_{sat}	$\geq$0.5 V	$\geq$0.4 V	$\geq$0.3 V	$\geq$0.2 V
THD_3	$\leq$0.0125 %	$\leq$0.032 %	$\leq$0.106 %	$\leq$0.225 %

Table 4-3 A summary of circuit requirements for the 4-2-2 bandpass sigma-delta converter

CHAPTER 5

IMPLEMENTATION

5.0 INTRODUCTION

As previously stated in Chapter 1, one goal of this work is to design a bandpass sigma-delta modulator with the peak SNR better than 62 dB for a signal bandwidth of 1.23 MHz. Towards this goal, the 4-2-2 bandpass architecture established in Chapter 4 has been implemented in a 1 μm CMOS technology with single-poly capacitors. The details of this experimental circuit are presented in this chapter.

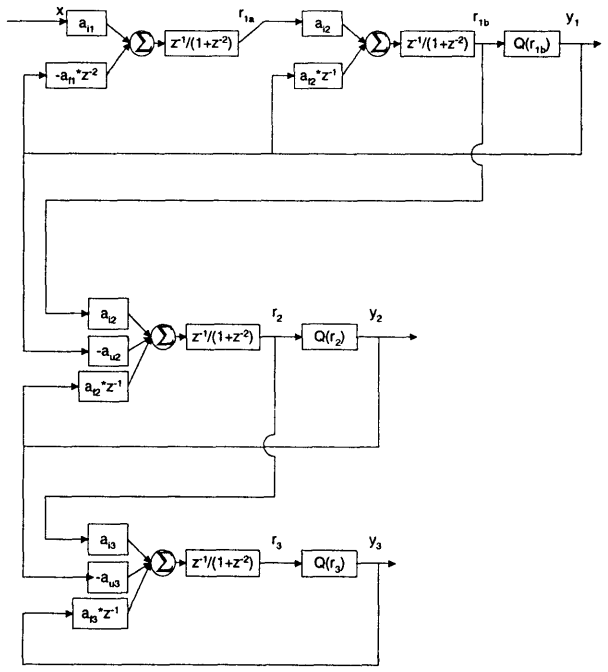


Figure 5.1 Block diagram of 4-2-2 architecture

The overall structure of the analog portion of the 4-2-2 converter was given in Figure 3.14 and is repeated here for convenience in Figure 5.1. The 4-2-2 architecture that was actually implemented in this chapter is illustrated in Figure 5.2, and the more detailed diagram of the implemented circuit topology is shown in Figure 5.3.

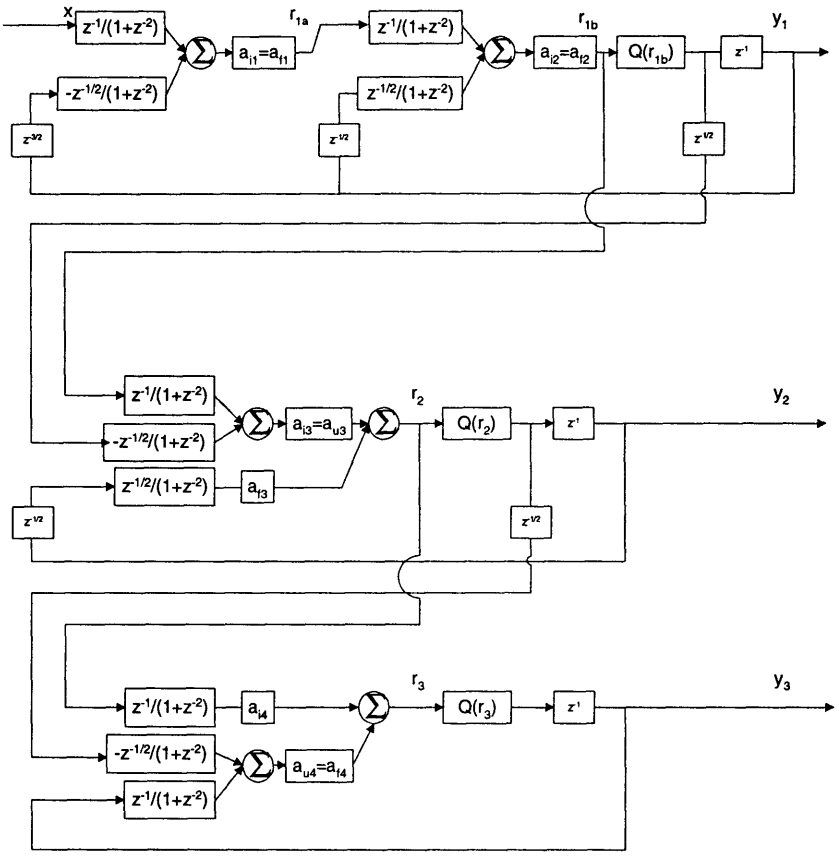


Figure 5.2 Implemented 4-2-2 architecture

The major difference between the two architectures is the slight change in timing scheme. In the actual implementation, some of the resonator inputs are clocked on the clock phase 2, rather than 1, as illustrated in Figure 5.3, which changes the transfer function of the resonator from that input to the output from the original $z^{-1}/(1+z^{-2})$ to $z^{-1/2}/(1+z^{-2})$. Consequently, $z^{-1/2}$ delays had to be added to these inputs to properly implement resonator transfer function. The idea was to reduce the effects of component mismatch and the circuit area, by implementing the ratioless subtraction using only one capacitor per subtraction, for any resonator inputs with

the same gains, namely , for the inputs 1 and 2 in the first, second and third resonator, and for the inputs 2 and 3 in the fourth resonator.

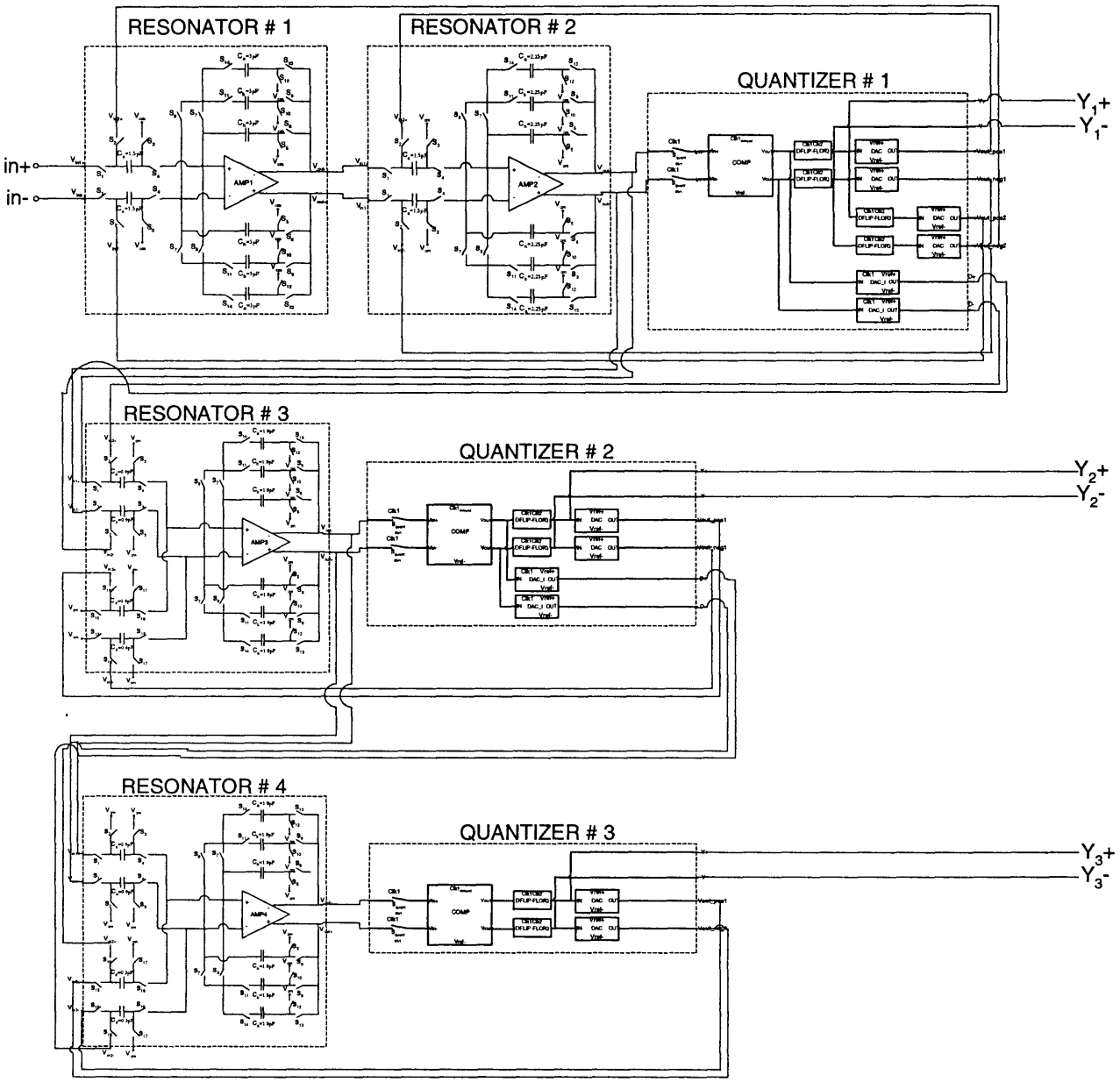


Figure 5.3 Top level diagram of the actual implementation of the 4-2-2 architecture

The principle difference between the architecture that was to be implemented, as illustrated in Figure 5.2, and the implemented circuit topology, as shown in Figure 5.3, is that the circuits in the actual implementation are fully differential. A fully differential arrangement is used because

of its immunity to switch charge injection, substrate noise, supply noise, and other common-mode disturbances [50]. The differential arrangement also doubles the effective signal voltages and slewing currents, increasing the signal power by a factor of four. The effective noise power is doubled because of the two independent signal paths, so that the net results ends up being a 3 dB increase in the dynamic range of the circuits over the single ended arrangement.

The experimental converter described in this chapter uses an oversampling ratio, M, of 16, which, according to the analyses and simulations in Chapters 3 and 4, is sufficient to reduce the quantization noise in an eight order bandpass sigma delta modulator to below the design requirements. With the signal bandwidth of 1.23 MHz, this oversampling ratio corresponds to the sampling frequency, fs, of 39.36 MHz and the sampling period, Ts, of 25.4 ns. The circuitry is operated from a single 3.3 V supply. So that the resonator inputs and outputs are centered between the power supply and ground, the circuits are designed to operate with the same input and output common-mode voltage, Vcm, of 1.65 V.

Throughout this chapter, all NMOS and PMOS MOSFETs have only three terminals explicitly shown. The fourth terminal, the substrate, of any NMOS transistors is hooked to the ground, while the PMOS transistors have the substrate always hooked to the source (this was possible since no PMOS switches were used). This terminal is therefore omitted for easier viewing.

Prior to embarking on the details of the 4-2-2 architecture implementation, the Section 5.1 briefly discusses the power reduction techniques employed, as well as the low power supply voltage implementations of the key building blocks. The next three sections, Section 5.2, Section 5.3 and Section 5.4 describe the details of the implementations of the four resonators, the three quantizers and the clock generation circuitry.

5.1 POWER REDUCTION TECHNIQUES AND LOW VOLTAGE OPERATION

In the sigma-delta converters, a major portion of the total power dissipation is from the static power dissipated in analog circuit components that require DC bias currents, such as op amp and precision comparators. The charging/discharging of sampling capacitors, clock drivers and digital circuits contribute a relatively small amount to the overall power dissipation.

In this implementation, a major effort was taken to reduce DC power dissipation, in both op-amp and comparator design. First method was to use the minimum possible size of sampling capacitors at each point in the converter, as dictated by kT/C thermal-noise considerations, discussed in the previous chapter. As a result, the op-amps in the resonators can be scaled down throughout the converter and made small in later stages to reduce power consumption, as described in the next section. This is possible since later stages can tolerate more noise due to decreasing stage resolution down the converter. Second method used to reduce power consumption was to use pseudo two-path resonators to implement fs/4 resonators, cutting the number of opamps needed by factor of two in comparison to all other reported resonator topologies [2], [30], [38], that utilize two op amps to implement the same transfer function. Third method was to use low precision dynamic comparators to implement 1 bit A/D section in each quantizer, as described in Section 5.3. Note that in this chapter, for simplicity, we use term "quantizer" for both comparator and D/A converter.

The low power supply of 3.3 V introduces two problems. First, a high-speed 3.3 V op amp with large enough voltage gain for the desired resolution is required. The solution to this problem is the op-amp described in Section 5.2.2. A second major problem is the fact that for 3.3 V power supplies, transmission gates produce a high resistance region near the mid-supply voltage due to insufficient gate drive. Namely, in standard CMOS technologies, the threshold voltage of MOSFETs (typically ~ |0.8 V|) becomes a large portion of the supply voltage, leading to problems when MOSFETs are used as switches at low voltages. For instance, assuming supply voltage of 3.3 V, the input signal voltage at the mid-point of the supply, and threshold voltage of about 1.35 V with body-effect, the gate voltage overdrive, i.e. Vgs-Vt, becomes 0.3 V. Low voltage overdrive implies high switch on-resistance, whereas the low switch on-resistance is desired. Although the large transistor switches can be used, the switch parasitic capacitance can significantly overload the output of the switched-capacitor circuits, especially in later stages where the switched-capacitor circuits are small due to the scaling . In order to solve this problem, increasing the gate overdrive is desirable to implement low on-resistance MOS switch without adding too much parasitic capacitance. There are several ways of increasing the gate voltage drive. One method is to clock boost the external reference clocks to drive all switches in the converter, but potential problems include the crosstalk to some sensitive nodes through the common clock line. Another solution, the one used in this design,

is to use a dynamic circuit to locally boost the clock drive. In this case each individual charge pump circuit drives a set of transmission gates that use the same clock to avoid the problem of crosstalk through the clock line [30]. The dynamic clock boosting circuitry is described in more detail in Section 5.4.

5.2 THE RESONATORS

The resonators are the most important components in the modulator circuit. Of the resonators, the first resonator is the most crucial. The first subsection in this section details the design of the first resonator, including the subsection on the first op amp, while the second subsection describes the remaining resonators and the op amps within them.

5.2.1 THE FIRST RESONATOR

The first resonator is the fully differential parasitic-insensitive pseudo two-path resonator whose basic operation is described in Section 4.1. A detailed schematic of the first resonator is shown in Figure 5.4. For $a_{i1}=a_{f1}=0.5$, the feedback capacitances C_h, C_a and C_b must be equal to $2C_s$, as indicated in the schematic.

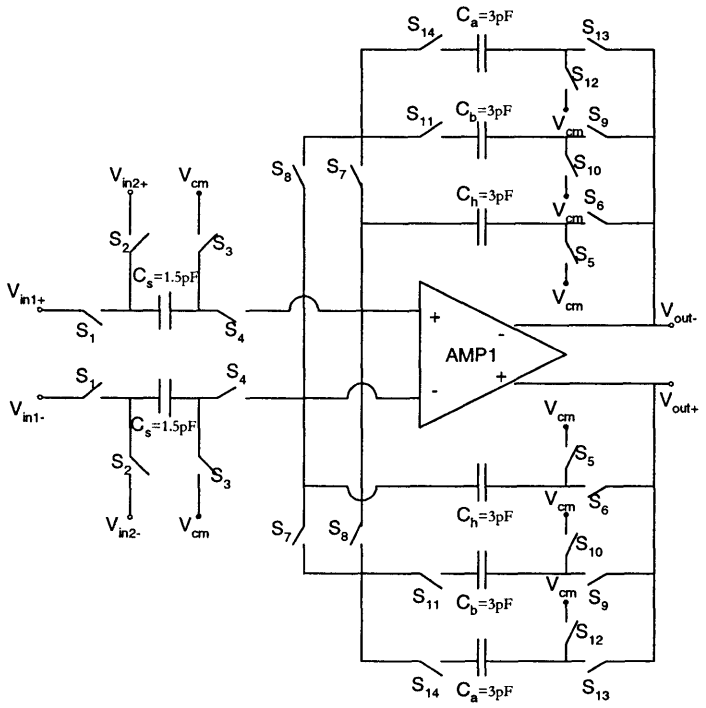


Figure 5.4 The first resonator

With the capacitances Cs, Ch, Ca and Cb known, the switches were sized so that their on-resistance does not aversely affect the settling properties of the resonator. The input switches S_1, S_2, S_5, S_{10}, S_{11}, S_{12} and S_{14} and the summing switches S_4, S_7 and S_8 affect the sampling bandwidth of the input signal forming a RC network with the sampling capacitances. The high switch on-conductance is therefore desirable, but there is a trade off between the high on-conductance on one hand and charge injection from large switches at the sampling instance on the other hand. The charge injection is not a problem for the input switches since they will be shorted out to reference voltage source. However, the amount of charge injection from the summing switches can change the input common mode voltage. The input switches S_1, S_2, S_5, S_{10}, S_{11}, S_{12} and S_{14} were sized so that the settling accuracy to the 0.069 % is still met. The summing node switches S_4, S_7 and S_8 were sized to constrain the charge injection at the sampling instance to allow the maximum change of 100 mV in the input common mode voltage. Finally, the simulations were used to determine the switch sizes for the feedback switches S_6, S_9 and S_{13}. The proper sizing of these switches is crucial, since the high on-resistance of the feedback switches can not only slow down the circuit but also make the feedback system poorly damped or unstable due to the increase in phase shift by increasing the delay and thereby reducing the phase margin. Using a too large of a feedback switch, however, adds significant amount of drain/source junction parasitic capacitance at the output reducing the overall bandwidth. Switch widths that simulations indicate are a good design compromise are summarized in Table 5-1, along with the clock phase for each switch. All gate lengths were the technology minimum of 1μm.

Switch	Phase	W (μm)
S1	1D	90
S2	2D	90
S3	1	90
S4	2	90
S5	1	90
S6	2	90
S7	1	135
S8	2	135
S9	B1	135
S10	B2	135
S11	B	135
S12	A2	135
S13	A1	135
S14	A	135

Table 5-1 Switch sizes for the first resonator

5.2.2 THE FIRST AMPLIFIER

The amplifier in the first resonator is a gain boosted version of the high speed telescopic amplifier described in Section 4.1.1. The schematic of the first amplifier is shown in Figure 5.5. In the particular technology used for the prototype modulator, the output resistance of the PMOS transistors was much worse than that of the NMOS transistor for the same bias condition. Thus the idea of using the series feedback gain-boost amplifiers [52] around the PMOS cascoded transistors to boost up their output resistance was used here, boosting the amplifier overall voltage gain from 56 dB to 63.42 dB. The single differential amplifier was used instead of two single-ended feedback amplifiers, which has the advantage of lower power consumption and improved dynamic response over the conventional technique [51]. This amplifier is capacitively coupled into the signal path using level shift capacitors C_1 and C_2 which are initialized by closing the switches S_1 and S_2. The common-mode feedback for this feedback amplifier is accomplished by a single transistor Mcmfb that senses the desired input common mode level. The common-mode feedback of the main amplifier is also capacitive through C_3 and C_4. The common-mode level is set by voltages V_{bias3} and V_{cm}, and the difference between these two voltages is sampled onto the common-mode feedback capacitors once each clock cycle through the switches S_3, S_4, S_5 and S_6.

The bias network, described in Section 5.2.5, sets the bias voltages, while the common-mode voltage, Vcm, is provided externally.

Simulated characteristics of the complete opamp at 3.3 power supply and 6.5 pF output load are summarized in Table 5-2.

Parameter	Value
DC gain	63.42 dB
Unity Gain Frequency	405.2 MHz
Phase Margin	66.76°
Slew Rate	461 V/μs
Differential Output Swing	2 V
Tail Current (Main Amplifier)	6.051 mA
Tail Current (Feedback Amplifier)	388.9 μA
Gm	0.01897 Ω^{-1}
Power Dissipation	19.97 mW

Table 5-2 Simulated characteristics of the first amplifier for 6.5 pF load capacitance

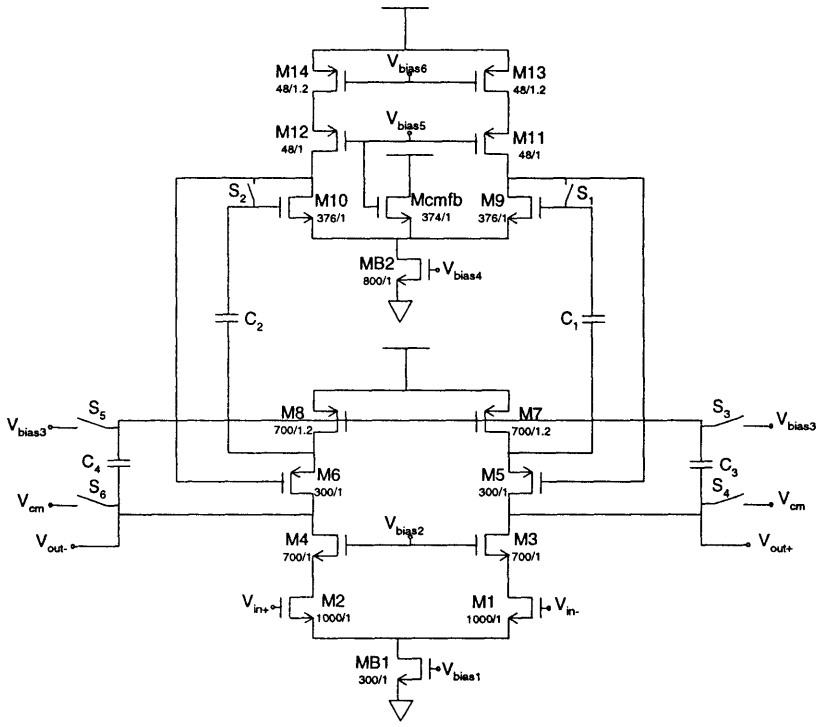


Figure 5.5 The first amplifier

The worst case settling time of the first resonator happens during the clock phase A1/B1, for the maximum input change of 1.2 differential volts, as calculated in Section 4.3.2.1.3. The worst case settling time of the first resonator was therefore simulated in Hspice using the schematic of Figure 5.6 and for the input step of 1.2 differential volts. The settling time to 0.069 % of the final value in this configuration was measured to be 8.34 ns, as shown in Figure 5.7.

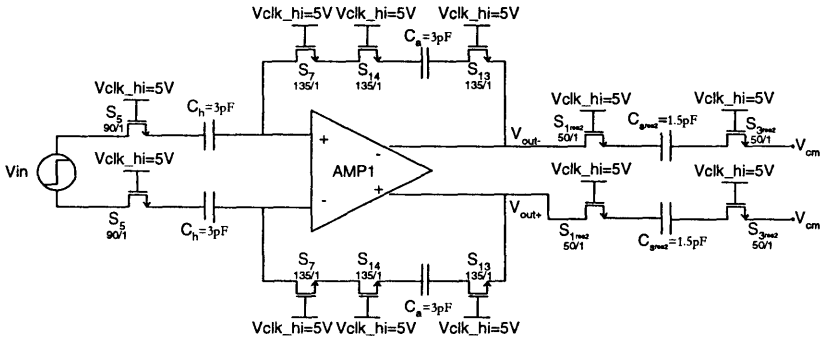


Figure 5.6 Test structure for the settling time simulations for the first resonator

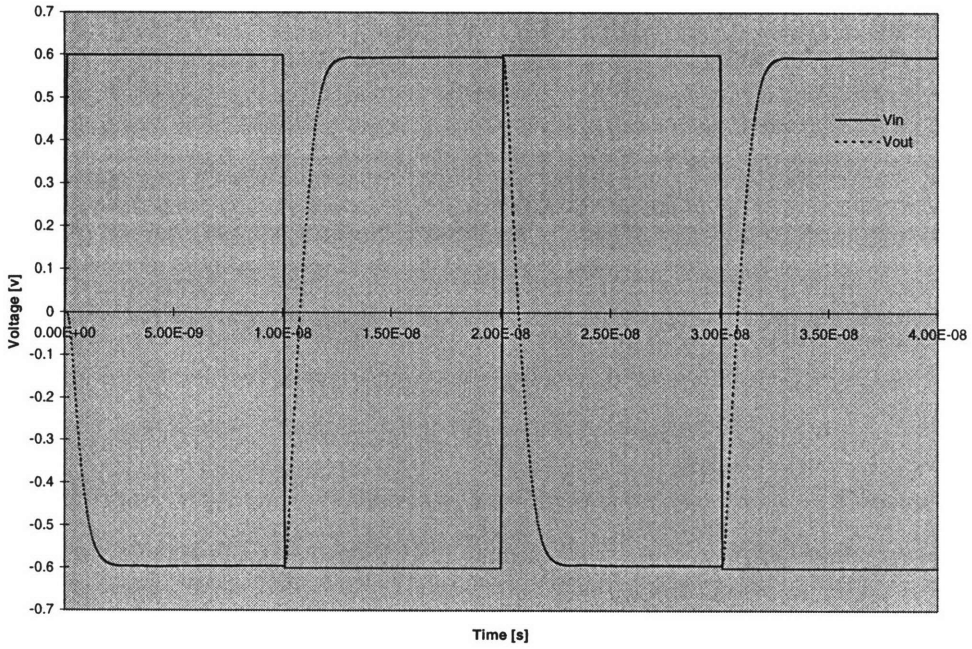


Figure 5.7 Worst case settling time simulation for the first resonator in Hspice

5.2.3 THE SECOND, THIRD AND FOURTH RESONATORS

The circuit noise generated in the resonators further down the converter gets attenuated by the noise-shaping, the stage requirements on the speed and accuracy become less stringent too. Therefore, the resonators in the later part of the converter can be scaled down by using smaller sampling capacitors and opamps, resulting in the optimization of the power dissipation. As a result, the first, second, third and fourth resonators are all versions of the fully differential pseudo two-path resonator whose basic operation is detailed in 4.3.2.1.3. The second, third and fourth resonators are scaled down versions of the first resonator, as prescribed by the analysis detailed in the previous chapter. A detailed schematics of the second, third and fourth resonators are shown in Figure 5.8, Figure 5.9 and Figure 5.10 and, respectively.

The second resonator has two inputs and since $a_{i2}=a_{f2}=2/3$, they are implemented using one input sampling capacitor C_s. The feedback capacitances C_h, C_a and C_b must be equal to $1.5C_s$, as indicated in the schematic.

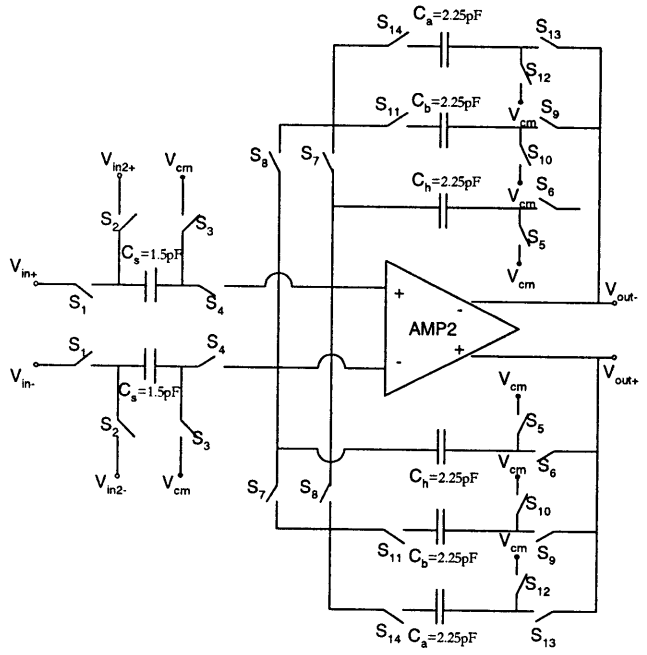


Figure 5.8 The second resonator

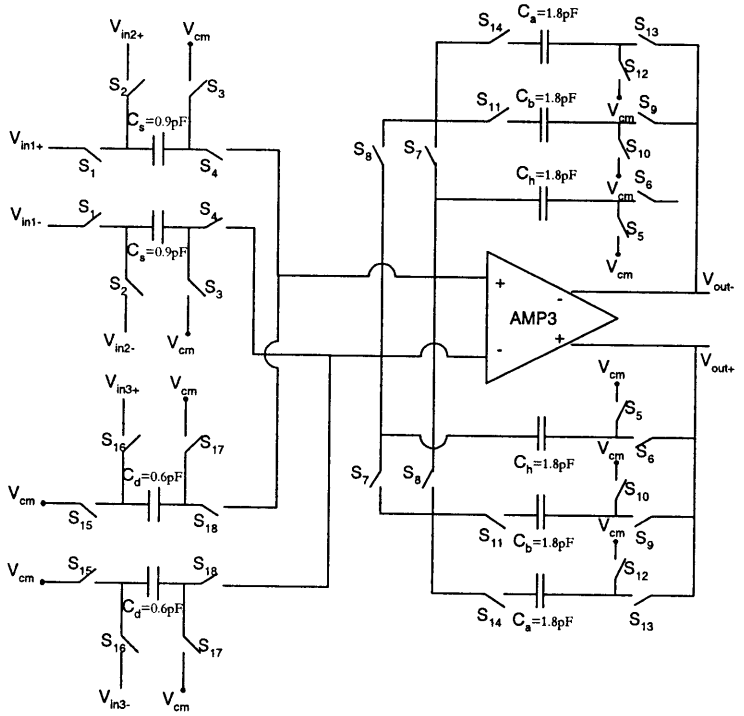


Figure 5.9 The third resonator

The third resonator has three inputs. Since $a_{i3}=a_{u3}=0.5$, the first two inputs are implemented using the same input sampling capacitor, $C_s=0.9$ pF. Since $a_{f3}=1/3$, the third requires a

separate sampling capacitor, C_d=0.6 pF. The feedback capacitances C_h, C_a and C_b must be equal to $2C_s$ and $3C_d$, as indicated in the schematic.

Similarly, the fourth resonator has three inputs. Now $a_{u4}=a_{f4}=1/6$, so that the second and the third inputs are implemented using the same input sampling capacitor, C_d=0.3 pF. Since $a_{i4}=1/2$, the first input requires a separate sampling capacitor, C_s=0.9 pF. The feedback capacitances C_h, C_a and C_b must be equal to $6C_s$ and $2C_d$, as indicated in the schematic.

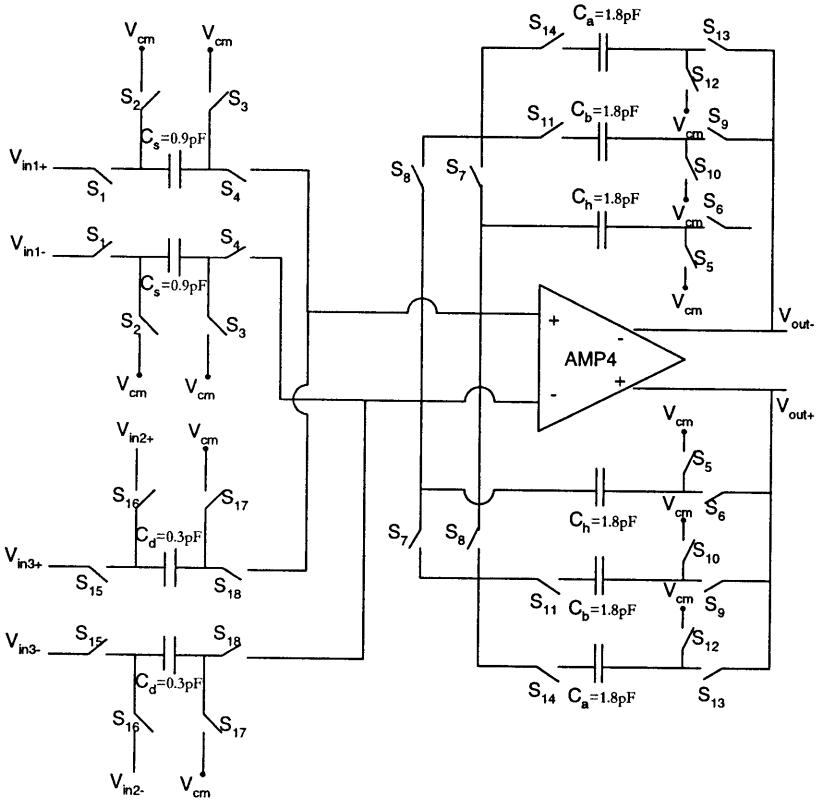


Figure 5.10 The fourth resonator

The switches were sized so that their on-resistance does not adversely affect the settling properties of the resonator, much in the same manner employed in the sizing of the switches in the first resonator. The input switches S_1, S_2, S_5, S_{10}, S_{11}, S_{12} and S_{14} in all three resonators and the additional input switches S_{15}, S_{16} and S_{17} in the third and fourth resonators were sized so that the desired settling accuracy to the 0.2 %, 0.78 % and 2.91 % is achieved in the three resonators respectively. The summing node switches S_4, S_7 and S_8 in all three resonators plus the additional summing switch S_{18} in the third and the fourth resonator were sized to constrain

the charge injection at the sampling instance to allow the maximum change of 100 mV in the input common mode voltage. Finally, the simulations were used to determine the switch sizes for the feedback switches S_6, S_9 and S_{13}. Switch widths that simulations indicate are a good design compromise are summarized in Table 5-3, Table 5-4 and Table 5-5, along with the clock phase for each switch. All gate lengths were the technology minimum of 1μm.

Switch	Phase	W (μm)
S1	1D	50
S2	2D	50
S3	1	50
S4	2	50
S5	1	30
S6	2	20
S7	1	50
S8	2	50
S9	B1	100
S10	B2	100
S11	B	100
S12	A2	100
S13	A1	100
S14	A	100

Table 5-3 Switch sizes for the second resonator

Switch	Phase	W (μm)
S1	1D	50
S2	2D	90
S3	1	50
S4	2	20
S5	1	50
S6	2	90
S7	1	50
S8	2	20
S9	B1	90
S10	B2	90
S11	B	90
S12	A2	90
S13	A1	90
S14	A	90
S15	1D	50
S16	2D	90
S17	1	50
S18	2	20

Table 5-4 Switch sizes for the third resonator

Switch	Phase	W (µm)
S1	1D	50
S2	2D	50
S3	1	50
S4	2	15
S5	1	50
S6	2	90
S7	1	50
S8	2	40
S9	B1	90
S10	B2	90
S11	B	90
S12	A2	90
S13	A1	90
S14	A	90
S15	1D	50
S16	2D	50
S17	1	50
S18	2	15

Table 5-5 Switch sizes for the fourth resonator

5.2.4 THE SECOND, THIRD AND FOURTH AMPLIFIERS

The amplifiers for the second, third and fourth resonators are of identical topology, and are simply scaled versions of the main high speed telescopic amplifier in the first resonator, with the devices sizes as given in Table 5-6, Table 5-7 and Table 5-8, respectively.

MOSFET	M1	M2	M3	M4	M5	M6	M7	M8	MB1
W [µm]	1000	1000	700	700	500	500	510	510	1000
L [µm]	1	1	1	1	1	1	1.2	1.2	1

Table 5-6 Transistor sizes for the second amplifier

MOSFET	M1	M2	M3	M4	M5	M6	M7	M8	MB1
W [µm]	900	900	300	300	100	100	365	365	690
L [µm]	1	1	1	1	1	1	1.2	1.2	1

Table 5-7 Transistor sizes for the third amplifier

MOSFET	M1	M2	M3	M4	M5	M6	M7	M8	MB1
W [µm]	700	700	150	150	100	100	160	160	450
L [µm]	1	1	1	1	1	1	1.2	1.2	1

Table 5-8 Transistor sizes for the fourth amplifier

The quiescent tail currents in the second, third and fourth amplifiers are 4.32 mA, 2 mA and 952.4 μA, respectively. Because the capacitances in the second, third and fourth resonator are much smaller than those in the first resonator, the scaled amplifiers still exceed the speed and slew requirement specified at the end of the previous chapter. Simulated characteristics of the three opamps at power supply of 3.3 V and the output loads of 5.3 pF, 4.8 pF and 4.3 pF are given in Table 5-9, Table 5-10 and Table 5-11. The worst case settling time of the second, third and fourth resonators happens during the clock phases A1/B1, for the maximum input change of 1.4, 1.2 and 0.52 differential volts, respectively, as discussed in Section 4.3.2.1.3. The worst case settling time of the second, third and fourth resonators were therefore simulated in Hspice using the test structures shown in Figure 5.11, Figure 5.13 and Figure 5.15, and for the input steps of 1.4, 1.2 and 0.52 differential volts, respectively. The settling time to desired accuracy for the second, third and forth resonator (0.2 %, 0.78 % and 2.9 % of the final value, respectively) in these configurations was measured to be 8.16 ns, 4.18 ns and 3.34 ns, respectively, as shown in Figure 5.12, Figure 5.14 and Figure 5.16.

Parameter	Value
DC gain	55.95 dB
Unity Gain Frequency	400.1 MHz
Phase Margin	63.02°
Slew Rate	407 V/μs
Differential Output Swing	2.4 V
Tail Current	4.319 mA
Gm	0.0161 Ω^{-1}
Power Dissipation	14.25 mW

Table 5-9 Simulated characteristics of the second amplifier for 5.3 pF load capacitance

Parameter	Value
DC gain	49.96 dB
Unity Gain Frequency	284.6 MHz
Phase Margin	62.69°
Slew Rate	208 V/μs
Differential Output Swing	2.8 V
Tail Current	2 mA
Gm	0.01039 Ω^{-1}
Power Dissipation	6.6 mW

Table 5-10 Simulated characteristics of the third amplifier for 4.8 pF load capacitance

Parameter	Value
DC gain	59.44 dB
Unity Gain Frequency	182.3 MHz
Phase Margin	65.1°
Slew Rate	110 V/μs
Differential Output Swing	3.2 V
Tail Current	952.4 μA
Gm	0.00632 Ω^{-1}
Power Dissipation	3.14 mW

Table 5-11 Simulated characteristics of the fourth amplifier for 4.3 pF load capacitance

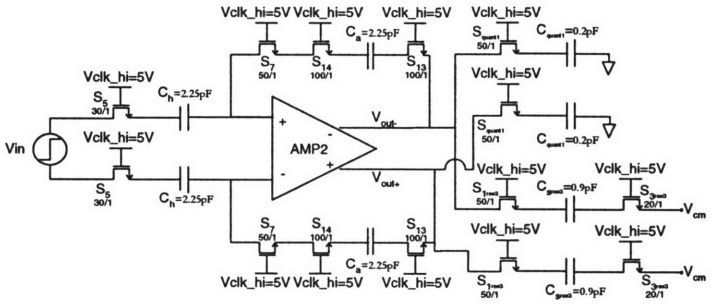


Figure 5.11 Test structure for the settling time for the second resonator

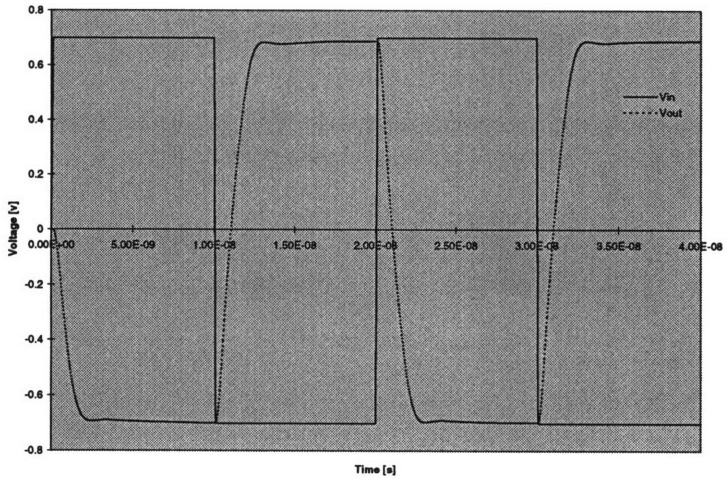


Figure 5.12 Worst case settling time simulations for the second resonator in Hspice

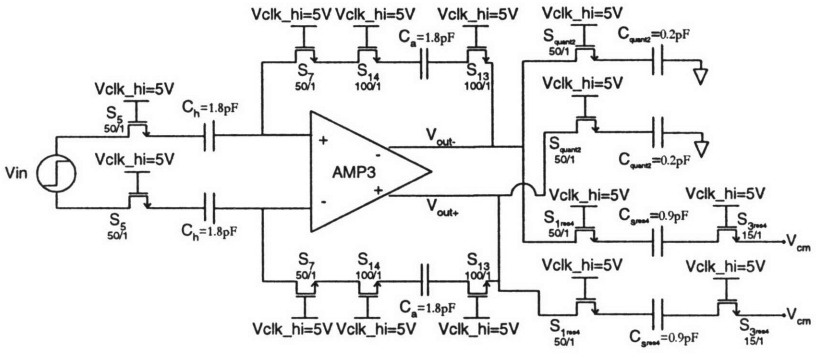


Figure 5.13 Test structure for the settling time simulations for the third resonator

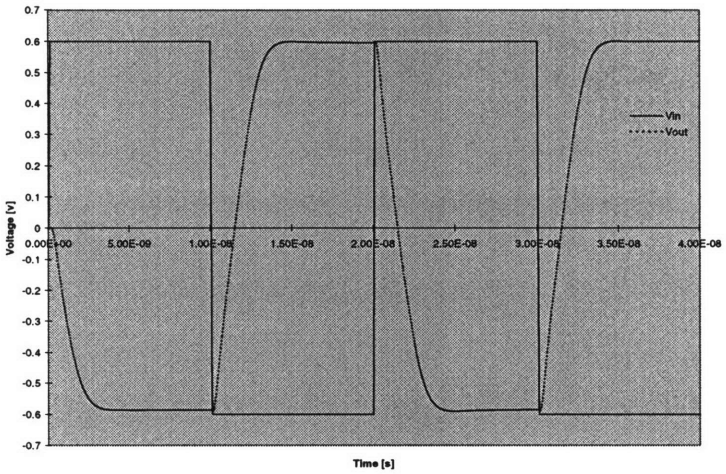


Figure 5.14 Worst case settling time simulation for the third resonator in Hspice

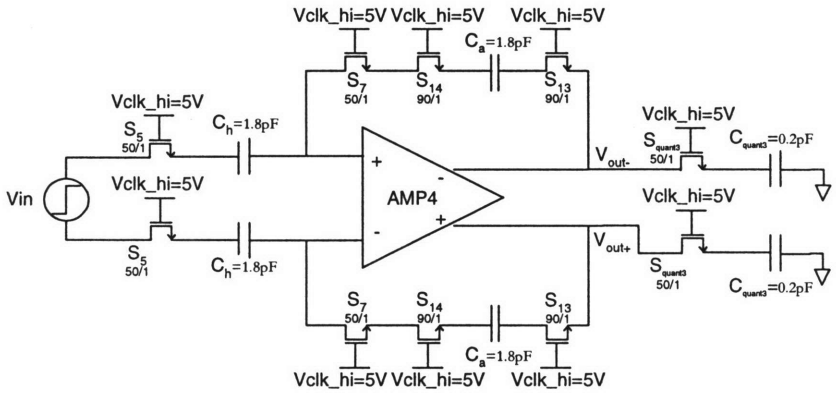


Figure 5.15 Test structure for the settling time simulations for the fourth resonator

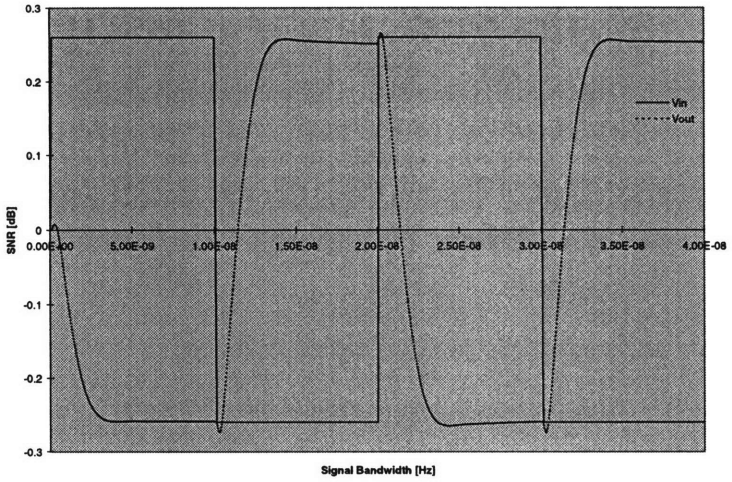


Figure 5.16 Worst case settling time simulations for the fourth resonator in Hspice

5.2.5 OP AMP BIAS CIRCUITRY

In the prototype, one master bias current produces several reference currents by current mirrors, and they are distributed to the op amp bias circuits as shown in Figure 5.17. Currents are distributed instead of the gate voltage V_{gs} of the master current source. This is because the finite resistance of the supply line can produce small voltage drop which can change the V_{gs} of the current source and in turn can alter the current value. For instance, if the voltage drop is 5 mV and Vgs -Vt of the current source is 100 mV, the difference can cause about 10 % change in current under the assumption of the square law device characteristics. If currents are distributed instead, this problem can essentially be eliminated by generating necessary gate voltages locally from the reference current, and the voltage drop can be minimized.

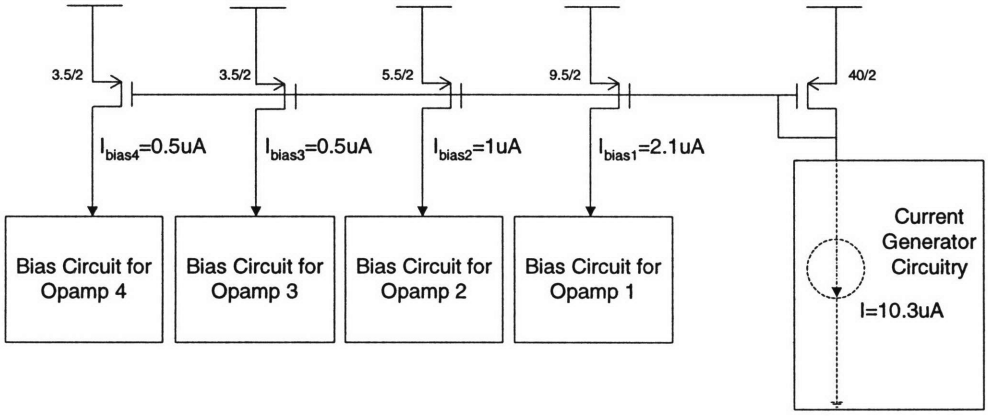


Figure 5.17 The distribution of bias currents from the master current source

The master current generator circuitry is a bandgap referenced current source [51] shown in Figure 5.18. Figure 5.19 shows the bias circuits used for the four op amps.

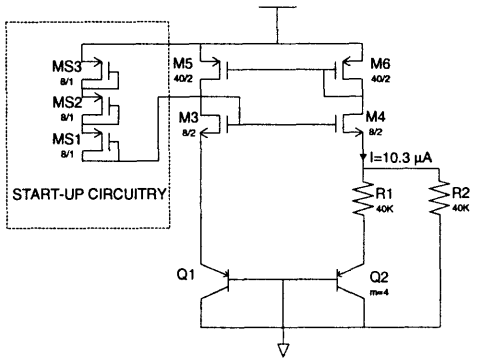


Figure 5.18 the master current generator circuitry

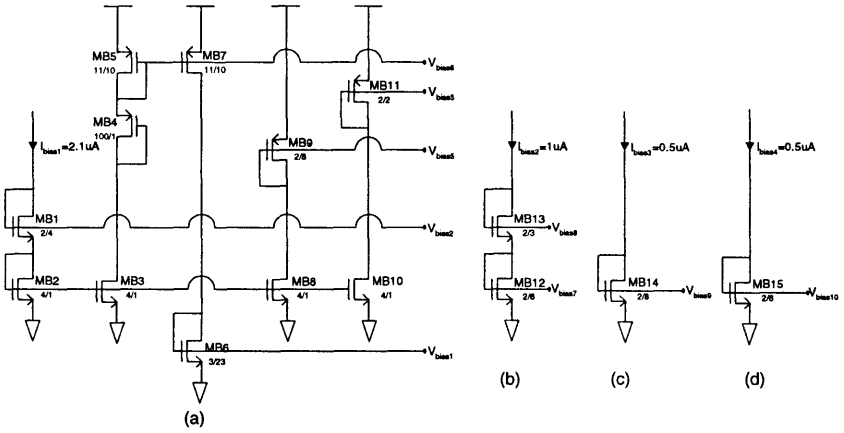


Figure 5.19 Op amp bias circuit

The total power dissipated in the op amp bias circuitry is 105.83 μW.

5.3 THE QUANTIZERS

A quantizer in sigma-delta converter has two main functions. First, it digitizes the analog input, producing the digital output . Second, it converts back the digitized signal to the analog signal that is then fed back into the converter for the corrective action. In this converter, quantizers have a third function too. To properly implement the chosen transfer function, the quantizers also need to delay their analog outputs, in accordance with the Figure 5.2.

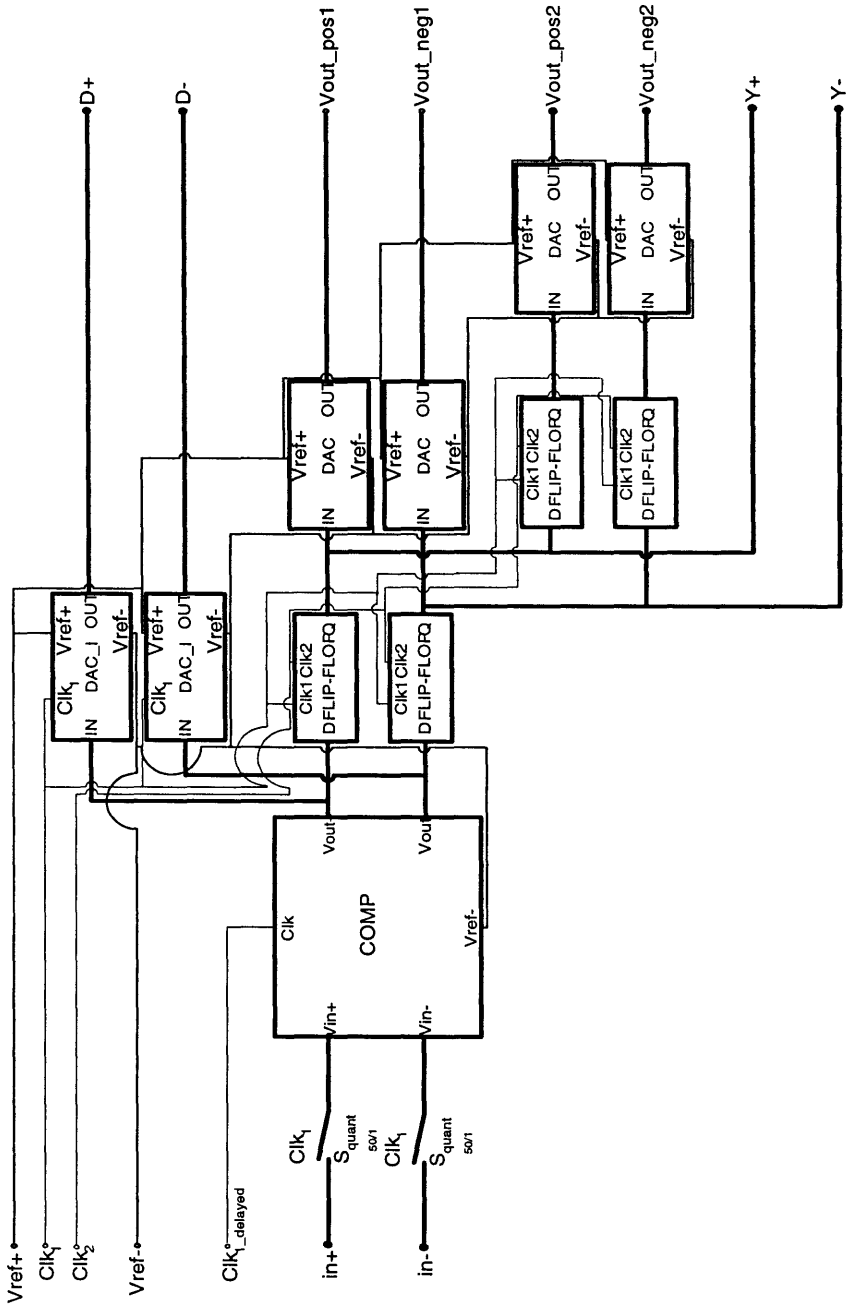


Figure 5.20 Block diagram of the first quantizer

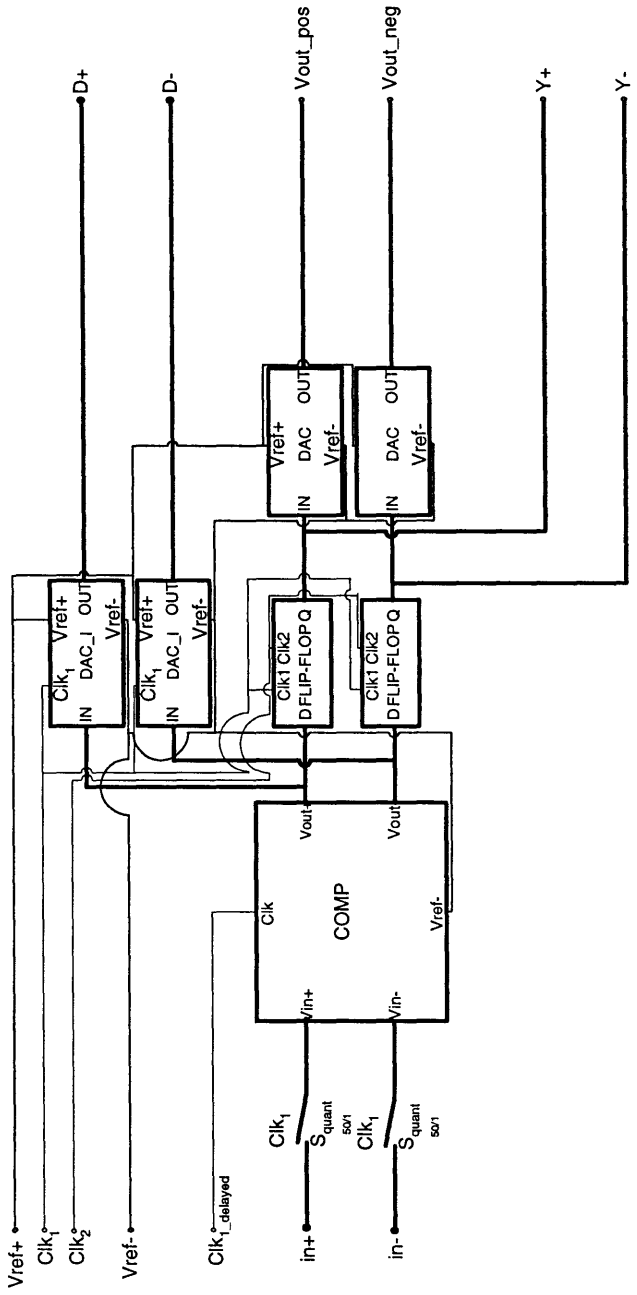


Figure 5.21 Block diagram of the second quantizer

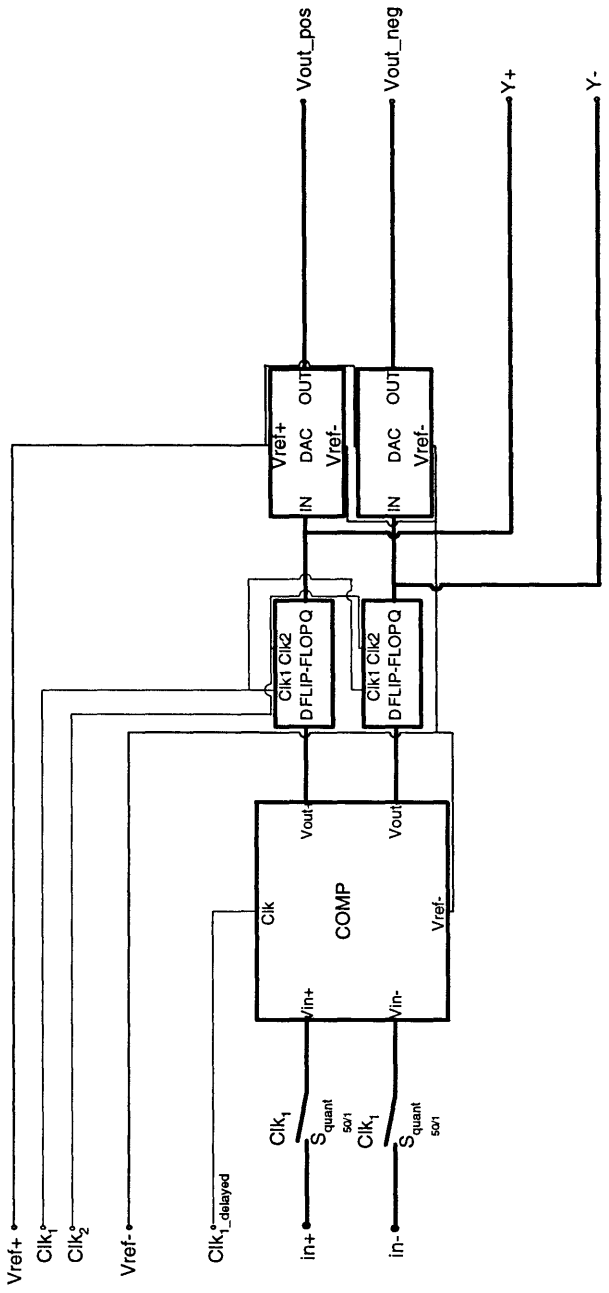


Figure 5.22 Block diagram of the third quantizer

The core circuitry of the three quantizers is therefore essentially the same and consists of a differential comparator that digitizes the input analog signal, the flip-flops that delay the outputs of the comparator, and the D/A converters that produce the corrective differential analog outputs. The number of flip-flops varies, depending on the number of delays needed. The number of the analog outputs is different, too. The detailed block diagrams of the quantizers are given in Figure 5.20, Figure 5.21 and Figure 5.22.

The first quantizer, shown in Figure 5.20, generates three versions of the analog output, the output D available a clock phase after the comparator decision has been made, Vout_1 a clock cycle later and Vout_2 another clock cycle later. The output D is fed to the third resonator in the next stage, while Vout_1 and Vout_2 are being fed back into the first and second resonators of the first stage, as shown in Figure 5.3. The only deviations from the timing as described in Figure 5.1 is that they are fed to the inputs that are sampled during the clock phase 2, so that they are all available on the clock phase 2 rather than clock phase 1. Similarly, the second quantizer has two analog outputs, the output D, which is fed to the fourth resonator in the next stage, while Vout_1 is being fed back into the third resonators of the second stage, and finally, the third quantizer has only one analog output Vout_1 being fed back to the fourth resonator.

A schematic diagram of the differential comparator [30] used is shown in Figure 5.23. According to the behavioral analysis from the previous chapter, results of which are summarized in Section 4.5, the offset of Vref/35 can be tolerated for the converter's desired worst case resolution of 62 dB. So, without the use of a power sinking pre-amp usually required to amplify the signal before an accurate comparison is made in a high resolution A/D converters, a simple dynamic differential latch can implement the low resolution comparator, that will in this sigma-delta converter suffice to realize a high resolution A/D converter, removing the dc power dissipation. The lower set of NMOS devices connected to the input and to the reference in Figure 5.23, namely M1, M2, M3 and M4, operate in the triode region. As the upper cross-coupled inverter-latch regenerates when the latch clock, CLK, goes high, the drain currents of the active switching NMOS devices are steered to obtain the final state determined by the mismatch in the total resistance. In this case, the resistances of NMOS pairs biased in triode region are given to the first order by

$$R_1 = \frac{1}{k' \cdot \left[\frac{W_1}{L} \cdot (Vin_+ - V_t) + \frac{W_2}{L} \cdot (Vin_- - V_t) \right]} \text{ and}$$

Equation 5-1

$$R_2 = \frac{1}{\mu \cdot C_{ox} \cdot \left[\frac{W_1}{L} \cdot (Vin_- - V_t) + \frac{W_2}{L} \cdot (Vin_+ - V_t) \right]}.$$

Equation 5-2

When the latch clock , CLK is brought low, the comparator is reset forcing its single-ended output nodes, $Vout_+$ and $Vout_-$, to Vdd.

The input voltage which causes R1 equal to R2 is equal to the comparator threshold voltage. From Equation 5-1 and Equation 5-2, the comparator threshold voltage is given by

$$Vin|_{threshold} = \frac{W_2}{W_1} \cdot V_{ref}$$

Equation 5-3

where $Vin=Vin_+-Vin_-$ and $Vref=Vref_+-Vref_-$. Therefore, arbitrary decision levels can be set by properly ratioing the triode region devices widths, W_2 and W_1, without the use of any resistive reference voltage divider, sampling capacitors, buffers, switching transistors, and all parasitics associated with these devices at the input. In this implementation, the ratio of the triode region devices is set to 1/35 to generate comparator decision levels at $\pm$ Vref/35. Because the comparator is clocked and dynamic, a decision is made at the rising edge of the latched clock, CLK. Any signal difference at this point will trigger an output change. This process is irreversible until the next clock edge. Care must be taken to ensure that the inputs have completely settled and no charge gets injected into inputs at the time of decision, so as to avoid force latching. The NMOS switches $Scomp_1$ and $Scomp_2$ are inserted at the input of the comparator and switched at clock 1, to make sure that the inputs to the comparator are stable

and are not changing for 2 ns prior to comparator being strobed, i.e prior to the comparator latch clock CLK=$1_{delayed}$ going high. All loading and switching on the comparator is symmetric, to avoid any charge injection at the time of decision.

A disadvantage of this comparator is its limited input common-mode range. As either single-ended input approaches Vt, the input transistors approach end eventually enter cut-off. This limits the single-ended input to about a volt from the ground, and since the differential common voltage is set at Vdd/2, here 1.65 V, it further limits the input single-ended signal to about volt from the Vdd. In this particular implementation, however, the highest input swing is for the comparator in the first quantizer, and is equal to the output swing of the second resonator, 0.4 volts from the differential common-mode voltage, which is still within the comparators input common-mode range.

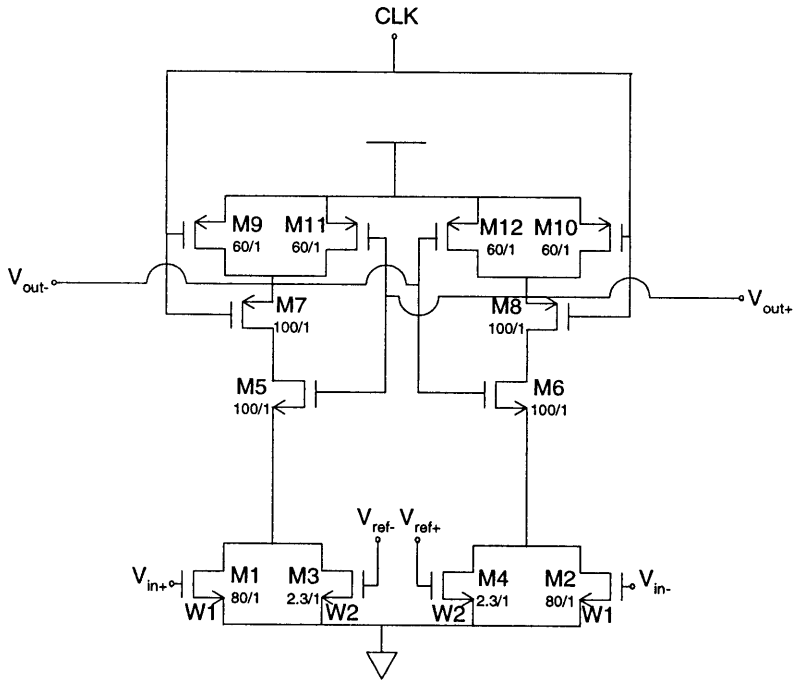


Figure 5.23 The differential comparator

The output of the comparator is fed to two different branches producing the three analog outputs, D, Vout_1 and Vout_2. To generate the first analog differential output D, the output of the comparator is fed to two interstage D/A converter, schematic of one of which is shown in Figure 5.24.

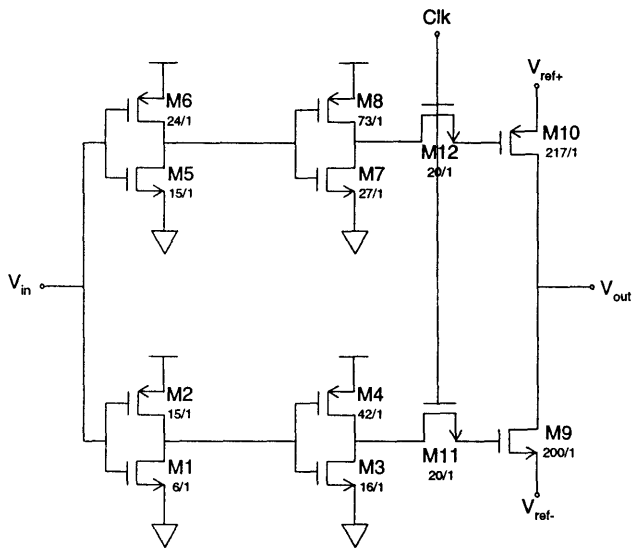


Figure 5.24 The inter-stage feedback D/A converter

In this circuit, transistors M9 and M10 act as switches between the analog output, V_{out}, and the positive and negative reference voltages, Vref+ and Vref-, set to Vcm $\pm$ 0.35 V, that is at 2 V and 1.3 V, respectively. These devices are sized so that in the worst case, together with the RC network formed by the input switching transistor and input sampling capacitors of the first resonator, allow the settling time constant to be short enough to meet the settling accuracy of the first resonator. The gates of M9 and M10 are independently driven by two inverter buffers that buffer the comparator output from the large gate capacitances of M9 and M10. These two inverter buffers are sized according to the multiply-by-e rule for the maximum switching speed. As previously mentioned, the analog output D, i.e. the output Vout in this circuit, need to be available at the clock phase 2 after the clock phase $1_{delayed}$ in which the comparison decision was made. During the clock phase 2, however, the comparator clock, $1_{delayed}$, will be low, and the comparator outputs will be reset to the Vdd. The switching transistors M11 and M12, clocked at the clock phase 1 are therefore inserted before the gates of M9 and M10, to make sure that the M9 and M10 are switched by the comparator decision made during 1delayed rather then by the comparator outputs during the reset state. The comparator is sized to be fast enough that the entire comparator-inter-stage D/A subsystem settles before the clock phase 1 finishes and clock phase 2 starts, properly implementing the desired $z^{-1/2}$ function.

To generate the second analog output, Vout_1, the comparator output is also fed to two identical dynamic flip-flops, delaying it for a clock cycle, and then to the feedback D/A converter. The dynamic flip-flop [57] in Figure 5.25 is chosen for this

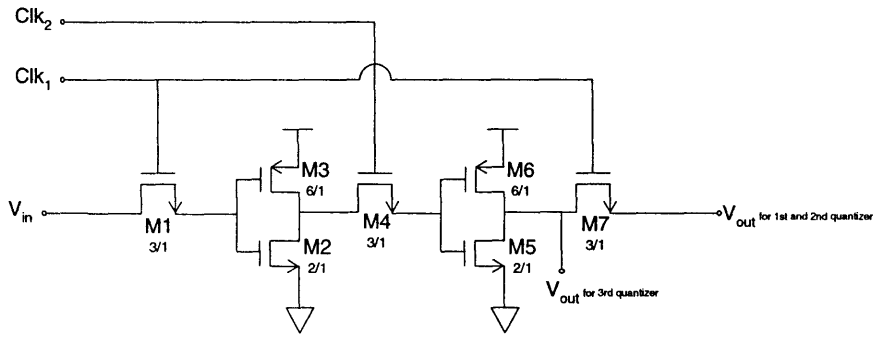


Figure 5.25 The dynamic flip-flop

implementation for three reasons. It is dynamic, removing a dc power dissipation, it is simple in terms of circuitry, and together with the comparator and the feedback A/D converter, it properly implements $z^{-3/2}$ function indicated in Figure 5.2. Namely, it latches its inputs on the rising edge of clock phase 2, so that it allows the comparator decision to be made during clock phase 1delayed, and the outputs are available during the next clock phase 1, and are still held available during the clock phase 2 after, allowing enough time the signal to propagate through the feedback D/A converter during clock phase 1 and be ready and stable to be locked at during clock phase 2.

Note that in the third quantizer, the output Vout_1 is clocked at clock phase 1, unlike in the first two quantizers, where this ouput gets clocked on clock phase 2. Consequently, the need for the switch M7 is eliminated, and Vout is taken from the output of inverter formed by transistors M5 and M6, as illustrated in Figure 5.25.

The feedback D/A converter, [36] shown in Figure 5.26, is essentially the same as the inter-state D/A converter. The gates of the switching transistors M9 and M10 are held to the proper value during the clock phase 2 by the flip-flop, eliminating the need for the switches present in the inter-state D/A converter. Another difference is that the two inverter-buffers driving the gates of switching transistors M9 and M10 are sized not only to buffer the flip-flop output

from the large gate capacitance of M9 and M10, but also to never allow M9 and M10 to conduct simultaneously, reducing the power dissipation further. Specifically, M1 and M2 are sized so that a falling edge at the D/A converter's input voltage, Vin, propagates faster than the a rising edge, and M5 and M6 are sized so that a rising edge at Vin propagates faster than a falling edge.

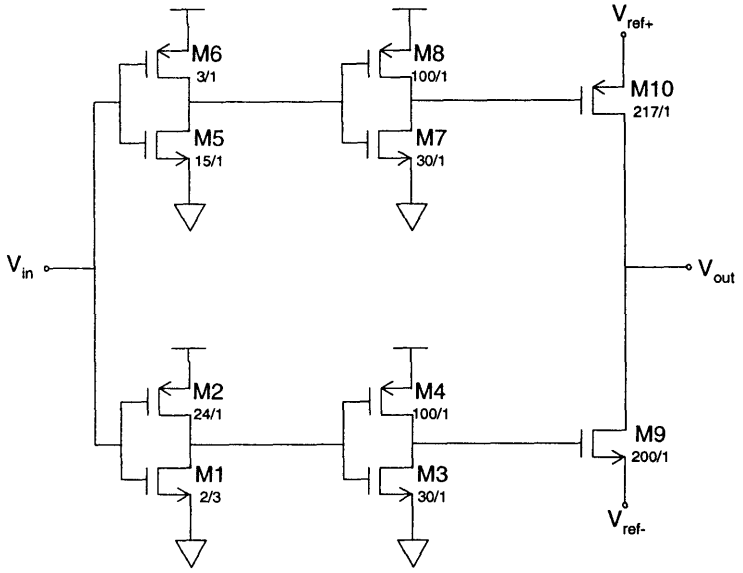


Figure 5.26 The feedback converter

The outputs of the flip-flops are also fed to another set of the same flip-flops, providing additional delay, and feedback D/A converters, forming the third comparator-two-flip-flops-feedback-D/A-converter sub-system that provides the third output Vout_2 with the necessary $z^{-5/2}$ of the delay.

To illustrate the proper functioning of the quantizer, the simulation results showing the clocks, the input and output signals for the first quantizer are included in Figure 5.27.

Simulations indicate that operating at the power supply of 3.3 V and the clock frequency of 39.96 MHz, the three comparator in the quantizer dissipate about 2 mW, the eight flip-flops dissipate about 10 μW, the eight feedback D/A converters dissipate about 0.924 mW, and the four inter-stage D/A converters dissipate about 1.584 mW, for the total of 4.52 mW of power dissipation in all three quantizers.

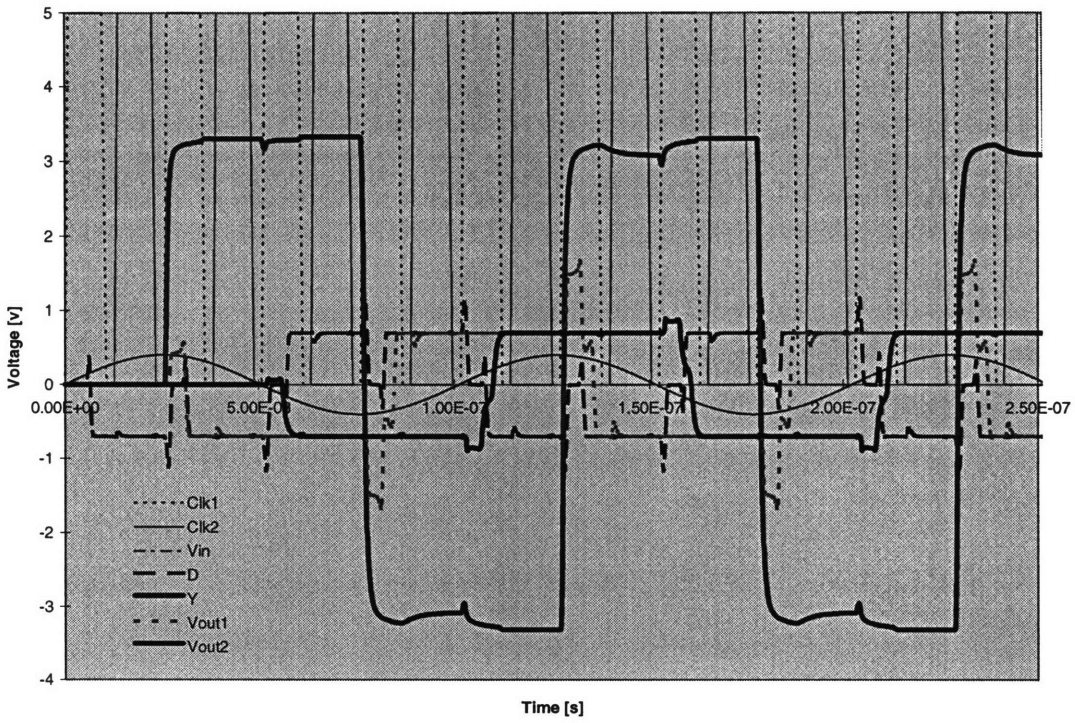


Figure 5.27 Test simulation for the first quantizer

5.4 CLOCK GENERATION CIRCUITRY

The remaining building block in the modulator is the clock generation circuitry. There are eight different clocks required for the operation of the pseudo two path resonators, clocks 1, 2, A, B, A1, A2, B1 and B2, as described in Section 4.1. Two delayed clocks were added, 1D and 2D, to operate switches S_1 and S_2, in order to ensure that there is no signal dependent charge injection integrated onto the sampling capacitors [53]. Another delayed clock is added, the clock $1_{delayed}$, in order to ensure proper functioning of the comparators in the quantizers, as described in Section 5.3. The required waveforms are shown in Figure 5.28.

The circuitry that generates these waveforms, illustrated in Figure 5.29, consists of four components: a non-overlapping clock generator circuit for clocks A and B, a non-overlapping clock generator circuit for clocks 1, 2, 1D, 2D and $1_{delayed}$, a clock generator circuit for clocks A1, A2, B1 and B2, and eleven clock boosting circuits, one for each clock. The two inputs to the clock generation circuitry are two external clocks, one 19.68 MHz and the other 39.36 MHz, both with 50 % duty cycle, 0.5 ns rise and fall times, and with aligned positive edges.

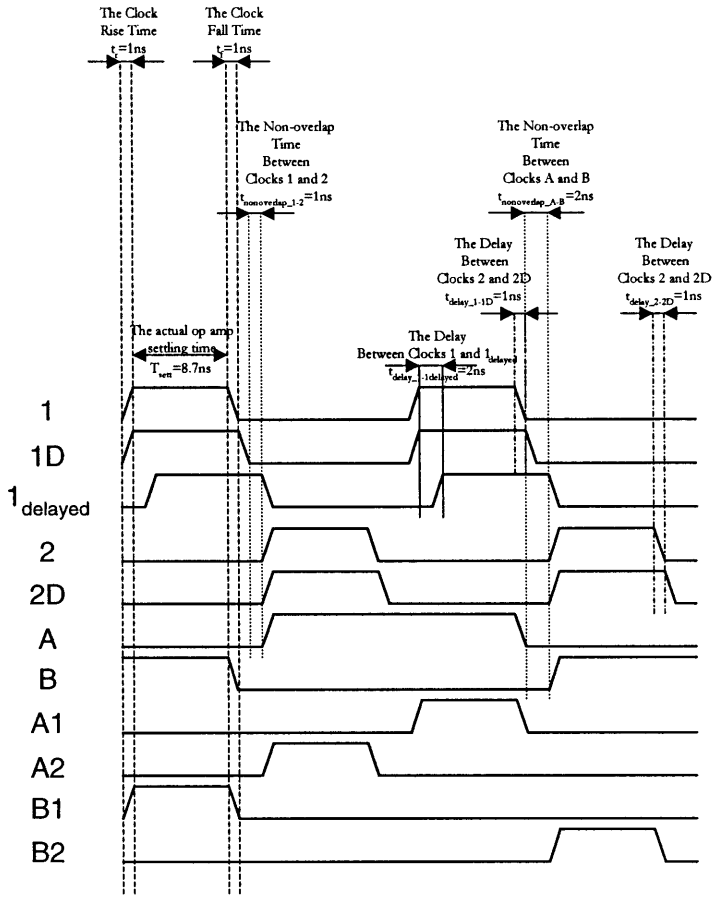


Figure 5.28 Clock waveforms for the bandpass sigma-delta A/D operation

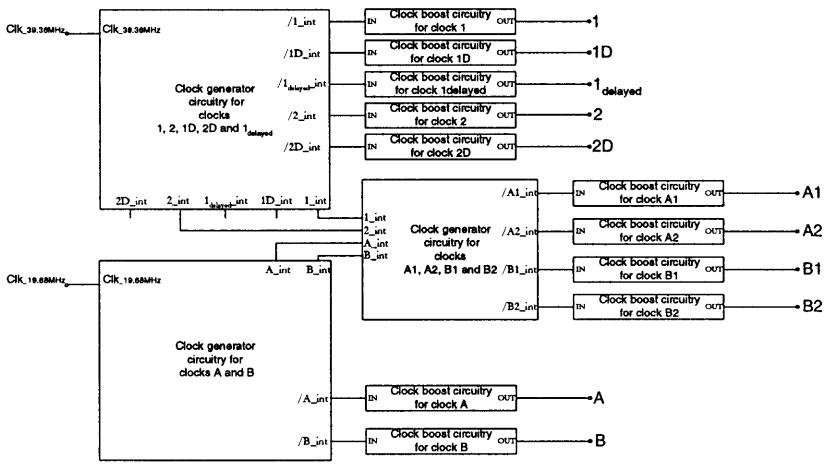


Figure 5.29 Clock generation circuitry

The clock generation circuitry for clocks A and B, illustrated in Figure 5.30, is a typical non-overlapping clock generation circuitry. An external 19.68 MHz clock, Clk_19.68MHz, drives a cross-coupled pair of NAND gates. The cross coupling network uses inverter chains to generate delays. The non-overlapping clocks are generated as follows. Consider the case when the signal A_int is high, and the signal B_int is low. When the external clock, Clk_19.68MHz, transitions from high to low, A_int is forced low, while B_int remains temporarily low, because one of the inputs to the NAND in the lower branch is still low. After seven inverter delays, the change in A_int propagates to the input of the NAND in the lower branch, and B_int goes high. Because of these inverter delays, A_int and B_int are never simultaneously high, and are therefore non-overlapping, as desired.

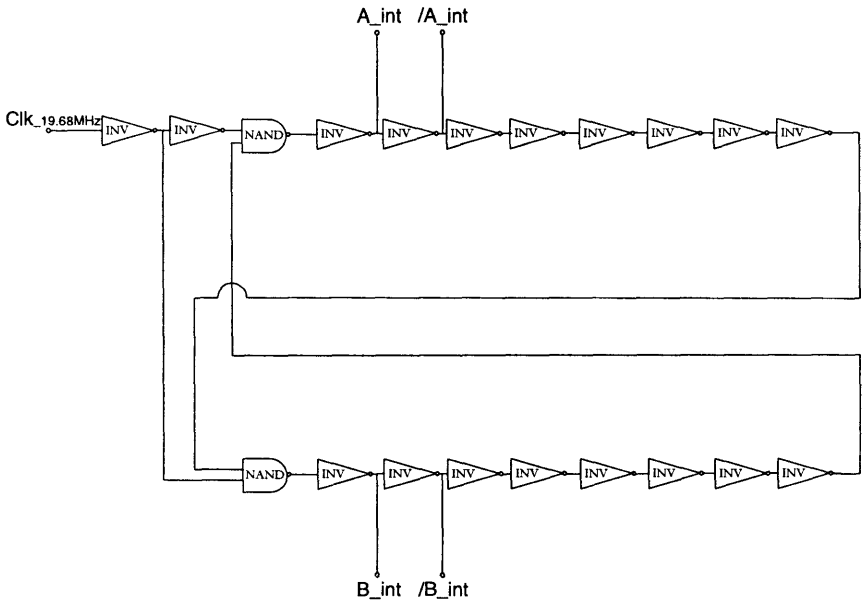


Figure 5.30 Non-overlapping clock generation circuitry for clocks A and B

The clock generation circuitry for clocks 1, 2, 1D, 2D and $1_{delayed}$ is illustrated in Figure 5.31. It is again a typical non-overlapping clock generation circuitry, slightly modified to include the delayed clocks 1D, 2D and $1_{delayed}$. An external 39.36 MHz clock, Clk_39.36MHz, drives a cross-coupled pair of NAND gates, and again, the cross-coupling network uses the inverter chains to generate delays.

Parts of the inverter delay chains were modified so that the delayed clocks 1D_int and 2D_int could be lined up with the early clocks 1_int and 2_int, respectively, at their rising edges. This was done by bypassing the delay chains with transistors M1, M2, M3 in the upper branch, and the transistors M4, M5, M6 in the lower branch, to reset the internal nodes and in turn to line up the rising edges of the clocks 2_int and 2D_int, and the clocks 1_int and 1D_int, respectively. Falling edges are again created by the inverter chain delay action. The additional clock, $1_{delayed}$ is generated, simply by delaying clock 1_int, using the inverter chain delay action.

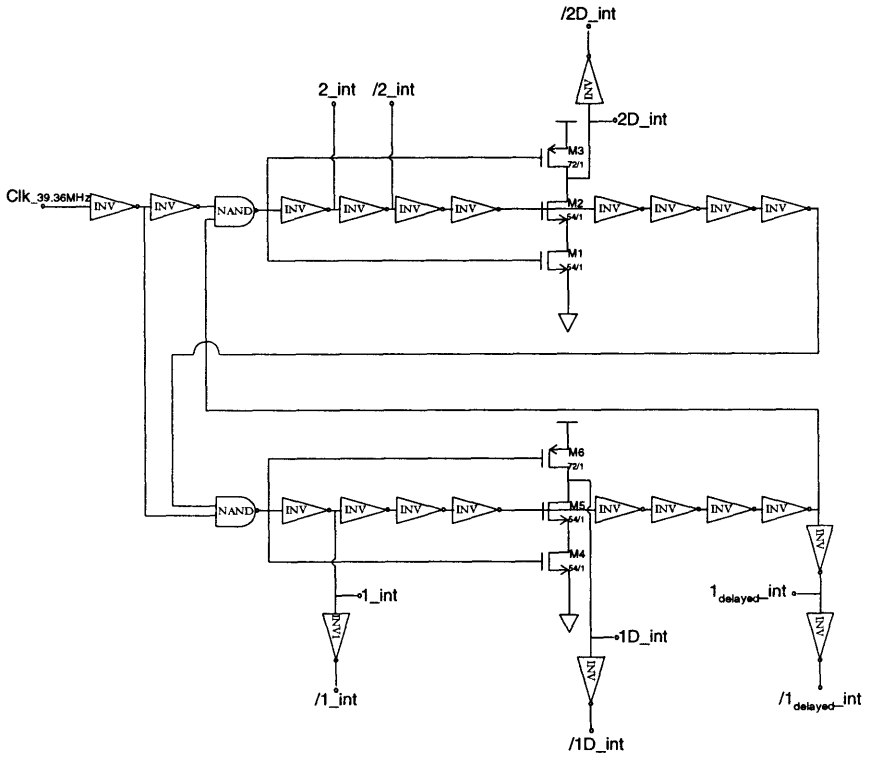


Figure 5.31 Non-overlapping clock generation circuit for clocks 1, 2, 1D, 2D and $1_{delayed}$

Finally, the clocks A1, A2, B1 and B2 are generated using 4 NAND gates, as illustrated in Figure 5.32. The inputs to these gates are the non-inverted outputs of the two non-overlapping clock generators, 1_int, 2_int, A_int and B_int. This circuitry is the only place where the non-inverted outputs were used, rather than the complementary outputs, to allow the delay of the NAND gate to replace the delay of the inverter INV that is necessary between the non-inverted and the complementary outputs. The NAND gates were sized to have the same delay

as the inverter INV in the clock generators, so that the resulting clocks, A1_int and B1_int line up with the positive edges of 1_int clock, while the resulting clocks A2_int and B2_int line up with the positive edges of 2_int clock.

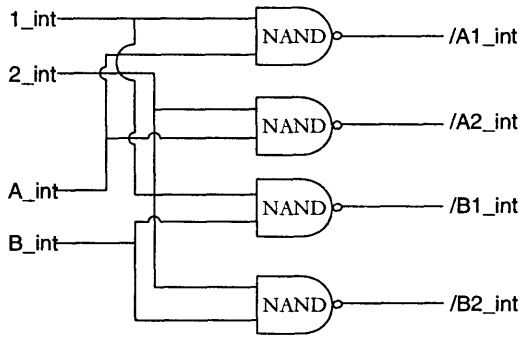


Figure 5.32 Clock generation circuit for clocks A1, A2, B1 and B2

The complements of the intermediate clock waveforms, namely, /1_int, /2_int, /1D_int, /2D_int, /1delayed_int, /A_int, /B_int, /A1_int, /A2_int, /B1_int and /B2_int are then inverted by the 11 different dynamic high-voltage generation circuits used to locally boost the clock drive from 3.3 V to 5 V. In this case, each individual charge pump circuit drives a set of transmission gates that use the same clock to avoid the problem of cross-talk through the clock line. A dynamic high-voltage generation circuit [30] used in the prototype modulator is shown in Figure 5.33. By applying a square wave input signal of 3.3 V, C1 and C2 are self-charged to

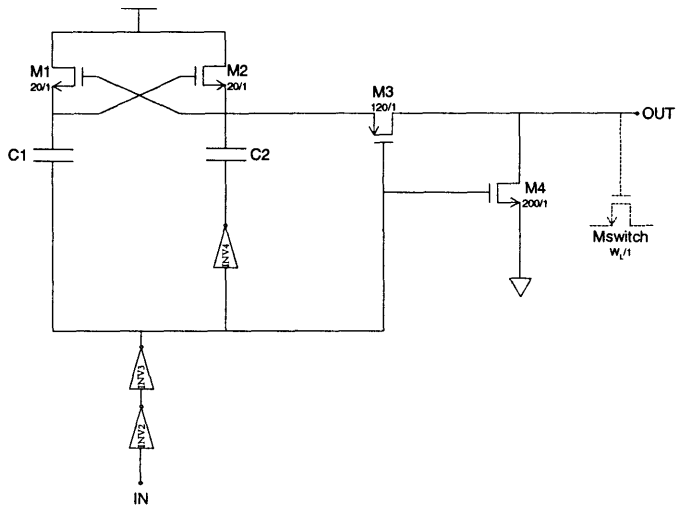


Figure 5.33 Clock boosting circuitry

3.3 V through the cross-coupled NMOS transistors [30], and an inverted square wave output of ~5 V is generated according to

$$Vhi = 2 \cdot Vcc \cdot \frac{C_2}{C_{gate,Mswitch} + C_2 + C_{parasitic}}$$

Equation 5-4

where $C_{gate,Mswitch}$ is the gate capacitance of all transmission gates switched by this clock. The sizes of C_1 and C_2 and the total widths of all transmission gates loading each clock for each clock boosting circuit are shown in Table 5-12.

Boosting circuit for clock	C_1 [fF]	C_2 [pF]	$W_{Mswitch}$ [µm]
1	150	12	2118
2	150	8	1514
1D	150	5.8	680
2D	150	6.1	840
$1_{delayed}$	150	5.5	600
A	150	6	850
B	150	6	850
A1	150	6	850
A2	150	6	850
B1	150	6	850
B2	150	6	850

Table 5-12 The sizes of C_1, C_2, and the widths of Mswitch in boosting circuitry

The inverter and NAND blocks used in the clock generation circuitry are shown in Figure 5.34 and Figure 5.35.

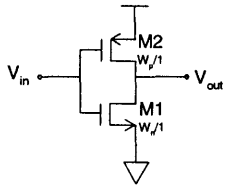


Figure 5.34 The inverter

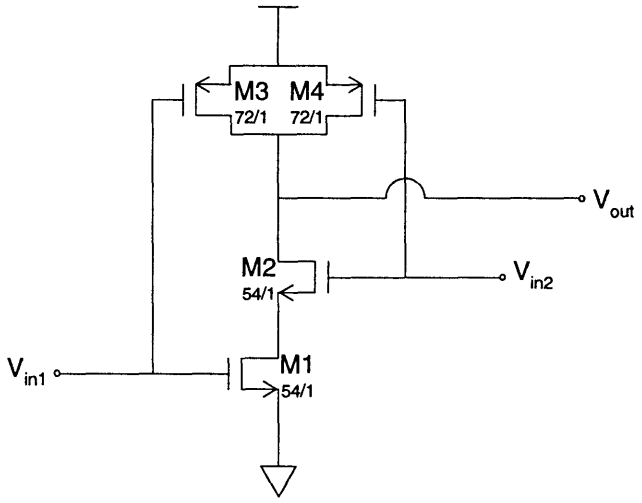


Figure 5.35 The NAND gate

The widths of the PMOS and NMOS MOSFETs in the different inverters used are given in Table 5-13.

Circuit Name	Wp [µm]	Wn [µm]
INV	72	27
INV1	216	81
INV2 in the clock boosting circuitry for clock 1	648	243
INV2 in the clock boosting circuitry for all other clocks	216	81
INV3 in the clock boosting circuitry for clock 1	1944	729
INV3 in the clock boosting circuitry for all other clocks	648	243
INV4	1944	729

Table 5-13 The sizes of various inverters in the clock generation circuitry

Note that the INV2 and INV3 are greater for the clock boosting circuitry for clock 1, since the loading of this clock is significantly greater then loading on any other clock. Note that this solution is optimized for area and power dissipation, but since it is open loop, it is very likely to suffer from component mismatch, as well as vary over process corners, temperature etc. If this circuitry is required to operate over all the corners, another solution may be applied. Namely, dummy devices could be inserted to make the loading on each clock equal, and then due to the circuit symmetry, the variations due to component mismatch and/or different corners will track and in this way be canceled. The price to pay is increased area and power consumption.

5.5 SIMULATION RESULTS AND DISCUSSION

Bandpass sigma-delta converter was designed according to specifications derived in chapter 3 and 4 in a 1 μm CMOS 1.5 fF/μm^2 process. It operates from a single 3.3 V supply at a clock frequency of 39.36 MHz, dissipating 48.5 mW. The input impedance of the converter is 17 k Ω. Implementation details and relevant HSPICE simulation results for individual circuit blocks are given in previous sections of this chapter. This section presents HSPICE simulation results for the overall converter, comparing the actual converter behavior to the predicted.

The performance of the converter is evaluated in the following manner. The converter was simulated in HSPICE for the sinusoidal input of various amplitudes, and 4000 bits obtained from each of the three stages for each input amplitude. The acquired digital data was then manipulated on with MIDAS to perform digital cancellation, obtain the plots of the output spectra, and calculate SNDR and DR. Alternately, C program implementing digital cancellation circuitry was used in conjunction with MATLAB fft capabilities to verify results obtained from MIDAS.

Note that for more precise fft results, the number of data points required is typically much greater than 4000. Due to limited time and the fact that each Hspice run for reasonable number of data points takes about 4 days, the number was limited to 4000. This number was, however, found to be sufficient to verify the proper functioning of the circuit and obtain fair estimates of SNDR and DR.

The predicted behavior and the actual results are summarized in Figure 5.36, where we can see that the actual behavior tracks the predicted one. There seems to be only one relevant deviation from the predicted behavior. Simulated SNDR is smaller than predicted by several dB's at higher input levels. Degradation in SNDR at higher input signals is attributed to non-linearity of op amps that was not modeled in MIDAS but is present in the actual circuits. While the amplifiers are always in saturation, large signal swings can cause the cascoded devices to operate near the triode region, resulting in highly nonlinear output resistance, and therefore increased distortion, for large signals.

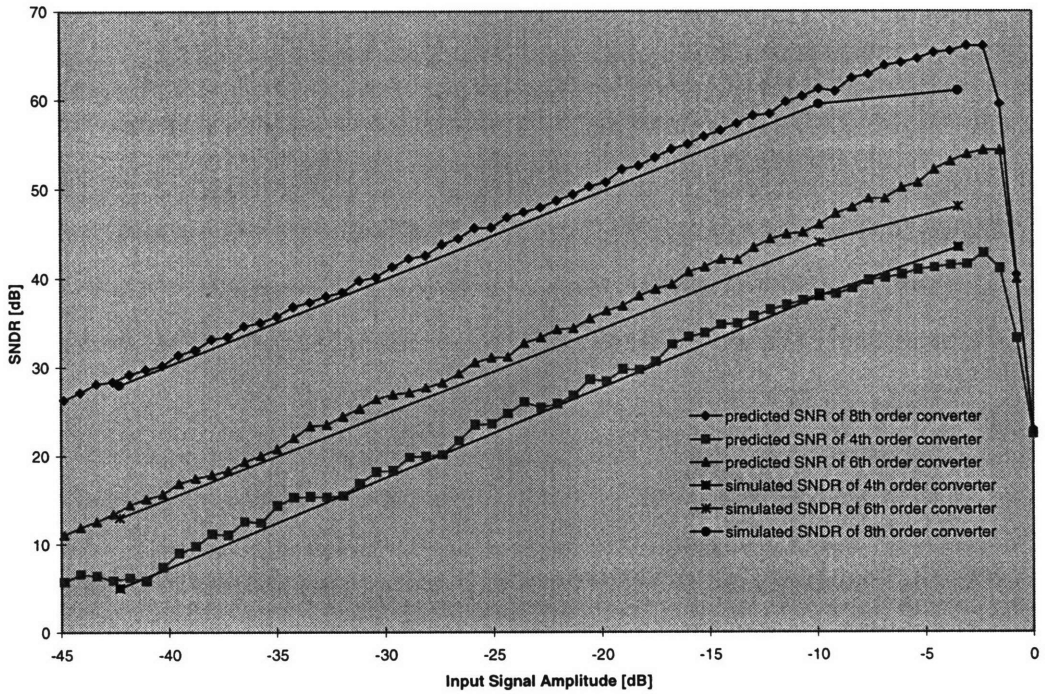


Figure 5.36 Simulated SNDR versus predicted SNR

5.6 SUMMARY

10.5 bit bandpass sigma-delta converter with fs=39.36 MHz and oversampling ratio of 16 for 1.23 MHz signal has been designed according to specifications derived in chapters 3 and 4. It is simulated in HSPICE, using 1 μm CMOS 1.5 fF/μm^2 process. The analog part dissipates 48.5 mW. Implementation details and relevant HSPICE simulation results for individual circuit blocks are given in first four sections of this chapter. Last section presents HSPICE simulation results for the overall converter, comparing the actual converter behavior to the predicted. The actual behavior tracks the predicted, except at the higher input levels. Degradation in SNDR at higher input signals is believed to be due to non-linearity of op amps that was not modeled in MIDAS but is present in the actual circuits.

CHAPTER 6

CONCLUSIONS

6.0 OVERVIEW

Motivated by the prospects of a simpler, more robust and more flexible system, and inspired by the reported success of monolithic bandpass sigma-delta converters for similar applications for narrowband systems, this work investigated whether "digital receiver" architecture could be the architecture of choice for a wideband system such as CDMA path of the dual CDMA/analog mode phone receiver. In particular, this thesis proposed that the dual conversion "digital receiver" architecture with the IF A/D conversion could overcome the deficiencies of the dual conversion receiver with baseband A/D conversion currently in use for a CDMA phone receiver by

- avoiding all the problems associated with digitizing at 0 Hz, such as DC offsets.
- avoiding all the problems associated with analog I/Q demodulation, such as phase and gain mismatch among I and Q paths.
- implementing most of the selectivity processing on digital side, resulting in reduction in analog filtering, flexibility of digital programmability, as well as improved testability and yield.

The problem is that "digital receiver" architecture for a wideband system places extremely high performance requirements on A/D converters. Achieving the desired precision of 10.5 bits at the bandwidth as high as 1.23 MHz is a challenging task by itself, and doing so while still meeting the tight power constraints is what ultimately sets the limit to the application of this receiver architecture. Consequently, this thesis focused on design of a bandpass sigma-delta A/D converter that is able to convert an entire 1.23 MHz band of the North American cellular standard IS-95 and with enough resolution to do most of channel selection on the digital side (here 10.5 bits), with the immediate goal of achieving the same power dissipation as the equivalent parts of the existing architecture.

This chapter summarizes the scope of work done in Section 6.1, presents the conclusions in Section 6.2 and finally proposes the areas for further investigation in Section 6.3.

6.1 SUMMARY

Chapter 1 summarizes the main features of the existing dual conversion receiver architecture with baseband A/D conversion for the North American cellular standard IS95, briefly discussing some of its main advantages and disadvantages. The alternate dual conversion "digital receiver" architecture with IF A/D conversion is further analyzed and compared to the first architecture. Frequency arrangements for the CDMA IF receiver are presented and some of the system level trade-offs for a bandpass modulator necessary for the "digital receiver" are discussed, such as sub-sampling versus analog mixing approach for the analog part, Nyquist-rate versus oversampled A/D conversion for the A/D part, and the impact of the frequency plans on design of the digital part of the modulator.

Chapter 2 reviews the basic principles of bandpass sigma-delta conversion. In particular, it discusses operation and performance modeling of two classes of sigma-delta converters, single-loop and cascaded converters. Modeling of single-loop converters has been discussed for a general case of an L-th order, N-bit converter, asuming Bennet's noise model. Model of L-th order, 1-bit converter has also been presented, assuming white noise approximation. Cascaded converters have been discussed by discussing the modeling of 4-2-2 architecture.

Chapter 3 first discusses the considerations involved in wide-bandwidth sigma-delta design, based on which it decides upon 4-2-2 architecture with 1-bit quantizers as the architecture of choice for the application in hand, for an oversampling ratio of 16. The rest of the chapter discusses system level design in ideal case. The choice of system parameters, such as D/A reference voltages, error gains and error mixing coefficients were chosen based on behavioral simulations done, since not all of the effects that system level parameters have on converter performance are captured by the analysis of Chapter 2. For system parameters chosen, the major converter building blocks were modeled in the ideal case.

Following the system level design in the ideal case, system level design in the presence of circuit non-idealities is necessary. To this goal, the relevant non-idealities of sigma-delta converter circuits were identified, studied and quantified for the design at hand in Chapter 4. The design procedure is outlined and the resulting noise budget allocation for each non-ideality

presented. Behavioral simulations were done to verify that the noise allocation indeed produces the converter with the desired performance.

Chapter 5 finally presents the actual circuits used to implement the converter designed in chapters 3 and 4. The simulations were done to verify that the implemented converter indeed achieves the targeted performance.

6.2 CONCLUSIONS

There are two major contributions of this work. First, this work verifies that the dual conversion "digital receiver" architecture with IF A/D conversion is a promising receiver architecture for systems with up to at least 1.23 MHz of a signal band. The verification is done by implementing the critical component of the "digital receiver" architecture for the CDMA path of a dual mode CDMA/analog phone receiver, namely bandpass sigma-delta modulator, and verifying through simulations that it achieves the performance equivalent to the components in an existing dual conversion receiver with baseband A/D conversion. The performance here is evaluated by metric that was of crucial concern for this wideband system, namely power consumption. Second, through implementation and simulation of this 10.5 bit bandpass sigma-delta converter with the oversampling ratio of 16, sampling frequency of 39.36 MHz and a signal band of 1.23 MHz signal, 4-2-2 architecture was found to be very attractive for high resolution high-bandwidth systems.

6.3 FUTURE WORK

This thesis was meant as a proof of concept that the "digital receiver" architecture is a promising alternative to the existing receiver architecture that utilizes baseband A/D conversion. As such it developed the converter and verified the performance in simulations, without actually fabricating the experimental circuitry. The next logical step would therefore be the actual fabrication to verify the simulation results. Also, this thesis discussed some of the system level issues for the bandpass IF receiver, without detailed characterization of all blocks. More research could be done to more precisely characterize the requirements on anti-aliasing filter and the digital part of the sigma-delta modulator, in order to obtain more precise performance figures, such as power consumption and area required, and/or implement the actual components.

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