Electric Field Engineering in GaN High Electron Mobility Transistors

by

Xu Zhao

B.S., Electrical Engineering (2005)

Tsinghua University

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Signature of Author .....
Department of Electrical Engineering and Computer Science
November 7, 2007

Certified by.....
Tomás Palacios
Assistant Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Accepted by .....
Terry P. Orlando
Chairman, Department Committee on Graduate Students

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BIOGRAPHY
XU ZHAO
January 2008

EDUCATION

Master candidate (since September 2005, expected February 2008)
Department of Electrical Engineering and Computer Science, MIT
Advisor: Professor Tomás Palacios
Thesis: Electric Field Engineering in GaN High Electron Mobility Transistors

Bachelor of Science (September 2001-July 2005)
Department of Electrical Engineering, Tsinghua University, Beijing, China

AWARDS AND PRIZES

2007 IEEE Electron Device Society Master Student Fellowship
2004 Merit based "Yukang Zhou" National Fellowship, First Prize
2004 Mathematical Contest in Modeling (MCM), the Consortium for Mathematics and Its Applications (COMAP), USA
2003 Merit based Chinese National Fellowship, First Prize (2 out of 370)
2003 Chinese National Mathematical Modeling Contest, First Prize
2002 Merit based Chinese National Fellowship, First Prize (2 out of 370)
2002 Chinese National undergraduate Physics Olympic Contest, Beijing, Third Prize
2001 Chinese National Chemistry Winter Camp member (about 100 in China), Chinese Chemical Society
2000 Chinese National Chemistry Olympic Contest, Liaoning province, First Prize (2nd out of all participants, about 5000 in total), Chinese Chemical Society
2000 Chinese National Physics Olympic Contest, Liaoning province, First Prize (27th out of all participants, about 5000 in total), Chinese Physics Society
2000 Chinese National Mathematical Olympic Contest, Liaoning province, Second Prize (52ed out of all participants, about 5000 in total), Chinese Mathematics Society
1999 Chinese National Mathematical Olympic Contest, Liaoning province, Second Prize, Chinese Mathematics Society

PUBLICATIONS

"Study of RF MEMS Actuations using Matlab/Simulink"
Xu Zhao, Zewen Liu, Sensor&Transducer Conference'05

"Modeling of Chirality-Dependent I-V Characteristics of Carbon Nanotube FETs"
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"Improvement of Electron Velocity in GaN HEMTs by Electric Field Engineering"
Xu Zhao, Jinwook Chung, Tomás Palacios, MARC'07

"Effect of image charges in the drain delay of AlGaN/GaN HEMT"
Jinwook Chung, Xu Zhao, Tomás Palacios, MARC'07

"Schottky Drain AlGaN/GaN HEMTs for mm-wave Applications"
Xu Zhao, Jinwook Chung, Hui Tang, Tomás Palacios, Device Research Conference, 2007

"Estimation of Trap Density in AlGaN/GaN HEMTs from Subthreshold Slope Study"
Jinwook Chung, Xu Zhao, Tomás Palacios, Device Research Conference, 2007

"Improvement of Electron Velocity in GaN HEMTs by Electric Field Engineering"
Xu Zhao, Jinwook Chung, Tomás Palacios, ICNS 2007

"Atomic Layer Etching of AlGaN/GaN Structures"
Xu Zhao, Jinwook Chung, Tomás Palacios, ICNS 2007

"Effect of Image Charges in the Drain Delay of AlGaN/GaN HEMTs"
Jinwook Chung, Xu Zhao, Tomás Palacios, ICNS 2007

ABSTRACT

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In the last few years, AlGaN/GaN high electron mobility transistors (HEMTs) have become the top choice for power amplification at frequencies up to 20 GHz. Great interest currently exists in industry and academia to increase the frequency to mm-wave frequencies. The goal of this thesis has been to identify new solutions to some of the main challenges to increase this frequency performance even further.

Electron velocity is a critical parameter affecting the transistor performance. In standard GaN transistors, the extremely high electric fields present in the channel of the device reduce the average electron velocity well below the peak electron velocity, resulting in low cutoff frequencies. In this thesis, we introduced a partial recess in the drain access region of the transistor to engineer the electric field along the channel of the device without introducing parasitic capacitances. By reducing the peak electric field, the average electron velocity is increased by 50%. This new technology has the potential to improve not only the cutoff frequencies, but also the breakdown voltage of GaN transistors.

To successfully engineer the electric field in GaN devices, an accurate, reliable and low damage etching technology is needed. However none of the traditional GaN dry etching technologies meets these requirements. This lack of suitable technology has motivated us to develop a new atomic layer etching technique of AlGaN/GaN structures. This technology has been shown to be a self limited process with very high reliability and low damage, which will be very useful both in electric field engineering and gate recess.

Finally, another factor hindering GaN HEMTs from competing with InGaAs devices at high frequencies are their high parasitic capacitances and resistances. In this thesis, ohmic drain contacts are replaced with Schottky drain contacts to reduce the drain access resistance. ADS simulations predict a very significant increase in the cutoff frequencies by virtue of the lowered parasitic resistances.

In conclusion, the theoretical and experimental work developed during this project has demonstrated the great potential of three new technologies to overcome the main challenges of mm-wave GaN HEMTs. The application of these technologies to actual devices is under way and it will represent an important element of the ultra-high GaN transistors of the future.

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Chapter 1: Introduction

1.1 Historical Development

The term "*Nitride semiconductors*" include a unique material system which comprises Galium Nitride (GaN), Aluminum Nitride (AlN), Indium Nitride (InN) and their alloys. Nitrides cover a wider spectrum of bandgaps than most other material systems, as shown in Figure 1.1. Research in nitrides started three decades ago when Pankove et al. reported the first GaN-based light-emitting diode (LED) [Pankove1971]. However, the performance of these early devices was not due to their intrinsic material properties, but due to the high defect density and poor surface morphology of the heteroepitaxial films. It was not until mid-1980s that these problems began to be overcome, thanks to the work of Isamu Akasaki at Nagoya and Meijo Universities and Shuji Nakamura at Nichia Chemical Company in Japan [Amano1990][Nakamura1991]. High quality GaN films on sapphire substrates were grown by metal-organic chemical vapor deposition (MOCVD) using AlN or GaN nucleation layers. Since then, the research field using GaN has exploded, first in optoelectronics, later in electronics.

Shuji Nakamura, now a professor in University of California at Santa Barbara, was the first one to fabricate blue, white, green and violet LEDs and blue light semiconductor lasers using this material family. Today, nitride based optoelectronics are everywhere, from traffic light to large displays and high definition DVD players.

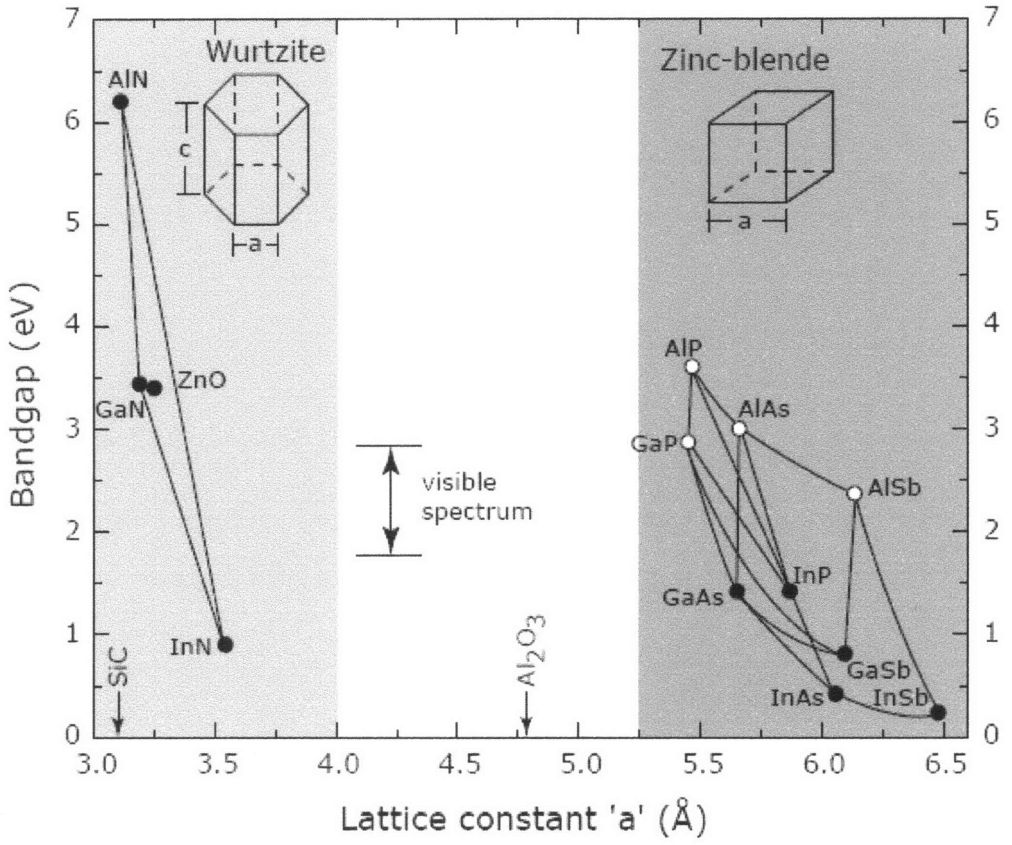


Figure 1.1 The bandgap-lattice constant plot. All bandgaps plotted are the direct gaps, indirect gap semiconductors are shown by open circles. Wurtzite crystals are characterized (see insets) by two lattice constants (a,c) of which the a-lattice constant is used for the figure. The a-lattice constants of the common substrates for growth of III-V Nitrides-SiC and Al_2O_3 (sapphire) are indicated by arrows.

Besides optoelectronics, this decade has also witnessed the use of nitrides as electronic devices. Figure 1.2 summarizes some of the most important applications for GaN based power transistors. For commercial applications, GaN has already been employed in cell phone base stations. Other important applications in the near future include satellite communications, high speed digital communications and digital radio. For military applications, the use of GaN amplifiers in radar and 94 GHz direct energy weapons is driving the interest of companies such as Raytheon, Northrop Grumman and others.

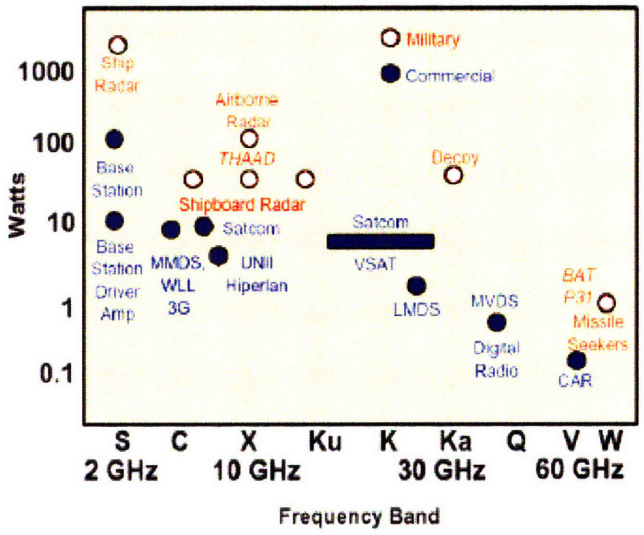


Figure 1.2 Some of the most important potential applications for GaN-based power transistors

The use of GaN for electronic applications started in the early 1990s, several groups managed to grow high quality AlN films on sapphire substrates [Amano1990][Nakamuru1991][Khan1992a]. AlN was proved to have a highly insulating nature, making it a good candidate for gate insulating layer, just as the oxide in Silicon MOSFET [Khan1992a]. Later, Khan et al. successfully grew n-GaN/$Al_{0.14}Ga_{0.86}N$ heterojunctions and attributed the high electron mobility values in this structure to the 2-dimensional electron gas conduction [Khan1992b]. After that, the first GaN transistors were demonstrated in 1993 [Khan1993]. At that time, the transconductance was limited to only 28 mS/mm at 300K and they showed no significant frequency performance. But in the last 15 years, the performance of these devices has evolved tremendously both in terms of frequency and output power.

1. High frequency performance (f_T and f_{max})

Although the only commercial devices available nowadays operate at frequencies around 2 GHz (cell phone base stations), several groups have successfully fabricated devices with f_T and f_{max} higher than 100 GHz. In 2000, Micovic demonstrated an extrinsic f_T of 110GHz and a f_{max} over 140 GHz in an AlGaN/GaN HEMT with 50 nm gate length [Micovic2000]. In 2005, Higashiwaki reported a f_T of 163 GHz in devices

with a gate length (L_g) of 60nm and a peak f_{max} in the 163-192 GHz range in devices with L_g=80nm [Higashiwaki2005]. And finally, Palacios reported a f_T of 163 GHz and a f_{max} in excess of 180 GHz in a passivated device with L_g=90nm [Palacios2005].

2. Power performance (output power and power added efficiency)

At the same time, the output power and power added efficiency (PAE) have also shown great progress. At 2GHz, power amplifiers with a total output power in excess of 250 W have been reported [Wakejima2005]. At 4GHz, 32 W/mm output power and 54.8% PAE have been achieved at V_{DS}=120V [Wu2004]. At higher frequency range, an output power of 7.8 W/mm and a PAE of 65% have been demonstrated at 15GHz and V_{DS}=30V [Palacios2005b]. In 2003, Wu et al. obtained more than 3.3W/mm of output power and 22% PAE at 35 GHz [Wu2003]. In 2005, Moon et al. measured an output power of 6.9W/mm and a PAE of 29% at 30 GHz [Moon2005]. Table 1.1 summarizes the major breakthroughs in the last 15 years.

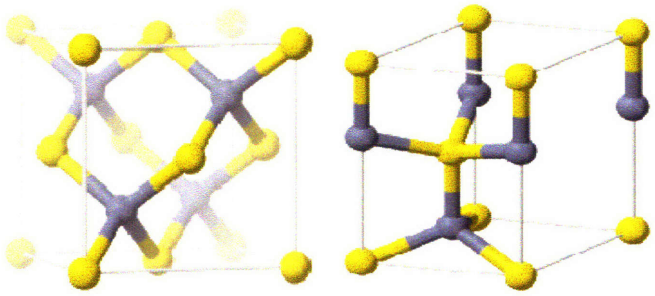
Author	Year	Gate length(μm)	f_T (GHz)	f_{max} (GHz)	P_{out}	PAE
Kahn	1994	0.25	11	35		
Wu	1997	0.2	50	92		
Wu	1997	0.25			3W/mm@18GHz	
Micovic	2000	0.05	110	140		
Wu	2003				3.3W/mm@35GHz	22%@35GHz
Wu	2004				32W/mm@4GHz	54.8%@4GHz
Moon	2005				6.9W/mm@30GHz	29%@30GHz
Palacios	2005				7.8W/mm@15GHz	65%@15GHz
Higashiwaki	2005	0.06-0.08	163	163-192		
Palacios	2005		163	>180	10.5W/mm@40GHz	33%@40GHz

Table 1.1 Major power and frequency breakthroughs in GaN HEMTs during the last 15 years.

1.2 Material Properties

GaN can be grown in two different crystalline structures: Zinc Blend and Wurtzite, which are illustrated in Figure 1.3. However, the Wurtzite structure is used by the

great majority of current electronic and optoelectronics devices.



(a) (b)

Fig. 1.3 Zinc blend (a) and Wurtzite (b) crystal structures for GaN

	Si	GaAs (AlGaAs/InGaAs)	InP (InAlAs/InGaAs)	SiC	GaN (AlGaN/GaN)
Eg (eV)	1.1	1.42	1.35	3.26	3.49
Mobility($cm^2/V{\cdot}s$)	1500	8500	5400	700	1000-2000
Saturated(peak) electron velocity ($10^7 cm/s$)	1.0 (1.0)	1.3 (2.1)	1.0 (2.3)	2.0 (2.0)	1.3 (2.5)
Breakdown field (MV/cm)	0.3	0.4	0.5	3.0	3.0
Thermal conductivity (W/cm·k)	1.5	0.5	0.7	4.5	>1.5

Table 1.2 Material properties of most commonly used semiconductors for power applications

Table 1.2 compares the key electronic parameters of the five most commonly used semiconductor systems. The large bandgap and critical breakdown field of GaN makes it very attractive for high voltage power applications.

At first glance, GaN is not very advantageous in terms of mobility. An electron mobility of 1000-2000 $cm^2/V{\cdot}s$ is only as good as Silicon, but inferior to GaAs and InP. However, in high frequency applications, the electron velocity is much more important than the mobility.

In different semiconductor material systems, electron velocities show different functions with the electric field. In Silicon the electron velocity increases with the

electric field in an almost linear way with a slope characterized by the low field mobility. At high electric field, the electron velocity reaches a saturation value of 1.0×10^7cm/s. In GaAs the shape of the electron velocity with electric field is different. In this semiconductor, after reaching the peak electron velocity of 2.1×10^7cm/s, the electron velocity starts to decrease and saturates at a value much lower than the peak value. The electron velocity versus electric field relation for GaN is even more complex, as shown in Figure 1.4. At 60 kV/cm electric field, the electron velocity has a quasi-saturation, but the real saturation occurs at electric field higher than 250 kV/(cm). The peak electron velocity takes place around 150 kV/(cm). A peak electron velocity of 2.5×10^7 cm/s makes GaN an excellent candidate for power applications in terms of electron velocity. In addition, this irregular velocity versus electric field relation has a profound influence on the device performance, which we will explain in detail later in chapter 2.

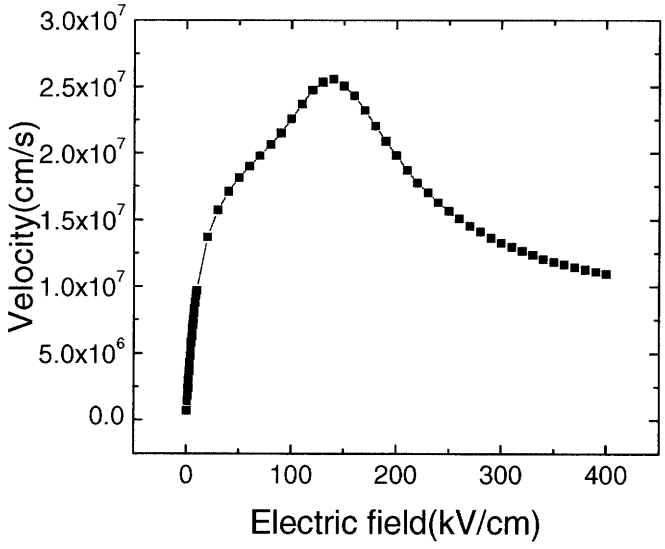


Figure 1.4 Velocity against electric field in GaN

Another unique and important property of GaN is its polarization. Due to the non-centro-symmetry of the GaN unit cell and the different electron negativities of the Gallium and Nitrogen atoms, the crystal structure of GaN exhibits an important

spontaneous polarization. As an example of the magnitude of this polarization, the surface polarization charge density for GaN is $P_{sp}/e \approx 1.8\times10^{13}/cm^2$, and for AlN is $5\times10^{13}/cm^2$. The electric field induced by these polarization sheet charges is estimated to be 1-10 MV/cm, high enough to change the electrostatics and influence the entire band structure of GaN devices.

Besides spontaneous polarization, GaN also has piezoelectric polarization. The piezoelectric field along the i th direction can be expressed as a function of the strain ε_{jk} and the stress σ_{jk},

$$P_{pz,i} = e_{ijk}\varepsilon_{jk} = d_{ijk}\sigma_{jk}$$

where the Levi-Civita convention of summation over the repeated indices is employed [Jena2003]. Since the moduli are symmetric in the indices j,k, the third rank-tensors e_{ijk}, d_{ijk} reduce to a simpler 3×6 matrix form e_{ij}, d_{ij}. For the Wurtzite crystal, symmetry theory further reduces the matrix to only three constants, expressed as

$$e = \begin{pmatrix} 0 & 0 & 0 & 0 & e_{14} & 0 \\ 0 & 0 & 0 & e_{15} & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{pmatrix}$$

Stress and strain coefficients are related in a crystal by the relation $e_{jk} = c_{ij}d_{ik}$ where the elastic coefficients c_{ij} are expressed as a matrix

$$\begin{pmatrix} c_{11} & c_{12} & c_{13} & 0 & 0 & 0 \\ c_{12} & c_{11} & c_{13} & 0 & 0 & 0 \\ c_{13} & c_{13} & c_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & c_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{2}(c_{11}-c_{12}) \end{pmatrix}$$

For analysis of polarization in III-V nitrides, only two elastic coefficients c_{13}, c_{33} are necessary. The value of these coefficients in GaN are $c_{13} = 103GPa$ and $c_{33} = 405GPa$. Additionally, since most GaN/AlGaN systems are epitaxially grown

along the [0001] direction, the piezoelectric field along this direction can be expressed as

$$P_3 = e_{33}\varepsilon_3 + e_{31}(\varepsilon_1 + \varepsilon_2)$$

The strain components ε_1 and ε_3 are related by $\varepsilon_3 = -2\varepsilon_1(c_{13}/c_{33})$, and $\varepsilon_1 = \varepsilon_2$, thus piezoelectric field along the [0001] direction can be rewritten as

$$P_{pz,[0001]} = 2(e_{31} - e_{33}\frac{c_{13}}{c_{33}})\varepsilon_1$$

where $\varepsilon_1 = (a - a_{GaN})/a_{GaN}$ is the in-plane strain. The piezoelectric polarization for alloys, such as $Al_xGa_{1-x}N$ can be obtained by a linear combination of all the parameters of the underlying constituents.

In Figure 1.5, we illustrate the polarization fields in the AlN/GaN system. Here we assume that GaN is strain relaxed, hence there is no piezoelectric field in GaN layer. Due to the lattice mismatch (AlN has a smaller in-plane lattice constant than GaN), there is an in-plane tensile strain in the AlN layer, resulting in a piezoelectric field pointing downward. Here, we adopt an Al-face AlN and Ga-face GaN, as the case in most epitaxial growth, thus the spontaneous polarization fields in both AlN and GaN are also directed downward. At the AlN/GaN interface, AlN contributes a layer of positive polarization charges, while GaN contributes a layer of negative polarization charges. They compensate with each other, coming up with net positive polarization charges at the interface:

$$\sigma_\pi = (P_{AlN} - P_{GaN}) \bullet \hat{n} = 6.4 \times 10^{13}/cm^2$$

The polarization charge for $Al_xGa_{1-x}N$/GaN system can be analytically calculated in a similar way but with a linear interpolation.

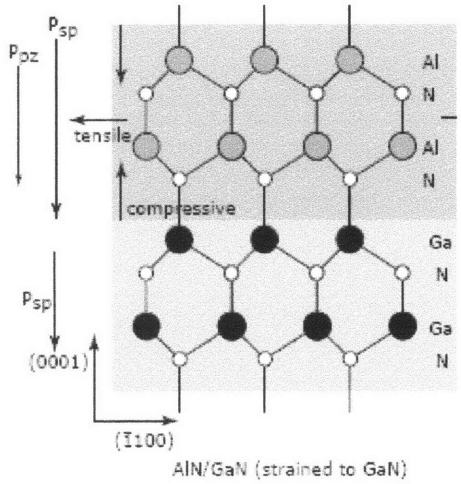


Figure 1.5 Polarization field in AlN/GaN system

Due to the existence of large polarization electric field in the AlGaN barrier, one layer of electron carriers is formed at the AlGaN/GaN interface. Under equilibrium conditions, these electrons come from the AlGaN surface states and are swept through the AlGaN layer into the GaN layer. The electron density in this layer is on the order of $10^{13}/cm^2$, superior to the charge density typical in modulation doped AlGaAs/GaAs system. On the other hand, because of the absence of doping in the AlGaN layer, electrons in the channel are further freed from ionized charge scattering.

In summary, all these unique and superior material properties, such as large and tunable bandgap, high electron velocity and polarization-induced electron density make nitride semiconductor ideal for high-frequency high-power applications.

1.3 GaN HEMTs

GaN is an ideal semiconductor for power amplifiers. In these devices, the maximum linear output power can be calculated from

$$P_{\max,lin} = I_{\max}(V_{BD} - V_{knee})/8$$

Where I_{max} is the maximum drain current density, V_{BD} is the breakdown voltage of the device and V_{knee} is the knee voltage. The maximum drain current I_{max} is determined by

the carrier density and electron velocity. From Table 1.2, GaN has the highest peak electron velocity and similar saturation velocity, compared with other material systems. Due to the polarization effect (both spontaneous and piezoelectric), GaN also has a much higher two-dimensional electron density than, for example, GaAs-based devices. In addition, GaN has the largest bandgap, thus is able to withstand much higher electric field. All these material properties lead to superior V_{BD} and I_{max}, making GaN inherently advantageous for power applications.

Another figure of merit evaluating power devices is the current gain cut-off frequency, which is inversely proportional to the total electron delay. As pointed out by N. Moll [Moll1988], the total delay of electrons in a field effect transistor consists of three components: intrinsic delay, channel charging delay and drain delay. In the figure of total delay as a function of the corrected drain to source voltage (Figure 1.6), the linear part is associated with the drain delay, which increases with the voltage because the drain depletion region extends as voltage increases. Then the linearly extrapolated delay is the delay without drain delay, which is the sum of intrinsic delay and channel charging delay.

On the other hand, if we plot the total delay against the reciprocal of drain current density, the linearity of total delay at low, and even not so low, drain current is quite striking. If we assume the electron velocity at the drain end is constant, then the current density is proportional to the electron density in the channel. Figure 1.7 indicates that the linear part is associated with a delay contribution related to a RC time constant, which is just the channel charging delay we have defined. By extrapolating the linear part to zero, we have eliminated the channel charging delay, so the result is a pure component of intrinsic delay and drain delay.

Using these two figures, we can extract the different delay components. In Figure 1.6 and Figure 1.7, the drain delay and channel charging delay can both be calculated from the difference between the linear part and the extrapolated delay. Since the

extrapolated intercepts are the sum of either the intrinsic and channel charging delay or the sum of the intrinsic and drain delay, we can determine the intrinsic delay from any intercept.

To the first order, intrinsic delay is determined by the gate length and the average electron velocity under the gate. The channel charging delay is related to the parasitic resistances and capacitances. The drain delay equals the time taken by the electrons to cross the depletion region at the drain side of the gate. With e-beam lithography, nowadays devices can be fabricated with shorter gate length down to 30nm. In this regime, drain delay and channel charging delay are expected to play a more important role. Therefore, how to improve the electron velocity and reduce the parasitics becomes the main issue ahead of us. The next section describes the main challenges when trying to increase the electron velocity and to reduce the parasitics.

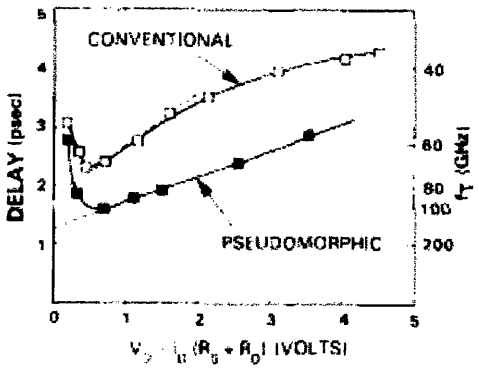


Figure 1.6 Total delay as a function of voltage across the channel and drain depletion region, for conventional and pseudomorphic FET's, from [Moll1988]

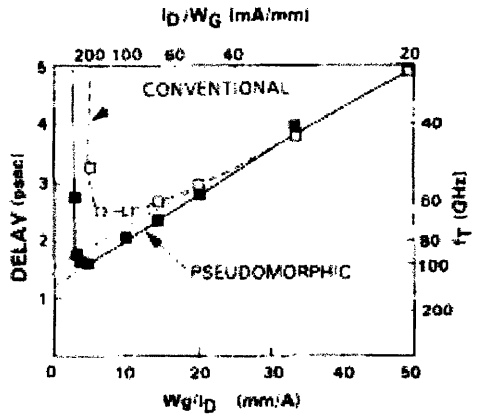


Figure 1.7 Total delay as a function of the reciprocal drain current density at V_{DS}=1V, for conventional and pseudomorphic FET's, from [Moll1988]

1.4 Factors limiting frequency performance

In spite of the superior material properties and the great progress achieved during the last few years, the performance of state-of-the-art GaN HEMTs is still far below theoretical limit. Figure 1.8 shows the cutoff frequency f_T as a function of the gate length L_g in the ideal case ($f_T = v_e/(2\pi L_g)$, $v_e = 2.5\times10^7 cm/s$) and also the experimental results from literature. It is obvious that devices are not optimized yet. There are two reasons behind the discrepancy of theoretical predictions and real device performance: lower electron velocity and higher parasitic resistances and capacitances.

The first factor limiting f_T is the lower-than-expected electron velocity. Although the peak electron velocity of GaN is 2.5×10^7 cm/s, often used to calculate the theoretical predictions, the electron velocity decreases very rapidly due to polar optical phonon scattering, for electric field in excess of 150 kV/(cm) [Singh2003]. Unfortunately, high electric fields are common when devices are used in power amplifiers. The lower electron velocity affects both the intrinsic delay and the drain delay, which result in lower f_T and f_{max}. Several groups have tried to reduce the electric field in the channel through the use of field plate technology [Ando2003][Chini2004]. However, field plates increase the parasitic capacitances, typically reducing the frequency performance.

The second factor limiting f_T is the high parasitic resistances and capacitances. For instance, in GaN HEMTs, R_s and R_d are still above 0.2 Ω·mm, which is 10 times higher than GaAs transistors. As is shown by Tasker [Tasker1989], the current gain cutoff frequency f_T is expressed as

$$f_T = \frac{g_m/2\pi}{[C_{gs}+C_{gd}][1+(R_s+R_d)/R_{ds}]+C_{gd}\cdot g_m\cdot(R_s+R_d)}$$

High parasitic resistances and capacitances will dramatically degrade f_T and also f_{max} (f_{max} is a function of f_T).

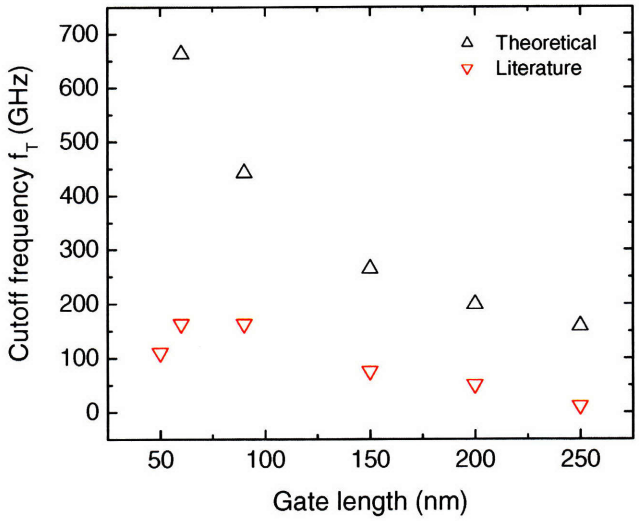


Figure 1.8 Cutoff frequency as a function of the gate length from theoretical calculation and literature data

1.5 Synopsis of the thesis

This thesis has demonstrated two new device technologies to improve the high frequency performance of GaN HEMTs: electric field engineering and Schottky drain contact. In addition, a new etching technology is developed to allow the successful fabrication of these devices.

Chapter 2 introduces a new method to increase the electron velocity in GaN HEMTs. Using a partial recess in the drain access region, the electric field is reduced by 50%. As a result, the electron velocity is increased by 50% while the drain access resistance is only increased by 5%. This is therefore a very promising method to improve both the electron velocity and the breakdown voltage.

To successfully fabricate devices with a partial recess in the drain access region, an

accurate, reliable, reproducible and self-limited etching process is highly needed. After a survey of available etching technologies, we find that none of them meet the requirements to fabricate high performance devices. Therefore, we developed a completely different solution: atomic layer etching (ALE). The development of this recess technique is the topic of Chapter 3. Combining the chemical etching of Cl_2 and physical etching of Ar, ALE achieved a self limited process with high depth resolution, reproducibility and minimum surface damage. This new technology will be very useful not only for electric field engineering (partial recess in the drain access region), but also for reliable gate recess.

Chapter 4 introduces a new device structure to reduce the parasitic delays in GaN transistors: Schottky drain contacts. By replacing the conventional ohmic drain contact with a Schottky drain contact, both the access resistance and contact resistance are reduced as shown both by experiments and theory. ADS simulation results show that, by reducing the drain parasitic resistance (access resistance + contact resistance) from 2 Ω·mm to 0.2 Ω·mm, f_T increases from 116 GHz to 162 GHz and f_{max} increases from 162 GHz to 477 GHz.

Finally, chapter 5 provides a summary of the thesis as well as future work to take the devices developed in this work to higher levels of performance.

Chapter 2: Electric Field Engineering

2.1 Motivation

One of the critical parameters limiting the high frequency performance of GaN HEMTs is the electron velocity. Not only the maximum frequency of operation of an amplifier is directly related to the electron velocity but also the gain and efficiencies of the amplifier at lower frequencies are strongly affected by this velocity. With a 2.5×10^7cm/s peak electron velocity, GaN is anticipated to outperform most other material systems. However, in spite of this very high theoretical value, this velocity has unfortunately not been achieved in practical devices yet. The reason behind this is explained below.

As shown in Figure 2.1, GaN has a strongly nonlinear electron velocity versus electric field relation. At electric fields around 150 kV/cm, the electron velocity reaches 2.5×10^7 cm/s, but once it reaches that value, it drops dramatically with increasing electric field. Unfortunately, as shown in Figure 2.2, in most GaN HEMTs applications, the electric field in the channel is very high, exceeding 300 kV/cm, which makes the devices actually work in the region where the electron velocity is dramatically reduced. To take full advantage of the very high electron velocity in GaN, it is necessary to reduce the electric field, moving the operating point of the intrinsic transistor to the region where the peak electron velocity is located.

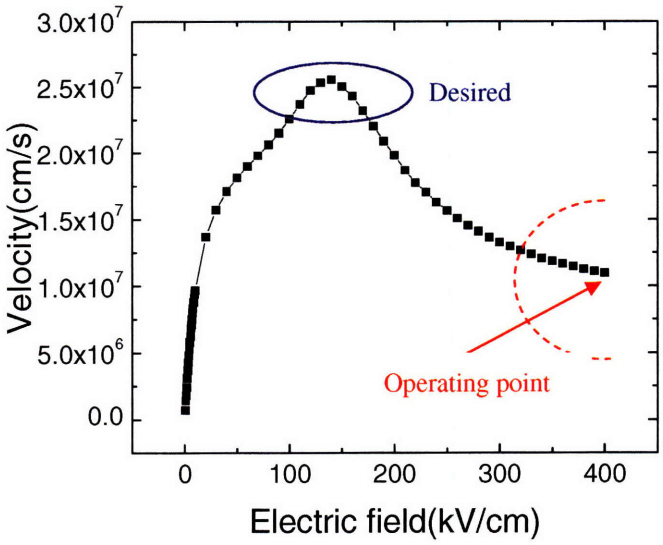


Figure 2.1 Electron velocity versus Electric field in GaN

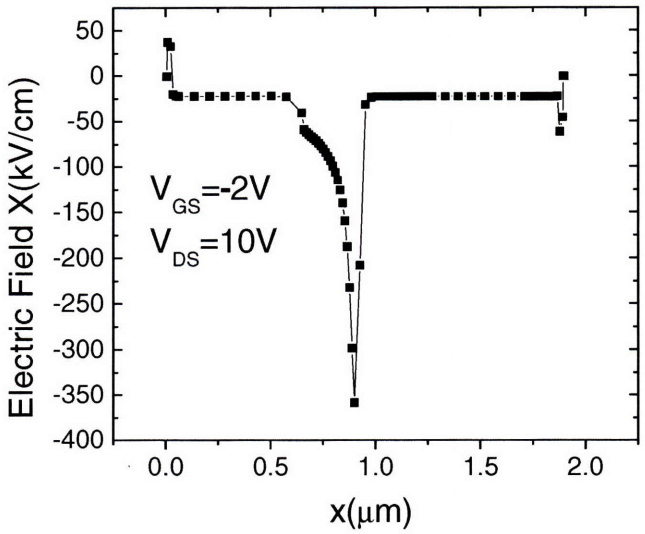


Figure 2.2 Electric field distribution in standard AlGaN/GaN HEMTs. V_{GS}=-2V, V_{DS}=10V. The electric field is negative, since it points toward the source.

In the literature there are several methods to reduce the electric field in the channel, e.g., field plate technology and fluorine treatment. Both of them have pros and cons.

A device with field plate structure is shown in Figure 2.3. This figure also shows the effect of the field plate on the electric field distribution [Karmalkar2001] [Chini2004]

[Ando2003]. It is obvious that field plate redistributes the electric field in the channel so that the peak electric field is reduced. However, as a side effect, the field plate also forms a parasitic capacitance with the channel which reduces the frequency performance of the device, partly offsetting the benefit of a higher electron velocity.

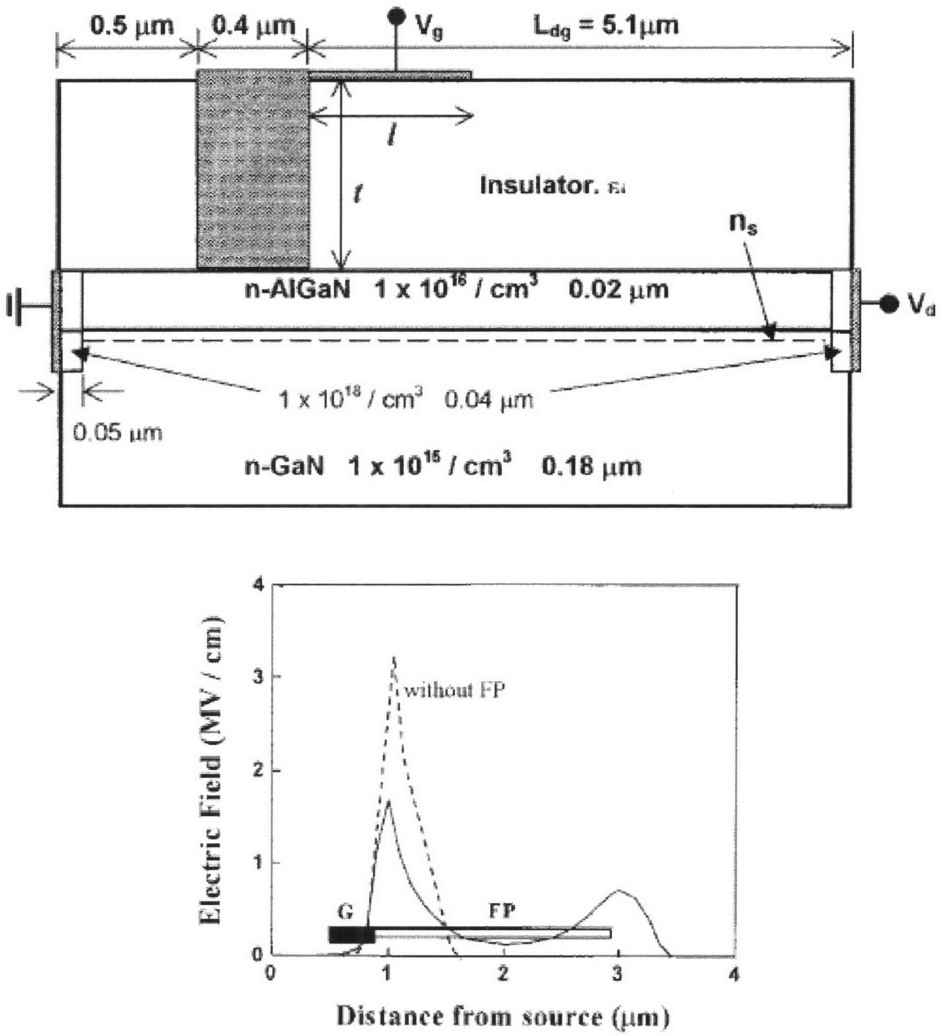


Figure 2.3 Use of field plate to redistribute the electric field in AlGaN/GaN HEMTs

A second option is to apply a fluorine plasma treatment, as is shown in Figure 2.4 [Cai2005][Shen2006]. Similar to the field plate technology, the peak electric field is also reduced by the introduction of the fluorine ions, but in this case, the effect is very limited. At the same time, the thermal stability of the introduced ions, and therefore the device, is a big issue still under investigation.

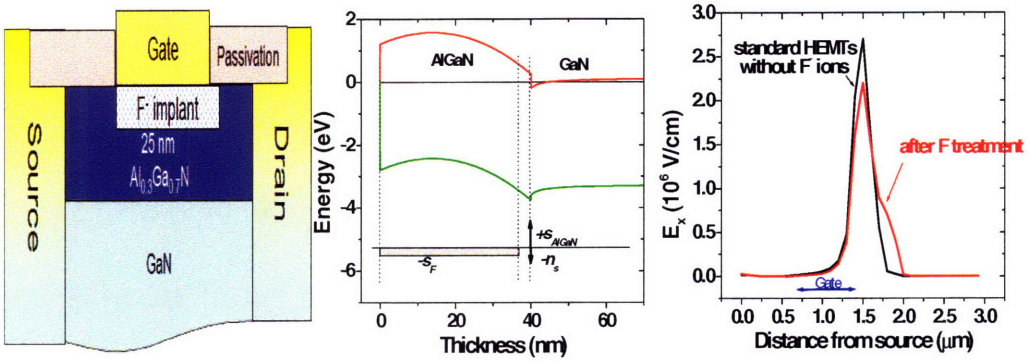


Figure 2.4 Use of fluorine treatment to reduce the electric field in AlGaN/GaN HEMTs

Although the two different techniques described to reduce the electric field have shown great promise in improving the device performance, none of them are ideal solutions due to their problems at high frequencies and reliability issues. Therefore, in this thesis, we propose a completely new method to reduce the peak electric field under the gate. The new structure we are exploring introduces a partial recess in the drain access region, as shown in Figure 2.5.

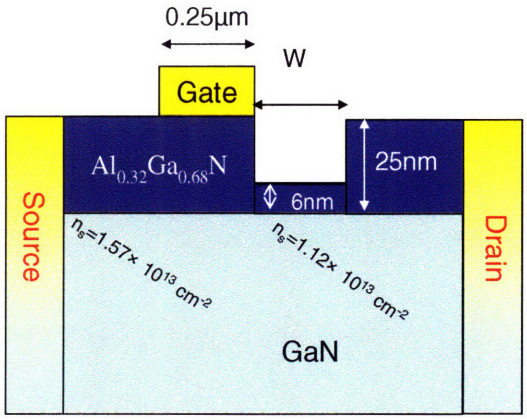


Figure 2.5 AlGaN/GaN HEMTs with a partial recess in the drain access region

2.2 Principles and Simulation

When an $Al_xGa_{1-x}N$ layer is grown on top of a GaN buffer, the polarization difference between the two semiconductor layers induces an electron channel at the $Al_xGa_{1-x}N$/GaN interface in the GaN side. The electron density in the channel is a strong function of the $Al_xGa_{1-x}N$ thickness, as illustrated in Figure 2.6 [Zhang2002].

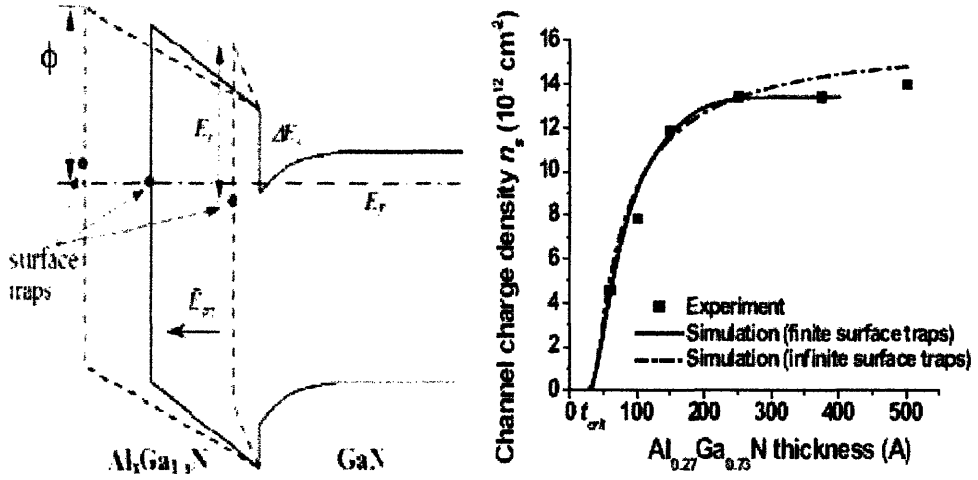


Figure 2.6 Electron density versus AlGaN thickness. With varying the AlGaN thickness, the energy level of surface traps moves to change the electron density in the channel.

As the electron density varies with the $Al_xGa_{1-x}N$ thickness, the electron density underneath the recessed region will be lower than the electron density in other regions. Lower electron density results in higher resistivity and higher electric field under the recessed region. Since the voltage drop along the channel direction is a constant, the electric field under the gate will be reduced, so that the average electron velocity in that region will be increased. To evaluate the effect of this recessed region on the peak electric field and average electron velocity, we have used the commercial device simulator Silvaco/Atlas to study this new device structure and compare it with standard devices.

Silvaco/Atlas is a commercial device simulator originally designed for Si and GaAs device simulations. To correctly simulate GaN devices, a new material library has to be introduced. The main parameters used during this work are shown in table 2.1 [Piprek2007].

Band gap	3.42 eV
Electron mobility	425 cm^2/Vs
Hole mobility	5 cm^2/Vs
Relative permittivity	10.4
N_{c300}	2.2e18 $/cm^3$
N_{v300}	1.16e19 $/cm^3$
affinity	4.1 eV

v_{satn}	2.5e7 cm/s
v_{satp}	1e3 cm/s

Table 2.1 Parameters of GaN used in Atlas simulation

In addition to the material parameters, Atlas does not take into account the polarization effect present in nitride semiconductors. Therefore the polarization induced surface charges in the AlGaN layer have to be included manually. In our simulations, the effect of polarization was simulated by adding two sheets of charges at both sides of each material layer. The electric field induced by the ionized atoms replicates the polarization induced electric field, as long as the doping parameters are chosen correctly.

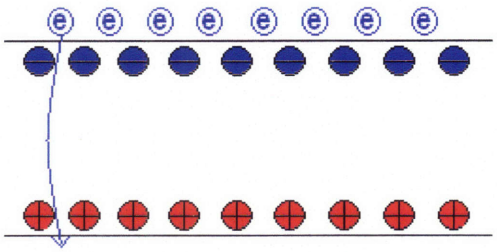


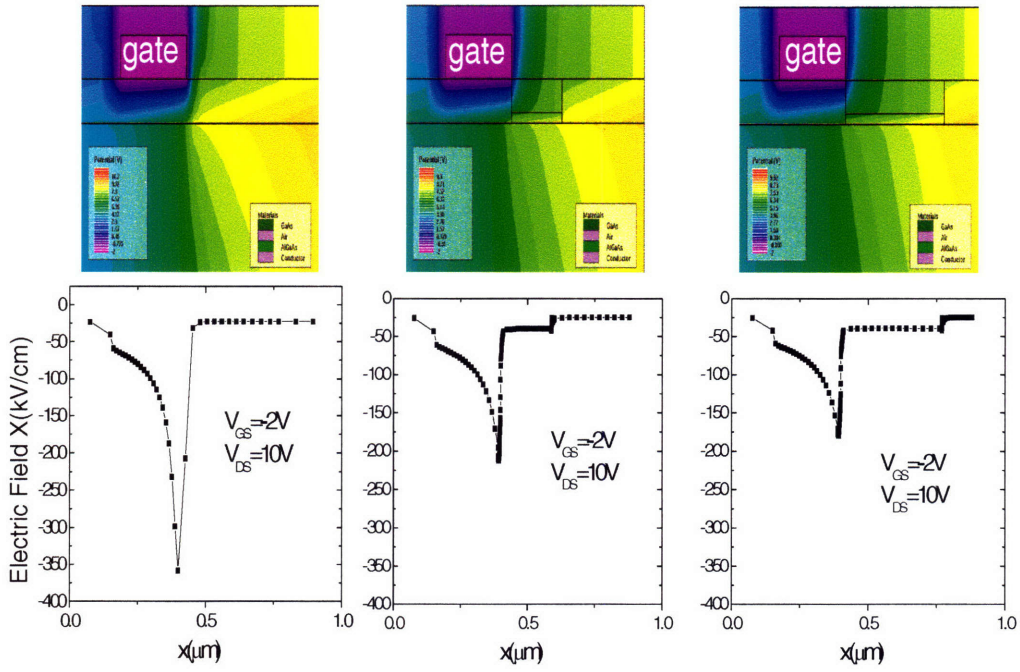
Figure 2.7 Illustration of the polarization charges and the electrons leaving the surface traps for the channel

In real AlGaN/GaN HEMTs, the polarization-induced electric field brings electrons from the surface states to the channel. This phenomenon can be simulated in Atlas using the TRAP model. To calibrate our simulations we calculated the electron density in the channel with the software Bandeng developed by M. Grundmann at UCSB (http://my.ece.ucsb.edu/mgrundmann/bandeng.htm) and we modified the value of the surface charges in the Atlas model until we acquired good agreement in the value of the channel charge density. After this step, the electron density would behave the same as Figure 2.6.

We simulated three device structures: standard AlGaN/GaN HEMT, AlGaN/GaN HEMT with 0.19 μm recessed width and AlGaN/GaN HEMT with 0.37 μm recessed width in the drain access region. The electric field distribution of these devices is shown in Figure 2.8. Using the formula,

$$v_{e,eff} = \frac{L_g}{\int_0^{L_g} \frac{dx}{v_e(x)}}$$

the effective electron velocity is also calculated in these three devices.



(a) without recess (b) recess width=0.19 μm (c)recess width=0.37 μm

Figure 2.8 Electric field distribution in (a) standard device without recess (b) device with a partial recess of 0.19 μm recess width (c) device with a partial recess of 0.37 μm recess width. The effective electron velocities in these three devices are 1.53×10^7 cm/s, 2.36×10^7 cm/s and 2.41×10^7 cm/s, respectively.

As is shown in Figure 2.8, by introducing a partial recess in the drain access region, the peak electric field is reduced from 360 kV/(cm) to 180 kV/(cm), very close to the optimal electric field 150 kV/(cm). Due to the lower electric field, the average electron velocity reaches 2.41×10^7 cm/s, very close to the peak electron velocity and achieving 50% improvement compared with 1.53×10^7 cm/s in standard devices. Moreover, by increasing the recess width from 0.19 to 0.37 μm (comparing (b) and (c)), the electric field is further reduced, but the effect in electron velocity is not as pronounced as that comparing (a) and (b). These results demonstrate, on one hand, that a recess in the drain access region is able to reduce the electric field so as to

improve the effective electron velocity dramatically. On the other hand, the recess width does not need to be very long, which is important to avoid the potential increase of the access resistance, as explained in the next section.

2.3 Potential Challenges

One of the main potential problems of the proposed technology is the possible increase of the effective gate length. To study this effect, we have analyzed whether the electron density underneath the second recess is also modulated by the gate or not. Figure 2.9 shows the electron densities when the gate voltage is -0.5, -1.5 and -3V. As the result indicates, the gate voltage V_{GS} only modulates the electron density below the gate, not the electron density underneath the recessed region, which implies that the effective gate length does not increase with the recess.

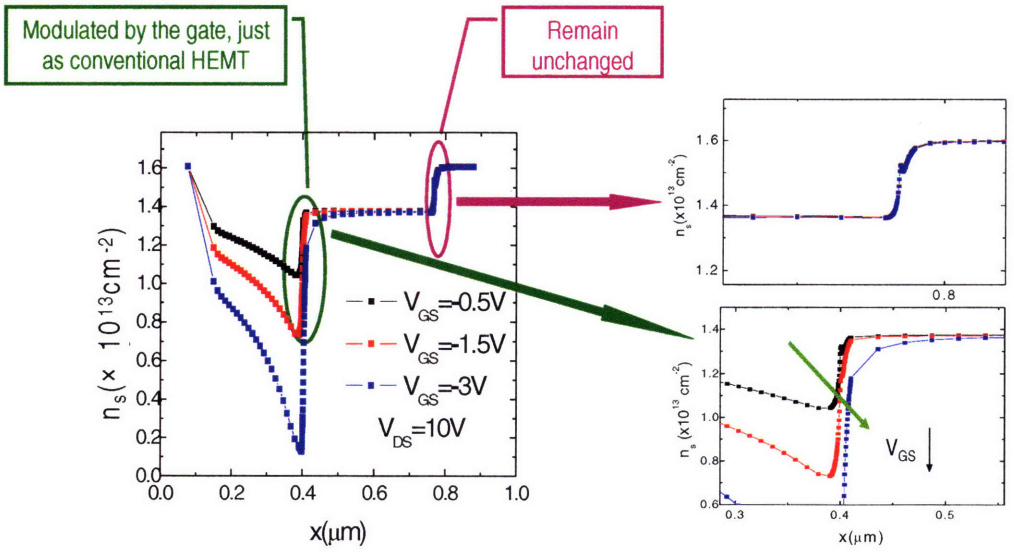


Figure 2.9 Electron densities at different gate voltages. Gate voltage modulates the electron density underneath the gate, with longer effective gate length at lower gate voltage. However, it does not change the electron density profile underneath the recessed region, which means the effective gate length in this new device structure remains the same as standard devices.

The second potential problem with this new structure is the access resistance. It is true that, the lower electron density underneath the recessed drain access region will increase the access resistance. However, the increase is negligible. To the first approximation, the drain access resistance of the device in Figure 2.10 is expressed as

$$R_c = \frac{L_1}{\mu_e \cdot n_1} + \frac{L_2}{\mu_e \cdot n_2}$$

Since L_1 is much smaller than L_2, the second term in the right hand side of the equation is the dominant one, which means the decrease of n_1 only has a minor effect on R_c. For example, in a device with a gate to drain distance of 1 μm and a drain recess of 19 nm, R_c equals 0.0905 Ω·cm in standard devices and 0.0973 Ω·cm in recessed devices with 0.19 μm recess width.

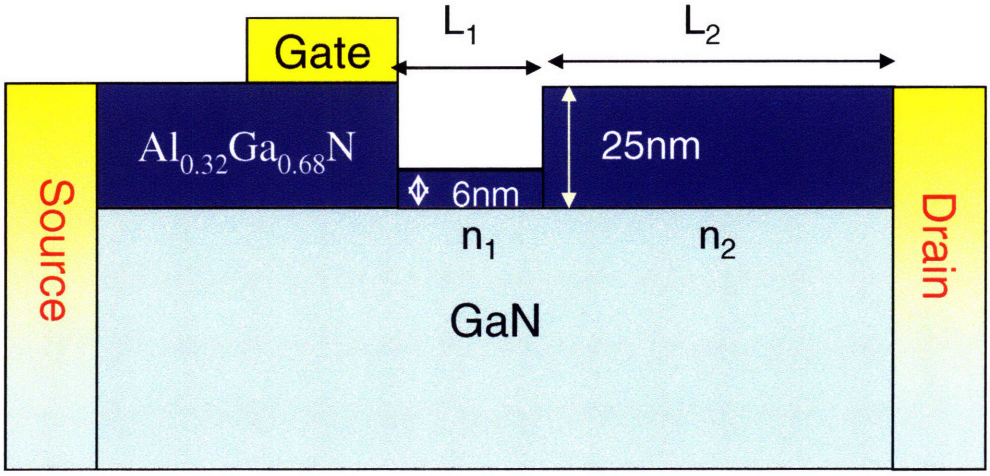


Figure 2.10 AlGaN/GaN HEMT with a partial recess in the drain access region. Since L_1 is much smaller than L_2, decrease of n_1 has negligible effect on the increase of the access resistance

2.4 Device Fabrication

GaN HEMTs with a partial recess in the drain access region can be fabricated in a similar way as standard devices. The process flow is shown in Figure 2.11. Ti/Al/Ni/Au are evaporated and then annealed to form the ohmic contact in the source and drain regions. BCl_3/Cl_2 is explored to do mesa etching. Afterwards, gate recess region is formed using atomic layer etching (will be introduced in chapter 3). Ni/Au/Ni is evaporated but not annealed to form gate Schottky metal. A second recess in the drain access region is self aligned to the gate metal. Finally, SiN passivation layer and pads are formed to finish the process flow.

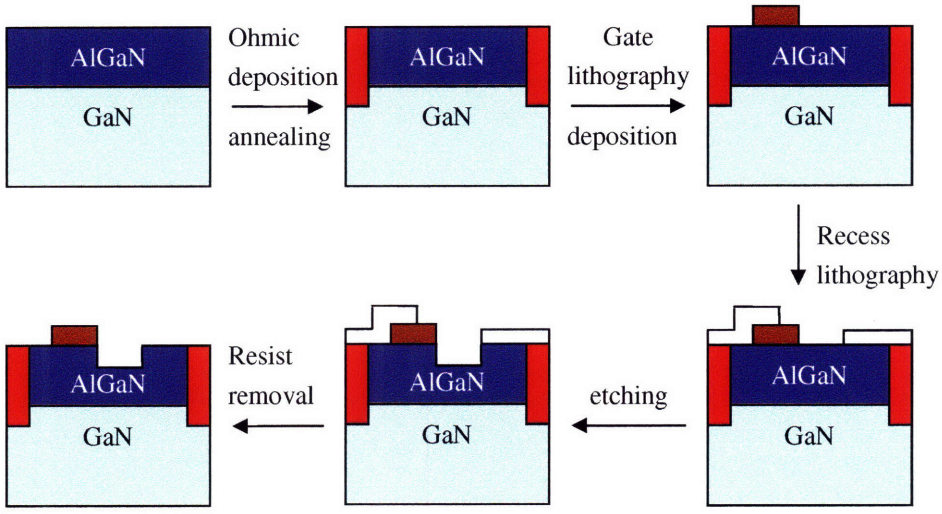


Figure 2.11 the process flow of GaN HEMTs with a partial recess in the drain access region

2.5 Similar Approaches in other materials

The partial recess proposed in this thesis is somehow similar to the double recess used in GaAs and InP devices reported in the literature. In 1991, Huang et al. demonstrated a double recessed 0.2 μm gate length $Al_{0.24}GaAs/In_{0.16}GaAs$ pseudomorphic HEMT (device structure shown in Figure 2.12) with 500 mW of output power, 6-dB gain and 35% PAE at 32 GHz. At 44 GHz, the device exhibited 494 mW of output power, 4.3-dB gain and 30% PAE [Huang1991].

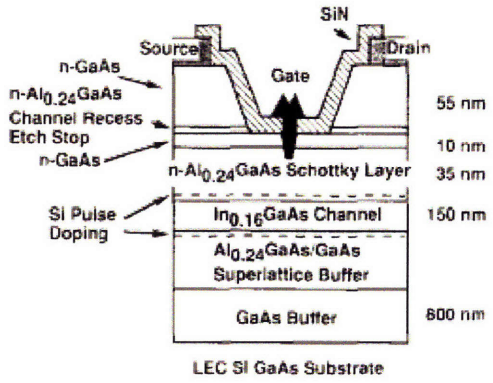


Figure 2.12 Schematic of reported AlGaAs/InGaAs PHEMT

Later, Hur applied this technique to InP devices [Hur1995]. By comparing the DC and

RF characterisitcs of double recessed and single recessed AlInAs/GaInAs/InP HEMTs, it is found that double recessed HEMTs have higher breakdown voltages, lower input and feedback capacitance, higher f_T and f_{max}.

Built upon the success of double recessed structure in GaAs and InP devices and the very promising simulations presented in this chapter, we are confident of our proposed structure in improving both the frequency performance and the breakdown voltage of GaN HEMTs.

2.6 Summary

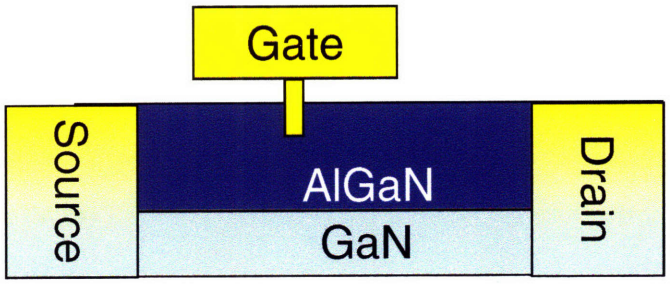
To summarize, we have introduced a new method to engineer the electric field in the drain access region of GaN HEMTs. The use of drain recesses allows a 50% decrease of the peak electric field and 50% increase of the average electron velocity while the effective gate length remains the same as standard devices. Access resistance only increases by 5%. This approach also represents a new way to increase the breakdown voltage, which is very important in higher voltage applications and in ultra-short devices. Electric field engineering gives us a new degree of freedom to design high performance AlGaN/GaN HEMTs.

Chapter 3: Atomic Layer Etching

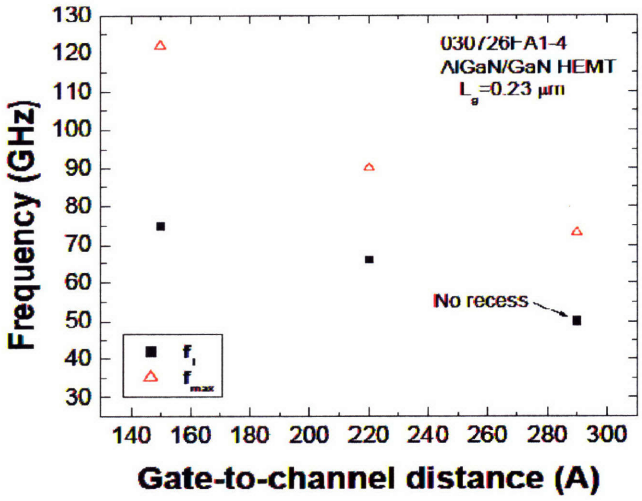
3.1 Motivation

GaN is a very promising candidate for high frequency power amplifiers. However, its difficult technology is hindering many potential applications. One critical processing shortcome in nitride technology is the lack of a reliable etching technology. The lack of a uniform, controllable and low damage etching technology has limited the use of technologies such as gate recesses, common in other semiconductor materials, to improve the performance of commercial devices.

With transistor gate length dimensions becoming shorter and shorter, short channel effects have started to severely limit the device performance. To mitigate these short channel effects and to improve the high frequency performance, one approach widely used in conventional transistors is to increase the gate-to-channel aspect ratio by performing gate recesses. The important effect of gate recess in the current gain cutoff frequency f_T and power gain cutoff frequency f_{max} is shown in Figure 3.1. Without gate recess, f_T and f_{max} are only 50 GHz and 73 GHz, respectively. After reducing the gate-to-channel distance to 14 nm, f_T and f_{max} reach 75 GHz and 122 GHz respectively. In fact, a gate to channel distance of 14 nm is still high compared to the value used for InGaAs HEMT devices [Kim2005], which means there is still a lot of room for improvement. However, in order to control the gate recess depth accurately, a uniform, controllable and low damage etching technology is highly desirable.



(a)



(b)

Figure 3.1 (a) a standard AlGaN/GaN HEMT with gate recess
(b) The current gain cutoff frequency and power gain cutoff frequency as a function of the gate-to-channel distance. Without doing recess, f_T and f_{max} are only 50 GHz and 73 GHz, respectively. After a gate recess to 14 nm gate-to-channel distance, f_T and f_{max} reach 75 GHz and 122 GHz respectively. In state of the art InGaAs HEMTs, gate-to-channel distances as low as 4nm have been reported.

The second potential application of accurate recess technology in nitrides is the electric field engineering described in chapter 2. One of the reasons why the high frequency performance of GaN HEMTs is well below the theoretical predictions is the very high electric field common in the channel of these devices reduces the electron velocity. As shown in chapter 2, drain recesses are very useful to reduce the electric field in this region. As in the case of gate recess, electric field engineering is only plausible through a uniform, controllable and low damage etching technology.

Table 3.1 lists some available etching technologies for GaN. They use either Cl_2, Ar, BCl_3 or SF_6 gases, but none of them offer the required level of reproducibility, depth control and low damage required by commercial applications

[Buttari2002][Shul1995][Kim1999][Feng1996]. Therefore, in this thesis project, we developed a completely new etching technology for GaN, Atomic Layer Etching (ALE), with the potential of overcoming the difficulties mentioned before.

	Pros	Cons
Cl_2 reactive ion etching (RIE)	1. low damage 2. breakdown voltage unchanged	1. no etch stop layer 2. nonlinear with the etch time 3. increase gate leakage
$Cl_2/H_2/CH_4/Ar$ ECR or ICP	1. low damage 2. highly anisotropic 3. high etch rate	1. no etch stop layer 2. rough surface
BCL_3/Cl_2	1. high etching rate 2. uniform etch rate	1. no etching stoppers
Selective etching by SF_6/BCl_3	1. selective etch	1. selectivity between GaN and AlGaN is only 10:1 2. does not work on AlGaN/GaN structures

Table 3.1 the available etching technologies that are currently being used. They all have pros and cons. None of them offer the level of accuracy, reliability and low damage, which is required in advanced device fabrication.

3.2 Atomic Layer Etching

Figure 3.2 illustrates the flow chart of our new ALE technology for GaN etching. First, the etching chamber is carefully cleaned and the oxide on GaN sample surface is removed before the sample is loaded into the etching chamber. Then Cl_2 is fed into the chamber. By introducing plasma into the chamber, Cl_2 is adsorbed onto the GaN surface. Then, the excess Cl_2 is pumped out of the chamber, leaving only a single layer of Cl_2 adsorbed on the surface. Next, the adsorbed Cl_2 is activated through either an Ar or Ne plasma, high energy illumination or high temperature. The activated Cl_2 reacts with the Ga on the surface of GaN to form $GaCl_3$. As $GaCl_3$ is volatile, it is subsequently pumped out of the chamber. It is important to note that in this etching technology only the top GaN monolayer is etched in each cycle, although the process can be repeated as many times as needed to etch the desired number of GaN

monolayers.

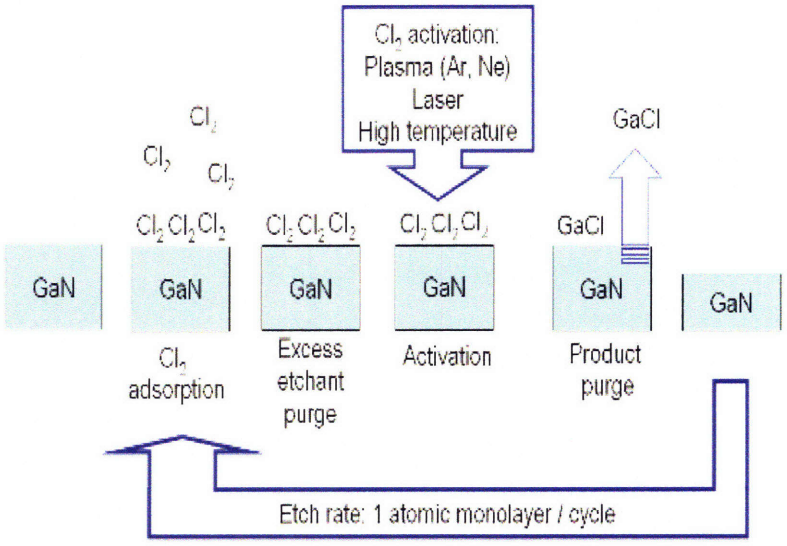


Figure 3.2 Basic process flow of the proposed atomic layer etching.

The etching system used in this project is an Electron Cyclotron Resonance (ECR) Reactive Ion Etcher (Figure 3.3). This system can apply both the ECR power and RF power. ECR power ranges from 0 to 700W and RF power ranges from 0 to 50W. ECR power is manually tuned, while the tuning of the RF power is automatic. There is also a one to one relation between the RF power and the RF bias voltage.

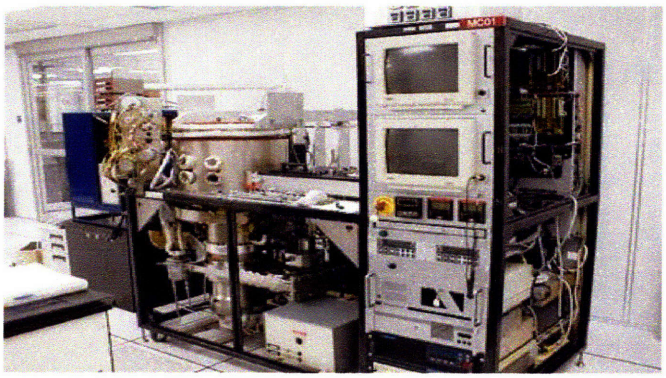


Figure 3.3 Electron Cyclotron Resonance (ECR) Reactive Ion Etcher available in the TRL laboratory of MTL.

In all the etching studies presented in this chapter we used a photolithography mask made of several hundreds of 80 μm×80 μm squares with 40 μm spacing (Figure 3.4). Since image reversal photolithography is used, the region inside the squares will be etched away.

Figure 3.5 shows the process flow of the ALE technology developed during this project. To make sure the process works as expected, several key issues have to be investigated. First, we need to get Cl_2 adsorbed onto the sample surface. Otherwise, the etching will become a pure Ar sputtering process. Second, a proper Ar plasma power has to be selected. If the Ar plasma power is too high, it will introduce excess pure Ar sputtering. On the other hand, if the plasma power is too low, the power will not be sufficient to remove the $GaCl_3$ from the surface. Finally, it is important to demonstrate that this etching technology is indeed a self limited process with low surface damage and high reliability. All these issues will be studied and resolved in the following sections.

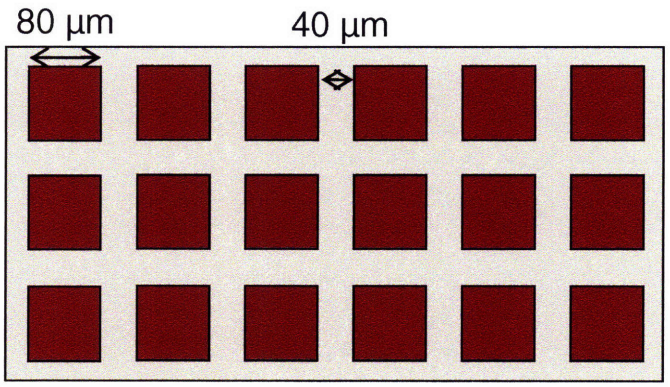


Figure 3.4 Diagram of the photolithography mask used in this study.

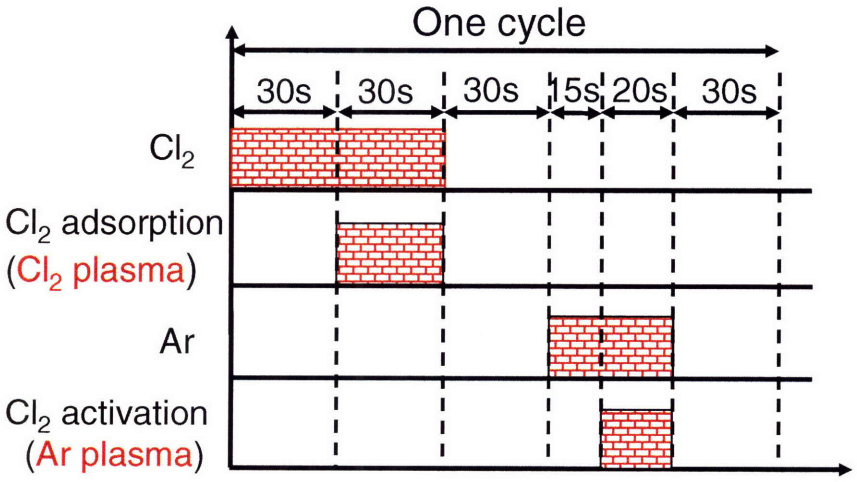


Figure 3.5 Illustration of the ALE recipe in one cycle. The etching times are only examples as in this work we have varied them.

3.3 Cl_2 adsorption: XPS Measurement

One of the key steps in the ALE process is the correct adsorption of Cl_2 onto the GaN surface. To study this adsoption, we prepared three samples to analyze with X-ray Photoelectron Spectroscopy (XPS) measurement. The first sample (sample A) is a fresh un-treated GaN sample. The second sample (sample B) is a GaN sample exposed to Cl_2 gas and the third sample (sample C) is a GaN sample exposed to Cl^- ions. The conditions for each one of these experiments are listed in Table 3.2. All of the samples were loaded into a vacuum desiccator immediately after the gas treatment to prevent surface contamination before the XPS measurement.

To study the adsorption of Cl_2 on the surface, we looked at the Cl_2 binding energy in the XPS spectrum. Neither sample A nor sample B showed any significant signal in the XPS spectrum at the energy corresponding to the Cl_2 binding energy. (Cl_2 binding energy is around 200 eV) (Figure 3.6). On the other hand, the sample exposed to Cl_2 plasma (sample C) showed a clear signal resulting from the Cl_2 gas adsorbed onto its surface (Figure 3.7). Therefore, Cl_2 plasma (i.e. Cl^- ions) is needed to get Cl_2 adsorbed onto the sample surface. To avoid pure Cl_2 physical sputtering or chemical etching, the Cl_2 plasma needs to have ultra low power. In the rest of this study, a plasma voltage of 20 V will be used. The etch rate of 20 V Cl_2 plasma is below 0.01 Å/s.

Sample 1	Original GaN sample
Sample 2	GaN sample exposed to Cl_2 gas ➢ Cl_2 30sccm 30mtorr 30s ➢ Pump 30s
Sample 3	GaN sample exposed to Cl- ions ➢ Cl_2 30sccm 30mtorr 30s ➢ Cl_2 30sccm 30mtorr 20V 30s ➢ Pump 30s

Table 3.2. Samples used to study the adsorption of Cl_2 onto the GaN surface.

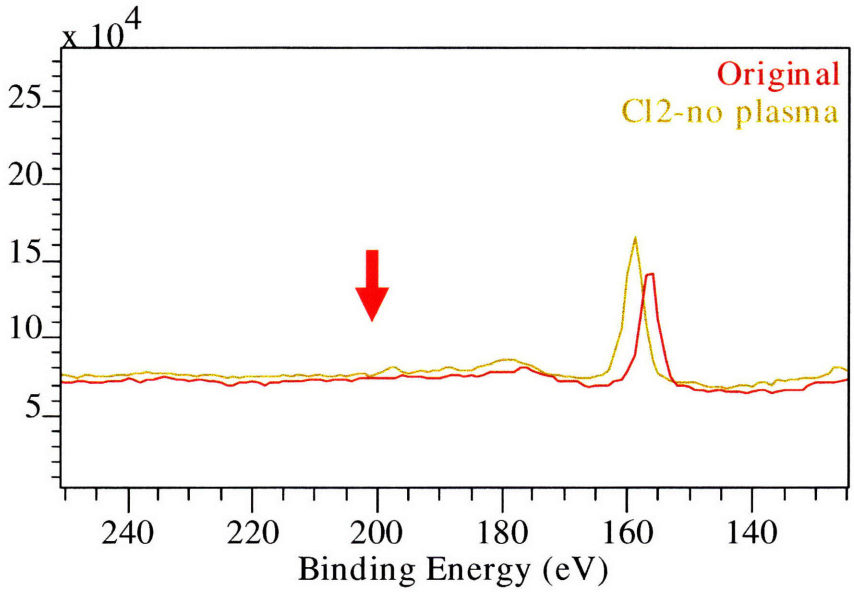


Figure 3.6. the XPS measurement results from the first two samples. Cl_2 binding energy is at around 200 eV.

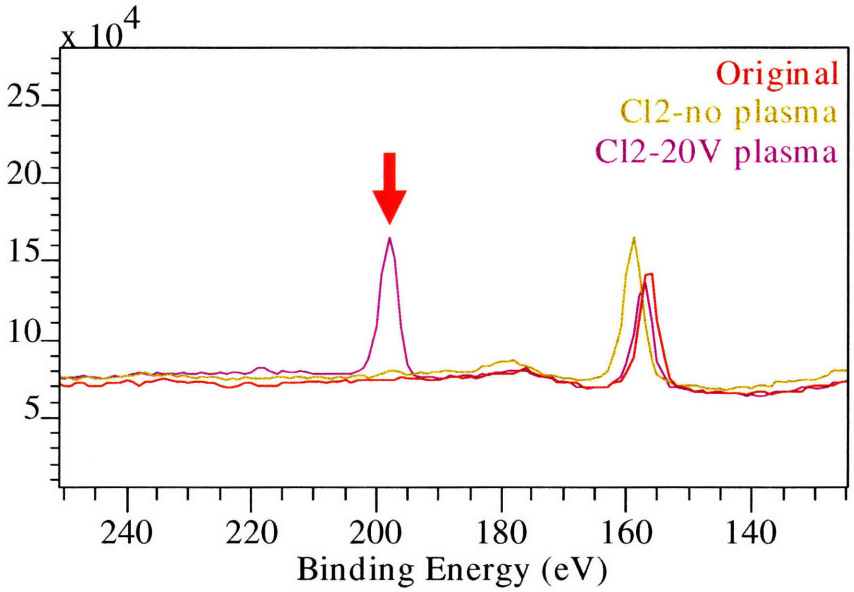


Figure 3.7 the XPS measurement results for the three samples. Cl_2 binding energy is at around 200 eV.

3.4 Minimum power for etching

It is important to select the power of the Ar plasma needed to activate Cl_2 properly. On

one hand, the power needs to be high enough to activate the etching gas. On the other hand, the power should be as low as possible to minimize the plasma damage and sputtering etching. To find the optimum plasma conditions, we first characterized the etching rate from pure Ar sputtering, which is shown in Figure 3.8.

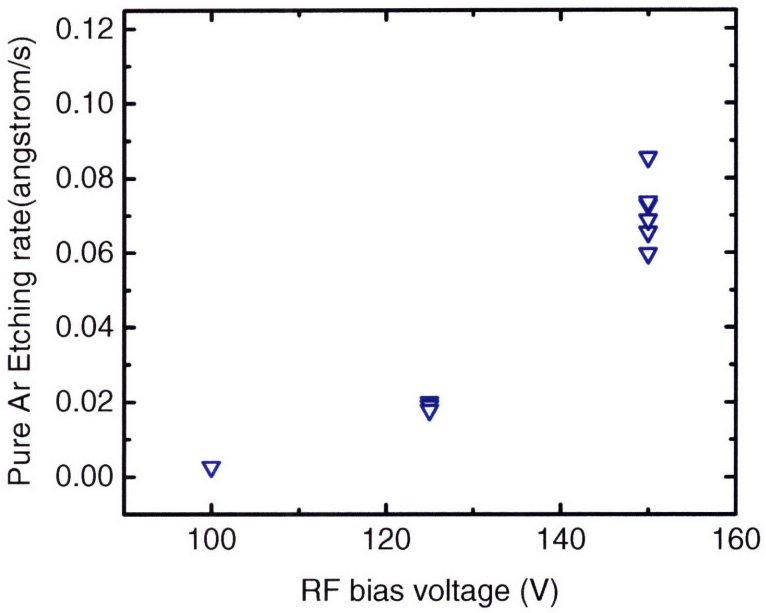


Figure 3.8 the pure Ar etching rate as a function of the RF bias voltage

Then we characterized the etching rate per cycle using the following ALE recipe:

Gas	Flow rate	Pressure	RF bias voltage	Time
Cl_2	30sccm	30mtorr		30s
Cl_2	30sccm	30mtorr	20V	30s
--				30s
Ar	30sccm	30mtorr		15s
Ar	30sccm	30mtorr	varies	20s
--				30s

Table 3.3 ALE recipe for one etching cycle.

The etching rate per cycle is shown in Figure 3.9. To find out the etching rate due to Cl_2 adsorption and $GaCl_3$ removal, we need to subtract the contribution from pure Ar sputtering. Figure 3.10 shows the two results in the same graph. As shown, at 100V and 125V RF bias voltage, Ar plasma does not have enough power to activate Cl_2, so

there is no difference between the total etching rate in atomic layer etching and the pure Ar etching rate. However, at 150V RF bias voltage, the Ar plasma has enough energy to activate Cl_2 and we see a clear difference between the total ALE etching rate and the pure Ar etching rate. Therefore, 150V is the minimum power that allows the full activation of the adsorbed Cl_2 layer. In what follows, we will use 150V Ar bias voltage.

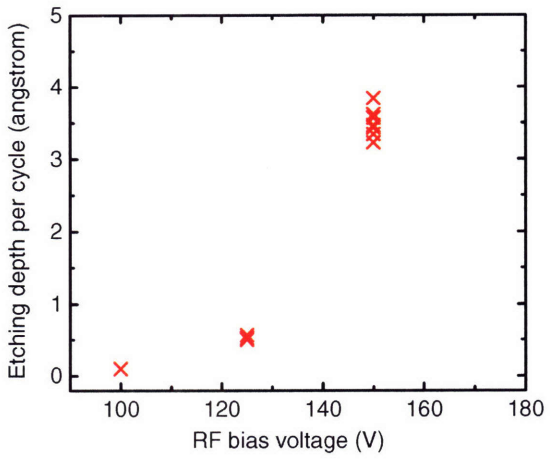


Figure 3.9 the ALE etching depth per cycle as a function of the RF bias voltage

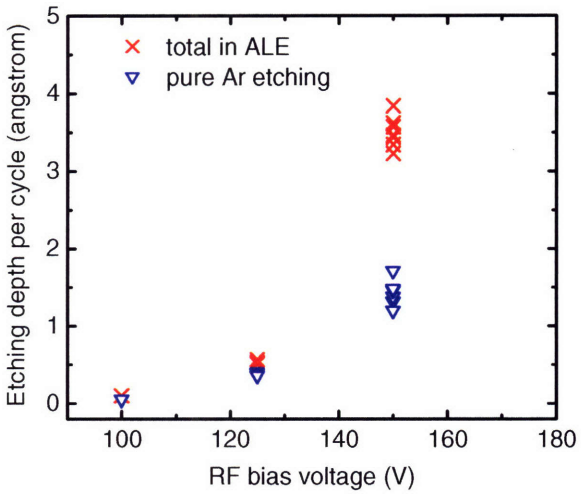


Figure 3.10 the etching depth per cycle as a function of the RF bias voltage. At 100V and 125V, there is no difference between the total ALE etching depth and pure Ar etching depth, indicating that the Ar plasma does not have enough power to activate Cl_2. While at 150V RF bias voltage, we see a clear difference between the total ALE etching rate and the pure Ar etching rate. This difference must come from the Cl_2 adsorption.

3.5 Amount of Cl_2 on the GaN surface

In the previous section, we have demonstrated that, using 20V Cl_2 plasma, Cl_2 can be adsorbed onto the GaN surface. On the other hand, 150 V Ar RF bias voltage is needed to activate this adsorbed layer of Cl_2. The next step in the development of the ALE process consisted in proving that the ALE is a self limited process, which means the etching depth per cycle due to ALE should saturate with the Ar plasma time after the removal of the top GaN monolayer. However, if too much Cl_2 is adsorbed on the GaN surface, the ALE process will remove more than one GaN monolayers and the etching depth will not saturate with time.

To understand the effect of the amount of Cl_2 adsorbed on the GaN surface on the etch depth, three different etch conditions were studied. Table 3.4 shows the different conditions used.

Gas	Flow rate	Pressure	RF bias voltage	Time
Cl_2	30sccm	30mtorr		30s
Cl_2	30sccm	30mtorr	20V	30s
No				30s
Ar	30sccm	30mtorr		15s
Ar	30sccm	30mtorr	150V	varies
No				30s

(a)

Gas	Flow rate	Pressure	RF bias voltage	Time
Cl_2	30sccm	30mtorr		30s
Cl_2	30sccm	30mtorr	20V	12s
No				30s
Ar	30sccm	30mtorr		15s
Ar	30sccm	30mtorr	150V	varies
No				30s

(b)

Gas	Flow rate	Pressure	RF bias voltage	Time
Cl_2 and Ar	Cl_2 5sccm Ar 10sccm	15mtorr		30s

Cl_2 and Ar	Cl_2 5sccm Ar 10sccm	15mtorr	20V	12s
No				30s
Ar	30sccm	30mtorr		15s
Ar	30sccm	30mtorr	150V	varies
No				30s

(c)

Table 3.4 Process conditions used to study the effect of changing the amount of adsorbed Cl_2 on the ALE process. Condition (b) uses shorter Cl_2 plasma time (12s) compared to 30s in condition (a). While in condition (c), Cl_2 is mixed with Ar, at the same time, the pressure is reduced from 30 mtorr to 15 mtorr.

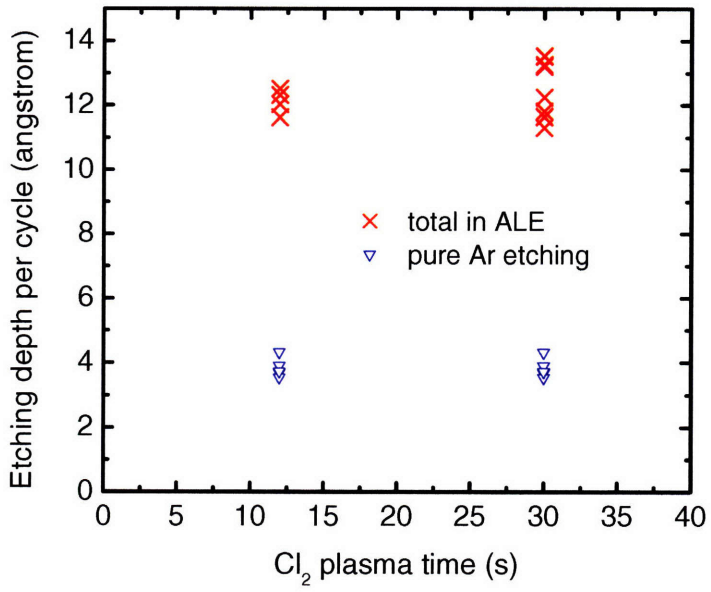


Figure 3.11 the etching results from condition (a) and condition (b). The Ar plasma time is 60s for both conditions.

Figure 3.11 shows the etching results from condition (a) and condition (b) both with a 60s Ar plasma time but different Cl_2 plasma time. The etching rate is found to be independent of the Cl_2 plasma time.

The etching results for condition (a) and (c) are then compared in Figure 3.12. As is

seen, for condition (a), the atomic layer etching depth per cycle does not saturate for Ar etching times as long as 60s. This behavior is due to an excessive amount of Cl_2 being adsorbed on the GaN surface. Therefore, it is not as we expected that only one layer of Cl_2 is adsorbed, but Cl_2 actually accumulates and forms multi-layers on top of sample surface.

The etch behavior is completely different for condition (c). By mixing Cl_2 with Ar in the first two steps of each cycle and at the same time reducing the pressure to 15mtorr, the amount of Cl_2 adsorbed onto the sample surface is reduced. In this case, the etching rate per cycle almost saturates with increasing the Ar plasma time (Figure 3.12), which demonstrates that this etching recipe produces a self limited process.

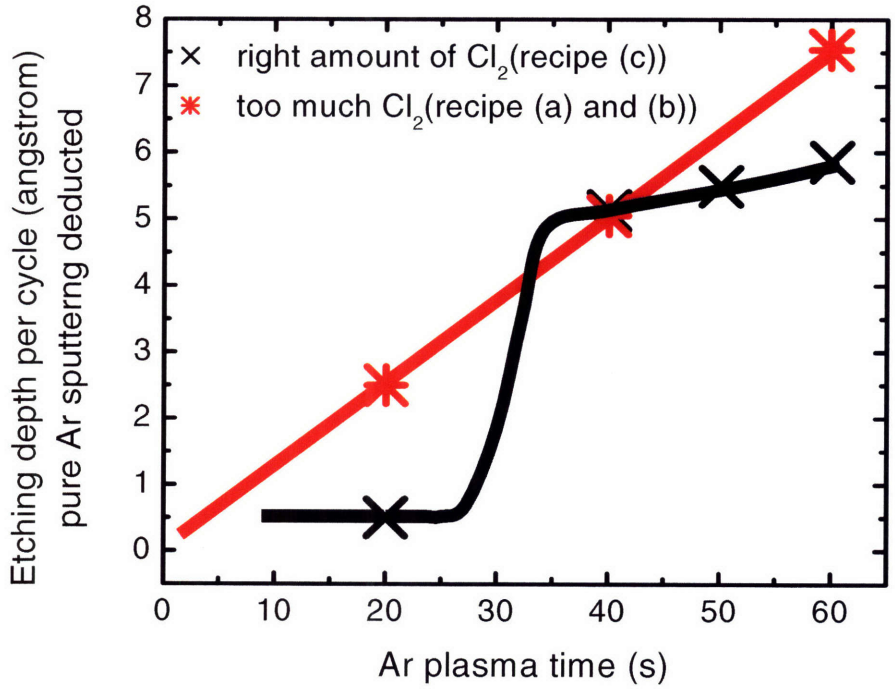


Figure 3.12 the etching depth per cycle in the ALE process subtracting the pure Ar sputtering versus Ar plasma time. If there is too much Cl_2 adsorbed as in condition (a) and (b), the ALE etching rate does not saturate with the Ar plasma time. After we reduced the Cl_2 adsorbed in condition (c), the etching depth per cycle reaches saturation with the Ar plasma time after a 20-30s stabilization period.

3.6 Low damage etching

To study the morphological damage of this new etching technology, we have analyzed the surface morphology of the samples before and after ALE process (Figures 3.13 and 3.14). After a 60 cycles etch, the RMS surface roughness is 0.66nm in a 10 μm^2 surface area, compared to an original value of 0.60 nm in fresh un-etched samples. The minimum change in surface roughness proves the very low morphological damage characteristic of atomic layer etching.

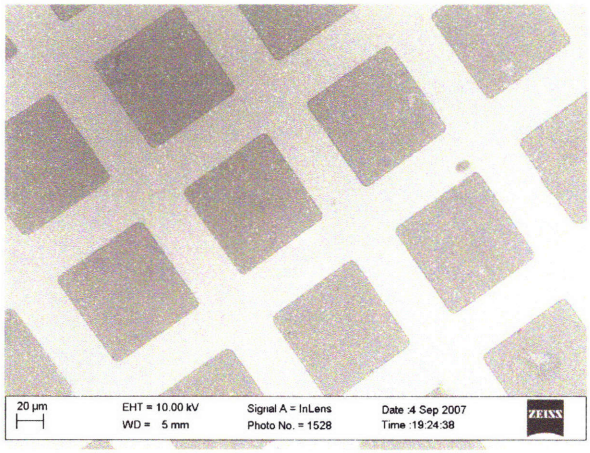


Figure 3.13 SEM image of the GaN sample after etching

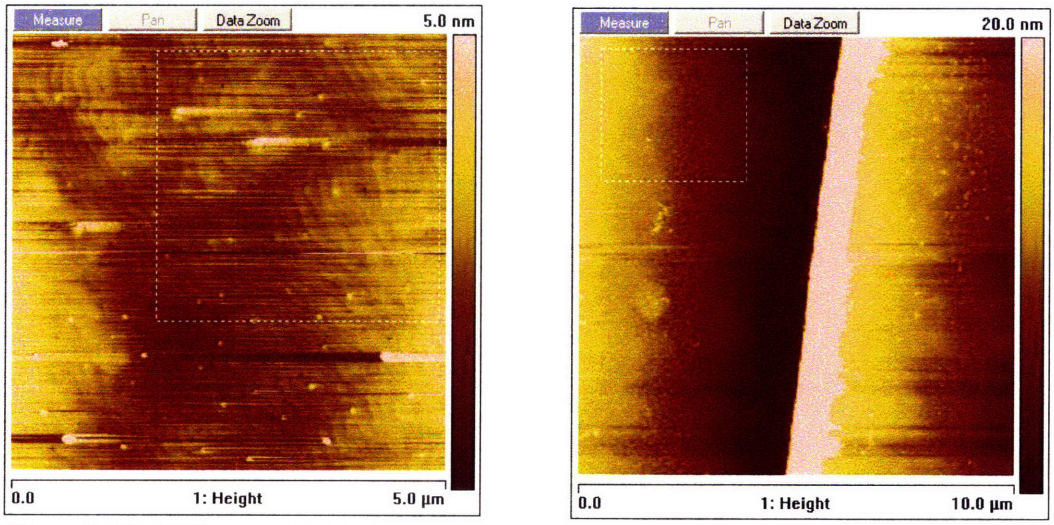


Figure 3.14 AFM image of GaN sample before and after etching. The RMS surface roughness after etching is 0.66 nm in 10 μm^2 surface area, compared with the value of 0.60 nm before etching.

3.7 Reliability

To increase the reproducibility of the new Atomic Layer Etching technology, we have developed a cleaning procedure to condition the etching chamber before starting the actual etching. This conditioning process consists of the following steps:

1. Run recipe ETCHCLN

O_2 15sccm He 15sccm CF_4 40sccm 15mtorr 30s

O_2 15sccm He 15sccm CF_4 40sccm 15mtorr ECR=50W RF=50W 5s

O_2 15sccm He 15sccm CF_4 40sccm 15mtorr ECR=300W RF=50W (about 437V bias) throttle valve about 50.0% 600s

2. Run recipe called BCL3PURG

BCl_3 50sccm 600s

3. Run recipe called ALETCH

BCl_3 30sccm Cl_2 20sccm 40mtorr 30s

BCl_3 30sccm Cl_2 20sccm 40mtorr ECR=50W RF=20W 5s

BCl_3 30sccm Cl_2 20sccm 40mtorr ECR=450W RF=20W (280V) throttle valve 42.5% 120s

4. Load a dummy wafer to keep the condition similar every time

5. Preconditioning the chamber

6. Oxide strip the GaN sample

7. Immediately load the GaN sample into the etching chamber

8. Run recipe called BCL3RF

BCl_3 10sccm 10mtorr 15s

BCl_3 10sccm 10mtorr RF=10W 60s

9. Run the Atomic Layer Etching recipe for as many times as needed at 80°C.

By using the above preconditioning recipe, the reproducibility of the ALE process was greatly improved.

3.8 Summary

The etching technology developed in this thesis is the first demonstration of Atomic Layer Etching in nitride semiconductors. This new etching technique has been shown to allow reproducible dry etching of AlGaN/GaN heterostructures with atomic layer depth resolution if the Cl_2 adsorption on the surface is carefully controlled. To achieve reproducible Cl_2 adsorption, we have demonstrated that an untra-low-power plasma is needed. Also to control the Cl_2 adsorbed and achieve atomic layer etching it is important to dilute the reactive Cl_2 gas with an inert gas such as Ar. In this way, the dry etching process is self-limited and unprecedented depth resolution and reproducibility are achieved with minimal surface damage This new etching technology is extremely promising for multiple technological processes in GaN devices such as gate recess and electric field engineering.

Chapter 4: Schottky Drain Contact

4.1 Motivation

As mentioned in the previous chapter, one of the main factors limiting the frequency performance of GaN HEMTs is their relatively large parasitic capacitances and resistances. As shown by Tasker [Tasker1989], the maximum current gain cutoff frequency f_T is determined by the transconductance g_m (which is proportional to the electron velocity), parasitic capacitances C_{gs}, C_{gd} and the parasitic resistances R_s, R_d and R_{ds}:

$$f_T = \frac{g_m / 2\pi}{[C_{gs} + C_{gd}][1 + (R_s + R_d)/R_{ds}] + C_{gd} \cdot g_m \cdot (R_s + R_d)}$$

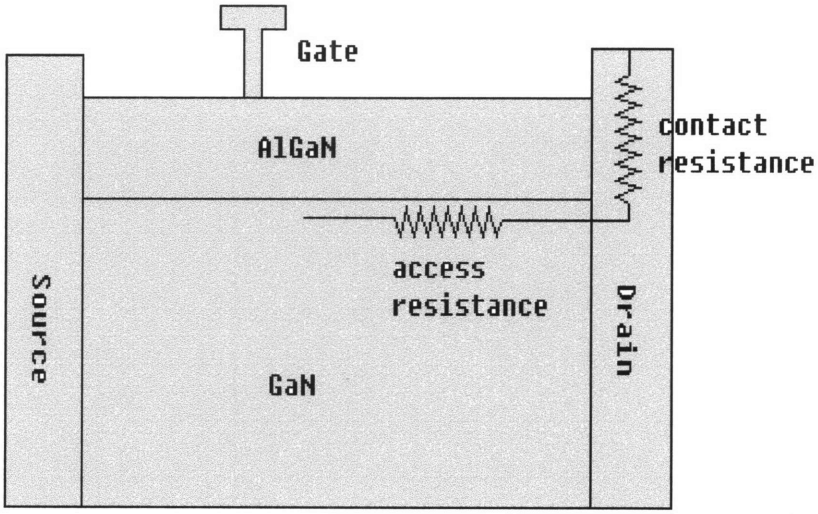
Table 4.1 lists those parameters in today's 100 nm gate length technology. To improve f_T, as well as f_{max} (which is closely related to f_T), it is necessary to either increase the transconductance and/or to reduce the parasitic capacitances and resistances. Two techniques to improve g_m include the use high k dielectrics [Luo2002][Mehandru2003] [Balachander2005][Yagi2006] and the use of 2D nanowire heterostructures [Li2006] to improve the electron confinement. On the other hand, to reduce C_{gs} and C_{gd}, new device and gate geometries are necessary. Finally, to reduce the parasitic resistances, self aligned structures, new contact schemes and electric field engineering are several of the possible approaches. In this thesis, we propose a new concept to reduce R_d: *Schottky drain contacts.*

C_{gs}	0.75 pF.mm	R_s	0.6 Ω.mm
C_{gd}	0.20 pF.mm	R_d	1.3 Ω.mm
R_g	18 Ω/mm	$g_{m,ext}$	0.6 S/mm

Table 4.1 Parameters of parasitics and transconductance in today's 100 nm gate length GaN HEMTs for 40 GHz applications. The cutoff frequency of these devices are f_T=153 GHz and f_{max}=185 GHz

4.2 Conventional technologies to reduce drain parasitic resistance

The drain parasitic resistance (R_d) consists of two components: the contact resistance between the metal contact and the channel and the access resistance due to the distance between the gate edge and drain contact, as illustrated in Figure 4.1. In the literature there are several ways to reduce R_d. One approach is to grow n^+ cap layer on the top of AlGaN layer. Non annealed ohmic contacts with ultra low resistance can be formed to this layer. In 2005, W. Wang compared the performance of recessed GaN HEMTs with a n^+ cap layer to conventional GaN HEMTs [Wang2005]. Their device structures are shown in Figure 4.2 and their small signal parameters are listed in Table 4.2. As shown in the table, using a n^+ cap layer, R_s and R_d are improved from 26 Ω and 38 Ω to 17 Ω and 23 Ω, respectively. As a result, f_T and f_{max} increase from 37 GHz and 50 GHz to 43 GHz and 68 GHz, respectively. Despite the improvement, the addition of this top n^+ layer degrades the surface morphology, which will degrade the device performance and reliability.



access resistance+contact resistance=drain parasitic resistance

Figure 4.1 Illustration of the contact resistance and access resistance in AlGaN/GaN HEMTs. The access resistance is introduced by the distance between the gate edge and drain contact.

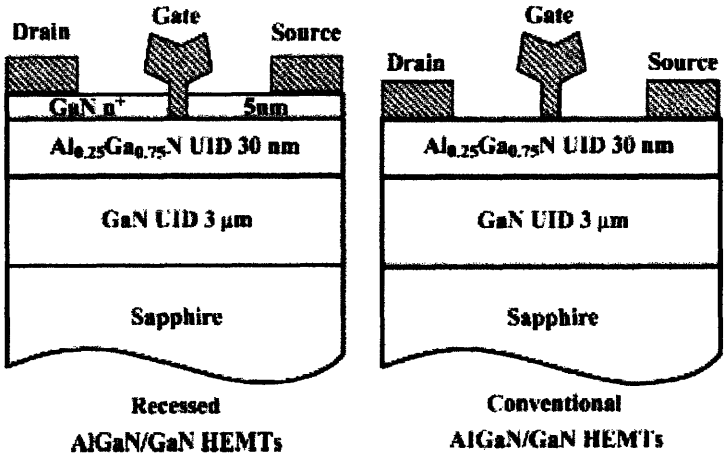


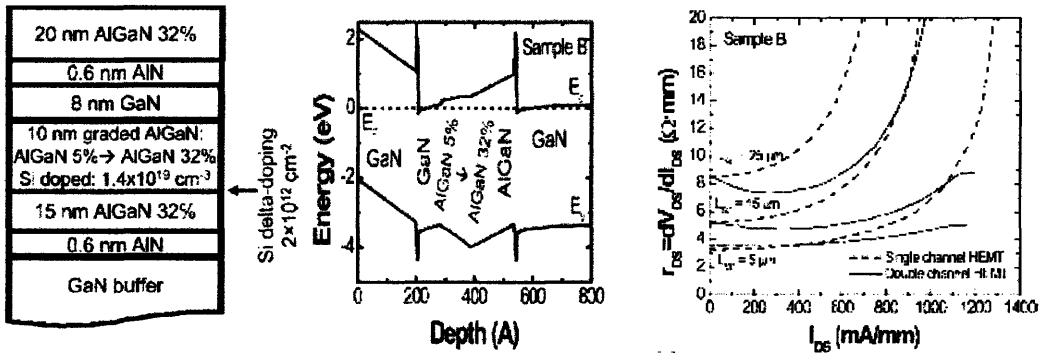
Figure 4.2 Device cross-sectional structures of the recessed GaN HEMT with a n^+ cap layer and the conventional GaN HEMT

Parameter	Recessed GaN HEMTs	Conventional GaN HEMTs
R_s (Ω)	17	26
R_d (Ω)	23	38
R_g (Ω)	6	7
R_i (Ω)	8	22
R_{ch} (Ω)	600	800
C_{gs} (fF)	37	35
C_{gd} (fF)	14	13.5
C_{ds} (fF)	2	2.1
$g_{m,ext}$ (mS/mm)	280	240
f_T (GHz)	43	37
f_{max} (GHz)	68	50

Table 4.2 Small signal device parameters comparisons between the recessed GaN HEMT with a n+ cap layer and the conventional GaN HEMT

The second approach to reduce the access resistances is to use multiple channels (Figure 4.3(a)). Figure 4.3(b) shows the band diagram and Figure 4.3(c) the device characteristics of a multichannel transistor compared with single channel device [Palacios2004][Palacios2006]. The use of multiple channels increases the electron density in the channel to $2.9\times10^{13}cm^{-2}$. This approach allows an important improvement in access resistances as shown in Figure 4.3(c). However, it is important

to note that for this approach to be useful, the correct design of the device band diagram is critical to allow good communication between the different channels.



(a) (b) (c)

Figure 4.3 Use of multiple channels to reduce the access resistance in GaN HEMTs

Another approach to reduce the access resistances is to use ion implantation in a way similar to Silicon technology, as shown in Figure 4.4 [Recht2006]. Source and drain areas were implanted with a Si dose of $1\times10^{16}cm^{-2}$ and were activated at ~1260°C in a metal-organic chemical vapor deposition system in ammonia and nitrogen at atmospheric pressure. Nonalloyed ohmic contacts to ion-implanted devices showed a contact resistance of 0.96 Ω·mm to the channel. An output power density of 5 W/mm was measured at 4 GHz, with 58% power-added efficiency and a gain of 11.7 dB at a drain bias of 30 V. This is a simple technique which allows great flexibility and low resistances, however, it has the drawback of requiring a very high activation temperature to recover the damage induced by the implanted species.

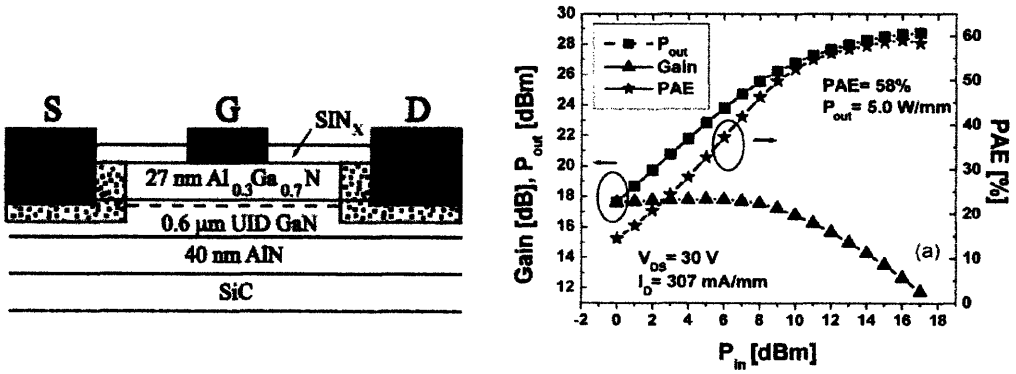


Figure 4.4 Use of implantation to reduce the contact resistance in GaN HEMTs

As we have seen, none of the traditional approaches is perfect. New ideas are required

to solve the critical issue of reducing access resistances. In this thesis project, we propose a new drain contact technology based on the use of a Schottky metallization in the drain contact. This new technology allows a significant reduction in both the contact and access resistances.

4.3 Ohmic and Schottky drain contact technology

Figure 4.5 illustrates the I-V characteristics of typical ohmic and Schottky contacts. The resistance for these two types of contacts changes with current in a very different way. While in ohmic contacts, the resistance remains constant for low and medium current levels and then it increases, in Schottky contacts, the differential resistance is inversely proportional to the current:

$r_c = mk_BT / qI$,

where r_c is the differential resistance, m is the ideality factor, k_B is the Boltzmann constant, T is the temperature, q is the unit charge and I is the current. For moderate current levels, this contact resistance is much lower than what is achievable with conventional ohmic technology (Table 4.3) which make this Schottky contact very interesting for the drain contact of a transistor, as in these devices the contact is always operating in the first quadrant of the I-V curve.

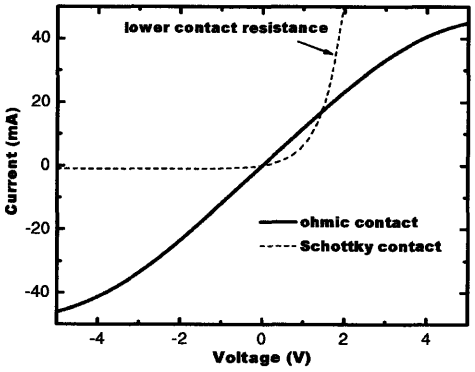


Figure 4.5 I-V characteristics of ohmic contact and Schottky contact. In high frequency applications, the differential resistance of Schottky contact is lower than that of ohmic contact at moderate and high current levels.

Id (mA)	Rc (ohmic)	Rc (Schottky)
10	> 0.6 Ω·mm	1.17 Ω·mm
50	> 0.6 Ω·mm	0.23 Ω·mm
100	> 0.6 Ω·mm	0.11 Ω·mm

Table 4.3 contact resistances of ohmic and Schottky contacts.

In addition to their better differential resistance, the low thermal budget required in Schottky contacts makes this technology very useful for self-aligned gate structures such as the one illustrated in Figure 4.6 to further reduce the access resistance. Therefore, in high voltage applications, Schottky drain contact has the potential to outperform the ohmic contact in both contact resistance and access resistance. This technology however can not be applied to GaAs HEMTs due to the much lower bias voltages of these devices, which make the voltage drop in the Schottky contact inadmissible.

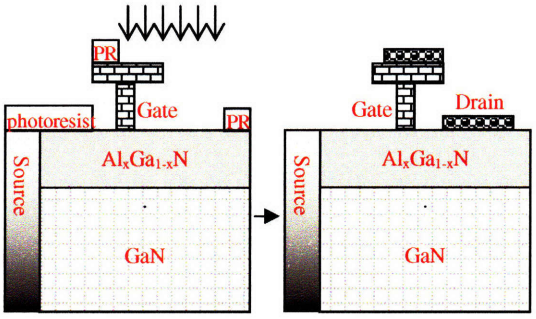


Figure 4.6 Illustration of the self aligned process for Schottky drain contact.

4.4 Device characterization

To test the performance of this new kind of drain contact, we have fabricated the AlGaN/GaN HEMTs following the process flow reported in ref. [Palacios2006b]. Some of these devices had Schottky drain contacts and others have conventional ohmic drain contacts. The small signal resistances of these transistors were characterized using an Agilent 4155 parameter analyzer as a function of the drain

current (Figure 4.7). In conventional AlGaN/GaN HEMTs, the total drain parasitic resistance is above 2 Ω·mm and increases with the drain current. In contrast, by using a Schottky drain contact, the contact resistance is ~0.2Ω·mm at 500 mA/mm current level. The access resistance measured in Schottky devices is limited by an ideality factor m=3 (Figure 4.8). Even better performance can be expected upon optimization of the ideality factor.

It is noted that, in the I-V characteristics of the Schottky drain contact, there is a kink at 1-2V. It appears in almost all the samples we have fabricated. Figure 4.9 shows the measurement from three samples. This kink severely degrades the ideality factor of Schottky contacts and increases the contact resistance. This kink is found to be related to the tunneling transport in GaN samples [Hasegawa2002]. We can use the circuit diagram in the inset of Figure 4.9 to model this effect. R_1 represents the tunneling component, R_2 represents the access resistance. The curve with squares is reproduced when R_1=1 MΩ and R_2=15Ω. It agrees with the experiments pretty well.

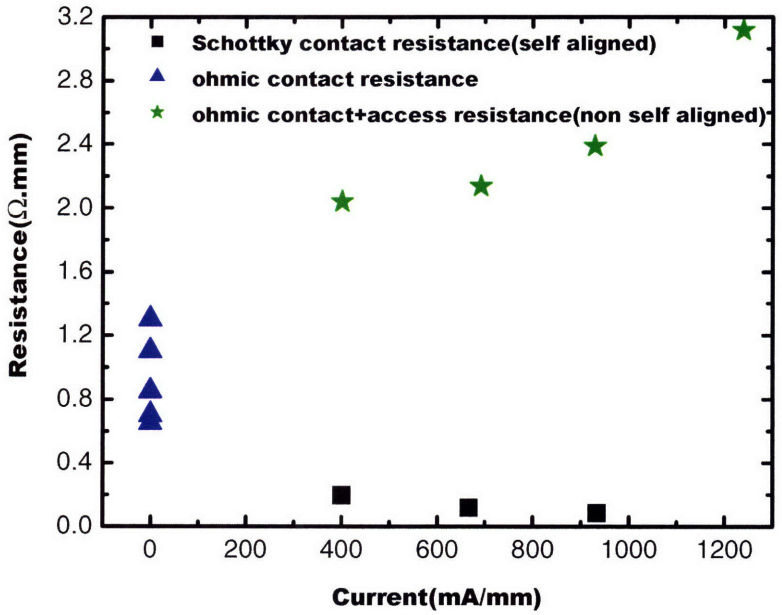


Figure 4.7 Measurement of the ohmic contact resistance, Schottky contact resistance and the total drain parasitic resistance in ohmic contact devices.

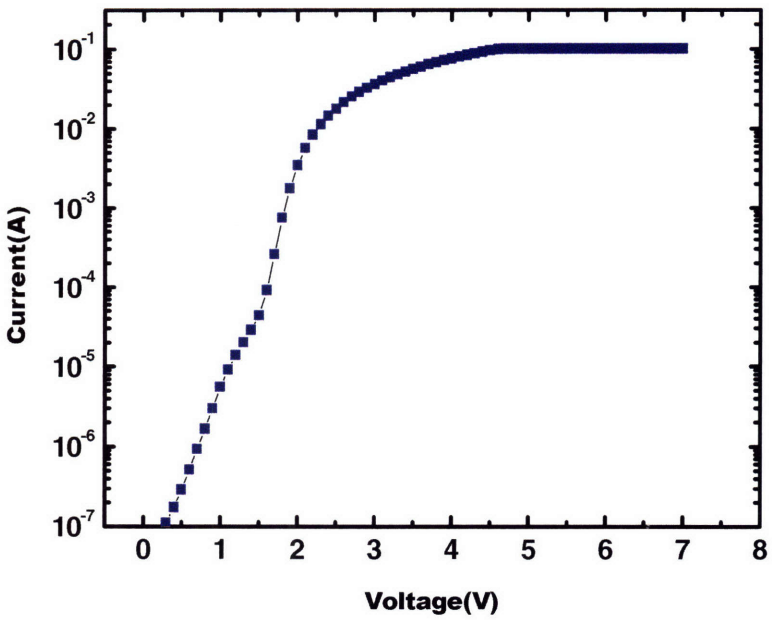


Figure 4.8 I-V characteristics of Schottky contact. The maximum current is set at 100 mA. An ideality factor of 3 can be extracted in this device.

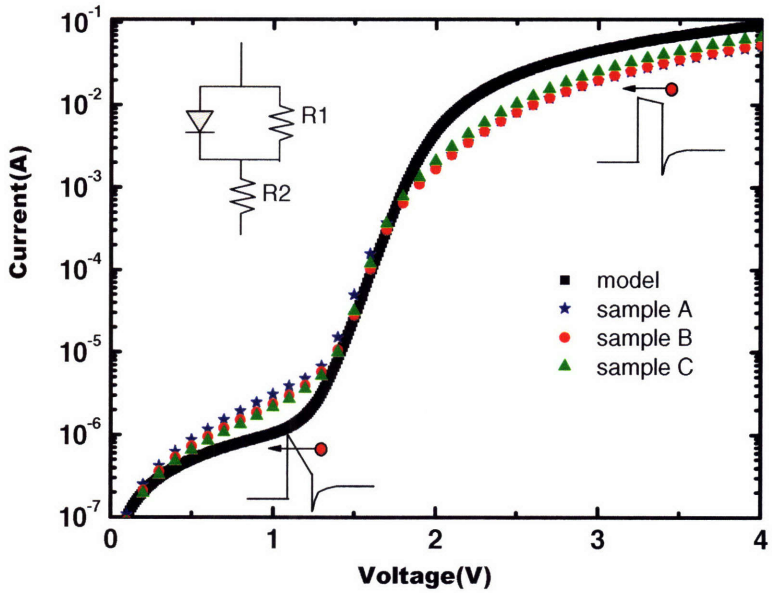


Figure 4.9 Tunneling currents degrade the ideality factor in Schottky contacts, which increases the differential resistance. We can model the tunneling current with the circuit shown in the inset, where R1=1 MΩ, R2=15 Ω. In this case, the contact is not self-aligned to the gate, which introduces some access resistance (R2).

4.5 ADS and Atlas Simulation

The commercial software ADS has been used to simulate the high frequency performance of Schottky drain AlGaN/GaN HEMTs through small signal equivalent

circuit simulations (Figure 4.10) [Hughes1989]. The values of all the components in the equivalent circuit model are extracted from s-parameter measurements of state-of-the-art 100 nm gate length, 150 μm width devices. The key components of the simulated small signal circuit include the parasitic capacitances C_{gs}=147 fF and C_{gd}=13fF and the parasitic resistances R_g=4 Ω, R_s=10 Ω. As shown in Figure 4.11, if the drain parasitic resistance R_d is reduced from 13.3 Ω (2 Ω·mm) to 0.133 Ω (0.2 Ω·mm), f_T will increase from 116 GHz to 162 GHz and f_{max} will increase from 162 GHz to 477 GHz.

It should be noted that the use of Schottky drain contacts induces a non linearity in the I-V curve which could potentially decrease the large signal linearity of the device. We have studied this issue using Silvaco/Atlas simulations. As shown in Figure 4.12, our preliminary simulations reveal that the asymmetric contacts will not significantly degrade the linearity in the output characteristics.

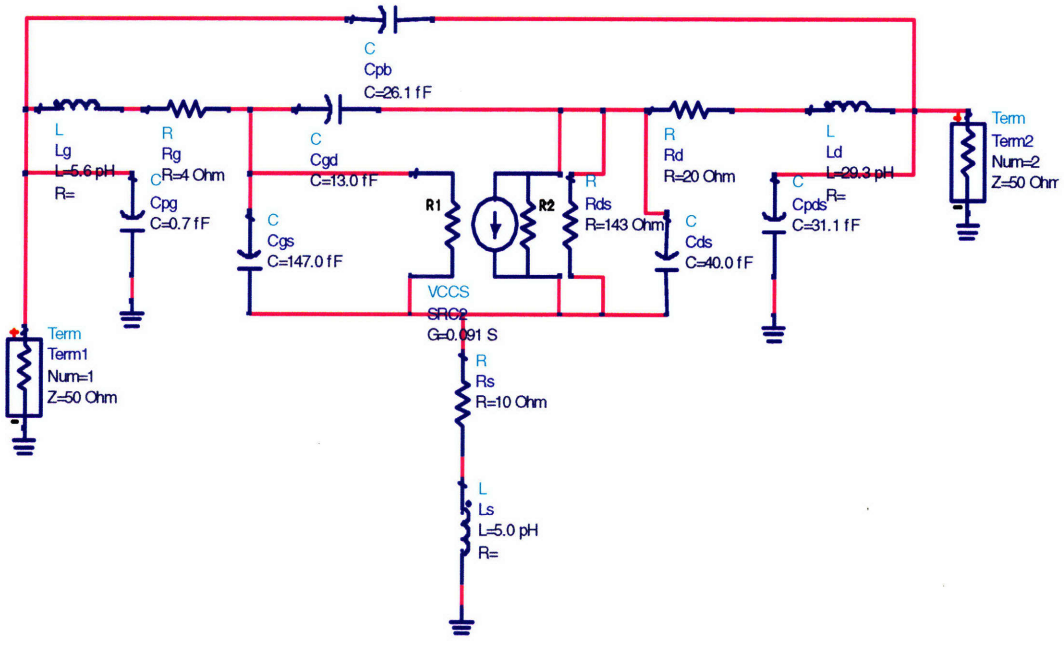


Figure 4.10 Small signal equivalent circuit implemented in ADS. The values of all the components are extracted from s-parameter measurement of state-of-the-art devices.

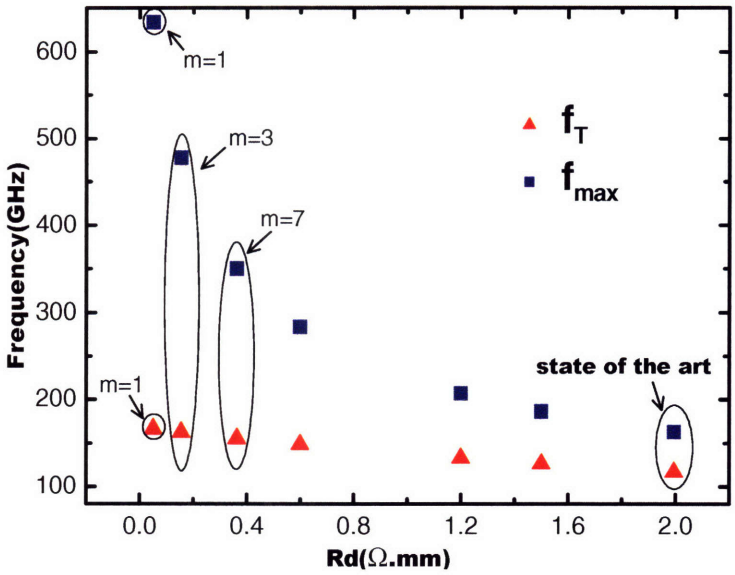


Figure 4.11 Small signal simulations of the f_T and f_{max} performance as a function of R_d. By reducing the drain parasitic resistance from 2Ω·mm to 0.2 Ω·mm, f_T increases from 116 GHz to 162 GHz and f_{max} increases from 162 GHz to 477 GHz. The use of Schottky drain contacts with low ideality factors (m) can significantly improve the frequency performance of these devices.

	R_d	f_T	f_{max}
Ohmic drain	2 Ω·mm	116 GHz	162 GHz
Schottky drain	0.2 Ω·mm	162 GHz	477 GHz

Table 4.4 Comparison of f_T and f_{max} using ohmic drain contact and Schottky drain contact

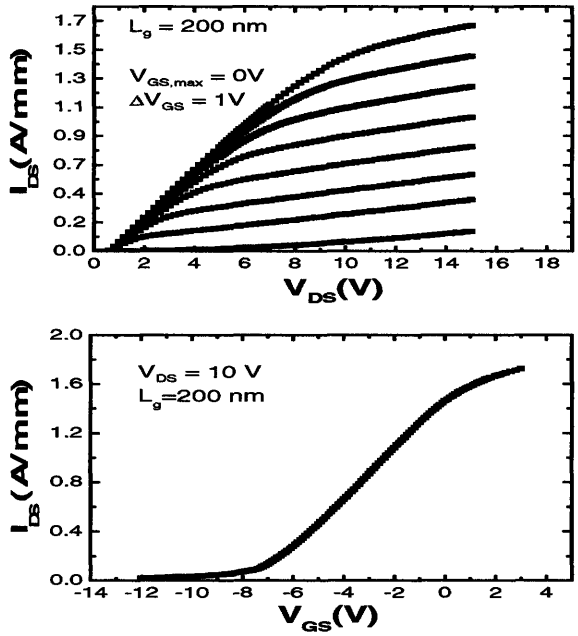


Figure 4.12 I_D-V_{DS} and I_D-V_{GS} characteristics of a Schottky drain AlGaN/GaN HEMT simulated in ATLAS.

4.6 Summary

In conclusion, Schottky drain contacts have been evaluated to reduce the parasitic resistance in AlGaN/GaN HEMTs. As shown from our experimental results and simulations, Schottky drain technology can significantly improve the f_T and f_{max} of AlGaN/GaN HEMTs by reducing both the contact and access resistances. This improvement is critical to take GaN power amplifiers beyond 60 GHz. The measurement of the RF performance of these devices is part of the on-going work.

Chapter 5: Conclusions and Future Work

5.1 Conclusions

This thesis has outlined some of the main challenges to extend GaN HEMTs operation to mm- and sub-mm waves. To overcome some of these obstacles, we have proposed two new device structures. First, through electric field engineering in the drain region we have demonstrated an increase of the electron velocity both under the gate and in the drain access region, which can effectively reduce both the intrinsic delay and drain delay. Second, to reduce the channel delay, we have proposed, for the first time, the use of Schottky drain contacts.

Electric field engineering

Electric field engineering was motivated by the high non-uniformity of the electric field in the channel of GaN HEMTs. The peak electric field appears at the gate edge near the drain side of the device and it reaches several hundred kV/cm at even a moderate voltage range. Unfortunately, electric fields in excess of 150 kV/cm significantly reduce the frequency performance of GaN HEMTs due to the low saturation velocity of these devices. To overcome this problem, a partial recess in the drain access region has been proposed. Since the electron density in the channel of these devices is a strong function of the AlGaN thickness, a locally thinner AlGaN layer will cause a local reduction in the charge density underneath the recess region. A lower electron density locally increases the resistivity, which results in higher electric field in that region. As the total voltage drop is constant along the channel, the electric field underneath the gate will be reduced.

Silvaco/Atlas simulations show that the peak electric field is reduced from 360 kV/(cm) to 180 kV/(cm) by introducing a partial recess in the drain access region.

Consequently, the average electron velocity is improved by 50%. This increase in average electron velocity is very promising to increase f_T in GaN HEMTs beyond 200 GHz. Besides that, the averaged electric field will also significantly improve the breakdown voltage.

To perform the local recess required by the proposed electric field engineering, a uniform, controllable and low damage etching technology is needed. However, none of the available etching technologies offer the required level of uniformity, accuracy and reliability. To overcome this problem, in this project we have developed a new dry etching technology based on the self-limited etch of only one atomic monolayer at a time.

This etching is a combination of Cl_2 chemical etching and Ar activation. Cl_2 forms bonds with GaN surface. The application of a low power Ar plasma activates the Cl_2, forming volatile $GaCl_3$. The Ar plasma power is low enough to avoid pure Ar sputtering, but high enough to activate the adsorbed Cl_2. This new etching technology is very promising not only for electric field engineering, but also for gate recess.

Schottky drain contacts

Schottky drain contact is a new technology to reduce the relatively large parasitic resistance typical of GaN HEMTs. In GaN transistors, R_d is almost one order of magnitude larger than in InGaAs devices. Larger R_d significantly degrades both f_T and f_{max}. In this thesis we have shown that the use of Schottky drain contacts can successfully overcome these problems and significantly improve the performance of these devices. Four different reasons support the use of Schottky drain contacts:

1. Since HEMTs are always working in the first quadrant of the I-V curve, the I-V characteristics of the drain contact does not need to be symmetric.
2. f_T and f_{max} are determined by the differential resistance in small signal equivalent

circuit model. At moderate and high drain current level, the differential resistance of a Schottky contact is much lower than an ohmic contact.

3. The drain parasitic resistance using ohmic contact increases with the drain bias current, while it decreases with drain bias current using Schottky contact.

4. Because of the low thermal budget of Schottky contact, self aligned process is easily achievable, which helps to further reduce the access resistance.

In conventional AlGaN/GaN HEMTs, the total drain parasitic resistance (contact plus access resistance) is above 2 Ω·mm and increases with the drain current. In contrast, by using a Schottky drain contact, the contact resistance is ~0.2Ω·mm at 500 mA/mm current level and decreases with current. Small signal equivalent circuit model performed in ADS predicts that, by reducing R_d from 2 Ω·mm to 0.2 Ω·mm, f_T improves from 116 GHz to 162 GHz, and f_{max} will improve from 162 GHz to 477 GHz.

In conclusion, lower than expected electron velocity, high parasitic resistances and capacitances and the non uniform and extremely high electric field are the main bottlenecks towards sub-millimeter wave applications of GaN transistors. The two new device structures proposed in this thesis in combination with the advanced etching technology developed in this project, are very promising to significantly improve the frequency performance of these devices and approach their performance to the "impossible" limit of 1 THz.

5.2 Future Work

This thesis has proposed solutions to some of the main challenges of sub-mm wave GaN transistors, there are still several issues to be resolved or improved in future.

The etching technology developed in this project is the first demonstration of Atomic

Layer Etching of GaN. It has been proved to be a self limited process with high depth resolution and very low damage. However as shown in Figure 5.1, the atomic layer etching still has two components: Ar-activated Cl_2 etching and pure Ar sputtering. Ideally the etching component due to Ar sputtering should be completely removed. High temperature etches will be used in the future to increase the chemical etching with respect to the sputtering etching. At high temperature, Cl_2 becomes more active which will allow a reduction in the RF bias voltage of the Ar plasma, which will reduce the Ar sputtering.

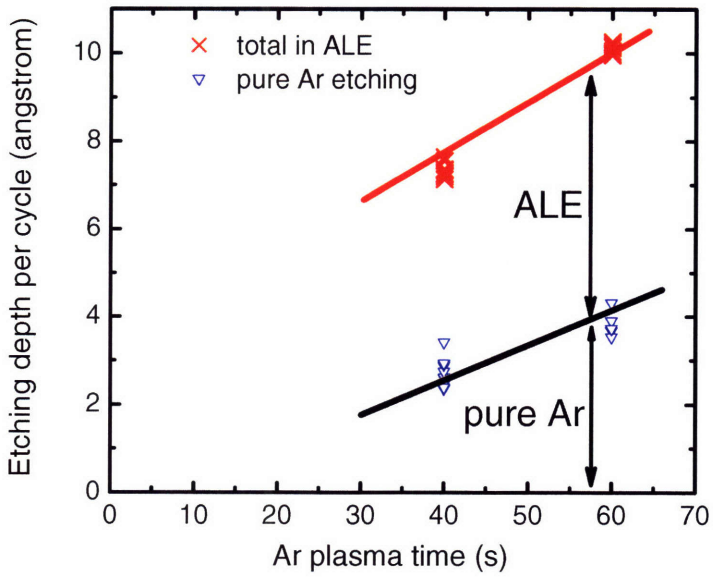


Figure 5.1 The Atomic Layer Etching has two components. One is from Ar-activated Cl_2 atomic layer etching, the other one is from pure Ar sputtering.

Also, the developed ALE process is slow as each cycle of this process takes more than 2 minutes. For this technology to be adopted by industry, it is necessary to optimize the duration of each step in order to reduce the time required by each cycle.

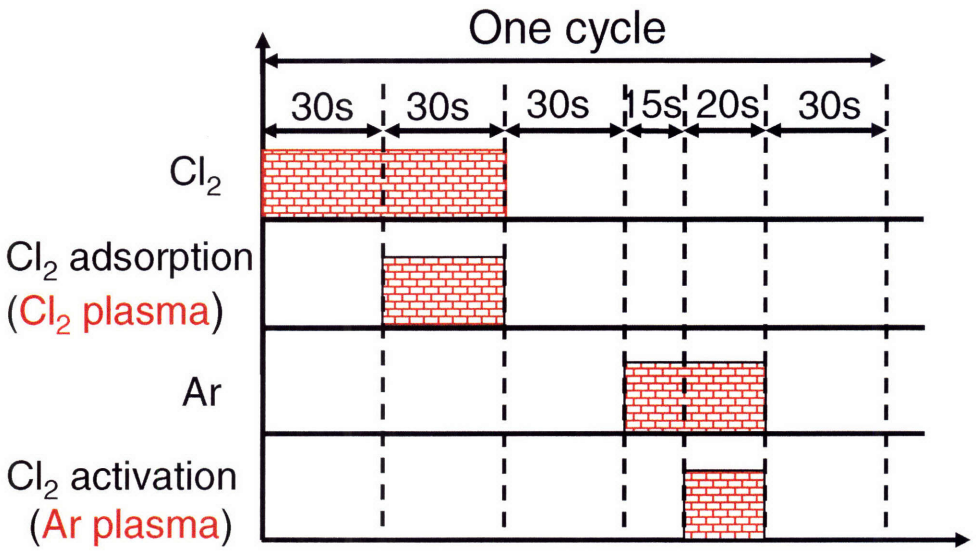


Figure 5.2 Atomic Layer Etching recipe in one cycle. It takes more than 2 mins to finish one cycle

Regarding the technology of electric field engineering for improving the electron velocity, the fabrication of these devices is currently on the way. DC and RF measurements will be carried out in the near future to compare the electron velocity in these devices and to better understand the trade-off's of this technology.

For devices with Schottky drain contact, we have measured the parasitic resistances and compared it with conventional ohmic drain devices. Small signal measurements are on the way to study the RF performance, especially f_T and f_{max} of these devices and compare it with our ADS simulation.

To conclude, the performance of GaN HEMTs has made great progress in the last decade due to breakthroughs such as SiN passivation and field plate structures. In order to keep up with this trend, new device structures and new fabrication methods have to be explored. This thesis made several contributions in this direction. Both the theoretical predictions and experimental work show great promise to further improve the performance of GaN HEMTs. Today the record performance is f_T=163 GHz and f_{max}=185 GHz in passivated devices by T. Palacios *et al.* We believe the new

technologies described in this work will be fundamental for the next generation of GaN high frequency devices.

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