Design of a Low-Voltage Low-Power dc-dc HF Converter

by

Jingying Hu

B.S., Illinois Institute of Technology (2005)

Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of

Master of Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 2008

Author_____

Department of Electrical Engineering and Computer Science

February 1, 2008

Certified by_____

David J. Perreault

Associate Professor of Electrical Engineering

Thesis Supervisor

Accepted by_____

Terry P. Orlando

Chairman, Department Committee on Graduate Students

Design of a Low-Voltage Low-Power dc-dc HF Converter

by

Jingying Hu

Submitted to the Department of Electrical Engineering and Computer Science
on February 1, 2008, in partial fulfillment of the
requirements for the degree of
Master of Science

Abstract

Many portable electronic applications could benefit from a power converter able to achieve high efficiency across wide input and output voltage ranges at a small size. However, it is difficult for many conventional power converter designs to provide wide operation range while maintaining high efficiency, especially if both up-and-down voltage conversion is to be achieved. Furthermore, the bulk energy storage required at contemporary switching frequencies of a few megahertz and below limits the degree of miniaturization that can be achieved and hampers fast transient response. Therefore, design methods that reduce energy storage requirements and expand efficient operation range are desirable. This thesis focuses on the development of a High Frequency (HF) dc-dc SEPIC converter exploiting resonant switching and gating with fixed frequency control techniques to achieve these goals.

The proposed approach provides high efficiency over very wide input and output voltage ranges and power levels. It also provides up-and-down conversion, and requires little energy storage which allows for excellent transient response.

The proposed design strategies are discussed in the context of a prototype converter operating over wide input voltage (3.6 - 7.2V), output voltage (3 - 9V) and power (0.3 - 3W) ranges. The $20MHz$ converter prototype, utilizing commercial vertical MOSFETs, takes advantage of a quasi-resonant SEPIC topology and resonant gating technique to provide good efficiency across the wide operating ranges required. The converter efficiency stays above 80% across the entire input voltage range at the nominal output voltage. The closed-loop performance is demonstrated via an implementation of a PWM on-off control scheme, illustrating the salient characteristics in terms of additional control circuitry power dissipation and transient response.

Thesis Supervisor: David J. Perreault
Title: Associate Professor of Electrical Engineering

Acknowledgements

First and foremost, I want to thank my thesis advisor, Professor David J. Perreault, for his patience and support throughout the course of this work. I feel extremely blessed to be working under and with such an outstanding engineer, caring advisor and knowledgable individual. I cannot thank him enough for all the extra hours he has spent guiding and assisting me through the course of this project.

My thanks go to the Society of Presidential Fellows at MIT and The Charles Stark Draper Laboratory for sponsorship. To Seth M. Davis, my supervisor at C.S. Draper Laboratory, for providing his valuable time and inputs.

To Juan Rivas and Anthony Sagneri, my knowledgable co-workers, inspiring teachers, and close friends, for their invaluable technical expertise and experience in addition to their constant encouragements. To Grace Cheung, our UROP, for her very much enjoyed company. Thank you all for making the basement laboratory such a pleasant place to work at. I also want to acknowledge the contributions, things I have learned and help I have received from other members of my research group, Yehui Han, Robert Pilawa, David Giuliano, Olivia Leitermann, Brandon Pierquet and Wei Li. I am also grateful for all the assistance the LEES staff has provided.

To Dr. Alexander J. Flueck, Dr. Qing H. Liu and Dr. Loren W. Nolte, for offering their advise, guidance and knowledge throughout my undergraduate years to help me grow as a student and as a person. Without the support and the opportunities they have given me, I would not have been given this chance to study at this institution.

To all my friends who have been there for me over the years: Wenting (my closest friend in Shanghai), Chao, Jiang, Rach (my beloved roomie), Gina, Kelly, Sahar, Sushma, Patricia, Devonte, Matt, Nathan, Nick, Justin, Sanj, Richard and Kalvyn. To LP, for always knowing the hottest spots in town, whom I can count on whenever I need a fun night out to relax and recharge. Thank you all for everything! The time that we have shared together will always be a part of my most cherished memories.

To Randy, for his selfless friendship during a stressful period when I felt like there was nobody else to turn to. Thanks for being there for me through that difficult phase of my life.

To Steve, for going through the ups and downs of my life with me and challenging me to be better. Thank you for having walked a memorable part of my life journey with me. Thank you for having composed a wonderful chapter of my life story with me.

To Rui, my cousin, for being the perfect daughter, setting the standards high, and putting up with me through all these years. To my grandparents, for their balanced encouragement and discipline as I was growing up (in addition for providing a safe haven whenever dad got mad).

I owe my deepest gratitude to my parents, who gave up everything they had in Shanghai(family, friends, career, status, title and reputation) and moved to the US in their late 40s/early 50s so that I can have a place to call home in the US. Thank you for teaching me so much about love, work and life. Without your unconditional love and support, I would be nowhere close to where I am today.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

THE demand for battery-powered portable electronic systems having smaller size and more capabilities has imposed challenging requirements for dc-dc power converters. Battery-powered systems must often accept the energy they draw from a wide input voltage range. This is due to both battery voltage variations with state of charge or charging and the possible need to accept varying battery types, configurations, and sources. Moreover, in systems with communication circuits (e.g. RF power amplifiers) and displays, there is often a need for compact dc-dc converters that can supply power (and control voltage) over a wide output voltage range. These requirements imply a need for dc-dc converters that can function across wide input and output voltage ranges at a high efficiency to allow for longer battery life. Furthermore, in some applications there is a need to achieve better transient response, which has previously been acceptable.

In spite of the need for smaller and better dc-dc power converters, it is difficult for many existing conventional power converter designs to provide wide operation range while maintaining high efficiency and a small volume, especially if both up-and-down voltage conversion is to be achieved. Furthermore, while switched mode power supplies (SMPS) have taken advantage of scaling trends in the form of improved semiconductors and higher integration, the bulk energy storage (comprising most of the volume) required at contemporary switching frequencies of a few megahertz and below has not scaled to the same degree, leaving most commercial converters with a not-so-subtle footprint. Shrinking passive component volume is one obvious way to target the needs for a smaller converter, however, the fundamental scaling issues that bring efficiency down beyond acceptable limits for modern converters make this approach impractical. An alternative method to resolve the tradeoffs between small size and high efficiency is to reduce the required energy storage and passive component values by increasing the switching frequency.

As described in [1], increasing the switching frequency of a power converter directly

reduces the energy storage requirements of inductors and capacitors of the circuit. In many cases, this corresponds to a reduction in the size of the passive components. Moreover, a higher switching frequency (and reduced intermediate energy storage) enables faster response to load transient and reduction filter components (e.g. output capacitors). Higher switching frequencies can considerably widen converter control-loop bandwidth, which is typically limited to about a tenth of the switching frequency.

The advantages of increasing switching frequency suggest that this method may hold the key to achieving designs that can meet all the demands of the next generation of portable electronic systems. This, in fact, has been an ongoing pursuit in power electronics since at least the 1970's [2] as switching frequencies have risen from tens of kilohertz to a few megahertz. This thesis will explore design methods suitable for implementing a low power dc-dc converter required to operate efficiently across a wide input and output range, and provide both up-and-down voltage conversion.

1.1 Challenges of Increasing Converter Switching Frequency

A typical switched mode power stage consists of semiconductor devices and passive energy storage elements. While losses are distributed among the active and passive components in the power stage of a converter, the bulk of the system mainly resides in the volume of the passive elements. Increasing operating frequency can significantly improve the size, cost and transient response of the system. However, increasing power loss at higher operating frequency in conventional converters places an upper bound on the switching frequency.

Switching power MOSFETs needed in portable electronic appliances have experienced tremendous improvements in the last few years, yielding devices with lower on-state resistance and smaller packages. However, under high frequency operation, switching loss (including loss associated discharging the output capacitance and overlap loss), instead of conduction loss, becomes the dominant loss mechanism in a conventional hard-switched converter. This places an upper bound on acceptable switching frequencies in such converters

Another loss mechanism closely related to the characteristics of switching devices such

as MOSFETs is gating loss, which results from charging and discharging the device input capacitance, C_{ISS}. For both lateral and vertical MOSFETs, gating loss has a linear dependency on the switching frequency [3, 4]. In the case of a conventional hard-switched converter, the gating loss is described by the following equation:

$$P_{GATE} = Q_{GATE}V_{GATE}f = C_{GATE}V_{GATE}^2 f \tag{1.1}$$

For a typical commercial 30V vertical MOSFET with effective gate capacitance of 200 pF operating at a switching frequency of a few megahertz, the loss is measured from hundreds of milliwatts to over a watt, which makes the efficiency (battery life) unacceptable for modern low-power portable electronics.

The energy requirement (the values of passive components) may be reduced as the operating frequency of the converter increases. On the other hand, the core loss of inductors becomes a major concern at high operating frequency. Core loss in even the best magnetic materials rises sharply as the switching frequency goes beyond a few megahertz, imposing a frequency limit. However, as designs move to high switching frequencies, converters employing air-cored magnetics have been successfully implemented with reasonable size and performance [5, 6, 7, 4]

These major loss mechanisms associated with conventional converter designs suggest that alternative design methods must be exploited to improve converter performance if we are to increase switching frequency to reduce the volume of modern switch mode power supplies.

1.2 High Frequency Resonant Power Conversion

The predicted poor performance of conventional hard-switched converters at high frequency, exacerbated in the case of low-power converters, suggests that resonant power conversion may be a more viable candidate as the switching frequency moves beyond a few megahertz.

Efficient power conversion at high frequency has been achieved using switched-mode RF inverters taking advantage of zero-voltage switching (ZVS). [8, 9, 10, 11, 12, 13,

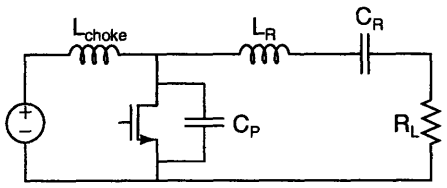


Figure 1.1: **Class E inverter**

14, 15, 16, 5, 6, 7, 2, 17, 3, 4, 18] Inverters like the Class E inverter [8, 9, 10], Figure 1.1, have been popular in various applications, ranging from communication systems to biotelemetry instruments. By utilizing reactive elements to shape the voltage and current waveforms, resonant power conversion can eliminate the significant amount of switching loss faced by traditional hard-switched converters at higher operating frequencies. Taking the advantages of resonant network one step further, gating loss can also be significantly reduced when a resonant network recycling a portion of the gate energy each cycle is utilized to drive the gate [3, 4, 19, 20, 21, 22, 17, 18].

However, resonant power conversion has its own challenges, which limits its range of use. Reactive elements in resonant topologies are usually tuned to provide desirable ZVS performance (and high efficiency) at a single operating point. However, as the load moves away from the nominal load value, with which the resonant topology is tuned, converter performance can plummet. Furthermore, Designing a suitable control method is also a non-trivial issue. Duty ratio control becomes difficult (if not impossible) to implement for resonant converters at high frequencies. Controlling power by varying switching frequency yields varying component stresses and efficiency reductions across load control limitations become yet another drawback for high frequency resonant converters.

Burst mode control [5, 23, 17, 3] has been shown to address the control challenges above, by separating the control function from the power stage operation of the converter. The converter cell is switched on and off at a modulation frequency, often much lower than the converter switching frequency, to control the average power delivered to the output. When the converter is on, it delivers a fixed power maintaining ZVS characteristics and good efficiency. When off, no power is delivered and there is no associated resonating loss. Although the controllers implemented by [5, 23, 17, 3, 18] are unconditionally stable and provide good performance at a very light load, the input and output waveforms have variable frequency content (owing to the variable-frequency modulation). This shortcoming makes this control method undesirable in

some applications (such as communication systems), and increases the difficulty of designing input and output filters.

1.3 Contributions and Organization of the Thesis

As suggested in the previous discussion, HF or VHF resonant power conversion is a suitable design method for low power converters to meet the two major concerns of future portable electronic systems, namely, efficiency and volume. The primary goal of this thesis is to develop and experimentally demonstrate a circuit topology, gating and control schemes for low-power dc-dc converters. These converter must operate efficiently across a wide input and output voltage range while providing for up and down voltage conversion. To demonstrate the proposed approach, we focus on design of a 3W dc-dc converter operating from a wide input voltage of 3.6 V - 7.2 V and supporting a wide output voltage range of 3 V - 9 V.

In Chapter 2 a quasi-resonant SEPIC topology is introduced and compared with various other topologies that may be suitable for the operating range and power level of the converter. This topology eliminates the need for a bulk inductor and keeps a low component count to simplify the system structure. The converter operates at fixed frequency and duty ratio. A detailed tuning method for this topology, including tuning of the rectifier and the inverter, will be discussed.

Losses associated with inductors is a major loss mechanisms for resonant converters that cannot be neglected, Resonant inductor designs are certainly not trivial issues at the HF and VHF operating regime. Achieving inductors with better Qs directly translates improved converter performance across the entire operating range. Chapter 3 briefly describes the opportunities and challenges in inductor designs via a comparison study of commercial off-the-shelf air-core inductors, custom designed air-core inductors and planar spiral inductors.

A low-loss resonant gate drive method and a new fixed-frequency on/off control is introduced in chapter 4. For low-power converters operating at substantial voltages in the HF and VHF regime, traditional hard gating with a totem-pole drive simply incurs too much loss for acceptable efficiency. Resonant gating can reduce the gating loss significantly at these frequencies [7, 6, 24, 19, 20, 21, 22, 25]. By recovering a portion of the gate energy each cycle, much lower power is required to drive the gate,

minimizing the impact that gating loss has on overall converter efficiency.

In order to overcome the challenge (faced by many resonant converters) of maintaining good efficiency across a wide load range, an on-off control scheme is utilized, in which switching of the converter is gated on and off to control the average power delivered to the output. This control approach which we term PWM on-off control is discussed in chapter 5. Unlike voltage hysteretic on-off control, which has been successfully implemented in some previous designs [26, 6, 7, 24, 27, 3], PWM on-off control operates a fixed modulation frequency, leading to well-defined frequency content at the converter input and output.

Chapter 6 presents the design and experimental evaluation of the proposed resonant SEPIC converter. Table 1.1 lists the converter specifications. The converter operates at 20 MHz and utilizes two commercial 30 V vertical MOSFETs in parallel. Open loop performance and closed loop performance are presented and discussed. The performance of the prototype converter will also be discussed in the context of commercial converters operating with similar input ranges and power levels, further demonstrating the design challenges the prototype converter has overcome.

Table 1.1: **dc-dc converter specifications**

Input Voltage Range	3.6 - 7.2 V
Output Voltage Range	3 - 9 V
Switching Frequency	20 MHz
Output Power	0.3 - 3 W

Resonant power conversion at HF and VHF, along with suitable gating and control schemes, has proven its merits in the context of a low power dc-dc converter with wide input range, wide output range, and up-and-down voltage conversion capability. Chapter 7 summarizes the design considerations for HF resonant power conversion and suggests direction for continued work in this area.

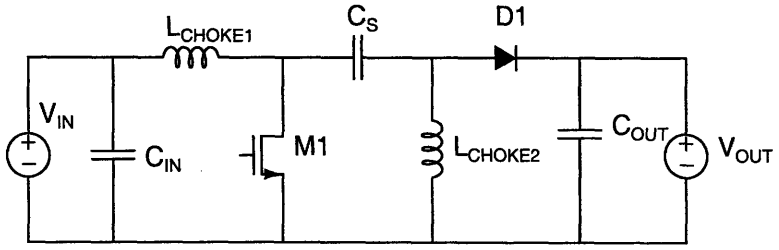
Chapter 2

A Quasi-Resonant SEPIC Converter

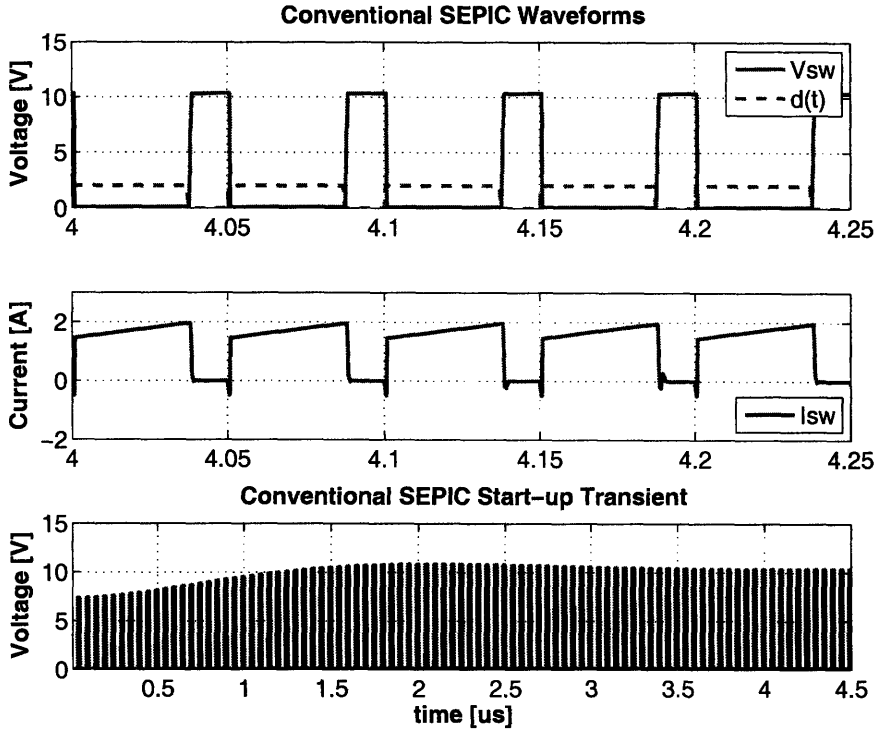
ADVANTAGES of increasing switching frequency and utilizing resonant power conversion are described in Chapter 1. Here we demonstrate that high frequency resonant power conversion is a suitable converter design method for achieving high efficiency over a wide input and output range. The SEPIC (Single Ended Primary Inductance Converter) converter is often used when the desired output voltage can be higher or lower than the input voltage. However, conventional SEPIC designs suffers from substantial switching loss at HF, slow response speed, poor load-step performance or all of the above performance deficiencies. These drawbacks have prevented most existing SEPIC designs from offering acceptable performance when a large operating range and a small size are both required. Here we introduce a new quasi-resonant SEPIC topology that maintains ZVS characteristics (and good efficiency) across a wide input and output voltage range and provides excellent dynamics performance, while keeping minimal energy storage requirement and low component count.

2.1 Limitations of conventional SEPIC converters

To illustrate the design challenges that the proposed topology has overcome, the limitations of traditional SEPIC converters are examined and discussed.



(a) A Conventional SEPIC Converter Topology



(b) Conventional SEPIC Waveforms

Figure 2.1: **A conventional SEPIC converter hard switching at 20 MHz. Significantly voltage and current overlap loss is evident at device turn-on/off. In addition, poor dynamic performance due to bulk inductors is apparent at start-up transient. See appendix A for component values and simulation files.**

2.1.1 Conventional Hard-switched SEPIC Converters

The conventional SEPIC converter has two bulk (ac choke) inductors, shown in Figure 2.1(a), yields hard switching of the switch and diode, Figure 2.1(a) and incurs significant switching loss at HF and VHF operation regime. If we are to design a conventional SEPIC converter according to [28] to meet the same criteria listed in Table 1.1, the choke inductor values are about 380 nH given by

$$L_{CHOKE} = \frac{V_{IN(MIN)}}{\Delta I_L \times f_{sw}} \times D_{max} \tag{2.1}$$

$$D_{max} = \frac{V_{OUT} + V_D}{V_{IN(min)} + V_{OUT} + V_D} \tag{2.2}$$

$$\Delta I_L = I_{OUT} \times \frac{V_{OUT}}{V_{IN(min)}} \times 40\% \tag{2.3}$$

where V_D is the forward voltage drop of the diode, f_{sw} is the switching frequency and D_{max} is the duty cycle at the minimum V_{in}. These bulk inductors severely deteriorates the dynamic performance of the converter (as shown by fig. 2.1(b), with a settling time over 1 μ s for a 20 MHz converter) and are extremely difficult to integrate. Furthermore, power dissipation associated with a commercial vertical MOSFET given by

$$P_{sw} = I^2_{sw(rms)} \times R_{DS(ON)} \times D_{MAX} + (V_{IN(min)} + V_{OUT}) \times I_{sw(peak)} \tag{2.4}$$

$$I_{sw(peak)} = I_{L1(peak)} + I_{L2(peak)} \tag{2.5}$$

$$I_{sw(rms)} = I_{OUT}\sqrt{\frac{(V_{OUT} + V_{IN(min)} \times V_{OUT}}{V^2_{IN(min)}}} \tag{2.6}$$

is about 980mW, which alone lowers the maximum efficiency achievable to barely

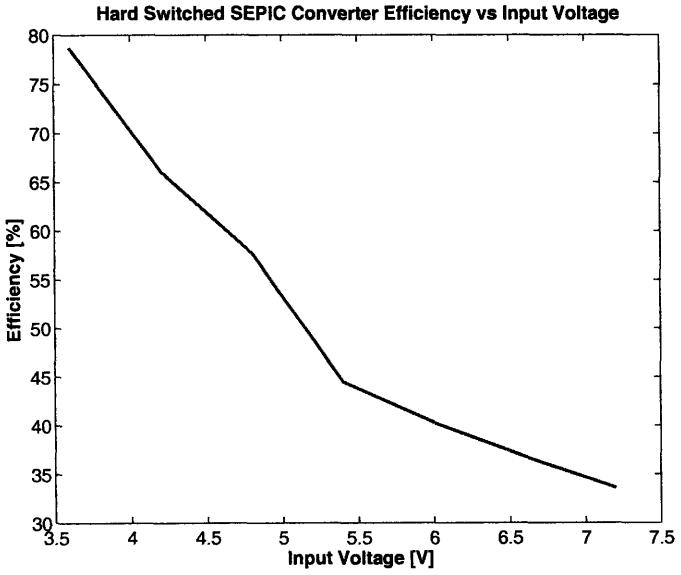


Figure 2.2: **Efficiency of a hard-switched SEPIC with various input voltages**

70% for a 3 W converter, which is simply unacceptable for most (if not all) portable electronic systems. Even if we scale the on-state resistance and the device capacitance of the commercial vertical MOSFET (assuming the on-state resistance halves and the capacitance doubles as the device area doubles, and vice versa) to obtain a optimal tradeoff (lowest total loss) between switching loss (given by the first term in equation 2.4) and conduction loss (given by the second term in equation 2.4), the efficiency is still only about 74% at the nominal output (See appendix A for component values and simulation files).

In addition, Figure 2.2, which shows the efficiency as a function of input voltage, clearly indicates that performance suffers severely if the converter is to be operating across a wide input and output voltage range.

2.1.2 Multi-Resonant SEPIC converters

The multi-resonant SEPIC topology [29], fig. 2.3, addresses excessive switching loss by utilizing a multi-resonant network to absorb the parasitic capacitance from the transistor and the diode, and to shape the transistor voltage for zero-voltage turn on. This topology explicitly introduces capacitances in parallel with the switch and

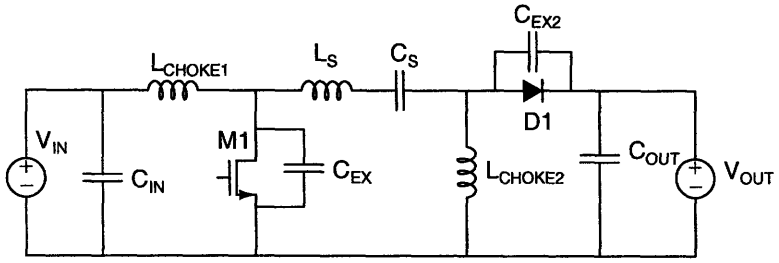
diode along with a resonant inductor L_S in series with the coupling capacitor C_S to achieve zero-voltage soft switching of the switch and diode, as shown in Figure 2.3(b). However, with frequency modulation control, the power stage and control function is tightly coupled, which prevents this converter from maintaining good efficiency as the load condition changes. Figure 2.4 illustrates the operation of the multi-resonant SEPIC converter as the output voltage varies. The multi-resonant SEPIC converter is designed such that the body diode "catches" the ringing across different output voltages. However, using the body diode in such a way can introduce significantly loss due to the diode forward voltage drop. Moreover, when the switch turns on, there is a significant amount of circulating current in the system, introducing yet another loss mechanism that deteriorates the performance. Furthermore, like the conventional SEPIC converters, the bulk inductors limit the response speed of the multi-resonant SEPIC converter.

2.2 A New Quasi-Resonant SEPIC Topology

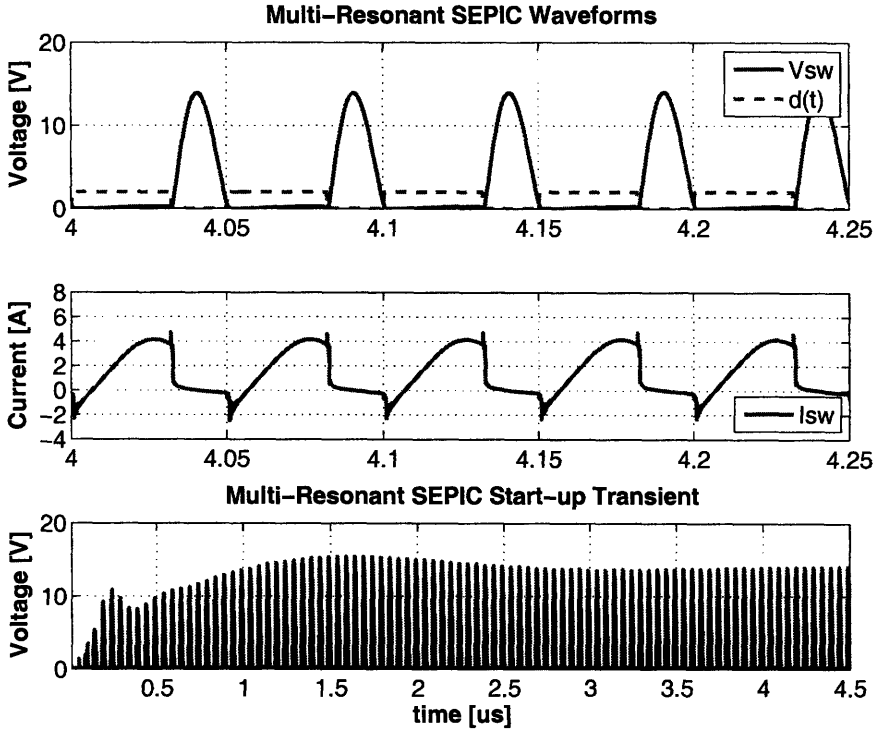
Here we introduce a new quasi-resonant SEPIC topology, Figure 2.5, suitable for efficient HF resonant power conversion across a wide operating range in addition to providing up-and-down voltage conversion. The topology used here has some topological similarities with both the conventional SEPIC converter [30] and with the multi-resonant SEPIC converter proposed in [31, 29]. However, the detailed component placement and sizing, operating characteristics, and control approach are all very different from these previous designs.

2.2.1 Background

The conventional SEPIC converter has two bulk (ac choke) inductors, and yields hard switching of the switch and diode. The multi-resonant SEPIC [29] utilizes similar bulk inductors, but explicitly introduces capacitances in parallel with the switch and diode along with a resonant inductor in series with the coupling capacitor C_B to achieve zero-voltage soft switching of the switch and diode. Furthermore, conventional SEPIC converter and multi-resonant SEPIC converter are controlled via frequency modulation. One major drawback associated with frequency modulation control resides in its substantial impact on efficiency under closed-loop operation



(a) A Multi-Resonant SEPIC Converter Topology



(b) Multi-Resonant SEPIC Waveforms

Figure 2.3: **A multi-resonant SEPIC converter [29]. ZVS switching characteristics are obtained from absorbing device parasitic capacitance by adding external capacitors. Although this converter is not operated under constant frequency, this simulation at $20MHz$ illustrates the poor transient response due to bulk inductors. See appendix A for component values and simulation files.**

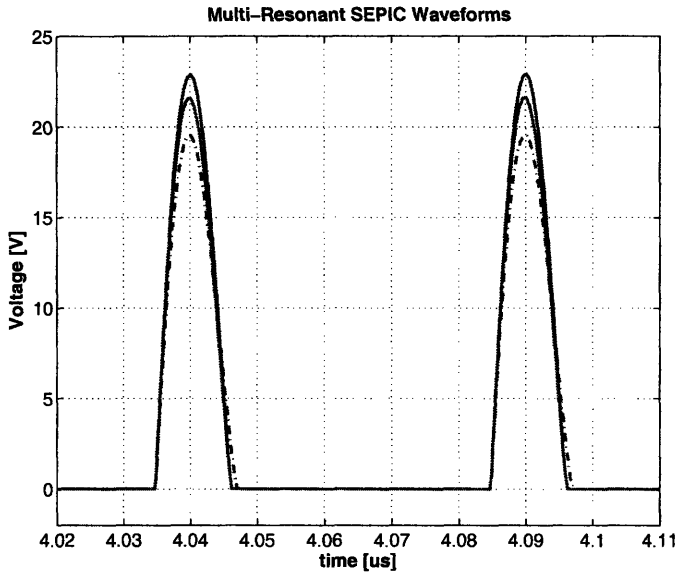


Figure 2.4: **Operation of multi-resonant SEPIC as output voltage varies from 3V to 7V**

due to its tight coupling between the power stage and the control function. As the soft-switching characteristics are closely tied to the impedance of the overall system, any deviation away from this optimal impedance (caused by changes in operating frequency as in the case of frequency modulation) can result in exacerbated circulating current loss and V-I overlap switching loss. Also, at the typical operating frequencies of the frequency conventional SEPIC and multi-resonant SEPIC converter [29], a large amount of output bulk capacitance is needed. This translates to larger size, deteriorated power density and higher cost.

The design introduced here also explicitly utilizes capacitances in parallel with the switch and diode. However, in contrast to previous resonant SEPIC designs [31, 29], the design here has no bulk inductors. Rather, it uses only two resonant inductors: one inductor, L_F, resonates with the net switch capacitance, $C_{OSS} + C_{EX}$, for resonant inversion, while the other inductor, L_{REC}, resonates with the rectifier capacitance, C_{REC}, for resonant rectification. This design method leads to reduced magnetic component count, along with greatly increased response speed.

Operation of this converter can be understood as a linking of three subsystems: a resonant inverter, a matching network and a resonant rectifier (Figure 2.5). A resonant rectifier connected to the inverter via a matching network forms a dc-dc

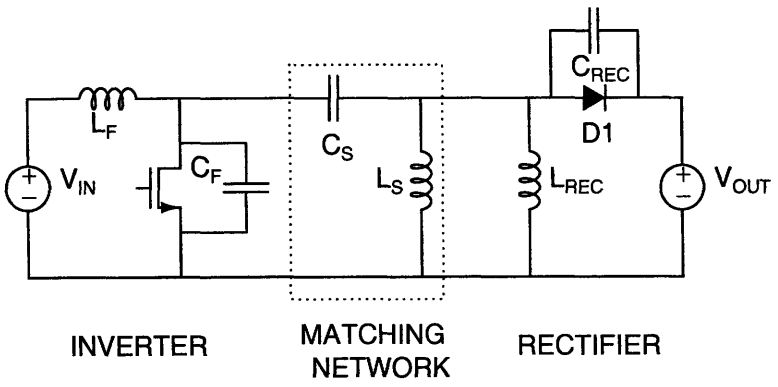
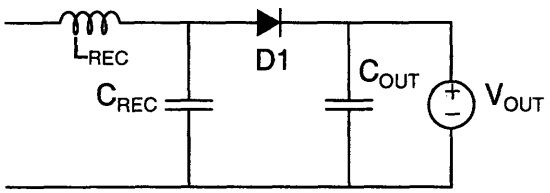


Figure 2.5: **Three subsystems of a resonant SEPIC topology**

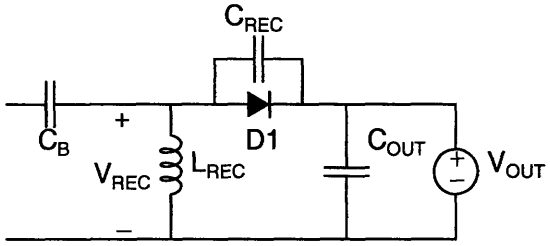
converter when properly tuned can deliver power efficiently at a constant switching frequency and duty ratio. As will be described, the high pass nature of the matching/interconnect significantly impacts the system operation.

2.2.2 Converter Design

The design procedure of a full dc-dc converter starts with a rectifier. The rectifier is tuned at the specified output power and voltage to exhibit certain characteristics and behaviors. Once the equivalent impedance at the operating frequency is determined, the rectifier can be replaced with this impedance to a resonant inverter, assuming majority of the output power delivered to the load is transferred at the fundamental. The inverter is then designed following a tuning process described in Section 2.2.5 to achieve desired performance. If the equivalent impedance of the rectifier is too high for a given inverter topology to deliver the required amount of output power, to obtain acceptable efficiency across the whole operating range, or to obtain reasonable component values, a matching network will be necessary to transform the rectifier impedance. The transformed impedance will then be used as the load impedance for the inverter. After a working inverter design is obtained with the equivalent rectifier impedance (with or without a matching network), a full dc-dc converter can simply be obtained by replacing the equivalent impedance with the full rectifier. Additional minor tunings may be required to achieve optimum efficiency and ZVS characteristics due to the interaction between the inverter and the rectifier since the rectifier is a nonlinear device, and is only approximately represented by an equivalent impedance.



(a) Boost Rectifier



(b) Rectifier with DC Block

Figure 2.6: **Two resonant rectifier topologies. The boost rectifier can only used in cases where the output voltage is higher than the dc voltage at the rectifier input, and the input provides a dc current path. The rectifier with dc block is suitable to provide up-and-down voltage conversion.**

The following sections will address the detailed tuning of each subsystem and design of a full dc-dc converter by connecting these three subsystems.

2.2.3 Resonant Rectifier

Rectification involves changing ac to dc, which is essential of a dc-dc converter. While classic square wave rectifiers may be a simple and viable solution at low switching frequencies, hard-switched rectifiers incur a significant amount of losses when operating at high frequency,. Among them, there are switching losses due to reverse recovery and capacitive charging of the diodes. Furthermore, losses due to low-Q parasitic junction capacitance and package inductance can easily exacerbate the rectifier loss.

It is therefore desirable to design a rectifier topology that provides good efficiency at HF while maintaining a small component count and a small size. While the "series loaded" resonant rectifier [32], Figure 2.6(a) discussed in [3, 33, 32] is a solution proven to meet these three criteria, its inability to provide buck and boost power conversion (due to the dc path provided by L_{REC}) makes it an unsuitable candidate

to meet the input and output voltage requirements of this application.

Figure 2.6(b) shows the schematic of the resonant rectifier to be implemented here. This rectifier topology is similar to Figure 2.6(a) except for the change in the location of the resonant inductor and the resonant capacitance. However, this seemingly minor component re-arraignment eliminates the dc path from the rectifier input and enables the topology to be utilized in applications where the output voltage is required to be lower and higher than the dc rectifier input voltage.

2.2.3.1 Basic Operating Principles

The particular resonant rectifier topology of interest here utilizes a resonant tank comprising of a resonant inductor L_{REC} (which provides a dc path for the output current) and a capacitance comprising the external capacitor C_{REC} along with additional parasitic junction capacitance from the diode. To evaluate rectifier operation, the rectifier is driven by sinusoidal current source at the switching frequency, providing an approximate representation of the inverter behavior. The output is modeled as a voltage source of value V_{OUT}, which represents the behavior of the rectifier load when the output voltage is controlled under closed-loop operation. Figure 2.7 illustrates the rectifier operation via time domain simulation results. V_{REC} is equal to the output voltage when the diode is on; When the diode turns off, L_{REC} and C_{REC} plus junction capacitance resonate until the V_{REC} once again reaches the V_{OUT}. At turn-off, the voltage across the capacitor equals V_{OUT} and I_{LREC} start decreasing. V_{REC} is being discharged until the inductor current is lower than the driving current source. Once this condition is reached, I_{LREC} continues to decrease, however, capacitor C_{REC} will start absorbing energy and V_{REC} rings up. Once V_{REC} reaches V_{OUT}, the diode again turns on and the inductor current increases until it exceeds the driving current, then the diode shuts off and the cycle repeats.

2.2.3.2 Rectifier Tuning Procedure

Consider the circuit for rectifier tuning shown in Figure 2.8(a), the amplitude of the current source driving the rectifier is selected such that the output power requirement can be met (Note that a whole range of values may be successfully used). The resonance between L_{REC} and C_{REC} can be selected such that the impedance looking

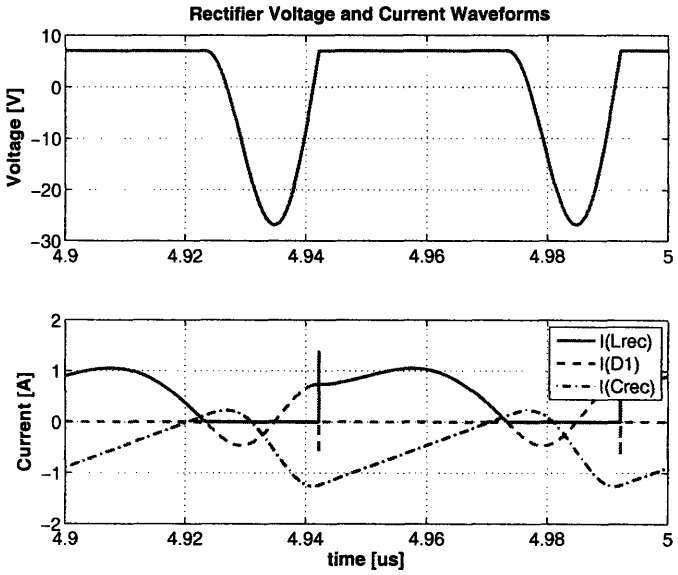
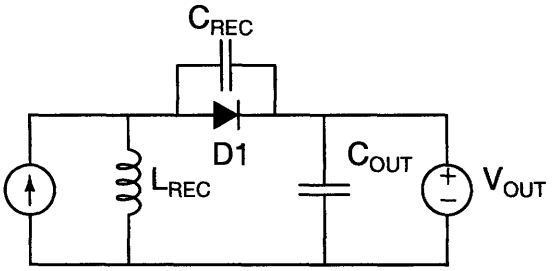


Figure 2.7: **Rectifier Waveforms**

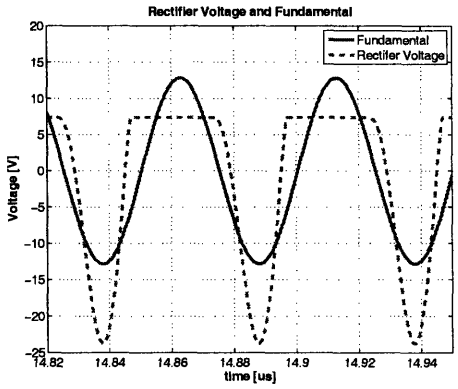
into the input port of the rectifier appear resistive at the fundamental frequency. This equivalent resistance can be readily obtained from the fundamental voltage waveform and the sinusoidal current waveform, Figure 2.8.

A straightforward way to tune this rectifier topology given a specified amplitude of the current source is to adjust C_{RECT} and L_{RECT} until a desired characteristic impedance and center frequency is achieved. The rectifier input impedance can be tuned to look resistive, slightly capacitive or slightly inductive.

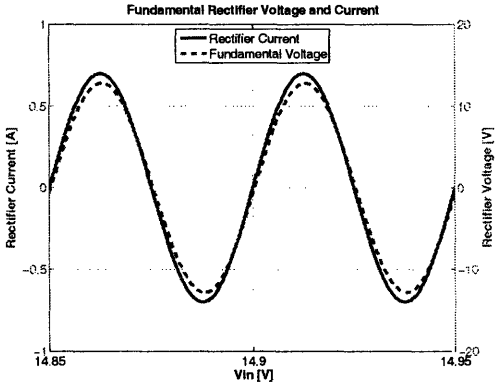
To achieve a purely resistive impedance at the fundamental frequency, there are two design handles, the resonant inductor L_{REC} and the resonant capacitor C_{REC}. By adjusting the resonant capacitor along with the resonant inductor, the peak reverse voltage and the length of the conduction interval of the diode can be traded off [27]. While capacitors with Q values in the thousands are relatively easy to obtain, it is much more difficult to obtain small inductors with Q of more than 100 at HF. Since it is possible to trade off low-Q inductance with high-Q capacitance to achieve the same impedance, it is generally desirable to do so, as indicated in Figure 2.9 where the rectifier output power and efficiency is plotted for two different values of L_{REC}. It is apparent from Figure 2.9 that a small low-Q inductor with a large high-Q capacitor generally leads to a more efficient rectifier design than a large low-Q inductor with



(a) Rectifier Tuning Circuit



(b) Rectifier Voltage with its Fundamental



(c) Fundamentals of Rectifier Voltage and Current

Figure 2.8: **Rectifier Voltage with its fundamental component extracted. The equivalent impedance of the rectifier can be calculated from the fundamentals of the rectifier voltage and current.The equivalent rectifier resistance R_{EQ} is** 17.14Ω

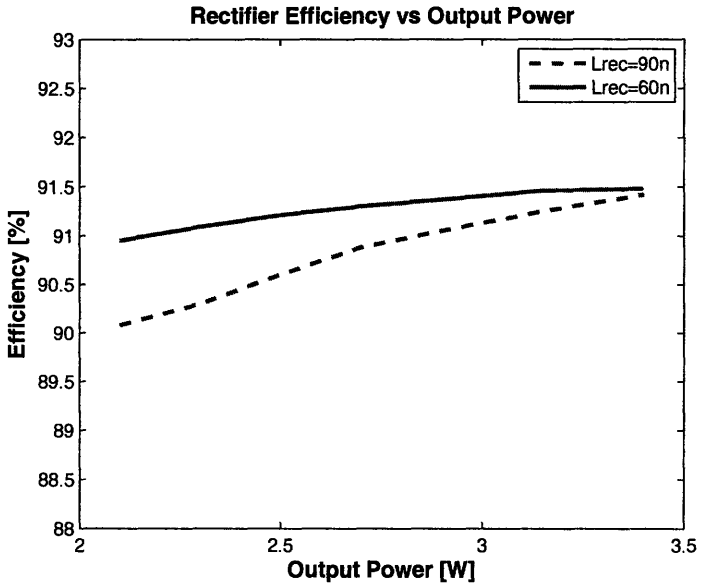


Figure 2.9: **Performance comparisons of rectifiers with different values of L_{RECT}. Better rectifier performance can be obtained by trading off large-valued relatively low-Q inductors with large-valued high-Q ceramic capacitance. A switching frequency of $20MHz$ with an inductor Q of 70 and capacitor Q of 3000 is assumed in simulations. When $L_{REC} = 90nH$, C_{REC} is swept from $125pF$ to $160pF$ to attain output power from $2W$ to $3W$. When $L_{REC} = 60n$, C_{REC} is swept from $700pF$ to $1100pF$ to achieve similar power levels. Simulation files for this example may be found in Appendix A**

a small high-Q capacitors achieving the same desired rectifier impedance. However, the approach cannot be practiced blindly. Once the required inductance is reduced down to a few nano-henries when the parasitic package inductance and parasitic prototype board inductance (both of which are extremely lossy (low Q) in nature) are on the same order of magnitude as the required resonant inductor, the performance (waveforms and efficiency) can be tremendously compromised.

The rectifier can also be tuned to be slightly inductive or slightly capacitive to aid switching. However, for a given output power, the rectifier performance is generally better (more efficient) when it is tuned to be slightly inductive, Figure 2.10. A capacitively-tuned rectifier often has more circulating current loss that deteriorates the performance.

In certain cases, it is more desirable that all of the rectifier capacitance needed by the

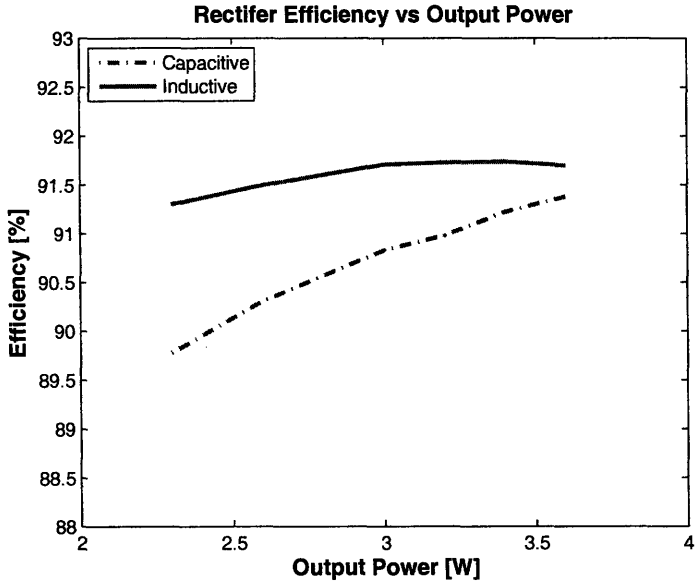


Figure 2.10: **Performance comparisons of rectifiers tuned inductively vs capacitively. A switching frequency of $20MHz$ with an inductor Q of 70 and capacitor Q of 3000 is assumed in simulations. L_{REC} is kept at $70nH$, while the C_{REC} is swept from $260pF$ to $1200pF$ to achieve different phases between the fundamental voltage and current. It is obvious that the performance for an inductively tuned rectifier is generally better for a given output power. Simulation files may be found in Appendix A**

rectifier to be provided by the rectifier device (e.g. a diode) to reduce losses associated with forward conduction drop and to avoid resonances between the capacitors and the device package [27]. However, that external capacitance can achieve much higher Q than lossy parasitic device junction capacitance suggests that adding additional high Q capacitors may result in less losses in some other cases. The decision of whether to add an additional diode in parallel or to add external capacitance entails a careful study of the dominant loss mechanism for each specific design. While in some designs, the circulating current loss associated with the low-Q diode capacitance may be the dominant loss mechanism in a given rectifier; the forward drop associated with the series resistance of the diode may be significant in others. In this case, it is the circulating current that dominates the rectifier loss. Therefore, a better rectifier design can be achieved via adding external high-Q capacitance instead of placing two diodes in parallel, as illustrated in Figure 2.11, where the rectifier performance of utilizing one diode versus two diodes is compared.

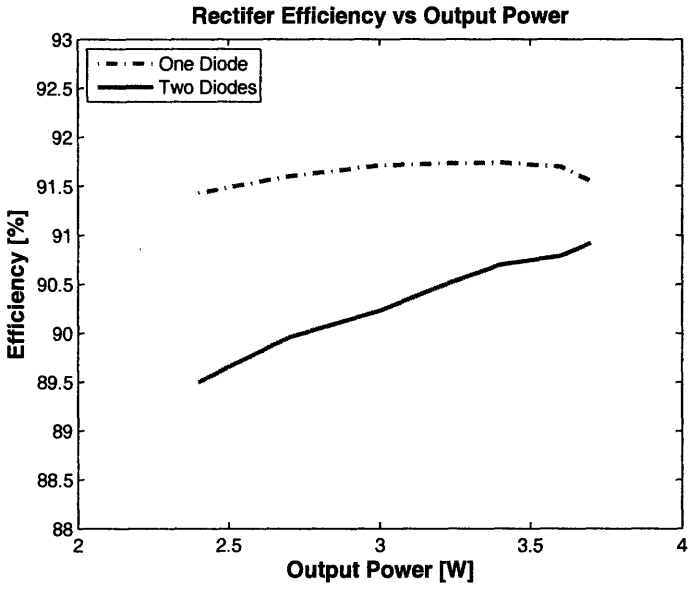
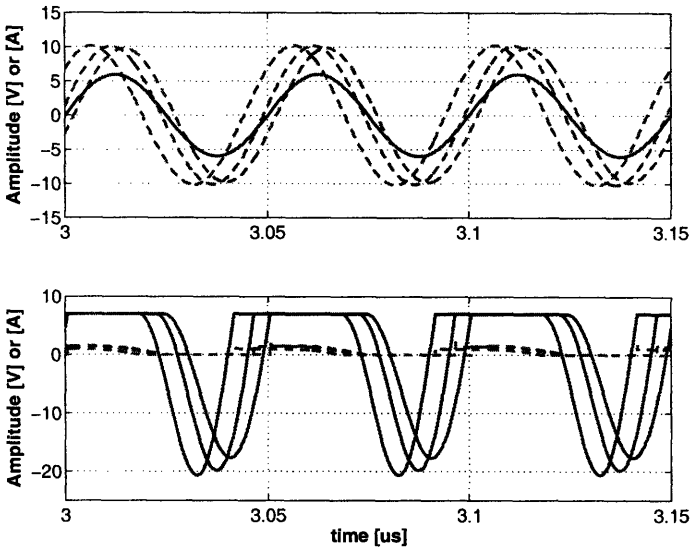


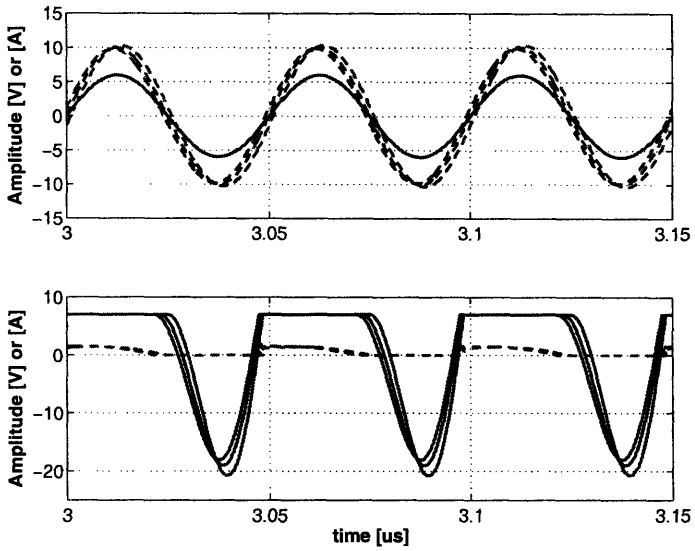
Figure 2.11: **Performance comparisons of rectifiers with two diodes vs one diode with additional external capacitance. A switching frequency of $20MHz$ with an inductor Q of 70 and capacitor Q of 3000 is assumed in simulations. L_{REC} is kept at $70nH$, while C_{REC} is swept from $180pF$ to $300pF$ when two diodes are employed to achieve similar power levels as the previous plot where only one diode is used. In this case, the performance improvement brought by high-Q external capacitance reducing circulating current losses exceeds the improvement brought by reduction in lower forward conduction drop. Simulation files may be found in Appendix A**

Although this rectifier topology is highly efficient and simple to tune, it has several shortcomings. Unlike the rectifier topology in [3], there is no additional tuning knob such as the dc source bias. Instead, once the output power are determined, the properties of the input current source is determined. Changing either the characteristic impedance $Z_O = \sqrt{\frac{L_{REC}}{C_{REC}}}$ or the center frequency $F_C = \frac{1}{2\pi\sqrt{L_{REC}C_{REC}}}$of the LC resonance will result a change in the behavior of the rectifier, indicated by the variations in V_{RECT} waveforms, illustrated in Figure 2.12. Therefore, this topology does not have the flexibility to maintain the overall switching behavior of the rectifier while the characteristic impedance is adjusted up and down, unlike the boost rectifier topology employed in [3].

In addition, as the amplitude of the current source is swept, the nonlinear element (diode and its nonlinear junction capacitance) prevents the impedance from staying



(a) Rectifier Waveforms as F_C is swept



(b) Rectifier Waveforms as Z_O is swept

Figure 2.12: **The rectifier waveforms for various center frequency $F_C = \frac{1}{2\pi\sqrt{L_{RECT}C_{RECT}}}$ and characteristic impedance $Z_O = \frac{L_{RECT}}{C_{RECT}}$. Unlike [3], the rectifier does not have the extra degree of freedom from adjusting dc-bias of the source. Therefore, changing either F_C and Z_O changes both the current and voltage waveforms. See appendix A for component values and simulation files.**

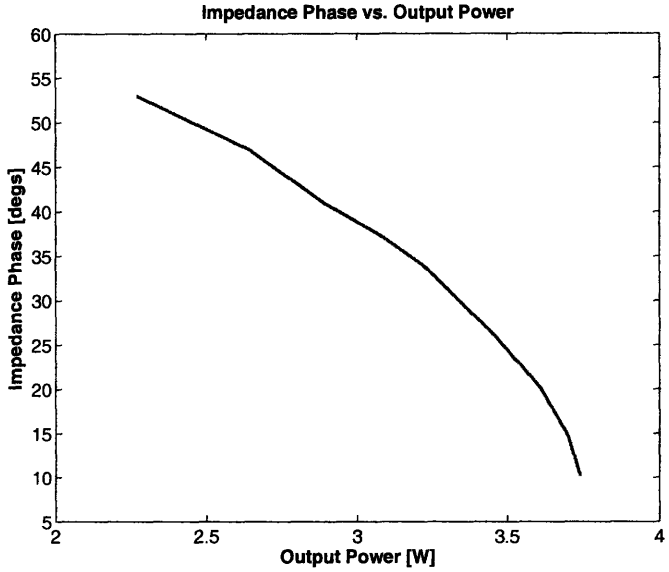
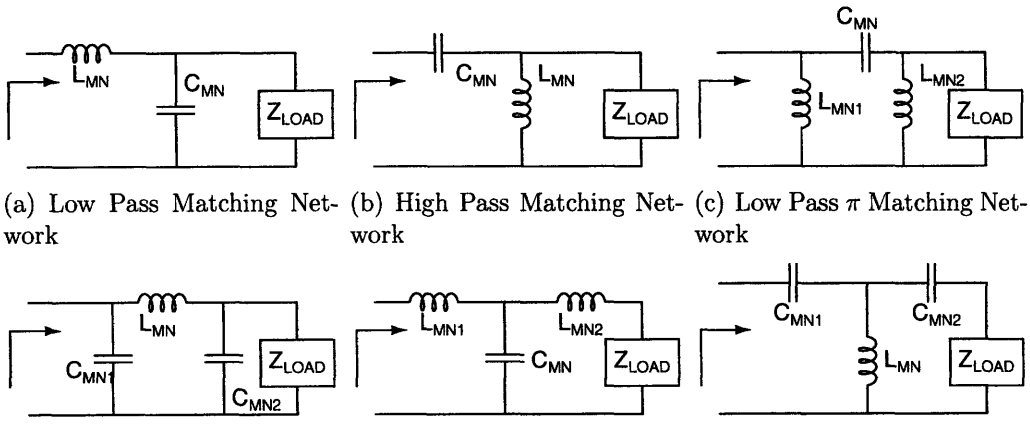


Figure 2.13: **Rectifier Impedance phase (at the fundamental) as a function of output power. A switching frequency of $20MHz$ with an inductor Q of 70 and capacitor Q of 3000 is assumed in simulations. Over a wide output power range, changes in the equivalent impedance of the resonant rectifier is significant. Simulation files may be found in Appendix A**

purely resistive across different operating conditions. As the amplitude of the current source is increased (the output power is increased), the phase between the voltage and current fundamentals typically increases and the rectifier appears more inductive. On the other hand, as the amplitude of the current sources is decreased (the output power is decreased), the rectifier appears more capacitive indicated by the decreased phase angle between the voltage and current fundamentals. Unlike the high-voltage and high-power rectifier design in [27], this phase change varies significantly across a wide range of output power, as shown in Figure 2.13. This characteristic of the rectifier imposes another challenge on the converter design, requiring an inverter topology that is relatively insensitive to the rectifier phase variation, as will be discussed in Section 2.2.5.



(a) Low Pass Matching Network (b) High Pass Matching Network (c) Low Pass π Matching Network

(d) High Pass π Matching Network (e) Low Pass T Matching Network (f) High Pass T Matching Network

Figure 2.14: **Various matching network configurations**

2.2.4 Matching Network

The purpose of the transformation stage, a subsystem between the inverter and the rectifier, is to alter the way the rectifier input impedance appears at the output of the inverter, to provide voltage and current level transformation, and to provide electrical isolation required by some applications [34]. In some cases, this subsystem is not required. The inverter and the rectifier can be connected merely by adding a dc blocking capacitor, whose capacitive reactance at the switching frequency is substantially smaller than the load impedance provided by the rectifier. This transformation stage is useful when the impedance achieved by the rectifier at a given output power level (following the tuning procedure from the previous section) is too high for the inverter to achieve ZVS, provide minimum output power, or operate at acceptable efficiencies. The transformation stage can be realized via conventional transformers, transmission-line transformers, matching network or similar means.

In an application (such as the one pursued in this thesis) where the input impedance provided by the rectifier is too high to deliver the amount of output power required (if to be directly employed at the output of an inverter topology), a matching network which steps down the rectifier impedance is a suitable approach. A matching network is a useful technique to transform impedance with a small number of components and very low loss [35, 34]. A matching network structure is designed to transform a given load impedance to a source impedance at a given frequency. The matching network can take on many forms. Figure 2.14 shows a few examples of matching networks

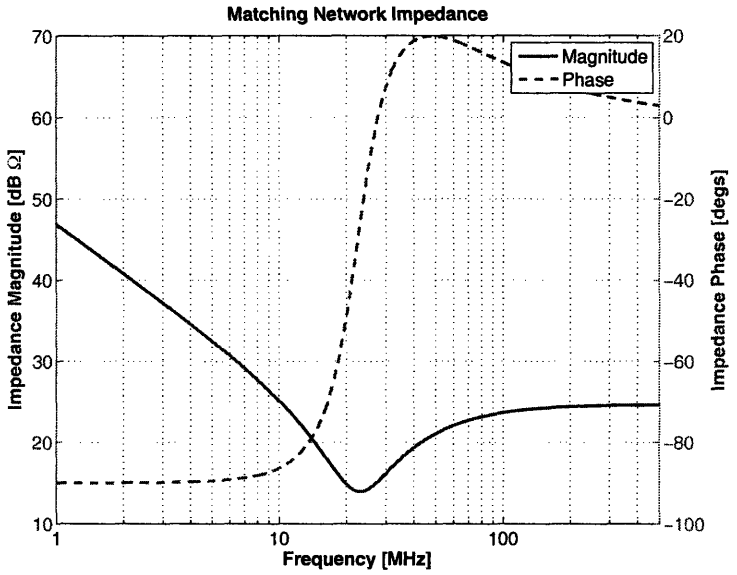


Figure 2.15: **Input impedance of a matching network with Figure 2.14(b) configuration.** $C_{MN} = 720pF$, $L_{MN} = 70nH$ **and** $Z_{LOAD} = 17\Omega$.

that reduce the load impedance. The effects that a given matching network has at frequencies besides the switching frequency are very important. Among these matching network configurations, the ones that provide a dc path between the inverter and the rectifier such as Figure 2.14(a), 2.14(d), 2.14(f) may be used with an additional dc blocking capacitors to provide up-and-down voltage conversion while others may be employed without any extra components. Also, the way in which these networks pass or block harmonic currents and voltages may greatly affect circuit operation.

One consideration in determining the matching network topology relates to the fundamental operating principle of a matching network. The matching network is designed to provide a specific transformation ratio at one frequency, and this frequency only. Since matching networks are comprised of reactive elements, the transformation characteristic is bound to change as the frequency moves away from the frequency at which the matching network is designed. When designing an inverter, the rectifier is modeled by its equivalent impedance(complex ratio of fundamental voltage to fundamental current) to simplify the design process. Given a rectifier input impedance, a matching network can be designed so that the inverter can achieve some desired output power, efficiency requirement and switching characteristics. However, when the inverter is connected to the rectifier, the matching network now sees the actual

voltage and current waveforms of the rectifier (instead of an equivalent resistance) and the voltages and currents of the rectifier are not scaled by the same transformation ratio across the whole frequency spectrum, which may complicate the tuning procedure. For example, Figure 2.15 illustrates a matching network designed to provide a transformation ratio from a 17Ω resistive load to 5Ω (at the input port of the matching network) at about $20MHz$. However, it is apparent that the this transformation ratio only occurs at one frequency, with the impedance at other frequencies scaled by completely different complex ratios.

Although different configurations can result in the same impedance transformation ratio at a given frequency, the effect of different matching network topologies on a load impedance won't stay the same across a range of frequencies. A matching network capable of achieving multiple resonances from having more than two reactive elements such as the T and π networks has lower efficiency and narrower bandwidth [35], is more prone to completely modifying the rectifier characteristic impedance, and complicates the inverter design even more. Therefore, a simple matching network with minimum component count, such as the one in Figure 2.14(b) is desirable for efficiency, size and volume considerations and converter design and tuning simplicity.

2.2.4.1 Tuning the Matching Network

The first step in matching network design is to determine a configuration. For the reasons mentioned previously, Figure 2.14(b) is a suitable matching network topology for this application, and will serve as a starting point for a matching network design.

To determine the transformation ratio required, we can begin by assuming that the drain voltage V_{DS} is a triangle wave (which will be apparent from simulation waveforms shown in Section 2.2.5.1) with 50 % duty cycle and swings between 0 and $\frac{8}{\pi}2V_{IN}$. If we assume that all the ac power is delivered to the load only at the fundamental of the switching frequency, the maximum load impedance allowed at the output of the inverter for a pre-determined output power level is given by

$$R_{LOAD} = \frac{V_{RMS}^2}{P_{OUT}} \tag{2.7}$$

Once the maximum load impedance (therefore, the minimum transformation ratio)

is determined, a matching network can be designed accordingly. Ideally, once the source impedance, load impedance and switching frequency is known, the component values for a given L-section matching network topology are determined. For this specific topology, the values for the inductor and capacitor can be calculated using the following equations.

$$\omega L_S = Z_{LOAD} \times \sqrt{\frac{Z_{MN}}{Z_{LOAD} - Z_{MN}}} \tag{2.8}$$

$$\frac{1}{\omega C_S} = \sqrt{Z_{MN} \times (Z_{LOAD} - Z_{MN})} \tag{2.9}$$

where Z_{LOAD} is the load impedance and Z_{MN} is the input impedance looking into the matching network. However, for a matching network to be employed in a converter operating under the characteristics of ZVS, high efficiency and wide operation range, its component values are not so set in stone by the equations above. Instead, the interaction between the matching network impedance Z_L, Figure 2.20, and the equivalent impedance of input resonant network of the converter Z_{IN}, Figure 2.20 shapes the total impedance seen at the drain-to-source node of the converter, allowing an extra dimension of flexibility in matching network design. In fact, the matching network can be designed such that it looks capacitive or inductive at the switching frequency. Therefore, Equations 2.8 and 2.9 alone cannot determine the final component values needed for a matching network to be used in a converter. A further study of interactions between the input resonant network, matching network and the load will be helpful in determining an optimum transformation stage design. This cannot be accomplished without entailing a discussion of the inverter operation.

2.2.5 Inverter Design

This section introduces an inverter design, Figure 2.16, together with the matching network and rectifier design discussed previously, suitable to meet the requirements outlined in Table 1.1. Although other topologies are known to provide lower device stress while maintaining ZVS and high efficiency [17, 3, 18], the specific operation regime of this converter (input voltage and output power requirement) makes the simplicity of the proposed approach desirable, especially considering the negligible

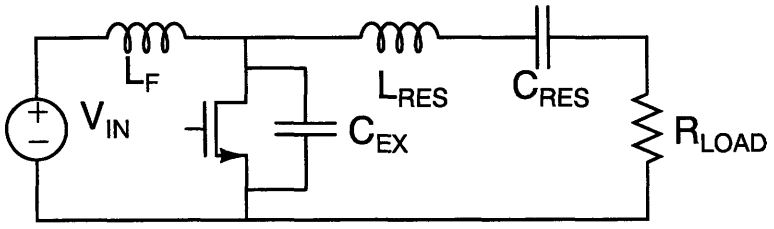


Figure 2.16: **A resonant inverter topology**

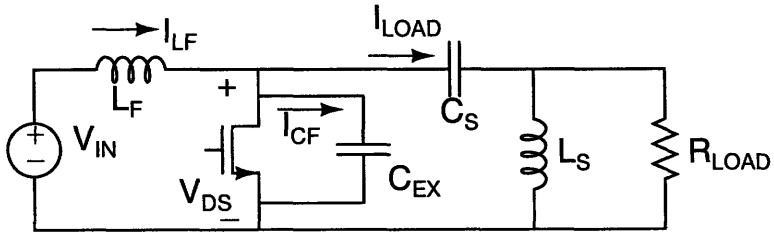


Figure 2.17: **A resonant inverter topology including a matching network**

improvements between available 20V and 30V devices at the time the converter was designed.

The resonant inverter topology may appear similar to that of a conventional a Class-E inverter. Its details are, however, quite different. Instead of a bulk input choke inductor, this topology utilizes a small-valued inductor L_F, resonating with any parasitic switch capacitance plus any external capacitors. The seemingly small change from a bulky inductor to a resonant inductor is in fact significant. It allows the converter to achieve excellent transient response and to be utilized with an on-off modulation control scheme, which will be discussed more in details in Chapter 5.

The output "tank" comprising L_{RES}, C_{RES} and R_{LOAD} can be tuned to be resistive at the fundamental of switching frequency, slightly inductive or slightly capacitive. However, in order to study the effects of matching network on the overall drain-to-source impedance along with the input resonant network, a slightly modified output tank is used in this inverter topology. Figure 2.17 shows the modified topology incorporating the matching network into the inverter topology of Figure 2.16. In this case, L_S and C_S form a matching network to transform the load impedance R_{LOAD}, which is obtained from the rectifier design following the tuning procedure outlined in Section 2.2.4.1. In certain case where the impedance provided by the rectifier is low enough not to significantly load down the overall impedance of the inverter, the

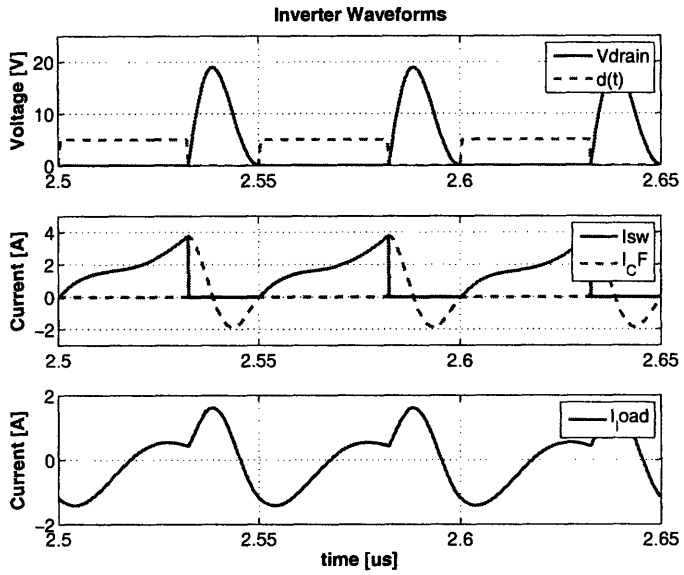


Figure 2.18: **The inverter tuned for operation at 20MHz with an ideal switch.** $L_F = 21nH$, $C_S = 720pF$, $L_S = 70nH$, **and** $C_F = 712.5pF$. **Inductor** Q **of 70 and capacitor** Q **of 3000 is assumed. Simulation files may be found in Appendix A**

inverter can meet the output power requirement without this matching network.

The simulated waveforms in Figure 2.18 illustrate the operation of the inverter. When the switch is off, the network looks like Figure 2.19. Upon turning off the switch, the voltage at the drain of the device, V_{DS} rises, the current in the resonant inductor L_F increases while capacitor C_F in parallel to the switch is being charged. The voltage at the drain continues to rise until the the current in C_F becomes zero and then goes negative ringing the drain voltage down. As the voltage of drain rings down to zero from its peak value, the current in C_F rings down to zero, at which point the switching turns on, establishing ZVS characteristic. For the interval in which the switch is on, C_F is now replaced by a short circuit, with the initial conditions of all passive components provided by the states at the end of the "off" interval. During this interval, the current in resonant inductor L_F continues to increase; energy flows from the input voltage and is stored in L_F. Similarly, the initial conditions of all passive components when the switch turns off again is established by the end state of the "on" interval and the cycle repeats.

Although writing out equations (one set for when the switch is on and another for when the switch if off, with initial conditions of each cycle provided by previous end

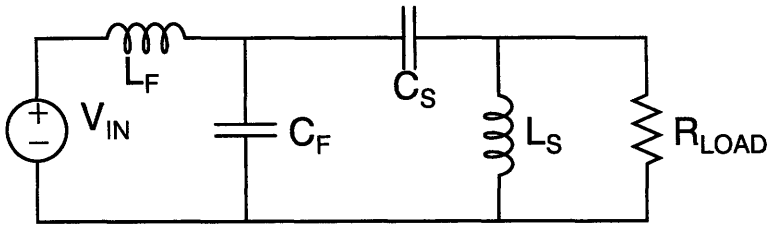


Figure 2.19: **When the switch is open, the network is comprised entirely of linear components, with initial conditions of all passive components set by the end state of the previous cycle**

states) is one solution to finding the exact component values for desired switching characteristics, the number of unknowns and the degree of freedom suggests that such a brute force approach may be not the wisest one. Numerical simulations provide a much more feasible method to determine the exact component values that provide zero-voltage, zero dv/dt switching behavior at a given operating range. While blindly sweeping parameters, including component values, duty ratio and switching frequency may eventually result in a working design, it may not arrive at an optimal one, especially when several operating regimes may be possible. The approach described in the following section is to first tackle the tuning procedure in the frequency domain by examining and adjusting the impedance characteristic of the inverter. Afterwards, minor modifications, which are based on a knowledge of the effect each component has on the inverter behavior, are made to achieve the desired switching characteristic and to account for any non-linear elements (such as device parasitic capacitance) from time-domain simulations.

2.2.5.1 Inverter Tuning Procedure

Here we describe an impedance-based tuning strategy, similar to that employed in [17, 6].

To better illustrate the tuning procedure behind the inverter operation, the inverter topology is divided into two parts, as illustrated in Figure 2.20. One part consists of the switch and the input resonant network comprising L_F and C_F. Looking back from the interconnection of the two circuit parts, this portion of the circuit exhibits impedance Z_{IN} when the switch is off. The other part is the load network, consisting of a matching network and the equivalent load resistance provided by the rectifier and

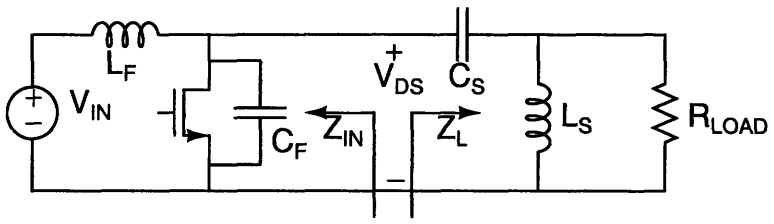


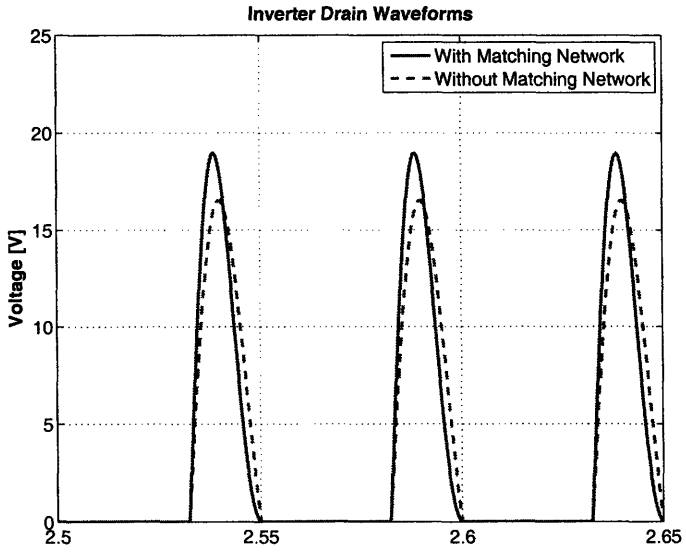
Figure 2.20: **Key impedances for tuning the inverter topology, Z_{DS}, Z_{IN} and Z_L**

representing an impedance Z_L as seen from the interconnection of the two circuits. The total impedance looking into the drain-source part of the device (with the switching off), Z_{DS}, is given by a parallel combination of Z_{IN} and Z_L. By understanding the characteristics of Z_{DS}, which determines the inverter's switching behavior, the inverter can be tuned to operate over a wide range.

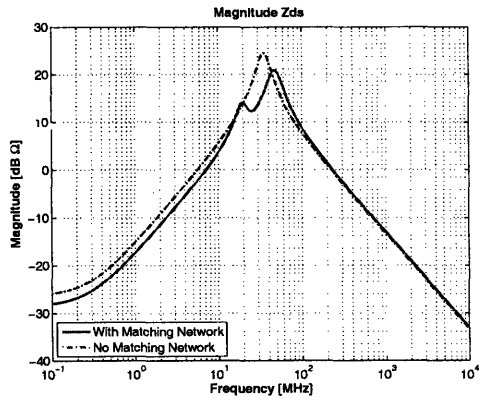
Inverter tuning begins with deciding whether a matching network is necessary or not. As described in Section 2.2.4, when the rectifier equivalent resistance is too high to meet the output power requirement, a matching network which transforms the load impedance to a lower value is required.

Figure 2.21 compares the time domain drain voltage waveforms along with the impedance Z_{DS}, Z_{IN} and Z_L for two inverter designs, one with a matching network and the other one without. The matching network effectively lowers the impedance. When a matching network is present, the drain voltage rings up to a higher peak voltage than it would otherwise, which means, a higher RMS voltage can be achieved with such a transformation stage. From the impedance plot of Z_{DS}, shown in Figure 2.21(b), the impedance at $20MHz$ is about the same for two cases and that at $40MHz$ is lower for an inverter with a matching network. Since the power is transferred to the load at the switching frequency and its harmonics, a lower impedance at the second harmonics indicates that more power may be transferred at this frequency for an inverter with such a matching network than it could otherwise (even if the same RMS voltage were presented at drain-to-source node). For the reasons above, it then becomes apparent how a matching network can help to increase the power delivered to the load than an inverter alone.

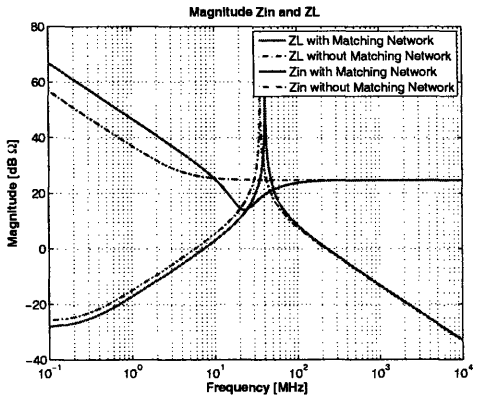
If the inverter cannot deliver the required amount of power without a transformation stage, the transformation ratio needed can be calculated from the procedure outlined in Section 2.2.4. If the interactions between Z_L and Z_{IN} could be ignored, the



(a) Drain Voltages for Inverters with or without a Matching Network



(b) Z_{DS} for Inverters with or without a Matching Network



(c) Z_{IN} and Z_L for Inverters with or without a Matching Network

Figure 2.21: **Drain voltages along with the impedance of the input network Z_{IN}, load network Z_L, and the overall drain-to-source impedance Z_{DS} for inverters tuned with or without a matching network. For the same $R_{LOAD} = 17.14\Omega$, an inverter with a matching network can deliver 3.9W to the load whereas the one without a matching network merely delivers 1.8W. The inverter tuned for operation at 20MHz with an ideal switch. Inductor Q of 70 and capacitor Q of 3000 is assumed. See appendix A for component values and simulation files.**

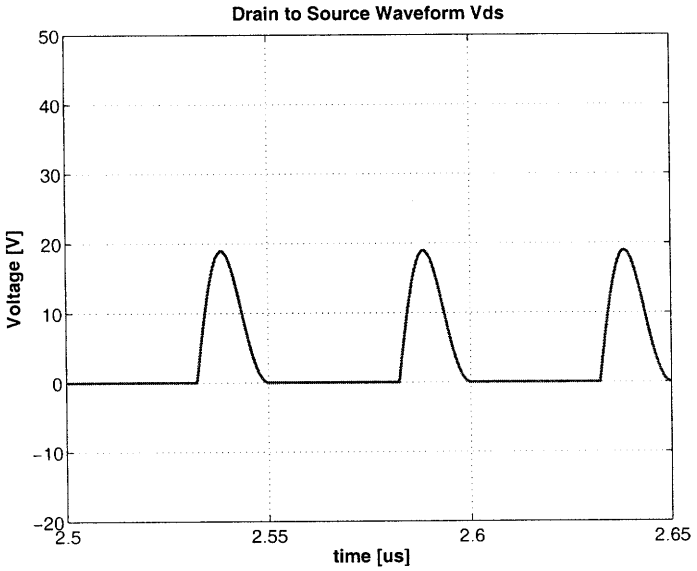
component values for the load network could be immediately determined from the transformation ratio required and the switching frequency, using Equations 2.8 and 2.9. Unfortunately, the characteristics of Z_{DS}, a parallel combination of Z_L and Z_{IN}, ultimately shape the switching behavior of the inverter. Therefore, the component values of Z_L cannot be determined from the equations alone.

There are several ways the required transformation ratio can be achieved through a given matching network topology. The resonance of L_S and C_S can be set to be exactly at the switching frequency, slightly above or below, all of which are viable and will lead to a working design (see design examples in Section 2.2.5.2). In some applications, one tuning method may result in more achievable component values and therefore, may be more favorable compared to the others.

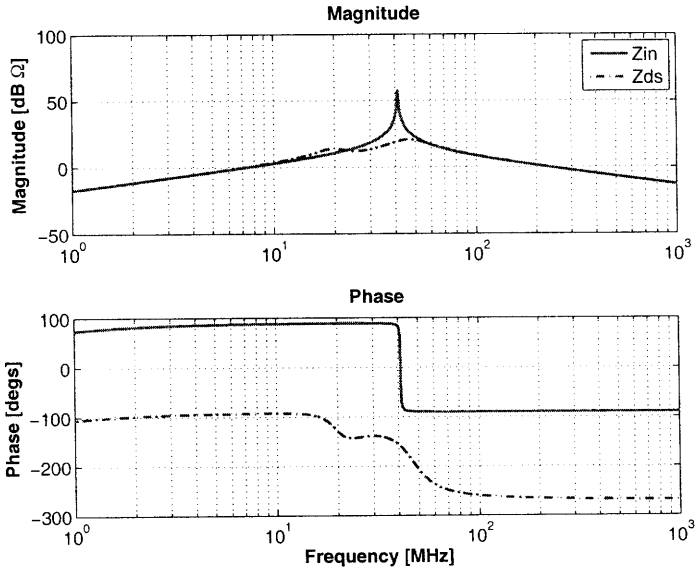
The input resonant network, L_F and C_F largely shapes the frequency at which the drain waveform rings up and down. For an inverter operating at a 50% duty ratio, one possible starting point for L_F, equation 2.10, is to tune the input resonant network such that its resonant frequency is at twice the switching frequency, in this case, 40MHz. This tuning selection gis like that of the "second harmonic" class E inverter in [15, 13]. The resulting drain-to-source switching waveform V_{DS} achieves ZVS and zero dv/dt, and the corresponding waveforms and drain-to-source impedance Z_{DS} are shown in Figure 2.22

$$L_S = \frac{1}{16\pi^2 F_{SW}^2 C_S} \tag{2.10}$$

Having a resonant frequency significantly lower than this value will results in the drain-to-source waveform ringing at a much slower speed, which corresponds to a time-domain switching waveform V_{DS} in Figure 2.24, assuming a 50% duty ratio. From Figure 2.24, it is apparent that the period at which the drain waveform is ringing is much longer than half of a switching cycle, and V_{DS} will continue to ring if the switch is not forced to be closed due to its duty ratio. On the other hand, when the resonant frequency of L_F and C_F is much higher than twice the switching frequency for a 50% duty ratio operation, V_{DS} will ring up and down at a much faster speed, resulting in a switching waveform in Figure 2.23. Clearly, neither of the waveforms in Figure 2.23, 2.24 satisfy the low-loss ZVS and zero dv/dt switching characteristics.

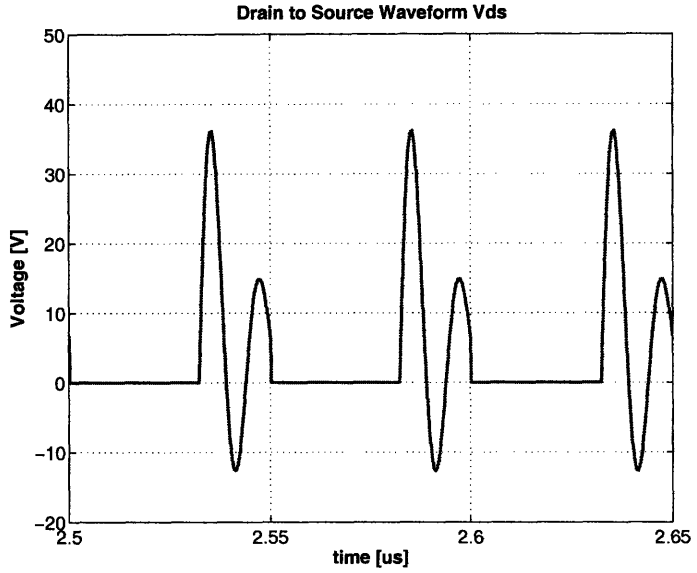


(a) Drain Voltage

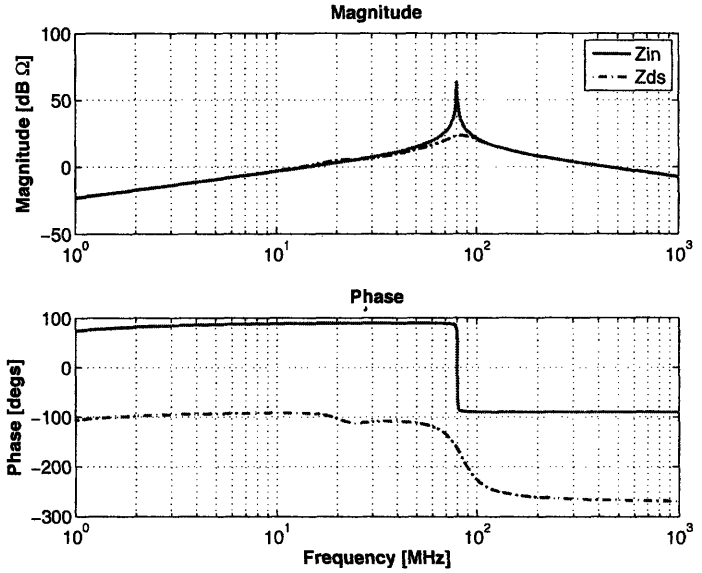


(b) Input and Drain-to-source Impedance

Figure 2.22: **When the resonant frequency of input network L_F and C_F is at about twice the switching frequency (given a 50% duty ratio operation), the drain waveform rings up and down exactly once during the period when the switch is off, and the desired ZVS characteristic can be obtained. The inverter tuned for operation at 20MHz with an ideal switch. $L_F = 21nH$, $C_F = 712.5pF$, $C_S = 720pF$, and $L_S = 70nH$. Inductor Q of 70 and capacitor Q of 3000 is assumed. Simulation files and component values may be found in Appendix A**

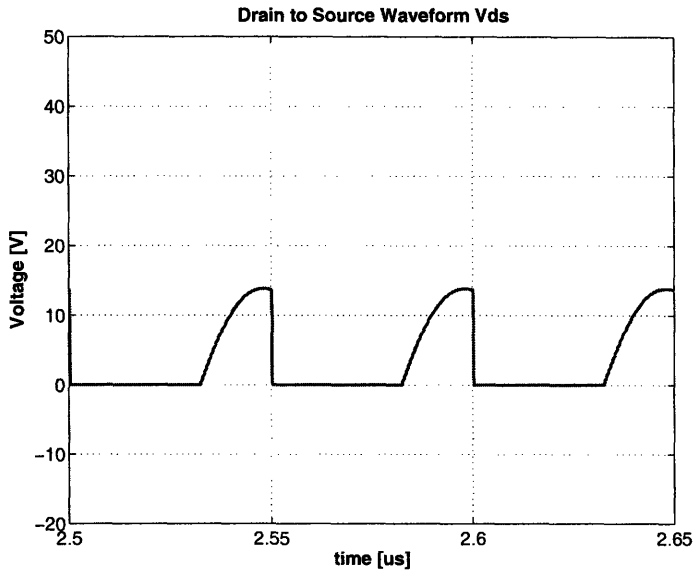


(a) Drain Voltage

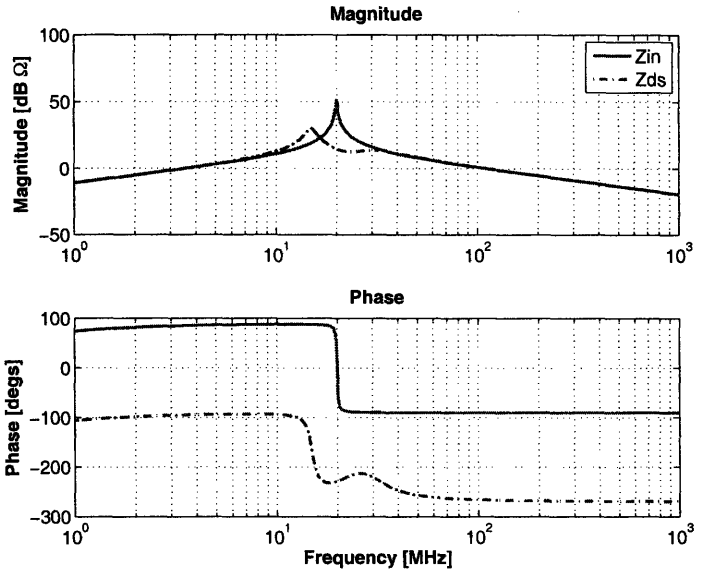


(b) Input and Drain-to-source Impedance

Figure 2.23: **When the resonant frequency of input network L_F and C_F is substantially higher than twice the switching frequency (given a 50% duty ratio operation), the drain waveform, instead of ringing up and down once during the period the switch is off, will ring at a higher frequency. The inverter tuned for operation at 20MHz with an ideal switch.** $L_F = 10.8nH$, $C_F = 366.45pF$, $C_S = 720pF$, **and** $L_S = 70nH$. **Inductor Q of 70 and capacitor Q of 3000 is assumed. Simulation files and component values may be found in Appendix A**



(a) Drain Voltage



(b) Input and Drain-to-source Impedance

Figure 2.24: **When the resonant frequency of input network L_F and C_F is substantially lower than twice the switching frequency (given a 50% duty ratio operation), the drain waveform will rise slowly, will be abruptly forced (instead of naturally ring down) to 0. The inverter tuned for operation at 20MHz with an ideal switch. $L_F = 43.2nH$, $C_F = 1465.8pF$, $C_S = 720pF$, and $L_S = 70nH$. Inductor Q of 70 and capacitor Q of 3000 is assumed. Simulation files and component values may be found in Appendix A**

Notice that the capacitor C_F includes the parasitic capacitance of the semiconductor switch and possibly an external capacitor C_{EX}. In some applications where the packaging inductance of the semiconductor switch is significant, allowing C_F to be solely provided by the device capacitance may be a good choice, because it prevents waveform distortion caused by additional ringing between the external capacitance and the package inductance. In other cases where the circulating current is significant, it is a better choice to add additional high-Q ceramic capacitance in parallel with the lossy device parasitic capacitance to reduce the circulating current loss. This requires that the value of L_F given by Equation 2.10 is not on the same order of magnitude as the low-Q board parasitic inductances.

Once the initial component values of the input resonant network and the matching network are determined from the procedure above, additional tuning can be done based on time domain simulations to achieve V_{DS} waveforms with desired switching characteristics. In general, ZVS and zero dv/dt switching behaviors in the time domain corresponds to the following impedance characteristics in the frequency domain.

1. The input resonant network Z_{IN} peaks at about twice the switching frequency
2. The frequency at which the matching network transforms the equivalent rectifier input impedance is approximately at the switching frequency
3. Z_{IN} and Z_L must intersect each other somewhere around the switching frequency. Otherwise the impedance to the matching network Z_L is not low enough at the switching frequency to load down the Z_{IN}, and therefore, the matching network does not have much of an impact on the Z_{DS} (or V_{DS}).
4. The net impedance Z_{DS} has two peaks. The low frequency peak is at about the switching frequency, and the high frequency peak occurs at about twice the switching frequency. This yields a drain-source waveform having mainly fundamental and second-harmonic components.
5. The high frequency peak should be about 4-10dB higher than the low frequency peak to obtain V_{DS} waveform that completes one ringing cycle at 50% duty ratio. Having a much more pronounced high-frequency peak corresponds to a V_{DS} waveform that rings much faster, Figure 2.23. Having a much more pronounced low-frequency peak corresponds to a V_{DS} waveform that rings much slower and is forced to zero abruptly if a 50% duty ratio is to be achieved, Figure 2.22.

6. The low frequency peak should be at least 1-2dB higher than the local minima. When it is not, the first peak is hardly detectable and the total impedance is dominated by the Z_{IN}.

Notice that unlike the inverter described in [3, 27], having an inductive phase or not at the switching frequency is not important for the inverter to achieve ZVS.

2.2.5.2 Other Tuning Considerations

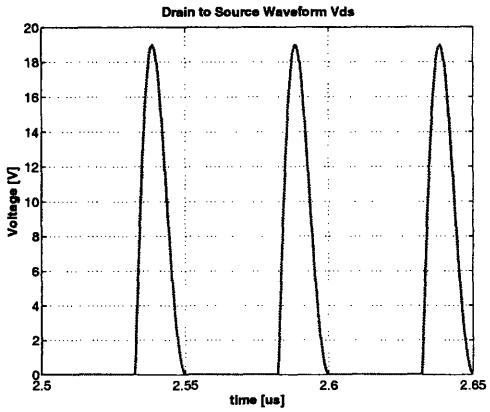
After a favorable tuning point is found and a desired impedance characteristic is known for a working inverter, the effects of varying input resonant network comprised of L_F and C_F, and different matching network configurations have on the drain to source impedance can be studied and compared.

Low Pass Matching Network:

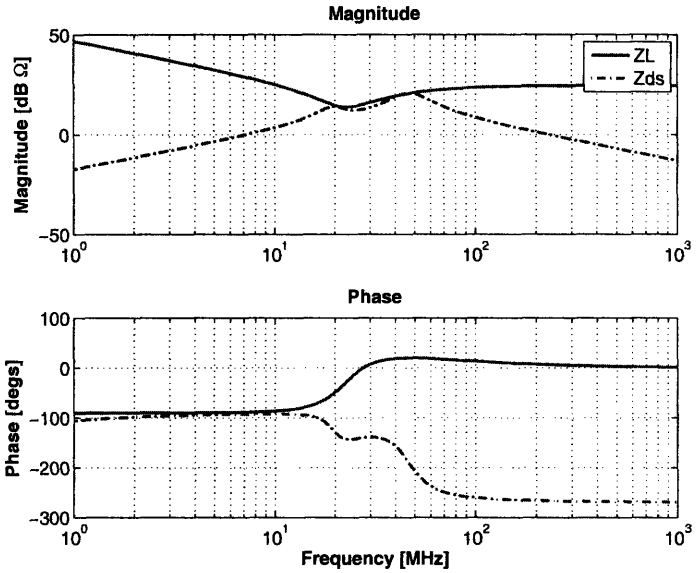
As described in Section 2.2.4, a matching network can take on many forms. So far, the discussion of a transformation stage has been made in the context of a high pass matching network, Figure 2.14(b). If the impedance at one specific frequency is of interest, a known high pass network, Figure 2.14(b) can be easily modified to a low pass network, Figure 2.14(a) with Equations 2.8 and 2.9. In this case, the fact that not only are we interested in the matching network impedance characteristics across a wide frequency spectrum, but also in its interaction with the input resonant network Z_{IN} makes this slight modification not such a trivial matter.

This matching network configuration variation, along with its impact on the inverter behaviors and the procedure required to re-tune the inverter is demonstrated in the Figure 2.25, 2.26 and 2.27, starting with a tuned inverter utilizing a high-pass matching network Figure 2.25.

The component values for a low pass matching network, Figure 2.14(b), with the same transformation ratio at the resonant frequency, can be calculated via Equations 2.9 and 2.8. It is of no surprise that this minor adjustment changes the impedance characteristic in the frequency domain and the switching behavior in the time domain due to the nature of a matching network (in that a transformation ratio can only be maintained at one frequency). The low pass network results in a lower impedance at



(a) V_{DS} for a tuned inverter with a high pass matching network



(b) Z_{DS} and Z_L for a tuned inverter with a high pass matching network

Figure 2.25: **Time domain switching waveforms for a tuned inverter with a high pass matching network, and its corresponding total drain-to-source impedance Z_{DS} and matching network impedance Z_L. The inverter tuned for operation at 20MHz with an ideal switch. $L_F = 21nH$, $C_F = 712.5pF$, $C_S = 720pF$, and $L_S = 70nH$. Inductor Q of 70 and capacitor Q of 3000 is assumed. See appendix A for component values and simulation files.**

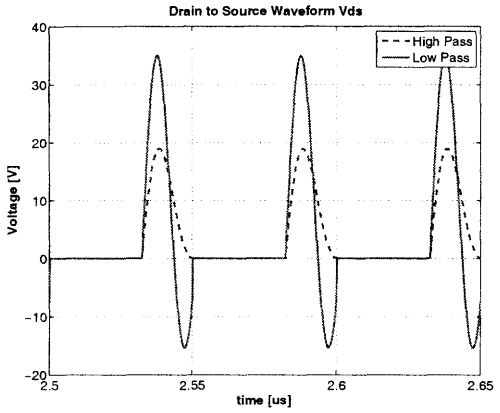
the switching frequency, 20MHz and the switching waveforms clearly do not exhibit the desired ZVS and zero dv/dt switching behavior, Figure 2.26.

After increasing C_F (while the other components and the duty ratio remain unchanged), the impedance can be adjusted to display a similar characteristics as a tuned inverter (with the second peak less pronounced, the magnitude of impedance at 20MHz slightly higher, the phase at 20MHz slightly more inductive) and not surprisingly, the inverter once again displays ZVS behavior in the time domain and now operates at an even higher efficiency at approximately the same power level, Figure 2.27.

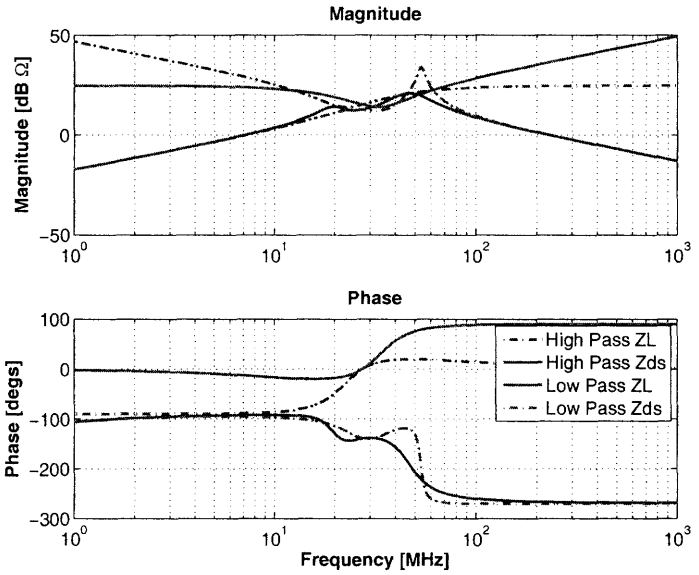
However, there is one problem with the topology above, Figure 2.28. By changing a high pass matching network to a low pass one without additional components, the inverter applies the dc input voltage to the load resistor, when combined with the rectifier topology described in Section 2.2.3 results in a converter that can only boost the input voltage instead of providing up-and-down voltage conversion. It is therefore essential to add an additional blocking capacitor in series with L_S to prevent any dc current (and dc power) from flowing in that branch, Figure 2.28. Notice that the rectifier topology described in Section 2.2.3 can no longer by employed due to the lack of a rectifier dc path. Instead, an alternative rectifier topology, illustrated in Figure 2.29 can be utilized to achieve the same load impedance. However, after an additional blocking capacitor is added to the matching network, the inverter can no longer provide the required output power. The maximum output power the inverter can provide is now only 2.8W at an efficiency of 87.2% (See appendix A for component values and simulation file).

While it is possible to re-tune the inverter topology shown in Figure 2.28 by adjusting L_S in parallel with the duty ratio to meet the output power requirement (See appendix A for component values and simulation file). This cannot be achieved without an unacceptable efficiency penalty or small duty ratios that impose challenges on gate drive design and/or incur significant gating loss, which will be discussed in Chapter 4.

The difficulty in designing an inverter operating at good efficiency and reasonable duty ratio suggests that a low pass matching network is not suitable to provide impedance transformation for this operation range and topology. The reason that a high pass matching network is able to provide the transformation ratio required while maintaining a good efficiency is partly due to its ability to transfer part of

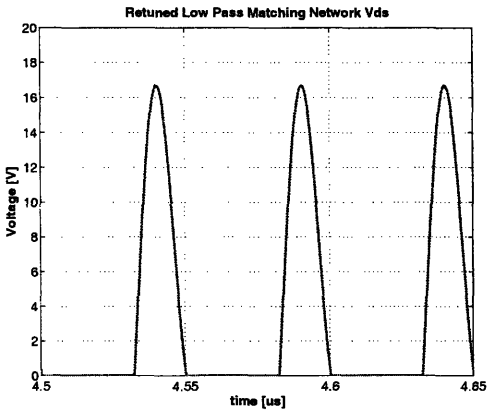


(a) V_{DS} for an inverter with a low-pass matching network with the same transformation ratio

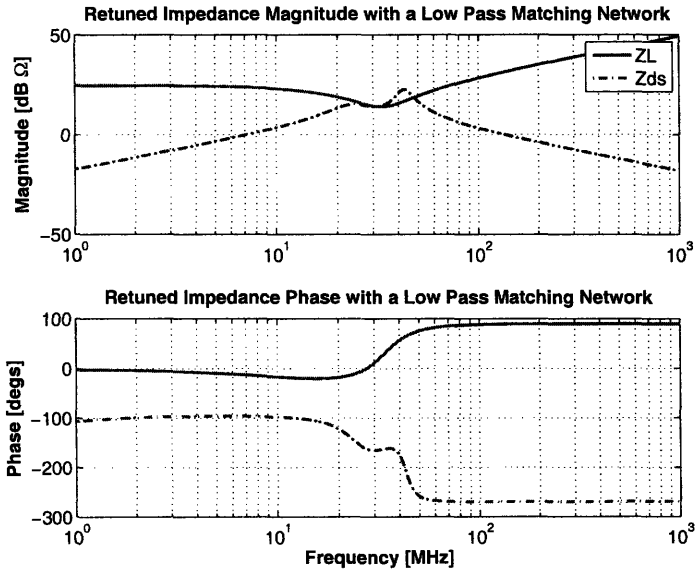


(b) Z_{DS} and Z_L for an inverter with a low-pass matching network with the same transformation ratio

Figure 2.26: **Time domain switching waveforms for an inverter with a low pass matching network, and its corresponding total drain-to-source impedance Z_{DS} and matching network impedance Z_L. The low pass matching network transforms a large load resistance to the a lower value, while maintaining the same transformation ratio at the same transformation frequency as the high pass network. The inverter tuned for operation at 20MHz with an ideal switch. $L_F = 21nH$, $C_F = 712.5pF$, $C_S = 481pF$, and $L_S = 46.8nH$. Inductor Q of 70 and capacitor Q of 3000 is assumed. See appendix A for component values and simulation files.**



(a) V_{DS} for an inverter re-tuned with a low pass matching network



(b) Z_{DS} and Z_L for an retuned inverter with a low pass matching network

Figure 2.27: **Time domain switching waveforms for an re-tuned inverter with a low pass matching network. This tuned inverter is obtained from increasing C_F from the previous un-tuned inverter figure 2.26. The inverter is designed for operation at 20MHz with an ideal switch. $L_F = 21nH$, $C_F = 1275pF$, $C_S = 481pF$, and $L_S = 46.8nH$. Inductor Q of 70 and capacitor Q of 3000 is assumed. See appendix A for component values and simulation files.**

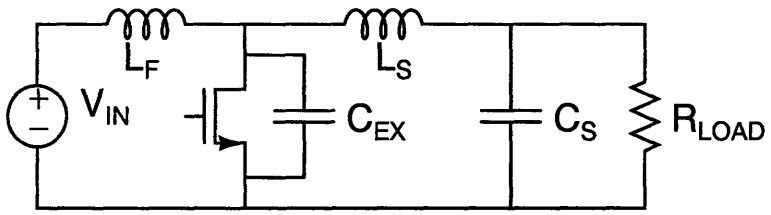


Figure 2.28: **Changing from a high pass matching network, figure 2.14(b) to a low pass one without adding additional component results in a boost converter which can only provide up voltage conversion.**

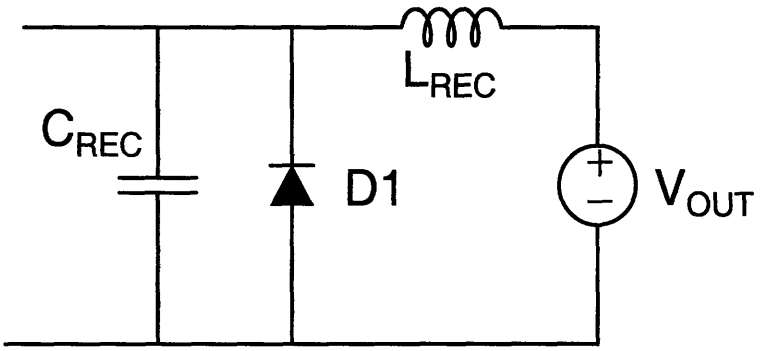


Figure 2.29: **An alternative rectifier topology suitable to be employed with an inverter topology with a low-pass matching network with a blocking capacitor, Figure 2.30**

the power to the load via high frequency harmonics, a characteristic that a low pass matching network cannot offer.

Z_{IN} and its effect on Z_{DS}:

The impedance of the input resonant tank is simply the parallel combination of the impedance of L_F and C_F. As described in Section 2.2.5.2, the resonant frequency of this network determines the speed at which the drain waveform rings. For a given output tank, the input resonant network, together with the inverter's duty ratio, shapes V_{DS} and decides whether ZVS characteristics can be achieved or not. The key characteristics of this resonant network are its resonant frequency, given by $f_c = \frac{1}{2\pi}\sqrt{\frac{1}{L_F C_F}}$ and its impedance at this frequency, given by $Z_o = \sqrt{\frac{L_F}{C_F}}$.

Figure 2.31 and 2.32 demonstrates changes in the resonant frequency and the peak impedance have on the total impedance looking into the drain-source port of the

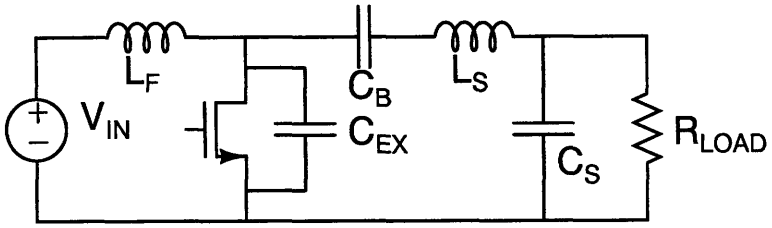


Figure 2.30: **Adding a dc blocking capacitor to figure 2.28 will result in a new inverter configuration that provides up-and-down voltage conversion.**

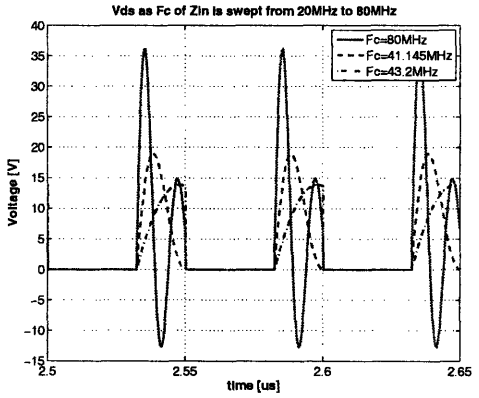
switch Z_{DS} and their corresponding time domain waveforms.

Starting with a tuned inverter with $L_F = 21nH$ and $C_F = 712.5pF$, of which $f_c = 41.145MHz$ and $z_o = 5.42\Omega$, the center frequency and the characteristic impedance are varied independently and their impacts on the inverter are examined.

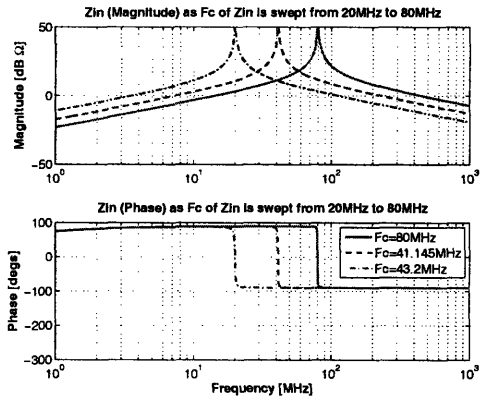
Figure 2.31 demonstrates the cases where the characteristic impedance remains the same while the center frequency is adjusted. When the center frequency of the resonant network is significantly lowered from twice the switching frequency (40MHz) to be close to the switching frequency (20MHz), the low-frequency peak in Z_{DS} becomes more pronounced while the high-frequency peak in Z_{DS} now becomes lower than the low-frequency peak. The dominant low-frequency peak suggests that the resonant network will now ring at a slower speed, which is verified by corresponding time domain waveform. Similarly, when the center frequency is significantly increased to a frequency higher than twice the switching frequency, say 80MHz, the high frequency peak is now moved to even a higher frequency. The low-frequency peak becomes unrecognizable, because the low frequency impedance of Z_{DS} is now dominated by the impedance of L_F and the impedance of the matching network at this frequency range is too high to load down the Z_{IN} to result in a low-frequency peak, Figure 2.31(c). V_{DS} now rings at a higher frequency due to its high-frequency peak and results in the solid switching waveform of Figure 2.31(a).

Varying the characteristic impedance (while leaving the center frequency at 41.145MHz) does not change the speed at which the V_{DS} rings up and down, instead it changes the magnitude of low frequency peak and the total stored energy in the system. Its impacts on the V_{DS} and Z_{DS} are illustrated in Figure 2.32.

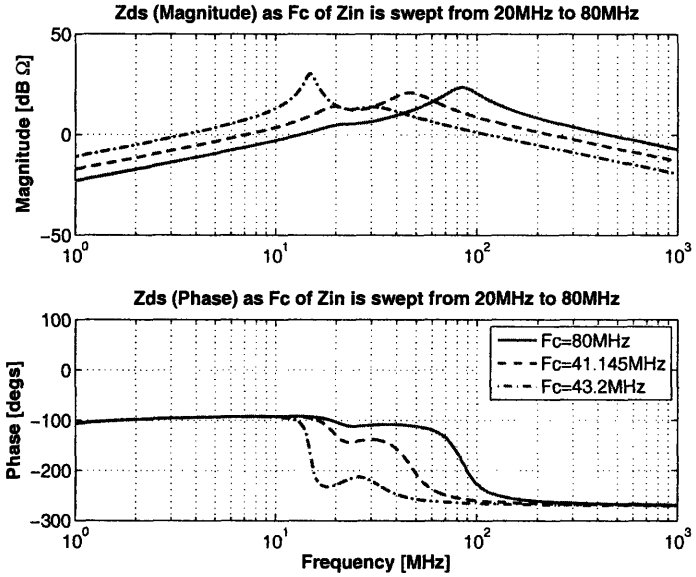
Z_L and its effect on Z_{DS}:



(a) V_{DS} waveforms as F_C of Z_{IN} is swept

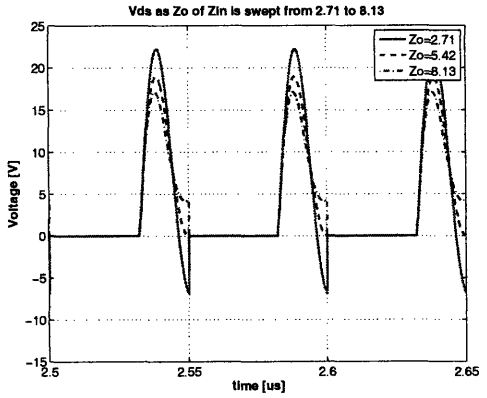


(b) Z_{IN} as F_C of Z_{IN} is swept

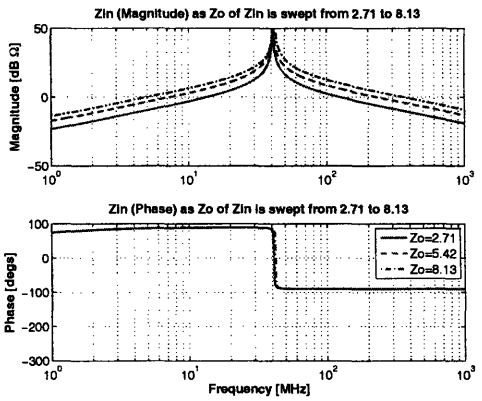


(c) Z_{DS} as F_C of Z_{IN} is swept

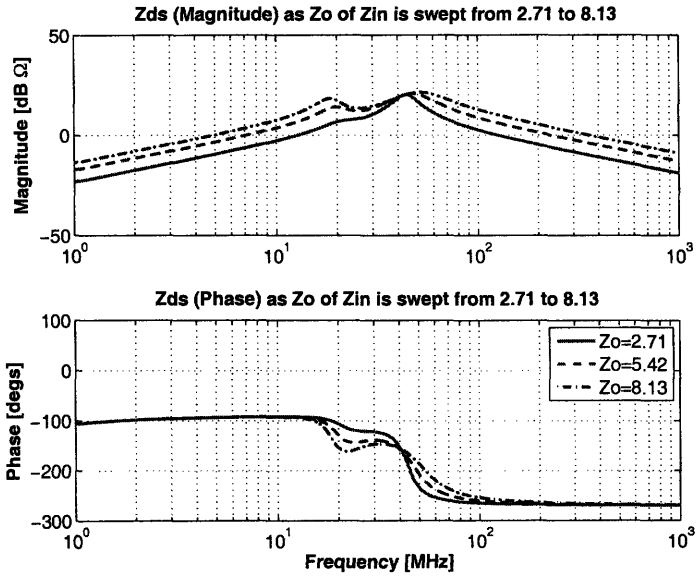
Figure 2.31: **As the resonance frequency of L_F and C_F is swept, the magnitude ratios between the high frequency and low frequency peak of Z_{DS} change. The dominant magnitude peak of Z_{DS} determines the frequency at which V_{DS} rings up and down. The inverter is designed for operation at 20MHz with an ideal switch. The component values C_S and L_S for the matching network are kept the same at $C_S = 720pF$ and $L_S = 70nH$, while L_F varies from 10.8nH to 43.2nH and C_F varies from 366.45pF to 1465.8pF. Inductor Q of 70 and capacitor Q of 3000 is assumed. See appendix A for component values and simulation files.**



(a) V_{DS} waveforms as Z_O of Z_{IN} is swept



(b) Z_{IN} as Z_O of Z_{IN} is swept



(c) Z_{DS} as Z_C of Z_{IN} is swept

Figure 2.32: **As the characteristic impedance of L_F and C_F is swept, the magnitude of the low frequency peak of Z_{DS} changes while the high frequency peak stays at approximately the same magnitude and frequency. The characteristic impedance changes the total energy stored in the network. The inverter is designed for operation at 20MHz with an ideal switch. The component values C_S and L_S for the matching network are kept the same at $C_S = 720pF$ and $L_S = 70nH$, while L_F varies from 10.5nH to 31.5nH and C_F varies from 1425pF to 450pF. Inductor Q of 70 and capacitor Q of 3000 is assumed. See appendix A for component values and simulation files.**

The key characteristics of the high-pass matching network topology for tuning this inverter is its transformation ratio and the frequency at which the transformation ratio is attained. For a given input resonant tank, the transformation ratio along with that frequency determines whether the inverter is operating into a capacitive or inductive load and the maximum amount of power that can be transferred.

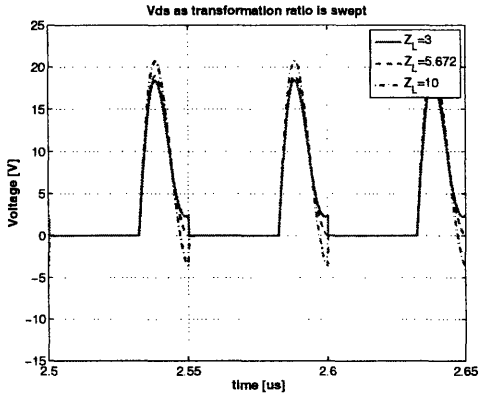
Starting with a tuned matching network with $L_S = 70nH$ and $C_S = 720pF$, of which the transformation ratio is 5.672 and the transformation frequency is 27.4MHz, the changes in total drain impedance Z_{DS} and switching waveforms V_{DS} due to various transformation ratios and transformation frequencies are studied via Figure 2.33, 2.34.

In either case, whether it is varying the transformation ratio while maintaining the transformation frequency or vice versa, changes in the two matching network key characteristics results in the changes in relative magnitude of the low-frequency peak and the high-frequency peak (in certain cases, the low-frequency peak is not unrecognizable) while the frequencies at which the high-frequency peak occurs stay relatively constant, Figure 2.34(c). Comparing Figure 2.32, Figure 2.33 and Figure 2.34, it becomes apparent that changing the transformation ratio and frequency independently of each other results in similar changes in Z_{DS} as varying the characteristics impedance of the input resonant network, Z_{IN} described in the previous section. Not surprisingly, changes seen in the switching waveform V_{DS} due to various transformation ratios and frequencies are also similar to that of changing the characteristic impedance of Z_{IN}.

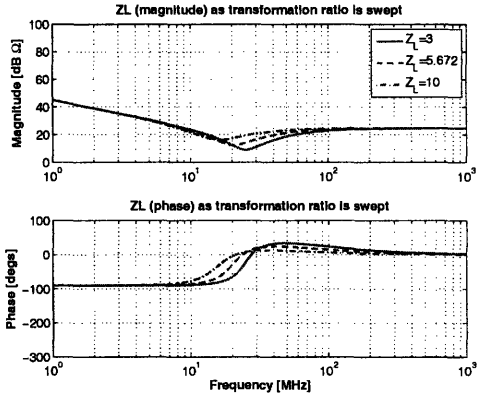
Adjusting Output Power:

The discussion of the previous two sections indicate that changing the transformation ratio (or the frequency at which the transformation occurs) of the matching network has a similar impact on Z_{DS} and V_{DS} as varying the characteristic impedance of the Z_{IN} (while leaving the center frequency intact). Furthermore, the maximum output power level is closely tied to the transformation ratio of the matching network. These two characteristics of this inverter topology suggest a simple approach if output power is to be adjusted.

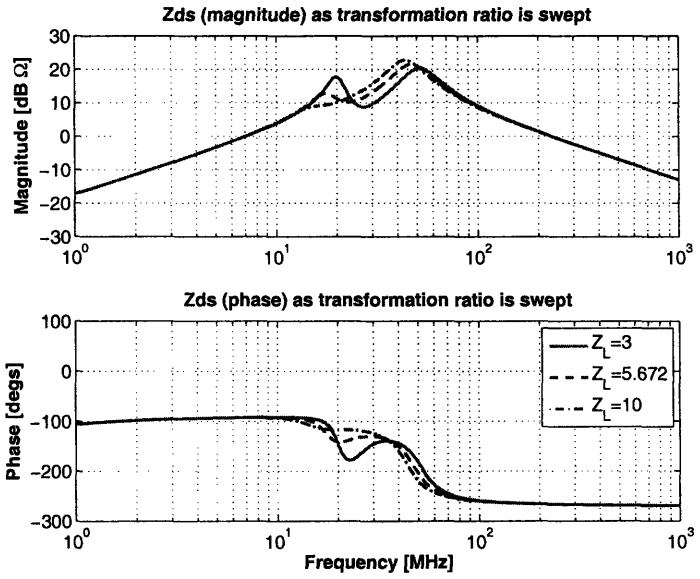
If a favorable operating tuning point is found and the output were to be increased slightly, it can be done by first increasing the matching network transformation ratio without changing the frequency at which the transformation occurs, at which point the ZVS characteristics clearly do not exist. However, the non-ZVS drain waveforms



(a) V_{DS} waveforms as transformation ratio of Z_L is swept

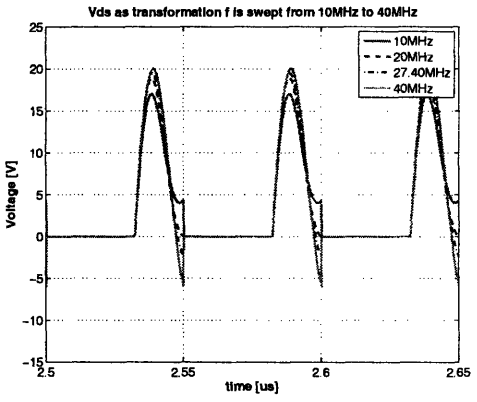


(b) Z_L as transformation ratio of Z_L is swept

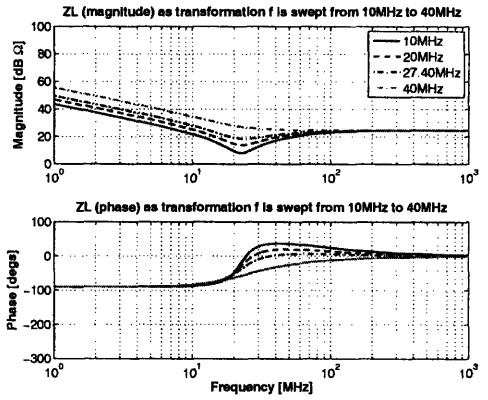


(c) Z_{DS} as transformation ratio of Z_L is swept

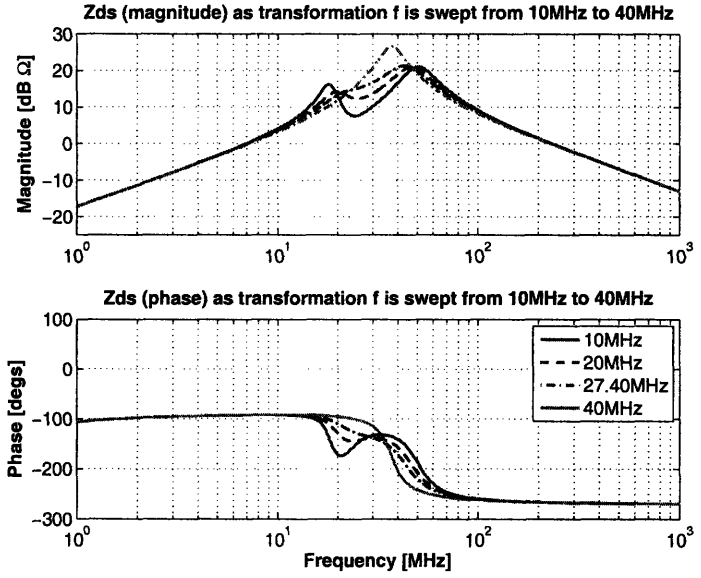
Figure 2.33: **As the matching network input resistance is increased (the transformation ratio decreased), the magnitude of the low frequency peak of Z_{DS} decreases and moves to a higher frequency, the local minima becomes less apparent, and the high frequency peak increases and moves to a lower frequency. The switching waveforms no longer maintains ZVS and zero dv/dt. The inverter is designed for operation at 20MHz with an ideal switch. The component values L_F and C_F for the input network are kept the same at $C_F = 712.5pF$ and $L_F = 21nH$, while L_S varies from 10.5nH to 117.79nH and C_S varies from 891pF to 687pF. Inductor Q of 70 and capacitor Q of 3000 is assumed. See appendix A for component values and simulation files.**



(a) V_{DS} waveforms as transformation frequency of Z_L is swept



(b) Z_L as transformation frequency of Z_L is swept



(c) Z_{DS} as transformation frequency of Z_L is swept

Figure 2.34: **As the matching network transformation frequency is increased, the changes to Z_{DS} and V_{DS} are similar to that of figure 2.33. The inverter is designed for operation at 20MHz with an ideal switch. The component values L_F and C_F for the input network are kept the same at $C_F = 712.5pF$ and $L_F = 21nH$, while L_S varies from 47.95nH to 191.8nH and C_S varies from 1051pF to 262pF. Inductor Q of 70 and capacitor Q of 3000 is assumed. See appendix A for component values and simulation files.**

can then be counter-acted by lowering the characteristic impedance of the input resonant network without varying its center frequency by adjusting C_F in parallel with L_F. If the output power is to be decreased, it can be achieved by decreasing the transformation ratio of the load network and then increasing the characteristic impedance of the input resonant network. Waveforms of inverters of different power levels achieved via this method are shown in Figure 2.35, along with its performance.

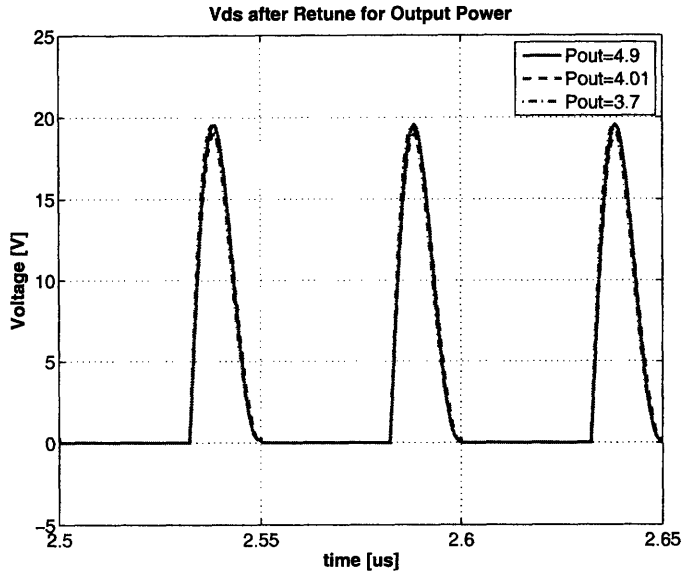
Adjusting transformation ratios and then readjusting the characteristic impedance of the input resonant tank is not the only way to readjust the output power level. Since adjusting the frequency at which a specific transformation ratio occurs can achieve similar impacts on Z_{DS} and V_{DS}, the output power level can also be increased/decreased by increasing/decreasing the transformation frequency (independently from varying the transformation ratio) and increasing/decreasing the characteristics impedance of Z_{IN}, Figure 2.36.

L_F and its impacts on startup:

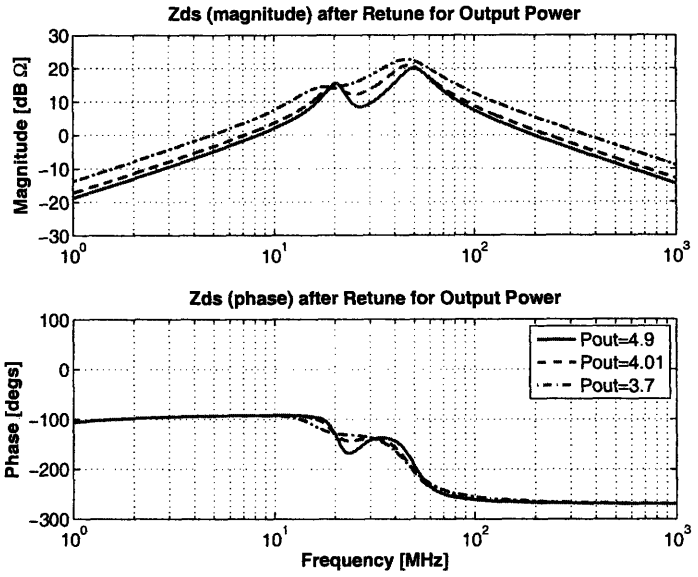
One significant difference between this inverter topology and a conventional class-E lies in the input inductor L_F. In this topology, L_F is a small-valued inductor (tens of nano-henries at 20MHz operating frequency and several watts and volts) which resonates with C_F whereas the input inductor in a Class-E topology is a choke inductor whose value will be around hundreds of nano-henries for a similar design point. Increasing L_F directly degrades the transient response speed, Figure 2.37. The intended control strategy, Chapter 5, relies fast transient performance to minimize losses associated with modulation. Given a modulation frequency, the more time a converter cell operates at steady state (less time at starting up and turning off), the closer the closed-loop efficiency is to open-loop efficiency. The small valued resonant inductor L_F significantly improves the transient performance (compared to that of a Class-E) and makes this inverter topology compatible with the intended control scheme.

2.2.6 Summary

The number of components in this topology, Figure 2.17, along with duty ratio and operating frequency offers a great degree of freedom in designing a converter and an abundant array of design tradeoffs. Furthermore, under different operating conditions

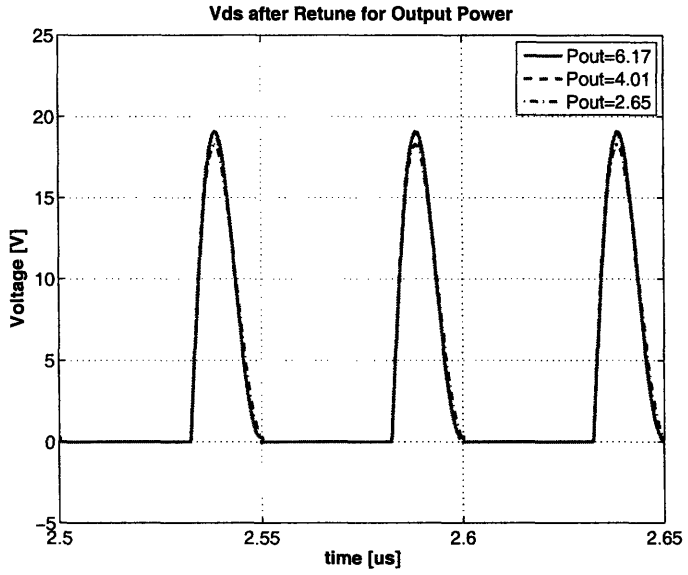


(a) V_{DS} after re-tuned transformation ratio and Z_O to adjust output power

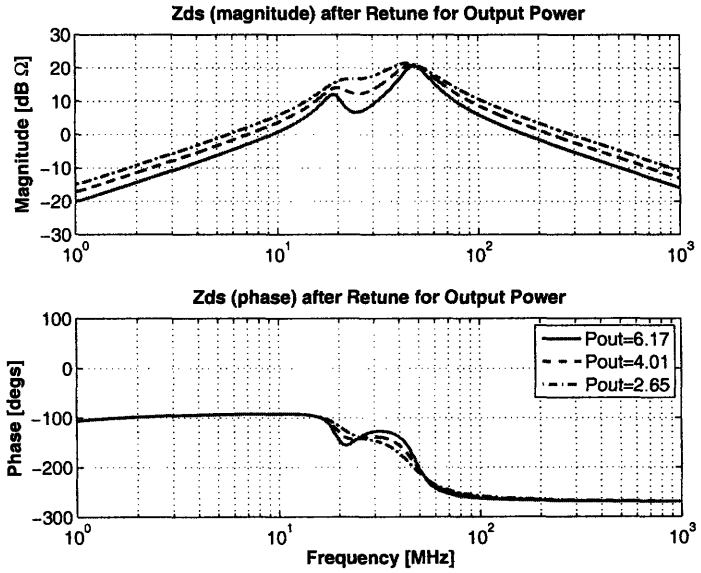


(b) Z_{DS} after re-tuned transformation ratio and Z_O to adjust output power

Figure 2.35: **Once an operating point is established, power may be adjusted by changing the transformation ratio of the matching network in parallel with changing the characteristic impedance of the input resonant network, Z_{IN}. By shifting the overall drain impedance Z_{DS} up and down, different output power levels may be achieved. The inverter is designed for operation at 20MHz with an ideal switch. The values of C_S vary from 891pF to 687pF, those of L_S vary from 17.5nH to 117nH, those of L_F vary from 10.5nH to 31nH, and those of C_F vary from 1425pF to 450pF for different power levels. See appendix A for component values and simulation files.**



(a) V_{DS} after re-tuned transformation frequency and Z_O to adjust output power



(b) Z_{DS} after re-tuned transformation frequency and Z_O to adjust output power

Figure 2.36: **In addition to changing the transformation ratio of the matching network along with the characteristic impedance of the input resonant network, Z_{IN}, changing the transformation frequency of the matching network in parallel with the characteristic impedance can also lead to designs operating at different power levels. The inverter is designed for operation at 20MHz with an ideal switch. The values of C_S vary from 1051pF to 525pF, those of L_S vary from 15nH to 96nH, those of L_F vary from 15nH to 31nH, and those of C_F vary from 997pF to 450pF for different power levels. See appendix A for component values and simulation files.**

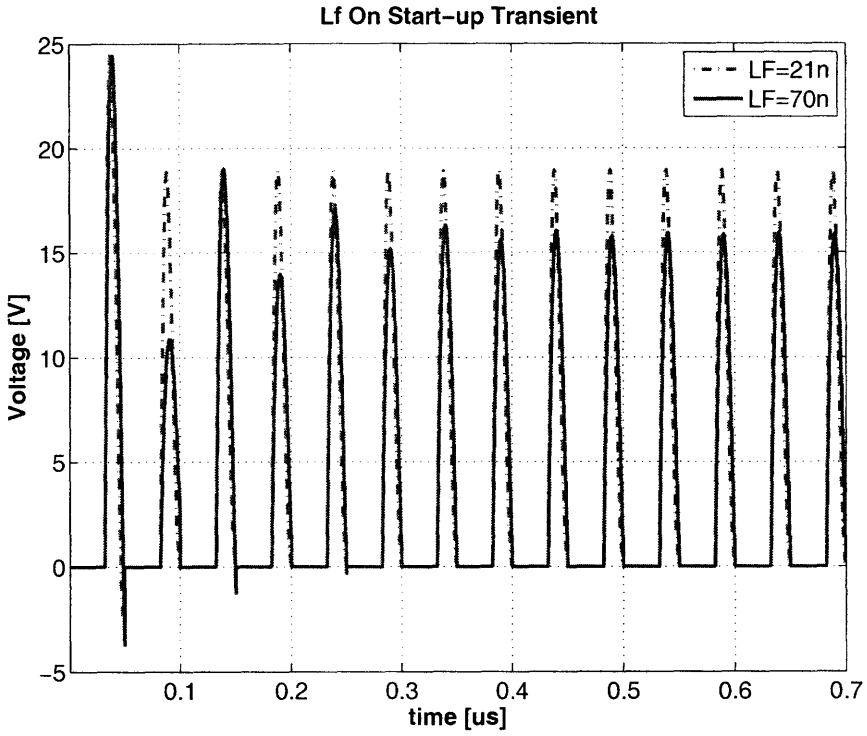


Figure 2.37: **Larger L_F deteriorates the startup transient performance and slows down the settling time. Small valued L_F are preferred with the intended control strategy. The inverter is designed for operation at 20MHz with an ideal switch. When $L_F = 21nH$, $C_F = 712.5pF$, $C_S = 720pF$ and $L_S = 70nH$. When $L_F = 70nH$, $C_F = 205pF$, $C_S = 130pF$ and $L_S = 140nH$. Simulation files and component values may be found in Appendix A**

(such as input voltage, output voltage and output power), the tradeoffs can be entirely different. It is difficult to reach a set-stone design procedure which will lead to a most efficient design. With that being said, blindly sweeping different parameters and component values until a working design however, is no means the only (or the most efficient) way to reach a converter design. From the discussions above, there are some basic procedures that will lead to a working design.

1. Obtain equivalent rectifier input impedance following the rectifier tuning procedure outlined in Section 2.2.3.2
2. Assume the drain voltage may be modeled as a triangle wave of amplitude $\frac{8}{\pi}2V_{IN}$
3. Determine the minimum resistance R_{MIN} needed to deliver the output power with the RMS voltage at the drain and the required output power level with $R_{LOAD,MIN} = V_{RMS}^2/P_{OUT}$.
4. Determine whether a transformation stage is necessary. If so, calculate the transformation ratio required.
5. Select a frequency at which the transformation ratio is to be obtained (it can be slightly higher, lower or at the switching frequency). Based on the transformation ratio and this frequency, calculate the component values required for L_S and C_S from Equations 2.8 and 2.9.
6. A good starting point for L_F is to calculate its value based on Equation 2.10, assuming C_F is entirely provided by a given semiconductor switch.
7. If this initial L_F is not so small that it is on the same order of board and packaging parasitic inductances, it is usually desirable to add external high-Q capacitance in parallel with the switch to reduce circulating losses. A new L_F is obtained based on the amount of C_{EX} added, maintaining the product of L_F and C_F
8. Minor adjustments of the component values may be necessary to find optimum efficiency, transient performance or other design metrics.
9. Output power may be readjusted by varying the transformation ratio (or the transformation frequency) of the matching network along with the characteristic impedance of the input resonant network.
10. Adjust the characteristic impedance of the network for efficiency and component size

11. Iterate as necessary

2.3 The Power Stage

Having discussed the tuning procedures for each of the three major components of a resonant SEPIC converter, shown in Figure 2.5, it remains to connect all these components together to arrive at a dc-dc converter design. Since a matching network is incorporated into the discussion of inverter design in Section 2.2.5, the interconnection can simply done via substituting the resistive load, R_{LOAD}, with a tuned rectifier described in Section 2.2.3.

The previous discussions were mostly made in the context of ideal semiconductor devices (namely MOSFET and diode) so that a thorough study could be done on each of three major components of a converter without introducing additional complexity. A practical converter implementation requires a careful examination of device characteristics as they may tremendously impact the achievable impedance and the performance of a otherwise well-designed converter.

2.3.1 Device Selection Considerations

Figure 2.38, adopted from [3], is an accurate representation of a real switching device, MOSFET, including its parasitic elements. Due to major loss mechanisms associated with each parasitic element, they are important to the operation of HF resonant converters [3, 18, 17], such as the one being pursued in this thesis. C_{ISS} and R_G are both key parameters in determining power dissipation at the gate as is, apparent from Equation 2.4. Even with a low-loss resonant gate drive method (to be discussed in Chapter 4), good overall efficiencies will be impossible to achieve with a MOSFET with too large of a gate resistance and/or gate capacitance, especially in the case of a low-power converter application [25]. The displacement current loss associated with C_{OSS} and R_{OSS} can be another major loss mechanism in a HF resonant converter. In addition, larger on-state resistance R_{DS-ON} directly translates to larger conduction loss, a device characteristic that can substantially deteriorate the performance of a converter.

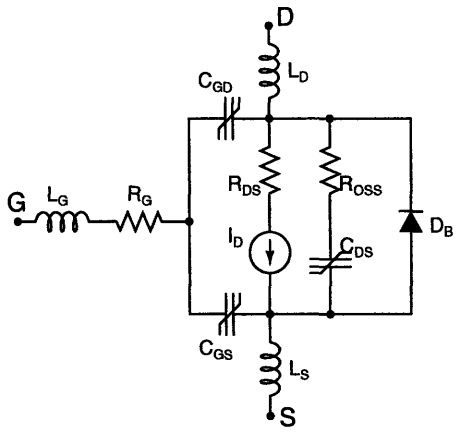


Figure 2.38: **The MOSFET parasitic elements important to Φ_2 converter operation must be accounted for at design time.**

In addition to their direct ties with major loss mechanisms in a HF resonant converter, device parasitic elements can also affect a converter performance in numerous other ways [3]. When C_F is entirely comprised of the output device parasitic capacitance, the minimum characteristic impedance is reached and the value of L_F could be determined if they are to be at resonance at twice the switching frequency as described by the tuning procedure in Section 2.2.5.2. When C_F is not comprised of C_{OSS} alone, device parasitic inductances L_S and L_D may deteriorate the converter efficiency by resonating with the external capacitor and resulting in undesirable ringing behaviors, shown in Figure 2.39. R_{DS-ON} with respect to V_{GS} is also an important parameter that determine how large the gate voltage amplitude is required to fully enhance the device, which directly impacts the gating loss. The feedback from drain to gate caused by capacitance C_{GD} may help attain a required gate voltage amplitude (to fully enhance a device given a duty ratio and a dc offset gate voltage) when the drain to gate transfer function has a phase close to 180°. However, C_{GD} may also contribute to additional gating loss by increasing effective reverse capacitance via the Miller effect.

The impacts that device characteristics have on a converter performance are studied via three $30V$ commercial MOSFETs: Vishay-Siliconix vertical MOSFET $SI4346DY$, Greatwall LDMOSFET $GWS12N30$ and Sync Power vertical device $SPN1443$; key device parameters are listed in Table 2.3.1. The $SI4346DY$ offers a good tradeoff between losses due to parasitic capacitance and channel resistance. This device would have been a suitable candidate for a practical implementation, except that it comes in a relatively large package $SO-8$ with a packaging inductance of nearly $2nH$.

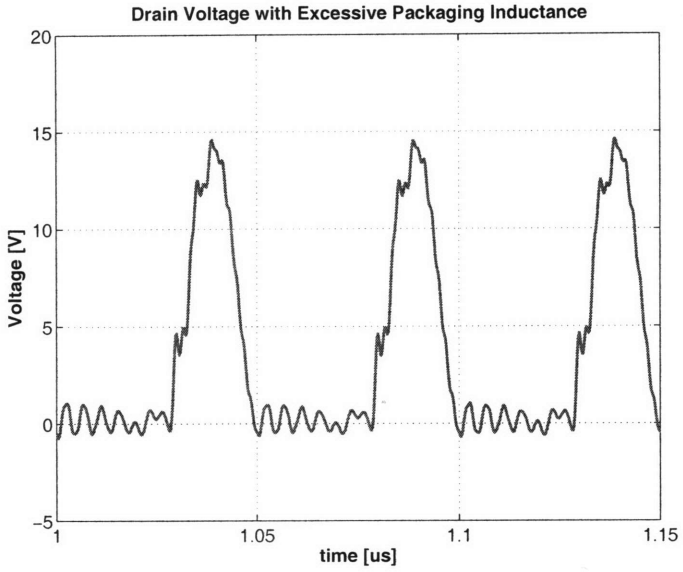


Figure 2.39: **Drain voltage waveform when excessive device packaging inductance is present.**

This package inductance resonates with the external capacitor, and significantly deteriorates the waveforms and performance, and offsets the advantages the otherwise excellent device characteristics bring. On the other hand, the $GWS12N30$ comes in a Ball Grid Array (BGA) package that minimizes the package inductance, Figure 2.40. However, the extremely low on-state resistance and the relatively large device parasitic capacitance does not offer a good loss tradeoff for a converter targeting at the specifications listed in Table 1.1. A $12W$ converter utilizing the topology shown in Figure 2.5 would be an appropriate application for such a device. The $SPN1443$ is a vertical device in a $SOT-23$ package based on which a full dc-dc converter will

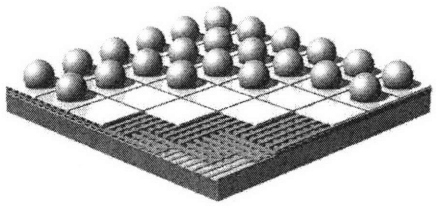


Figure 2.40: **BGA devices can minimize parasitic inductances associated with packaging. Figure adopted from $GWS12N30$ datasheet. The package layout strategy for this device is described in [36]**

Values of MOSFETs' Parasitic Elements					
	R_{DS-ON}	R_G	C_{ISS}	C_{OSS}	C_{RSS}
$SI4346DY$	$32m$	0.5	$1049pF$	$273pF$	$124pF$
$GWS12N30$	$5m$	0.388	$2600pF$	$1250pF$	$200pF$
$SPN1443$	$75m$	1.17	$593pF$	$83pF$	$43pF$

Table 2.1: **Values of key device characteristic parameters for different $30V$ commercial MOSFETs. Note that the values of $GWS12N30$ are taken directly off the datasheet whereas the parameter values for the other two devices were measured experimentally on Agilent 4195A.**

be designed and implemented. The device has relatively low parasitic capacitance, reasonable channel resistance and gate resistance, as Table 2.3.1 indicates.

Parasitic elements in diodes are equally important. Circulating current loss associated with junction capacitance, undesired ringing and waveform distortions caused by package inductance, conduction loss associated with forward voltage drop are just a few examples illustrating the importance of finding a suitable device. The $DFLS230L$ is a Schottky diode (which can avoid occurring reverse recovery losses associated with minority carrier devices like conventional P-N junction diode) with a low forward drop ($0.3V$), low parasitic capacitance and small packaging inductance. These characteristics makes the device a desirable candidate with which the resonant rectifier design will be implemented.

The procedures for extracting parasitic components for these two types of semiconductor devices are well-described in [17, 3, 18], and thus are not repeated here. The vales of parasitic components are summarized in Table 2.3.1.

2.3.2 Converter Design

With the tuning procedures discussed in Section 2.2.2 for each of the three subsystems of the resonant SEPIC converter along with the two suitable semiconductor devices ($SPN1443$ and $DFLS230L$), a practical implementation of a $20MHz$ dc-dc converter can now be designed.

The design starts with tuning the resonant rectifier following the procedure described in Section 2.2.3. With a diode model including all parasitic components of the

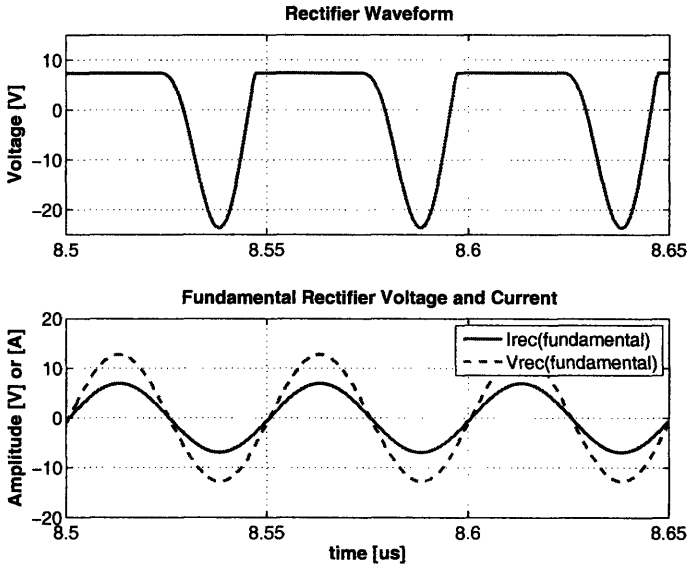


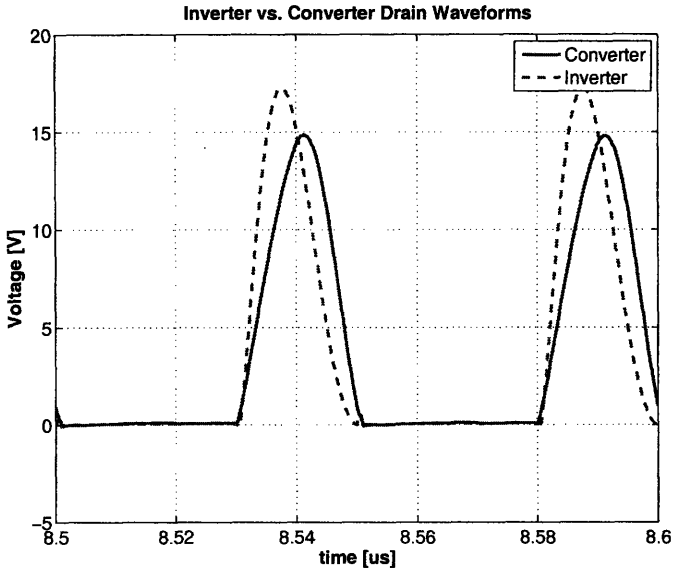
Figure 2.41: **Waveforms for a tuned rectifier with Schottky diode $DFLS230L$, $L_{REC} = 121nH$, $C_{REC} = 153pF$. Simulation files may be found in Appendix A**

$DFLS230L$, the rectifier, Figure 2.8(a), is tuned (by adjusting L_{REC} and C_{REC} to appear resistive at the fundamental when the driving current source is $0.7A$ at an output voltage of $7V$ to provide an output power of about $3W$. Figure 2.41 shows the rectifier waveforms and the fundamental voltage and current, from which the rectifier equivalent resistance, V_F/I_F can be extracted.

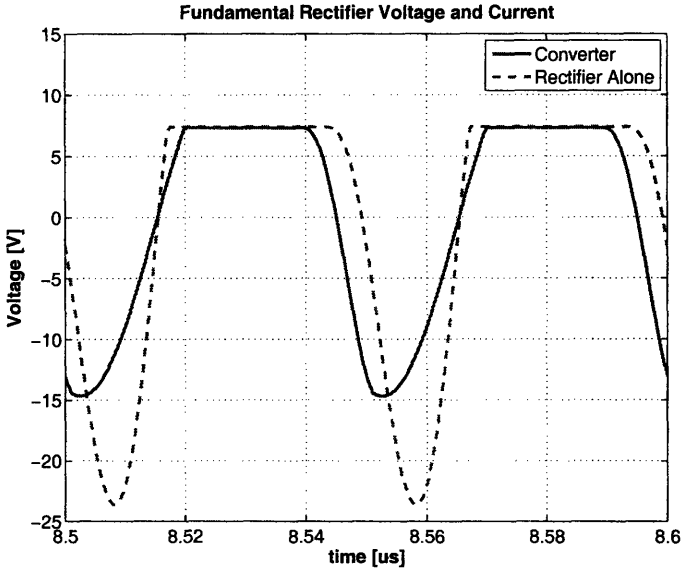
The equivalent rectifier resistance, $R_{LOAD} = 18.63$ can now be used to tune the inverter along with the matching network, shown in Figure 2.5. L_F and C_F including the device parasitic capacitance and any additional external capacitor is tuned to resonate at about twice the switching frequency if a duty cycle of 50% is to be obtained (if a duty ratio other than 50% is to be achieved, the resonant frequency can be adjusted accordingly). As the attainable Q of external capacitance is much higher than the device parasitic capacitance and the achievable inductor Q of inductor, it is desirable to tradeoff a large inductor with a large external capacitor in order to achieve better efficiency (in addition to better transient performance). However, the value of L_F can not be on the same order of magnitude as the board parasitics and device packaging inductance. Otherwise, the performance will be severely deteriorated by these lossy parasitic elements. In this case, $L_F = 31nH$ and $C_{EX} = 520pF$ provides a good tradeoff. The transformation ratio that the matching network is required to

achieve is given by R_{LOAD}/R_{MIN} where R_{MIN} is the minimum resistance for the input voltage to deliver the required output power (which can be calculated by following the procedure outlined in Section 2.2.4). With the required transformation ratio along with the switching frequency, the component values of the matching network can be obtained: $C_B = 1000pF$ and $L_S = 105nH$.

When the inverter and rectifier are connected, the drain waveforms and the output power level may be slightly different from what the inverter provides due to the non-linear interaction between the inverter/matching network with the rectifier; and minor additional tuning may be required to achieve ZVS and the required power level. If the converter is no longer displaying ZVS characteristic, minor adjustments to component values, by changing the center frequency of C_F and L_F or L_S and C_S following the same procedure outlined for achieving ZVS in tuning an inverter in Section 2.2.5.1, will lead to soft-switching drain voltage waveforms. If the power level of the converter is lower than required, the impedance of all components may be lowered until the output power is as desired. On the other hand, the impedance of all components may be increased by the same factor to maintain the overall switching behaviors if the output power is higher than desired. In this case, connecting the rectifier directly with the inverter/matching network subsystem resulted in a converter with a similar drain waveform as Figure 2.31(a)(slightly off from ZVS). Therefore, C_F and L_F are adjusted in parallel until the desired soft-switching characteristic is achieved. Additional tuning is also needed to adjust the output power level as the converter delivers more power ($6.4W$) than required. Consequently, the impedance of all components are increased until the appropriate output power level is attained. While the minor additional tuning may take a few iterations to achieve the desired output power level and switching characteristics, it can be done very quickly. Figure 2.42 shows the final converter simulation waveforms. The component values for a tuned rectifier (with the rectifier fundamental voltage and current in phase), a tuned inverter (achieving ZVS and zero dv/dt, and meeting the output power requirement with the equivalent resistance of a tuned rectifier), and a tuned converter (after component values are adjusted to provide the desired output power level and soft-switching behaviors) are listed in Table 2.3.2. As Figure 2.42 indicates, the drain and rectifier waveforms are not identical for those of a converter as that of an inverter or a rectifier due to the non-linear interaction between the two subsystems. The experimental results for such a converter implementation will be presented in Chapter 6.



(a) Drain Waveforms



(b) Rectifier Waveforms

Figure 2.42: **Waveforms of drain and rectifier waveforms of a full dc-dc converter with the drain waveform of an inverter and the waveform of a standalone rectifier, using the component values listed in Table 2.3.2. The changes in waveforms are mainly to the non-linear interaction between the inverter and the rectifier. See appendix A for component values and simulation files.**

Component	Inverter	Rectifier	Final dc-dc Converter
L_F	$31.05nH$	n/a	$24nH$
C_F	$520pF$	n/a	$780pF$
L_S	$105nH$	n/a	$70nH$
C_S	$1000pF$	n/a	$1250pF$
L_{REC}	n/a	$121nH$	$125nH$
C_{REC}	n/a	$100pF$	$150pF$
$f_S W$	$20MHz$	$20MHz$	$20MHz$

Table 2.2: **The components of the dc-dc converter example are listed in this table. More detailed information including the full spice models and values of parasitic inductances may be found in appendix A**

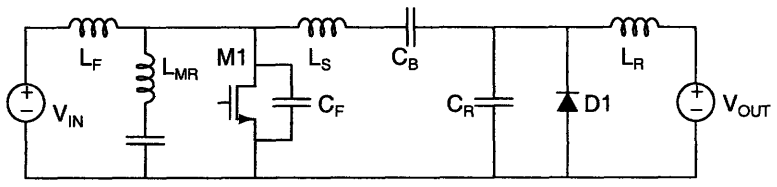
2.4 Comparison with other Resonant Topologies

The quasi-resonant SEPIC topology is by no means the only HF resonant topology which can provide efficient operation across wide operating ranges. There are other resonant inverter designs such as $\phi 2$ inverter [6, 7, 24, 17, 3], when connected with similar resonant rectifier designs, have proven their salient performance in the VHF regime. Before selecting the quasi-resonant SEPIC topology as the final candidate based on which an practical implementation is built, a comparison study exploring the advantage and disadvantages of this topology with three other potential resonant converter designs will provide further insights of design tradeoffs in resonant power conversion in the HF and VHF regime.

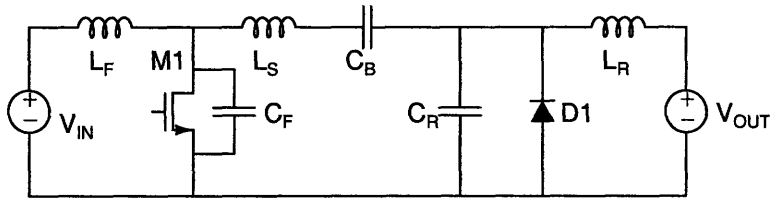
Figure 2.43 illustrates several other topologies whose performance is compared with that of the quasi-resonant SEPIC converter studied in this chapter.

The comparison discussion is conducted via comparing the performance across the entire input voltage range ($3.6V$ to $7.2V$) at the nominal output voltage $7V$ with an output power of $3.9W$ at $V_{IN} = 3.6V$ and $V_{OUT} = 7V$.

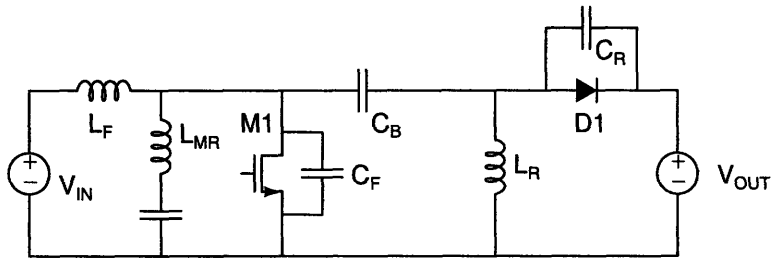
The drain voltage waveforms are displayed in Figure 2.44(a). It is apparently that voltage stress from $\Phi 2$ converter topologies in Figure 2.43(a) and 2.43(c) is much lower, as [6, 7, 24, 17, 3] predict. However, it is difficult to take advantage of the device voltage reduction given available semiconductor devices. Using the same device in the $\phi 2$ designs as in the topology studied here does not result in a favorable efficiency improvement, as shown in Figure 2.44(b). As efficiencies of the topology



(a) Alternative Topology 1



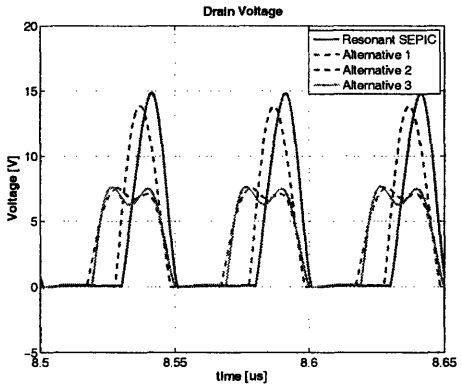
(b) Alternative Topology 2



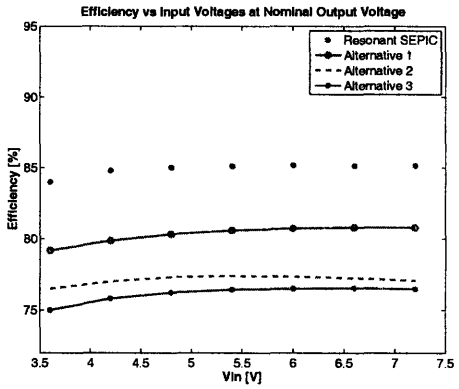
(c) Alternative Topology 3

Figure 2.43: **Other resonant topologies on which a comparison study is conducted. Figure 2.43(a) utilizes a similar matching network and rectifier topology with a $\phi 2$ inverter. Figure 2.43(b) utilizes a similar inverter topology with an alternative matching network and rectifier configuration. Figure 2.43(c) utilizes a $\phi 2$ inverter with an alternative matching network and rectifier configuration.**

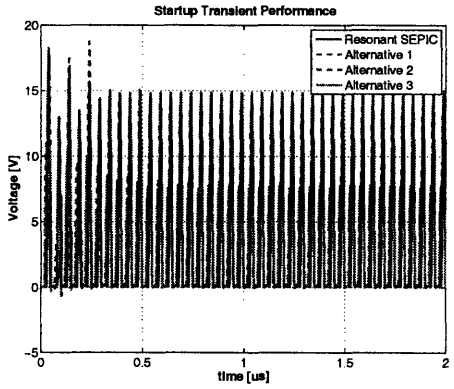
studied in this thesis are much higher than the other three resonant topologies, the quasi-resonant SEPIC topology is a much more suitable candidate for implementing a converter with the required input/output voltages and output power level. The transient performance of all four topologies are similar, Figure 2.44(c), due to utilization of small-valued inductors in all topologies. Simulation files and component values for all topologies may be found in Appendix A.



(a) Drain Voltages



(b) Efficiencies



(c) Transient Performance

Figure 2.44: **Drain Voltages, efficiencies and transient performance comparison of all four topologies. Topologies of Figure 2.43(a) and 2.43(a) achieves lower device stress, while the topology being pursued in this thesis, Figure 2.5, is well-suited to achieve high efficiencies in the required operating regime. The transient performance of all topologies are similar.**

Chapter 3

Inductor Design

AMONG the major loss mechanisms associated with switch mode power supplies (SMPS), including device conduction loss, switching loss, gating loss and inductor loss, the latter two are areas yet to be addressed. The discussions made so far have been more focused on the tuning procedure of achieving certain desirable impedance characteristics in the frequency domain with the SEPIC topology in order to achieve zero-voltage-switching waveforms in the time domain. While this technique mitigates switching losses associated with voltage-current overlap loss and reverse recovery loss via soft switching, the benefits of utilizing such a resonant topology at HF can easily be offset by substantial magnetics loss and gating loss (to be address in Chapter 4), resulting in unsatisfactory overall efficiency. This chapter will discuss the opportunities and challenges in inductor designs via a comparison study of commercial off-the-shelf air-core inductors, custom designed air-core inductors, and planar spiral inductors.

3.1 Air Core Inductors

Core losses associated with inductor constructed with conventional magnetic materials have a frequency dependent loss proportional to f^k where k is typically a constant between 1 and 3 [1]. The significant amount of loss associated with employing cored inductor at HF and VHF regime is yet another reason that most conventional switch-mode converters operate well below $10MHz$. However, with the operating frequency regime, the application being pursued in this thesis is designed at ($20MHz$ to $30MHz$), air-core inductors can be employed, eliminating frequency dependent core losses.

3.1.1 Commercial Air Core Inductors

With the inductors listed under the converter implementation component values, Table 2.3.2, commercial off-the-shelf coreless inductors such as the midi-spring and mini-spring designs offered by Coilcraft are attractive options. At $20MHz$, the measured Qs for a $22nH$ Coilcraft inductor (B07T) is about 67; that for a $43nH$ inductor (B10T) is about 73. While Qs for similar component values of larger packaged inductors are slightly higher (with Qs now ranging from 73 to 76), the additional volume increases the converter size and detriments the overall power density, and therefore is deemed unsuitable as miniaturization is a one major design concern.

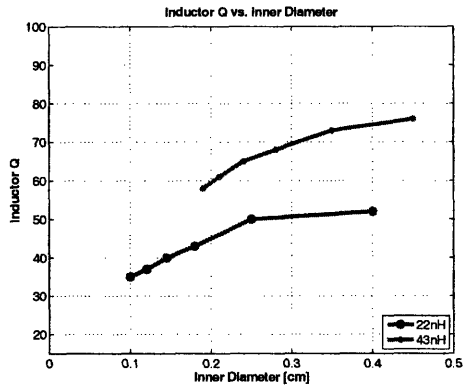
3.1.2 Air-cored Solenoid Inductors

Single-layer solenoid inductor can be designed via an iterative techniques to achieve accurate inductors with good Qs [37]. Using a air-core analysis program utilizing the technique above, a solenoid inductor can be designed given a inner diameter size and the desired inductance. Figure 3.1 illustrates the design tradeoffs in custom designed air-cored solenoid inductors for the application considered here. Generally, the observed tradeoffs are as follows: Given an inductor value and a wire diameter, the achievable Q typically gets better as the allowable inside diameter as gets larger. In addition, smaller number of turns typically results in higher Qs for a given inductor value and wire diameter. Also, the maximum achievable Q for a given inductor value tends to go up as the wire diameter increases.

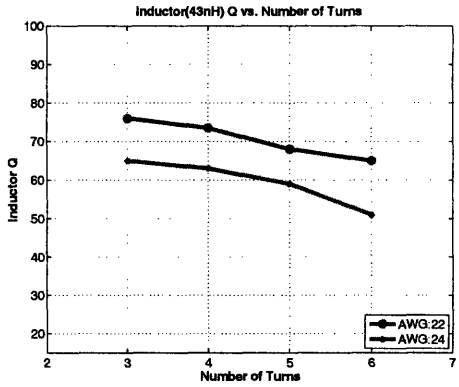
3.1.3 Multi-layer Air-Cored Toroidal Inductors

With the techniques introduced in [38] for design of multi-layer air-cored toroidal inductors, a significant size improvement may be achieved compared to off-the-shelf air-core inductors. In [38], inductance for a single layer toroid with circular winding section can be obtained via the following equations, where W is the total length of wire required, N is the number of turns of required, and d is the wire diameter:

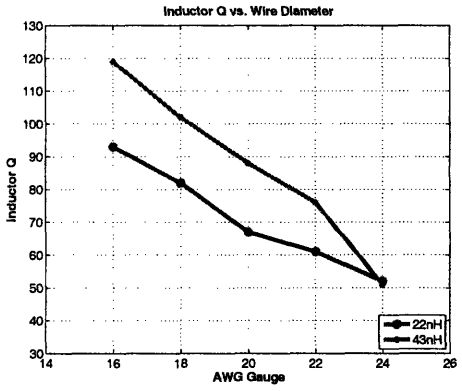
$$\frac{L}{L_0} = 0.2722k^{1.5} + 0.25k \tag{3.1}$$



(a) Inductor Q as the wire size changes



(b) Inductor Q as the number of turns changes



(c) Maximum attainable Inductor Q as the wire size changes

Figure 3.1: **These plots illustrate design tradeoffs for air-core solenoids designed at $20MHz$ using the methods of [37]. All simulated values for Qs are obtained at $20MHz$. Copper wire with a resistivity of $1.72^{-8}\Omega m$ is used in all cases. In 3.1(a), a 24 AWG gauge wire is employed. Given an inductor value and a wire diameter, the achievable Q tends to get better as the allowable inside diameter as gets larger. Smaller numbers of turns typically results in higher Qs for a given inductor value and wire diameter. Also, the maximum achievable Q for a given inductor value typically goes up as the wire diameter increases.**

$$N = 0.8165k^{1/2} \tag{3.2}$$

$$L_0 = \frac{\mu_0 d}{2\pi} \tag{3.3}$$

$$k = W/d \tag{3.4}$$

For an inductor of $22nH$ using 24 gauge wire, 8 turns with a $41mm$ long wire is needed to achieve such an inductor. Such an inductor is certainly not trivial to construct, especially when uniformity is desired to achieve an optimum design. The situation is further exacerbated in a multi-layer design, when even more turns are required to be packed into a smaller volume.

3.2 Planar Spiral Inductor Design

Limitations with planar magnetic structures such as limited power handling capability and the reality of magnetic scaling laws [39] have prevented them from being widely utilized in many magnetic applications. However, planar inductors offer the advantage of integration, small size and reproducibility, all of which are extremely desirable for achieving a small-sized converter with miniaturization and integration potential. While planar spiral inductor designs are difficult to achieve for bulky choke inductors within a small allowable area without introducing magnetic substrate, the small-valued resonant inductors in the ranges of $20nH$ to $40nH$ needed in this converter implementation provide a good application for planar spiral inductor designs.

3.2.1 Hand Calculations

The following is a list of design rules developed to optimize planar spiral inductor Qs [39].

Symbol	Description
a	Mean radius of circular coil (m)
c	Radial thickness of coil
N	Number of turns
R_o	Outer radius (m)

Table 3.1: **Table of Symbols for Inductors**

1. The maximum inductance is achieved with a square geometry, for a given outer diameter. However, attainable Qs for a square planar spiral is lower (on the order of 10%) than its circular spiral counterpart [40].

2. The resistance of a spiral inductor may be minimized by tapering the widths of the turns [41].

3. For a given area, having as wide a conductor path as possible helps to achieve highest Q. Therefore, conductor-to-conductor spacing should be much less than the conductor width [39].

4. Using conductor thickness of 1-3 skin depths is necessary in order to attain high-Q inductors. At 20MHz, 1-3 skin depths is about 0.0005-0.0015" which makes 2 ounce copper traces with 0.001" width sufficient [42]

5. When the inner coil diameter is one-fifth of the outer coil diameter for circular spiral coils, maximum Q can be achieved for this configuration [43]

Based on the previous design rules, circular spiral structure is selected as the primary structure based on which planar inductors will be designed, due to the better attainable Qs.

Numerous equations are available to calculate the inductance of a circular spiral coil. Parameters for the following equations are listed in Table 3.2.1 and illustrated in Figure 3.2.

Equation 3.5 offers a quick means to hand calculate the inductance associated with spiral inductor where L is in henries, n is the number of turns, and r is the radius of the spiral in meters. This equation does not take the effects of how the shape (whether it's square, hexagonal, or circular) may affect the inductance, and thus only provides a crude zeroth-order estimate (within 30% of the correct value) [44].

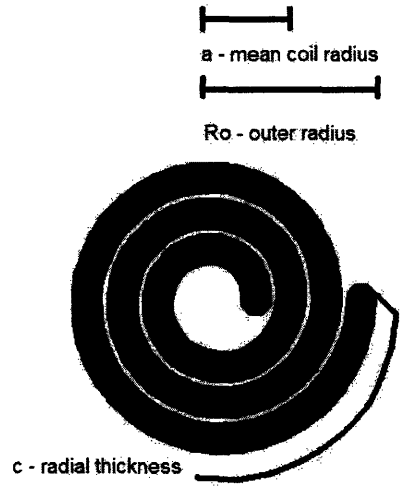


Figure 3.2: **Parameters used in spiral inductor hand calculations**

$$L = \mu_0 N^2 r \tag{3.5}$$

Using the Grover method [45],

$$L = 0.1aN^2P \tag{3.6}$$

where L is in μH, a is the mean radius in meters and P is a function of radial thickness of $c/2a$ where c is the radial thickness of coil. Figure 3.3 shows the corresponding P for a given $c/2a$.

In [46], where R_o is the outer radius of a coil in meters and L is in μH, the inductance for a circular planar spiral inductor can be obtained from

$$L = 0.1748\mu_0 \pi R_o N^2 \tag{3.7}$$

When windings are used over the entire area [47], the inductance can be calculated via

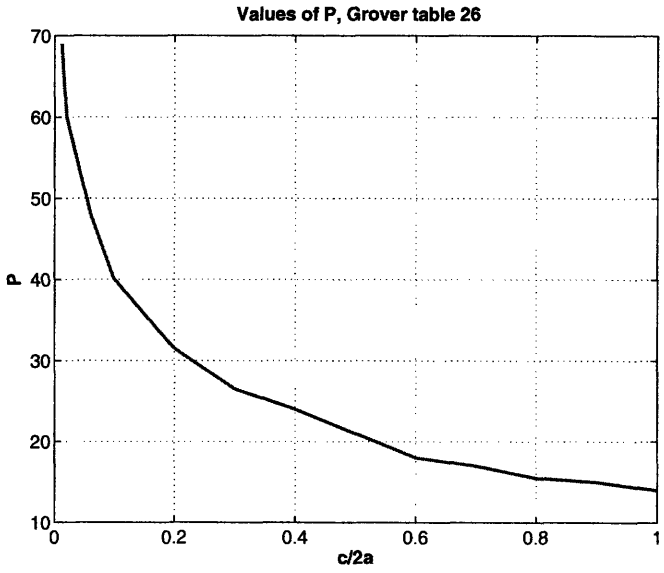


Figure 3.3: **Function P, from Grover, Table 26, pp.113**

$$L = 0.0349N^2 \frac{a^2}{8a + 11c} \tag{3.8}$$

In designing circular spiral inductors for inductors appropriate for this application (with values in the range of $20nH$ to $40nH$), the number of turns implemented is obtained by averaging calculated N from all of the equations above and rounding off to the nearest turn. The AC resistance of the coil is calculated by Equation 3.9 (where a is the mean coil radius, N is the number of turns, and W is the trace width) along with the low frequency resistance R_{DC} of the coil found via the dimensions of the copper trace required. The Q of a circular spiral inductor can then be obtained from $Q = 2\pi fL/R_{ac}$, where

$$R_{ac} \approx \frac{2Na\pi}{\sigma\delta W} \tag{3.9}$$

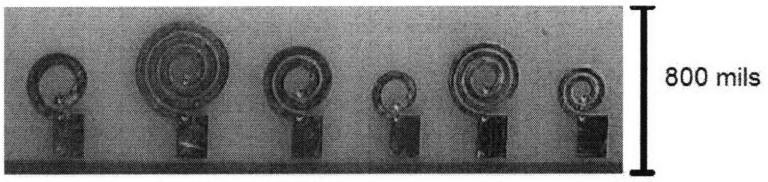


Figure 3.4: **Spiral Inductor Implementation**

Spiral Inductor Value	Measured Q at 30MHz
$3nH$	37
$27nH$	43
$49nH$	51
$72nH$	80

Table 3.2: **Planar spiral inductors and their Q at 30MHz**

3.2.2 Spiral Inductor Implementation

With CAD tools such as EAGLE along with simulations tools such as FastHenry, a spiral inductors (given a trace width, number of turns, and trace spacing) can be easily designed, laid out and evaluated. Spiral inductor design ULPs (spiral-coil.zip and print-inductor.zip) can be downloaded from Eagle CAD official web site. The ULPs allow users to enter information such as the number of turns, the trace width, and the trace spacing, based on which planar spiral inductors are designed. The spiral inductor designs can then be exported to generate FastHenry simulation files to obtain inductor Qs. Figure 3.4 shows initial designs of circular spiral inductors ranging from $3nH$ to $70nH$ designed with 2 ounce copper trace, achieving Qs from 37 to 80 at $30MHz$. The second inductor terminal is brought out on the other side of the circuit board.

Chapter 4

Resonant Gate Drive

EFFICIENT dc-dc power conversion in HF and VHF regime not only imposes challenges on the power stage, but also introduces obstacles in the implementation of gate drive circuitry. For low-power applications, such as the one being pursued in this thesis, gating loss can easily becomes a major loss mechanism, if not carefully designed, which compromises the overall converter performance substantially.

While use of fixed-frequency and fixed duty ratio operation reduces driver complexity, the use of on-off control of the output, which will soon be discussed in Chapter 5, introduces some important requirements. In addition to achieving low power operation at steady state, a practical gate drive for the system must settle rapidly at startup and shutdown to maintain good converter transient response and high efficiency under modulation. A low-loss gate drive method is designed to meet these criteria for this converter.

This chapter first explores different gate drive schemes, their advantages and disadvantages when being utilized in HF operation. Later a low-loss sinusoidal resonant gate drive design, consisting of an oscillator, a drive circuit, a resonant tank and a pull-down network, suitable for high frequency and low power power conversion will be discussed.

4.1 Hard Gating

A totem pole driver scheme, illustrated in Figure 4.1, is a commonly-used gate drive technique for conventional converters switching at relatively low frequencies (1MHz or below). For switching periods much longer than the time constant $C_{GS}R_G$, which usually holds for low frequency operation, the gate voltage is approximately a square

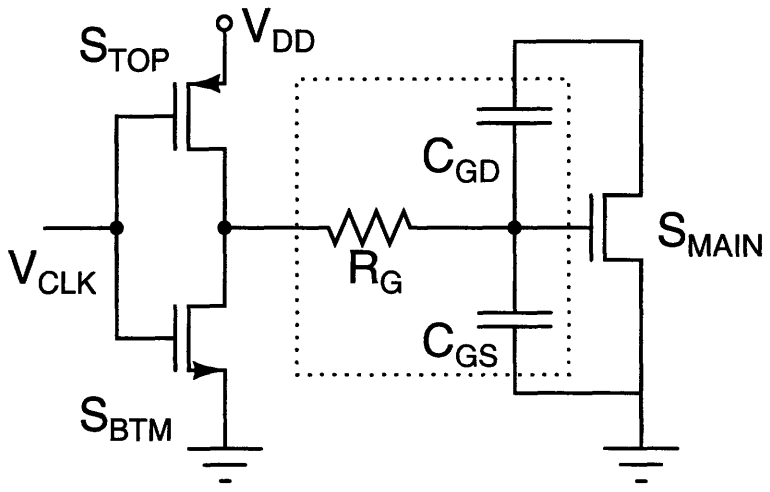


Figure 4.1: **Hard-switched totem pole gate drive**

wave [18]. In a hard switched gating scheme, energy associated with charging and discharging the device input capacitance, C_{ISS} is completely dissipated every cycle. For a converter hard-switched at a frequency f, the power loss associated with gating is described by Equation 1.1, $P_{GATE} = Q_{GATE}V_{GATE}f \approx C_{GATE}V_{GATE}^2 f$. Furthermore, the previous equation merely describes a theoretical loss calculation associated with a gate voltage of a perfect square wave. In practice, when shoot-through current spike is present, a finite amount of time (t_{ON} and t_{OFF}) required to turn S_{TOP} and S_{BOTTOM} on and off introduces yet more power dissipation and even cause device failures.

From Equation 1.1, hard-switched gating loss clearly has a linear dependency on frequency , which often becomes a limiting factor for efficient high frequency switching for traditional topologies. This situation is exacerbated in low power applications, where hundreds of milliwatts can easily translate to an efficiency impact of 10% or more. Therefore, in order to achieve acceptable performance (and battery life) for low power electronic applications (operating in HF regime to maintain a portable size), an alternative gate drive approach must be sought after.

Component	Hard Gating	Sinusoidal Resonant Gating
f_{SW}	$20MHz$	$20MHz$
C_{ISS}	$650pF$	$650pF$
$V_{Gate,amplitude}$	$5V$	$4V$ with $2.5V$ dc bias
R_{Gate}	N/A	1.17Ω
$Power$	$325mW$	$73mW$

Table 4.1: **Hard gating requires more than six times as much power for a typical commercial $30V$ switching device at $20MHz$.**

4.2 Resonant Gating

To mitigate significant losses incurred by conventional hard-switched gating schemes at HF, resonant approaches that recover a part of the energy required to turn on/off the semiconductor switch each cycle may be utilized. In resonant gating topologies, semiconductor switching is accomplished via ringing charge on and off the gate capacitance [17, 19, 20, 21, 22]. Much of the energy stored on the gate can therefore be recovered, and total gating loss can then be reduced to a small fraction of what can be achieved by hard switching.

4.2.1 A Basic Resonant Gate Drive

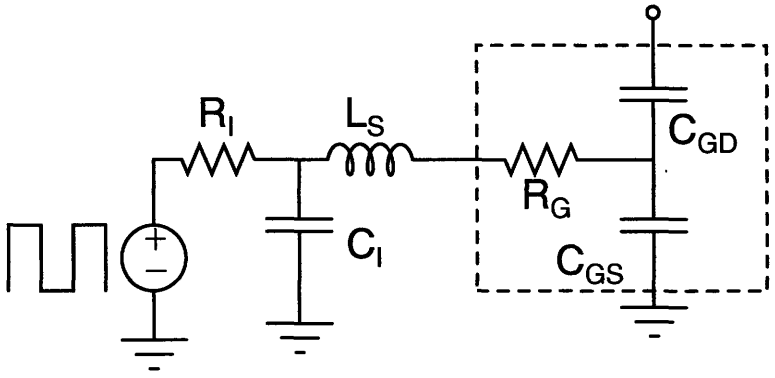
Figure 4.2(a) illustrates a simple resonant gate drive circuit with a minimum component count. With this series resonant circuit [3, 25, 19, 20, 21, 22], a sinusoidal gate voltage can be obtained by filtering a dc voltage with a LRC tank. Furthermore, by adding two resistors to this network to set the dc bias, this circuitry can now be designed to statically operate at a wide range of duty ratios. However, losses introduced by the resonating current passing through the channel resistance of the totem pole driver can quickly offset the advantages of resonant gating [3, 4], and therefore results in an unacceptable efficiency at HF.

4.2.2 Improved Resonant Gate Drive

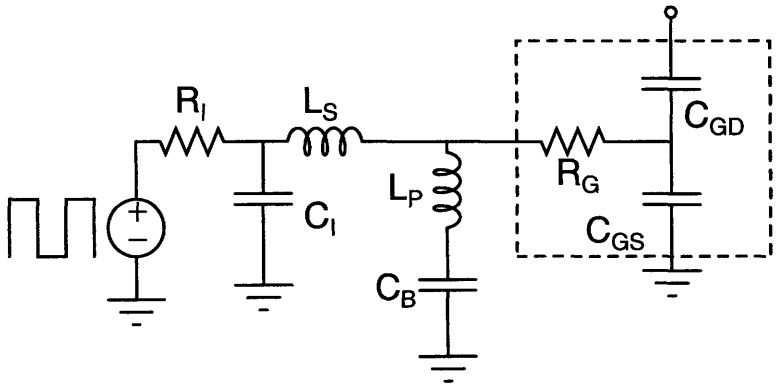
To address the substantial losses associated with the channel resistance of the totem pole driver (without compromising the amplitude of the gate voltage or the duty cycle), two potential approaches can be implemented.

The first approach entails reducing the total channel resistance R_{IN} of the totem pole driver. When the totem pole drivers are implemented via commercially designed CMOS inverter stages, the total channel resistance can be reduced via placing multiple inverters in parallel. However, this method comes at a price. While the inverter resistance is scaled down by a factor of $1/N$ by placing N inverters in parallel, the output capacitance of the inverter stages is now increased to $C_{OUT} * N$. If the series resonant circuit is tuned at resonance, the output capacitance C_{OUT} is being hard-switched at the operating frequency, energy charging and discharging this capacitance is lost. If the series resonant circuit is operating above resonance (tuned inductively), ZVS switching of the driver can be maintained, however, neither the input capacitance nor the turn-off overlap loss can be reduced. This tradeoff suggests that blindly adding an arbitrary number of inverters in hope to reduce the losses associated with resonating current via the channel resistance is not such a wise approach, and that there exists an optimal number of inverters that minimizes the total loss.

Another approach (to reduce the losses in R_{IN}) addresses this issue by adding an additional shunt branch, Figure 4.2(b) for reactive current to flow [3, 4]. The additional shunt branch comprised of a resonant inductor, L_P, and a blocking capacitor, C_B, which carry a portion of the resonating current, and therefore diminishes the losses associated with the on-state resistance of the inverter switches. However, note that the component value of the blocking capacitor C_B cannot be selected arbitrarily. While the impedance of the C_B must be low at the switching frequency compared to the rest of the network for it to be a blocking capacitor, it is not desirable for the value of C_B to be arbitrarily large because each time the gate drive circuit is enabled and disabled via the control circuitry (to be discussed in Chapter 5), C_B is hard-switched with a power dissipation of $P_{SHUNT} = C_B(V_{DD}/2)^2 f_{MOD}$ [4], where V_{DD} is the inverter rail voltage and f_{MOD} is the frequency at the converter is modulated to regulate the output.



(a) A Basic Resonant Gate Drive



(b) An Improved Resonant Gate Drive

Figure 4.2: **Two examples of resonant gate drivers. An additional shunt leg in Figure 4.2(b) can reduce the resonating current through the channel resistance R_I and improve efficiency.**

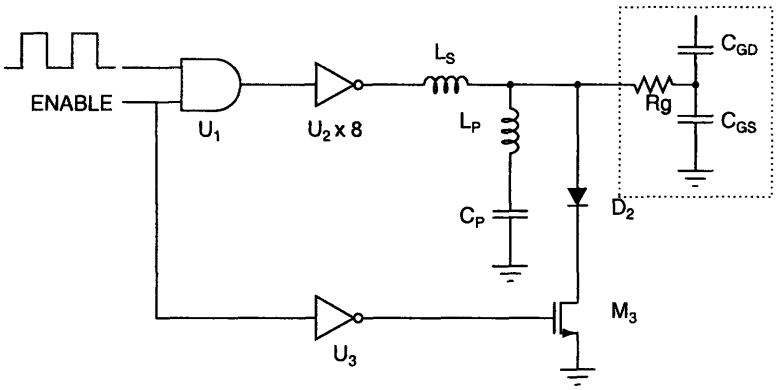


Figure 4.3: **Sinusoidal Resonant Gate Drive Circuit.**

4.2.2.1 Tuning the Gate Drive

Gate characteristics of switching devices are important to the design of a resonant gate drive. The gate characteristics (R_{GATE} and C_{ISS}) of the switching device $SPN1443$ are listed under Table 2.3.1. Figure 4.3 shows a schematic of the resonant driver circuit we have adopted. The drive topology is a variant of one described in [24], but utilizes a different biasing and tuning strategy to match the different gate characteristics and drive requirements in our system.

In [4], the design of a similar resonant gate driver, focusing on minimizing the drain to gate transfer function V_G/V_D to ensure a rapid device shut-down (while maintaining enough amplitude to fully enhance the device) is discussed. By setting the gate to drivers transfer function V_G/V_{IN} via L_S while resonating L_P with C_{ISS} at a frequency below the switching frequency, this tuning method may not result in the lowest gating loss when tested with,a MOSFET on its own or with a converter running under open-loop. However, a better overall efficiency is achieved under closed-loop operation when the device can rapidly turn off without sustained oscillations, preventing the converter spending a significant amount of time operating inefficiently under non-optimal conditions when modulating on and off.

After a pull-down network, similar to the one introduced in [3], is added to ensure that the main switching device cannot self-oscillate when a shutdown command is issued under modulation, minimizing V_G/V_D may no longer lead to the most efficient gate drive design overall. Adding the additional pull-down network does however have its disadvantage. When used in parallel with the control scheme implementation (to

be introduced in Chapter 5), the pull-down network does not allow the dc-bias to be set separately via additional biasing resistors. It will instead remain at about half of the inverter rail voltage, V_{DD}. This limitation of the pull-down network in turn places additional constraints on the switching device and/or the power stage. A device threshold voltage lower than $V_{DD}/2$ implies that a converter utilizing such a device must be able to operate efficiently at a duty cycle less than 0.5; whereas, a threshold voltage higher than $V_{DD}/2$ calls for a converter performing well at a duty cycle larger than 0.5. Furthermore, in order to fully enhance the device with a sinusoidal gate voltage with a pre-determined dc offset, a sharp turn-on transition of the device with respect of the gate voltage is also preferable for a better overall converter performance.

The tuning method applied to the resonant gate drive is similar to that described in [3], with slight changes due to different device and overall system characteristics. In this case, an optimal gate drive design cannot be achieved with the phase of a drain to gate transfer function close to 180°. Achieving such a phase angle will either incur too much gating loss or require a large L_S and a small L_P which will slow the gate drive startup (and deteriorates the overall system's performance). Fortunately, for this application, the drain-to-gate feedback is not crucial to help achieving a desired amplitude at the gate. A better overall efficiency is achieved with a drain-to-gate phase angle around 250°.

The shunt branch of L_P and C_P is inductive at the switching frequency (with C_P simply acting as a dc block). L_P is sized to partially cancel the gate admittance, leaving the parallel combination of L_P and the gate capacitive, but with higher impedance than the gate capacitance alone. L_P thus provides some of the reactive power needed to charge and discharge the gate. L_S serves multiple functions. First, it is resonant with the parallel combination of the L_P and C_{GATE} near the switching frequency such that there is significant voltage gain from the CMOS inverter bank to the gate at the switching frequency. Second, it provides a high impedance to harmonic voltages applied by the CMOS inverter, reducing inverter loss.

For the case of interest here, it has been found (through simulations and experimentations) that the gating loss is more significant in the case where the shunt inductor L_P is larger than the series inductor L_S than a gate drive design where the series inductor is slightly larger, similar to [3]. Figure 4.4 and 4.5 illustrate these two cases. For two converters with identical operating conditions (such as operating frequency, input and output voltage, and output power level), the gating loss (and the

overall efficiency) is better for a gate drive design when L_S is slightly larger than L_P (even though the drain efficiency of the converter may not be better). The frequency domain simulations provide some insights why one design is preferred over the other. At the switching frequency, the magnitude of V_{GATE}/V_{DRAIN} of the "better" gate drive design (where L_S is larger than L_P) is much smaller, diminishing the Miller effect (and therefore, the effective reverse transfer capacitance C_{GD}). As the value of L_S increases, the amplitude of V_{GATE} increases, with V_{GATE}/V_{IN} less inductive at the switching frequency, a condition that increases the power dissipated by the gate.

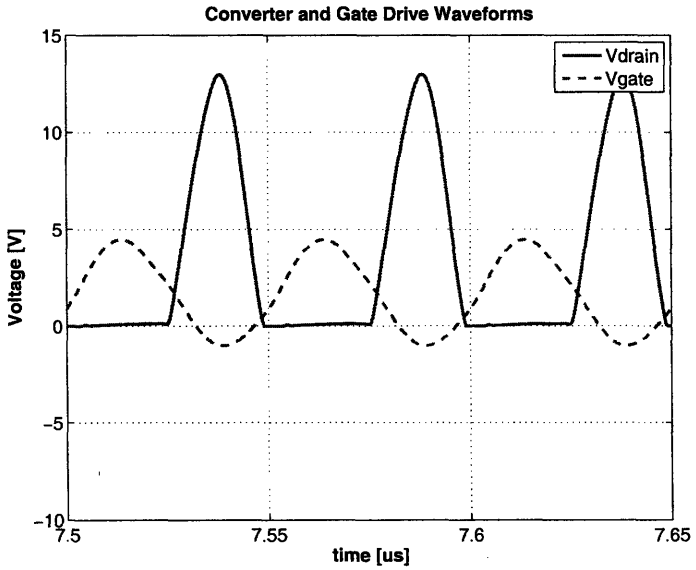
4.2.2.2 Implementation of a Resonant Gate Drive

Figure 4.3 shows a simplified schematic of the resonant driver circuit, implemented to drive the power stage discussed in Chapter 2. A more complete schematic with component values is included in Chapter 6.

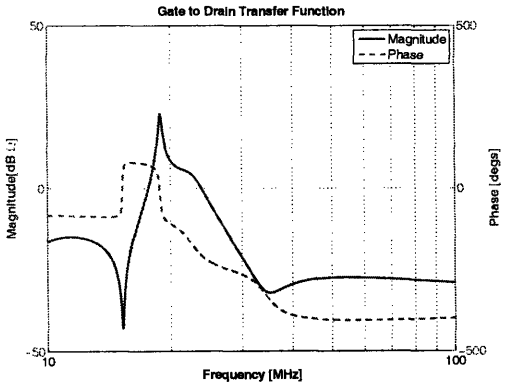
To provide on/off modulation capability, the CMOS inverter bank is driven by an oscillator signal that is gated by an enable input. The enable input provides on/off control. Moreover, an active pull-down network comprising a CMOS inverter, a MOSFET, and a diode helps provide rapid shutdown at turnoff.

A square-wave with the desired amplitude and frequency is generated via a commercial oscillator $LTC1799$ as the drive voltage for a bank of eight parallel Fairchild $NC7ZW04$ CMOS inverters. A ring oscillator implemented in [3, 4] is replaced by this commercial oscillator due to its difficulty in setting and maintaining a precise switching frequency with substantial temperature variations and its significantly loss. The number of CMOS inverters used is to ensure that each component maximum power dissipation limits are not exceed and to reduce the total channel resistance of the inverters. It was determined experimentally that eight inverters provide the best tradeoff between the losses associated with the source resistance and hard-switched inverter capacitance. A command signal (generated by the control scheme) provides the on/off modulation capability via a Fairchild $NC7SZ08$ AND Gate.

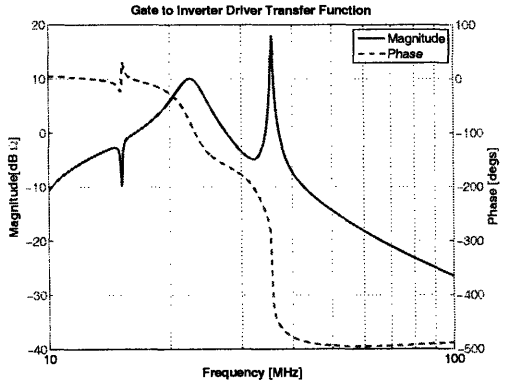
The experimental results including component values, gate drive power dissipation, start-up and shut-down transient will be presented along with closed-loop performance in Chapter 6.



(a) Drain and Gate Waveforms

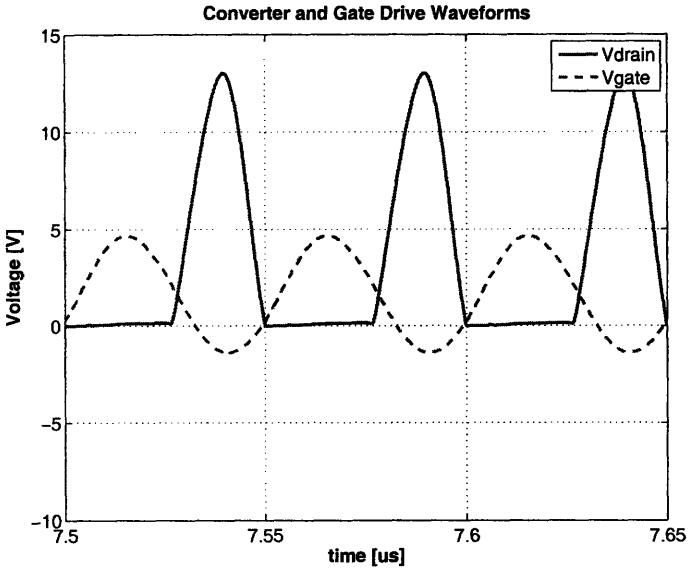


(b) Gate to Drain Transfer Function V_{GATE}/V_{DRAIN}

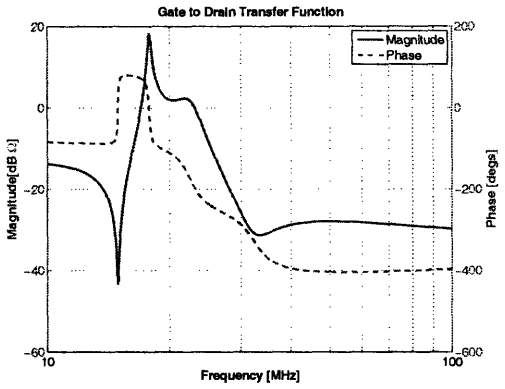


(c) Gate to Inverter Driver Transfer Function V_{GATE}/V_{INV}

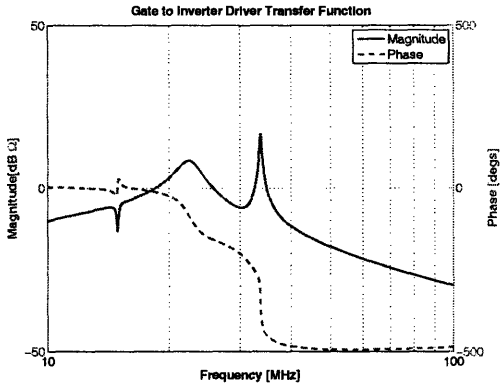
Figure 4.4: **A $3W$ converter design operating at $20MHz$ with gate drive component values of $L_P = 120n, L_S = 72n$. Magnitude and Phase of V_{GATE}/V_{INV} at $20MHz$: $5.91dB, -26.38°$. Magnitude and Phase of V_{GATE}/V_{DRAIN} at $20MHz$: $9.48dB, -109.33°$. Total gating loss is about $167mW$. See appendix A for component values and simulation files.**



(a) Drain and Gate Waveforms



(b) Gate to Drain Transfer Function V_{GATE}/V_{DRAIN}



(c) Gate to Inverter Driver Transfer Function V_{GATE}/V_{INV}

Figure 4.5: **A $3W$ converter design operating at $20MHz$ with gate drive component values of $L_P = 72n, L_S = 110n$. Magnitude and Phase of V_{GATE}/V_{INV} at $20MHz$: $3.25dB, --24.18°$. Magnitude and Phase of V_{GATE}/V_{DRAIN} at $20MHz$: $2.52dB, -110.76°$. Total gating loss is about $78mW$. See appendix A for component values and simulation files.**

4.3 Comparison with other Resonant Gate Drive Methods

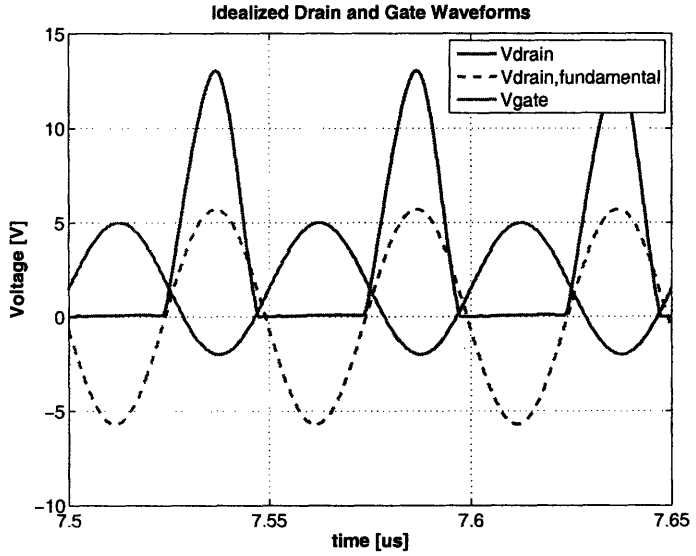
In addition to the gate drive method discussed in details in Section 4.2.2, there are other resonant gate drive designs that have proven their merits in HF and VHF operation regime. This section will explore two other resonant gate drive methods and discuss their advantages and disadvantages compared to the gate drive scheme pursued in this thesis.

4.3.1 A Simple Self Oscillating Gate Driver

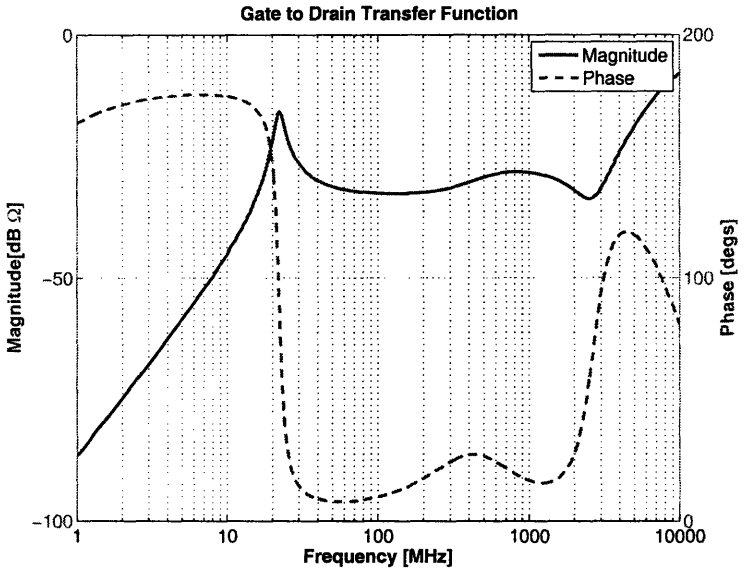
In [27], a resonant feedback network shown in Figure 4.7(a) is used to extract and phase shift the fundamental component of the drain voltage of a $100MHz$ Class E converter to generate a sinusoidal gating signal, which is capable of sustaining oscillation at the desired frequency. A self-oscillating phase shift and feedback network can be designed by first determining the phase angle between the fundamental component of the drain voltage and an idealized gate signal, then implementing a network, illustrated in Figure 4.6, to achieve such a phase at the operating frequency to attained sustained oscillation.

A similar self-oscillating resonant gate driver may be tailored to meet the drive requirement of the system studied in this thesis. Figure 4.6 illustrates how such a resonant gate driver may be designed.

The gating loss associated with this gate drive scheme operating at $20MHz$, driving a power stage discussed in Chapter 2 is about $120mW$, slightly higher than the resonant gate drive studied in Section 4.2.2. However, losses associated with an on/off and startup circuit required to start and stop this gating method (under on-off modulation) have not been included. Furthermore, this gating scheme implementation depends heavily on obtaining an accurate phase match between the transfer function V_{GATE}/V_{DRAIN} (which heavily depends on the value of L_{FB} and the phase of the gate drive voltage and the fundamental drain voltage. While this may not be so difficult in simulations via a parameter sweep, this may not be such a trivial task in practical implementations when inductors usually come in discrete values. The complexity(the number of components) and the difficulty associated with experimental implementa-



(a) Drain and Gate Waveforms



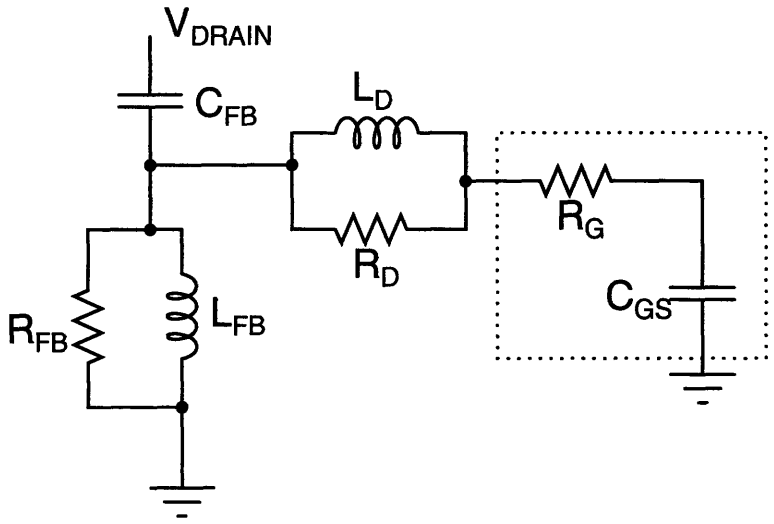
(b) Gate to Drain Transfer Function V_{GATE}/V_{DRAIN}

Figure 4.6: **A simulated $20MHz$ self-resonant gate drive may be designed by determining the phase angle between the fundamental component of the drain voltage and an idealized gate signal, 172° in this case, and adjusting L_{FB} until the phase of the drain to gate transfer function at the switching frequency is 172°. See [27] for tuning details. See appendix A for component values and simulation files.**

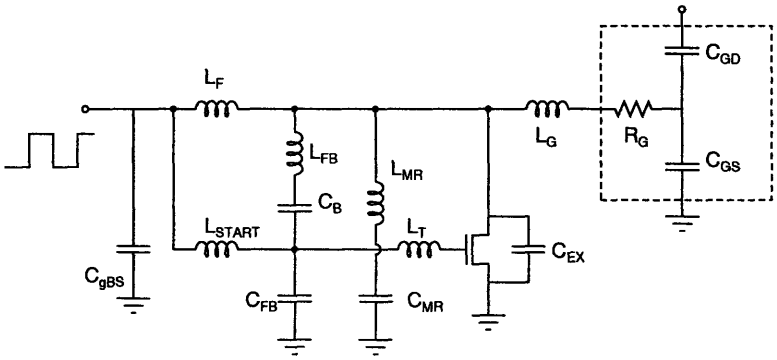
tion in addition to higher losses make this gate drive method less preferable for the application pursued in this thesis.

4.3.2 A Multi-Resonant Self-Oscillating Gate Driver

The multi-resonant self-oscillating gate driver, Figure 4.7(b) introduced in [24, 27] generates a trapezoidal drive voltage waveform, yielding an approximately constant current on the rising and falling edges of the gate voltage and thus minimizing the power dissipated in the gate resistance, given by $P_{GATE} = C_{ISS}^2 V_{GATE}^2 R_{GATE}(\frac{1}{t_r}+\frac{1}{t_f})f_s$ where V_{GATE} is the maximum voltage of the trapezoid, C_{ISS} is the input capacitance of the switching device, and t_r and t_f are the rise time and the fall time respectively of the drive waveform. While the theoretical gating loss achievable from this equation yields a lower gate power dissipation than that of a sinusoidal drive voltage, a practical implementation requires an additional startup circuitry and a phase-shift network (in addition to the multi-resonant network) [27, 24]. While the "overhead" losses associated with the additional circuitry may be tolerable for converters operating at output power level of tens of Watts to hundreds of Watts, it may become a significant portion of total loss for a $3W$ converter. The number of components required to implement this gate drive circuitry will not only introduce more loss mechanisms, but also deteriorates the power density of the power stage studied in this thesis. Furthermore, the multi-resonant self-oscillating gate drive requires an exact impedance characteristic at the second harmonic of the switching frequency, introducing even more tuning and complexity to such an implementation.



(a) A Simple Self-Oscillating Gate Driver



(b) A Multi-Resonant Self-Oscillating Gate Driver

Figure 4.7: **Two self-oscillating gating scheme. Figure 4.7(a) generates a sinusoidal gate waveform whereas a trapezoidal gate waveform can be obtained from Figure 4.7(b)**

Chapter 5

Control Architecture

BURST mode control architecture has proven its merits when utilized in combination with HF and VHF resonant converters [26, 7, 24, 17, 3]. This control method is compatible with constraints imposed by resonant gate drive discussed in Chapter 4 such as constant frequency and fixed duty ratio. In addition, by separating power stage from the control functions, this architecture allows regulation of the output across a wide load range and high light-load efficiency while enabling switching frequency in the HF and VHF regime. This chapter introduces a new on-off modulation control method, which enables fast transient response and efficient light load operation while providing controlled spectral characteristics of the input and output waveforms.

5.1 Background

One commonly employed control methods for resonant power conversion in frequency modulation [31, 12, 48, 49]. However, one major shortcoming of this strategy resides in its substantial impact on efficiency under closed-loop operation due to its tight coupling between the power stage and the control function. As the soft-switching characteristics is closely tied to the impedance of the overall system, any deviation away from this optimal impedance (caused by changes in operating frequency as in the case of frequency modulation) can results in exacerbated circulating current loss and V-I overlap switching loss. Furthermore, constraints imposed by resonant gate drives such as fixed duty ratio and constant frequency eliminates the usages of some other control methods including traditional PWM scheme unless significant gating loss is to be tolerated. Finally, achieving good efficiency across a wide load range and wide operating ranges is yet another limitation that frequency modulation and traditional PMW control technique does not overcome.

5.2 Burst Mode Control

Burst mode control architecture implementations have demonstrated their distinct advantages in resonant power conversion in the HF and VHF regimes [26, 7, 24, 17, 3]. The unregulated cells are designed to have high output impedance so that they can be treated as current sources that are enabled/disabled by an on-off command signal.

This control scheme addresses the major challenges faced by most conventional configurations. By separating the power stage from the control circuitry, burst mode control allows the power stage components sized at the switching frequency while the input/output filter components are sized at a relatively slower modulation frequency. Consequently, the inductor in the power stage remains small leading to tremendously improved transient performance. Furthermore, unlike traditional PWM control scheme where total power loss remains relatively constant throughout load range [7, 24, 17, 3], when the converter cell is disabled, it is (ideally) not incurring any additional losses. Its operation at one fixed (optimal) high-efficiency point where it is tuned to makes efficient operation over a very wide load range and operating range possible. Finally, as the converter cell is only run at fixed frequency and duty ratios, this control method is compatible with low-loss resonant gate drive approach discussed in Chapter 4.

A variety modulation strategies can be employed under this control architecture. One implementation is hysteretic control of the output voltage [26, 7, 24, 17, 3, 19, 20, 21, 22]. In hysteretic control, when the output voltage falls below a specified threshold, the converter is enabled and power is delivered to the load as the output voltage gradually increases. When the output voltage rises above a specified maximum threshold, the converter cell is disabled and the output voltage gradually decreases until the minimum threshold is reached and the cycle repeats. With hysteretic control, the input and output voltage ripples have components near the modulation frequency and its harmonics in addition to components near the high switching frequency [3, 24].

5.3 PWM On-off Control

In a PWM on-off control strategy, the major fundamental design concepts are the same as that of hysteretic on-off control. Switching of the converter is gated on and

off to control the average power delivered to the output. The frequency at which the converter is modulated on and off is much lower than the converter switching frequency. With fixed switching frequency operation, the control strategy is well-matched with a HF resonant converter tuned to be highly efficient at one switching frequency. Similar to that of hysteretic control, the power stage components are sized for the the very high switching frequency, while the converter input and output filters (e.g. capacitors) are sized for the lower modulation frequency.

While voltage hysteretic on-off control offers advantages such as a well-controlled voltage band, good efficiency at very light load, and unconditional stability. the input and output waveforms have variable frequency content (owing to the variable-frequency modulation) making this control method undesirable in some applications (such as communication systems), and increasing the difficulty of designing input and output filters.

To address the variable frequency components residing in the input/output waveforms, a new approach, in which the on-time of the converter is pulse-width modulated within a fixed modulation period, is utilized to implement the on-off control method. Unlike hysteretic on-off control, PWM on-off control operates a fixed modulation frequency, leading to well-defined frequency content at the converter input and output. On the other hand, efficiency tends to decline at extreme light loads, when the converter may operate for only a few switching cycles each modulation period. The characteristics of this control method are similar in many regards to conventional fixed-frequency PWM. However, instead of modulating the voltage applied to a filter, the power delivered to the output capacitor and load is modulated.

The basic scheme illustrated in Figure 5.1 is implemented with a conventional PWM chip whose PWM output is the enable signal of the power stage gate drive. The converter is modeled as a controlled current source feeding the output filter and load, and is represented with an averaged state-space model. A P-I controller provides stable operation across the entire converter operating range.

5.3.1 Implementation

The $UCC2813$ is a low-power Bi-CMOS PWM chip employed to implement the PWM on-off control scheme. An error amplifier internal to the chip with a reference voltage

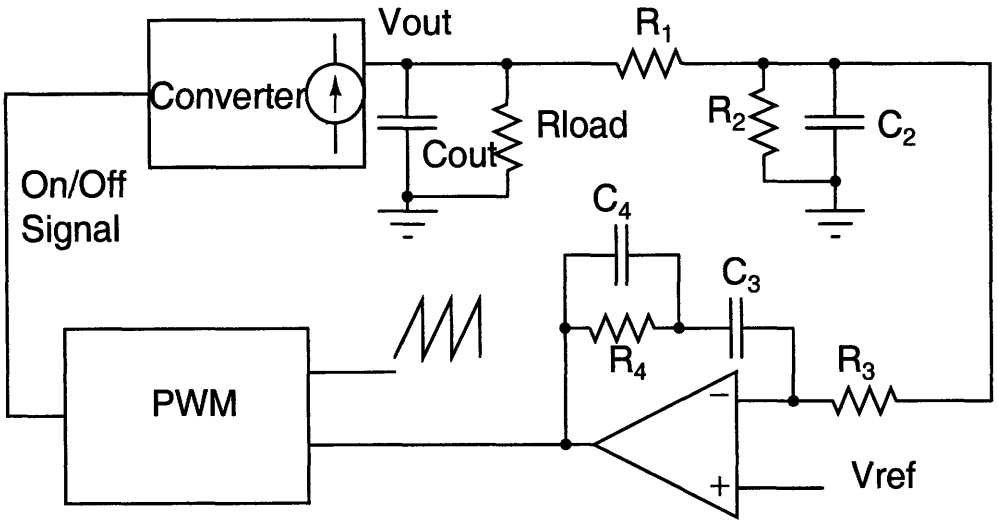


Figure 5.1: **PWM on-off control scheme**

of $2V$ is employed to implement a P-I controller. The P-I controller looks at the output voltage of the converter (possibly after a resistor divider) and integrates the error between the reference voltage and the output voltage to obtain an error voltage. The error voltage is then compared with the sawtooth voltage of the PWM chip to generate a command signal turning the converter cell on and off at a duty ratio such that the output remains regulated even as the load changes. The component values of the P-I controller are selected such that the controller is designed to be stable across the entire operating range, including at the lightest load condition where the phase margin is the smallest(in this case, at the lowest input voltage and highest output voltage).

The converter power stage can be modeled as a one-pole system with the converter approximated as a controlled current source feeding the output capacitor and load C_{OUT} and R_{LOAD}. In order to reach a P-I controller design that provides stable operation across the required operating ranges, the transfer function for the closed-loop system is obtained:

$$\frac{R_{LOAD}}{C_{OUT}S} * \frac{R_2}{R_2 + R_1} * K1 * \frac{1}{R_3}(\frac{1}{C_3S} + \frac{C_4SR_4}{C_4S + R_4}) \tag{5.1}$$

where R_{LOAD} is the load resistance of the converter obtained from P_{OUTPUT}/I^2_{OUT}, C_{OUT} is the output capacitance, K1 is a gain factor introduced by the PWM sawtooth

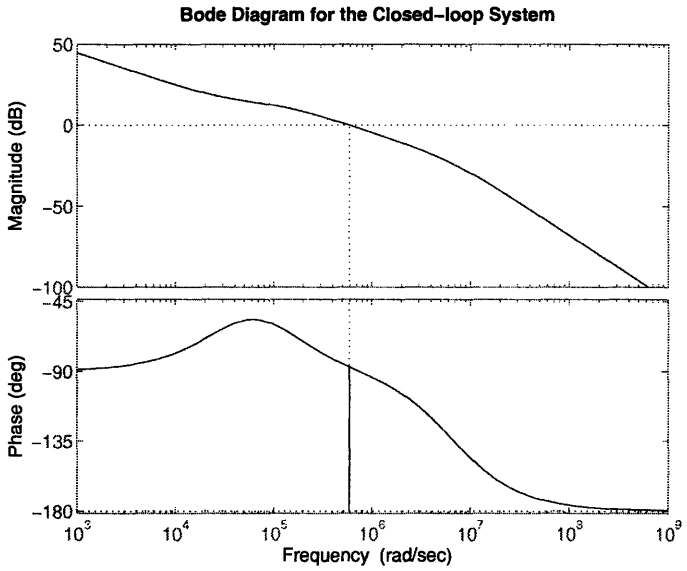


Figure 5.2: **Bode Plot for the Closed-loop System**

waveform which converts an error voltage to a duty ratio (in this case, $K1 = 2.5$), R_1, R_2, R_3, R_4, C_3 and C_4 are the components of the output voltage divider and the P-I controller in Figure 5.1. The bode plot for the system is shown in Figure 5.2

In reality, there are a few more components that were needed to implement a working PWM on-off controller and close the loop.

A high-frequency filter and a resistor divider comprised of $R1$, $R2$ and $C2$ is needed at the output voltage such that $C2$ together with $R1$ is providing low-pass filtering of the high-frequency content of the output voltage, and $R1$ and $R2$ are sized such that the voltage at the $V\_$ of the error amplifier is equal to the V_{REF} for a desired output voltage level.

A voltage doubler is needed at the input of the converter to power $UCC2813$ due to the start threshold voltage of under-voltage lockout of the chip. The start threshold voltage of the PWM chip start at $4.1V$, which makes the input voltage range (from $3.6V$ to $7.2V$) insufficient to power the chip. In addition, a linear regulator is added such that the maximum V_{CC} limit of $UCC2713$ is not exceed due to the voltage doubler.

The $UCC2813$ has an additional pin (pin 3, CS) for current-sensing which can be

used for internal leading-edge blanking of the current-sense input when needed. An additional amplifier, providing a voltage division, is needed such that the sawtooth voltage waveform observed at the oscillator pin (pin 4, RC) is present at the current-sense input with a scaled amplitude (to meet the maximum input limit of CS pin).

The detailed implementation with component values will be presented in Chapter 6, along with closed-loop experimental results.

5.3.2 Comparison with Hysteretic On-off Control

In addition to well-controlled frequency spectra of input/output voltage waveforms by PWM on-off modulation, this on-off control implementation is different from hysteretic burst-mode control in numerous other ways.

With PWM on-off modulation, output voltage ripple can be made arbitrarily small by adding additional output capacitance at the expense of achievable bandwidth. Because the converter can be modeled as a single pole dominated system, the attainable bandwidth is reduced as the phase margin increases. In addition, the noise in the system does not severely affect the ripple size.

On the other hand, in hysteretic control, the bandwidth of the controller is determined by the delay through the control circuitry. Furthermore, the ripple size cannot be made arbitrarily small by trading off the bandwidth. Rather, the ripple size is constant and is largely affected by noise for a given design. Furthermore, the output capacitance is sized at the nominal modulation frequency.

Chapter 6

Converter Prototype

PREVIOUS chapter have discussed major design concepts and tuning procedures of a power stage, gate drive and control architecture for a full dc-dc converter, targeting at the specifications listed in Table 1.1. This chapter presents the design and experimental validation of the pursued design approaches and strategies via a $20MHz$ quasi-resonant SEPIC converter utilizing sinusoidal resonant gate drive and PWM on-off control.

6.1 Prototype Layout

Board layout is an important stage of the design process, especially for converters operating in the HF and VHF regime, where undesirable parasitics can significantly distort the switching waveforms and deteriorate the overall performance of a converter. While parasitic capacitances can be absorbed (as a fraction of required component values) in most cases, additional inductances are more problematic. Picking devices with small packaging inductance is a major criterion in device selection, as described in Section 2.3.1. However, doing so can only partially addresses problematic effects due to lossy parasitics components. More importantly, component placement and board traces must be carefully thought out to prevent (or at least minimize) the presence of low-Q parasitic inductance in critical loops that introduce high-frequency ringing in the drain waveforms. For a resonant converter, in which the efficiency and performance is closely tied to the switching characteristics (such as ZVS and zero dv/dt) of the drain waveform, such high-frequency ringing can directly translate to decreased overall converter efficiency. Moreover, in some cases, it can lead to exceeding maximum device ratings (voltage and/or current) and device failures.

The converter was constructed on a 4-layer PCB, using the $EAGLE^{TM}$ Layout Editor.

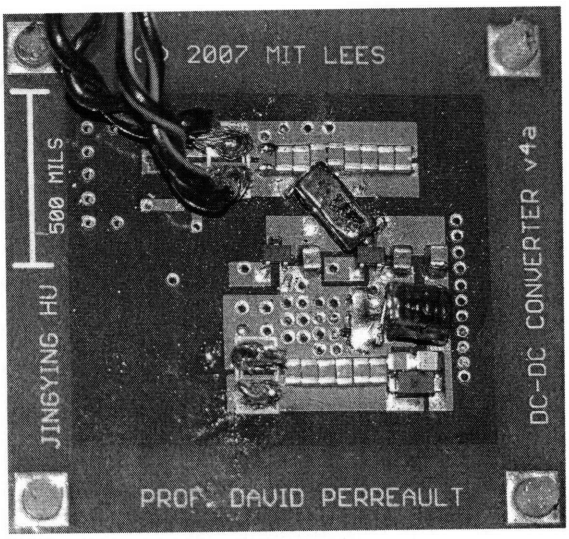


Figure 6.1: **Converter picture of a $20MHz$ quasi-resonant SEPIC converter prototype**

A photograph of the board is shown in Figure 6.1 with schematics and layout artwork are provided in Appendix B. Similar to [3, 18], the reason that prototyping was carried out with a 4-layer PCB is mainly due to concerns for minimizing parasitic inductances, as the parasitic inductances over 4 layer PCB (with the inner two layers used as ground planes) are much reduced over what could be achieved with a normal 2-layer FR4 board. In addition, components (especially those in critical loops where additional inductance can severely affect performance negatively) are placed as close to each other as possible, with the copper traces kept wide and short to minimize additional losses due to low-Q parasitic inductance.

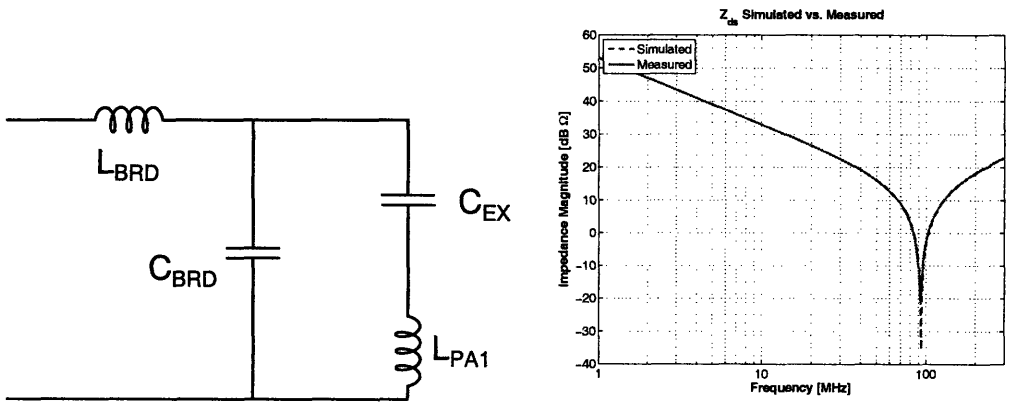
6.2 Impedance Characterization

From the tuning considerations described in Chapter 2, it is established that the impedance characteristics looking into the drain-to-source port of the switch determines the time-domain drain voltage waveform shapes. If certain desired impedance characteristics are achieved in the frequency domain at the drain node, the converter will operate with desirable switching waveforms (e.g. ZVS, zero dv/dt etc). This suggests that characterization of the drain-to-source impedance (including converter components and any additional parasitics) on a prototype board is an essential step

to reach at a working design with optimized performance, as parasitic components associated with the prototype board can affect the drain-to-source impedance significantly.

The following impedance measurements were obtained with an impedance analyzer, Agilent 4195A. The impedance measurement starts with characterizing the parasitic components of a measurement fixture, which is a SMA connector; placed across the drain and the source on the board. The parasitic components of the SMA fixture can be either compensated out via re-calibrating the impedance analyzer or be accounted as an additional component in any further measurements. The converter is then constructed with the drain node impedance characterized, one branch at a time. The impedance is characterized with appropriate bias voltage (e.g. at switch drain and output) to account for the influence of nonlinear device capacitances. Although the final drain impedance along with the parasitic components should be identical regardless of the order at which the converter branches are added, constructing the converter branches in a certain order (starting with the components closest to the drain-to-source node and expanding by adding the most adjacent components) may help locating where the parasitics are present and simplify the characterization process. Starting with a bare board calibrated with the SMA fixture on the impedance analyzer, the order at which individual branches are constructed to achieve the impedance characterization (Z_{DS}) at the drain-to-source node is summarized as follows, with schematics and impedance plots for each individual step shown in Figure 6.2 to Figure 6.10:

1. Add C_{EX1}, the first external capacitor in parallel with the switching devices, along with additional parasitic inductance L_{PA1} in that branch (Figure 6.2)
2. Add C_{EX2}, the second external capacitor in parallel with the switching devices, along with additional parasitic inductances L_{PA1} and L_{PA3} (Figure 6.3)
3. Add C_S, the matching network capacitor with additional parasitic inductance L_{PA4} (Figure 6.4)
4. Add L_{REC}, the rectifier inductor, with additional parasitic inductance absorbed in this component value (Figure 6.5)
5. Add C_{EX3}, the external capacitor to the rectifier diode, with additional parasitic inductance L_{PA5} (Figure 6.6)



(a) Circuit model of components along with parasitic for Z_{DS} characterization, Step 1

(b) Z_{DS} Matched Impedance, Step 1

Figure 6.2: **Characterization of Drain-to-source Impedance Z_{DS}, step 1.**

6. Add D1, the diode as it is biased to the expected operating voltage (at nominal output voltage $7V$) to achieve its capacitance under operation, along with additional parasitic inductance L_{PA6} (Figure 6.7)

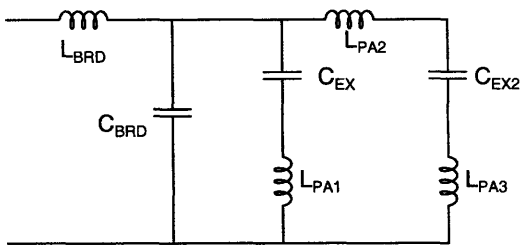
7. Add L_F, with additional board inductance absorbed in this component value (Figure 6.8)

8. Add M1,the first MOSFET as it is biased to the expected operating voltage (at $7.2V$) to achieve its capacitance under operation, along with parasitic inductance L_{PA6} and L_{PA7} (Figure 6.9)

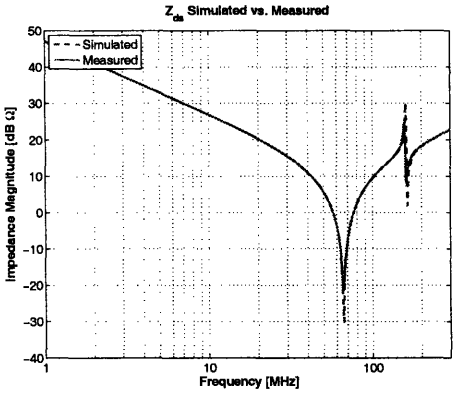
9. Repeat the previous step with M2, the second MOSFET, along with parasitic inductance L_{PA8} and L_{PA9} (Figure 6.10)

With an accurate converter model including all parasitic elements associated with the PCB, we are now in a position to optimize the converter implementation with the parasitics included. Fortunately, not much additional retuning is required in this case to achieve a design with desired switching behaviors. The schematics including all components along with board parasitic inductances of the power stage prototype is shown in Figure 6.11, along with the component values listed in Table 6.2.

However, among all extracted parasitic components, L_{PA4} is the most significant in terms of its affect on the drain voltage waveforms and performance in this design, even when it is extremely small (about $1.5nH$). The importance of this parasitic

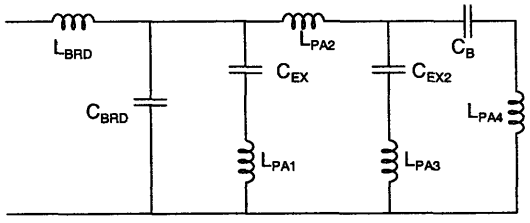


(a) Circuit model of components along with parasitic for Z_{DS} characterization, Step 2

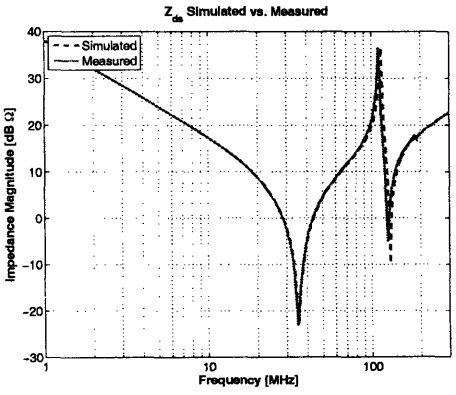


(b) Z_{DS} Matched Impedance, Step 2

Figure 6.3: **Characterization of Drain-to-source Impedance Z_{DS}, step 2.**

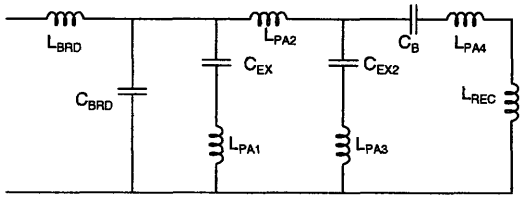


(a) Circuit model of components along with parasitic for Z_{DS} characterization, Step 3

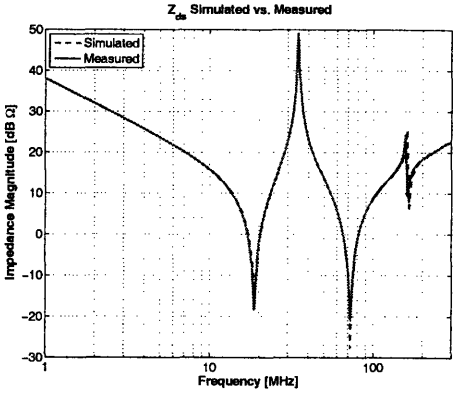


(b) Z_{DS} Matched Impedance, Step 3

Figure 6.4: **Characterization of Drain-to-source Impedance Z_{DS}, step 3.**

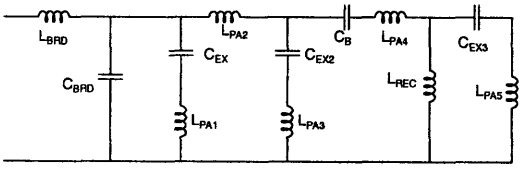


(a) Circuit model of components along with parasitic for Z_{DS} characterization, Step 4

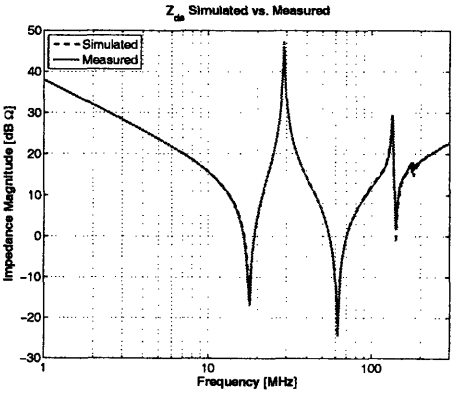


(b) Z_{DS} Matched Impedance, Step 4

Figure 6.5: **Characterization of Drain-to-source Impedance Z_{DS}, step 4.**

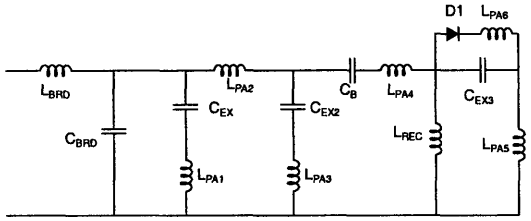


(a) Circuit model of components along with parasitic for Z_{DS} characterization, Step 5

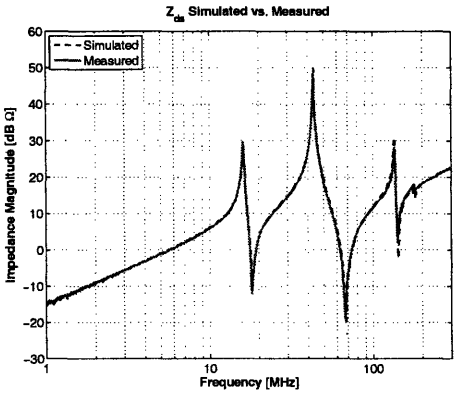


(b) Z_{DS} Matched Impedance, Step 5

Figure 6.6: **Characterization of Drain-to-source Impedance Z_{DS}, step 5.**

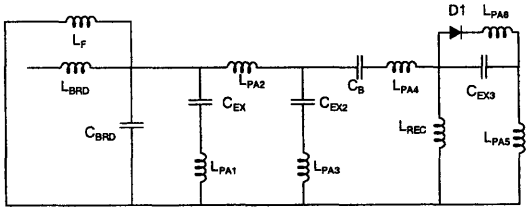


(a) Circuit model of components along with parasitic for Z_{DS} characterization, Step 6

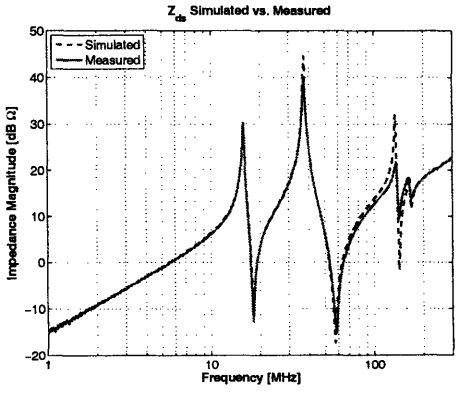


(b) Z_{DS} Matched Impedance, Step 6

Figure 6.7: **Characterization of Drain-to-source Impedance Z_{DS}, step 6. A $7V$ bias is applied to account for the influence of nonlinear parasitic capacitance of the diode**

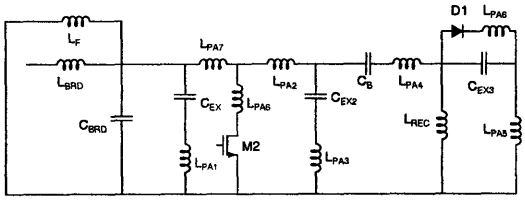


(a) Circuit model of components along with parasitic for Z_{DS} characterization, Step 7

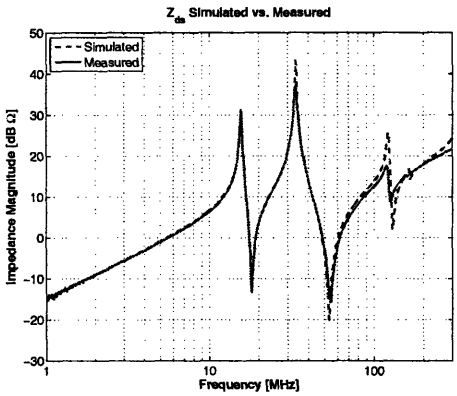


(b) Z_{DS} Matched Impedance, Step 7

Figure 6.8: **Characterization of Drain-to-source Impedance Z_{DS}, step 7.**

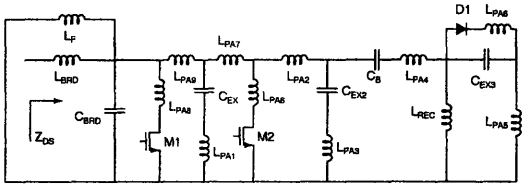


(a) Circuit model of components along with parasitic for Z_{DS} characterization, Step 8

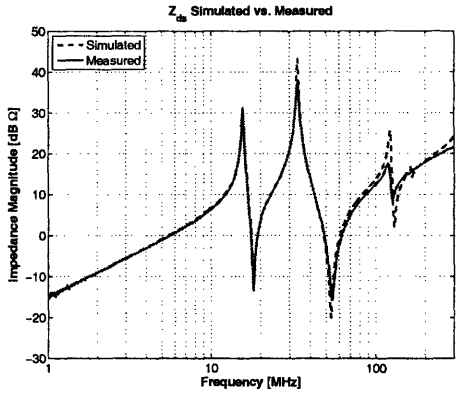


(b) Z_{DS} Matched Impedance, Step 8

Figure 6.9: **Characterization of Drain-to-source Impedance Z_{DS}, step 8. A $7.2V$ bias is applied to account for the influence of nonlinear parasitic capacitance of the MOSFET**



(a) Circuit model of components along with parasitic for Z_{DS} characterization, Step 9



(b) Z_{DS} Matched Impedance, Step 9

Figure 6.10: **Characterization of Drain-to-source Impedance Z_{DS}, step 9. A $7.2V$ bias is applied to account for the influence of nonlinear parasitic capacitance of the MOSFETs**

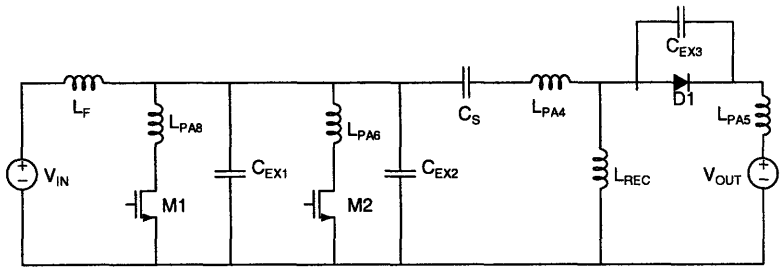


Figure 6.11: **A circuit model including parasitic inductances in addition to all converter components**

Component Name	Value
L_F	$22nH$
C_{EX1}	$390pF$
C_{EX2}	$390pF$
C_S	$1270pF$
L_{REC}	$43nH$
C_{EX3}	$100pF$
L_{PA4}	$1.5nH$
L_{PA5}	$1nH$
L_{PA6}	$0.7nH$
L_{PA8}	$0.7nH$
$D1$	$DFLS230L$
$M1$ and $M2$	$SPN1443$

Table 6.1: **Component values in addition to parasitic inductances for a converter prototype board characterized using the techniques outlined from Figure 6.2 to 6.10.**

inductance suggests that topologies such as the ones in Figure 2.44(a) and 2.44(b) where there is a series inductor present with C_S may be more appropriate if we are to further increase operating frequency in future designs (where parasitic effects on waveforms and performance become even more apparent).

6.3 Experimental Results

This section presents component values for a quasi-resonant SEPIC converter, a resonant gate drive and a PWM on-off control along with experimental waveforms and performance data.

6.3.1 Open Loop Performance

Gating loss is important, especially in the case of a low-power dc-dc converter. Before we can evaluate the open-loop performance of the converter, a low-loss sinusoidal resonant gate-drive, following the design considerations and implementation strategies described in Chapter 4, is constructed. A schematic of the gate drive circuit is provided in Figure 6.12 for reference with the component values listed in Table 6.3.1. Similar general layout considerations as those of the power stage are applied to the gate drive, with L_S, C_B and L_P as the critical loop where the parasitic inductance should be minimized.

With a working gate drive, the open-loop performance of the converter is be readily obtained. Converter steady state waveforms are presented in Figure 6.13, which shows the measured drain voltages across the entire input voltage range at the nominal output voltage and the measured drain voltage with corresponding gate and rectifier voltage at $V_{IN} = 3.6V$ and nominal output voltage. From the experimental waveforms, the topology indeed provides good zero voltage switching characteristics. However, a degree of turn-off delay due to device capacitance C_{GD} can be observed in the gate voltage waveform; observed as a short flattening of the gate voltage before it goes below the threshold. As the device is still carrying current during this time period and the drain voltage is rising, this delay results in overlap switching loss of the device. Open-loop efficiency measurements were obtained with a bank of zener diodes connected in parallel to maintain a constant output voltage. Figure 6.15

Component	Value	Package	Part No.	Manufacturer
$U1$	Oscillator	SOT-23	LTC1799	Linear Technology
$U2$	AND Gate	SOT-23	NC7SZ08	Fairchild
$U3x4$	CMOS Inverter	SC70	NC7WZ04	Fairchild
$U4$	Linear Regulator	SOT-23	TPS76933	Texas Instruments
C_1	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_2	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_{O4}	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_{O3}	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_{O2}	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_O	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_{O1}	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_{IN}	$4.7\mu F$	6032-28	TPSC475K035R0600	AVX
	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
R_1	$4.7k\Omega$	0603	ERJ-3GEYJ472V	Panasonic
L_S	$110nH$	0603	0603CS-R11X	Coilcraft
L_P	$72nH$	0603	0603CS-72NX	Coilcraft
C_P	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
$D2$	20V, 100mA	SSSMINI2	MA27D27	Panasonic
$M3$	25V, 680mA	SOT-23	FDV303N	Fairchild

Table 6.2: **Component values and part numbers for gate drive circuit**

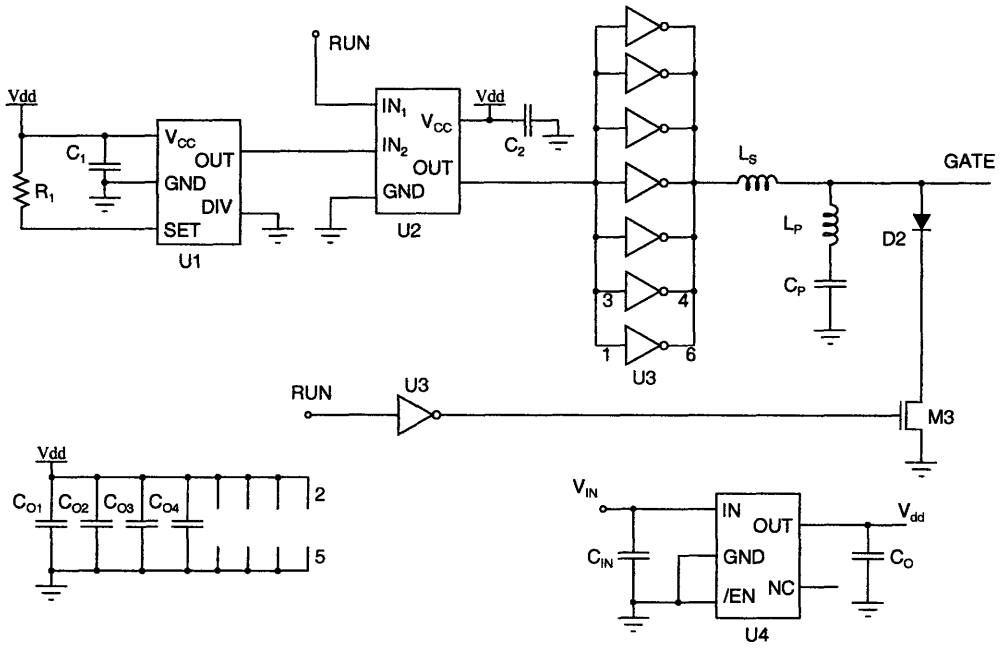


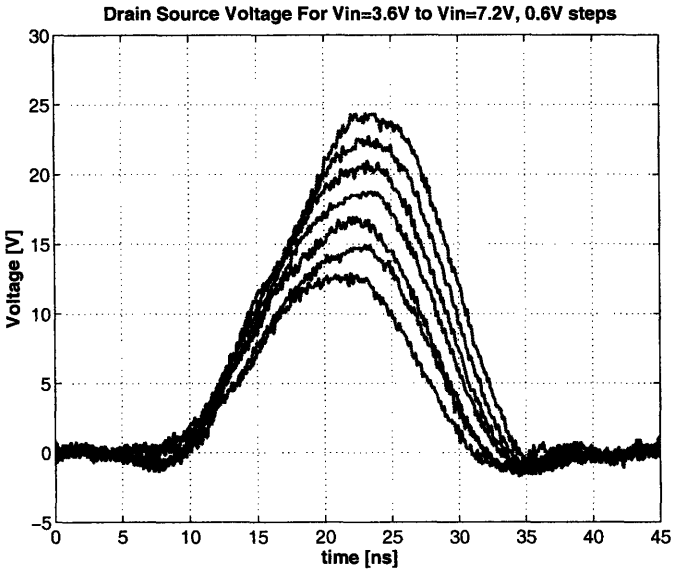
Figure 6.12: **Complete gate drive schematic.**

shows the output power and efficiency measurement at the nominal output voltage (7V) across the entire input range. Figure 6.14 shows the open-loop efficiency measurements with the losses from the gate driver included. The converter maintains good efficiency across the entire operating range (with V_{IN} ranging from $3.6V$ to $7.2V$ and V_{OUT} ranging from $3V$ to $9V$), with efficiency greater than 80% across the entire input voltage range at the nominal output voltage. The measured efficiency clearly indicates the merits of HF resonant power conversion together with resonant gate drive scheme across a wide operating range for a low-power application.

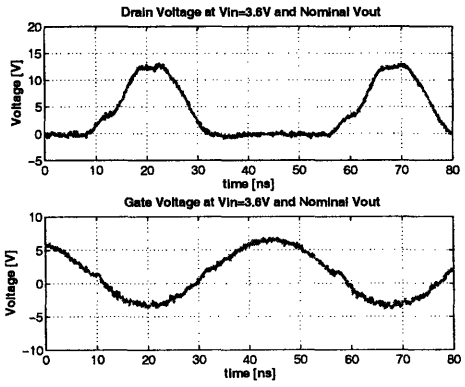
6.3.2 Closed Loop Performance

The closed-loop performance is demonstrated via a PWM on-off controller implementing the design strategies discussed in Chapter 5. A schematic of the controller is provided in Figure 6.16 for reference with the component values listed in Table 6.3.2.

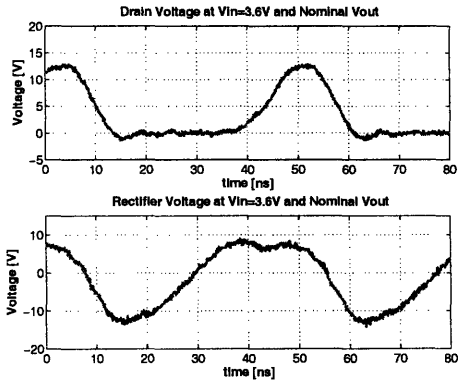
Figure 6.17 illustrates the case where the converter is operating under on-off modulation with a load of 1.7Ω at an input voltage of $3.6V$ and an output voltage of $4.4V$. The modulation frequency at which is the converter is turned on and off is 170 kHz.



(a) Drain Waveforms



(b) Drain and Gate Voltage



(c) Drain and Rectifier Voltage

Figure 6.13: **The measured converter waveforms. Figure 6.13(a) shows the measured drain voltages across the entire input voltage range at the nominal output voltage. Figure 6.13(b) and 6.13(c) illustrates the measured drain voltage with corresponding gate and rectifier voltage at $V_{IN} = 3.6V$ and nominal output voltage.**

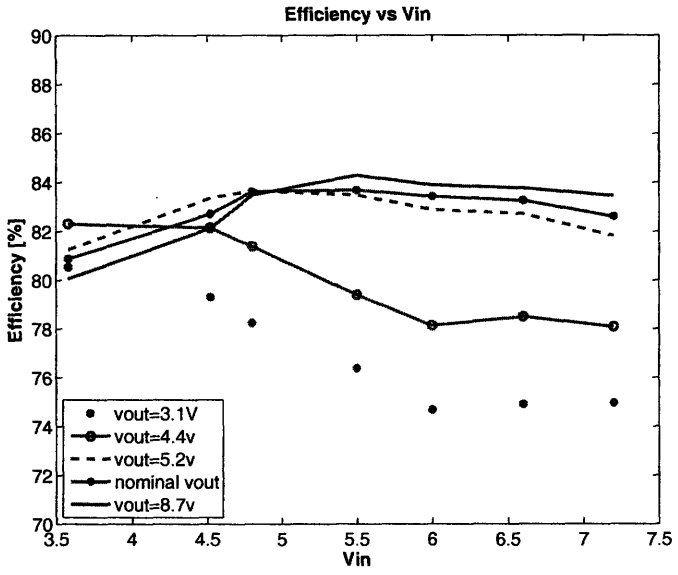


Figure 6.14: **Open-loop efficiency measurements across the entire operating range**

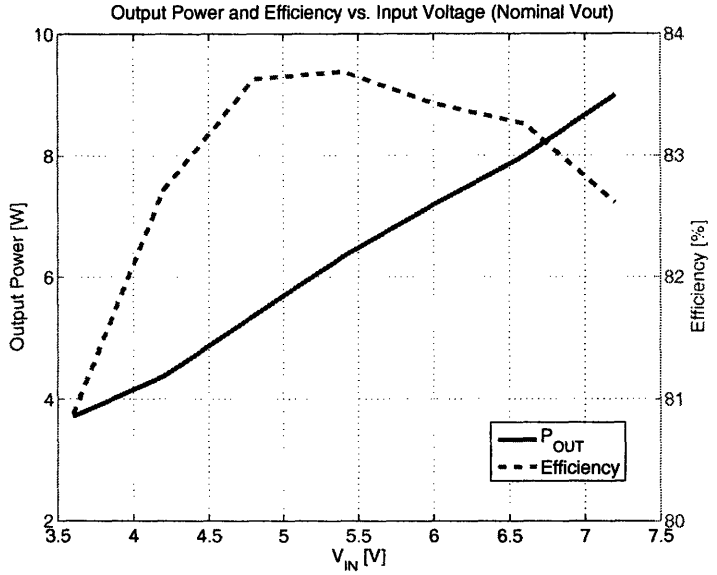


Figure 6.15: **Output power and efficiency measurements across the entire input voltage range at the nominal output voltage**

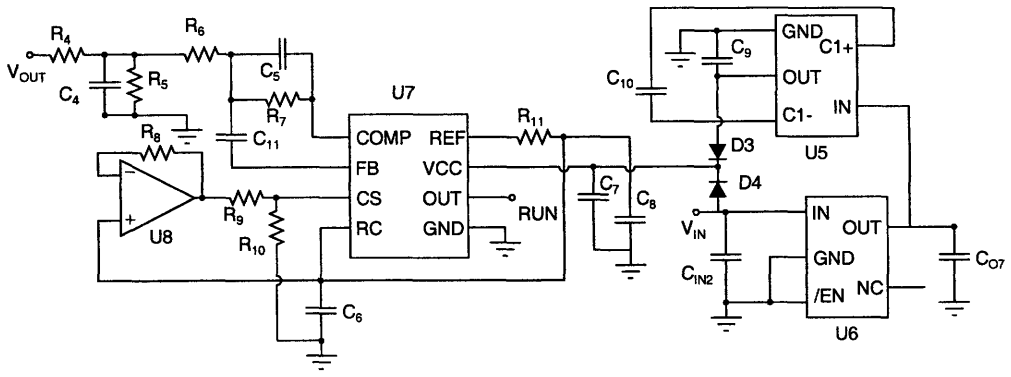


Figure 6.16: **Complete control schematic.**

Component	Value	Package	Part No.	Manufacturer
$U5$	Voltage Doubler	SOT-23	MAX1683	Maxim
$U7$	PWM chip	SO-8	UCC2813	Texas Instruments
$U8$	High Speed Amplifier	SO-8	MAX9003	Maxim
$U6$	Linear Regulator	SOT-23	TPS76925	Texas Instruments
C_{O7}	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_9	$3.3\mu F$	0603	TPCL335K010R5000	AVX
C_{10}	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_{IN2}	$4.7\mu F$	6032-28	TPSC475K035R0600	AVX
	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_4	$5pF$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_5	$1nF$	0603	LD03ZC102KAB2A	AVX
C_{11}	$5pF$	0603	ECJ-2VC1H050C	Panasonic
C_6	$100pF$	0603	ECJ-2VC1H101J	Panasonic
C_7	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_8	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
R_4	$22k\Omega$	0603	ERJ-3GEYJ223V	Panasonic
R_5	$8.2k\Omega$	0603	ERJ-3GEYJ822V	Panasonic
R_6	$10k\Omega$	0603	ERJ-3GEYJ103V	Panasonic
R_7	$30k\Omega$	0603	ERJ-3GEYJ303V	Panasonic
R_8	100Ω	0603	ERJ-3GEYJ101V	Panasonic
R_9	$30k\Omega$	0603	ERJ-3GEYJ303V	Panasonic
R_{10}	$30k\Omega$	0603	ERJ-3GEYJ203V	Panasonic
R_{11}	$56k\Omega$	0603	ERJ-3GEYJ563V	Panasonic
$D4$, $D3$	20V, 100mA	SSSMINI2	MA27D27	Panasonic

Table 6.3: **Component values and part numbers for controller circuit**

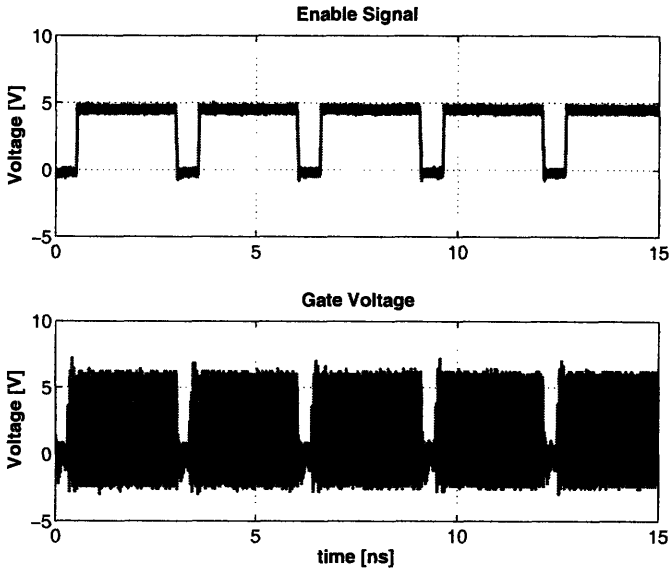
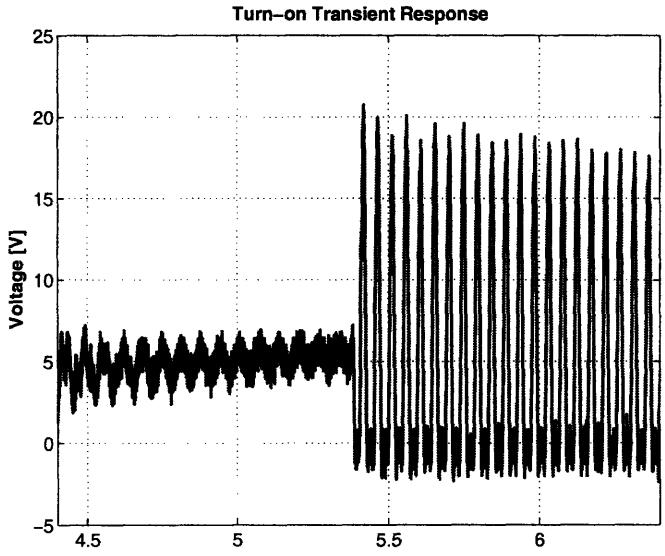


Figure 6.17: **Command signal and gate voltage for a converter operating under modulation at 170kHz**

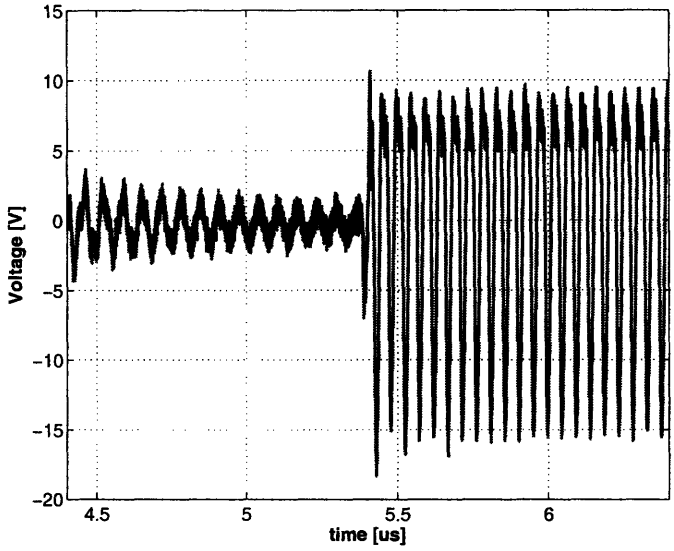
When on-off control method is utilized in combination with small-valued resonant inductors (such as L_F and L_{REC} in the power stage), the converter can turn on and off rapidly. Fast startup and shutdown comes with major performance advantages. Under burst mode control, fast startup and shutdown directly translates to better closed-loop efficiency for a given modulation frequency. During startup and shutdown transitions, the converter is not operating under its most-efficient steady state conditions. The less time a converter has to operate with additional losses associated with transition times, the better the overall efficiency may be achieved. Furthermore, the achievable bandwidth is closely tied to the transient response as well. The highest achievable modulation frequency is largely determined by the startup and shutdown transition time of the converter to ensure the converter is operating mostly under steady state condition when being modulated. In conventional dc-dc converters, the total required output capacitance is determined by the allowed voltage ripple and the desired transient performance. It is often the latter condition that determines the minimum capacitance, calling for a larger capacitance than demanded by output ripple requirements alone. However, the resonant SEPIC converter, with its inherently fast transient response due to small valued inductors, does not have this problem. The output capacitor is sized solely based on the desired on/off modulation frequency and output ripple, not by transient response limitations. Higher modulation frequency results in smaller output capacitance, which leads to a smaller overall converter size,

which is also desirable where converter miniaturization is important, such as the application being pursued in this thesis. For a given modulation frequency, if a smaller output ripple is desired, the output capacitance can be increased, however, it is done at the expense of the bandwidth of the controller.

Figure 6.18 and 6.19 shows the corresponding voltage waveforms for the converter at turn on and turn off at $V_{IN} = 5.4V$ and nominal output voltage. Figure 6.20 also shows the efficiency under closed loop operation across the entire input and output voltage ranges for the rated 3W output power. The minor differences in efficiency under open-loop and closed-loop conditions indicate that the controller indeed consumes very little power when the converter is turned off, and that modulation on and off to regulate power does not greatly impact efficiency.

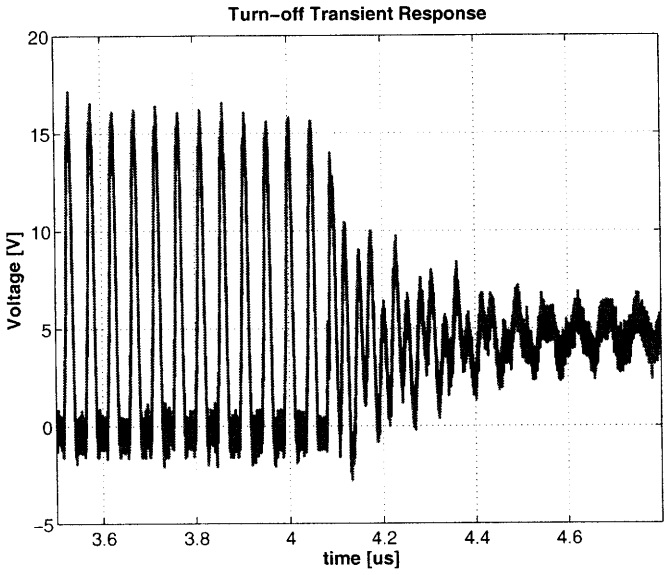


(a) Startup Drain Voltage

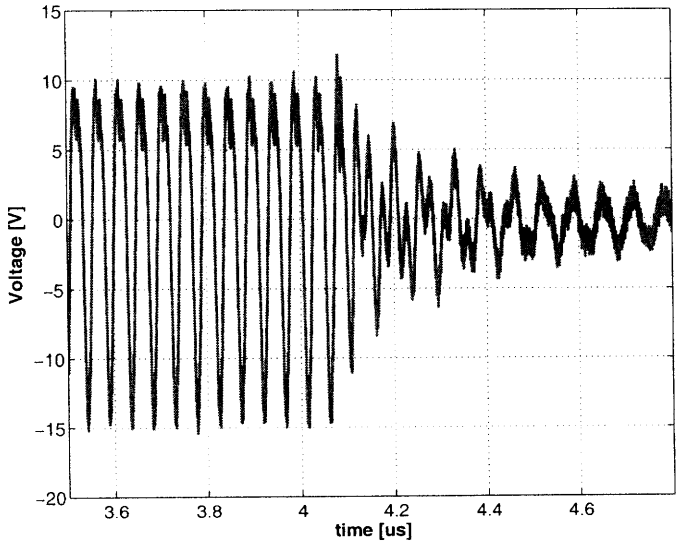


(b) Startup Rectifier Voltage

Figure 6.18: **Waveforms illustrating converter startup transient at $V_{IN} = 5.4V$ and nominal output voltage**



(a) Shutdown Drain Voltage



(b) Shutdown Rectifier Voltage

Figure 6.19: **Waveforms illustrating converter shutdown transient at $V_{IN} = 5.4V$ and nominal output voltage**

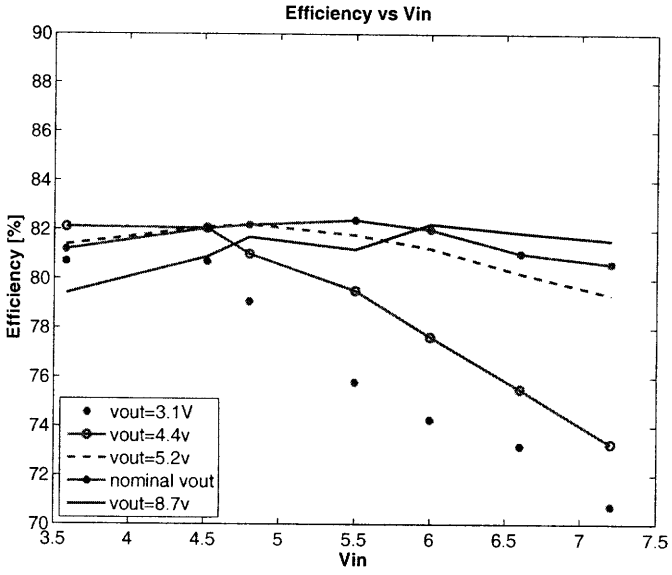


Figure 6.20: **Closed-loop efficiency measurements across the entire operating range**

Chapter 7

Conclusion

THIS thesis explores resonant power conversion design strategies suitable for a dc-dc converter operating over a wide range, utilizing design techniques such as HF operation, resonant gating and on-off control modulation. A prototype implementation provides good efficiencies across the entire operating range while maintaining a small size. The prototype converter was constructed with off the shelf vertical power MOSFETs; future developments such as utilizing custom designed MOSFETs and better magnetics design will significantly improve the performance to the next level.

7.1 Thesis Summary

Chapter 1 provides an overview of challenges associated with design of miniaturized and high bandwidth power converters using conventional techniques, especially when wide operating ranges (including input voltages and output voltages) and good efficiencies are also required. Traditional resonant converters are able to sidestep some of the challenges faced by conventional hard-switched converters, yet achieving good efficiencies across wide operating ranges is still an issue. A high frequency (HF) resonant converter utilizing resonant gate drive scheme and burst mode control is proposed to can address these thorny issues. The proposed design uses soft-switching (to significantly reduce switching loss), utilizes resonant gating (to recover a part of the energy delivered to the gate, employs small-valued air-core inductors (to eliminate core loss and improve transient response) and separates energy storage and control functions via on-off control(to achieve a wide operating range and attain minimal control circuitry power dissipation).

Chapter 2 introduces a quasi-resonant SEPIC converter topology that can meet the requirements of maintaining good efficiency and small size while operating across a

wide range of input and output voltages, and providing up-and-down voltage conversion. The topology is explored through discussions of each of the three major subsystems, namely a resonant rectifier, a matching network and an inverter. The tuning procedures are described in the context of an implementation of a $3W$ converter operating at input voltages from $3.6 - 7.2V$ and output voltages from $3 - 9V$.

Chapter 3 briefly describes the opportunities and challenges in inductor designs via a comparison study of commercial off-the-shelf air-core inductors, custom designed air-core inductors and planar spiral inductors.

Chapter 4 details the challenges and considerations in gate drive designs for low-power applications, such as the one being pursued in this thesis. The procedure tuning for a sinusoidal gating scheme is described, and the performance of such a gate drive is compared with other resonant gate drive implementations.

Chapter 5 introduces a PWM on-off control scheme compatible with the constraints imposed by resonant gating method, including constant frequency and fixed duty ratio operation. By separating the energy storage and control functions, the control scheme enables fixed-switching frequency operation and allows a converter to switch exclusively at its optimal frequency (for which the power stage is tuned); passive energy storage components of the power stage can now be sized for a much faster switching frequency whereas the input/output capacitors are sized according to ripple requirements at a slower modulation frequency.

Chapter 6 presents a practical implementation of the converter topology, gate driver, and control method discussed in the previous chapters. The $3W$ prototype converter switching at a frequency of $20MHz$ provides good efficiency across the entire operating ranges while maintaining a small size, thus meeting the two key requirements of its intended application. Open-loop and closed-loop performance are presented illustrating the merits of HF resonant power conversion when used in combination with resonant gating and burst-mode control scheme.

7.2 Thesis Conclusions

This thesis presents a resonant SEPIC converter suitable for extremely high frequency operation and for operating across a wide input and output voltage range. The

topology addresses several shortcomings of conventional resonant SEPIC converters through the development of topology, gate drive method and control scheme. Detailed tuning procedures to achieve the good performance, are described in detail for the topology. The merits of these design methods are verified via a 20 MHz prototype with an input voltage range from 3.6V to 7.2V, an output voltage range of 3V to 9V and a rated output power of 3W. The converter utilizes a low-loss sinusoidal gate drive and an PWM on-off control method modulating at fixed frequency, provides both fast transient response and good control over spectral characteristics of the input and output voltage. As the prototype converter has demonstrated, it is possible for resonant SEPIC converters to achieve a wide operating range, a small size and excellent transient response while maintaining good efficiency. It is hoped that these techniques will contribute to future development of low-power converters operating over wide ranges and extreme high frequencies to meet the increasing demands of modern portable electronics.

7.3 Future Work

Further research and development in this field may yield converters achieving small volume along with better efficiencies, since there exists strong opportunities for further improvement with the HF quasi-resonant SEPIC converter studied in this thesis.

Improvements in area such as device design and magnetic design will help achieve higher converter efficiency across the entire operating range. While the prototype discussed in Chapter 6 utilizes commercial off-the-shelf semiconductor devices which are not built to provide the optimal tradeoffs between conduction loss, circulating current loss and gating loss, a more careful study of these design tradeoffs will lead to better devices with desired characteristics to minimize the total energy dissipation associated with the device. In addition, losses associated with the resonant inductors employed in the converter prototype can be tremendously reduced with further research. While the commercial off-the-shelf air core inductors (employed in the prototype) and the custom designed planar spiral inductors (studied in Chapter 3) yield inductor Qs in the range of 50 to 70 at $20MHz$, major improvements in Qs, which directly translate to better efficiencies across the entire operating ranges, may be made through appropriate applications of RF core materials.

Additional capabilities including integrated gate drive/control circuitry and multiple

output capabilities may also be introduced to further cut down loss, reduce converter size and to provide the converter with even more flexibility. By integrating gate drive and control circuitry on the same process on which the switching device will be designed, the converter power density can be significantly improved. Moreover, losses due to quiescent currents associated with discrete parts (required to implement the gate drive and control circuitry in the prototype shown in Chapter 6) may be eliminated. Finally, with the burst mode control techniques demonstrated via the converter prototype, multiple output capabilities can be introduced to the converter implementation with very minimal additional circuitry, which can further reduce the overall system size when several outputs need to be served via a single input supply.

In summary, techniques in HF or VHF resonant power conversion addressed in this thesis have proven their merits in terms of converter size, efficiency and transient performance in a low-power application where a wide range of input voltages and output voltages along with up-and-down voltage conversion capability is required. Future research developments in areas such as custom device designs, magnetics design, improved gate drive and control circuitry (with the possibility of being integrated on the same process as the custom device), and multiple output handling capability will lead to substantial performance improvement and introduce even more versatility to HF or VHF power conversion.

Appendix A

SPICE DECKS AND COMPONENT VALUES

This appendix includes spice files and/or values for the simulations used in each chapter as a demonstration and for the converter designs.

A.1 Chapter 2 Data

A.1.1 Conventional and Multi-Resonant SEPIC data:

```
************************
*Conventional SEPIC***
**********************

.lib "..\PIPP.lib"
.LIB "..\SIMOS.LIB"
.LIB "..\RECT.LIB"
.LIB "..\MOSNL2PSPICE.LIB"
.LIB "..\diodenl2.LIB"



.OPTIONS ABSTOL=5nA
+          GMIN=10p
+          ITL1=6000
+          ITL2=4000
+          ITL4=500
+          RELTOL=0.003
+          VNTOL=0.04mV
```

```
.OPTION STEPGMIN


.OPTIONS
+ NOPAGE
+ NOBIAS
+ NOECHO
+ NOMOD
+ NUMDGT=8
.WIDTH OUT=132

.PARAM:
+ICLF=0;
+ICLMR=0;
+ICCMR=0;
+ICCF=0;
+ICCP=0;
+ICCS=0;
+ICLS=0;
+ICCFT=0;

.PARAM:
+TR={1/(100*FT)}              ;RISE TIME
+PWIDTH={(DUTY/(FT))-TR-TR}   ;PULSE WIDTH
+FS=20MEG
+FT=20MEG
+FMR=20MEG
+VIN=3.6
+DUTY=0.75
+ VOUT=7
+ CS=0.5u
+ COUT=100U
+ CIN=100U
+ VDON=0.375
+ L1=380n
+ RDSON=0.001
+ QI=70
+ QC=3K
+ PI=3.141592

VGATE GATE 0 PULSE(-25 25 0 {TR} {TR} {PWIDTH} {1/FT})
```

```
VIN IN 0 {VIN}

XLCHOKE1 IN DRAIN LQS
+ PARAMS:
+ L= {L1}
+ QL={QI}
+ FQ={FS}
+ IC={ICLF}

XCS DRAIN REC CQS
+ PARAMS:
+ C= {CS}
+ QC={QC}
+ FQ={FS}
+ IC={ICCMR}

XSIMOS GATE DRAIN 0 MOSFETNLC
+ PARAMS:
+ RDSON=0.059*1.6
+ RG=1.17
+ CGS=600P
+ RCOUT=0.118
+ RSHUNT=12MEG
+ CJO=235.24P
+ VJ=0.5476556
+ M=0.448313

XLCHOKE2 REC 0 LQS
+ PARAMS:
+ L= {L1}
+ QL={QI}
+ FQ={FS}
+ IC={ICLF}

DIDEAL REC REC2  IDEAL
.MODEL IDEAL D(N=0.001)
*FORWARD VOLTAGE DROP MODEL
VDON   REC2  OUT    {VDON}
```

```
VOUT OUT 0 {VOUT}


**************************
***MEASUREMENT CIRCUITS ***
**************************

.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                               ;COMPONENT OF THE MEASURMENT
                               ;CIRCUITS TWO DECADES BEFORE THE
                               ;SWITCHING FREQUENCY

*-----INPUT POWER MEASUREMENT
EPI PIN01 0  VALUE={V(IN)*(-I(VIN))}
LPI PIN01 PIN {LORC(FS)}
CPI PIN   0  {LORC(FS)}
RPI PIN   0  1

*-----OUTPUT POWER MEASUREMENT
EPO PO01 0    VALUE={v(OUT)*I(Vout)}
LPO PO01 POUT {LORC(FS)}
CPO POUT 0    {LORC(FS)}
RPO POUT 0    1  ;OUTPUT POWER


*-----EFFICIENCY
EEFF   EFF   0    VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))}

.tran 5000p 5U 0.01u uic
*.ac dec 1k 100k 10g
.PROBE



**************************
***MR SEPIC***************
**************************

.lib "..\PIPP.lib"
.LIB "..\SIMOS.LIB"
.LIB "..\RECT.LIB"
.LIB "..\MOSNL2PSPICE.LIB"
```

```
.LIB "..\diodenl2.LIB"


.OPTIONS ABSTOL=5nA
+          GMIN=10p
+          ITL1=6000
+          ITL2=4000
+          ITL4=500
+          RELTOL=0.003
+          VNTOL=0.04mV
.OPTION STEPGMIN


.OPTIONS
+ NOPAGE
+ NOBIAS
+ NOECHO
+ NOMOD
+ NUMDGT=8
.WIDTH OUT=132


.PARAM:
+ICLF=0;
+ICLMR=0;
+ICCMR=0;
+ICCF=0;
+ICCP=0;
+ICCS=0;
+ICLS=0;
+ICCFT=0;

.PARAM:
+TR={1/(100*FT)}
+PWIDTH={(DUTY/(FT))-TR-TR}

VGATE GATE 0 PULSE(-25 25 0 {TR} {TR} {PWIDTH} {1/FT})

.PARAM:
+FS=20MEG
+FT=20MEG
```

```
+FMR=20MEG
+VIN=3.6
+DUTY=0.7
+ VOUT=7
+ CS=0.5u
+ Cex=0.4n
+ Cex2=1.4n
+ LS=40n
+ COUT=4.7u
+ CIN=4.7u
+ L1=180n
+ QI=70
+ QC=3K
+ PI=3.141592


VIN IN 0 {VIN}

XLCHOKE1 IN DRAIN LQS
+ PARAMS:
+ L= {L1}
+ QL={QI}
+ FQ={FS}
+ IC={ICLF}

XLS DRAIN DRAINM LQS
+ PARAMS:
+ L= {LS}
+ QL={QI}
+ FQ={FS}
+ IC={ICLF}

XCS DRAINM REC CQS
+ PARAMS:
+ C= {CS}
+ QC={QC}
+ FQ={FS}
+ IC={ICCMR}

switch drain source gate 0 sw1
.model sw1 vswitch(ron=1m roff=1meg von=2)
```

```
vdsource source 0 0

DIDEAL SOURCE DRAIN DIODE
.model DIODE D(N=.0001)

XCEX DRAIN 0 CQS
+ PARAMS:
+ C= {Cex}
+ QC={QC}
+ FQ={FS}
+ IC={ICCMR}

XLCHOKE2 REC 0 LQS
+ PARAMS:
+ L= {L1}
+ QL={QI}
+ FQ={FS}
+ IC={ICLF}



XDFLS220L REC OUT SS36NL
+ PARAMS:
+ LDS=3.7668p
+ VDON=0.375
+ CJO=252P
+ VJ=0.62638
+ M=0.42102
+ FS=20MEG

XCEX2 REC OUT CQS
+ PARAMS:
+ C= {Cex2}
+ QC={QC}
+ FQ={FS}
+ IC={ICCMR}

VOUT OUT 0 {VOUT}

**************************
***MEASUREMENT CIRCUITS ***
```

```
**************************

.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                               ;COMPONENT OF THE MEASURMENT
                               ;CIRCUITS TWO DECADES BEFORE THE
                               ;SWITCHING FREQUENCY

*-----INPUT POWER MEASUREMENT
EPI PIN01 0  VALUE={V(IN)*(-I(VIN))}
LPI PIN01 PIN {LORC(FS)}
CPI PIN   0  {LORC(FS)}
RPI PIN   0  1

*-----OUTPUT POWER MEASUREMENT
*EPO PO01 0    VALUE={v(M05)*I(VDUCS)}
EPO PO01 0    VALUE={v(OUT)*I(Vout)}
LPO PO01 POUT {LORC(FS)}
CPO POUT 0    {LORC(FS)}
RPO POUT 0    1  ;OUTPUT POWER


*-----EFFICIENCY
EEFF   EFF   0    VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))}

.tran 500p 5.5U 3.5u 500p uic
.PROBE
```

A.1.2 Rectifier data:

```
*********************
***RECTIFIER TUNING***
***********************

.LIB "..\PIPP.LIB"
.LIB "..\diodenl1.LIB"

.OPTIONS ABSTOL=1nA
+          GMIN=10p
+          ITL1=6000
```

```
+          ITL2=4000
+          ITL4=500
+          RELTOL=0.002
+          VNTOL=0.01mV
.OPTION STEPGMIN

.OPTIONS
+ NOPAGE
+ NOBIAS
+ NOECHO
+ NOMOD
+ NUMDGT=8
.WIDTH OUT=132

.PARAM
+ PI=3.14159265
+FS=20MEG
+IIN=0.7
+ VOUT=7
+ QLR=70
+ QC=3K
+ C2=153p
+ LR=118n

*********************************
*tuning rectifier with Zo and Fc
*********************************

*+ Z0=18.7
*+ fc=28.35Meg
*+ LR={Z0/(2*pi*fc)}
*+ C2={1/(z0*2*pi*fc)}

*LR: 90n
*C2: 125p, 127p, 130p, 135p, 140p, 150p, 160p
*LR: 60n
*CR: 1100p, 1050p, 1000p, 950p, 900p, 860p, 700p

*inductive vs capacitive
*LR: 70n
*C2: 260p, 270p, 290p, 325p 350p
```

```
*C2: 925p, 825p, 700p, 600p, 500p

*two diodes
*LR=70n
*C2: 180p, 190p, 200p, 215p, 225p, 235p, 250p, 275p, 300p


IT1  0 R00 SIN(0  {IIN} {FS} 0 0)


VDUREC R00 R01 0

vdlr r01 r01x 0

XLR  0 R01x LQS
+ PARAMS:
+ L={LR}
+ QL={QLR}
+ FQ={FS}
+ IC=0

XC  R01 R02 CQS
+ PARAMS:
+ C= {C2}
+ QC={QC}
+ FQ={FS}
+ IC=0

XSS36 R01 R02 SS36NL
+ PARAMS:
+ LDS=3.7668p
+ VDON=0.375
+ CJO=252P
+ VJ=0.62638
+ M=0.42102
+ FS=20MEG

VOUT  R02 0 {VOUT}

*-----PARAMETERS FOR THE BANDPASS FILTER
.PARAM
```

```
+ QBP=100
.FUNC  CBPQ(FS,QBP) {1/(2*PI*FS*QBP)}
.FUNC  LBPQ(FS,QBP) {QBP/(2*PI*FS)}


*-----FUNAMDENTAL OF THE RECT. VOLTAGE
EBPRV  BPRV1  0      VALUE={V(R01)}
LBPRV  BPRV1  BPRV2  {LBPQ(FS,QBP)}
CBPRV  BPRV2  BPRV3  {CBPQ(FS,QBP)}
RBPRV  BPRV3  0      1

*-----FUNDAMENTAL OF THE RECT. CURRENT
EBPRI  BPRI1  0      VALUE={I(VDUREC)}
LBPRI  BPRI1  BPRI2  {LBPQ(FS,QBP)}
CBPRI  BPRI2  BPRI3  {CBPQ(FS,QBP)}
RBPRI  BPRI3  0      1


****************************
*** MEASURMENT CIRCUITS  ***
****************************
*-----FUNCTION USED BY THE MEASUREMNT CIRCUITS

.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                               ;COMPONENT OF THE MEASURMENT
                               ;CIRCUITS TWO DECADES BEFORE THE
                               ;SWITCHING FREQUENCY

*-----OUTPUT POWER MEASUREMENT
EPO PO01 0 VALUE={v(R02)*I(VOUT)}
LPO PO01 POUT {LORC(FS)}
CPO POUT 0    {LORC(FS)}
RPO POUT 0    1  ;OUTPUT POWER

*-----AVERAGE OUTPUT CURRENT
EAVIO  AVIO1 0     VALUE={I(VOUT)}
LAVIO  AVIO1 AVIO  {LORC(FS)}
CAVIO  AVIO  0     {LORC(FS)}
RAVIO  AVIO  0     1   ;AVERAGE OUTPUT CURRENT

*INPUT POWER MEASUREMENT
```

```
EPI PI01 0 VALUE={V(r00)*I(VDUREC)}
LPI PI01 PIN {LORC(FS)}
CPI PIN 0   {LORC(FS)}
RPI PIN 0   1    ;INPUT POWER

*EFFICIENCY MEASUREMENT
EEF EFF 0 VALUE={IF(V(PIN)<=0.01,0,V(POUT)/V(PIN))}
REF EFF 0 1

.TRAN 0.50N 15U 13u 0.50N UIC
.PROBE
```

A.1.3 Inverter data:

```
****************************
*******TUNED INVERTER*******
****************************

.lib "..\PIPP.lib"
.LIB "..\SIMOS.LIB"
.LIB "..\RECT.LIB"
.LIB "..\MOSNL2.LIB"
.LIB "..\DIODENL2.LIB"

.OPTIONS ABSTOL=5nA
+          GMIN=10p
+          ITL1=6000
+          ITL2=4000
+          ITL4=500
+          RELTOL=0.003
+          VNTOL=0.04mV
.OPTION STEPGMIN

.OPTIONS
+ NOPAGE
+ NOBIAS
+ NOECHO
+ NOMOD
```

```
+ NUMDGT=8
.WIDTH OUT=132

.PARAM:
+ICLF=0;
+ICLMR=0;
+ICCMR=0;
+ICCF=0;
+ICCP=0;
+ICCS=0;
+ICLS=0;
+ICCFT=0;

.param
+PI=3.1415926

*IACT 0 N07 AC 1
VDUSMOS N01 N07 0


switch n07 source gate 0 sw1
.model sw1 vswitch(ron=1m roff=1meg von=2)
vdsource source 0 0

vgate gate 0 pulse(0 5 0 {TR} {TR} {PWIDTH} {1/FT})


.PARAM:
+TR={1/(100*FT)}
+PWIDTH={(DUTY/(FT))-TR-TR}

.PARAM:
+FS=20MEG
+FT=20MEG
+FMR=20MEG;
+VIN=3.6
+DUTY=0.65
+QI=70
+QC=3K
+RDC=10M
```

```
.PARAM:
+CFNOM=712.5p
+CFEXTRA=0.001p
+CF={CFNOM+CFEXTRA}
+K=1
+CP=0.001p
+CS=720p
+LS=70n
+RLOAD=17.14
+LF= 21n

VDULF  N01 N02 0

XLF    n02 n03 LQS
+ PARAMS:
+ L= {LF}
+ QL={QI}
+ FQ={FS}

+ IC={ICLF}

VIN    N03 0   {VIN}


VDUCFEX N01 N04 0

XCFEXTRA N04 0 CQS
+ PARAMS:
+ C= {CF}
+ QC={QC}
+ FQ={FS}
+ IC={ICCMR}

VDUZMR NT N01 0

VDUZL  NT  M01 0

VDUCP M01 M02

XCP  M02 0 CQS
+ PARAMS:
```

```
+ C= {CP}
+ QC={QC}
+ FQ={FS}
+ IC={ICCP}

VDUCS M01 M03

XCS  M03 M05 CQS
+ PARAMS:
+ C= {CS}
+ QC={QC}
+ FQ={FS}
+ IC={ICCS}


XLS M05 M05X LQS
+ PARAMS:
+ L= {LS}
+ QL={QI}
+ FQ={FS}
+ IC={ICLS}

VDULS M05X 0 0

RLOAD M05 M06 {RLOAD}
VDRLOAD M06 0 0

.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                               ;COMPONENT OF THE MEASURMENT
                               ;CIRCUITS TWO DECADES BEFORE THE
                               ;SWITCHING FREQUENCY

*-----INPUT POWER MEASUREMENT
EPI PIN01 0  VALUE={V(n03)*(-I(VIN))}
LPI PIN01 PIN {LORC(FS)}
CPI PIN   0  {LORC(FS)}
RPI PIN   0  1

*-----OUTPUT POWER MEASUREMENT
*EPO PO01 0    VALUE={v(M05)*I(VDUCS)}
EPO PO01 0    VALUE={v(m05)*I(Vdrload)}
```

```
LPO PO01 POUT {LORC(FS)}
CPO POUT 0    {LORC(FS)}
RPO POUT 0    1   ;OUTPUT POWER


*-----EFFICIENCY
EEFF   EFF   0    VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))}

.tran 500p 10U 2.5u 500p uic
*.ac dec 1k 100k 10g
.PROBE



*************************
*LOW PASS MATCHING NETWORK
*************************
.lib "..\PIPP.lib"
.LIB "..\SIMOS.LIB"
.LIB "..\RECT.LIB"
.LIB "..\MOSNL2.LIB"
.LIB "..\DIODENL2.LIB"

.PARAM:
+ICLF=0;
+ICLMR=0;
+ICCMR=0;
+ICCF=0;
+ICCP=0;
+ICCS=0;
+ICLS=0;
+ICCFT=0;


.param
+PI=3.1415926

*VACT NT 0 {Vin} AC 1
VDUSMOS N01 N07 0


switch n07 source gate 0 sw1
```

```
.model sw1 vswitch(ron=1m roff=1meg von=2)
vdsource source 0 0

vgate gate 0 pulse(0 5 0 {TR} {TR} {PWIDTH} {1/FT})


.PARAM:
+TR={1/(100*FT)}
+PWIDTH={(DUTY/(FT))-TR-TR}

.PARAM:
+FS=20MEG
+FT=20MEG
+FMR=20MEG
+VIN=3.6
+DUTY=0.65
+QI=70
+QC=3K
+RDC=10M

.PARAM:
+CFNOM=712.5p
+CFEXTRA=0.001p
+CF={CFNOM+CFEXTRA}
+LFEXTRA= -27.5n
+K=1
+CP=0.001p
+CS=481p
+LS=46.8n
+RLOAD=17.14
+LF= 21n;

VDULF  N01 N02 0

XLF    n02 n03 LQS
+ PARAMS:
+ L= {LF}
+ QL={QI}
+ FQ={FS}
+ IC={ICLF}
```

```
VIN    N03 0   {VIN}

VDUCFEX N01 N04 0

XCFEXTRA N04 0 CQS
+ PARAMS:
+ C= {CF}
+ QC={QC}
+ FQ={FS}
+ IC={ICCMR}

VDUZMR NT N01 0

VDUZL  NT  M01 0

VDUCP M01 M02

XCP  M02 0 CQS
+ PARAMS:
+ C= {CP}
+ QC={QC}
+ FQ={FS}
+ IC={ICCP}

XLS  M03 M05 LQS
+ PARAMS:
+ L= {LS}
+ QL={QI}
+ FQ={FS}
+ IC={ICLS}
VDULS M01 M03 0

XCS M05 M05X CQS
+ PARAMS:
+ C= {CS}
+ QC={QC}
+ FQ={FS}
+ IC={ICCS}
VDUCS M05X 0 0
```

```
RLOAD M05 M06 {RLOAD}
VDRLOAD M06 0 0

.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                               ;COMPONENT OF THE MEASURMENT
                               ;CIRCUITS TWO DECADES BEFORE THE
                               ;SWITCHING FREQUENCY

*-----INPUT POWER MEASUREMENT
EPI PIN01 0  VALUE={V(n03)*(-I(VIN))}
LPI PIN01 PIN {LORC(FS)}
CPI PIN   0  {LORC(FS)}
RPI PIN   0  1

*-----OUTPUT POWER MEASUREMENT
*EPO PO01 0    VALUE={v(M05)*I(VDUCS)}
EPO PO01 0    VALUE={v(m05)*I(Vdrload)}
LPO PO01 POUT {LORC(FS)}
CPO POUT 0    {LORC(FS)}
RPO POUT 0    1  ;OUTPUT POWER


*-----EFFICIENCY
EEFF   EFF   0    VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))}

.tran 500p 3U 2.5u 500p uic
*.ac dec 1k 100k 10g
.PROBE


********************
*Low Pass MN Retuned*
**********************
.lib "..\PIPP.lib"
.LIB "..\SIMOS.LIB"
.LIB "..\RECT.LIB"
.LIB "..\MOSNL2.LIB"
.LIB "..\DIODENL2.LIB"


.PARAM:
+ICLF=0;
```

```
+ICLMR=0;
+ICCMR=0;
+ICCF=0;
+ICCP=0;
+ICCS=0;
+ICLS=0;
+ICCFT=0;

.param
+PI=3.1415926


VDUSMOS N01 N07 0


switch n07 source gate 0 sw1
.model sw1 vswitch(ron=1m roff=1meg von=2)
vdsource source 0 0

vgate gate 0 pulse(0 5 0 {TR} {TR} {PWIDTH} {1/FT})

.PARAM:
+TR={1/(100*FT)}
+PWIDTH={(DUTY/(FT))-TR-TR}


.PARAM:
+FS=20MEG
+FT=20MEG
+FMR=20MEG
+VIN=3.6
+DUTY=0.65
+QI=70
+QC=3K
+RDC=10M


.PARAM:
+CFNOM=1275p
+CFEXTRA=0.001p
+CF={CFNOM+CFEXTRA}
```

```
+LFEXTRA= -27.5n

+K=1
+CP=0.001p

+CS=481p
+LS=46.8n
+RLOAD=17.14
+LF= 21n

VDULF  N01 N02 0

XLF    n02 n03 LQS
+ PARAMS:
+ L= {LF}
+ QL={QI}
+ FQ={FS}
+ IC={ICLF}

VIN    N03 0   {VIN}


VDUCFEX N01 N04 0

XCFEXTRA N04 0 CQS
+ PARAMS:
+ C= {CF}
+ QC={QC}
+ FQ={FS}
+ IC={ICCMR}

VDUZMR NT N01 0

VDUZL  NT  M01 0

VDUCP M01 M02

XCP  M02 0 CQS
+ PARAMS:
+ C= {CP}
+ QC={QC}
```

```
+ FQ={FS}
+ IC={ICCP}

XLS  M03 M05 LQS
+ PARAMS:
+ L= {LS}
+ QL={QI}
+ FQ={FS}
+ IC={ICLS}
VDULS M01 M03 0

XCS M05 M05X CQS
+ PARAMS:
+ C= {CS}
+ QC={QC}
+ FQ={FS}
+ IC={ICCS}

VDUCS M05X 0 0

RLOAD M05 M06 {RLOAD}
VDRLOAD M06 0 0

.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                               ;COMPONENT OF THE MEASURMENT
                               ;CIRCUITS TWO DECADES BEFORE THE
                               ;SWITCHING FREQUENCY

*-----INPUT POWER MEASUREMENT
EPI PIN01 0  VALUE={V(n03)*(-I(VIN))}
LPI PIN01 PIN {LORC(FS)}
CPI PIN   0  {LORC(FS)}
RPI PIN   0  1

*-----OUTPUT POWER MEASUREMENT
EPO PO01 0    VALUE={v(m05)*I(Vdrload)}
LPO PO01 POUT {LORC(FS)}
CPO POUT 0    {LORC(FS)}
RPO POUT 0    1  ;OUTPUT POWER
```

```
*-----EFFICIENCY
EEFF   EFF   0    VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))}

.tran 500p 5U 4.5u 500p uic
*.ac dec 1k 100k 10g
.PROBE


***************
*NO Matching Network
*****************
.lib "..\PIPP.lib"
.LIB "..\SIMOS.LIB"
.LIB "..\RECT.LIB"
.LIB "..\MOSNL2.LIB"
.LIB "..\DIODENL2.LIB"

.PARAM:
+ICLF=0;
+ICLMR=0;
+ICCMR=0;
+ICCF=0;
+ICCP=0;
+ICCS=0;
+ICLS=0;
+ICCFT=0;

.param
+PI=3.1415926

*IACT 0 N07 AC 1
VDUSMOS N01 N07 0


switch n07 source gate 0 sw1
.model sw1 vswitch(ron=1m roff=1meg von=2)
vdsource source 0 0

vgate gate 0 pulse(0 5 0 {TR} {TR} {PWIDTH} {1/FT})

.PARAM:
+TR={1/(100*FT)}
```

```
+PWIDTH={(DUTY/(FT))-TR-TR}


.PARAM:
+FS=20MEG
+FT=20MEG
+FMR=20MEG
+VIN=3.6
+DUTY=0.65
+QI=70
+QC=3K
+RDC=10M

*---TUNING PARAMETERS
.PARAM:
+CFNOM=760p
+CFEXTRA=0.001p
+CF={CFNOM+CFEXTRA}
+LFEXTRA= -27.5n
+K=1
+CP=0.001p
+CS=2300p
+RLOAD=17.14
+LF=29n

VDULF  N01 N02 0

XLF    n02 n03 LQS
+ PARAMS:
+ L= {LF}
+ QL={QI}
+ FQ={FS}
+ IC={ICLF}

VIN    N03 0   {VIN}

VDUCFEX N01 N04 0

XCFEXTRA N04 0 CQS
+ PARAMS:
+ C= {CF}
```

```
+ QC={QC}
+ FQ={FS}
+ IC={ICCMR}

VDUZMR NT N01 0

VDUZL  NT  M01 0

VDUCP M01 M02

XCP  M02 0 CQS
+ PARAMS:
+ C= {CP}
+ QC={QC}
+ FQ={FS}
+ IC={ICCP}


VDUCS M01 M03

XCS  M03 M05 CQS
+ PARAMS:
+ C= {CS}
+ QC={QC}
+ FQ={FS}
+ IC={ICCS}

RLOAD M05 M06 {RLOAD}
VDRLOAD M06 0 0

.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                               ;COMPONENT OF THE MEASURMENT
                               ;CIRCUITS TWO DECADES BEFORE THE
                               ;SWITCHING FREQUENCY

*-----INPUT POWER MEASUREMENT
EPI PIN01 0  VALUE={V(n03)*(-I(VIN))}
LPI PIN01 PIN {LORC(FS)}
CPI PIN   0  {LORC(FS)}
RPI PIN   0  1
```

```
*-----OUTPUT POWER MEASUREMENT
EPO PO01 0    VALUE={v(m05)*I(Vdrload)}
LPO PO01 POUT {LORC(FS)}
CPO POUT 0    {LORC(FS)}
RPO POUT 0    1  ;OUTPUT POWER

*-----EFFICIENCY
EEFF   EFF   0    VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))}

.tran 500p 5U 4.5u 500p uic
*.ac dec 1k 100k 10g
.PROBE


************************************
*LS CS Center Frequency************
************************************
.lib "..\PIPP.lib"
.LIB "..\SIMOS.LIB"
.LIB "..\RECT.LIB"
.LIB "..\MOSNL2.LIB"
.LIB "..\DIODENL2.LIB"

.PARAM:
+ICLF=0;
+ICLMR=0;
+ICCMR=0;
+ICCF=0;
+ICCP=0;
+ICCS=0;
+ICLS=0;
+ICCFT=0;

.param
+PI=3.1415926

VDUSMOS N01 N07 0

switch n07 source gate 0 sw1
.model sw1 vswitch(ron=1m roff=1meg von=2)
vdsource source 0 0
```

```
vgate gate 0 pulse(0 5 0 {TR} {TR} {PWIDTH} {1/FT})

.PARAM:
+TR={1/(100*FT)}              ;RISE TIME
+PWIDTH={(DUTY/(FT))-TR-TR}   ;PULSE WIDTH

.PARAM:
+FS=20MEG
+FT=20MEG
+FMR=20MEG
+VIN=3.6
+DUTY=0.65
+QI=70
+QC=3K
+RDC=10M
+LF= 21.08n
+CFNOM=712.5pF
;{table(LF,10.5n,1425p,15n, 997.5p, 16n, 935.15p, 17n, 880.147p, 18n, 831.25p, 21n,71
+CFEXTRA=0.001p
+K=1
+CP=0.001p
+CS={table(LS,45.84n,891.61p,70n,720p,117.79n,687p)}
+LS=45.75n
+RLOAD=17.14

VDULF  N01 N02 0

XLF    n02 n03 LQS
+ PARAMS:
+ L= {LF}
+ QL={QI}
+ FQ={FS}

+ IC={ICLF}

VIN    N03 0   {VIN}

VDUCFEX N01 N04 0

CFEXTRA N04 0 {CFNOM}
```

```
VDUZMR NT N01 0


VDUZL  NT  M01 0

VDUCP M01 M02

XCP  M02 0 CQS
+ PARAMS:
+ C= {CP}
+ QC={QC}
+ FQ={FS}
+ IC={ICCP}

VDUCS M01 M03

XCS  M03 M05 CQS
+ PARAMS:
+ C= {CS}
+ QC={QC}
+ FQ={FS}
+ IC={ICCS}


XLS M05 M05X LQS
+ PARAMS:
+ L= {LS}
+ QL={QI}
+ FQ={FS}
+ IC={ICLS}

VDULS M05X 0 0

RLOAD M05 M06 {RLOAD}
VDRLOAD M06 0 0

.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                               ;COMPONENT OF THE MEASURMENT
                               ;CIRCUITS TWO DECADES BEFORE THE
                               ;SWITCHING FREQUENCY
```

```
*-----INPUT POWER MEASUREMENT
EPI PIN01 0  VALUE={V(n03)*(-I(VIN))}
LPI PIN01 PIN {LORC(FS)}
CPI PIN   0  {LORC(FS)}
RPI PIN   0  1

*-----OUTPUT POWER MEASUREMENT
EPO PO01 0    VALUE={v(m05)*I(Vdrload)}
LPO PO01 POUT {LORC(FS)}
CPO POUT 0    {LORC(FS)}
RPO POUT 0    1  ;OUTPUT POWER


*-----EFFICIENCY
EEFF   EFF   0    VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))}

.PROBE

*.ac dec 1k 100k 10g
.tran 500p 3U 2.5u 500p uic
.end




*************************
*LS, CS Variation (Zo)***
**********************
.lib "..\PIPP.lib"
.LIB "..\SIMOS.LIB"
.LIB "..\RECT.LIB"
.LIB "..\MOSNL2.LIB"
.LIB "..\DIODENL2.LIB"

.PARAM:
+ICLF=0;
+ICLMR=0;
+ICCMR=0;
+ICCF=0;
+ICCP=0;
+ICCS=0;
```

```
+ICLS=0;
+ICCFT=0;

.param
+PI=3.1415926

*IACT 0 N07 AC 1
VDUSMOS N01 N07 0

switch n07 source gate 0 sw1
.model sw1 vswitch(ron=1m roff=1meg von=2)
vdsource source 0 0

vgate gate 0 pulse(0 5 0 {TR} {TR} {PWIDTH} {1/FT})

.PARAM:
+TR={1/(100*FT)}
+PWIDTH={(DUTY/(FT))-TR-TR}

.PARAM:
+FS=20MEG
+FT=20MEG
+FMR=20MEG
+VIN=3.6
+DUTY=0.65
+QI=70
+QC=3K
+RDC=10M

+LF= 21.08n
*+CFNOM=
+CFNOM={table(LF, 88.64n,2857.66p,44.3n,1428.68p,21n, 675p)}
;{table(LF,10.5n,1425p,15n, 997.5p, 16n, 935.15p, 17n, 880.147p, 18n, 831.25p,
;21n,712.5p,25n, 598.5p, 26n, 882.14p, 27n, 916.07p, 31.5n,450p)}
+CFEXTRA=0.001p
+K=1
+CP=0.001p

****20.17ohm to 5ohm at 25Mhz
+CS={table(LS, 47.95n, 1051.09p,70n,720p,95.9n, 525.54p,191.8n,262.77p)}
;{table(LS,45.84n,891.61p,70n,720p,117.79n,687p)};720p ;600p ;1379p ;600p; 566.67p;8
```

```
+LS=47.95n
+RLOAD=17.14

VDULF  N01 N02 0

XLF    n02 n03 LQS
+ PARAMS:
+ L= {LF}
+ QL={QI}
+ FQ={FS}
+ IC={ICLF}

VIN    N03 0   {VIN}

VDUCFEX N01 N04 0

CFEXTRA N04 0 {CFNOM}

VDUZMR NT N01 0


VDUZL  NT  M01 0

VDUCP M01 M02

XCP  M02 0 CQS
+ PARAMS:
+ C= {CP}
+ QC={QC}
+ FQ={FS}
+ IC={ICCP}

VDUCS M01 M03

XCS  M03 M05 CQS
+ PARAMS:
+ C= {CS}
+ QC={QC}
+ FQ={FS}
+ IC={ICCS}
```

```
XLS M05 M05X LQS
+ PARAMS:
+ L= {LS}
+ QL={QI}
+ FQ={FS}
+ IC={ICLS}

VDULS M05X 0 0

RLOAD M05 M06 {RLOAD}
VDRLOAD M06 0 0

.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                               ;COMPONENT OF THE MEASURMENT
                               ;CIRCUITS TWO DECADES BEFORE THE
                               ;SWITCHING FREQUENCY

*-----INPUT POWER MEASUREMENT
EPI PIN01 0  VALUE={V(n03)*(-I(VIN))}
LPI PIN01 PIN {LORC(FS)}
CPI PIN   0  {LORC(FS)}
RPI PIN   0  1

*-----OUTPUT POWER MEASUREMENT
EPO PO01 0    VALUE={v(m05)*I(Vdrload)}
LPO PO01 POUT {LORC(FS)}
CPO POUT 0    {LORC(FS)}
RPO POUT 0    1  ;OUTPUT POWER


*-----EFFICIENCY
EEFF   EFF   0    VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))}

.PROBE
*.ac dec 1k 100k 10g
.tran 500p 12U 2.5u 500p uic
.end
```

****

```
****LF, CF Variation (FC and Zo)*
*******************************


.lib "..\PIPP.lib"
.LIB "..\SIMOS.LIB"
.LIB "..\RECT.LIB"
.LIB "..\MOSNL2.LIB"
.LIB "..\DIODENL2.LIB"


.PARAM:
+ICLF=0;
+ICLMR=0;
+ICCMR=0;
+ICCF=0;
+ICCP=0;
+ICCS=0;
+ICLS=0;
+ICCFT=0;

.param
+PI=3.1415926

*IACT 0 N07 AC 1
VDUSMOS N01 N07 0

switch n07 source gate 0 sw1
.model sw1 vswitch(ron=1m roff=1meg von=2)
vdsource source 0 0

vgate gate 0 pulse(0 5 0 {TR} {TR} {PWIDTH} {1/FT})

.PARAM:
+TR={1/(100*FT)}
+PWIDTH={(DUTY/(FT))-TR-TR}

.PARAM:
+FS=20MEG
+FT=20MEG
+FMR=20MEG
```

```
+VIN=3.6
+DUTY=0.5
+QI=70
+QC=3K
+RDC=10M
+LF= 21.08n
+CFNOM={table(LF,10.8n,366.45p,21n,712.5p,43.2n,1465.8p)}
+CFEXTRA=0.001p
+K=1
+CP=0.001p
+CS=720p
+LS=70n
+RLOAD=17.14


VDULF  N01 N02 0

XLF    n02 n03 LQS
+ PARAMS:
+ L= {LF}
+ QL={QI}
+ FQ={FS}
+ IC={ICLF}

VIN    N03 0   {VIN}

VDUCFEX N01 N04 0

CFEXTRA N04 0 {CFNOM}

VDUZMR NT N01 0

VDUZL  NT  M01 0

VDUCP M01 M02

XCP  M02 0 CQS
+ PARAMS:
+ C= {CP}
+ QC={QC}
+ FQ={FS}
```

```
+ IC={ICCP}

VDUCS M01 M03

XCS  M03 M05 CQS
+ PARAMS:
+ C= {CS}
+ QC={QC}
+ FQ={FS}
+ IC={ICCS}

XLS M05 M05X LQS
+ PARAMS:
+ L= {LS}
+ QL={QI}
+ FQ={FS}
+ IC={ICLS}

VDULS M05X 0 0

RLOAD M05 M06 {RLOAD}
VDRLOAD M06 0 0

.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                               ;COMPONENT OF THE MEASURMENT
                               ;CIRCUITS TWO DECADES BEFORE THE
                               ;SWITCHING FREQUENCY

*-----INPUT POWER MEASUREMENT
EPI PIN01 0  VALUE={V(n03)*(-I(VIN))}
LPI PIN01 PIN {LORC(FS)}
CPI PIN   0  {LORC(FS)}
RPI PIN   0  1

*-----OUTPUT POWER MEASUREMENT
*EPO PO01 0    VALUE={v(M05)*I(VDUCS)}
EPO PO01 0    VALUE={v(m05)*I(Vdrload)}
LPO PO01 POUT {LORC(FS)}
CPO POUT 0    {LORC(FS)}
RPO POUT 0    1  ;OUTPUT POWER
```

```
*-----EFFICIENCY
EEFF    EFF    0     VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))}

.PROBE
.step param LF list 10.8n 21n 43.2n
.tran 500p 3U 2.5u 500p uic
.end




**************************
***LF transient response**
************************
.lib "..\PIPP.lib"
.LIB "..\SIMOS.LIB"
.LIB "..\RECT.LIB"
.LIB "..\MOSNL2.LIB"
.LIB "..\DIODENL2.LIB"

.PARAM:
+ICLF=0;
+ICLMR=0;
+ICCMR=0;
+ICCF=0;
+ICCP=0;
+ICCS=0;
+ICLS=0;
+ICCFT=0;

.param
+PI=3.1415926

*IACT 0 N07 AC 1
VDUSMOS N01 N07 0

switch n07 source gate 0 sw1
.model sw1 vswitch(ron=1m roff=1meg von=2)
vdsource source 0 0
```

```
vgate gate 0 pulse(0 5 0 {TR} {TR} {PWIDTH} {1/FT})

.PARAM:
+TR={1/(100*FT)}
+PWIDTH={(DUTY/(FT))-TR-TR}

.PARAM:
+FS=20MEG
+FT=20MEG
+FMR=20MEG
+VIN=3.6
+DUTY=0.65
+QI=70
+QC=3K
+RDC=10M


.PARAM:
+CFNOM={table(lf,21n,712.5p,70n,205p)}
+CFEXTRA=0.001p
+CF={CFNOM+CFEXTRA}
+K=1
+CP=0.001p
+CS={table(Lf,21n,720p,70n,130p)}
+LS={table(Lf,21n,70n,70n,140n)}
+RLOAD=17.14
+LF= 70n

VDULF  N01 N02 0

XLF    n02 n03 LQS
+ PARAMS:
+ L= {LF}
+ QL={QI}
+ FQ={FS}
+ IC={ICLF}

VIN    N03 0   {VIN}

VDUCFEX N01 N04 0
```

```
XCFEXTRA N04 0 CQS
+ PARAMS:
+ C= {CF}
+ QC={QC}
+ FQ={FS}
+ IC={ICCMR}

VDUZMR NT N01 0

VDUZL  NT  M01 0

VDUCP M01 M02

XCP  M02 0 CQS
+ PARAMS:
+ C= {CP}
+ QC={QC}
+ FQ={FS}
+ IC={ICCP}


VDUCS M01 M03

XCS  M03 M05 CQS
+ PARAMS:
+ C= {CS}
+ QC={QC}
+ FQ={FS}
+ IC={ICCS}


XLS M05 M05X LQS
+ PARAMS:
+ L= {LS}
+ QL={QI}
+ FQ={FS}
+ IC={ICLS}

VDULS M05X 0 0

RLOAD M05 M06 {RLOAD}
```

```
VDRLOAD M06 0 0

.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                               ;COMPONENT OF THE MEASURMENT
                               ;CIRCUITS TWO DECADES BEFORE THE
                               ;SWITCHING FREQUENCY

*-----INPUT POWER MEASUREMENT
EPI PIN01 0  VALUE={V(n03)*(-I(VIN))}
LPI PIN01 PIN {LORC(FS)}
CPI PIN   0  {LORC(FS)}
RPI PIN   0  1

*-----OUTPUT POWER MEASUREMENT
EPO PO01 0    VALUE={v(m05)*I(Vdrload)}
LPO PO01 POUT {LORC(FS)}
CPO POUT 0    {LORC(FS)}
RPO POUT 0    1  ;OUTPUT POWER


*-----EFFICIENCY
EEFF   EFF   0    VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))}

.step param lf list 21n 70n
.tran 500p 0.7U 0.001u 500p uic
.PROBE
```

A.1.4 Converter data:

```
************************
**full converter*****
************************


.lib "..\PIPP.lib"
.LIB "..\SIMOS.LIB"
.LIB "..\RECT.LIB"
.LIB "..\MOSNL2.LIB"
.LIB "..\DIODENL2.LIB"
```

```
.OPTIONS ABSTOL=5nA
+          GMIN=10p
+          ITL1=6000
+          ITL2=4000
+          ITL4=500
+          RELTOL=0.003
+          VNTOL=0.04mV
.OPTION STEPGMIN


.OPTIONS
+ NOPAGE
+ NOBIAS
+ NOECHO
+ NOMOD
+ NUMDGT=8
.WIDTH OUT=132


.PARAM:
+ICLF=0;
+ICLMR=0;
+ICCMR=0;
+ICCF=0;
+ICCP=0;
+ICCS=0;
+ICLS=0;
+ICCFT=0;


.param
+PI=3.1415926

VDUSMOS N01 N07 0

VGATE GATE 0 PULSE(-25 25 0 {TR} {TR} {PWIDTH} {1/FT})

XSIMOS GATE N07 0 MOSFETNLC
+ PARAMS:
```

```
+ RDSON=0.059*1.6
+ RG=1.17
+ CGS=600P
+ RCOUT=0.118
+ RSHUNT=12MEG
+ CJO=235.24P
+ VJ=0.5476556
+ M=0.448313

XSIMOS2 GATE N07 0 MOSFETNLC
+ PARAMS:
+ RDSON=0.059*1.6
+ RG=1.17
+ CGS=600P
+ RCOUT=0.118
+ RSHUNT=12MEG
+ CJO=235.24P
+ VJ=0.5476556
+ M=0.448313


.PARAM:
+TR={1/(100*FT)}              ;RISE TIME
+PWIDTH={(DUTY/(FT))-TR-TR}   ;PULSE WIDTH

.PARAM:
+FS=20MEG
+FT=20MEG
+FMR=20MEG
+VIN=3.6
+DUTY=0.55
+QI=70
+QC=3K
+RDC=10M

.PARAM:
+CFNOM=780p
+CFEXTRA=0.001p
+CF={CFNOM+CFEXTRA}
+LFEXTRA= -27.5n
+K=1
```

```
+CP=0.001p
+CS=1000p
+LS=105n
+RLOAD=18.63
+LF= 24n

.param
+ Vout=7
+ QLR=70
+ C2=100p
+ Lr=125n


VDULF  N01 N02 0

XLF    n02 n03 LQS
+ PARAMS:
+ L= {LF}
+ QL={QI}
+ FQ={FS}
+ IC={ICLF}

VIN    N03 0   {VIN}


VDUCFEX N01 N04 0

XCFEXTRA N04 0 CQS
+ PARAMS:
+ C= {CF}
+ QC={QC}
+ FQ={FS}
+ IC={ICCMR}

VDUZMR NT N01 0

VDUZL  NT  M01 0

VDUCP M01 M02

XCP  M02 0 CQS
```

```
+ PARAMS:
+ C= {CP}
+ QC={QC}
+ FQ={FS}
+ IC={ICCP}


VDUCS M01 M03

XCS  M03 M05 CQS
+ PARAMS:
+ C= {CS}
+ QC={QC}
+ FQ={FS}
+ IC={ICCS}


XLS M05 M05X LQS
+ PARAMS:
+ L= {LS}
+ QL={QI}
+ FQ={FS}
+ IC={ICLS}


VDULS M05X 0 0

VDUREC m05 r01 0

vdlr r01 r01x 0

XLR  0 R01x LQS
+ PARAMS:
+ L={LR}
+ QL={QLR}
+ FQ={FS}
+ IC=0

XC  R01 R02 CQS
+ PARAMS:
+ C= {C2}
```

```
+ QC={QC}
+ FQ={FS}
+ IC=0

XSS36 R01 R02 SS36NL
+ PARAMS:
+ LDS=3.7668p
+ VDON=0.3
+ CJO=252P
+ VJ=0.62638
+ M=0.42102
+ FS=20MEG

VOUT  R02 0 {VOUT}

.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                               ;COMPONENT OF THE MEASURMENT
                               ;CIRCUITS TWO DECADES BEFORE THE
                               ;SWITCHING FREQUENCY

*-----INPUT POWER MEASUREMENT
EPI PIN01 0  VALUE={V(n03)*(-I(VIN))}
LPI PIN01 PIN {LORC(FS)}
CPI PIN   0  {LORC(FS)}
RPI PIN   0  1

*-----OUTPUT POWER MEASUREMENT

EPO PO01 0    VALUE={v(r02)*I(Vout)}
LPO PO01 POUT {LORC(FS)}
CPO POUT 0    {LORC(FS)}
RPO POUT 0    1  ;OUTPUT POWER


*-----EFFICIENCY
EEFF   EFF   0    VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))}


.tran 500p 10U 2.5u 500p uic
*.ac dec 1k 100k 10g
.PROBE
```

A.1.5 Other Topologies data:

```
*****************************
***Alternative Topology*****
*****************************
.lib "PIPP.lib"
.LIB "SIMOS.LIB"
.LIB "RECT.LIB"
.LIB "MOSNL2_PSPICE.LIB"
.LIB "diodenl1.LIB"

.OPTIONS ABSTOL=5nA
+          GMIN=10p
+          ITL1=6000
+          ITL2=4000
+          ITL4=500
+          RELTOL=0.003
+          VNTOL=0.04mV
.OPTION STEPGMIN

.OPTIONS
+ NOPAGE
+ NOBIAS
+ NOECHO
+ NOMOD
+ NUMDGT=8
.WIDTH OUT=132       ;TO PRINT MORE COLUMNS

.PARAM:
+ICLF=0;
+ICLMR=0;
+ICCMR=0;
+ICCF=0;
+ICCP=0;
+ICCS=0;
+ICLS=0;
+ICCFT=0;

.INC "alternative_inverter1.CIR"

VDUSMOS N01 N07 0
```

```
XSIMOS GATE N07 0 MOSFETNLC
+ PARAMS:
+ RDSON=0.059*1.65
+ RG=1.17
+ CGS=600P
+ RCOUT=0.118
+ RSHUNT=12MEG
+ CJO=235.24P
+ VJ=0.5476556
+ M=0.448313


XSIMOS2 GATE N07 0 MOSFETNLC
+ PARAMS:
+ RDSON=0.059*1.65
+ RG=1.17
+ CGS=600P
+ RCOUT=0.118
+ RSHUNT=12MEG
+ CJO=235.24P
+ VJ=0.5476556
+ M=0.448313

.PARAM:
+TR={1/(100*FT)}              ;RISE TIME
+PWIDTH={(DUTY/(FT))-TR-TR}   ;PULSE WIDTH

VGATE GATE 0 PULSE(-25 25 0 {TR} {TR} {PWIDTH} {1/FT})

IT 0 NT AC 1

.inc "alternative_rectifier1.cir"

.PARAM:
+FS=20MEG
+FT=20MEG
+FMR=20MEG
+VIN=3.6
+DUTY=0.34
+QI=70
```

```
+QC=3K
+RDC=10M

.PARAM:
+CFNOM=450p
+CFEXTRA=0.001p
+CF={CFNOM+CFEXTRA}
+LFEXTRA= -41.25n
+LF=14.33n
+K=1
+LMREXTRA=0
+CMREXTRA=0
+CP=1350p
+CS=2100p
+LS=43n


.param
+ VOUT=7
+ QLR=70
+ Crec=344.25p
+ Lrec=63n

.tran 235p 3U 0.01u 235p uic
.PROBE


**********************
*alternative topology 3
**********************
.lib "PIPP.lib"
.LIB "SIMOS.LIB"
.LIB "RECT.LIB"
.LIB "MOSNL2_PSPICE.LIB"
.LIB "diodenl1.LIB"

.OPTIONS ABSTOL=5nA
+          GMIN=10p
+          ITL1=6000
+          ITL2=4000
+          ITL4=500
+          RELTOL=0.003
```

```
+          VNTOL=0.04mV
.OPTION STEPGMIN


.OPTIONS
+ NOPAGE
+ NOBIAS
+ NOECHO
+ NOMOD
+ NUMDGT=8
.WIDTH OUT=132       ;TO PRINT MORE COLUMNS


.PARAM:
+ICLF=0;
+ICLMR=0;
+ICCMR=0;
+ICCF=0;
+ICCP=0;
+ICCS=0;
+ICLS=0;
+ICCFT=0;

.INC "INVERTER.CIR"

VDUSMOS N01 N07 0

XSIMOS GATE N07 0 MOSFETNLC
+ PARAMS:
+ RDSON=0.059*1.65
+ RG=1.17
+ CGS=600P
+ RCOUT=0.118
+ RSHUNT=12MEG
+ CJO=235.24P
+ VJ=0.5476556
+ M=0.448313

XSIMOS2 GATE N07 0 MOSFETNLC
+ PARAMS:
+ RDSON=0.059*1.65
```

```
+ RG=1.17
+ CGS=600P
+ RCOUT=0.118
+ RSHUNT=12MEG
+ CJO=235.24P
+ VJ=0.5476556
+ M=0.448313

.PARAM:
+TR={1/(100*FT)}              ;RISE TIME
+PWIDTH={(DUTY/(FT))-TR-TR}   ;PULSE WIDTH

VGATE GATE 0 PULSE(-25 25 0 {TR} {TR} {PWIDTH} {1/FT})

IT 0 NT AC 1

.inc "alternative_rectifier2.cir"

.PARAM:
+FS=20MEG
+FT=20MEG
+FMR=20MEG
+VIN=3.6
+DUTY=0.55
+QI=70
+QC=3K
+RDC=10M

.PARAM:
+CFNOM=562.5p
+CFEXTRA=0.001p
+CF={CFNOM+CFEXTRA}
+LFEXTRA= -12n
+K=1
+LMREXTRA=0
+CMREXTRA=0
+CP=1312p
+Cb=187.5p
+CS= 1652p
+LS= 85n
+RLOAD=20.17
```

```
.param
+ VOUT=7
+ QLR=70
+ Crec=285p
+ Lrec=75.6n

.tran 235p 3U 0.01u 235p uic
*.ac dec 1k 100k 10g
.PROBE


**************************
*****alternative topology 2

**************************
.lib "PIPP.lib"
.LIB "SIMOS.LIB"
.LIB "RECT.LIB"
.LIB "MOSNL2_PSPICE.LIB"
.LIB "diodenl1.LIB"

.OPTIONS ABSTOL=5nA
+          GMIN=10p
+          ITL1=6000
+          ITL2=4000
+          ITL4=500
+          RELTOL=0.003
+          VNTOL=0.04mV
.OPTION STEPGMIN

.OPTIONS
+ NOPAGE
+ NOBIAS
+ NOECHO
+ NOMOD
+ NUMDGT=8
.WIDTH OUT=132       ;TO PRINT MORE COLUMNS

.PARAM:
+ICLF=0;
+ICLMR=0;
```

```
+ICCMR=0;
+ICCF=0;
+ICCP=0;
+ICCS=0;
+ICLS=0;
+ICCFT=0;

.INC "alternative_inverter1.CIR"

VDUSMOS N01 N07 0


XSIMOS GATE N07 0 MOSFETNLC
+ PARAMS:
+ RDSON=0.059*1.65
+ RG=1.17
+ CGS=600P
+ RCOUT=0.118
+ RSHUNT=12MEG
+ CJO=235.24P
+ VJ=0.5476556
+ M=0.448313


XSIMOS2 GATE N07 0 MOSFETNLC
+ PARAMS:
+ RDSON=0.059*1.65
+ RG=1.17
+ CGS=600P
+ RCOUT=0.118
+ RSHUNT=12MEG
+ CJO=235.24P
+ VJ=0.5476556
+ M=0.448313

.PARAM:
+TR={1/(100*FT)}              ;RISE TIME
+PWIDTH={(DUTY/(FT))-TR-TR}   ;PULSE WIDTH

VGATE GATE 0 PULSE(-25 25 0 {TR} {TR} {PWIDTH} {1/FT})
```

```
IT 0 NT AC 1

.inc "alternative_rectifier2.cir"

.PARAM:
+FS=20MEG
+FT=20MEG
+FMR=20MEG
+VIN=3.6
+DUTY=0.38
+QI=70
+QC=3K
+RDC=10M

.PARAM:
+CFNOM=810p
+CFEXTRA=0.001p
+CF={CFNOM+CFEXTRA}
+LFEXTRA= -4.33n
+K=1
+LMREXTRA=0
+CMREXTRA=0
+CP=1890p
+Cb=150p
+CS=2377p
+LS= 59n
+RLOAD=20.17

.param
+ VOUT=7
+ QLR=70
+ Crec=412p
+ Lrec=56.66n

.tran 235p 3U 0.01u 235p uic
.PROBE


.PARAM:
+ PI=3.14159     ;GUESS WHAT
```

```
**************************
***alternative inverter1
**************************

.PARAM:
+LF={1/(9*CF*PWR((PI*FMR),2))+LFEXTRA}
+LMR0={1/(15*CF*PWR((PI*FMR),2))}
+LMR={(K*LMR0)+LMREXTRA}
+CMR0={(15*CF/16)}
+CMR={(CMR0/K)+CMREXTRA}

VDULF  N01 N02 0

XLF    n02 n03 LQS
+ PARAMS:
+ L= {LF}
+ QL={QI}
+ FQ={FS}
+ IC={ICLF}

VIN    N03 0   {VIN}


VDUCFEX N01 N04 0

XCFEXTRA N04 0 CQS
+ PARAMS:
+ C= {CFEXTRA}
+ QC={QC}
+ FQ={FS}
+ IC={ICCMR}


VDUMR N01 N05 0

XLMR    N05 N06 LQS
+ PARAMS:
+ L= {LMR}
+ QL={QI}
+ FQ={FS}
+ IC={ICLMR}
```

```
XCMR    N06 0 CQS
+ PARAMS:
+ C= {CMR}
+ QC={QC}
+ FQ={FS}
+ IC={ICCMR}


VDUZMR NT N01 0
```

```
**********************
***Alternative Topology 1 Rectifier
*******************************


VDUZL  NT  M01 0

VDUCP M01 M02

XCP  M02 0 CQS
+ PARAMS:
+ C= {CP}
+ QC={QC}
+ FQ={FS}
+ IC={ICCP}


VDUCS M01 M03

XCS  M03 M05 CQS
```

```
+ PARAMS:
+ C= {CS}
+ QC={QC}
+ FQ={FS}
+ IC={ICCS}


XLS M05 M05X LQS
+ PARAMS:
+ L= {LS}
+ QL={QI}
+ FQ={FS}
+ IC={ICLS}

VDULS M05X 0 0

VDUREC M05 R01 0

XLR r01x R01 LQS
+ PARAMS:
+ L={Lrec}
+ QL={QLR}
+ FQ={FS}
+ IC=0

VDULR R01x 0 0

XC R01 R02 CQS
+ PARAMS:
+ C= {Crec}
+ QC={QC}
+ FQ={FS}
+ IC=0


XDFLS220L R01 R02X SS36NL
+ PARAMS:
+ LDS=3.7668p
+ VDON=0.3
+ CJO=252P
+ VJ=0.62638
```

```
+ M=0.42102
+ FS=20MEG

VDUDio R02X R02 0

VOUT  R02 0 {VOUT}

.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                               ;COMPONENT OF THE MEASURMENT
                               ;CIRCUITS TWO DECADES BEFORE THE
                               ;SWITCHING FREQUENCY

*-----INPUT POWER MEASUREMENT
EPI PIN01 0  VALUE={V(n03)*(-I(VIN))}
LPI PIN01 PIN {LORC(FS)}
CPI PIN   0  {LORC(FS)}
RPI PIN   0  1

*-----OUTPUT POWER MEASUREMENT
EPO PO01 0    VALUE={v(R02)*I(Vout)}
LPO PO01 POUT {LORC(FS)}
CPO POUT 0    {LORC(FS)}
RPO POUT 0    1  ;OUTPUT POWER


*-----EFFICIENCY
EEFF   EFF   0    VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))}
EEFF2   EFF2   0    VALUE={IF(TIME<100N,0,V(POUT)/(v(PIN)+0.192))}

*---RMS OF DRAIN VOLTAGE

ERMS1 RMS1 0 VALUE={V(NT)**2}
LRMS1 RMS1 RMS2 {LORC(FS)}
CRMS1 RMS2 0    {LORC(FS)}
RRMS1 RMS2 0    1  ;RMS OUTPUT VOLTAGE
ERMS2 VNTRMS 0 VALUE={SQRT(V(RMS2))}
RRMS2 VNTRMS 0  1

VPLF PLF 0  {LF}
VPLMR PLMR 0 {LMR}
VPCMR PCMR 0 {CMR}
```

```
********************
*alternative_rectifier3
**********************


VDUZL  NT  M01 0

VDUCP M01 M02 0

XCP  M02 0 CQS
+ PARAMS:
+ C= {CP}
+ QC={QC}
+ FQ={FS}
+ IC={ICCP}


VDUCS M01 M03 0

XCB  M04 M05 CQS
+ PARAMS:
+ C= {Cs}
+ QC={QC}
+ FQ={FS}
+ IC={ICCS}


XLS M03 M04X LQS
+ PARAMS:
+ L= {LS}
+ QL={QI}
+ FQ={FS}
+ IC={ICLS}

XCS  M05 0 CQS
+ PARAMS:
+ C= {CS}
+ QC={QC}
```

```
+ FQ={FS}
+ IC={ICCS}

VDURL M04X M04 0

VDUREC M05 R01 0

XLR r01x R01 LQS
+ PARAMS:
+ L={Lrec}
+ QL={QLR}
+ FQ={FS}
+ IC=0

VDULR R01x R02 0

XC 0 R01 CQS
+ PARAMS:
+ C= {Crec}
+ QC={QC}
+ FQ={FS}
+ IC=0



XDFLS220L 0 R02X SS36NL
+ PARAMS:
+ LDS=3.7668p
+ VDON=0.3
+ CJO=252P
+ VJ=0.62638
+ M=0.42102
+ FS=30MEG

VDUDio R02X R01 0

VOUT  R02 0 {VOUT}

**************************

.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
```

```
                                ;COMPONENT OF THE MEASURMENT
                                ;CIRCUITS TWO DECADES BEFORE THE
                                ;SWITCHING FREQUENCY

*-----INPUT POWER MEASUREMENT
EPI PIN01 0  VALUE={V(n03)*(-I(VIN))}
LPI PIN01 PIN {LORC(FS)}
CPI PIN   0  {LORC(FS)}
RPI PIN   0  1

*-----OUTPUT POWER MEASUREMENT

EPO PO01 0    VALUE={v(R02)*I(VOUT)}
LPO PO01 POUT {LORC(FS)}
CPO POUT 0    {LORC(FS)}
RPO POUT 0    1  ;OUTPUT POWER


*-----EFFICIENCY
EEFF   EFF   0    VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))}


*---RMS OF DRAIN VOLTAGE

ERMS1 RMS1 0 VALUE={V(NT)**2}
LRMS1 RMS1 RMS2 {LORC(FS)}
CRMS1 RMS2 0    {LORC(FS)}
RRMS1 RMS2 0    1  ;RMS OUTPUT VOLTAGE
ERMS2 VNTRMS 0 VALUE={SQRT(V(RMS2))}
RRMS2 VNTRMS 0  1
```

A.2 Chapter 4 Data

A.2.1 Sinusoidal Resonant Gate Drive data:

```
**********************************
****GATE DRIVE w POWER STAGE*******
**********************************
```

```
.lib "PIPP.lib"
.LIB "SIMOS.LIB"
.LIB "RECT.LIB"
.LIB "MOSNL2.LIB"
.LIB "diodenl2.LIB"



.OPTIONS ABSTOL=5nA
+          GMIN=10p
+          ITL1=6000
+          ITL2=4000
+          ITL4=500
+          RELTOL=0.003
+          VNTOL=0.04mV
.OPTION STEPGMIN


.OPTIONS
+ NOPAGE
+ NOBIAS
+ NOECHO
+ NOMOD
+ NUMDGT=8
.WIDTH OUT=132       ;TO PRINT MORE COLUMNS


.PARAM:
+ICLF=0;
+ICLMR=0;
+ICCMR=0;
+ICCF=0;
+ICCP=0;
+ICCS=0;
+ICLS=0;
+ICCFT=0;

.INC "INVERTER.CIR"
```

```
.PARAM
+L1=110n
+L2={table(L1,72n,110n,110n,72n)}
+CBYP=0.008u
+Rinv=1.11
+Cin=0.1u
+CinInput=22.5p
+Cinv=40p
+VCC=3.2

VINGate INGate 0 PULSE(0.25 {VCC} 0 100P 100P {(1/(2*FS))-200P} {1/FS}) AC 1

Rsource INgate INR {Rinv}

Csource INR 0 {Cinv}

XCin INR INC CQS
+ PARAMS:
+ C= {Cin}
+ QC=100k
+ FQ={FS}
+ IC=0

XL1 INC Gate LQS
+ PARAMS:
+ L= {L1}
+ QL={QI}
+ FQ={FS}
+ IC=0


XL2 Gate SHUNT_INT LQS
+ PARAMS:
+ L= {L2}
+ QL={QI}
+ FQ={FS}
+ IC=0

XCBYP SHUNT_INT 0 CQS
+ PARAMS:
+ C= {CBYP}
```

```
+ QC={QC}
+ FQ={FS}
+ IC=0

VDUSMOS N01 N07 0  ;DUMMY MEASURE SWITCH CURRENT


XSIMOS GATE N07 0 MOSFETNLC
+ PARAMS:
+ RDSON=0.059*1.65
+ RG=1.17
+ CGS=600P
+ RCOUT=0.118
+ RSHUNT=12MEG
+ CJO=235.24P
+ VJ=0.5476556
+ M=0.448313


XSIMOS2 GATE N07 0 MOSFETNLC
+ PARAMS:
+ RDSON=0.059*1.65
+ RG=1.17
+ CGS=600P
+ RCOUT=0.118
+ RSHUNT=12MEG
+ CJO=235.24P
+ VJ=0.5476556
+ M=0.448313

.PARAM:
+TR={1/(100*FT)}
+PWIDTH={(DUTY/(FT))-TR-TR}


IT 0 NT AC 1

.inc "Rectifier.cir"


.PARAM:
```

```
+FS=20MEG
+FT=20MEG
+FMR=20MEG
+VIN=3.6
+DUTY=0.4
+QI=70
+QC=3K
+RDC=10M

.PARAM:
+CFNOM=75p
+CFEXTRA=630p
+CF={CFNOM+CFEXTRA}
+LF=27n
+K=1
+CP=10p
+CS=1275p
+LS=139.5n


.param
+ Vout=7
+ QLR=70
+ Crec=450p
+ Lrec=64.5n



.tran 3000p 10.5U 2.5u 3000p uic
.PROBE
```

A.2.2 Self-Oscillating Gate Drive data:

```
************************
*self oscillating gate drive*
*****************************
.lib "PIPP.lib"
.LIB "SIMOS.LIB"
.LIB "RECT.LIB"
```

```
.LIB "MOSNL2PSPICE.LIB"
.LIB "diodenl2.LIB"

.PARAM:
+ICLF=0;
+ICLMR=0;
+ICCMR=0;
+ICCF=0;
+ICCP=0;
+ICCS=0;
+ICLS=0;
+ICCFT=0;

.INC "INVERTER.CIR"

.param:
+cfb=10p
+rfb=2.7k
+lfb=30n
+Ld2r=12n
+Rd2r=20

xcfb n07 g01 CQS
+ PARAMS:
+ C= {Cfb}
+ QC=100k
+ FQ={FS}
+ IC=0

xLfb g01 0 LQS
+ PARAMS:
+ L= {Lfb}
+ QL={QI}
+ FQ={FS}
+ IC=0

Rfb g01 0 {Rfb}

xLd2r g01 gate LQS
+ PARAMS:
+ L= {Ld2r}
```

```
+ QL={QI}
+ FQ={FS}
+ IC=0

Rd2r g01 gate {Rd2r}


VDUSMOS N01 N07 0


XSIMOS GATE N07 0 MOSFETNLC
+ PARAMS:
+ RDSON=0.059*1.65
+ RG=1.17
+ CGS=600P
+ RCOUT=0.118
+ RSHUNT=12MEG
+ CJO=235.24P
+ VJ=0.5476556
+ M=0.448313


XSIMOS2 GATE N07 0 MOSFETNLC
+ PARAMS:
+ RDSON=0.059*1.65
+ RG=1.17
+ CGS=600P
+ RCOUT=0.118
+ RSHUNT=12MEG
+ CJO=235.24P
+ VJ=0.5476556
+ M=0.448313


.PARAM:
+TR={1/(100*FT)}              ;RISE TIME
+PWIDTH={(DUTY/(FT))-TR-TR}   ;PULSE WIDTH


IT 0 NT AC 1
```

```
.inc "rectifier.cir"


.PARAM:
+FS=20MEG
+FT=20MEG
+FMR=20MEG
+VIN=3.6
+DUTY=0.55
+QI=70
+QC=3K
+RDC=10M
+CFNOM=75p
+CFEXTRA=630p
+CF={CFNOM+CFEXTRA}
+LF=27n
+K=1
+CP=10p
+CS=1275p
+LS=139.5n
+ Vout=7
+ QLR=70
+ Crec=100p
+ Lrec=64.5n


VDUZL  NT  M01 0

VDUCP M01 M02

XCP  M02 0 CQS
+ PARAMS:
+ C= {CP}
+ QC={QC}
+ FQ={FS}
+ IC={ICCP}


VDUCS M01 M03

XCS  M03 M05 CQS
```

```
+ PARAMS:
+ C= {CS}
+ QC={QC}
+ FQ={FS}
+ IC={ICCS}


XLS M05 M05X LQS
+ PARAMS:
+ L= {LS}
+ QL={QI}
+ FQ={FS}
+ IC={ICLS}

VDULS M05X 0 0

VDUREC M05 R01 0

XLR r01x R01 LQS
+ PARAMS:
+ L={Lrec}
+ QL={QLR}
+ FQ={FS}
+ IC=0

VDULR R01x 0 0

XC R01 R02 CQS
+ PARAMS:
+ C= {Crec}
+ QC={QC}
+ FQ={FS}
+ IC=0

XDFLS220L R01 R02X SS36NL
+ PARAMS:
+ LDS=3.7668p
+ VDON=0.3
+ CJO=252P
+ VJ=0.62638
+ M=0.42102
```

```
+ FS=30MEG

VDUDio R02X R02 0

VOUT  R02 0 {VOUT}


.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                               ;COMPONENT OF THE MEASURMENT
                               ;CIRCUITS TWO DECADES BEFORE THE
                               ;SWITCHING FREQUENCY

*-----INPUT POWER MEASUREMENT
EPI PIN01 0  VALUE={V(n03)*(-I(VIN))}
LPI PIN01 PIN {LORC(FS)}
CPI PIN   0  {LORC(FS)}
RPI PIN   0  1

*-----OUTPUT POWER MEASUREMENT

EPO PO01 0    VALUE={v(R02)*I(Vout)}
LPO PO01 POUT {LORC(FS)}
CPO POUT 0    {LORC(FS)}
RPO POUT 0    1  ;OUTPUT POWER

*-----EFFICIENCY
EEFF   EFF   0    VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))}


*---RMS OF DRAIN VOLTAGE
ERMS1 RMS1 0 VALUE={V(NT)**2}
LRMS1 RMS1 RMS2 {LORC(FS)}
CRMS1 RMS2 0    {LORC(FS)}
RRMS1 RMS2 0    1  ;RMS OUTPUT VOLTAGE
ERMS2 VNTRMS 0 VALUE={SQRT(V(RMS2))}
RRMS2 VNTRMS 0  1


*-----PARAMETERS FOR THE BANDPASS FILTER
.PARAM
+ QBP=100
```

```
.FUNC  CBPQ(FS,QBP) {1/(2*PI*FS*QBP)}
.FUNC  LBPQ(FS,QBP) {QBP/(2*PI*FS)}

*-----FUNAMDENTAL OF THE RECT. VOLTAGE
EBPRVd  BPRVd1  0      VALUE={V(NO7)}
LBPRVd  BPRVd1  BPRVd2  {LBPQ(FS,QBP)}
CBPRVd  BPRVd2  BPRVd3  {CBPQ(FS,QBP)}
RBPRVd  BPRVd3  0      1


*-----FUNAMDENTAL OF THE RECT. VOLTAGE
EBPRV  BPRV1  0      VALUE={V(NT)}
LBPRV  BPRV1  BPRV2  {LBPQ(FS,QBP)}
CBPRV  BPRV2  BPRV3  {CBPQ(FS,QBP)}
RBPRV  BPRV3  0      1

*-----FUNDAMENTAL OF THE RECT. CURRENT
EBPRI  BPRI1  0      VALUE={v(NT)}
LBPRI  BPRI1  BPRI2  {LBPQ(3*FS,QBP)}
CBPRI  BPRI2  BPRI3  {CBPQ(3*FS,QBP)}
RBPRI  BPRI3  0      1


.ac dec 1k 1MEG 10g
.PROBE
```

A.2.3 SPICE Model Libraries

```
**************************
**DIODENL2 MODEL**********
**************************

.SUBCKT SS36NL A K
+ PARAMS:
+ LDS=3.7668p  ;SERIES INDUCTANCE
+ VDON=0.375  ;DIODE FORWARD DROP
+ CJO=252P
+ VJ=0.62638
+ M=0.42102
```

```
+ FS=30MEG


*PARASITIC LEAD INDUCTANCE
LDS     A     101   {LDS}  IC=0
*

*IDEAL DIODE MODEL
DIDEAL 101   102   IDEAL
.MODEL IDEAL D(N=0.001)

*FORWARD VOLTAGE DROP MODEL
VDON    102  K     {VDON}

*NONLINEAR CAPACITANCE EVALUATED AS A CONTROLLED CURRENT
*SOURCE

GCNL   K 101 VALUE={IF((V(K)-V(101))<0,CJO*V(201)*(1/LDER),V(201)*(1/LDER)*(CJO/((1+(


****SUBCIRCUIT TO EVALUATE THE DERIVATIVE***

*PARAMETERS AND DEFINITION FOR THIS SUBCIRCUIT
.PARAM:
+ LDER=1U     ;INDUCT FOR THE DERIVATIVE SUBCIRCUIT
+ PI=3.14159265

*FUNC. FOR R OF THE DERIVATIVE SUBCIRCUIT
.FUNC RDER(LDER,FS) {3000*2*PI*FS*LDER}
GY 0 201 VALUE={V(K)-V(101)}
L1 201 0 {LDER}
R1 201 0 {RDER(LDER,FS)}

.ENDS SS36NL



**********
```

```
*MOSNL2 MODEL**
***************

.SUBCKT MOSFETNLC  GATE DRAIN SOURCE
+ PARAMS:
+ RDSON=0.04
+ RG=0.3
+ CGS=1750P
+ RCOUT=0.08
+ RSHUNT=12MEG
+ CJO=1450P
+ VJ=0.818366
+ M=0.5049
+ LDRAIN = 1p
+ LSOURCE = 1p
+ LGATE = 1p
+ CRSS = 10p


LDRAIN DRAIN DRAINL {LDRAIN}
RSHUNT DRAINL SOURCEL {RSHUNT}
LSOURCE SOURCEL SOURCE {LSOURCE}


SW      DRAINL   SOURCEL   GMAIN  SOURCE   SWIDEAL
*.MODEL SWIDEAL VSWITCH (RON={RDSON} ROFF=1MEG VON=2.5 VOFF=1.5 ILIMIT=50)
*PSPICE MODEL
.MODEL SWIDEAL VSWITCH (RON={RDSON} ROFF=1MEG VON=2.5 VOFF=1.5)


*NONLINEAR CAPACITANCE EVALUATED AS A CONTROLLED CURRENT SOURCE
GCNL  N101 DRAINL VALUE={IF((V(DRAINL)-V(N101))<0,CJO*V(201)*(1/LDER),V(201)*(1/LDER)

DIDEAL SOURCEL DRAINL DIODE
.model DIODE D(N=.0001)


RCOUT N101   SOURCEL {RCOUT}

LGATE GATE GATEL {LGATE} ;RSER=10m RPAR=1MEG
RG  GATEL GMAIN    {RG}
```

```
CGS GMAIN SOURCEL {CGS} ;RSER=10m RPAR=1MEG
*RRSS DRAINL DRAINR 10
CRSS DRAINL GMAIN {CRSS} ;RSER=30 RPAR=1MEG

****SUBCIRCUIT TO EVALUATE THE DERIVATIVE***

*PARAMETERS AND DEFINITION FOR THIS SUBCIRCUIT
.PARAM:
+ LDER=.01U     ;INDUCT FOR THE DERIVATIVE SUBCIRCUIT
+ PI=3.1416

*FUNC. FOR R OF THE DERIVATIVE SUBCIRCUIT
.FUNC RDER(LDER,FS) {1000*2*PI*FS*LDER}
GY 0 201 VALUE={V(N101)-V(DRAINL)}
L1 201 0 {LDER}
R1 201 0 {RDER(LDER,FS)}
.ENDS MOSFETNLC
*$




*****************************************
*****INDUCTOR, CAPACITOR MODELS************
*****************************************

.SUBCKT LQS LSI LSO
+ PARAMS:
+ L=1U
+ QL=300
+ FQ=60MEG
+ IC=0

.PARAM: PI=3.1416

.FUNC ESR(L,QL,FQ) {2*PI*FQ*L/QL}

R1 LSI  101 {ESR(L,QL,FQ)}  ;SERIES RESISTANCE
L1 101 LSO  {L} IC={IC}     ;SERIES INDUCTANCE
```

```
.ENDS LQS


.SUBCKT LCHOKE LSI LSO
+ PARAMS:
+ L=1U
+ QL=300
+ FQ=60MEG
+ RDC=1M
+ IC=0

.PARAM:
+ PI=3.1416
+ OMEGA_0={2*PI*FQ/100}

.FUNC ESR(L,QL,FQ) {2*PI*FQ*L/QL}


*DC RESISTANCE AND BYPASS CAPACITOR
RDC LSI  101 {RDC}              ;DC RESISTANCE
CBP LSI  101 {1/(RDC*OMEGA_0)} IC={IC};BYPASS CAP

*AC RESISTANCE AND BYPASS INDUCTOR
RAC 101 102 {ESR(L,QL,FQ)}      ;AC RESISTANCE
LBP 101 102 {ESR(L,QL,FQ)/OMEGA_0} IC={IC}


L1 102 LSO  {L} IC={IC}      ;CHOKE INDUCTANCE

.ENDS LCHOKE


.SUBCKT CQS CSP CSN
+ PARAMS:
+ C=1U
+ QC=10K
+ FQ=60MEG
+ IC=0

.PARAM PI=3.1416
```

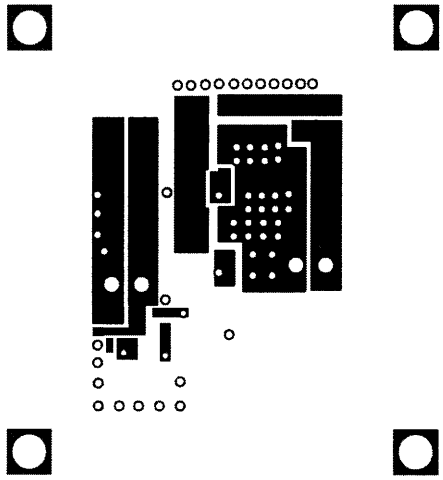
```
.FUNC ESR(C,QC,FQ) {1/(2*PI*FQ*C*QC)}

C1 CSP  101 {C}  IC={IC}      ;SERIES RESISTANCE
R1 101 CSN  {ESR(C,QC,FQ)}    ;SERIES CAPACITANCE

.ENDS CQS


.SUBCKT SICMOS19193E15NLC   GATE DRAIN SOURCE
+ PARAMS:
+ RDSON=0.98
+ RG=0.67
+ CGS=498.569821344P
+ RSHUNT=120MEG
+ CJO=231.8112972P
+ VCCAP=300
+ M=0.49942464614589
+ VJ=2.09239340510056
+ KR=0.15 ;FACTOR

RDMAIN DRAIN DMAIN  {RDSON}
RSHUNT DRAIN SOURCE {RSHUNT}

SW      DMAIN   SOURCE   GMAIN  SOURCE   SWIDEAL
.MODEL SWIDEAL VSWITCH (RON=10m ROFF=1MEG VON=2.5 VOFF=2.4)


*NONLINEAR CAPACITANCE EVALUATED AS A CONTROLLED CURRENT
*SOURCE

GCNL  N101 DRAIN VALUE={IF((V(DRAIN)-V(N101))<0,CJO*V(201)*(1/LDER),
+IF((V(DRAIN)-V(N101))<VCCAP,V(201)*(1/LDER)*(CJO/((1+((V(DRAIN)-V(N101))/VJ))**M)),
+V(201)*(1/LDER)*(CJO/((1+((VCCAP)/VJ))**M))))}
*+CCAP*V(201)*(1/LDER)))}


RCOUT N101   SOURCE {KR*RDSON}

RG  GATE GMAIN    {RG}
CGS GMAIN 0 {CGS}
```

```
****SUBCIRCUIT TO EVALUATE THE DERIVATIVE***

*PARAMETERS AND DEFINITION FOR THIS SUBCIRCUIT
.PARAM:
+ LDER=.01U     ;INDUCT FOR THE DERIVATIVE SUBCIRCUIT
+ PI=3.1416

*FUNC. FOR R OF THE DERIVATIVE SUBCIRCUIT

.FUNC RDER(LDER,FS) {3000*2*PI*FS*LDER}

GY 0 201 VALUE={V(N101)-V(DRAIN)}
L1 201 0 {LDER}
R1 201 0 {RDER(LDER,FS)}

.ENDS SICMOS19193E15NLC


.SUBCKT DNLCFD A K
+ PARAMS:
+ LDS=3.7668N  ;SERIES INDUCTANCE
+ VDON=0.4  ;DIODE FORWARD DROP
+ CJO=998.7P
+ VJ=0.5201
+ M=0.4783
+ FS=100MEG


*PARASITIC LEAD INDUCTANCE
LDS    A    101  {LDS}  IC=0

*IDEAL DIODE MODEL
DIDEAL 101  102  IDEAL
.MODEL IDEAL D(N=0.001)

*FORWARD VOLTAGE DROP MODEL
VDON   102  K    {VDON}

*NONLINEAR CAPACITANCE EVALUATED AS A CONTROLLED CURRENT
*SOURCE
```

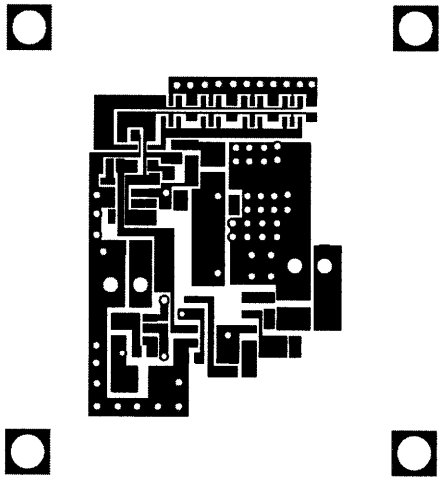
```
GCNL  K 101 VALUE={IF((V(K)-V(101))<0,CJO*V(201)*(1/LDER),V(201)*(1/LDER)*(CJO/((1+(


****SUBCIRCUIT TO EVALUATE THE DERIVATIVE***

*PARAMETERS AND DEFINITION FOR THIS SUBCIRCUIT
.PARAM:
+ LDER=1U     ;INDUCT FOR THE DERIVATIVE SUBCIRCUIT
+ PI=3.14159265

*FUNC. FOR R OF THE DERIVATIVE SUBCIRCUIT
.FUNC RDER(LDER,FS) {3000*2*PI*FS*LDER}
GY 0 201 VALUE={V(K)-V(101)}
L1 201 0 {LDER}
R1 201 0 {RDER(LDER,FS)}

.ENDS DNLCFD
*$
```

Appendix B

PCB Layout Masks and Schematics

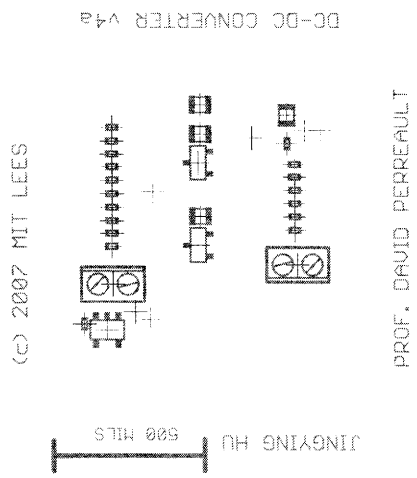


(a) PCB Top copper

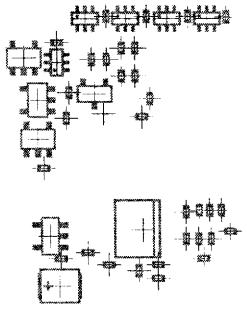


(b) PCB Bottom copper

Figure B.1: **Prototype Board layout masks**

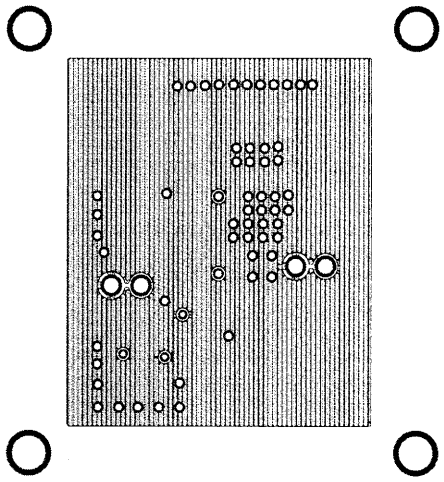


(a) PCB Top silkscreen

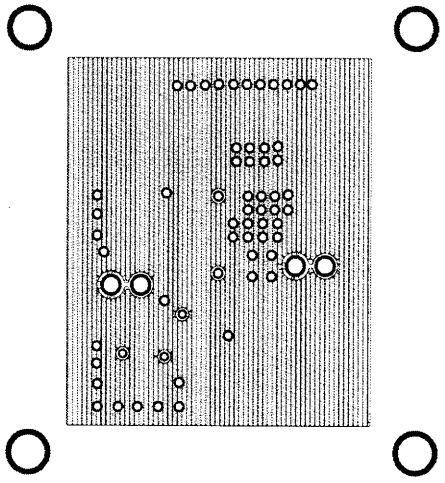


(b) PCB bottom silkscreen

Figure B.2: **Prototype board layout masks**



(a) PCB Route2



(b) PCB Route3

Figure B.3: **Prototype board layout masks**

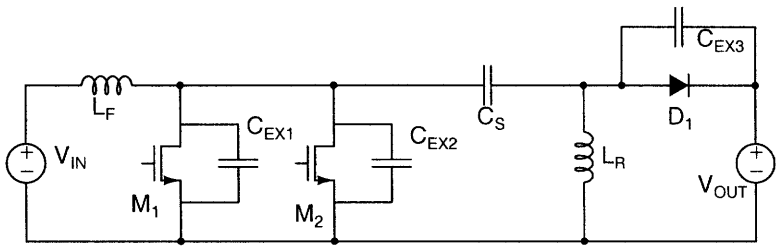


Figure B.4: **Final schematic of the quasi-resonant SEPIC converter implemented with commercial MOSFETs**

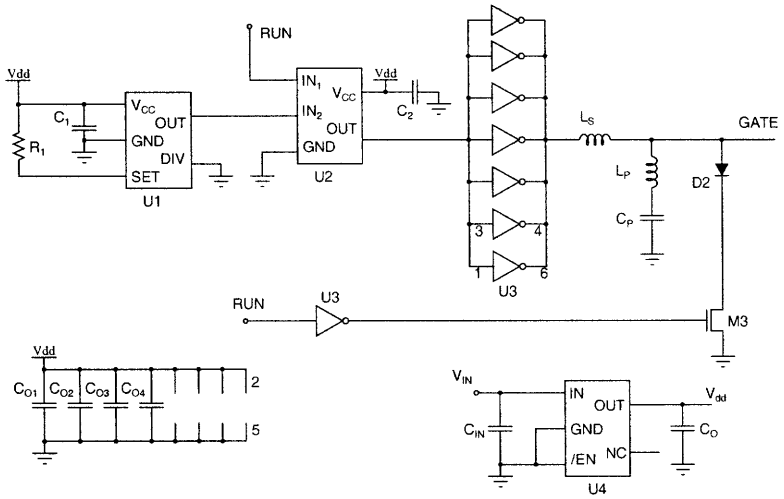


Figure B.5: **Complete gate drive schematic.**

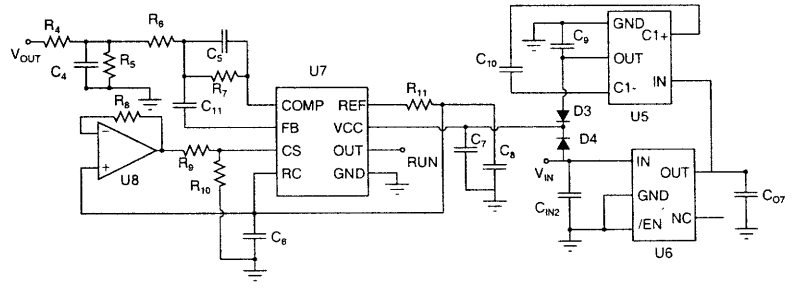


Figure B.6: **Complete control schematic.**

Component	Value	Package	Part No.	Manufacturer
L_F	$22nH$	Mini-Spring	B07T L L	Coilcraft
C_{EX1}	$390pF$	0.055" × 0.055"	ATC700A391JW	ATC
C_{EX2}	$390pF$	0.055" × 0.055"	ATC700A391JW	ATC
L_R	$43nH$	Mini-Spring	B10T L	Coilcraft
C_{EX3}	$100pF$	0.055" × 0.055"	ATC700A101JW	ATC
C_S	$1000pF$	0.055" × 0.055"	ATC700A102JW	ATC
	$270pF$	0.055" × 0.055"	ATC700A271JW	ATC
D_1	30V, 2A	$POWERDI^{TM}$ 123	DFLS230L	Diodes,Inc
M_1	30V	SOT-23	SPN1443	Sync Power
M_2	30V	SOT-23	SPN1443	Sync Power

Table B.1: **Component values and part numbers for SEPIC converter prototype**

Component	Value	Package	Part No.	Manufacturer
$U1$	Oscillator	SOT-23	LTC1799	Linear Technology
$U2$	AND Gate	SOT-23	NC7SZ08	Fairchild
$U3x4$	CMOS Inverter	SC70	NC7WZ04	Fairchild
$U4$	Linear Regulator	SOT-23	TPS76933	Texas Instruments
C_1,C_2,C_{O4}, C_{O3}	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_{O2},C_O,C_{O1}	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_{IN}	$4.7\mu F$	6032-28	TPSC475K035R0600	AVX
	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
R_1	$4.7k\Omega$	0603	ERJ-3GEYJ472V	Panasonic
L_S	$110nH$	0603	0603CS-R11X	Coilcraft
L_P	$72nH$	0603	0603CS-72NX	Coilcraft
C_P	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
$D2$	20V, 100mA	SSSMINI2	MA27D27	Panasonic
$M3$	25V, 680mA	SOT-23	FDV303N	Fairchild

Table B.2: **Component values and part numbers for gate drive circuit**

Component	Value	Package	Part No.	Manufacturer
$U5$	Voltage Doubler	SOT-23	MAX1683	Maxim
$U7$	PWM chip	SO-8	UCC2813	Texas Instruments
$U8$	High Speed Amplifier	SO-8	MAX9003	Maxim
$U6$	Linear Regulator	SOT-23	TPS76925	Texas Instruments
C_{O7},C_{10}	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_9	$3.3\mu F$	0603	TPCL335K010R5000	AVX
C_{IN2}	$4.7\mu F$	6032-28	TPSC475K035R0600	AVX
	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_4,C_{11}	$5pF$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_5	$1nF$	0603	LD03ZC102KAB2A	AVX
C_6	$100pF$	0603	ECJ-2VC1H101J	Panasonic
C_7	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
C_8	$0.1\mu F$	0603	UMK107BJ104KA-T	Taiyo Yuden
R_4	$22k\Omega$	0603	ERJ-3GEYJ223V	Panasonic
R_5	$8.2k\Omega$	0603	ERJ-3GEYJ822V	Panasonic
R_6	$10k\Omega$	0603	ERJ-3GEYJ103V	Panasonic
R_7	$30k\Omega$	0603	ERJ-3GEYJ303V	Panasonic
R_8	100Ω	0603	ERJ-3GEYJ101V	Panasonic
R_9	$30k\Omega$	0603	ERJ-3GEYJ303V	Panasonic
R_{10}	$30k\Omega$	0603	ERJ-3GEYJ203V	Panasonic
R_{11}	$56k\Omega$	0603	ERJ-3GEYJ563V	Panasonic
$D4$, $D3$	20V, 100mA	SSSMINI2	MA27D27	Panasonic

Table B.3: **Component values and part numbers for controller circuit**

Bibliography

[1] J.G. Kassakian, M.F. Schlecht, and G.C. Verghese. *Principles of Power Electronics.* (Addison-Wesley), NY, 1991.

[2] Joshua W. Phinney. *Multi-resonant Passive Components for Power Conversion.* Ph.D. Thesis, Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA., June 2005.

[3] Anthony D. Sagneri. The design of a very high frequency dc-dc boost converter. Master's thesis, Massachusetts Institute of Technology, February 2007.

[4] James Warren, III. Cell-modulated resonant dc/dc power converter. M. Eng. Thesis, Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA., August 2005.

[5] J.M. Rivas, J. Shafran, R.S. Wahby, and D.J. Perreault. New architectures for radio-frequency dc/dc power conversion. In *35th Annual IEEE Power Electronics Specialists Conference Proceedings*, pages 4074–4084, June 2004.

[6] Juan. M. Rivas, Yehui Han, Olivia Lietermann, Anthony Sagneri, and David J. Perreault. A high-frequency resonant inverter topology with low voltage stress. In *IEEE Power Electronics Specialist Conference 2007*, June 2007.

[7] J.M. Rivas, D. Jackson, O. Leitermann, A.D. Sagneri, Yehui Han, and D.J. Perreault. Design considerations for very high frequency dc-dc converters. In *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, pages 1–11, 18-22 June 2006.

[8] N.O. Sokal and A.D. Sokal. Class E—a new class of high-efficiency tuned single-ended switching power amplifiers. *IEEE Journal of Solid-State Circuits*, SC-10(3):168–176, June 1975.

[9] Nathan O. Sokal. Class-E RF Power Amplifiers. *QEX*, pages 9–20, Jan/Feb 2001.

[10] R. Redl and N.O. Sokal. A new class-e dc/dc converter family with reduced parts count: Derivation, topologies, and design considerations. In *Technical Papers of*

the Fourth International High Frequency Power Conversion Conference, pages 395–415, 1989.

[11] R. Redl and N.O. Sokal. A 14 MHz 100 Watt class E resonant converter: Principles, design considerations, and measured performance. In *17th Annual IEEE Power Electronics Specialists Conference Proceedings*, pages 68–77, June 1986.

[12] R.J. Gutmann. Application of RF circuit design principles to distributed power converters. *IEEE Transactions on Industrial Electronics and Control Instrumentation*, IEC127(3):156–164, 1980.

[13] M. Iwadare, S. Mori, and K. Ikeda. Even harmonic resonant class e tuned power amplifier without rf choke. In *Electronics and Communications in Japan*, volume 79, pages 23–30, Jan. 1996.

[14] J.J. Jozwik and M.K. Kazimierczuk. Analysis and design of class-e dc/dc converter. *Industrial Electronics, IEEE Transactions on*, 37(2):173–183, April 1990.

[15] H. Koizumi, Iwadare M., and Mori S. Class e^2 dc/dc converter with second harmonic resonant class e inverter and class e rectifier. In *Thirs Annual Applied Power Electronics Conference Proceedings*, pages 1012–1018, 1994.

[16] H. Koizumi, H. Sekiya, M. Matsuo, S. Mori, and I. Sasae. Resonant dc/dc converter with class de inverter and class e rectifier using thinned-out method (deleting some of the pulses to the rectifier). *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on]*, 48(1):123–126, Jan. 2001.

[17] Juan M. Rivas. *Radio Frequency dc-dc Power Conversion.* PhD thesis, Massachusetts Institute of Technology, September 2006.

[18] Robert. C. Pilawa-Podgurski. Design and evaluation of a very high frequency dc/dc converter. Master's thesis, Massachusetts Institute of Technology, Cambridge, MA, Februrary 2007.

[19] D. Maksimović. A MOS gate drive with resonant transitions. In *22nd Annual IEEE Power Electronics Specialists Conference Proceedings*, pages 527–532, June 1991.

[20] D.M. Van de Sype, A.P.M. Van den Bossche, J. Maes, and J.A. Melkebeek. Gate-drive circuit for zero-voltage-switching half- and full-bridge converters. *IEEE Transactions on Industry Applications*, 38(5):1380–1388, Sept./Oct. 2002.

[21] I. D. de Vries. A resonant power MOSFET/IGBT gate driver. In *17th Annual IEEE Applied Power Electronics Conference Proceedings*, volume 1, pages 179–185, 2002.

[22] K. Yao and F.C. Lee. A novel resonant gate driver for high frequency synchronous buck converters. *IEEE Transactions on Power Electronics*, 17(2):180–186, March 2002.

[23] J.M. Rivas, R.S. Wahby, J.S. Shafran, and D.J. Perreault. New architectures for radio-frequency dc/dc power conversion. In *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, volume 5, pages 4074–4084Vol.5, 20-25 June 2004.

[24] Robert C.N. Pilawa-Podgurski, Anthony D. Sagneri, Juan M. Rivas, David I. Anderson, and David J. Perreault. Very high frequency resonant boost converters. In *Power Electronics Specialist Conference Proceedings*, June 2007.

[25] James R Warren, III, Kathryn A. Rosowski, and David J. Perreault. Transistor selection and design of a VHF dc-dc power converter. *IEEE Transactions on Power Electronics*, Vol.23 No. 1, January 2008.

[26] Y.S. Lee and Y.C. Cheng. A 580 khz switching regulator using on-off control. *Journal of the Institution of Electronic and Radio Engineers*, 57(5):221–226, September/October 1987.

[27] Juan M. Rivas. *"Radio Frequency dc-dc Power Conversion"*. PhD thesis, Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, September 2006.

[28] Wei Gu. Designing a sepic converter. National Semiconductor Application Note 1484, June 2007.

[29] W.A. Tabisz and F.C.Y. Lee. Zero-voltage-switching multiresonant technique-a novel approach to improve performance of high-frequency quasi-resonant converters. *Power Electronics, IEEE Transactions on*, 4(4):450–458, Oct. 1989.

[30] R.W. Erickson and D. Maksimović. *Fundamentals of Power Electronics.* (Kluwer Academic Publishers), Norwell, MA, 2000.

[31] F.C. Lee. High-frequency quasi-resonant converter technologies. In *Proceedings of the IEEE*, volume 76, pages 377–390, April 1988.

[32] W.A. Nitz, W.C. Bowman, F.T. Dickens, F.M. Magalhaes, W. Strauss, W.B. Suiter, and N.G. Zeisse. A new family of resonant rectifier circuits for high frequency DC-DC converter applications. In *Third Annual Applied Power Electronics Conference Proceedings*, pages 12–22, 1988.

[33] R.J. Gutmann and J.M. Borrego. Power combining in an array of microwave power rectifiers. *IEEE Transactions on Microwave Theory and Techniques*, MTT-27(12):958–968, Dec. 1979.

[34] Yehui Han, Olivia Leitermann, David A. Jackson, Juan M. Rivas, and David J. Perreault. Resistance compression networks for resonant power conversion. In *IEEE 36th Annual Power Electronics Specialists Conference Proceedings*, pages 1282–1292, June 2005.

[35] W.L. Everitt and G.E. Anner. *Communications Engineering.* (McGraw-Hill), New York, third edition, 1956.

[36] Z. Shen, D. Okada, F. Lin, S. Anderson, and X Cheng. Lateral power mosfet for megahertz-frequency, high-density dc/dc converters. *IEEE Transactions on Power Electronics*, Vol.21 No. 1, January 2006.

[37] Philip R Geffe. The design of single-layer solenoids for rf filters. *Microwave Journal*, December 1996.

[38] P.N. Murgatroyd. Optimal designs for multilayer air-cored toroidal inductors with circular windows. *IEE Proceedings*, Vol.135, September 1988.

[39] M. Thompson. On the optimization of planar spiral inductor geometries.

[40] R. Chaddock. The application of lumped element techniques to high frequency hybrid integrated circuits. In *Conference on Hybrid Microelectonics (pp. 209-220)*, 1973.

[41] X. Huang, K. Ngo, and E. Bloom. Techniques for planar windings with low resistances. In *Tenth Annual Applied Power Electronics Conference and Exposition (Vol.2 pp. 533-539)*, 1995.

[42] M. Adler. A field-theoretical approach to magnetic induction heating of thin circular plates. *IEEE Transactions of Magnetics*, Vol. Mag-10, No. 4:pp. 1118–1125, December 1974.

[43] D. Daly, S. Knight, M. Caulton, and R. Ekholdt. Lumped elements in microwave integrated circuits. *IEEE Transactions on Microwave Theory and Techiniques*, vol. MTT-15, no. 12:pp. 713–721, December 1967.

[44] Thomas H. Lee. *The Design of CMOS Radio-Frequency Integrated Circuits.* Cambridge, 2004.

[45] Francis Grover. *Inductance Calculations.* New York: Dover, 1946.

[46] D. Schieber. On the inductance of printed spiral coils. Archiv fur Elektrotechnik, 1985.

[47] H.A. Wheeler. Simple inductance formulas for radio coils. *Proceedings of the I.R.E.*, October 1928.

[48] R. Redl, B. Molnar, and N.O. Sokal. Class E resonant regulated dc/dc power converters: Analysis of operations and experimental results at 1.5 MHz. *IEEE Transactions on Power Electronics*, PE-1(2):111–120, April 1986.

[49] W.C. Bowman, J.F. Balicki, F.T. Dickens, R.M. Honeycutt, W.A. Nitz, W. Strauss, W.B. Suiter, and N.G. Zeisse. A resonant dc-to-dc converter operating at 22 megahertz. In *Third Annual Applied Power Electronics Conference Proceedings*, pages 3–11, 1988.