Circuit Designs for the MAP Chip

by

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Submitted to the Department of Electrical Engineering and Computer Science
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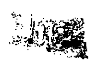

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Abstract

This thesis describes some of the many circuit-level designs included in the M-Machine Multi-ALU Processor (MAP Chip). Standard cells have been created or modified to reduce the area and propagation delay of synthesized logic. The global clock distribution system has been designed at the circuit level and preliminary simulations performed. The Local Translation Lookaside Buffer (LTLB), consisting of SRAM arrays and standard cell logic, has been implemented using components similar to those in other MAP Chip memory arrays.

Thesis Supervisor: William J. Dally
Title: Professor

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The M-Machine project has been an extremely challenging and instructive experience, and the most valuable professional experience I have encountered thus far. Thanks to Bill Dally for bringing me in to the group and providing a vast amount of knowledge and guidance. Thanks to all the M-Machiners for making this a great project.

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Chapter 1

Introduction

1.1 Overview

The M-Machine is an experimental multicomputer being developed at the Massachusetts Institute of Technology. It will be used to investigate methods for parallelism, efficient and innovative uses of high-performance integrated circuit technology, and to support experimental parallel software. It is organized as a three dimensional mesh of nodes, each containing a Multi-ALU Processor (MAP) and conventional DRAM.

This thesis describes some of the many circuit-level design efforts that contibute to the MAP Chip, including standard cells, clock distribution, and implementation of the LTLB memory array.

1.1.1 The M-Machine

One goal of the M-Machine architecture is to efficiently utilize DRAM, which typically occupies the vast majority of silicon area in the system. In contrast to conventional designs where a large amount of memory is dedicated to a single processor, each M-Machine node contains 8MB of DRAM[6].

The MAP Chip includes three execution clusters, network and memory subsystems. Execution clusters on the MAP Chip are analogous to RISC microprocessor cores, each being a a 64-bit three-issue, fully pipelined microprocessor. Memory requests are issued over the M-Switch, and the C-Switch carries inter-cluster communications and return data from the memory system. The MAP Chip has a target cycle time of 10 nanoseconds, corresponding to 100MHz.

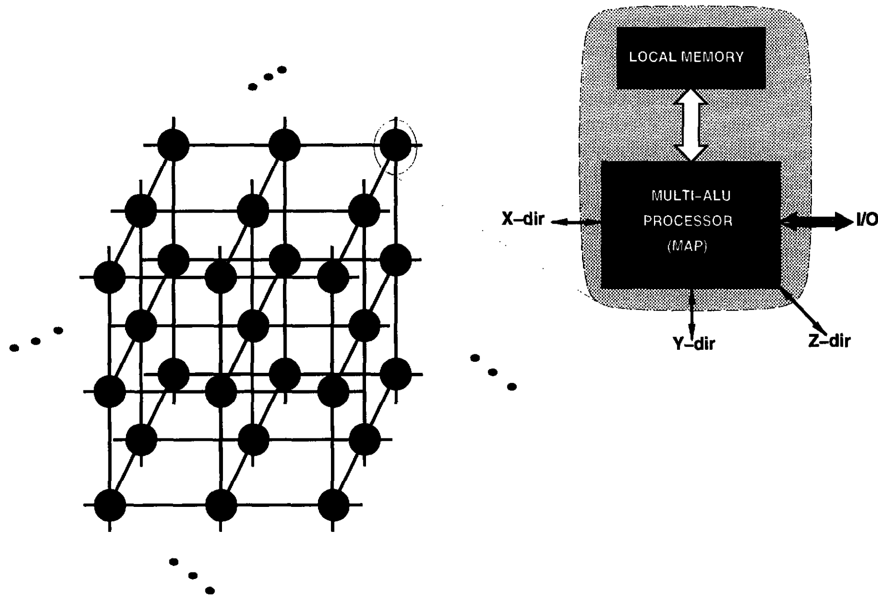


Figure 1-1: M-Machine Architecture

1.1.2 Outline

Modules in the MAP Chip are divided into control and datapath sections. Generally, datapaths are time-critical and include full-custom circuit design. Control logic and less-critical circuits will be synthesized from standard cells. A set of latches suitable for the M-Machine diagnostic methodology has been developed [3]. A static latch cell (register cell) similar to the classic six-transistor SRAM cell is used in small arrays including network queues. Large-sized cells with stronger output drive have been designed to reduce propagation delays, and the need for buffering, in synthesized logic.

Clock distribution is a challenging design task for the MAP Chip. Special attention to signal distribution is necessary because of the its large die size and high clock speed. Differential reference signals are carried by a tree structure with three levels of buffering. A final stage of pulse-generator buffers drive CLK and CLK_L signals onto wire grids that span the chip. Latches and other clock loads are connected to the grids.

The Local Translation Lookaside Buffer (LTLB) translates virtual addresses to physical addresses for data stored in an M-Machine node. It contains 128 entries, each representing the translation for a 4KB page of data. The LTLB also stores status information for the 64-byte data blocks within each page.

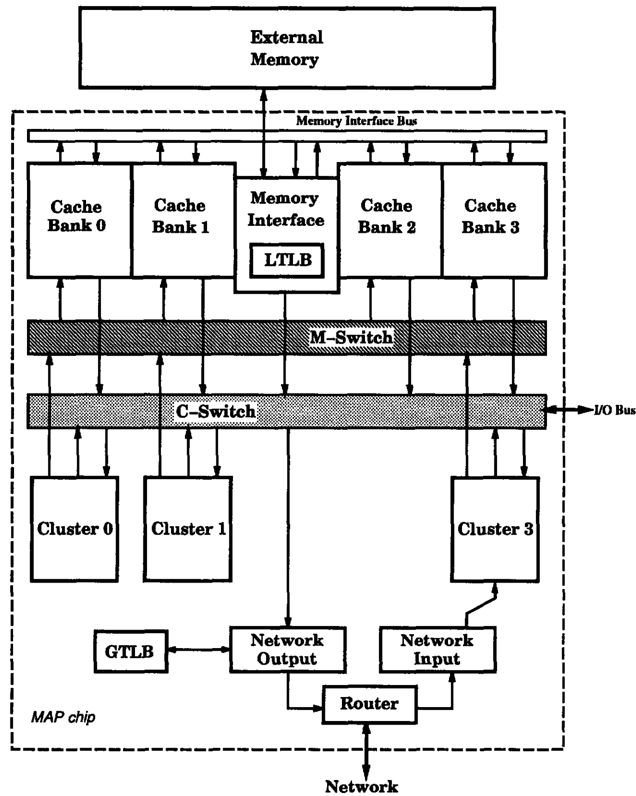


Figure 1-2: MAP Chip Architecture

The LTLB is similar in construction to the other MAP Chip memory arrays. It includes SRAM arrays, support circuitry, and datapath elements such as comparators and multiplexers. The major challenges of implementing the LTLB are generation and distribution of time-critical signals for the SRAM arrays, and design of standard-cell based logic incorporated into the LTLB module.

Chapter 2

Standard Cells

2.1 Introduction

A standard cell design methodology greatly eases the task of circuit design in applications where circuit speed and area can be traded for ease of implementation. The MAP Chip uses standard cells to create control logic, small memory arrays, and other logic which is not on critical timing paths. New cells have been added to the standard cell library. These include scannable latches for the M-Machine diagnostic methodology, an SRAM-like register cell, and logic gates with large device sizes.

2.2 Latches

2.2.1 Introduction

The MAP chip standard cell library includes three latch cells: a positive edge-triggered flip-flop (PDFF), positive transparent latch (PLTCH), and negative transparent latch (NLTCH). These are staticized versions of the basic CMOS passgate-inverter latch, as shown in figure 2.1, with scan capability added.

The ability to set and examine the internal state of the MAP chip at a given clock cycle is a valuable tool for testing, debugging, and verification purposes. This can be accomplished with the use of scannable latches.

In the M-Machine diagnostic system architecture, the flip-flop and negative latch are scannable. These cells include two datapaths and clock signals: one for normal operation and one for scanning. The normal datapath and clock control the flow of signals through

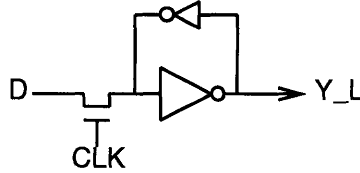


Figure 2-1: *MAP Chip positive latch.*

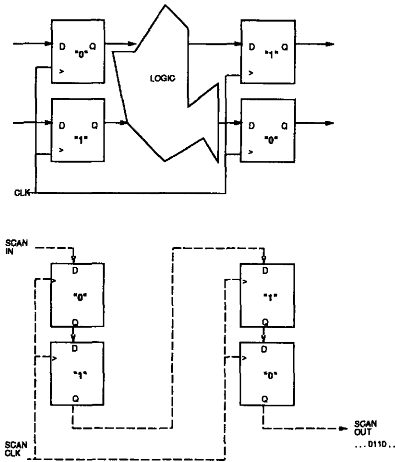


Figure 2-2: *Scannable registers, illustrating normal and scan operation.*

logic circuits. The scan path connects groups of latches into shift registers which can be shifted in or out using the scan clock. The concept is illustrated in figure 2-2. The MAP chip will include multiple scan chains, controlled and accessed through the diagnostic port, as shown in figure 2-3. The diagnostic port will handle multiplexing of scan chain inputs and outputs, and generate the necessary control and clock signals for proper latch function.

2.2.2 Circuit Designs

During a scan operation, it is important that the data outputs of latches remain at constant and valid values. For example, if a latch outputs control large devices such as bus drivers, an invalid combination of values could cause excess power dissipation or physical damage to the chip.

Two possible solutions are to force outputs to a default value during scan, or for the latches to hold their last output values from immediately before the scan operation started. Cells to support the default value methodology would be simple to design. Conceptually,

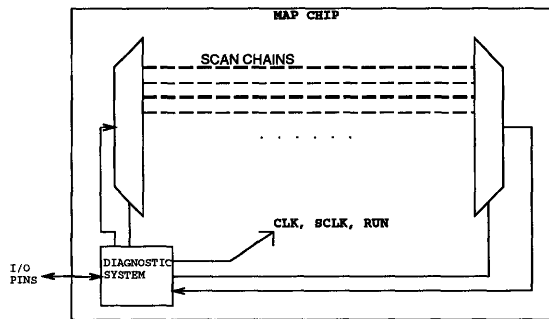


Figure 2-3: *High-level design of the MAP Chip Scannable Paths.*

the cells could be seen as an ordinary latch connected to a 2:1 multiplexer. The multiplexer would select between the latch value and a constant determined by its other input. However, this would require manual definition of a default value for every scannable latch on the chip.

Latches that hold their last valid output value during scan are easier for logic designers to use because they do not require attention to default values. However, isolation of the data output from the rest of the latch increases the size of these cells.

The required functions for the scannable cells are:

- Cell behaves like ordinary latch or flip-flop.
- Cell copies current state to scan output during normal operation.
- Cell behaves like positive edge-triggered shift register for scan path; data output remains at its last valid value.
- Cell copies scanned-in data to current state when scanning operation is finished.

The control signals for the PDFF and NLTCH cells are system clock, scan clock, and mode select (CLK, SCLK, and RUN, respectively). Symbolic representations of the cells are shown in figure 2-4. Complementary clock signals (CLKN and SCLKN) are created internally to reduce the number of signals that require global routing.

Because of limitations of the support hardware that will test the MAP Chip, it is desirable that scan operations run slower than the normal system clock frequency. The target system clock speed is 100MHz, and scan clock is expected to run at 10MHz. A separate scan clock is used because it allows system and scan clock frequencies to be completely independent. The main drawback is that it requires two gated clock signals to be distributed

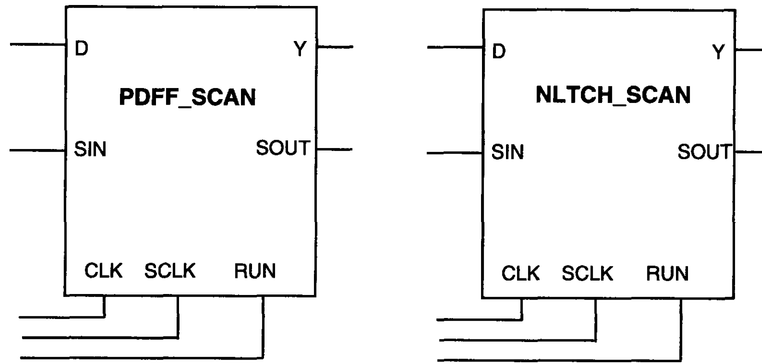


Figure 2-4: *Block diagrams of PDFF_SCAN and NLTCH_SCAN*

throughout the chip.

Latch designs that used system clock and two independent control signals were also evaluated. This interface reduces the number of time-critical signals that need to be routed. However, it increases the complexity of using different clock speeds for normal operation and scanning.

2.2.3 Implementation

Schematic diagrams of the new latch cells, PDFF_SCAN and NLTCH_SCAN, can be found in Appendix A. The cells are similar in high-level design, although device sizes are optimized for different functions.

NLTCH_SCAN

During normal operation, data passes from the D input through the complementary passgate when CLK is low. This passgate and the middle inverter form an inverting negative-transparent latch. From the middle inverter, data propagates through the RUN passgate and the output inverter. The passgate to SIN is normally opaque and the passgate between midout and SOUT transparent, thus SOUT is also a negative-latched copy of the D input.

NMOS-only passgates reduces the number of control signals within the latch cells. The passgates at the D and SIN inputs are complementary because node 'midin' is dynamic. Good signal transmission for both high and low values is necessary to create rail-to-rail voltage swing at this node. Use of a PMOS pass device with keeper would provide the same functionality, but also allow the the cell to drive a signal backwards through its unbuffered

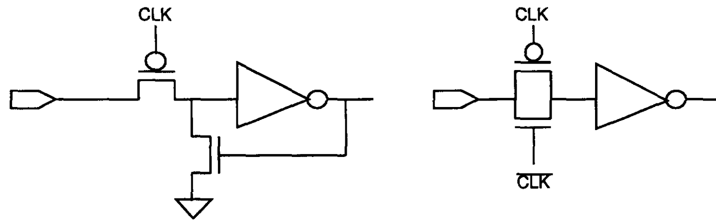


Figure 2-5: *PMOS with keeper vs. complementary passgate*

inputs. These circuits are illustrated in figure 2-5

During scan, the D input passgate and Y-output passgate are opaque. The output inverter and feedback inverter are isolated from the rest of the cell, and the Y-output retains its last valid data value. The SIN passgate and middle inverter form a negative-transparent latch, controlled by SCLK. The SOUT passgate and the SOUT output inverter form a positive-transparent latch controlled by SCLK. The latch cell acts as a positive edge-triggered flip-flop for the scan path.

PDFF_SCAN

In the PDFF_SCAN cell, the D and SIN passgates and middle inverter form negative-transparent latches controlled by CLK and SCLK, respectively.

The passgate between the middle inverter and the output inverter forms a positive-active latch, controlled by a gated clock signal. During normal operation, RUN is high and the passgate is transparent when CLK is high. RUN is held low during scanning, the passgate remains opaque, and the output inverter and keeper are isolated from the rest of the cell.

Use of a CLKA-style circuit to gate the system clock instead of a standard AND gate significantly reduces the propagation delay of PDFF_SCAN. For comparison purposes, simulations were run with input signals having 400ps edge times. The CLKA used in the PDFF_SCAN cell has a propagation delay for CLK of 60ps. This compares to over 200ps for a NAND gate and inverter.

In PDFF_SCAN, the inverter that creates CLKN is asymmetric because the critical transition is CLKN falling. Reducing the size of the PMOS transistor also reduces the clock load of the register.

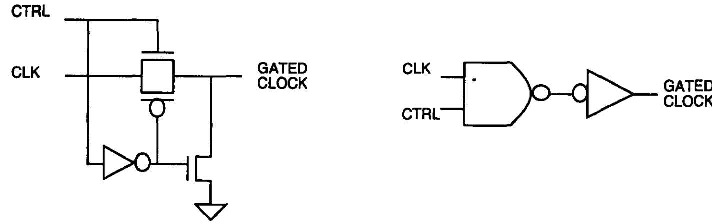


Figure 2-6: *Two methods for generating a gated clock.*

2.2.4 Usage

The PDFF and NLTCH cells share the same control signals. For normal operation, SCLK and RUN are held high while CLK toggles. SOUT will follow node 'midin', which is a negative-latched version of D.

In scan mode, CLK is held high. SCLK toggles, and RUN is low to isolate the Y-output from the rest of the circuit.

To change from normal to scan mode:

- CLK stops in and remains in the high state.
- RUN remains high for at least Tcq after the last rising edge of CLK, then falls. This delay allows the correct data value to propagate to X before the RUN passgate closes.
- After RUN falls, SCLK falls. Data from the scan path propagates to the middle inverter.
- At least one SCLK period after the last falling edge of CLK, SCLK begins to toggle. (constraint for NLTCH_SCAN)

To change from scan to normal mode:

- SCLK stops and remains in the high state.
- RUN rises. Y changes immediately to reflect the last scanned value.
- At least one SCLK period after the last rising edge of SCLK, CLK begins to toggle. The value at SOUT changes immmediately after the falling edge of CLK.

The maximum idle time for the latches is determined by the charge storage properties of the dynamic nodes, and the required level of noise immunity. Figures 2-7 and 2-8 illustrate the timing of the new latch cells.

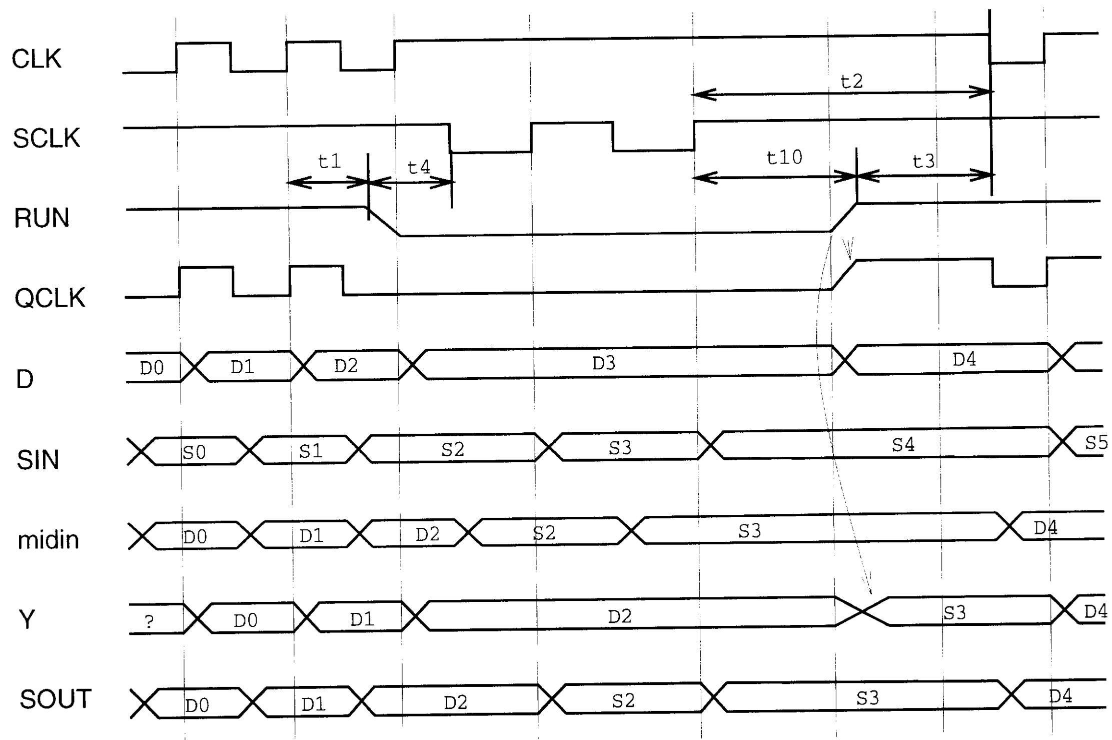


Figure 2-7: *Timing diagram for PDFF_SCAN*

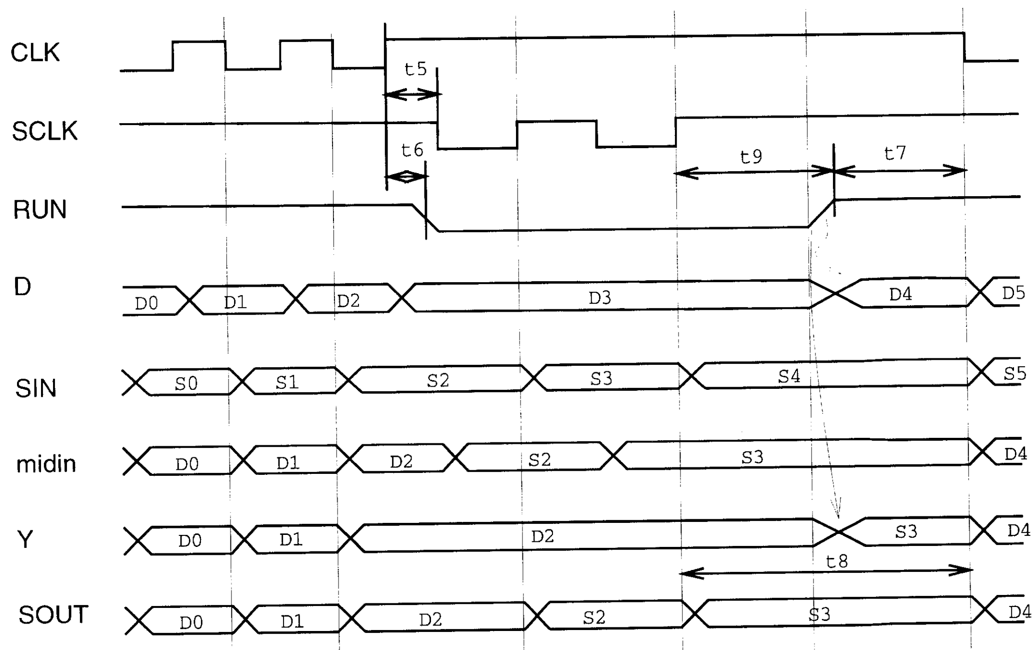


Figure 2-8: *Timing diagram for NLTCH_SCAN*

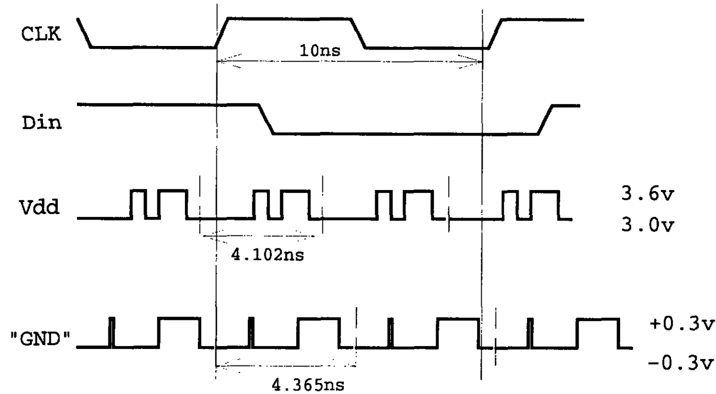


Figure 2-9: Typical waveforms for noise testing

2.2.5 Function

Simulations were initially performed on schematic netlists of the latches. As layout was completed, many tests were repeated using netlists with extracted capacitances from layout.

The cells were optimized for performance at TTL conditions (typical NMOS, typical PMOS, Vdd=3.0v). In addition, they were tested for functionality at the other process corners (SS, SF, FS, FF). The following configurations were checked for ****************** race-through and for proper functionality at the process corners. Both data and scan paths have been checked for each configuration.

- Three PDFF_SCANs connected in series.
- A shift-register consisting of seven cells in series: PDFF_SCAN, NLTCH_SCAN, PLTCH, NLTCH_SCAN, PLTCH, PDFF_SCAN, PDFF_SCAN.

Noise

The seven-cell shift register described above was tested with noise added to ground and Vdd. Clock and data inputs were driven so that each register stage would toggle every clock cycle. Meanwhile, various step-function noise was added to Vdd and ground. The simulation was run for approximately 200 clock cycles, and the output checked for signs of failure.

The PDFF_SCAN, NLTCH_SCAN, and PLTCH operate at 100MHz with up to 600mV

peak-to-peak noise on power and ground. The scan path can function with at least 400mV total peak-to-peak noise on power and ground. Below are the results of some noise test simulations:

- DATA with f=111MHz; 300mV noise on Vdd, 300mV noise on GND – pass
- DATA with f=111MHz; 325mV noise on Vdd, 350mv noise on GND – fail
- SCAN with f=100MHz; 200mV noise on Vdd, 200mV noise on GND – pass
- SCAN with f=100, 80, 66MHz; 300mV noise on Vdd, 250mV on GND – fail

Power

HSPICE simulations were used to estimate power consumption by measuring the amount of current drawn from the positive supply. Values for typical process conditions and nominal supply voltage (TTL) are shown below.

Cell	0-1 (pJ)	1-0 (pJ)	toggle @ 100 MHz (uW)
PDFF_SCAN	2.2	1.6	190
NLTCH_SCAN	2.2	1.6	190

Input Load

The PDFF_SCAN and NLTCH_SCAN cells were designed to have small input loads. This reduces the demand on the MAP chip's clock distribution system. The table below provides a comparison between obsolete scannable latch cell designs and the final cells used in the MAP Chip.

Cell	CLK	D	SCLK	SIN
PDFF (old)	39fF	53fF	-	6fF
PDFF_SCAN	27fF	20fF	8fF	15fF
NLTCH (old)	28fF	41fF	-	37fF
NLTCH_SCAN	22fF	33fF	8fF	21 fF

2.2.6 Evaluation

Optimization techniques such as diffusion-sharing and transistor folding were used throughout the physical designs of the latches. The extensive use of passgates reduces the potential for diffusion-sharing, and also increases the complexity of wiring.

The new scannable latch cells incorporate more devices than their predecessors, and are also slightly larger in size. All cells conform to M-Machine standard cell design conventions. Transistor counts and cell sizes are listed below:

Cell	Transistors	Width (tracks)
PDFF	20	18
PDFF_SCAN	23	19
NLTCH	16	16
NLTCH_SCAN	18	17

Timings

To guarantee correct operation, timing constraints exist for some operations of the latch cells. These are described in the following table. Symbols refer to the indicated locations in figures 2.7 and 2.8.

Symbol	Description	Min. Timing
t1	PDFF: Last CLK rising edge to RUN falling	greater than maximum Tcq
t2	PDFF: SCLK rises to first CLK falling edge	1 SCLK period
t3	PDFF: RUN rises first CLK falling edge	1 CLK period
t4	PDFF: RUN falls to SCLK falls	0ps.*
t10	PDFF: SCLK rising edge to RUN rising edge	greater than maximum Tcq
t5	NLTCH: CLK rises to SCLK falls	greater than maximum Tcq
t6	NLTCH: CLK rises to RUN falls	greater than maximum Tcq
t7	NLTCH: RUN rises to CLK falls	0ps.
t8	NLTCH: SCLK rising edge to CLK falling edge	1 SCLK period
t9	NLTCH: SCLK rising edge to RUN rising edge	greater than maximum Tcq

* Note that to prevent contention, CLK and SCLK cannot both be LOW simultaneously.

For the positive edge-triggered flip-flop, Tcqmin is the minimum clock-to-q delay when the data input is stable long before the clock edge. Ts is the time before the rising clock edge that data must be stable so that the clock-to-q delay is less than or equal to Tcqmin + 15ps. This definition is consistent with M-Machine circuit design conventions.

The sum of setup and propagation time is a measure of a register's overall performance, since circuit design can change how the total delay is divided between these two quantities. The following table lists the setup and propagation times for the new cells.

All HSPICE timing measurements are made with the following configuration, unless otherwise noted:

- TTL process corner.
- 90fF load on Y, to simulate four medium-sized gates (4*INV_2).
- 40fF load on Sout.
- All signals measured at 50% points.
- inputs driven by voltage sources with 400ps edge times.

Cell	Transition	Ts (ps)	Tcqmin (ps)	Best sum Ts+Tcq (ps)
PDFF_SCAN	data 0-1	430	510	280+590=870
PDFF_SCAN	data 1-0	130	680	140+680=820
PDFF_SCAN	scan 0-1	540	480	400+570=970
PDFF_SCAN	scan 1-0	310	770	290+790=1080

For negative latches, Tdq is the time necessary for a change in input data to propagate to the output while the latch is transparent. Ts is the minimum time before the rising edge of CLK such that the data-to-output delay of the latch is less than or equal to the minimum Tdq + 15ps.

Cell	Transition	Ts(ps)	Tdq (ps)
NLTCH_SCAN	data 0-1	350	640
NLTCH_SCAN	data 1-0	180	640

Edge times and propagation delays for NLTCH_SCAN at various process corners are shown below. Tcq is the delay between the falling transition of CLK (50%) and the change

in Y to 50% if the input data changed long before the clock edge. For the scan path, Tcq is the delay between the rising edge of SCLK and the corresponding change in SOUT. Tdq is the delay between changing input data and the corresponding change in Y, when the latch is transparent. All times are measured in picoseconds.

Process corners are represented by two or three letter abbreviations where the first letter represents the NMOS device, the second represents the PMOS device, and the third represents power supply voltage (F=fast, S=slow, T=typical, L=low voltage). Power supply voltage is 3.3v for TT, 3.6v for FF, and 3.0v for FS, SF, SS, and TTL.

Cell	Pin	Load	Corner	Tr	Tf	Tcq01	Tcq10	Tdq01	Tdq10
NLTCH_SCAN	Y	0fF	FF	160	100	290	250	310	170
			FS	170	160	500	410	390	390
			SF	180	540	500	710	520	620
			SS	240	270	710	730	630	640
			TT	150	170	460	420	450	380
			TTL	180	190	500	460	480	430
		90fF	FF	260	220	360	320	400	260
			FS	550	330	720	550	610	530
			SF	370	960	640	1090	690	1010
			SS	610	740	930	1060	870	980
			TT	410	380	620	550	620	530
			TTL	460	470	690	640	660	600
		180fF	FF	440	290	440	380	500	320
			FS	900	400	890	610	780	610
			SF	560	1350	760	1420	790	1340
			SS	950	1120	1120	1340	1050	1260
			TT	650	580	740	670	730	650
			TTL	690	660	820	790	790	750

Cell	Output	Load	Corner	Tr	Tf	Tcq01	Tcq10
NLTCH_SCAN	SOUT	40fF	FF	500	410	200	350
			FS	1110	440	570	400
			SF	630	2500	310	1580
			SS	1120	1500	650	1220
			TT	730	710	390	620
			TTL	790	840	460	720

The corresponding measurements for PDFF_SCAN are shown below.

Cell	Output	Load	Corner	Tr	Tf	Tcq01	Tcq10
PDFF_SCAN	Y	0fF	FF	130	180	150	220
			FS	180	220	250	280
			SF	170	610	370	790
			SS	220	350	470	670
			TT	130	260	300	390
			TTL	150	260	320	460
PDFF_SCAN		90fF	FF	300	300	260	330
			FS	570	320	470	410
			SF	390	1170	520	1300
			SS	620	880	730	1080
			TT	410	470	460	570
			TTL	450	550	510	680
PDFF_SCAN		180fF	FF	460	410	350	400
			FS	980	440	670	510
			SF	580	1680	630	1750
			SS	1010	1360	930	1430
			TT	690	660	600	720
			TTL	740	800	660	860

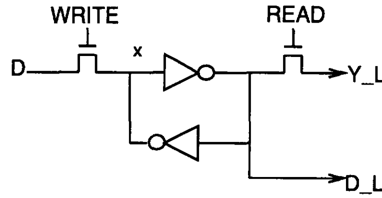


Figure 2-10: *Six-transistor SRAM Cell.*

Cell	Output	Load	Corner	Tr	Tf	Tcq01	Tcq10
PDFF_SCAN	SOUT	40fF	FF	530	410	210	370
			FS	1160	440	600	410
			SF	690	2860	310	1660
			SS	1180	1580	670	1280
			TT	770	730	400	650
			TTL	830	890	470	750

2.3 Register Cell

2.3.1 Background

The MAP chip contains modules with a wide range of information storage needs. When few bits need to be stored, standard-cell registers may be used. This is easy to design, but is costly in terms of circuit area. For very large arrays such as the on-chip L1 cache, SRAM arrays and analog support circuitry are used. SRAM-based arrays approach allows very dense information storage, but involves analog design. As an intermediate solution for small arrays, a *register cell* has been designed.

The register cell is a six-transistor cross-coupled inverter circuit, typical of ASIC memories [10]. In the MAP chip, it will be used as a two-port (one write, one read), single-ended cell. The write-bit lines are driven by standard cell inverters. During reads, bit-line voltage swing will be approximately 2 volts, and a ratioed CMOS inverter will sense the state of the bitline. The physical layout will follow standard cell conventions to ease the design of the arrays.

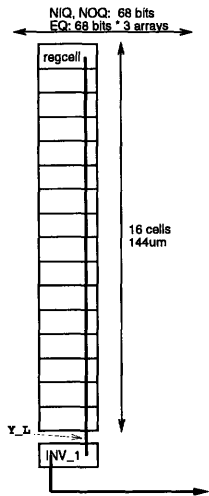


Figure 2-11: *Arrays of the register cell used in queues.*

2.3.2 Design

The message subsystem of the MAP chip includes register files and queues which are implemented as memory arrays. The storage element for these arrays is the register cell (REG_CELL), a six-transistor static latch configured with single ended read and write ports. The cell is shown in figure 2-10.

The SRAM cell is asynchronous, responding immediately to the control signals read and write. When WRITE is asserted, the the value held in the cross-coupled inverters is forced to the value at input pin D. This assumes that the D input is driven strongly by low-impedance devices. When WRITE is deasserted, the cell will hold its current value. To read the value from a cell, READ is asserted, allowing the cell to drive the bit line. When

READ is deasserted, the output is in high-impedance state.

In addition to a tri-state output, the register cell also has a pin allowing access to an internal storage node. This is used in the GTLB array to support logic for pattern-matching. Note that adding capacitive load to this node may increase the time needed to write to the register cell.

The register cell is used in several different systems, including the GTLB, network input and output queues, network router, and event queue. In all of these arrays, the register cell drives a capacitive load of approximately 80fF, consisting of interconnect, drain, and input gate capacitance.

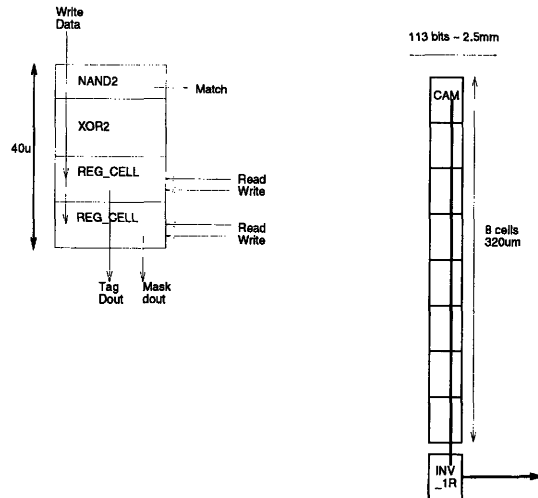


Figure 2-12: *The CAM cell and its arrangment in the GTLB.*

2.3.3 Implementation

To simplify physical implementation, the register cell layout is designed using MAP chip standard-cell conventions. It is five tracks wide to accomodate its five signal pins. Signal pins are arranged so that each signal can be assigned to a seperate horizontal and vertical track. The output is single-ended and will be sensed by a standard CMOS inverter.

Initial estimates indicated that the driving inverter should have an NFET of approximately 3.5, with balanced PFET. Assuming that the READ pass transistor is also 3.5, the worst-case total output load for a 16-cell bitline is 73fF.

Based on the approximation of an ideal fanout of 3 (e=2.7), the driving NFET should have a width of roughly 4-5. In the layout, there is sufficient area for a 3.7 NFET. The width of the PFET is equal to that of the NFET to reduce the switching voltage of the inverter. This is necessary because signals from the input pin passthrough an NFET device and range between ground and Vdd-Vtn. The keeper inverter is implemented as a minimum-size PFET and a minimum width, double length NFET.

Increasing the width of the output pass transistor can improve the read-out speed. However, because a significant part of the bit line load capacitance consists of drain capacitance of these devices, the improvement is small.

Read time is reduced significantly for the '0' case by using a sense inverter (INV_1R) with reduced threshold voltage instead of a standard INV_1. Results of HSPICE simulations

are presented in the following section.

2.3.4 Evaluation

The Cell

The times below are measured with HSPICE at TTL conditions for the circuit in figure 2-11. Inputs are driven by voltage sources with 400ps edge times. Propagation times are from READ signal rising to 50% to the Y output reaching 50%. A capacitive load of 45fF is placed on the output of the sense inverter to simulate a fan-out of four. The sense inverter is a modified INV_1 cell, with PMOS=2.5um, NMOS=5.5um.

Output device size	Total output load	Tpd 0-1	Tpd 1-0
3.7um	70fF	680ps	740ps

The times necessary to write to the cell are shown below. Because of feedback from the keeper-inverter, the load on pin D_L affects the time necessary to write the cell. These simulations were run at TTL conditions, with inputs driven by voltage sources with 400ps edge times. Times are measured from WRITE rising to 50% to the voltage at node x reaching 80% of its final value. Times are measured to node x reaching 80% of final value instead of the midpoint in order to guarantee that the cell will remain stable with the correct data value.

D_L load	write 1	write 0
0fF	930ps	180ps
10fF	1030ps	180ps
20fF	1120ps	180ps
50fF	1390ps	180ps
100fF	1780ps	180ps

When READ is asserted, charge sharing with the bit line causes a voltage spike to appear on the D_L node. At TTL conditions with 70fF of load from the bit line, the '1' voltage dips to 2.2 volts, and the '0' voltage peaks at 0.5v. The keeper inverter has a threshold of Vdd/2 = 1.5v, so noise margins are acceptable for both cases.

In the extreme case, a large bit line load could cause the cell to change state. At TTL conditions with no external load on D_L, this occurs when the bitline load exceeds 600fF. Thus, the maximum safe load is much larger than the load of the arrays.

The table below lists the register cell's performance with varying process conditions. The simulations reflect the configuration shown in Figure 2-11, and measure from READ rising to 50% to Y output reaching 50%.

Corner	Vdd	Read 1	Read 0	Write 1	Write 0
FF	3.6v	440 ps	330 ps	410 ps	80 ps
FS	3.0v	800	400	680	90
SF	3.0v	510	1300	1460	240
SS	3.0v	810	1100	1470	200
TT	3.3v	630	610	780	160
TTL	3.0v	680	740	930	130

The driver inverter is ratioed for a reduced switching threshold. This improves speed by adjusting the threshold to meet the limited voltage output of the NMOS passgate. With a balanced 2/1 ratioed inverter, the cell fails to write a '1' at the slow-N fast-P process corner.

Arrays: Queues

Simulations were performed using driver and receiver circuits, a single active register cell, and capacitive loads to model the the rest of the network queue. The arrangements shown in figures 2-11 and 2-12 were evaluated with standard cell inverters of various sizes used to drive control and data inputs to the array.

The following capacitances were used in the array model to simulate the network input queue, which has the largest capacitive loads of the queue-type structures:

Name	Description	Total (fF)
C1	write-bit line	210
C2	write control	625
C3	read control	650
C4	read-bit line	75
C5	Y output	45
C6	D_L load	0

The estimate for C1 assumes that all write-bit lines of the 16*4 array are connected together and driven by the same inverter.

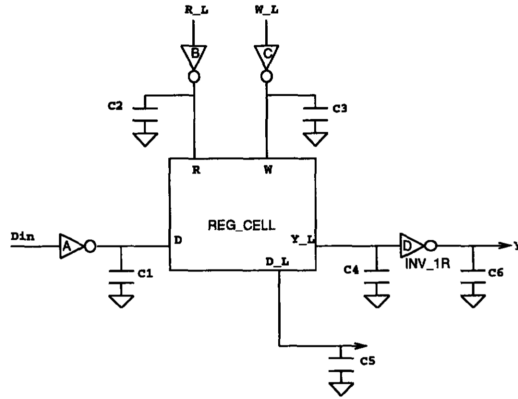


Figure 2-13: *Model for capacitive load of arrays.*

Data and control inputs to the register cell array are driven by standard cell inverters. For the queues, the following sizes were used. Propagation time is measured from when the input signal reaches 50% (Vdd/2) to the output reaching 50%.

Inverter	Standard Cell(s)	Tpd
A	INV_2	450ps
B	INV_8	380ps
C	INV_8	380ps

The following simulation results were obtained using the conditions listed below, unless otherwise noted.

- TTL process corner, Vdd=3.0v
- Inputs (Din, R_L, W_L) are voltage sources with 400ps edge times.
- Layout parasitic capacitances (lpe) are included in the HSPICE models.

Setup time (Ts) is the minimum time between D becoming stable and the falling edge of W to guarantee correct data is written to the register cell. This is measured from D reaching 80% of its final value to W reaching 50%, as shown in figure 2-14. For the queue array, the worst-case setup time (write '1') is 600ps.

Read time is the time between R being asserted and the correct data value appearing at the array's Y-output, measured from R reaching 50% to Y reaching 50% of its final value. Read times are 830ps for '0' and 700ps for '1'.

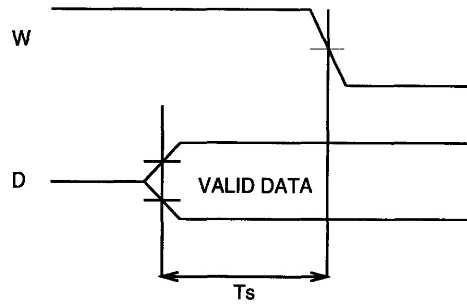


Figure 2-14: Setup time for register cell

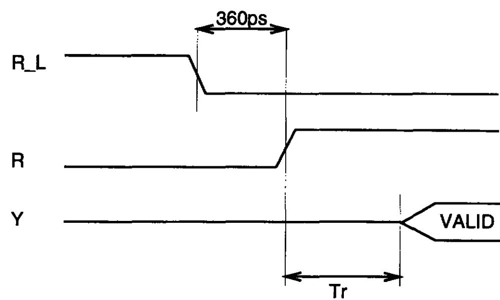


Figure 2-15: *Read time for register cell*

2.3.5 Arrays: GTLB

The following capacitances were used in the array model to simulate the CAM cell array in the GTLB.

Name	Description	Total (fF)
C1	write-bit line	80
C2	write control	1050
C3	read control	1090
C4	read-bit line	80
C5	Y output	45
C6	D_L load	18

Inputs to the arrays are driven by scaled inverters with the following sizes. Inverters for the read and write control signals are connected in parallel to increase drive strength.

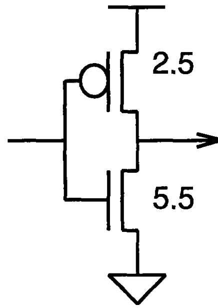


Figure 2-16: *Schematic for INV_1R.*

Inverter	Standard Cell(s)	Tpd
A	INV_4	340ps
B	2 * INV_16	310ps
C	2 * INV_16	340ps

In the GTLB configuration, the minimum setup time is 570ps. Read times for '0' and '1' are 1150ps and 1060ps, respectively.

2.3.6 Low Threshold Inverter

An inverter with reduced switching voltage is used to sense the state of the read-data bitline. All standard cell inverters are sized for a Vdd/2 switching threshold, however the register cell's NMOS-only passgates do not create full-swing output signals. To improve speed and tolerance to process variations, a new cell was created. The new cell, INV_1R, has comparable drive strength to an INV_1, but a lower switching threshold. Its physical design is a simple modification of the INV_1 layout, thus pin locations and overall size are identical.

The new ratio of device sizes results in a threshold of approximately 1.1v at TTL conditions, compared with 1.5v for standard cell inverters. At varying process corners and power supply voltages, the threshold voltage changes as listed below:

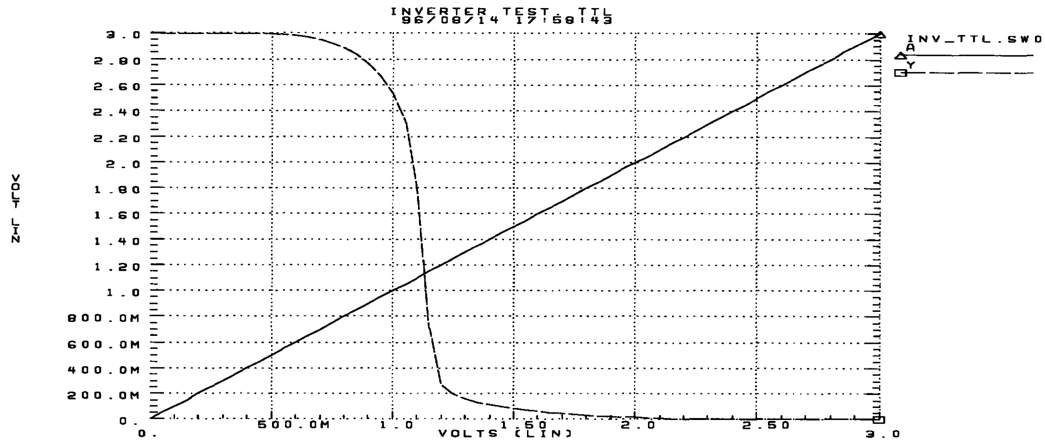


Figure 2-17: *Transfer curve for INV_1R at TTL conditions.*

Corner	Vdd (volts)	Vt (volts)
FF	3.6	1.22
FS	3.0	0.88
SF	3.0	1.38
SS	3.0	1.20
TT	3.3	1.25
TTL	3.0	1.18

2.3.7 Summary

Based on the specifications in CVA Memo #90, "Datapath Proposals for GTLB, NETOUT, NETIN, ROUTER, AND EVENTQ," a physical design for the register cell has been created. A standard cell inverter layout has been modified to produce a sense-inverter with reduced threshold voltage. Layouts have been verified using standard simulation and verification tools.

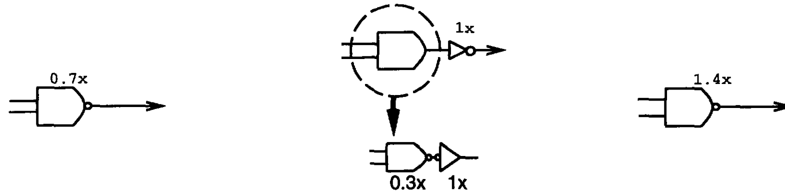


Figure 2-18: *weak NAND, AND with buffer, and proposed NAND_2.*

2.4 Logic Cells

The original standard cell library used to synthesize logic for the MAP chip includes logic gates in only one device size. Only inverters and tri-state inverters are available in a variety sizes to drive large loads. When large fan-out nodes or long runs of interconnect occur, large sized inverters are used to drive the loads. Available sizes for inverters are 1x, 2x, 4x, and 8x, where 1x is the standard output drive of a logic gate with a fan-out of four.

Not all logic gates have full output drive (1x). Due to size and input load constraints, some gates have as little as half of normal output drive. If an output must drive several other gates, it must be buffered using inverters.

An example of buffering using inverters appears in figure 2.18. Suppose the desired output is Y = NAND(A,B). The leftmost picture shows the one-cell implementation (NAND2), which has inadequate drive strength. To remedy this, the NAND gate is implemented as an AND gate and a 2x inverter added as shown in the center. Note that this requires three stages of logic, a large increase from the single-stage NAND gate.

Use of logic gates with larger device sizes can result in significant reductions in propagation delay and/or area. Three double-sized logic gates were designed: two-input AND, NAND, and NOR gates.

The table below lists propagation delays for a 1x-sized inverter driving the logic gate under test and a 20fF load to represent other gates or interconnect capacitance. The gate+inverter combination or 2x-sized gate drives a load of 90fF. Refer to figure 2-19 for a diagram of the test circuit. A plot of the circuit used for timing measurement is included in the appendix. The input load for double-sized gates is double that of the 1x gates. The increased input capacitance affects the propagation delay of the previous output stage, as shown below.

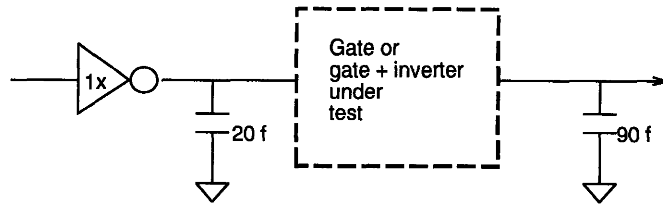


Figure 2-19: *Circuit to evaluate logic gate propagation delay.*

Logic	Inverter Tpd	Logic gate Tpd	Total
NAND + INV_2	185ps	525ps	710ps
AND_2	190ps	545ps	735ps
AND + INV_2	170ps	640ps	810ps
NAND_2	250ps	270ps	520ps

There is little timing difference between the AND_2 and NAND+INV_2. In contrast, the NAND_2 provides a significantly lower delay than the AND+INV_2 combination. This is because the NAND gate contains only one stage of logic while the AND+INV_2 has three: a NAND gate and inverter to make an AND gate, and the 2x-sized inverter.

The double-sized logic gates also use less area than a combination of gate and inverter. This is caused by better device sizing, and efficient physical design. Standard cells have uniform heights, therefore area is proportional to their widths, measured in tracks. The 2x-sized cells are 16% to 37% smaller than the gate+inverter combinations that they replace.

Circuit	Width (tracks)
NAND + INV_2	6
AND_2	5
AND + INV_2	8
NAND2_2	5
OR2 + INV_2	8
NOR_2	5

Based on the above results, 2x-sized logic gates provide a significant reduction in propagation delay and/or area when they can be used. Their major drawback is that input capacitance increases proportionately. The NOR_2 has nearly 3x input capacitance, and may require buffering of the previous logic stage. The OR_2 gate was not implemented because the expected benefits are small, similar to the AND_2.

In addition to the double-sized logic gates, additional standard cells with improved drive strength have been created as macros which contain a normal-sized logic gate and a larger-sized inverter. These macros have the same area and delay characteristics as the sum of the cells they include, and are primarily intended to aid in the automatic synthesis of standard cell logic. Macro-cells which incorporate a latch and multiplexers have also been designed to simplify logic synthesis.

Chapter 3

Clock Distribution

3.1 Introduction

The MAP Chip accepts a differential clock reference signal from an external source, distributes differential signals throughout the chip, and uses these to create single-ended single-phase clock signals for use in its modules. Three levels of differential-in differential-out buffers (DIDOs) and interconnect transmit the differential signals to differential-in single-ended-out pulse generators (DISOPGs), which drive local CLK and CLK_L loads.

3.2 Design

3.2.1 Overview

The clock distribution system is organized as follows:

- Level 1: Two DIDO buffers located at the center of the chip. One drives the horizontal distribution tree for the left half of the chip, the other supplies the right half.

- Level 2: Sixteen DIDOs organized as eight pairs, evenly spaced on a horizontal line along the center of the chip. Each buffer drives a vertical distribution tree for either the top or bottom half of the chip.

- Level 3: Sixty-four DIDOs arranged on a grid with approximately 2mm spacing. Each L3 may drive up to twelve pulse generators (DISOPG). The load on L3 buffers may vary depending on the number of DISOPG being driven.

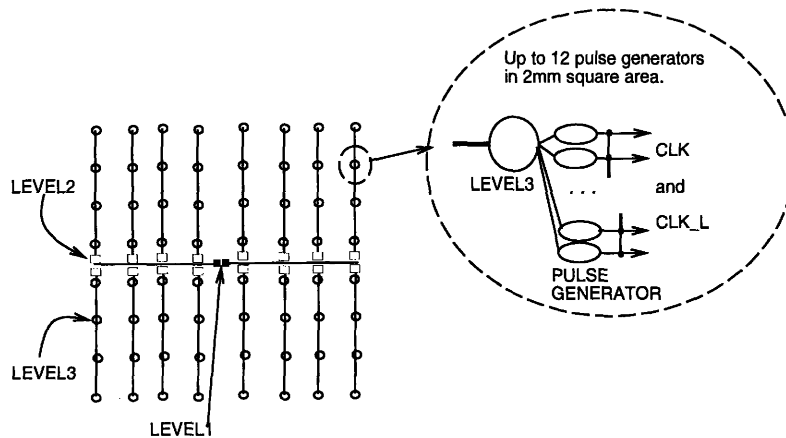


Figure 3-1: *Global Clock Distribution.*

- Level 4: Differential-in Single-ended out Pulse Generators (DISOPG), each driving up to 5pF of clock load. Pulse generators are used instead of standard buffers to avoid large short-circuit currents. DISOPGs with reversed differential inputs will be used to generate CLK_L.
- The outputs of all DISOPGs for CLK are tied together into a global clock grid to reduce skew. Likewise, CLK_L outputs are connected into a global CLK_L grid.
- The total CLK load of the MAP Chip is estimated to be 1nF. The CLK_L load is estimated to be 0.4nF Note that clock load density varies greatly across the chip.

3.2.2 Wires and Wire Models

Tree structures are used to transmit differential clock signals throughout the chip. A tree is illustrated in figure 3-2. This structure guarantees that all receiving nodes are equidistant from the transmitting node, thus minimizing skew due to varying propagation times.

Interconnect capacitances were estimated using process design information. Assuming that the routing in adjacent metal layers is perpendicular (M1 vertical, M2 horizontal, etc), there is a maximum of 50% coverage for up and down capacitances. Fringe and line-to-plate capacitances are scaled accordingly.

The horizontal and vertical trees will run in the two topmost metal layers, consistent with the MAP routing conventions. The horizontal distribution trees may be implemented

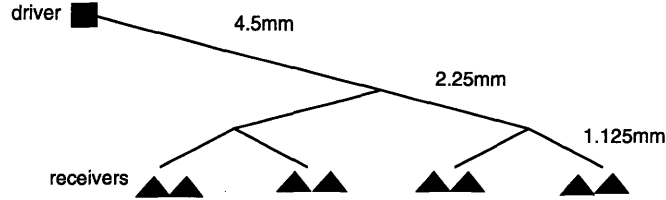


Figure 3-2: *Clock Distribution Tree.*

with minimum-width wires. The vertical trees will be triple-width (2.7um) wires. This reduces wiring resistance by a factor of three while increasing capacitance by only about one-third, thus reducing interconnect RC delay. The results are shown below. The total capacitances include input capacitance of the next-level driver. Ideal edge time is to the time for the receiver node to change from 20% to 80% of its final value when a step input is applied to the top of the tree.

Wire type	Width	Ideal edge time
LM	1x	220 ps
M4	1x	1700 ps
M4	3x	510 ps

Each Level 3 DIDO distributes the clock reference signals to up to twelve DISOPGs within a 2mm square area. Each DISOPG drives up to 5pF of load. An estimate for maximum L3 wire length is $12^*\sqrt{2}/2 = 8.4$mm, and the total load for the L3 DIDO is 1.8pF.

3.2.3 Differential Buffers

General Design

The three levels of DIDOs will all use the same buffer circuit. Representative waveforms for the differential clock distribution system are shown in Figure 3-3.

The DIDO consists of three stages: a modified Chappell amplifier and two Hartman-type buffers of increasing size. The Chappell amplifier stage [2] is used for its large differential gain and common-mode rejection. A variation of the Double Mirror-Compensated CMOS ECL Receiver designed by Chappell is used as differential receiver in the DIDO. The differential input signal is supplied to the gates of the NMOS input devices. The bias voltage for

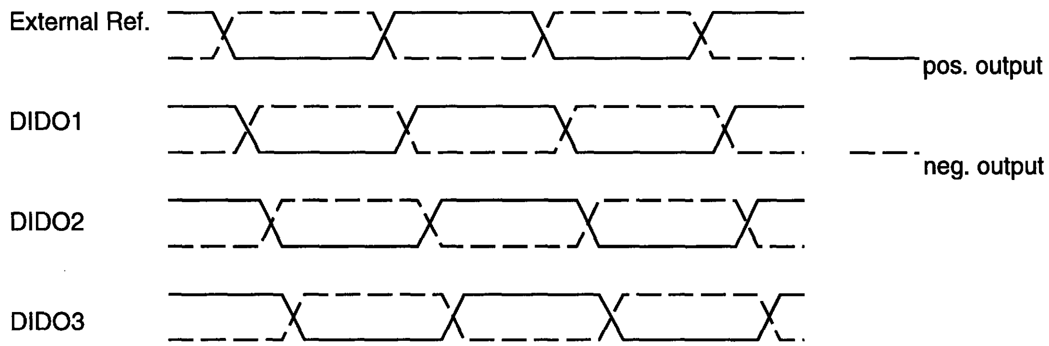


Figure 3-3: *Ideal Waveforms for DIDO*

each side of the amplifier is the output voltage of the other half. The P-channel load devices are in mirror-bias configuration. During a transition, the bias voltage of a half-circuit changes, causing the PMOS load device and NMOS current source to change their transconductances in the direction to improve the differential gain. The circuit is self-biased with both PMOS and NMOS load devices, and provides good compensation to power supply and P/N device common-mode variations.

The Hartman buffers, also known as Push-Pull Cascode Logic [5] include cross-coupling to maintain the complementary properties of the differential signals. The two stages increase in size to provide adequate drive current for large capacitive loads. The second stage is also sized to provide similar output rise and fall times.

The Hartman differential amplifier is designed to provide fast worst-case edge times. It uses NMOS devices to provide most of the switching currents, and cross-coupled PMOS devices to provide full- swing outputs. For example, when the positive input rises from ground to Vdd and the negative input falls to ground, NMOS transistors pull down the negative output and pull up the positive output. Short- circuit current flows until the opposite-polarity NMOS devices are completely turned off. When the negative output falls below Vdd-Vtp, a PMOS transistor turns on and helps to pull the positive output to Vdd.

The final stage Hartman amplifier is sized to provide similar rise and fall times. In this arrangement, the pull-down NMOS and pull-up PMOS devices are provide most of the current for transitions. The pull-up NMOS devices are small to reduce the input load of the buffer.

The relative rise and fall times for the Hartman buffer depend on the output load. As

currently sized, the unloaded buffer has equal edge times. When loaded with 1.8pF to 4pF, edge times are nearly equal.

Sizing

The DIDO is designed to drive a load of 4pF, which corresponds to a triple-width wire tree as described in the previous section. The edge time requirement is flexible for the DIDO because of its analog nature. The maximum edge time is set by the required level of noise tolerance. The DISOPG will function with edge times greater than one nanosecond (see following section). A schematic for the DIDO can be found at the end of this document.

The second Hartman stage consists of 120-wide NMOS devices to drive a 4pF capacitive load. The approximation that an NMOS device drives ten times its own width of gate suggested that the first Hartman stage should be 24um wide. The Chappell amplifier was then sized to drive the input load of the first Hartman stage. The second Hartman stage was resized to provide similar output rise and fall times.

3.2.4 Pulse Generators

General Design

The pulse generator accepts a differential reference signal and generates a single-ended system clock that can drive up 5pF of load with 400ps edge times. Pulse generators are used instead of conventional buffers (inverters) to reduce the amount of short-circuit current caused by the large output driver stage. The polarity of pulse generator differential inputs can be reversed to produce either CLK or CLK_L.

The differential amplifier accepts a differential clock reference signal and creates a single-ended output. This is buffered by a series of inverters which drive the pulse generator.

The pulse generator controls its output drivers based on the difference between its input signal (pg_in) and a delayed and inverted version of it. At DC, the output drivers are off and a small keeper maintains the proper voltage level for CLK. When pg_in transitions from low to high, both the input and delayed signal are high for a period determined by the delay chain. This is detected by the NAND gate and used to turn on the PMOS output driver, causing CLK to rise. Likewise, when pg_in falls both it and the delayed signal are low. This is detected by the NOR gate and turns on the NMOS output driver, pulling CLK

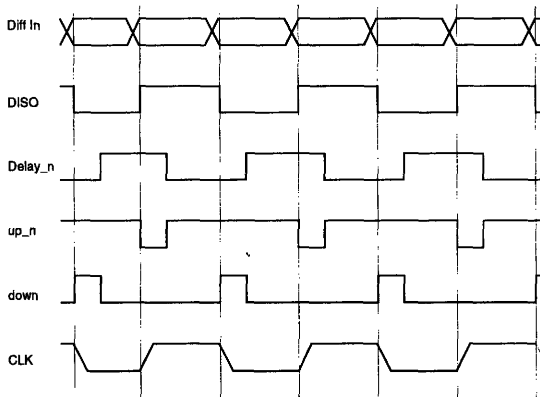


Figure 3-4: *Ideal Waveforms for DISOPG*

low. This is illustrated in Figure 3-4.

Sizing

The large output driver devices were sized to provide 400ps edge times on the CLK signal. HSPICE measures 430pS rise time and 390pS fall time on CLK. The high and low times are closely balanced, as HSPICE measures 4.97ns high time (CLK 50% to 50%). Times in this section are measured with 5pF load on CLK, and differential inputs driven by standard cell INV_1's.

The NAND and NOR gates are sized to drive these large devices with fast rise/fall times for critical edges (up_n Tf=320ps, down Tr=350ps), and slow transitions for non-critical edges. The transistors active in the critical edges are sized asymetrically, with the early-arriving signal (d3n) controlling large transistors and the late arriving signal (pg_in) controlling smaller devices closer to the outputs. The slow-transition devices were sized to keep the voltage change of up_n and down from the supply rails due to capacitive coupling at less than 200mV.

The keeper inverters maintain CLK at full-swing voltages when the driver transistors are off. With 5pF of clock load, the CLK signal will change less than 0.5v with up to 1pF of capacitive coupling between CLK and a full-swing signal with 300ps edge time.

The delay chain consists of three inverters. At TTL conditions, the width of up_n pulse was measured to be 1.6ns (50% to 50%), or 760ps (10% to 10%). The down pulse was measured to be 1.8ns (50% to 50%), or 790ps (90% to 90%).

In the worst case process corner (FF), The up_n pulse remains below 10% for 260ps after CLK rises to 90%. Down remains above 90% for 280ps after CLK falls to 10%.

The pulse generator is sensitive to the edge times of pg_in, since slow edge times affect the edge times of the pulses and cause slower edge times on CLK. Edge times of pg_in were measured to be Tr=370ps, Tf=320ps.

The DISO amplifier converts a full-swing differential signal to a full-swing single-ended signal. High gain is not required. The circuit was sized to provide reasonable edge times (Tr=420ps, Tf=300ps) and propagation delays. The following inverter is sized to correct for the rise/fall time asymmetry of the differential amplifier. This inverter is also a convenient way to fine-tune the duty cycle of CLK.

3.3 Sources of Clock Skew

Temporal differences between the clock signals in different parts of the chip is caused by many factors. Some important ones are described below, along with possible ways to tolerate or compensate for them.

Power supply variation, either local or chip-wide, causes skew between single-ended signals by creating a difference between transmitter and receiver switching thresholds. The use of differential circuits with common-mode rejection and are less affected by changes in the power supply.

The L3 DIDOs may have different loading because of varying numbers of pulse generators in a given area. This changes the amount of interconnect capacitance, and thus the propagation delay between the L3 DIDO and connected DISOPGs. This effect can be lessened by controlling the total number of pulse generators connected to each L3 buffer. Extra wires or capacitors can be added to equalize the loads seen by the third level DIDO.

Process variation can influence the properties of both devices and interconnect. Simulation has been performed to examine system behavior with device variation. If interconnect properties exhibit large process variation, multiple wire models could be created to represent the different conditions.

The length of interconnect between DISOPG output grid and where CLK is used can vary. In addition, the load on DISOPGs may vary. These can be controlled by careful layout and routing.

3.4 Evaluation

The following sections describe the circuit-level simulations done during the design of the clock buffers. Detailed analysis which includes extracted layout capacitances is being performed as the physical design is completed. Detailed chip-wide evaluation using RC and transmission line models to evaluate skew is also in progress.

3.4.1 Differential Buffers

The following table shows the expected performance for the DIDO circuit driving a triple-width distribution tree, corresponding to a 3.9pF load. Devices are typical-N, typical-P, with a 3.0 volt power supply ("TTL" conditions).

All edge time measurements are from 20% to 80% of the final output value. Nodes cp, h1p, and outp refer to the output nodes of the three differential amplifier stages, as shown on the schematics in the appendix. Node 'leaf' is one of the leaf nodes in the clock distribution tree. Measurements at this node represent the input signals to the next-level differential receivers. T_{high} is the period between the 50% point of the signal's rising transition to the 50% point of the falling transition.

Node	Trise	Tfall	T_{high}
cp	510ps	400ps	
h1p	380ps	350ps	
outp	550ps	460ps	4.88ns
leaf	750ps	670ps	4.86ns

As noted above, the relative rise and fall times of the DIDO depend on the load on its output. The level 3 DIDO will drive a capacitive load of up to 1.8pF. The following table lists the edge times for a DIDO at TTL conditions driving a 1.8pF load. As an indication of the optimal performance of the circuit, edge times with no load are also shown.

Load	Trise	Tfall	T_{high}
0pF	170ps	180ps	5.00ns
1.8pF	410ps	390ps	4.88ns

To evaluate the noise sensitivity of the DIDO, HSPICE simulations with step changes in power supply voltages were used. Test scenarios included 600mV peak-to-peak noise

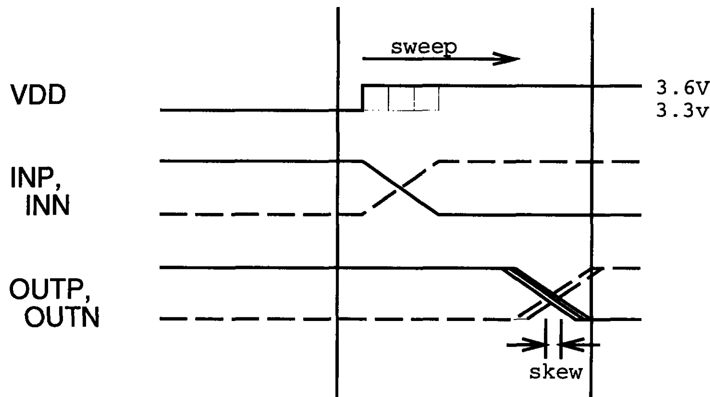


Figure 3-5: *Noise Test Waveforms for DIDO*

on Vdd or ground. The DIDO has good immunity to power supply noise. Representative waveforms are shown in figure 3-5.

The crossover point of the differential inputs shifts in time in response to power supply changes. This point is significant because the differential receiver compares the relative voltages of its two inputs. The following table summarizes this shift for a DIDO driving a triple-width wire model (3.9pf). The shift measured at the driver output was within 10ps of the shift at the wiring tree's receiver nodes.

Initial Vdd	Initial GND	Noise	Max. change of crossover
3.3v	0v	Vdd step to 3.6v	-140ps
		Vdd step to 3.0v	+160ps
		none	0ps
		GND step to 0.3v	+170ps
		GND step to -0.3v	-130ps

Measurements of DIDO output currents into its largest expected load, a triple-width distribution tree, are shown below. These measurements can be used to determine the minimum wire widths and contact quantities to prevent electromigration.

Process Corner	Vdd	RMS Current	Average Current
FF	3.6v	5.1mA	2.4mA
TT	3.3v	4.3mA	2.2mA

3.4.2 Pulse Generators

The Differential to single-ended amplifier stage is sized for low gain. This is a compromise between large input devices for high gain, and reducing the input capacitance. The following table shows the pulse generator's performance with slowly changing input signals. T_{high} is the time between a signal rising to 50% and falling to 50%. Rise and fall times are measured between 10% and 90% points. Times measured at TTL conditions with 5pF load on CLK.

Edge time	DISO T_{high} (ns)	Tr (ps)	Tf (ps)	CLK T_{high} (ps)	Tr (ps)	Tf (ps)
400ps	4.90	540	340	4.97	435	420
800ps	4.90	610	440	4.99	435	400
1200ps	4.95	620	450	5.03	435	410
1600ps	4.96	690	510	5.07	445	410

The rated clock load for the pulse generator is 5pF, but actual clock load may vary. The following table shows the DISOPG output characteristics with varying clock load, at TTL conditions. Differential inputs are symmetric with 800ps edge times.

Load (pF)	T_{high} (ns)	Tr (ps)	Tf (ps)
0	4.99	165	215
2.5	4.99	310	315
5.0	4.99	435	400
6.0	5.00	470	460

The following measurements reflect the performance of the DISOPG under varying process and power supply conditions. Differential inputs are symmetric with 800ps edge times.

Process corner	Vdd (v)	T_{high} (ns)	Tr (ps)	Tf (ps)
FF	3.6	5.18	265	255
FS	3.0	5.16	515	350
SF	3.0	4.97	330	470
SS	3.0	4.85	575	555
TT	3.3	5.02	395	385
TT	3.0	4.99	435	400

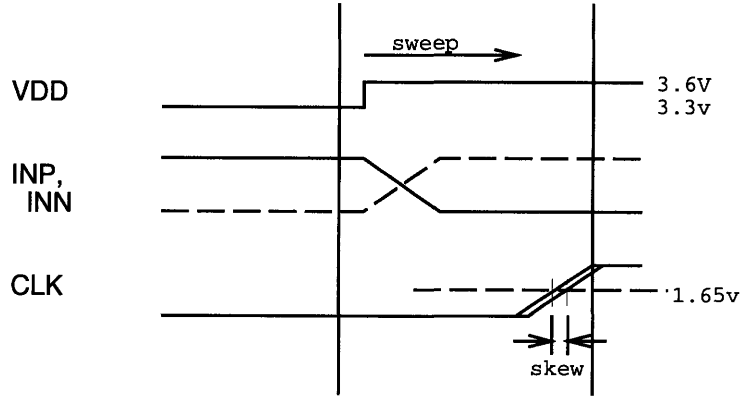


Figure 3-6: *Noise Test Waveforms for DISOPG*

Noise tests similar to those for the DIDO were performed on the DISOPG. Eight scenarios were tested: 300mV step change in the up or down direction on either Vdd or GND, with CLK either rising or falling. The voltage step was swept over the period between the DISOPG input starting to change and the output transition finishing, in 50pS steps. Figure 3-6 illustrates typical test waveforms.

Skew was defined as the maximum variation between the time CLK reaches 3.3/2=1.65 volts with a step change in either Vdd or GND, and when CLK would reach 1.65v for a DISOPG with 3.3v constant power supply. The measured skew was between -100ps and +100ps for all test scenarios.

The output devices of the DISOPG create large currrents. Output wires must be wide enough to prevent electromigration. The following are RMS current measurements at various process corners. Current was measured between the output node of the large load-driving devices and a 5pF load.

Process Corner	Vdd	RMS Current	Average Current
FF	3.6v	14mA	3.8mA
TT	3.3v	11mA	3.5mA

3.5 Power Dissipation

The clock distribution system includes many large devices, and has high power dissipation. The DIDO and DISOPG both include differential receiver circuits that dissipate static power. Total clock power dissipation for the chip is 6.2W at fast-N fast-P 3.6v power

supply conditions (FF), and 4.3W at nominal-N nominal-P 3.3v power supply conditions (TT). The total static power dissipation is 1.5W at FF conditions, and 750mW at TT conditions.

Estimated power consumption for the DIDO is shown below. Estimates for the entire system are based on 82 DIDOs (2 L1, 16 L2, and 64 L3) operating at 100MHz. The figures below correspond to fast-N, fast-P, 3.6v power supply (FF), and typical-N, typical-P, 3.3v power supply (TT) conditions.

Corner	Vdd	Total, unloaded	with 1.8pF	with M4 2.7um	Whole Chip
FF	3.6v	18mW	27mW	30mW	2.3W
TT	3.3v	7mW	17mW	21mW	1.5W

The table below lists the power consumption for the DISOPG at various process corners. Estimates for the entire chip assume 280 pulse generators (1.0nF/5pF=200 for CLK, 0.4nF/5pF=80 for CLK_L), each driving a 5pF load and operating at 100MHz.

Process Corner	Vdd	Total per cell	Whole Chip
FF	3.6v	14mW	3.9 W
TT	3.3v	10mW	2.8 W

The table below shows the static power dissipation for the DIDO and DISOPG at FF and TT process conditions.

Cell	Process Corner	Vdd	Static Power per Cell
DIDO	FF	3.6v	10mW
DIDO	TT	3.3v	5mW
DISOPG	FF	3.6v	1.3mW
DISOPG	TT	3.3v	0.65mW

3.6 Layout Issues

3.6.1 Differential Buffers

All differential circuits used in the clock distribution system depend on symmetry for good performance. Care must be taken to the layout of these circuits. Folded transistors with asymmetric shapes and source/drain capacitance should appear in the same orientation on

each side of the circuit to minimize the effect of mask alignment error. Load capacitance from the source/drain and wire load should be identical on both sides of the circuit.

3.6.2 Interconnect

The differential signals should be routed as twisted-pairs, or with shield wires connected to a power supply rail. The layout of the distribution trees should maintain symmetry between branches by either minimizing or balancing capacitive coupling between branches. Long differential pairs may be arranged as twisted pairs, with crossovers at regular intervals.

Greater than minimum-width spacing should be used between differential clock signals and external signals wherever possible. Shield wires can also be used to reduce coupling to noise- critical signals.

3.6.3 Electromigration

Both the differential buffers and the pulse generator outputs produce large currents that require attention to prevent electromigration. The single-width horizontal and triple-width vertical trees satisfy electromigration limits at all points. Multiple contacts should be used wherever feasible, in particular at the top of distribution trees. The connection from the pulse generator output to clock grid will require wide wires and multiple contacts.

Chapter 4

Design of the LTLB

4.1 Introduction

The LTLB of the MAP chip performs virtual-to-physical address translation for data stored in an M-Machine node. Each entry represents the virtual-physical translation for a 4KB page of data. The LTLB also stores block status information for the page translations it contains. Block status information is used to determine if 8-word blocks of data within a page are present on the local node. The LTLB is similar in physical design to the other MAP Chip SRAM arrays.

The LTLB was initially designed to store 128 entries. Later, to meet area constraints, the size of the LTLB was reduced. This chapter describes the original LTLB design, and a section at the end describes the simple modifications made to reduce its size.

4.2 Function

The LTLB operates in two modes: virtual-to-physical address translation, and as raw data for configuration space accesses. During address translation, the output of the data arrays is processed as address, LRU, valid, and block-status fields. For configuration space accesses, input and output is handled as 64-bit words. Except for LRU bits, all writes are performed on 64-bit words. The LRU bit has its own input and write control signals, and can be written independently from the rest of the array. Its output is available through a dedicated output with some built-in logic, and as part of the 64-bit address word.

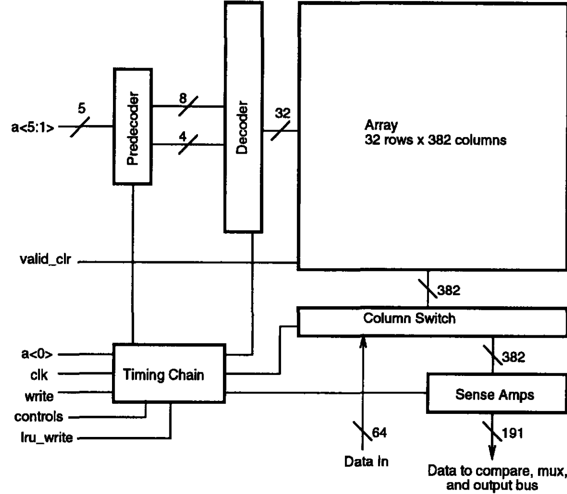


Figure 4-1: *LTLB SRAM Array Block Diagram.*

4.3 Implementation

4.3.1 Overview

The LTLB consists of SRAM arrays and and datapath elements including multiplexers and comparators. To allow rapid implementation, circuit components are reused from other memory array designs (ICRAM, MCRAM) or synthesized from standard cells whenever possible.

The SRAM cells are divided into two 382-bit by 32-row half-arrays. This design allows the array to fit into the current floorplan. 191 bits of a half-array are accessible at a time, due to 2:1 multiplexing of sense amplifiers. Data is written to one-sixth of the array at a time, in 64-bit words. Figure 4-1 shows the organization of an LTLB half-array and its support circuits.

A 5-to-32 dynamic tree decoder based on the design in *MAP SRAM Circuit Design* is used in the LTLBRAM. The decoder first converts a 5-bit input to two one-hot fields (1-of-4 and 1-of-8). A second stage uses these two fields to generate the 32 wordline signals. The LTLB will include two decoders, one for each half-array. Because wordlines are metal-strapped, placement of the decoders has little effect on array timing. For simplicity of layout, decoders are placed on the sides of the SRAM arrays. Stitch cells are included in the SRAM array, inserted after every 32 bitcell columns.

Column switch and sense amplifier cells are identical to those used in other MAP Chip

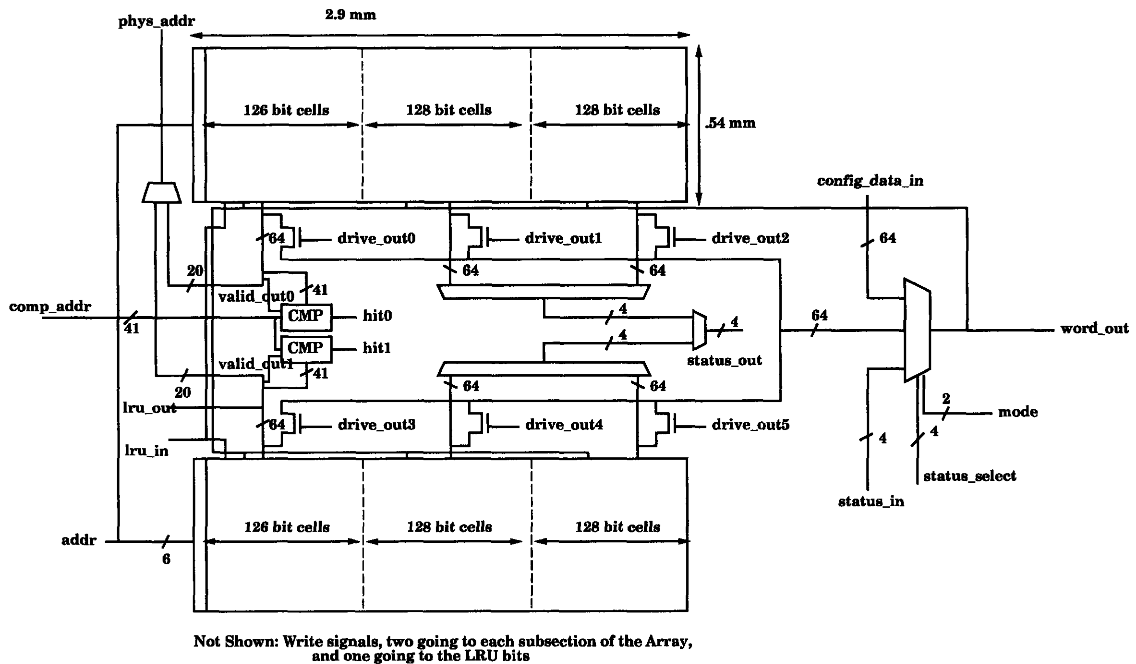


Figure 4-2: *LTLBRAM Block Diagram.*

memory arrays. The timing chain uses the same general design as the MCDRAM timing chain.

To make the half-arrays identical, both halves include column-pairs with correct functionality for LRU bits. Only one of half-arrays is used to store LRU values, the other has input and write signals connected, and an unconnected output.

The sense amplifier data outputs are connected to address translation circuits, and also to tri-state buffers that drive a 64-bit bus. This internal data bus transmits data to the cell LTLB_MUX, a multiplexer that controls the writeback path and output data word.

4.3.2 Datapath

Figure 4-2 is a high-level block diagram for the LTLB. During address translation, the output of the LTLBRAM arrays is interpreted as a virtual address, a physical address, LRU bit, valid bit, and block status bits. The virtual address is compared to an input value, and the valid bit to TRUE, by a standard-cell based comparator. The results from the two half-arrays, match<1:0>, are available to the EMI and also control multiplexing of address and status outputs.

When a LTLB hit occurs, the proper physical address and block status bits must be

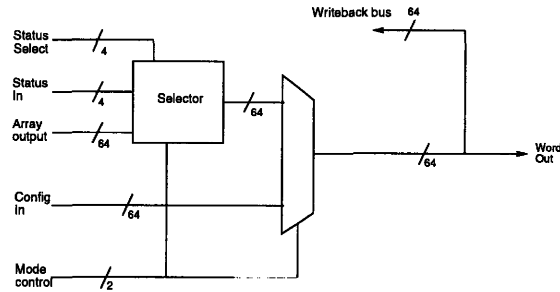


Figure 4-3: *Concept for Output and Read-Modify-Write selector*

selected from the two half-arrays. This is done with multiplexer composed of standard cells. A 128:4 multiplexer is used to select 4-bit groups of block status bits. Two 64-bit banks of tristate drivers select half of the 128 bits, and a 64-to-4 bit multiplexer composed of standard cell logic generates the 4-bit result.

The LTLB performs all data writes on 64-bit words. To write data, a word is produced by the LTLB_MUX and driven onto the writeback bus, which is connected to the LTLBRAM column switch data inputs. The multiplexer LTLB_MUX, shown in figure 4-3 produces an output word suitable for different purposes:

- Configuration space read: 64-bit word is driven from internal bus to output bus.
- Configuration space write: 64-bit config space input is driven onto the writeback bus.
- Modify a 4-bit status field: The 64-bit word containing the field to be changed is driven on the internal data bus. The new status field is input to the selector, along with a 4-bit selection field. The mux replaces the selected status field with the input data, leaving all other fields unchanged, and outputs the new 64-bit word.
- Address translation: value of output word doesn't matter.

Figure 4-4 shows the correspondence between control inputs and their respective sub-arrays.

4.3.3 Cell Descriptions

The following sections describe the major cells in the LTLBRAM hierarchy. The LTLB schematics can be divided into full-custom cells and cells composed of standard cells. Figure 4-5 shows the division of cells within the hierarchy between standard-cell and custom design.

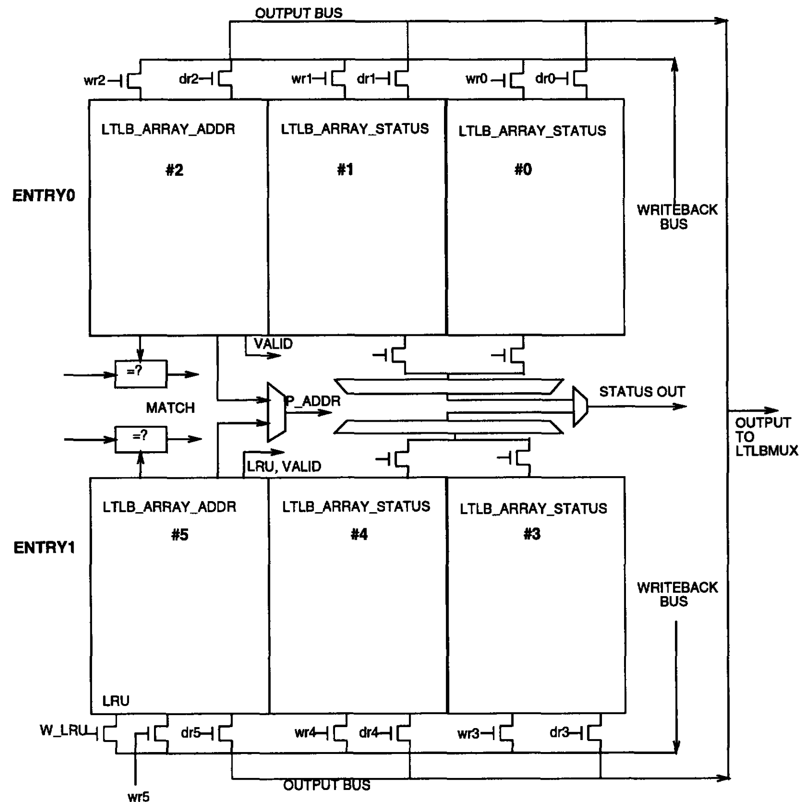


Figure 4-4: *Numbering of sub-arrays and their control signals.*

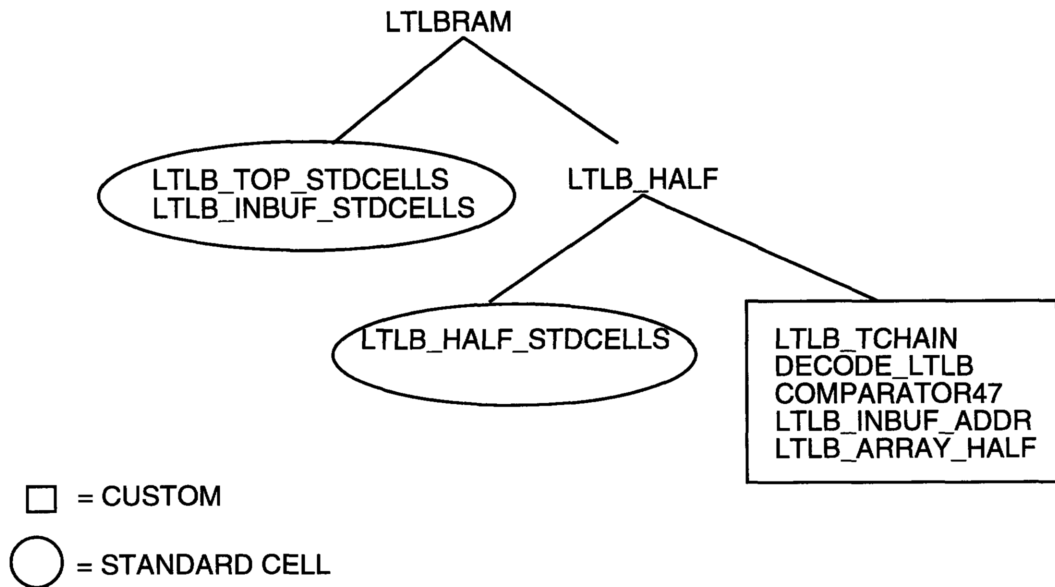


Figure 4-5: *Organization of standard-cells and custom cells.*

LTLB_BITLINE1

This is a 1x32 array of BIT_CELL, the SRAM cell supplied by IBM. Inputs are wl<31:0>, an array of one-hot encoded word lines. Outputs are b and b_L, the complementary bit lines. When a word line is asserted, the corresponding bit cell is connected through passgates to the precharged bit lines. One bit line will be pulled toward ground, while the other will remain near its initial voltage. The sense amplifier will read the output value when the voltage difference between the bit lines is at least 300mV. To write into a bit cell, the proper word line is asserted while the value to be written is driven on the bit lines by the column switch.

LTLB_BITLINE2

Cell LTLB_BITLINE2 includes two instances of LTLB_BITLINE1, two column switches, and the sense amplifier shared between the two columns. Inputs are the 32 one-hot word lines, two independent read control lines, two independent write lines, and signals relating to precharge and the sense amplifier (pc, spcn, sclk). Only one of the read control lines should be asserted at any time. Likewise, only one of the write control lines should be asserted at any time.

During a read cycle, the appropriate word line from wl<31:0>, and one of the read controls rd_L<1:0> are asserted. The timing chain associated with the half-array will produce the proper pc, spcn, and sclk signals. One bit of data will appear at the data_out pin.

LTLB_BITLINE1_CLR

This cell is similar to BITLINE1, but composed of SRAM cells with flash clear. It will be used to store valid-bits.

LTLB_BITLINE2_CLR

This cell includes two columns of BITLINE_CLR, two column switches, and a shared sense amplifier. It is similar to BITLINE2, with the addition of a CLR input that flash-clears all of the bit cells.

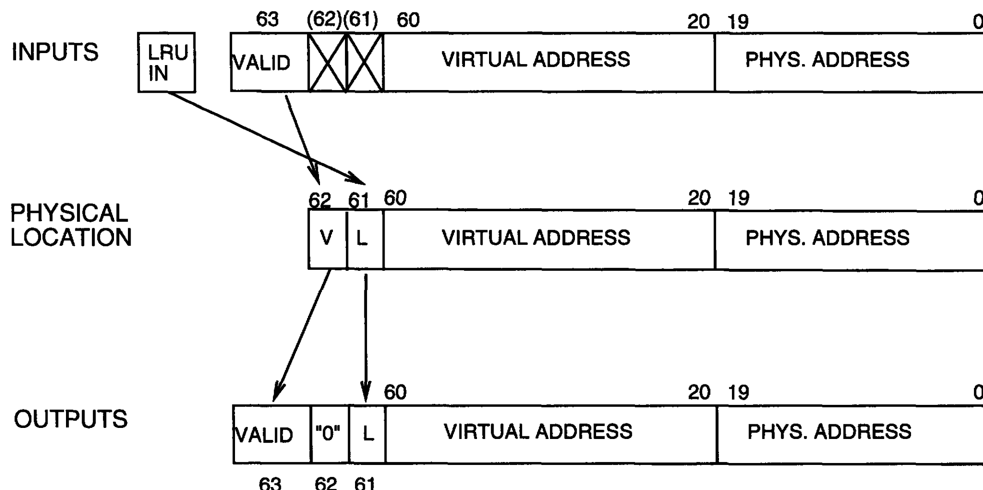


Figure 4-6: *Data organization within LTLB_ARRAY_ADDR.*

LTLB_INBUF_ADDR

To reduce the capacitive load of LTLBRAM address inputs, buffers are inserted to drive the wordline decoder. This cell includes buffers for the five decoder inputs. The low-order LTLBRAM address input goes to the timing chain and has little load, thus it is not buffered.

LTLB_ARRAY_ADDR

This cell includes the array elements that store valid, LRU, and address bits. There are only 63 bits in each word in this array. Figure 4-6 shows the organization of data in the input, physical, and output words of the array.

- 1 bit for VALID. This uses BITLINE2_CLR to provide flash-clear ability.
- 1 bit for LRU.
- 20 bits for physical address.
- 41 bits for virtual address.

The LRU bits have independent write control and output lines from the rest of the array. The valid bits are written at the same time as data, controlled by the write_data lines. Valid bits are read and written as bit position 63 in input and output words. The external interface of this cell is described in the following table:

Name	I/O	Description
wl<31:0>	I	32 word lines (one-hot)
data_in<63:0>	I	1-bit valid, 20-bit physical, 41-bit virtual addr.
data_out<62:0>	O	output from sense amplifiers.
rd_L<1:0>	I	one-hot selector for 2:1 column mux during reading.
write_data<1:0>	I	one-hot write control signal
lru_in	I	input for LRU columns
write_lru<1:0>	I	write control for LRU columns.
CLR_VALID	I	Flash-clears valid bits when asserted high
pc	I	precharge clock, from timing chain to column switches
sclk	I	clock signal to sense amps
spcn	I	control signal to sense amps

During a read, the appropriate word line from wl<31:0> and one of the control lines rd_L<1:0> are asserted. The timing chain generates the appropriate pc, sclk, and spcn signals. Writes are accomplished by providing the appropriate data or LRU inputs and asserting a write control signal.

The LRU bit is written independently from the rest of the array and has a seperate input pin. Input to data_in<61> is ignored.

LTLB_ARRAY_STATUS

This cell contains 64 instances of BITLINE2. Two instances of this cell are used to store the 128 block-status bits associated with each LTLB entry. The organization of block status bits within the LTLB_ARRAY_STATUS cells is shown in figure 4-7.

I/O pin descriptions:

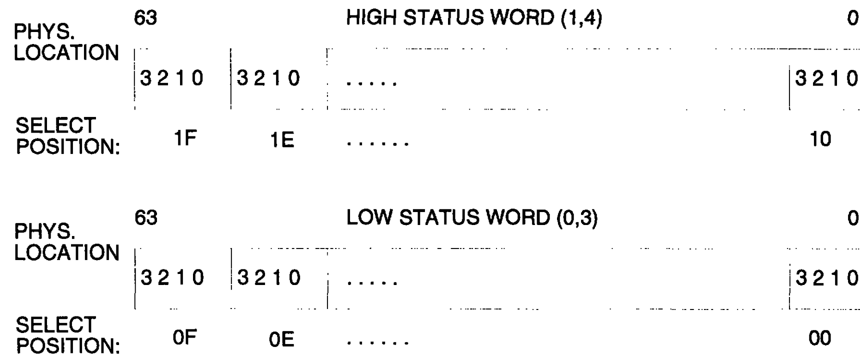


Figure 4-7: *Data organization within LTLB_ARRAY_STATUS.*

Pin	I/O	Description
rd_L<1:0>	I	One-hot control to select 1 of 2 sets of columns for read.
data_in<63:0>	IO	64-bit data word to be written.
wl<31:0>	I	One-hot array of 32 word lines.
write_data<1:0>	I	One-hot write controls.
data_out<63:0>	O	64-bit array data output.
pc	I	Precharge clock
sclk	I	Clock signal for sense amps.
spcn	I	Control signal for sense amps.

4.3.4 LTLB_ARRAY_HALF

This cell includes arrays of SRAM bit-cells, column switches, and sense amplifiers. The LTLB_ARRAY_ADDR and LTLB_ARRAY_STATUS cells have seperate data input pins, which are tied together at a higher level in the hierarchy to form a bus structure.

Pin	I/O	Description
data_in_addr<63:0>	I	64-bit data word to be written.
data_in_s1<63:0>	I	64-bit data word to be written.
data_in_s0<63:0>	I	64-bit data word to be written.
lru_in	I	Input for LRU bit.
array_out_addr<62:0>	O	Output from ltlb_array_addr sense amps
array_out_s1<62:0>	O	Output from ltlb_array_status sense amps
array_out_s0<62:0>	O	Output from ltlb_array_status sense amps
wl<31:0>	I	One-hot array of 32 word lines.
write_data<5:0>	I	One-hot write controls.
write_lru<1:0>	I	write controls for LRU bit
rd_L<1:0>	I	Select 1 of 2 sets of columns for reading.
pc	I	Precharge clock
sclk	I	Clock signal for sense amps.
spcn	I	Control signal for sense amps.

LTLB_HALF_STDCELLS

This cell groups together all of the components in LTLB_HALF that are built from standard cells. It includes the 128:4 multiplexer for block status bits, banks of 64-bit tristate bus drivers, buffers for various signals.

The block status multiplexer is designed in two stages: a 128:64 multiplexer based on tristate drivers, and a static combinational 64:4 multiplexer.

LTLB_HALF

This cell is one of the identical half-arrays that compose the LTLB.

It includes a word line decoder, SRAM array, timing chain, comparator, and the cell ltlb_half_stdcells which contains various components composed of standard cells. Note that the two LTLB_HALF instances will have independent wordline decoders and timing chains.

The 5-32 word line decoder (DECODE_LTLB) is composed of cells used in the MCRAM. It is a precharged dynamic decoder that accepts a 5-bit input address, and a precharge clock signal from the timing chain. Outputs are 32 one-hot word lines, with adequate drive strength to switch the array word lines directly. The MCRAM decoder included a 'nomatch'

active-low input to allow the use of redundant rows to improve fault-tolerance. The LTLB does not include redundant rows, and this input is tied high. Because of the tree structure of the decoder, its address inputs dec<4:0> have high capacitive loads. LTLB_HALF includes buffering of address inputs, contained in cell LTLB_INBUF_ADDR, to remedy this problem.

The timing chain is of similar design to those used in the other MAP Chip memory arrays.

Pin descriptions for LTLB_HALF:

Pin	I/O	Description
dec<4:0>	I	5-bit buffered input for wordline decoder
block_select<5:0>	I	Select 1 of 64 blocks per page
drive_bus<2:0>	I	One-hot control, drives 1 of 3 64-bit words to bus.
comp_addr<40:0>	I	41-bit virtual address input for compare
data_in_addr<63:0>	I	64-bit input for ltlb_array_addr.
data_in_s1<63:0>	I	64-bit input for high word ltlb_array_status
data_in_s0<63:0>	I	64-bit input for low word ltlb_array_status
lru_in	I	Input value for LRU
word_addr<63:0>	IO	tri-state output, to LTLB internal bus.
word_status_hi<63:0>	IO	tri-state output, to LTLB internal bus.
word_status_lo<63:0>	IO	tri-state output, to LTLB internal bus.
status_out<3:0>	O	4-bit block status output.
phys_addr<19:0>	O	Buffered physical address output.
lru_out	O	Buffered LRU output (ltlb_array_addr bit 61)
valid_out	O	Buffered VALID output (ltlb_array_addr bit 62)
hit	O	Buffered comparator output
w_data<2:0>	I	One-hot write request signals
w_lru	I	write control for LRU bit
CLR_VALID	I	Flash-clears all valid bits in half-array when asserted
CLK	I	System clock, to timing chain
SCD	I	Timing chain control
SEL<1:0>	I	Timing chain control
WPS	I	Write pulse width selector
SET	I	Choose active bit columns (2:1 sense amp muxing)

LTLB_INBUF_STDCELLS

To reduce the input load seen by modules driving inputs to the LTLBRAM, the LTLBRAM includes buffering for inputs with large capacitive loads. This cell includes standard cell inverters with appropriate sizes to deliver input signals into the LTLBRAM. These buffers should be physically located close to the input pins of the LTLBRAM.

LTLB_MUX

This multiplexer creates 64-bit words for writeback and output to configuration space. It will be created from standard cells. It has three modes: Copy config_data_in to output (10), Copy data from internal bus to output (00), and update selected 4-bit status field while copying other bits from internal bus (00).

I/O description:

Pin	I/O	Description
mode<1:0>	I	Sets mode: data_out, data_update, config_data_in
data_in<63:0>	I	data word from the LTLB arrays
config_data_in<63:0>	I	data word from configuration space
status_in<3:0>	I	new value for 2-bit block status field
status_select<3:0>	I	Placement of new status bits within 64-bit word
mux_out<63:0>	O	Output word, for writeback and config space output

LTLB_TOP_STDCELLS

Included in this cell are the standard cell-based components shared between the two LTLB half-arrays. These include LTLB_MUX, logic for the LRU bit, status and physical address output multiplexers, and some buffers.

The LRU output is defined by (lru_bit AND (valid0 OR valid1)). If neither entry is valid, then the LRU bit is forced to zero.

LTLB_TCHAIN

This cell is similar to the timing chains used in the instruction cache and main cache arrays. Control signal timings are determined by long chains of inverters referenced to the positive and negative edges of system clock. The signals PC, SPCN, and SCLK are referenced from the positive edge of clock. SCD affects the width of the DC, PC, and SPCN pulses.

Nominally SCD is low, and increases the width of these pulses by 500ps (TTL) if asserted. Decode clock (DC) falls before the rising edge of clock, after the time reserved for the previous cycle's write pulse. It rises based on a delay from the long inverter chain.

Timing of write pulses is determined by an inverter chain based on the falling edge of system clock. A variable delay cell provides up to 1.5ns variation in delay to allow correct positioning of write pulse. In addition, WPS doubles the width of the write pulse when asserted high.

The read control signals RDN<1:0> are gated with the first half-cycle of system clock (CLK high). This disconnects the sense amplifier from the bitlines during the write pulse, limiting the voltage swing of sense amplifier inputs.

Pin	I/O	Description
CLK	I	System clock
SCD	I	Controls width of DC, PC pulses.
SET	I	Low address bit - selects column for 2:1 colswitch muxing.
SEL<1:0>	I	Allows variation of write pulse position.
WREN<2:0>	I	Write request signals for address and status words.
W_LRU	I	Write request signal for LRU bit.
WPS	I	Doubles width of write pulse when high. Normally low.
DC	O	Controls precharge/evaluation of wordline decoder.
PC	O	Controls precharge of bitlines through column switch.
SPCN	O	Controls precharge of sense amplifiers.
SCLK	O	Clock to control sense amp sampling and latching.
RDN<1:0>	O	Selects columns for reading through column switches.
wp_out<5:0>	O	Write control signals to column switches.
wp_lru<1:0>	O	Write control signals for LRU bits.

The signals PC, SPCN, and SCLK are generated from a delay line based on the rising edge of system clock. Write pulses are generated from a delay line based on the falling edge of clock. A variable delay cell provides can be adjusted through DIP switches to change the position of the write pulse. Figure 4-8 illustrates timing chain output signals for a typical cycle.

The signal DC falls after the time reserved for the previous cycle's write pulse, and rises several inverter delays after rising edge of clock. Figure 4-9 shows the relationship of DC

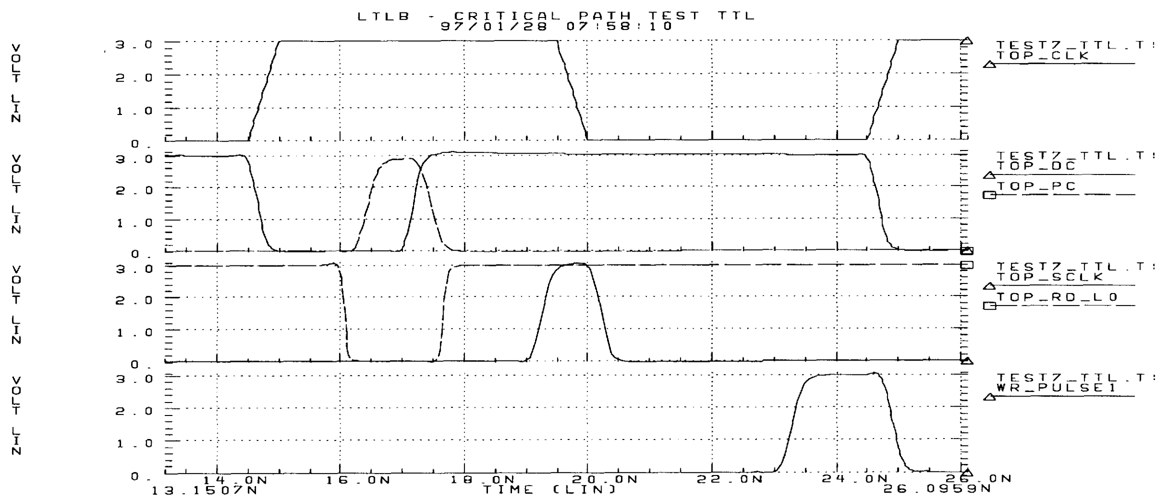


Figure 4-8: *Timing chain signals, TTL conditions.*

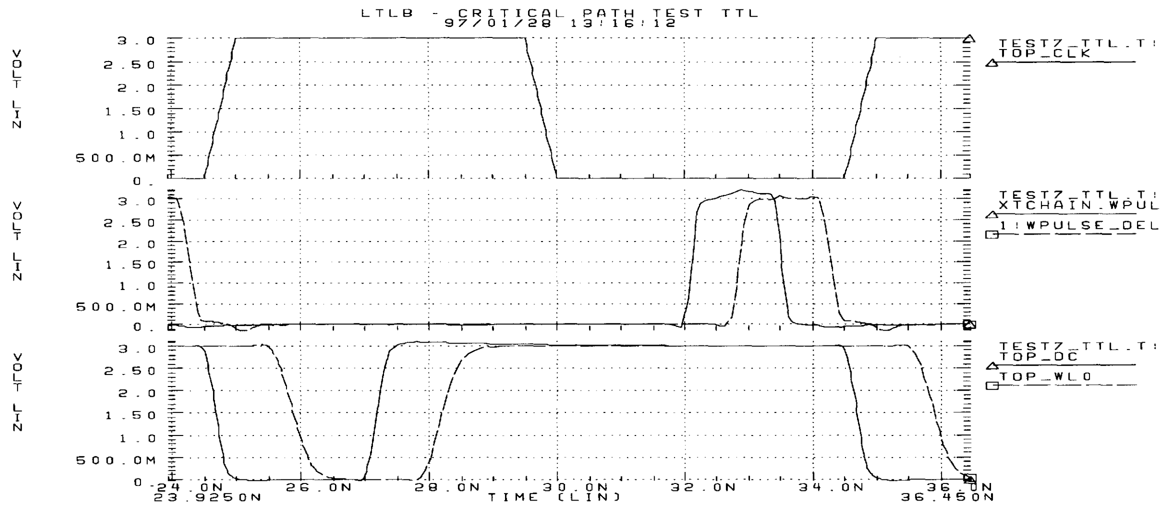


Figure 4-9: *Decode clock (DC) signal timing, TTL conditions.*

with system clock and the internal write pulse reference signal.

DECODE_LTLB

The decoder converts a 5-bit address input into a 32 wordline one-hot output suitable for driving the wordlines found in the LTLB. Because the LTLB does not contain redundant rows, the "nomatch" input is tied high and the decoder functions on every cycle. The decoder is constructed of the same cells used for the ICDRAM and MCRAM arrays.

The LTLB does not contain redundant rows, therefore the 'nomatch' input to the decoder is tied high. This signal controls a pass-NFET and pullup PFET in the pulldown tree. If convenient, the device could be removed and replaced with a wire.

Because the decoder is a dynamic pulldown tree, address inputs must be stable during each evaluation cycle. If inputs change at other times, multiple bitlines may become asserted simultaneously.

LTLBRAM

The top-level schematic includes four cells: the two half-arrays, standard cell input buffers, and standard cell logic and output buffers (ltlb_top_stdcells). The six data word inputs from the LTLB_HALF cells are tied together in a bus structure in the LTLBRAM. Likewise, the six tristate 64-bit outputs are tied to form a bus.

Pin	I/O	Description
addr<5:0>	I	6-bit address, to wordline decoder and column select
block_select<4:0>	I	Selects block within current page
w_data<5:0>	I	Write control signal, each controls a 64-bit word
drive_out<5:0>	I	One-hot, selects a 64-bit word onto internal bus
comp_addr<41:0>	I	Input to 41-bit virtual address comparator
lru_in	I	Value to be written to LRU bit.
w_lru	I	Write control signals for LRU bits.
lru_out	O	LRU bit for selected LTLB entry
status_in<3:0>	I	Status bits input
update_select<3:0>	I	Sets location of 4-bit status entry in 64-bit word
mux_mode<1:0>	I	sets ltlb_mux: data out, data modify, config data in
config_data_in<63:0>	I	Data word from global configuration space
word_out<63:0>	O	Word output, for reading through GCFG
status_out<3:0>	O	4-bit status for selected LTLB entry
phys_addr<19:0>	O	20-bit physical address for selected entry
hit<1:0>	O	True if half-array indicates both MATCH and VALID
valid_out<1:0>	O	Valid-bit outputs
CLR_VALID	I	Flash-clears all valid bits when asserted
CLK	I	System clock, to timing chain
SCD	I	Timing chain control
SEL<1:0>	I	Timing chain control
WPS	I	Write pulse width selector

The LTLBRAM includes some muxing and logic of 'hit' and 'lru' outputs. *Hit* indicates that the virtual address of an entry matches the comparison address input, and that the VALID bit of the entry is high. The LRU output is the function ((valid1 or valid0) and lru_bit). Thus, a high output is caused by an entry having both its LRU and valid bit set.

4.4 Cell Reuse

The following cells are reused without modification from the library RAM: ICTAG_BITCLR, COLSWITCH, SENSEAMP, BIT_CELL, ICTAG_TDRV66_33, TC_NOR3, PD3TO8, PD2TO4, WLD. From library MCRAM: write_cell, var_delay, TDRV400_200, udec, mctag_tdec; From library SHARE: inv2.

4.5 Layout

Figure 4.5 shows the approximate layout of the LTLBRAM. Its overall size is 640 tracks wide by 1600 tracks high (1150u x 2880u). The two sides are mirror images of each other, each including the SRAM array, column switches, sense amplifiers, decoder, and timing chain. In the center there is space for signal buses in M2 and M4. Standard cell rows will be placed below the signal buses. LTLBRAM inputs and outputs are on opposite sides of the cell in order to minimize the width of the center routing channel. The area between arrays is to be wire-limited, with space for standard cell rows beneath. Standard cell rows should be organized across the center channel, so that M1 follows the global preferred direction. This allows easier alignment of tristate buffers and array outputs because the fixed dimension of the standard cells aligns with the fixed-pitch array outputs.

The LTLBRAM will have duplicate input ports for address and timing chain inputs. Duplicate inputs will be connected together outside the LTLBRAM. There are five groups of input signals: a pair for the timing chains, a pair of address inputs, and a collection of signals which feed into standard cell buffers for distribution into the LTLBRAM.

Initial simulations assume that standard cell components are placed near the arrays that supply their inputs. Input buffers included in cell LTLB_INBUF_STDCELLS should be placed as close as possible to the input pins. Multiplexers, buffers, and tristate bus drivers contained in LTLB_HALF_STDCELLS should be placed close their respective array sources. Components of LTLB_TOP_STDCELLS should be placed near the outputs. Components of LTLB_TRISTATE should be located close to their respective array outputs, and may be organized in a long, thin area running parallel to the arrays. The LTLB_MUX_64_4 cell includes one level of tri-state buffers which could be kept in a row near the array sources, and a reducing tree of combinational logic which should be approximately centered with respect to the tri-state bus.

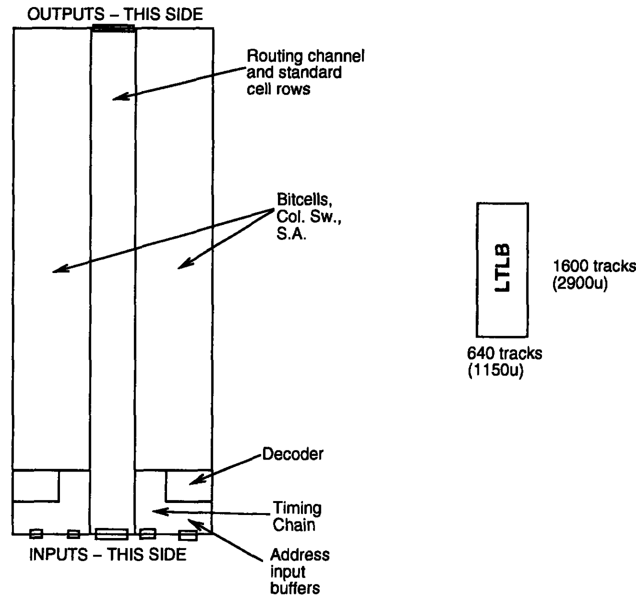


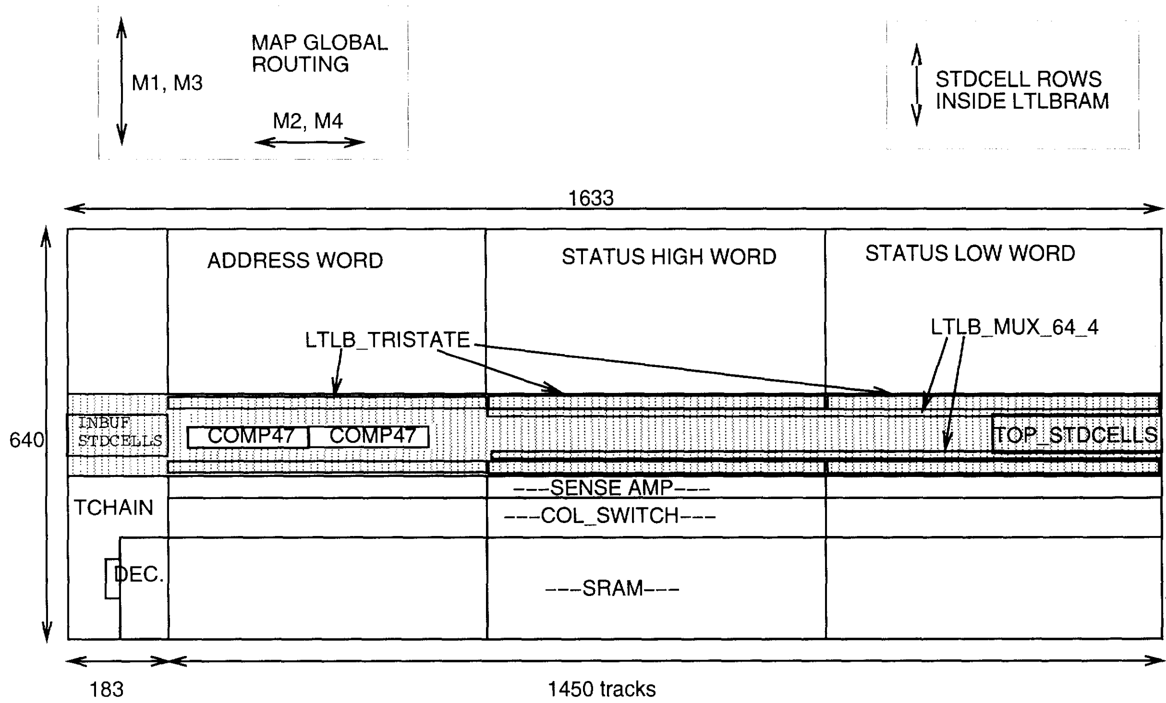
Figure 4-10: *LTLB Layout.*

A more detailed layout plan appears in figure 4-11. 132 tracks are reserved for the central routing channel and standard cell region. This would allow all inputs to enter the LTLBRAM on a single metal layer (M2 or M4). Circuits (comparators and standard cells) occupy approximately 65% of the total area in the central channel. By stacking inputs on multiple layers, it may be possible to make the channel narrower, and reduce the overall size of the LTLBRAM. Unused space in the center region should be filled with the usual filler cells, assorted logic, and/or inverters of various sizes (for driving signals long distances).

The wordline decoder (decode_ltlb) supports the use of redundant rows, however the LTLB does not have any. The decoder 'nomatch' input is tied high to disable this feature. If convenient, the NFET connected to 'nomatch' (maindec_ltlb: N0) could be replaced by a wire and the PFET P1 removed.

4.6 Evaluation

To evaluate signal timings within the LTLBRAM, a simplified HSPICE model was constructed. The model includes a full timing chain, decoder, LTLB_MUX, and buffers. Only one instance of LTLB_BITLINE2 is used, with the remainder of the array modelled with lumped capacitances that reflect the estimated wire and gate loads.



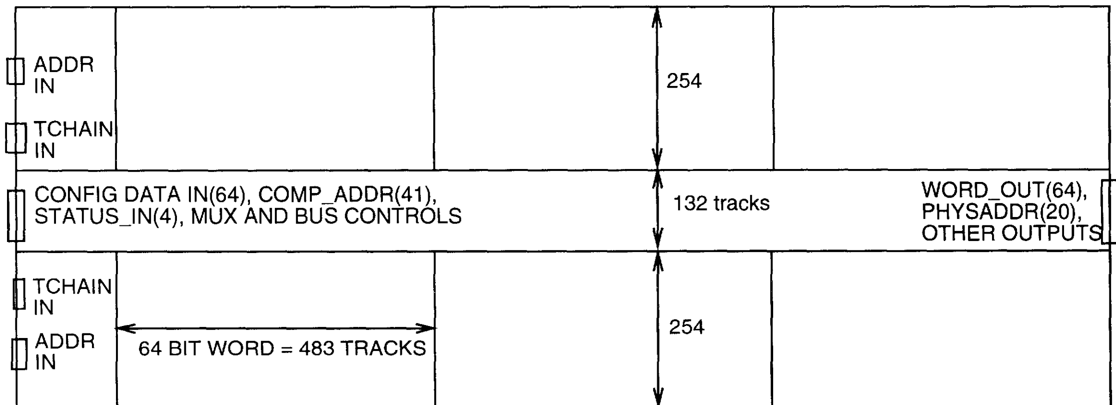


Figure 4-11: *Layout with dimensions and positions of major components.*

Transition times of selected signals are listed below for nominal (TTL) conditions. Note that the write pulse extends into the next clock cycle. The write circuitry operates by pulling down one of the precharged bitlines, therefore data must be stable during the entire duration of the write pulse. The nominal value of SEL<1:0> = 00, SCD = 0, WPS = 0. Setting SEL<1:0> to 01 delays the write pulse by approximately 700ps at TTL conditions.

Time (ns)	Internal event	Output-related event
0	CLK rises	
1.5	SPCN falls	
1.7	PC rises	
2.4	DC rises	
2.7	PC falls	
2.8	SPCN rises	
4.4	SCLK rises	
5.1		Data available from sense amp
5.4	SCLK falls	
6.0		Data valid on internal bus
6.8		Data available at LTLB_MUX output
7.3		Block status bits available
7.4	write pulse generation starts	
7.6		HIT available
8.5	write pulse rises	
9.9	DC falls	
10.2	write pulse falls	

Tt TTL conditions (typical process conditions, 3.0v power supply), propagation delays for some LTLBRAM components are: are: comp47: 1.7ns, ltlb_mux_64_4: 600ps, ltlb_mux (data change only): 700ps, buffers and writeback bus: 700ps. At TTL conditions, the bit cell switches state 700ps after the write pulse rises to 50%. This leaves about 1ns of write pulse as safety margin. Waveforms are shown in figure 4-12.

Address inputs to the wordline decoder are only allowed to change during the interval when decode clock (dc) is low. The falling edge of DC is controlled by the falling edge of the write pulse reference signal, and occurs before the rising edge of system clock. At TTL conditions, DC rises 2.4ns after the rising edge of clock. Because of internal buffering of

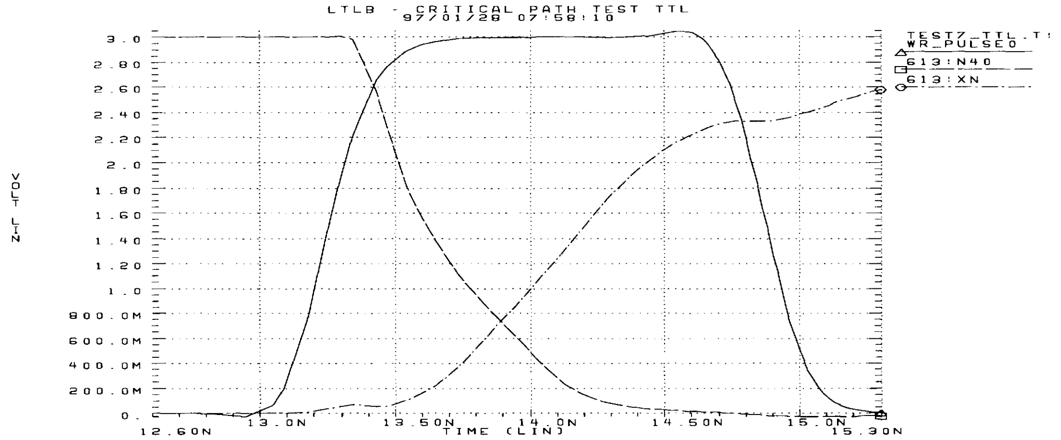


Figure 4-12: *Writing of bit cell, TTL.*

address inputs (cell LTLB_INBUF_ADDR), the window for address changes extends from the rising edge of clock to approximately six inverter delays, or 1.8ns at TTL conditions.

The following table presents timing figures at various process corners.

Event	FF	FS	SF	SS	TT	TTL
PC rise – bitlines within 30mv	0.39	0.65	0.55	0.79	0.45	0.49
PC rise 50% – PC fall 50%	0.58	0.90	1.19	1.35	0.94	1.02
DC fall – wordline drop to 0.5v	0.88	1.43	1.46	1.79	1.35	1.44
Writepulse fall – wordline to 0.5v	0.76	1.06	1.16	1.51	1.10	1.20
DC rise – wordline rise to 50%	0.60	0.93	1.15	1.26	0.94	1.03
wordline rise – bitline 300mV diff.	0.25	0.43	0.72	0.70	0.48	0.62
SCLK rise – output rises	0.33	0.58	–	0.73	0.52	0.57
write pulse rises, SEL=00	7.0	8.4	9.1	9.6	8.3	8.6
write pulse falls, SEL=00	8.1	9.9	11.4	12.0	10.0	10.4

Note that with slow-n fast-p conditions, the SRAM cell fails to write. The SF corner is overly pessimistic for M-Machine because it assumes different gate oxide thicknesses for NMOS and PMOS devices. Using a more realistic SF model, the SRAM cell has been shown

to function. Consult MCRAM documentation for details.

The timing chain output PC controls the precharging of bitlines, and is distributed to all BITLINE2 cells in the LTLB_HALF. The signal is inverted there, and the inverted signal controls PMOS devices within the column switches. Because of its short bitline length (32 bits), the LTLB bitlines charge quickly. Sample waveforms are shown in Figure 4-13. Signals XBITS.NET54 and XBITS.NET17 are a bitline pair, and 332:NET343 is the locally-generated precharge signal (inverted PC).

At various process conditions, precharge characteristics are listed below. Time to charge is the time from inverted PC falling to 50% to the bitlines precharging to within 30mV of each other. Safety margin is the time between bitlines equalizing and inverted PC rising to 50%.

Corner	Time to charge	Safety margin
FF	200ps	350ps
FS	500	650
SF	210	850
SS	470	960
TT	180	750
TTL	380	680

Estimated input load capacitances for the LTLBRAM are summarized in the following table. Buffers for address pins are located between the address inputs and the wordline decoder. All other buffers are standard cells, and should be positioned close to the inputs witin the standard cell region. These were calculated by summing the lengths of input gates, and adding a rough estimate of wire load. For signals with multiple input pins, the figures below are the total for each signal.

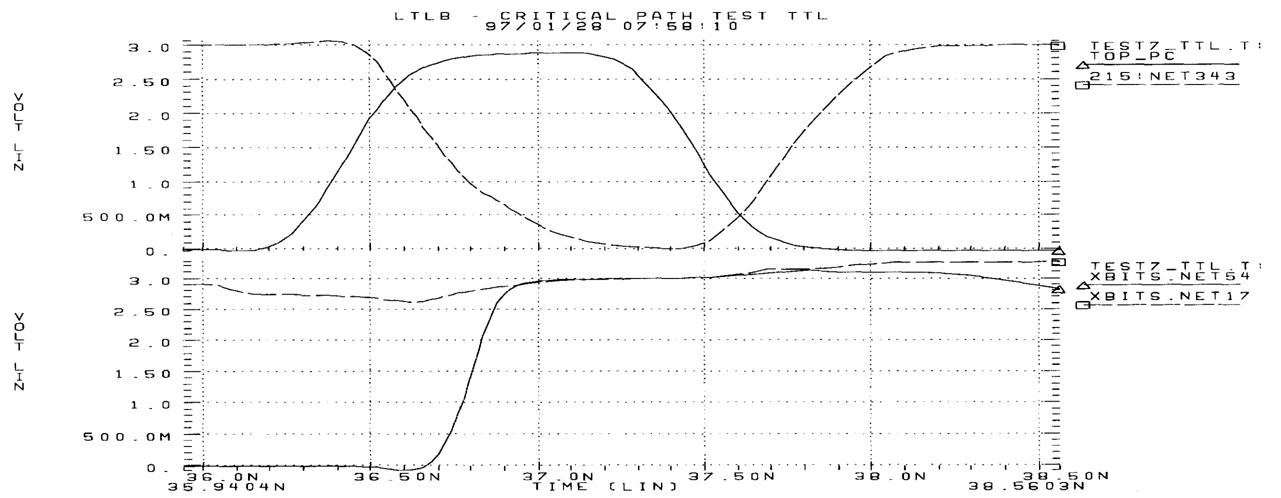


Figure 4-13: *Precharging of bitlines, TTL.*

Pin	Gate (fF)	Wire (fF)	Total (fF)
ADDR<5>	48	60	108
ADDR<4>	48	60	108
ADDR<3>	74	60	134
ADDR<2>	48	60	108
ADDR<1>	48	60	108
ADDR<0>	60	80	140
W_DATA<5:0>	26	40	66
W_LRU	26	40	66
LRU_IN	44	100	144
CLK	180	40	220
SCD<1:0>	40	40	80
SEL<1:0>	40	40	80
CLR_VALID	44	100	144
COMP_ADDR<40:0>	11	50	61
DRIVE_OUT<5:0>	43	50	93
BLOCK_SELECT<4:0>	22	50	72
UPDATE_MODE	43	50	93
UPDATE_SELECT	11	50	61
STATUS_IN<3:0>	11	50	61
CONFIG_DATA_IN<63:0>	11	50	61

4.7 Shrink

After the LTLB design was completed, chip area constraints required that the LTLB be reduced in size. The number of entries in the LTLB has been reduced from 128 to 64 by the removal of one instance of LTLB_HALF (the instance ENTRY0 in figure 4-4). The signal hit0 has been tied to ground so that the nonexistant half-array never reports a hit. Inputs to the nonexistant half have been termintated with instances of NoConn, and floating output wires tied to ground. These changes only affect the top-level LTLBRAM cell; all other cells are unchanged by the shrink. A revised top-level schematic (LTLBRAM, version A.2.00.00) is included in the appendix.

The timing of signals within the array of the modified LTLB are unchanged because each half includes an independent timing chain. Propagation delays of output and writeback signals are reduced slightly by the reduction of drain/source capacitances on the tri-state data buses. Input capacitances for the address and timing chain controls is also reduced by one-half.

Chapter 5

Conclusion

5.1 Summary

This thesis describes a variety of circuit designs for the M-Machine Multi-ALU Processor. Circuits for standard cell latches and combinational logic global clock distribution, and the LTLB module have been designed from high-level descriptions. Physical designs have also been created for standard cells. These designs constitute a broad sample of the circuit and physical designs used in a high-performance microprocessor.

Many opportunities for research and innovation at the circuit level could be explored with additional time and resources. Evaluation of the MAP Chip scan methodology and further optimization of scannable latch cells could improve the performance of synthesized logic. The use of custom-designed circuits instead of standard cells for the LTLB datapath could reduce area and propagation delay. Detailed analysis of the utilization and impact of large-sized standard cells in logic synthesis would provide useful information for future standard-cell based designs.

5.2 And Finally...

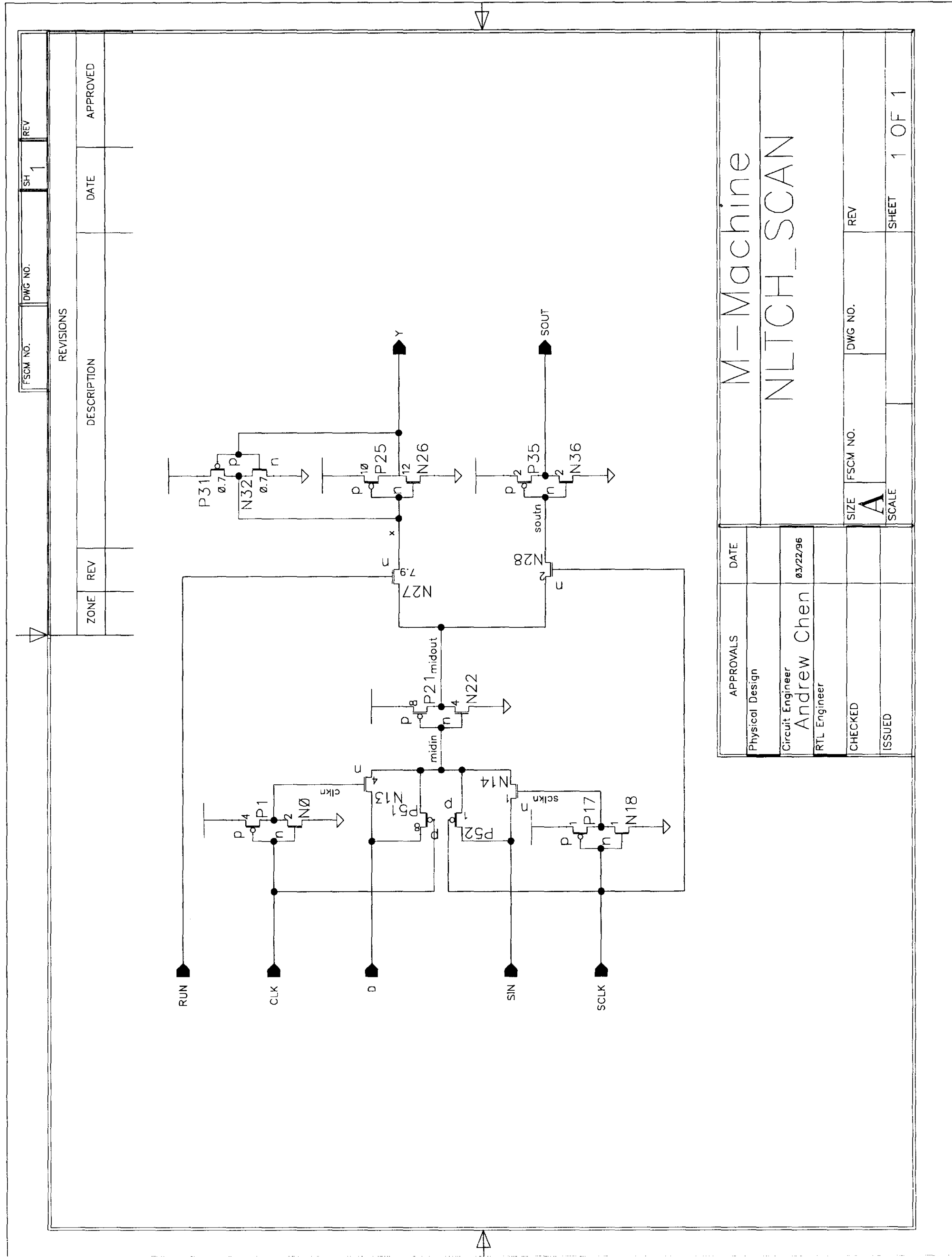
Here are some useful tidbits of information learned from the project:

- Knowledge of physical design constraints is essential to good circuit design. Likewise, knowledge of circuit constraints is important for the creation of efficient logic designs.
- Testing and verification require more time than initial design and debugging.

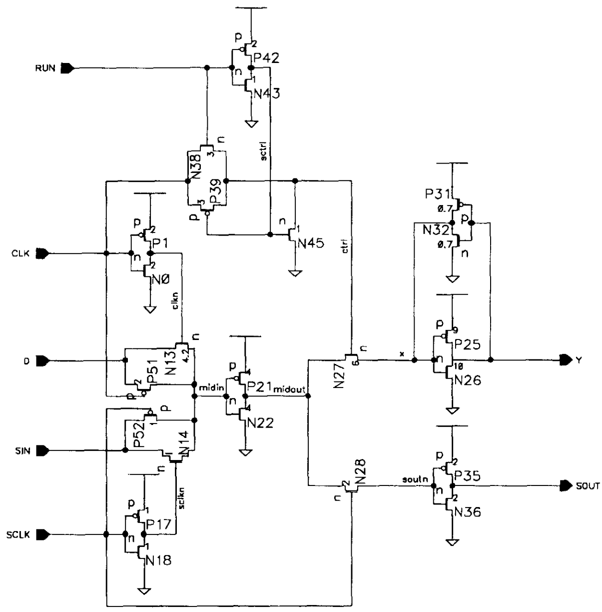
- Scannable latches are a necessity for hardware debugging, but costly in terms of speed and size.
- Designing circuits in isolation is relatively simple. Designing ones that conform to the protocols, requirements, and constraints imposed by being part of a large-scale system adds much complexity.
- Scheduling for a project of this size is a definite challenge.
- As many others in the field have stated, the wires are a very big problem indeed!

Appendix A

A.1 Latch, REG_CELL, and Standard Cell Related



Scannable Negative Latch Schematic



FSCM NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

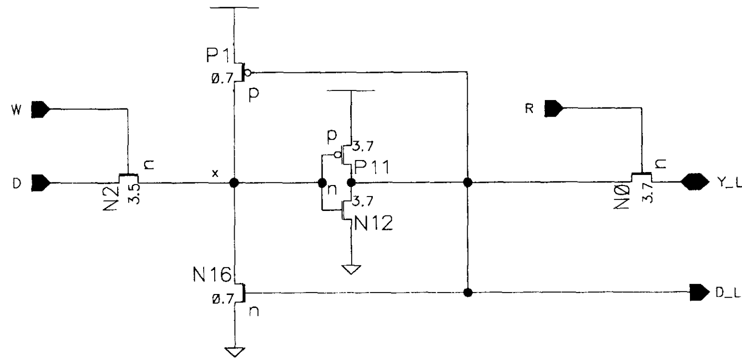
APPROVALS	DATE	
Physical Design Andrew Chen		M—Machine
Circuit Engineer Andrew Chen	03/22/96	PDFF_SCAN
RTL Engineer		
CHECKED		SIZE B · FSCM NO. · DWG NO. · REV
ISSUED		SCALE · SHEET 1 OF 1

Scannable Positive Register Schematic

FSCM NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



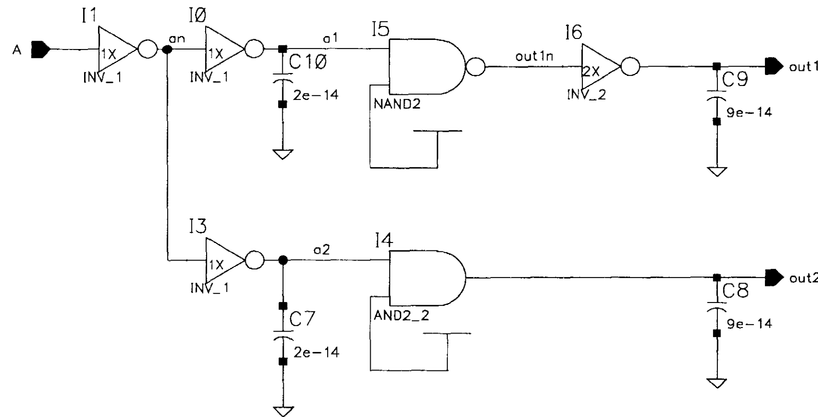
APPROVALS	DATE
Physical Design achen	
Circuit Engineer wslee	
RTL Engineer	
CHECKED	
ISSUED	

M-Machine

REG_CELL

SIZE A	FSCM NO.	DWG NO.	REV
SCALE		SHEET 1 OF 1	

Register Cell Schematic



FSCM NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

APPROVALS	DATE
Physical Design	
Circuit Engineer Andrew Chen	03/02/97
RTL Engineer	
CHECKED	
ISSUED	

M—Machine

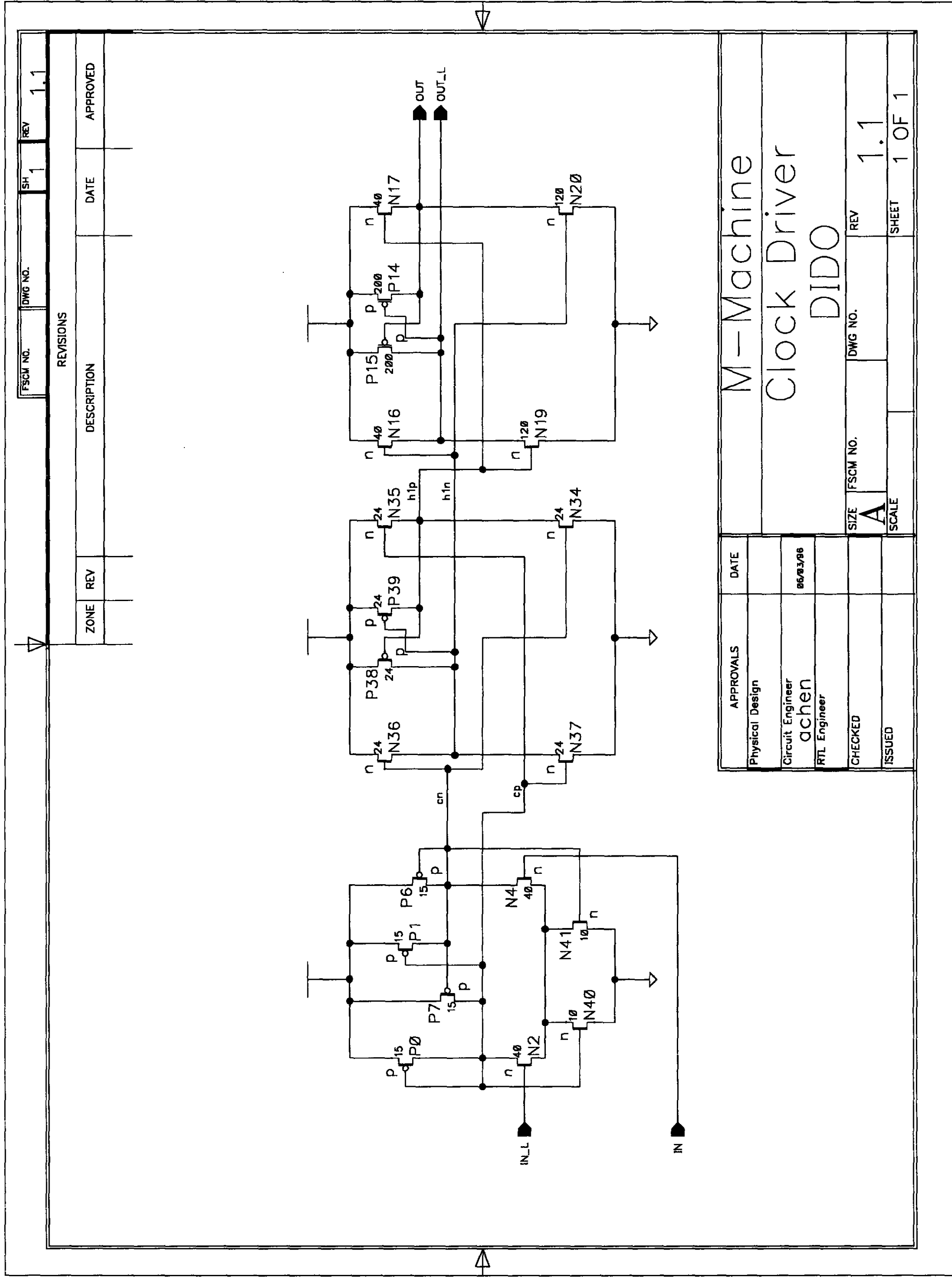
Standard Cell Test

AND2_2

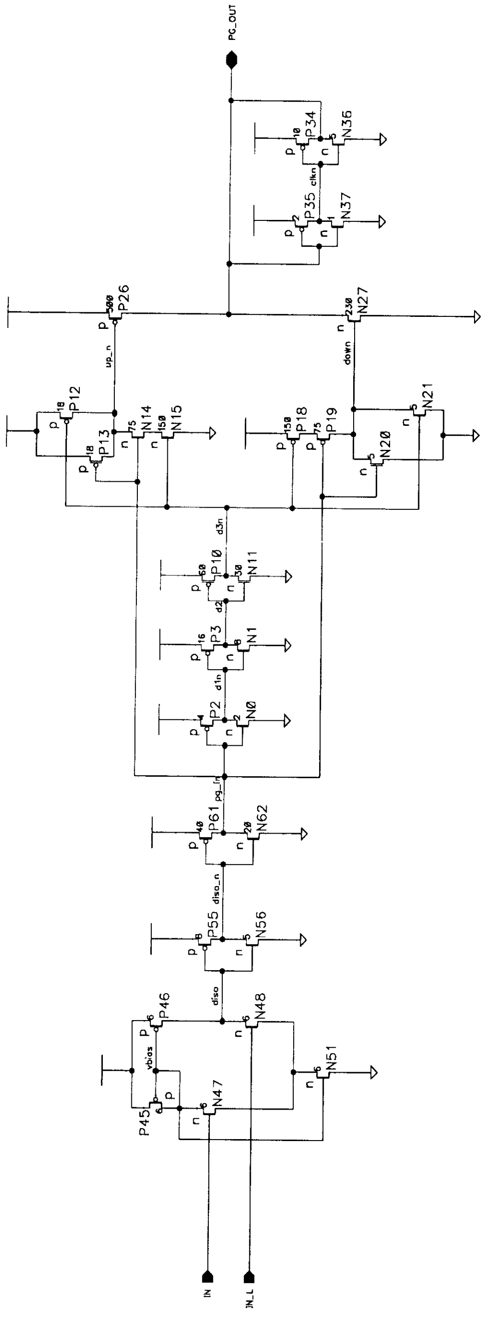
SIZE A	FSCM NO.	DWG NO.	REV
SCALE			SHEET 1 OF 1

Circuit to Evaluate 2x-sized Standard Cell Logic

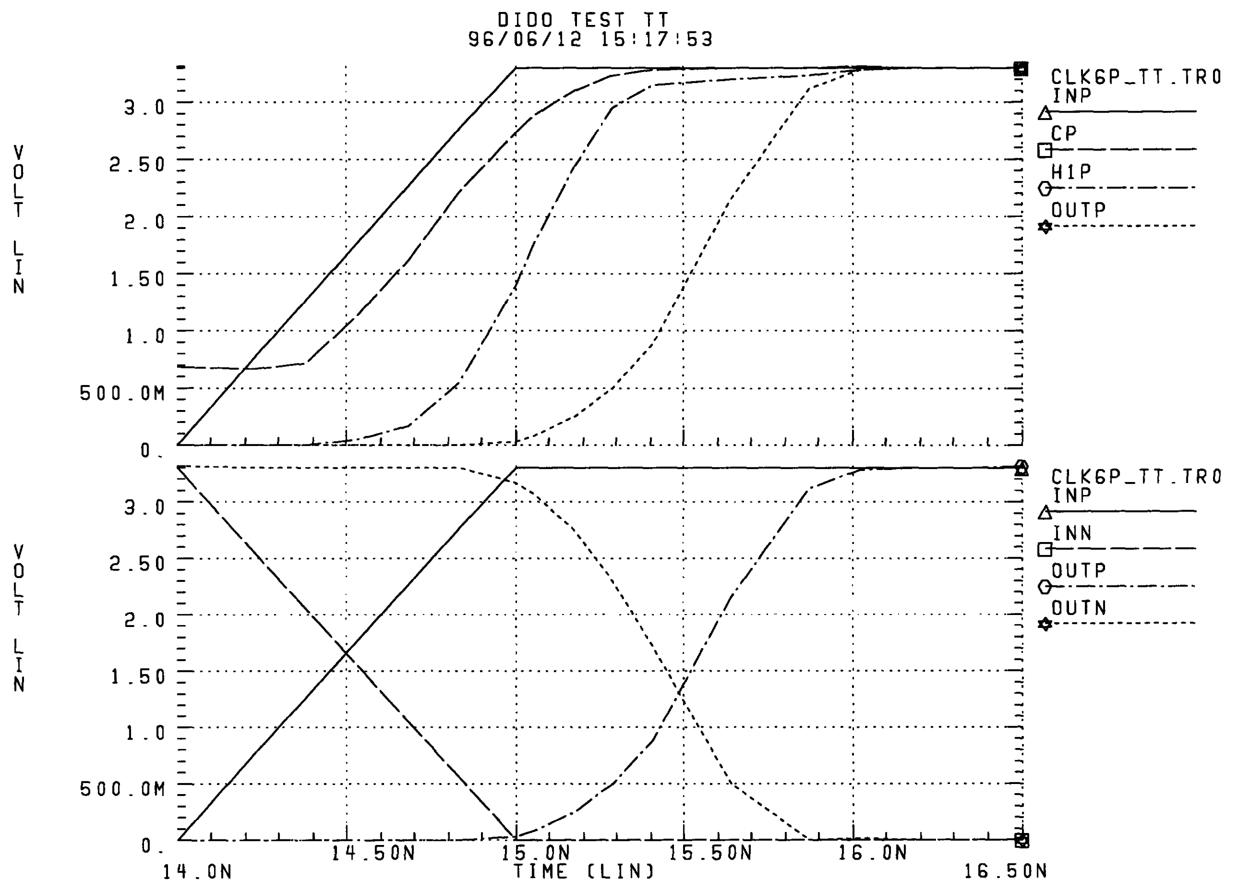
A.2 Clock Distribution System



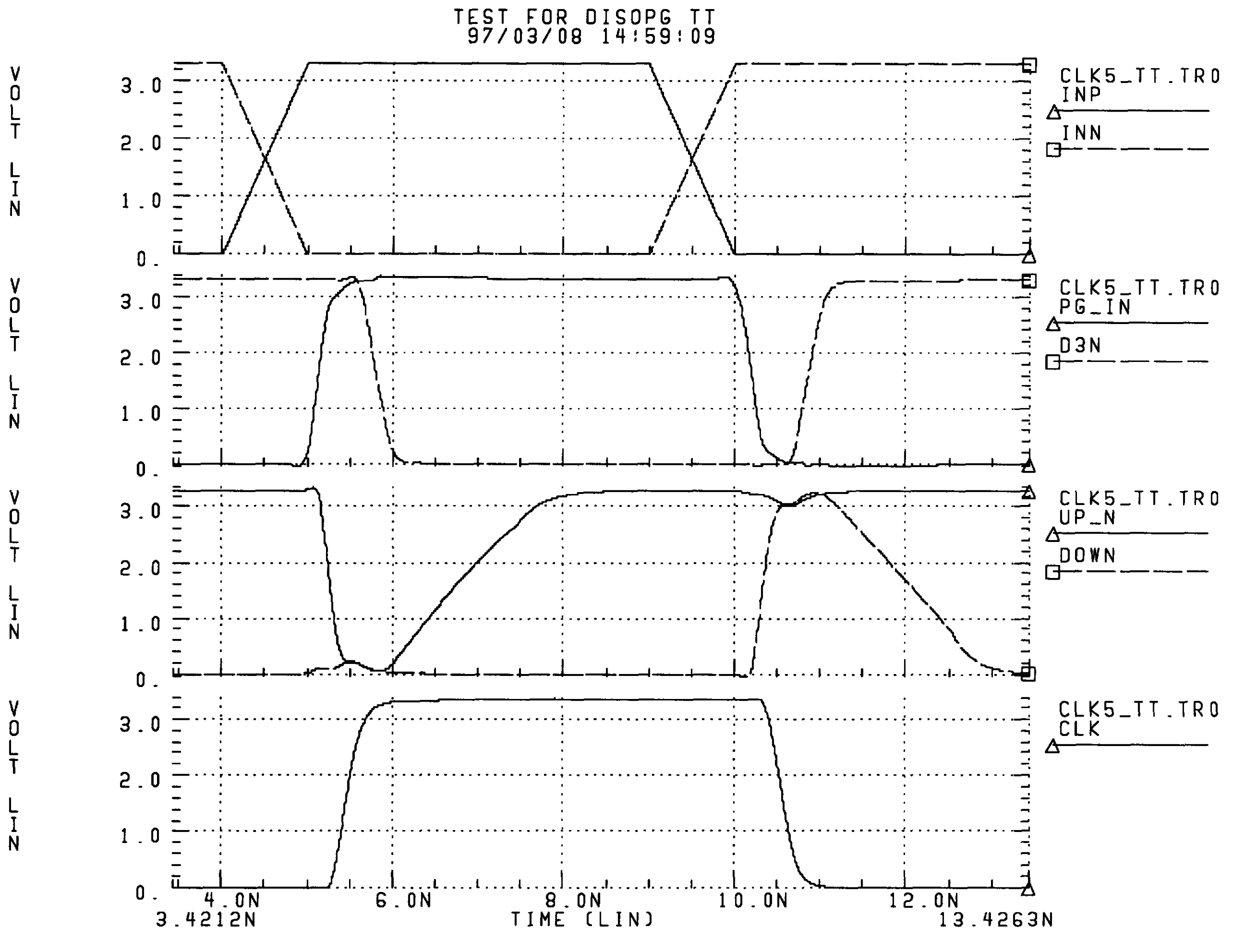
Differential-In Differential-Out Buffer for Clock Distribution



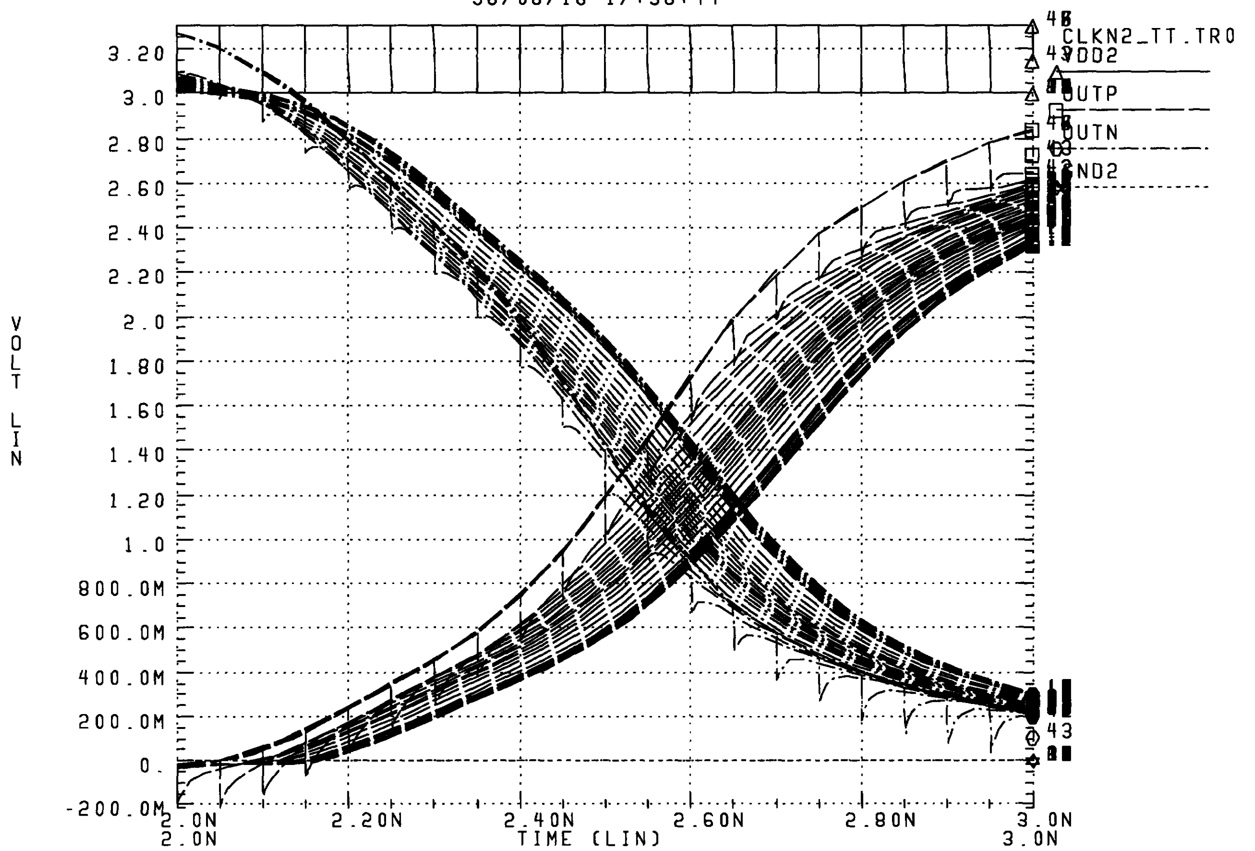
Differential-In Single-ended-Out Pulse Generator



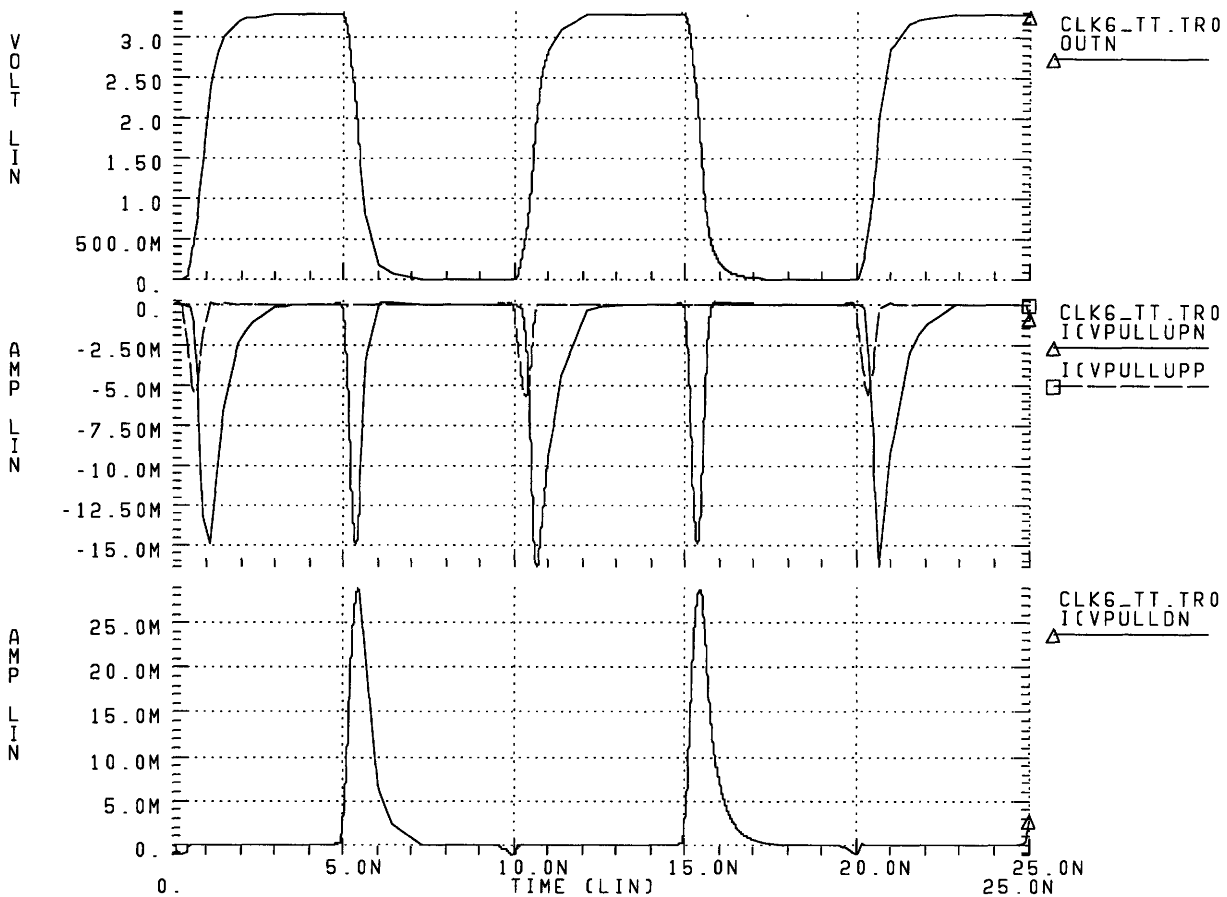
Typical function of a DIDO with 1.8pF output load, TT conditions



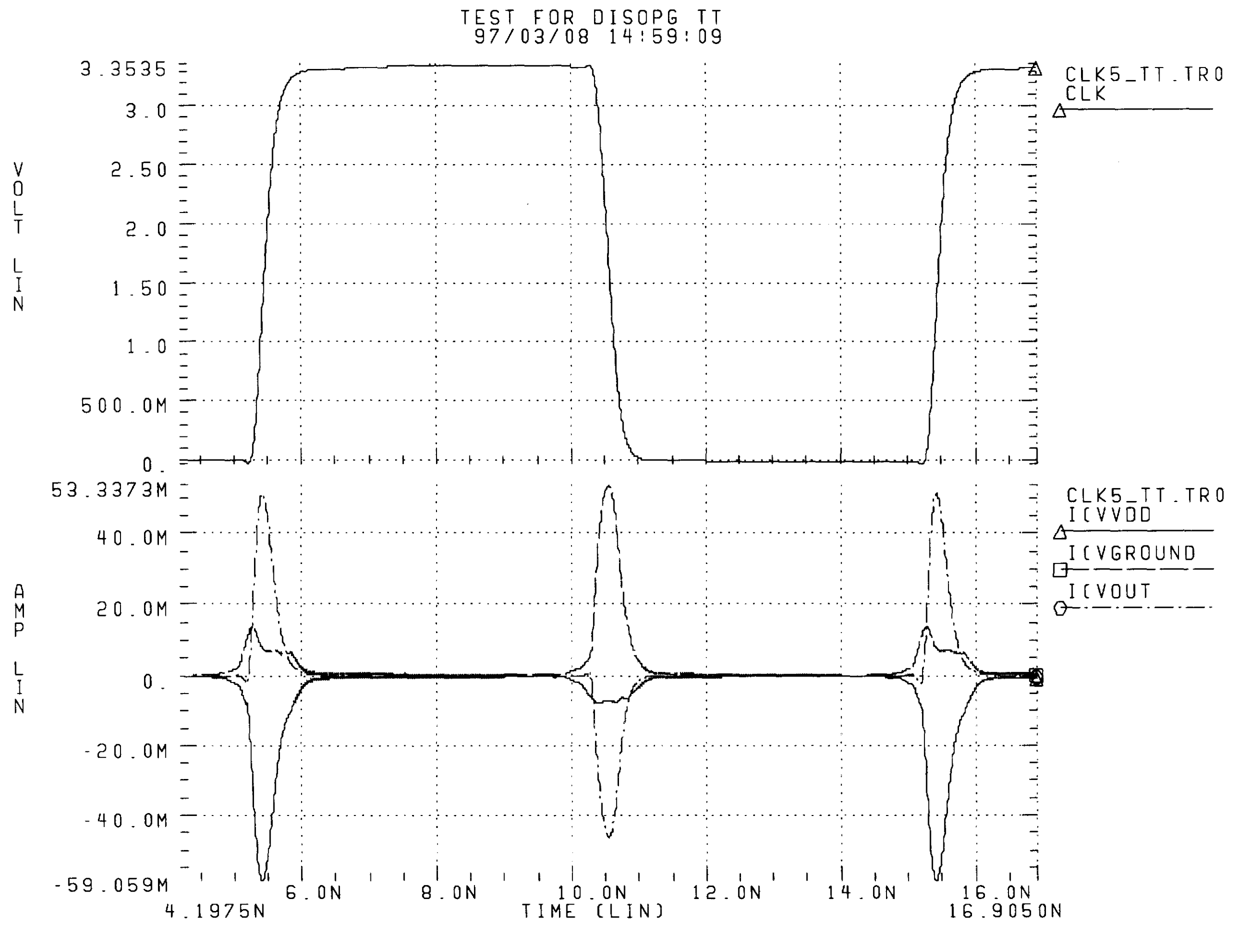
HSPICE waveforms for DISOPG driving a 5pF load



Sample DIDO Noise test: Vdd step from 3.3v to 3.0v

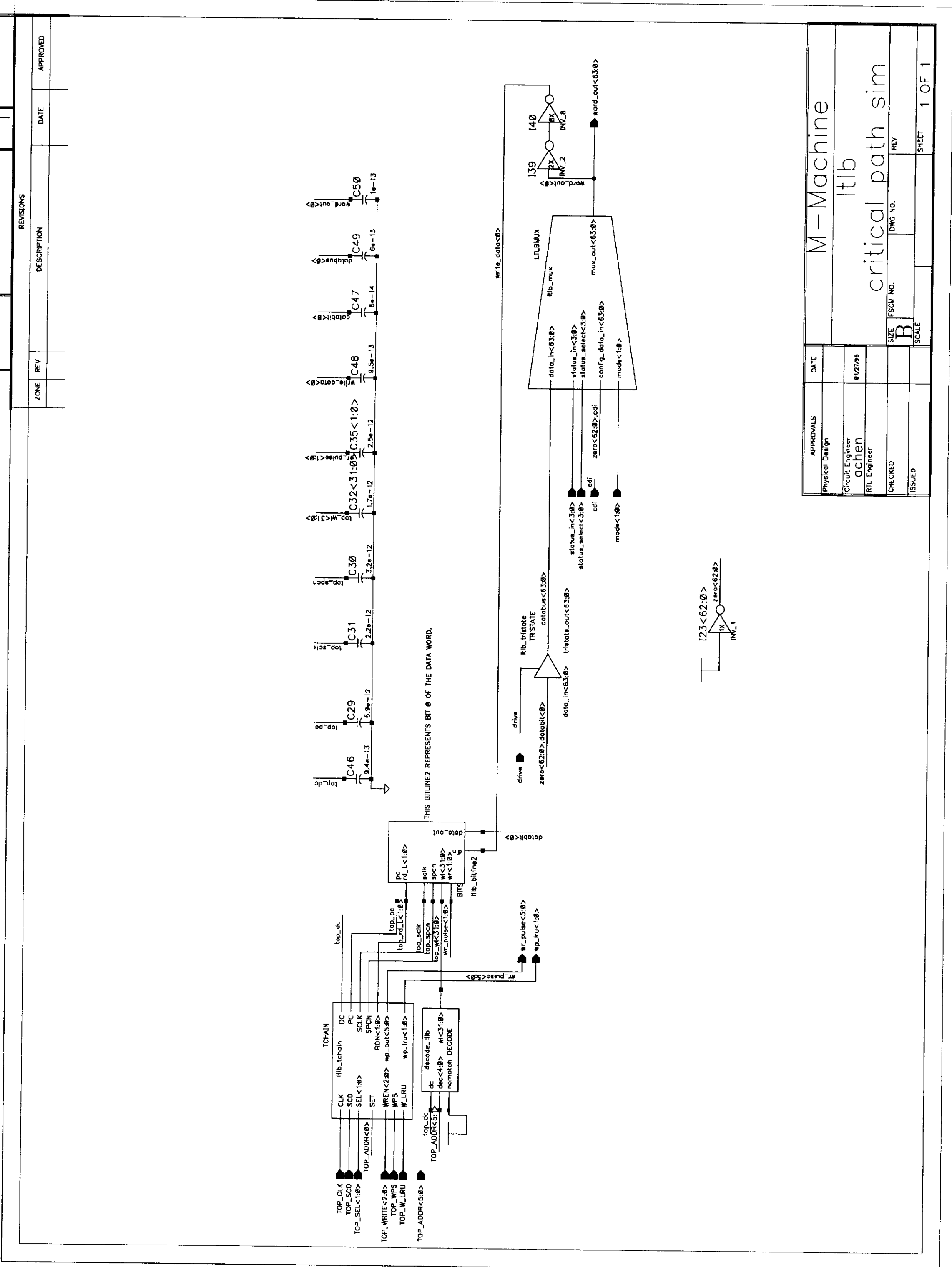


Power supply switching currents for final stage of DIDO



Power supply switching currents for DISOPG (total)

A.3 LTLB



Model used to evaluate signal timings in LTLB.

FSCM NO.	DWG NO.	SH 1	REV A.1.ØØ.ØØ

REVISIONS

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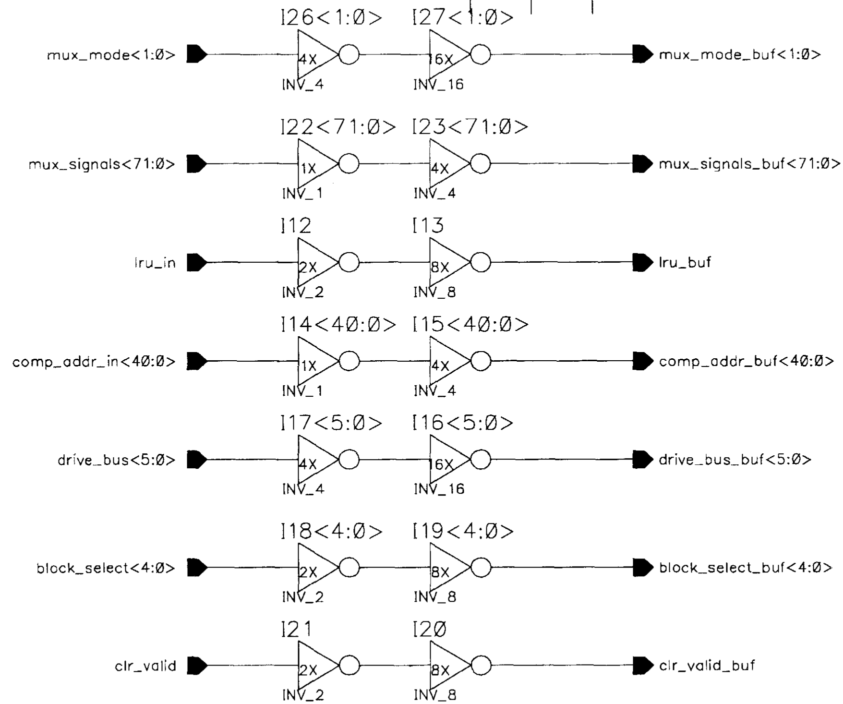

APPROVALS	DATE
Physical Design	
Circuit Engineer achen	Ø1/24/97
RTL Engineer Nick Carter	
CHECKED	
ISSUED	

M-Machine

ltlb

ltlb_inbuf_stdcells

SIZE A	FSCM NO.	DWG NO.	REV A.1.ØØ.ØØ
SCALE			SHEET 1 OF 1

FSCM NO.	DWG NO.	SH 1	REV A.1.ØØ.ØØ

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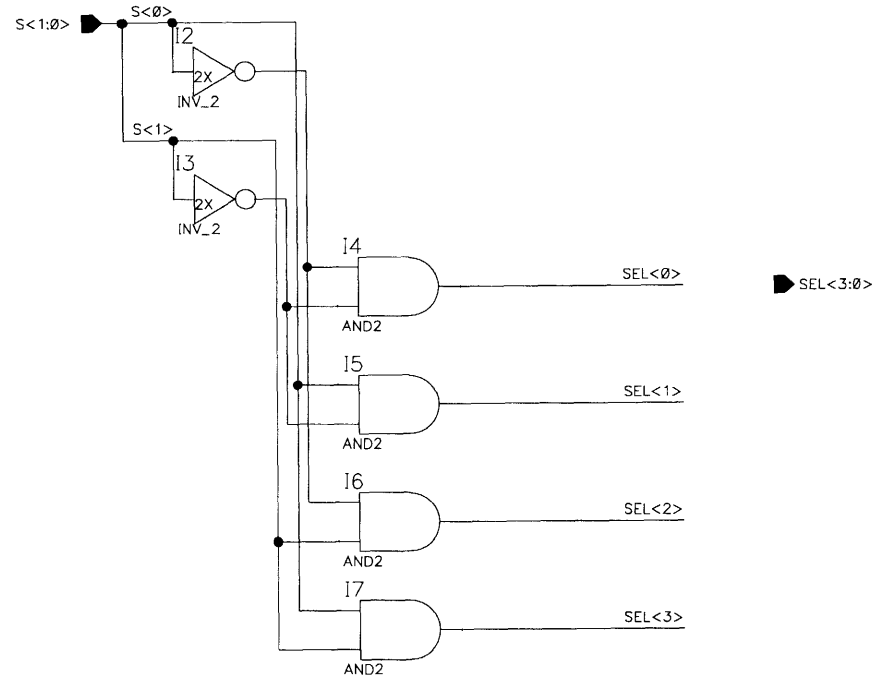

APPROVALS	DATE
Physical Design	
Circuit Engineer achen	11/20/96
RTL Engineer	
CHECKED	
ISSUED	

M—Machine

Itlb

Itlb_select_4

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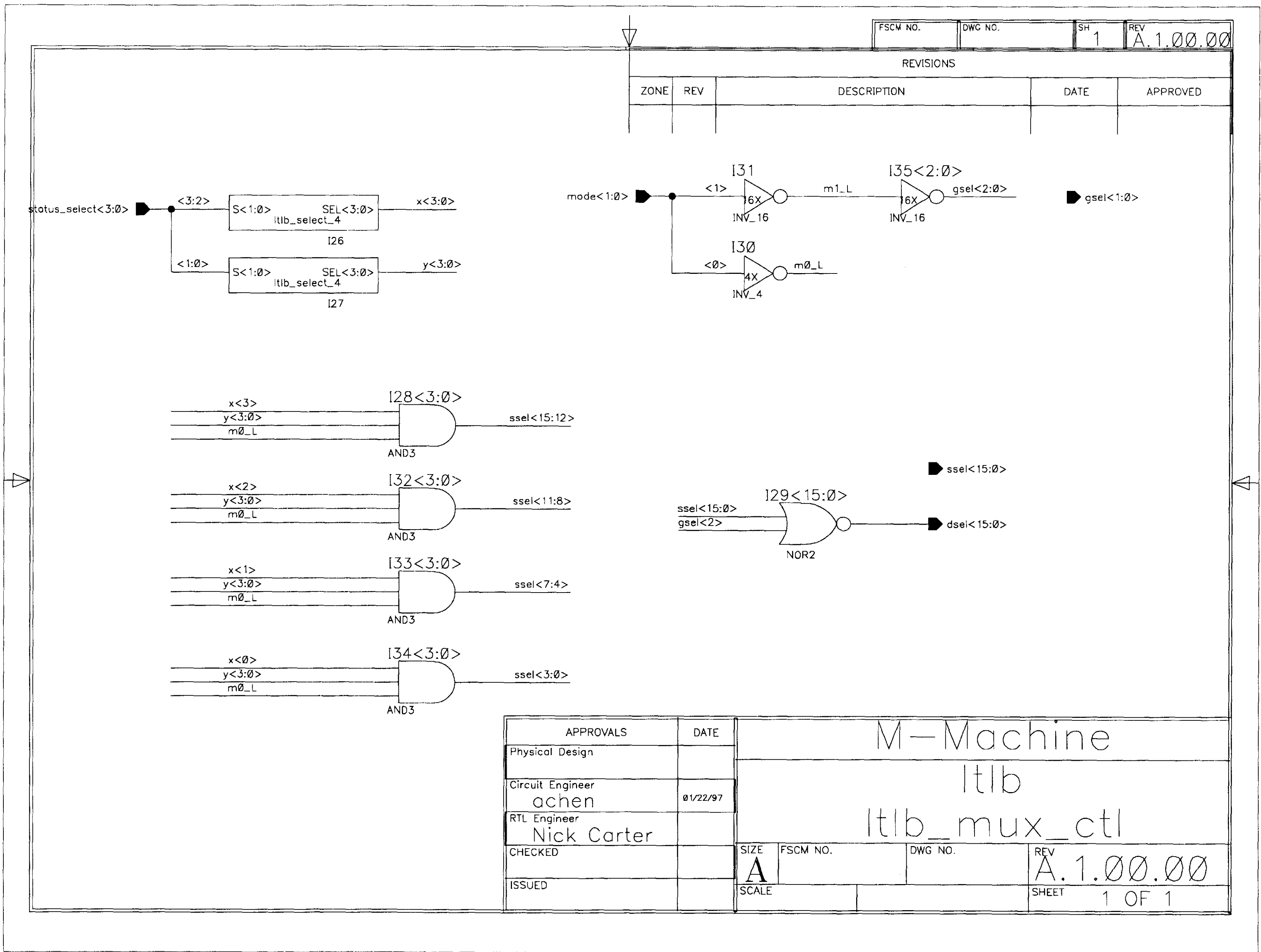

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SH 1
REV A.1.00.00
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DATE
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I30
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4X
INV_4
m0_L
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y<3:0>
m0_L
I28<3:0>
AND3
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x<2>
y<3:0>
m0_L
I32<3:0>
AND3
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y<3:0>
m0_L
I33<3:0>
AND3
ssel<7:4>
x<0>
y<3:0>
m0_L
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AND3
ssel<3:0>
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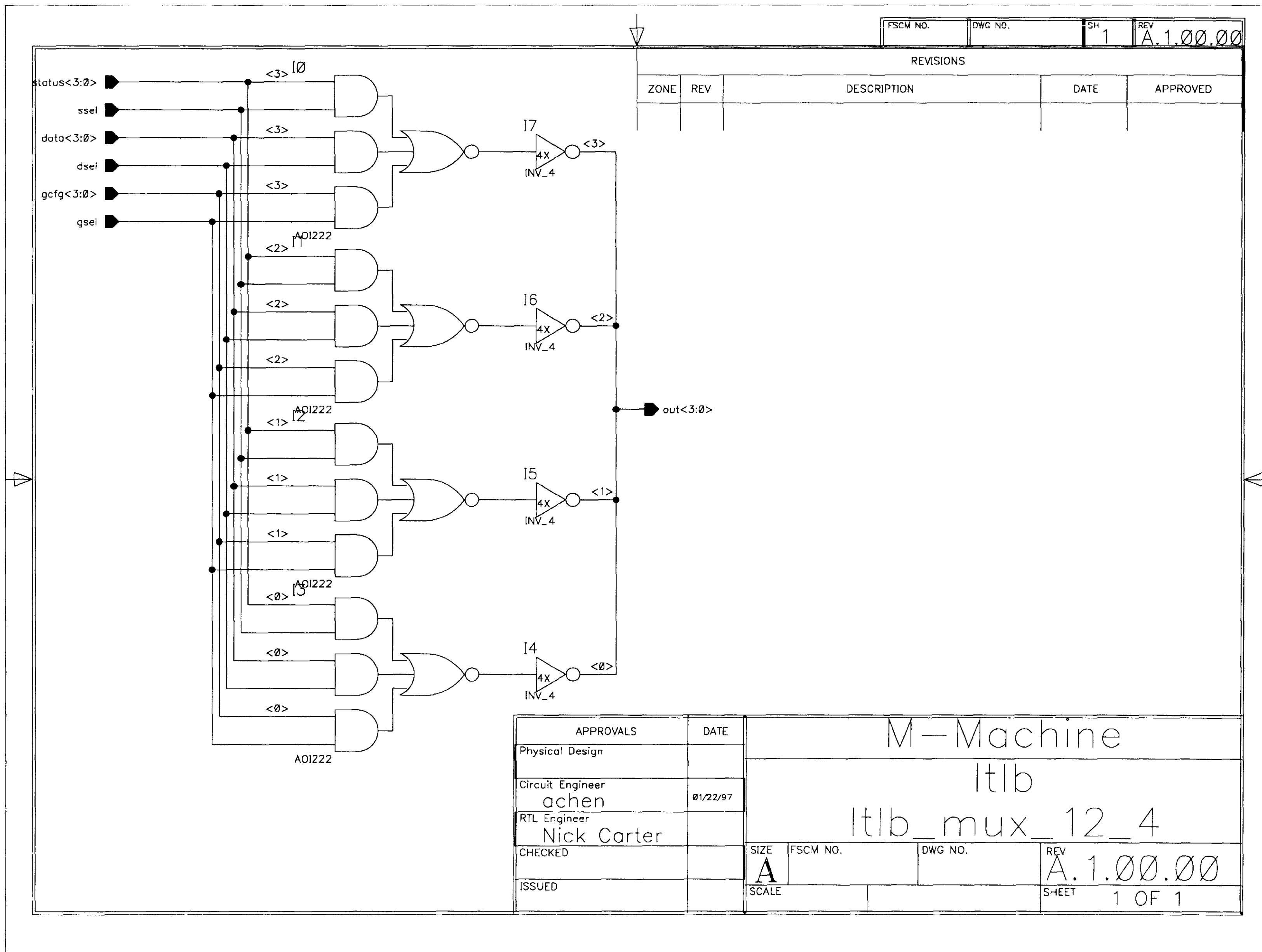
gsel<2>
NOR2
dsel<15:0>
APPROVALS
DATE
Physical Design
Circuit Engineer
achen
01/22/97
RTL Engineer
Nick Carter
CHECKED
ISSUED
M-Machine
ltlb
ltlb_mux_ctl
SIZE A
FSCM NO.
DWG NO.
REV A.1.00.00
SCALE
SHEET 1 OF 1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data<3:0>
dsel
gcfg<3:0>
gsel
I0
I1
I2
I3
AOI222
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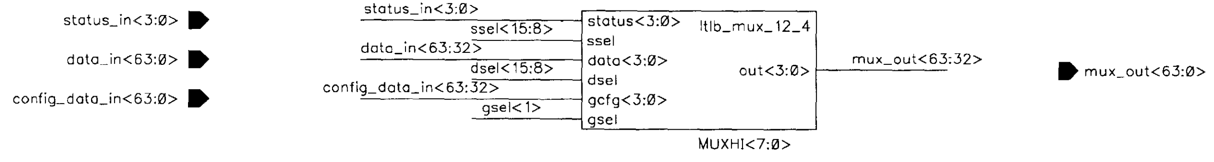
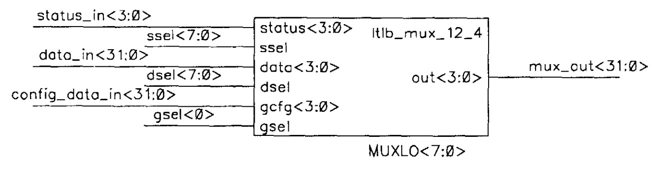
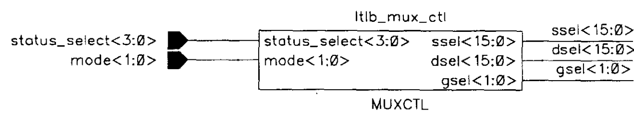
I6
I5
I4
4X
INV_4
out<3:0>
REVISIONS
ZONE
REV
DESCRIPTION
DATE
APPROVED
FSCM NO.
DWG NO.
SH
1
REV
A.1.00.00
APPROVALS
DATE
Physical Design
Circuit Engineer
achen
01/22/97
RTL Engineer
Nick Carter
CHECKED
ISSUED
M-Machine
ltlb
ltlb_mux_12_4
SIZE
A
FSCM NO.
DWG NO.
REV
A.1.00.00
SCALE
SHEET
1 OF 1

FSCM NO.	DWG NO.	SH	REV
		1	A.1.00.00

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED







APPROVALS	DATE
Physical Design	
Circuit Engineer achen	11/19/96
RTL Engineer Nick Carter	
CHECKED	
ISSUED	

M-Machine

ltlb

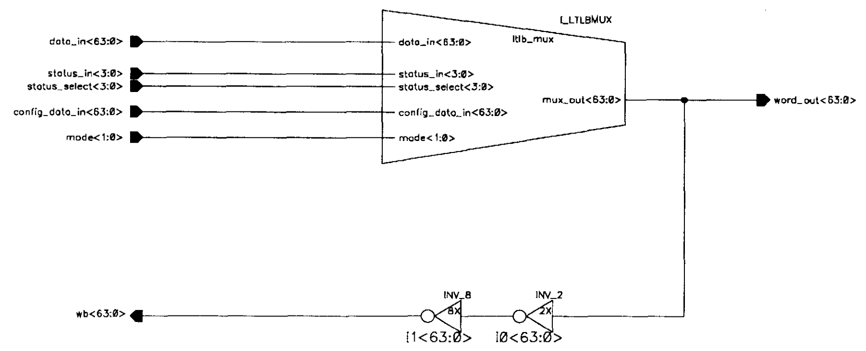
ltlb_mux

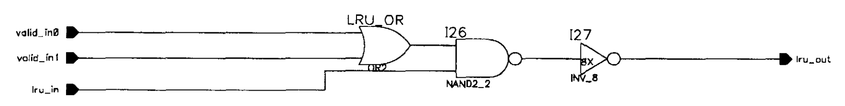
SIZE	FSCM NO.	DWG NO.	REV
A			A.1.00.00
SCALE			SHEET 1 OF 1

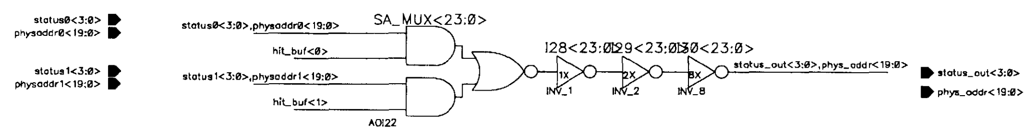
FSCM NO.	DWG NO.	SH	REV
		1	A.2.ØØ.ØØ

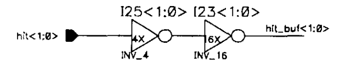
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED







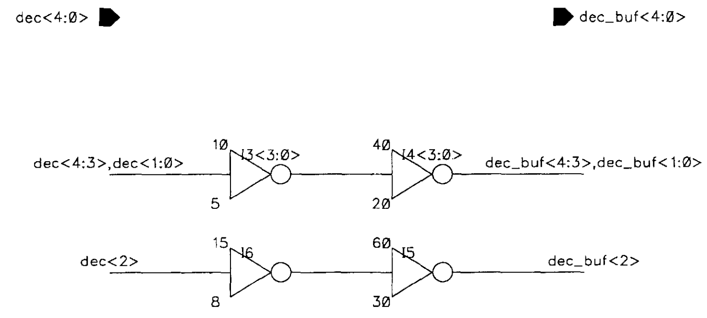


APPROVALS	DATE	
Physical Design		M-Machine
Circuit Engineer achen	01/22/97	ltlb
RTL Engineer Nick Carter		ltlb_top_stdcells
CHECKED		SIZE B · FSCM NO. · DWG NO. · REV A.2.ØØ.ØØ
ISSUED		SCALE · SHEET 1 OF 1

FSCM NO.	DWG NO.	SH	REV
		1	A.1.ØØ.ØØ

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
Physical Design	
Circuit Engineer achen	Ø1/24/97
RTL Engineer Nick Carter	
CHECKED	
ISSUED	

M-Machine

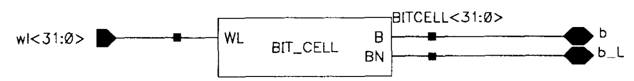
ltlb

ltlb_inbuf_addr

SIZE	FSCM NO.	DWG NO.	REV
A			A.1.ØØ.ØØ
SCALE			SHEET 1 OF 1

FSCM NO.	DWG NO.	SH	REV
		1	A.1.ØØ.ØØ

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
Physical Design	
Circuit Engineer achen	1Ø/23/96
RTL Engineer Nick Carter	5/22/96
CHECKED	
ISSUED	

M—Machine

ltlb

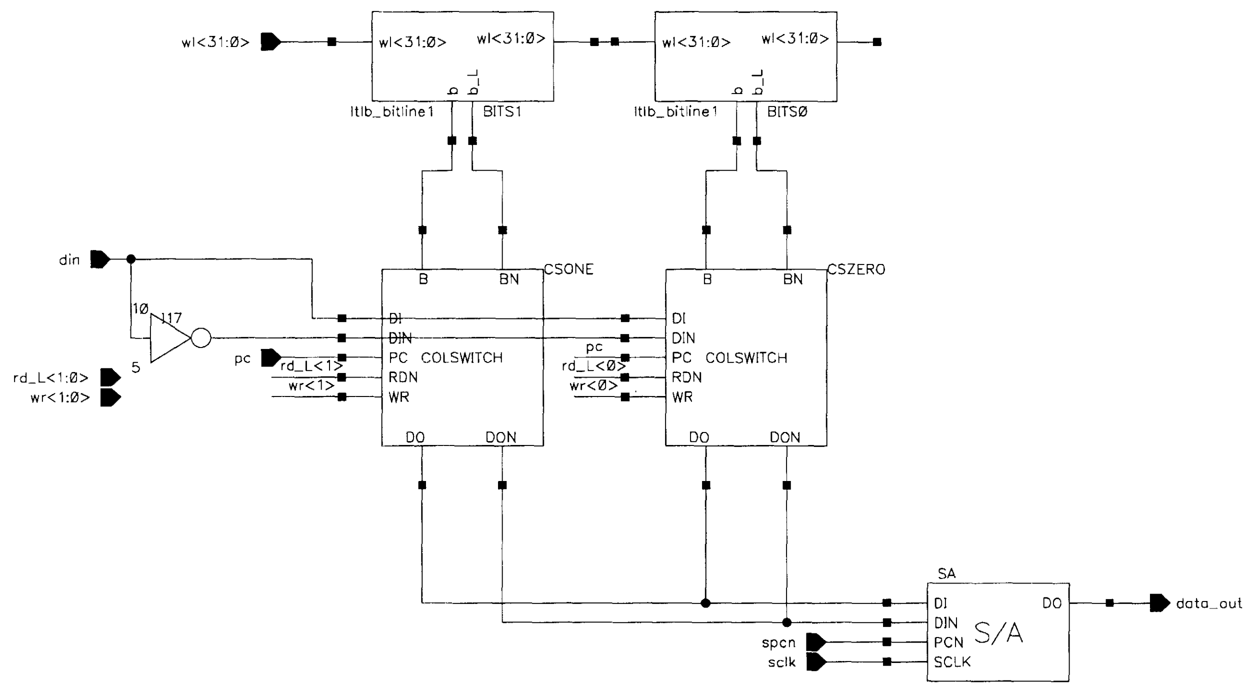
ltlb_bitline1

SIZE	FSCM NO.	DWG NO.	REV
A			A.1.ØØ.ØØ
SCALE			SHEET 1 OF 1

FSCM NO.	DWG NO.	SH 1	REV A.1.ØØ.ØØ

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
Physical Design	
Circuit Engineer Andrew Chen	1Ø/23/96
RTL Engineer Nick Carter	5/22/96
CHECKED	
ISSUED	

M–Machine

ltlb

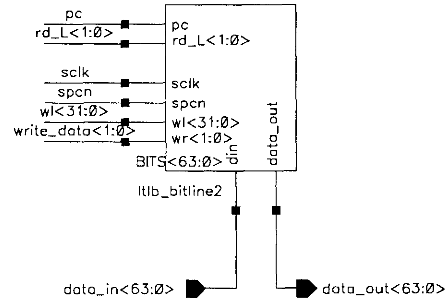
ltlb_bitline2

SIZE A	FSCM NO.	DWG NO.	REV A.1.ØØ.ØØ
SCALE			SHEET 1 OF 1

FSCM NO.	DWG NO.	SH 1	REV A.1.00.00

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



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spcn
wl<31:0>
write_data<1:0>

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APPROVALS	DATE
Physical Design	
Circuit Engineer Andrew Chen	10/31/96
RTL Engineer Nick Carter	5/22/96
CHECKED	
ISSUED	

M—Machine

ltlb

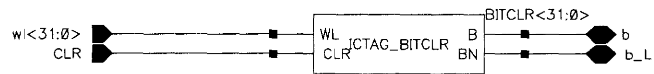
ltlb_array_status

SIZE A	FSCM NO.	DWG NO.	REV A.1.00.00
SCALE			SHEET 1 OF 1

FSCM NO.	DWG NO.	SH 1	REV A.1.ØØ.ØØ

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
Physical Design	
Circuit Engineer achen	11/20/96
RTL Engineer Nick Carter	
CHECKED	
ISSUED	

M-Machine

ltlb

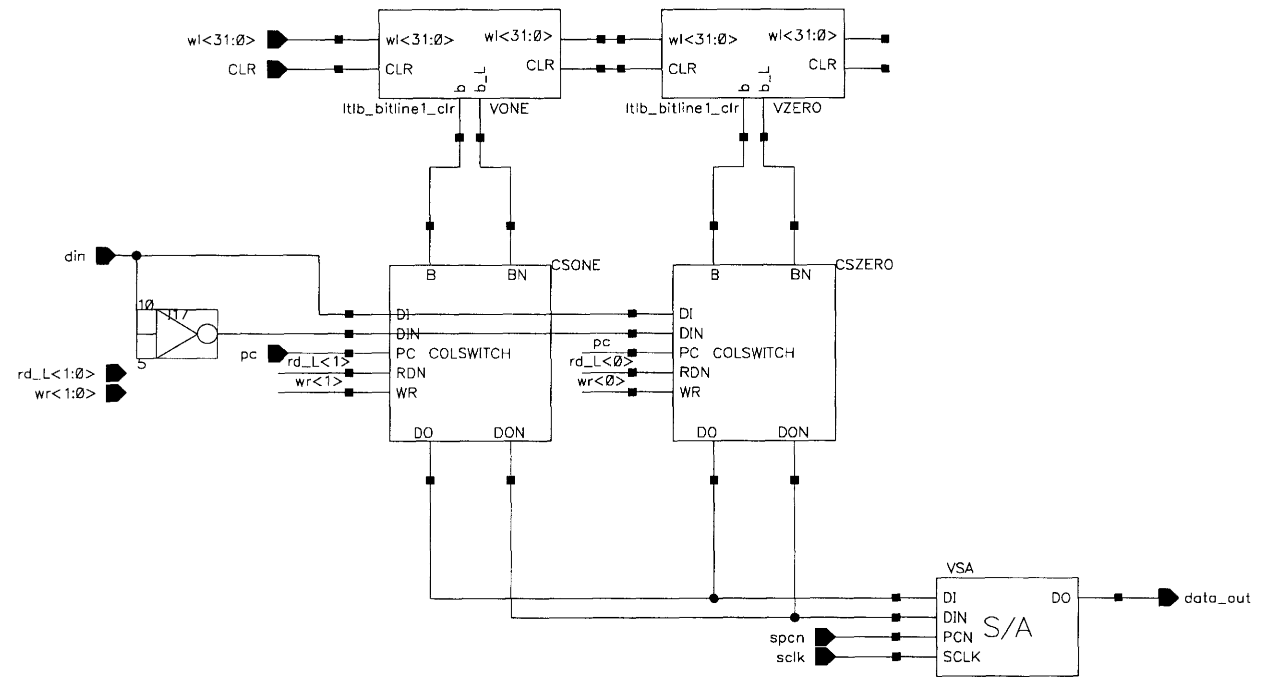
ltlb_bitline1_clr

SIZE A	FSCM NO.	DWG NO.	REV A.1.ØØ.ØØ
SCALE			SHEET 1 OF 1

FSCM NO.	DWG NO.	SH	REV
		1	A.1.ØØ.ØØ

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
Physical Design	
Circuit Engineer achen	12/12/96
RTL Engineer Nick Carter	5/22/96
CHECKED	
ISSUED	

M-Machine

ltlb

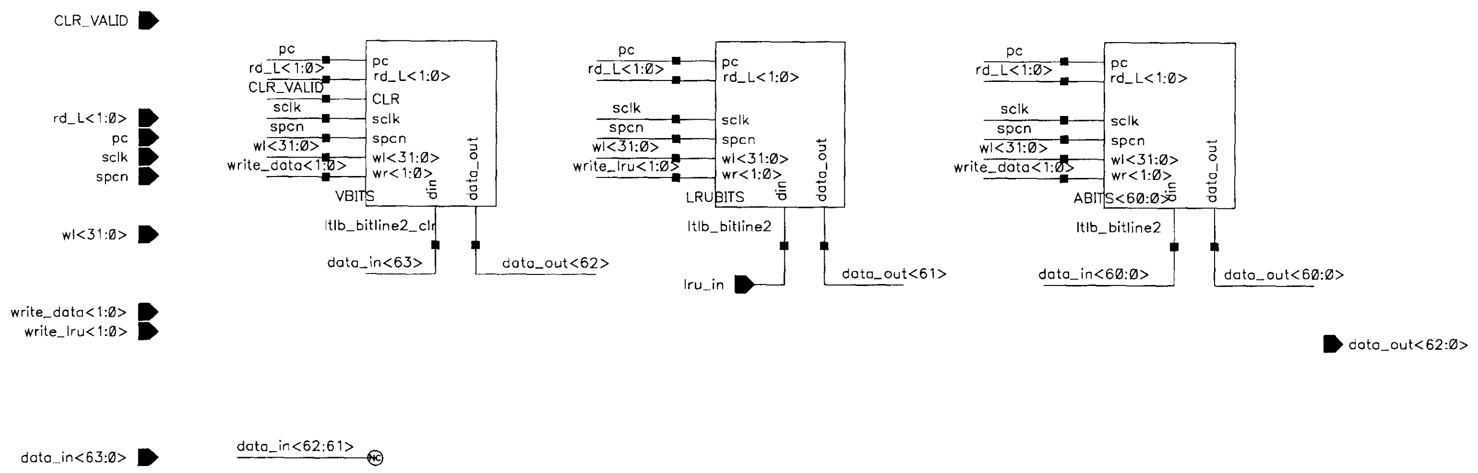
ltlb_bitline2_clr

SIZE	FSCM NO.	DWG NO.	REV
A			A.1.ØØ.ØØ
SCALE			SHEET 1 OF 1

FSCM NO.	DWG NO.	SH 1	REV A.1.00.00

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
Physical Design	
Circuit Engineer achen	01/22/97
RTL Engineer Nick Carter	5/22/96
CHECKED	
ISSUED	

M-Machine

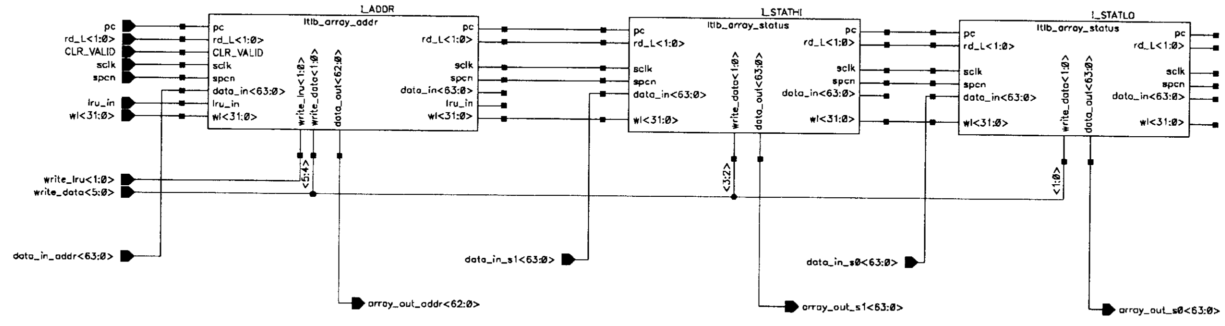
ltlb

ltlb_array_addr

SIZE	FSCM NO.	DWG NO.	REV
A			A.1.00.00
SCALE			SHEET 1 OF 1

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
Physical Design	
Circuit Engineer achen	01/23/97
RTL Engineer Nick Carter	
CHECKED	
ISSUED	

M-Machine

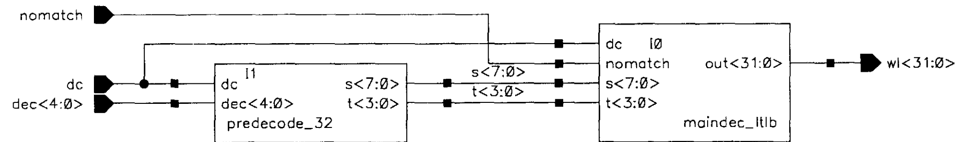
ltlb

ltlb_array_half

SIZE	FSCM NO.	DWG NO.	REV
B			A.1.00.00
SCALE			SHEET 1 OF 1

FSCM NO.	DWG NO.	SH 1	REV A.1.ØØ.ØØ

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



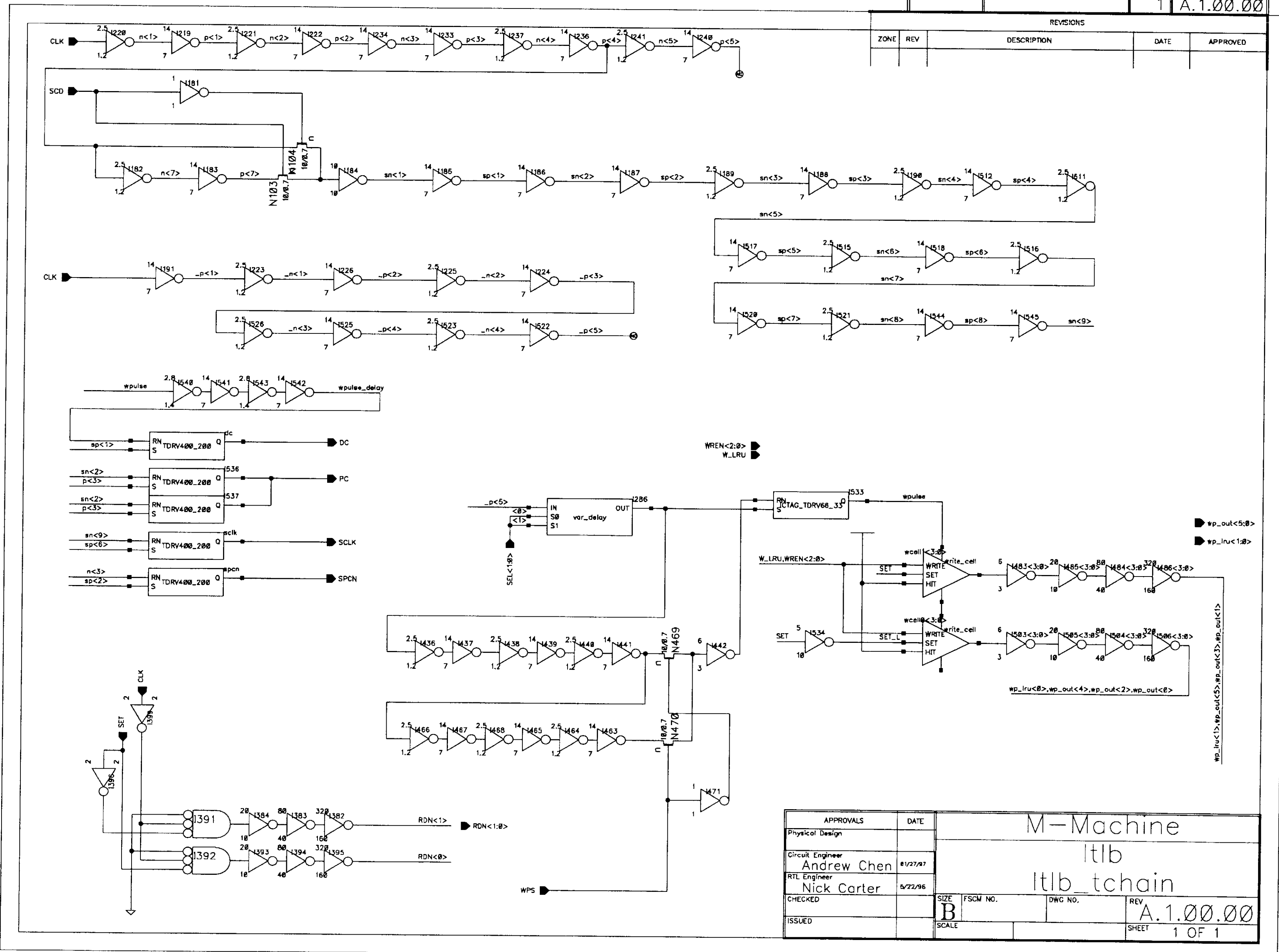
APPROVALS	DATE
Physical Design	
Circuit Engineer Parag Gupta	5/13/96
RTL Engineer Bill Dally	
CHECKED	
ISSUED	

M–Machine

ltlb

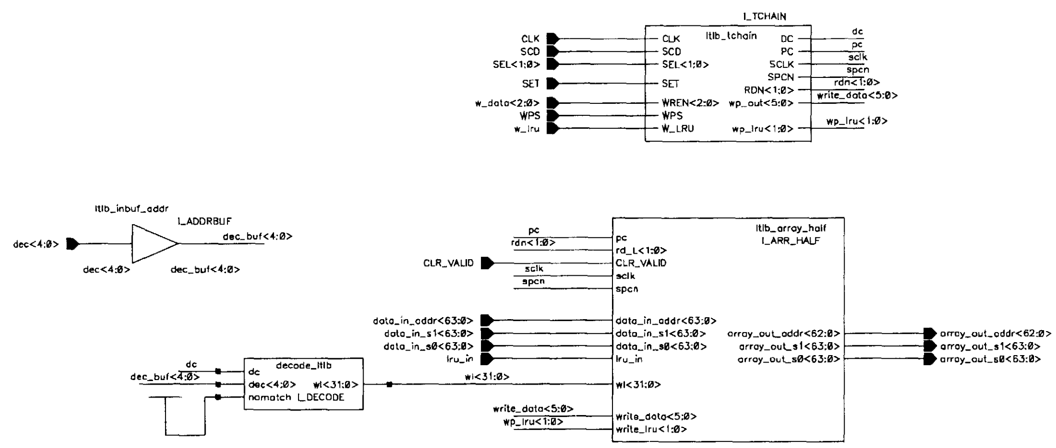
decode_ltlb

SIZE A	FSCM NO.	DWG NO.	REV A.1.ØØ.ØØ
SCALE			SHEET 1 OF 1


FSCM NO.
DWG NO.
SH 1
REV A.1.00.00
REVISIONS
ZONE
REV
DESCRIPTION
DATE
APPROVED
CLK
SCD
CLK
wpulse
wpulse_delay
TDRV400_200
DC
PC
SCLK
SPCN
WREN<2:0>
W_LRU
var_delay
SEL<1:0>
CTAG_TDRV68_33
W_LRU,WREN<2:0>
write_cell
wp_out<5:0>
wp_lru<1:0>
wp_lru<0>,wp_out<4>,wp_out<2>,wp_out<0>
wp_lru<1>,wp_out<5>,wp_out<3>,wp_out<1>
SET
RDN<1>
RDN<0>
RDN<1:0>
WPS
APPROVALS
DATE
Physical Design
Circuit Engineer
Andrew Chen
01/27/97
RTL Engineer
Nick Carter
5/22/96
CHECKED
ISSUED
M-Machine
ltlb
ltlb_tchain
SIZE B
FSCM NO.
DWG NO.
REV A.1.00.00
SCALE
SHEET 1 OF 1

FSCM NO.	DWG NO.	SH	REV
		1	A.1.ØØ.ØØ

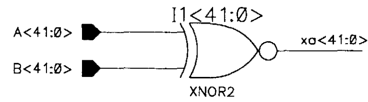
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

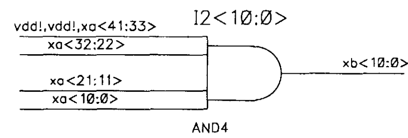


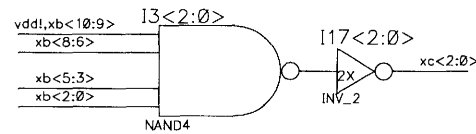
APPROVALS	DATE	
Physical Design		M—Machine
Circuit Engineer achen	02/18/97	ltlb
RTL Engineer Nick Carter		ltlb_half_custom
CHECKED		SIZE B · FSCM NO. · DWG NO. · REV A.1.ØØ.ØØ
ISSUED		SCALE · SHEET 1 OF 1

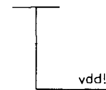
FSCM NO.	DWG NO.	SH 1	REV A.1.00.00

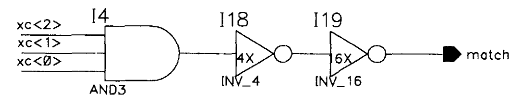
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED











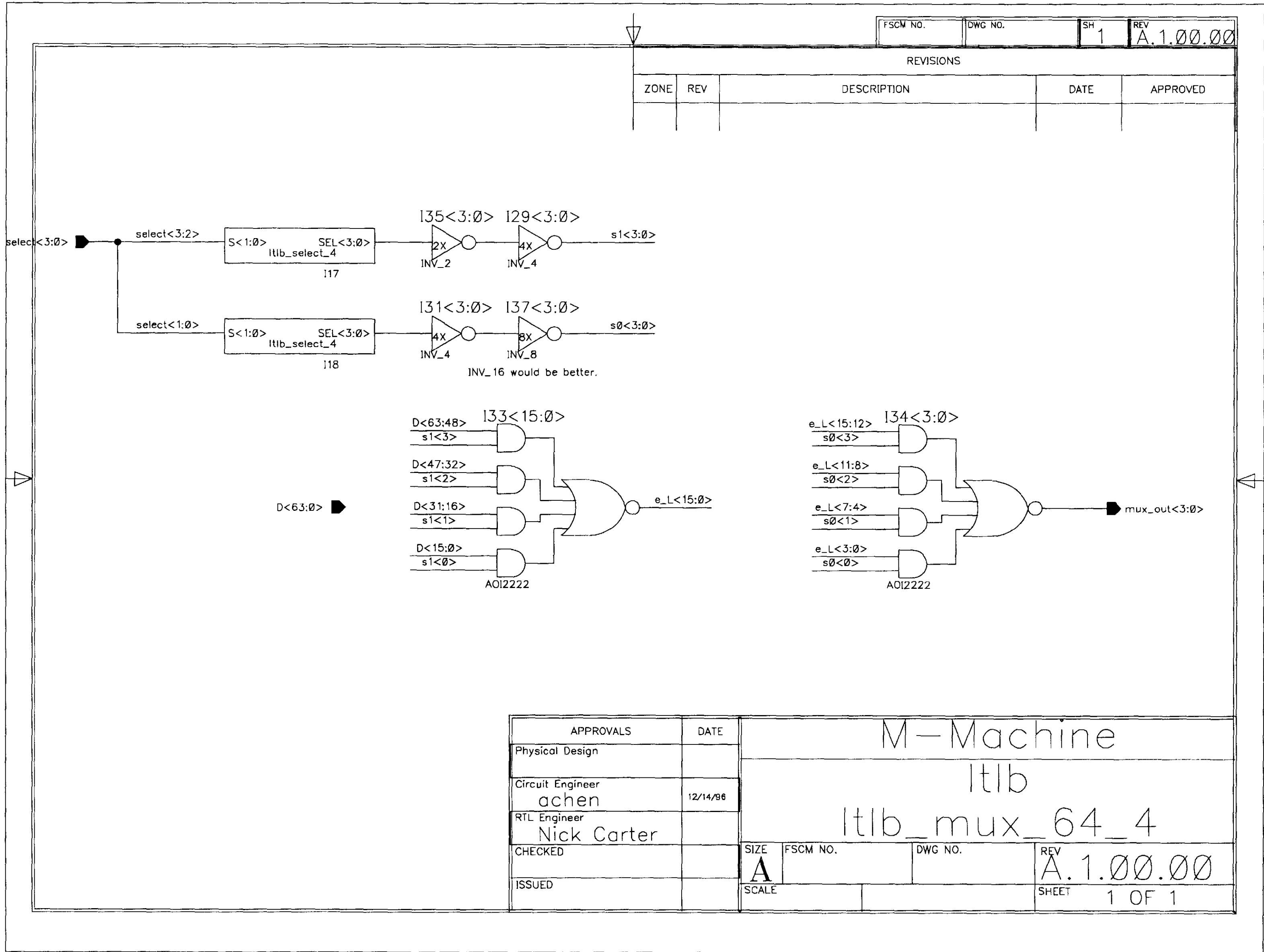
APPROVALS	DATE
Physical Design	
Circuit Engineer achen	03/02/97
RTL Engineer Nick Carter	
CHECKED	
ISSUED	

M—Machine

ltlb

ltlb_comp42_stdcell

SIZE A	FSCM NO.	DWG NO.	REV A.1.00.00
SCALE			SHEET 1 OF 1


FSCM NO.
DWG NO.
SH 1
REV A.1.ØØ.ØØ
REVISIONS
ZONE
REV
DESCRIPTION
DATE
APPROVED
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SEL<3:Ø>
ltlb_select_4
I17
I35<3:Ø>
I29<3:Ø>
2X
4X
INV_2
INV_4
s1<3:Ø>
select<1:Ø>
S<1:Ø>
SEL<3:Ø>
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I31<3:Ø>
I37<3:Ø>
4X
8X
INV_4
INV_8
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INV_16 would be better.
D<63:Ø>
I33<15:Ø>
D<63:48>
s1<3>
D<47:32>
s1<2>
D<31:16>
s1<1>
D<15:Ø>
s1<Ø>
AOI2222
e_L<15:Ø>
I34<3:Ø>
e_L<15:12>
sØ<3>
e_L<11:8>
sØ<2>
e_L<7:4>
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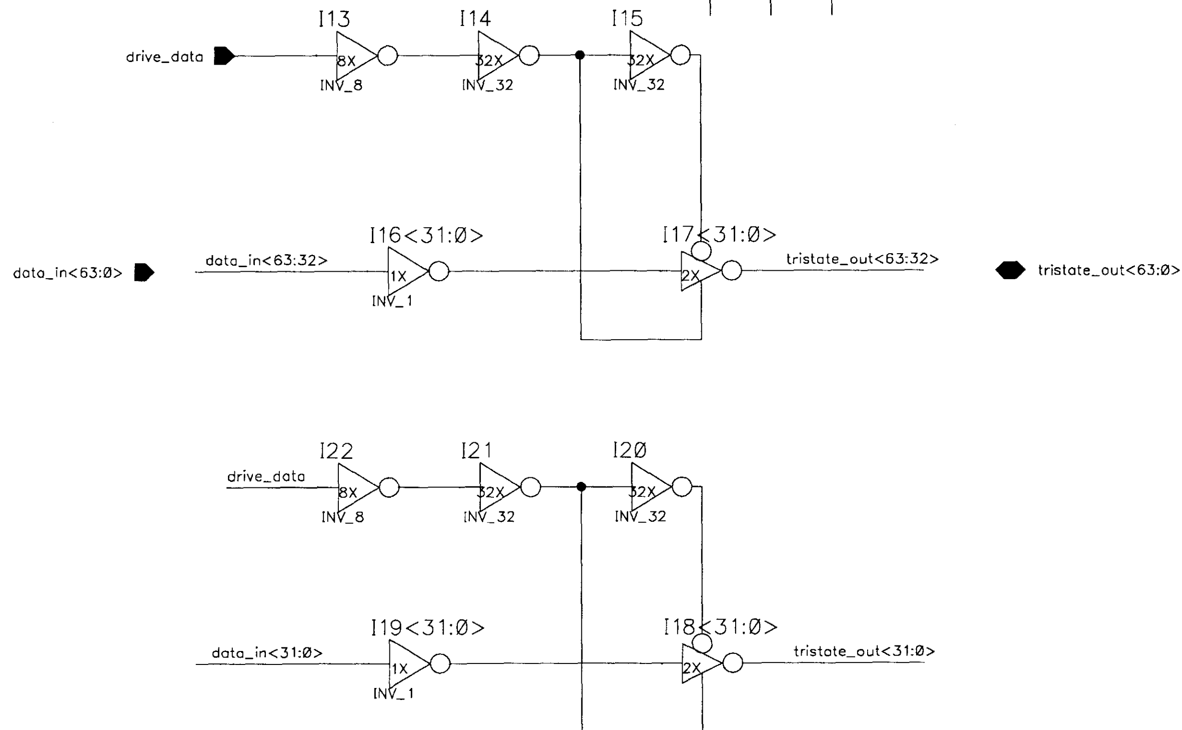
e_L<3:Ø>
sØ<Ø>
AOI2222
mux_out<3:Ø>
APPROVALS
DATE
Physical Design
Circuit Engineer
achen
12/14/96
RTL Engineer
Nick Carter
CHECKED
ISSUED
M-Machine
ltlb
ltlb_mux_64_4
SIZE A
FSCM NO.
DWG NO.
REV A.1.ØØ.ØØ
SCALE
SHEET 1 OF 1

FSCM NO.	DWG NO.	SH	REV
		1	A.1.ØØ.ØØ

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
Physical Design	
Circuit Engineer Andrew Chen	Ø1/23/97
RTL Engineer Nick Carter	
CHECKED	
ISSUED	

M-Machine

ltlb

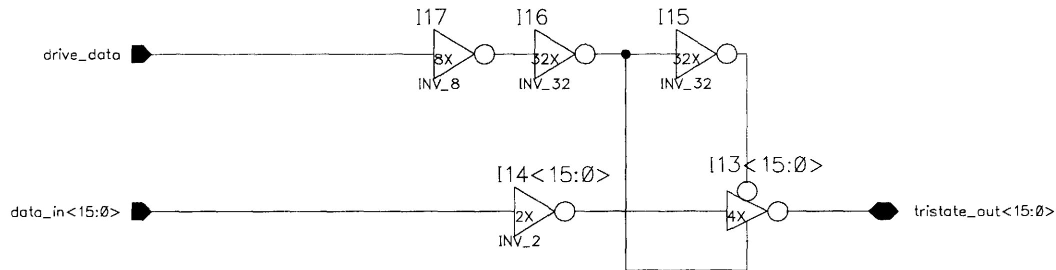
ltlb_tristate_2

SIZE	FSCM NO.	DWG NO.	REV
A			A.1.ØØ.ØØ
SCALE			SHEET 1 OF 1

FSCM NO.	DWG NO.	SH	REV
		1	A.1.ØØ.ØØ

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
Physical Design	
Circuit Engineer achen	Ø1/23/97
RTL Engineer	
CHECKED	
ISSUED	

M–Machine

ltlb

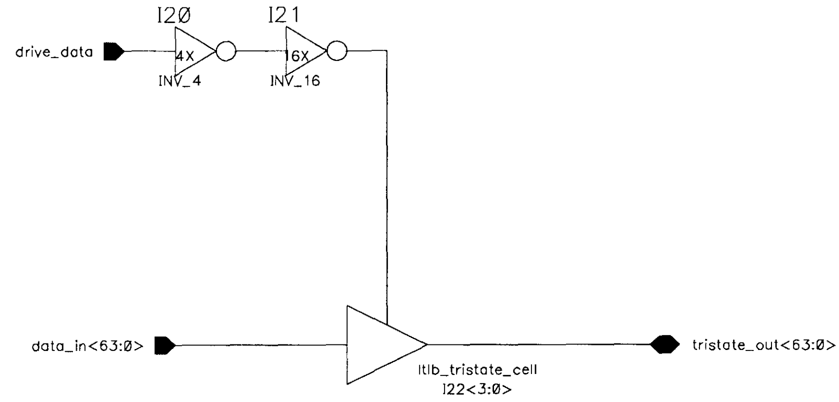
ltlb_tristate_cell

SIZE	FSCM NO.	DWG NO.	REV
A			A.1.ØØ.ØØ
SCALE		SHEET	1 OF 1

FSCM NO.	DWG NO.	SH	REV
		1	A.1.00.00

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
Physical Design	
Circuit Engineer Andrew Chen	01/23/97
RTL Engineer Nick Carter	
CHECKED	
ISSUED	

M-Machine

ltlb

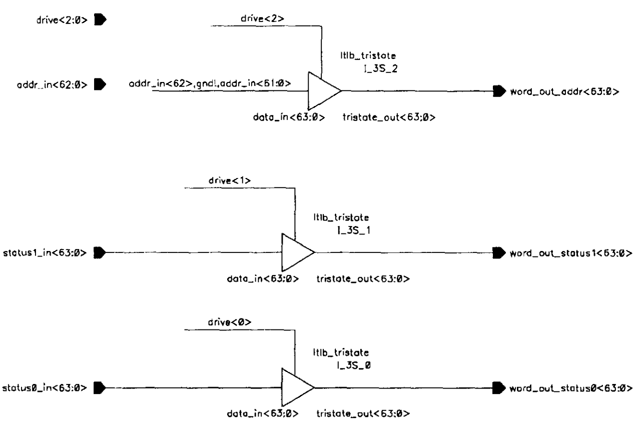
ltlb_tristate

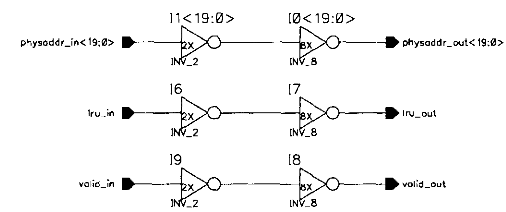
SIZE	FSCM NO.	DWG NO.	REV
A			A.1.00.00
SCALE			SHEET 1 OF 1

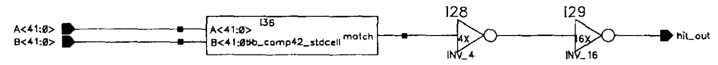
FSCM NO.	DWG NO.	SH	REV
		1	A.2.00.00

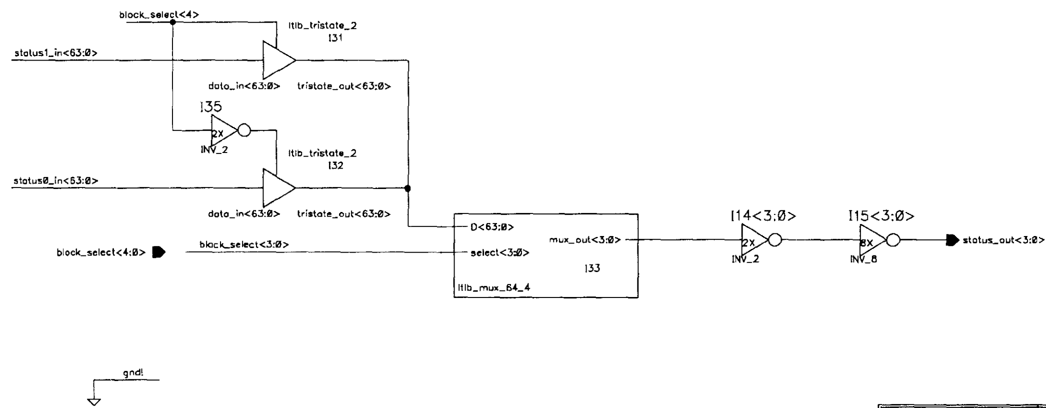
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED









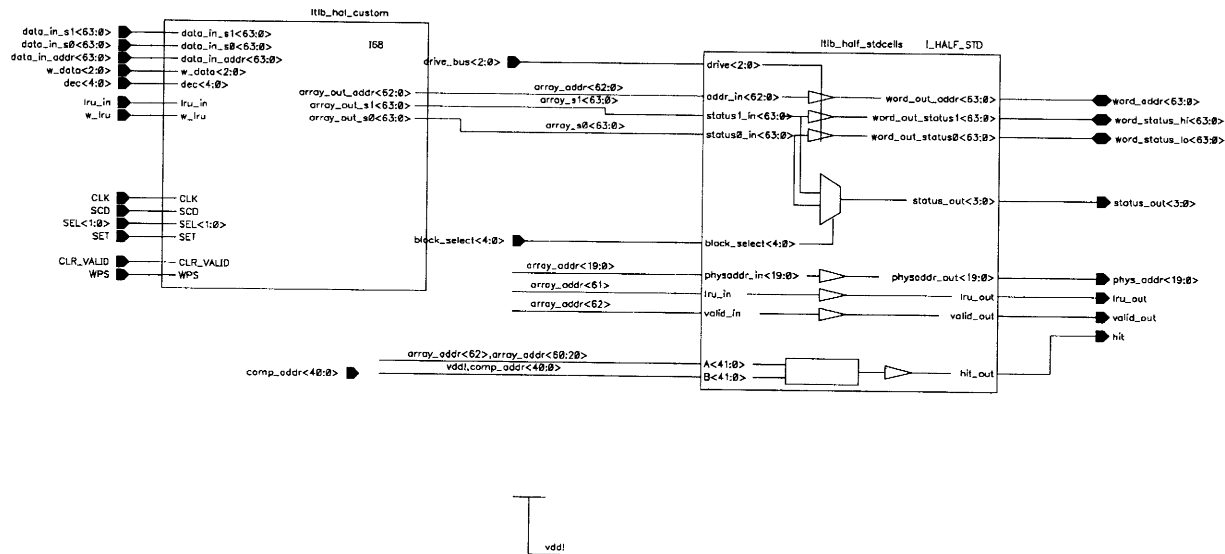
gnd!

APPROVALS	DATE	M-Machine
Physical Design		ltlb
Circuit Engineer achen	01/23/97	ltlb_half_stdcells
RTL Engineer Nick Carter		
CHECKED		SIZE B / FSCM NO. / DWG NO. / REV A.2.00.00
ISSUED		SCALE / SHEET 1 OF 1

FSCM NO.	DWG NO.	SH 1	REV A.2.00.00

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
Physical Design	
Circuit Engineer achen	01/11/97
RTL Engineer Nick Carter	
CHECKED	
ISSUED	

M-Machine

ltlb

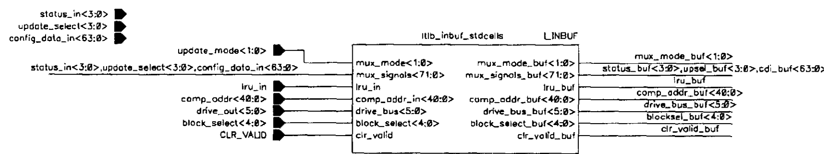
ltlb_half

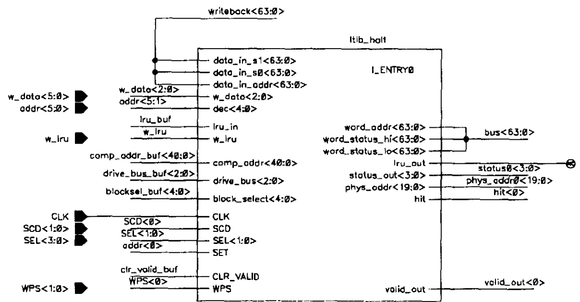
SIZE B	FSCM NO.	DWG NO.	REV A.2.00.00
SCALE			SHEET 1 OF 1

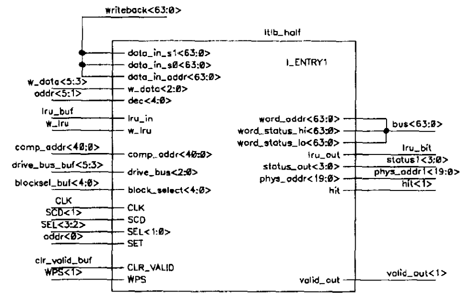
FSCM NO.	DWG NO.	SH	REV
		1	A.1.ØØ.ØØ

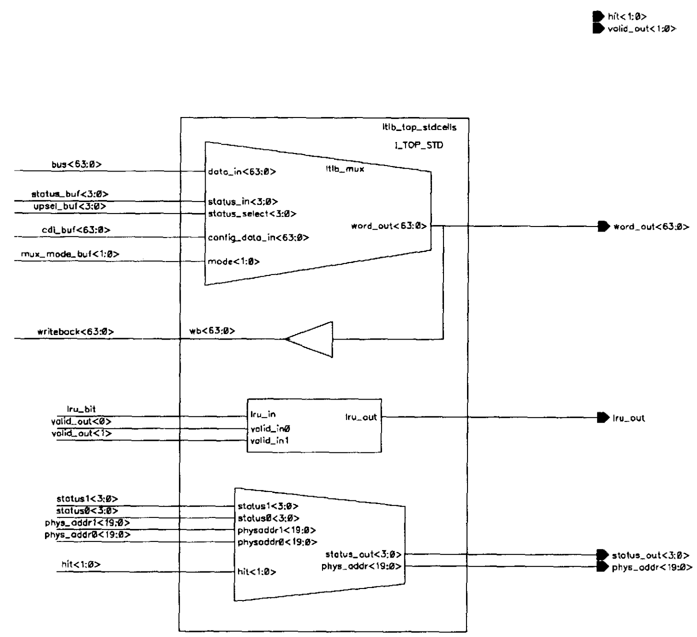
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



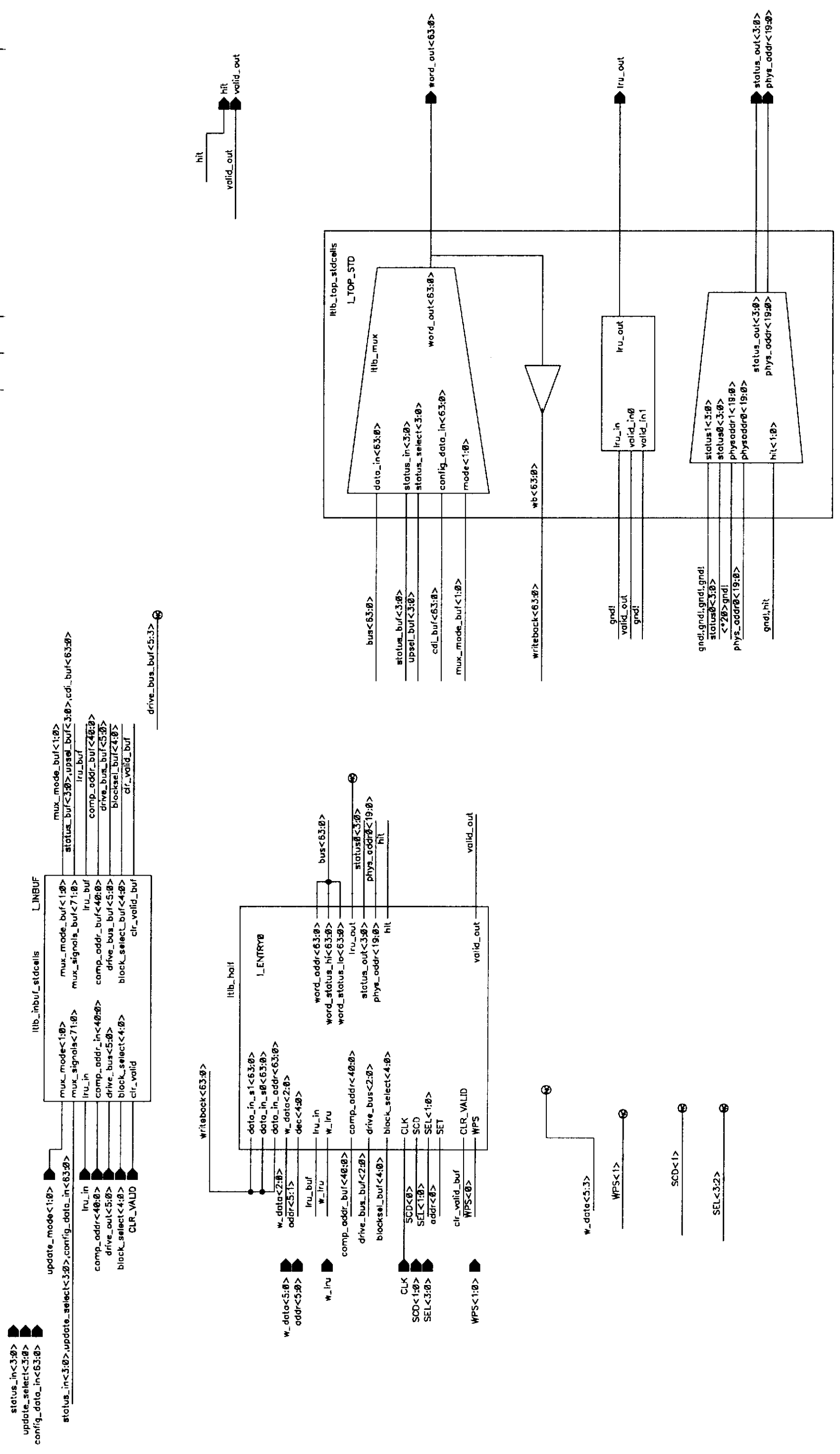






APPROVALS	DATE	
Physical Design		M—Machine
Circuit Engineer achen	01/24/97	ltlb
RTL Engineer Nick Carter		LTLBRAM
CHECKED		SIZE B · FSCM NO. · DWG NO. · REV A.1.ØØ.ØØ
ISSUED		SCALE · SHEET 1 OF 1

Early LTLBRAM Top-Level Schematic (128 entries)



Final LTLBRAM Top-Level Schematic (64 entries)

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I Have The Final Phrase... I.H.T.F.P...