Strained SiGe-channel p-MOSFETs: Impact of Heterostructure Design and Process Technology

by

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Abstract

Conventional Si CMOS intrinsic device performance has improved by 17% per year over the last 30 years through scaling of the gate length of the MOSFET along with process innovations such as the super-steep retrograde channel doping and ultra shallow source-drain junctions. In order to continue performance scaling with gate length for the 90 nm node and beyond (physical gate length 45 nm) an increase in the carrier mobility through the introduction of strain to the Si channel was required. To continue this scaling down to gate lengths of 10 nm new channel materials with superior mobility will be required.

Superior hole mobility (up to 10X enhancement over bulk Si channels) and compatibility with mainstream Si processing technology make compressively strained SiGe an attractive channel material for sub 45 nm p-MOSFETs. This research investigates strained SiGe as a suitable channel material for p-MOSFETs using SiGe grown pseudomorphically on both relaxed SiGe and bulk Si substrates. Some of the fundamental and technological challenges that must be faced in order to incorporate SiGe channel materials are addressed, including the impact of heterostructure composition and SiGe channel thickness on mobility and MOSFET off-state leakage, as well as critical thickness and thermal budget constraints. In particular, the impact of the strained channel thickness on mobility is analyzed in detail. This work provides a detailed analysis of the design space for the SiGe heterostructure required to evaluate the trade off's between mobility enhancement, subthreshold characteristics and ease of integration with conventional CMOS processing in order to determine the optimum device structure.

Thesis Supervisor: Judy L. Hoyt
Title: Professor of Electrical Engineering

To My Parents

For their perseverance.

To My Husband Oliver

Honey you are the rock,

Upon which I stand.

To Sorcha

When you came in my life,

You changed my world.

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Chapter 1

Introduction

Historically, CMOS intrinsic performance has improved by 17% per year over the last few decades through increases in the virtual source injection velocity [1]. This performance improvement has been realized by scaling the gate length (L_G) combined with innovations in channel and source drain engineering including ultra shallow junctions, halo doping and super-steep retrograde channel doping [2]. In order to continue performance scaling at the 90 nm node (~45 nm gate length) increased carrier mobility was required. Increased electron and hole mobility has been achieved through process introduced strain of the bulk Si channel by uniaxial tensile and compressive strain respectively [3]. However, new higher mobility channel materials will be required to continue device performance scaling to the 10 nm gate length [1].

Strained SiGe and Ge channel pMOSFETs have shown excellent mobility enhancement over bulk Si channels, with hole mobility enhancements of up to 10X demonstrated [4] [5]. Compatibility with mainstream Si processing technology makes compressively strained SiGe an attractive channel material for sub 45 nm p-MOSFETs. Hole mobility in compressively SiGe channel MOSFETs has been shown to increase with increasing Ge composition [4]. However, strain and increasing Ge composition cause the bandgap of the alloy to decrease in comparison to the bandgap of bulk Si. This results in an increase in diode leakage due to BBT. A Si cap is required to form a low electronic defect interface between the gate dielectric and the channel. If the Si cap is too thick, a parasitic channel can form in the cap and mobility can degrade,

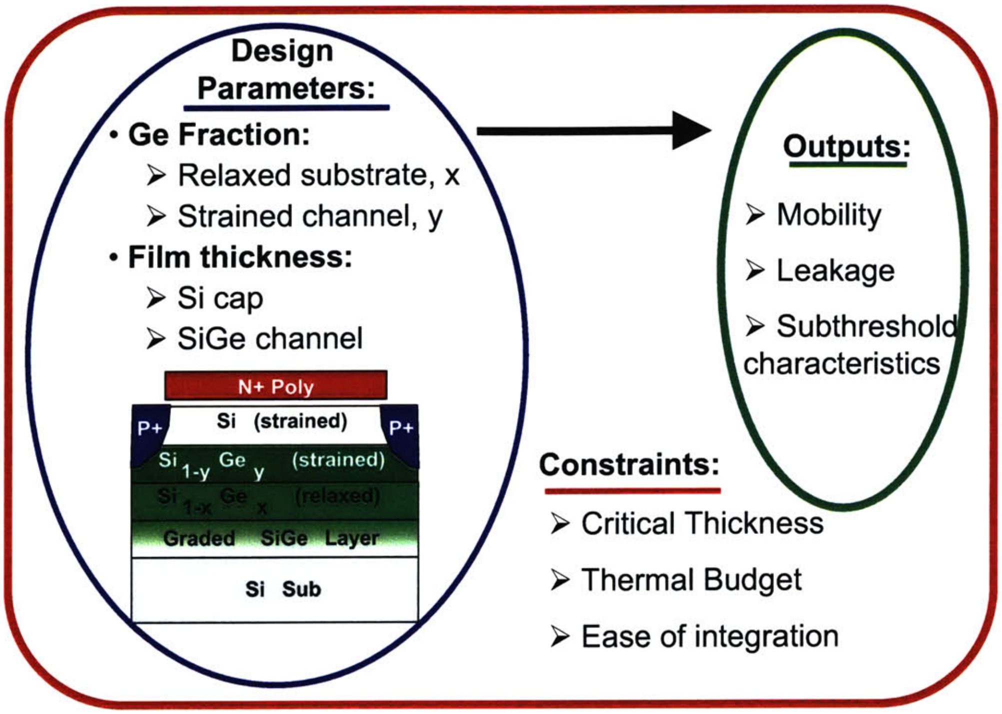


Figure 1-1: Schematic of strained SiGe pMOSFET heterostructure design space investigated in this thesis.

especially at high N_{inv} [6]. Furthermore, if the Si cap is too thin mobility can degrade due to the diffusion of Ge from the channel to the Si/oxide interface. The thermal budget must be kept low in order to minimize Ge diffusion which can reduce the peak Ge composition in the strained SiGe channel and lead to a reduction in mobility [7]. Finally, in order to form a high quality strained SiGe channel the channel thickness must be kept below the critical thickness [8]. However, limiting channel thickness can lead to a reduction in mobility compared to a bulk channel MOSFET [9].

This work provides a detailed analysis of the design space for the SiGe heterostructure, required to evaluate the trade off's between mobility enhancement, subthreshold characteristics and ease of integration with conventional CMOS processing in order to determine the optimum device structure.

Section 1.1 will give an overview of the goals of this thesis. Section 1.2 will outline the material covered in each chapter.

1.1 Thesis Goals

This research investigates strained SiGe as a suitable channel material for p-MOSFETs using SiGe grown pseudomorphically on both relaxed SiGe and bulk Si substrates. Some of the fundamental and technological challenges that must be faced in order to incorporate SiGe channel materials are addressed. To optimize device performance for the SiGe heterostructure it is important to understand the design space. A schematic of the design space investigated in this thesis is shown in Figure 1-1. It is divided into 3 main sections:

1. Inputs: Device Design Parameters

2. Outputs: Device Electrical Characteristics

3. Processing Constraints

Variations of the device inputs including Si cap and strained SiGe channel thickness, and the Ge fraction in the strained SiGe and relaxed SiGe substrate will be investigated in detail. The impact of the design parameters on the device electrical characteristics including hole mobility, leakage and subthreshold characteristics will be considered. There are some constraints on the device design including strained film critical thickness, thermal budget and ease of integration which will be addressed.

This thorough investigation of the design space will allow evaluation of the device trade-offs, including the impact of heterostructure composition and SiGe channel thickness on mobility and MOSFET off-state leakage, as well as critical thickness and thermal budget constraints. In particular, the impact of the strained channel thickness on mobility will be considered, which is especially important in deciding between a virtual SiGe substrate or bulk Si substrate. Understanding these trade-offs is required in order to tailor the SiGe heterostructure for optimum device performance.

1.2 Outline

In Chapter 2 some of the relevant existing theory on the band structure, hole transport and critical thickness constraints is reviewed. In Chapter 3 extraction of valence band offsets through inverse modeling, necessary for accurate simulation of the SiGe heterostructure, is shown. The impact of the design parameters on hole mobility and subthreshold characteristics is discussed in Chapters 4 and 5 respectively. Evaluation of Laser Spike Annealing as a low thermal budget solution for SiGe processing is covered in Chapter 6. Finally, in Chapter 7 all the experimental results are summarized and the trade-offs examined. The major contributions and suggestions for future are also covered.

Chapter 2

Theory

In this chapter some basic background theory necessary for understanding the work carried out in this thesis will be presented. It is essential to know the bandstructure of relaxed and strained Si and SiGe in order to understand the behavior of SiGe heterostructure devices. Section 2.1 will review the published work on the SiGe bandstructure. A large section of this thesis addresses hole mobility in SiGe heterostructures. An overview of hole transport will be given in Section 2.2, with particular attention to the impact of strain on effective mass, and a brief review of scattering mechanisms in semiconductor materials. A background to band-to-band tunneling (BBT) and critical thickness constraints will be covered in Sections 2.3 and 2.4 respectively. Finally a brief review of the mobility extraction method used in this work will be given.

2.1 Bandstructure

In this section the impact of Ge composition and strain on the bandstructure of strained and relaxed SiGe and strained Si/SiGe heterostructures will be discussed. The aim of this section is to give an overview of the impact of strain and Ge composition on bandstructure and band offsets between materials in the SiGe heterostructure, and to identify the origin of the parameters used in some of the electrical simulations carried out in this thesis. It is important to note that the alignment of the bands

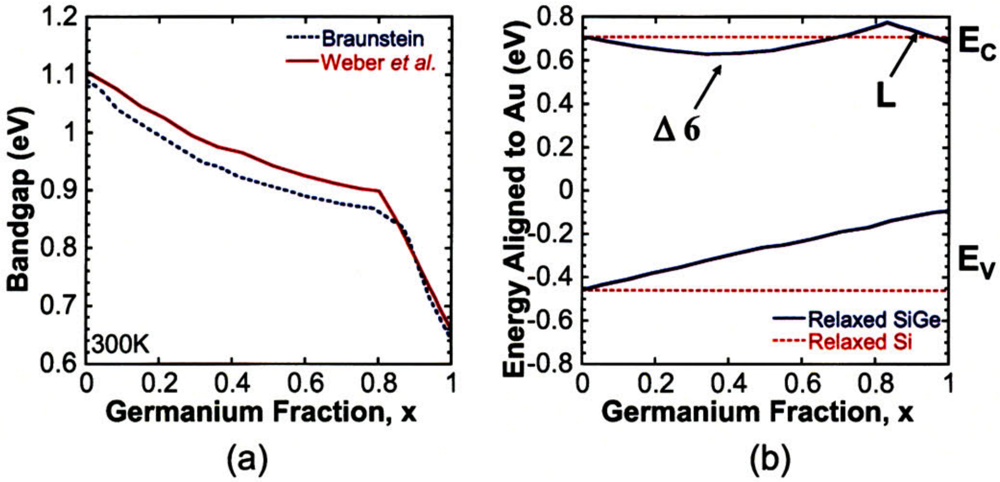


Figure 2-1: (a) Measured bandgap for relaxed SiGe alloy from Braunstein *et al.* [10] and Weber *et al.* [11]. (b) Conduction and valence band position relative to Au from Fischetti *et al.* [13]. The conduction band is based on experimental results from Morar *et al.* [14], and the valence band from experimental data for the energy gap from Weber *et al.* [11].

between materials in the heterostructure is just as important as the bandgap of the materials, as it is the band offsets that determine the confinement of carriers in the heterostructure.

2.1.1 Bandstructure of Relaxed SiGe

The original work to determine the bulk SiGe band structure was performed by Braunstein *et al.* [10] by optical absorption measurements. A more recent analysis has been done by Weber and Alonso [11] using photoluminescence to determine the indirect band gap. The bandgap quoted from [11] is approximately 40 meV higher than the results obtained by [10]. The discrepancy between the results is attributed by [12] to an over simplification in the analysis of [10]. The SiGe bandgap determined by Weber and Alonso is used in this thesis. The bandgap as a function of Ge fraction in the relaxed SiGe alloy is plotted in Figure 2-1 (a). The bandgap shrinks with increasing Ge fraction.

The SiGe alloy has an indirect bandgap for all compositions. The structure is Si-like for Ge fractions up to x=0.85. The valence band is comprised of the degenerate heavy hole and light hole bands (HH and LH), and the conduction band edge comprises of the 6 fold degenerate Δ valley. For Ge fractions above 0.85 the SiGe alloy becomes Ge-like and the conduction band edge changes to the L valley. This can be seen in the rapid change in bandgap for Ge fractions above 0.85. The band offsets between materials is very important for heterostructure behavior. Therefore, the alignment of the bands is just as important as the actual bandgap. The change in position of the conduction and valence band as a function of Ge fraction with respect to Au from [13] is plotted in Figure 2-1 (b). The valence band energy, E_V, increases linearly with increasing Ge fraction by approximately 37 meV/10 at. % Ge. There is a relatively small shift in the position of the conduction band energy, E_C, of less than 100 meV.

2.1.2 Biaxial Strain

The lattice constants of bulk Si and Ge are 0.5431 nm and 0.5658 nm respectively. The lattice constant for relaxed $Si_{1-x}Ge_x$ follows Vegards rule which is a linear interpolation between the Si and Ge lattice constants. Experimental work [15] has shown that the lattice constant deviates slightly from a linear interpolation (less than 0.2%) due to a small shift in bond angle that is not accounted for in Vegards rule, which assumes only a shift in bond length.

Biaxial tensile strained Si and compressive strained $Si_{1-y}Ge_y$ pseudomorphically strained to a relaxed Si or $Si_{1-x}Ge_x$ substrate (y>x) are considered in this study. The interested reader is referred to the excellent review by Van de Walle on the impact of strain on the valence and conduction band for Si and SiGe alloys [16],[17]. For a simple overview, it is easiest to think of biaxial strain in terms of hydrostatic strain with an additional uniaxial component. The impact of strain on the band edges in strained Si and SiGe is summarized in Figure 2-2.

The introduction of hydrostatic tensile strain in the Si lattice causes a net shift downwards in the positions of the valence and conduction bands. Introducing compressive strain in the z direction (equivalent to biaxial tensile strain) causes the 6-fold degenerate Δ valley in the conduction band to split, with a shift downward in the $\Delta 2$

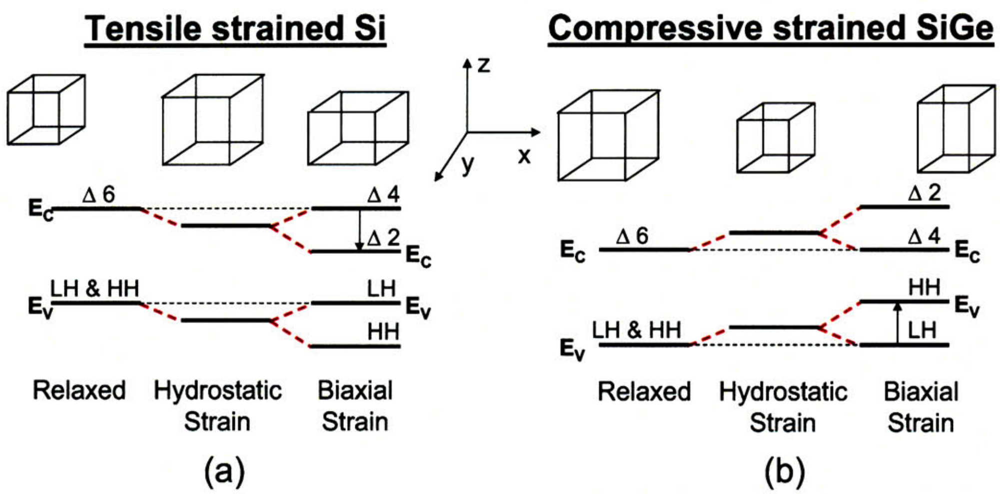
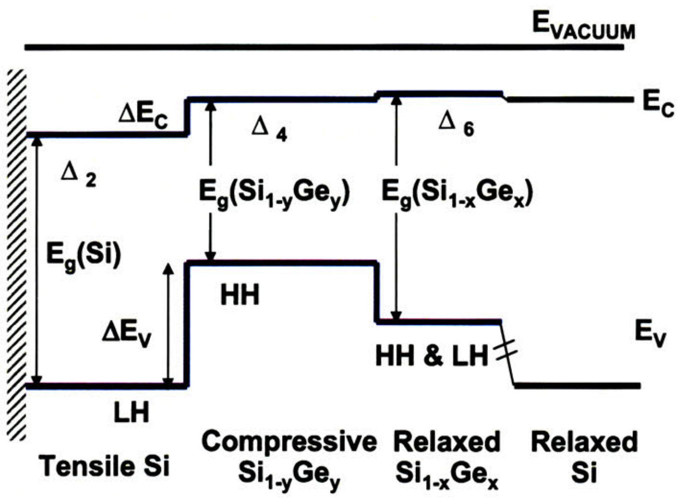


Figure 2-2: (a) Effect of biaxial tensile strain on the Si band edge, and (b) effect of biaxial compressive strain on the SiGe band edge.

valleys. There is also a splitting of the degenerate HH and LH valence band with the LH band shifting upwards. This results in a net shift downwards in the conduction band edge and a relatively small shift (< 50meV) in the position of the valence band edge with respect to the unstrained bands.

For SiGe, the introduction of hydrostatic compressive strain causes a net shift upwards in the position of the valence and conduction band. Introducing tensile strain in the z direction (equivalent to biaxial compressive strain) causes the 6-fold degenerate Δ valley in the conduction band to split with a shift downward in the $\Delta 4$ valleys. There is also a splitting of the degenerate HH and LH valence band with the HH band shifting upwards. This results in a net shift upwards in the valence band edge and a relatively small shift (< 50meV) in the position of the conduction band edge with respect to the unstrained bands.

The effect of strain on the bandstructure results in a staggered (type II) alignment of the bands between the tensile strained Si and compressive strained SiGe. An example of a typical band alignment is shown in Figure 2-3. Increasing the Ge composition in the relaxed layer increases the strain in the Si layer, leading to a reduction of bandgap and increased conduction band offset. This also reduces the strain in the compressively strained $Si_{1-y}Ge_y$ layer, leading to an increase in the



Ge	Eg_{Si}	ΔE_C	$Eg_{Si(1-y)Gey}$	ΔE_V
x ↑	↓	↑	↑	↓
y ↑			↓	↑

Figure 2-3: Band alignment for the strained Si/ strained $Si_{1-y}Ge_y$ / relaxed $Si_{1-x}Ge_x$ (y>x) heterostructure. The table indicates the impact of Ge composition in the strained and relaxed layers on the bandgap and band offsets.

band gap and decrease in the valence band offset between the strained Si and strained SiGe layers. The Ge composition in the strained $Si_{1-y}Ge_y$ has no impact on the Si band structure as it is strained pseudomorphically to the relaxed $Si_{1-x}Ge_x$ virtual substrate. Increasing the Ge composition in the strained $Si_{1-y}Ge_y$ layer causes the bandgap to decrease and the valence band offset to increase.

Theoretical studies of strained SiGe band offsets with respect to relaxed Si and SiGe have been performed [18][19][20] and are summarized in [21][22][23]. Experimental bandgap and band offsets for $Si_{1-y}Ge_y$ strained pseudomorphically to relaxed Si [24][25] compares well to theory [18]. However, there is little experimental work for strained SiGe grown on relaxed SiGe, and there is an expected error of $\pm$ 100meV in determination of band offsets using the theoretical results. In Chapter 3 of this work the valence band offset between strained Si and strained $Si_{1-y}Ge_y$ is determined from inverse modeling of experimental capacitance-voltage characteristics and compared to the theoretical results, for a wide range of Ge compositions in the strained and relaxed substrate. These values are used for subsequent simulations in this thesis, unless otherwise stated. The bandgap for strained Si and the conduction band offset between strained Si and SiGe is taken from the experimental work of Welser [62].

2.2 Hole Transport

In this section the conductivity effective mass and scattering mechanism relevant to hole transport in the SiGe heterostructure pMOSFET will be reviewed. Low field mobility for holes is given by

$$\mu_h = \frac{e\tau}{m^*} \tag{2.1}$$

where e is the electronic charge, $1/\tau$ is the scattering rate and m^* is the conductivity effective mass. It can be seen from Equation 2.3 that knowledge of the conductivity effective mass and scattering mechanisms in SiGe heterostructure MOSFETs is critical to understanding of the potential for mobility enhancement in these devices.

2.2.1 Hole Effective Mass

The effective mass for holes in Si-like bandstructure materials is difficult to quantify, as the valence bands are non-parabolic and anisotropic, unlike the conduction band. In relaxed Si and SiGe the valence band edge consists of degenerate HH and LH bands at the Γ point. When biaxial compressive strain is introduced, the HH and LH bands split, with the HH band moving up in energy. There is a reduction in the HH effective mass and decrease in the band warping with strain.

The valence band structure for the SiGe alloys investigated in this work is determined by 6-band k.p simulations [26][27][28][13] using *nextnano*^{3} [29] with a non-linear interpolation of valence band parameters described by Rieger and Vogl [20]. An excellent review of valence band parameters for SiGe can be found in Ref. [30]. The valence band for relaxed $Si_{0.3}Ge_{0.7}$ and $Si_{0.3}Ge_{0.7}$ strained pseudomorphically to relaxed $Si_{0.7}Ge_{0.3}$, obtained from 6-band k.p simulations using *nextanano*^{3} is shown

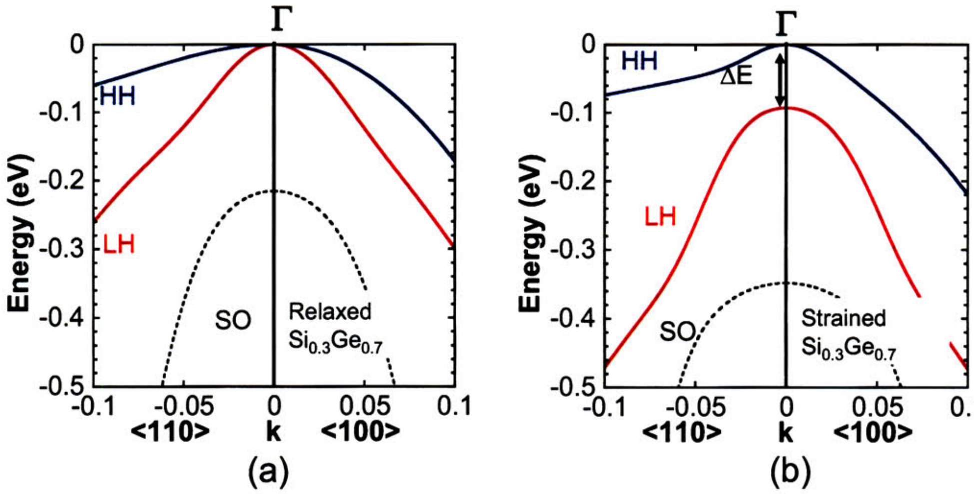


Figure 2-4: (a) Valence band for relaxed $Si_{0.3}Ge_{0.7}$ from 6-band k.p simulations using *nextanano*[3]. The HH and LH are degenerate at the gamma point. (b)Valence band for $Si_{0.3}Ge_{0.7}$ strained pseudomorphically to relaxed $Si_{0.7}Ge_{0.3}$. Biaxial compressive strain results in 93 meV splitting of the HH and LH bands.

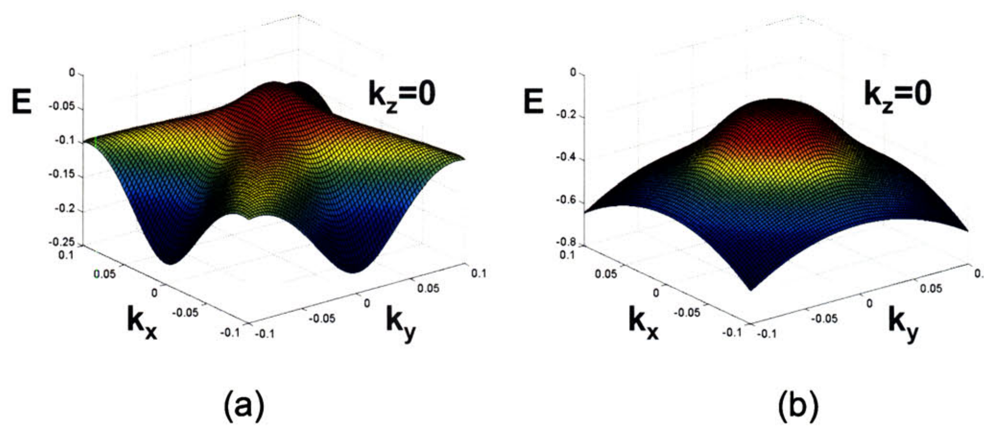


Figure 2-5: 2D (a) HH and (b) LH band for for $Si_{0.3}Ge_{0.7}$ strained pseudomorphically to relaxed $Si_{0.7}Ge_{0.3}$. There is a large deformation of the HH band with crystal orientation, although the band is almost isotropic for |E|< 30 meV.

in Figure 2-4 (a) and (b) respectively. Introduction of biaxial compressive strain results in 93 meV splitting of the HH and LH bands for $Si_{0.3}Ge_{0.7}$ strained pseudomorphically to relaxed $Si_{0.7}Ge_{0.3}$. A 2D plot of the HH and LH band for strained $Si_{0.3}Ge_{0.7}$ is shown in Figure 2-5 (a) and (b) respectively. The HH band curvature is isotropic near the band edge (|E|< 30 meV), but at higher energies there is significant deformation of the band with curvature changing with crystal orientation. The band warping decreases with increased strain due to the increased separation of HH and

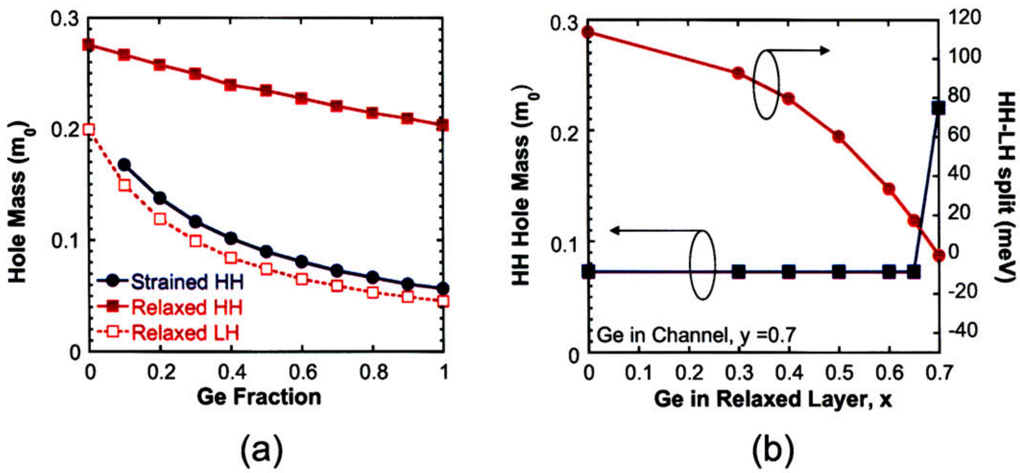


Figure 2-6: (a) In plane (< 100 >) LH and HH band edge effective mass for relaxed and biaxial compressive strained SiGe. (b) HH band edge effective mass and energy split between HH and LH bands for $Si_{0.3}Ge_{0.7}$ pseudomorphically strained to a relaxed $Si_{1-x}Ge_x$ substrate. Calculations performed using *nextnano*^{3}.

LH bands. The LH band, while still not parabolic, is isotropic with crystal direction.

Once the band structure is determined, the effective mass is then calculated from the band curvature using

$$\frac{1}{m^*} = \frac{1}{\hbar^2}\frac{\partial^2 E(k)}{\partial k^2} \tag{2.2}$$

Since the valence band is not parabolic the calculated effective mass changes with energy. This results in an effective hole mass that is dependent on temperature, doping and carrier concentration. The band edge hole effective mass for relaxed and compressively strained SiGe as a function of Ge composition is shown in Figure 2-6 (a). For relaxed SiGe the effective mass decreases with increasing Ge composition, and the LH mass is significantly smaller than the HH mass.

With the introduction of biaxial compressive strain, the HH mass decreases significantly and becomes LH in character. Initial introduction of strain leads to a large shift in the band edge effective mass. Increasing the strain does not change the band edge effective mass. This can be seen in Figure 2-6 (b) where the band edge effective mass is plotted as a function of Ge composition in the relaxed layer for $Si_{0.3}Ge_{0.7}$ grown pseudomorphically on relaxed $Si_{1-x}Ge_x$. The splitting of the bands increases with increasing strain as shown in Figure 2-6 (b). The increased splitting leads to a reduction in deformation and the HH band becomes more parabolic. Thus, while the band edge effective mass does not change with strain, the effective mass at higher energies decreases with increasing strain. For 1D Schrödinger-Poisson simulations performed in this thesis, the hole mass at 25 meV is used.

The in-plane effective mass ($< 100 >$ direction) will impact the hole mobility. The effective mass in the $< 001 >$ direction (i.e. quantization effective mass) and the band offset will determine the carrier confinement. With biaxial compressive strain the effective mass in the $< 100 >$ and $< 010 >$ directions are isotropic. The lattice in the $< 001 >$ direction is under tensile strain and has a different effective mass. The effective mass and HH-LH band splitting for the various strained SiGe channels investigated in this study are given in Table 2.1. Note that the effective mass values calculated for bulk Si differ from the values typically quoted in the literature [31] of 0.573 and 0.153 for the HH and LH respectively. These values are based on a simple isotropic parabolic approximation of the the valence bands and differ significantly from the effective mass calculated at 25 meV from the band edge. It was found that the 25 meV effective mass values are required to obtain a good fit of simulations to the measured capacitance-voltage characteristics for bulk Si/Strained SiGe heterostructures.

Table 2.1: Effective masses (at 25 meV) and HH-LH band splitting from k.p simulations. Note that in compressive (tensile) strained layers, the lowest energy, or top-most band is the HH (LH) band.

Ge fraction of relaxed buffer (x)	Ge fraction of layer (y)	HH $< 100 >$, $< 001 >$	LH $< 100 >$, $< 001 >$	HH-LH Split (meV)
0	0	0.28,0.28	0.24,0.24	0
0.3	0	0.27,0.28	0.28,0.18	128
0.5	0	0.28,0.28	0.28,0.18	221
0.0	0.4	0.30,0.24	0.07,0.24	71
0.0	0.7	0.19,0.22	0.05,0.21	114
0.3	1.0	0.13,0.20	0.04,0.18	143
0.5	1.0	0.15,0.20	0.04,0.16	125
0.7	1.0	0.21,0.20	0.04,0.12	93

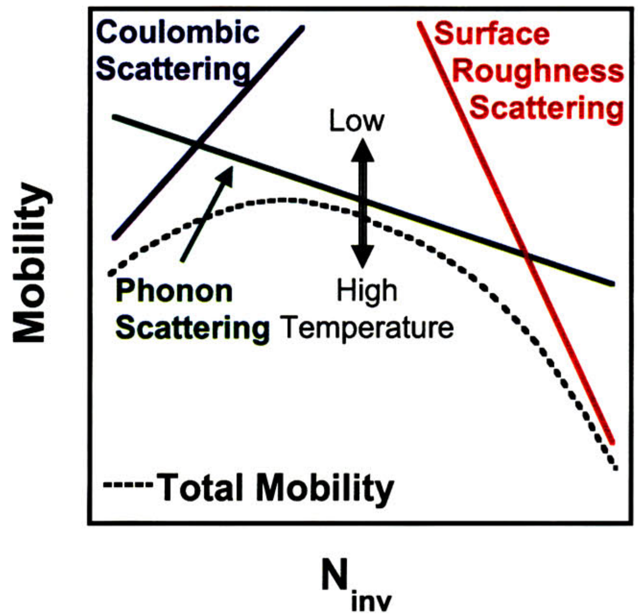


Figure 2-7: Summary of main scattering mechanisms contributing to mobility in a bulk Si MOSFET inversion layer as a function of N_{inv} [32].

2.2.2 Scattering Mechanisms

The scattering rate $\frac{1}{\tau}$ from Equation 2.3 is the sum of all scattering mechanisms given by Mattheissen's rule. For a bulk Si MOSFET

$$\frac{1}{\tau} = \frac{1}{\tau_{ii}} + \frac{1}{\tau_{ph}} + \frac{1}{\tau_{ir}} \tag{2.3}$$

where τ_{ii} is the momentum relaxation time for ionized impurity scattering (coulombic scattering), τ_{ph} for phonon scattering and τ_{ir} for interface roughness scattering at the Si-SiO$_2$ interface. These mechanisms are summarized as a function of inversion charge density (N_{inv}) which is directly related to the vertical effective field (E_{eff}) in Figure 2-7. In SiGe alloys, alloy scattering, due to the random arrangement of Si and Ge atoms in the SiGe alloy lattice contributes to a drop in mobility. Thickness fluctuation scattering becomes significant in ultra-thin body SOI channels. These scattering mechanisms are discussed in the following sections.

2.2.2.1 Coloumbic Scattering

As seen in Figure 2-7, coulombic scattering dominates at low N_{inv} due to the presence of ionized impurities in the device. A higher substrate doping will lead to increased scattering. The scattering decreases with increasing N_{inv} due to screening of the ionized impurities by the carriers in the channel of the MOSFET. The interested reader is referred to [26][34] for a detailed treatment of ionised impurity scattering.

2.2.2.2 Phonon Scattering

Carriers can scatter from quantized lattice vibrations, i.e. phonons, leading to a reduction in mobility. In bulk Si, holes can scatter from optical and acoustic phonons. Acoustic phonon scattering is the dominant phonon scattering mechanism in compressively strained SiGe. Interband optical phonon scattering is significantly reduced in compressively strained SiGe due to the large band splitting between the HH and LH bands [28][33] as there is no final state to scatter into (Si-Si and Ge-Ge optical phonon energies are 63 meV and 37 meV respectively). The bulk acoustic phonon scattering rate is given by

$$\frac{1}{\tau_{AC}} = \frac{\pi D_A^2 k_B T_L}{\hbar c_l} g_{3D}(E) \tag{2.4}$$

where D_A is the deformation potential for acoustic phonon scattering, k_B is Boltzmann's constant, T_L is the lattice temperature, c_l is the elastic constant for the material and g_{3D}(E) is the density of states. It can be seen from this equation and Figure 2-7 that phonon scattering decreases with decreasing temperature. Phonon scattering in a 2D quantum well such as a MOSFET inversion layer or ultra thin channel in an SOI or heterostructure MOSFET is given by

$$\frac{1}{\tau_{AC}} = \frac{\pi D_A^2 k_B T_L}{\hbar c_l} \frac{1}{W_{fi}} g_{2D}(E) \tag{2.5}$$

where $\frac{1}{W_{fi}}$ is the effective interaction in the z-direction and where W_{fi} can be approximated by the inversion layer thickness or well width for narrow quantum wells and

g_{2D}(E) is the 2D density of states. For parabolic bands $g_{3D}(E) \propto E^{1/2}m^{*3/2}$ and is continuous. The 2D density of states is piecewise constant where $g_{2D}(E) = m^*/\pi\hbar^2$ and $\frac{1}{W_{fi}}$ is given by

$$\frac{1}{W_{fi}} = \int_{-\infty}^{+\infty} |F_f(z)|^2|F_i(z)|^2 dz \tag{2.6}$$

F(z) is the hole envelope function where f and i represent the final and initial scattering states. Equation 2.5 suggests that phonon scattering increases with increasing confinement. This is demonstrated in Figure 2-7 where phonon limited mobility decreases with increasing confinement, which increases with N_{inv} (or vertical effective field, E_{eff}). The increase in phonon scattering with confinement can also be thought of in terms of the Heisenberg uncertainty principal given by

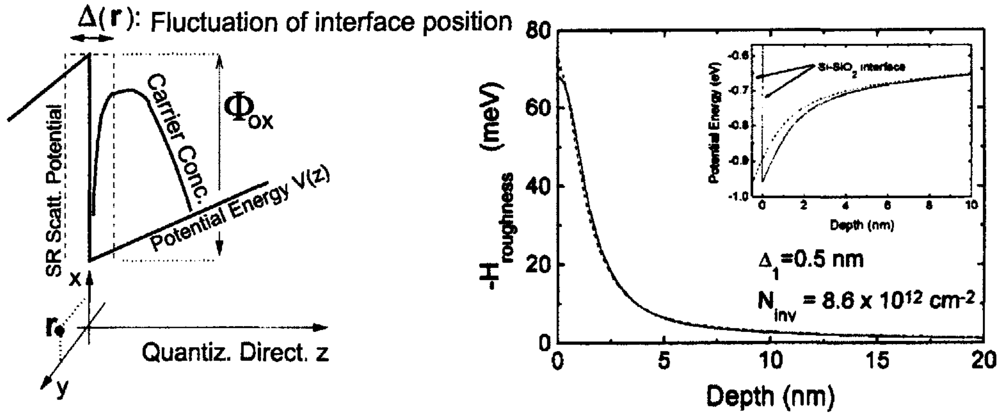
$$\Delta p \Delta x \geq \frac{\hbar}{2} \tag{2.7}$$

This simply states that confinement in real space (x) leads to a spread in momentum space (p) allowing carriers to interact with more phonons and thus increase scattering. Further insight into phonon scattering can be found in [26][34][35][36].

The important points to be taken from this analysis in terms of SiGe heterostructures can be summarized as follows. Phonon scattering depends on the density of states. Therefore, the splitting of the HH and LH valence band degeneracy will lead to a reduction of phonon scattering in strained SiGe compared to relaxed Si and SiGe. The density of states is dependent on the effective mass. The decrease in effective mass with increasing Ge composition will lead to a reduction in phonon scattering. Phonon scattering increases with confinement so a reduction in mobility is expected for ultra thin channel SiGe heterostructures.

2.2.2.3 Interface Roughness Scattering

In bulk Si MOSFETs interface roughness scattering at the Si-SiO_2 surface increases with increasing N_{inv} as seen in Figure 2-7. In this review, we will follow the analysis of Gámiz *et al.* [37] which improves on the model by Ando *et al.* [38] to be accurate



(a) (b)

Figure 2-8: (a) Schematic of carrier concentration close to the Si-oxide interface of a MOSFET with an interface fluctuation of Δ(r), reproduced from [39]. (b) Perturbation Hamiltonian due to the 0.5 nm displacement of the interface from the plane z=0 at a given position r_0 of the gate interface in a bulk silicon inversion layer.Inset: Actual potential well in a bulk silicon inversion layer when a z displacement of the interface of 1 nm from the ideal interface plane located at z=0. Reproduced from [37].

in both bulk Si and SOI structures.

For a MOSFET, the Si-oxide interface is thought of as an abrupt boundary that varies randomly due to roughness by an amount Δ as a function of position r in the plane of the Si-oxide interface, as sketched in Figure 2-8 (a). The surface potential V(z) may be expanded about the interface as

$$V[z+\Delta(r)] - V(z) = \frac{V[z+\Delta_m] - V(z)}{\Delta_m}\Delta(r) \tag{2.8}$$

where Δ_m is the root mean square (RMS) roughness of Δ(r). This gives the perturbation Hamiltonian (scattering potential)

$$H_{SR}(z,r) = -\frac{e\Delta(r)\Delta V_m(z)}{\Delta_m} \tag{2.9}$$

where

$$\Delta V_m(z) = V[z+\Delta_m] - V(z) \tag{2.10}$$

The surface roughness scattering is then related to the perturbation Hamiltonian through the matrix element M_{fi} by

$$\frac{1}{\tau_{SR}} \propto |M_{fi}|^2 = |\psi_i(z) H_{SR} \psi_f(z)|^2 \tag{2.11}$$

where $\psi_{i/f}$ is the initial and final envelope function for the scattered carrier.

From Equation 2.9 it can be seen that the scattering potential increases with applied surface potential and increased roughness. The perturbation varies with proximity to the interface due to band bending, decreasing as you move away from the interface. The perturbation Hamiltonian is illustrated in Figure 2-8 (b) as a function of distance from the Si-oxide interface for Δ(r)=0.5 nm. The actual variation in the surface potential for a 1 nm shift in the position of the interface is shown in the inset. This suggests that the scattering will be higher for carriers closer to the interface, and is included mathematically in Equation 2.11 through the envelope functions $\psi_{i/f}$.

To summarize, increasing the surface potential causes surface roughness scattering to increase through two main effects. The increased potential leads to an increase in the perturbation Hamiltonian (scattering potential) through increased band bending. The increased band bending at the surface also causes the carriers to be confined more closely to the scattering potential. This leads to the very strong dependance of SR scattering on N_{inv} (E_{eff}) shown in Figure 2-7.

2.2.2.4 Thickness Fluctuation Scattering

Thickness fluctuation scattering has been identified as the main scattering mechanism for ultra thin body SOI for body thickness less than 4 nm [9]. As shown in Figure 2-9 (a), the mobility decreases proportional to W_{SOI}^6, where W_{SOI} is the SOI Si layer thickness. Local variation in the Si body thickness causes a spatial fluctuation in the ground state energy of the quantum well leading to scattering. Ground state energy fluctuation for a thickness variation of $\pm$ 0.2 nm as a function of body thickness is plotted in Figure 2-9 (b). For SOI thickness below 4 nm the energy fluctuation is significant and becomes the dominant scattering mechanism for these structures.

Thickness fluctuation scattering was originally identified as a scattering mecha-

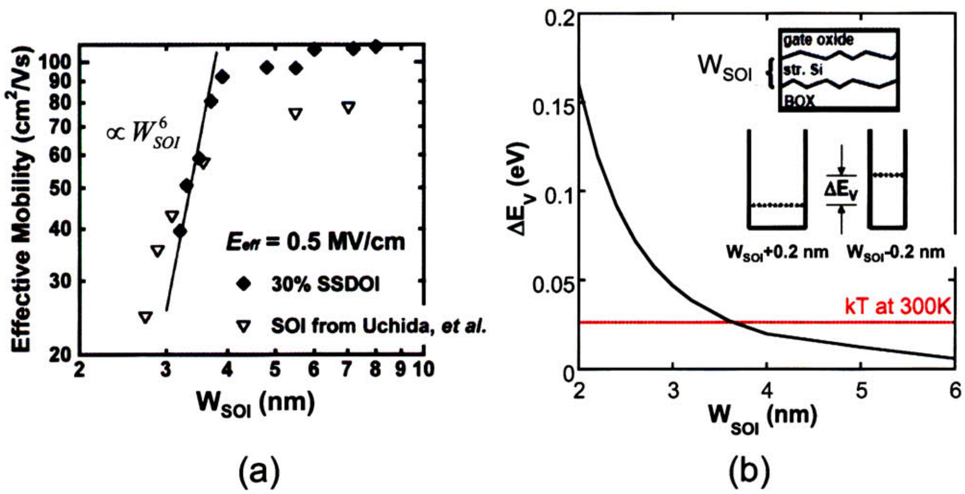


Figure 2-9: (a) Hole mobility as a function of film thickness at a vertical effective field of 0.5 MV/cm for 30% Strained Si Directly on Insulator (SSDOI) (diamonds) [40] and unstrained SOI (triangles) from Uchida, *et al.* [9], reproduced from [40]. The drop in mobility follows a characteristic W^6 dependence. (b) Ground state energy fluctuation for a thickness variation of $\pm$ 0.2 nm as a function of body thickness. Interface roughness at the Si-oxide interface in ultra thin body SOI and SSDOI result in a local variation in body thickness. The fluctuation in body thickness leads to a spatial fluctuation in the ground state energy of the Si quantum well causing thickness fluctuation scattering, following the simple model from [41].

nism in AlGaAs/GaAs heterostructures. Following the analysis of Sakaki *et al.* [42], the ground state energy in an infinite quantum well is given by

$$E_0 = \frac{\hbar^2 \pi^2}{2m^* W^2} \tag{2.12}$$

where m^* is the effective mass and W is the width of the quantum well. The energy fluctuation due to a change in well thickness Δ is given by

$$\delta E = \frac{\partial E_0}{\partial W}\Delta = \frac{\hbar^2 \pi^2}{m^* W^3}\Delta \tag{2.13}$$

The thickness fluctuation scattering limited mobility is given by [42]:

$$\mu_{TF} \propto \frac{1}{(\delta E)^2} \propto W^6 \tag{2.14}$$

leading to the W^6 dependance shown in Figure 2-9 (a).

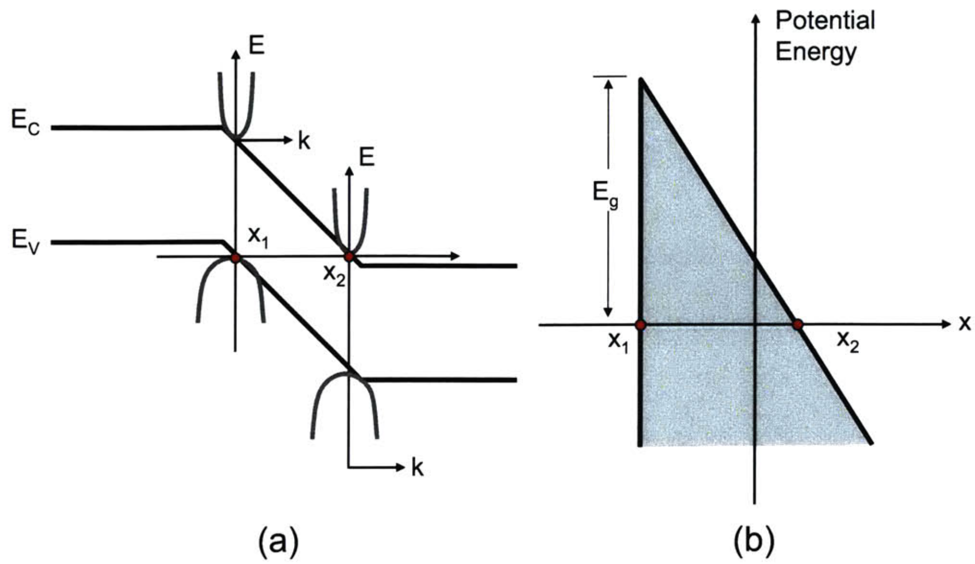


Figure 2-10: (a) Schematic of BBT in a p-n junction. Tunneling can occur when the valence band edge at X_1 coincides with the conduction band edge at X_2 at the same energy. (b) Potential profile seen by an electron tunneling from X_1 to X_2 in (a). Reproduced from [26].

Thickness fluctuation scattering differs from surface roughness scattering in the fact that there is very little dependence on the surface potential as the carriers are confined through quantum confinement of the physical well thickness, rather than the surface field.

In summary, coulombic scattering will dominate at low N_{inv}. Phonon scattering will dominate at intermediate N_{inv}, with the scattering rate increasing with increasing N_{inv}. At high N_{inv} surface roughness scattering will dominate. Thickness fluctuation scattering has very little dependence on N_{inv} and becomes significant for thin channel devices.

2.3 BBT Leakage

Band-to-band tunneling (BBT) is a significant form of leakage in SiGe heterostructure MOSFETs due to the smaller bandgap compared to bulk Si devices. Following the sketch in Figure 2-10 [26], due to band bending in a reversed biased p-n junction, an electron at point X_1 at the top of the valence band has the same energy as an electron at the bottom of conduction band at point X_2. Tunneling can occur through the forbidden band gap, which is typically treated as a triangular barrier using the WKB approximation, leading to a tunneling probability

$$T \approx exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3e\hbar F}\right) \tag{2.15}$$

where F is the electric field across the junction. The tunneling probability depends exponentially on the bandgap E_g.

BBT in MOSFETs has been addressed by many researchers, most notably Kane [43], Hurkx [44] and Schenk [45]. All the models for the carrier tunneling rate R^{BBT} have been used to fit to experimental data and take the same general form:

$$R^{BBT} = AF^P exp\left(-\frac{B}{F}\right) \tag{2.16}$$

where A is a pre-exponential constant with a weak dependence on E_g, m_r is the reduced effective tunneling mass: $1/m_r = 1/m_c + 1/m_v$ where m_c and m_v are the effective mass in the conduction band and valence band respectively [46], F is the local electric field, P is the power varying from 1 to 3.5 and

$$B \propto \sqrt{m_r} E_g^{3/2} \tag{2.17}$$

The tunneling rate is sensitive to all the parameters within the exponent. Schenk [45] shows that varying the hole mass between 0.16 and 0.49 (LH and HH mass for bulk Si) results in difference of 7 orders of magnitude and 2 orders of magnitude for electric fields of 0.4 MV/cm and 1.5 MV/cm respectively, and attributes the uncertainty in the tunneling mass as the greatest source of error in the model. The effective mass in the valence band is dependent on transport direction, especially for strained Si and SiGe, so the direction of the electric field in the semiconductor will impact the BBT rate. In general, where these models are used in the literature to fit to experimental data, the issue of effective mass is avoided by using B as a fitting parameter, see for example [47][48][49]. BBT can be identified by its characteristically

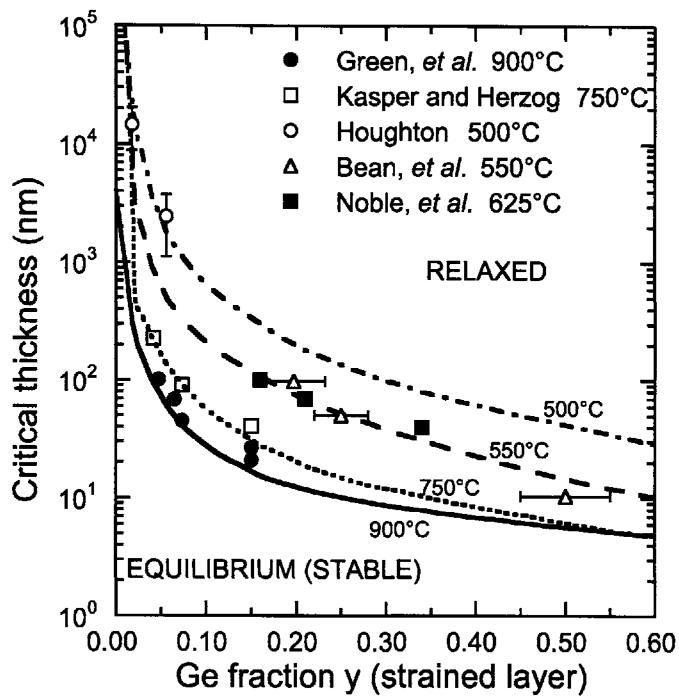


Figure 2-11: Critical thickness for $Si_{1-x}Ge_x$ grown on relaxed (100) Si as a function of Ge fraction, x. Calculated Equilibrium critical thickness shown by solid line. Theoretical metastable regime shown by dashed lines. Experimental results from [51][52][8][53][54]. Figure reproduced from [8].

small temperature dependence, where the leakage varies with temperature through the temperature dependence of the bandgap.

2.4 Critical Thickness

A strained film can be grown pseudomorphically on a relaxed substrate below a certain critical thickness. Above this critical thickness dislocations become energetically favorable and the film will start to relax through dislocation formation [50]. For strained SiGe layers grown on relaxed SiGe substrates, the critical thickness depends on the Ge fraction in the strained layer and substrate, i.e. the lattice mismatch, and the film growth and subsequent processing temperatures. Based on the work of Houghton [8], the equilibrium critical thickness T_{crit} for SiGe grown on a relaxed Si substrate can be calculated from the semiempirical model

$$T_{crit} = \left(\frac{0.55}{x}\right) ln\left(10T_{crit}\right) \tag{2.18}$$

Fully strained films can be grown above the critical thickness if the temperature is kept sufficiently low and are called metastable films. However, subsequent high temperature heat treatment can cause dislocation formation and relaxation. The equilibrium critical thickness and the metastable regime are plotted in Figure 2-11 [8]. The equilibrium critical thickness is less than 5 nm for Ge compositions above 60 at. % grown directly on a Si substrate. The lattice mismatch can be reduced by growing on a relaxed SiGe virtual substrate and hence the critical thickness is increased. The equilibrium critical thickness for strained $Si_{1-y}Ge_y$ on a relaxed $Si_{1-x}Ge_x$ where x is less than y, can be obtained from Equation 2.18 where x is replace by (y-x).

2.5 Effective Mobility Extraction

Following the description in [55], the drain current of a long channel MOSFET is given by

$$I_D = \frac{W\mu_{eff}Q_pV_{DS}}{L} - W\mu_{eff}\frac{kT}{q}\frac{dQ_p}{dx} \tag{2.19}$$

where Q_p is the mobile channel sheet charge density which is determined by the split CV technique [56] and μ_{eff} is the effective mobility. The first term is the drift component and the second term is the diffusion component of the drain current. By using a low V_{DS} (<100 mV) and a long channel length the charge distribution in the channel is uniform and the diffusion term can be dropped. The effective mobility is then given by

$$\mu_{eff} = \frac{g_dL}{WQ_p} \tag{2.20}$$

where the drain conductance g_d is given by

$$g_d = \frac{\partial I_D}{\partial V_{DS}} \tag{2.21}$$

In this work, typical values for V_{DS} used for mobility extraction were 10-60 mV. Mobility measurements were made on devices with a WxL of 50 μm x 50 μm for the majority of the mobility measurements reported in this work. Low temperature and channel orientation mobility measurements were made on devices with a WxL of 15 μm x 100 μm.

2.6 Chapter Summary

In this chapter the basic theory behind the work in this thesis has been presented. The key points from the chapter can be summarized as follows. Increasing Ge fraction and strain lead to a reduction in the bandgap of compressively strained SiGe, and an increase in the valance band offset between the strained SiGe and strained Si cap, forming a potential well in the strained SiGe layer for holes. The hole effective mass decreases with increasing strain and Ge composition leading to increased mobility. The mobility in bulk devices is dominated by scattering due to coulombic scattering, phonon scattering and interface roughness scattering at low, intermediate and high N_{inv} respectively. Thickness fluctuation scattering is expected to become significant for thin channel structures. Band-to-band tunneling leakage is found to increase exponentially with decreasing bandgap which leads to increased leakage for higher Ge composition channels. The thickness of the strained SiGe channel is limited by the critical thickness, which decreases with increasing strain. Finally, the method for mobility extraction used in this thesis is outlined.

Chapter 3

Valence Band Offset Extraction in Strained Si/Strained $Si_{1-y}Ge_y$ on Relaxed $Si_{1-x}Ge_x$ Heterostructures

3.1 Introduction

It is essential to know the band structure in order to accurately model SiGe heterostructure MOSFETs. In particular the valence band offset, ΔE_V, between the Si cap and strained $Si_{1-y}Ge_y$ layers determines the degree of hole confinement in the $Si_{1-y}Ge_y$ layer. The positions of the conduction band edge in the strained Si and the valence band edge in the strained $Si_{1-y}Ge_y$ significantly impact the effective bandgap of the structure and can be used to tune the threshold voltage of both n- and p-MOSFETs for use with a single workfunction metal gate [57]. Theoretical predictions of these band parameters are uncertain by ± 100 meV [58][21]. In this work ΔE_V is extracted over a wide range of Ge composition and strain, using measurements and modeling of MOS capacitors. It is also shown that the appropriate value of density of states for the strained layers must be used in order to accurately model the capacitance-voltage (C-V) and MOSFET behavior.

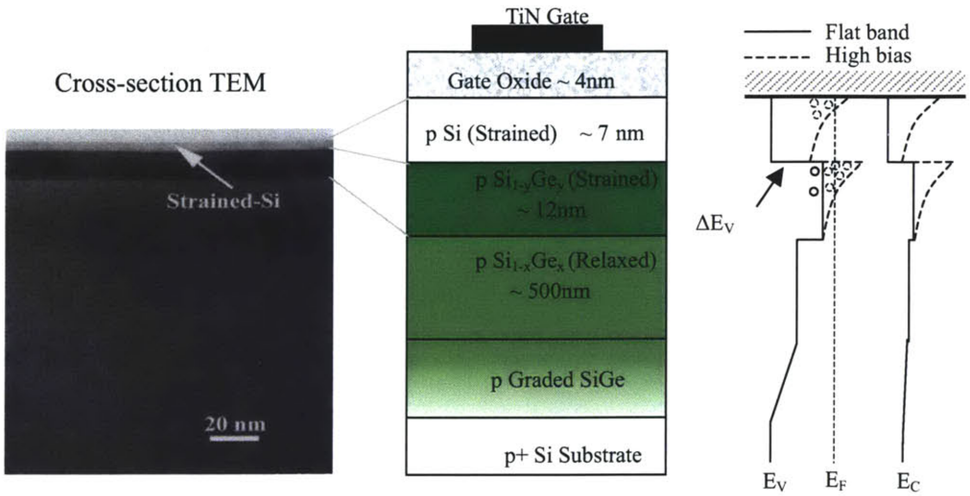


Figure 3-1: Structure and band diagram for strained Si on strained $Si_{1-y}Ge_y$ on relaxed $Si_{1-x}Ge_x$ ($x < y$) dual channel p-type MOS capacitor. TEM image of strained Si, strained $Si_{0.4}Ge_{0.6}$ on relaxed $Si_{0.7}Ge_{0.3}$ structure grown in the Applied Materials Epi-Centura system.

3.2 Device Fabrication

Large area capacitors were fabricated in order to extract ΔE_V between the strained Si and strained $Si_{1-y}Ge_y$ layer. The layer structure is illustrated in Figure 3-1. Epitaxial layers were grown in an Applied Materials low pressure chemical vapor deposition (LPCVD) "Epi-Centura" system. To achieve a low defect density in the relaxed $Si_{1-x}Ge_x$ layer a graded layer was initially grown on the bulk silicon substrate. Starting at 2% Ge at the Si substrate the Ge percentage is increased linearly at 12%/μm to a final composition x, where x ranged from 0.2 to 0.4 in this experiment. This technique has been shown to be effective at minimizing the number of threading dislocations at the surface of the graded buffer layer [59]. A 500 nm-thick relaxed $Si_{1-x}Ge_x$ layer is grown at 900°C on the graded layer to form a relaxed $Si_{1-x}Ge_x$ virtual substrate. A 12 nm-thick strained $Si_{1-y}Ge_y$ layer was then grown at 525°C with Ge compositions, y, ranging from 0.4 to 0.8. An 8 nm-thick strained cap layer was grown at 600°C. Layer thicknesses were chosen to optimize the sensitivity for ΔE_V extraction. The final germanium compositions were measured using Secondary Ion Mass Spectrometry (SIMS) and Rutherford backscattering (RBS).

The heterostructure was grown on highly doped p-type substrates (0.005 - 0.01 Ω-cm) to ensure a good substrate contact and minimize series resistance effects. The graded buffer and constant composition relaxed layer were in-situ doped with Boron to a doping level of 10^{17} cm^{-3} during epitaxial growth. To reduce sensitivity to doping variation and increase accuracy for ΔE_V extraction, the strained Si and strained $Si_{1-y}Ge_y$ layer were un-doped to insure doping concentration levels below 10^{16} cm^{-3}. Variations in doping below this level do not impact the extraction of ΔE_V. A cross-section transmission electron microscopy (TEM) image of strained Si, strained $Si_{0.4}Ge_{0.6}$ on relaxed $Si_{0.7}Ge_{0.3}$ structure grown in the Epi-Centura system is shown in Figure 3-1.

The thermal budget of the process was kept low to minimize the inter-diffusion of the SiGe layers which has been shown to be an issue for these structures [7]. The 4 nm-thick gate oxide was grown in a wet ambient at 650°C for 1 hour and 50 minutes with total time of 4 hours at 650°C. A metal gate of Titanium-Nitride (TiN) was deposited in a sputtering system. The metal gate has the dual advantage over poly gates of low thermal process requirements and absence of gate depletion which improves the accuracy of the ΔE_V extraction. The final capacitors were annealed in forming gas at 500°C for 30 minutes to passivate oxide interface states.

The strained Si and SiGe layers are expected to remain fully strained due to the relatively thin strained layer thickness and the very low thermal budget used in this process. MOSFETs with high mobility and low leakage have been made on similar substrates (see Chapter 4) indicating strain is maintained in these types of structures.

3.3 Modeling and Analysis

In this section the main features of the C-V characteristics of the dual channel MOS structure are explained. Details of the measurement of the C-V characteristics are provided. The parameters used for the simulation are described, and the procedure for fitting the simulation to the measured C-V characteristics is explained. Finally, the importance of using a suitable value for the valence band density of states when

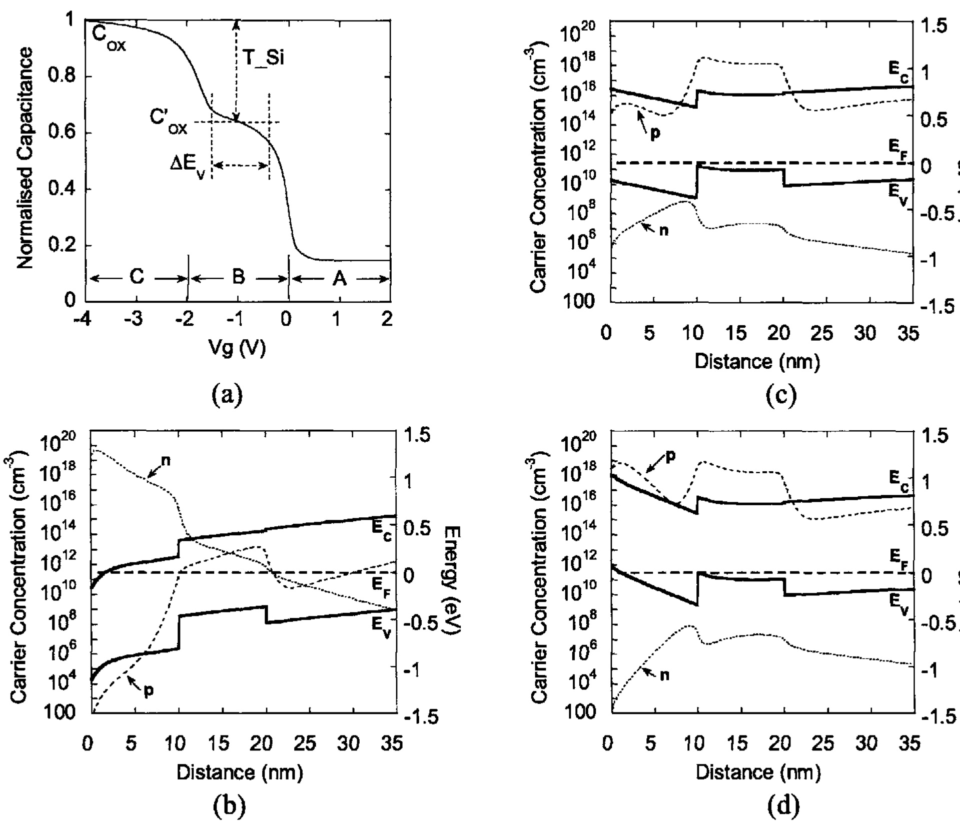


Figure 3-2: (a) Normalized C-V plot for the strained Si/strained $Si_{0.4}Ge_{0.6}$ on relaxed $Si_{0.7}Ge_{0.3}$ p-type capacitor structure, with the inversion (A), accumulation in the strained $Si_{1-y}Ge_y$ (B), and accumulation at the strained Si/oxide interface (C) regions of the C-V curve indicated. The energy bands, Fermi level, and carrier densities are shown for regions A, B and C in (b), (c) and (d) respectively.

simulating these structures is shown. A strained Si on strained $Si_{0.4}Ge_{0.6}$ on relaxed $Si_{0.7}Ge_{0.3}$ p-substrate structure is used as an example to illustrate the procedure for extraction of ΔE_V.

3.3.1 C-V Structure

The normalized C-V characteristics for a strained Si, strained $Si_{0.4}Ge_{0.6}$ on relaxed $Si_{0.7}Ge_{0.3}$ p-substrate capacitor structure are shown in Figure 3-2 (a). The plot is divided into three main regions: inversion, hole accumulation in the strained $Si_{0.4}Ge_{0.6}$ layer, and hole accumulation at the strained Si/oxide interface. These regions are indicated in the C-V plot by regions A, B and C respectively. Simulations of the conduction band, valence band and Fermi level positions along with the electron and hole carrier concentration for each of these regions are plotted in Figure 3-2 (b), (c), and (d). Starting from inversion, region A, the surface is depleted of holes and electrons pile up at the strained Si/oxide interface. As the gate bias is decreased, the bands bend downward and holes accumulate in the strained $Si_{1-y}Ge_y$ layer, forming a plateau in the C-V characteristics, region B. The capacitance of the plateau, C'_{OX}, is a series combination of the oxide capacitance C_{OX} and the strained Si layer capacitance. As the gate bias is decreased still further the bands are bent sufficiently for accumulation to occur at the strained Si/oxide interface and the capacitance approaches C_{OX}. The plateau width is related to the valence band offset between the strained Si and the strained $Si_{1-x}Ge_x$ layer. For a larger valence band offset, a larger gate field is required to move holes from the buried strained $Si_{1-y}Ge_y$ layer to the surface, causing the plateau width to increase. This relationship is exploited in this study to extract ΔE_V.

3.3.2 C-V Measurement

High frequency C-V (100kHz) was obtained on 250μm x 250μm and 100μm x 100μm capacitors for the dual channel MOS structure using a Agilent 4294A. The C-V characteristics did not show anomalous area or perimeter effects or hysteresis. Gate leakage was less than 0.1 μA/cm^2 at 4 MV/cm. There was no frequency dispersion observed over the range of 10 to 200 kHz indicating that the oxide/Si density of interface states (D_{it}) is not a concern, and series resistance R_s is not significant at the measurement frequency of 100 kHz. D_{it} of 1 x 10^{11} cm^2 has been measured on MOSFETs fabricated on similar substrates using the charge pumping method (see Section 5.2.1). This level of D_{it} would lead to a stretch out of the C-V by approximately 18 mV and is not a significant source of error for the band offset extraction.

3.3.3 Simulation Parameters

One-dimensional simulations were performed to fit the experimental data using the device simulator tool Dessis [60]. Quantum effects were taken into account by using the density gradient quantum correction model with the Dessis default parameters [61]. A linear interpolation between the Si and Ge values was assumed for the dielectric constant and electron affinity for both the relaxed $Si_{1-x}Ge_x$ and strained $Si_{1-y}Ge_y$ layers. The bandgap of the relaxed $Si_{1-x}Ge_x$ was obtained from Ref. [11]. The electron affinity and the bandgap for the strained Si were taken from Ref. [62]. The band gap of the strained $Si_{1-y}Ge_y$ layer was then varied by moving the position of the valence band to fit the experimental CV data. The fitting of the simulation to the experimental data is very insensitive to the absolute position of the conduction band, E_C, as only the accumulation side of a p-substrate capacitor is being studied in this work. Therefore, inaccuracy in electron affinity on the order of 100 meV does not affect the accuracy of the extraction of ΔE_V. The simulation fitting is sensitive to the relative position of the strained Si valence band with respect to the strained $Si_{1-y}Ge_y$ valence band, and therefore the extraction method is insensitive to errors in the bandgap (or absolute position of the valence band with respect to the conduction band) of the strained Si and strained $Si_{1-y}Ge_y$ layer on the order of 100 meV.

3.3.4 Fitting to Measured C-V Data

In order to fit the simulation to the measured data, oxide thickness (T_Ox), strained Si thickness (T_Si), strained $Si_{1-y}Ge_y$ thickness (T_SiGe), and substrate doping (Na-sub) were varied. These parameters were adjusted in order to obtain the best fit of the simulation to the measured C-V characteristics. These parameters have physical effects that impact very specific aspects of the C-V characteristics. Thus, they can be extracted reasonably independently, though some interrelationships exist. The doping in the strained Si and $Si_{1-y}Ge_y$ layers, N_a, was assumed to be 10^{16} cm^{-3}. From simulation, variation in doping concentrations below 10^{16} cm^{-3} does not impact the accuracy of the extraction of ΔE_V. Doping levels below 10^{16} cm^{-3} were confirmed by

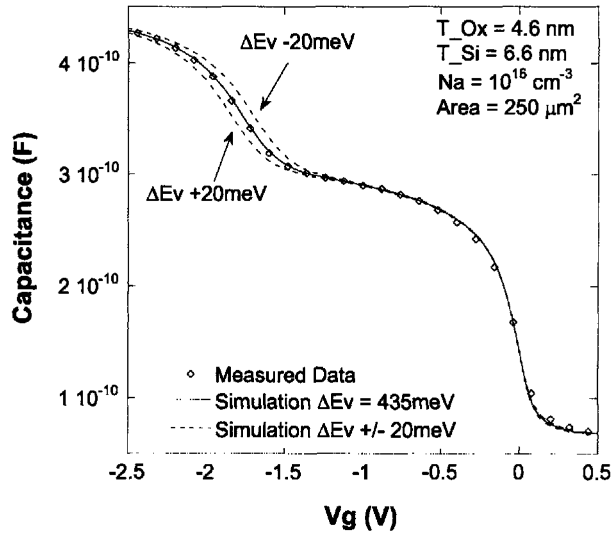


Figure 3-3: E_V extraction and sensitivity for strained Si, strained $Si_{0.4}Ge_{0.6}$ on a relaxed $Si_{0.7}Ge_{0.3}$ substrate. Measured data with simulation of E_V = 435 meV ± 20 meV.

secondary ion mass spectrometry (SIMS) analysis. ΔE_V is used as a fitting parameter and is adjusted by varying the value of the bandgap for the strained $Si_{1-y}Ge_y$ layer.

Figure 3-3 shows the C-V characteristics for the strained Si, strained $Si_{0.4}Ge_{0.6}$ on relaxed $Si_{0.7}Ge_{0.3}$ structure. The simulation parameters were varied in order to obtain the best fit quality. For this structure a ΔE_V of 435 meV was found to provide the best fit to the measured C-V data. The fit quality is very sensitive to small changes in ΔE_V. Variation in the simulated C-V characteristics due to a ± 20 meV shift in ΔE_V is also compared to the measured C-V characteristics in Figure 3-3. A shift of 40 meV translates to 160 mV shift in the plateau width for this particular structure. This demonstrates that the method is very sensitive to ΔE_V.

3.3.5 Effect of Density of States

The effective valence band density of states N_V decreases with strain and increasing Ge content [63] due to splitting and deformation of the degenerate light and heavy hole (LH, HH) valence bands. N_V values calculated by the non-local empirical pseudopotential method from full-band Monte Carlo simulations [20] were used in the Dessis C-V simulations. Figure 3-4 illustrates the improved C-V fit obtained when

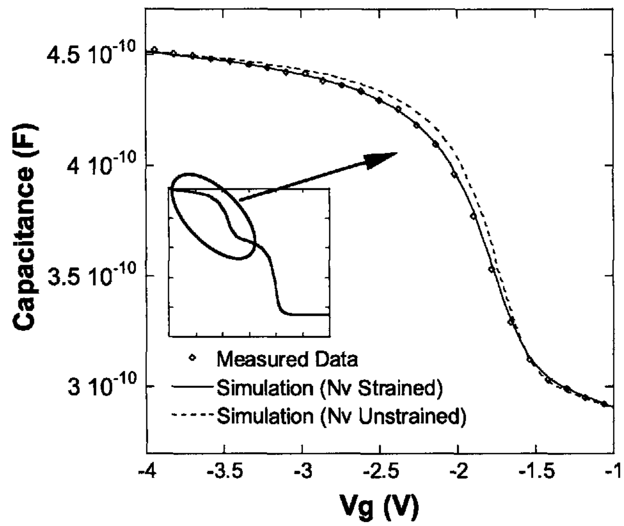


Figure 3-4: Impact of N_V value on fitting of simulation to experimental results for strained Si, strained $Si_{0.4}Ge_{0.6}$ on a relaxed $Si_{0.7}Ge_{0.3}$ substrate. Same structure as Figure 3-3.

the appropriate values are used for N_V in the strained Si and strained $Si_{1-y}Ge_y$ layers. The simulation parameters were adjusted in order to obtain the best fit using unstrained values of N_V for strained Si and strained $Si_{1-y}Ge_y$. This is repeated with the strained values of N_V, and the simulation parameters are readjusted to obtain a new best fit. It can be seen that the value of N_V significantly impacts the quality of the fitting to the experimental data, and that using the strained N_V values produces a much better fit to the C-V data in the portion of the curve corresponding to the population of the strained Si valence bands. The differences in fitting parameters used for these simulations are shown in Table 3.1. There is significant difference in several of the extracted parameter values including the oxide thickness, strained Si thickness and ΔE_V between the two simulations. Therefore, the ΔE_V value extracted in this method is dependent on the value of N_V used. This demonstrates the importance of using the correct N_V value, and the importance of using a self-consistent ΔE_V-N_V parameter set when using these band offsets to model devices.

Table 3.1: Fitting parameters used in Figure 3-4.

Simulation	N_V Si	N_V SiGe	T_Ox	T_Si	ΔE_V
N_V unstrained	2.24e19	9.80e18	4.83 nm	6.1 nm	450 meV
N_V strained	5.49e18	4.39e18	4.57 nm	6.6 nm	435 meV

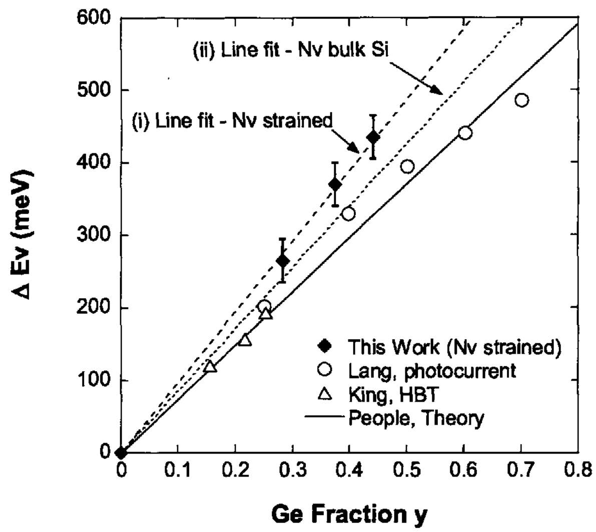


Figure 3-5: E_V for strained $Si_{1-y}Ge_y$ on relaxed Si. N_V values used for line fit (i) N_V (Strained $Si_{1-y}Ge_y$), and (ii) N_V (Relaxed Si).

3.4 Extracted Bandoffsets

The methodology described above has been used to extract ΔE_V for three structures. The valence band offset between strained $Si_{1-y}Ge_y$ grown pseudomorphically on a relaxed Si substrate has been examined both theoretically [58] and experimentally [24] [25] in the literature. Results from this study are compared to existing data. The single channel structure of strained Si on relaxed $Si_{1-x}Ge_x$ is investigated and compared to existing theory [58] and data [62]. Finally, experimental ΔE_V between strained $Si_{1-y}Ge_y$ and strained Si in dual-channel structures is extracted and compared to theory. To demonstrate the importance of the extracted ΔE_V in device modeling, the impact of ΔE_V and N_V on sub-threshold slope and V_T characteristics of a p-MOSFET are shown.

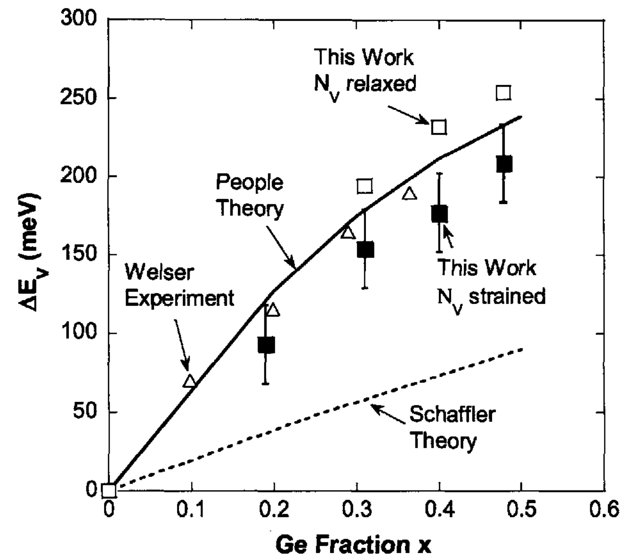


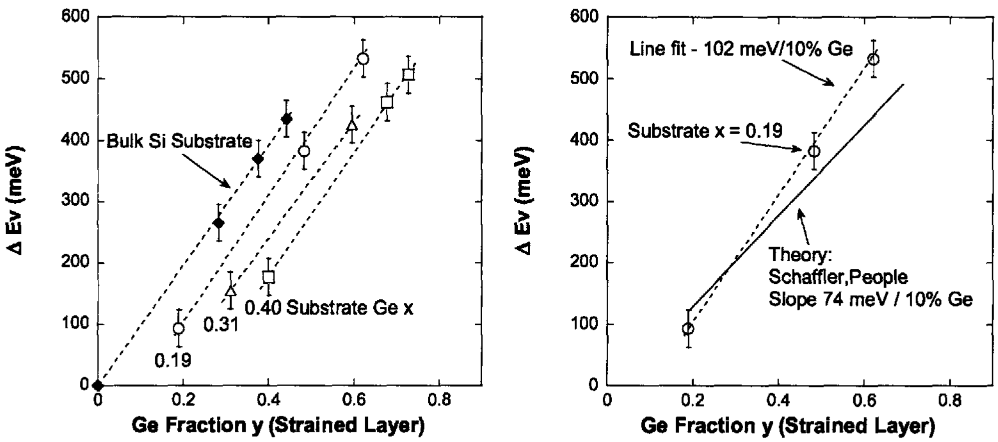
Figure 3-6: E_V for strained Si on relaxed $Si_{1-x}Ge_x$. Results from this work compare well with previously reported experimental data.

3.4.1 Pseudomorphic Strained $Si_{1-y}Ge_y$ on Relaxed Si

Figure 3-5 compares values of extracted ΔE_V for strained $Si_{1-y}Ge_y$ grown on relaxed Si. As predicted by theory, the ΔE_V is linearly related to the Ge fraction in the strained layer. Using the full-band strained N_V values we obtain a slope of 101 meV/10% Ge for ΔE_V, and a corresponding value of 87 meV/10% Ge when the relaxed Si value is used for N_V. These values are slightly higher than the theoretical result of 74 meV/10% Ge [58]. It should be noted that in the work of King et al. [25] who obtained 75 meV/10% Ge, the relaxed Si value of N_V was assumed for the strained $Si_{1-y}Ge_y$ layer.

3.4.2 Strained Si on Relaxed $Si_{1-x}Ge_x$

In Figure 3-6 the ΔE_V for the single channel structure of strained Si on relaxed $Si_{1-x}Ge_x$ layer is shown. The data follows the theory predicted by People, and the experimental results of Welser [62]. N_V for relaxed Si was assumed for all layers in the analysis by Welser. The large spread in theoretical results can be seen from the deviation in theory between People [58] and Schaffler [21] for ΔE_V between strained Si and relaxed $Si_{1-x}Ge_x$.



(a) (b)

Figure 3-7: (a) Extracted E_V for strained Si on strained $Si_{1-y}Ge_y$ on various relaxed $Si_{1-x}Ge_x$ substrates. The strained $Si_{1-y}Ge_y$ on relaxed Si substrate result from Figure 3-5 is plotted. The strained Si on relaxed $Si_{1-x}Ge_x$ data from Figure 3-6 is included as the first data point for each substrate curve. The 31% substrate is compared to theory in (b).

3.4.3 Strained Si on strained $Si_{1-y}Ge_y$ on relaxed $Si_{1-x}Ge_x$

Extracted ΔE_V for strained Si on strained $Si_{1-y}Ge_y$ is plotted in Figure 3-7. ΔE_V is plotted as a function the Ge fraction, y, in the $Si_{1-y}Ge_y$ strained layer for three different relaxed $Si_{1-x}Ge_x$ substrate compositions. From the results we see that ΔE_V increases with both composition in the strained layer, y, and strain. For a given substrate composition,ΔE_V increases linearly with Ge content y. A line fit to the data gives a slope of 105, 97, 99 meV / 10% Ge in the $Si_{1-y}Ge_y$ strained layer for relaxed $Si_{1-x}Ge_x$ substrates with x of 0.19, 0.31 and 0.40 respectively. This follows the trends predicted by theory [58] [21], with a slope of 74 meV / 10% Ge. It should also be noted that band offsets as large as 500 to 550 meV, which will lead to good confinement of holes in the $Si_{1-y}Ge_y$ layer, have been demonstrated in this work.

The results in Figure 3-7 can be summarized in a simple formula where ΔE_V (in meV) between the strained Si and strained SiGe layer is given by

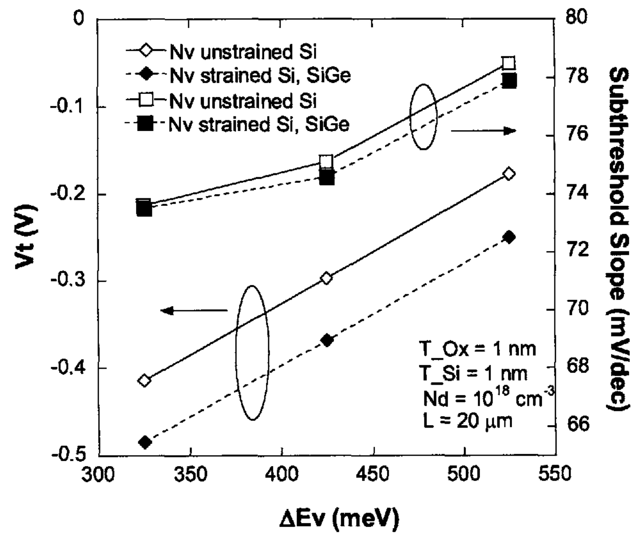


Figure 3-8: Simulated V_T and subthreshold slope versus ΔE_V for dual channel p-MOSFET on relaxed $Si_{0.7}Ge_{0.3}$ substrate with N_V for unstrained Si and strained Si and $Si_{1-y}Ge_y$.

$$\Delta E_V = -197x^2 + 557x + 1000(y - x) \tag{3.1}$$

where x and y are the Ge fraction in the relaxed and strained SiGe layer respectively.

3.4.4 p-MOSFET Characteristics

The impact of ΔE_V on threshold voltage, V_T, and subthreshold slope, SS, for a p-MOSFET dual channel structure is shown in Figure 3-8. At this doping level, 10^{18} cm^{-3}, the V_T is very sensitive to the value of ΔE_V, with 120 mV shift in V_T for 100 meV shift in ΔE_V. The value of N_V has a significant impact on V_T and demonstrates the importance of using appropriate values of ΔE_V and N_V for accurate modeling of these devices.

3.5 Chapter Summary

MOS C-V analysis has been used to extract critical band parameters for strained Si/strained $Si_{1-y}Ge_y$ dual-channel structures. On structures where previous experimental data exists, the results of this study compare well with published values when the N_V value used is taken into account. Extracted ΔE_V for strained Si on strained $Si_{1-y}Ge_y$ follows the trend predicted by theory. Valence band offsets as large as 500 meV have been demonstrated in this work (e.g. for y=0.7, x=0.3). Such large values will produce good hole confinement and high mobility in dual-channel p-MOSFETs. These band parameters are essential for modeling such high mobility structures accurately.

Chapter 4

Mobility in Compressively Strained SiGe Heterostructure pMOSFETs

Mobility enhancements over a Si control of up to 10X [5] and 3X [65] have been demonstrated for compressively strained Ge on a $Si_{0.5}Ge_{0.5}$ virtual substrate and relaxed Si substrate respectively. The difference in mobility is due to the Ge channel thickness for each structure, where the critical thickness due to the large lattice mismatch limits the channel thickness to 2 nm for Ge grown on a relaxed Si substrate, compared to the 12 nm Ge channel grown on the $Si_{0.5}Ge_{0.5}$ virtual substrate. For integration of compressively strained SiGe channels with commercial CMOS, growing SiGe directly on bulk Si is much simpler than using a virtual substrate. Therefore it is very important to understand the impact of channel thickness on mobility.

In this chapter the mobility of compressively strained SiGe heterostructure pMOSFETs is investigated. The impact of Ge fraction in the strained SiGe channel and the relaxed virtual substrate, as well as the level of strain and strained SiGe channel thickness are investigated in detail. A large range of Ge fractions in the strained layer and the relaxed substrate are investigated in order to map the design space and understand the mobility trade off for strained SiGe channels grown on virtual substrates and relaxed Si substrates.

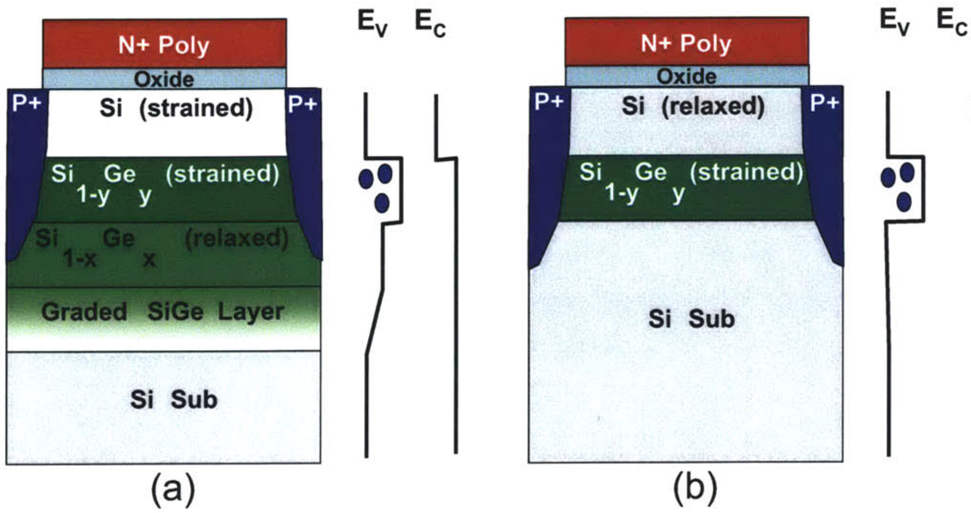


Figure 4-1: pMOSFET structure and schematic energy band diagram for strained $Si_{1-y}Ge_y$ on relaxed $Si_{1-x}Ge_x$ ($x < y$) (a) and relaxed Si substrate (b).

4.1 SiGe pMOSFET hetrostructure

In this section the fabrication of heterostructure p-MOSFETS for mobility analysis is outlined. The layer structures studied are illustrated in Figure 4-1 for (a) a virtual substrate and (b) the pseudomorphic structure (bulk Si substrate). The virtual substrate was grown as outlined in Section 3.2. The strained $Si_{1-y}Ge_y$ layer was then grown at temperatures ranging from 525°C to 365°C with Ge compositions ranging from 0.4 to pure Ge. A strained Si cap layer was grown at 600°C. For the majority of devices, the gate oxide consists of 3.5 nm thermal oxide grown at 600°C in a wet ambient. For Ge channel devices 7 to 11 nm gate oxide deposited by LPCVD at 400°C was used in place of thermal oxide, to reduce the thermal budget. The epitaxial layers were grown on highly doped n-type substrates (0.005 - 0.01 Ω-cm) to ensure a good substrate contact and minimize series resistance effects. The graded buffer and constant composition relaxed layer were in-situ doped with Phosphorus to a doping level of 10^{17} cm^{-3} during epitaxial growth. The mobility is measured on 50 μm x 50 μm LxW p-MOSFETs unless otherwise stated. The final germanium compositions were measured using SIMS and high resolution RBS.

The thermal budget of the process was kept low to minimize the inter-diffusion

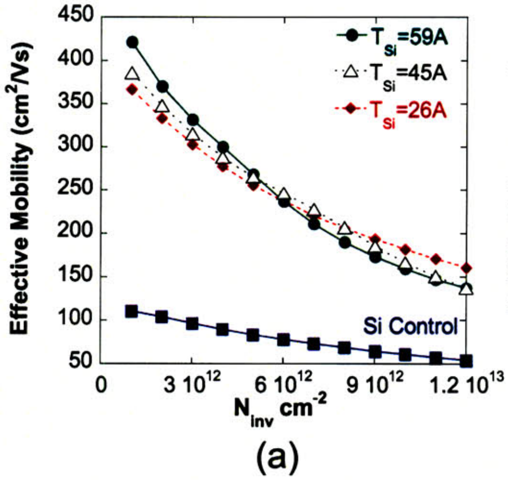


Figure 4-2: Effective mobility as a function of N_{inv} for various Si cap thickness, T_{Si} for the $Si_{0.3}Ge_{0.7}$ on $Si_{0.6}Ge_{0.4}$ structure and (b) enhancement over Si control. Mobility enhancement at high N_{inv} is dependent on Si cap thickness.

of the SiGe layers which has been shown to be an issue for these structures [7]. The gate was formed by depositing 150 nm of Phosphorus in-situ doped polysilicon by LPCVD at 560°C. Source drain activation was achieved through a rapid thermal anneal, RTA, of 10 seconds at 800°C for strained Ge channel composition up to 70 at. %, 700°C for Ge channel composition above 70 at. % and 650°C for strained Ge channels. A 30 minute forming gas anneal at 500°C was performed prior to metallization to passivate oxide interface states, D_{it}, in the gate oxide. The final devices were annealed in forming gas at 420°C for 30 minutes to minimize D_{it} post metal deposition and etch.

4.2 Si Cap Thickness Dependence of Mobility

A Si capping layer is required on top of the strained SiGe channel in order to make a high quality low defect interface with the gate dielectric. Hole mobility for strained Si/Strained $Si_{0.7}Ge_{0.3}$ on relaxed $Si_{0.4}Ge_{0.6}$ heterostructure pMOSFETs with a range of Si cap thickness values is shown in Figure 4-2 (a). The data presented here are for ring MOSFETs with L x W of 50 x 1000 μm . The Si cap thickness was extracted on each device by fitting measured capacitance-voltage characteristics to simulations as

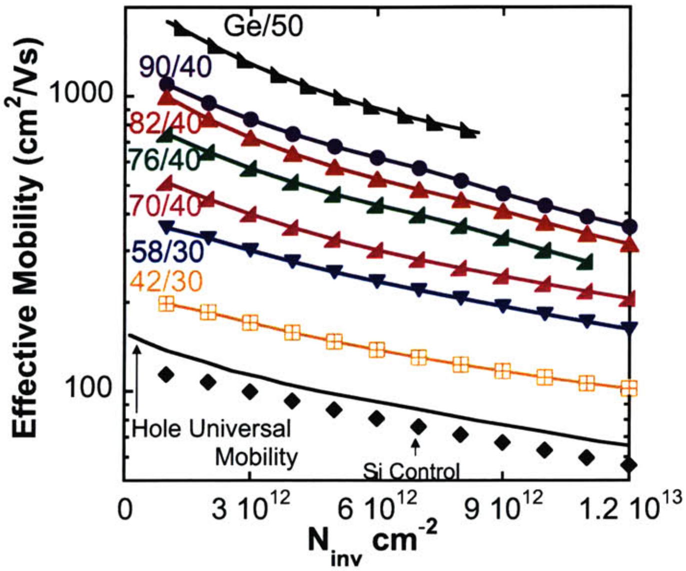


Figure 4-3: Effective hole mobility for strained Si/strained $Si_{1-y}Ge_y$ (y=0.4 to 1)/relaxed $Si_{1-x}Ge_x$ structures, denoted as y/x for each curve, for devices listed in Table 4.1.

discussed in Section 3.3.1.

Hole mobility enhancement over a Si control is shown in Figure 4-2 (b). At high N_{inv} enhancement is strongly dependant on the Si cap thickness, as in [5] [7]. At low N_{inv} the majority of carriers are in the high mobility strained $Si_{0.3}Ge_{0.7}$ channel. At higher N_{inv} (applied gate bias) with sufficient band bending at the surface the carriers start to populate the lower mobility Si cap layer leading to a reduction in mobility. Thinner Si caps require a larger gate potential/band bending to induce inversion in the cap layer. Therefore, for a thinner cap at a high N_{inv} more of the hole charge remains in the SiGe layer, yielding higher mobility at high N_{inv}. This demonstrates the importance of minimizing the Si cap thickness.

4.3 Hole Mobility Dependence on Ge Fraction

In order to map the design space, a wide range of Ge fractions was investigated. Hole mobility for Ge fraction in the strained $Si_{1-y}Ge_y$ channel with $0.4 \leq y = 1$ and Ge fraction in the relaxed $Si_{1-x}Ge_x$ virtual substrate of $0.3 \leq x \leq 0.5$ is shown in Figure 4-3.

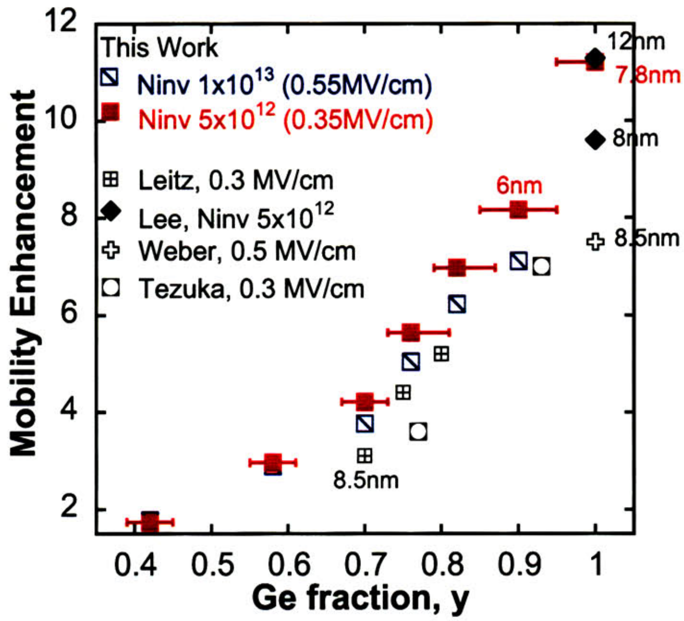


Figure 4-4: Hole mobility enhancement relative to Si control devices at N_{inv} of 5 x 10^{12} and 1 x 10^{13} cm^{-2}. Previously published results are also shown for dual channel [4] [5] [66] and Ge condensation technique structures [67]. The N_{inv} or corresponding Vertical Effective Field, E_{eff} values at which the mobility enhancements are quoted is indicated in the legend. Device structure listed in Table 4.1

The mobility data is based on the results of three experimental fabrication lots. The hole mobility increases with increasing Ge fraction in the strained $Si_{1-y}Ge_y$ channel. The oxide and Si cap and strained SiGe channel thickness is given in Table 4.1.

Table 4.1: Gate oxide, Si cap thickness and strained SiGe channel thickness for devices plotted in Figure 4-3.

y	x	SiGe Channel (nm)	Si Cap (nm)	T_Ox (nm)
0.42	0.3	11	2.5	3.5
0.58	0.3	13	2.5	3.5
0.70	0.4	13	2.7	3.5
0.76	0.4	9	4.5	3.5
0.82	0.4	9	4.5	3.5
0.90	0.4	6	5	7
1.0	0.5	8	3.4	11

Mobility enhancements ranging from 2x up to 10x are achieved for y=0.4 to 1. The hole mobility enhancement based on the data in Figure 4-3, at inversion charge

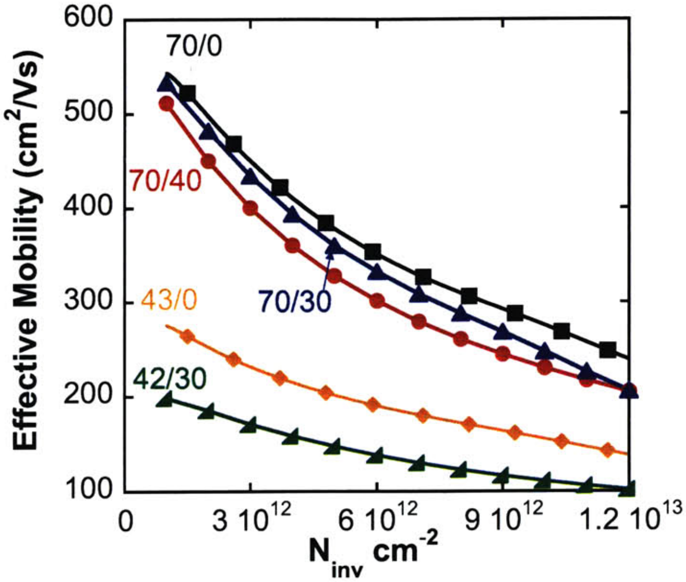


Figure 4-5: Effective hole mobility for strained Si/strained $Si_{1-y}Ge_y$ (y=0.4 and 0.7) on various relaxed $Si_{1-x}Ge_x$ substrates (x=0,0.3 and 0.4). Level of strain has relatively small effect on mobility in the range investigated.

densities, N_{inv}=5 and 10 x 10^{12} cm^{-2} is shown in Figure 4-4, along with previously published values [4] [5] [66] [67]. It is very important to take into account the strained Si and strained SiGe film thickness when comparing results from different work, since Si cap thicknesses vary significantly and thus mobility enhancements can differ at low and high vertical electric fields. In addition, for film thicknesses less than 10 nm, the mobility varies with the strained $Si_{1-y}Ge_y$ channel thickness, which can make comparison difficult. This is of special concern for films with high Ge fraction where the level of strain limits the maximum film thickness before relaxation occurs. The mobility enhancements achieved in this study compare very well to the previously published results.

4.4 Hole Mobility Dependance on Strain

Hole mobility versus strain is plotted in Figure 4-5. This data suggests there is some increase in mobility with strain although it is not significant at the level of

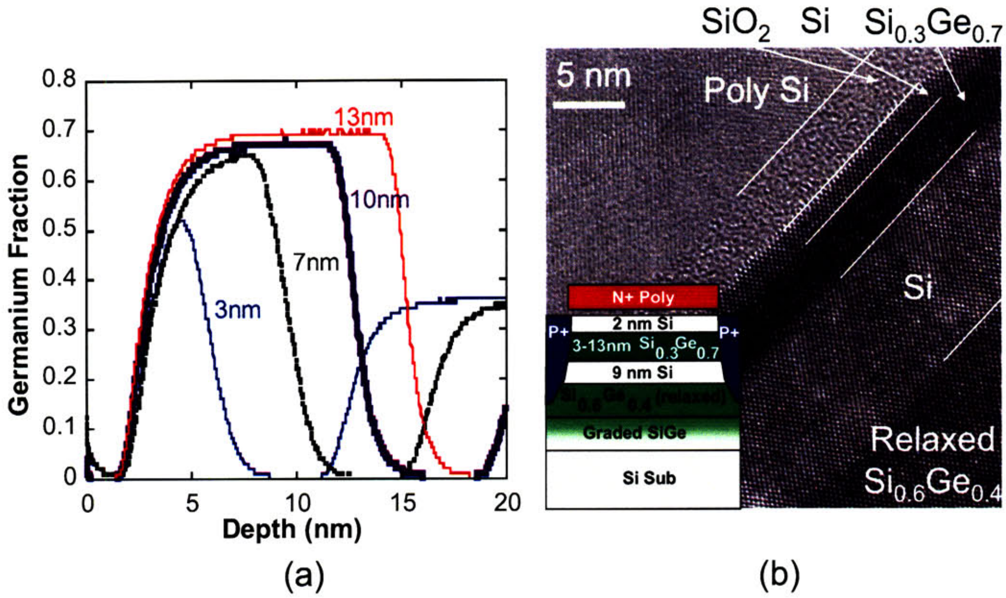


Figure 4-6: (a) Low energy SIMS (250eV) for strained $Si_{0.3}Ge_{0.7}$ on relaxed $Si_{0.6}Ge_{0.4}$ virtual substrate (structure shown in inset of (b)). The 10 - 13 nm thick SiGe channels have a peak Ge concentration of 70% which is reduced to 65% and 56% for the 7 nm and 3 nm film respectively. (b) XTEM for extraction of the channel thickness for the 3 nm channel. SIMS courtesy of H.-Ulrich Ehrke, CAMECA GmbH. XTEM courtesy of A. Domenicucci, IBM.

strains investigated. As described in Section 2.2.1 the initial introduction of biaxial compressive strain decreases the band edge heavy hole mass. This band-edge mass does not change with increasing strain. Increasing strain results in increased warping of the HH band and a reduction of effective mass at energies higher than the band edge. There is also increased splitting of the HH/LH bands with increasing strain leading to the reduction of inter-band phonon scattering. In order to fully understand the effect of strain, the mobility for relaxed SiGe alloys is required. Unfortunately there is very little suitable experimental data available for comparison. Available data suggests that bulk hole mobility is less than that of silicon for Ge fractions less than 0.6 due to the very large impact of alloy scattering [69] [70] [71]. For a review of bulk SiGe hole mobilities see [72].

4.5 Hole Mobility Dependence on Channel Thickness

As outlined in the introduction to this chapter, it is very important to understand the impact of the strained SiGe channel thickness on mobility. The maximum channel thickness allowed is constrained by the critical thickness for dislocation formation and strain relaxation, and thus the dependence of the mobility on channel thickness must be understood. In this section two structures are investigated to examine the relationship between mobility and strained SiGe channel thickness. In Section 4.5.1 the strained Si/ strained $Si_{0.3}Ge_{0.7}$/ relaxed $Si_{0.6}Ge_{0.4}$ heterostructure is investigated. A more in depth study of channel thickness is carried out in Section 4.5.2 on the strained $Si_{0.57}Ge_{0.43}$ on bulk Si heterostructure.

4.5.1 Strained $Si_{0.3}Ge_{0.7}$ on relaxed $Si_{0.6}Ge_{0.4}$

A tri-layer heterostructure, Figure 4-6 inset, with a strained Si layer above and below the strained SiGe channel, was used to investigate the impact of SiGe film thickness on hole mobility. This structure maximizes hole confinement in the strained SiGe channel compared to the standard structure (Figure 4-1 (a)) since the band offset at the strained $Si_{0.3}Ge_{0.7}$/relaxed $Si_{0.6}Ge_{0.4}$ interface is 315 meV compared to 470 meV at the strained $Si_{0.3}Ge_{0.7}$/strained Si interface [64]. The $Si_{0.3}Ge_{0.7}$ channel film thickness and Ge fraction was measured using low energy SIMS, Figure 4-6 (a). The thickness of the thinnest film was measured using XTEM, Figure 4-6 (b), and the Ge fraction was found by integrating over the SIMS curve. The Ge fraction for the 3 nm film was found to be 0.56 which is significantly lower than 0.7 for the thickest film. The drop in Ge fraction is thought to be due to Si-Ge interdiffusion.

The measured hole mobility for strained Si/ strained $Si_{0.3}Ge_{0.7}$ heterostructures decreases with decreasing buried SiGe layer thickness, as shown in Figure 4-7 (a). The mobility enhancement factor relative to Si control devices is shown in Figure 4-7 (b). There is very little change in mobility for film thicknesses between 13 and 7

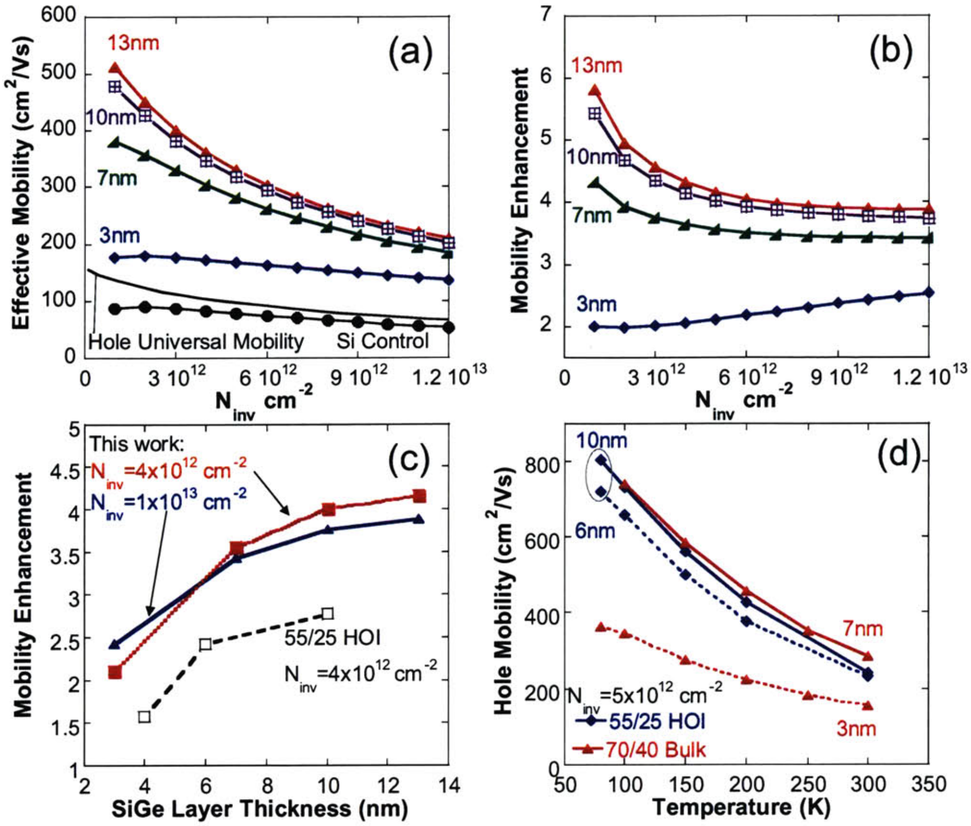


Figure 4-7: (a)Effective hole mobility and (b) mobility enhancement over a Si control as a function of inversion charge density, N_{inv}, for strained Si/strained $Si_{0.3}Ge_{0.7}$/relaxed $Si_{0.6}Ge_{0.4}$ structures, extracted on 50 μm x 50 μm devices using the split C-V technique. Si cap layer thickness is 2-3 nm for all devices. (c) Enhancement at N_{inv}=1 x 10^{13} cm^{-2} (triangles) and 4 x 10^{12} cm^{-2} (squares) versus strained SiGe layer thickness. Solid symbols represent data from this work and open symbols show results for strained Si (25%)/strained $Si_{0.45}Ge_{0.55}$/strained Si (25%) HOI structures [68]. (d) Temperature dependance of hole mobility for bulk and HOI structures plotted in (c).

nm, while there is a significant decrease in mobility when the SiGe channel thickness is reduced to 3 nm. This is demonstrated more clearly in Figure 4-7 (c) where the mobility enhancement at inversion charge densities of 4 x 10^{12} cm^{-2} and 1 x 10^{13} cm^{-2} is plotted versus strained $Si_{0.3}Ge_{0.7}$ channel thickness. Results for heterostructure on insulator (HOI) $Si_{0.45}Ge_{0.55}$ strained to a virtual substrate of $Si_{0.75}Ge_{0.25}$ are shown for comparison [68]. Both structures show a similar mobility dependence on strained SiGe channel thickness. The temperature dependence of mobility is shown in Figure 4-7 (d). Mobility increases with decreasing temperature as would be expected for phonon

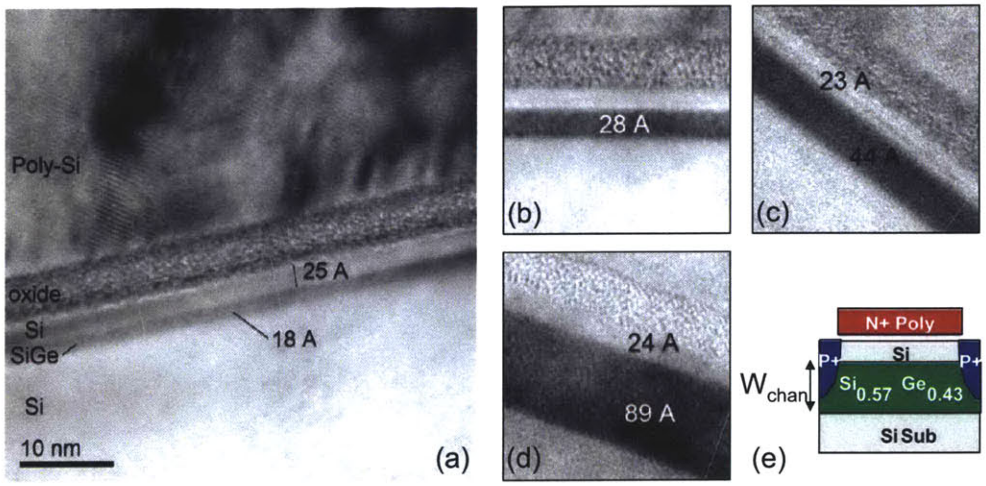
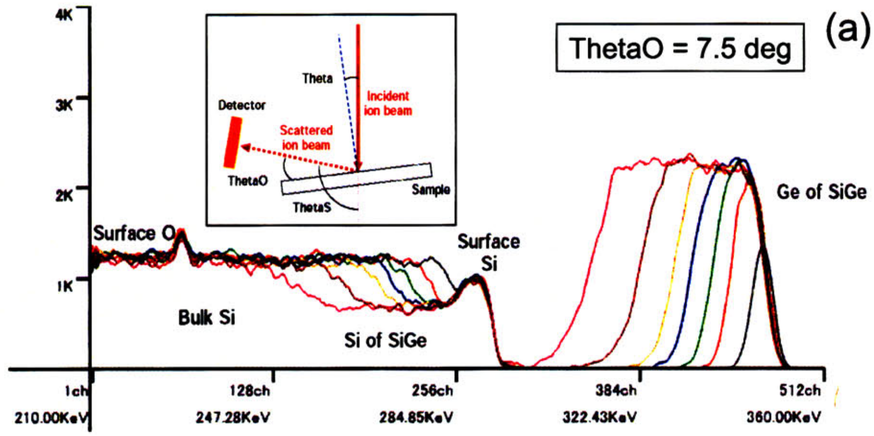


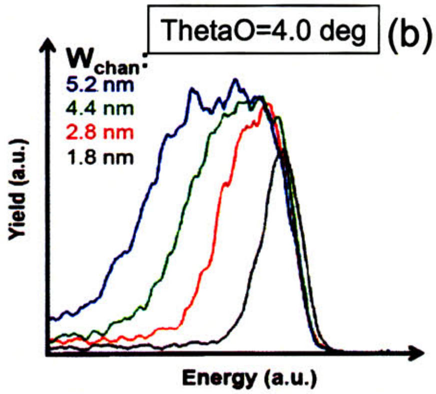
Figure 4-8: XTEM (a) - (d) and schematic of structure (e) indicating the channel thickness, W_{chan}, for the strained $Si_{0.57}Ge_{0.43}$ on bulk Si pseudomorphic structure. XTEM courtesy of N. D. Theodore of Freescale Semiconductor, Inc.

limited mobility. However, there is a smaller dependence on temperature shown for the 3 nm strained $Si_{0.3}Ge_{0.7}$ channel. Unfortunately the change in Ge fraction with film thickness makes it difficult to do a more rigorous analysis of the mechanism for mobility degradation. This issue is addressed in the following section.

4.5.2 Strained $Si_{0.57}Ge_{0.43}$ on bulk Si

As shown in Section 4.5.1 mobility degrades for decreasing strained SiGe channel thickness. However, this experiment was not ideal as there was a reduction in the Ge fraction for the thinnest film due to Ge diffusion. In order to do a more thorough investigation of the impact strained SiGe channel thickness on hole mobility, a pseudomorphic structure (Figure 4-1 (b)) with a strained channel of $Si_{0.57}Ge_{0.43}$ was chosen. This structure has a number of advantages over the 70/40 heterostructure examined in Section 4.5.1. First, the lower of Ge fraction in the strained layer will reduce Si-Ge inter-diffusivity and thus the peak, as-grown Ge fraction in the thinner channels can be maintained during the fabrication process. In addition, growing the strained SiGe channel directly on bulk Si simplifies the metrology for channel thickness (W_{chan}) and Ge fraction extraction.





(c)

XTEM	HR-RBS	
T_{SiGe} (nm)	T_{SiGe} (nm)	Ge
1.8	1.8	0.36
2.8	2.7	0.43
4.4	3.9	0.43
	5.2	0.43
	6.5	0.43
8.9	**8.9**	0.43
	12.7	0.43

Figure 4-9: (a) HR-RBS for for the strained $Si_{0.57}Ge_{0.43}$ on bulk Si pseudomorphic structure for exit angle, ThetaO, of 7.5 degrees (angle definition in inset). Measurement spot size $\sim$ 100 μm (b) Ge signal for thinnest films at ThetaO=4.0 degrees (higher depth resolution with smaller angle). (c) Ge composition and W_{chan} determined from XTEM and HR-RBS. W_{chan} from HR-RBS determined by fixing the 8.9 nm channel based on XTEM and interpolating for the other films, based on the Ge signal at full width half max, FWHM. HR-RBS results courtesy of Kobe Steel, LTD.

4.5.2.1 Film Thickness and Ge Fraction Extraction

The strained $Si_{0.57}Ge_{0.43}$ channel thickness, W_{chan}, was determined by XTEM for four of the films. The XTEM results are shown in Figure 4-8 (a)-(d), along with a schematic of the structure in (e). The Si cap thickness was found to be 2.4 nm $\pm$ 0.2 nm for all the structures. The Ge fraction for all the films was determined by high resolution RBS, and is shown in Figure 4-9 (a) for an output angle of 7.5 degrees(ThetaO, illustrated in the inset of Figure 4-9 (a)). A smaller output angle increases the depth resolution. The Ge signal for an output angle of 4.0 degrees for the four thinnest films suggests that the peak Ge fraction is the same for all but the thinnest film (Figure 4-9 (b)). The thinnest film shows a peak Ge fraction of 0.36. However, the RBS spectrum for this film does not have a flat top suggesting that the film is not fully resolved. This leads to large uncertainty in the peak Ge concentration for the thinnest film, although a lower bound of 36 at. % can be assumed. Simulation of the C-V profile (to be discussed in the next section) suggests that the peak Ge composition in the thinnest film is ~40 at. %. Where XTEM was not done, W_{chan} was obtained by fitting the film thickness of the 8.9 nm film to the HR-RBS data and extracting the thickness for the other films based on the width of the Ge peak. The calculated film thickness and peak Ge fraction obtained by XTEM and HR-RBS are shown in Figure 4-9 (c).

4.5.2.2 Hole Distribution in SiGe Heterostructure

In order to analyze the mobility degradation versus W_{chan} it is important to be able to determine the carrier distribution within the heterostructure for varying W_{chan}. This was done by fitting 1-D Schrödinger-Poisson simulations to the measured C-V characteristics of MOSFETs using *nextnano*^{3} [29]. The measured and simulated C-V curves are plotted in Figure 4-10 (a) using the channel thickness extracted from XTEM in the simulations. Oxide thickness and Si cap thickness were used as fitting parameters. The valence band offset between the Si and strained SiGe was also used as a fitting parameter and was found to be 400 meV for all but the thinnest film. This is good agreement with predicted value of 430 meV based on work in Section 3.4.3. A band offset of 370 meV was used for the 1.8 nm-thick film suggesting that the Ge composition is approximately 3 at. % lower than the thicker films. The valence band effective masses used were extracted from 6x6 k.p simulations as outlined in Section 2.2.1. The simulations fit the measured data very well. The hole density can then be extracted from the simulation, as shown in Figure 4-10 (b) for N_{inv} of $4x10^{12}$ cm^{-2}. The percentage holes in the strained $Si_{0.57}Ge_{0.43}$ channel is plotted in Figure 4-10 (c).

There is an increase in the ground state energy in the channel due to quantum

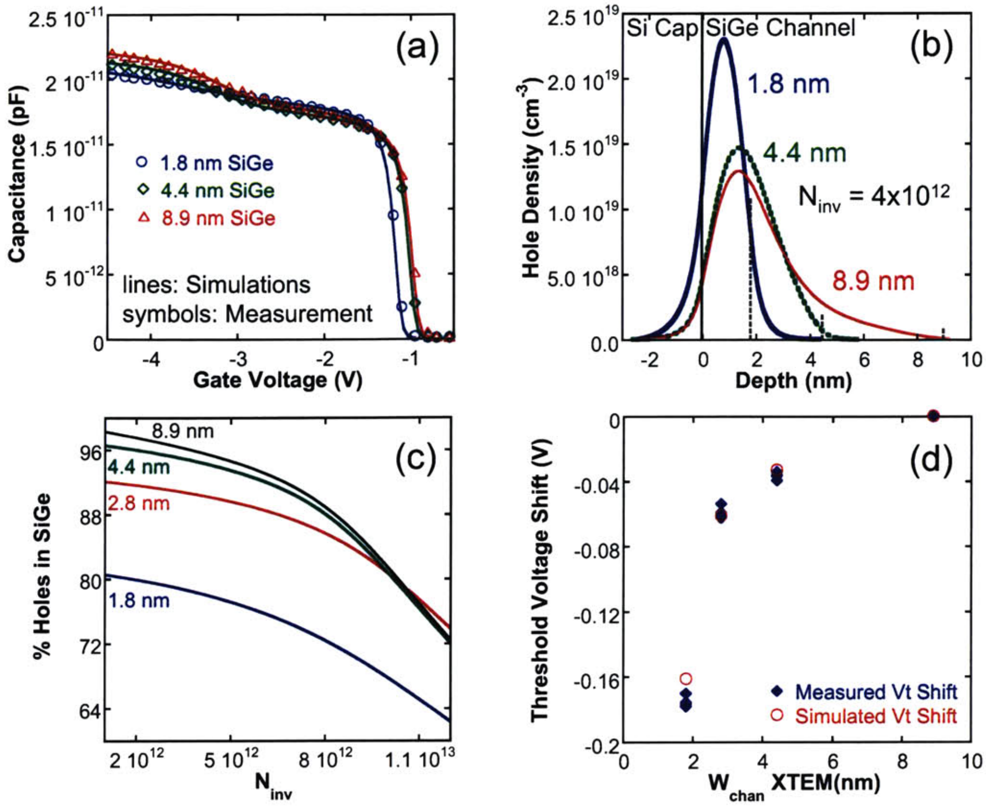


Figure 4-10: (a) Simulated and measured C-V for W_{chan} of 1.8, 4.4 and 8.9 nm-thick strained $Si_{0.57}Ge_{0.43}$ channel. The valence band offset was reduced by 30 meV for the 1.8 nm-thick channel suggesting a reduction of the Ge concentration of 3 at. %. W_{chan} from XTEM used in simulation. (b) Hole density distribution extracted from simulation for 4x10^{12} cm^{-2} N_{inv}. (c) Simulated % holes in the strained $Si_{0.57}Ge_{0.43}$ channel as a function of N_{inv}. (d) Measured and simulated threshold voltage (V_T) shift with respect to the 8.9 nm device

confinement which leads to an increase in the magnitude of the threshold voltage, $\mid V_T \mid$, for thinner films. Further confirmation of the accuracy of the simulation fit to the measured data is obtained by comparing the measured shift in threshold voltage, V_T, for the thinner channels with respect to the 8.9 nm channel to the V_T shift from simulation (Figure 4-10 (d)).

4.5.2.3 Effect of W_{chan} on Mobility

The mobility for the strained $Si_{0.53}Ge_{0.43}$ on bulk Si pMOSFETs is plotted for varying W_{chan} in Figure 4-11 (a). Mobility degrades with decreasing W_{chan} for W_{chan} below

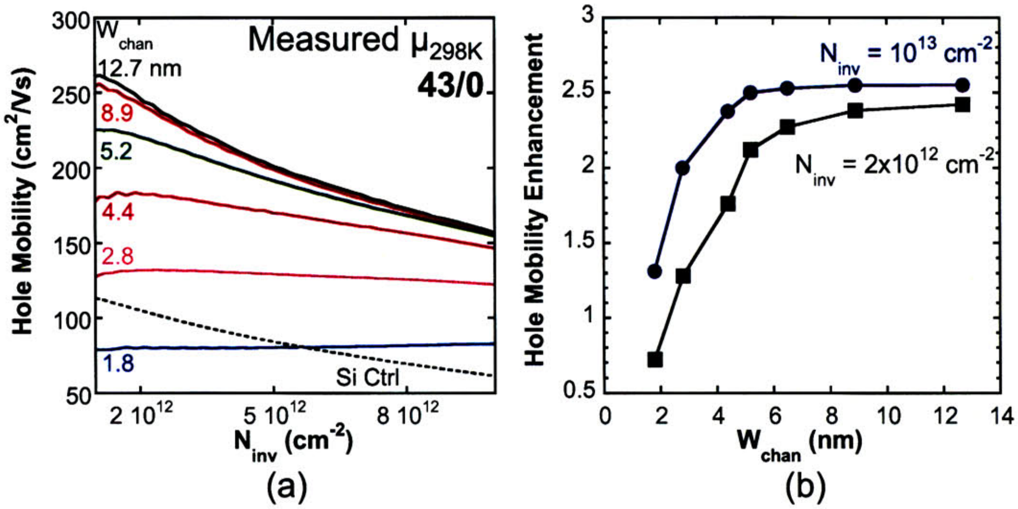


Figure 4-11: (a) Effective hole mobility for the strained $Si_{0.53}Ge_{0.43}$ on bulk Si pMOSFET for varying W_{chan}. (b) Mobility enhancement as a function of W_{chan} at 2x10^{12} cm^{-2} and 10^{13} cm^{-2} N_{inv}.

8.9 nm. For W_{chan} down to 4.4 nm the mobility degradation is dominant at low N_{inv} and the mobility converges at high N_{inv}. For W_{chan} below 4.4 nm the mobility is degraded at all N_{inv}. For the thinnest channels the mobility is almost independent of N_{inv}. Mobility enhancement over a Si control device versus W_{chan} is plotted in Figure 4-11 (b) for N_{inv} of 2x10^{12} and 10^{13} cm^{-2}. Enhancement of 2.5X is achieved at high N_{inv} for W_{chan} above 4 nm. Figure 4-10 (c) shows the simulated percentage of holes in the SiGe channel versus N_{inv} for W_{chan} from 1.8 nm up to 8.9 nm. For the 1.8 nm W_{chan} there is some loss of carriers due to penetration of the wavefunction into the surrounding layers. However, the drop in carriers in the SiGe from 96% for the 8.9 nm channel to 80% for the 1.8 nm-thick channel is not sufficient to explain the large drop in mobility seen between these channel thicknesses. Therefore, some other mechanism is required to explain the drop in mobility for the thinner films. The following sections discuss these mechanisms.

4.5.2.4 Phonon Scattering

Acoustic phonon scattering is expected to increase with decreasing W_{chan} due to confinement as discussed in Section 2.2.2. As a reminder of the relevant equations, the scattering rate in a 2-D quantum well is given by

$$\frac{1}{\tau_{fi}} = \frac{\pi D_A^2 k_B T_L}{\hbar c_l} \frac{1}{W_{fi}} g_{2Df}(E) \tag{4.1}$$

where W_{fi} is the effective width of the channel or inversion layer, leading to a phonon limited mobility dependence of

$$\mu_{ph} \propto W_{fi} \tag{4.2}$$

The phonon limited mobility, μ_{ph}, which is dominant at room temperature, is temperature dependent, as shown in Figure 2-7, with μ_{ph} increasing with decreasing temperature. At sufficiently low temperature (below 25K) phonon scattering becomes negligible and the low temperature mobility, μ_{LowT} is dominated by other mechanisms. The μ_{ph} can be extracted from the room temperature mobility, μ_{298K} as outlined by Takagi [32] using Matthiessen's rule where

$$\frac{1}{\mu_{ph}} = \frac{1}{\mu_{298K}} - \frac{1}{\mu_{LowT}} \tag{4.3}$$

It should also be noted that while Matthiessen's rule is approximately valid in each subband, it overestimates the total mobility [73]. Therefore trends extracted using this method will be valid but it should not be used as an exact quantitative technique.

Due to the limitation of the low temperature measurement system, the low temperature mobility could only be measured down to 80K. However, in the work of Takagi et al. [32] very little increase in hole mobility was seen for temperatures between 77K and 30K. The hole mobility for the 8.9 nm channel is plotted in Figure 4-12 (a) for temperatures from 298K to 80K. Mobility was found to increase with decreasing temperature for all channel thickness down to 1.8 nm, indicating that some phonon scattering is still present at 80K. Figure 4-12 (b) shows the hole mobility versus temperature at N_{inv} of $3x10^{12}$ cm^{-2} for W_{chan} of 2.8, 4.4 and 8.9 nm. A line with slope of 1/T is fit to each curve. It can be seen from these curves, that while the mobility continues to increase with decreasing temperature, even at 80K, the dependence on temperature is significantly reduced, indicating a large reduction

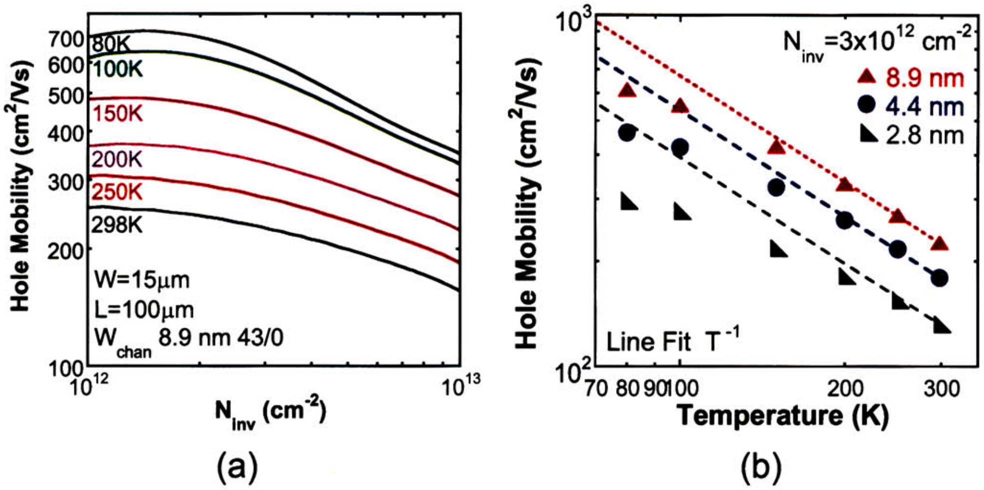


Figure 4-12: (a) Effective hole mobility as a function of N_{inv} for the strained 8.9 nm $Si_{0.53}Ge_{0.43}$ on bulk Si pMOSFET for varying temperature. (b) Measured temperature dependance of mobility for W_{chan} = 2.8, 4.4 and 8.9 nm (symbols). Lines represent fit $\propto T^{-1}$.

in phonon scattering.

An example of the μ_{ph} extraction using Equation 4.3 is plotted in Figure 4-13 (a). The phonon limited mobility should scale linearly with W_{fi}. In order to check the validity of the μ_{ph} extraction, W_{fi} was calculated and found to scale linearly with μ_{ph} giving confidence in the μ_{ph} extraction method. The details of these calculations are given in Appendix B. The extracted μ_{ph} for each W_{chan} is plotted in Figure 4-13 (b). For W_{chan} from 5 to 13 nm, μ_{ph} is shown to decrease with increasing N_{inv}. This correlates to a reduction in the effective channel width, W_{fi} from Equation 4.1, due to increased confinement with increasing vertical field. This is the same behavior as seen in a bulk Si MOSFET inversion layer, where increasing N_{inv}(vertical electrical field) leads to increased confinement in the inversion layer, and results in increased phonon scattering. For W_{chan} from 1.8 to 4.4 nm mobility is effectively independent of N_{inv}. In the thinnest channels, confinement of the carriers in the SiGe channel is defined by the channel thickness rather than the vertical electric field i.e. increasing the electric field does not lead to increased confinement. The drop in μ_{ph} seen above N_{inv} of 8x10^{12} cm^{-2} is due to inversion in the Si cap leading to carriers being lost from the SiGe channel. This is illustrated more clearly in the plot of percentage of

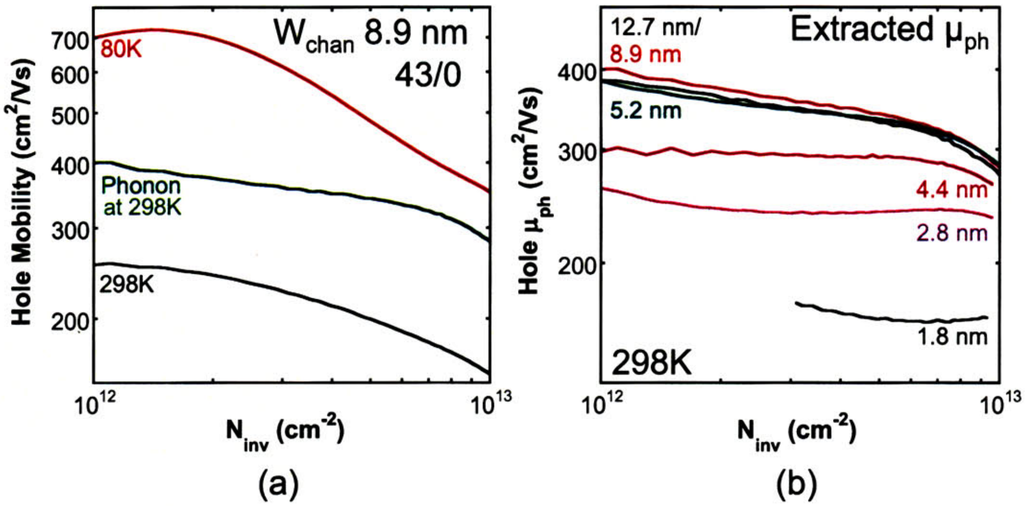


Figure 4-13: (a) Measured effective hole mobility at 298K and 80K and extracted phonon limited mobility at 298K using Matthiessen's rule, Equation 4.3 for W_{chan} of 8.9 nm. (b) Extracted phonon limited mobility as a function of N_{inv} for W_{chan} from 1.8 nm to 12.7 nm.

holes in the SiGe layer versus N_{inv} (Figure 4-10 (c)) where the % holes in the SiGe channel starts to drop for N_{inv} above 8x10^{12} cm^{-2}.

To summarize, μ_{ph} decreases for W_{chan} below 5 nm due to enhanced phonon scattering that arises from confinement in the thin channel. For thicker channels the mobility degrades with increasing N_{inv} due to increased confinement from the vertical electric field. However, while some of the room temperature mobility degradation can be accounted for by increased phonon scattering, it does not explain all the mobility degradation seen. This is illustrated in Figure 4-14 where μ_{ph} and μ_{298K} are plotted on the same scale in (a) and (b) respectively. This is especially true for the thinnest films where the extracted phonon limited mobility is over 2X the room temperature mobility. Therefore, another mechanism is contributing to the room temperature mobility degradation.

4.5.2.5 Interface Scattering

As discussed in Section 2.2.2, interface roughness scattering at the Si/gate dielectric interface is a significant source of mobility degradation in bulk Si MOSFETs, especially at higher N_{inv}(vertical effective fields). A number of mechanisms can contribute

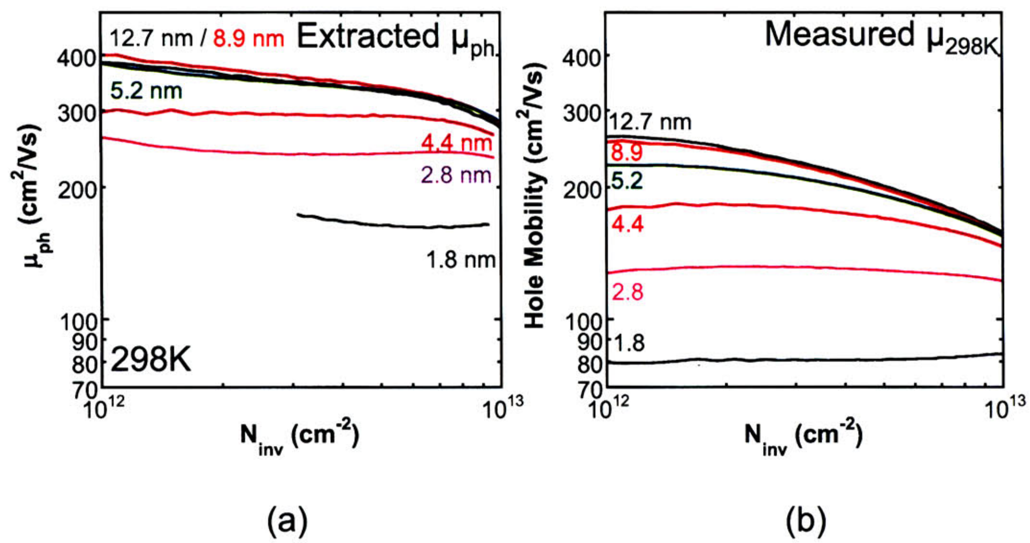


Figure 4-14: (a) Extracted phonon limited mobility and (b) measured room temperature mobility as a function of N_{inv} for W_{chan} from 1.8 nm to 12.7 nm. Same scale used on x and y axis.

to scattering at the interface in a SiGe heterostructure MOSFET including interface roughness at the Si/strained SiGe interface and strain or Ge composition fluctuation.

For interface roughness scattering the mobility is dependent on both the spatial variation in potential due to the interface roughness and the proximity of the carriers to the scattering potential. The potential and proximity dependence can be seen from the mobility equation. As shown in Section 2.2.2, the interface roughness limited mobility is proportional to the square of the scattering matrix element

$$\mu_{IR} \propto |M_{fi}|^2 \propto |\psi_i(z) H_{IR} \psi_f(z)|^2 \tag{4.4}$$

where H_{IR} is the perturbation potential and $\psi_{f/i}$ is the initial and final envelope function for the scattering particle. Therefore, interface roughness scattering will increase with increasing vertical electric field for two reasons. The potential perturbation will increase with increased band bending and the carriers will be forced closer to the interface with increasing field. A cartoon of interface roughness scattering is illustrated in Figure 4-15 (a). A hole moving in the x direction will see a potential that varies spatially with the surface roughness. This is clearly illustrated in Figure 4-15

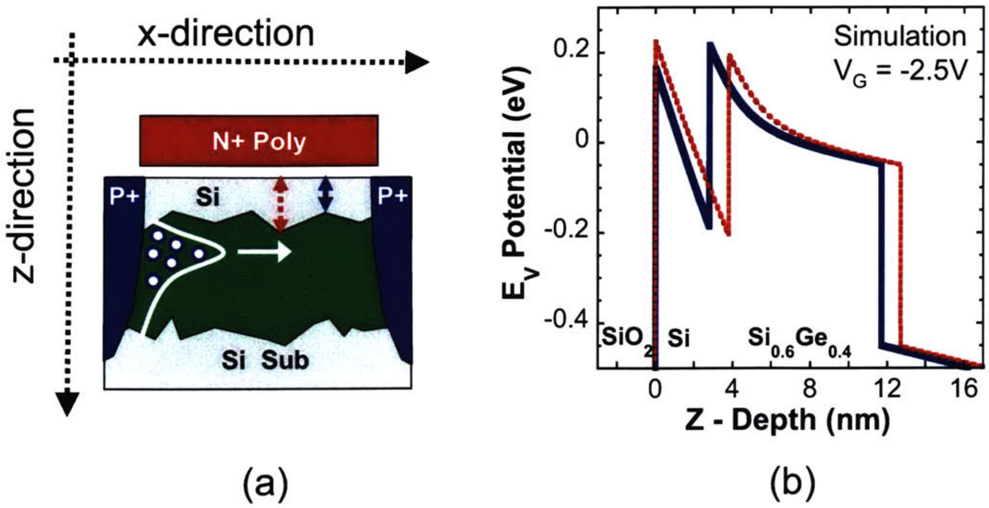


Figure 4-15: (a) Schematic of interface roughness for carriers moving in the x-direction with a vertical electrical field in the z-direction. (b) 1-D Schrödinger-Poisson simulation done in *nextnano*^{3} of the potential at two different points in the channel (Si cap thickness varied by 1 nm) is shown.

(b), where a simulation of the potential at two different points in the channel (Si cap thickness varied by 1 nm) is shown.

Strain and Ge composition can have a large effect on the band structure of the SiGe heterostructure, as discussed in Section 2.1. Strain and Ge composition fluctuation will be most significant at the Si/SiGe interface as the Ge composition transitions from the strained SiGe alloy to the Si cap. This will result in spatial variation of the valence band potential, resulting in increased scattering. Again, the level of scattering will depend on the proximity of the carriers to the scattering potential. Therefore, the scattering rate will depend on the vertical electric field and on the thickness of the channel, especially for the thinnest channels.

In order to determine the remaining scattering mechanisms we look at the low temperature mobility. From Figure 4-16, the mobility behavior with respect to N_{inv} can be divided into two sections. The thicker channels from 4 nm to 13 nm show a very similar dependence on N_{inv}, while the 1.8 nm and 2.8 nm channels behave quite differently. The increase in mobility with increasing N_{inv} for N_{inv} below 2x10^{12} cm^{-2} will be addressed in Section 4.5.2.7. In this section we will focus on the mobility for

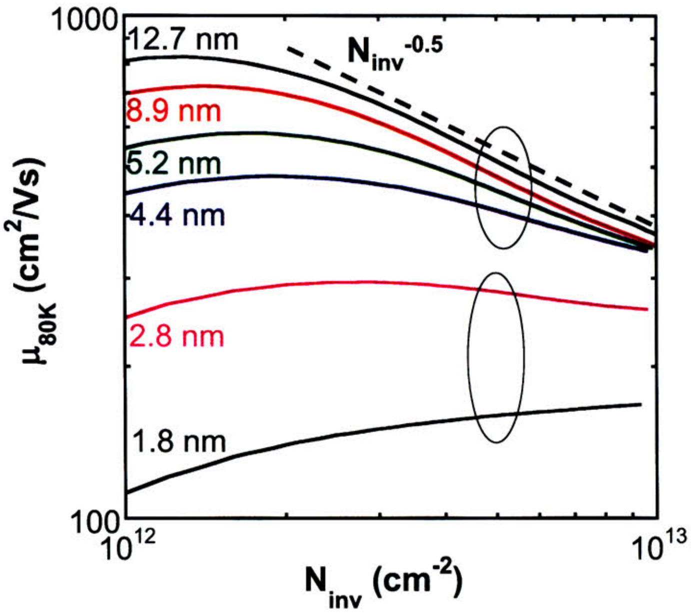


Figure 4-16: Measured effective hole mobility at 80K as a function of N_{inv} for W_{chan} from 1.8 nm to 12.7 nm. Dotted line is shown as guide to eye for $N_{inv}^{-0.5}$ dependence.

N_{inv} above 2x10^{12} cm^{-2}.

For W_{chan} 12.7 to 4.4 nm, μ_{80K} decreases with increasing N_{inv} with the biggest degradation at low N_{inv}. The mobility converges at high N_{inv}, which is consistent with scattering at the interface between the Si cap and SiGe channel. This can be illustrated more clearly by looking at the hole distribution in the SiGe channel. Figure 4-17 (a) shows the simulated hole distribution in the 4.4 nm and 8.9 nm channel at 2x10^{12} cm^{-2} N_{inv} at 300K. From this plot it can be seen that the channel thickness has a significant impact on the hole distribution. For the 4.4 nm film, the confinement due to the well thickness forces more carriers towards the top interface resulting in increased scattering compared to the 8.9 nm channel. This is further confirmed by plotting the accumulated hole density as function of depth (inset Figure 4-17 (a)). For example, 61% of the carriers are within 2nm of the Si/SiGe interface for the 4.4 nm channel compared to only 46% for the 8.9 nm film channel (25% difference). At N_{inv} of 9x10^{12} cm^{-2}, shown in Figure 4-17 (b), the hole density distribution for the 4.4 nm and 8.9 nm-thick samples are very similar. This convergence in hole distribution corresponds to the convergence in the mobility at higher N_{inv}. This convergence in

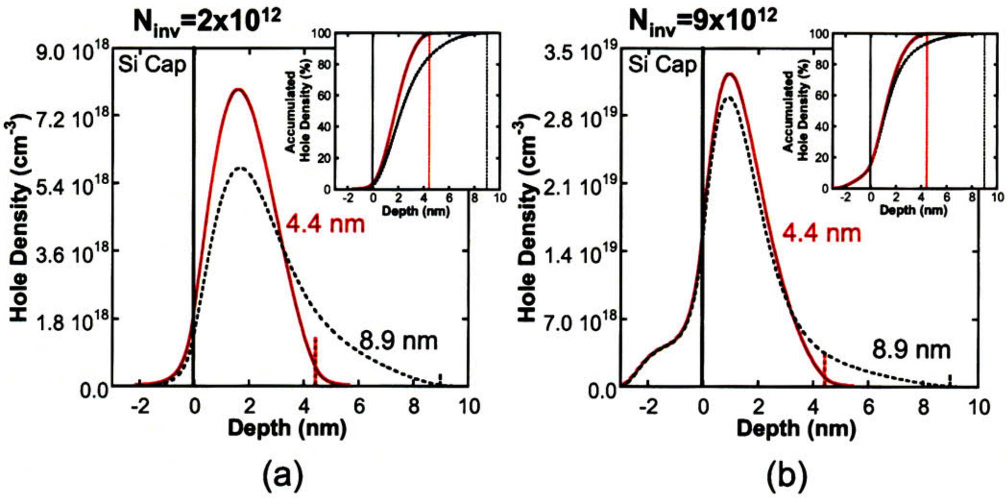


Figure 4-17: Hole density distribution for W_{chan} of 4.4 nm and 8.9 nm from 1-D Schrödinger-Poisson simulation done in *nextnano*^{3} for N_{inv} of 2x10^{12} cm^{-2} (a) and 9x10^{12} cm^{-2} (b). The inset shows the % accumulated hole density (integral of hole distribution over depth). Dotted line on x-axis indicates the bottom SiGe/Si interface. Simulations at 300K.

the accumulated hole density can also be seen in the inset.

For W_{chan} 1.8 nm and 2.8 nm the mobility behavior with respect to N_{inv} is quite different than for the thicker films. There is a large degradation in mobility at low N_{inv} and the mobility does not converge at high N_{inv}. Again it is insightful to look at the hole distribution in the channel to help understand what is happening here. The distance of the peak of the hole distribution to the Si/SiGe interface versus N_{inv} is plotted in Figure 4-18 (a) for W_{chan} from 1.8 nm to 8.9 nm. It is interesting to note that the trend with N_{inv} is very similar to the mobility trend with N_{inv} shown in Figure 4-16. For 1.8 nm and 2.8 nm-thick films, the position of the peak hole distribution is dominated by film thickness. The carriers are significantly closer to both the top interface and bottom interface compared to the thicker films. In fact, the peak is almost equidistant from the top and bottom interface suggesting that scattering is occurring at both interfaces for the 1.8 and 2.8 nm films. There is also very little dependence of the peak position on N_{inv} (vertical field) for the thinnest films.

The hole distribution at N_{inv} of 2x10^{12} cm^{-2} and 9x10^{12} cm^{-2} is plotted in Fig-

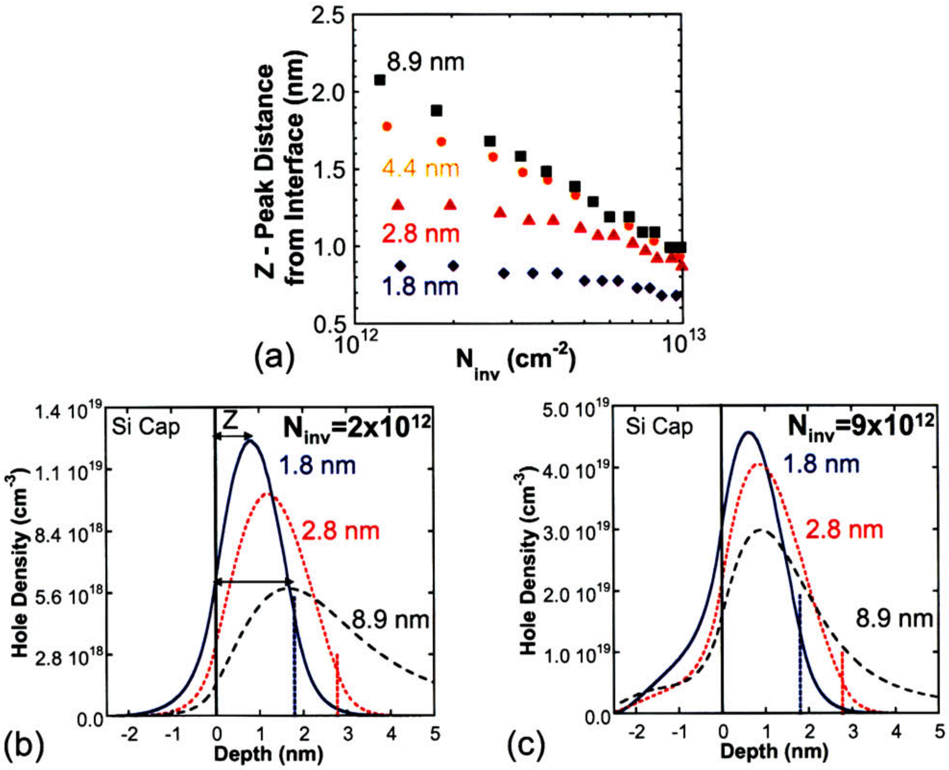


Figure 4-18: 1-D Schrödinger-Poisson simulation done in *nextnano*^{3} for(a) Distance from peak of hole distribution to the Si/SiGe interface as a function of N_{inv} for W_{chan} from 1.8 nm to 8.9 nm. Hole density distribution for W_{chan} of 1.8 nm, 2.8 nm and 8.9 nm for N_{inv} of (b) $2x10^{12}$ cm^{-2} (c) and $9x10^{12}$ cm^{-2}. Simulations at 300K.

ure 4-18 (b) and (c) respectively. This shows that at low N_{inv}, the confinement is due to W_{chan}, and unlike the case for the thicker films, the hole distribution does not converge at high N_{inv}. Therefore, for the thinnest films, the proximity of the carriers to the interface is dominated by the channel thickness with little influence from the vertical electric field. This confinement forces the carriers closer to both the top and the bottom interface leading to increased scattering compared to the thicker films.

4.5.2.5 Thickness Fluctuation Scattering

Thickness fluctuation scattering is similar to interface roughness scattering in that the mobility decreases with increasing roughness. However, thickness fluctuation scattering does not require a vertical electric field to produce the variation in the well potential, as the variation occurs naturally due to quantum confinement. Also,

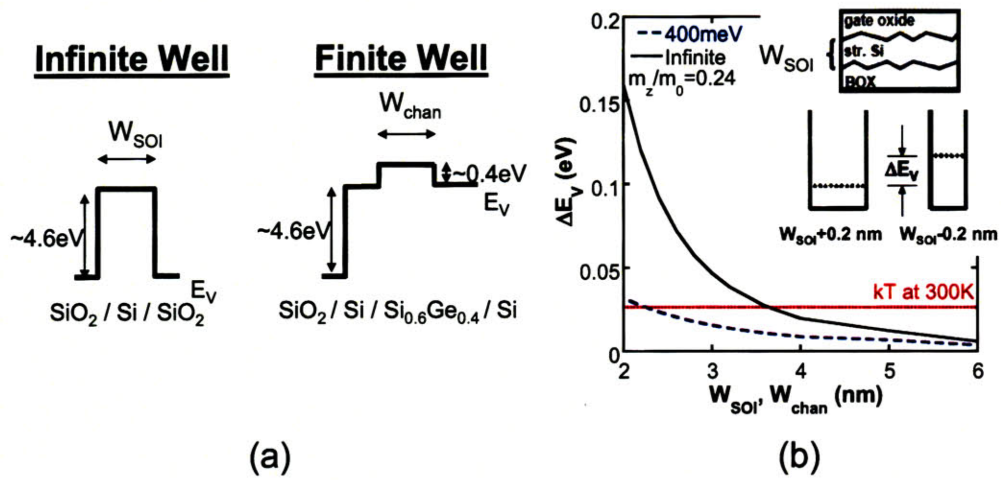


Figure 4-19: (a) Sketch of valence band structure for SOI and strained $Si_{0.57}Ge_{0.43}$ heterostructure system. (b) Fluctuation in ground state energy due to a thickness fluctuation of $\pm$ 0.2 nm for the finite and infinite square well described in (a).

the vertical electric field will not influence the carrier distribution significantly in a very narrow well. As discussed in Section 2.2.2 for ultra thin body SOI MOSFETs, mobility scales with body thickness to the power of 6. However, the ground state energy fluctuation in the SOI quantum well system is well modeled by an infinite quantum well. A schematic of the valence band structure for the SOI system and the $Si_{0.57}Ge_{0.43}$ heterostructure system is shown in Figure 4-19 (a). The ground state energy fluctuation in the SOI quantum well system is well modeled by an infinite quantum well due to the 4.6 eV band offset between the Si and the SiO_2. However, the valence band offset is on the order of 400 meV between the $Si_{0.57}Ge_{0.43}$ and Si in the case of the heterostructure. This is best modeled as a finite quantum, as the finite nature of the barrier allows penetration of the hole wavefunction outside the well. This leads to a significant reduction in the groundstate energy fluctuation with thickness variation, as the well appears wider ($\sim$1.3 nm for the $Si_{0.57}Ge_{0.43}$/ Si quantum well) compared to an infinite quantum well. The fluctuation in ground state energy due to a thickness fluctuation of $\pm$ 0.2 nm for the finite and infinite square well is plotted in Figure 4-19 (b). This demonstrates that the influence of thickness fluctuation scattering will be much lower for the $Si_{0.57}Ge_{0.43}$/Si heterostructure compared to the SOI system.

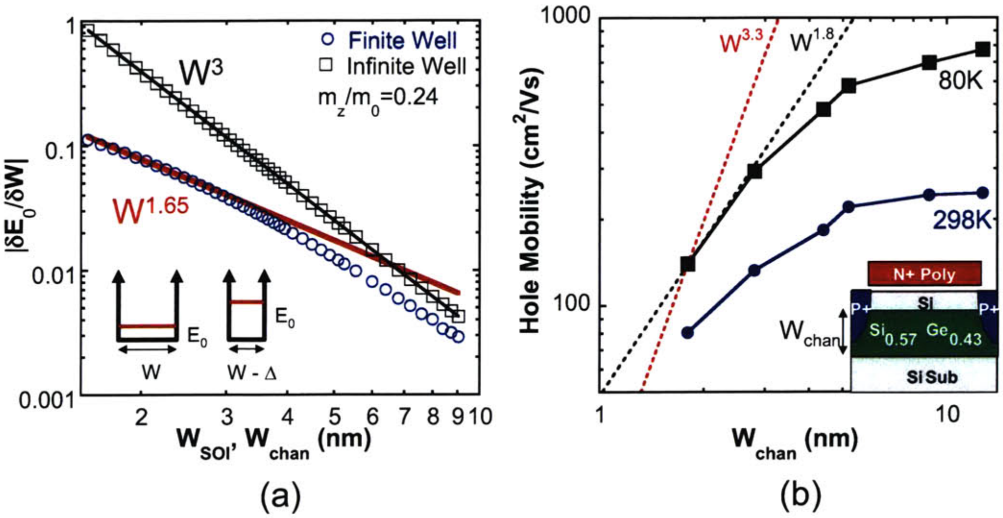


Figure 4-20: (a) Energy fluctuation with respect to channel width for finite and infinite quantum well described in Figure 4-19 (symbols) with a line fit of $W^{1.65}$ and W^3 for the finite and infinite well respectively. (b) Measured effective hole mobility as a function of $Si_{0.57}Ge_{0.43}$ W_{chan} at 298K and 80K. Lines represent a fit of $W^{1.8}$ and $W^{3.3}$

In order to determine the thickness dependence of thickness fluctuation in this finite quantum well, Equations 2.13 and 2.14 from Section 2.2.2 are utilized. The local energy fluctuation is given by

$$\delta E = \frac{\partial E_0}{\partial W}\Delta \tag{4.5}$$

where E_0 is the ground state energy of the quantum well. This leads to a thickness fluctuation limited mobility of

$$\mu_{TF} \propto \frac{1}{(\delta E)^2} \propto \frac{W^6}{\Delta^2} \tag{4.6}$$

$\partial E_0/\partial$W is plotted in Figure 4-20 (a) for the infinite and finite quantum well. As seen from Equation 2.13, the energy fluctuation in an infinite quantum well scales with W^3 which leads to a mobility dependence of W^6. The finite quantum well cannot be fit by a simple power dependence on W. Since thickness fluctuation scattering is only important for the thinnest films, a line was fit for film thicknesses between 1.8 and 2.8 nm, yielding a $W^{1.65}$ dependence. This suggests that mobility should

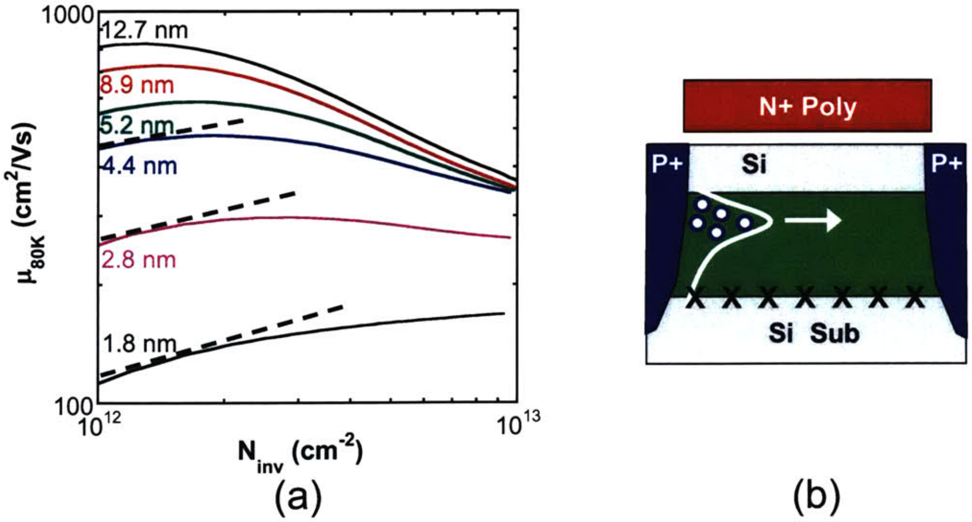


Figure 4-21: (a) Measured effective hole mobility at 80K and versus N_{inv} for W_{chan} from 1.8 nm to 12.7 nm. Dashed lines indicate coulombic scattering limited mobility, which increases with increasing N_{inv} due to screening. Scattering worse for thinner films. (b) Schematic of heterostructure indicating position of phosphorus spike. Carriers will be further away from the scattering potential for thicker films.

scale with $W^{3.3}$ for the thinnest $Si_{0.57}Ge_{0.43}$ channels. The low temperature mobility versus W_{chan} is plotted in Figure 4-20 (b). A line fit between the 1.8 and 2.8 nm-thick channels shows a $W^{1.8}$ dependence which is less than the $W^{3.3}$ expected for this finite quantum well structure. This suggests that the mobility degradation between 2.8 nm and 1.8 nm channels is not due to thickness fluctuation scattering. The 1.8 nm channel mobility may be degraded due thickness fluctuation scattering, but there is not sufficient mobility versus W_{chan} data around this thickness to determine that.

4.5.2.7 Coulombic Scattering

As discussed in Section 2.2.2 coulombic scattering is dominant at low N_{inv} but is screened at higher N_{inv}, leading to an increase in coulombic limited mobility with increasing N_{inv}. From the low temperature mobility measurement shown in Figure 4-21 (a) there is some indication of coulombic scattering in these structures, illustrated by the dashed line. This scattering is more significant for the thinner films suggesting that the scattering charge is at the bottom interface between the Si substrate and the strained SiGe channel. This is most likely due to a phosphorus doping spike at this interface, as illustrated in Figure 4-21 (b). For the thicker films the carriers are moved away from the bottom interface due to the band bending by the vertical electric field. However, as we saw in the analysis of interface scattering, for the thinnest films the vertical field has little influence on the hole distribution and the carriers are very close to both interfaces.

For the growth of the $Si_{0.57}Ge_{0.43}$ heterostructure a 2μm layer of epitaxial Si was grown on the n+ substrate. This epitaxial layer was doped in-situ with phosphorus to 10^{17} cm^{-3}. The doping gas, phosphine (PH_3), was turned off while a 20 nm i-Si layer was grown followed by the strained $Si_{0.57}Ge_{0.43}$ channel and the Si cap. Due to the change in growth temperature for the epitaxial Si substrate and the strained SiGe layer, dopant segregation to the interface can occur, resulting in a spike in the doping concentration at the Si substrate/SiGe interface [74]. While precautions were taken to avoid this by inserting the 20 nm undoped Si layer before the strained SiGe channel was grown, some dopant possibly segregated to the interface resulting in the coulombic scattering seen on these devices. This dopant spike can be avoided by careful fabrication and so is not a fundamental limit to the mobility of these structures.

4.5.2.8 N_{inv} Dependence of μ_{80K}

The dependence of interface roughness scattering on inversion charge density N_{inv} is a complex function of roughness parameters, confinement effects and screening of the perturbation with increasing N_{inv} [75] and is outside the scope of this work to analyze in detail. However, we can note the differences seen on the 43/0 structure compared to theoretical and experimental results for bulk and strained Si.

Experimental work on bulk Si devices by Takagi *et al.* [32] found an N_{inv} power dependence of -2.6 and -1.0 for electrons and holes respectively for surface roughness scattering. The smaller dependence for holes was thought to be due to the improved dielectric screening by heavier holes compared to electrons. Theoretical work by Fischetti *et al.* [73] found N_{inv} to scale to the power of -1.15 and -0.605 for surface roughness limited mobility for holes at 77K for relaxed and 1% biaxial compressive strained Si respectively. A reason for this difference between unstrained and strained Si is not given in the work. It is possibly due to the strain-induced band splitting which reduces the density of states and effectively moves the charge centroid of the carrier distribution further away from the interface, and hence further from the perturbation, compared to the bulk Si case at a given N_{inv}. However, illustrating the complexity of the N_{inv} dependence, the introduction of compressive strain causes the effective mass to decrease which should produce a stronger dependence of mobility on N_{inv}.

Table 4.2: N_{inv} dependence of interface scattering limited mobility, μ_{80K}, as illustrated in Figure 4-16 for 43/0 structure as a function of W_{chan}.

$W_{chan}(nm)$	N_{inv}^{τ}
12.7	-0.5
8.9	-0.5
5.2	-0.4
4.4	-0.25
2.8	-0.1
1.8	0.1

Understanding the N_{inv} dependence of the 43/0 structure is further complicated by the finite nature of the quantum well. As discussed for thickness fluctuation scattering, for the finite quantum well there is some penetration of the wavefunction into the barrier. This means that the carriers are closer to the interface for a given N_{inv} compared to the bulk Si case where the Si-SiO_2 interface is closer to an infinite quantum well with very negligible wavefunction penetration. The N_{inv} dependence for interface roughness scattering (illustrated in Figure 4-16) is shown as a function of channel thickness in Table 4.2. For the thicker films, where confinement is not influenced by W_{chan}, N_{inv} scales to the power of -0.5. This value compares well with the theoretical value predicted by Fischetti of -0.605 for 1% compressive strain. As stated earlier it is difficult to interpret the effects determining the N_{inv} dependence as the Si/SiGe interface roughness is expected to be quite different than the Si-SiO_2 interface. The N_{inv} dependence drops significantly for W_{chan} less than 5 nm due to the confinement effect of the channel thickness.

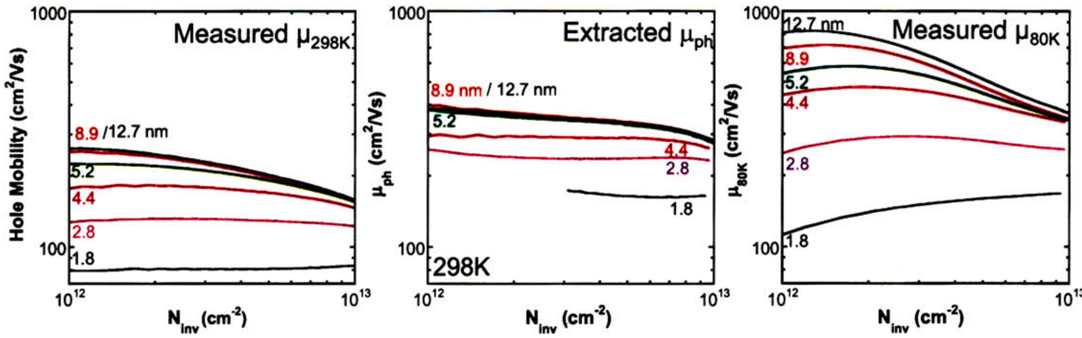


Figure 4-22: Summary of measured room temperature mobility, extracted phonon limited mobility and measured low temperature mobility at 80K as a function of N_{inv} for W_{chan} from 1.8 nm to 12.7 nm for the 43/0 structure. Same scale used on x and y axis.

4.5.2.9 Summary of Scattering versus W_{chan}

The mobility degradation versus W_{chan} has been analyzed in detail for the strained $Si_{0.57}Ge_{0.43}$/bulk Si heterostructure. The room temperature mobility, the phonon limited mobility and the low temperature mobility are all plotted on the same scale in Figure 4-22. It can be seen from these plots that the room temperature mobility decreases for W_{chan} below 5 nm due to a combination of phonon scattering and interface scattering. There is some indication of coulombic scattering at low N_{inv}, especially for the thinnest films, possibly due to phosphorus spiking at the Si substrate/SiGe interface. There may be thickness fluctuation scattering present for the 1.8 nm channel, but there is not enough data to confirm this.

4.6 Ge Channel pMOSFETs

As demonstrated in Section 4.3 the highest hole mobilities (over 10X enhancement relative to bulk Si) have been achieved with a strained Ge channel. In this section the strained Si/strained Ge/relaxed SiGe heterostructure pMOSFET is discussed. The impact of strained Ge channel thickness is investigated. A number of virtual substrates were investigated with Ge fractions varying from 0.3 to 0.6. The relaxed $Si_{0.7}Ge_{0.3}$ substrate is of particular interest due to the commercial availability of strained Si on insulator substrates with the same lattice parameter [76].

Table 4.3: Ge fraction in virtual substrate and Ge channel thickness for strained Ge channel pMOSFETs, extracted from XTEM.

Ge Fraction (x)	W_{chan} (nm)
0.3	4.8
0.4	6.8
0.5	4
0.5	8
0.5	16
0.6	9.5

4.6.1 Ge pMOSFET Heterostructure

The virtual substrate was formed as described in Section 3.2 and doped with phosphorus to 10^{17} cm^{-3}. The Ge channel was grown at 365°C. The Si cap was grown at 600°C. The SiH_4 was turned on in an effort to stabilize the Ge surface during the temperature ramp from 365°C to 600°C, with a pause for 5 minutes at 450°C and 525°C. A 6 nm Si cap was grown leaving ~3.5 nm-thick cap after MOSFET processing. A summary of the Ge channel thickness and virtual substrate composition for the devices discussed in this section are shown in Table 4.3.

In an effort to minimize Si-Ge inter-diffusion during processing the thermal budget was kept to a minimum. The gate oxide (11 nm) was deposited in a low pressure chemical vapor deposition (LPCVD) system at 400°C. The source/drain dopant activation anneal was performed at 650°C for 10 seconds in a RTP system.

4.6.2 Mobility for Ge Channel pMOSFETs

The hole mobility and mobility enhancement relative to the Si control is shown in Figure 4-23 (a) and (b) respectively for a $Si_{0.5}Ge_{0.5}$ virtual substrate with channel thickness varying between 4 nm and 16 nm. The highest mobility is found for the 8 nm-thick Ge channel with enhancement greater than 10X over the Si control device. The drop in mobility for the 16 nm-thick channel is believed to be due to relaxation of the channel, as 16 nm is well above the equilibrium critical thickness of 5 nm for a film with this level of strain. There is a very large drop in mobility for the 4 nm film compared to the 8 nm channel. Even though the thermal budget was kept as low as possible in order to minimize Si-Ge inter-diffusion, there is evidence from EELS analysis that there is some diffusion of Si into the Ge layer for the 4 nm-thick film. A XTEM of the 4 nm and 8 nm Ge channel and the EELS spectra for Si is shown in Figure 4-24 (a) - (d).

The EELS Si signal for the 8 nm film is effectively zero suggesting the film is close to pure Ge. This is further confirmed by energy dispersive spectroscopy (EDS) results shown in Figure 4-24 (d). The EELS spectra for Si shows that there is some Si in the Ge film for the thinnest film. Therefore, some of the mobility drop is due to the decrease in Ge concentration for the 4 nm film. The local interface compositional profile (EDS and EELS) is a convolution of the actual compositional profile, electron beam size, probe broadening due to the sample thickness, electron beam-specimen interaction volume (EDS signal originates from a larger area than the EELS signal) and other effects (e.g. data acquisition and processing conditions, and instrumental and environmental stability). Thus, it is difficult to use the EELS and EDS data quantitatively. Based on the mobility data from Section 4.3 the channel Ge concen-

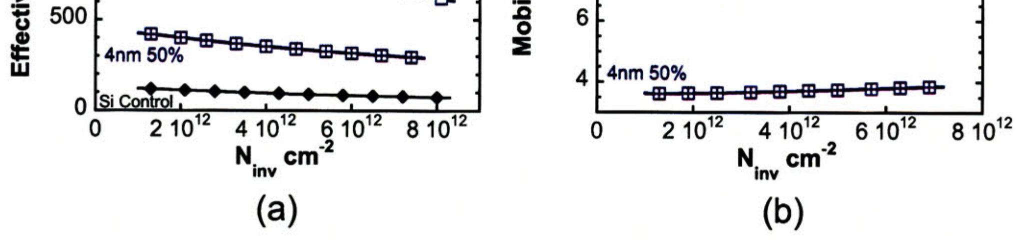


Figure 4-23: (a)Effective hole mobility and (b) mobility enhancement relative to a Si control as a function of inversion charge density, N_{inv}, for strained Si/strained Ge/relaxed $Si_{0.5}Ge_{0.5}$ structures, extracted on 50 μm x 50 μm devices using the split C-V technique. W_{chan} of 4 nm, 8 nm and 16 nm determined by XTEM.

tration would need to drop to 70 at. % in order to account for the observed loss in mobility enhancement compared to the 8 nm film. Comparing the Ge channel XTEM in Figure 4-24 to the strained $Si_{0.57}Ge_{0.43}$ channel XTEM in Figure 4-8, the Ge channel interface to the Si cap looks significantly rougher. Further evidence to support increased roughness compared to the strained $Si_{0.57}Ge_{0.43}$ on bulk Si structure can be seen in the Atomic Force Microscopy, AFM, data in Figure 4-25.

This AFM data was obtained from unprocessed heterostructure substrates similar to those used for the pMOSFET analysis in this thesis. There is a peak-to-valley roughness of ~1 nm for the strained Si/strained Ge/ relaxed $Si_{0.5}Ge_{0.5}$ substrate (Figure 4-25 (a)) while the peak-to-valley roughness is significantly smaller at ~0.45 nm for the relaxed Si/ strained $Si_{0.6}Ge_{0.4}$/ bulk Si substrate (Figure 4-25 (b)). This suggests that part of the drop in mobility is due to the large roughness at the Ge/strained

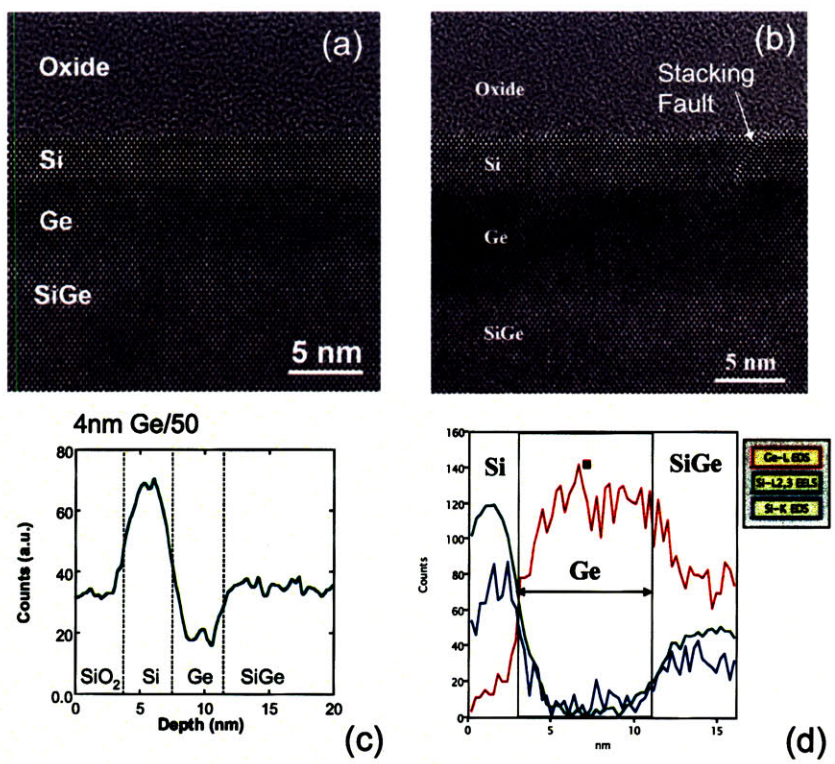
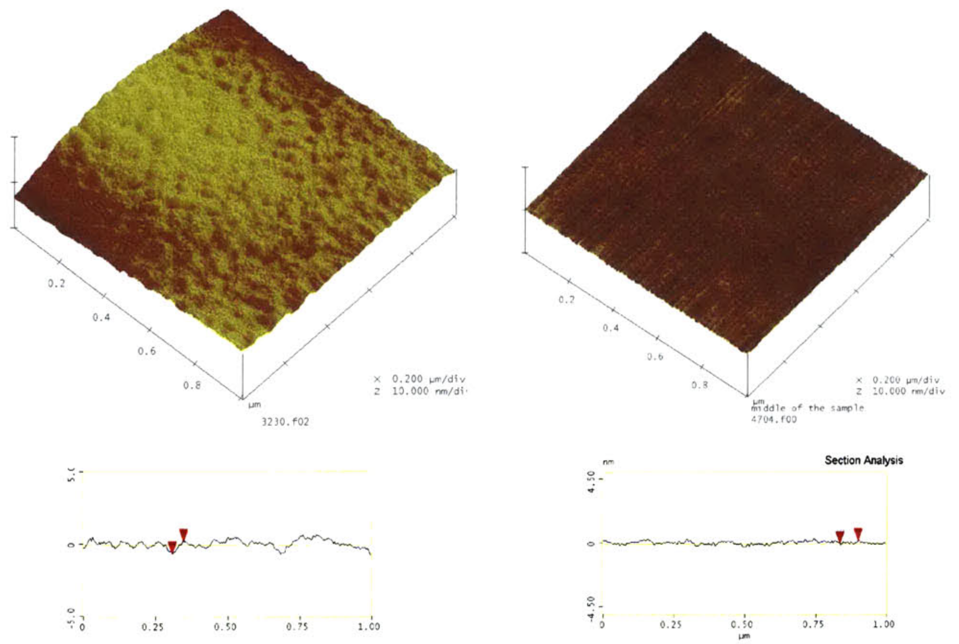


Figure 4-24: XTEM for (a) 4 nm and (b) 8 nm Ge channel on $Si_{0.5}Ge_{0.5}$ virtual substrate. EELS spectra for the (c) 4 nm and (d) 8 nm Ge channel indicate significant Si-Ge interdiffusion for the 4 nm channel. EDS signal for Si and Ge also shown for 8 nm channel XTEM, EELS and EDS courtesy of Prof. M. Kim, UT Dallas.



(a) (b)

Figure 4-25: AFM for unprocessed epitaxial layers: (a) 5 nm strained Si/ 8 nm strained Ge / relaxed $Si_{0.5}Ge_{0.5}$ and (b) 4.5 nm relaxed Si/ 5 nm strained $Si_{0.6}Ge_{0.4}$/ bulk Si. AFM courtesy of M. K. Kim.

Si interface.

It has been suggested that the decrease in mobility with channel thickness for Ge channel pMOSFETs may be associated with loss of carriers from the quantum well due to wavefunction penetration into the barrier layer due to the small effective hole mass for pure Ge [5]. 1-D Schrödinger-Poisson simulation of the hole density distribution at N_{inv} of 7x10^{12} cm^{-2} for the Ge on $Si_{0.5}Ge_{0.5}$ heterostructure is shown in Figure 4-26 (a). There is excellent hole confinement for both the 8 nm and 4 nm-thick Ge channel. In fact over 95% of the carriers are confined to the Ge layer for the 4 nm Ge channel, Figure 4-26 (a). The reason for the excellent carrier confinement in the Ge channels is the very large valence band offset between the Ge and the Si/SiGe layers (640 meV and 530 meV for the Ge/Si and Ge/$Si_{0.5}Ge_{0.5}$ layers). The band edge quantization mass (HH mass in the $\langle 001 \rangle$ direction) is relatively large at $0.2m_0$ compared to $0.24m_0$ for compressively strained $Si_{0.6}Ge_{0.4}$ (obtained from 6x6

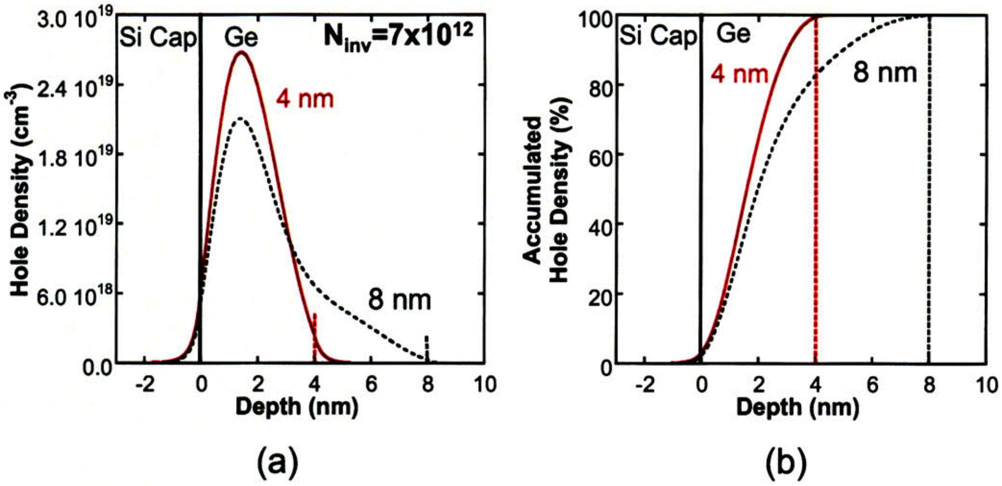


Figure 4-26: Hole density distribution in strained Ge channel on $Si_{0.5}Ge_{0.5}$ for W_{chan} of 4 nm and 8 nm from 1-D Schrödinger-Poisson simulation done in $nextnano^3$ for N_{inv} of $7x10^{12}$ cm^{-2} (b) The % accumulated hole density (integral of hole distribution over depth) for 4 and 8 nm channels plotted in (a). Dotted line on x-axis indicates the bottom Ge/ $Si_{0.5}Ge_{0.5}$ interface.

k.p simulations). From the simulation results, the mobility drop in the 4 nm channel does not appear to be due to wavefunction penetration.

It is interesting to note that there are some stacking faults appearing in the Si cap for the Ge/50 structures, indicated in Figure 4-24 (b). However, the stacking fault does not extend into the Ge channel. The very high mobility on the 8 nm structure (comparable to best published data) suggests that the stacking faults are not affecting long channel mobility. It does indicate that the Si cap may be starting to relax due to the high level of strain from the $Si_{0.5}Ge_{0.5}$ virtual substrate.

Further evidence of the onset of relaxation in the Si cap can be seen in the mobility of the Ge on $Si_{0.4}Ge_{0.6}$ structure shown in Figure 4-27 (a), where there is a 30% drop in mobility compared to the 8 nm Ge on $Si_{0.5}Ge_{0.5}$ structure. The XTEM in Figure 4-27 (b) shows that there is some mismatch between the $\langle 111 \rangle$ planes in the Ge channel and Si cap layer (~1.4 degrees) suggesting some relaxation has taken place. This mismatch is not seen in the Ge on $Si_{0.5}Ge_{0.5}$ structure.

The hole mobilities for the Ge channel on $Si_{1-x}Ge_x$ ($0.3 \leq x \leq 0.5$) virtual substrate structures are plotted in Figure 4-28 (a). The mobility enhancement plotted

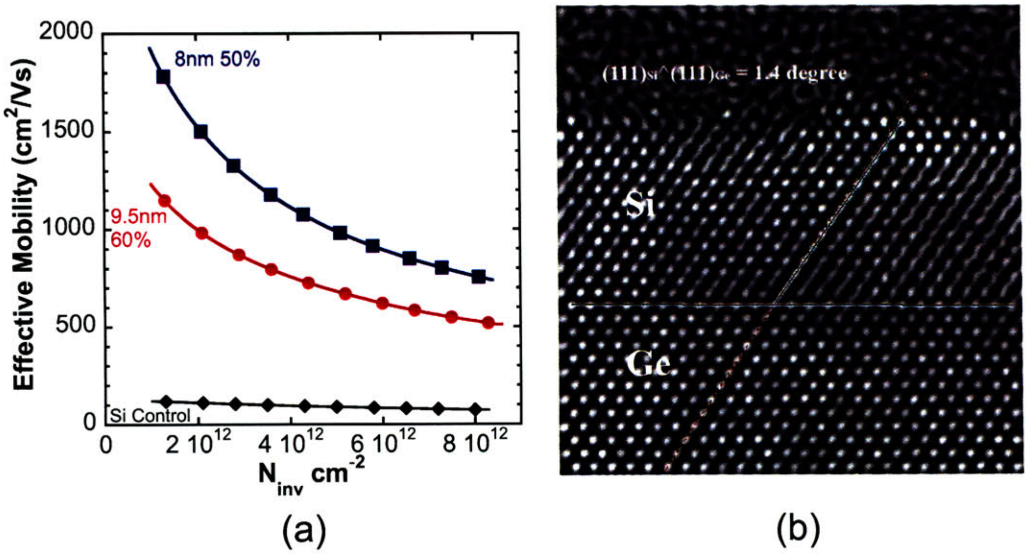


Figure 4-27: (a) Effective hole mobility as a function of inversion charge density, N_{inv}, for 8 nm strained Ge on relaxed $Si_{0.5}Ge_{0.5}$ and 9.5 nm strained Ge on relaxed $Si_{0.4}Ge_{0.6}$. (b) XTEM showing mismatch of 1.4 degrees in orientation of the $\langle 111 \rangle$ plane between the strained Ge and strained Si cap for the $Si_{0.4}Ge_{0.6}$ virtual substrate structure.

in Figure 4-28 (b) shows a large drop in mobility for Ge channels below 6 nm. This is in contrast to the $Si_{0.57}Ge_{0.43}$ on Si structure discussed in Section 4.5.2 where the mobility started to degrade for channels below 4 nm. Based on the results in Section 4.4 the level of strain (and hence the Ge composition of the virtual substrate) is not expected to have a large impact on the mobility for structures investigated in this study.

The XTEM and the scanning transmission electron microscopy (STEM) high angle annular dark field (HAADF)image for the 4.8 nm Ge on $Si_{0.7}Ge_{0.3}$ (Figure 4-29) shows very clear contrast between the Ge and the Si cap layer. The STEM-HAADF images are formed predominantly from electrons scattered to high angles by interactions close to the atom core. The scattering intensity is approximately proportional to the square of the atomic number (Z). Therefore the contrast is related directly to the atomic number and the total amount of that material through which the beam has passed. These images further emphasize the large surface roughness on the Ge channel pMOSFETs.

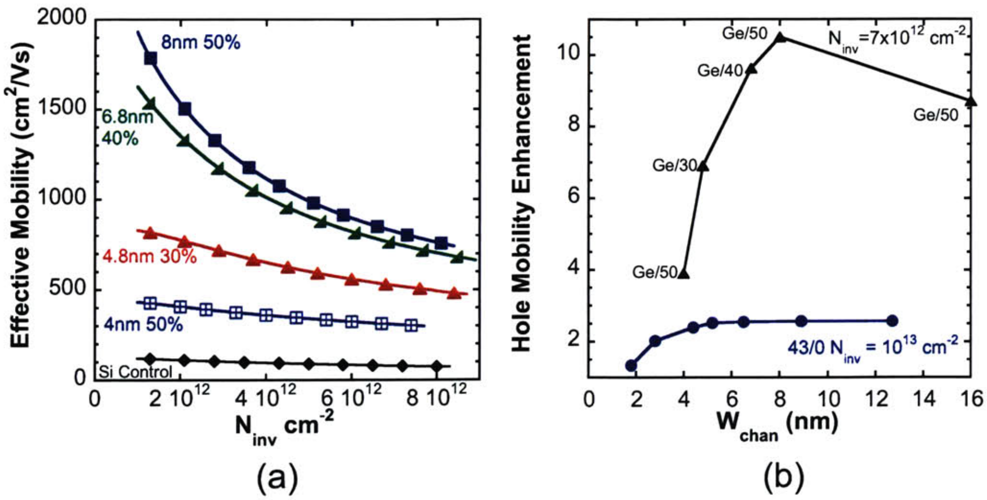


Figure 4-28: (a) Effective hole mobility as a function of inversion charge density, N_{inv}, for strained Ge (W_{chan} = 4 nm - 8 nm) on relaxed $Si_{1-x}Ge_x$ (x=0.3 to 0.5). (b) Mobility enhancement over Si control as a function of channel thickness for strained Ge channel (triangles) and strained $Si_{0.57}Ge_{0.43}$ channels (circles).

4.6.3 Ge Channel Summary

Ge channel pMOSFETs fabricated in this study have produced a 10X mobility enhancement over a Si control and are comparable to the best published data on strained Ge channels. The mobility decreases dramatically for Ge channel thickness below 6 nm due to a combination of Si-Ge inter-diffusion and the relatively large interface roughness on these structures. Si-Ge inter-diffusion is a possible limiting factor in achieving maximum mobility enhancement in thin Ge channels. The thermal budget in this study is extremely low compared to a conventional CMOS process, yet there is evidence from EELS that there is some Si present in the thinnest Ge channels. Mobility degradation due to interface roughness can be improved considerably through epitaxial growth optimization for the Ge channel and Si cap layer. Capping of Ge with Si at 350°C using Si_3H_8 has been demonstrated in the literature [77], resulting in significant reduction of Ge related electronic defects at the oxide/Si interface compared to Si deposited at 500°C

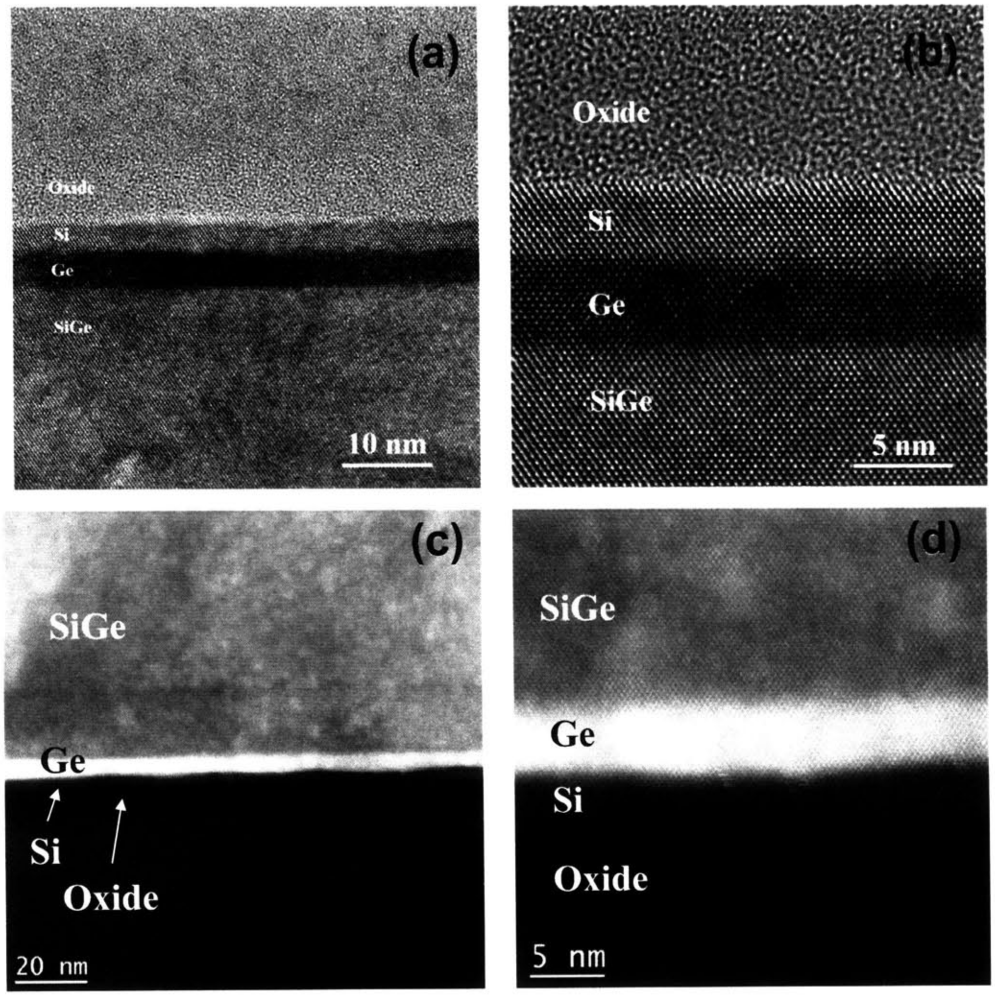


Figure 4-29: (a), (b) XTEM and (c), (d) scanning transmission electron microscopy (STEM) high angle annular dark field (HAADF) for 4.8 nm Ge channel on $Si_{0.7}Ge_{0.3}$. Courtesy of Prof. M. Kim,UT Dallas.

4.7 Strained $Si_{0.3}Ge_{0.7}$ on bulk Si pMOSFETs

In Section 4.5.2 we saw that hole mobility enhancements of 2.5X over a bulk Si channel are achievable with a strained $Si_{0.57}Ge_{0.43}$ channel grown pseudomorphically on a bulk Si substrate. In order to look at higher mobility pseudomorphic structures, in this section, $Si_{0.3}Ge_{0.7}$ channels grown on bulk Si substrates will be analyzed.

4.7.1 Fabrication and Metrology

Fabrication process and thermal budget for these structures is the same as used for the $Si_{0.57}Ge_{0.43}$ structures with the exception of the epitaxial growth temperature for the strained $Si_{0.3}Ge_{0.7}$ channel, which was grown at 450°C compared to 525°C for the strained $Si_{0.57}Ge_{0.43}$. The SD anneal was carried out at 800°C for 10 seconds in an RTP system, except for one of the structures shown which received laser spike annealing at 850°C for 800μseconds (see Chapter 6 for further details on laser annealing).

Table 4.4: $Si_{0.3}Ge_{0.7}$ channel thickness and composition from HR-RBS courtesy of Kobe Steel. All wafers received SD anneal at 800°C for 10 seconds except for wafer 17 which received a laser spike anneal at 850°C for 800μsecs

Sample ID	Ge Fraction	W_{chan} (nm)
8	0.43	1.7
9	0.52	3.2
10	0.57	5.2
11	0.63	6.7
12	0.70	8.8
13	0.74	11.3
17	0.70	6.6

HR-RBS was used to extract the Ge composition and the results are given in Table 4.4. W_{chan} was obtained by fitting the RBS spectra to simulation using the SiGe atomic density. The Ge fraction in the strained SiGe channel decreases with decreasing thickness. This is most likely due to Si-Ge inter-diffusion. Si-Ge diffusivity increases exponentially with strain and Ge composition [86]. The thermal budget of 800°C for 10 seconds was sufficiently low for the $Si_{0.57}Ge_{0.43}$ on Si heterostructure to maintain the peak Ge concentration, even for the 2.8 nm channel. The increase in strain and Ge fraction for the $Si_{0.3}Ge_{0.7}$ on Si heterostructure results in a drop in Ge composition with film thickness for these processing conditions. This is further confirmed by comparing sample 11 and 17, where the Ge fraction dropped from 0.7 to 0.63. These two wafers had the same starting substrate and processing, and only varied at the SD anneal stage, with wafer 17 receiving the laser spike anneal. This result demonstrates the difficulty in maintaining the peak Ge concentration in thin, high Ge concentration SiGe channels, even with a relatively low thermal budget of 800°C for 10 seconds.

This set of structures is not suitable for analyzing the impact of W_{chan} for high Ge composition channels as the Ge fraction varies significantly with film thickness. However, the devices do give an interesting range of Ge compositions to examine the impact of Ge fraction on mobility for the pseudomorphic structure.

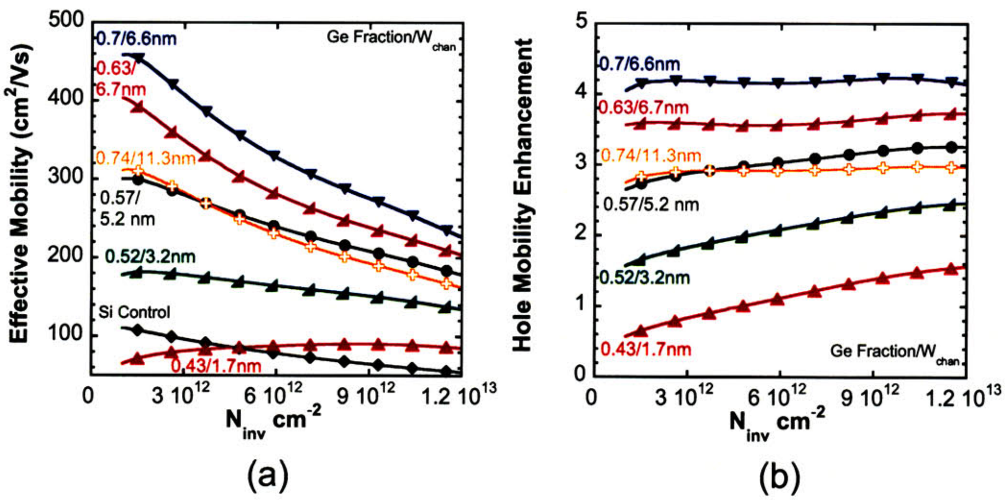


Figure 4-30: Mobility (a) and mobility enhancement (b) for $Si_{0.3}Ge_{0.7}$ channels grown pseudomorphically on bulk Si. The peak Ge fraction and W_{chan} are noted for each structure.

4.7.2 Mobility for $Si_{1-y}Ge_y$ on Bulk Si

The hole mobility and mobility enhancement over the Si control is shown in Figure 4-30 (a) and (b) respectively for the devices listed in Table 4.4. Mobility increases monotonically with increasing Ge fraction in the strained SiGe channel with a peak enhancement of over 4X, except for the 11.3 nm $Si_{0.26}Ge_{0.74}$ channel. The drop in mobility for this structure is most likely due to relaxation of the channel as the equilibrium critical thickness for $Si_{0.26}Ge_{0.74}$ is less than 4 nm. The mobility enhancements are similar to enhancements obtained for strained SiGe channels on virtual substrates explored in Section 4.3. For example, enhancements of 3X and 4X obtained for the strained $Si_{0.43}Ge_{0.57}$ and $Si_{0.3}Ge_{0.7}$ channels respectively are in excellent agreement with the results plotted in Figure 4-3 for the 58/30 and 70/40 and structures. It is also worth noting that the mobility for the 1.7 nm $Si_{0.57}Ge_{0.43}$ channel is very similar to the 1.8 nm strained $Si_{0.6}Ge_{0.4}$ channel evaluated in Section 4.5.2.

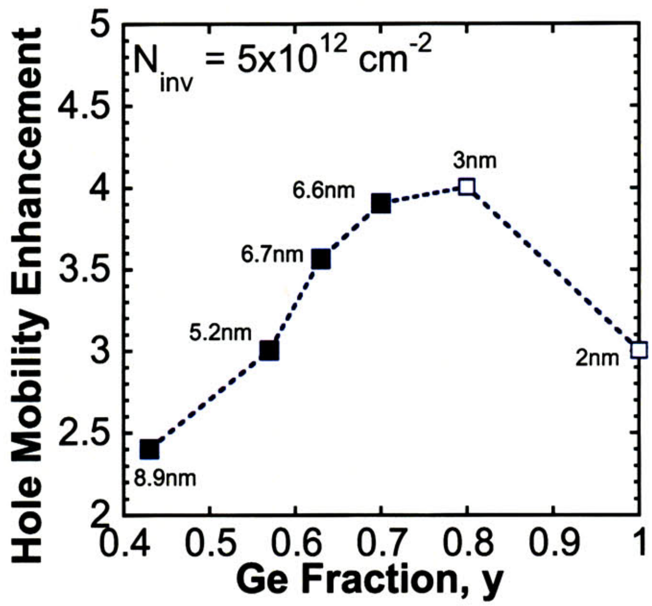


Figure 4-31: Mobility enhancement versus Ge fraction for strained SiGe channels grown pseudomorphically on bulk Si. Strained SiGe channel thickness noted for each point. Closed symbols represent experimental data from this work. Open symbols represent experimental data from Krishnamohan et al. for strained SiGe channels grown on SOI substrates [65].

The hole mobility enhancement for strained SiGe channels grown pseudomorphically on bulk Si is shown in Figure 4-31. The solid symbols represent the results from this work. Mobility enhancements from 2.5X up to 4X are achievable for the pseudomorphic structure by varying the Ge fraction in the strained SiGe layer from 0.4 to 0.7. The open symbols represent the best published results for high Ge composition strained SiGe layers grown on relaxed Si SOI by Krishnamohan *et al.* [65]. The mobility enhancements of 4X and 3X are achieved for a 3 nm $Si_{0.2}Ge_{0.8}$ and 2 nm Ge channel respectively. This figure shows there is a break even point in Ge composition at $Si_{0.3}Ge_{0.7}$: increasing the Ge composition above this value dues not bring increased mobility enhancement, as the channel thickness is limited due to critical thickness constraints. Mobility enhancements of 6X are expected for a strained

$Si_{0.2}Ge_{0.8}$ channel without critical thickness constraints. There is possibly some room for improvement in mobility for $Si_{0.2}Ge_{0.8}$ channels. The equilibrium critical thickness is 3 nm. With an optimum SiGe and Si growth process it should be possible to obtain a 4 - 5 nm-thick channel without relaxation. There should be minimal mobility degradation due to channel thickness at high N_{inv} for a 4 - 5 nm channel, so the break even point is possibly around 80% Ge. However, as we have seen for the Ge composition versus channel thickness observed in this experiment (Table 4.4), the thermal budget will have a large influence on the final Ge composition of the channel. Therefore, the thermal budget combined with the critical thickness will determine the peak mobility enhancement achievable for strained SiGe channels pseudomorphically strained to bulk Si.

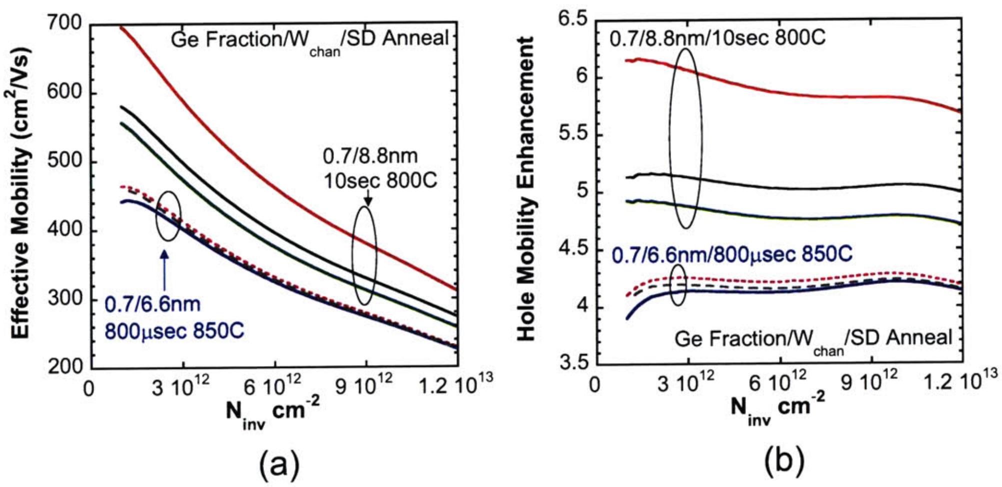


Figure 4-32: Mobility (a) and mobility enhancement (b) for 8.8 nm and 6.6 nm strained $Si_{0.3}Ge_{0.7}$ channels. The three curves are from 3 different devices from the same 1 cm^2 region of the wafer.

4.7.3 Anomalous Mobility for 8.8 nm $Si_{0.3}Ge_{0.7}$ Channel

The hole mobility and mobility enhancement relative to the Si control is shown in Figure 4-32 (a) and (b) for the 8.8 nm and 6.6 nm $Si_{0.3}Ge_{0.7}$ channel structures respectively. Three devices from within the same 1 cm^2 area on the wafer are plotted for each structure. There are two significant differences between the mobilities on

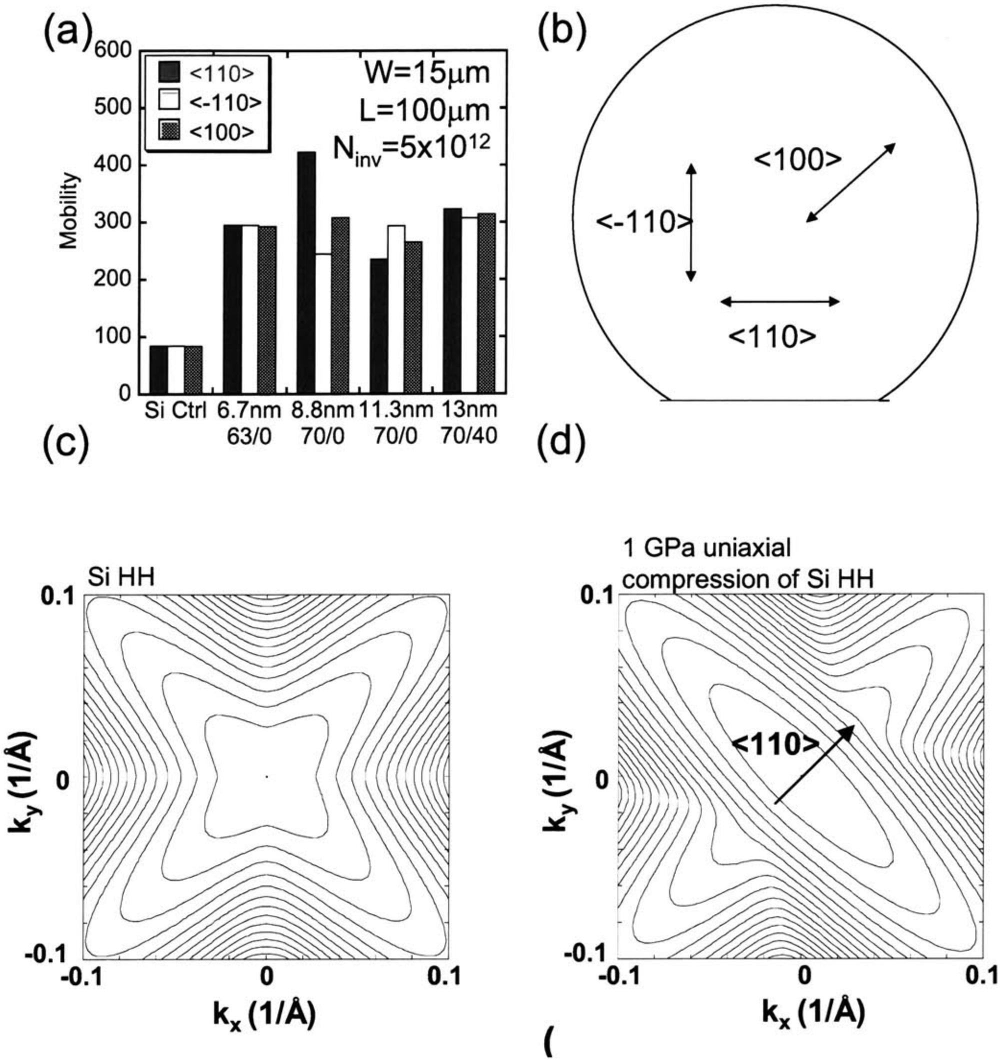


Figure 4-33: (a) Hole mobility for strained $Si_{0.3}Ge_{0.7}$ vs. channel orientation. Metastable films (8.8 nm) are known to relax uniaxially in $\langle 110 \rangle$ direction due to damage (most likely SD implant) and subsequent heat treatment [78]. Orientation dependence of mobility not seen on other structures. (b) Channel orientation for mobility results in (a). (c) HH band for unstrained and (d) uniaxial compressive strain in the $\langle 110 \rangle$ direction from nextnano^3 simulations. Valence band structure courtesy of I. Åberg [79].

these structures. Firstly, the mobility for the 8.8 nm channel is significantly higher than the 6.6 nm structure. In fact, a 6X enhancement is achieved for the devices, which is 50% greater than mobility enhancement seen for strained $Si_{0.3}Ge_{0.7}$ channels on bulk Si or virtual substrates examined in this work. There is also a very large variation in the mobility for the 8.8 nm channel compared to the 6.6 nm channel

(20% compared to 2% at 5x10^{12} cm^{-2} N_{inv}).

The orientation dependence of mobility for the two structures is shown in Figure 4-33 (a). The channel direction on the wafer is shown in Figure 4-33 (b). The different orientations are measured on adjacent devices in order to minimize the effect of mobility variation with position for the 8.8 nm channel. There is effectively no variation in mobility with orientation for the 6.6 nm channel, as expected for a biaxial strained material. The 8.8 nm channel shows a very large orientation dependance on mobility. This suggests that the 8.8 nm strained SiGe channel is no longer biaxially strained. The fact that the mobility is highest in the $\langle 110 \rangle$ direction and lowest in the $\langle -110 \rangle$ direction, with the mobility in the $\langle 100 \rangle$ direction somewhere in between, suggests that the channel has partially relaxed leaving the uniaxial compressive strain in the $\langle 110 \rangle$ direction. This is analogous to the process induced uniaxial compressive strain for bulk Si channels which causes deformation of the HH band, reducing the effective mass in the $\langle 110 \rangle$ direction and increasing it in the $\langle -110 \rangle$ direction. Figure 4-33 (c) and (d) illustrates the impact of uniaxial compressive strain on the bulk Si HH band.

The origin of the asymmetric strain relaxation in these samples is not clear, especially for such large devices (W x L = 15 μm x 100 μm). One possible mechanism for the uniaxial relaxation may be associated with the SD implant. Work by Noble *et al.* [78] on metastable SiGe films has shown that dislocations will form in the $\langle 110 \rangle$ direction perpendicular to a surface scratch with subsequent thermal processing. The scratch acts to reduce any activation energy barrier to misfit dislocation nucleation for the relaxation of the metastable film. Interestingly, the dislocations only occur in the $\langle 110 \rangle$ direction. The 8.8 nm $Si_{0.3}Ge_{0.7}$ film is well above the equilibrium critical thickness of 3.5 nm. The SD implant may act as the nucleation site for dislocations that grow during the SD anneal. Dislocations in the $\langle 110 \rangle$ direction would cause the compressive strain to be relaxed in the $\langle -110 \rangle$ direction, leaving uniaxial compressive strain in the $\langle 110 \rangle$ direction.

The exact mechanism at work for the very high mobility seen on the 8.8 nm structure is not well understood, however it suggests that hole mobilities on uniaxial compressive strain SiGe channels can exceed mobilities obtained on biaxial strained

SiGe channels.

4.7.4 Summary of Strained $Si_{1-y}Ge_y$ Channel Heterostructures

Hole mobility enhancements of up to 4X have been demonstrated for strained $Si_{0.3}Ge_{0.7}$ channels grown pseudomorphically on bulk Si substrates, comparable to the best mobility enhancements obtained in this work for strained $Si_{0.3}Ge_{0.7}$ channels grown on virtual substrates. Due to the high level of strain these channels are critical thickness limited (3.5 nm). The high Ge composition and strain for these channels leads to a high level of Si-Ge inter-diffusion, even for relatively low thermal budgets. This makes it difficult to maintain the peak Ge concentration for thinner channels, resulting in a drop in mobility. The idea of a Ge composition mobility breakeven point was introduced for the pseudomorphic structure, where increasing the Ge concentration beyond a certain point no longer leads to an increase in mobility, due to channel-thickness-related mobility degradation imposed by the critical thickness constraint. An anomalous mobility enhancement of 6X relative to Si control MOSFETs suggests the possibility of increasing the mobility on these structures by careful engineering of uniaxial strain.

4.8 Chapter Summary

In this chapter, the mobility for the SiGe channel heterostructure has been examined in detail. The Ge composition in both the strained and relaxed layer was varied over a wide range in order to map the mobility design space for these structures. A comprehensive analysis of the impact of film thickness on mobility, essential to understanding the mobility - critical thickness trade-off, was carried out.

It was shown that the Si cap thickness must be kept at a minimum in order to maximize mobility at high N_{inv}, and prevent carrier inversion in the low mobility Si cap. Mobility enhancements of 2X up to 10X were demonstrated for strained

SiGe channels grown on a virtual substrate. Enhancements of 2.5X up to 4X were demonstrated for strained SiGe channels grown on a bulk Si substrate. The high strain, high Ge composition and thin channels due to critical thickness constraints for the pseudomorphic structure make it particularly sensitive to the thermal budget, which will limit the peak mobility achievable for this structure.

For the strained $Si_{0.57}Ge_{0.43}$ on bulk Si heterostructure, the mobility was shown to degrade significantly for channel thickness below 4 nm due to a combination of phonon and interface scattering. The mobility was found to drop for thicknesses below 6-7 nm for strained Ge channels, due to a combination of increased interface roughness scattering and Si-Ge inter-diffusion.

Chapter 5

Subthreshold and Leakage Characteristics of Compressively Strained SiGe Heterostructure pMOSFETs

As was shown in the previous chapter, very high hole mobilities can be obtained with SiGe heterostructures. This high mobility comes at a price. The band gap of SiGe decreases with increasing Ge fraction leading to increased leakage. The Si cap can also degrade the subthreshold characteristics.

In this chapter, the leakage and subthreshold characteristics for the strained SiGe heterostructure will be studied for a wide range of Ge compositions, strain and film thickness.

5.1 Subthreshold Swing

If was shown in Section 4.2 that mobility will degrade at high N_{inv} due to inversion of carriers in the low mobility Si cap. A Si capping layer is required on top of the strained SiGe channel in order to make a high quality, low electronic defect interface with the gate dielectric. The sub-threshold swing for the SiGe heterostructure for a wide range

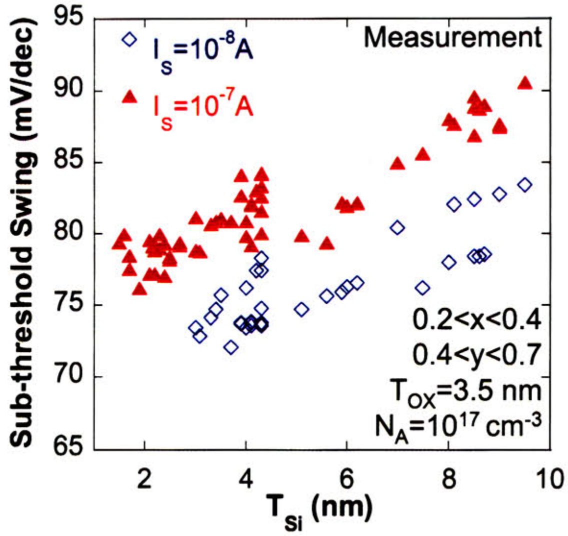


Figure 5-1: Sub-threshold swing (SS) for Ge range 0.2<x<0.4, 0.4<y<0.7, taken at two different source/drain currents (I_S). SS decreases with Si cap thickness, T_{Si}. Data from ring type pMOSFET, W=1000 μm, L=50μm.

of Ge fractions in the strained and relaxed layer (y, x) is plotted in Figure 5-1. Sub-threshold swing is relatively independent of Ge fraction, but increases with Si cap thickness. While the carriers are confined in the strained SiGe channel, as is the case below threshold, the Si cap acts as a parasitic dielectric in series with the gate dielectric, leading to an effective gate capacitance of

$$C_{GateEff} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_{Si}}} \tag{5.1}$$

and reduced gate control of the channel. This will also increase the DIBL for short channel structures. Therefore, the Si cap thickness must be minimized without compromising the integrity of the gate oxide interface. Fortunately, this is the same conclusion reached for the impact of the Si cap thickness on mobility.

5.2 Leakage in Heterostructure pMOSFETs

The bandgap of strained Si and SiGe can be significantly smaller than bulk Si, especially at the high Ge fractions investigated in this work. Off-state leakage (V_G =

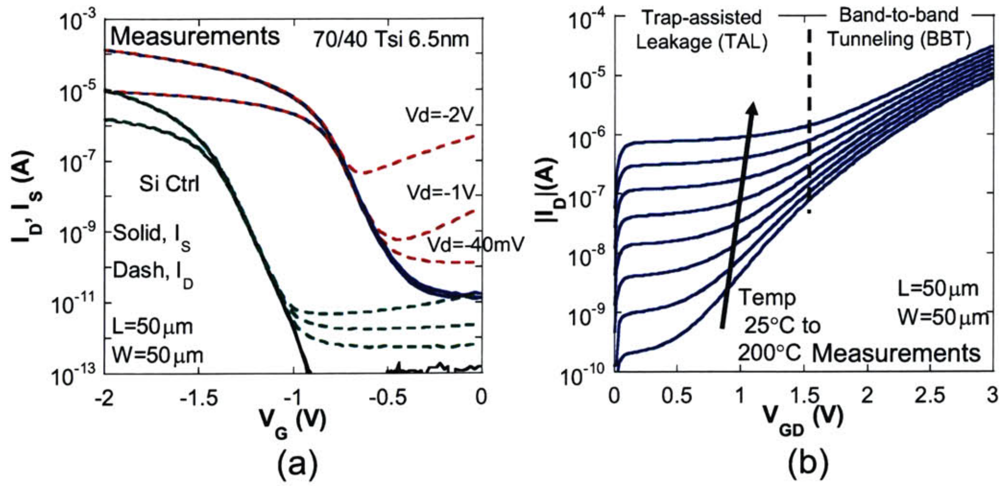


Figure 5-2: (a) Sub-threshold characteristics for 6.5 nm strained Si/ 12 nm strained $Si_{0.3}Ge_{0.7}$ / strained Si/ relaxed $Si_{0.6}Ge_{0.4}$ structure. The gate oxide thickness is 3.5 nm. Off-state leakage (I_D at $V_G = 0$V) increases with increasing drain bias. (b) Temperature characteristics of off-state leakage for 25°C to 200°C in steps of 25°C. The gate is held at 0 volts and the drain is ramped from 0 to -3V. The off-state leakage scales with W, the width of the device, indicating the leakage occurs at the SD/gate overlap.

0V) due to band-to-band tunneling (BBT) is higher in heterostructure MOSFETs due to the smaller bandgap in the strained Si and strained $Si_{1-y}Ge_y$ channel. This leakage can be seen in the sub-threshold characteristics of the 70/40 device shown in Figure 5-2 (a). The off-state leakage due to BBT is dependant on the electric field in the gate-to-drain overlap region and the bandgap in the high field region. The leakage scales with the device width, i.e. the length of the gate-to-drain overlap region, and not with the drain area. Increasing the drain bias causes an increase in the electric field in the drain-to-gate overlap region, which increases the off-state leakage. The temperature dependence of the leakage is shown in Figure 5-2 (b). At low drain bias the leakage is dependent on temperature with very little drain bias or electric field dependence, suggesting that the leakage is dominated by trap assisted leakage [49]. The leakage at high drain bias has a small temperature dependence and a large electric field dependence consistent with a BBT leakage mechanism. For reference, the subthreshold characteristics are shown for the 57/0 structure and the Ge/40 structure in Figures 5-3 and 5-4 respectively.

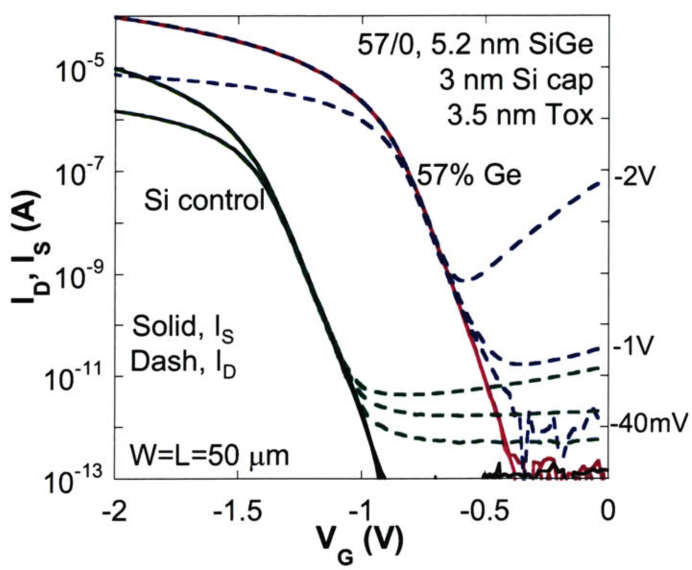


Figure 5-3: Sub-threshold characteristics for 3 nm Si cap / 5.2 nm strained $Si_{0.3}Ge_{0.7}$ / bulk Si structure. Off-state leakage (I_D at V_G = 0V) increases with increasing drain bias. The off-state leakage scales with W, the width of the device, indicating the leakage occurs at the SD/gate overlap region.

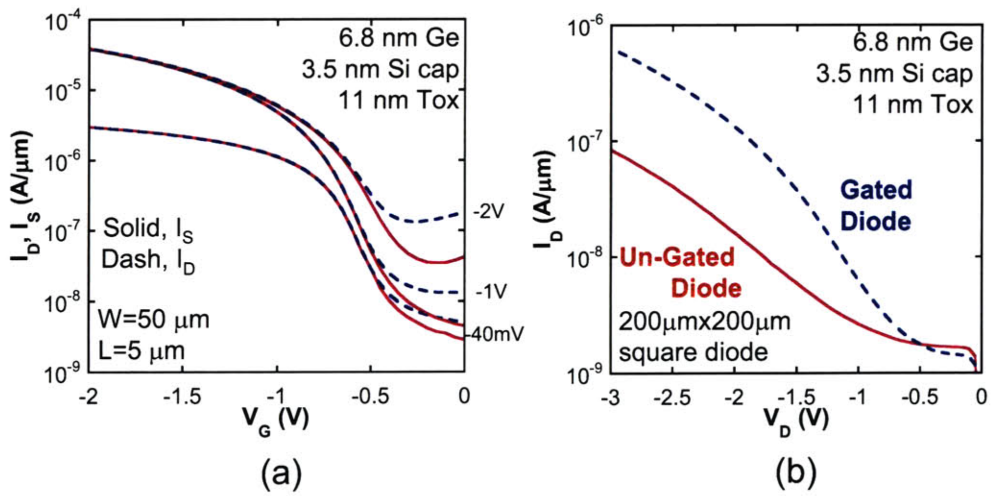


Figure 5-4: (a) Sub-threshold characteristics for 3.5 nm strained Si/ 6.8 nm strained Ge / relaxed $Si_{0.6}Ge_{0.4}$ structure. Off-state leakage (I_D at V_G = 0V) increases with increasing drain bias. Leakage for the Ge channel MOSFET is significant in comparison to the onstate current. Up to 20% of the offstate leakage is collected at the source contact suggesting some loss of gate control. The off-state leakage scales with W, the width of the device, indicating the leakage occurs at the SD/gate overlap.(b) Gated and ungated diode leakage characteristics with V_G = 0V for a 200 μm x 200 μm square diode. Gated diode leakage matches offstate leakage in (a).

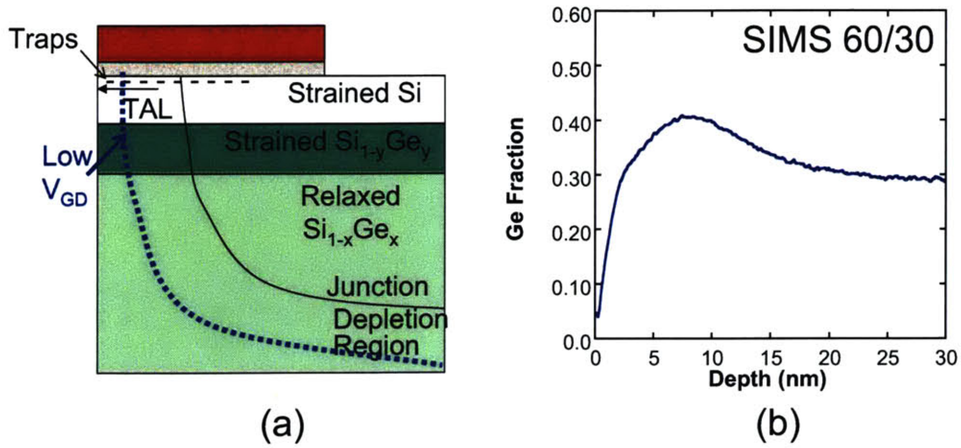


Figure 5-5: (a) Trap assisted leakage mechanism in SiGe heterostructure MOSFETs. Traps in the space charge region act as generation-recombination centers. (b) SIMS from the SD region of 6 nm strained Si/10 nm strained $Si_{0.4}Ge_{0.6}$/ relaxed $Si_{0.7}Ge_{0.3}$ after SD implant (B, 4x10^{15} cm^{-2}, 10 keV) and anneal (10 sec, 800°C RTP). There is a significant enhancement in Si-Ge interdiffusion for the implanted strained SiGe layer.

5.2.1 Trap Assisted Leakage

A schematic of trap assisted leakage (TAL) is shown in Figure 5-5 (a). At low drain bias traps within the bandgap in the depletion region of the reverse biased SD junction act as generation-recombination centers and lead to increased leakage. This is consistent with the large temperature dependance shown in Figure 5-2 (b). The two main sources of traps in these structures are interface states at the oxide-Si interface, and Ge traps in the oxide due to enhanced Ge diffusion in the gate-drain overlap region. These structures have a non-optimized gate oxide process. In order to minimize the thermal budget, the oxide is grown in a wet ambient at 600°C for 3 hours. The resulting oxide has a high density of interface traps, D_{it}, 1 x 10^{11} cm^{-2} (D$_{it}$ was measured using the charge pumping method). Figure 5-5 (b) shows SIMS from the SD region of 6 nm strained Si/10nm strained $Si_{0.4}Ge_{0.6}$/ relaxed $Si_{0.7}Ge_{0.3}$ post SD implant (B, 4x10^{15} cm^{-2}, 10 keV) and anneal (10sec, 800°C RTP). This implant was determined to be fully amorphizing to a depth of 50 nm using UT-MARLOW simulations [90]. The peak Ge composition has dropped to 40 at. % and there is significant broadening of the strained $Si_{0.4}Ge_{0.6}$ layer. This shows significant enhancement in

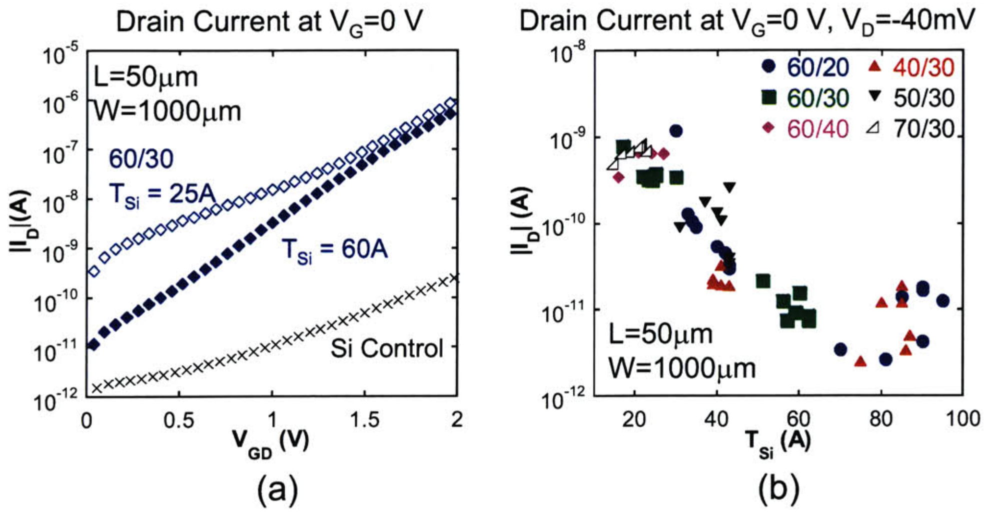


Figure 5-6: (a) I_D versus V_{DG} with $V_G = 0$V for strained Si/10nm strained $Si_{0.4}Ge_{0.6}$/ relaxed $Si_{0.7}Ge_{0.3}$. I_D shows strong Si cap thickness dependence at low V_{GD}. (b) Off-state drain to substrate leakage current at $V_{DG} = 40$mV. Leakage shows strong dependence on cap thickness, T_{Si} at low V_{GD} for $T_{Si} < 70$Å. Ge fraction in virtual substrate of $0.2 \leq x \leq 0.4$ and Ge fraction in the strained layer of $0.4 \leq y \leq 0.7$.

Si-Ge interdiffusion for implanted strained SiGe layer, consistent with the work by Xia *et. al.* [81].

I_D versus V_{GD} with $V_G = 0$V for strained Si/10nm strained $Si_{0.4}Ge_{0.6}$/ relaxed $Si_{0.7}Ge_{0.3}$ for Si cap thicknesses of 2.5 and 6 nm is plotted in Figure 5-6 (a). The leakage at low V_{GD} is almost two orders of magnitude higher for the thinner Si cap. It is interesting to note, that at low V_{GD} the the off-state leakage for the 6 nm Si cap is only 10X greater than the Si control. Off state leakage for V_D=-40mV and V_G=0V is plotted as a function of Si cap thickness in Figure 5-6 (b). The Si cap thickness is extracted for each data point using simulation as outlined in Section 3.3.3. A wide range of Ge compositions in both the strained and relaxed layer are plotted, with Ge fraction in virtual substrate of $0.2 \leq x \leq 0.4$ and Ge fraction in the strained layer of $0.4 \leq y \leq 0.7$. This shows that the TAL scales with T_{Si} for T_{Si} below 7 nm with I_D increasing exponentially with decreasing cap thickness. This scaling appears effectively independent of the SiGe heterostructure. For T_{Si} above 7 nm I_D is very close to the Si control value. This result suggests that the increase in leakage with decreasing Si cap thickness is due to an increase in Ge-related traps at the oxide

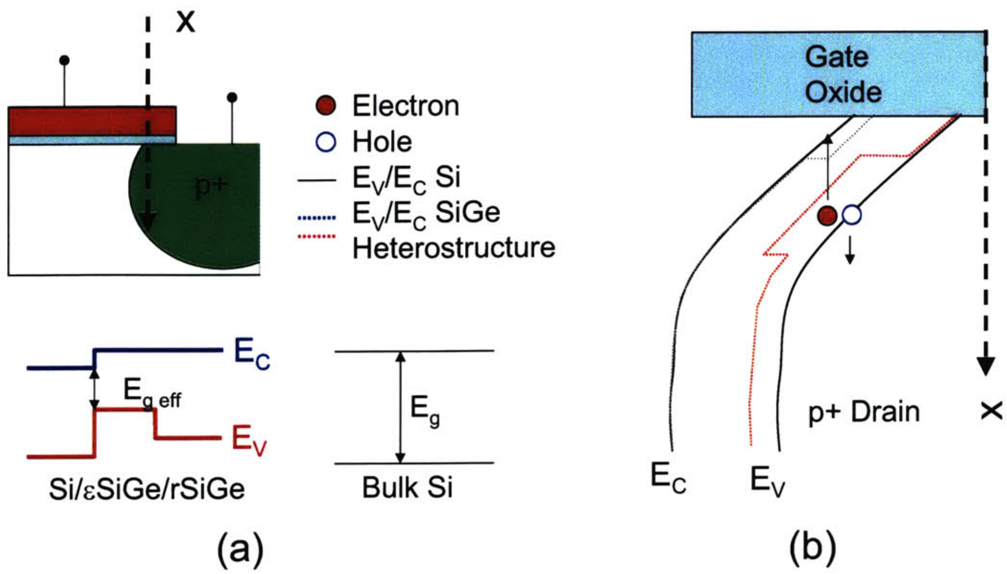


Figure 5-7: Band structure in the SD/gate overlap region at high V_{GD}. There is large band bending and high electric field in the vertical direction due to the high potential difference between the gate and drain. Electrons can tunnel from the p+ SD valence band into the inversion region at the Si/oxide interface. The reduced band gap/effective band gap in the SiGe heterostructure leads to a shorter tunneling distance and increased leakage compared to bulk Si. This is type of BBT leakage is referred to as gate induced drain leakage, GIDL.

interface. Ge is able to diffuse to the Si-Oxide interface in the SD-gate overlap region due to enhanced Si-Ge inter-diffusion from the amorphizing SD implant. A higher level of Ge can reach the interface with a thinner Si cap resulting in increased leakage.

For state of the art devices a very thin Si cap is required (<1 nm as discussed in Section 4.2). Based on the data in Figure 5-6 (b), such a thin cap would result in very high leakage at low V_D. However, the fabrication process for these devices is quite crude with a very heavy SD implant. A state of the art process would include a much lower dose and energy extension implant in the SD-gate overlap region, resulting in significantly lower implant damage enhanced diffusion.

5.2.2 BBT and Gate Induced Drain Leakage

A schematic of the BBT mechanism for the structures investigated in this study is shown in Figure 5-7. There is large band bending and high electric field in the

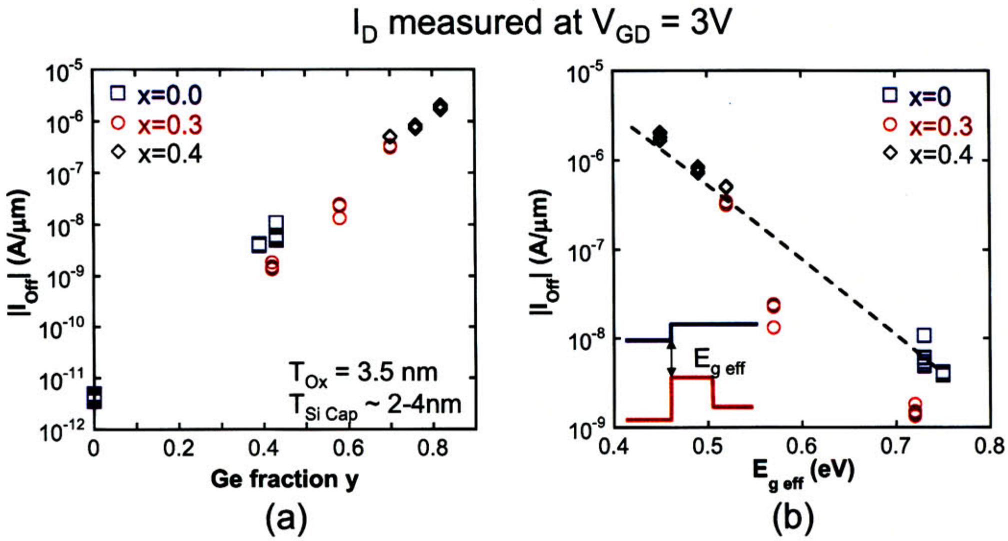


Figure 5-8: (a) Off-state leakage for dual channel heterostructures as a function of Ge fraction in the relaxed buffer layer, x, and in the strained SiGe channel, y. V_{GD}=3V, V_G=0V. (b) Data from (a) plotted as a function of effective band gap, E_{geff}. Line fit is based on Equation 5.2 and F_{max} of 1.6MV/cm.

vertical direction in the drain-gate overlap region due to the high potential difference between the gate and drain at high V_{GD}. As outlined in Section 2.3, with sufficient band bending the valence band on one side of a junction lines up with the conduction band on the other. In the drain-gate overlap region, electrons can tunnel from the p+ valence band in the drain into the inversion region at the Si-oxide interface. The reduced band gap and effective band gap in the SiGe heterostructure leads to a shorter tunneling distance and increased leakage compared to bulk Si. This type of BBT leakage is referred to as gate induced drain leakage, GIDL [80].

The offstate leakage for dual channel heterostructures as a function of Ge fraction in the relaxed buffer layer, $0 \leq x \leq 0.4$, and in the strained SiGe channel, $0.4 \leq y \leq 0.82$ for V_{GD} = 3V is plotted in Figure 5-8 (a). The leakage increases exponentially with increasing Ge fraction in the strained layer. The same data is plotted in Figure 5-8 (b) as a function of effective bandgap. E_{geff} was determined from the conduction band offset in strained Si from Welser [62] and the valence band offset from Van de Walle *et al.* [19]. It is important to note that there is at least a ± 100 meV uncertainty in the values obtained for effective bandgap. An ideal heterostructure in the drain-gate overlap region is also assumed, which is not necessarily a good assumption based upon implant damage effects discussed in Section 5.2.1. As shown in Figure 5-8 (b) a line was fitted using a simplification of the Schenk model (see section 2.3):

$$I_{off} = Const E_{geff} F_{max}^{7/2} exp\left(-\frac{B E_{geff}^{3/2}}{F_{max}}\right) \tag{5.2}$$

where F_{max} is the peak vertical electric field in the drain-gate overlap region obtained from simulation using Dessis [60].

The simulation used a simplified bulk Si structure with the bandgap adjusted to 0.75 eV (SiGe band gap predicted by [19] for strained $Si_{0.61}Ge_{0.39}$ on bulk Si), and the doping adjusted in the SD-gate overlap region to match the offstate leakage on the 39/0 structure at V_{GD}=3V. The Schenk model with the Dessis default parameters was used for BBT generation. After extracting an F_{max} value of 1.6 MV/cm, the constant, Const, was used as a fitting parameter to match the leakage on 39/0 structure using the default value for B in Dessis (B=2.147x10^7 $(eV)^{-3/2}Vcm^{-1}$) and E_{geff} of 0.75 eV. While this is a crude approximation, it serves to show that the leakage does scale with effective bandgap. The effective band gap can be significantly smaller than the band gap of the strained SiGe layer depending on the level of strain. However, its effect can be minimized by making the Si cap as thin as possible (which is required for electrostatic purposes also). Looking back at Figure 5-7, electrons can only tunnel to a position where there is an available state. If the Si cap is very thin there will be significant quantization in the quantum well formed in the conduction band, causing the effective conduction band edge to rise, hence increasing the effective bandgap. Therefore, the bandgap in the SiGe as opposed to the effective band gap is expected be more relevant for state of the art devices with very thin Si cap layers.

5.2.3 Impact of W_{chan} on GIDL

The structures analyzed in this section have been discussed in detail already in this thesis for mobility. Further details on structure and metrology can be obtained in Section 4.5.

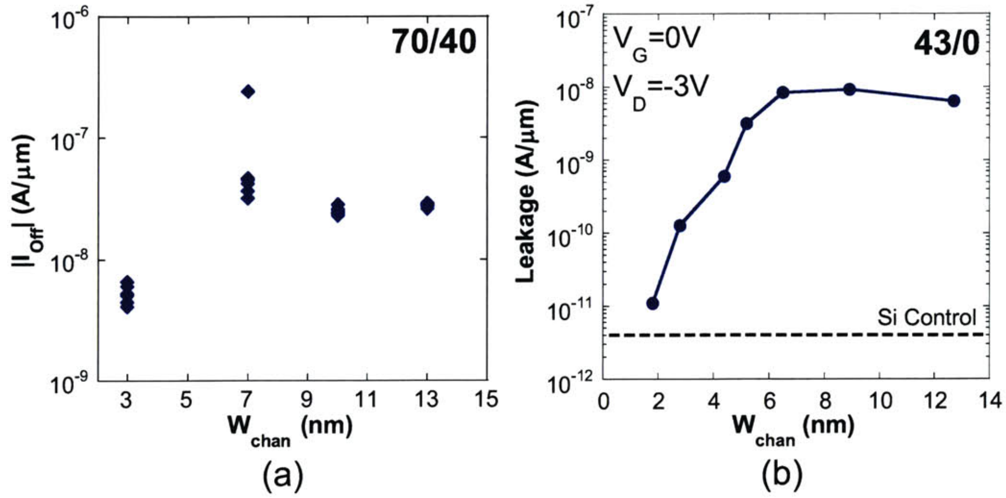


Figure 5-9: Off-state leakage at V_G=0V and V_D=-3V as a function of strained SiGe channel thickness, W_{chan} for (a) strained Si/ strained $Si_{0.3}Ge_{0.7}$ / relaxed $Si_{0.6}Ge_{0.4}$ structures and (b) strained $Si_{0.57}Ge_{0.43}$ on bulk Si

Reducing the thickness of the high-Ge-content layer in heterostructure p-MOSFETs has been suggested as a means of reducing off-state leakage [82]. For very thin films quantization in the quantum well leads to an effective increase in the bandgap. However, this effect only becomes significant for W_{chan} < 2-3 nm [82]. The off-state leakage versus channel thickness for the strained Si/ strained $Si_{0.3}Ge_{0.7}$ / relaxed $Si_{0.6}Ge_{0.4}$ structures is plotted in Figure 5-9 (a). Channel thickness has little impact on the leakage until the thickness drops to 3 nm. However, from SIMS/XTEM analysis the Ge composition in the 3 nm film has dropped to ~56%. Based on the dependence of leakage on Ge composition in the strained layer shown in Figure 5-8 (a), the drop in leakage is accounted for by the drop in Ge composition rather than a dependence on W_{chan}. This 10X drop in leakage comes at the expense of a very large drop in mobility enhancement from 4X down to 2.5X (Figure 4-7).

A more comprehensive study of leakage as a function of W_{chan} was performed for pseudomorphic structures discussed in Section 4.5.2. The leakage as a function of SiGe channel thickness for strained $Si_{0.57}Ge_{0.43}$ on bulk Si is shown in Figure 5-9 (b). The peak Ge composition is maintained at 43 at. % for W_{chan} down to 2.8 nm. The Ge concentration in the 1.8 nm film is ~ 40 at. %. It can be seen that the leakage

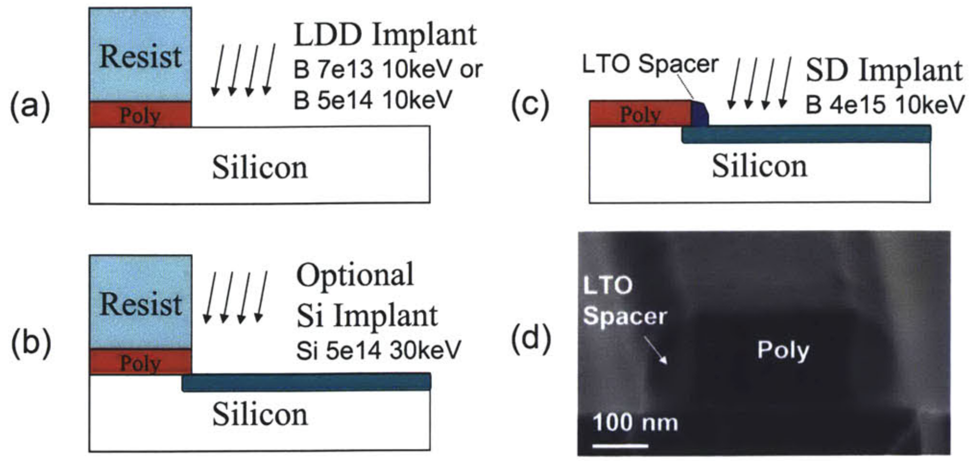


Figure 5-10: Spacer process for analysis of SD extension dose and implant damage on off-state leakage. (a) Lightly doped drain, LDD, of boron at 10keV with a dose of either $7\text{x}10^{13}cm^{-2}$ or $5\text{x}10^{14}cm^{-2}$ is implanted. (b) This is followed by an optional Si implant of $5\text{x}10^{14}cm^{-2}$ at 30keV. (c) The SD of $4\text{x}10^{15}cm^{-2}$ B at 10keV is implanted after the formation of 100 nm LTO spacer. (d) Cross-sectional SEM of LTO spacer on a bulk Si substrate.

starts to drop for $W_{chan} < 6$ nm, with 2 orders of magnitude reduction in leakage for the 2.8 nm film. This decrease in leakage does not correlate fully to the increase in the effective bandgap due quantization in the channel. For example, in a 2.8 nm 43/0 finite quantum square well, the ground state energy will shift by $\sim$90 meV. Figure 5-8 (b) suggests a drop in leakage of $\sim$ 10X for 100 meV drop in the band gap. Therefore, some of the drop in leakage for the thinner films is probably due to a decrease in the peak Ge composition in the SD overlap region due to enhanced Si-Ge interdiffusion as suggested in Section 5.2.1. As demonstrated for the 70/40 structure, the drop in off-state leakage is obtained at the expense of a large decrease in mobility for $W_{chan} <$ 4 nm (Figure 4-11). The leakage dependence on channel layer thickness is consistent with results obtained for HOI MOSFETs [68].

5.2.4 Impact of SD implant on GIDL

In order to look at the impact of the SD implant conditions on the off-state leakage, devices were fabricated with spacer technology, as outlined in Figure 5-10. The Ge composition and layer thickness were determined by SIMS. In this experiment the

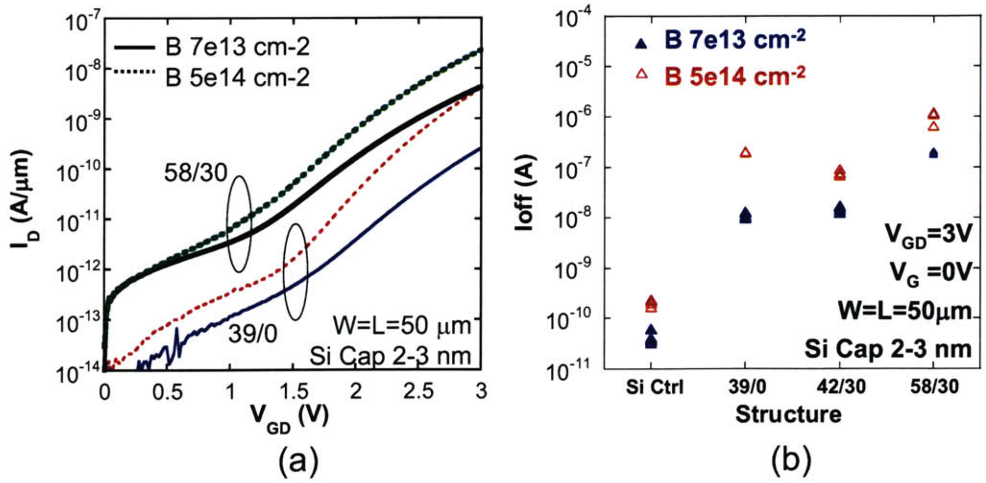


Figure 5-11: (a) Off-state leakage (V_G=0V) for 58/30 and 39/0 structure with LDD implant of B, 10keV at 7x10$^{13}cm^{-2}$ or 5x10$^{14}cm^{-2}$. (b) Off-state leakage (V_G=0V, V_{GD}=3V for all the structures in this study. 6 devices measured from the same 1 cm x 1 cm die on each wafer.)

impact of SD dose and implant damage are investigated. To examine the impact of dose a lightly doped drain, LDD, was employed with implant conditions of boron at 10 keV with a dose of either 7x10$^{13}cm^{-2}$ or 5x10$^{14}cm^{-2}$. The deep SD implant of 4x10$^{15}cm^{-2}$ B at 10 keV was separated from the SD/gate overlap region with a spacer. An optional Si implant of 5x10$^{14}cm^{-2}$ at 30 keV was included after the LDD implant to examine the effect of implant damage without affecting the B dose. The Si implant is fully amorphizing down to a depth of 30 nm, and is almost identical to the amorphization caused by the 10 keV 4x10$^{15}cm^{-2}$ B SD implant. This is in contrast to 20% and 2% amorphization for 7x10$^{13}cm^{-2}$ or 5x10$^{14}cm^{-2}$ B LDD implants respectively. The degree of amorphization was determined from simulation using UT-MARLOW [90] based on the work of Xia *et al.* [81]. When the interstitial concentration reaches 5x10$^{21}cm^{-3}$ (10% of Si lattice density) at a given depth, the sample is assumed to be amorphized at that depth.

The impact of LDD dose on off-state leakage is shown in Figure 5-11 (a) for the 39/0 and the 58/30 structure. Increasing the dose from 7x10^{13} to 5x10$^{14}cm^{-2}$ results in an increase in leakage. This is expected as increasing the doping concentration in the SD/gate overlap region will result in a higher electric field at the surface and

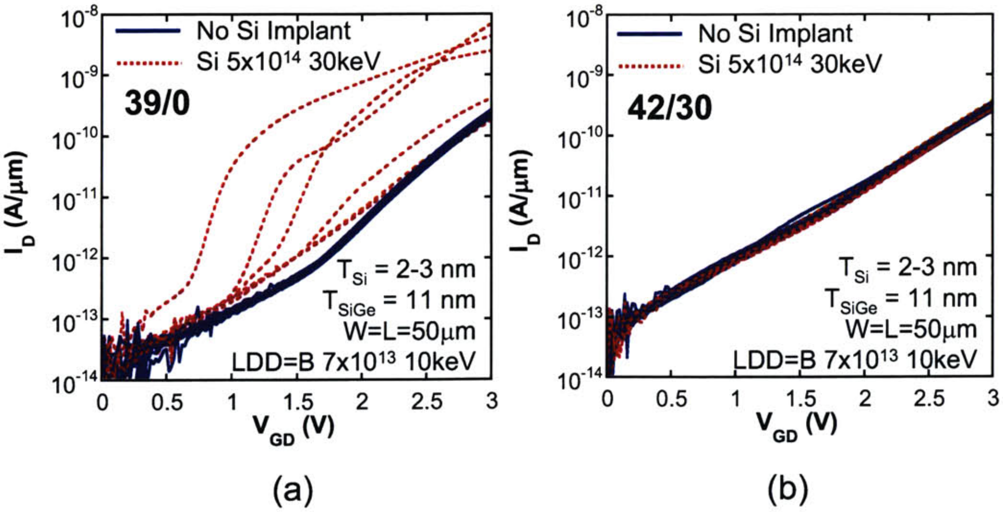


Figure 5-12: Off-state leakage (V_G=0V) 39/0 structure with LDD implant of B, 10keV at 7x10$^{13}cm^{-2}$ with and without a 30keV, 5x10$^{14}cm^{-2}$ Si implant. 6 devices measured from the same 1 cm x 1 cm die. (a) 39/0 structure, (b) 42/30 structure.)

hence higher BBT. The leakage is $\sim$ 10X higher for the 5x10$^{14}cm^{-2}$ dose for all the structures analyzed in this study (Figure 5-11 (b)). This result illustrates the importance of SD doping to BBT. The off-state leakage can be minimized by careful design of the SD doping profiles.

Figure 5-12 shows the impact of an amorphising Si implant on the off-state leakage for the 39/0 and the 42/30 structures. Both structures have similar strained SiGe film thickness ($\sim$ 11 nm) and Ge fraction ($\sim$ 40 at. %) in the strained SiGe channel, however, the level of strain is much lower for the 42/30 structure. For both the 39/0 and the 42/30 structure without the Si implant, the leakage is very uniform between devices. The Si implant causes the leakage to increases significantly for the 39/0 structure with a large variation in leakage between devices. However, the Si implant does not seem to have any impact on the off-state leakage of the 42/30 structure. The high leakage on the 39/0 structure is most likely due to defects in the SiGe layer in the depletion region of the SD junction caused by relaxation of the strained SiGe layer. The 39/0 structure is likely to relax with an amorphizing implant, as the equilibrium critical thickness for the strained $Si_{0.61}Ge_{0.39}$ film is $\sim$ 6.5 nm, which is significantly thinner than the 11 nm channel thickness on these structures. This is in contrast

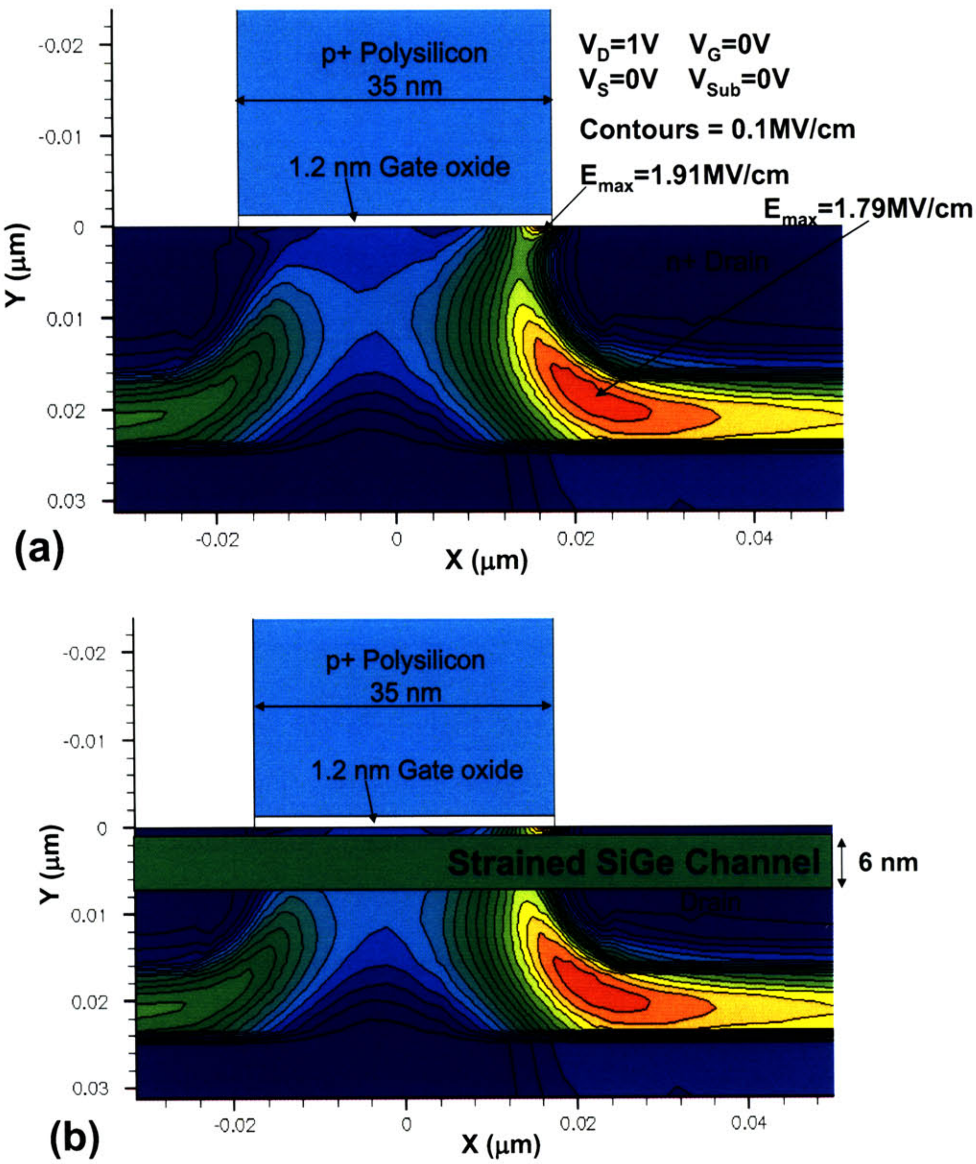


Figure 5-13: (a) Intel 65 nm node NMOS simulation of off-state electric field based on inverse modeling courtesy of O. Nayfeh. There are high fields at both the drain-gate overlap region and the drain-to-halo junction leading to BBT. (b) Suggested structure for strained SiGe on a bulk Si substrate in order to minimize BBT.

to the 25 nm critical thickness for the $Si_{0.58}Ge_{0.42}$ film. Again, this result suggests that careful SD and heterostructure engineering is required for SiGe heterostructure MOSFETs to minimize defects and leakage in the SD region.

5.3 BBT in state of the art devices

The presence of halo doping required to suppress short channel effects leads to very high electric fields at the drain-halo junction in state of the art devices [84]. This results in leakage due to BBT across the junction as well as GIDL. As the doping in the channel increases with decreasing channel length, BBT at the drain-halo junction is becoming more and more significant. A simulation of the electric field in the off-state of a state-of-the-art device is shown in Figure 5-13 (a). Very high electric fields appear in both the drain-gate overlap region and the drain-to-halo junction. The very high electric field in the SD junction means that the bandgap of the substrate becomes important for BBT. This suggests that strained SiGe channels grown pseudomorphically on bulk Si substrates may be advantageous in minimizing BBT in short channel devices due to the large bandgap of bulk Si compared to the smaller bandgap in relaxed SiGe virtual substrate.

Figure 5-13 (b) shows a suggested implementation of such a structure. The strained SiGe channel should be kept as thin as possible to avoid overlap with the high electric field.

5.4 Chapter Summary

In this chapter we have looked at the subthreshold and off-state leakage for strained SiGe heterostructures. Complementing the work on mobility, it was shown that the Si cap thickness must be minimized to maximize gate control of the channel.

The results demonstrate that the off-state leakage in these devices is a complex product of structure, SD engineering and processing effects. This makes it difficult to make any quantitative conclusions based on this work. However, the following trends have been observed.

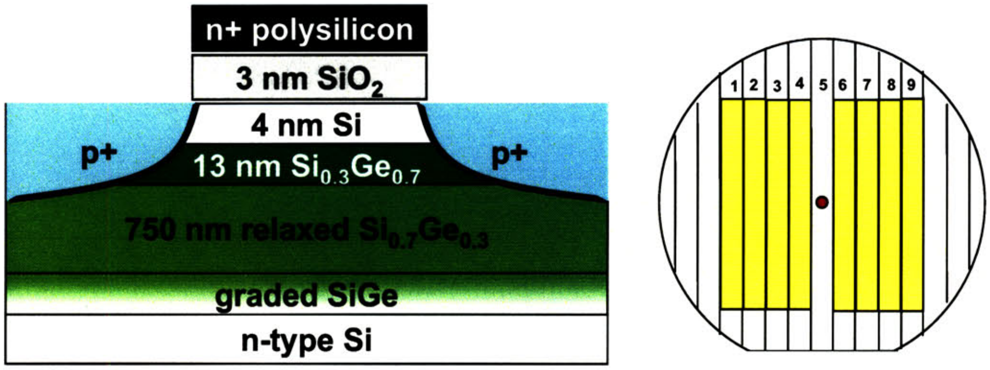
The off-state leakage in the SiGe heterostructures studied is due to a combination of trap assisted leakage at low V_{GD} and BBT due to GIDL at high V_{GD}. The trap assisted leakage can increase due to the presence of Ge traps at the oxide in the drain-gate overlap region. GIDL is found to increase exponentially with increasing Ge fraction in the strained SiGe channel and the effective bandgap between the strained SiGe and Si cap. There is some suggestion that leakage can be reduced by decreasing the channel thickness below 4 nm. However, this comes at the expense to reduced channel mobility. Leakage can be reduced by reducing the electric field in the drain-gate overlap region through doping control, although this must be traded off against SD series resistance. Implant damage can have a large effect on the off-state leakage for strained SiGe layers above the critical thickness. Finally the bandgap of the substrate becomes important for state of the art devices due to BBT at the drain-halo junction.

Chapter 6

Laser Spike Annealing as a low thermal budget solution

6.1 Introduction

SiGe hetrostructure devices require a relatively low thermal budget due to the very high diffusivity of Ge in compressively strained SiGe layers. Ge diffusion causes the peak Ge concentration in the strained SiGe channel to drop and can result in Ge related traps at the strained Si-gate dielectric interface, both of which degrade the channel mobility [7][85]. Ge diffusivity increases exponentially with increasing Ge concentration and strain [86]. A number of low thermal budget process techniques have been investigated to achieve good dopant activation in Si ultra-shallow junctions including Laser Thermal Processing (LTP) [87] and Laser Spike Annealing (LSA)[88]. LSA achieves sub-melt temperatures in the μsec-msec time frame, making it an attractive candidate as a low thermal budget solution for SiGe processing. In this chapter the impact of LSA on mobility and leakage in strained Si/ strained $Si_{0.3}Ge_{0.7}$/ relaxed $Si_{0.7}Ge_{0.3}$ dual channel p-MOSFETs is examined.



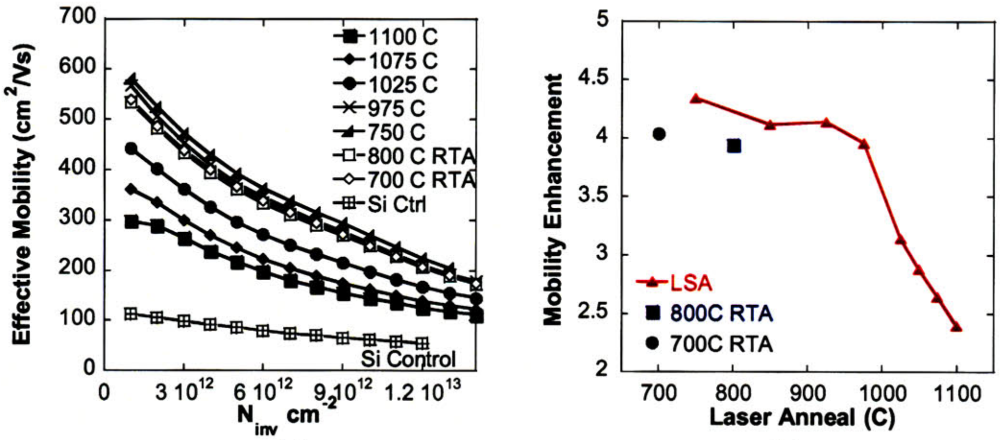
(a) (b)

Figure 6-1: (a) Dual channel p-MOSFET layer structure. Relaxed layers are doped in-situ with phosphorus to a level of 1 x 10^{17} cm^{-2}. Strained SiGe and strained Si layers are undoped. (b) Columns of area 11 mm x 92 mm received a laser anneal with various power densities, as described in the text. Four columns on either side of the center were annealed and the center column is a control and was not annealed. LSA was performed at Ultratech Inc. courtesy of X. Wang.

6.2 Mobility dependence on LSA temperature

6.2.1 Experiment Design

Heterostructure p-MOSFETS were fabricated and analyzed for this study. The layer structure is illustrated in Figure 6-1 (a). Source drain activation was achieved through either a rapid thermal anneal, RTA, for 10 seconds or a LSA. LSA was performed at Ultratech Inc. courtesy of X. Wang. The wafers which received the laser anneal were annealed in columns with each column receiving a different temperature anneal (Figure 6-1 (b)). The quoted LSA anneal temperature corresponds to the surface temperature a bare Si wafer would reach under the laser annealing conditions (CO_2, dwell time = 800 μs, laser power density = 0.15 $\sim$ 0.3 $kWmm^{-2}$, the temperatures were calibrated by the Si melting temperature (1412°C)). Therefore, the actual surface temperature for the SiGe samples is possibly higher than the quoted temperature, due to the poor thermal conductivity of the relaxed $Si_{0.7}Ge_{0.3}$ virtual substrate ($\sim$20X lower than Si) [15]. A relaxed $Si_{0.7}Ge_{0.3}$ virtual substrate (no strained Si or strained SiGe layer) was found to melt at the Si equivalent temperature of 1270°C, based on



(a) (b)

Figure 6-2: (a) Effective hole mobility as a function of inversion charge density, N_{inv}, for strained Si/ strained $Si_{0.3}Ge_{0.7}$ / relaxed $Si_{0.7}Ge_{0.3}$ structures, extracted on 50 μm x 50 μm devices using the split C-V technique. Si cap layer thickness is 4-5 nm for all devices. (b) Hole mobility enhancement factor relative to Si control devices at N_{inv}=1 x 10^{13} cm^{-2} for different laser anneal and RTA temperatures. Note: The quoted LSA anneal temperature corresponds to the surface temperature a bare Si wafer would reach under the laser annealing conditions.

visual inspection, which is significantly lower than equlibrium liquidus temperature of bulk $Si_{0.7}Ge_{0.3}$ of approximately 1350°C, but above the equilibrium solidus temperature of 1214°C [89]. The equilibrium liquidus and solidus temperatures of bulk $Si_{0.3}Ge_{0.7}$ are 1160°C and 1024°C respectively.

6.2.2 Mobility

The measured hole mobility for strained Si/ strained $Si_{0.3}Ge_{0.7}$/ relaxed $Si_{0.7}Ge_{0.3}$ p-MOSFETs is shown in Figure 6-2 (a) for various LSA and RTA anneal temperatures. The Si control received an RTA at 800°C. The measured hole mobility remains high for LSA temperatures up to ~1000°C, and drops for higher temperatures. This temperature is very close to the equilibrium solidus temperature of $Si_{0.3}Ge_{0.7}$ of 1024°C. The RTA temperatures examined in this study of 800°C and 700°C do not affect mobility significantly, but higher RTA temperatures are known to degrade the mobility [7]. Figure 6-2(b) shows hole mobility enhancement relative to the Si control device at an inversion charge density N_{inv}=10^{13} cm^{-2} as a function of anneal temperature.

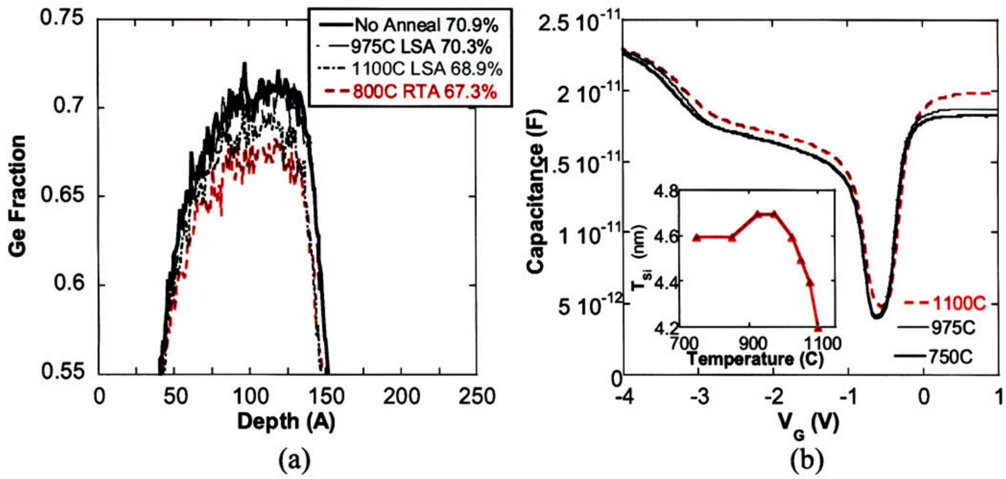
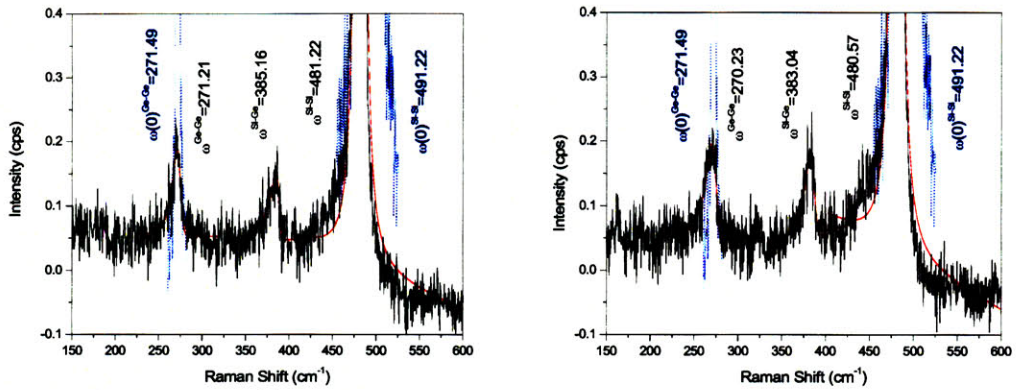


Figure 6-3: (a) SIMS profiles for the strained $Si_{0.3}Ge_{0.7}$ layer. There is very little Ge outdiffusion, even for the 1100°C laser anneal, compared to reduction of 4 at. % Ge for the 800°C RTA. (b) Capacitance-Voltage characteristics for strained Si/ strained $Si_{0.3}Ge_{0.7}$ / relaxed $Si_{0.7}Ge_{0.3}$ p-MOSFETS with different laser annealing conditions. Inset shows Si cap thickness extracted from C-V analysis.

A hole mobility enhancement of ~4X is achieved for heterostructure p-MOSFETs subject to LSA, similar to that achieved for RTA. The hole mobility enhancement decreases rapidly for LSA above 975°C. This temperature is significantly higher than possible with Rapid Thermal Annealing, due to device degradation associated with Ge diffusion in the heterostructure.

6.2.3 Analysis

Secondary Ion Mass Spectrometry (Figure 6-3(a)) indicates that there is very little diffusion of Ge from the strained $Si_{0.3}Ge_{0.7}$ layer in samples subject to LSA, and thus Ge outdiffusion cannot account for the decrease in hole mobility above 975°C. The drop in Ge concentration for the sample subject to 1100°C LSA is only 2 at. %. Capacitance-voltage (C-V) measurements were used to extract the Si cap layer thickness as described in Section 3.3. This analysis indicates a 0.5 nm decrease in the Si cap thickness for the 1100°C anneal, due to Ge diffusion into the Si cap, which can be seen as an increase in the characteristic plateau capacitance in inversion (Figure 6-3(b)). The inset in Figure 6-3(b) shows that the Si cap layer thickness decreases for



(a) (b)

Figure 6-4: UV-Raman spectra of the Si cap and strained SiGe channel phonons (black) for (a) 1100°C LSA, (b) 975°C LSA samples, along with unstrained Si and Ge reference samples (blue). A fit to the phonon peaks using Lorentzian and Exponentially Modified Gaussians (EMG) lineshapes is shown in red. The Ge-Ge mode is used to calculate the strain in the $Si_{0.3}Ge_{0.7}$ channel. Raman spectroscopy courtesy of M. Canonico of Freescale Semiconductor, Inc.

LSA temperatures above 1000°C. The reduced plateau width indicates a reduction in the strained Si/ strained $Si_{0.3}Ge_{0.7}$ valence band offset, ΔE_V of approximately 60 meV, which suggests some decrease in Ge fraction or strain.

To verify the strain state after annealing, Raman spectra were collected using the 364 nm Ar-Ion line and fit with a combination of Lorentzian and Exponentially Modified Gaussian (EMG) lineshapes to the phonon modes (Figure 6-4). The 364 nm line was chosen in order to eliminate contributions to the spectra arising from the $Si_{0.7}Ge_{0.3}$ virtual substrate, as the sampling depth at 364 nm is estimated to be 6 nm in Si. The Ge-Ge mode is used to calculate the strain in the $Si_{0.3}Ge_{0.7}$ channel since for Ge-rich alloys, the Si-Si band intensity is not sufficient for accurate fitting and is difficult to decouple from the signal from the Si cap layer. There is a slight broadening in the Ge-Ge phonon peak for the 1100°C LSA suggesting an increase in variation in strain across the sampling depth and/or increased grading of the Ge composition. UV Raman analysis on the 1100°C sample suggests that the Ge-Ge phonon peak is shifted by 1 cm^{-1} relative to the Ge-Ge peak in the 975°C or un-annealed sample. A shift of approximately 7 cm^{-1} is expected for a fully relaxed film.

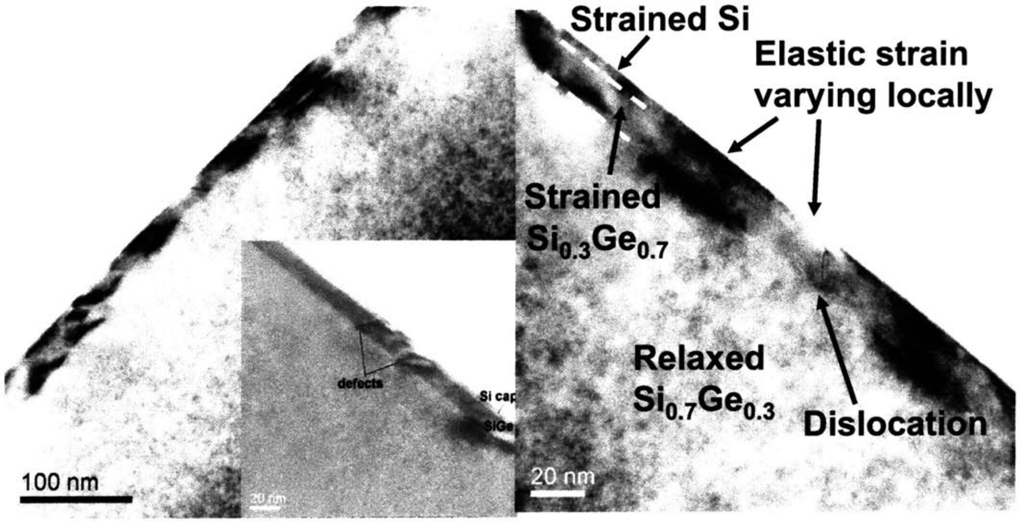


Figure 6-5: XTEM of strained Si/ strained $Si_{0.3}Ge_{0.7}$/ relaxed $Si_{0.7}Ge_{0.3}$ dual channel heterostructure subjected to 1100°C LSA. XTEM courtesy of N. D. Theodore of Freescale Semiconductor, Inc.

Based on the Ge concentration obtained through SIMS, a frequency shift of 1 cm^{-1} corresponds to a reduction in strain of approximately 0.2 GPa, between the 1100°C and 975°C LSA splits, which is equivalent to a relaxation of 10% of the original strain in the $Si_{0.3}Ge_{0.7}$. This partial strain relaxation is consistent with the generation of dislocations in the $Si_{0.3}Ge_{0.7}$ channel which can severely degrade mobility. The partial relaxation and defect formation is not surprising as the 13 nm-thick channel is well above the equilibrium critical thickness of 7 nm for strained $Si_{0.3}Ge_{0.7}$ on relaxed $Si_{0.7}Ge_{0.3}$, and the estimated anneal temperature is very close to the melting point of $Si_{0.3}Ge_{0.7}$.

Cross-sectional Transmission Electron Microscopy analysis, XTEM, was performed on the 1100°C laser anneal sample (Figure 6-5). The XTEM shows periodic lobes of strain contrast in the strained Si and strained $Si_{0.3}Ge_{0.7}$ layers suggesting that the elastic strain is varying locally. On closer inspection, microtwins and defects can be seen in the strained $Si_{0.3}Ge_{0.7}$ layer. The defect density is estimated to be 10^7 cm^{-2}. This data suggests that the reduction in mobility at very high LSA temperatures is due to a combination of local strain variation or relaxation and scattering from defects.

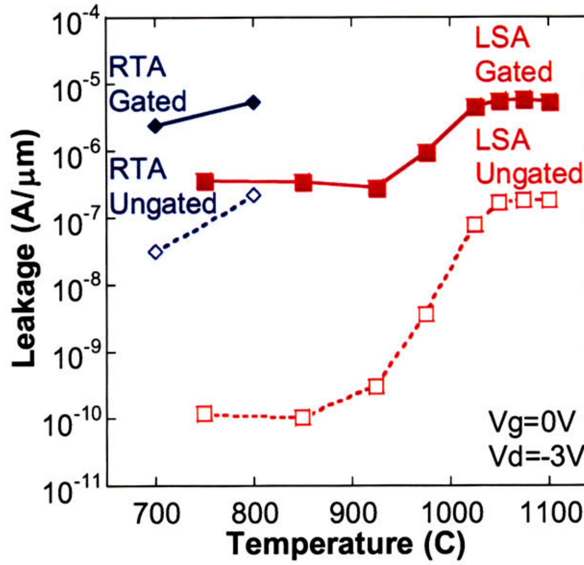


Figure 6-6: Leakage current (V_D=-3V with gate and substrate grounded) for gated and un-gated p+/n diodes subject to LSA and RTA. The leakage current for Si control was roughly 3 x 10^{-12} A/μm for un-gated and gated diodes respectively.

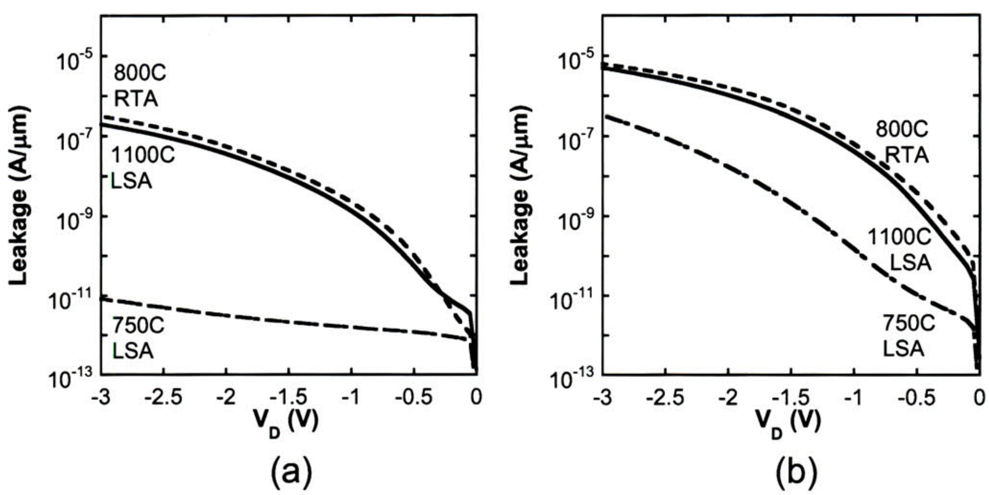


Figure 6-7: Diode leakage current (in A per micron of perimeter) for (a) un-gated and (b) gated diodes versus applied drain bias with gate and substrate grounded. Leakage for both the gated and un-gated diodes scales with perimeter.

6.3 LSA of Super-Critical Thickness SiGe

The leakage current at V_{DB}=-3V for gated and un-gated p+/n diodes is plotted as a function of anneal temperature in Figure 6-6. The leakage is found to be perimeter dependent for both the gated and un-gated diodes subject to either RTA or LSA. The gated p+/n diode represents the drain/body diode of the MOSFET, and in fact the measured MOSFET off-state leakage (I_{DS} at V_G=0, V_D=-3V) is equal to the drain-body diode leakage. For un-gated diodes, the leakage for LSA devices annealed below 975°C is over three orders of magnitude lower than for the 800°C RTA sample. The leakage on the RTA devices is comparable to the leakage on the LSA devices annealed above 1000°C, where the mobility was severely degraded.

The current-voltage (I-V) characteristics for the 750°C LSA, 1100°C LSA and 800°C RTA diodes are plotted in Figure 6-7. Significantly, the leakage characteristics for the RTA and 1100°C LSA are almost identical and very different from the 750°C LSA device. The difference is most dramatic for the un-gated diodes (Figure 6-7 (a)). The results suggest that the leakage mechanism for the RTA and high temperature LSA diodes is the same, and likely associated with crystal defects in the S/D junction region. This is consistent with the very high perimeter dependent leakage for the un-gated diode, suggesting that the leakage occurs where the S/D junction edge overlaps the strained SiGe channel. The low leakage measured on the un-gated 750°C LSA diodes is consistent with that measured for such a heterostructure with the strained SiGe channel thickness below the critical thickness [11]. The boron implant used for the S/D (10 keV, 4 x 10^{15} cm^{-2}) was determined to be fully amorphizing to a depth of 50 nm using UT-MARLOW simulations [90].

XTEM of the drain-gate overlap region is shown for the 800°C RTA and the 850°C LSA in Figure 6-8 (a,c,e) and (b,d,f) respectively with increasing magnification. There are a number of differences between the SD region for the RTA and LSA samples. First, the damage due to the SD implant is significantly higher on the RTA samples. This damage appears in the strained $Si_{0.3}Ge_{0.7}$ layer as end of range damage, EOR, in the relaxed $Si_{0.3}Ge_{0.7}$ substrate. The damage to both the strained $Si_{0.3}Ge_{0.7}$ layer and the EOR damage is significantly less on the LSA sample. Of more importance for understanding the leakage mechanism is the evolution of the implant damage at the SD-gate overlap region. For the RTA sample, the damage-induced defects in the strained $Si_{0.3}Ge_{0.7}$ layer extends under the gate. On the LSA sample the defects terminate before the gate edge. This difference in implant damage-induced defects

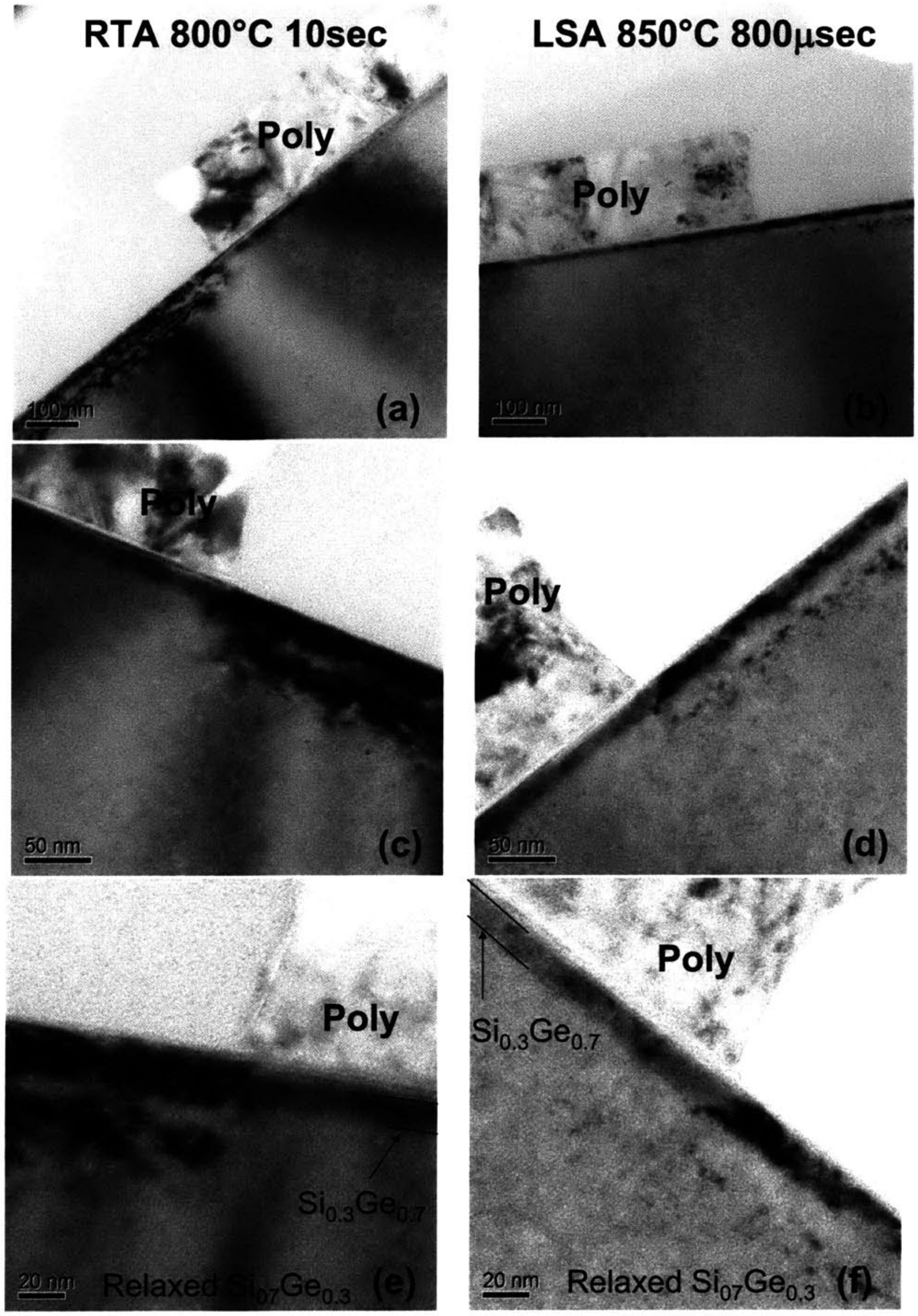


Figure 6-8: XTEM of SD-Gate overlap region of strained Si/ strained $Si_{0.3}Ge_{0.7}$/ relaxed $Si_{0.7}Ge_{0.3}$ dual channel heterostructure subjected to 800°C RTA (a,c,e) and 850°C LSA (b,d,f). Implant damage induced defects in strained SiGe and end of range damage are significantly higher for RTA anneal. Damage extends under the gate for RTA, but does not appear to do so for the LSA anneal. XTEM courtesy of N. D. Theodore of Freescale Semiconductor, Inc.

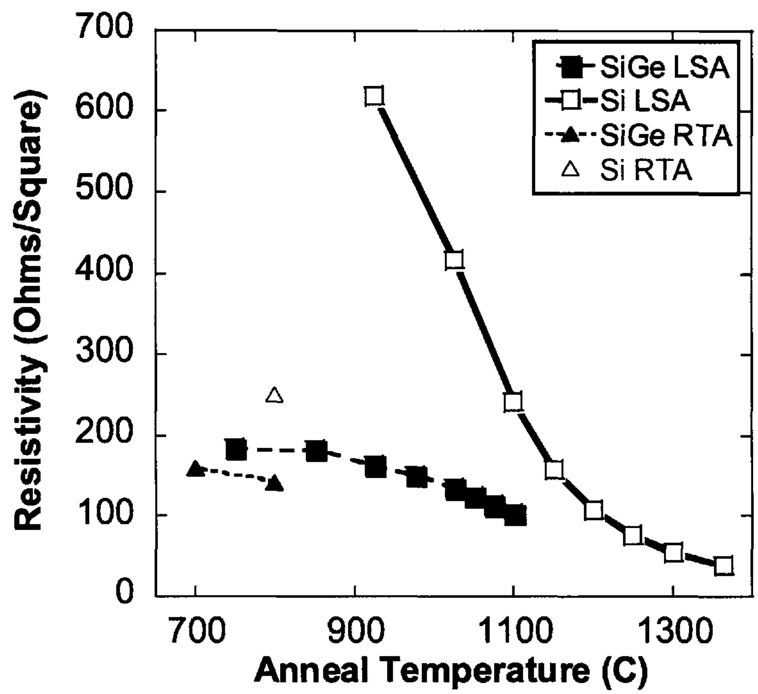


Figure 6-9: Source/Drain sheet resistance vs. anneal conditions for 4x10^{15} cm^{-2} 10keV boron implant measured on a 100 μm x 100 μm Van der Pauw structure.

explains the difference in leakage seen between the RTA and lower temperature LSA anneals.

It is believed that defects and dislocations are formed in the strained SiGe channel layer and relaxed SiGe substrate during the SD implant. During the 10 second RTA, at temperatures as low as 700°C, the defects grow and extend under the SD-gate overlap region causing a significant increase in off-state leakage. This leakage can be avoided by using LSA with temperatures up to 925°C where the shorter anneal time (800μsec) is not long enough for the implant damage to extend to the SD-gate overlap region.

6.4 Boron activation dependence on LSA temperature

The sheet resistance, R_{sh} of a 4x10^{15} cm^{-2} 10 keV boron implant was measured for different LSA and RTA anneal temperatures. The anneal temperature quoted is the temperature that a Si wafer surface would reach under the laser annealing conditions, and may be different for the Si and SiGe wafers. At the same laser fluence, the SiGe sample may be hotter than the Si sample due to the reduced thermal conductivity of the SiGe substrate. Measured R_{sh} for the SiGe heterostructure and Si control samples are shown in Figure 6-9. Boron diffusion decreases with increasing Ge fraction [91]. For the short anneal times employed in LSA there should be very little diffusion and so the R_{sh} should be representative of the dopant activation, although there may be some diffusion and hence deeper junction depth for the RTA anneals. R_{sh} is very low in the SiGe heterostructures compared to the Si control wafer, especially at low anneal temperatures [92]. R_{sh} in Si is lower only for the highest temperature anneals which are above the melting point of $Si_{0.3}Ge_{0.7}$.

6.5 Chapter Summary

Sub-melt temperature laser spike annealing has been investigated as a low thermal budget solution for high Ge concentration Strained Si/ Strained SiGe p-MOSFETs. Laser anneal temperatures of ~1000°C have been demonstrated without degradation to hole mobility. This temperature is significantly higher than possible with RTA, due to device degradation associated with Ge diffusion. For LSA temperatures above 1000°C mobility is found to decrease dramatically. SIMS analysis shows very little Ge diffusion, even for an 1100°C anneal. C-V analysis and Raman spectroscopy suggest that there is some strain relaxation for the 1100°C anneal. XTEM analysis identified localized strain variation and defect densities on the order of 10^7 cm^{-2} for the sample subject to LSA at 1100°C. The mobility degradation for LSA temperatures above 1000°C is due to a combination of strain relaxation and scattering from defects.

It is important to note that the 13 nm-thick channel is well above the equilibrium critical thickness of 7 nm for strained $Si_{0.3}Ge_{0.7}$ on relaxed $Si_{0.7}Ge_{0.3}$. For super critical thickness strained SiGe channels, increased leakage due to implant damage is found at the source drain edge for RTA anneal temperatures in the range of 700 to 800°C. This leakage is not observed for LSA devices with anneal temperatures up to 925°C.

Good Boron activation in the SiGe heterostructure is achieved with LSA. This study demonstrates LSA as a promising solution for the thermal budget constraints in high Ge % MOSFETs. The abrupt profiles and high dopant activation achievable with LSA make it suitable for future scaling of these high-mobility devices.

Chapter 7

Summary and Suggestion for Future Work

The goal of this thesis, outlined in chapter 1, was to address some of the fundamental and technological challenges that must be faced in order to incorporate SiGe channel materials in conventional bulk Si CMOS. The understanding of the design space for the SiGe heterostructure is essential for optimization of device performance.

As we saw in Figure 1-1, the heterostructure design and process constraints all impact the electrical properties of the device and must be taken into account when trying to optimize device performance. Improving one metric of device performance through device design, e.g. mobility, can lead to degradation in another performance metric, e.g. off-state leakage. Therefore, the design trade-off is a more valid way to evaluate the design space for SiGe heterostructures.

The important results from this thesis will be reviewed in this chapter from the point of view of the design trade-offs. The contributions of this thesis and suggestions for future work will also be covered in this chapter.

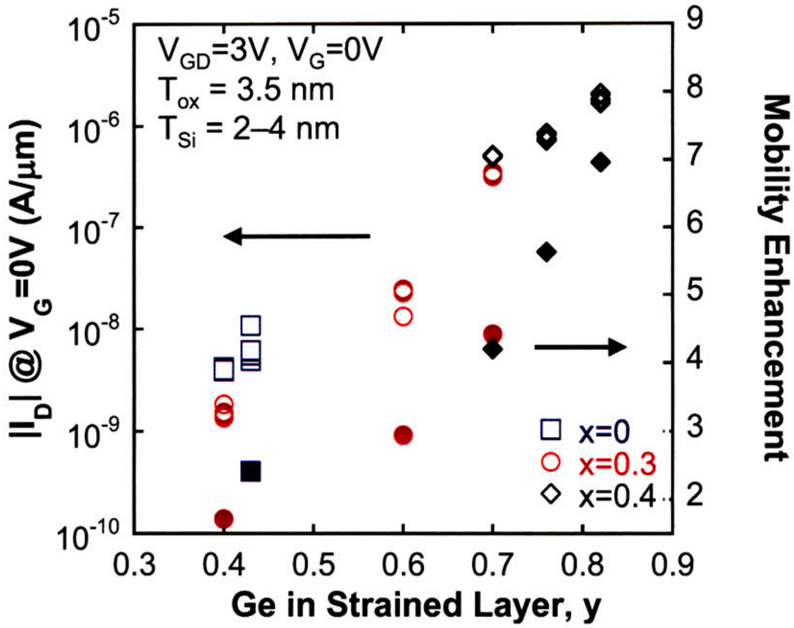


Figure 7-1: Off-state leakage for dual channel heterostructures on y1 axis as a function of Ge fraction in the relaxed buffer layer, x, and in the strained SiGe channel, y. V_{GD}=3V, V_G=0V. Hole mobility enhancement relative to Si control device at N_{inv} of 5 x 10^{12} on y2 axis. Linear increase in mobility enhancement results in an exponential increase in leakage.

7.1 Summary of Heterostructure and Thermal Budget Design Trade-offs

The key design trade-offs addressed by this thesis will be reviewed in this section. The purpose of introducing SiGe channels is to improve the hole mobility. As was demonstrated in Section 4.3, higher Ge composition in the strained channel leads to higher mobility. Therefore, the trade-offs covered in this section all relate to the negative impact of increasing the Ge composition in the SiGe heterostructure, with the positive impact of increased mobility.

7.1.1 Mobility vs. Leakage

The most obvious trade-off for increasing mobility is the accompanying increase in off-state leakage. This is clearly shown in Figure 7-1. The off-state leakage is found to increase exponentially with increasing Ge composition in the strained SiGe channel

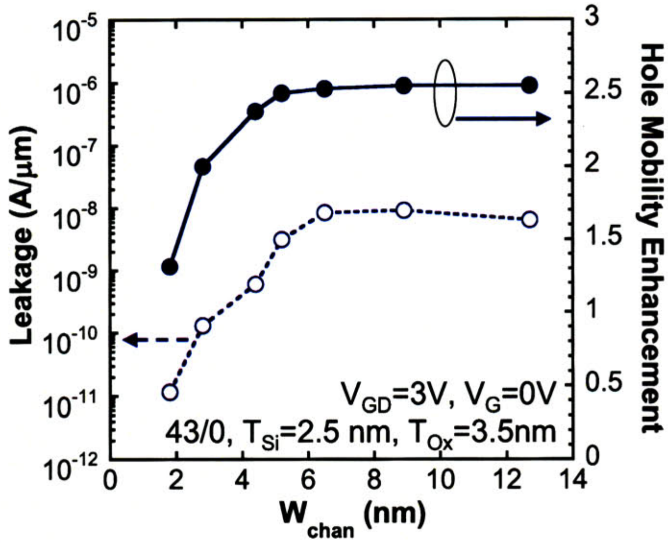


Figure 7-2: Off-state leakage for strained $Si_{0.57}Ge_{0.43}$ on bulk Si as a function of channel thickness, W_{chan}, y. V_{GD}=3V, V_G=0V. Hole mobility enhancement relative to Si control device at N_{inv} of 10^{13} on y2 axis.

(open symbols on y1-axis). The mobility enhancement on the other hand increases linearly with increasing Ge composition (closed symbols on y2-axis). The increased leakage is due to the decreasing bandgap that occurs with increasing Ge composition leading to enhanced BBT. The leakage was found to occur at the SD-gate overlap region in the form of GIDL and is expected to occur at the SD-halo junction in state of the art devices.

The electric field and the bandgap are the fundamental parameters that determine the level of BBT. It was shown in Chapter 5 that lowering the doping in the SD-gate overlap region can help reduce leakage through reduction of the elecric field. This can come at the expense of increased SD series resistance. Defects introduced through implantation can cause the leakage to increase, especially to strained SiGe channels above the critical thickness. There is also some indication that leakage can be reduced by thinning the strained SiGe to a point where quantum confinement results in an increase in the effective bandgap. However, this also comes at the price of decreased mobility due to increased phonon and interface roughness scattering, as illustrated in Figure 7-2.

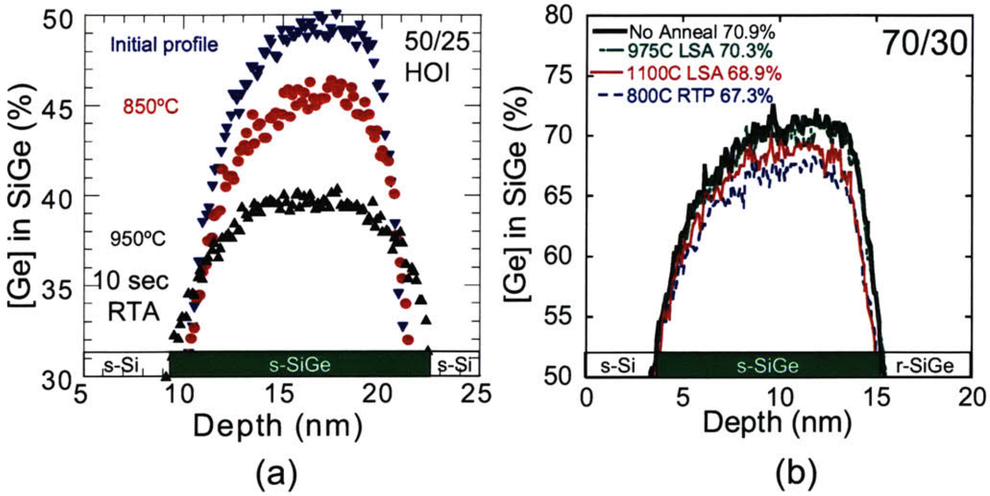


Figure 7-3: SIMS profiles of the strained SiGe layer in (a) 50/25 HOI structure [85] for a 10sec RTA and (b) 70/30 bulk structure with 800μs LSA or 10sec RTA. Si-Ge interdiffusion can be significantly reduced by using LSA compared to RTA technology, even at 1100°C

An increase in leakage for SiGe heterostructures compared to a bulk Si device is unavoidable due to the smaller band gap material. However, the leakage can be minimized by careful optimization of the SD doping profile to engineer the peak electric fields away from the lowest bandgap material.

7.1.2 Thermal Budget vs. Ge Fraction

Even relatively low thermal budgets (by conventional Si CMOS standards) can result in a high level of Si-Ge inter-diffusion. This can be seen from the work of Åberg *et. al.* [85] shown in Figure 7-3 (a). For a 10 sec 800°C RTA there is a drop of 10 at. % in the peak Ge composition as well as a widening of the strained SiGe channel for a strained $Si_{0.5}Ge_{0.5}$ channel pseudomorphically strained to a relaxed $Si_{0.75}Ge_{0.25}$ layer. Ge diffusion causes the peak Ge concentration in the strained SiGe channel to drop and can result in Ge related traps at the Strained Si/ gate dielectric interface, both of which degrade the channel mobility. Diffusivity increases exponentially with Ge fraction and strain [86]. Figure 7-3 (b) shows SIMS profiles for the strained $Si_{0.3}Ge_{0.7}$ layer in MOSFETs fabricated in this work. There is very little Ge outdiffusion, even for the 1100°C laser anneal, compared to reduction of 4 at. % Ge for the 800°C RTA.

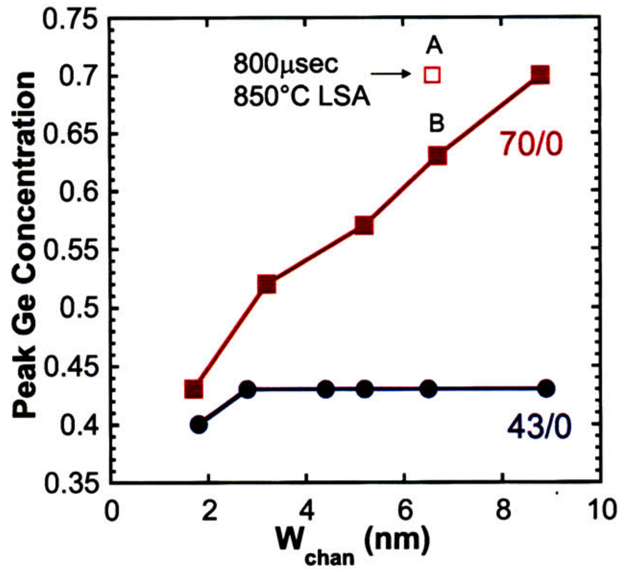


Figure 7-4: Peak Ge fraction in a strained SiGe layer grown pseudomorphically on a bulk Si substrate as a function of W_{chan}. Ge composition determined by HR-RBS. Circles represent strained channel grown nominally at 43 at. % and squares represent strained channel grown nominally at 70 at. %. All structures received a 10sec RTA at 800°C except for the open square which received an 800μsec 850°C LSA. Structures A and B received the same epitaxial growth recipe.

For a very high Ge composition and strain, Si-Ge inter-diffusion can effectively be eliminated by using LSA for SD activation.

The effect of Ge diffusion will have a very significant impact on thin channel strained SiGe heterostructures, as even a small amount of diffusion can have a dramatic effect on the peak Ge concentration in the strained SiGe channel, especially for the high Ge compositions required for high mobility enhancement. This effect is demonstrated in Figure 7-4 where the peak Ge composition in a strained $Si_{1-y}Ge_y$ channel (y=0.43, 0.7) grown pseudomorphically on bulk Si is plotted as a function of W_{chan}. All the structures were grown with channel Ge composition of nominally 43 at. % or 70 at. %, and received a 10 sec 800°C SD anneal (except for one which received an 800μsec 850°C LSA). The peak Ge composition is determined by HR-RBS. The strained $Si_{0.57}Ge_{0.43}$ channel maintains its peak Ge concentration at 43 at. % except for the 1.8 nm-thick film. This is in stark contrast to the strained $Si_{0.3}Ge_{0.7}$ channel which displays a monotonic decrease in Ge composition with W_{chan}. The very high Ge concentration and level of strain in these films leads to significantly higher diffusion compared to the 43/0 structure. This illustrates the difficulty in maintaining the peak Ge composition for thin films with conventional annealing techniques. This is especially relevant to strained SiGe on bulk Si where the strain is high, which increases the diffusivity, and the critical thickness limits the maximum channel thickness achievable.

Points A and B in Figure 7-4 had identical starting substrate and processing, except sample A received LSA instead of the RTA for the SD anneal. The structure receiving the LSA, A, maintains the peak Ge composition of 70 at. % compared to a drop to 63 at. % for B which recieved the RTA. Again, this demonstrates LSA as a promising technique for processing high Ge composition/strained SiGe heterostructures.

7.1.3 Mobility vs. Strained SiGe Thickness

The impact of strained channel thickness on mobility is especially important in comparing the benefits of a virtual SiGe substrate to those of a bulk Si substrate. Hole mobility as a function of W_{chan} is plotted in Figure 7-5 for a number of heterostructures. For the 'ideal case' (e.g. 43/0, peak Ge composition maintained in all but the thinnest film, smooth Si/SiGe interface), the mobility drops for W_{chan} below 4 nm due to increased phonon and Si/SiGe interface scattering. The 70/40 structure follows a similar trend, however there is a large drop in Ge concentration for the 3 nm channel. The thermal budget will reduce the final Ge % (and mobility) especially for thinner films, higher Ge fraction and increased strain. For the strained Ge channel heterostructure there is a dramatic drop in mobility for W_{chan} below 6 nm. This is due to the high level of interface roughness on these structures and some drop in the Ge concentration. The interface roughness can be improved significantly by optimizing the growth and processing of the Ge channel heterostructures.

This work suggests that there is a 'mobility critical thickness', below which a large penalty is paid in terms of mobility degradation. This thickness is $\sim$ 4 nm for 43/0 and 70/40 structure $\sim$ 6 nm for Ge structure.

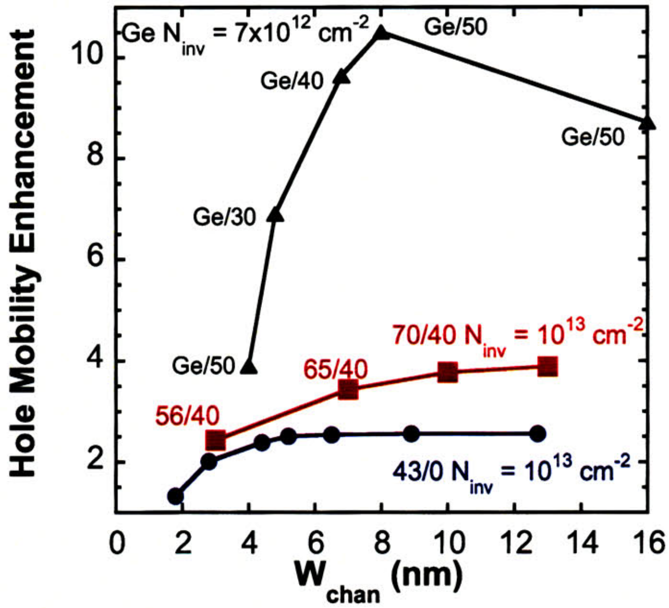


Figure 7-5: Hole mobility enhancement as a function of strained SiGe channel thickness, W_{chan} for strained Ge on a a relaxed SiGe virtual substrate (triangles), strained $Si_{0.3}Ge_{0.7}$ on relaxed $Si_{0.6}Ge_{0.4}$ (squares) and strained $Si_{0.57}Ge_{0.43}$ on bulk Si (circles). There is a drop in mobility for strained SiGe channels for W_{chan} below 4 nm. The decrease in mobility below 6 nm for Ge channels is due to interface roughness, and some drop in Ge fraction.

7.1.4 Mobility and Critical Thickness Constraints

As reviewed in Section 7.1.3 there is a 'mobility critical thickness' for strained SiGe channel heterostructures. The use of a relaxed SiGe virtual substrate avoids the critical thickness constraint by reducing the level of strain in the strained SiGe channel. For strained SiGe channels grown directly on bulk Si, the strain increases with increasing Ge composition. Therefore, the maximum thickness of the channel will depend on the Ge composition of strained SiGe channel. This leads to an optimum Ge content. Increasing the Ge composition above this optimum content does not increase the mobility, due to confinement induced mobility degradation for thin layers.

Mobility enhancements for SiGe heterostructres investigated in this thesis are plotted in Figure 7-6 (a) as a function of Ge fraction in the strained layer for bulk Si and relaxed $Si_{0.6}Ge_{0.4}$ virtual substrate. The equilibrium critical thickness assuming a Si substrate is shown as a function of Ge fraction in the strained layer in Figure 7-6

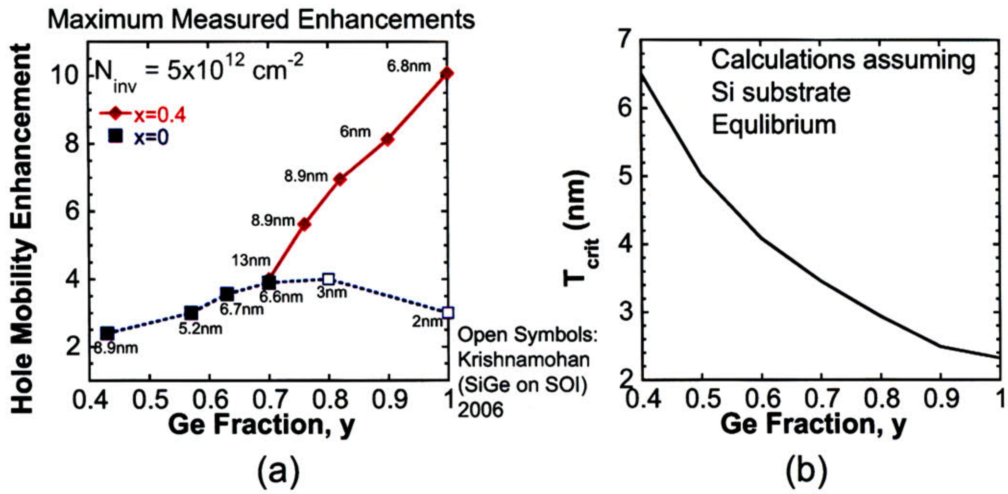


Figure 7-6: (a) Mobility enhancement as a function of Ge fraction for strained SiGe channels grown bulk Si (squares) and relaxed $Si_{0.6}Ge_{0.4}$ virtual substrate (diamonds). Solid symbols: results from this work. Open symbols: [82]. Strained SiGe channel thickness noted for each point. (b) Calculated equilibrium critical thickness for strained SiGe grown on bulk Si as a function of Ge fraction in the strained layer. Calculations courtesy of MK Kim.

(b). When using a virtual substrate, peak mobility enhancements of up to 10X can be achieved with a pure Ge channel. For the relaxed Si substrate the maximum mobility enhancement achievable is $\sim$ 4X at 70% Ge. Above 70% Ge, W_{chan} is reduced due to critical thickness constraints, and no further increase in mobility enhancement is achieved, based on data from Krishamohan *et al.* [82] for SiGe channels on bulk Si. In fact, a decrease in mobility is seen when a pure Ge channel is used on bulk Si, resulting in a mobility enhancement of only 3X compared to 10X achievable without critical thickness constraints.

In summary, peak mobility enhancements of 10X can be obtained for virtual substrate heterostructures. For strained SiGe channels grown on bulk Si substrates, peak mobility enhancement for biaxially strained SiGe is limited to $\sim$ 4X.

7.1.5 Scaling Considerations

A Si cap is required to create a low defect semiconductor-dielectric interface. It was shown in Section 4.2 that the Si cap thickness needs to be minimized in order to confine the carriers to the high mobility strained SiGe channel at high N_{inv}. The Si

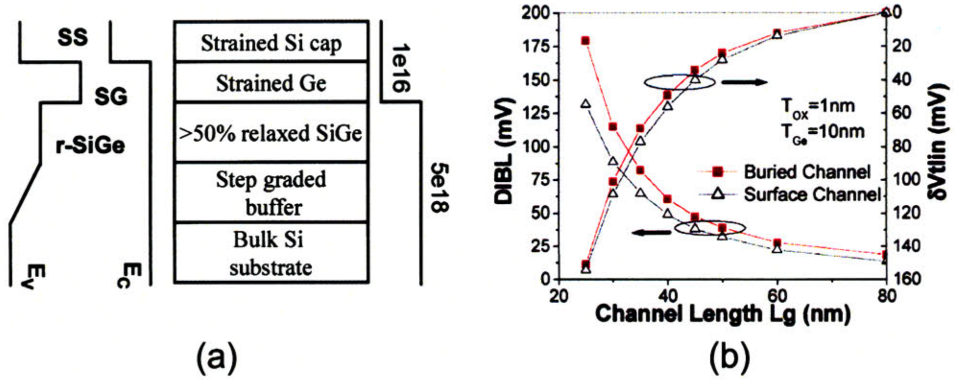


Figure 7-7: (a)Energy band offset, layer structure, and retrograde doping profile of strained Ge channel pMOSFETs used in electro-static simulation. (b) Simulated Vt roll-off and DIBL of strained Ge channel pMOSFET as compared to the Si control with a retrograde doping profile of 1016 and 5x$10^{18}/cm^3$ as shown in (a) with a Si cap thickness of 1.5 nm. Reproduced from [93].

cap acts as a parasitic capacitance in series with the gate oxide, effectively reducing gate control of the channel. This is not a problem for the long channel structures investigated in this study, but for short channel devices the parasitic Si capacitance can result in increased drain induced barrier lowering, DIBL, and increased subthreshold swing, SS.

Scaling has been investigated through simulations by Shang et al. [93] for strained Si/Ge heterostructures as shown in Figure 7-7. For a Si cap thickness of 1.5 nm there is a relatively small degradation in the MOSFET electrostatics, as measured by DIBL and threshold voltage roll off, for channel lengths down to 25 nm. Simulations by Åberg [79] for strained Si/SiGe HOI structures with a 1 nm Si cap show similar results, with comparable performance to a relaxed Si SOI structure for channel lengths down to 20 nm for a body thickness of 6 nm. Therefore, while there is some degradation in electrostatic performance due to the parasitic Si cap for SiGe heterostructure pMOSFETs, it is not a limiting factor for scaling channel lengths down to 20 nm with a Si cap thickness of 1 nm. For scalability below channel lengths of 20 nm, a high-k dielectric that is compatible with SiGe and Ge needs to be found.

7.1.6 Design Trade-off Summary

High mobilities achievable with compressively strained SiGe/Ge channels come at the expense of increased leakage, with an exponential increase in leakage obtained for a linear increase in mobility enhancement. Although off-state leakage is increased, it is expected that acceptable on-to-off current ratios can be obtained by suitable structure engineering, including reducing the SiGe channel thickness, using a bulk Si substrate, and drain profile design.

Due to increased phonon and interface scattering in thin films, it is necessary to keep strained SiGe channel thickness (W_{chan}) above 4 nm, or 6 nm for the Ge channels studied in this thesis. Further work is required to optimize Ge channel heterostructure growth.

For strained SiGe channels grown on bulk Si substrates, peak mobility enhancements up to ~4X have been demonstrated (70% Ge). The large bandgap in the Si substrate leads to lower diode leakage. This type of structure is relatively straightforward to integrate in mainstream CMOS processing.

When using a relaxed SiGe virtual substrate, hole mobility enhancements up to 10X can be achieved. The smaller bangap of relaxed SiGe compared to bulk Si leads to higher diode leakage. These structures are more difficult to integrate into mainstream CMOS than the fully pseudomorphic structures. For currently available technology there is a threading dislocation density of $\sim 10^4 cm^{-2}$ in virtual substrates.

The results presented in this work pertain to biaxial strained channels. However, there is an indication that mobility enhancements can be increased still further with the introduction of uniaxial strain in SiGe which reduces the in plane effective mass, as demonstrated for the 70/0 structure, where enhancements of 6X were shown in Section 4.7.3 (compared to 4X for the biaxial strained case).

7.2 Contributions

The major contributions from this work are listed below.

1. Determination of $\triangle E_V$ for a wide range of Ge fractions and strain.

2. Demonstration of mobility and leakage for long-channel heterostructure p-MOSFETs for strained SiGe compositions from 40% Ge up to pure Ge.

3. Determination of the physics limiting mobility in ultra thin (< 6 nm) SiGe channels.

4. Investigation of laser spike annealing as a low thermal budget processing solution for strained SiGe heterostructures.

5. Illustration of the trade off between mobility and off-state leakage.

6. Suggestions for optimizing the heterostructure p-MOSFET layer design.

7. Demonstration of the highest hole to date mobility for a strained SiGe channel heterostructure grown on bulk Si (6X enhancement for 70/0 structure relative to Si control devices).

7.3 Suggestions for future work

Suggestions for future work are listed below.

1. From the work presented in Section 4.7.3, there is some indication that hole mobility in SiGe channel heterostructures can be increased further by the introduction of uniaxial strain in the <110> direction compared to biaxially strained SiGe. Further work is required to understand the possibilities for hole mobility with uniaxial strain. This can be investigated initially by introduction of mechanical strain using a bending apparatus on biaxially strained SiGe channels. The maximum amount of strain achievable through this method is quite small. In order to maximize the uniaxial strain component, it would be interesting to investigate the effect of patterning of the SiGe heterostructure to induce the biaxially strained SiGe to relax uniaxially as demonstrated by Irisawa *et al.* [94].

Such studies should be performed for the strained channels with Ge contents up to pure Ge.

2. The best mobilities to date have been shown for SiGe heterostructures with pure Ge channels. However, the performance degrades quite rapidly for channel thickness below 7 nm due to non-ideal epitaxial growth. More work is required to understand the fundamental limitations of mobility as a function of channel thickness for Ge channels compared to the $Si_{0.57}Ge_{0.43}$ channels investigated in Section 4.5.2.

3. Thermal budget constraints have been shown to be a limiting factor for high Ge composition channels. This poses a very significant hurdle for introducing high mobility SiGe channels into a mainstream CMOS process. The thermal budget is minimized for the fabrication process of the devices in this study. However, these low temperatures are not compatible with current CMOS processing. Work is required to determine the optimum structure for integration with CMOS which maximizes mobility enhancements and device performance with a realistic thermal budget. This will include a more detailed investigation of LSA as a low thermal budget solution.

4. The exponential increase in leakage with increasing Ge composition in the strained SiGe channel is a significant issue for strained SiGe heterostructures. In order to minimize the leakage in these structures, careful channel and SD engineering are required. Due to the complexity of the structures, present simulations do not reproduce the leakage very well. Work is required to obtain accurate simulations with more physically robust models of BBT for these structures in order to determine ultimate limitations of these devices and optimize performance.

5. While mobility is relevant to long channel devices it is the injection velocity at the source that determines the performance of short channel structures. Strained SiGe channels need to be investigated in short channel structures to

determine how much of the long channel mobility enhancement can be converted to on current enhancement in short channel structures. This also entails finding a suitable low series resistance SD/silicide.

Appendix A

Device Fabrication Process Flow

A.1 Standard Flow

A. Field Oxide			
1	RCA	RCA/ICL	Piranha (5min) +50:1HF 15sec + SC2 5min
2	LTO (ILD) depo.	6C/ ICL	Rec: 400 53A spike FF= 55min Texp=3200A
5	Coat PR on front side for poly wafers	Coater6/ ICL	T1HMDS
6	BOE dip backside	BOE /ICL	2min Remove LTO from backside
8	Remove PR by Piranha	Premetal /ICL	Bluepirnah only(10m)
3	Coat PR	Coater6/ ICL	(3000rpm) T1HMDS
4	Pattern Active	I-stepper /ICL	CAIT-ACT CAIT-DUMA for metrology die
5	Develop PR	Coater6/ ICL	Develop - DEV6 Reflow 1min 170C- T2BK170

6	Etch Field oxide (leave 500A)	AME5000 /ICL	Recipe: Caitfox (based on hasanfox)
7	Ashing PR after field etch	Asher ICL	3min
8	Wafer inspect	Scope ICL	
9	10min green piranha		
10	Remove 500A ox 50:1 HF	Premetal /ICL	1min40 in HF (depends on etch rate)
B. Gate Oxide Stack			
1	RCA	RCA/ICL	Piranha (5min) +50:1HF 15sec + SC2 5min
2	Gate oxide	5D/ICL	600C WET 5D FF:3hours 35min Total=6hrs
2 Alternativ	Low temp Gox	6C - LTO ICL	LTO Gate1 75A 6min dep 3hrs52min total
3	Deposit n+ poly	6A /ICL	560'C Dep FF=1hr45min40sec Texp=1500A, Total=4hr45min
4	Coat PR on front side for poly wafers	Coater6/ ICL	T1HMDS
5	Etch poly backside	LAM490 /ICL	Timed to remove Poly and gate oxide
5 -optional	BOE dip backside	or AME BOE /ICL	CAIT PE (ep recipe) 15sec Remove poly native oxide
6 6a	Etch undoped poly from backside	LAM or AME	2-4 min CAIT BS CLEAR 200sec (~40A/sec)
7	Remove PR by Piranha	Premetal /ICL	Bluepirnah only(10m)
8 (optional)	Ashing PR after BE etch	Asher ICL	3min
9	Coat PR	Coater6/ ICL	(3000rpm) T1HMDS
10	Pattern Gate	I-stepper /ICL	CAIT-PLY1

11	Develop PR	Coater6/ ICL	DEV6
12	Etch gate poly	AME5000 /ICL	Poly etch: Cait OX BT Cait Soft PE
13	Send wafers for SD implant.	Innovion	4e15 10keV 10' Boron
14	Receive back wafers for main wafers	Vendor	
15	Piranha	Premetal/ ICL	Blue(10min)
16	Asher	Matrix/ ICL	3mins
17	Piranha	Premetal/ ICL	Green 10min
C. ILD stack/LTO backside removal for RTP			
1	RCA	RCA/ ICL	5minPiranha + 5sec 50:1 HF SC2 5min
2	LTO (ILD) depo.	6C/ ICL	Rec: 400 53A min FF= 1hour 40min Texp=5000 Recipe: LTO 400C 53A spk
3	Coat PR on front side	Coater6/ ICL	Protect (130'C bake)
4	BOE dip backside	BOE /ICL	Remove LTO from back
5	Piranha Remove PR	Premetal/ ICL ICL	Blue(10min)
6	RCA	RCA/ ICL	Std: SC1 10min 30sec HF SC2 15min
7	RTP	RTP/ ICL	Temp to be decided
D. Contact			
1	CONT pattern	iStepper /ICL	E=160 F=0
2	CONT etching (DRY)	AME5000 /ICL	Leave 1000A
3	CONT etching (wet)	BOE /ICL	Timed using Dummy Remove 2000A
4	Ashing PR		

5	Premetal	Premetal	5min Green Piranha
	cleaning	/ICL	15sec 50:1
6	Sinter	TRL	500C 30mins - H2/N2 flow at 75%
E. Metal Pattern and sinter			
1	Premetal cleaning	Premetal /ICL	5min Green Piranha 15sec 50:1
2	Metal depostion	Endura /ICL	1000A Ti 1um Al
3	Metal pattern	iStepper /ICL	
4	Metal etch wet or dry	Acidhood /TRL or Rainbow/ ICL	Pan Etch (45'C 1min) With DI rinse
5	PR ashing before sinter	ICL asher /ICL	3min
6	Sinter	A3-Sinter	450'C 30mins

A.2 Spacer Flow

The process flow for the spacer process is the same as the standard flow shown in the previous section with the following steps inserted between steps 12 and 13 in module B, the gate oxide stack.

A. LDD			
1	Send wafers for LDD implant.	Innovion	Boron 10keV 7e13
2	Receive back wafers for main wafers	Vendor	
3	Piranha	Premetal/ ICL	Blue(10min)
4	Asher	Matrix/ ICL	3mins
5	Piranha	Premetal/ ICL	Green 10min
B. Spacer			
1	RCA	RCA/ ICL	Piranha + 5sec 50:1 HF SC2 5min Rec: 400 45A min
2	LTO (ILD) depo.	6C/ ICL	Texp=1500A
3	Etch spacer	AME5000 /ICL	CAIT SPCR (Timed etch - leave ~150A on the wafer)
4	50:1 HF dip	Piranha bench ICL	Timed etch (must do etch rate) Remove 150A

Appendix B

Phonon Limited Mobility Dependence on W_{fi}

Acoustic phonon limited mobility should scale linearly with W_{fi} due to confinement as discussed in Section 4.5.2, where W_{fi} is the effective width of the quantum well. It can be seen from Figure B-1 that the phonon limited mobility, μ_{ph}, does not scale linearly with the channel width. However, $W_{fi} \neq W_{chan}$. There are a number of reasons for this. The penetration of the wavefunction outside the channel due to the finite nature of the energy barrier makes the well appear wider than a well with an infinite barrier. For thicker channels, the application of a vertical electric field forms a triangular well, confining the carriers to a region smaller than the actual channel width.

As a reminder of the relevant equations, the scattering rate in a 2-D quantum well is given by

$$\frac{1}{\tau_{fi}} = \frac{\pi D_A^2 k_B T_L}{\hbar c_l} \frac{1}{W_{fi}} g_{2Df}(E) \tag{B.1}$$

where W_{fi} is the effective width of the channel and is given by

$$\frac{1}{W_{fi}} = \int_{-\infty}^{+\infty} |F_f(z)|^2 |F_i(z)|^2 dz \tag{B.2}$$

F(z) is the hole envelope function where f and i represent the final and initial scattering

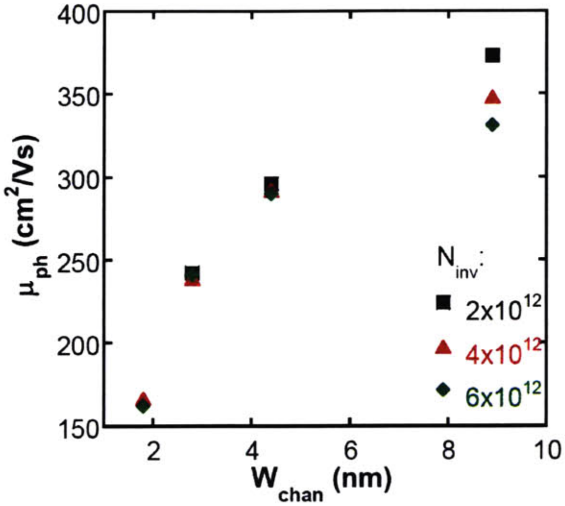


Figure B-1: Phonon limited mobility as a function of W_{chan} at 298K.

states, where

$$\int_{-\infty}^{+\infty} |F(z)|^2 dz = 1 \tag{B.3}$$

i.e. the probability of finding the particle within the envelope function is 1. $|F(z)|^2$ can be approximated by using the hole distribution determined by simulation (see Section 4.5.2). The simulated hole distribution is the un-normalized average $|F(z)|^2$ for all carriers in the quantum well. Whilst this is an approximation, due to the large band splitting induced by strain the vast majority of the carriers are in the heavy hole band and so its a valid approximation to make.

W_{fi} was calculate from the hole distribution from 1-D Schrödinger-poisson simulation. W_{fi} versus μ_{ph} is plotted in Figure B-2 for a number of W_{chan} and N_{inv}. W_{fi} does scale linearly with μ_{ph} for channel thickness from 2.8 nm to 8.9 nm. As expected from the mobility dependence on N_{inv} discussed in Section 4.5.2, W_{fi} does not vary with N_{inv} for W_{chan} below 5 nm. However increasing N_{inv}/vertical electric field does cause W_{fi} to decrease for the 8.9 nm channel. The 1.8 nm film does not follow the W_{fi} dependance on mobility shown by the thicker channels. One reason for this is that there is significant penetration of the wave function into the barrier layers compared to the thicker films, which can be seen from Figure 4-10 (c).

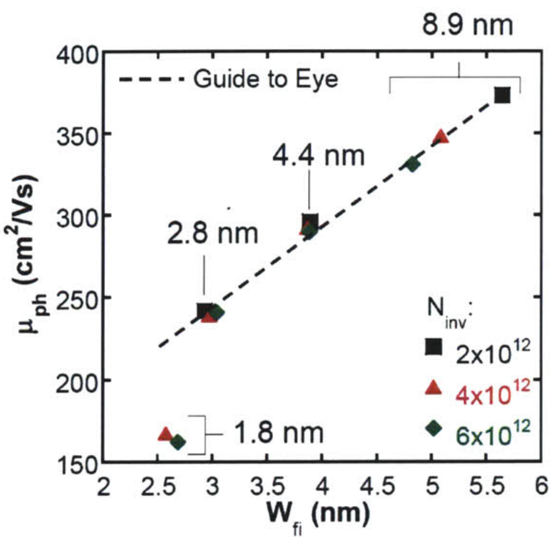


Figure B-2: Phonon limited mobility as a function of W_{fi} at 298K.

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