Photonic Integrated Circuits for Optical Logic Applications

by

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Abstract

The optical logic unit cell is the photonic analog to transistor-transistor logic in electronic devices. Active devices such as InP-based semiconductor optical amplifiers (SOA) emitting at 1550 nm are vertically integrated with passive waveguides using the asymmetric twin waveguide technique and the SOAs are placed in a Mach-Zehnder interferometer (MZI) configuration. By sending in high-intensity pulses, the gain characteristics, phase-shifting, and refractive indices of the SOA can be altered, creating constructive or deconstructive interference at the MZI output. Boolean logic and wavelength conversion can be achieved using this technique, building blocks for optical switching and signal regeneration. The fabrication of these devices is complex and the fabrication of two generations of devices is described in this thesis, including optimization of the mask design, photolithography, etching, and backside processing techniques. Testing and characterization of the active and passive components is also reported, confirming gain and emission at 1550 nm for the SOAs, as well as verifying evanescent coupling between the active and passive waveguides. In addition to the vertical integration of photonic waveguides, Esaki tunnel junctions are investigated for vertical electronic integration. Quantum dot formation and growth via molecular beam epitaxy is investigated for emission at the technologically important wavelength of 1310 nm. The effect of indium incorporation on tunnel junctions is investigated. The tunnel junctions are used to epitaxially link multiple quantum dot active regions in series and lasers are designed, fabricated, and tested.

Thesis Supervisor: Leslie A. Kolodziejski
Title: Professor of Electrical Engineering

Acknowledgements

As I mark this milestone in my education, it only makes sense to begin by thanking the most important educators in my life, my parents. For as long as I can remember, they always emphasized the importance of education, from my very first "Big Book of Knowledge" all the way to this little book of knowledge that I am now writing. Particularly, they always stressed that my education should be measured against my potential, not merely to the standards of a test or a grade. This notion of self-directed learning has proved invaluable in graduate school where grades are of little importance and the real tests are against yourself (and the lab equipment). I can say with confidence that I would not be here today had they not insisted, cajoled, demanded, and finally bribed me with tacos when I refused to learn my multiplication tables in the second grade. From being thrown out of the first grade all the way to MIT, their loving support has been constant. I would also like to thank my brother, Michael, as my oldest and dearest friend. My sister, Shannon, has offered continuing encouragement, inspiration, and companionship.

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seem to know a lot about everything. When I first arrived at MIT he told me, "I don't mind if you break anything as long as you're willing to help fix it," an outlook which has encouraged me to take a hands-on approach to research. Gale, you have been not only a mentor, but a friend.

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CHAPTER 1

Introduction

1.1 Optical Communication

The advent of high quality optical fiber in the 1960s enabled the widespread development of optical telecommunications networks whose growth has accelerated through the present day. The global backbone of optical fiber has not only improved communications but has revolutionized related technologies and enabled far-reaching services. Nearly every industry has experienced increased efficiencies brought about by improved data processing and communication. Computers are no longer freestanding calculators, but integrated members of a global data processing network.

Wide-ranging end-user applications such as World Wide Web surfing, data communications, phone calls using voice-over-internet-protocol (VoIP), video-on-demand, streaming music and others are all leading to an explosion in Internet traffic.

These new applications are extremely bandwidth intensive. As an illustration, consider that the delivery of a single high-definition movie is equivalent to 35,000 web pages. Furthermore, users are spending more time than ever using broadband services. A user study showed that in just a three-year period, average weekly use of broadband connections went from 25.5 hours to 30.5 hours, an increase of nearly an hour a day [1]. Industry reports estimate that data traffic will double every year for the sustainable future [2].

A few key developments led to the widespread availability of this technology. First, the development of single-mode optical fiber in the early 1980s allowed for transmission of optical solitons (pulses) over extremely long distances, enabling practical design of affordable long-haul networks. Secondly, the late 1980s saw laser diodes mature to the point that they could generate the optical data streams at extremely fast modulation rates and at affordable costs. Additionally, the development to erbium-doped fiber amplifiers (EDFAs) allowed for high-power and cost-effective transmission of data without the need for expensive electronic reprocessing [3].

Once enabled, there was tremendous investment in long-haul fiber networks in the 1990s. That is now being followed with increasingly granular fiber networks such as fiber-to-the-premises (FTTP) and fiber-to-the-home (FTTH). The resulting explosion of data services is now reaching maturity and there is nearly ubiquitous access and widespread convergence of voice, data, and video services. All of these technologies depend on and feed into fiber optic networks, with demand for bandwidth growing continually.

The optical fibers themselves have adequate speed and capacity to meet bandwidth demands for the foreseeable future. The fiber infrastructure for long-haul networks has already been widely installed, but these networks have yet to realize their full capacity. One of the key bottlenecks preventing increased data speeds remains the switching technologies that manage and direct network traffic. These nodes are plagued by optical-to-electronic-to-optical (OEO) conversions that greatly reduce the overall speed and efficiency of data transmission. The ideal solution is to make the network entirely optical between end users. The research presented in this thesis explores the

development of photonic devices and photonic integrated circuits for the next generation of optical switching technologies.

1.2 Optical Materials

Direct bandgap materials such as indium phosphide (InP) and gallium arsenide (GaAs) have long been known to be efficient emitters of optical photons when electrically or optically pumped. Additionally, their electron mobilities are generally much higher than that of silicon, so they are widely used in applications such as communication devices where high-speed electronics are a necessity. Both GaAs and InP are available in large substrates at moderate prices, making them attractive candidates for both photonic devices, electronic devices, and hybrids of the two.

Compositional grading of two or more materials allows for extremely precise control over the emission wavelength. By combining one or more binary compounds (e.g GaAs, InP, GaSb), it is possible to create ternary (e.g. $In_xGa_{1-x}As$), quaternary (e.g $In_xGa_{1-x}As_yP_{1-y}$), and even quintary compounds (e.g GaInNAsSb). In a three-dimensional bulk form, these materials are limited to emission at a characteristic wavelength corresponding to their bandgap energy. Reduced dimensionality forms of the material such as quantum wells and, more recently, quantum dots allow the emission wavelength to be even more precisely tailored. Quantum dots have unique carrier dynamic behavior that benefits high-speed operation and also allow the emission wavelength to be extended to 1310 nm on GaAs substrates.

In this study, all material growth was done using molecular beam epitaxy, which allows for precise control over the atomic compositions and monolayer control over the material thickness.

1.3 Vertical Integration

Traditionally, integration of photonic components has focused on lateral integration within a single plane at the surface of the substrate. For example, a laser and a waveguide would be constructed so that they are coplanar, with the laser's

emission laterally coupling into the waveguide. The relatively large size of most photonic components limits the amount of two-dimensional integration that can be achieved by more densely packing components, as has been successfully done with electronic integrated circuits by constantly shrinking successive photolithography generations.

The work in this thesis examines vertical integration of photonic components, where devices are constructed on more than one plane, breaking into the third dimension. Vertical integration allows greater freedom of the design and optimization of each component layer. Furthermore, the fabrication of each layer has greater independence, yet the final device still operates as an integrated whole. In this study, the asymmetric twin-waveguide configuration is used to vertically integrate semiconductor optical amplifiers on top of passive waveguides. This structure effectively transfers optical power between the two layers, but does not address the issue of electronic integration in the vertical direction. Towards this end, Esaki tunnel junctions are explored as a device for cascading electrical current between vertically integrated active devices. These two techniques form the basis for more complex vertically integrated photonic structures, allowing for the construction of three-dimensional photonic integrated circuits and devices.

1.4 Thesis Organization

Chapter 2 covers tunnel junctions and tunnel-junction-coupled quantum dot lasers. Tunnel-junction-coupled quantum dot lasers are one or more semiconductor active regions placed in epitaxial series. Reverse-biased Esaki tunnel junctions enable the cascading of electrons between the active regions. As implemented, tunnel junctions allow electrons to emit a photon via a conduction band to valence band transition and then tunnel to the conduction band of the next active region. Therefore, a single electron can emit multiple photons by cascading from active region to active region and allowing for quantum efficiencies greater than unity. The effect of indium incorporation on the tunnel junctions is also examined.

Chapter 3 examines semiconductor optical amplifiers (SOA) and their implementation in optical logic structures. When SOAs are arranged in a Mach-Zehnder

interferometer configuration, Boolean logic functions can be implemented. Furthermore, the SOAs are vertically integrated with passive waveguide interconnects using an asymmetric twin waveguide configuration. The fabrication of these devices is complex and optimization of the various process steps is explored, particularly the effects of various processing steps on the waveguide roughness.

Chapter 4 explores future directions for both areas of research, including 1550 nm quantum dot lasers and more advanced optical logic structures. The combination of 1550 nm quantum dots with asymmetric twin waveguide optical logic devices is proposed for ultrafast optical switching in excess of 200 Gbit/s and increased vertical integration is explored. The appendices in Chapter 5 provide additional detail on the fabrication sequence, device layout, and other relevant information.

1.5 References

1. Herring, H.B., With Broadband, the PC's Siren Call is Tough to Resist, in The New York Times. 2006: New York.
2. Coffman, K.G. and A.M. Odlyzko, Growth of the Internet, in Optical Fiber Telecommunications IV B: Systems and Impairments, I. Kaminow and T. Li, Editors. 2002, Academic: New York. p. 17-56.
3. Poole, S., et al., Fabrication and characterization of low-loss optical fibers containing rare-earth ions. Lightwave Technology, Journal of, 1986. 4(7): p. 870-876.

CHAPTER 2

Quantum Dot Lasers

2.1 Tunnel-Junction-Coupled Quantum Dot Lasers

Semiconductor lasers have seen rapid development in the past two decades, which has resulted in their widespread implementation in large-scale fiber optic networks as data transmitters. State of the art lasers today are capable of high intensities, narrow spectral linewidths, and high modulation speeds. The availability of reliable, powerful, yet compact, semiconductor lasers has been one of the key enablers in the enormous expansion in network capacity seen in the past twenty years.

The fundamental materials properties of silica fibers dictate that the associated lasers must operate in one of two primary wavelength windows for optimal network performance (Figure 2-1). 1310 and 1550 nm are the dispersion and attenuation

minima, respectively, for optical fibers. Although new fiber designs and materials such as photonic bandgap fibers [1, 2] and low-OH- fibers [3] can eliminate these wavelength restrictions, the widely installed and enormously expensive silica fiber base guarantees that these wavelengths will be technologically important for years to come. Semiconductor lasers are particularly attractive optical emitters due to their small size, high gain, and electronic compatibility. However, the properties of the optical fibers constrain the choice to a relatively small subset of materials systems, primarily the III-V semiconductor family. Economic considerations further constrain the list of available materials systems to two sets, gallium arsenide (GaAs)-based and indium phosphide (InP)-based systems, as these two materials are by far the most widely available and cost-effective III-V substrate materials. Only these two systems have associated technologies that are sufficiently well developed to allow for commercial production at an economically viable scale. GaAs devices are now being manufactured on wafers as large as 150 mm and electronic devices such as heterojunction bipolar transistors are ubiquitous in consumer electronics such as cellular phones. Now available in 2" and 4" wafers, InP is increasingly becoming an important material in radio-frequency (RF) and high-speed electronics, in addition to its unchallenged position as the dominant materials system for infrared emitters and lasers.

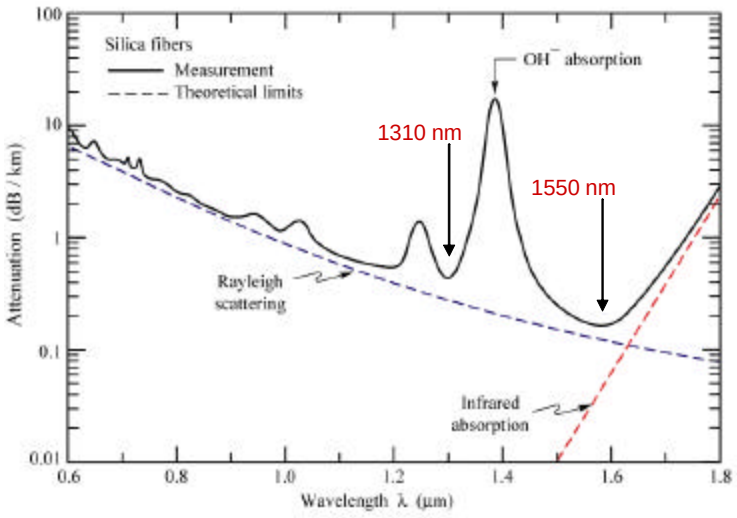


Figure 2-1: The absorption spectra of silica fiber. The attenuation minimum occurs at 1550 nm while the dispersion minimum occurs at 1310 nm [4].

Of these two, the GaAs system has substantial cost benefits over InP making it desirable to produce semiconductor lasers which operate in the infrared regime on this substrate. However, for a long time there was no bulk material that is both epitaxially compatible with GaAs and which can simultaneously emit in the 1310 nm window. Epitaxial constraints are paramount in semiconductor lasers because they have traditionally dictated the choice of materials that can be integrated with the semiconductor substrate. Until quite recently, only bulk material or strained quantum wells could be epitaxially grown on semiconductor substrates. Theoretical work in the 1980s [5-7] and experimental work in the 1990s [8-11] has led to the development of quantum dots. These small clusters of semiconductor material, generally indium arsenide (InAs), have simultaneously satisfied the requirements of 1310 nm emission and epitaxial compatibility with GaAs. Quantum dots have further advantages that make them particularly attractive for semiconductor lasers.

Aside from semiconductor lasers emitting in the infrared region of the spectrum, there is a great interest in making semiconductor lasers with high internal efficiencies for they promise higher output powers with lower threshold currents. Connecting multiple laser diodes in series could potentially yield extremely high internal efficiency lasers. In a series configuration, the same current passing through each diode would stimulate photon emission. In essence, the same electron would yield multiple photons – greater than one hundred percent quantum efficiency. The most effective method of implementing such a series connection would be to connect the lasers within the epitaxial structure. While seemingly simple, one hurdle remains: how to get the electron now in the valence band after the first radiative transition back into the conduction band for a second radiative transition (Figure 2-2). The answer is the Esaki tunnel junction. Prior work, both at MIT [12, 13] and elsewhere [14-17], has already demonstrated this technology in different semiconductor laser structures and at different wavelengths.

The Esaki tunnel junction is a reverse-biased diode which allows carrier tunneling between the valence band and the conduction band [18, 19]. In effect, the reverse bias leakage current normally undesirable in a regular diode is exploited to couple the two laser diodes in series and transport the electron between the valence band and the conduction band.

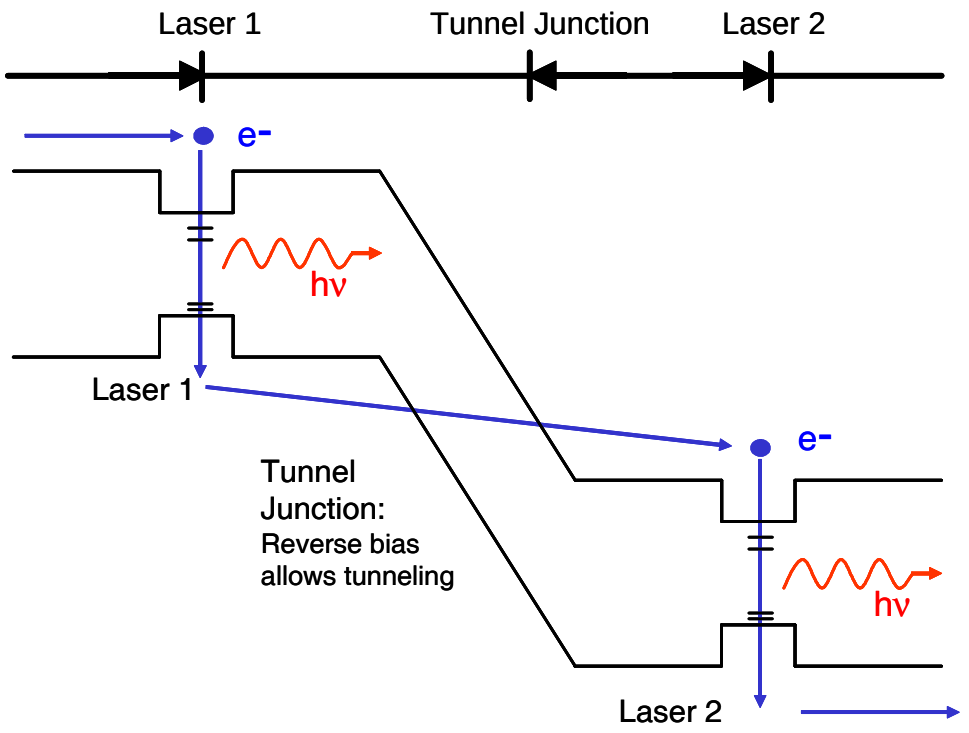


Figure 2-2: Band diagram of the tunnel-junction-coupled laser. The injected electron enters the first laser diode and emits a photon. It then is injected from the valence band of the first laser to the conduction band of the second laser by tunneling through the reverse-biased tunnel junction. In the second laser diode, the electron emits a second photon..

Combining quantum dots and tunnel junctions allows the development of infrared lasers with differential efficiencies exceeding one hundred percent. Placing quantum dots in the active regions and connecting them with tunnel junctions has the potential to create new and exciting laser devices for telecommunications applications.

2.2 Molecular Beam Epitaxy

Essentially a multi-source evaporator, molecular beam epitaxy (MBE) allows a wide range of III-V semiconductor materials to be epitaxially deposited within the same vacuum chamber. Binary, ternary, and even quaternary and quintary semiconductors can be combined in such a manner to produce a wide variety of semiconductor device

structures. By combining materials of different bandgaps, laser structures can be tailored to precisely control the electronic and photonic properties of the device.

2.2.1 Crystallography of III-V Semiconductors

Electronic materials are remarkably sensitive to defects; in fact, impurities at the level of parts per million can have dramatic effects on the material properties. This sensitivity is exploited when impurities are intentionally added to semiconductor materials because this doping allows precise control over the electronic behavior of the semiconductor. However, unwanted impurities can have disastrous effects on electronic behavior and diminish or destroy device performance. Furthermore, aberrations from perfection within the crystal structure can lead to deleterious phenomena in optoelectronic devices such as nonradiative recombination, a process by which electron-hole pairs are annihilated without the emission of the desired photon. Molecular beam epitaxy addresses both of these potential problems, allowing for the deposition of materials that are atomically precise in both composition and crystalline quality.

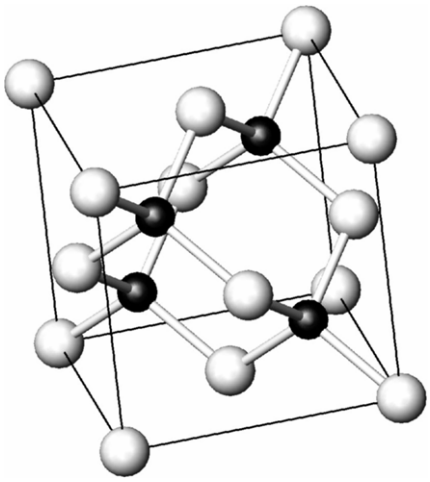


Figure 2-3: The zincblende structure common to most III-V materials such as GaAs, InP, AlAs, and their alloys.

From the Greek *epi* "above" and *taxis* "in ordered manner," epitaxy means that the deposited material exactly mimics the crystalline structure of the underlying

substrate. For this thesis, all of the work was done using the III-V group of materials. These materials generally have a zincblende (ZnS) crystal structure similar to that of crystalline diamond. In the simplest case, the two constituent elements comprising the III-V compound occupy alternate positions in the two interpenetrating face-centered cubic (FCC) sublattices (space group $F\bar{4}3m$), each atomic species having tetrahedral coordination with the other (Figure 2-3). Wafers of the most common materials, GaAs and InP, are generally manufactured so that one of the major crystalline planes, often (100) or (111), corresponds to the top surface of the wafer.

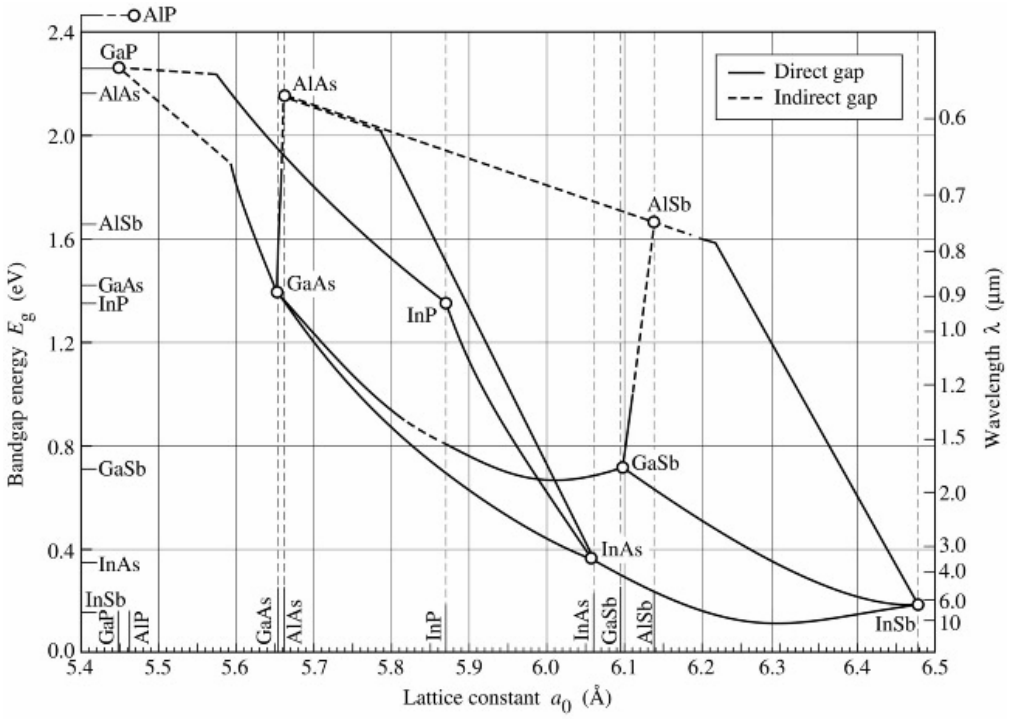


Figure 2-4: Lattice constant and bandgap/emission wavelength of common III-V semiconductors. This diagram is the fundamental basis for all epitaxial growth. Important substrate materials are shown with their lattice constant on the horizontal axis [4].

In Figure 2-4, the lattice constant (distance between atomic unit cells) and bandgap energy of important III-V materials is shown. The black lines in Figure 2-4 correspond to ternary compounds such as $In_xGa_{1-x}As$ and they bound areas that

represent quaternary compounds such as $In_xGa_{1-x}As_yP_{1-y}$. Five and even six constituent compounds are possible, but are difficult to render graphically. In the simple case of a ternary alloy, the lattice constant usually varies linearly with composition according to Vegard's Law [20]. The bandgap variation is given by a more complex quadratic term, as shown by the bowing of the lines. Vertical lines of constant lattice constant represent the epitaxial constraints of growing on a particular substrate.

While epitaxy restrictions generally limit materials growth to materials with the same lattice constant, it is possible to make brief excursions to materials of different lattice constants. When a lattice-mismatched film is grown on a substrate epitaxially, the epilayer is generally restricted in thickness by the Matthews-Blakeslee condition [21-23]. The Matthews-Blakeslee condition, based on a force balance model, represents the thickness limit for a strained film before dislocations begin to form. These dislocations, interruptions in the periodicity of the perfect lattice, are devastating for semiconductor lasers because they serve as nonradiative recombination centers. The critical thickness of a film (h_c) is defined explicitly as:

$$h_c = \frac{1}{2}\frac{a_s\left(1-\frac{1}{4}\nu_L\right)}{e_{ll}(1+\nu_L)p}\left[1+\ln\left(\frac{h_c\sqrt{2}}{a_s}\right)\right] \qquad \textbf{Equation 2-1}$$

where a_s is the unstrained lattice constant of the substrate and a_f is the lattice constant of the epilayer. The strain within the plane ε_{ll} is given by:

$$e_{ll} = \frac{a_s - a_f}{a_f} \qquad \textbf{Equation 2-2}$$

and the Poisson's ratio, ν, is given as:

$$\nu_L = \frac{C_{12}^{film}}{C_{11}^{film} + C_{11}^{sub}} \qquad \textbf{Equation 2-3}$$

where C_{12} and C_{11} are materials properties representing the film and substrate's mechanical behavior. The Matthews-Blakeslee analysis is for that of an epitaxial film, growing by the Frank – Van der Merwe mechanism, extending infinitely in either direction within the plane and growth perpendicular to the plane. Table 2-1 contains values for common semiconductor materials at or near room temperature.

Table 2-1

	GaAs [24]	InP [25]	InAs [26]	GaP [27]
a (Å)	5.65325	5.8687	6.0583	5.4505
C_{11} (dyn/cm^2)	11.90 x 10^{11}	10.11 x 10^{11}	8.34 x 10^{11}	4.05 x 10^{11}
C_{12} (dyn/cm^2)	5.34 x10^{11}	5.61 x 10^{11}	4.54 x 10^{11}	6.20 x 10^{11}
ν_L [100]	0.31	0.36	0.35	0.31

2.2.2 Molecular beams

A schematic of a MBE chamber is shown in Figure 2-5. Within the MBE chamber, individual elements are placed in isolated locations, each with its own independent heating element. When the atoms of a particular element are thermally excited, they vaporize and are collimated to form a linear molecular beam that spreads out in a conical fashion. The overall geometry of the chamber is such that each molecular beam travels linearly from the source and simultaneously overlaps with the other beams at the substrate. The substrate resides on a heating element to provide sufficient thermal energy for the incoming molecules to diffuse on the surface and to find low-energy locations for incorporation. Under ideal conditions, the deposited material will exactly duplicate the crystal structure of the underlying template – epitaxy.

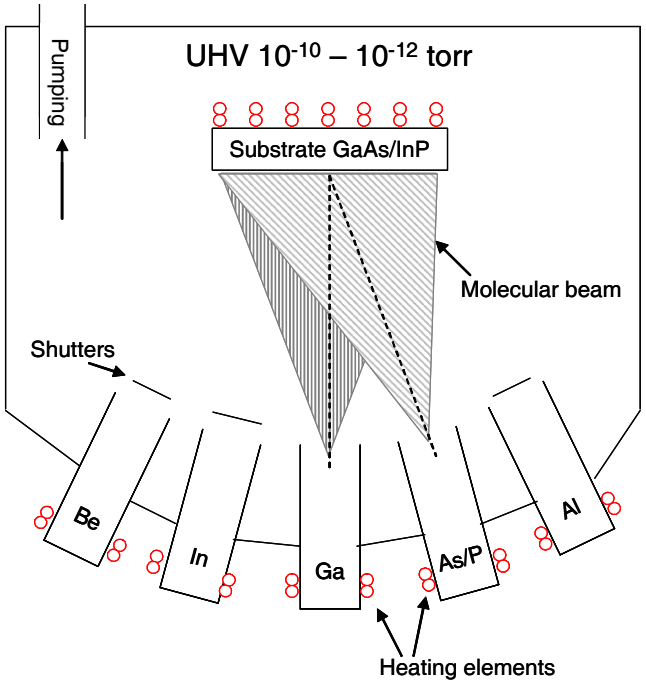


Figure 2-5: A simplified schematic of a molecular beam epitaxy system.

The MBE system that was used is a Riber 32P gas-source MBE (GSMBE). GSMBE is a particular arrangement where the group-V elements, arsenic and phosphorus, are supplied from the gaseous hydride precursors arsine (AsH_3) and phosphine (PH_3), respectively. The group-III elements are high-purity metallic sources, in this case, molten elemental gallium, indium, or aluminum. Doping elements such as beryllium (p-type) and silicon (n-type) are also elemental sources, but they remain in the solid phase at typical operating temperatures.

The effusion cells which hold the group-III elements are made of a refractory ceramic material, pyrolitic boron nitride (PBN), which can withstand the high temperatures and is chemically nonreactive in order to maintain the purity of the molten elements. Typical operating temperatures for these cells range from 600 °C to 1200 °C. Heating the group-III elements to such high temperatures causes the elements to evaporate or sublimate (material dependent) as given by their vapor pressures. By precisely controlling the temperature, the evaporation rate can be changed to alter the

flux arriving at the substrate and therefore the growth rate of the deposited film. After passing through a mass flow controller, the group-V precursors enter a special cell that is designed to "crack" the molecules, that is, to disassociate the hydrogen from the group-V atoms. The cracking is achieved by passing the hydride gas through a series of baffles made of PBN. Upon collision with the high-temperature baffles – the temperature for this work was 900 °C – the gas molecules will undergo a decomposition reaction from AsH_3 into As_2 and H_2 (and PH_3 to P_2, P_4, and H_2) as well as various other species. In GSMBE, the growth rate is primarily determined by the group-III flux with an excess of group-V molecules present as an ambient overpressure.

All of the cells have shutters made of molybdenum that block the molecular beams when they are not needed. By opening and closing the appropriate shutters, layers of different constituents can be deposited in sequence.

2.2.3 Ultra-high Vacuum

MBE deposition occurs in an ultra-high vacuum (UHV) environment. Typical base pressures for a MBE chamber range from 10^{-9} to 10^{-12} torr. From the kinetic theory of gases, an ideal gas of atomic diameter D, at pressure, P, and temperature, T, will have a mean free path, Λ, given by :

$$\Lambda = \frac{kT}{pD_{atom}^2 P\sqrt{2}}$$

Equation 2-4 [28]

In an ultra-high vacuum environment, the mean free path of an atom or molecule can be hundreds or even thousands of meters long. This condition puts particles in the molecular flow regime, where it is assumed that the molecules move independently of each other and rarely collide with each other. The ultra-high vacuum ensures that the elements will travel in a straight line from the sources to the substrate and also minimizes the amount of unwanted impurities that will incorporate into the film.

The ultra-high vacuum condition is achieved using a variety of specially designed pumps and techniques. Foremost is a simple attentiveness to maintaining strict cleanliness any time the vacuum chamber is exposed to atmospheric conditions.

Careful preparations are made to properly degrease and dehydrate any materials that are placed within the chamber. Degreasing typically involves a sequence of trichloroethylene, acetone, methanol, and isopropanol soaks,15 minutes in each solvent and repeating as necessary. Any tool or piece of equipment used in the MBE is dedicated exclusively for the MBE to avoid cross-contamination.

Pumping is achieved using a standard roughing and UHV configuration. Rouging pumps are used to take the MBE chamber from atmospheric pressures to vacuum conditions. UHV pumping is accomplished using a high throughput turbomolecular pump owing to the considerable volume of the vacuum chamber. Alternatively, cryopumps or ion pumps could be used for MBE UHV pumping, but these are capture pumps and are not ideal for GSMBE due to the large volume of cracked gases entering the chamber. All GSMBE pumping equipment is specially designed to tolerate hydride gases and all process effluent are adsorbed in a high-surface area copper oxide scrubber for neutralization and sequestration. The hydride gases, AsH_3 and PH_3, are highly toxic, even at the parts per million levels, so double containment is maintained throughout the system. In addition to the pumping equipment, the GSMBE has a cryoshroud through which liquid nitrogen flows during film deposition. By cooling the chamber's inner surface to cryogenic temperatures, any spurious gases will be incapacitated at the chamber wall and hence will not interfere with film growth. Periodically, and after any venting to atmosphere, the entire chamber is baked in excess of 200°C to drive off water vapor and other volatile species from the chamber walls and into the vacuum pumps. A residual gas analyzer is used to monitor the composition of any constituents remaining in the chamber. The end result of this considerable attention is vacuum conditions below 10^{-10} torr, a better vacuum condition than what is encountered in low-earth orbit.

2.2.4 Epitaxial growth and in-situ monitoring

Once the molecular beams arrive at the substrate, specific conditions are necessary for an epitaxial film to grow. Most importantly, the substrate temperature must be hot enough so that the adatoms have adequate mobility on the surface. The arriving adatoms impinge on the surface randomly; they will not necessarily land in the

correct crystallographic position. With sufficient mobility, the adatom will travel locally on the substrate for many nanometers [29] until it finds an energetically favorable crystallographic site to incorporate. Typical layer-by-layer epitaxial growth is understood to occur by the Frank-van der Merwe mechanism. For simplicity, the growth of GaAs will be considered as a general description of the GSMBE technique.

Before growth begins, the substrate is first baked at low temperature (210 °C) under ultra-high vacuum (~10^{-9} torr) for one hour to drive off any water vapor and other volatile compounds that may be present on the wafer surface. Furthermore, once the substrate is moved in to the UHV MBE reactor, the GaAs wafer must be heated to approximately 600°C to allow for the desorption of the native oxide from the surface. The substrate temperature is monitored using an optical pyrometer and thermocouple. While ramping the substrate temperature to desorb the native oxide, arsenic is introduced into the system. Above ~450°C, GaAs will begin to dissociate and arsenic atoms begin to evaporate from the surface. By keeping the arsenic pressure above the vapor pressure, this undesirable phenomenon can be avoided. The end result of this surface preparation is a substrate surface that is atomically pure in a vacuum chamber with very few impurities that could be incorporated into the film.

Having previously established an ultra-high vacuum environment and by increasing the temperatures of the substrate and effusion cells to their operational values, the epitaxial growth is ready to commence. The ability to monitor the growth *in-situ* is highly desirable and this is generally accomplished using reflection high-energy electron diffraction (RHEED). The UHV conditions as well as the geometry of the MBE chamber are ideal for electron diffraction. Using an electron gun, high-energy (keV) electrons are accelerated towards the sample at a shallow angle, typically a few degrees. The electrons glance off the surface of the growing film and reflect onto a phosphorescent screen. Due to their high energy, the electrons exhibit wavelike behavior, as given by DeBroglie wavelength, and diffract from the surface in a pattern characteristic of the thin film. The resulting diffraction pattern is projected to a phosphorescent screen where it can provide several pieces of useful information. Qualitatively, the sharpness of the diffraction pattern can give a cursory idea of film quality and lattice matching. Most commonly, the RHEED diffraction pattern is used to

monitor film deposition rate. By monitoring the intensity of a single diffracted beam over time, the deposition of individual monolayers can be observed and the growth rate determined. A schematic is shown in Figure 2-6, illustrating how the intensity oscillates as the electrons scatter from the growing surface and interfere with each other. In addition to RHEED oscillations, effusion cell temperatures were re-normalized before every growth using a flux gauge.

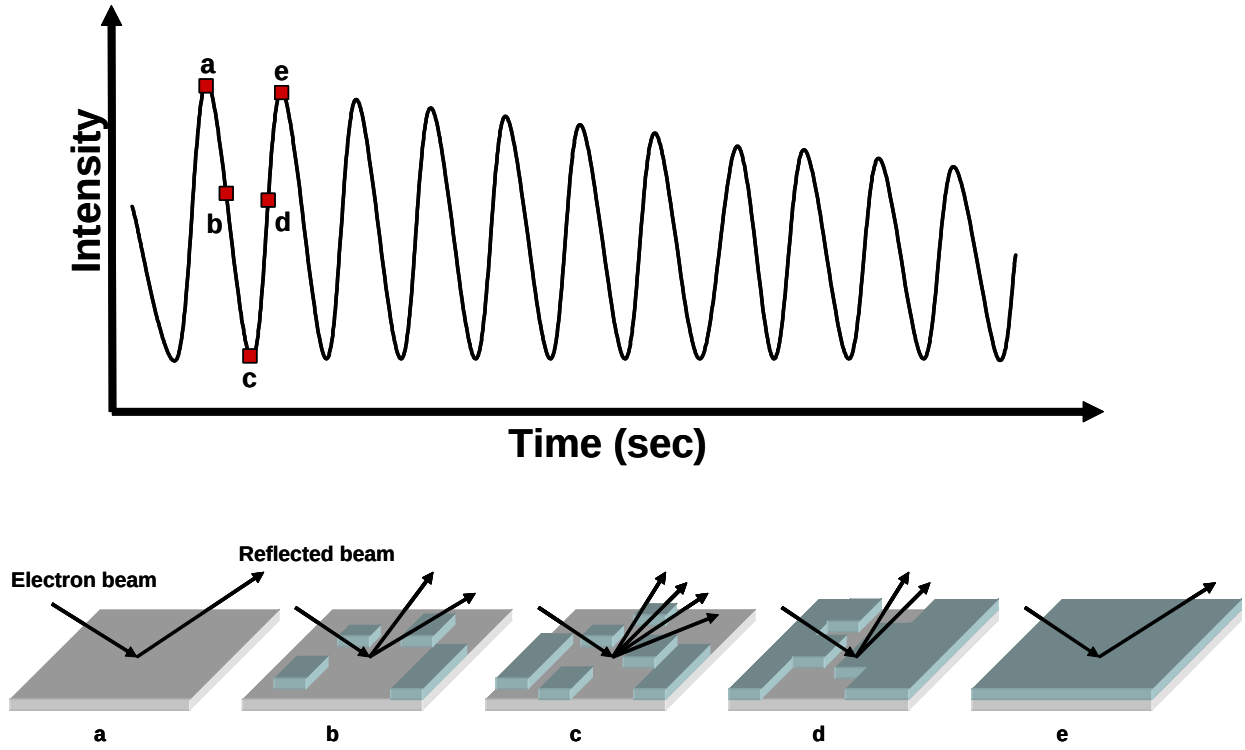


Figure 2-6: Schematic representation of reflection high energy electron diffraction (RHEED). The intensity of the reflected beam varies as each monolayer assembles on the substrate. By monitoring this intensity in time, the growth rate can be calculated.

2.3 Quantum Dots

2.3.1 Extending Infrared Emission on GaAs

In a modern semiconductor laser, at least three different materials are required: the core, cladding, and active regions. GaAs lasers were first designed with bulk GaAs

serving as both the core and active regions with alloys of AlAs and GaAs ($Al_xGa_{1-x}As$) acting as the cladding. The primary drawback of this design is that it restricts the lasing wavelength to that of the bulk GaAs, namely 870 nm. In an effort to tailor the wavelength more specifically, quantum wells were introduced. Quantum wells allowed an extra degree of freedom in semiconductor lasers because they allowed for somewhat independent choice of the active region material and the lasing wavelength. Still the AlGaAs-GaAs system is limited to the red and near-infrared portion of the spectrum. In an effort to expand further into the infrared, strained quantum wells of $In_xGa_{1-x}As$ were introduced. $In_xGa_{1-x}As$ alloys are not lattice-matched to GaAs so only thin layers ($t < 10$ nm) and small indium percentages ($x < 0.3$) are practical. Even with the integration of InGaAs quantum wells, emission wavelengths greater than 1100 nm are not possible due to materials constraints. Figure 2-4 shows the family of III-V semiconductors available to researchers as a function of bandgap, emission wavelength, and lattice constant.

In the 1980s, researchers began considering the possibility of ignoring the strict lattice-matching criteria traditionally imposed on semiconductor laser systems [5-7]. By taking advantage of the fact that two materials were in fact *mis*matched, they realized they could produce small particles of active material which made it possible to emit in the technologically important infrared region of the spectrum. The result was InAs and $In_xGa_{1-x}As$ quantum dots on GaAs substrates. The first demonstrations of quantum dot lasers in a GaAs system were reported in the 1990s [8-11].

2.3.2 Advantages of Quantum Dots

In addition to their ability to extend the emission range of GaAs-based materials further into the infrared, quantum dots possess a number of unique qualities of particular interest to the optoelectronic device designer. Their zero-dimensionality leads to a density of states that is a series of delta functions of increasing energy as shown in Figure 2-7. In practice, quantum dots do not have perfectly discrete energy levels, but still have extremely narrow distributions, corresponding to narrow emission spectra centered on a single wavelength. Furthermore, these energy levels are rapidly filled by captured electrons and holes allowing inversion via electrical pumping to occur at much

lower injected current values. The result is lasers with theoretical threshold currents dramatically lower than traditional quantum well lasers [30]. Additionally, quantum dots should yield laser devices with higher characteristic temperatures, a measure of the device's temperature stability with respect to self-induced heating and threshold currents shifts. Quantum dot lasers should therefore be relatively insensitive to temperature [5].

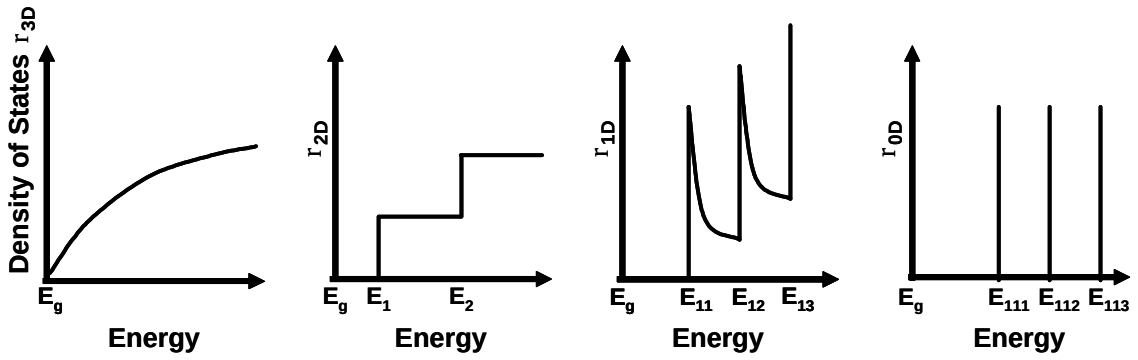


Figure 2-7: The density of states for decreasing levels of dimensionality. From left to right, the density of states for a bulk material, a quantum well, a quantum wire, and a quantum dot.

Another important advantage of quantum dots is their dynamic behavior. Owing to the limited number of energy levels within each dot, devices based on quantum dots are capable of extremely fast modulation speeds. Typical line rates for fiber optic network data is 10 Gb/s, with 40 Gb/s systems now emerging. Future generations call for 160 Gb/s and even 320 Gb/s line rates, so the need for sources with extremely high-speed modulation capabilities will become increasingly important.

However, quantum dots in practice are not perfect cubes of material, but rather slightly irregular hemispheres or pyramids of material. Their overall shape is flattened, with their diameter being quite large compared to their height. Unlike quantum wells, precise calculation of their energy levels is not straightforward and is best done using numerical methods [31].

2.4 Quantum Dot Formation and Growth

For a semiconductor quantum dot, the formation of the reduced dimensionality particle is a result of the difference in lattice constants of the substrate material and the quantum dot material. The Matthews-Blakeslee analysis no longer holds for quantum dots growing by the Stranski-Krastanov islanding mechanism, because the material is no longer constrained within the two-dimensional plane. Instead, the three-dimensional structure of the dot modifies the analysis. The end result is that quantum dots can be grown to thicknesses in excess of the traditionally defined critical thickness while still maintaining the lattice constant of the underlying substrate. Typical InAs or InGaAs quantum dots are around 20-25 nm in diameter and 3-5 nm in height [11, 32].

The crystallographic properties of the dots are extremely important to the eventual device performance. High areal densities of dots improve carrier capture and subsequent output power with typical designs having dot densities around 5×10^{10} cm^{-2}. Growth conditions often create a tradeoff between dots sufficiently large to emit at 1310 nm and areal densities high enough to ensure intense light output. Careful optimization and understanding of the growth kinetics [33] have resulted in dot densities as high as 1.6×10^{11} cm^{-2} [34]. The quality of the dots' interface with the surrounding material is particularly important because of the high surface-to-volume ratio of the dots. Interfacial defects in the dots can be catastrophic to device performance, acting as sites for nonradiative recombination.

2.5 Quantum Dot Optimization

Extensive materials characterization was required to confirm the presence of quantum dots and to fine-tune their emission behavior. Initial observations of the reflection high-energy electron diffraction (RHEED) pattern showed behavior characteristic of quantum dots. A number of different experiments were performed to optimize the growth conditions for the InAs quantum dots. The variables explored included substrate temperature, the growth rate, and the arsine overpressure. All of the quantum dots in this study are self-assembled, that is, no template was formed on the

surface prior to growth and no subsequent processing was done to modify quantum dot dimensions.

2.5.1 Photoluminescence

Characterization of the dots emission behavior was performed using photoluminescence (PL). A schematic of the PL system is shown in Figure 2-8. In PL, a high intensity argon laser (λ=488 nm) is incident upon the sample, exciting electrons into the conduction band. Upon relaxation of the electrons back to the valence band, the sample emits photons characteristic of the bandgap of the semiconductor. By collecting and measuring the intensity of the emitted photons, the emission behavior of the quantum dots can be characterized. Photoluminescence is an important characterization technique because it is non-destructive, quick, and an easy way to obtain valuable information about deposited films.

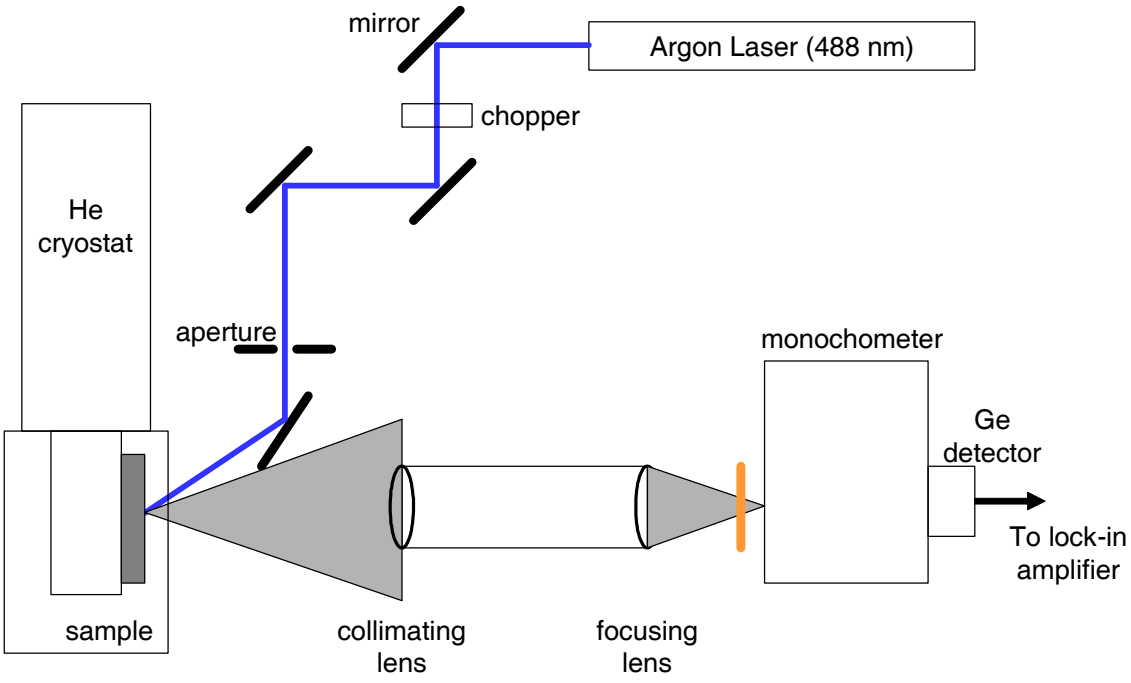


Figure 2-8: The photoluminescence configuration used for this thesis work. The high energy argon laser beam excites electrons into the conduction band. The electrons then relax and emit photons characteristic of the bandgap of the materials in the sample.

The ability to cool the samples to 10 Kelvin is extremely useful for characterizing materials that will not emit at room temperature. Using a helium cryostat in conjunction with a heating element, a sample can be analyzed at any temperature between 10 K and room temperature. The thermal energy present at room temperature can diminish the ground state emission from weakly emitting or small volume materials because it can excite carriers out of the ground state to higher order excited states. However, the semiconductor bandgap increases with temperature and a general blue shift is seen in the emission spectrum. An example of this is shown in Figure 2-9.

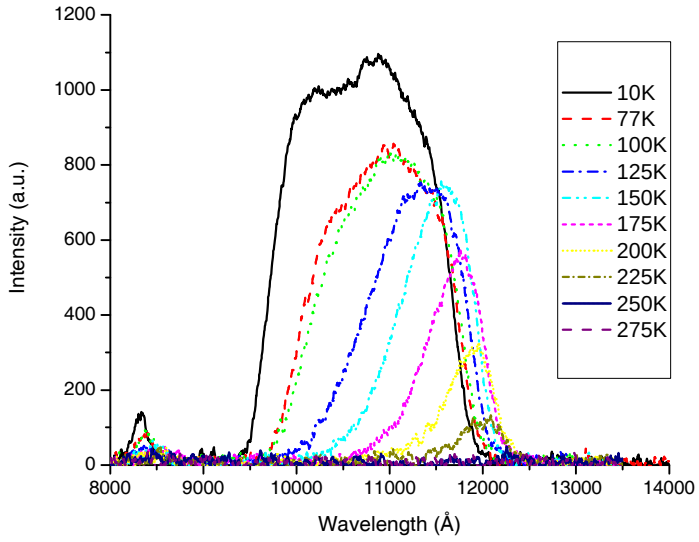


Figure 2-9: Photoluminescence spectrum of a quantum dot sample at various temperatures. The peak intensifies and blue shifts as the sample temperature decreases.

In order to compare growth conditions for the quantum dots, the same epitaxial growth structure is used in order to make simplified comparisons. The epitaxial structure used in this work is shown in Figure 2-10; the structure is the same as the active region that is used in the laser diodes.

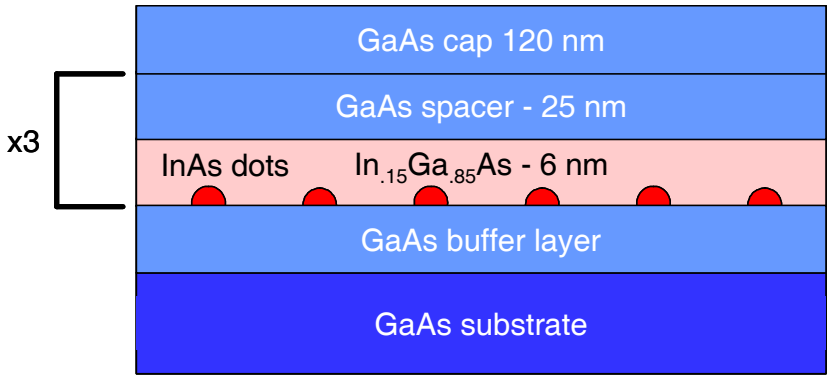


Figure 2-10: The epitaxial structure used to evaluate the quantum dot growth conditions.

The InAs dots are placed in a dot-in-well (DWELL) [35] configuration to increase carrier confinement and to increase the carrier capture efficiency of the dots. The quantum well layer isolates the strain fields of the quantum dots and serves to trap carriers in the vicinity of the quantum dots and thereby aid in carrier capture for the dots [36]. The increased carrier capture helps in the injection efficiency and helps to improve modulation speeds of quantum dot lasers by lowering the rate-limiting carrier capture time. Additionally, the strain relief provided by the quantum well appears to red shift the emission spectrum of the dots. The DWELL structures are comprised of three 6-nm thick $In_{0.15}Ga_{0.85}As$ quantum wells with 25-nm thick GaAs barrier layers between each quantum well. The GaAs barrier thickness is sufficiently wide so that the dots will be isolated from the strain field of the underlying quantum dot layers. If the spacer layers are not sufficiently thick, the quantum dots could template off of each other or possibly experience a broadening of the size distribution.

2.5.2 Growth Rate

Quantum dot formation is heavily affected by the growth rate. Quantum dots grown by the Stranski-Krastanov islanding mechanism are best understood as a kinetic process of nucleation and growth, unlike the steady-state process that describes growth of thicker layers.

Quantum dot kinetics are extremely sensitive to the number of atoms arriving at the surface, the growth rate. The growth rate for bulk materials, and even quantum wells, is most commonly defined as the time-averaged process of monolayer-by-monolayer deposition. However, due to their relative thickness, it is commonly ignored that there are in fact two separate domains of materials growth. The first domain is the initial domain, where the atomic species first begin to impinge upon the crystalline surface. Upon close inspection, these surfaces are not simply flat crystal planes like those found within the bulk substrate rather the surfaces are quite different from their buried counterparts. Particularly at higher growth temperatures, a crystalline surface is an evolving and dynamic surface of terraces and steps. Furthermore, the dangling bonds at the surface undergo reorganization to minimize the surface energy. The surface reconstructions have many different geometries, as many as seven, each dependent on the particular stoichiometry at the surface [37, 38]. Under normal GSMBE conditions, the GaAs (100) surface atoms preferably stabilize into a so-called 2x4 reconstruction. Upon the initiation of growth, these surface atoms must undergo reorganization to their crystallographically appropriate positions to accommodate the newly arriving atomic species. This reorganization is actually an evolution through several different reconstruction geometries and it takes some time before the first monolayer of the new material can organize itself. Essentially, a great deal of surface diffusion is required before the crystal can begin to grow in an ordered fashion. Upon opening of the shutter, the effusion cell begins to cool down slightly as atoms escape from the cell, lowering the temperature and flux rate of the cell. As such, the initial growth rate is slightly higher than that the steady-state growth rate of the uncapped effusion cells.

Careful calibration of each cell in the GSMBE chamber – in both growth regimes – is essential for accurate film deposition. This calibration process occurs by measuring and averaging RHEED oscillations in both growth regimes at a number of different cell temperatures. A curve-fitting method is then used to predict growth rates at any temperature within the cell's operational range. Whenever a major equipment or process change is made to the MBE, this process is repeated for each group-III effusion cell. Even cooling the materials and reheating them can cause the flux rate to change for a particular effusion cell temperature, as a result of material settling within the PBN

crucible. Before each growth, the flux rate is measured to renormalize the cell. At the start of each growth, a buffer layer identical to the substrate (i.e. 200 nm GaAs on GaAs substrate) is grown to prepare the surface for epitaxial growth and to bury impurities and defects before the important film deposition begins. During this time, RHEED oscillations are taken to confirm that the growth rate curve-fitting prediction is accurate.

Quantum dot growth is unique in that the entirety of it occurs during the initial growth rate regime. There are no subsequent atoms that arrive at the surface – until sometime later – and the restructuring and reorganization is the essence of the process. The lattice mismatch is the driving force for the formation of the quantum dots. The inherent bulk lattice constant of InAs is 6.0585 Å while that of GaAs is 5.6534 Å, resulting in high interfacial energies between the materials. Even a few monolayers is beyond the Matthews-Blakeslee limit and the result is that a single monolayer of InAs will wet the GaAs surface, followed by beads of InAs, not unlike water beading upon the surface of a newly waxed car. These beads assemble locally and are constantly evolving. A few atoms will cluster together for a time and then will disassemble just as rapidly. For all quantum dot growths in this study, just 2.7 monolayers of InAs material was deposited in times ranging from 27 seconds to almost 3 minutes. Upon the closure of the GSMBE's shutters, InAs islands of a variety of sizes are present on the surface. Dots that are bigger or smaller than the thermodynamically stable size, or range of sizes, will either increase or decrease in size by the movement of adatoms upon the surface.

For this study, quantum dots were grown using initial growth rates of 0.10, 0.05, and 0.01 monolayers per second. The substrate temperature was 500°C and the arsine flow rate was 1.0 sccm, corresponding to a chamber pressure of 1.7×10^{-5} torr. The results of photoluminescence taken at 10K are shown in Figure 2-11. Growing the quantum dots at slower growth rates leads to a red shift in their emission wavelength. Knowing that larger dots emit at longer wavelengths, this phenomena is most likely the result of allowing the dots more time to self-assemble and grow to a larger size. However, this comes at the cost of decreased emission intensity. Interesting to note is that the secondary peak corresponding to the quantum well layer is seen to the left of the main peak. In some cases, the emission peak of the quantum dots excited state can also be seen.

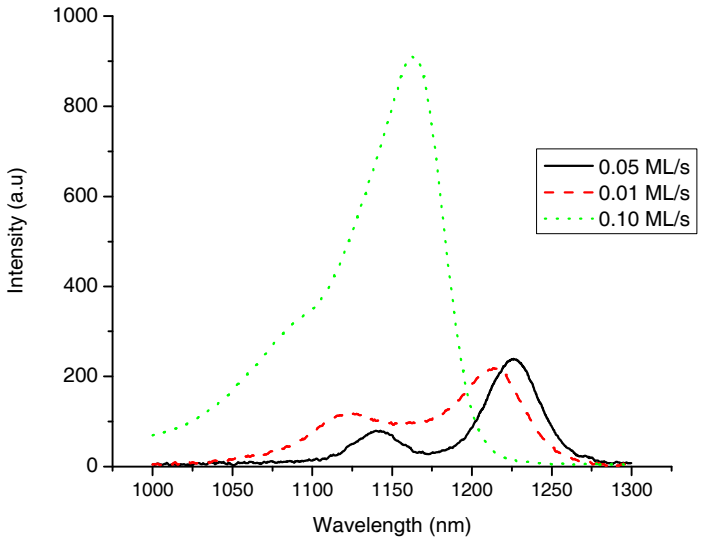


Figure 2-11: Photoluminescence spectra taken at 10K for quantum dots grown at various growth rates. It can be clearly seen that slower growth rates red shift the emission peak, but at the cost of greatly diminished intensity.

While the quantum mechanics of quantum dots dictate that the dots emit at a single wavelength of light that is related to the dot's size, a wide distribution of sizes will result in a wide distribution of wavelengths. The size distribution is generally counterproductive for quantum dots for photonic emission applications where a single emission wavelength is highly desirable, but a range of sizes is an unavoidable result of the kinetic process. The inhomogeneous spectrum broadening can be minimized, but not entirely eliminated [39]. Furthermore, since dots are only capable of emitting at a single wavelength, quantum dots that do not emit at the wavelength determined by the laser's device cavity dimensions – or selected by a distributed feedback grating structure – are not contributing to the lasing mode. It is important to let this dynamic competition occurring between dots of different sizes play out. Once the subsequent growth of wells or spacer layers commences, the dots are "frozen" within the crystal and incapable of further reorganization. Therefore, after the deposition of dots a growth interruption of 6 seconds was chosen to give the dots adequate time to reach their thermodynamically

stable sizes. The result is a dot size distribution and corresponding emission spectrum that is narrower.

2.5.3 Substrate Temperature

The Brownian motion of atoms upon the growing crystal surface is the primary mechanism by which the quantum dots self-assemble. As Brownian motion is an energetically activated process, it can be directly correlated to the temperature of the substrate. Changing the temperature of the substrate can dramatically change the mobility of the surface atoms and ultimately effect the equilibrium size distribution of the quantum dots. A study was prepared to understand the effect of substrate temperature upon the emission wavelength. Samples were grown at substrate temperatures of 470, 500, 515, and 530°C. This represents the entire range of temperatures at which quantum dots are typically grown. The room temperature photoluminescence spectra are shown in Figure 2-12 and Figure 2-13

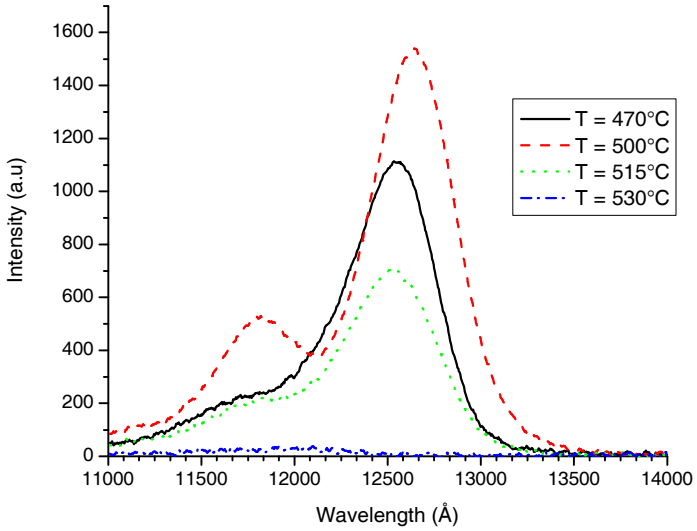


Figure 2-12: The room-temperature photoluminescence spectra of quantum dots grown at different substrate temperatures.

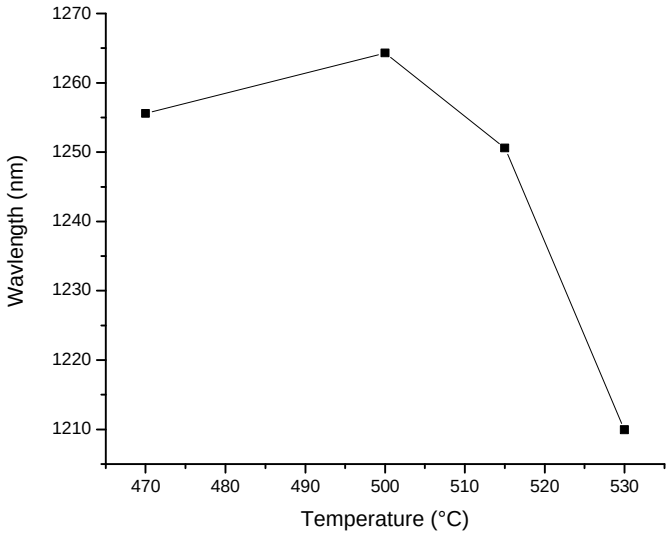


Figure 2-13: The wavelength of the quantum dots peaked at a substrate temperature of 500°C.

From the PL, the emission wavelength is indeed dependent upon the substrate temperature. Quantum dots grown at 530°C are clearly inferior to dots grown at any of the other temperatures. Emission is barely detectable at room temperature and the wavelength is well below that of the other three, almost 50 nm towards the blue. The wavelength did not vary significantly between the samples grown at 470, 500, and 515°C but the intensity was much greater for the sample grown at 500° and it exhibited the longest emission wavelength. When pushing the limits of emission on GaAs substrates, every nanometer closer to 1310 is important. Furthermore, the 500°C samples have the smallest size distribution of quantum dots as indicated by the full-width-half-maximum (FWHM) value of 55.5 nm.

2.5.4 Arsine Pressure

During one particular quantum dot growth, the arsine gas flow diminished due to a decrease in the pressure across the mass flow controller and resulting in a decrease of the supply of arsine to the GSMBE chamber. A serendipitous result was the discovery that the intensity of the photoluminescence had greatly increased while the emission

wavelength remained constant. To confirm this result, a series of film depositions was planned to validate this auspicious discovery.

Samples were grown with arsine flow rates of 0.1, 0.25, 0.50, 0.75, and 1.0 sccm in order to change the partial pressure of arsenic in the growth chamber. The samples were then characterized using PL. The study showed substantial correlation between lower arsenic pressures and higher emission intensity. Interestingly, the emission wavelength of the dots did not change appreciably, indicating that the diameter of the dots remained constant. The increased emission intensity is believed to be caused by a higher density of high quality quantum dots. The PL results are shown in Figure 2-14.

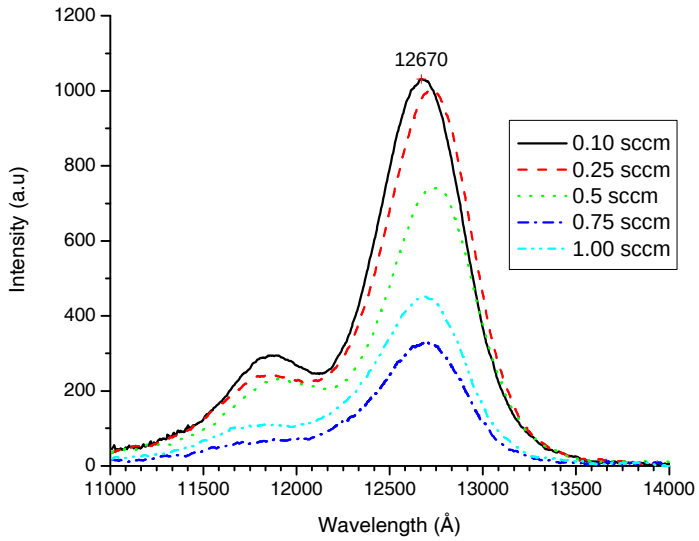


Figure 2-14: Photoluminescence of quantum dots grown with varying arsine flows. A clear correlation is seen between lower arsine flows and higher intensity emission.

The arsine flow rate appears to be a strong factor in determining the emission intensity of the quantum dots. The photoluminescence intensity nearly quadruples with the emission wavelength remaining virtually constant at around 1265-1270 nm and the FWHM remains nearly constant. There are a number of possible causes for this

phenomenon. The limited size of quantum dots and the peculiarities of their formation makes them particularly susceptible to arsenic incorporation irregularities. At higher arsenic overpressures anti-site defects may form where arsenic incorporates on to the Ga sublattice positions, although this is unlikely at these substrate temperatures. These anti-site defects could lead to non-radiative recombination and decrease the overall intensity of dot emission. Other researchers have examined the role of the initial surface reconstruction and the effect of the subsequent capping layer on the dot formation [40]. Most likely, the increased emission intensity is due to enhanced surface kinetics that enable the formation of either greater numbers or lower defect quantum dots [29]. In order to get a better picture of what is occurring on the substrate, direct imaging of the quantum dots could yield insight into the surface phenomena.

2.5.5 Atomic Force Microscopy

Direct observation of the presence of quantum dots on the surface is useful for understanding the kinetics of quantum dot formation. Atomic force microscopy (AFM), a variety of surface probe microscopy, is a powerful surface analysis technique that can image the quantum dots. AFM allows for precise determination of surface topology with a resolution approaching that of single atoms. Using fabrication techniques that expose the sharp crystallographic planes in silicon, extremely sharp AFM tips with diameters of just a few nanometers can be manufactured. The AFM tips are fabricated on a cantilever that interacts with the surface, either continuously or discretely, while a laser interferometer measures the deflection of the tip. The result is an extremely high resolution image of the height of the sample surface.

Samples were prepared for AFM by terminating the epitaxial growth directly after the deposition of the quantum dots. The substrate temperature was rapidly quenched from 500°C to 300° in six minutes – about as fast as is practical with the equipment – to freeze the dots in position and to reduce the surface mobility of the adatoms. The samples were then removed from the vacuum chamber and immediately scanned in the AFM, to prevent the formation of a substantial surface oxide.

Two different depositions were performed to compare the quantum dot formation. Both samples were grown under identical conditions but with different arsenic flow rates.

The AFM results are shown in Figure 2-15. Using image analysis software from *Scion Image* [41], the dot's density and average diameter was determined.

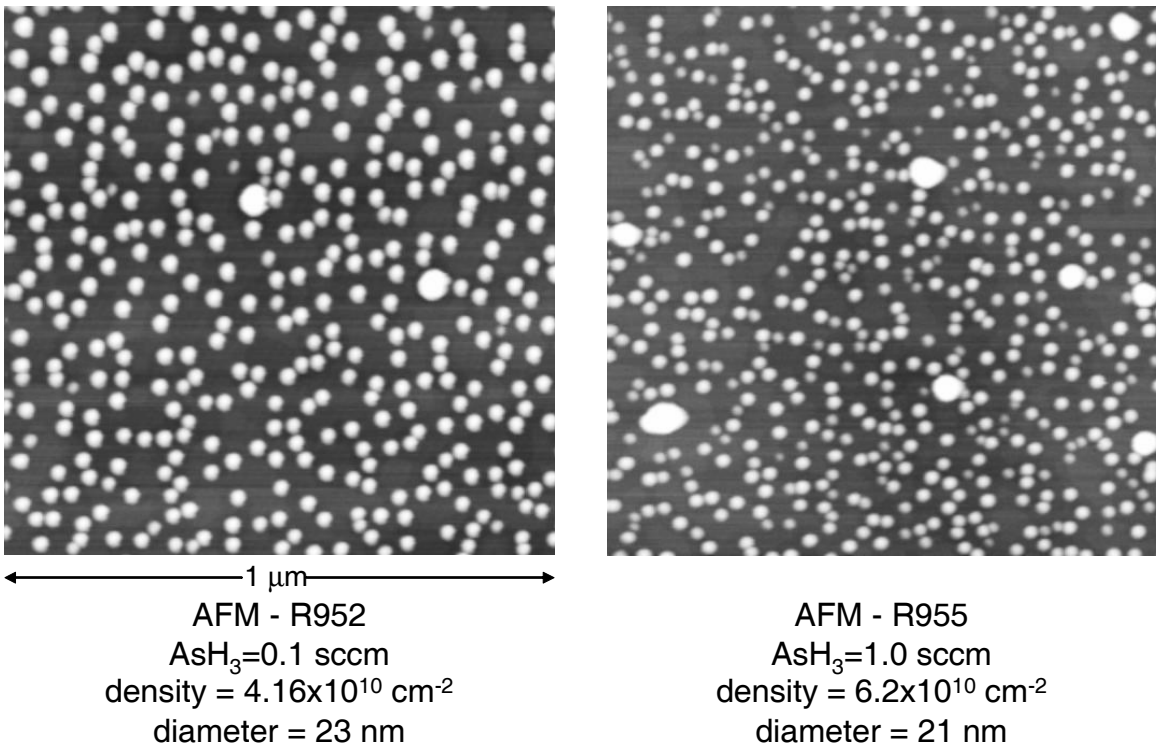


Figure 2-15: Atomic force microscopy image of quantum dots grown with different arsine flows. The sample grown at higher arsine flow clearly has more anomalously large dots.

For the sample that was grown with an arsine flow rate of 0.1 sccm, the average diameter of the dots was 23 nm with a dot density of 4.16×10^{10} cm^{-2}. The sample that was grown with a higher arsine flow rate of 1.0 sccm, the average diameter of the dots was 21nm with a dot density of 6.2×10^{-10} cm^{-2}. The two arsine flows corresponded to chamber pressures of $3.4 \times 10^{-6}$and 1.7×10^{-5} torr, respectively. The dots have nearly identical sizes and densities, but the prevalence of anomalously large dots is much greater in the sample grown at higher pressure. This phenomenon could have a number of possible causes. Prior studies have suggested that the dot density increases and the size decreases with increasing arsenic pressure [42, 43], and these results confirm that

observation. The higher overpressure of arsenic could be suppressing the indium adatom surface mobility and preventing larger dots from decomposing into the smaller dots which are kinetically favored. Additionally, the sample that was grown at a low pressure has a slight growth interruption of 6 seconds while the arsine flow rate is ramped to the lower value just before the quantum dot deposition begins. The short pause may allow for surface reconstructions that are more favorable to quantum dot self-assembly.

2.6 Tunnel Junctions

2.6.1 Tunnel Junction Theory

An initial study was performed to independently characterize the tunnel junctions that would eventually be used in the laser structure. In particular, the effect of indium incorporation was studied in order to explore if the tunneling could be enhanced by decreasing the bandgap, and hence the tunneling energy barrier.

A tunnel junction, or an Esaki junction, is a p-n junction composed of two degenerately-doped layers. As doping levels increase within a semiconductor layer, the Fermi level moves closer to the band edge. As the doping level increases yet further, the Fermi level actually moves beyond the band edge and into the band itself. Typically, this can be achieved for doping level in excess of 10^{19} cm^{-3}.

The current-voltage (IV) behavior of the Esaki junction is quite unusual. The IV curve is shown schematically in Figure 2-16 along with band diagrams to show the movement of the energy bands and Fermi levels as a bias is applied. In negative bias (Figure 2-16a), the Esaki junction essentially goes immediately into Zener breakdown. The leakage current is a result of tunneling across the bandgap due to the relative position of the Fermi levels. In positive bias (Figure 2-16c), the current immediately increases, again as a result of tunneling. However, this tunneling current reaches a maximum (Figure 2-16c), and then actually starts to decrease (Figure 2-16d). The subsequent region is one of negative differential resistance and is of considerable interest to some device designers. At even higher biases (Figure 2-16e), the Esaki

junction eventually begins to behave like a typical p-n diode and exhibits the exponentially increasing current as expected from the Shockley equation.

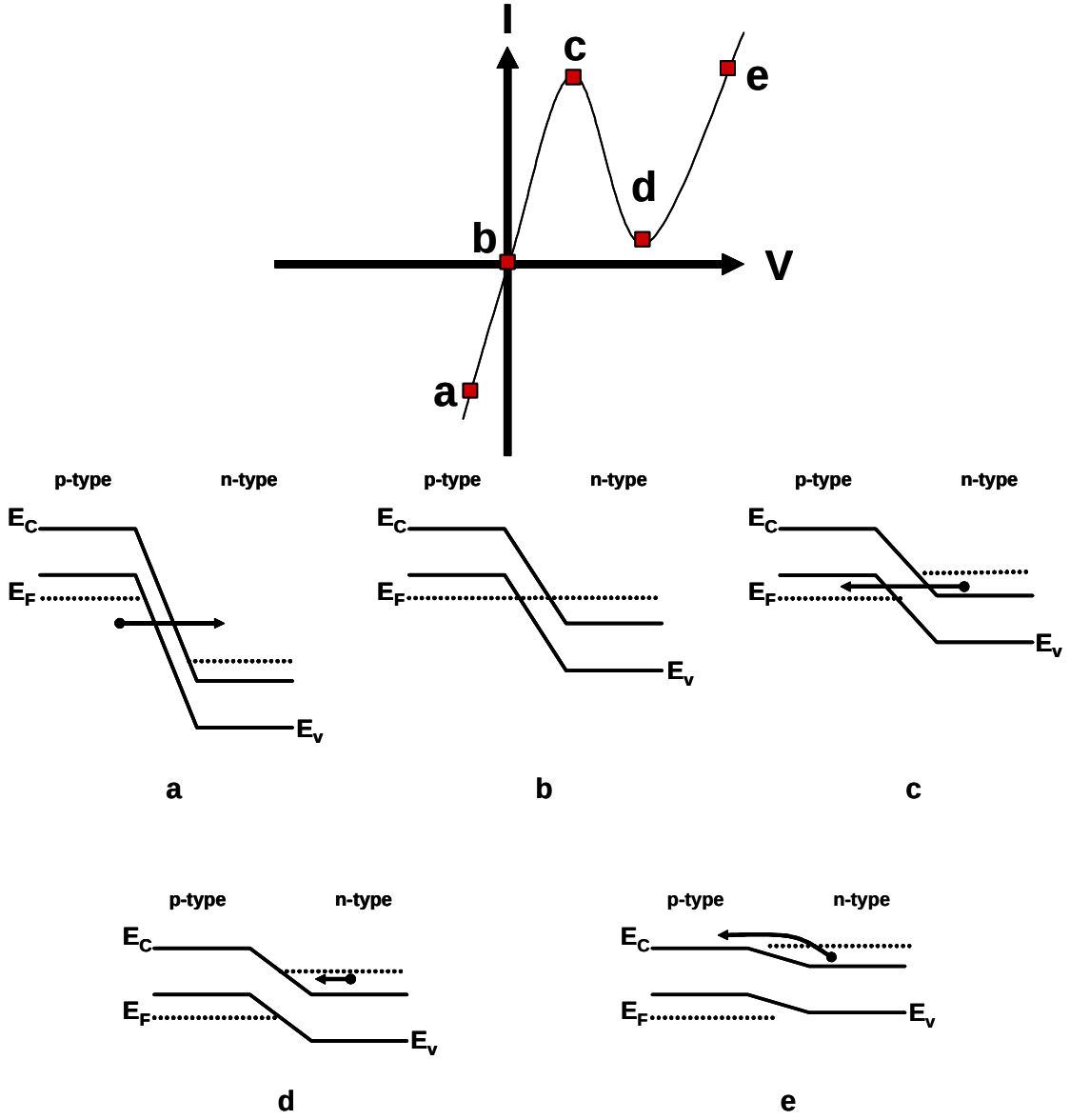


Figure 2-16: The current-voltage (IV) and band diagrams of a tunnel junction. The arrows indicate the direction of electron flow.

2.6.2 Tunnel Junction Growth and Fabrication

The tunnel junctions require the quasi-Fermi levels to reside within the conduction and valence bands, a degeneracy that is created by excessive doping. High

doping concentrations (above 10^{19} cm^{-3}) can be difficult to attain, so a number of structures were grown to explore the optimal growth conditions for high dopant incorporation. A Hall measurement is a technique for determining the density of carriers with a semiconductor. By flowing current in one direction, by applying a magnetic field in an orthogonal direction, and by measuring the Hall voltage in the third orthogonal direction, the density of dopants can be determined. Hall measurements confirmed that doping concentrations of approximately $1x10^{19}$ cm^{-3} for both the n-type and p-type doping were produced at substrate temperatures of 480°C using a growth rate of approximately 0.5 μm/hr. Control of the growth rate is important because a low growth rate allows for more dopant atoms to be incorporated in the thickness of the film for a given flux of dopants from the effusion cell. The result is a sample with an impurity concentration corresponding to a Fermi level within the band edge of the semiconductor. A p-n junction formed by two degenerate layers is an Esaki tunnel junction and will exhibit the desired I-V performance.

Once adequate dopant concentrations were obtained, $In_xGa_{1-x}As$ tunnel junctions were grown with In concentrations of x=0, 5, 10, and 15%. Ellipsometric measurements determined the actual indium compositions to be 0, 6.5, 11.5, and 13.5% due to some imprecision in the growth conditions. Nonetheless, the trend of increasing In concentration is more interesting than the precise percentages. The structure is shown schematically in Figure 2-17. Precise sample growth conditions are included in the Appendix.

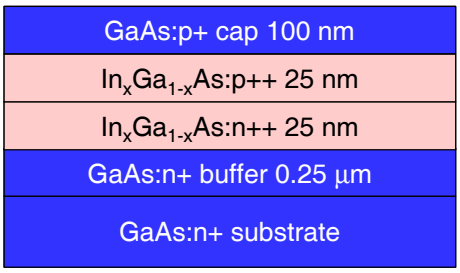


Figure 2-17: The epitaxial structure of the tunnel junction samples.

Once grown, the samples underwent cleanroom fabrication to create devices that could be tested. Ti/Pt/Au (300Å / 200Å / 2500Å) contacts were evaporated and

patterned to form circular contacts with diameters varying from 10 to 90 μm. The circular contacts were used as a mask to wet etch mesas 0.75 μm deep through the tunnel junction using a $NH_3OH:H_2O_2:H_2O$ (10:5:240) chemistry. Finally, an identical Ti/Pt/Au contact was deposited on the backside of the wafer and the whole structure underwent rapid thermal annealing (RTA). The RTA procedure first ramped the temperature to 250°C; after 10 sec at 250°C the temperature was ramped to 380°C. The 10 second intermediate pause ensures that the temperature will not overshoot the desired temperature of 380°C. If the temperature exceeds 400°C, undesirable effects such as dopant diffusion or sample decomposition could occur. Micrographs of the finished devices are shown in Figure 2-18.

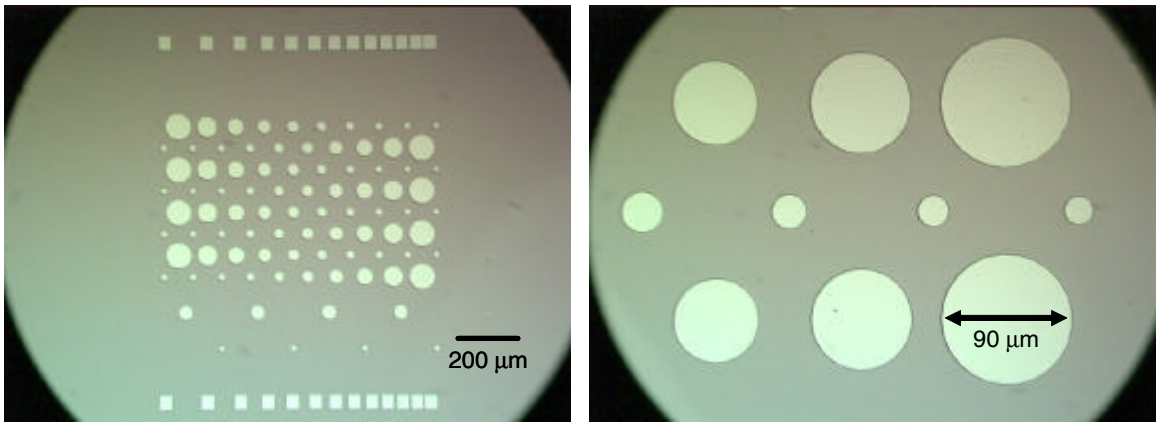


Figure 2-18: Nomarski micrographs of fabricated tunnel junction samples. The largest circles are 90 μm in diameter.

2.6.3 Tunnel Junction Testing and Results

The structures were electrically tested using a Hewlett-Packard semiconductor parameter analyzer. The current-voltage (IV) behavior shown in Figure 2-19 confirms that the samples behave like Esaki junctions. Most notably, the devices immediately breakdown in reverse-bias and in forward-bias there is a peak in current followed by an region of negative differential resistance.

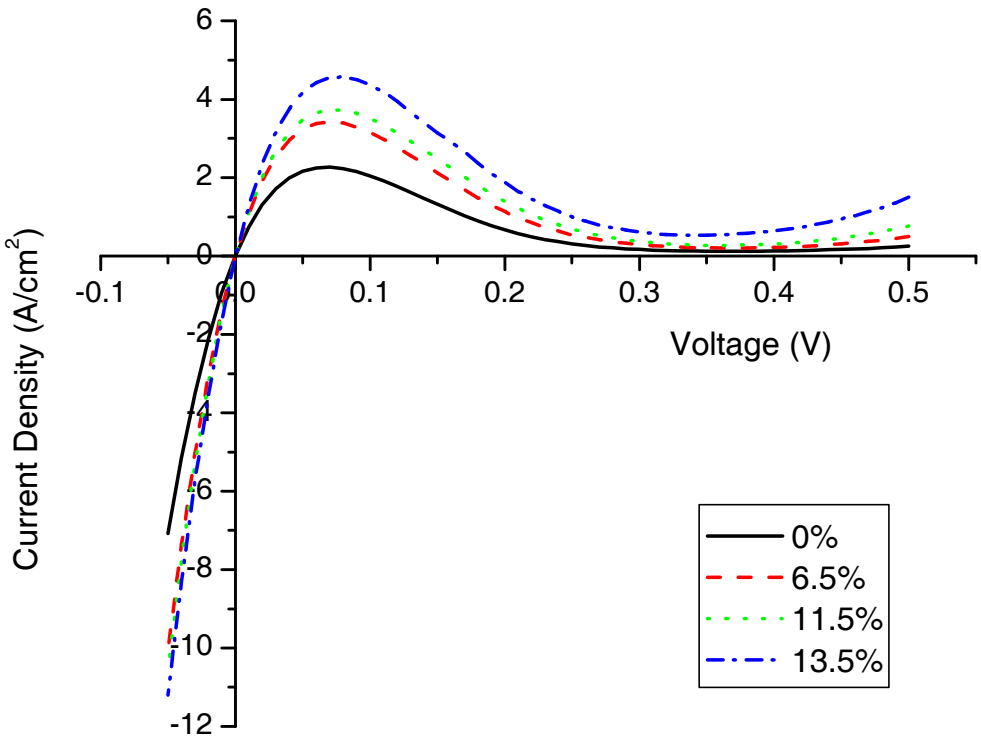
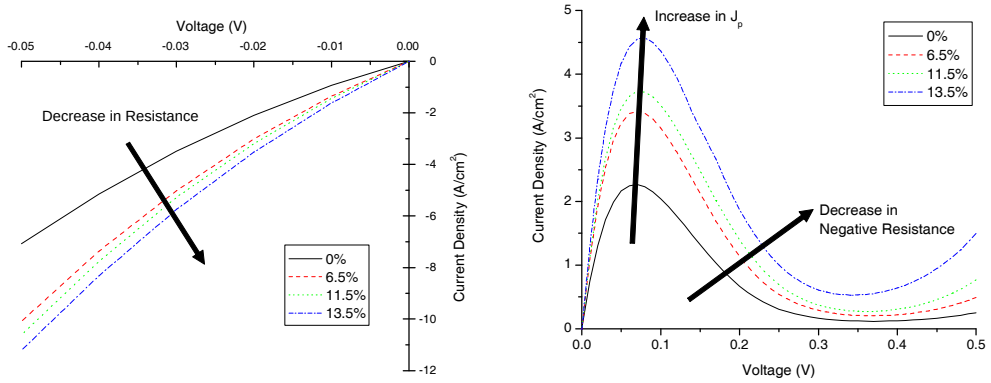


Figure 2-19: Current-voltage (IV) curve for the Esaki tunnel junctions. The experimental behavior closely resembles theoretical predictions.

Closer examination of the IV characteristics confirms the presence of increased tunneling (reduced resistance) with increasing indium content as shown in Figure 2-20a. This key result confirms theoretical predictions and is useful for improving the device design. As the tunnel-junction-coupled quantum dot lasers utilize reverse-biased tunnel junctions, larger tunneling currents directly correspond to higher number of electrons emitting additional photons. Additionally, the rollover and negative differential resistance characteristics of Esaki tunnel junctions were observed under forward bias (Figure 2-20b). With increasing indium content, a number of interesting trends are observed. First, the peak current increases with increasing indium content. Secondly, the slope of the negative differential resistance increases with increasing indium content. Both phenomena can be understood by considering the greater band offset (with respect to

GaAs) that is created by increasing the indium content. Furthermore, higher indium contents decrease the InGaAs bandgap, so effectively there is a lower energy barrier to tunneling and therefore an increase in tunneling current.



a) **b)**

Figure 2-20: a) Forward bias behavior shows that the negative differential resistance gets more steeply sloped with increasing indium content. b) Reverse bias behavior of tunnel junctions shows decreasing resistance with increasing indium content.

These tunnel junction results have potential implications for improving the operation of a wide variety of devices. Tunnel junctions have already been implemented as low-resistance ohmic contacts for materials such as GaN, where p-type ohmic contacts are difficult to obtain [44]. On the p-type side of the device, the tunnel junction converts a n-type electron current to a p-type hole current avoiding the difficulty of creating a p-type contact by simply using two n-type metallization schemes. Tunnel junctions may offer lower resistance ohmic contacts in other materials systems as well. Tunnel junctions have also been used in lasers and light-emitting diodes to minimize the amount of p-type material where the p-type material is operationally inferior [45]. Vertical-cavity surface emitting lasers are yet another application for tunnel junctions [46, 47], and the results of this work encourage additional applications in photonic devices.

2.7 Laser Structure

2.7.1 $In_{0.49}Ga_{0.51}P$ Cladding

Typical GaAs-based lasers utilize AlGaAs for the cladding material. However, substrate temperatures of at least 600°C, and more likely 700°C, are necessary to deposit AlGaAs of any reasonable quality. This high-temperature growth requirement is incompatible with the low-substrate temperatures required for quantum dot formation. If the already-deposited quantum dots were exposed to these excessive temperatures, substantial indium diffusion and intermixing could occur and the dots would experience a significant blue-shift. Furthermore, the highly-doped regions of the tunnel junction could undergo diffusion that would reduce the tunneling currents. These incompatibilities necessitate the choice of a cladding material which can be grown at temperatures around 500°C. Conveniently, $In_{0.51}Ga_{.49}P$ can be grown lattice-matched to GaAs and can be grown at approximately 500°C. The optimal InGaP growth temperature was determined to be 480°C and two 0.75 μm thick layers of InGaP were used as the n- and p-type cladding material. The InGaP was doped with Si and Be, respectively, at a concentration of approximately 10^{18} cm^{-3}.

Lattice matching is extremely important to epitaxial quality and device performance, particularly when thick layers such as the $In_{0.49}Ga_{0.51}P$ cladding are used. Lattice mismatch can lead to crystallographic defects such as dislocations that are nonradiative recombination centers. Furthermore, the extreme sensitivity of quantum dot self-assembly to strain fields demands that the underlying layers be grown with a minimum of lattice mismatch.

In order to characterize the $In_{0.49}Ga_{0.51}P$ lattice matching, high-resolution x-ray diffraction was used. High-resolution x-ray diffraction is a powerful technique for the analysis of deposited films. High-resolution x-ray diffraction allows the experimenter to non-destructively examine the film quality and obtain precise information about film quality and composition. The x-ray diffractometer that was use is shown in Figure 2-21. Diffracting the source x-rays through the beam conditioning crystals allows a single x-ray wavelength to be selected. With the Cu $K\alpha_1$ wavelength incident upon the sample, it is

possible to collect diffracted wavelengths at extremely high-resolution. Relatively thin samples of InGaP (40 nm thick) that were grown on GaAs substrates were examined via high resolution rocking curves about the GaAs (004) diffraction peak. The thin InGaP layer thickness is deliberately chosen to be below the Matthews-Blakeslee criteria. Were a lattice-mismatched film grown too thick, the strain buildup would cause the film to undergo a relaxation process and precise calculation of its composition would become more difficult.

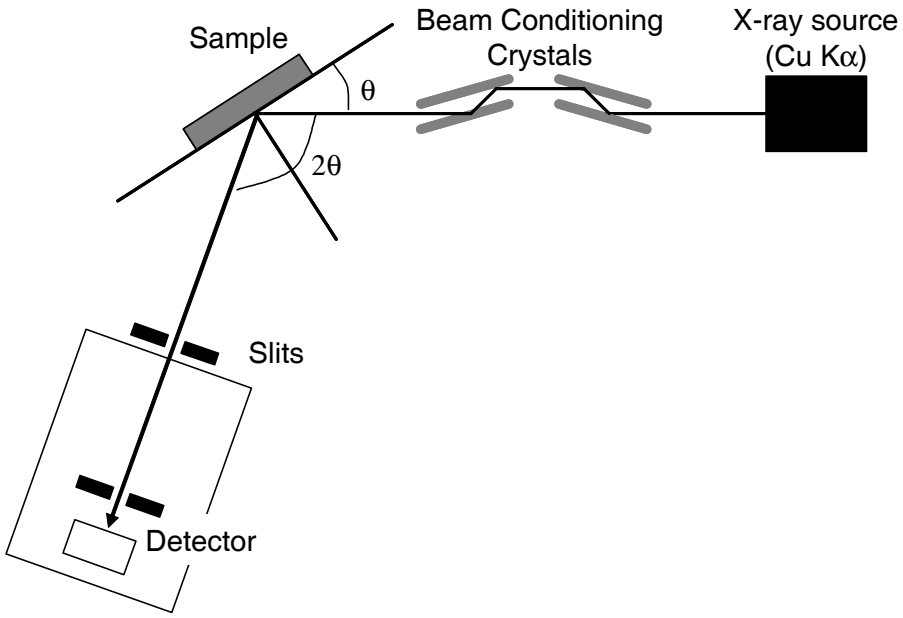


Figure 2-21: Schematic of high-resolution x-ray diffraction.

By analyzing the rocking curves [48, 49], the InGaP growth initially showed high indium concentrations in the film. The effusion cell temperatures were adjusted and a second film was grown in which the indium concentration was now too low. Final adjustments yielded a film that was well lattice-matched, with the InGaP diffraction peak residing within 300 arcsec of the substrate peak. This corresponds to a gallium percentage of 50.1%. The results are shown in Figure 2-22. Even with this seemingly encouraging result, lattice-matching thick films of InGaP to GaAs continued to plague subsequent epitaxial growths.

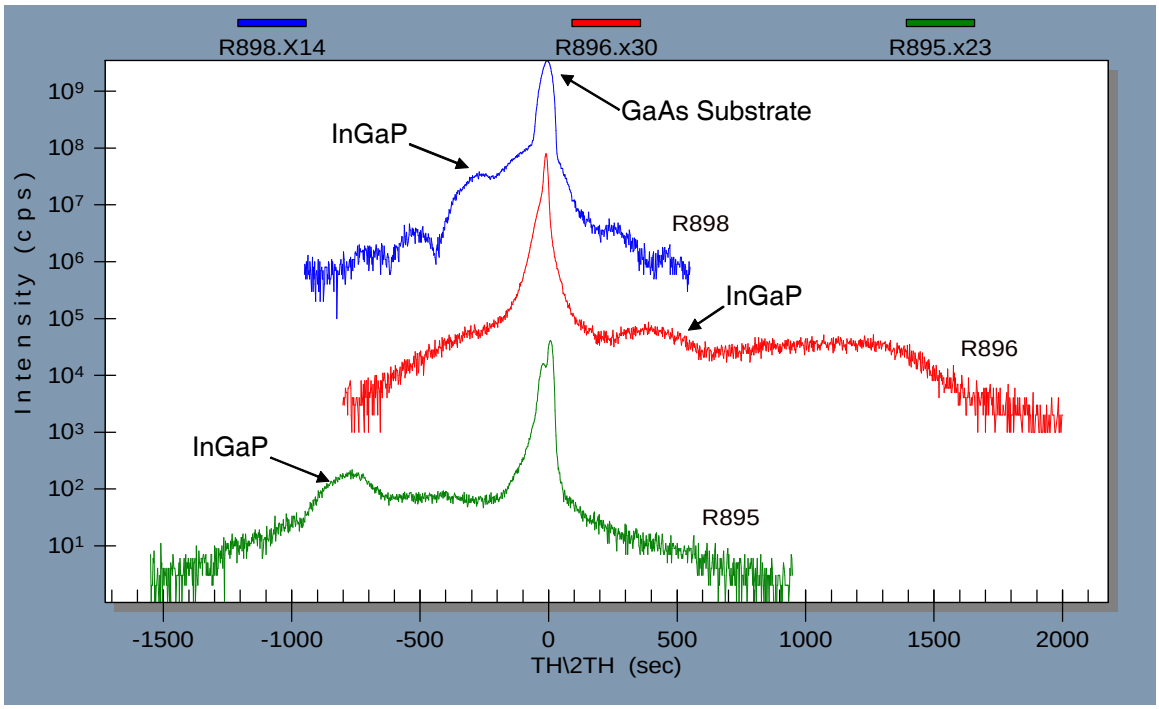


Figure 2-22: High-resolution x-ray diffraction helped to determine the optimum growth conditions for lattice-matched $In_{0.49}Ga_{0.51}P$. Each rocking curve is offset from each other by a factor of 10^2.

2.7.2 Epitaxial structure

The laser structure is based around the quantum dot active regions. The rest of the core region is composed of GaAs, for a total thickness of 168 nm. The core region is grown at a substrate temperature of 500°C, a temperature which was chosen after extensive optimization of the quantum dots emission wavelength and intensity.

In addition to tunnel-junction-coupled lasers (two-stage), single-stage lasers with only one active region were produced. In the case of a single-stage laser, the aforementioned structure was simply capped with a highly-doped GaAs cap layer for metallization. For a two-stage laser, a reverse-biased tunnel junction was grown at 480°C before an identical laser structure was grown, followed by the highly doped contact layers. The single and two stage laser structures are shown in Figure 2-23 and Figure 2-24, respectively.

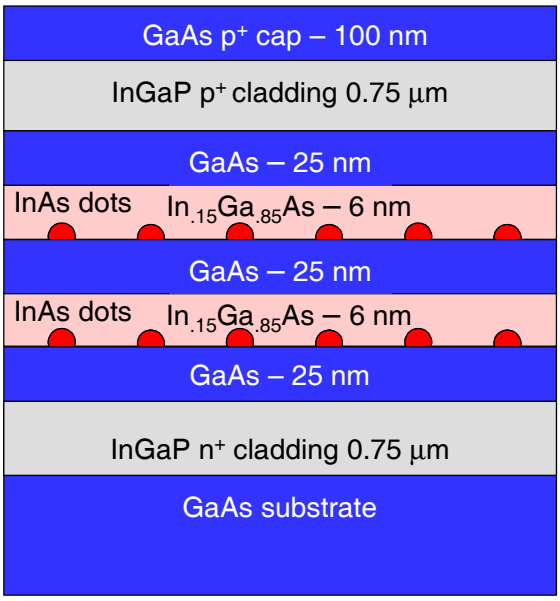


Figure 2-23: Epitaxial structure of single-stage 1310 nm quantum dot laser.

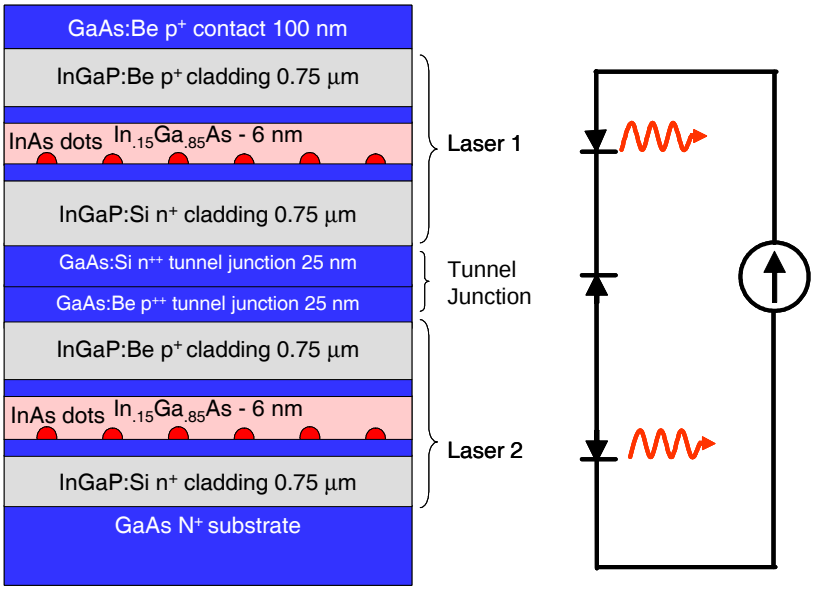


Figure 2-24: The epitaxial structure of the entire two-stage quantum dot laser with tunnel junction.

Single and two stage lasers were fabricated, the latter both with and without indium in the tunnel junctions. Additionally, $In_{0.20}Ga_{0.80}As$ quantum well lasers emitting at

980 nm with and without indium tunnel junctions were deposited to confirm and to expand upon prior work [12, 13].

2.8 Laser Fabrication

Oxide stripe lasers were fabricated from the epitaxial laser structures. These relatively simple lasers consist of a stripe of metal in contact with the semiconductor with isolation between devices. The lasers are gain-guided, as opposed to index-guided devices such as ridge-waveguide lasers. In a gain-guided laser, the injected current induces a population inversion in the region beneath the ohmic contact. If the gain within the semiconductor is high enough, the optical mode will guide along the region of high gain despite the absence of an index-contrast structure such as a waveguide. However, the requirement of extremely high gain generally means that greater electrical pumping is required than for an index-guided device. Therefore, their simpler fabrication is attractive but not ideal for devices with weak gain or devices where high optical power is desirable.

The initial devices used a 250-nm thick layer of hydrogensilsesquioxane (HSQ), a low-k dielectric spin-on insulator, as the isolation layer. This was chosen due to the relative ease of processing with a spin-on insulator as opposed to a silicon dioxide or silicon nitride deposition by physical or chemical vapor deposition. The HSQ that was used was Dow Corning Fox 16 and it was combined with methyl isobutyl ketone (MIBK) in the ratio 1:1.5 (HSQ:MIBK) to achieve thinner layer thickness. The mixture was spun at 3000 rpm on a vacuum chuck spinner to achieve the desired thickness. After two short hotplate bakes of 150°C for 2 minutes and 200°C for 2 minutes, a 400°C curing bake in a nitrogen tube furnace is performed to drive off the solvent and to densify the HSQ into a solid with properties similar to SiO_2. However, initial work with HSQ found that HSQ is very susceptible to crystallization in the liquid phase leading to pitting and crystallites in the solid film (Figure 2-25). Upon etching, these pinholes can lead to micromasking of the underlying semiconductor, particularly during reactive ion etching.

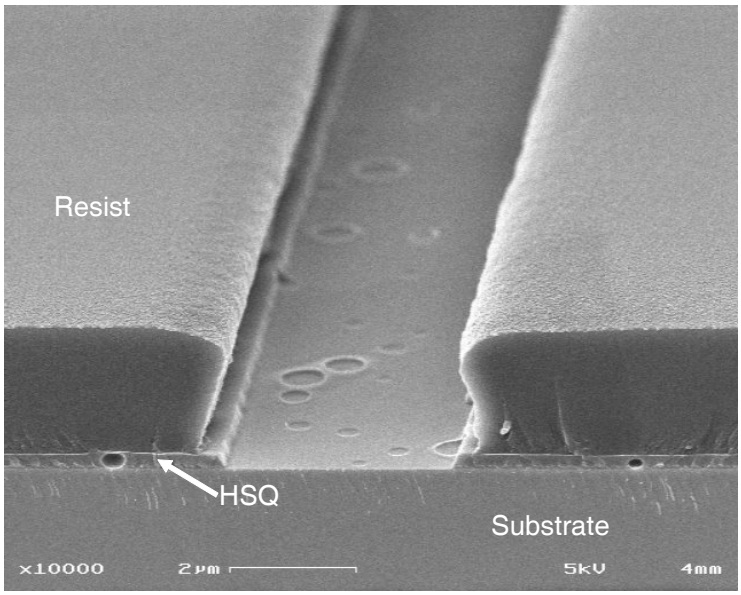


Figure 2-25: Semiconductor surface after a dry etch of HSQ. Crystallites and pinholes in the HSQ lead to micromasking and cratering of the semiconductor.

Plasma etching also leads to undesirable damage to the surface of the semiconductor surface that will eventually be used for an ohmic contacts. Owing to high-energy ion bombardment, the plasma induced surface damage can cause degraded performance of the ohmic contact and electrical performance. Therefore, wet etching is a more desirable processing technique for this application, particularly with the relative process insensitivity of the large feature sizes involved.

As a result, plasma-enhanced chemical vapor deposition (PECVD) was chosen to deposit 250 nm of SiO_2. Photolithography and a 10:1 H_2O:HF etch is used to pattern stripes into the insulator. The stripes vary from 5 to 50 μm wide. Next, image-reversal photolithography is performed again to generate a liftoff pattern for the subsequent Ti/Pt/Au metallization. Once the liftoff process is completed, the back of the sample is lapped with 6 μm alumina grit to thin the substrate to 150-200 μm thick. Ti/Pt/Au is deposited on the backside and the whole structure is rapid thermal annealed at 380°C. Nomarski micrographs of completed laser structures are shown in Figure 2-27. More detailed descriptions of the processing techniques are included in Chapter 3.

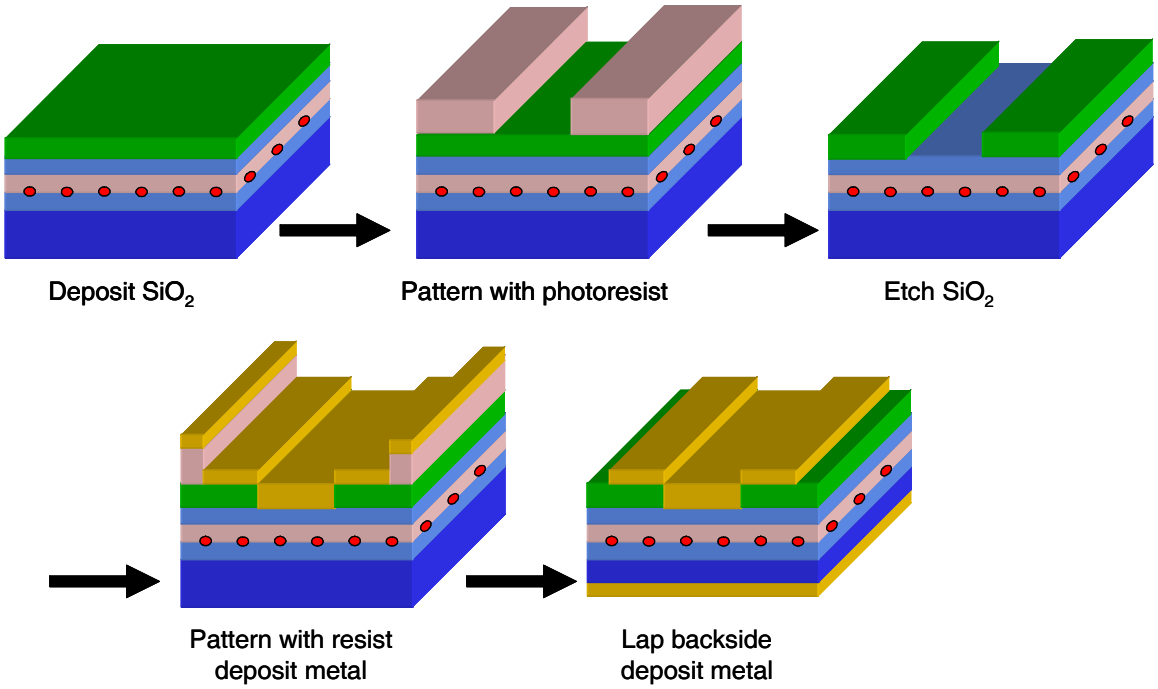
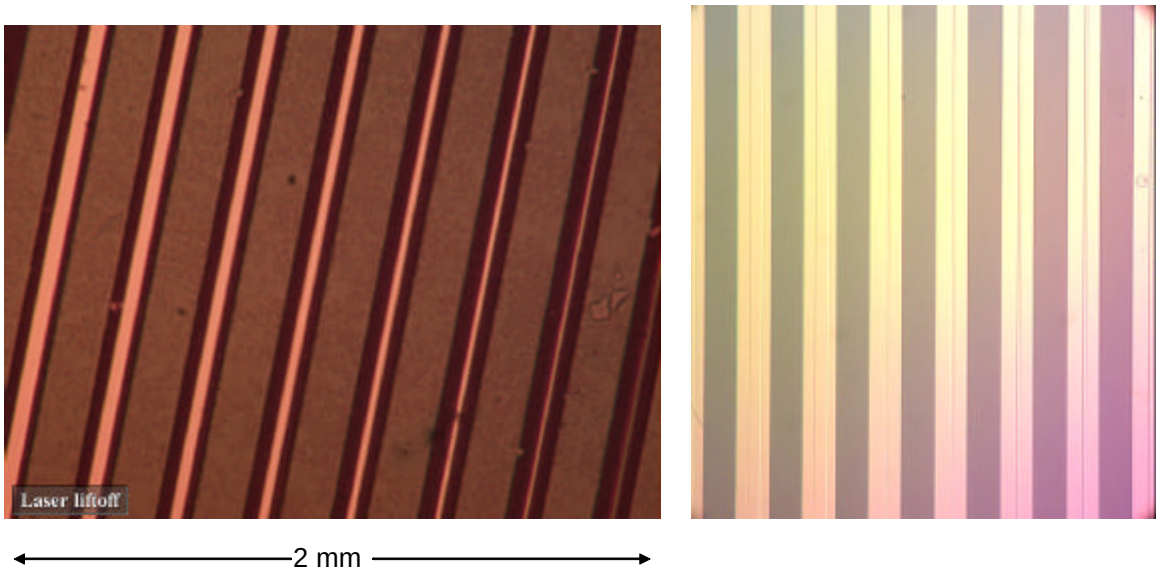
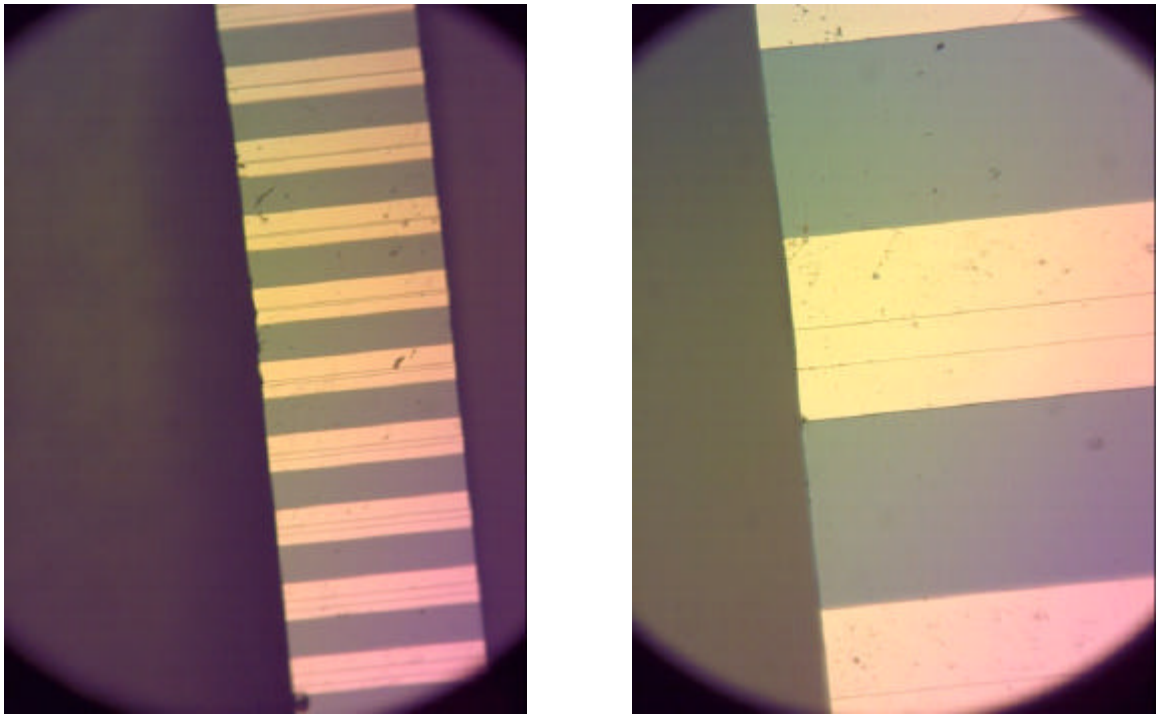


Figure 2-26: The process flow for gain-guided oxide strip lasers.



a) b)



c) d)

Figure 2-27: Nomarski micrograph of fabricated lasers. Metal (Ti/Pt/Au) stripes are 100 μm wide and oxide windows vary from 1-50 μm in width.

2.9 Laser Testing

2.9.1 Testing Configuration

Once fabricated, initial testing of the lasers was performed. The testing setup, as shown in Figure 2-28, involved a Newport 5005 laser diode driver as the current source for the laser. The emitted light was then collected by an InGaAs photodetector connected to an ILX Lightprobe optical multimeter (OMM-6810B). The sample is mounted on thermoelectrically-cooled stage controlled by a Newport 3040 temperature controller (not shown).

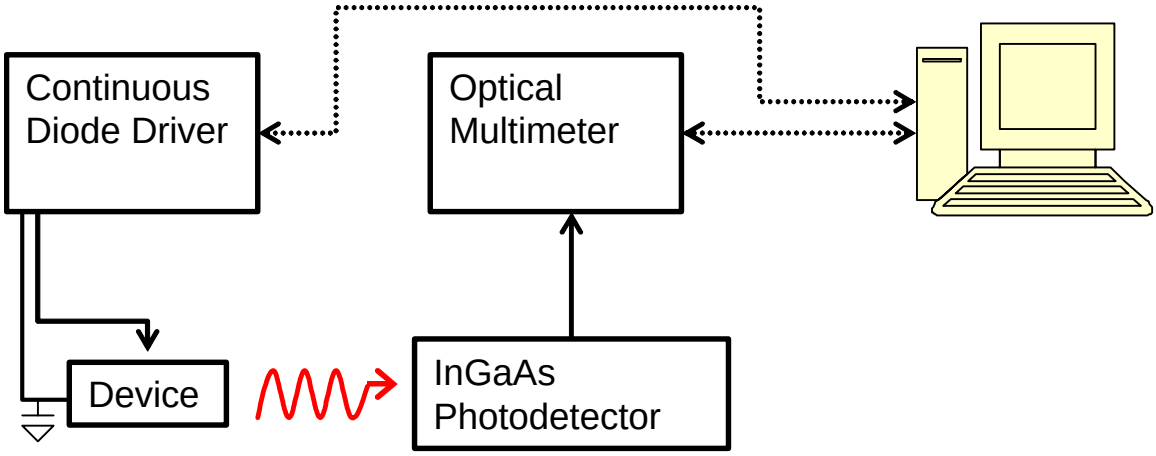


Figure 2-28: The lasers were driven using a laser diode drive current source and their output was measured using an InGaAs photodetector [50].

Using an optical spectrum analyzer, the electroluminesence spectrum was collected. The laser showed emission at 1330 nm as shown in Figure 2-29. Laser output was limited under room-temperature, continuous wave operation by significant Joule heating.

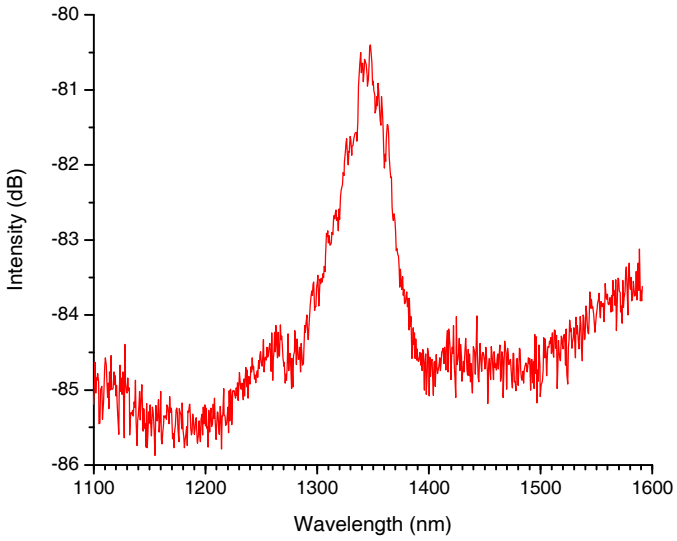


Figure 2-29: Electroluminesence of lasers showed emission within the 1310 nm range.

In order to reduce the excessive heating of the lasers, the lasers' heatsink was improved. The lasers were placed upon well-cleaned copper (Cu) mounts where both the backside of the laser and the front-side of the mount were coated with Ti/Pt/Au (500Å/1000Å/300Å). Subsequently, 2 μm of indium was deposited on the Cu mount to serve as a low-temperature solder. The choice of indium is not accidental, In is chosen because it has a coefficient of thermal expansion (CTE) which closely matches that of copper. Prior to bonding, the indium layer is scrubbed with a fluorine-based flux, rinsed with water and methanol, and then dried with nitrogen to ensure that no surface oxide resides on the indium and promote good adhesion and thermal contact with the laser. Finally, the laser samples were placed on top of the In/Cu mount and alloyed using a carbon strip heater in the presence of an N_2 atmosphere to prevent oxidation. During heating, pressure is applied using an electrical probe tip to encourage better adhesion. Samples mounted on CuW with AuSn solder – again CTE matched – were also prepared and showed improved electrical characteristics as well as greater mechanical stability.

2.9.2 Laser Testing Results

The single-stage and two-stage lasers were first cleaved to lengths of 930 μm and 1002 μm, respectively, and then were mounted using the heatsink method that was discussed earlier. All measurements are normalized for the cavity length. The majority of the quantum dot laser testing was performed in conjunction with Sue Y. Young and is discussed in her thesis [50].

The first measurement performed on the quantum dot lasers was a measurement of the current-voltage (IV) characteristics to confirm that the lasers exhibited diode behavior. The IV curve is shown in Figure 2-30 and shows that each laser has a diode-like behavior and has a clear turn-on voltage. As expected, the two diodes in series that comprise the two-stage laser will each have a voltage drop across them, in addition to the voltage drop across the tunnel junction. Therefore, the two-stage laser has a voltage drop more than double that of the single-stage laser. However, the voltage drops in all cases are unusually large, indicating the presence of additional parasitic resistances in the device. These resistances are likely contributing to the heating observed during testing of the light output characteristics

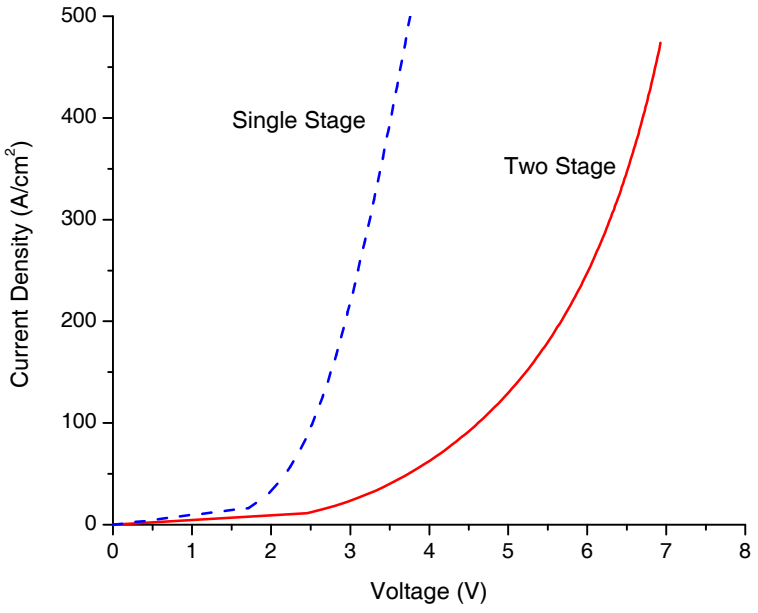


Figure 2-30: Current-voltage (IV) measurements for the single-stage and two-stage quantum dot lasers.

Having confirmed the diode-like behavior of the lasers, the light output was measured by varying the current and monitoring the power of the light impinging on the photodetector. The light intensity-current density (LI) curve is shown in Figure 2-31. The light output of the lasers is very weak, most likely a result of the significant heating of the device. The poor lattice matching of the $In_{0.49}Ga_{0.51}P$ cladding layers could have caused dislocations in the epitaxial structure, created strain in the quantum dot region, or caused other effects that are leading to nonradiative recombination and heating of the device. Heating of the device increases the amount of spontaneous emission and therefore increases the number of injected electrons required to maintain a population inversion. Despite the poor output of the lasers, there are some encouraging results contained in the LI curve. The slope of the LI curve is a measure of the quantum efficiency of the device – the number of emitted photons per injected electron – and the two-stage laser has a slope that is more than triple that of the single stage laser when normalized for the area [50].

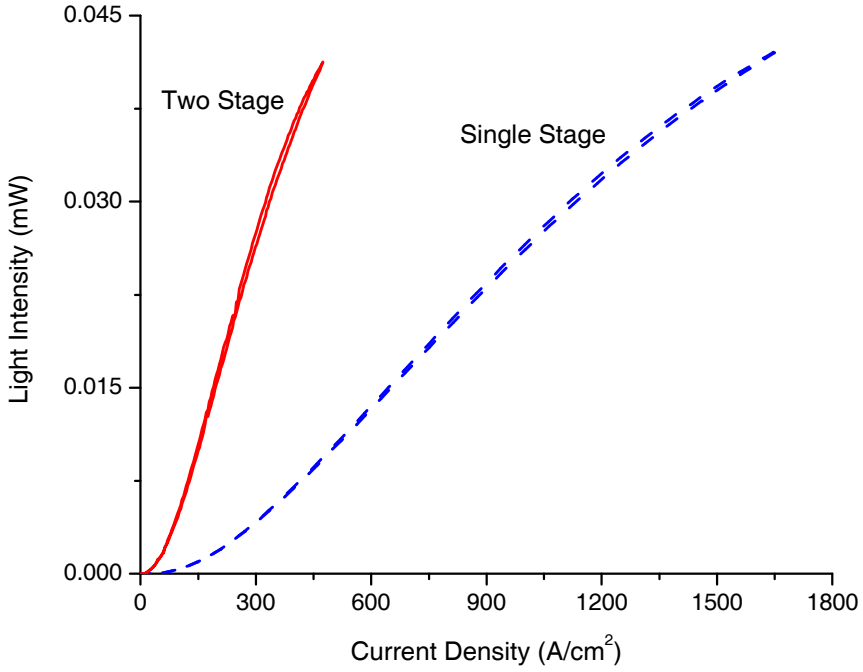


Figure 2-31: The light intensity versus current density (LI) curve of the quantum dot lasers. The greater slope of the two-stage laser indicates the higher quantum efficiency of the two-stage device [50].

2.10 Conclusions

Tunnel junctions, or Esaki junctions, are p-n diodes degenerately doped so that the quasi-Fermi level resides within the band edge. Various $In_xGa_{1-x}As$ tunnel junctions were fabricated with indium concentrations of x=0, 5, 10, and 15% and the reverse-biased tunneling current increases with increasing indium concentration. In addition to the tunnel-junction-coupled lasers in this study, the observation of increasing tunneling current with In content could be exploited in a number of optoelectronic devices such as vertical cavity surface emitting lasers (VCSELs) [51] or any application where interband tunneling is desirable.

The photoluminescence results of the InAs quantum dot growth studies revealed that the maximum light output at 1310 nm was achieved for 2.7 monolayers of InAs quantum dot material grown at a substrate temperature of 500°C, an initial growth rate of 0.7 monolayers/sec, a six-second growth interruption after the quantum dot deposition, and an AsH_3 flow of 0.1 sccm corresponding to a reactor pressure of $3.4x10^{-6}$ torr. The intensity of the quantum dot emission was shown to be highly dependent on the arsenic flux in the chamber, with lower fluxes corresponding to higher output, most likely as a result of increased indium diffusion on the surface leading to a more uniform size distribution and higher quality of quantum dots. Gain-guided oxide stripe lasers were fabricated using the optimized quantum dot material and electroluminescent emission was observed at 1310 nm. Significant Joule heating hinders the amount of light generated, but it is possible that operating the lasers under pulsed conditions or cooling them to cryogenic temperatures could increase light output.

2.11 References

1. Knight, J.C., *Photonic crystal fibres.* Nature, 2003. **424**(6950): p. 847-851.
2. Temelkuran, B., et al., *Wavelength-scalable hollow optical fibres with large photonic bandgaps for CO2 laser transmission.* Nature, 2002. **420**(6916): p. 650-653.
3. Partus, F.P., et al., *Optical fiber with low OH impurity and communication system using the optical fiber*. 1995, Lucent Technologies Inc: USA.
4. Schubert, E.F., *Light Emitting Diodes [Electronic Version]*. 2003: Cambridge University Press.
5. Arakawa, Y. and H. Sakaki, *Multidimensional Quantum Well Laser and Temperature-Dependence of Its Threshold Current.* Applied Physics Letters, 1982. **40**(11): p. 939-941.
6. Asada, M., Y. Miyamoto, and Y. Suematsu, *Gain and the Threshold of 3-Dimensional Quantum-Box Lasers.* IEEE Journal of Quantum Electronics, 1986. **22**(9): p. 1915-1921.
7. Arakawa, Y. and A. Yariv, *Quantum-Well Lasers Gain, Spectra, Dynamics.* IEEE Journal of Quantum Electronics, 1986. **22**(9): p. 1887-1899.
8. Huffaker, D.L., et al., *1.3 mu m room-temperature GaAs-based quantum-dot laser.* Applied Physics Letters, 1998. **73**(18): p. 2564-2566.
9. Shernyakov, Y.M., et al., *1.3 mu m GaAs-based laser using quantum dots obtained by activated spinodal decomposition.* Electronics Letters, 1999. **35**(11): p. 898-900.
10. Zhukov, A.E., et al., *Continuous-wave operation of long-wavelength quantum-dot diode laser on a GaAs substrate.* IEEE Photonics Technology Letters, 1999. **11**(11): p. 1345-1347.
11. Leonard, D., et al., *Direct Formation of Quantum-Sized Dots from Uniform Coherent Islands of InGaAs on GaAs-Surfaces.* Applied Physics Letters, 1993. **63**(23): p. 3203-3205.
12. Patterson, S.G., et al., *Temperature characteristics of bipolar cascade lasers.* Applied Physics Letters, 2000. **77**(2): p. 172-174.
13. Patterson, S.G., et al., *Continuous-wave room temperature operation of bipolar cascade laser.* Electronics Letters, 1999. **35**(5): p. 395-397.
14. Garcia, J.C., et al., *Epitaxially stacked lasers with Esaki junctions: A bipolar cascade laser.* Applied Physics Letters, 1997. **71**(26): p. 3752-3754.
15. Schmid, W., et al., *CW operation of a diode cascade InGaAs quantum well VCSEL.* Electronics Letters, 1998. **34**(6): p. 553-555.
16. Kim, J.K., et al., *Epitaxially-stacked multiple-active-region 1.55 mu m lasers for increased differential efficiency.* Applied Physics Letters, 1999. **74**(22): p. 3251-3253.
17. Knodl, T., et al., *Multi-diode cascade VCSEL with 130% differential quantum efficiency at CW room temperature operation.* Electronics Letters, 2001. **37**(1): p. 31-33.
18. Kane, E.O., *Zener Tunneling in semiconductors.* Journal of Physics and Chemistry of Solids, 1959. **12**: p. 181-188.

19. Kane, E.O., *Theory of Tunneling.* Journal of Applied Physics, 1960. **12**(1): p. 83-91.
20. Vegard, L., *Z. Phys.* Z. Phys, 1921. **5**: p. 17.
21. Matthews, J.W. and A.E. Blakeslee, *Defects in Epitaxial Multilayers .1. Misfit Dislocations.* Journal of Crystal Growth, 1974. **27**(DEC): p. 118-125.
22. Matthews, J.W. and A.E. Blakeslee, *Defects in Epitaxial Multilayers .2. Dislocation Pile-Ups, Threading Dislocations, Slip Lines and Cracks.* Journal of Crystal Growth, 1975. **29**(3): p. 273-280.
23. Matthews, J.W. and A.E. Blakeslee, *Defects in Epitaxial Multilayers .3. Preparation of Almost Perfect Multilayers.* Journal of Crystal Growth, 1976. **32**(2): p. 265-273.
24. Burenkov, Y.A., et al., Sov. Phys. Solid State, 1973. **15**(6): p. 1175-1177.
25. Nichols, D.N., D.S. Rimai, and R.J. Sladek, *Elastic Anharmonicity of InP - Its Relationship to the High-Pressure Transition.* Solid State Communications, 1980. **36**(8): p. 667-669.
26. Burenkov, Y.A., S.Y. Davydov, and S.P. Nikanorov, Sov. Phys. Solid State, 1975. **17**(7): p. 1446-1447.
27. Yogurtcu, Y., A. Miller, and G. Saunders, *Pressure dependence of elastic behaviour and force constants of GaP.* J. Phys Chem. Solids, 1981. **42**(1): p. 49-56.
28. Stokes, R.a.E., D.F., *Fundamentals of Interfacial Engineering*. 1997: Wiley-Vich.
29. Horikoshi, Y., *Migration-Enhanced Epitaxy of GaAs and AlGaAs.* Semiconductor Science and Technology, 1993. **8**(6): p. 1032-1051.
30. Yeh, N.T., et al., *Matrix dependence of strain-induced wavelength shift in self-assembled InAs quantum-dot heterostructures.* Applied Physics Letters, 2000. **76**(12): p. 1567-1569.
31. Marzin, J.Y. and G. Bastard, *Calculation of the Energy-Levels in InAs/GaAs Quantum Dots.* Solid State Communications, 1994. **92**(5): p. 437-442.
32. Lee, H.S., et al., *Dependence of the InAs size distribution on the stacked layer number for vertically stacked InAs/GaAs quantum dots.* Journal of Crystal Growth, 2002. **241**(1-2): p. 63-68.
33. Dobbs, H.T., et al., *Mean-field theory of quantum dot formation.* Physical Review Letters, 1997. **79**(5): p. 897-900.
34. da Silva, M.J., et al., *Maximization of the InAs quantum-dot density through the growth of an intentionally non-homogeneous sample.* Journal of Crystal Growth, 2002. **236**(1-3): p. 41-45.
35. Liu, G.T., et al., *The influence of quantum-well composition on the performance of quantum dot lasers using InAs/InGaAs dots-in-a-well (DWELL) structures.* IEEE Journal of Quantum Electronics, 2000. **36**(11): p. 1272-1279.
36. Groom, K.M., et al., *Comparative study of InGaAs quantum dot lasers with different degrees of dot layer confinement.* Applied Physics Letters, 2002. **81**(1): p. 1-3.
37. Srivastava, G.P. and S.J. Jenkins, *Atomic geometry and bonding on the GaAs(001)-beta 2(2x4) surface from ab initio pseudopotential calculations.* Physical Review B, 1996. **53**(19): p. 12589-12592.
38. Moll, N., et al., *GaAs equilibrium crystal shape from first principles.* Physical Review B, 1996. **54**(12): p. 8844-8855.

39. Asryan, L.V. and R.A. Suris, *Inhomogeneous line broadening and the threshold current density of a semiconductor quantum dot laser.* Semiconductor Science and Technology, 1996. **11**(4): p. 554-567.
40. Riel, B.J., et al., *InAs/GaAs(100) self-assembled quantum dots: Arsenic pressure and capping effects.* Journal of Crystal Growth, 2002. **236**(1-3): p. 145-154.
41. Rasband, W., *Scion Image for Windows*. 2000, Scion Corporation.
42. Yasuda, H., et al., *Arsenic flux dependence of InAs nanostructure formation on GaAs (211) B surface.* Applied Surface Science, 2000. **166**(1-4): p. 413-417.
43. Yamaguchi, K., K. Yujobo, and T. Kaizu, *Stranski-Krastanov growth of InAs quantum dots with narrow size distribution.* Japanese Journal of Applied Physics Part 2-Letters, 2000. **39**(12A): p. L1245-L1248.
44. Jeon, S.R., et al., *Lateral current spreading in GaN-based light-emitting diodes utilizing tunnel contact junctions.* Applied Physics Letters, 2001. **78**(21): p. 3265-3267.
45. Wierer, J.J., N. Holonyak Jr., and P.W. Evans, *United States Patent 5936266: Semiconductor devices and methods with tunnel contact hole sources*. 08/10/1999, The Board of Trustees of The University of Illinois: United States.
46. Jayaraman, V., et al., *High-power 1320-nm wafer-bonded VCSELs with tunnel junctions.* IEEE Photonics Technology Letters, 2003. **15**(11): p. 1495-1497.
47. Ortsiefer, M., et al., *Low-resistance InGa(Al)As tunnel junctions for long wavelength vertical-cavity surface-emitting lasers.* Japanese Journal of Applied Physics Part 1-Regular Papers Short Notes & Review Papers, 2000. **39**(4A): p. 1727-1729.
48. Fatemi, M., *Refinement of high-resolution X-ray diffraction data in characterizing epitaxial layers and multiple-quantum wells by the peak separation technique.* Journal of Crystal Growth, 1999. **207**(3): p. 188-199.
49. Fatemi, M., et al., *High-Resolution X-Ray-Analysis of Strain in Low-Temperature GaAs.* Physical Review B, 1993. **48**(12): p. 8911-8917.
50. Young, S.Y., *Characterization of Novel III-V Semiconductor Devices*, in *Electrical Engineering*. 2006, Massachusetts Institute of Technology.
51. Kim, J.K., et al., *Room-temperature, electrically-pumped multiple-active-region VCSELs with high differential efficiency at 1.55 mu m.* Electronics Letters, 1999. **35**(13): p. 1084-1085.

CHAPTER 3

Optical Logic

3.1 Photonic Switches

While optical-electronic-optical (OEO) conversions have been recognized as a fundamental rate limiting mechanism in data transmission, there remains no viable commercial alternative. Electronic routing is a mature technology, widely and densely integrated, and highly reliable. The optical analogs to the electronic transistors, buffers, and amplifiers that comprise the logic elements of routers and switches remain either in development or non-existent. Photonic switching could eliminate these OEO bottlenecks, delivering channel rates in excess of 100 Gb/s [1, 2]. However, this advance depends critically on the development of technologies in the photonic realm that are analogous or equivalent to current electronic components. Furthermore, these

photonic components must have the potential for monolithic integration in order to duplicate the performance of electronic systems within similar size, weight, energy consumption, and economic constraints. While fundamental physical limitations dictate larger sizes for optical devices than electronic devices, there are still many applications where photonic components offer equivalent or superior performance to their electronic counterparts.

Besides speed and capacity, there are added benefits to moving towards all-optical switching technologies. Power consumption is greatly reduced in optical switches, some experiments placing it as low as 2 pJ per bit [3]. Additionally, optical switches have more potential for scalability than electronic routers [1].

Just as electronic circuits evolved from discrete components, this thesis investigates elementary optical logic units that can be integrated into more complex device configurations for optical packet switching. The fundamental technology is the asymmetric twin-waveguide (ATG). This technology e enables optical circuits to be manufactured with both active and passive components using only one epitaxial growth followed by a fabrication sequence; this scheme greatly eases further monolithic integration of subsequent devices and components when compared with other integration techniques. The asymmetric twin-waveguide semiconductor optical amplifier (ATG-SOA) is used in a Mach-Zehnder interferometer configuration to demonstrate an optical logic unit cell with Boolean XOR functionality, the photonic equivalent of transistor-transistor-logic (TTL).

Once implemented, this technology has wide-ranging applications in communications technology. Low earth orbit (LEO) based free-space optical networks begin to outperform their radio-frequency counterparts at data rates in excess of 1 Gb/s [4]. In addition to terrestrial optical fiber lightwave networks, these satellite networks could also benefit from the increased data processing rates and expected reductions in size, weight, and power consumption offered by all-optical switches [5]. Additionally, the asymmetric twin-waveguide technology provides a platform for more complex and variable device integrations, as has already been demonstrated [6-9].

3.2 All-Optical Packet Switching

Electronic networking technology is widely implemented in existing lightwave networks. 10 Gb/s technologies have been installed extensively with 40 Gb/s components beginning to enter the marketplace [10]. The next generation of devices operating at 100 Gb/s and 160 Gb/s will exceed the limitations of electronic signal processing and OEO conversions will impose a fundamental limit upon transmission and reception rates [11]

There are two primary functions of switching components in fiber optic networks. The first is routing, the process by which data is directed to the correct destination. The second is signal regeneration to restore the integrity of the data after transmission. Attenuation and dispersion are the two most important causes of signal degeneration in optical fibers. Attenuation, or loss, is the absorption of the optical signal into the transmission medium and/or loss to the ambient environment. Chromatic dispersion is the smearing of the optical signal within the time domain whereby the distinction between optical pulses is lost. Figure 3-1 illustrates the two principles for a return-to-zero (RZ) data stream.

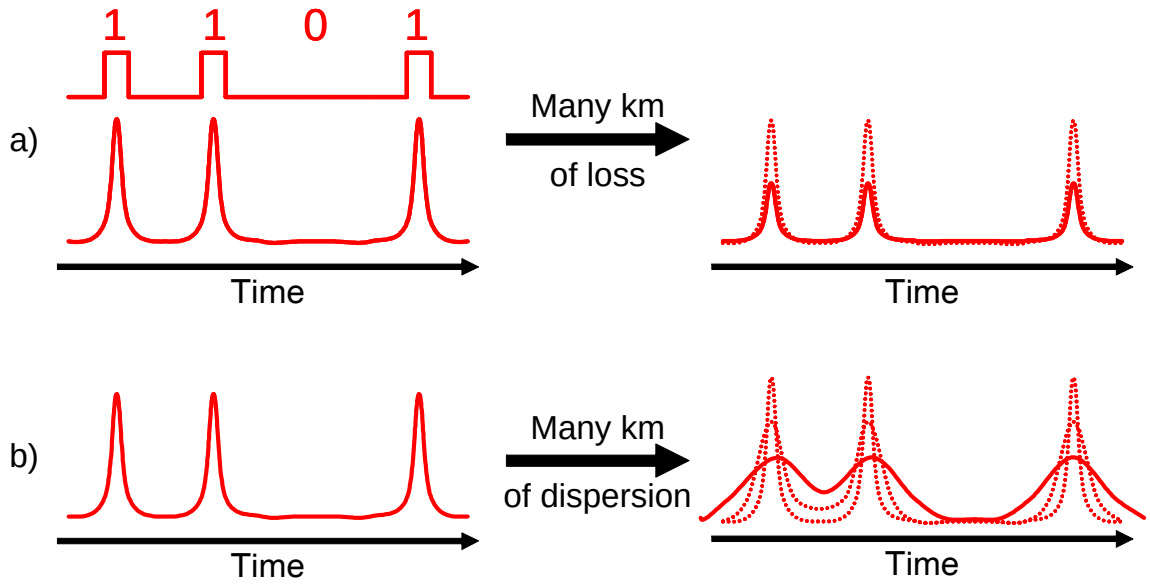


Figure 3-1: Signal degeneration in an optical fiber is primarily caused by a) attenuation and b) dispersion.

In order to compensate for this signal degradation, periodic regeneration of the optical signal is necessary, particularly at data rates in excess of 100 Gb/s where dispersion compensation in erbium-doped fiber amplifiers (EDFAs) becomes a serious problem. The data pulses must be re-amplified, re-timed, and re-shaped: so-called 3R regeneration. In an electronic switch, these functions are accomplished automatically because the signal is regenerated at every switching node as part of the OEO conversion. This same functionality must be duplicated in all-optical switching along with a fourth-R, re-polarization. The all-optical regeneration must be stable, polarization insensitive, and, ideally, wavelength maintaining [12].

3.3 Monolithic Integration

The idea of photonic integration is not a new one. As early as 1969, investigators were considering the cost and performance benefits of integrating photonic components on the same substrate [13]. Discrete components, such as lasers, modulators, and detectors were already available but relied on free-space transmission from device to device. Systems were assembled by mounting and precisely aligning devices on large optical tables sensitive to acoustic vibrations and thermal fluctuations. Taking a cue from microelectronics, the integration of multiple optical functions on the same chip using similar photolithographic techniques appeared highly desirable. Additionally, the small feature size and optical confinement opened the possibility of achieving non-linear affects at moderate power levels [13].

Elementary integration did not reach the InP materials platform for quite some time. Following similar developments in the GaAs system [14], the first practical integration was in 1984 with the integration of a laser diode with a heterojunction bipolar transistor, enabling drive electronics to be integrated with the associated laser. In the late 1980s, InP lasers and modulators were first integrated [15, 16] as an alternative to the direct-modulation of lasers at high speeds or the packaging and alignment difficulties inherent to discrete components. The next leap in integration came with the development of the arrayed waveguide grating (AWG) routers which allowed up to eight receivers to be incorporated on the same substrate [17-19]. It was not until a decade later that the next large leap in integration came with more 50 components (distributed-

feedback lasers, optical polarization modulators, electro-absorption modulators, variable optical attenuators, AWG), being integrated into an optoelectronic integrated circuit capable of transmitting data at 10 Gb/s on ten different channels [20].

The relatively slow pace of integration in optical components, particularly when compared to the explosive Moore's Law growth of microelectronic integration in the silicon integrated circuit industry, is due to a number of different reasons. For one, the processing of integrated circuits and photonic components is substantially different. Remarkably, even the processing of InP electronics is not necessarily similar to InP photonics manufacturing. Integrated circuit processing has been driven by continued improvement in optical lithography, with each successive equipment generation enabling denser integration. Instead, the fabrication of photonic components relies much more heavily on such technologies as plasma etching and epitaxy [20]. Photonic components are not scalable in the same way as integrated circuits. In fact, the size of photonic components is generally limited by the associated wavelength and dimensions much below that do not generally offer compelling performance enhancements and in many cases would actually degrade operation. Photonic bandgap materials are an exception to these size limitations, but they still do not match the extremely small sizes and high densities of electronic components. Additionally, photonic design requirements are much different than integrated circuits, with each component often requiring a unique set of electrical and optical properties. More often than not these demands are in competition, if not in outright opposition, to each other. Lastly, there simply have not been compelling economic and industrial drivers for integrated optical components. In short, the existing discrete technology was good enough and integration did not offer a persuasive economic benefit. Only recently, with network carriers beginning to feel the strain of increased user demand for higher-speed data connections has there been a convincing economic case for more complex integration.

3.3.1 Integration Techniques

There are a number of different approaches to integrating active devices such as lasers and SOAs with passive components such as waveguides and couplers, each having different advantages and disadvantages. Most of the important techniques are illustrated in Figure 3-2.

The first and perhaps the most obvious technique is regrowth. In this process, a device is epitaxially deposited and then fabricated. Subsequent materials are then regrown over the existing wafer and devices are further fabricated. This process is repeated for each integrated component [21-25]. The advantage is that the integration can be achieved within a single plane and each device can be individually optimized both in epitaxy and fabrication [26]. However, epitaxial growth is extremely sensitive to the initial conditions on the substrate surface. The intermediate processing steps can introduce a substantial amount of physical and chemical damage to the surface resulting in the growth of subsequent material that is of lesser quality than had it been grown on virgin semiconductor. Immediately prior to subsequent growth, extensive cleaning of the surface must be done *in-situ*, usually accomplished in MBE by exposing the wafer to atomic hydrogen at low-temperatures (200°C) to rid the surface of impurities and assist in oxide removal [27]. For MOCVD growth, the sample surface is prepared for regrowth through a series of plasma and wet etches [28]. Additionally, the alternating active and passive components will have abrupt changes in the refractive index in the propagation direction causing undesirable reflections and diminished transmission. Due to the challenging and complicated nature of this process, it is not ideal for high-volume manufacturing where considerations such as cost and yield are paramount. Nonetheless, the endfire or butt coupling technique has been used to integrate a wide variety of optoelectronic devices such as DFB lasers, filters, semiconductor optical amplifiers, modulators, and waveguides.

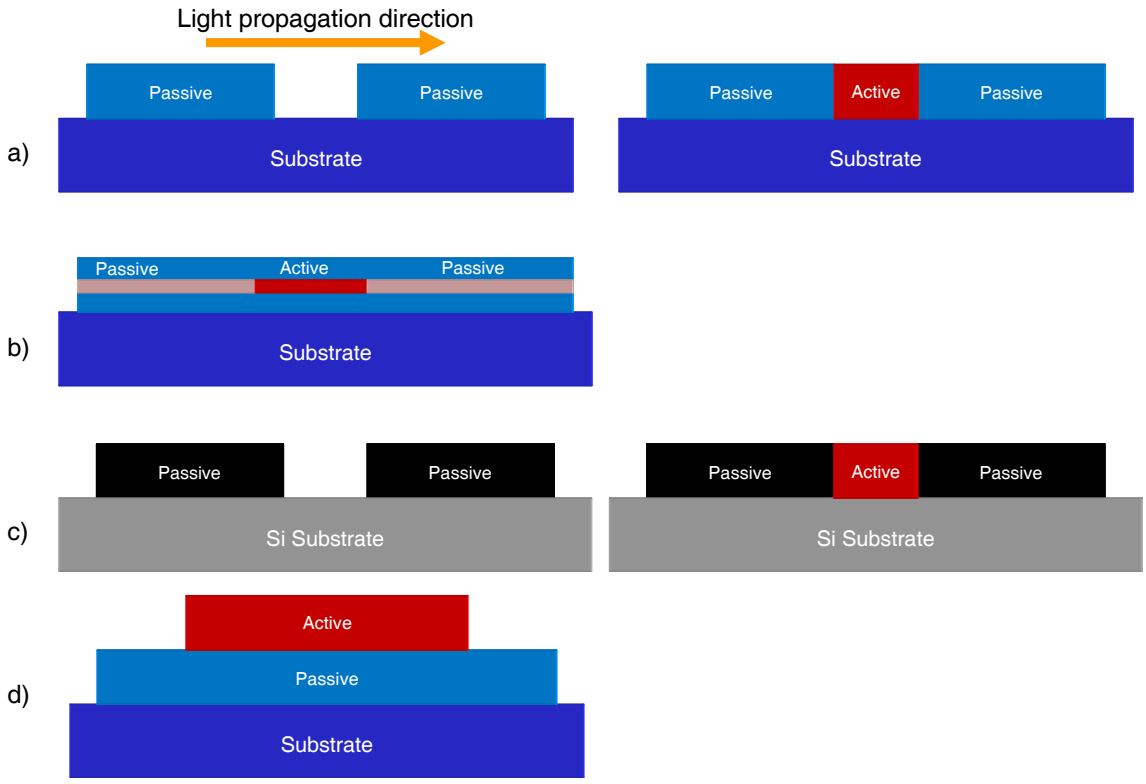


Figure 3-2: Techniques for monolithic integration include a) regrowth, b) quantum well intermixing, c) hybrid integration, and d) twin waveguides.

Another integration technique which has been investigated extensively is quantum well intermixing [29-32]. In this technique, both the passive and active regions of the sample are grown in one epitaxial growth. Subsequently, selective areas on the surface are heated to induce localized diffusion. By locally heating one area of the surface with, say, a laser, the materials within the quantum well will diffuse into the barrier layers. The diffusion can be partial, with the quantum wells retained albeit at different compositions and thickness, or it can be complete, with the quantum wells completely interdiffused with the barrier layers to form a bulk material with an averaged composition. The diffusion process can be enhanced and patterned by the presence of vacancies that are introduced by selectively depositing dielectric materials on the surface of the wafer [31, 33, 34]. Vacancies formed underneath the dielectric then aid in the intermixing of only the material directly below. Quantum well intermixing is attractive because it reduces the number of epitaxial growths and offers the possibility of coplanar

active and passive devices. However, control over this interdiffusion process is imprecise. A rapid thermal annealing (RTA) cycle [35] will heat the entire wafer, which may be undesirable. Laser-induced heating can be localized, but only to relatively large areas on the order of a few hundred microns. The diffusion process can actually be detrimental to device processing because dopants may diffuse into gain regions and introduce loss via free carrier absorption. Additionally, the shift in bandgap is relatively small, usually around a few hundred meV. This small difference between bandgaps limits the operational window for the device.

Hybrid integration is a third technique and can be implemented in a number of ways [36-40]. In its most simple form, components are fabricated separately and then assembled on a host chip, combining features such as III-V lasers with waveguides on a silicon wafer [36]. The scheme is attractive because each device can be grown and fabricated separately, so no design compromises are necessary and each device can be independently optimized. Furthermore, if implemented correctly the technique is versatile and flexible enough to allow for the integration of a wide variety of devices that might otherwise be impractical to integrate using another scheme. The actual integration can be performed in any number of ways, including flip-chip bonding, magnetically or geometrically self-assembling chips, and brute force pick-and-place. The key detriment to this technique, particularly for photonic devices, is that alignment control is imprecise and coupling between devices can suffer as a result. Additionally, lightwaves usually must travel through free space from device to device leading to undesirable reflections and scattering.

3.4 Asymmetric Twin-Waveguide Semiconductor Optical Amplifier

3.4.1 Twin Waveguides

The basic structure of the asymmetric twin-waveguide semiconductor optical amplifier (Figure 3-3) is active gain components lying above an underlying passive waveguide circuit. The active devices are comprised of materials with higher refractive indices so the light mode naturally migrates into the active devices. This migration is aided, and critically dependent upon, adiabatic tapers which gently guide the mode from

the underlying passive waveguides into the active devices, thereby minimizing the coupling loss [7]. The sequence for a traveling light pulse is shown in Figure 3-4: the lightwave is transmitted through the passive waveguide, evanescently coupled into the active device by the taper, amplified in the active region, and then returned by another taper to the passive waveguide from where the light proceeds to the next component. Electric current to power the active device flows perpendicular to the structures from a topside contact, through the active region, and to another contact either on the top or bottom of the wafer.

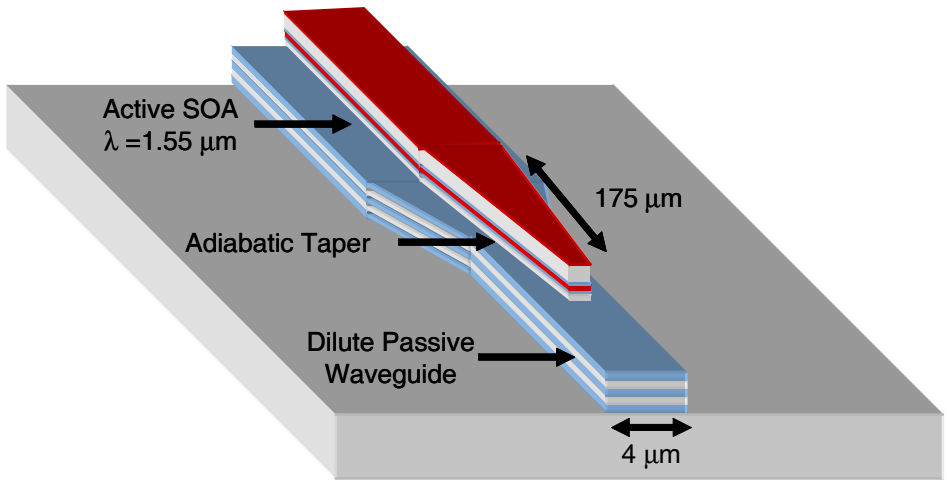


Figure 3-3: The asymmetric twin-waveguide semiconductor optical amplifier.

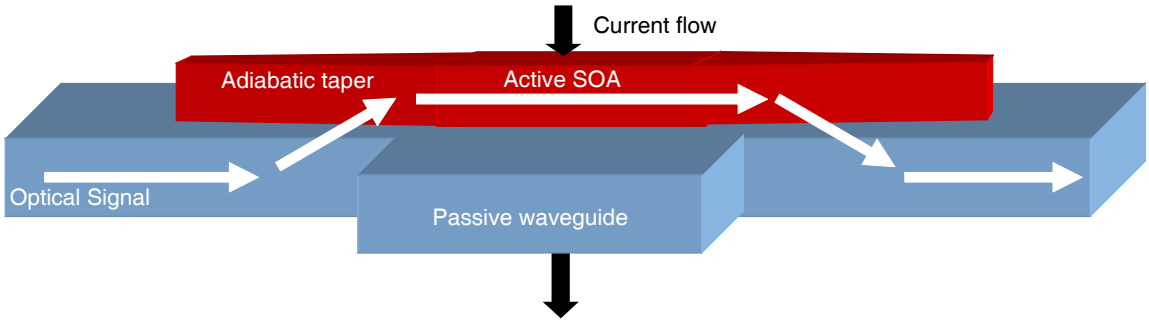


Figure 3-4: Lightwave propagation in asymmetric twin-waveguide semiconductor optical amplifier (ATG-SOA). Light travels within the passive waveguides and then couples into the higher index active waveguide via an adiabatic taper that is designed to minimize coupling losses.

The twin waveguide technique was first proposed and demonstrated in 1975 by Suematsu, *et al*. [41]. The key insight of this design is that by vertically integrating an active and passive waveguide together, photon energy can be transferred between them. The entire structure can be grown epitaxially as a single heterostructure and the devices can be fabricated using standard fabrication techniques such as lithography and etching. Suematsu's original design integrated AlGaAs lasers with passive waveguides as the basis for a photonic circuit [41]. Later work by Campbell and Bellavance [42] expanded and improved upon the design. A key feature common to all of the twin-waveguide designs is that the lower passive level has a higher bandgap, ensuring that the passive waveguide is transparent to the propagating light and absorption will be minimized.

In these earlier designs, the power transfer between the active and passive structures occurs via evanescent coupling where the radiation "leaking" from the active region excites modes in the passive waveguide [42]. The structures were symmetric designs in that both the even and odd modes have equal confinement factors in each of the two layers [43], that is, the effective indices of the two layers are the same [44]. Therefore, precise control over the composition and thickness of the epitaxial layers was required, a problem aggravated by the imprecision of vapor phase deposition methods available at the time. Additionally, the two layers needed to be close to each other to maximize the overlap of the evanescent fields leaking from one waveguide to the other. Even with optimization, coupling efficiencies in excess of 25% were not achieved [42].

To address many of the problems inherent to the symmetric twin-waveguide design, Studenkov, *et al*. [7, 8, 45], developed the asymmetric twin-waveguide (ATG), the design that is used in this thesis. The asymmetry refers to the differing effective indices between the active and passive layers. Therefore, the even and odd mode will encounter different refractive indices, propagate differently, and will not couple with each other. In this design, the even mode is concentrated in the active region and the odd in the passive region. With electrical pumping, the active region will have gain and the even mode will dominate in the twin-waveguide region.

The lack of coupling seems to be antithetical to the design objectives of the twin-waveguide. The key to resolving the absence of coupling is the adiabatic taper [44]. By

slowly varying the width of the active waveguide, the effective index of the waveguide will also slowly change. At a particular width, the active and passive waveguides will be locally symmetric, have matching effective indices, and a strong local resonance will exist between the two modes. Therefore, there will be strong coupling and optical power will be transferred from one mode to the other. In effect, the light will very suddenly "jump" between the two waveguides at a particular point along the taper [43, 44]. The final width of the taper is sufficiently small, less than 1 μm, to ensure that the taper's effective index is insignificant, to minimize any reflections, and to maximize coupling. To avoid confusion, adiabatic, as used in this context, refers to the very slow variation of the taper width, as in a slowly varying Hamiltonian of a system in quantum mechanics.

One advantage of the asymmetric twin-waveguide is that the active region can be used for any number of devices, such as lasers, SOAs, modulators, photodetectors, and other components [46-49]. By altering the electrical injection current, the active region can be operated in any of three regimes: loss, transparency, or gain. In all of the devices presented in this thesis, the active region is configured as a semiconductor optical amplifier where the propagating light has just a single pass through the gain region. A SOA is the critical component of the proposed optical logic unit cell. Just as several electronic transistors comprise a transistor-transistor logic (TTL) gate, these semiconductor optical amplifiers serve as the components that comprise the optical logic unit cell. When properly configured, these SOAs can be combined into structures that perform a variety of logical operations.

3.5 Design and Optimization

Device fabrication is a time-intensive and costly process. Individual devices can take weeks, even months, to grow, fabricate, and test. Taking an experimental approach to the design of complex devices is simply inefficient. Computer simulation techniques offer a powerful method for the design of photonic devices. In the space of a few hours, many design iterations can be examined to appropriately optimize many of the characteristics of the device. Furthermore, the tolerance of the device to fabrication deviations and perturbations can be estimated to identify critical and sensitive steps of the fabrication process. The design details of the device in this thesis are covered

extensively in the PhD thesis of Aleksandra Markina [43] and information presented here is a summary of that work.

Widely used in the photonics field, the beam propagation method (BPM) is a method for calculating optical modes, modeling waveguide propagation, and determining coupling lengths and losses. A full mathematical treatment of a waveguide would require generating solutions to a full set of Maxwell's equations in three dimensions. BPM involves using the electromagnetic field distribution in one plane to calculate subsequent distribution in the next using the finite difference method. The finite difference method is a technique for developing numerical solutions to differential equations where exact solutions are either impossible or impractical. In effect, by dividing a waveguide into slices and recursively solving for the field distributions in sequential slices, the behavior of the waveguide can be accurately approximated. Specifically, the software program RSoft BeamPROP Version 5.0 was used for BPM calculations.

3.5.1 Epitaxial Structure

Combining both passive and active components into the same epitaxial structure represents a challenging design problem. Considerations must be made for the growth and fabrication requirements as well as fabrication limitations. An improperly designed epitaxial structure can greatly hinder the eventual performance of the photonic device, so special care was taken to ensure the greatest ease of growth and processing, while still meeting the performance requirements of the device.

The photonic device was designed to perform at a wavelength of 1550 nm, the optimal wavelength for long-distance fiber transmission. The material system most commonly used at 1550 nm is based upon indium phosphide (InP) substrates. InP and the related InGaAsP materials system is very flexible and allows precise control over and considerable variation of the bandgap, refractive index, and lattice constant of the epitaxial film. Within the InGaAsP system, all of the materials that comprise the SOA and passive waveguide structure can be deposited, each optimized for its performance requirements. As the device is designed such that current flow is from the topside contact to the backside of the wafer, the substrate has a nominal n-type background

doping of 1-8x10^{18} cm^{-3}. Designs are possible that include both electrical contacts on the wafer's topside, but this scheme would require several additional photolithographic steps.

The passive waveguide ridge is configured as a dilute waveguide. That is, several layers of higher index InGaAsP are embedded within an InP waveguide [50-52]. These higher index layers create a higher "average" index for the entire waveguide ridge than the underlying InP substrate, thus ensuring that the mode stays confined within the waveguide, minimizing leakage and loss into the substrate. A schematic of the passive waveguide epitaxial structure is shown in Figure 3-5. The quaternary material is $In_{0.8}Ga_{0.2}As_{0.45}P_{0.55}$ with a characteristic wavelength of 1180 nm. The whole structure is n-doped with sulfur at a concentration of 5x10^{17} cm^{-3}. The waveguide can be designed using a thick quaternary material, but in order to achieve low effective index, low arsenic compositions would be required. These low concentrations are difficult to achieve using some MBE techniques, particularly gas-source MBE, as arsenic has a much higher sticking coefficient than phosphorus. Furthermore, thick quaternary layers can develop significant strain if the composition is even slightly off from the lattice constant of the substrate. Using a single quaternary composition, the effective index of the dilute waveguide can be precisely tailored by varying the quaternary thickness. An additional advantage of the dilute waveguide approach is that it minimizes the number of quaternary compounds and their accompanying time-intensive MBE or MOCVD film-growth calibrations.

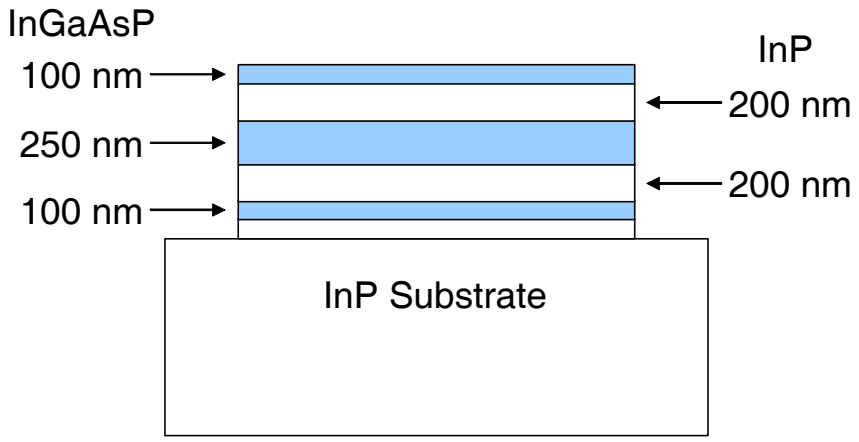


Figure 3-5: Epitaxial structure of dilute passive waveguide

The dilute waveguide structure chosen has 100, 250, and 100 nm thick $In_{0.8}Ga_{0.2}As_{0.45}P_{0.55}$ quaternary layers separated by 200 nm of InP. The refractive indices of InP and the quaternary are 3.167 and 3.29, respectively, yielding an effective index of 3.22 using the weighted squares method. The design was optimized for a ridge waveguide that is 4 μm wide and 1.05 μm tall.

The active portion of the epitaxial structure is a relatively standard double heterostructure configuration that is commonly seen in amplifiers and lasers. The entire epitaxial structure is shown in Figure 3-6. The double heterostructure consists of two tiers of materials with bandgaps smaller than that of the surrounding InP cladding. The active region is centered about a 200 nm thick $In_{0.56}Ga_{0.44}As_{0.94}P_{0.06}$ quaternary layer emitting at 1550 nm in order to amplify the incident data pulse. Electrical and optical confinement is aided by Type I band alignment in which the active region is surrounded by 100 nm of the same 1180 nm quaternary material that is used in the passive waveguide. As quaternary materials can be difficult to calibrate and lattice match, using the same 1180 nm quaternary material greatly simplifies the epitaxial growth. The separate confinement heterostructure aids in the confinement of the optical mode and helps to confine the carriers to the 1550 nm quaternary region. There is no doping in the active region, as doping could lead to deleterious optical losses from free carrier absorption.

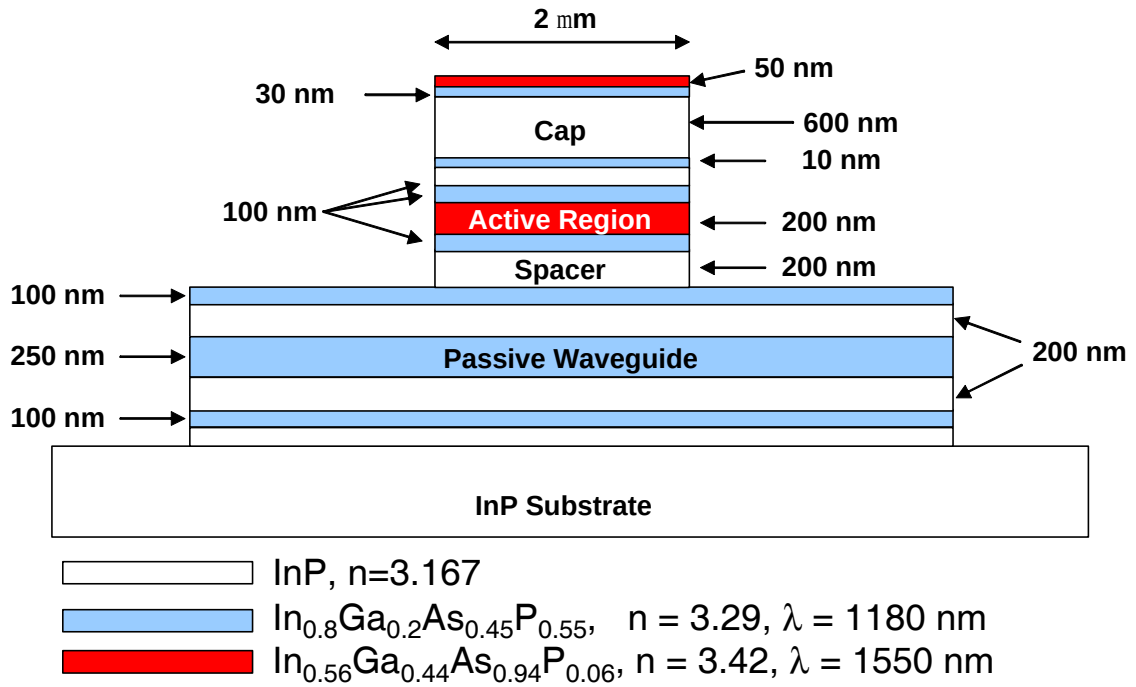


Figure 3-6: Epitaxial heterostructure of passive and active waveguides.

The active region is surrounded with InP to isolate it from the passive waveguide and the ohmic contact material. Simulation of the spacer and cap layer thicknesses were done to optimize the coupling with the passive region and to ensure adequate isolation of the optical mode from the highly doped contact layer. The contact layers help to improve the ohmic contact with the metal that will reside at the very top of the heterostructure. However, the high p-type doping concentration, $2x10^{18}$ cm^{-3}, can lead to excessive loss from free carrier absorption. The cap layers consist of InP, with highly doped 1180 nm and 1550 nm InGaAsP serving as contact layers for the p-type metallization. Using these smaller bandgap materials also helps to minimize the ohmic contact resistance. Simulations showed that the optical power transfer with the passive waveguide was maximized for a cap spacing of 100 nm, but this would place the optical mode too close to the highly doped layer. Therefore, the cap spacing was simulated using BPM and chosen to be 700 nm [43].

The spacer layer separates the active and passive regions and influences the effective index of the active region and therefore determines the resonance in the taper.

Simulations showed that for maximum power transfer, the spacer thickness should be less than 200 nm [43]. The thickest possible value of 200 nm was chosen because the etch of the active ridge must be stopped somewhere wtihin the spacer region to avoid etching into the passive waveguide. Etch rates can vary significantly between InP and quaternary materials, so this large window for stopping the etch allows for discrepancies in the etch rate.

A number of sacrificial etch stop layers are placed throughout the device to ease fabrication. They are sufficiently thin so that they do not play an important role in the effective index or the optical power transfer. By choosing etch chemistries that selectively etch phosphorus- or arsenic-rich semiconductors, the etch can be halted at the exact depth of the etch stop layer.

Mode profiles for the final epitaxial structures are shown in Figure 3-7. Good confinement can be seen in both structures. In the passive region, the mode is centered upon the thicker quaternary layer in the middle of the structure. The mode in the active region is centered upon the 1550 nm quaternary core. The mode is also well isolated from the highly doped contact layer and the sidewalls of the active ridge. Isolation of the optical mode from the potentially rough sidewalls helps to minimize scattering and loss in the active waveguide.

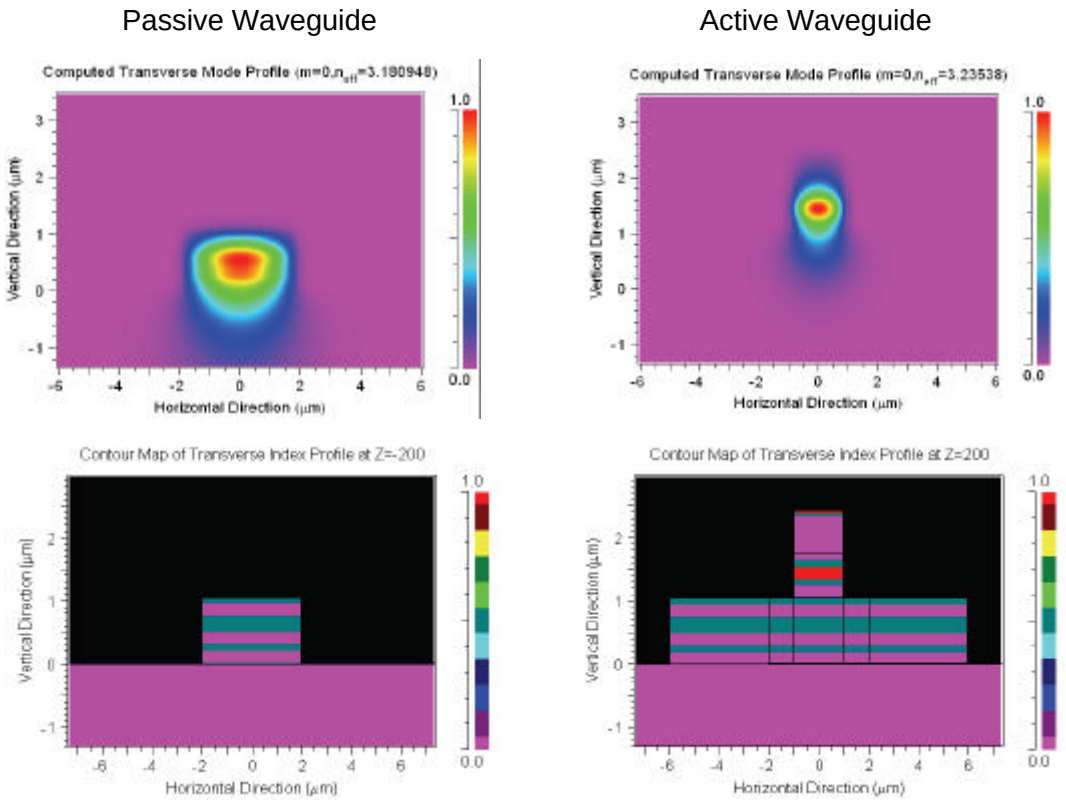


Figure 3-7: The BPM generated fundamental mode profiles for the passive (left) and active (right) waveguides. The mode profile is shown above and the epitaxial structure is show below [43].

3.5.2 Taper Design

Perhaps the most important feature modeled with BPM was the adiabatic tapers. The taper design is critical to the integration scheme, as the tapers provide the mechanism by which power is transferred between the active devices and the passive interconnects. The linear taper is the most basic taper and the easiest to fabricate. Ideally, the best power transfer is achieved by using a nonlinear taper, such as an exponential taper, where the taper angle decreases as the mode size increases [43]. However, optical power transfer simulations revealed that there is very little difference between the exponential and linear tapers for both short (<125 μm) and long (>175 μm) taper lengths. In the intermediate region, exponential tapers do hold a slight advantage. The simplified mask design and subsequent processing for a linear taper motivated the

choice of a linear taper length of 175 μm. Optical power transfer at that length is modeled to be nearly 96%. Longer lengths would yield even greater power transfer, but the advantage is slight and not significant enough to warrant the additional consumption of valuable on-chip real estate. The overall dimensions of the device as viewed from the top-down are shown in Figure 3-8.

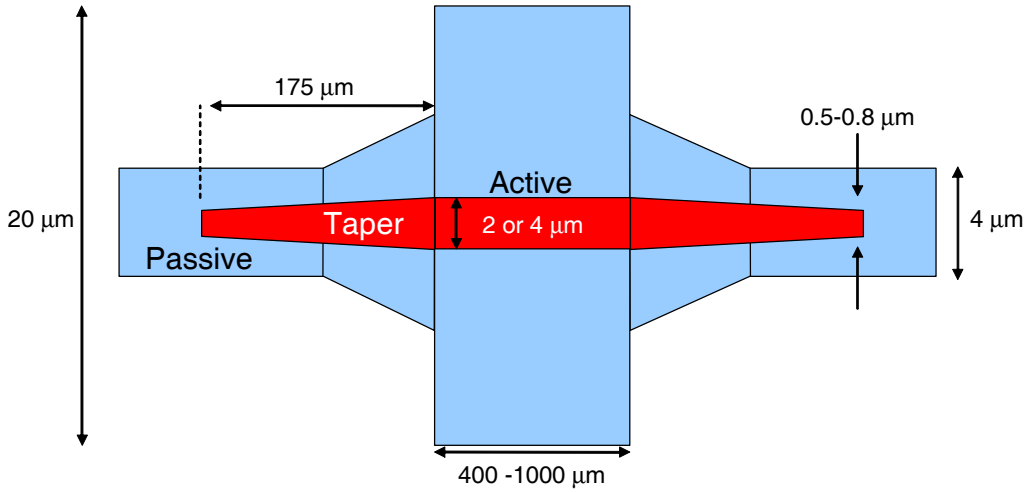
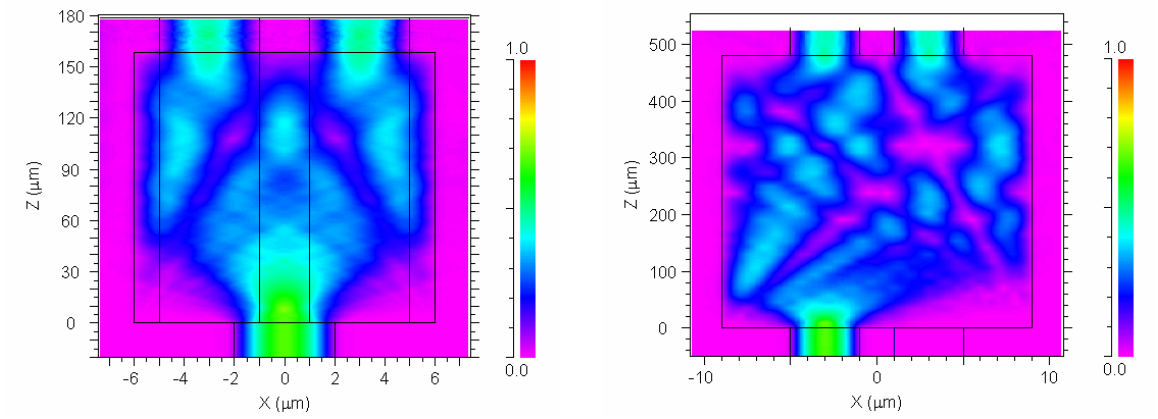


Figure 3-8: Top-down view of ATG-SOA showing tapers and relevant dimensions (drawing not to scale).

3.5.3 Multimode Interferometers (MMIs)

A multimode interferometer (MMI) is a device that is used for splitting and combining waveguides. The MMI has an NxM configuration, where N and M are the number of inputs and outputs, respectively. In the simple case of a 1x2 MMI, an optical signal in a single waveguide is split into two signals in two waveguides. Unlike the single-mode behavior of the incident ridge waveguide, an MMI is much wider and therefore can support a number of modes. These three or more modes interact with each other to create an interference pattern within the cavity. At certain lengths within the cavity, the incident optical signal will image to one, two, or more nodes. If the output waveguides are placed at these node locations, extremely efficient splitting, combining, and coupling can occur. More complex configurations such as 2x2 and even higher values of N and M are possible with proper design of the MMI cavity [53-55].

The MMIs for the optical logic unit cell consist of 1x2 and 2x2 geometries and are integrated at the passive waveguide level. Their height corresponds to the 1.05 μm height of the passive ridge waveguide. In order to minimize evanescent coupling, crosstalk, and loss, the 4 μm wide input and output waveguides are separated by a 2 μm trench at the MMI input and output. Using guided-mode propagation analysis and BPM simulations at 1550 nm, the optimized dimensions for the 1x2 MMI were determined to be 159 μm long and 12 μm wide. The optimum 2x2 MMI dimensions were determined to be 480 μm long and 18 μm wide. Simulations of the two MMIs show balanced 3 dB power splitting-ratios (Figure 3-9).



a) 1x2 MMI

b) 2x2 MMI

Figure 3-9: BPM simulations of a) 1x2 and b) 2x2 multimode interferometers (MMIs) show balanced splitting ratios and low loss at the output waveguides [43].

3.6 Mach-Zehnder Logical Unit Cell

3.6.1 Carrier Dynamics in SOAs

The carrier dynamics of the SOA play an important role in the SOA functionality in an optical logic cell. The gain, refractive index, and phase shifting behavior of the SOA are the result of complex interactions between the injected electrical carriers and the optical signals. When an optical signal encounters a semiconductor material with a

bandgap energy at or below the energy of the photon, the semiconductor material will absorb the photon by exciting an electron from the valence band to an energy state in the conduction band. In the case of a laser or amplifier, the injected electrical current will populate energy states in the conduction band. The incident photon can stimulate one of these excited electrons to recombine with a hole in the valence band and to emit a photon identical to the incident photon. This stimulated emission process is still in competition with the absorption process, in addition to spontaneous emission by the excited electrons. When the absorption and emission rates are equal, the semiconductor is said to be transparent. When the emission rate exceeds the absorption rate, the semiconductor is in a state of net optical gain and will amplify the overall intensity of the incident optical signal. However, there are only a limited number of states in the conduction band that correspond to the incident photon energy. If the number of photons exceeds the number of available states, the semiconductor can be saturated. Saturation can occur in both absorption and gain [56]. In the case of gain, the conduction band is depleted of electrons in states equal to the incident photon energy and it will take time for the injected carriers to replenish these depleted energy states. This phenomenon is known as spectral hole burning. The time that is required for an injected current to replenish the SOA is on the order of 1 ns, significantly longer than the rate at which optical signals are traveling in the SOA-MZI, typically on the order of 100 ps or less. Therefore, intraband carrier dynamics become important in SOA performance. For example, the energy distribution of electrons within the conduction band will redistribute themselves to fill the empty states. This phenomenon occurs on the order of 100 fs. Additionally, electrons in higher energy states will transition to the lower energy states to lower the overall energy of the carrier distribution. This last process is known as temperature relaxation and occurs within picoseconds [57].

In a SOA, the refractive index of the material is dependent upon the carrier density. If an optical signal of sufficient intensity enters the SOA, it will alter the carrier dynamics and change the refractive index. A low-intensity signal can pass through a SOA without significantly changing the refractive index.

For a photonic integrated circuit, the ability of a high-intensity optical signal to alter the refractive index is the key to changing the phase of the SOA. The optical path

length is a product of the refractive index and the geometric path length. Therefore, depletion of carriers within a SOA by an incident pulse can change the refractive index and hence the optical path length. If two optical paths are placed in parallel, a Mach-Zehnder interferometer (MZI) can be constructed. Varying the optical path length of one arm of the interferometer with respect to the other is the basis of the SOA-MZI.

3.6.2 SOA-MZI Principles of Operation

The optical logical unit cell is based upon a Mach-Zehnder interferometer configuration and is shown in Figure 3-10. The MZI configuration is flexible and can be cascaded into more complex logic and packet switching configurations [58, 59]. The fundamental unit cell consists of three inputs and two outputs allowing for a variety of Boolean operations such as INV, AND, or XOR to be implemented. The MMIs at each waveguide intersection are currently passive, but tunable MMI designs are possible which allow more precise control over the power splitting ratio.

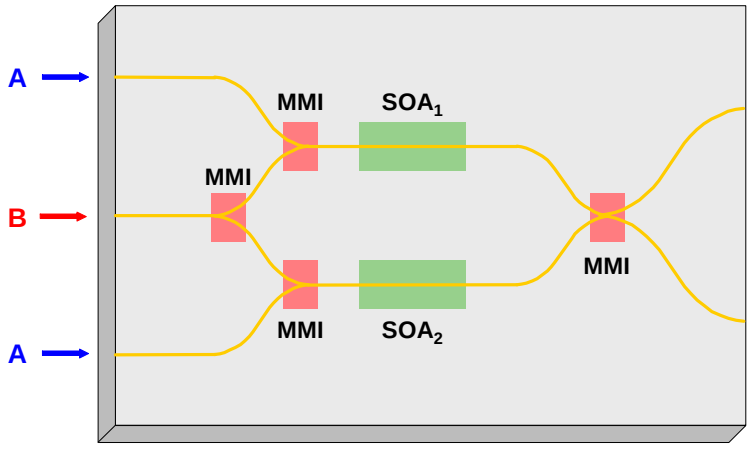


Figure 3-10: Schematic of optical logic unit cell.

The Mach-Zehnder interferometer is at the heart of the optical logic unit cell. There is at least one amplifier on each arm for phase-shifting, but several more can be added for additional amplification. More advanced constructions could include several additional SOAs solely for amplification (Figure 3-11) similar to the wavelength conversion devices marketed by Alcatel [58]. Nominally, the two SOAs within the MZI

balance each other and constructively interfere with each other at the outputs. For device operation, the introduction of a control optical pulse and the variation of the individual SOA bias currents, and therefore the resultant gain and phase shifting, allows a variety of Boolean operations to be performed.

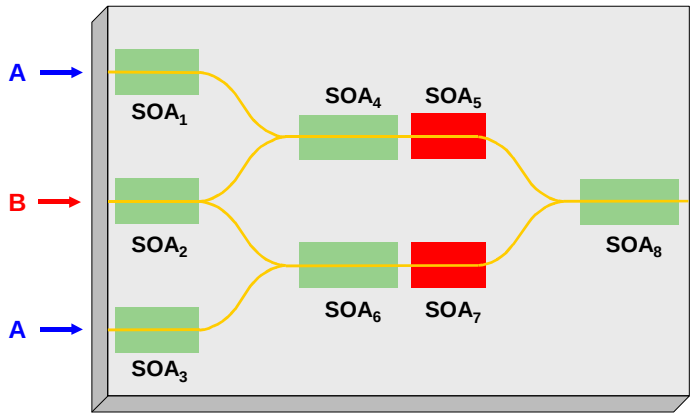


Figure 3-11: More advanced designs would include additional SOAs for amplification (SOAs 1, 2, 3, 4, 6, and 8) of the signals in addition to the SOAs for phase-shifting (SOAs 5 and 7).

Figure 3-12 shows a more detailed depiction of how the SOA-MZI performs logical operations. Under nominal conditions, the SOAs are balanced; the optical path length along each of the arms are equal and pulse B will constructively interfere at the output of the MZI. The signal is transmitted. If a high-intensity optical pulse (A) is fed into the upper arm of the MZI, it will cause a phase shift in SOA_1. Now, if a lower intensity signal (B) enters the MZI and SOA_1 is out of phase with SOA_2, destructive interference will occur at the output for signal B and no signal will be observed. Low intensity signals will not affect the carrier dynamics and will not induce a phase change. Next, a time-delayed high-intensity pulse – identical to A – is sent into SOA_2 and the two SOAs are back in relative phase with each other. The time-delay is currently done off-chip, but future designs could incorporate a buffer or other technique for signal delay. The time delay is on the order of 5 ps, at least twice the pulse width and shorter than the data rate.

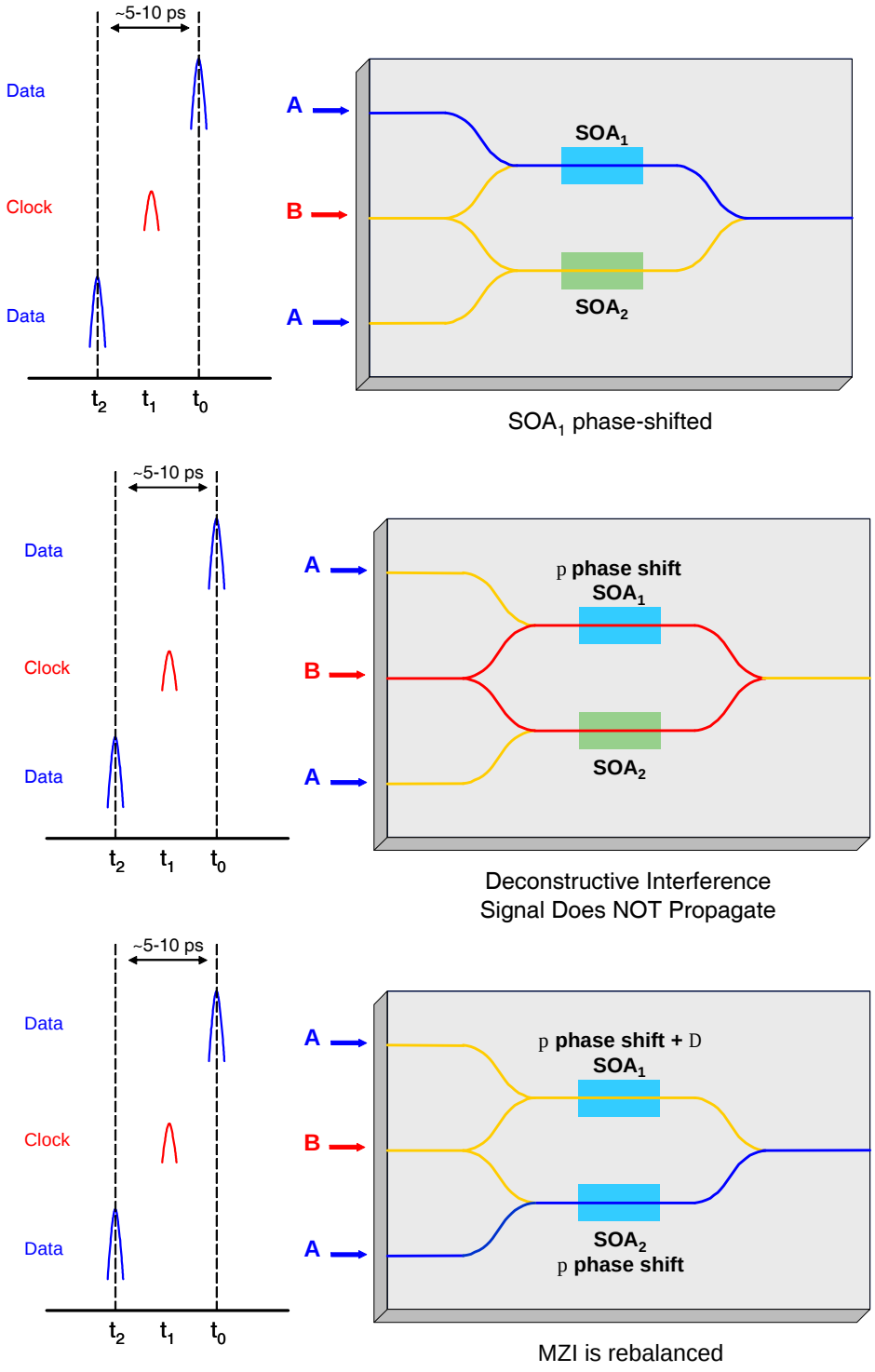


Figure 3-12: The optical logic unit cell operates by unbalancing the SOA in one arm of the Mach-Zehnder interferometer.

Consider the implications when this simple case of individual pulses is expanded to a data stream of ones and zeros. A high-intensity data stream is sent into one arm of the MZI followed by an exact copy in the other arm, with some time delay between them. The time delay, on the order of picoseconds, is in general different than the data rate, which is the time between successive ones and zeros and can range from picoseconds to nanoseconds. Another low-intensity data stream is sent into the middle waveguide and divides evenly between both arms of the MZI. For all instances here, a return-to-zero (RZ) scheme is used for the data stream. In the case where signal B is a clock signal, that is, a series of regularly spaced pulses (ones), the logic gate will perform an inversion (INV) operation (Figure 3-13) with the inverted signal imprinted on the wavelength of signal B. The addition of color to the signal is an extra piece of information and can be used to discriminate between two data signals. In a photonic integrated circuit, these different colors are actually finely spaced wavelengths in the optical fiber C-band (λ=1530-1562 nm).

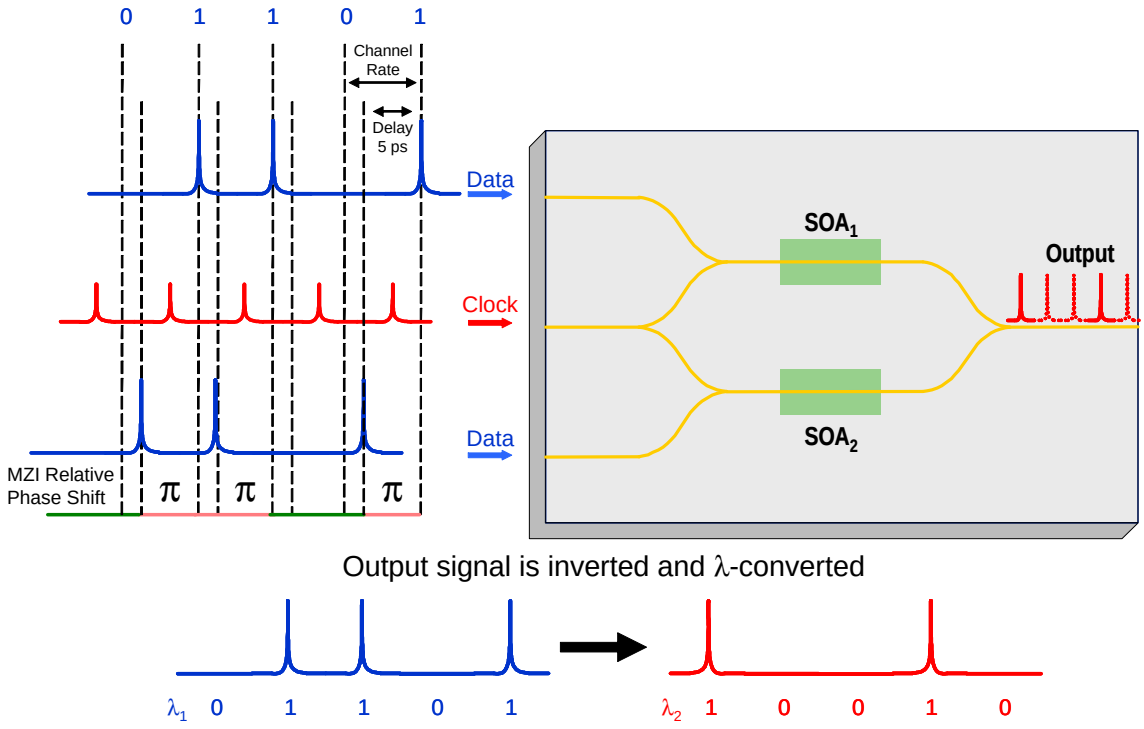


Figure 3-13: The optical logic unit cell will perform a basic inversion (INV) and wavelength conversion if signal B is a clock signal (series of ones).

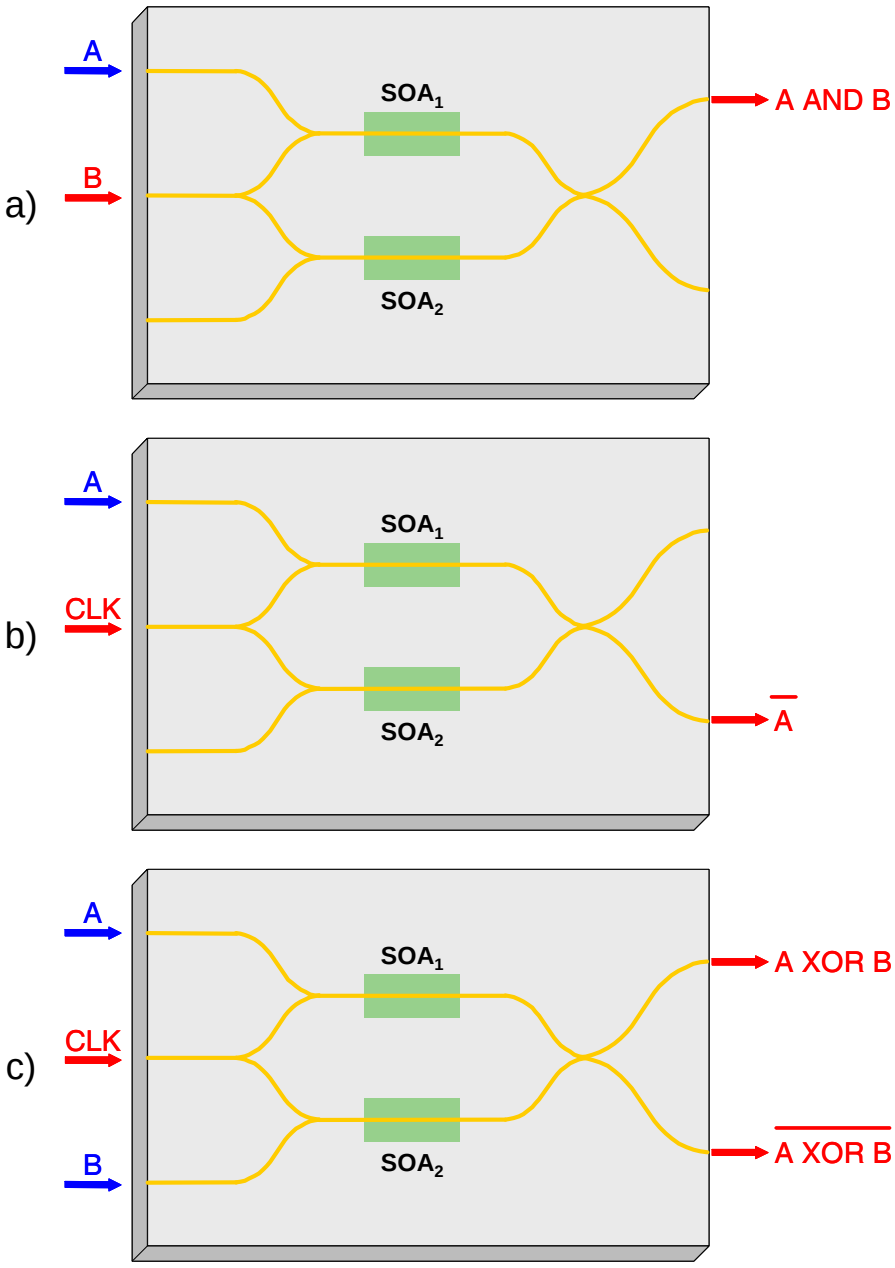


Figure 3-14: Coupling multiple data streams into the optical logic unit cell allows a variety of Boolean operations to be performed, such as AND, XOR, and INV.

An even more complex case would be where the clock signal is replaced with a second data stream (Figure 3-14a) or two different data streams are sent along with the clock signal (Figure 3-14c). In the case shown in Figure 3-14c, two different data streams are sent into the optical logic unit cell allowing a variety of Boolean logical

operations to be performed. These different cases reveal the versatility of the SOA-MZI. With the additional variable of electrical bias to the MZI, the optical logic cell can operate in inverting or non-inverting mode and perform a variety of other useful Boolean operations.

SOA-MZI devices have already been studied in a number of cases for all-optical signal processing applications such as wavelength conversion [60-63]. However, the combination of the SOA-MZI configuration with the advantages of the asymmetric twin waveguide technology is a powerful platform for photonic integrated circuits. The ATG design eliminates the need for regrowths in what is already a complex fabrication process for the SOA-MZI.

3.7 Fabrication Techniques

A number of standard optoelectronic fabrication tools are used for the fabrication of photonic integrated circuits. The enabling technology for all integrated circuits, both electronic and photonic, is photolithography, for it allows the patterning of extremely small features on the surface of the wafer. For most photolithographic techniques, the first step in the process is to coat the wafer with photoresist using a spin coater. After baking the resist to evaporate the solvents, the wafer is exposed to ultraviolet (UV) light through a chrome-coated quartz mask. The chrome selectively blocks UV light from illuminating the photoresist and initiating a chemical reaction within the resist. The photo-activated chemical reaction changes the solubility of the photoresist in a particular chemical called a developer, either making the exposed resist soluble (positive resist) or insoluble (negative resist). The developer is used to selectively remove the photoresist, leaving behind a pattern that is a replica of the pattern on the mask or that is an inverse of the pattern on the mask. The pattern is then used for subsequent fabrication processes. While the semiconductor industry has largely moved on to more complex photolithographic equipment such as steppers, the contact aligner remains the workhorse of academic research. The contact aligner places the quartz mask directly in contact with the photoresist-coated wafer, limiting the resolution of this technique to dimensions on the order of 1 μm, perhaps a bit smaller. The contact aligner used for the optical logic structures was an Electronic Visions 620.

III-V semiconductors are incapable of growing thick native oxide layers similar to SiO_2 on silicon substrates. Therefore, insulating materials must be deposited on III-V substrates using a variety of different physical or chemical vapor deposition techniques. In this work, SiO_2 films were deposited using plasma-enhanced chemical vapor deposition (PECVD). In PECVD, the wafer is placed in a vacuum chamber on a heated platform and gases are introduced into the chamber. These gases include inert atoms, such as argon, and chemically-reactive gases such as SiH_4, N_2O, O_2, NH_3, CH_4, CF_4, and PH_3 . A plasma is generated within the chamber using an electric field oscillating at radio-frequencies (13.56 MHz). Within the plasma the reactive gases undergo a series of chemical decompositions and the hot substrate surface provides energy for chemical reactions that form a film on the surface. By closely controlling the gas chemistry, a wide variety of films can be deposited such as oxides, nitrides, oxy-nitrides, and amorphous silicon. Oxide films were deposited for fabrication of the optical logic unit cell using an Multiplex PECVD by Surface Technology Systems. The oxide films were used as hard masks, which are the more durable counterparts to “soft” photoresist masks, in order to etch patterns within the semiconductor material to form the ridges that comprise the active and passive waveguides.

In order to etch ridge waveguides into semiconductor materials, an etching technique is needed which can produce smooth, vertical sidewalls. Wet chemical etches typically etch isotropically or preferentially etch particular crystal planes, and generally do not exhibit good uniformity. Therefore, wet etches are generally unreliable for etching deep ridges and trenches. Reactive ion etching (RIE) is a plasma technique that can be thought of as essentially the opposite of PECVD. Similarly, inert and chemically reactive gases are introduced into a vacuum chamber except that, instead of depositing a film, the gases remove material from the substrate by chemically reacting with the semiconductor material to form a volatile species that is transported away by the vacuum system. Additionally, the physical bombardment of the surface caused by the ionized plasma can kinetically remove semiconductor material from the surface. Again, by carefully controlling the gas chemistry and the plasma characteristics, deep, anisotropic etches into the semiconductor material are possible. In this thesis, two different reactive ion etch techniques were used to etch InP-based materials, RIE using methane/hydrogen (CH_4/H_2) and chlorine-based inductively-coupled plasma reactive ion

etching (ICP-RIE). A comparison of these two techniques appears later in this chapter. Additionally, fluorine-based RIE etches were used to etch insulating materials.

Most active devices require metal contacts to introduce electrical current into the device. In this work, the metal was deposited, using either electron beam evaporation or sputtering, on top of a layer of developed photoresist. Then a solvent is used to remove the photoresist and with it any meta that was deposited on the photoresistl. The metal that was deposited on regions without photoresist remains.

These techniques comprise the basic fabrication process by which almost any photonic device can be produced. The next sections detail the sequence used to produce the passive waveguides, active devices such as SOAs, and the optical logic devices. Many of these methods are quite complex and continued refinement of these fabrication processes led to dramatic improvements in the device quality.

3.8 First-Generation Devices

Two generations of optical logic devices were fabricated. The first-generation was completed; however, there were a number of problems with the fabrication process which led to poor device performance. The first-generation devices will be discussed briefly and their problems outlined in order to motivate the discussion of the fabrication sequence used for the second generation of devices.

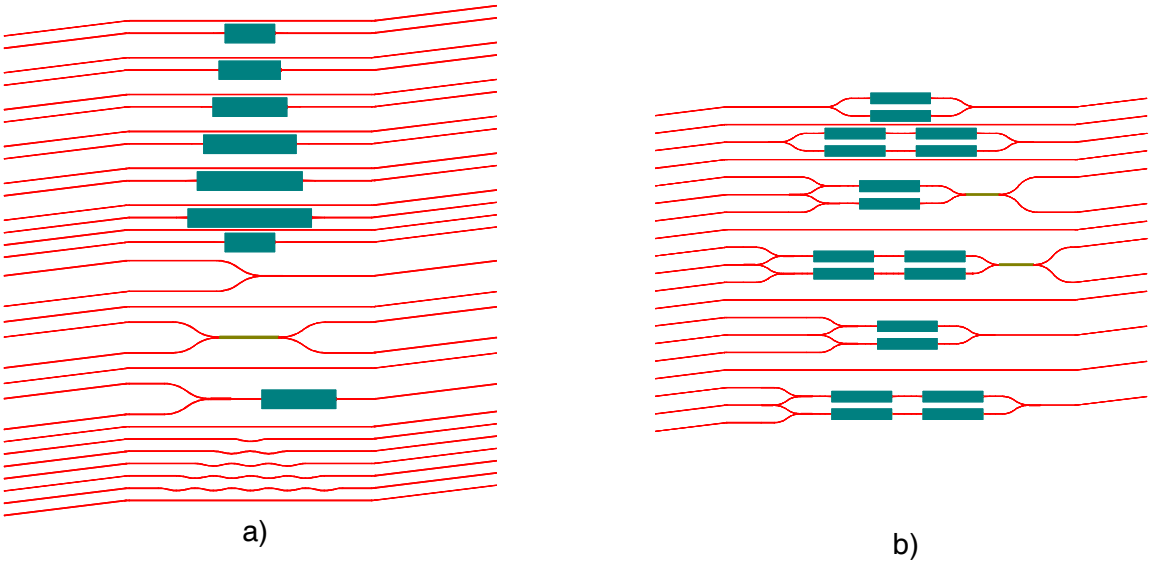
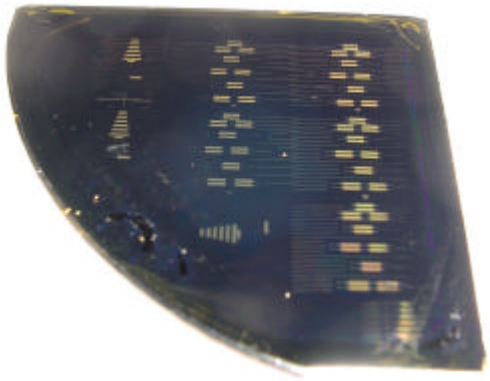


Figure 3-15: The first device generation mask set was comprised of two separate die. The first (a) included passive devices and SOAs and the second (b) contained more complex optical logic unit cell structures and wavelength-converters.

The first element of any semiconductor fabrication process is the mask design. For the first-generation fabrication, two separate die were designed and incorporated on the same mask. A quarter of a 2" InP wafer was fabricated at one time, and nine total die were included on each mask, four die with passive devices and SOAs and five die with optical logic devices. The two die are shown in Figure 3-15. Many bare InP wafers were processed in parallel to monitor the fabrication sequence.

The first generation devices were primarily used to test the fabrication process, as it often takes several processing iterations to perfect the fabrication sequence. Indeed, a number of problems in the first generation device fabrication sequence were revealed, including significant problems with sidewall roughness on the waveguide, planarization and passivation of the device, and mounting the device for optical testing. Finished devices are shown in Figure 3-16. While some limited waveguide coupling and spontaneous emission was observed, the problems listed above with etching, passivation, and mounting rendered complete testing of the devices impractical.

a)



b)

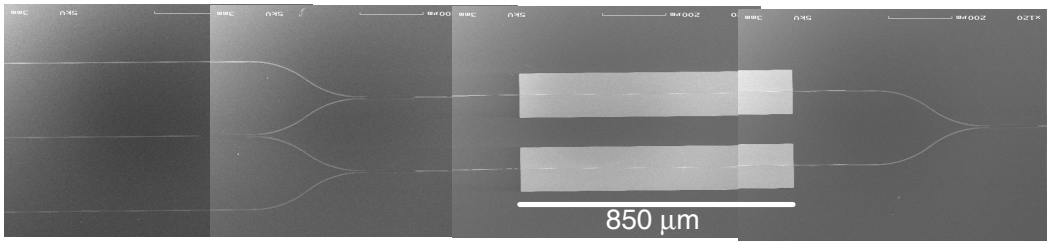


Figure 3-16: a) Photograph of fabricated first generation device wafer. b) Plan view scanning electron microscope (SEM) micrograph of a fabricated wavelength converter.

3.9 Second-Generation Devices

3.9.1 Fabrication Procedure

The fabrication of the optical logic unit cell is complex because it is not a planar device. The vertical integration scheme greatly complicates the fabrication process because the device must be processed on two levels, one layer containing the active devices and the other layer containing the passive structures, in addition to its two-dimensional planar layout. Furthermore, these two layers must be precisely aligned with each other in order to maintain high coupling and power transfer between the two levels. Explicit details of the entire fabrication sequence are included in Appendix 5.2.

The first step in the fabrication sequence is to deposit a Ti/Pt base metal to define and protect the active ridge of the SOA. A widely used image-reversal resist, AZ 5214, is first applied, exposed, and developed. Next, 20 nm of Ti and 20 nm of Pt are

deposited on the resist. An organic solvent, N-methylpyrrolidone (NMP), is heated to ~100°C to help remove the photoresist and liftoff the metal residing on top of the resist. The 20 nm of Ti and 20 nm of Pt are half of the eventual ohmic contact to the active region. By depositing the Ti/Pt metal layer first, the interface between the metal and the InGaAs contact material is protected from all of the aggressive processing techniques that follow. Specifically, high-energy plasmas can significantly damage a semiconductor surface through ion bombardment. Immediately depositing the metal helps to ensure that the ohmic contact will be of the lowest possible resistance. The metal only defines the active ridge, not the tapers, because current injection within the tapers could alter the refractive index and interfere with the passive-to-active coupling mechanism.

Next, a 450 nm thick film of SiO_2 is deposited using PECVD. The PECVD deposits material conformally, that is, PECVD deposits films on the top and sides of any topography on the surface. Photoresist is patterned to shape the tapers and to cover the metal on the active ridge. The metal contacts and oxide must exactly align, so this photolithographic step is critical. A fluorine-based RIE step is used to etch the oxide, transferring the photoresist pattern to the oxide. Together, the metal and oxide define the upper, active portion of the ATG structure (Figure 3-17a). The metal/oxide hard mask is used to transfer the pattern into the semiconductor using a chlorine-based ICP-RIE step, forming a ridge that is approximately 1.3 μm deep (Figure 3-17b).

After the first semiconductor etch, the now-defined ridge must be protected from subsequent processing damage, particularly the RIE etch of the passive ridge. Another 450 nm PECVD oxide layer is deposited over the whole wafer, which completely covers all exposed surfaces of the active ridge. A photolithographic step defines the passive waveguides, including the MMIs, and this pattern is again transferred to the oxide using a fluorine-based RIE process (Figure 3-17c). Again, this alignment is critical as the relative position of the active and passive waveguides plays an important role in their coupling efficiency. The resulting oxide pattern is transferred into the semiconductor using ICP-RIE. The active ridge should remain protected by the oxide mask throughout the etch. Now that the active and passive waveguides have been defined, a hydrofluoric acid (HF) etch is used to remove the oxide hard masks (Figure 3-17d). HF is known to etch titanium, so it is possible to unintentionally remove the Ti/Pt base metal. However,

the most severe processing steps are prior to this step, so the remove of the metal should not significantly affect the device performance.

In order to pattern a metal contact pad on the surface, a stable and flat surface is required. Furthermore, the metal contact must only contact the p-type material and not make contact with the n-type material below the 1550 nm quaternary material or it will short circuit the p-n junction. Therefore, a planarization material is needed which only reveals the very top surface of the p-type semiconductor material. There are a number of different planarization materials, including polyimide (PI), benzocyclobutene (BCB), and hydrogen silsesquioxane (HSQ). These are all spin-on insulators, liquids which are spun on to the substrate and then subjected to a heat treatment that cures and solidifies the material. Both PI and BCB were used in this study and will be compared later. HSQ required additional processing steps and prior experience showed some undesirable interactions with the III-V material, so HSQ was not used in this process. After planarization, a plasma etch is used to uniformly etch back the planarization material. By etching in short steps with frequent monitoring, the etch can be terminated just as the very top surface of the ridge is exposed (Figure 3-17e). Next, the Ti/Pt/Au (30 nm/20 nm/200 nm) p-type metal contact is evaporated.

Backside processing includes lapping the wafer using at 5 μm Al_2O_3 powder to take the wafer from a starting thickness of roughly 350 μm to approximately 150-175 μm. Lapping greatly improves the quality of the facets when later cleaved. A 1% bromine in methanol solution is used to chemically polish the wafer backside and remove any damage from the lapping procedure. A Ni/Au/Ge/Au (300/600/300/2000 Å) backside n-type contact is sputtered on and then the whole assembly is rapid-thermal annealed at 450°C for 30 sec to alloy the contacts. The wafer is then cleaved and mounted for device testing.

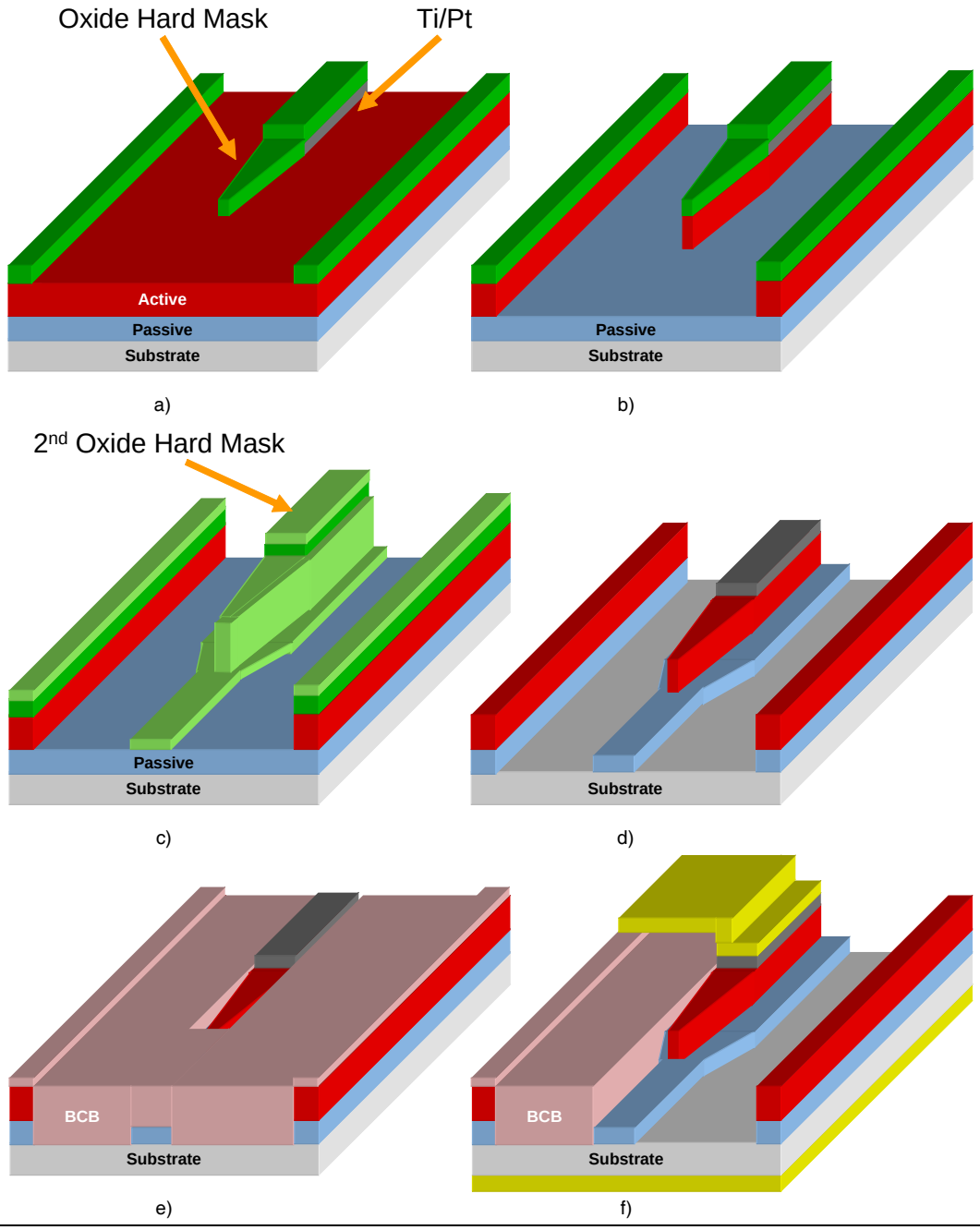
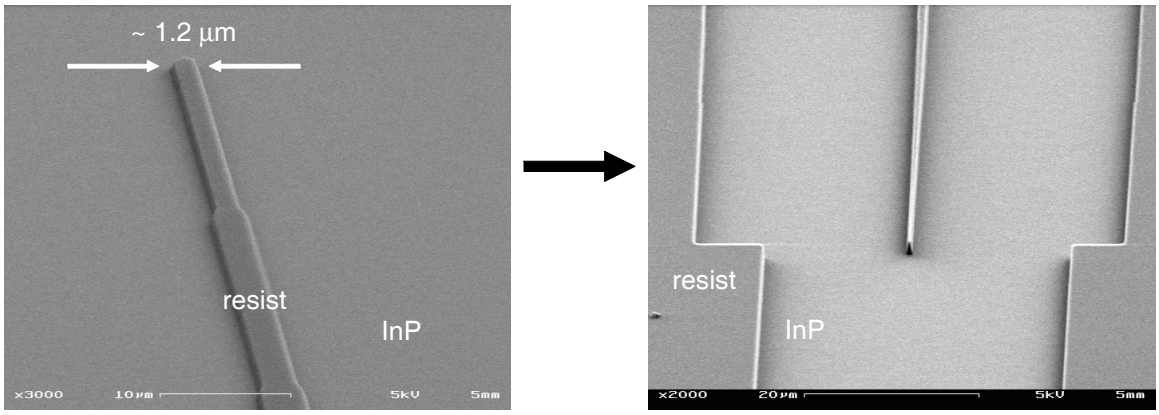


Figure 3-17: a) Ti/Pt base metal is patterned to protect the ohmic contact surface. PECVD oxide is patterned to form a hard mask that defines the tapers and the active ridge. b) RIE is used to transfer the oxide hard mask pattern into the semiconductor. c) The second oxide hard mask is deposited and patterned to define the passive waveguide. d) The passive waveguide is etched into the semiconductor and the oxide hard masks are removed using HF. e) Benzocyclobutene is used to planarize the device and then etched back to reveal the active ridge. f) The topside contact (Ti/Pt/Au) is deposited, then the backside is lapped and polished prior to the deposition of a metal contact (Ni/Au/Ge/Au).

3.9.2 Mask Design

The mask design is a vital part of any fabrication process and the knowledge gained from the first-generation devices motivated a number of changes for the second-generation devices. A significant design change was the addition of trenches surrounding the waveguide device. All of the passive waveguide interconnects, including the SOA regions, were placed within a 36 μm wide trench, a distance picked to be well outside the lateral evanescent coupling range of the waveguides. With the first mask generation, the area between ridge waveguides, spanning hundreds of microns, was etched during the semiconductor RIE processing step. The trench design significantly reduces the etch load of the RIE because rather than etching the entire wafer surface save the 2-4 μm ridges, only a narrow area around the devices is etched. This simple design change reduces the volume of material etched by 91%. By reducing the volume of material etched, the etch anisotropy improves, the etch rate slightly increases, and less redeposition and micromasking occurs.

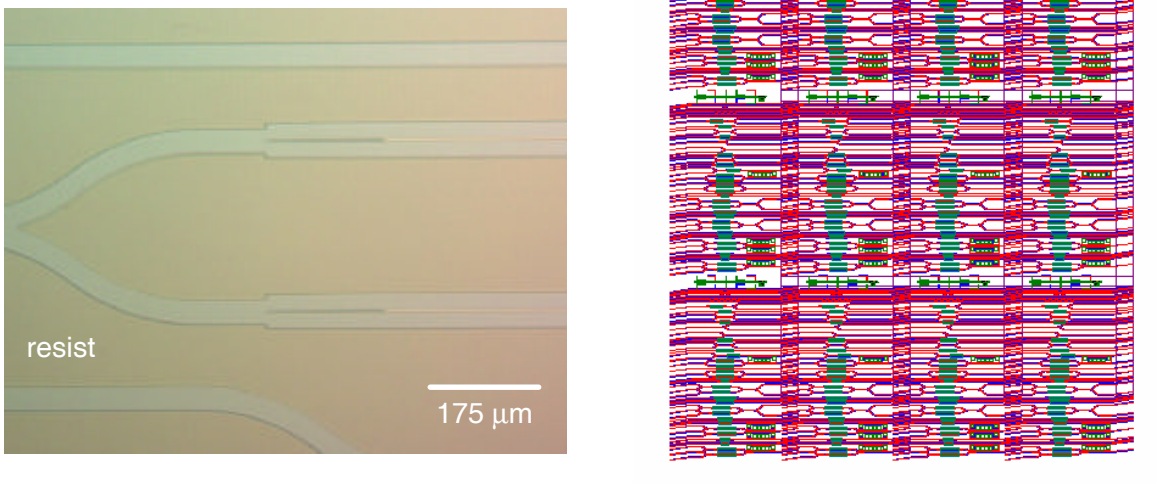
Additionally, the trench design allows for a tone change in the mask. The first generation passive waveguides were defined using a positive mask and a positive resist, that is, the chrome mask features were identical to the ridge waveguides. The small features, particularly the tapers, had to be directly written to the mask at 1x and suffered from pixelation problems due to the resolution limits of the mask-writing laser. The result was a taper that was not perfectly smooth, but was a series of steps. By writing the opposite feature in the second generation, two smooth rectangles that intersect at a point, the taper shape became a smooth continuous function. (Figure 3-18). The mask was produced as a negative mask and AZ-5214 image-reversal resist was used, two negatives forming a positive image. The trench is shown in Figure 3-19a, following the etch of the active ridge.



a) b)

Figure 3-18: SEM micrographs of a) first generation design showing jagged, pixilated taper and b) second generation design with a smooth, continuously varying linear taper.

Further improvements in the mask design were obtained from combining the two dies of the first generation into an integrated die with all of the device structures. The large optical logic structures require that the centers of the passive waveguide inputs be spaced 250 μm apart in order to be compatible with ribbon fiber inputs and outputs. However, the passive devices could be interleaved within the larger optical logic structures because they do not need to reside on the same 250-μm-pitch coordinate system. In the second-generation die, all of the devices are placed within an area that only accommodated half the number of devices of the first generation. While this more efficient use of on-chip real estate is attractive, the real advantage of having a single die is that that it can be written as a step-and-repeat mask. With a step-and-repeat mask, a single die is written at a 4x magnification allowing for much smoother features to be written with the direct-write laser. The 4x image is then projected down to 1x on the final mask, translated in x-y space, and projected again. The result is a mask with a series of die as show in Figure 3-19b. Details of the die are included in Appendix 5.4.

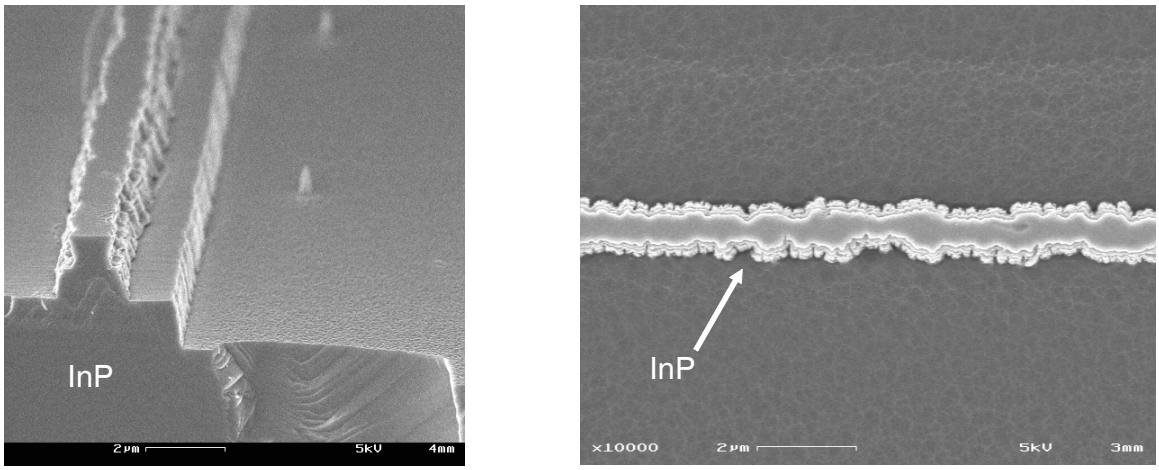


a) b)

Figure 3-19: a) The trench design greatly reduced the volume of InP material etched in the RIE and helped to improve etch quality. b) The use of a step-and-repeat mask allowed for more efficient use of space and smoother feature writing.

3.9.3 Sidewall Roughness – Photoresist

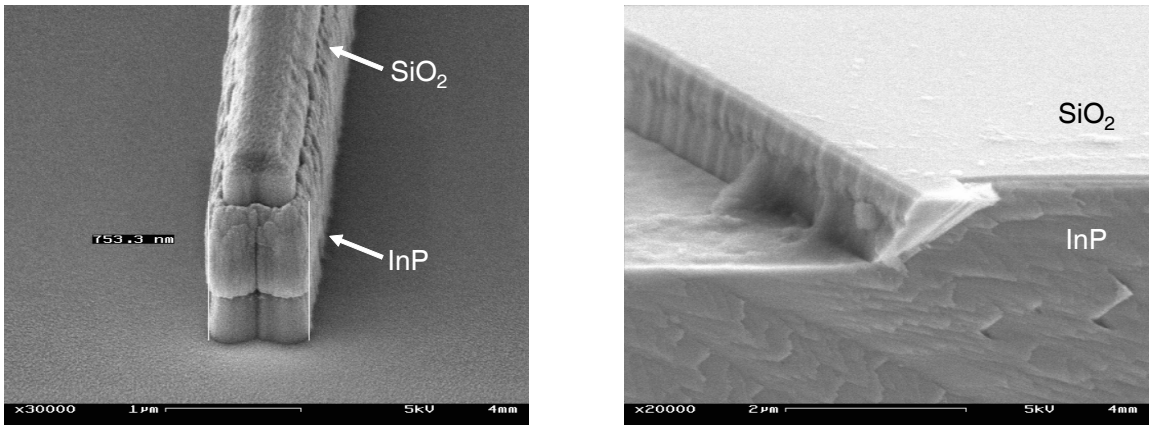
Scanning electron microscopy (SEM) micrographs of the first-generation devices revealed significant problems with sidewall roughness, in some cases so severe that the ridge could hardly be considered a waveguide (Figure 3-20). Obviously, coupling and propagating of light in these devices is impractical owing to the poorly defined mode and significant scattering losses.



a) b)

Figure 3-20: Sidewall roughness in some first generation devices was severe. a) A cross-sectional SEM micrograph and b) a plan view SEM micrograph show significant roughness along the ridge waveguide

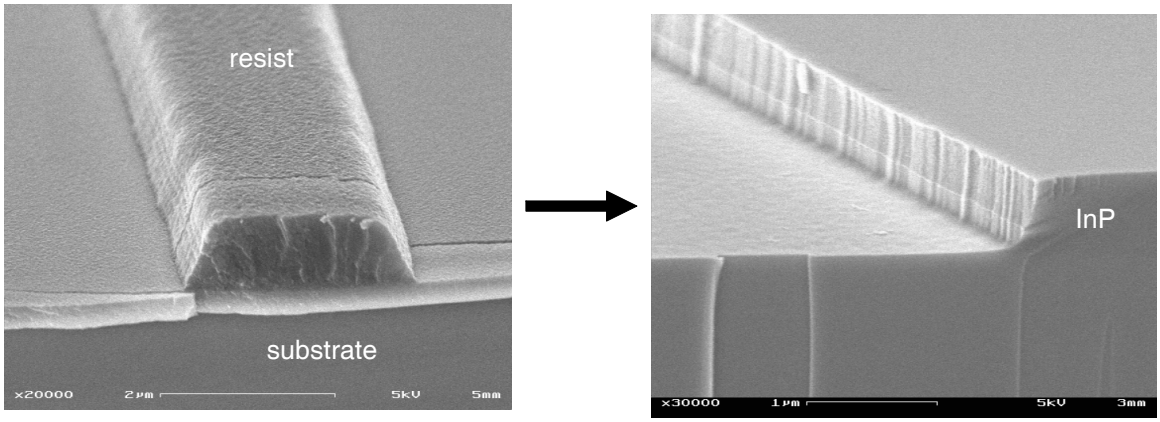
Even second-generation devices, with an improved mask design and smoother features, showed significant problems with sidewall roughness (Figure 3-21). With the new mask design, the resulting roughness is most likely not a result of the morphology of the mask pattern. Prior work has indicated that the cause of the sidewall roughness is often traced back several steps back in the fabrication process to the quality of the sidewall in the developed photoresist [64, 65]. Even under optimized conditions, certain resists may inherently exhibit more sidewall roughness than others.



a) b)

Figure 3-21: Sidewall roughness continued to be observed in SEM micrographs of second-generation devices, despite improvements in the mask design.

The resist used for the photolithography exposures and subsequent etches was OCG 825-20, a positive tone resist with a thickness of 600 to 900 nm. The suspicion that the OCG resist was playing a significant role in the sidewall roughness was investigated more thoroughly. Using scanning electron microscopy, all aspects of the photolithographic process were characterized.



a) b)

Figure 3-22: SEM micrographs show that a) roughness in the photoresist plays a significant role in b) roughness in the etched semiconductor.

Initial observations showed that AZ-5214 resist sidewalls were inherently smoother than the OCG-825 resist, for reasons that are not well understood. The AZ-5214 was chosen as a starting resist to minimize sidewall roughness. However, AZ-5214 resist is primarily used as an image-reversal resist, creating a negative image of the mask for applications such as metal liftoff. The versatility of the AZ-5214 resist is that it can actually be used as either an image-reversal resist or a positive resist. Experiments were conducted to optimize the process for use as both a positive and an image-reversal resist. The conditions, results, and conclusions of these experiments are catalogued completely in Appendix 5.5. Using the same resist for both positive and negative tone applications simplifies the overall fabrication process.

The first step in the photoresist optimization process was the selection of the exposure time. All resist studies were conducted using 1.4 μm thick layers of AZ-5214, corresponding to a spin speed of 4000 rpm for 30 sec. As the aligner is run exclusively in a constant intensity mode, the exposure time is directly proportional to the energy dose. In an ideal binary resist model, the dose is the amount of energy required to convert the photo-polymer for a certain thickness of resist. Different exposure times were chosen to determine the proper dose for AZ-5214 as a positive resist. The optimum exposure time for positive resist was determined to be 10 sec, corresponding to an energy dose of approximately 100 mJ/cm^2. For image-reversal, 2.0 seconds was the proper time for the initial exposure, followed by a bake and a 60 second flood exposure to complete the reversal reaction.

After exposure, the development time must be determined. Development times can be extremely sensitive, particularly with small features such as the taper tips. Optical simulation results showed that tip widths greater than 800 nm significantly reduce the coupling efficiency of the taper [43]. The taper is the smallest feature on the mask, so it is the first to overdevelop. Overdevelopment manifests itself as a recession of the taper tip, the tip getting wider as it recedes along the length of the taper. The overdevelopment of the taper may occur even if all of the other features on the mask appear to develop properly. The developer used for all studies was AZ 422, a metal-ion-free solution of ~2% tetramethylammonium hydroxide (TMAH) and water. The development time was determined to be ~75-80 seconds when AZ-5214 is used as a positive resist and ~50-60 seconds when AZ-5214 is used in an image-reversal process.

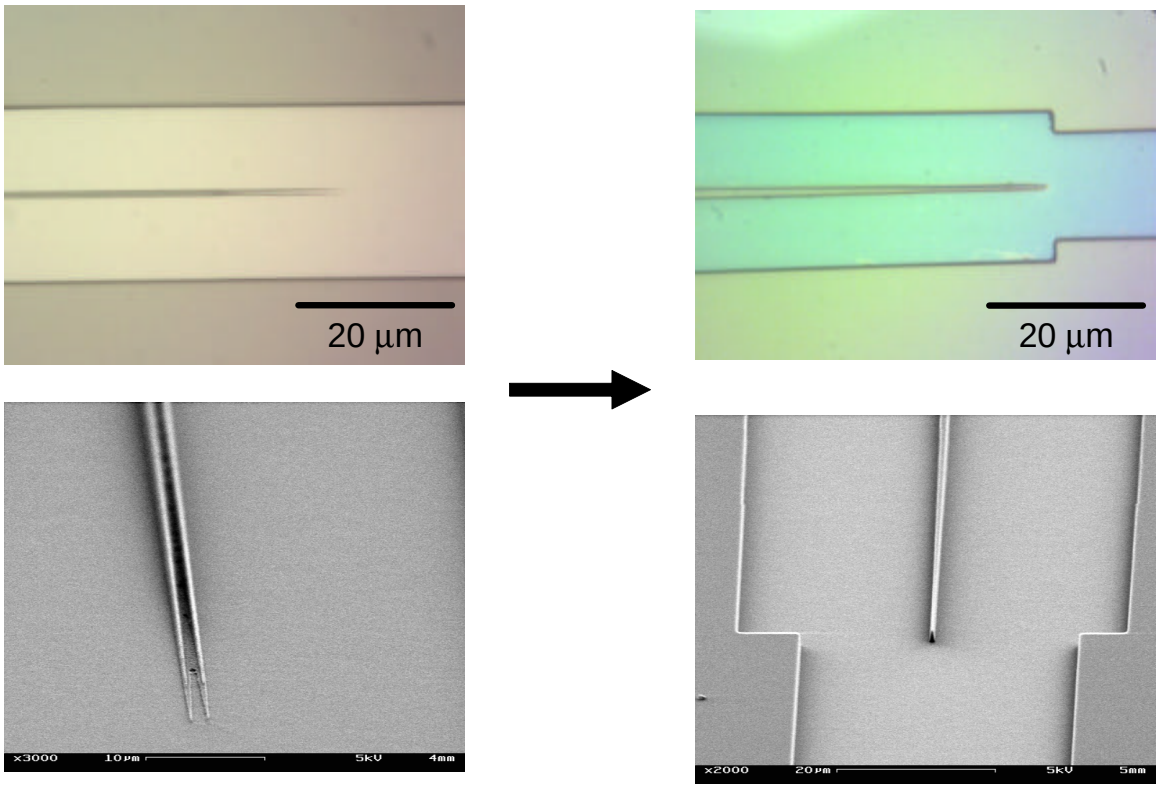
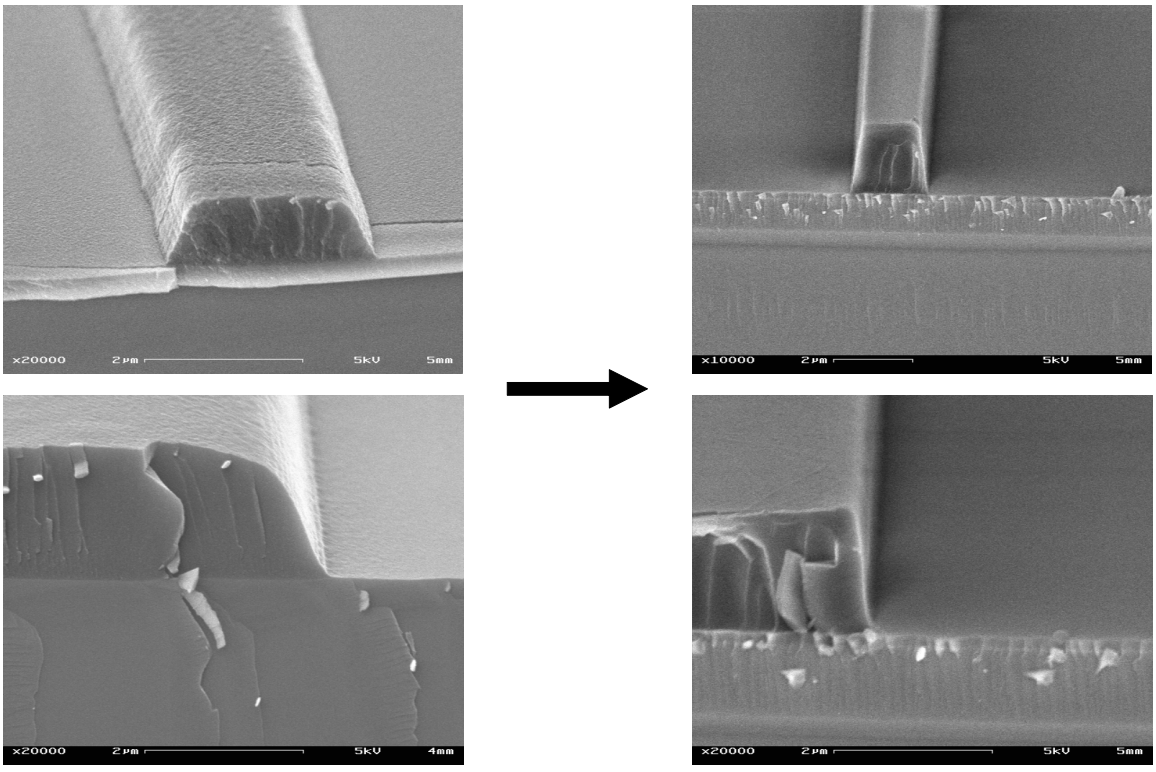


Figure 3-23: Nomarski micrographs and SEM micrographs of the development process. The a) overdeveloped sample show significant recession of the tip as compared to b) the properly developed image-reversal resist.

In addition to the determination of the exposure and development times, the resist undergoes a number of heat treatments, particularly when AZ-5214 is used as an image-reversal resist. After the first exposure, an image-reversal bake is used to activate the reversal chemical reaction. Initially, the image-reversal bake was done at 95°C for 30 minutes in an oven. However, the heating process in an oven is dominated by convection, in which the resist surface reaches the desired temperature before the center of the resist. As a result, a 'skin' can form on the outside of the resist, trapping any gases that are byproducts of the reversal reaction and solvents that continue to outgas and create a rough morphology. Transferring the process to a hotplate (123°C for 90 sec) immediately improved the sidewall profile. In the hotplate process, the heat is conducted from the wafer bottom to the top of the resist surface. The thermal gradient

is such that it drives solvents up and out of the resist, avoiding the problem of trapped gases within the resist. Not only did the resist appear smoother but also the short hotplate times did not allow the resist to reflow, improving the verticality of the sidewall profile. The non-optimized OCG-825 resist had a sidewall angle of 60° compared to the 85° sidewall profile of the optimized AZ-5214 (Figure 3-24). The improved sidewall angle helps to improve the verticality of the underlying oxide and semiconductor RIE etches.

An additional step that can be taken is a flood exposure of the resist after development. The flood exposure will convert the photo-polymer in any remaining resist and allow it to outgas in a controlled manner, rather than outgassing as a result of heating from subsequent processing steps [66]. As the first step in the pattern transfer, improvement of the resist profile and smoothness is extremely important to achieving waveguides with low sidewall roughness.



a) b)

Figure 3-24: SEM micrographs showing the sidewall profile of resist on a silicon wafer. a) The OCG-825 resist had a less vertical sidewall and greater roughness than b) the AZ-5214 image reversal resist.

3.9.4 Sidewall Roughness – Oxide RIE Etch

The next step in the fabrication process is to transfer the pattern from the resist to the oxide hard mask. This process is performed using fluorine-chemistry in a Plasmatherm Model 790 RIE. In this process, the plasma dissociates fluorine ions from either CHF_3 or CF_4 molecules. These fluorine radicals react with SiO_2 to form SiF_4 and O_2, both volatile species.

Initially, all oxide etches were performed using CHF_3 (15 sccm, 15 mTorr, 100 V). However, scanning electron microscopy revealed that this chemistry was severely damaging the photoresist and then transferring this damage into the oxide in the form of sidewall roughness (Figure 3-25). In order to eliminate or reduce this roughness, extensive experiments were conducted to optimize the RIE of the oxide. Appendix 5.6 includes details of all experiments performed to improve the oxide sidewall roughness.

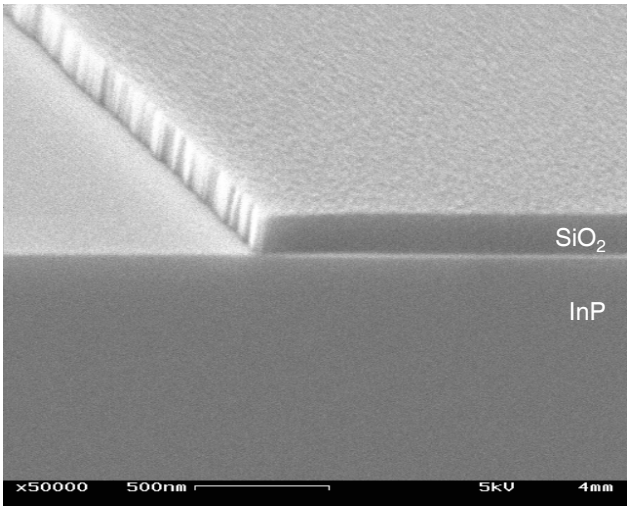
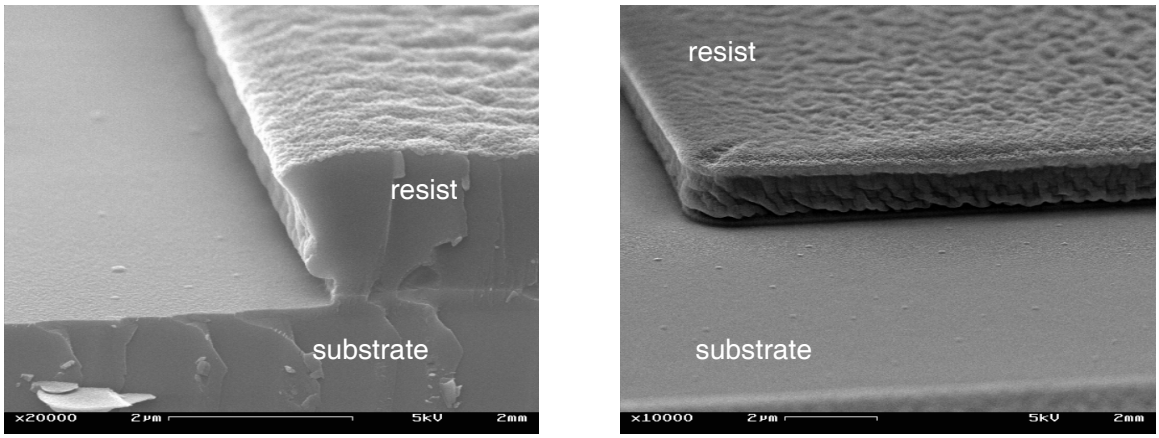


Figure 3-25: SEM micrograph showing rough oxide sidewall after RIE in CHF_3.

In order to improve the resist sidewalls, the wafer is exposed to a short He/O_2 plasma process for 10 sec (5 sccm/10 sccm He/O_2 , 20 mTorr, 150 W) prior to etch. High spots on the resist sidewall profile will be areas of slightly higher electric field concentration and will preferentially etch, thereby smoothing the resist sidewall. The effect is slight, but helps to eliminate any rough morphology from the photoresist.

The most dramatic improvements to the oxide etch came from two modifications: changing the gas chemistry to CF_4 and lowering the bias voltage to 50V. The CHF_3 etch at 100 V was forming a highly-textured film on the surface of the resist (Figure 3-26). The film is known to be fluorinated amorphous carbon [66]. This texture is transferred to the oxide in the form of roughness. The addition of oxygen to the plasma chemistry did not eliminate the film formation. Transition to a CF_4 chemistry immediately removed all evidence of the textured polymer. An alternative to the carbon-containing fluorine gases is $SF_{6,}$, but the gas was not available on the RIE system.

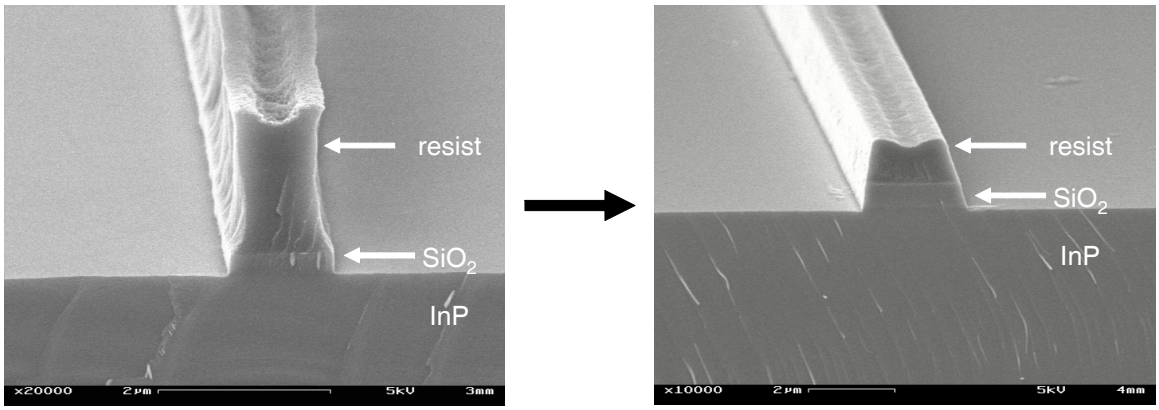


a) b)

Figure 3-26: SEM micrograph showing highly textured polymer formation on resist during RIE of the oxide using a CHF_3 plasma.

Furthermore, high voltage etches can significantly sputter photoresists because of the high-energy impact of ions from the plasma. Also, the higher voltages can lead to significant heating of the resist and outgassing of photolithographic reaction byproducts remaining in the resist. The damaged resist leads to additional roughness and poor pattern transfer. Lowering the RIE bias voltage to 50 V also made dramatic improvements to the sidewall profile. The post-etch SEM micrographs (Figure 3-27) show the progression from a rough, textured resist profile to a smooth resist profile as a result of changing the gas chemistry from CHF_3 to CF_4 and lowering the bias voltage from 100 V to 50 V. All other RIE-related processing parameters remained the same

(pressure, flow rate) and the etch rate did not change significantly from one gas chemistry to another.



a) b)

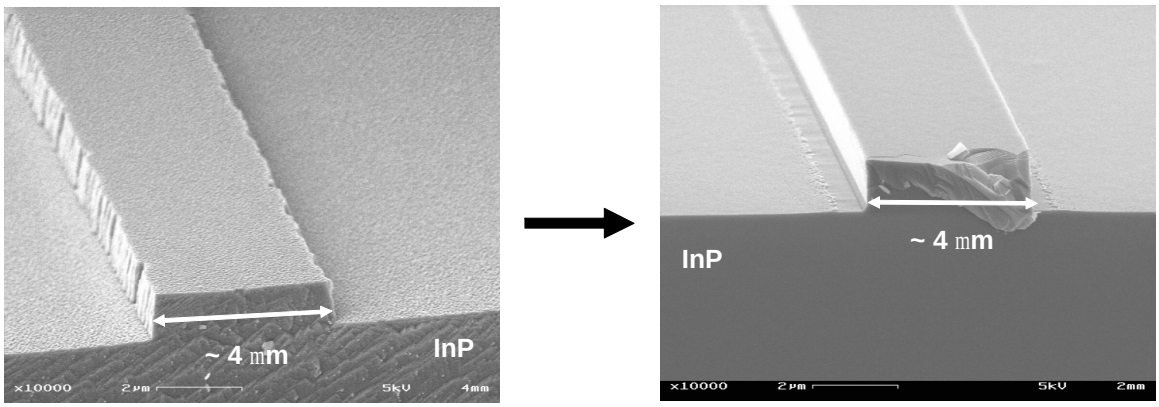
Figure 3-27 SEM micrographs of the oxide etch show that a) the high-voltage CHF_3 etch causes much more damage to the resist b) the low-voltage CF_4 etch. The result is a much smoother oxide hard mask.

3.9.5 Sidewall Roughness – RIE Etch of Semiconductor

The last improvement to the sidewall roughness problem was a change in the semiconductor RIE process. The initial InP etch process for the first generation devices used a $CH_4/H_2/O_2$ etch (25/30/0.5 sccm $CH_4/H_2/O_2$, 8.5 mTorr, 110V) in Perkin Elmer Model 3140 sputtering tool modified to carry out reactive ion etching. CH_4 etching of InP is prone to the formation of significant amounts of polymer material, which coats the sidewalls and the entire interior of the chamber. This polymer-based coating is extremely difficult to remove and leads to substantial problems with etch reliability, isotropy, and repeatability. A very low flow of O_2 (0.5 sccm) was added to help in the removal of the polymer, but did not improve the etch quality. Extensive cleaning and conditioning of the chamber does improve the etch characteristics, but repeatability is still a problem. In a device with two sequential semiconductor etch steps, repeatability of the etch is extremely important. Additionally, the chamber was also used for Cl-based chemistries and considerable cross-contamination could have been hindering the etch performance.

Inductively-coupled-plasma RIE (ICP-RIE) is a technique where a magnetic field within the chamber is created by an external oscillating electric field. The magnetic field generates a high-density plasma and the ions in the plasma are driven by a separate bias voltage towards the substrate. Traditional RIE forms a plasma using a capacitor arrangement, where the plasma is formed between two parallel plates with an oscillating electrical field. ICP also includes a parallel plate arrangement, but only for control of the voltage that drives the reactive species towards the substrate. This independent control of the plasma and the DC voltage allows for greater control over the etch characteristics, including improved anisotropy. Key advantages of ICP etching are higher density plasmas and generation of the magnetic field external to the chamber, avoiding contamination of the electrodes.

ICP-RIE etching was performed at Lincoln Laboratory using a SAMCO RIE 200 IP. Second generation devices were etched using a chlorine chemistry (0.5/0.5/10.0 sccm $SiCl_4/Cl_2$/Ar, 250 W bias, 250 W ICP). The chlorine ions react to form indium chloride ($InCl_3$), which has a low vapor pressure. Therefore, the sample is heated to 225°C in order to promote the desorption of the molecule from the etched surface. Compared to earlier CH_4/H_2 etches, the anisotropy and repeatability of the etch are dramatically improved. The etch rate also increased to nearly 150 nm/min. Additionally, CH_4/H_2 etches were subject to loading effects where the etch rate would vary with the amount of material in the vacuum chamber. The ICP-RIE etching showed no such dependence. The combination of the earlier improvements to the photoresist and oxide RIE with the greatly enhanced etch capabilities of the ICP RIE considerably reduced the sidewall roughness of the waveguides, which ultimately should reduce the scattering loss of the waveguides (Figure 3-28).



a) b)

Figure 3-28: By optimizing the photoresist, oxide RIE, and InP RIE, sidewall roughness was significantly improved from a) the first-generation devices to b) the second-generation devices as shown in SEM micrographs.

The repeatability of the CH_4/H_2 etch was a major hindrance to the development of operable devices. In addition to achieving two high-quality etches in a row, the second etch must not damage the ridge formed by the first etch. In between etches, a thick (450 nm) PECVD oxide is deposited, completely coating the top and sides of the ridge formed by the first etch. This oxide hard mask must not only serve as a pattern for the second etch, it must protect the active ridge and taper. Furthermore, the integrity of this protective layer must be maintained through the oxide RIE and the entirety of the ICP-RIE etch. The oxide hard mask etch rate in the ICP-RIE is significant (~30 nm/min), but using a sufficiently thick mask ensures the integrity of the active ridge is maintained. Figure 3-29 illustrates that the oxide mask remains after the completion of the passive ridge etch. The corners of the hard mask are faceted, but at no point does the mask erode completely.

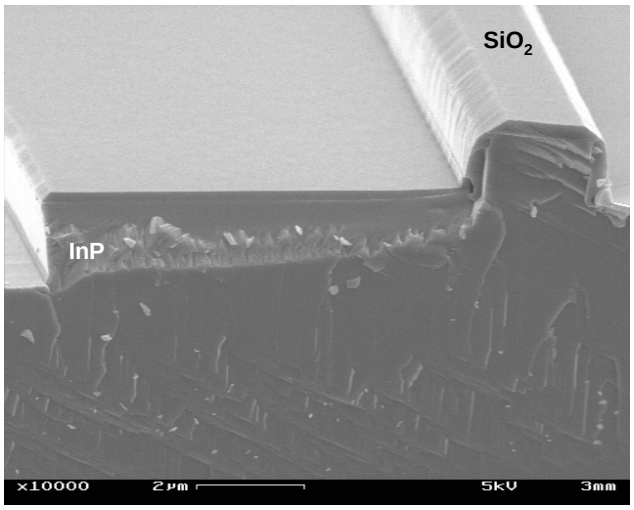


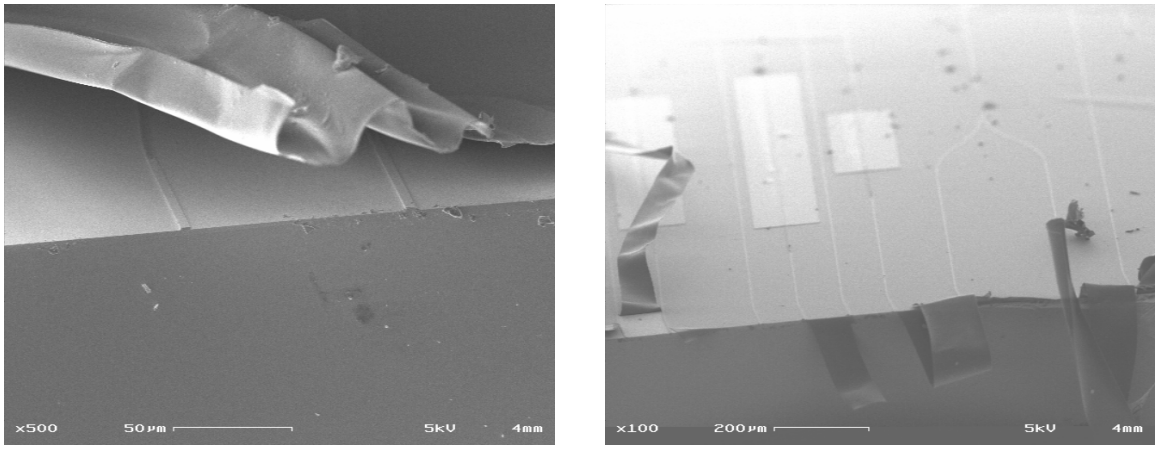
Figure 3-29: The second oxide deposition must protect the active waveguide during the passive waveguide etch.

3.9.6 Planarization

Planarization is an important component of most ridge waveguide device fabrications. The planarization layer normally serves to provide both electrical isolation layer and mechanical stability to the topside metal contact. The p-n junction at the heart of most active devices normally resides somewhere within the ridge. A topside electrical contact must connect to only one side of the junction to avoid short-circuiting the device. Furthermore, separate devices across the chip, for example, the two SOAs in the arms of the MZI, must be isolated from each other to allow independent electrical control. Therefore, the planarization layer must be electrically insulating. In addition, the planarization layer must provide good mechanical and thermal stability to the electrical contacts. Significant heating of the devices can occur during operation, so the materials must not show significant thermal expansion and must be robust enough to withstand electrical probing, packaging, and other device handling.

The first generation devices used a polyimide (HD Microsystems PI 2545) planarization layer. An adhesion promoter (HD Microsystems VM652) was first spun at 3000 rpm for 30 sec and hotplate-baked at 120°C for 60 sec. The polyimide was spun at 2000 rpm for 30 sec, hotplate soft-baked at 140°C for 4 minutes, and then cured in an N_2

furnace at 350°C for 1 hr. A slow temperature ramp was used to avoid cracking the polyimide during the curing process. A series of short RIE etch backs using CF_4/O_2 (3 sccm /15 sccm CF_4/O_2, 11 mTorr, 100 V) were performed until the top of the active ridge was revealed for metallization. However, upon inspection the polyimide was not a satisfactory planarization layer. The polyimide did not cleave well, delaminating from the substrate and elastically stretching rather than fracturing upon cleaving (Figure 3-30). Due to its bad adherence to the substrate, the delaminated polyimide would interfere with the cleaved facets of the passive waveguides and the lens fibers used to couple light into the waveguides. Additionally, the polyimide did not bury the waveguides, but instead conformally coated the ridges.



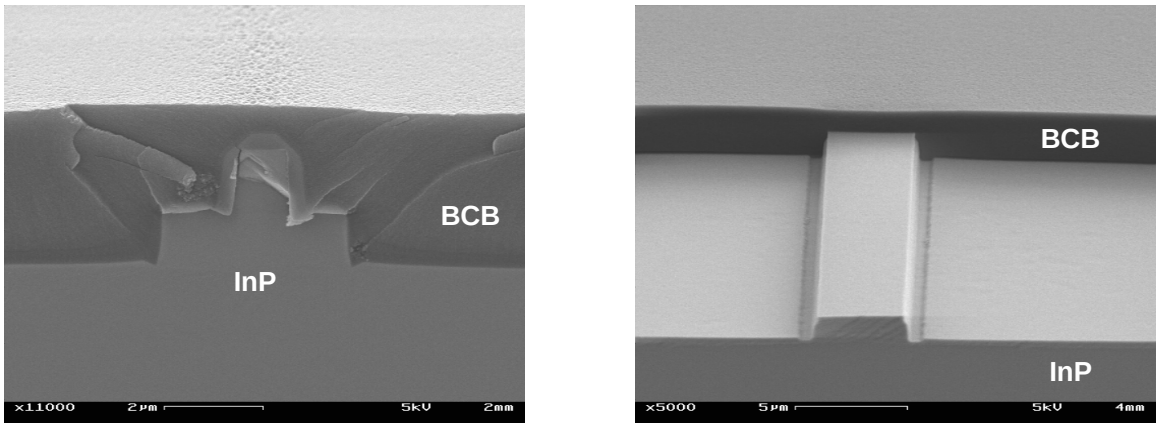
a) b)

Figure 3-30: The polyimide planarization layer showed extensive delamination and elastic extension rather than fracture at the cleaved facets.

Clearly, the polyimide process performance was not satisfactory for the first generation devices. A number of improvements were considered, including more extensive curing to improve the fracture behavior and liquid nitrogen cooling prior to cleaving to reduce the elastic behavior of the film. However, another material, benzocyclobutene (BCB), showed promise as a superior planarization layer for this application and was used for the second-generation devices. BCB is manufactured by

Dow Corning and sold as Cyclotene 3022-35 and is a spin-on low-dielectric film specifically designed for dry-etching.

The BCB process is very similar to that of polyimide. Prior to spin-on application, the wafer is dehydrated for 30 minutes in a 130°C oven and an adhesion promoter (Dow Corning AP3000) is spun at 2500 rpm and baked at 100°C for 1 min on a hotplate. The BCB is spun at 2500 rpm for 25 seconds to give a nominal BCB thickness of 1 μm. An additional benefit of the trench geometry used on the second-generation mask design is that the trenches trap the planarization liquid during the spin application, completely filling the trenches and providing superior planarization. The BCB is soft-cured on a hotplate at 100°C for 5 minutes. Profilometry measured roughly 10% variation in thickness even over ~2.5 μm deep trench features, a more than adequate uniformity across the substrate. Wider features tended to have slightly thicker BCB coverage than narrow features such as ridge waveguides. The complete burial of both active and passive ridges is shown in Figure 3-31.



a) b)

Figure 3-31: Benzocyclobutene (BCB) planarization of the second-generation devices. BCB provides uniform coverage and filling of deep features for both a) active and b) passive waveguide ridges.

Cured BCB is a dielectric comprised of both silicon and carbon containing molecules. In order to etch BCB, both CF_4 and O_2, respectively, are required to remove

those two constituents. Therefore, RIE using a CF_4/O_2 plasma is used to etch back the BCB and reveal the active ridge for metallization. The ratio of gases is important to the etch rate and etch characteristics [67, 68]. An O_2-rich etch will remove the carbon material, but will react with the silicon to from SiO_2. A CF_4-rich etch will remove the silicon but leave an amorphous carbon material behind. The etch rate is dependent on optimizing these two competing processes and a maximum etch rate of around 100 nm/min is achieved at a 60% CF_4 mixture (12 sccm/8 sccm CF_4/O_2, 15 mTorr, 100V). The etch must reveal the ridge – and only the ridge – so the etch is performed as a series of short etches with frequent microscope and profilometer inspections in between. The result of the etch is a ridge just barely revealed and surrounded by planar dielectric material (Figure 3-32).

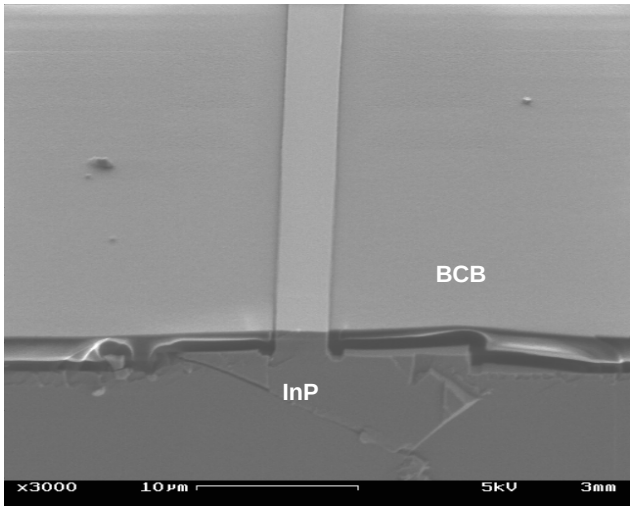


Figure 3-32: BCB etch back using 60%/40% CF_4/O_2 reveals the active ridge for metallization.

3.9.7 Backside Processing

The backside processing is seemingly simple but can greatly affect device operation. A number of processes must be performed on the wafer's backside. The thick wafer behaves as a resistor in series with the p-n diode that comprises the SOA active region. Therefore, the wafer should be thinned to reduce parasitic resistance.

Additionally, thinning the wafer greatly improves the quality of the cleaved facet and removes much of the damage induced by the fabrication process and extensive tweezer handling. Lapping was used to thin the wafer from 350 μm to approximately 150-175 μm thick. In the lapping procedure, the substrate is mounted to a glass plate (optical telescope lens blanks) using a wax that is soluble in trichloroethylene (TCE). The glass plate and wax is heated above the melting point of the wax (~150°C) and the wax is spread thin on the glass plate. Next, the substrate is placed on the glass plate and light pressure is applied to evenly seat the sample. Weighted blocks are placed on the sample to ensure intimate contact with the wax and the whole assembly is removed from the hotplate and allowed to cool. Any stray wax on the glass plate is scraped off and the whole plate is lightly rinsed with TCE. The samples are then hand-lapped in a figure-eight motion on a piece of optically smooth glass coated with a slurry of 5 μm Al_2O_3 powder and water. Once the sample has been lapped to the proper thickness, the sample is rigorously cleaned to remove any stray alumina particles.

The next step in the backside processing is polishing the wafer backside with a 1% bromine in methanol solution. The wafers are then immediately coated with Ni/Au/Ge/Au (300/600/300/2000 Å) in an electron beam evaporator (Temescal FCE-2500) while the samples remain mounted to the glass plate. Next, the samples are heated to melt the wax and are removed from the glass plate. Alternatively, the mounted wafers can be soaked in a warm TCE solution to more gently remove the wafer from the glass slide. The samples are rinsed thoroughly in TCE and isopropanol to remove any remaining wax from the wafer front side. In order to alloy the contacts on both the top and bottom of the substrate, the samples undergo a 30 second rapid thermal anneal (RTA) at 450°C.

At this stage, the samples must be prepared for eventual mounting to a heat sink. Prior to cleaving, the backside of the samples are sputter-coated with Ti/Pt/Au (500/700/500 Å) using a Denton Discovery 18 sputtering system. The samples are then cleaved using an automatic scriber machine (Loomis LSD-100). Machine cleaving of the devices is much more controlled than manual cleaving and allows for precise placement of the facets in relation to the angled waveguides.

Careful matching of the thermal coefficient of expansion (TCE) is important to device longevity and optimized performance. Often ignored for research and proof-of-concept devices, the mounting and soldering scheme is a vital processing step for commercially manufactured devices. Active devices can generate significant amounts of heat and thermal cycling of devices that are not TCE-matched can lead to fracture and delamination of the device from its mounting. Two mounting schemes were used for this study, each using materials TCE-matched to InP substrates (Figure 3-33). Indium solder was used for Cu mounts and $Au_{0.1}Sn_{0.9}$ solder was used for $Cu_{0.15}W_{0.85}$ mounts. Ti/Pt/Au was used to coat the mounts prior to soldering to promote adhesion and to improve thermal and electrical contact between the mount, solder, and substrate.

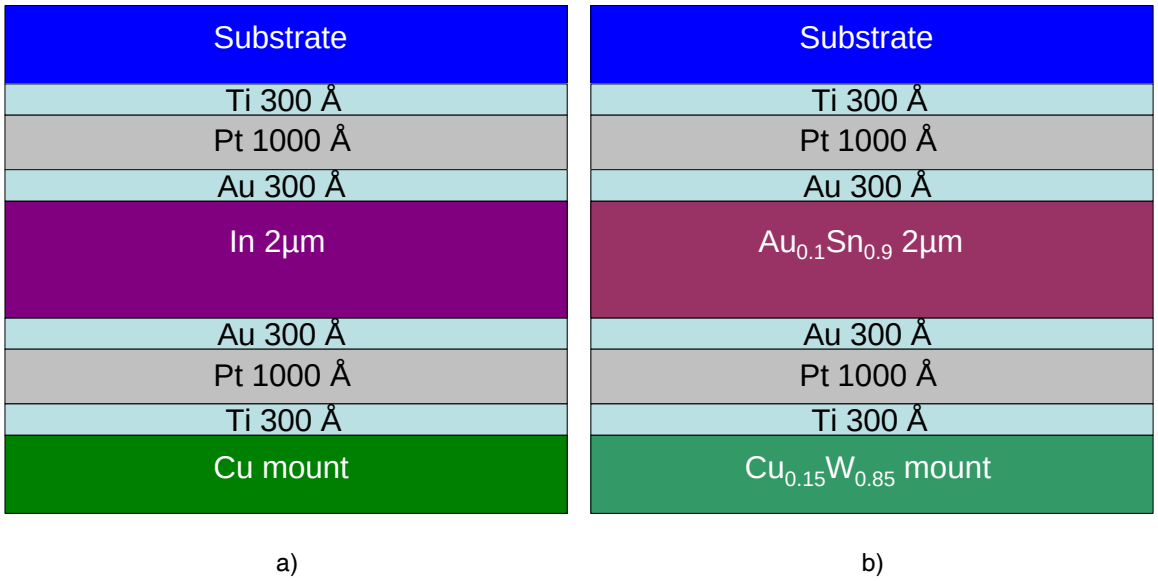


Figure 3-33: Matching the thermal coefficient of expansion of the mount, solder, and substrate is important to device longevity. Mounting schemes for the InP substrates included a) indium solder with a copper mount and b) AuSn solder with a CuW mount [69].

3.9.8 Final Devices

The second-generation devices are significant improvements over their first-generation counterparts. Substantial enhancements have been made in mask design, photoresist processing, sidewall roughness, RIE of the oxide, RIE of the semiconductor,

planarization, and backside processing. Carefully monitoring and optimizing each individual step of the process is vital to realizing devices with improved operation. Figure 3-34 illustrates the substantial improvements in etch quality and alignment in the second-generation devices.

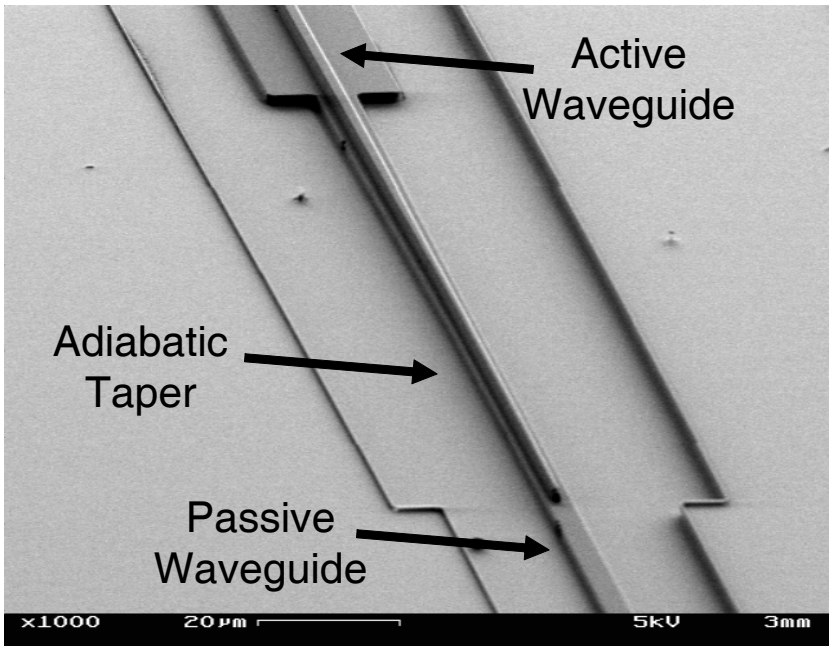
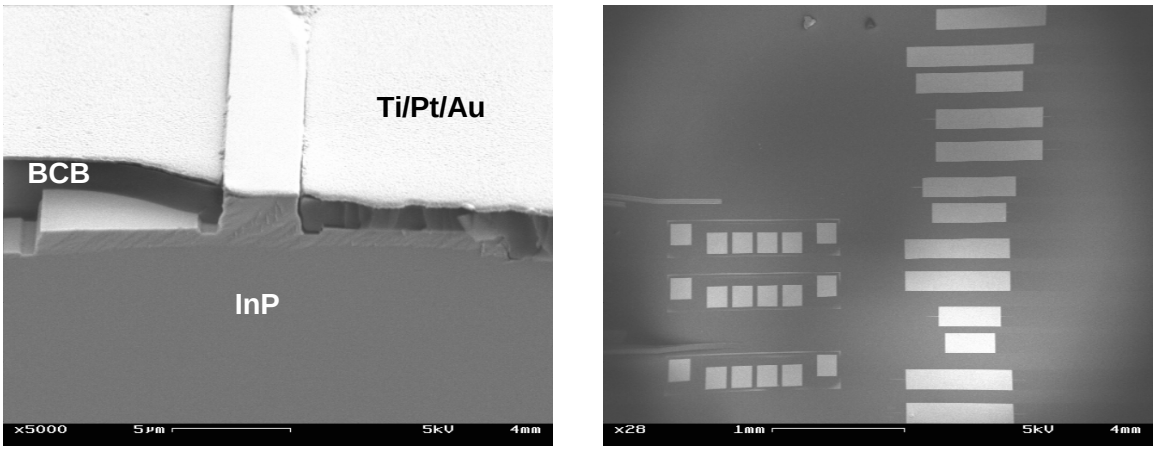


Figure 3-34: Fabricated second-generation twin waveguide.

Scanning electron microscopy micrographs of fully fabricated devices are shown in Figure 3-35. There are many potential improvements in subsequent generations of these devices, but the second-generation devices are a substantial improvement and an adequate platform for testing the concept of all-optical photonic switching using asymmetric twin waveguide semiconductor optical amplifiers in a Mach-Zehnder interferometer.



a) b)

Figure 3-35: Fully fabricated device with metal contacts.

3.10 Device Testing

The majority of device testing is performed at Lincoln Laboratory by Jade Wang. With the wide variety of devices, there is a substantial number of tests to be performed in order to adequately characterize the devices. The first step in device testing is simply to couple light in and out of the waveguides. After confirming that the waveguides confine and transmit light, it is useful to determine the waveguide loss, as this is essential to understanding the overall device characteristics.

The Hakki-Paoli method is a widely used technique for measuring waveguide loss based on the Fabry-Perot fringes resulting from reflections within the cavity formed by the waveguide facets [70]. The testing setup is shown in Figure 3-36. The sample is first lowered out of the optical path and optical fiber is aligned to a 5x microscope objective and imaged to a CCD camera. A tunable laser supplies optical power to the fiber and the light is amplified before entering the lens optical fiber interface (LOFI). The sample is then moved into the optical path and adjusted until the distinct waveguide output can be seen on the video monitor. Once the optical mode of the waveguide has been detected, a flip mirror is engaged to direct the light to an optical power meter.

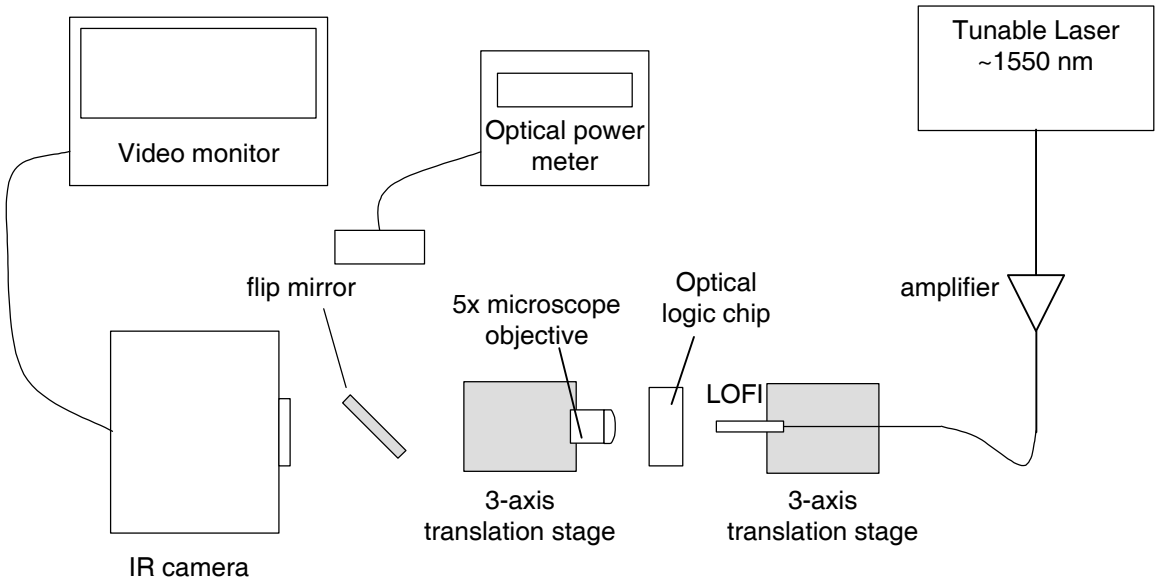


Figure 3-36: Schematic of the optical logic testing setup.

In the Hakki-Paoli method, the tunable laser wavelength is modulated while the output power is monitored. Due to the fixed length of the optical cavity, there are Fabry-Perot resonances within the cavity and the output power will oscillate as the wavelength changes. By comparing the minimum and maximum powers the internal loss of the device can be estimated using Equation 3-1. As a function of the wavelength, λ, the internal loss, α, of the waveguide of length, L, and having facet reflectivities, R_1 and R_2, can be determined by monitoring the maxima and minima of the power, P_{max} and P_{min}. For passive device testing, the angled facets were cleaved away, creating facets perpendicular to the waveguides and increasing the magnitude of the reflections within the cavity to help obtain better measurements.

$$a(l) = \frac{1}{L}\ln\left(\frac{\sqrt{P_{\max}} + \sqrt{P_{\min}}}{\sqrt{P_{\max}} - \sqrt{P_{\min}}}\right) + \frac{1}{2L}R_1R_2 \qquad \text{Equation 3-1}$$

The following values were used for the calculation:

$R_1 = R_2 = 0.272$ (Calculated using n=3.18)
$P_{max} = -4.4\text{dBm} = 3.63 \times 10^{-4}$ W
$P_{min} = -7.4\text{dBm} = 1.82 \times 10^{-4}$ W
$\lambda = 1551.6$ nm
L = 0.35 cm

The measurements and results are shown in Figure 3-37. The internal loss of a straight waveguide was determined to be 0.89 cm^{-1}, a value that is comparable to typical waveguide loss measurements [71]. The same technique was used to measure the bending loss of waveguides. Waveguides were constructed containing 2, 4, 6, 8, and 10 bends (see Appendix 5.4). There is significant difference in the internal loss between a straight waveguide and a waveguide with two bends. Increasing the number of bends increases the loss, but not as dramatically as the first set of bends.

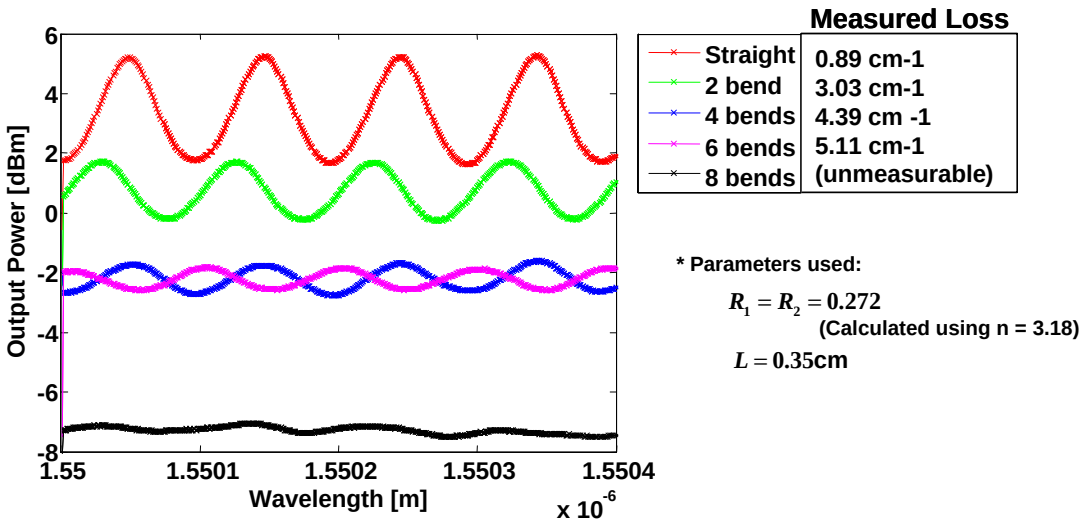


Figure 3-37: Fabry-Perot resonances of the waveguide are used to estimate the internal loss of the waveguide and the waveguide bends. Courtesy Jade Wang.

The next device to be characterized was the MMIs to confirm that they are effectively splitting power from one input waveguide to two output waveguides. Images from the CCD camera are shown in Figure 3-38. When light is directed into a single input waveguide of the MMI, two distinct spots are seen at the output waveguides. Due to their close proximity, the optical power of each output waveguide cannot be determined without coupling to optical fibers at the output. Qualitatively, the intensity of the spots appears approximately equivalent, which indicates that the MMI is most likely achieving near 3 dB power splitting. Further measurements to characterize the MMIs are ongoing.

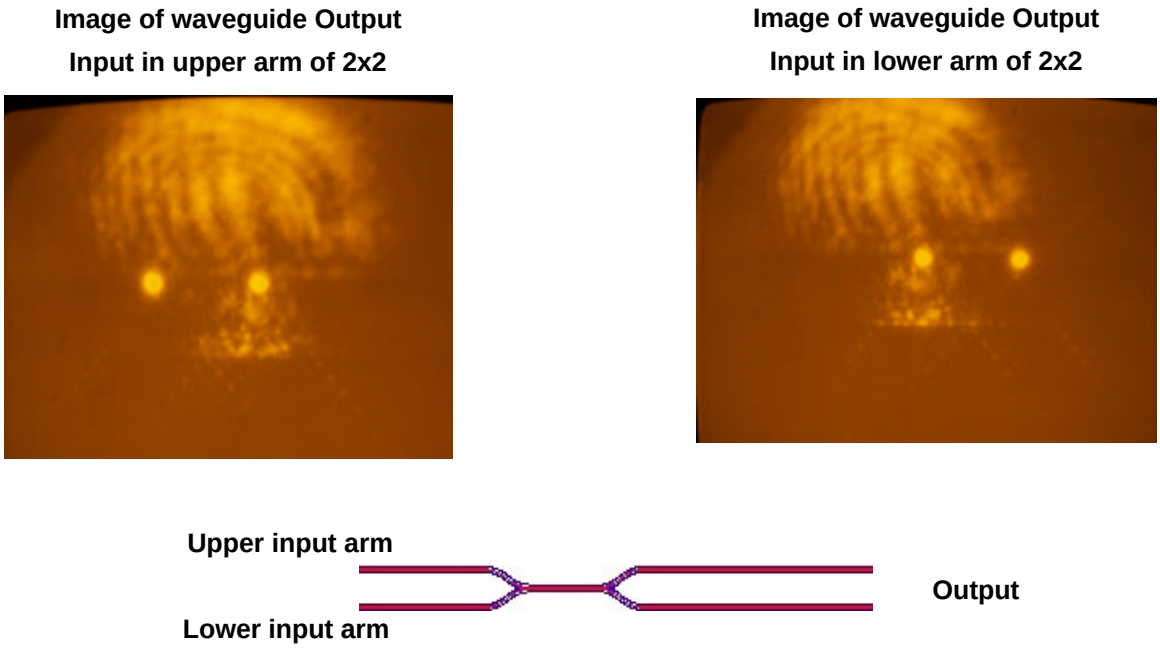


Figure 3-38: The two spots seen in images from the CCD camera demonstrate that the 2x2 MMI is splitting optical power from a single input waveguide to two output waveguides.

Active device testing confirmed that the semiconductor optical amplifiers exhibit diode-like behavior and emit at 1550 nm. When a continuous-wave signal at 1550 nm is coupled to the passive waveguide input, the intensity of the light at the waveguide output increases with increasing current to the SOA, demonstrating both gain and coupling between the passive and active waveguides. Gain characteristics of a representative SOA are shown in Figure 3-39. More extensive characterization of the SOAs as well as testing of the optical logic unit cell and wavelength converters is forthcoming.

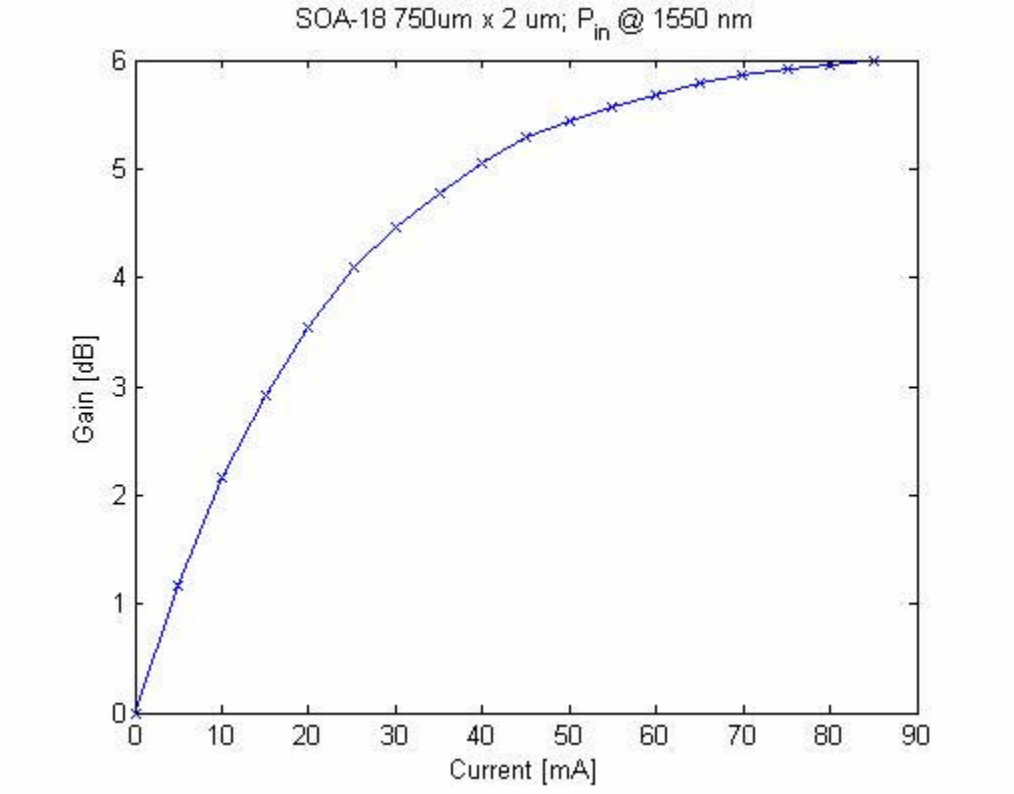


Figure 3-39: Gain characteristics of the SOAs with increasing current. Initial device testing of the SOAs demonstrated amplification of a continuous-wave input signal and coupling between the active and passive waveguides. Courtesy Jade Wang.

3.11 Summary

The optical logic unit cell is the photonic analog to transistor-transistor logic in electronic devices. Active devices such as SOAs are integrated with passive waveguides using the asymmetric twin waveguide technology and SOAs are placed in a Mach-Zehnder interferometer configuration. By sending in high-intensity pulses, the gain characteristics, phase-shifting, and refractive indices of the SOA can be altered, creating constructive or deconstructive interference at the MZI output. Boolean logic and wavelength conversion can be achieved using this technique, forming the building blocks for optical switching and signal regeneration.

The fabrication of these devices is complex and two generations of devices were fabricated. The mask design was improved from the first to second generation of devices. In the second-generation fabrication, optimizing the photoresist, oxide RIE etch, semiconductor ICP-RIE etch, and the backside processing improved the quality of the devices. Testing of the devices determined that the internal loss of the dilute passive waveguides is 0.89 cm^{-1}. The MMI couplers showed power splitting from one input waveguide to two output waveguides. Initial testing of the SOAs confirmed that the SOAs emit at 1550 nm, that the tapers evanescently couple the active and passive regions, and that the devices amplify the intensity of incident signals. Further testing of active devices such as SOAs, wavelength converters, and the optical logic unit cell is ongoing.

3.12 References

1. Hamilton, S.A. and B.S. Robinson, *40-Gb/s all-optical packet synchronization and address comparison for OTDM networks.* IEEE Photonics Technology Letters, 2002. **14**(2): p. 209-211.
2. Robinson, B.S., S.A. Hamilton, and E.P. Ippen, *Demultiplexing of 80-Gb/s pulse-position modulated data with an ultrafast nonlinear interferometer.* IEEE Photonics Technology Letters, 2002. **14**(2): p. 206-208.
3. Patel, N.S., K.L. Hall, and K.A. Rauschenbach, *Interferometric all-optical switches for ultrafast signal processing.* Applied Optics, 1998. **37**(14): p. 2831-2842.
4. Mauger, R. and C. Rosenberg, *QoS guarantees for multimedia services on a TDMA-based satellite network.* IEEE Communications Magazine, 1997. **35**(7): p. 56-65.
5. Wang, J. and T. Zaman, *Personal Conversation, High Speed Space Networks*. 2006.
6. Studenkov, P.V., et al., *Monolithic integration of a quantum-well laser and an optical amplifier using an asymmetric twin-waveguide structure.* IEEE Photonics Technology Letters, 1998. **10**(8): p. 1088-1090.
7. Studenkov, P.V., M.R. Gokhale, and S.R. Forrest, *Efficient coupling in integrated twin-waveguide lasers using waveguide tapers.* IEEE Photonics Technology Letters, 1999. **11**(9): p. 1096-1098.
8. Studenkov, P.V., et al., *Monolithic integration of an all-optical Mach-Zehnder demultiplexer using an asymmetric twin-waveguide structure.* IEEE Photonics Technology Letters, 2001. **13**(6): p. 600-602.
9. Studenkov, P.V., et al., *Asymmetric twin-waveguide 1.55-mu m wavelength laser with a distributed Bragg reflector.* IEEE Photonics Technology Letters, 2000. **12**(5): p. 468-470.
10. Mamyshev, P., C. Rassmussen, and B. Mikkelsen. *40-Gb/s upgradability of 10-Gb/s systems*. in *Advanced Modulation Formats, 2004 IEEE/LEOS Workshop on*. 2004.
11. Pau, S., et al., *160-Gb/s all-optical MEMS time-slot switch for OTDM and WDM application.* IEEE Photonics Technology Letters, 2002. **14**(10): p. 1460-1462.
12. Hamilton, S., *Personal Conversation.* 2006.
13. MIller, S.E., *Integrated optics - An introduction (Laser beam circuitry miniaturization facilitating laser circuit assembly isolation from thermal, mechanical and ambient changes).* Bell System Technical Journal, 1969. **48**: p. 2059-2069.
14. Koren, U., et al., *Monolithic Integration of a Very Low Threshold Gainasp Laser and Metal-Insulator-Semiconductor Field-Effect Transistor on Semi-Insulating Inp.* Applied Physics Letters, 1982. **40**(8): p. 643-645.
15. Soda, H., et al., *High-Power and High-Speed Semi-Insulating BH Structure Monolithic Electroabsorption Modulator DFB Laser-Light Source.* Electronics Letters, 1990. **26**(1): p. 9-10.
16. Kawamura, Y., et al., *Monolithic Integration of a DFB Laser and an MQW Optical Modulator in the 1.5 mu-m Wavelength Range.* IEEE Journal of Quantum Electronics, 1987. **23**(6): p. 915-918.

17. Dragone, C., *An N X N Optical Multiplexer Using a Planar Arrangement of 2 Star Couplers.* IEEE Photonics Technology Letters, 1991. **3**(9): p. 812-815.
18. Smit, M.K., *New Focusing and Dispersive Planar Component Based on an Optical Phased-Array.* Electronics Letters, 1988. **24**(7): p. 385-386.
19. Zirngibl, M., et al., *Digitally Tunable Laser-Based on the Integration of a Wave-Guide Grating Multiplexer and an Optical Amplifier.* IEEE Photonics Technology Letters, 1994. **6**(4): p. 516-518.
20. Nagarajan, R., et al., *Large-scale photonic integrated circuits.* IEEE Journal of Selected Topics in Quantum Electronics, 2005. **11**(1): p. 50-65.
21. Aiki, K., M. Nakamura, and J. Umeda, *Frequency-Multiplexing Light-Source with Monolithically Integrated Distributed-Feedback Diode-Lasers.* IEEE Journal of Quantum Electronics, 1977. **13**(4): p. 220-223.
22. Sysak, M.N., et al., *A single regrowth integration platform for photonic circuits incorporating tunable SGDBR lasers and quantum-well EAMs.* IEEE Photonics Technology Letters, 2006. **18**(13-16): p. 1630-1632.
23. Koontz, E.M., et al., *Overgrowth of (In,Ga)(As,P) on rectangular-patterned surfaces using gas source molecular beam epitaxy.* Journal of Crystal Growth, 1999. **199**: p. 1104-1110.
24. Berger, P.R., et al., *GaAs Quantum-Well Laser and Heterojunction Bipolar-Transistor Integration Using Molecular-Beam Epitaxial Regrowth.* Applied Physics Letters, 1991. **59**(22): p. 2826-2828.
25. Auvray, P., et al., *Epitaxial Regrowth of (100) InP Layers Amorphized by Ion-Implantation at Room-Temperature.* Journal of Applied Physics, 1982. **53**(9): p. 6202-6207.
26. Gaumont, E.G., et al. *Butt coupling process for InP based photonic integrated circuits*. in *International Conference on Indium Phosphide and Related Materials*. 1996.
27. Koontz, E.M., *The Development of Components for Ultrafast All-Optical Communications Networks*, in *Electrical Engineering*. 2000, Massachusetts Institute of Technology.
28. Skogen, E.J., et al., *High contrast InP/InGaAsP grating MOCVD regrowth using TBA and TBP.* Journal of Crystal Growth, 2004. **272**(1-4): p. 564-569.
29. Marsh, J.H., *Quantum-Well Intermixing.* Semiconductor Science and Technology, 1993. **8**(6): p. 1136-1155.
30. Thornton, R.L., W.J. Mosby, and T.L. Paoli, *Monolithic Wave-Guide Coupled Cavity Lasers and Modulators Fabricated by Impurity Induced Disordering.* Journal of Lightwave Technology, 1988. **6**(6): p. 786-792.
31. McDougall, S.D., et al., *Monolithic integration via a universal damage enhanced quantum-well intermixing technique.* Ieee Journal of Selected Topics in Quantum Electronics, 1998. **4**(4): p. 636-646.
32. Marsh, J.H. and A.C. Bryce, *Fabrication of Photonic Integrated-Circuits Using Quantum-Well Intermixing.* Materials Science and Engineering B-Solid State Materials for Advanced Technology, 1994. **28**(1-3): p. 272-278.
33. Ooi, B.S., et al., *Effect of p and n doping on neutral impurity and SiO2 dielectric cap induced quantum well intermixing in GaAs/AlGaAs structures.* Semiconductor Science and Technology, 1997. **12**(1): p. 121-127.
34. Djie, H.S., et al., *Group-III vacancy induced InxGa1-xAs quantum dot interdiffusion.* Physical Review B, 2006. **73**(15): p. -.

35. Si, S.K., et al., *Area selectivity of InGaAsP-InP multiquantum-well intermixing by impurity-free vacancy diffusion.* IEEE Journal of Selected Topics in Quantum Electronics, 1998. **4**(4): p. 619-623.
36. Terui, H., et al., *Hybrid Integration of a Laser Diode and High-Silica Multimode Optical Channel Wave-Guide on Silicon.* Electronics Letters, 1985. **21**(15): p. 646-648.
37. Joppe, J.L., A.J.T. Dekrijger, and O.F.J. Noordman, *Hybrid Integration of Laser Diode and Monomode High Contrast Slab Wave-Guide on Silicon.* Electronics Letters, 1991. **27**(2): p. 162-163.
38. Friedrich, E.E.L., et al., *Hybrid Integration of Semiconductor-Lasers with Si-Based Single-Mode Ridge Wave-Guides.* Journal of Lightwave Technology, 1992. **10**(3): p. 336-340.
39. Schleuning, D.A., et al., *Packaging multiple active and passive elements in a hybrid optical platform.* Journal of Lightwave Technology, 2004. **22**(5): p. 1320-1326.
40. Giziewicz, W.P. and C.G. Fonstad, *Optoelectronic integration using aligned metal-to-semiconductor bonding.* Journal of Vacuum Science & Technology A - Vacuum Surfaces and Films, 2002. **20**(3): p. 1052-1056.
41. Suematsu, Y., M. Yamada, and K. Hayashi, *Integrated Twin-Guide AlGaAs Laser with Multiheterostructure.* IEEE Journal of Quantum Electronics, 1975. **QE11**(7): p. 457-460.
42. Campbell, J.C. and D.W. Bellavance, *Monolithic Laser Waveguide Coupling by Evanescent Fields.* IEEE Journal of Quantum Electronics, 1977. **13**(4): p. 253-255.
43. Markina, A., *Design and Simulation for the Fabrication of Integrated Semiconductor Optical Logic Gates*, in *Electrical Engineering PhD Thesis*. 2005, MIT.
44. Studenkov, P.V., *Photonic Integration Using Assymetric Twin Waveguides*, in *Department of Electrical Engineering*. 2001, Princeton University.
45. Forrest, S.R., M.R. Gokhale, and P.V. Studenkov, *Photonic Integrated Detector Having a Plurality of Assymetric Twin Waveguides*. 2001, The Trustees of Princeton University: United States Patent.
46. Shiu, K.T., S.S. Agashe, and S.R. Forrest, *A simple monolithically integrated optical receiver consisting of an optical preamplifier and a p-i-n photodiode.* IEEE Photonics Technology Letters, 2006. **18**(5-8): p. 956-958.
47. Hou, L.P., et al., *Electroabsorption modulated semiconductor optical amplifier monolithically integrated with spot-size converters.* Journal of Crystal Growth, 2006. **288**(1): p. 148-152.
48. Tong, W., et al., *An asymmetric twin waveguide eight-channel polarization-independent arrayed waveguide grating with an integrated photodiode array.* IEEE Photonics Technology Letters, 2004. **16**(4): p. 1170-1172.
49. Xia, F.N., et al., *Monolithic integration of a semiconductor optical amplifier and a high bandwidth p-i-n photodiode using asymmetric twin-waveguide technology.* IEEE Photonics Technology Letters, 2003. **15**(3): p. 452-454.
50. Verdiell, J.M., M. Ziari, and D.F. Welch, *Low-loss coupling of 980 nm GaAs laser to cleaved singlemode fibre.* Electronics Letters, 1996. **32**(19): p. 1817-1818.

51. Shih, M.H., et al., *Alignment-Relaxed 1.55-mu-m Multiquantum-Well Lasers Fabricated Using Standard Buried Heterostructure Laser Processes.* Electronics Letters, 1995. **31**(13): p. 1058-1060.
52. Vusirikala, V., et al., *GaAs-AlGaAs QW diluted waveguide laser with low-loss, alignment-tolerant coupling to a single-mode fiber.* IEEE Photonics Technology Letters, 1996. **8**(9): p. 1130-1132.
53. Rabus, D.G., *Optical Multi-Mode Interference Devices Based on Self-Imaging: Principles and Applications*. 2002, Heinrich-Hertz-Instiut für Nachrichtentechnik: Berlin.
54. Besse, P.A., et al., *New 2x2 and 1x3 multimode interference couplers with free selection of power splitting ratios.* Journal of Lightwave Technology, 1996. **14**(10): p. 2286-2293.
55. Leuthold, J., et al., *Multimode interference couplers for the conversion and combining of zero- and first-order modes.* Journal of Lightwave Technology, 1998. **16**(7): p. 1228-1239.
56. Adams, M.J., et al., *Nonlinearities in Semiconductor-Laser Amplifiers.* Optical and Quantum Electronics, 1995. **27**(1): p. 1-13.
57. Mork, J., et al., *The role of fast carrier dynamics in SOA based devices.* IEICE Transactions on Electronics, 2004. **E87C**(7): p. 1126-1133.
58. Dagens, B., et al., *Design optimization of all-active Mach-Zehnder wavelength converters.* IEEE Photonics Technology Letters, 1999. **11**(4): p. 424-426.
59. Tajima, K., S. Nakamura, and Y. Sugimoto, *Ultrafast polarization-discriminating Mach-Zehnder all-optical switch.* Applied Physics Letters, 1995. **67**(25): p. 3709-3711.
60. Nielsen, M.L., et al., *40 Gbit/s standard-mode wavelength conversion in all-active MZI with very fast response.* Electronics Letters, 2003. **39**(4): p. 385-386.
61. Durhuus, T., et al., *All-Optical Wavelength Conversion by SOAs in a Mach-Zehnder Configuration.* IEEE Photonics Technology Letters, 1994. **6**(1): p. 53-55.
62. Durhuus, T., et al., *All-optical wavelength conversion by semiconductor optical amplifiers.* Journal of Lightwave Technology, 1996. **14**(6): p. 942-954.
63. Schilling, M., et al., *Wavelength Converter Based on Integrated All-Active 3-Port Mach-Zehnder Interferometer.* Electronics Letters, 1994. **30**(25): p. 2128-2130.
64. Lothian, J.R., F. Ren, and S.J. Pearton, *Mask Erosion During Dry Etching of Deep Features in III-V Semiconductor Structures.* Semiconductor Science and Technology, 1992. **7**(9): p. 1199-1209.
65. Chakrabarti, U.K., S.J. Pearton, and F. Ren, *Sidewall Roughness During Dry Etching of InP.* Semiconductor Science and Technology, 1991. **6**(5): p. 408-410.
66. Ren, F., et al., *Reduction of Sidewall Roughness During Dry Etching of SiO2.* Journal of Vacuum Science & Technology B, 1992. **10**(6): p. 2407-2411.
67. Baklanov, M.R., et al., *Effects of oxygen and fluorine on the dry etch characteristics of organic low-kappa dielectrics.* Journal of Vacuum Science & Technology B, 1999. **17**(2): p. 372-379.
68. Schier, M., *Reactive Ion Etching of Benzocyclobutene Using a Silicon-Nitride Dielectric Etch Mask.* Journal of the Electrochemical Society, 1995. **142**(9): p. 3238-3240.
69. Young, S.Y., *Characterization of Novel III-V Semiconductor Devices*, in *Electrical Engineering*. 2006, Massachusetts Institute of Technology.

70. Hakki, B.W. and T.L. Paoli, *CW Degradation at 300 Degrees K of GaAs Double-Heterostructure Junction Lasers .2. Electronic Gain.* Journal of Applied Physics, 1973. **44**(9): p. 4113-4119.
71. Kim, H.S., et al., *All-optical wavelength conversion in SOA-based Mach-Zehnder interferometer with monolithically integrated loss-coupled DFB laser diode.* Semiconductor Science and Technology, 2004. **19**(5): p. 574-578.

CHAPTER 4

Future Work

4.1 Quantum Dot Lasers at 1550 nm

InAs dots on InP substrates are a promising area of research. InAs dots on GaAs substrates is a relatively well-explored area and materials limitations seem to confine emission to the 1310 nm window. By moving to InP substrates, it is possible to extend the emission wavelength of quantum dots towards 1550 nm and beyond[1, 2]. Furthermore, moving to InAs quantum dots on InP implies compatibility with high-speed InP electronics. However, the scheme has increased complexity as an additional element, phosphorus, is introduced to the system. On GaAs, one must only be concerned with the interdiffusion of Ga-In. Now, in addition to the group-III interdiffusion, the group-V interdiffusion must also be considered.

The recent acquisition and installation of a Veeco Gen200 dual-chamber MBE system allows the growth of epitaxial structures unavailable on the previous Riber 32P system. The Veeco MBE is shown in Figure 4-1 and features two chambers, one primarily for InGaAsP materials and a second chamber for the investigation of newer materials systems such as antimonide and dilute nitride systems.

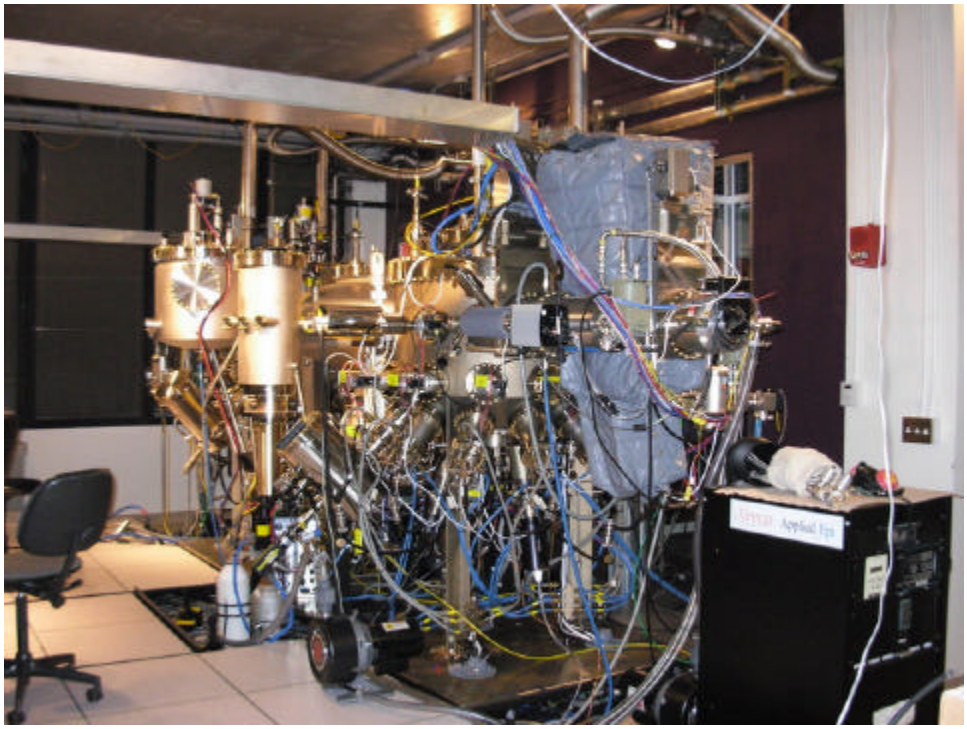


Figure 4-1: The Veeco Gen200 dual-chamber molecular beam epitaxy system.

With a newly installed MBE system, novel materials can be investigated to explore 1550 emission on both GaAs and InP substrates. A number of different schemes could prove promising candidates for quantum dot lasers and semiconductor optical amplifiers operating at 1550 nm.

Antimonide systems allow the substrate material to remain GaAs but the wavelength to be further extended towards 1550 nm. Dilute nitrides, incorporating a small percentage of nitrogen into the GaAs lattice, have proven to be viable candidates for 1310 and 1550 nm emission. Dilute nitrides are generally limited by problems with

nitrogen out-diffusion and 1550 nm emission remains difficult. However, the addition of antimony to the GaInNAs material, either as a surfactant or directly incorporated in the crystal, allows for higher percentage indium incorporation and therefore a greater redshift in the emission wavelength [3, 4]. Antimony incorporation has the added benefit of reducing the overall strain in the material, as they compensate for the compressive strain introduced by the nitrogen.

Quantum dots, dilute nitrides, antimonides, and other surfactant-aided growth techniques are all potential candidates for generating semiconductor lasers emitting at 1550 nm. They are all fertile areas for future research and development, as well as potential incorporation in existing device structures.

4.2 Photonic Switches

A third-generation of the optical logic devices could incorporate a number of design and fabrication improvements. More complex devices could be considered, including MZIs with multiple SOAs and cascades of several MZIs to create complicated optical logic structures with increased functionality.

A key consideration when designing more complex optical logic structures is the fabrication tolerance of the device. Especially with such large devices, small, localized defects such as scratches or surface damage from processing can render an entire device inoperable. Particularly for commercial applications, robust designs that mollify defects are highly desirable. One attractive approach is to create redundant optical waveguides in a configuration that allows the device to be operated even if a particular waveguide or device is inoperable, as shown in Figure 4-2 [5]. Furthermore, it allows for reconfiguration of the device should a particular component fail during the lifetime of the device. This approach is flexible but comes at the cost of increased consumption of valuable on-chip real estate and could potentially complicate cascading schemes. However, for discrete chips or research applications where processing is limited to only a few wafers, redundant components could potentially increase the yield of operable devices.

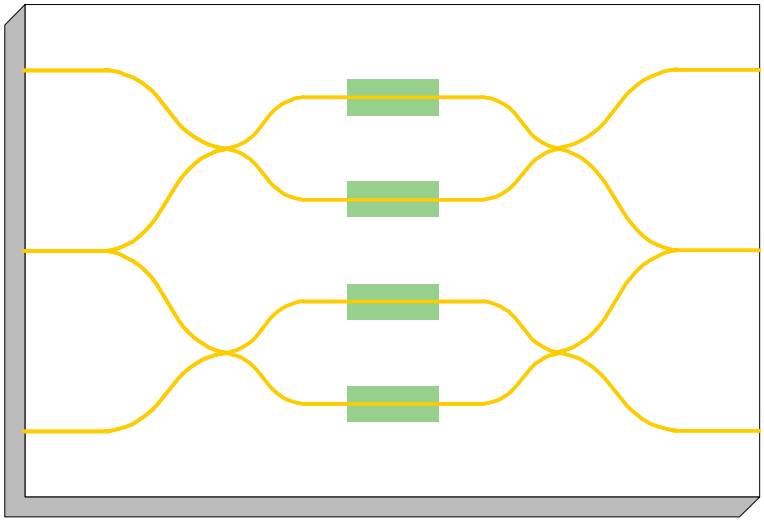


Figure 4-2: A optical logic unit cell constructed with redundancy. Should an SOA or waveguide fail, the device can be reconfigured and still operate [5].

Signal loss within the optical logic structure is a problem that can be counteracted with the incorporation of additional SOAs into the device. As opposed to the SOAs used for phase-shifting, the additional SOAs would be operated solely in the gain regime and would be used to control the amplitude of the signals. As the phase-shift and refractive index change of the SOAs are dependent on the intensity of the incoming optical signals, it is extremely important to properly balance the amplitude of the incoming signals. In practice, this greatly complicates the final optical logic structure because as many as eight different electrical contacts would be required. At the very least, electrical interconnects and bond pads would be needed to allow for current injection. A full-fledged electrical package compatible with multiple current probes would most likely need to be developed. Furthermore, supplying current to eight different SOAs requires either eight different current sources or the development of an electrical circuit that can divide current from one or more current sources. This complexity is beyond the scope of this thesis, but has been addressed for other photonic devices and is not an insurmountable challenge for third-generation devices.

Cascading of multiple MZI devices is an important step towards the development of integrated photonic circuits of increased functionality. However, the combination of

just three optical logic cells requires the addition of other technologies and devices and the integration rapidly beings to get immensely complicated, as shown in Figure 4-3.

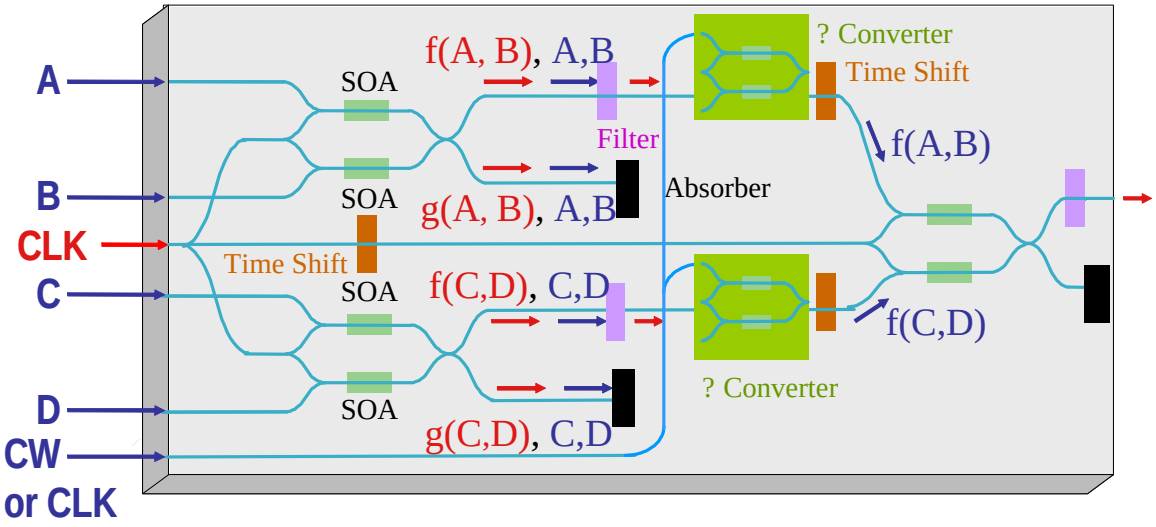


Figure 4-3: Cascading just three optical logic unit cells together involves complicated design and careful consideration of systems-level operation [6]. Courtesy Gale Petrich.

The output of a single optical logic cell contains multiple signals propagating on different wavelengths. Once cascaded, the output of a single optical logic unit cell becomes the input of the next optical logic cell. However, only one signal on one wavelength can be the input to the unit cell, so the other co-propagating wavelengths must be removed. Additionally, if a waveguide is terminated, the signal will not simply stop but could be reflected back into the optical logic unit cell. Some optical logic devices actually work in this counter-propagating configuration [7], but these back reflections are undesirable in this particular design, so absorbers must be included to capture signals at terminated waveguides.

Multiple clock signals are required for this device, one for each optical logic unit cell. However, the clock signals' arrival must be coordinated with the arrival of the data streams so precise control over the optical path length and time delays is extremely important. Time delays must be incorporated throughout the circuit to ensure that the

data signals arrive in the correct sequence. Intermittent wavelength converters may also be required to ensure that the data is encoded on the appropriate wavelength. In fact, with so many data signals propagating on multiple wavelengths within even this elementary integrated device, control over the signal traffic is an important problem that must be investigated. Photodetectors may be required to monitor optical power and to provide feedback to the amplifiers to adjust the intensity of the arriving signals. The whole device requires appropriate packaging and supporting electronics to control the devices.

4.3 Quantum Dot Optical Logic

Quantum dot semiconductor optical amplifiers have already been demonstrated [8-10] and could be further integrated into asymmetric twin waveguide devices and optical logic structures. Quantum dots offer a number of advantages that makes them ideal for this application. The fast carrier dynamics and short recovery times of quantum dots could enable even faster switching of SOAs and ultrafast operation in excess of 200 GHz [11]. Spectral hole burning studies of quantum dots have been used to investigate the gain recovery and carrier capture dynamics of quantum dots and have shown extremely fast gain recovery times of ~130 fs [12]. However, most of the ultrafast work has been done at 1310 nm and translation to 1550 nm is non-trivial as it involves a change in the substrate material to InP. Quantum dots based on InP are not nearly as well developed as InAs quantum dots on GaAs.

The frequency response of quantum dots can be improved using techniques such as p-type modulation doping [13, 14], which is a technique where carrier capture rates are improved by delta-doping the dot region with acceptors to create an excess of holes. Another alternative is cold carrier tunnel injection[15, 16].

Before embarking on the fabrication of complicated quantum dot asymmetric twin waveguide structures, the quantum dots should be studied using simple laser devices and SOAs. Photoluminesence studies of quantum dot growths and electroluminescence studies of fabricated lasers and SOAs should be performed in order to optimize the dot characteristics, similar to the method used to optimize the 1310 nm quantum dots in

Chapter 2. Before integration of the quantum dots into asymmetric twin waveguide structures, the BPM simulations should be repeated, as the active region is likely to look much differently than the bulk InGaAsP structure used in the first- and second-generation optical logic structures. Quantum dot active regions typically have multiple quantum well matrix layers and intermediate spacer layers, so the effective index of the active region could be considerably different. Simulations must be repeated to optimize the spacer layer thickness, cap layer thickness, taper length and other critical parameters to ensure that the ATG structure behaves appropriately and effective evanescent coupling can be achieved. A proposed epitaxial structure might look like that shown in Figure 4-4.

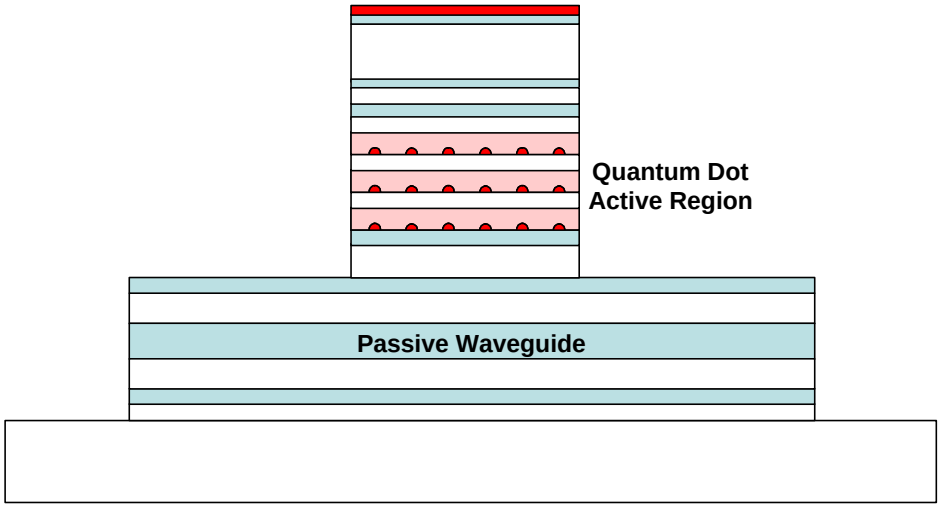


Figure 4-4: Schematic of proposed quantum dot asymmetric twin waveguide semiconductor optical amplifier. Note: not to scale.

4.4 Tunnel Junctions for Vertical Integration

Tunnel junctions allow vertical integration of more than one active region, a concept well-suited to the vertical integration scheme inherent to the asymmetric twin waveguide approach. Combining tunnel junctions with twin waveguides permits the possibility of multiple active regions – perhaps two lasers operating at different wavelengths, integrated optical pumps, photodetectors integrated with lasers or

amplifiers, spot-size converters, or other vertically integrated devices – to be implemented in photonic integrated circuits. Figure 4-5 is a schematic of a device incorporating multiple asymmetric waveguides, with a tunnel junction separating the two tapered layers. However, with the highly-doped tunnel junction epitaxial layers, there is the possibility of free-carrier absorption occurring during the evanescent coupling between waveguides. Placing the tunnel junction at the null of the even and odd modes would minimize the overlap of the highly-doped region with the optical mode and minimize absorption and, hence, loss.

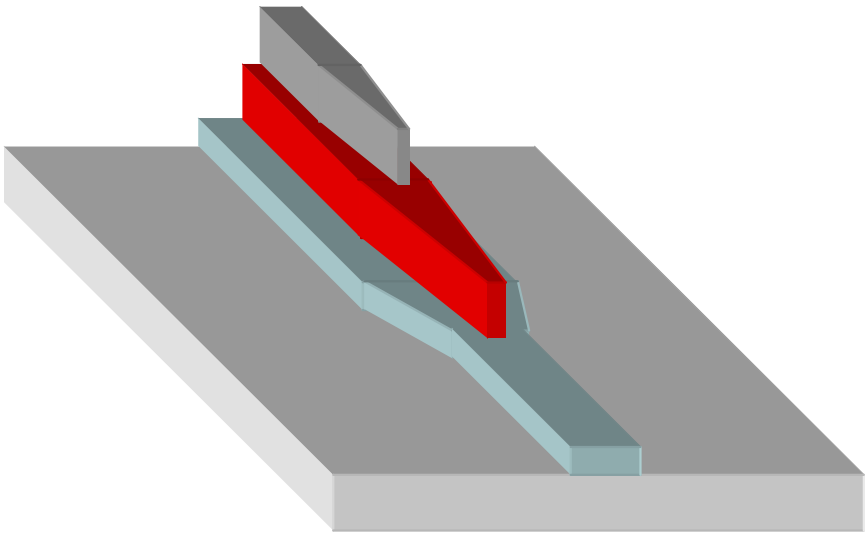


Figure 4-5: Integrating asymmetric twin waveguides with tunnel junctions would allow multiple active regions to be incorporated into multi-tiered photonic integrated circuits.

Breaking the two-dimensional planar design inherent to most traditional photonic integrated circuits allows for the development of increasingly complex designs and more extensive integration. In order to duplicate and exceed the functionality and speed of electronic routers and switches, versatile and flexible platform technologies for photonic integration must be developed. While the inclusion of additional levels would increase the fabrication complexity substantially, the fundamental techniques and approach to fabrication in this thesis could be extended to the optimization of these multi-tiered structures.

4.5 References

1. Zhuang, Q.D., S.F. Yoon, and H.Q. Zheng, *Growth and emission tuning of InAs/InP quantum dots superlattice.* Journal of Crystal Growth, 2001. **227**: p. 1084-1088.
2. Takemoto, K., et al., *Observation of exciton transition in 1.3-1.55 mu m band from single InAs/InP quantum dots in mesa structure.* Japanese Journal of Applied Physics Part 2-Letters & Express Letters, 2004. **43**(3A): p. L349-L351.
3. Ha, W.N., et al., *Long-wavelength GaInNAs(Sb) lasers on GaAs.* IEEE Journal of Quantum Electronics, 2002. **38**(9): p. 1260-1267.
4. Bank, S., et al., *1.5 mu m GaInNAs(Sb) lasers grown on GaAs by MBE.* Journal of Crystal Growth, 2003. **251**(1-4): p. 367-371.
5. Stefanov, B. *Practical Photonic Integration: New Devices, Applications, and Performance*. in *Center for Integrated Photonics (CIPS 2007)*. 2007. Cambridge, MA.
6. Markina, A., *Design and Simulation for the Fabrication of Integrated Semiconductor Optical Logic Gates*, in *Electrical Engineering PhD Thesis*. 2005, MIT.
7. Dagens, B., et al., *Design optimization of all-active Mach-Zehnder wavelength converters.* IEEE Photonics Technology Letters, 1999. **11**(4): p. 424-426.
8. Bilenca, A., et al., *InAs/InP 1550 nm quantum dash semiconductor optical amplifiers.* Electronics Letters, 2002. **38**(22): p. 1350-1351.
9. Akiyama, T., et al., *Pattern-effect-free semiconductor optical amplifier achieved using quantum dots.* Electronics Letters, 2002. **38**(19): p. 1139-1140.
10. Akiyama, T., et al., *Pattern-effect-free amplification and cross-gain modulation achieved by using ultrafast gain nonlinearity in quantum-dot semiconductor optical amplifiers.* Physica Status Solidi B-Basic Research, 2003. **238**(2): p. 301-304.
11. Dommers, S., et al., *Complete ground state gain recovery after ultrashort double pulses in quantum dot based semiconductor optical amplifier.* Applied Physics Letters, 2007. **90**(3).
12. Kim, K., et al., *Gain dynamics and ultrafast spectral hole burning in In(Ga)As self-organized quantum dots.* Applied Physics Letters, 2002. **81**(4): p. 670-672.
13. Otsubo, K., et al., *Temperature-insensitive eye-opening under 10-Gb/s modulation of 1.3-mu m p-doped quantum-dot lasers without current adjustments.* Japanese Journal of Applied Physics Part 2-Letters & Express Letters, 2004. **43**(8B): p. L1124-L1126.
14. Deppe, D.G. and H. Huang, *Fermi's golden rule, nonequilibrium electron capture from the wetting layer, and the modulation response in P-doped quantum-dot lasers.* IEEE Journal of Quantum Electronics, 2006. **42**(3-4): p. 324-330.
15. Bhattacharya, P., et al., *Carrier dynamics and high-speed modulation properties of tunnel injection InGaAs-GaAs quantum-dot lasers.* IEEE Journal of Quantum Electronics, 2003. **39**(8): p. 952-962.
16. Mi, Z., P. Bhattacharya, and S. Fathpour, *High-speed 1.3 mu m tunnel injection quantum-dot lasers.* Applied Physics Letters, 2005. **86**(15).

CHAPTER 5

Appendices

5.1 Oxide Stripe Laser Process

Oxide Deposition

1. Clean samples: Acetone/Methanol/Isopropanol/Dry N_2
2. Deposit 175 nm PECVD oxide (SiO_x)
   380 kHz, 550 mTorr, 300° C platen, 250° shower, 60 W, 137 sec
   N_2O 1420 sccm, N_2 392 sccm, SiH_4 12 sccm
3. Clean samples: Acetone/Methanol/Isopropanol/Dry N_2 to remove particles

Photolithography

4. HMDS Vapor Prime, 30 minute cycle, Recipe 5
5. Spin Resist: AZ5214 – image reversal

Dispense	3 sec	500 rpm
Spread	6 sec	750 rpm
Spin	30 sec	4000 rpm

6. Prebake: 30 min, 90-95°C oven
7. Contact Aligner – Electronics Visions 620 (MASK 2 – narrow stripes)
   Expose 1.5 sec
8. Reversal Bake: 90 sec, 123°C hotplate

9. Flood Exposure
   Expose 60 sec
10. Develop: AZ 422, 90 sec

Oxide Etch

11. Buffered Oxide Etch (BOE)
    BOE:H_2O, 1:7, ~50 sec
12. Strip Resist
    n-methylpyrrolidinone (NMP) (75-100°C, hotplate), swirling, ~5-10 min
13. Clean samples: Acetone/Methanol/Isopropanol/Dry N_2

Photolithography

14. HMDS Vapor Prime, 30 minute cycle, Recipe 5
15. Spin Resist: AZ5214 – image reversal

Dispense	3 sec	500 rpm
Spread	6 sec	750 rpm
Spin	30 sec	4000 rpm

16. Prebake: 30 min, 90-95°C oven
17. Contact Aligner – Electronics Visions 620 (Mask 1 – broad stripes)
    Expose 1.5 sec
18. Reversal Bake: 90 sec, 123°C hotplate
19. Flood Exposure
    Expose 60 sec
20. Develop: AZ 422, 90 sec

Metal Deposition

21. Evaporate Ti/Pt/Au (50/1500/2000Å)
22. Liftoff metal
    NMP (100°C) and acetone rinse – aggressive acetone spray aids in liftoff
23. Clean with Acetone/Methanol/Isopropanol/Dry N_2

Backside Processing

24. Lap wafer backside to ~150 μm thickness
25. Electron beam evaporation
    Ni/Au/Ge/Au/Ni/Au (50/100/500/900/300/2000 Å) on backside
26. Rapid thermal anneal metal contacts 380°C, 30 sec
27. Sputter depositon
    Ti/Pt/Au (300/1000/300 Å) on backside
28. Deposit metal on CuW mount
    Ti/Pt/Au (300/1000/300 Å)
    $Au_{0.1}Sn_{0.9}$ 2 μm
29. Cleave samples to desired length
30. Sputter CuW mounts in Argon to remove oxide
31. Mount samples on CuW
32. Anneal on carbon strip heater under N_2 vacuum to ~217°C

5.2 ATG-SOA Optical Logic Process

Notes:
– Solvent cleans are used frequently to remove particles or clean residue from the wafer surface. The typical sequence is an acetone/methanol/isopropanol rinse followed by drying with nitrogen.
– Photolithography exposure and development times are carefully calibrated using dummy wafers before committing to epitaxial wafers. Lithography processes should be monitored closely to account for variations in bulb intensity and environmental conditions.

Photolithography: The first photolithography step defines the active ridge area, with the exception of the tapers.

1. Dehydration bake: 15-20 min, 95°C oven
2. Spin Resist: AZ5214 – image reversal

Dispense	6 sec	500 rpm
Spread	6 sec	750 rpm
Spin	30 sec	4000 rpm

3. Prebake: 30 min, 90-95°C oven
4. Contact Aligner – Electronics Visions 620 (Mask 0)
   Expose 1.5 sec
5. Reversal Bake: 90 sec, 123°C hotplate
6. Contact Aligner – Flood Exposure:
   Expose 60 sec
7. Develop: AZ 422, 90 sec

Metal Deposition and Liftoff: Ti/Pt is deposited as a base metal to protect the ohmic contact interface through the subsequent processing steps.

8. Electron beam evaporation: Ti/Pt (20 nm/20 nm)
9. Liftoff in hot n-methylpyrrolidinone (NMP) (75-100°C, hotplate), gently swirling.
10. Solvent rinse to remove residual resist.

Oxide Deposition: PECVD oxide is deposited for later use as a hard mask.

11. Deposit 500 nm SiO_2 (HFSIO)
    13.56 MHz, 550 mTorr, 300° C platen, 250° shower, 60 W, 595 sec
    N_2O 1420 sccm, N_2 392 sccm, SiH_4 12 sccm

12. Cleave 2” wafer into quarters, solvent rinse to remove particles.

Photolithography: The second photolithography step defines oxide hard mask for the active ridge and the tapers.

13. Spin Resist: AZ5214 – image reversal

Dispense	3 sec	500 rpm
Spread	6 sec	750 rpm
Spin	30 sec	4000 rpm

14. Prebake: 35 min, 90-95°C oven

15. Contact Aligner – Electronics Visions 620 (Mask 1)
    Expose 8.5 sec
16. Develop: AZ 422, 80-85 sec
17. Flood Exposure:
    Expose 120 sec
18. Postbake: 20 min, 90-95°C oven

Oxide Reactive Ion Etch: Transfers photoresist soft mask to oxide hard mask.

19. Etch oxide in Plasmatherm 790 RIE:
    Clean Chamber: CF_4 4 sccm, O_2 20 sccm, 300 V (NEWCLEAN)
    Descum: He 5 sccm, O_2 10 sccm, 20 mTorr, 150 W
    Oxide etch: CF_4 15 sccm, 10 mTorr, 50V
    5+5+5+3 min = 18 min total @ ~30 nm/min
20. Remove Resist
    Solvent rinse with Acetone/Methanol/Isopropanol/Dry N_2
    Asher: He/O_2, 200 W, 2 min

InP Reactive Ion Etch: Etch active waveguide and tapers in semiconductor.

21. Mount sample on 6" Si carrier wafer with high-vacuum grease
22. Etch InP in inductively-coupled plasma (ICP) RIE (SAMCO RIE 200 IP)
    Cl_2 0.5 sccm, $SiCl_4$ 0.5 sccm, Ar 10 sccm, 250 W bias, 250 W ICP
    Inspect etch depth with profilometer and repeat etch as necessary
    Total etch depth 1.39 μm @ ~130-160 nm/min
23. Remove sample from carrier, clean vacuum grease
    Swab grease with trichloroethylene (TCE)
    Soak in TCE 5-10 min
    Rinse with methanol, isopropanol, dry N_2

Oxide Deposition: PECVD oxide is deposited for later use as a hard mask.

24. Deposit 400 nm SiO_2 (HFSIO)
    13.56 MHz, 550 mTorr, 300° C platen, 250° shower, 60 W, 476 sec
    N_2O 1420 sccm, N_2 392 sccm, SiH_4 12 sccm

Photolithography: The third photolithography step defines oxide hard mask for the passive waveguides.

25. Spin Resist: AZ5214 – positive resist

Dispense	3 sec	500 rpm
Spread	6 sec	750 rpm
Spin	30 sec	4000 rpm

26. Prebake: 35 min, 90-95°C oven
27. Contact Aligner – Electronics Visions 620 (Mask 2)
    Expose 11.5 sec
28. Develop: AZ 422, 90 sec
29. Flood Exposure:
    Expose 60 sec
30. Postbake: 20 min, 90-95°C oven

Oxide Reactive Ion Etch: Transfers photoresist soft mask to oxide hard mask.

32. Etch oxide in Plasmatherm 790 RIE:
    Clean Chamber: CF_4 4 sccm, O_2 20 sccm, 300 V (NEWCLEAN)
    Descum: He 5 sccm, O_2 10 sccm, 20 mTorr, 150 W
    Oxide etch: CF_4 15 sccm, 10 mTorr, 50V
    5+5+5+4 min = 19 min total @ ~30 nm/min
33. Remove Resist
    Rinse with Acetone/Methanol/Isopropanol/Dry N_2
    Asher: He/O_2, 200 W, 2 min

InP Reactive Ion Etch: Etch passive waveguide in semiconductor.
34. Mount sample on 6" Si carrier wafer with high-vacuum grease
35. Etch InP in inductively-coupled plasma (ICP) RIE (SAMCO RIE 200 IP)
    Cl_2 0.5 sccm, $SiCl_4$ 0.5 sccm, Ar 10 sccm, 250 W bias, 250 W ICP
    ~130-160 nm/min
    Inspect etch depth with profilometer and repeat etch as necessary
    Total etch depth 1.05 μm @ ~130-160 nm/min
36. Remove sample from carrier, clean vacuum grease
    Swab grease with trichloroethylene (TCE)
    Soak in TCE 5-10 min
    Rinse with methanol, isopropanol, dry N_2

37. Remove hard masks: BOE 2 min

Planarization:
38. Solvent Clean, 130°C Oven dehydration bake
39. Adhesion Layer
    AP3000 Static Dispense, 300 rpm (5 sec), 2-3k rpm (20 sec)
40. Hotplate Bake 100°C, 5 min
41. Planarization layer: Benzocyclobutene (BCB)
    Static Dispense, 500-750 rpm (5 sec), 3k rpm (25 sec) ~ 1.3 um thickness
42. Hotplate Bake 100°C, 1 min
43. BCB Curing: Tube furnace
    Load wafer, flow N2 (>20 scfh) for 30 min
    Slowly ramp 250°C, set N_2 flow to ~ 5-15 scfh
    60 min at 250°C, ramp down to room temperature

Etchback: Reveal top of active ridge by etching back BCB
44. Etch BCB in Plasmatherm 790 RIE:
    Clean Chamber: CF_4 4 sccm, O_2 20 sccm, 300 V (NEWCLEAN)
    Etch BCB: CF_4 12 sccm, O_2 8 sccm, 15 mTorr, 100 V
    Inspect BCB on ridge with microscope and repeat etch as necessary
    5+2:30+3+2:30+2:30+2:30=18 min @ ~90-100 nm/min

Photolithography: The fourth and last photolithography step defines the metal contact pads for liftoff.

45. Spin Resist: AZ5214 – image reversal

Dispense	3 sec	500 rpm
Spread	6 sec	750 rpm

Spin 30 sec 4000 rpm

46. Prebake: 30 min, 90-95°C oven
47. Contact Aligner – Electronics Visions 620 (Mask 3)
    Expose 1.5 sec
48. Reversal Bake: 90 sec, 123°C hotplate
49. Contact Aligner – Flood Exposure:
    Expose 60 sec
50. Develop: AZ 422, 90 sec

Metal Deposition and Liftoff: Ti/Pt/Au is deposited for ohmic contacts.

51. Electron beam evaporation
    Ti/Pt/Au (300/200/2000 Å)
52. Liftoff in hot n-methylpyrrolidinone (NMP) (75-100°C, hotplate), gently swirling.
53. Solvent rinse to remove residual resist.

Backside Processing

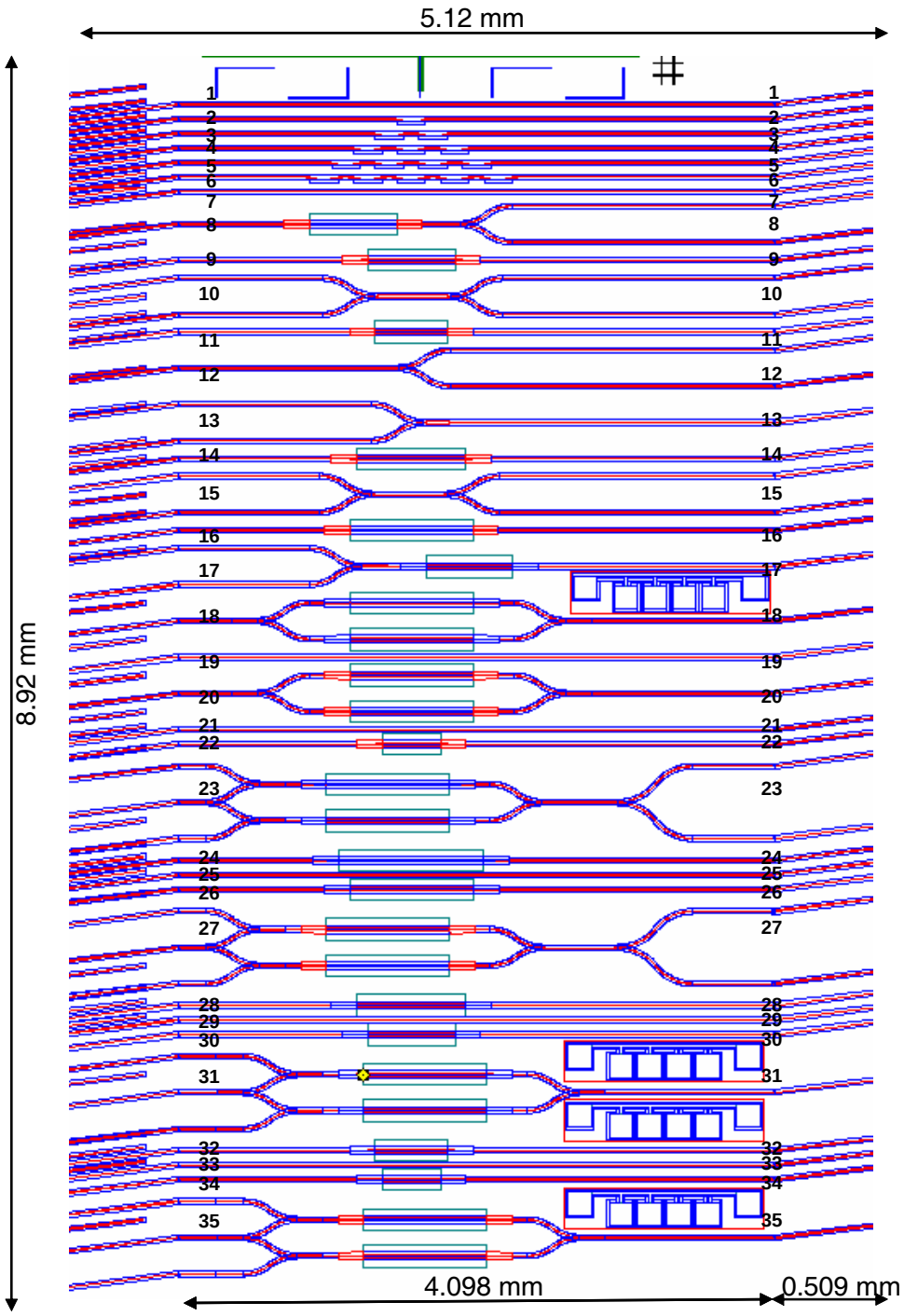
54. Lap wafer backside
    Mount sample on glass telescope blank using Loc-Wax
    Scrape excess wax, rinse with TCE, isopropanol
    Lap with 5 μm grit to ~175 μm thickness
    Rinse sample thoroughly with H_2O
55. Polish wafer backside
    1% Br in methanol
56. Electron beam evaporation bacside contact in Temescal FCE-2500
    Ge/Au/Ni/Au (300/600/300/2000 Å)
57. Dismount sample from glass by heating or dissolving in TCE
58. Clean wax with TCE, isopropanol
59. Rapid thermal annealing: Heatpulse 210
    450°C, 30 sec
60. Deposit metal in Denton Sputterer Discovery 18
    Ti/Pt/Au (500/700/500 Å)
61. Cleave samples on Loomis LSD-100
62. Prepare Cu mounts
    Ti/Pt/Au (500/700/500 Å)
63. Mount die on Cu mount
64. Anneal on carbon strip heater under N_2 vacuum to ~157°C

5.3 Epitaxial Structure of Optical Logic Wafers

Layer #	Material	x	y	PL (nm)	Thickness (μm)	Doping	Dopant
18	GaIn(x)As(y)P	0.56	0.94	1550±50	0.05	$>2x10^{18}$	Zn
17	GaIn(x)As(y)P	0.80	0.45	1180±50	0.03	$>1x10^{18}$	Zn
16	InP				0.60	$2.5\text{-}10x10^{17}$	Zn
15	GaIn(x)As(y)P	0.80	0.45	1180±50	0.01	$2.5x10^{17}$	Zn
14	InP				0.05	$2.5x10^{17}$	Zn
13	InP				0.05	—	—
12	GaIn(x)As(y)P	0.80	0.45	1180±50	0.10	—	—
11	GaIn(x)As(y)P	0.56	0.94	1550±50	0.20	—	—
10	GaIn(x)As(y)P	0.80	0.45	1180±50	0.10	—	—
9	InP				0.05	—	—
8	InP				0.15	$5x10^{17}$	S
7	GaIn(x)As(y)P	0.80	0.45	1180±50	0.10	$5x10^{17}$	S
6	InP				0.20	$5x10^{17}$	S
5	GaIn(x)As(y)P	0.80	0.45	1180±50	0.25	$5x10^{17}$	S
4	InP				0.20	$5x10^{17}$	S
3	GaIn(x)As(y)P	0.80	0.45	1180±50	0.10	$5x10^{17}$	S
2	InP				0.20	$5x10^{17}$	S
1	InP				0.30	$3\text{-}0.5x10^{17}$	S

Note: Wafers purchased from IQE.

5.4 Detailed Schematic of Second Generation Optical Logic Die



Optical Logic Devices

Device #	Description	SOA Length (μm)	SOA Width (μm)
1	Straight Waveguide	—	—
2	Waveguide 2 bends	—	—
3	Waveguide 4 bends	—	—
4	Waveguide 6 bends	—	—
5	Waveguide 8 bends	—	—
6	Waveguide 10 bends	—	—
7	Straight Waveguide	—	—
8	SOA with 1x2 MMI	600	4
9	Straight SOA	600	4
10	2x2 MMI	—	—
11	Straight SOA	500	4
12	1x2 MMI	—	—
13	2x1 MMI	—	—
14	Straight SOA	750	4
15	2x2 MMI	—	—
16	Straight SOA	850	4
17	SOA with 1x2 MMI	600	2

18	Simple MZI	850	2
19	Straight Waveguide	—	—
20	Simple MZI	850	4
21	Straight Waveguide	—	—
22	Straight SOA	400	4
23	Optical Logic Unit Cell	850	2
24	Straight SOA	1000	2
25	Straight Waveguide	—	—
26	Straight SOA	850	2
27	Optical Logic Unit Cell	850	4
28	Straight SOA	750	2
29	Straight Waveguide	—	—
30	Straight SOA	600	2
31	Wavelength Converter	850	2
32	Straight SOA	500	2
33	Straight Waveguide	—	—
34	Straight SOA	400	2
35	Wavelength Converter	850	4

5.5 Photoresist Evaluation Experiments

* AZ5214 resist was used throughout as either a positive (+) resist or an image-reversal (-) resist

** Resist was evaluated on various PECVD dielectric surfaces (STS Multiplex PECVD).
LFSIO: low-frequency 380 kHz SiO_2
HFSIO: high-frequency 13.56 MHz SiO_2
LFSIN: low-frequency 380 kHz Si_3N_4
HFSIN: high-frequency 13.56 MHz Si_3N_4

*** Photolithography procedures were rated on a scale of 1-5 (worst-best) based on scanning electron microscopy evaluation of the photolithography characteristics.

Sample	Resist Tone *	Surface **	t_{expose} (sec)	Developer	t_{devel} (sec)	Prebake	Rating ***
Experiment A: Determine proper exposure time for AZ5214 as a positive							
PR1A	+	—	1.5	AZ422	90	95°C oven 30 min	1
PR1C	+	—	10	AZ422	75	95°C oven 30 min	3
PR1D	+	—	10	AZ300	75	95°C oven 30 min	3
Result: ~10 sec is proper exposure time. Believed to correspond to ~100 mJ/cm^2							
Experiment B: Evaluate AZ5214 (+) with an oxide layer							
PR2A	+	400 nm LFSIO	10	AZ422	45	95°C oven 30 min	4
PR2C	+	400 nm LFSIO	12	AZ422	90	95°C oven 30 min	3
PR2D	+	400 nm LFSIO	10	AZ422	120	95°C oven 30 min	2
Result: ~10 sec is proper exposure time. Develop time changes. Vacuum contact mode better than hard contact.							
Experiment C: Determine proper spacing of mask/wafer. Determine develop time.							
PR3A	+	150 nm LFSIO	10	AZ422	130	95°C oven 30 min	2
PR3B	+	150 nm LFSIO	10	AZ422	45	95°C oven 30 min	4
PR3C	+	150 nm LFSIO	10	AZ422	45	95°C oven 30 min	4
PR3D	+	150 nm LFSIO	10	AZ422	105	95°C oven 30 min	2
Result: Fresh developer more consistent than old developer.							

Experiment D: Evaluate AZ300 as a developer.							
PR4A	+	150 nm LFSIO	10	AZ300	30	95°C oven 30 min	2
PR4B	+	150 nm LFSIO	10	AZ300:H_2O 1:1	90	95°C oven 30 min	1
PR4C	+	150 nm LFSIO	10	AZ300	20	95°C oven 30 min	2
PR4D	+	150 nm LFSIO	10	AZ300	15	95°C oven 30 min	3
Result: AZ300 too fast and aggressive as a developer. Diluted 1:1 doesn't develop.							
Experiment E: Evaluate vacuum + hard (v+h) contact mode, extended prebake time.							
PR5A	+	150 nm LFSIO	10	AZ422	115	95°C oven 35 min	4
PR5B	+	150 nm LFSIO	10	AZ422	120	95°C oven 35 min	4
Result: 35 min bake extends develop time and allows more precise control. v+h mode better than vacuum contact mode or hard contact mode.							
Experiment F: Check develop time.							
PR7A	+	150 nm LFSIO	10	AZ422	105	95°C oven 35 min	4
PR7B	+	150 nm LFSIO	10	AZ422	100	95°C oven 35 min	4
PR7C	+	150 nm LFSIO	10	AZ422	95	95°C oven 35 min	5
PR7C	+	150 nm LFSIO	10	AZ422	95	95°C oven 35 min	5
Result: Develop time closer to 90-95 sec.							
Experiment G: Evaluate 30 min 120°C postbake							
PR8A	+	150 nm LFSIO	10	AZ422	90	95°C oven 35 min	4
PR8B	+	150 nm LFSIO	10	AZ422	87	95°C oven 35 min	4
PR8C	+	150 nm LFSIO	10	AZ422	81	95°C oven 35 min	5
PR8D	+	150 nm LFSIO	10	AZ422	80	95°C oven 35 min	5
Result: Inconclusive.							

Experiment H: Evalute process for nitride layer.							
PR6A	+	150 nm LFSIN	10	AZ422	80	95°C oven 35 min	2
PR6B	+	150 nm LFSIN	10	AZ422	75	95°C oven 35 min	2
PR6C	+	150 nm LFSIN	10	AZ422	55	95°C oven 35 min	3
PR6D	+	150 nm LFSIN	10	AZ422	50	95°C oven 35 min	4
Result: Develop time for nitride is ~50-55 sec. $t_{nitride} < t_{oxide} < t_{bare}$							
Experiment I: Evaluate hotplate postbake 95°C 95 sec							
PR8A2	+	150 nm LFSIO	12	AZ422	80	95°C oven 35 min	3
PR8B2	+	150 nm LFSIO	12	AZ422	70	95°C oven 35 min	4
PR8C2	+	150 nm LFSIN	12	AZ422	50	95°C oven 35 min	3
PR8D2	+	150 nm LFSIN	12	AZ422	56	95°C oven 35 min	5
Result: Hotplate postbake gives more vertical sidewalls							
Experiment J: Evaluate post-develop flood exposure 60 sec							
PR9A	+	150 nm HFSIO	8.5	AZ422	70	95°C oven 35 min	3
PR9B	+	150 nm HFSIO	8.5	AZ422	65	95°C oven 35 min	4
Result: Post-exposure flood improves sidewall roughness in subsequent oxide RIE.							
Experiment K: Re-evaluate exposure and develop times after Hg bulb change for AZ5214 positive process.							
PR10B	+	150 nm HFSIN	8	AZ422	85	95°C oven 35 min	4
PR10C	+	150 nm HFSIN	10	AZ422	90	95°C oven 35 min	5
PR12C	+	500 nm HFSIO	10	AZ422	85	95°C oven 35 min	5
PR12D	+	400 nm HFSIO	9.5	AZ422	80	95°C oven 35 min	5
Result: New exposure and develop times determined.							

Experiment L: Re-evaluate exposure and develop times after Hg bulb change for AZ5214 image-reversal process.							
PR13A	-	—	1.5	AZ422	115	95°C oven 35 min	2
PR13B	-	—	1.2	AZ422	90	95°C oven 35 min	4
PR13C	-	—	1.2	AZ422	90	95°C oven 35 min	4
PR13D	-	—	0.6	AZ422	120	95°C oven 35 min	2
Result: Develop time for nitride is ~50-55 sec. $t_{nitride} < t_{oxide} < t_{bare}$							

5.6 Reactive Ion Etching of Oxide Hard Mask Experiments

* Etch quality was rated on a scale of 1-5 (worst-best) based on scanning electron microscopy evaluation of the etch characteristics after etch in Plasmatherm 790 RIE.

Sample	Material	Gas	Flow (sccm)	Pressure (mTorr)	Voltage (V)	Time (min)	He/O_2 DESCUM (sec)	Rating*
Experiment A: Evaluate DESCUM								
PR5A	SiO_2	—	—	—	—	—	10	5
Result: He/O_2 DESCUM slightly smoothes resist sidewalls after development.								
Experiment B: Determine CHF_3 etch rate								
PR3C	SiO_2	CHF_3	15	10	100	1:00	10	2
PR4B	SiO_2	CHF_3	15	10	100	2:00	10	2
PR4C	SiO_2	CHF_3	15	10	100	4:00	10	2
PR4D	SiO_2	CHF_3	15	10	100	5:00	10	2
Result: CHF_3 etch rate determined 32-35 nm/min, resist 12-17 nm/min.								
Experiment C: Determine CHF_3 etch rate								
PR7C	bare	CF_4	15	10	100	3:00	11	3
PR6A	Si_3N_4	CHF_3	15	10	100	4:00	11	2
Result: CHF_3 forms crust on resist. CF_4 slowly etches Si (~11 nm/min)								
Experiment D: Evaluate effect of adding O_2 and raising voltage								
PR6B	Si_3N_4	CHF_3 O_2	15 1.5	10	300	4:00	10	1
PR7D1	bare	CHF_3 O_2	15 1.5	10	300	4:00	10	1
PR7D2	bare	CHF_3 O_2	15 1.5	10	300	4:00	10	1
Result: Raising V and adding O_2 aggressively attacks and deforms resist.								
Experiment E: Evaluate CF_4 and low voltage								
PR8B	SiO_2	CF_4	15	10	100	5:00	—	4
PR8D	SiO_2	CF_4	15	10	50	5:00	—	5
Result: Very good. CF_4 does not deform resist or form crust. Low V better. Etch rate nearly the same ~30 nm/min								
Experiment F: Evaluate CF_4 with a DESCUM								
PR8C1	SiO_2	CF_4	15	10	50	5:00	10	5
PR8C1	SiO_2	CF_4	15	10	50	5:00	—	5
Result: DESCUM makes slight improvement. Hotplate bake better.								

Sample	Material	Gas	Flow (sccm)	Pressure (mTorr)	Voltage (V)	Time (min)	He/O_2 DESCUM (sec)	Rating
Experiment G: Evaluate on/off etch to reduce substrate heating								
PR6C	SiO_2	CF_4	15	10	50	5:00 On/Off	—	5
PR7A	SiO_2	CF_4	15	10	50	5:00 On/Off	—	5
Result: On/Off etch (1+1+1+1+1 min) does not improve etch.								
Experiment H: Evaluate effect of adding O_2 and raising voltage								
PR9A	SiO_2	CF_4	15	10	50	5:00	45	5
PR9B	SiO_2	CF_4	15	10	50	5:00	45	5
Result: Long DESCUM works well. Post-develop flood/hotplate works well								
Experiment I: Evaluate effect of adding O_2 and raising voltage								
12A1	SiO_2	CF_4	15	10	50	5:00	10	5
12A2	SiO_2	CF_4	15	10	50	5:00	10	5
Result: High-frequency SiO_2 (13.56 MHz) etches better than low-frequency (380 kHz)								