Frequency Translation Method for Low Frequency Variable Gain Amplification and Filtering

by

Mabel Y. Feng

Submitted to the Department of Electrical Engineering and Computer Science

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Abstract

This thesis discusses an innovative solution to an industry challenge. A frequency translation method is designed to shift low frequency signals to intermediate frequencies in order to utilize higher-frequency components. This solution, appropriate for applications involving 1-10MHz signals, can provide continuously variable gain and filtering at little cost in dynamic performance. The working system converts the low frequency signals up to the 70MHz band to achieve up to 28dB attenuation and 60-86MHz variable filtering. A Single Side Band system has a Signal-to-Noise Ratio (SNR) of 71dB with a 73dB SNR Analog-to-Digital Converter (ADC), 44 dB Output Third-Order Intercept Point (OIP3), and a Noise Figure (NF) of 14dB. Ultrasound and other applications in the 1-10MHz range benefit greatly from this upconversion scheme.

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I would also like to thank my family for their support, my friends for their encouragement as I worked through school and at Linear Technology. The lessons I have learned here in the six months in preparing, experimenting, and writing my thesis will go a long way in my life.

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Chapter 1

Introduction

1.1 Problem Statement

Ultrasound, sonar, and medical imaging rely on a method of receiving dispatched signals and properly processing them for image conversion. High-end ultrasound applications require a high dynamic range system for minimal interference and distortion. This would give the higher resolution imaging necessary in high-end image processing. One challenge in ultrasound has been how to implement a truly continuously adjustable gain control in a system with low distortion at the operational frequencies. Designing such a system can be a challenging feat and is not an easily solvable problem for engineers. Hence, if a solution that is simple to both implement and understand can be developed for this industry challenge, then there are many uses for the application. The following section expands the ultrasound background so that the reader may fully understand the scope of the problem at hand.

1.2 Background

1.2.1 Ultrasound

Much of medical imaging is made possible by ultrasound. The images are obtained by emitting an energy beam throughout the body or mass and reconstructing the

reflected energies into an image with analog to digital processing. This is similar to how radar and sonar sweep across an area and study the echoes back at the source. A transducer probe receives the reflected signal energies at different times across the surface structure, allowing the image to be reconstructed based on a signal attenuation versus time relation. Higher frequencies provide higher resolution images but attenuate faster as the signal travels through the body. The image energies are transmitted at frequencies optimized for signal strength and resolution, so ultrasound frequencies typically range from 2-7 MHz [35].

As an energy beam travels through a mass medium such as the human body, the signal strength decreases due to interfering media and noise. The reflected signal is more attenuated if it has traveled a longer distance in the body and through electronic cables. The beam signals can be subsequently amplified before digital conversion. Hence ultrasound systems require at least gain and attenuation control as well as a means of reducing noise degradation.

Current ultrasound applications incorporate time gain compensation (TGC) amplifiers to maintain a strong (and consistent) energy level as the signals are picked up by the transducer. A standard time-independent amplifier provides the same dB gain to every reflected signal, no matter how far away the signal. Hence, the reflected echoes are still of different magnitudes [Figure 1-1(a)]. With a TGC, the gain increases over time to maintain a constant level of signal attenuation in reflected pulses [Figure 1-1(b)].

What has been described so far is the analog domain of ultrasound. There is, however, the digital processing side that converts the analog echoes to digital signals for digital image processing. At the analog-to-digital converter (ADC) interface, high performance systems require low distortion and noise at the input to the ADC before digital processing. It is important to ensure also that the ADC quantization noise is not a significant factor to the overall noise; it sets the bit resolution. Also, interfering signals about the main desired signal (fundamental) can be prominent distortion sources in ultrasound. If the system has poor intermodulation distortion, the ADC will take the additional spurs as signals in the system and the reconstructed

signal will be heavily distorted. Using high dynamic range and high resolution ADCs like Linear Technology's LTC2249 allows designers to meet the high standards of ultrasound imaging.The system block diagram is shown below in Figure 1-2.

In the analog domain dynamic performance can be limited by ADCs and TGC amplifiers. It was established that the ADCs can meet the specifications for high performance so we take a look at the types of TGC or varying gain amplifiers to devise a high-end solution.

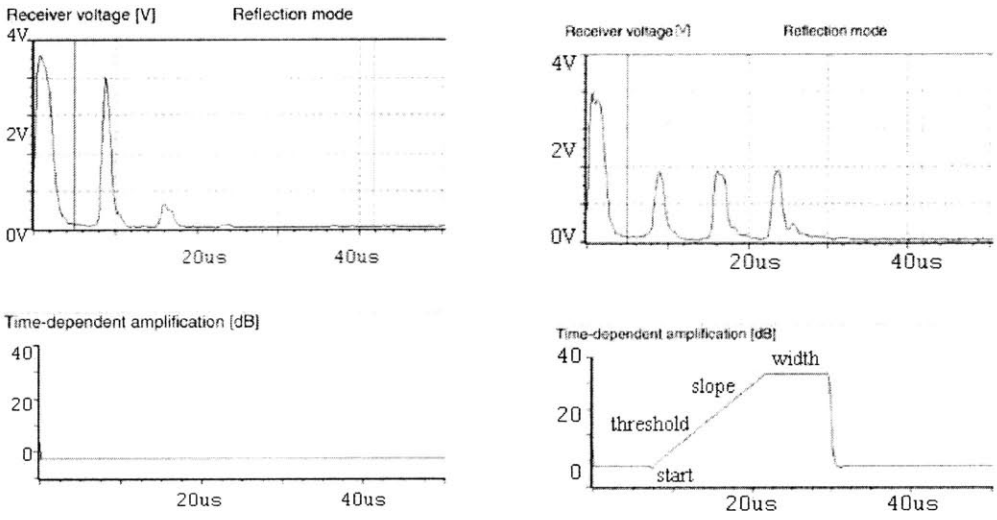


Figure 1-1: Ultrasound Time Gain Compensation. (a) Constant Gain Amplification. (b) TIme Varying Gain Amplification. [36]

1.2.2 The Frequency Spectrum

The challenge at hand is to find variable gain devices that are usable at specific parts on the frequency spectrum. Consider the entire frequency spectrum, from DC up to GHz (radio frequency RF or ultra high frequency). On the low frequency end (DC to 1 MHz), there are several options available for designers. There are discrete programmable step gain amplifiers but for ultrasound, continually adjustable gain amplifiers are more suitable. Instead of adjusting gain in the analog domain, it is also possible to first digitize the low frequency signal with an oversampling ADC and then digitally adjust the gain. Once we progress into the MHz range, we are offered the choice of using Analog Devices' patented XAmp continuous VGAs [23].

However, most adjustable gain amplifiers do not provide the same performance at low frequencies as in higher bandwidths (less than 100MHz).

At intermediate frequencies (IF) and above, continuous variable gain can be realized using PIN (p-intrinsicSi-n structure) diodes. This is a common component found in radio receiver and transmitter paths. PIN diodes are limited on the lower frequency side by two things : physical size and carrier lifetime. A more thorough background on PIN diodes is given in Section 2.4.

In addition to continuous variable gain capabilities, it is important to filter out interfering signals for the best signal processing. High frequency and RF use surface acoustic wave (SAW) filters for their steep filter response, but they are also limited on the low frequency end by size. As in the PIN diodes, a more thorough background on SAW filters is given in Section 2.3. Lower frequency applications would just implement high order filters to achieve as ideal of a filter response as possible. A quality filter in the signal path improves the dynamic performance of the system by preventing out of band noise from getting to the ADC.

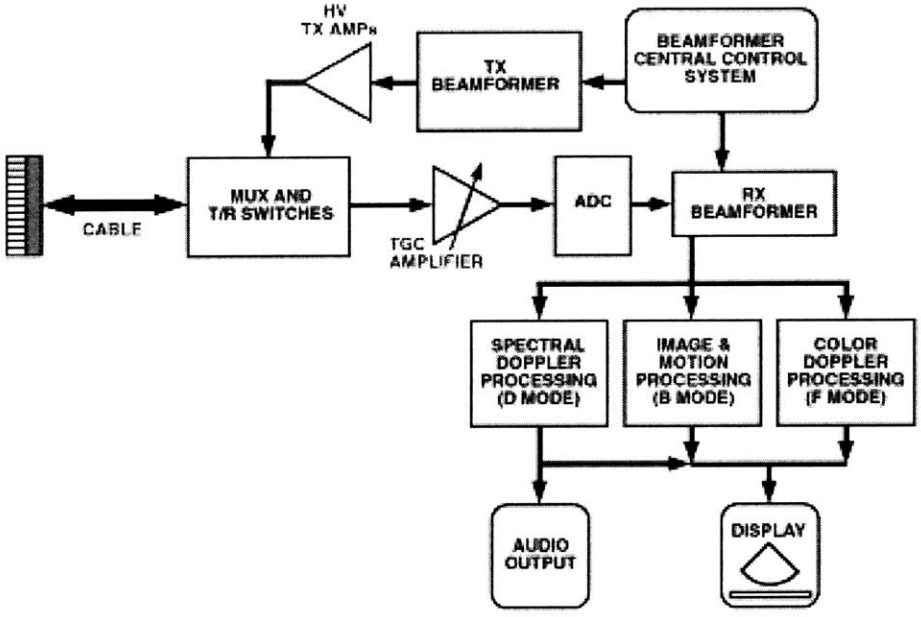


Figure 1-2: Ultrasound System Block Diagram. From [35]

1.3 Proposed Method

The background in the prior section discusses some of the challenges and limitations in low frequency applications. By using frequency translation, one can essentially move the problem to higher frequencies to take advantage of high frequency components. This method can provide continuously variable gain and filtering for ultrasound. The challenge then is to be able to design a system that offers good dynamic performance, on par or better than what low frequency processing can achieve. The thesis explains this method of frequency translation and develops a solution that meets the standards in the ultrasound industry.

1.4 Organization

The thesis is organized as follows: Chapter 2 describes the various components that will be used in the system and also defines the performance figures used. Chapters 3 and 4 discuss design solutions and modifications made to the system. Chapter 5 leads a discussion of the results and how they compare to theoretical expectations of the entire system. Chapter 6 gives a conclusive summary of the merits and drawbacks of this application and suggests future work.

Chapter 2

Building Blocks and Measuring Stick

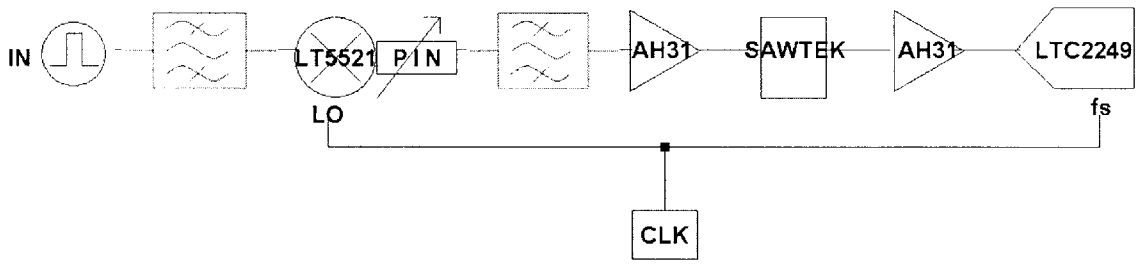


Figure 2-1: Frequency Translation Method General Block Diagram.

The general block diagram of the system is shown in Figure 2-1. This chapter provides background information for the building blocks of the system.

2.1 Frequency Translation

Frequency translation is the process of shifting a signal from one frequency to another, without loss of information in the signal. This is useful in any application that does not care at what frequency the information is transmitted (i.e. the carrier frequency contains no information). In modern communications, frequency translation is used in receivers to downconvert RF to a lower frequency and used in transmitters to upconvert baseband signals to RF.

Modulation is a standard example of frequency translation at work. Essentially, there is information summarized by the function $f(t) = A\cos(\omega_i t)$, and we want to transmit it at a frequency $f_c(t)$. The modulated signal $f_m(t)$ is now of the form $f_m(t) = \cos([\omega_i - \omega_c]t) + \cos([\omega_i + \omega_c]t)$, and is the frequency translated version of the original $f(t)$ signal. The information is preserved because modulation scales the amplitude of the signal but does not distort it. In downconversion, $f_c < f_i$ and in upconversion, $f_c > f_i$.

2.2 Undersampling

In sampling schemes, the choice of sampling frequency determines the quality of the sampled output signal. It makes sense that more samples taken over a period would ensure a better reconstruction of the signal. And, if the signal is not sampled at a fast enough rate, then the conversion will not produce an output that resembles anything like the input. The criterion for proper sampling is the Nyquist theorem (Equation 2.1). The input signal frequency f and the ADC sampling frequency f_s need to satisfy the Nyquist theorem to ensure that no information is lost in sampling:

$$\omega_s \geq 2\omega, \ \textit{where } \omega = 2\pi f \textit{ and } \omega_s = 2\pi f_s. \tag{2.1}$$

One of the ways to sample signals for analog-to-digital conversion is undersampling. For undersampling, we are concerned more about the input bandwidth rather than the input frequency. Here, the Nyquist theorem is concerned with the comparison between the sampling frequency and the input bandwidth.

It is important to note here the distinction between input signal bandwidth and input signal frequency. In an upconversion scheme, the input of interest has a bandwidth of the low frequency about the local oscillator frequency (i.e. 10MHz about LO=70MHz). The input signal frequency goes up to 80MHz but its bandwidth is 10MHz. Because the input does not have information from DC up to 80MHz, it is appropriate to consider only the 10MHz input bandwidth in Nyquist. Input bandwidths less than the Nyquist frequency ($\frac{f_s}{2}$) are fully recovered. Input bandwidths

greater than the Nyquist frequency will fold back into the baseband (DC to $\frac{f_s}{2}$) region. Therefore, if the input signal bandwidth is limited to one Nyquist zone at any location on the frequency spectrum, foldback of the signal will not cause the signal to fold on top of itself.

If the Nyquist criterion is not met, the ADC can produce an aliased component within the signal bandwidth. This aliased component is an undesired signal that needs to be pushed outside of the signal bandwidth. Figure 2-2 shows the frequency effects of aliasing.

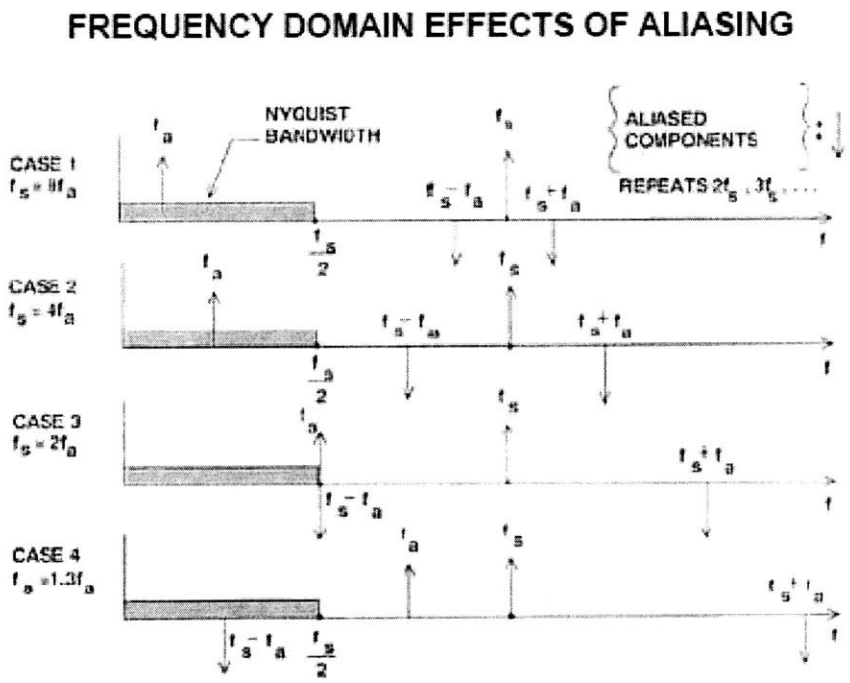


Figure 2-2: Sampling Analog Input Signal f_a at Sampling Rate f_s. For different f_s, the effects of aliasing can be seen in Case 3 when the Nyquist criterion is not met, because the aliased component $(f_s - f_a)$ is at the Nyquist frequency $\frac{f_s}{2}$. From [37].

Undersampled systems allow direct sampling at the IF frequencies as opposed to downconverting the IF signal down to baseband before sampling. Existence of high performance and high sampling rate ADCs (130MSPS or more) allow pre-receiver design to be simplified in cost and design.

Although undersampled systems eliminate the need to sample at the base rate, they tend to exhibit bad noise figures. Due to harmonic folding, every input frequency

harmonic is folded back into the Nyquist zone, which degrades noise performance. Typically, noise performance increases when bandwidth decreases. Another factor that degrades noise is flicker ($1/f$) noise that is introduced with direct-IF sampling receivers. Instead, efforts to improve linearity have to be made, to mitigate the degraded noise performance.

2.3 SAW Filters

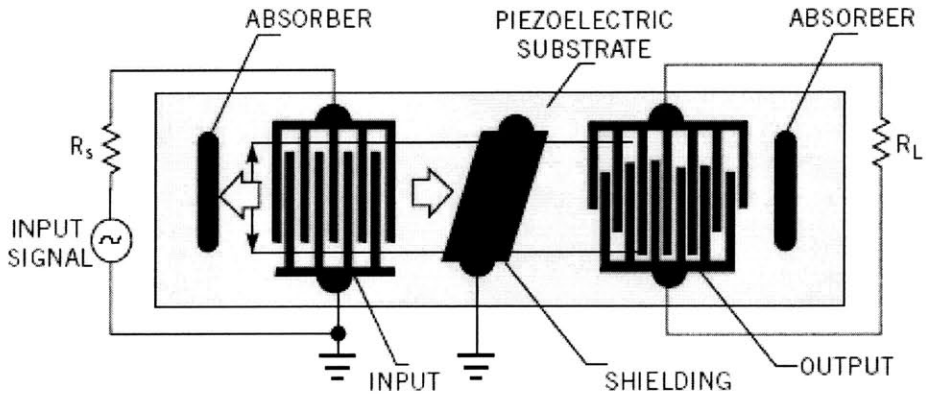


Figure 2-3: Physical Construction of a Typical Surface-Acoustic-Wave (SAW) Filter. [16]

In a surface acoustic wave filter, a mechanical wave travels along the surface of a material with elasticity, and has a decaying amplitude correlated with the depth of the surface [Figure 2-3]. SAW filters use piezoelectric crystals to convert electrical signals to mechanical waves, seen as vibrations. The wave is then delayed as it propagates across the crystal before being converted back to an electric wave. Only waves vibrating at certain (passband) frequencies are converted back into electric waves. SAW filters are ubiquitous in the communications market because they provide significant advantages in not just performance but also cost and size over other types of filters.

SAW filters provide much sharper frequency roll-off than other filters [Figure 2-4]. For example, to achieve the same order response, a passive LC (inductive-capacitive) filter needs to be very high order (possibly 7th-9th order). With their steep stopband

attenuation, the SAW filters are excellent at removing nearby interference, easing the dynamic range parameters of the ADC. This is especially important here because ultrasound signals are often subject to a lot of noise and interference, as discussed before.

In wave propogation, there is an intrinsic delay. If the signal is too low in frequency, the period of the signal becomes greater than this propogation delay, making SAW filters inappropriate for low frequency applications. For higher frequencies, there is a smaller delay so the size of the filters can be physically smaller. Hence SAW filters are better suited for higher frequency applications.

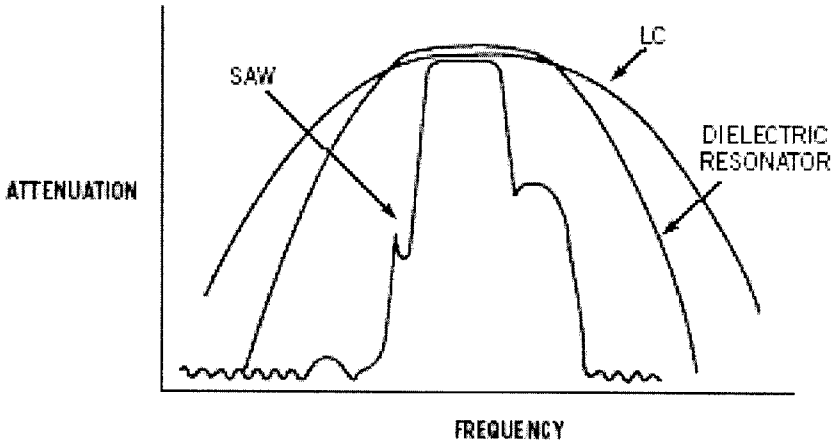


Figure 2-4: Comparison of Different Types of Filters.
SAW filters, seen here provide the sharpest rolloff. [16]

Although SAW filters provide impressive stopband response, they do have a higher insertion loss than passive LC filters. A following low-distortion amplifier can compensate for the gain loss.

The SAW filters used are from SAWTEK : f_c at 70MHz with both 5MHz and 20MHz bandwidths. The insertion loss was 7.25dB and 14.5dB respectively and the group delay variation was 80ns and 65ns respectively [7], [8].

2.4 PIN Diodes

P-Intrinsic-N diodes are often used in high frequency attenuator circuits. These devices are relatively simple devices yet they are excellent for providing continuously adjustable gain with little distortion, cost, and almost ideal linear resistive behavior. Many RF engineers are satisfied with the harmonic distortion and intermodulation distortion performances of available PIN diodes [33]. In addition, the wide range of gain can be achieved at very little DC excitation, which is suitable for low-power applications [28]. To understand the operation of the PIN diode, it is best to start with the well-known 'standard' PN diode and develop the model of the PIN diode from there.

A standard diode has an abrupt PN junction, with the well known I-V characteristic curve and equation $I = I_s(e^{\frac{qV}{kT}} - 1)$, where I_s is the saturation current, q is the charge of an electron, k is Boltzmann's constant, and T is the temperature, in Kelvin. It has a small signal dynamic resistance $r_d = \frac{kT}{qI}$ in forward bias ($V > 0$). We focus only on the forward bias of the diode here.

In the PIN diode, the lightly doped intrinsic region (of width W) inbetween the heavily doped P and N regions affects charge storage and resistive behavior of the device. The resistance of the PIN diode is controlled by a DC current bias I_d. When the PIN diode is forward biased, minority charge carriers are injected into the intrinsic layer (from both P and N doping regions). Therefore, there is charge in the intrinsic layer, which is the basis for the operation of the PIN diode. At frequencies greater than the inverse of the carrier lifetime τ, the intrinsic region charge $Q = I_d\tau$ dominates the resistance of the PIN diode. The carrier lifetime can be thought of as the average time that an injected (minority) carrier survives in the lightly doped intrinsic-region (until recombination in the intrinsic-region or the carrier has traveled a mean distance W to the other heavily doped region).

A simple model of the PIN diode is shown in Figure 2-5(a). The PIN diode has two junctions (P-I and I-N), each modeled as an ideal standard diode. The intrinsic region behaves as variable resistor R_{rf}, controlled by the current bias. The small

signal model of the PIN diode is in Figure 2-5(b). r_d is the small signal resistance found earlier from the I-V curve, and C_d is the capacitance of the junction.

The resistance R_{rf} can be derived using device geometry (W/L_D) and Einstein's relation $(qD = \mu kT)$ and its expression is given by:

$$R_{rf} = (W/L_D)^2 V_{th}/(2I_d) = \frac{W^2}{2\mu I_d \tau_{eff}}, \tag{2.2}$$

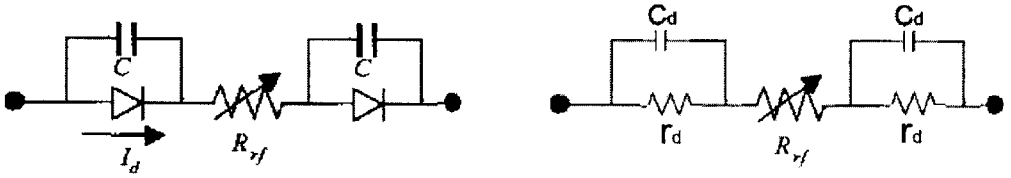
where $V_{th} = kT/q$, μ = mobility, I_d = DC forward current, τ_{eff} = effective carrier lifetime, W = width of intrinsic region, and $L_D = (D\tau_{eff})^{1/2}$, the diffusion length and the ratio $(W/L_D) < 1$. The D in Einstein's relation refers to the ambipolar diffusion constant, $D = 2D_nD_p/(D_n + D_p)$. τ_{eff} is discussed later in this section. With the device geometry less than unity, this approximation is useful for thin-PIN diodes. [32]

With this nonzero R_{rf}, the entire voltage drop across the PIN diode is

$$V_{PIN} = 2V_d + V_{rf} = 2V_d + I_d R_{rf}, \tag{2.3}$$

where V_d is the diode drop across the ideal PN diode and V_{rf} is the voltage drop across the variable resistance. The same I_d runs through the entire PIN diode, so one could add a load line for R_{rf} on-top the I-V curve for the PIN diode. The PIN diode I-V characteristic can be found then by fitting the points to the curve I_d v. V_{PIN}. The plot, in accordance with the model in Figure 2-5(a) is depicted in Figure 2-6.

The total small signal impedance across the entire PIN diode is $Z = 2r_d + R_{rf}$.



(a) Model

(b) Small Signal Circuit

Figure 2-5: (a) Circuit Model of PIN Diode in two parts - two ideal PN diodes with capacitance C across them for reverse-bias operation, and the variable resistance R_{rf}. (b) Small Signal Equivalent Circuit of PIN Diode - r_d and C_d are small signal parameters of a standard diode. [33]

From the equivalent circuit in Figure 2-5(b), we see that Z is actually frequency dependent. At low (down to DC) frequencies, the PIN diode behaves as a standard PN diode. In thin PIN diodes (where the device geometry is less than unity) R_{rf} is less than r_d, so for large currents, $Z \approx 2r_d$. At high frequencies, C_d shorts out r_d and $Z \approx R_{rf}$. The two approximations for Z at low and high frequencies hold for all non-zero values of forward bias current.

The current level affects the linearity of the variable resistor. Ideally, R_{rf} is K/I_d, where K is a constant value that is a function of the parameters in Equation 2.2. In

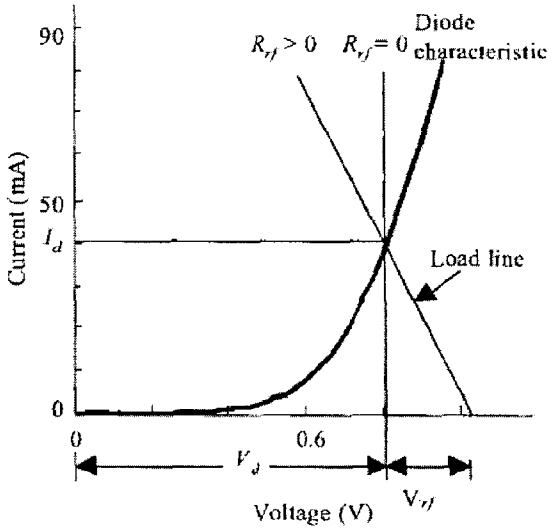


Figure 2-6: I-V Characteristic of PIN Diode, with standard PN I-V curve and load line for non-zero R_{rf} for high frequency operation of the diode. [30]

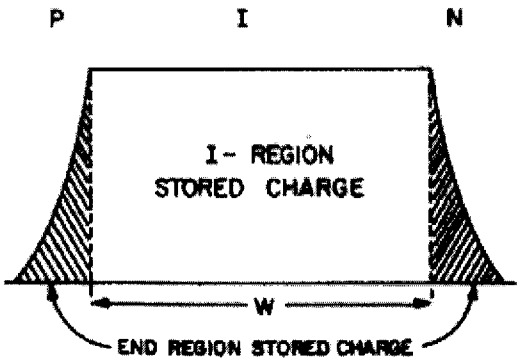


Figure 2-7: Plot of charge stored in a forward biased PIN diode, including end-region and intrinsic-region stored charge. [31]

the high-frequency case where Z is dominated by R_{rf}, increasing the DC bias current does not increase Z linearly. At low levels of bias, $\tau_{eff} \approx \tau$, which is a parameter that can be extracted experimentally and is not a function of bias current itself. Then K is a constant value and $R_{rf}I_d$ product is also constant. At higher levels of bias, there is a greater injection of carriers into the intrinsic region, and a buildup at the end regions occurs, as seen in Figure 2-7. There is a nonlinear increase in recombination rates in the end regions, which lowers the amount of charge stored in the intrinsic region. The effective charge in the intrinsic region is not $Q = I_d\tau$ anymore, but a new $Q_{eff} = I_d\tau_{eff}$ where τ_{eff} lumps the effects in the end regions with the intrinsic-region behavior for an empirical effective carrier lifetime [31].

Oftentimes, the parasitic elements are modeled in the PIN diode equivalent circuit to account for packaging. For example, a parasitic inductance L from packaging may be added in series with R_{rf}, making it a series RL circuit in forward bias. For simplicity, we design the PIN diode into the system without considering the L, because the 70MHz frequency of interest is not near the RF range that PIN diodes are often used.

The PIN diode used was the BAP50-05 from Philips Semiconductors. This double diode package (common cathode) provides a forward resistance up to 600Ω from 10μA to 10mA bias current [14]. Since 70MHz is not quite RF, we redefined R_{rf} to be R_{PIN}. Fitting the datasheet points to the I_d v. V_{PIN} curve, R_{PIN} can be modeled to have an exponential relationship with I_d,

$$R_{PIN} = AI_d^{-K}, \tag{2.4}$$

where A and K are determined by curve fitting the datasheet values of the BAP50-05 PIN diode [14]. A was found to be 14.538 and $K = 0.6862$ in Figure 2-8.

With I_d measurements and extrapolated A and K values from the PIN diode model, the diode resistance was plotted across a range of forward bias current, shown in Figure 2-9.

2.5 Varactor Diodes

Varactor diodes provide a variable capacitance as a reverse bias voltage is applied to the diode junction. If a diode is reverse biased, then there is a region void of carriers, nominally called the depletion region. The reverse-biased diode then is a P-region (plate), depletion region (dielectric), and a N-region (plate), which models a capacitor. The variable capacitance value arises from the change in depletion region in response to the applied voltage. Oftentimes, varactors are used for tuning over a range of frequencies. At higher frequencies, there is a wider tuning range possible for varactors. The varactors used are the Philips BB207 double diode package [15].

2.6 Mixers

Much of the pre-ADC design of this application resemble a standard receiver system where a signal is shifted in frequency then goes through a signal processing chain of various amplifiers and filters before being sampled by the ADC. In the design for the new application, mixers, amplifiers and filters will also be used. Thus design

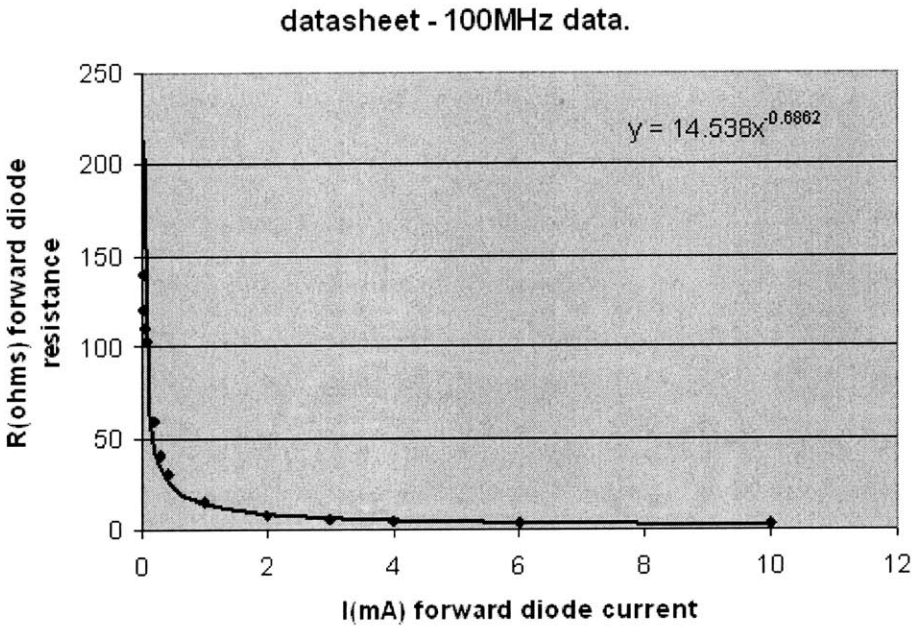


Figure 2-8: Fitted Curve to BAP50-05 Datasheet Values for 100 MHz Data.

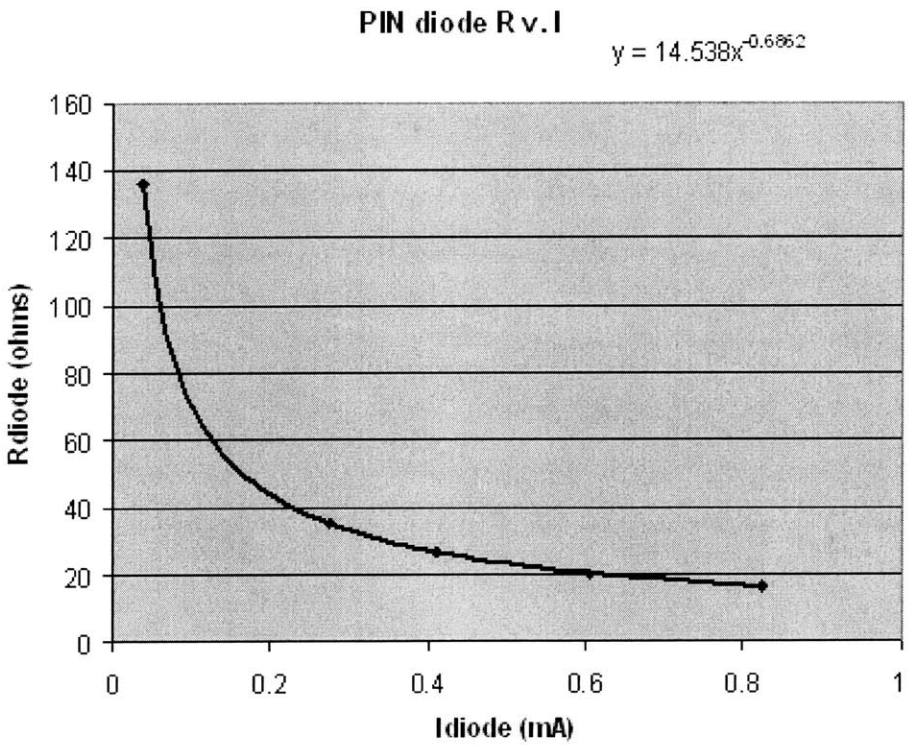


Figure 2-9: Diode Resistance Derived from Datasheet Equation, at $f_c = 70$MHz.

considerations for each of these analog components are important. Here, we look at the mixer design in more detail. In the proposed work, mixers will be used in the low frequency (MHz) domain instead of the RF domain. Their primary function is to perform upconversion like in transmitter systems rather than downcoversion mixers in standard receivers.

The mixer takes an input, often a low noise amplified signal, and translates it to a different frequency. Frequency translation is possible through the linear addition or subtraction of frequencies. The design of the mixer will be extremely important in this thesis because it is here where many considerations of modulation, noise, image rejection, and others must be accounted for in order to translate low-frequency signals to the IF band for further processing.

The mixer takes two signals and multiplies them in the time domain. Mathematically, if the two signals are $A\cos(\omega_1 t)$ and $B\cos(\omega_2 t)$, the product of the two signals is:

$$\frac{AB}{2}[\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t]. \tag{2.5}$$

The output of the mixer results in two output signals operating at the sum and difference of the two input frequencies. The mixer stage in the receiver is shown diagrammatically in Figure 2-10.

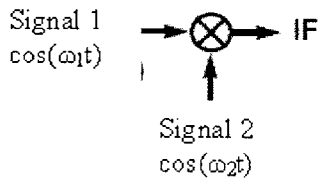


Figure 2-10: Mixer Diagram.

Signal 1 and Signal 2 multiply to produce a frequency shifted output signal in the IF Band. From Equation 2.5, A=B=1.

There are several nonidealities in mixers that need to be considered in design. Noise, linearity, dynamic range and isolation are discussed briefly.

Noise figure characterizes how effective the device is at rejecting noise while maintaining the signal. It is defined as the ratio of input signal-to-noise ratio (SNR) to output IF SNR. It varies across different types of mixers because it is highly dependent on whether or not both output frequencies are desired. If both bands (frequencies) are desirable because they contain useful information, there is twice the signal power. Noise figure improves in this case, which is termed the double-sideband (DSB) case. In the single-sideband (SSB) case where only one of the bands is considered, the noise figure is degraded by 3 dB ($3dB = 10\log(0.5)$). In the case that the mixer has the worst noise figure in the system additional pre-mixer stages may be necessary to improve the noise figure of the system. If SSB is preferred, it is possible that an image rejection filter will be implemented before the mixer to greatly attenuate the image signal before mixing.

Here, linearity and dynamic range are also important in mixer design. Linearity characterizes how the mixer output amplitude (power) varies as the input amplitude (power) changes, at a given frequency. Besides noise figure, gain, and power consid-

erations, the mixer must maintain linear operation with both strong and weak input signals. Distortion, in particular when a weak signal is in presence of a strong interfering signal, must be minimized. This is cruical in the application of ultrasound. Dynamic performance of the system may be dominated by the dynamic performance of the mixer as it is not only the first element in the signal chain but also a challenging element to design.

There are many topologies for mixers, such as square law mixers, multiplier based mixers and double-balanced mixers, to name a few [17]. Since dynamic performance is important, the active double-balanced mixer was selected. Active devices, although they require power, can provide conversion gain instead of loss. A double balanced mixer provides better isolation between the local oscillator and the output port of the mixer. Image reject and I/Q mixers were considered for SSB to properly obtain one sideband. However, these mixers are much more complicated. For this application if good filtering through SAWs can attenuate both the clock and image feedthrough signals, then the more complicated mixers are not necessary.

The mixer used in the thesis is Linear Technology's own LT5521 active double-balanced mixer. It has low distortion, 40dBm clock feedthrough, and an impressive 24.dBm output IP3 at output frequency 1.95GHz. The noise figure is acceptable at 12.5dB. Although designed for high frequencies, it is usable at the intermediate frequencies if it is designed with the proper network. The topology of the LT5521 follows a Gilbert cell mixer, with differential inputs feeding into degenerated common emitters of the differential pairs in the Gilbert topology [17]. The high frequency local oscillator switches between the differential pairs. The open collector differential output has 300Ω resistance across it. Additional information can be found in [2].

2.7 Amplifiers

The test experiment used two low noise AH31 amplifiers, with +16 to +20dB gain over 44MHz to 95MHz. The application circuit is shown in Figure 2-11. The ouput IP3 point is 42dBm at 75MHz and the noise figure is 2.4dB. Both amplifiers were

needed to ensure that the mixer would not be overdriven by a large input power. It is recommended that +20dB gain amplifiers with very low distortion are used in the system. It is also desirable to have a more limiting bandwidth amplifier. A bandwidth less than the Nyquist zone prevents foldback of any noise or distortion from the amplifier.

2.8 Analog-to-Digital Converters (ADCs)

The LTC2249 14-bit 80MSPS analog to digital converter was used for this particular experiment. This six stage pipelined ADC is low power, high resolution, and has 73dB SNR. Refer to [1] for more information.

2.9 Clock Sources

The clock rate of 70MHz is a typical intermediate frequency (IF) and many components such as SAW filters and IF amplifiers are designed with a center frequency of 70MHz, or a multiple of it. Two clocks are required: one for the ADC sampling source and another for the upconversion local oscillator (LO). The design lab owned a 70MHz crystal oscillator. For a clock frequency other than 70MHz, a narrowband tunable helical filter with a standard signal generator can be used as a clock source.

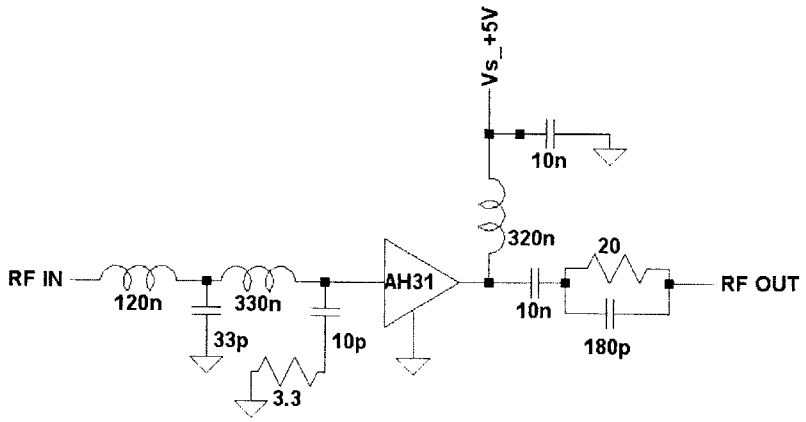


Figure 2-11: AH31 Amplifier Application Circuit.

Chapter 3

Design Modifications

3.1 Setup

In the application setup, there were many design considerations in the system. Some design changes were made after initial setup of the application, done in the Design Lab. Some design modifications were made directly on the demonstration boards while some required construction of a new part. Tools used were laboratory measuring and analyzing tools and programs for design and simulation.

3.2 Simulation

The program used for simulation was Linear Technology's SwitcherCAD SPICE simulator, available online at zero cost. Models of various components and filter designs were constructed in this program, and laboratory results were compared to simulation output.

3.3 Design

The signal chain, shown again in Figure 3-1, starts with a low frequency signal which is translated to a higher frequency using the LT5521 before going through a series of amplifiers, filters, and varying element networks. The end of the signal chain goes

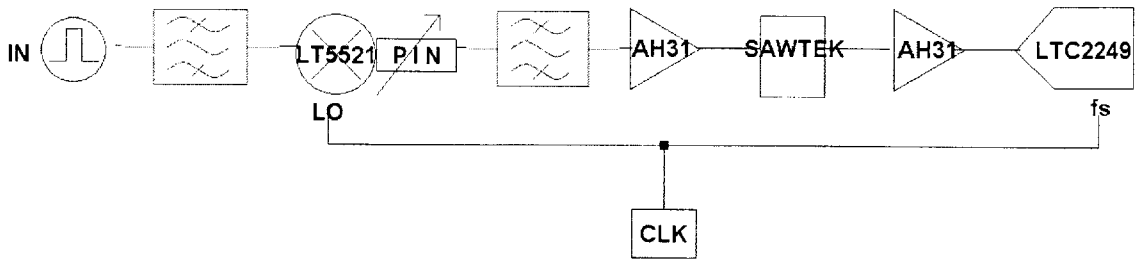


Figure 3-1: Frequency Translation Method General Block Diagram.

into the ADC input and is sampled by a clock source for data conversion.

Design components in the thesis were broken down into four categories: passive filters, mixer, variable gain devices, variable filter devices. Each component design is detailed in its own section, with references back to the complete system design.

3.3.1 Filter Design

The signal is filtered throughout the pre-ADC path in order to present a high quality, undistorted signal at the ADC input. Several types of filters are needed and were investigated for appropriate applications. The filters designed and used in this frequency translation method include: 1MHz – 40MHz cascaded lowpass–highpass elliptic section filter, 70MHz Butterworth wideband bandpass filter, 60 – 86MHz variable bandpass filter.

A 1MHz–40MHz bandpass filter was designed to filter the low frequency signal before upconversion. This filter was comprised of cascaded lowpass and highpass elliptic sections, each 5 poles. The filter design tables were taken from Williams' *Filter Design Handbook* and modified for a 1MHz high pass and 40MHz low pass with stopband attenuation $A_{min} = 40dB$ at a stopband frequency at 70MHz [38]. The high pass filter has a stopband frequency at 800kHz.

The 70MHz bandpass filter is designed with more relaxed requirements, because other components in the signal chain will subsequently filter the passband signal content. The bandpass filter diagram in Figure 3-2 shows the design specifications. In the passband, it is desirable to have as little loss from input to output. The

designed filter has -0.7dB insertion loss. It is also desirable for this bandpass filter to block reflected waves in the passband. The S11 or S22 parameters indicate return loss, so minimal levels of return loss in the passband is desired. A -24dB return loss in the passband is sufficient for the application. The filter performance matches expectations from simulation.

Elliptic sections, although more complicated to design than Butterworth or Chebyshev filters, provide a steeper stopband response and hence greater attenuation in regions outside the passband. These filters are useful for providing a steep attenuation at each of the stopbands. To prevent any interference from input signal harmonics at or around the local oscillator of the mixer, it is advantageous to design an elliptic section filter with a stopband at the particular local oscillator frequency. In the test system, LO=70MHz, so this 1MHz-40MHz filter has a stopband at 70MHz with 55dB attenuation. The schematic is shown in Figure 3-3(a).

The system requires approximately 20dB gain while using lossy SAW filters so two AH31 amplifiers are needed after the mixer and before the ADC to achieve a full scale ADC input. Instead of having the mixer output go straight to one of the amplifiers, it is better to bandpass filter the signal before one of the amplifiers. This ensures second (and higher order) harmonics are not passed through the amplifier, which will cause

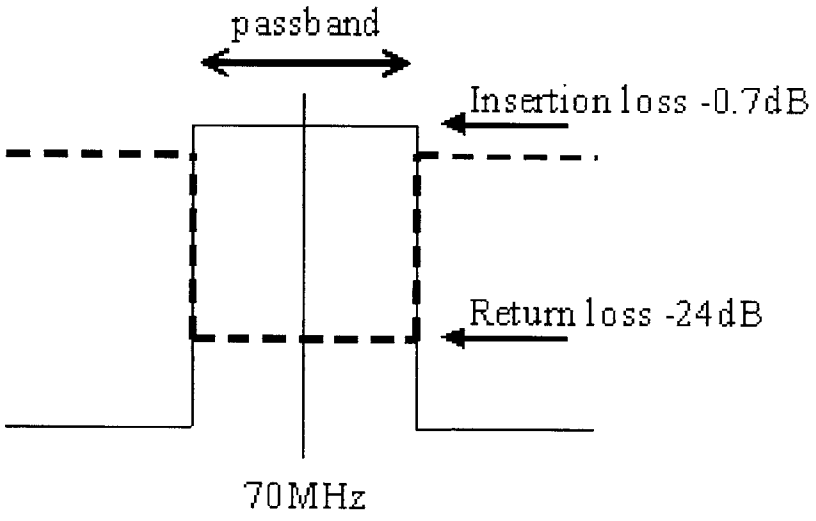
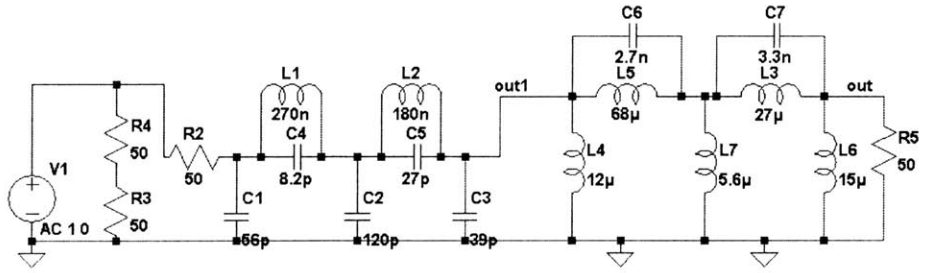
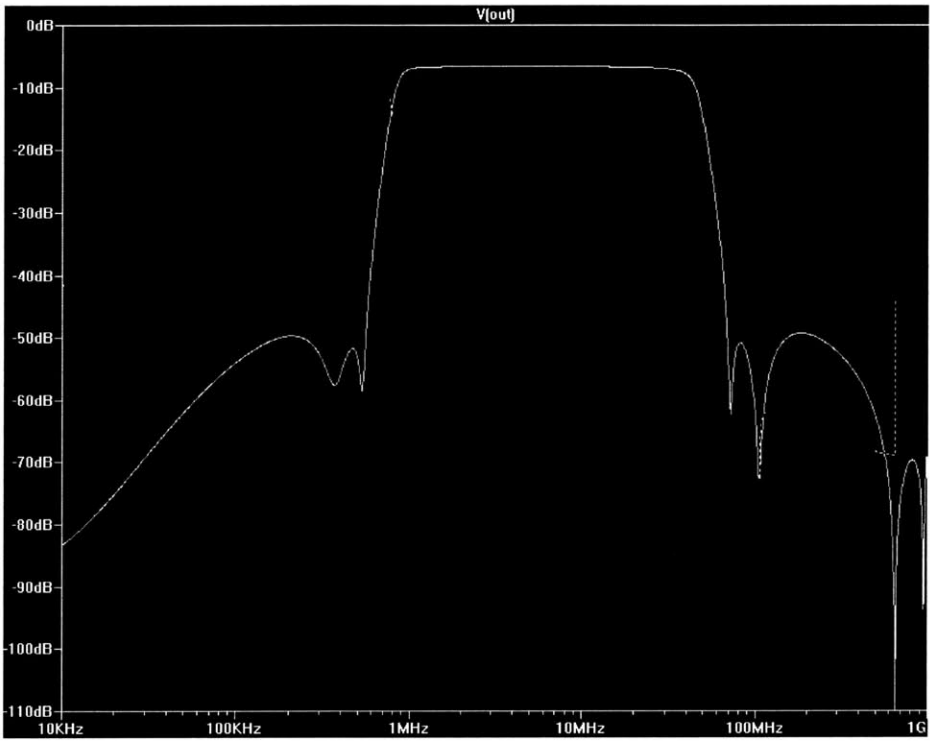


Figure 3-2: Diagram of 70MHz wideband bandpass filter.



(a) Schematic

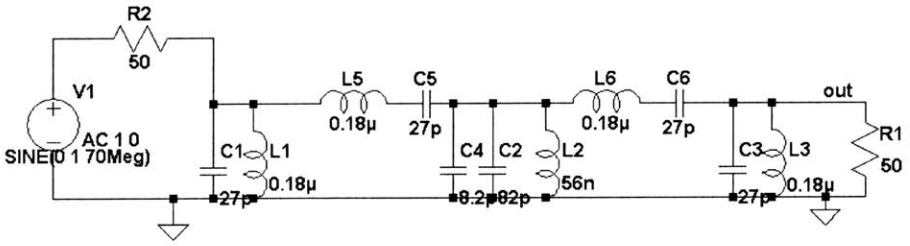


(b) Simulation

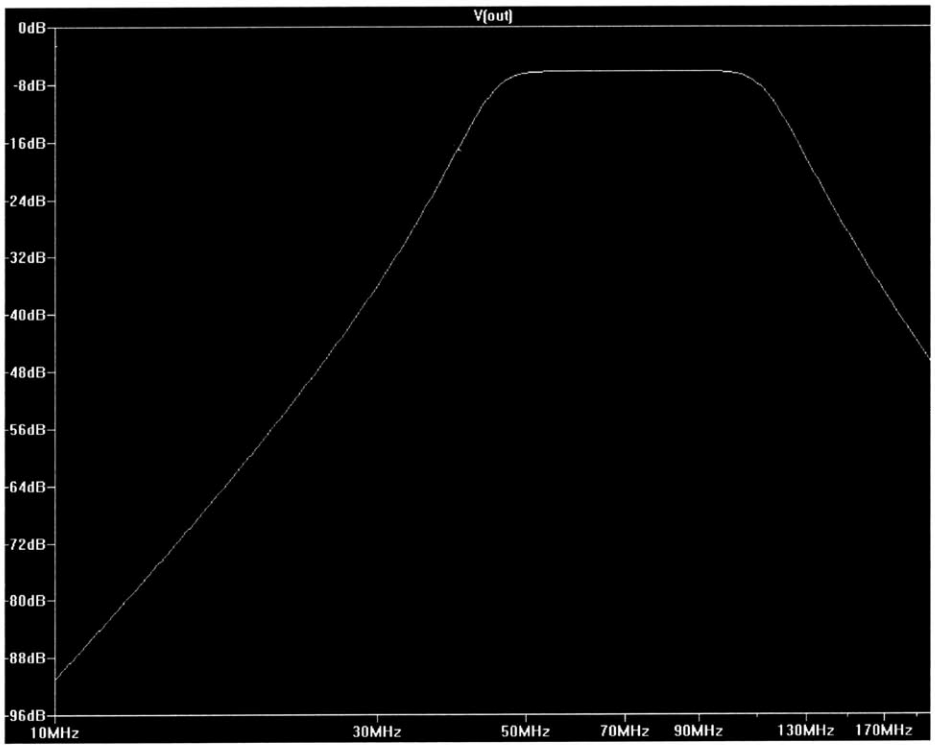
Figure 3-3: Passive Low Frequency Bandpass Filter.

distortion. The filter designed need not have a steep stopband attenuation factor, so elliptic sections are not required. A standard butterworth bandpass filter will suffice.

For a mixing LO frequency of 70MHz, a 40M – 100MHz 5-pole bandpass filter was designed, with -1.3dB insertion loss. The filter attenuates the 140MHz second harmonic by 24dB. The simulation results in Figure 3-4(b) match the design expectations and lab implementation.



(a) Schematic



(b) Simulation

Figure 3-4: Passive Bandpass Filter, $f_c = 70$ MHz

The variable filter, useful in some applications, was designed to provide approximately 20 – 30MHz variation. The discussion of this design is reserved for Section

3.3.4.

3.3.2 Mixer Network Design

The LT5521 was designed for an IF input and an upconversion to RF (GHz) and thus the DC642A demonstration board was configured for such an application. Because this frequency translation is operating at a much lower frequency range, modifications to the demo board circuit must be made to maximize the performance of the mixer.

The existing stock DC642A is shown in Figure 3-5 for $f_{IF} = 250MHz, V_{cc} = 5V$.

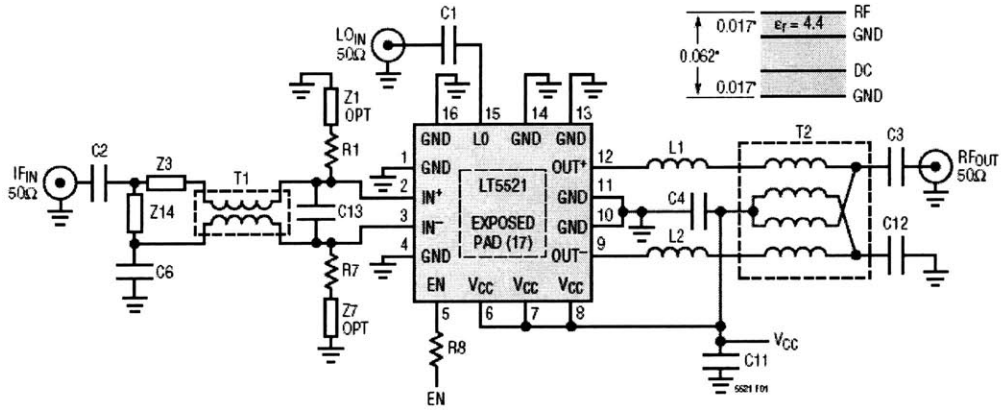


Figure 1. Demonstration Board Schematic

Table 1. Demonstration Board Bill of Materials[1, 2]

REF	f_{IF} = 250MHz, f_{RF} = 1.95GHz f_{LO} = 1.7GHz, V_{CC} = 5V	f_{IF} = 44MHz, f_{RF} = 1.045GHz f_{LO} = 1.001GHz, V_{CC} = 5V	f_{IF} = 250MHz, f_{RF} = 1.95GHz f_{LO} = 1.7GHz, V_{CC} = 3.3V
R1, R7	110Ω, 1%	110Ω, 1%	22.6Ω, 1%
Z14	10pF	120nH	10pF
Z3	0Ω	150pF	0Ω
L1, L2	2.7nH	10nH	2.7nH
T1	M/A-COM MABACT0010[3]	M/A-COM MABACT0010[3]	M/A-COM MABACT0010[3]
T2	M/A-COM ETC1.6-4-2-3	M/A-COM ETC1.6-4-2-3	M/A-COM ETC1.6-4-2-3
C1, C13	6.8pF	27pF	6.8pF
C3	82pF	3.9pF	82pF
C12	82pF	1nF	82pF
C2, C4, C6	1nF	1nF	1nF
C11	1µF	1µF	1µF
Z1, Z7	0Ω	0Ω	100nH
THIS COMPONENT CAN BE REPLACED BY PCB TRACE ON FINAL APPLICATION			
R8	10k	10k	10k

Note 1: Tabulated values are used for characterization measurements.
Note 2: Components shown on the schematic are included for consistency with the demo board. If no value is shown for the component, the site is unpopulated.
Note 3: T1 also M/A-COM ETC1-1-13 and Sprague Goodman GLSW4M202. These alternative transformers have been measured and have similar performance.

Figure 3-5: LT5521 Stock Demonstration Board (DC642A).

To adjust for a 1M – 10MHz input IF frequency, the coupling capacitors C2, C6,

C3 and C12 were changed to 100nF capacitance. L1 and L2 were replaced with wires for minimal resistance. T1 and T2 must be selected for the appropriate impedance matching and frequency. It was suggested[1] T2 be a 4:1 MABAES0054 transmission line transformer, with 5-1000MHz frequency range, -1dB insertion loss [10].

In initial testing of this circuit, it was discovered that there was a considerable DC offset at the output. Since the upconverted signal is sampled at a rate equal to the clock (LO), any clock feedthrough would be interpreted as DC offset. With the stock DC642A, there was offset on the order of 100-150mV from clock feedthrough. This offset is significant and reduces the dynamic range of the signal (there will be considerable clipping on one side of the signal, distorting the final output).

If LO feedthrough is significant, then DSB is not a practical method with this application because the LO frequency will pass through to the ADC. But design modifications can be made to attenuate carrier feedthrough. The bottleneck was found to be in the mixer design. Because the mixer was designed for much higher frequencies, certain transformers provide better isolation and impedance matching than others. But those transformers cannot be used at IF 70MHz when they are optimal in the GHz range. An unbalanced network at the mixer output can kill any quality output-LO isolation the mixer itself may have. So, even if the mixer datasheet isolation figure given at higher frequencies is about the same at the lower IF frequency, the output network design is important to ensure that there is a balanced differential output. Otherwise, local oscillator feedthrough can become significant.

Measuring the LO-output port isolation on Agilent's 8561EC Spectrum Analyzer, the stock board has -48dBm isolation (no signal at the IN port) with LO=70MHz, 0dBm. However, with an input signal at 3.58MHz -19dBm, the mixer output had the desired signals of -19.33dBm at the sum and difference frequencies (73.58MHz and 66.42MHz) and the undesired LO feedthrough of -52dBm. It is attenuated by only 32dBm from the desired output signal. With a post-mixer gain of about 20dB, the LO feedthrough seen would then be -12dB, which is very undesirable in the upconversion scheme.

[1]Suggestion made by Doug Stuetzle, Designer, Linear Technology. July 2006.

The output circuit was redesigned as such: Instead of just one T2 transformer (the 4:1 MABAES0054), a second transformer follows it, shown in Figure 3-6. This output circuit provides a much more balanced network in the desirable IF output frequencies. T1 is a 1:1 ETC1-1-13 M/A-COM balun transformer, 1.1-3000MHz frequency range, -1dB insertion loss. T1's purpose is to properly convert differential to single ended output. The values of the coupling capacitors were increased from 82pF to 100nF. Also, L1 and L2 are used to configure the output to a particular frequency, but they were replaced with wire again (mixer output directly connects to T2).

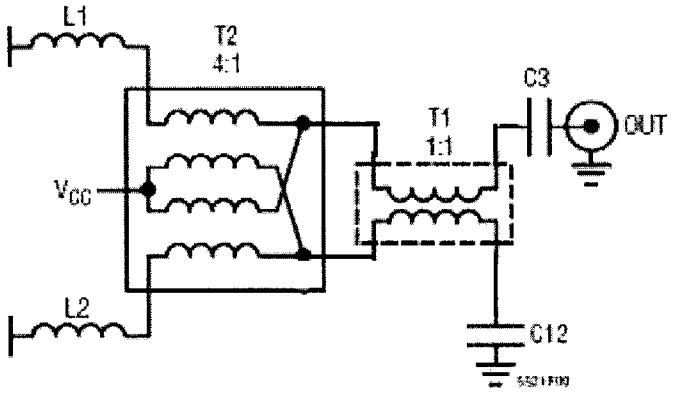


Figure 3-6: Redesigned LT5521 Output Network.

With this design modification, the entire system has a DC offset of -25dB. This is equivalent to 50mV or 400 of 8192 units. This was measured in two ways. The DC level can be measured with the same sample and mixing clock frequency. It can also be measured using PScope with different clocks, offset enough so that they do not a)interfere with each other nor b) lie at the same frequency as the upconverted input signal. The carrier feedthrough was measured to be -25dB in two cases : f_s = 70MHz (ADC clock), LO = 72MHz (mixer); and f_s = 70MHz, LO = 70.5MHz.

However, the spectrum still does not look incredibly clean. There is an elevated noise level about the desired frequency in Figure 3-7. Looking at the input network of the LT5521, it is not matched to at 50Ω output at 70MHz frequency. In fact, it is only 20Ω at 70MHz. This means an impedance transformation must occur through the input network. Thus, a 1:1 balun transformer like the ETC1-1-13 will not be

sufficient. Additionally, baluns at low frequencies (in the 1-10MHz range) do not function as intended, so a flux-coupled transformer is more appropriate. The ETC1-1T is the 1:1 flux-coupled transformer but it is 1:1. A 3:1 flux-coupled WBC3-1TL transformer from Coilcraft works from 0.3-900MHz and a -0.6dB insertion loss. This is the more appropriate choice for the input transformer, to convert the 50Ω line to the 20Ω differential input of the LT5521 mixer.

A quick check was to look at the return loss of the input network before and after impedance matching to a 50Ω transmission line. With the ETC1-1-13 1:1 balun in the input network, the S11 parameter was -3dB. With the WBC3-1TL 3:1 flux-coupled transformer, the S11 parameter was -12dB, a significant improvement over the original setup.

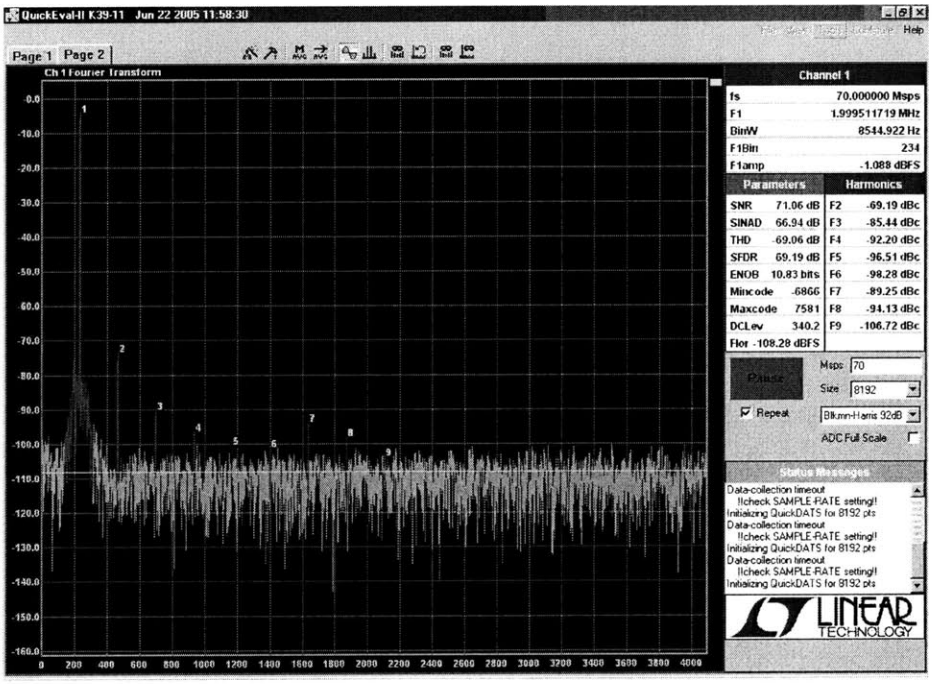
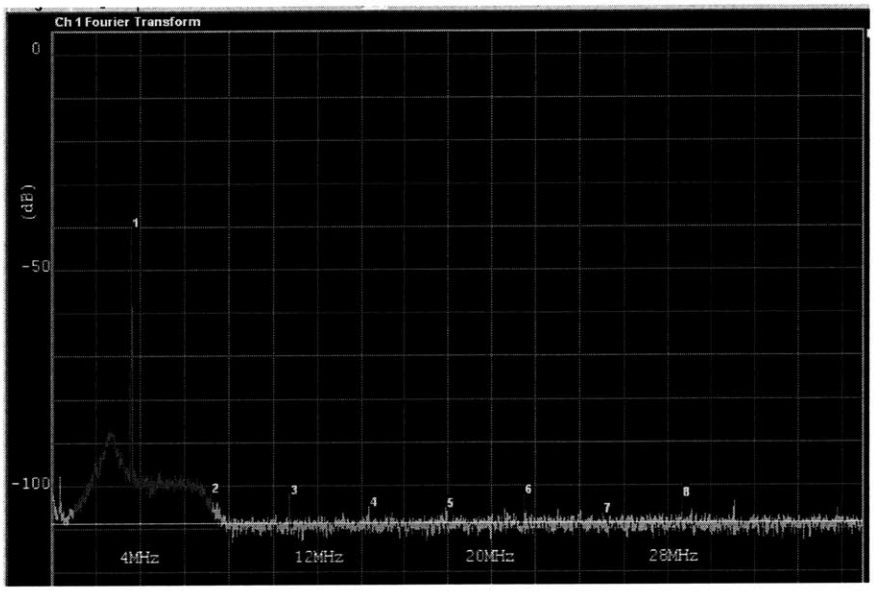


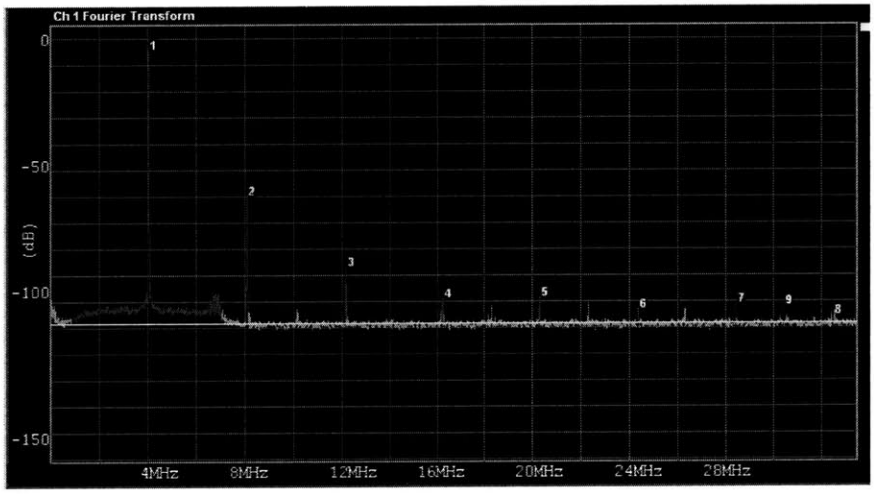
Figure 3-7: Mixer Output – Mismatched Input Impedance.

A comparison can be made between the upconversion scheme with a working modified board and the stock demonstration board, shown in Figure 3-8. The original board is not configured for the specified frequency range and cannot obtain full scale with the same input power level and signal chain as the working board. There is no significant DC level offset because it is attenuated by more than 30dB (expected

fundamental amplitude is full scale at -1dB). The working board can achieve full scale output and a much lower noise floor. The slightly raised noise level about the fundamental frequency is the ADC input bandwidth, limited by the 5MHz SAW filter.



(a) Stock Board



(b) Modified Board

Figure 3-8: Output Improvement with Modified LT5521 Board

3.3.3 Variable Gain Design

The PIN diodes' varying resistance changes the gain of the system. Placing the diodes at the output network of one of the components in the signal chain changes

the output impedance and the overall gain of the system. The mixer output has an internal impedance of 300Ω, so by placing the PIN diode at the output of the mixer, it is possible to achieve an output impedance of $0-300\Omega$. The LT5521 has a differential output, hence the choice of the double diode package (with a common cathode) is very useful here. By placing the two diodes across the differential output, then biasing the cathode of the diodes we can achieve variable mixer output impedance. The PIN diodes are placed right on the legs of the IC package to minimize parasitics on the board like in Figure 3-9.

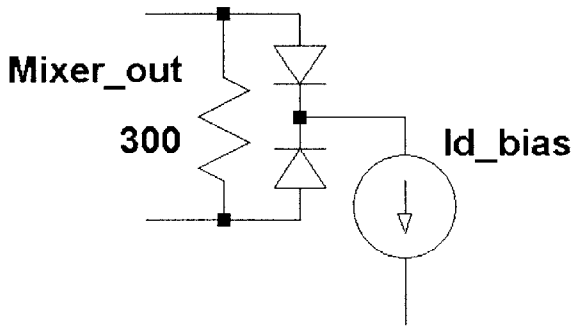


Figure 3-9: PIN Diode Package in System Design.

The anodes of the diodes are biased to the supplies through the center-tapped transmission line T2 transformer. Id_{bias} is determined by a control voltage and resistor $R_b = 180\Omega$. The bias network makes it easy to measure the current through the PIN diodes, using the 180Ω resistor. The voltage drop across the diode is about 0.8V in forward bias, and the voltage drop across R_b can be measured to find Id_{bias}. Each diode receives half the bias current Id_{bias}. The differential impedance of the diode is $2R_{PIN}$, R_{PIN} found in Equation 2.4, and the effective output impedance of the entire mixer network is $\frac{2R_{PIN} \| Z_o}{4}$, where Z_o is the mixer output impedance, and the 4:1 transformer is used. With this variation in mixer output impedance, a range of 27dB attenuation was achieved with a 0-5V bias (see Figure 3-10). The relationship between the overall system attenuation and the effective output impedance is plotted over a 400mV bias range in Figure 3-11.

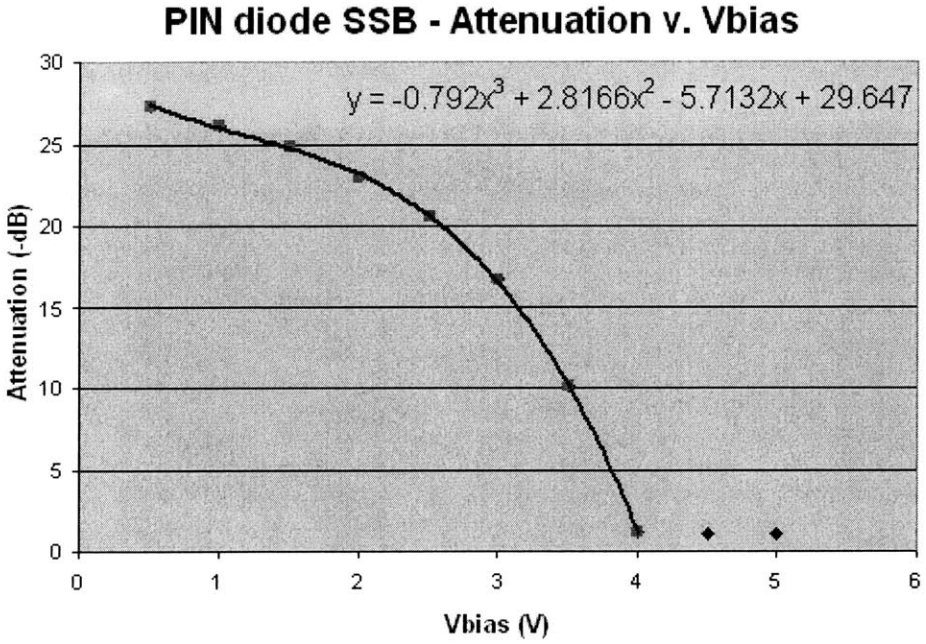


Figure 3-10: System Attenuation v. Bias Voltage on the PIN Diodes.

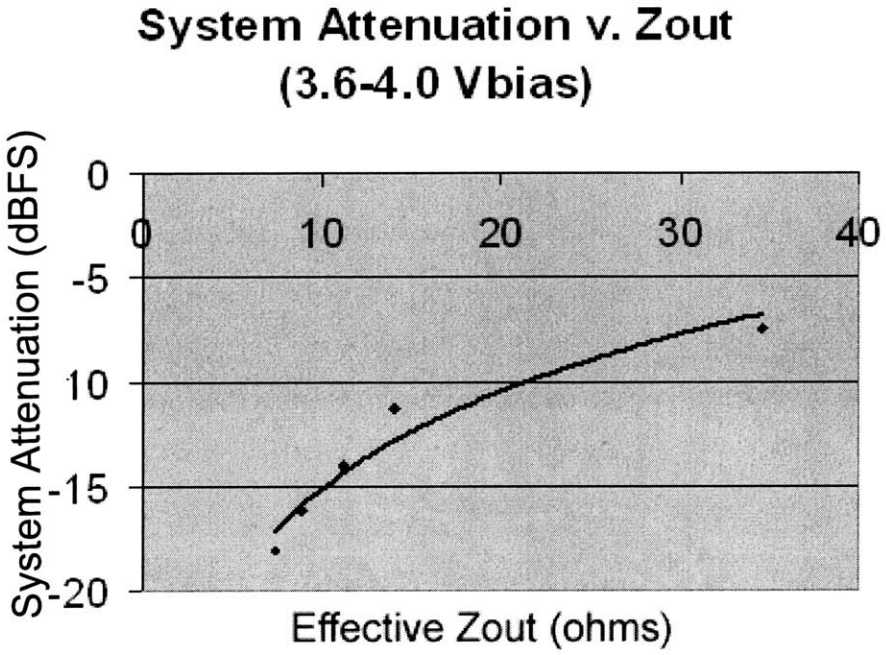


Figure 3-11: Attenuation v. Effective Output Impedance of the System

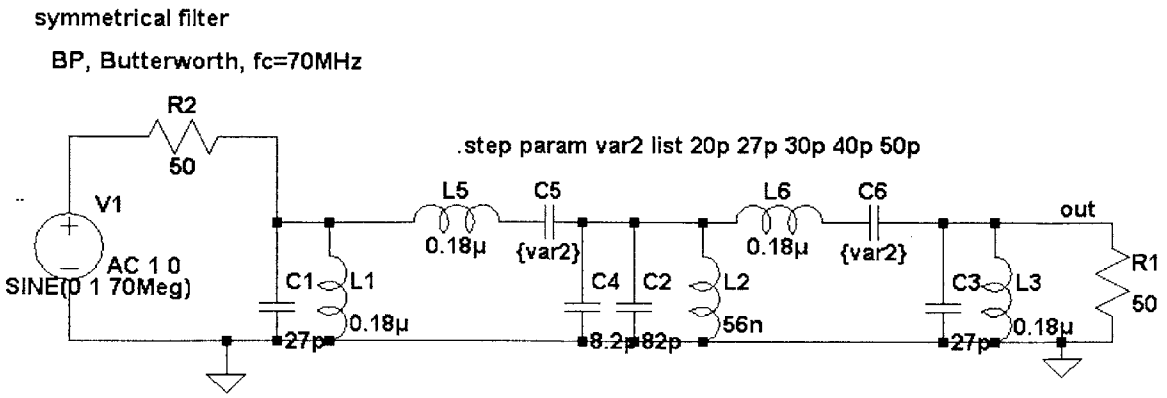
3.3.4 Variable Filter Design

The varactor diodes were fairly simple to design into the system. Each diode acts as a variable capacitor, so placing them in parallel with a capacitor in a filter design will suffice. The diodes can be biased at cathodes with a large resistor and control voltage (much like the PIN diode setup). The challenging part was determining what type of design to actually use. As discussed before, Butterworth and Chebyshev filter designs are easier to design than elliptic section filters. However, a simple test showed that adding varactor diodes into a Butterworth filter was much harder to do than anticipated.

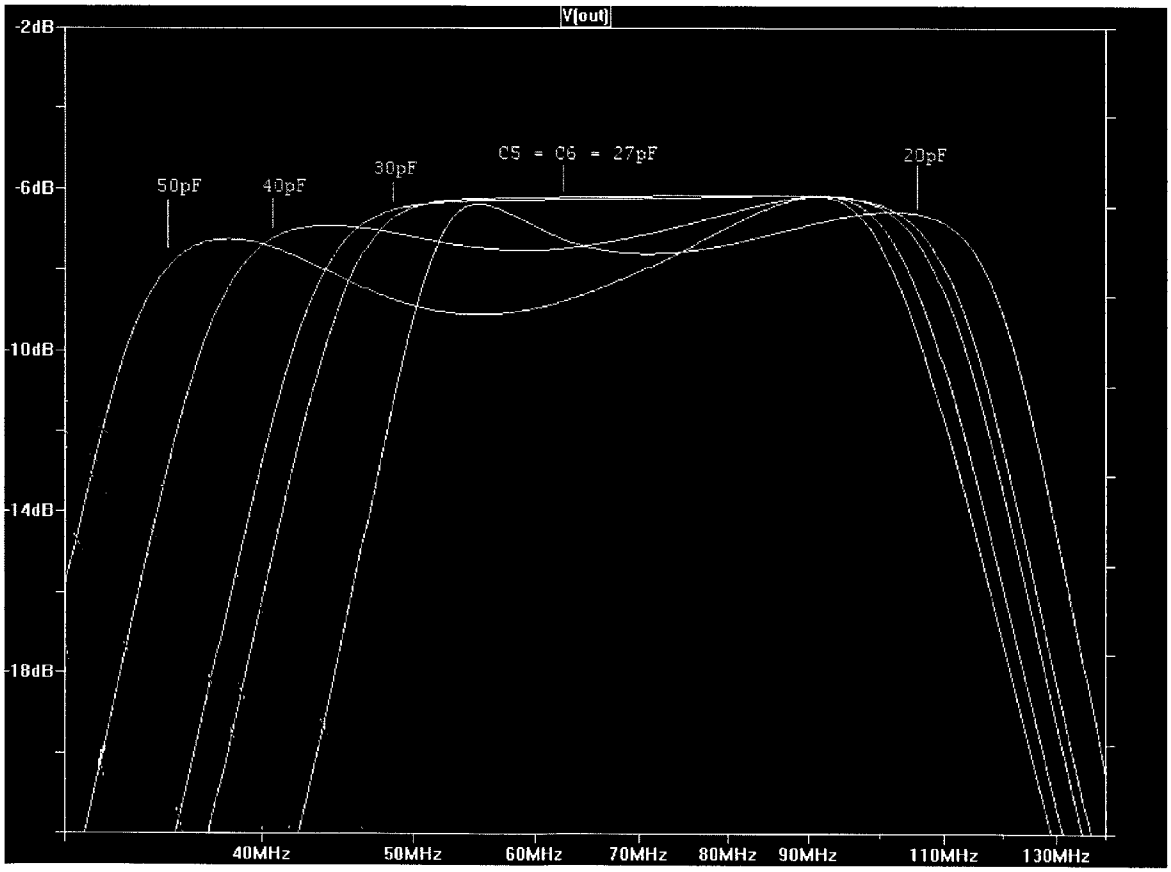
Figure 3-12(a) shows how C5 and C6 values were varied to producing the effects of a varactor diode circuit. To produce the original 70MHz bandpass five-pole butterworth filter, $C5 = C6 = 27pF$. Here, they are varied from 20pF to 50pF. The simulation results in Figure 3-12(b) show an inconsistent filter response across the capacitor range, quite unsatisfactory for a true variable filter. The ideal response is to have the same filter response shifted over a certain frequency range to provide the same performance in the system.

Elliptic sections were considered because their topologies allow for each section to have their own tuning varactor diodes. Construction of these filters with varactor diodes are easy, because the diodes can be just placed on top of each elliptic section. Although this is not a wideband filter, highpass 7-pole and lowpass 5-pole elliptic filters were designed independently, so that the effect of variable filter could be observed independently at each 3dB point. Figure 3-13 shows the two elliptic filters individually with varactor diodes. For the low pass filter $f_{3dB} = 80$MHz and for the high pass filter, $f_{3dB} = 70$MHz. These results show the highpass filter with varactor diodes across one of the elliptic sections. The behavior deviates from the expected response around the 3dB frequency.

Combining the two elliptic section filters as in Figure 3-14(a), and placing varactor diodes on each elliptic section to maintain the same response, produced the bandpass response in Figure 3-14(b). The varactor diodes are modeled in SPICE with the line



(a) Schematic



(b) Simulation

Figure 3-12: Variable Filter Design using Passive LC Bandpass Filter. In (b) the 5 plots correspond to simulations for different capacitor values (C5 and C6 as shown in (a)).

statement :

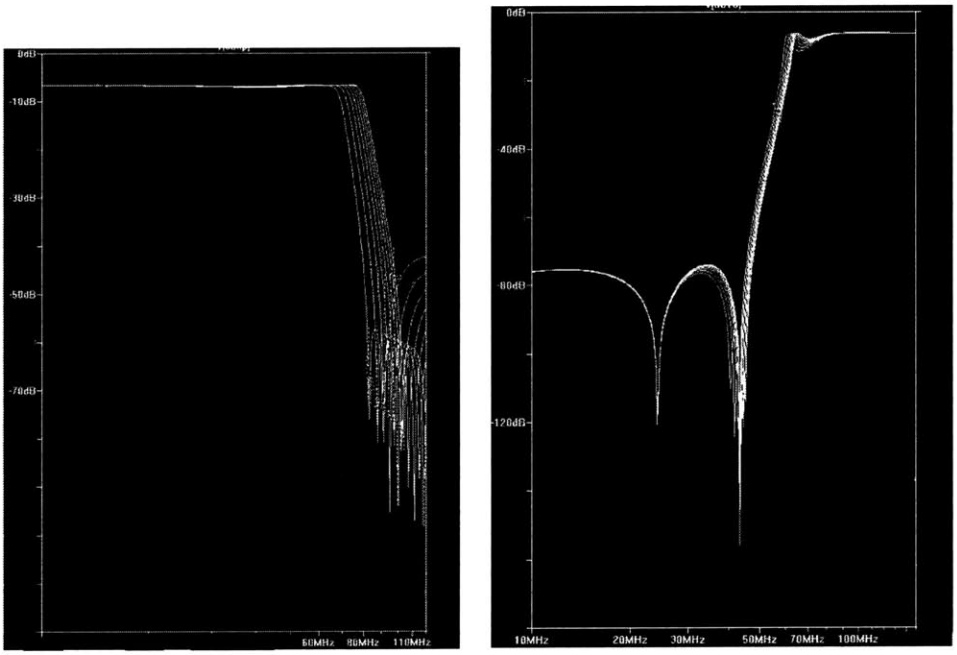
$$.model\ BB207VarCap\ D(R_s = 0.3\ \ C_{jo} = 122.5p\ \ M = 0.81153\ \ V_j = 1.4881$$
$$\text{mfg} = \text{Philips}\quad \text{type} = \text{Varactor})$$

The V2 voltage source is stepped from 1 to 10V, with 3-10V being the suitable operating range in the actual system setup. Each section has additional capacitance from the BB207 package and they are all stepped by the V2 voltage source.

The resultant elliptic section bandpass filter in Figure 3-14(b) shows consistent filter response across 60 to 85MHz. There is less than 0.2dB ripple in the passband across the filter range.

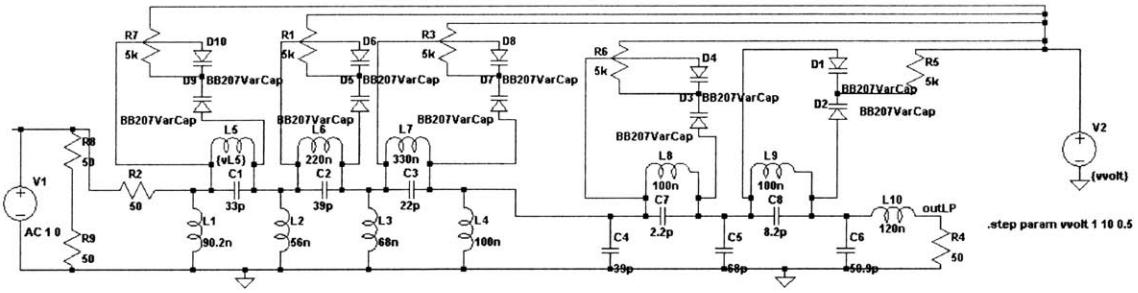
Figure 3-14(c) is the actual filter response of the design constructed on a copper clad board, with 50Ω transmission line. The measurement was made by the Network Analyzer. There is a greater change in passband insertion loss, but the filter response is similar to expected results.

The system achieved 60 to 86MHz variable filtering across a 10V bias range of the varactor diodes. From the network analyzer, the constructed elliptic bandpass filter

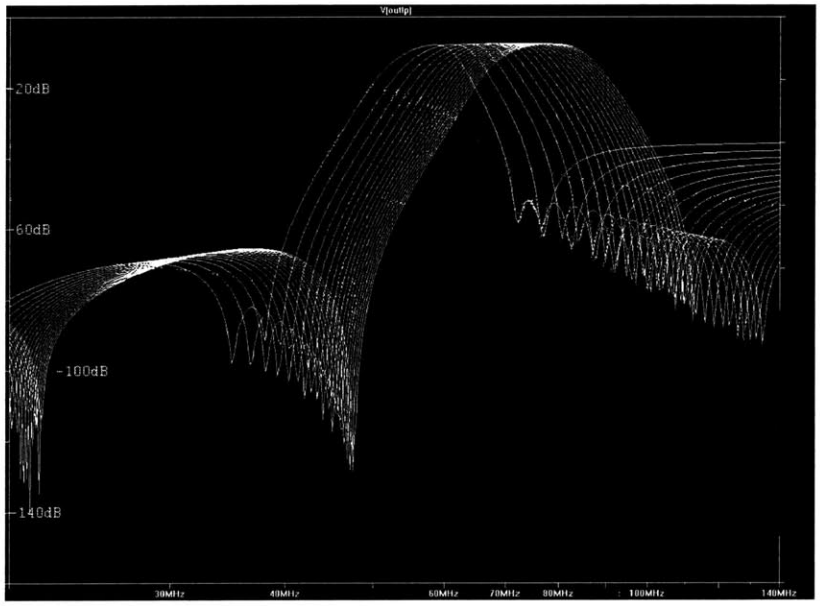


(a) Elliptic Low Pass Filter (b) Elliptic High Pass Filter

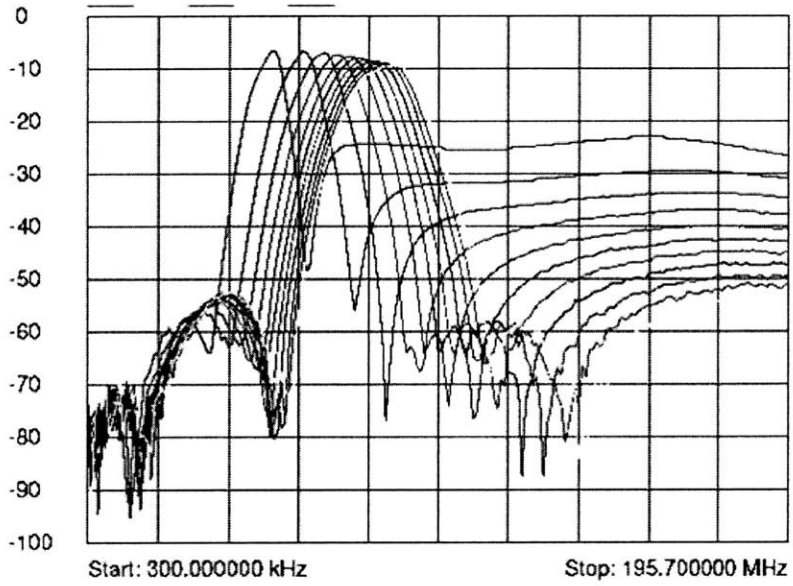
Figure 3-13: Simulation of Elliptic Filters with Varactor Diodes



(a) Schematic



(b) Simulation



(c) Network Plot

Figure 3-14: Elliptic Bandpass Variable Filter

has characteristics shown in Table 3.3.4.

Voltage Bias (V)	Center Freq (MHz)	S22 (-dB)
0	51.87	26
1	60.66	16
2	65.88	13
3	70	11.3
4	73.6	10.4
5	76.31	9.5
6	78.64	9
7	80.535	8.5
8	82.236	8
9	84.4	7.8
10	86.2	7.5

Table 3.1: Variable Filter Characteristics

The entire upconversion scheme with the varactor diodes biased at 2.8V, a 70MHz clock, and 2MHz input has 69dBFS SNR. As expected, adding variable filtering did not compromise the dynamic performance of the system.

3.3.5 Design Conclusion

Each component design was unique and challenging in its own respects, with novel techniques used to ensure practical implementation. Besides designing actual circuit networks, construction of the filters and setup of the system (it is after all heavily application based) are very important. I was able to design filters that work close to expected results from simulation, and achieve an improvement in results from mixer design. It became clear that filter and mixer design are two limiting components of such a frequency translation scheme. However, other application issues arise, as the next section highlights in the presentation and interpretation of results.

Chapter 4

Applications Setup

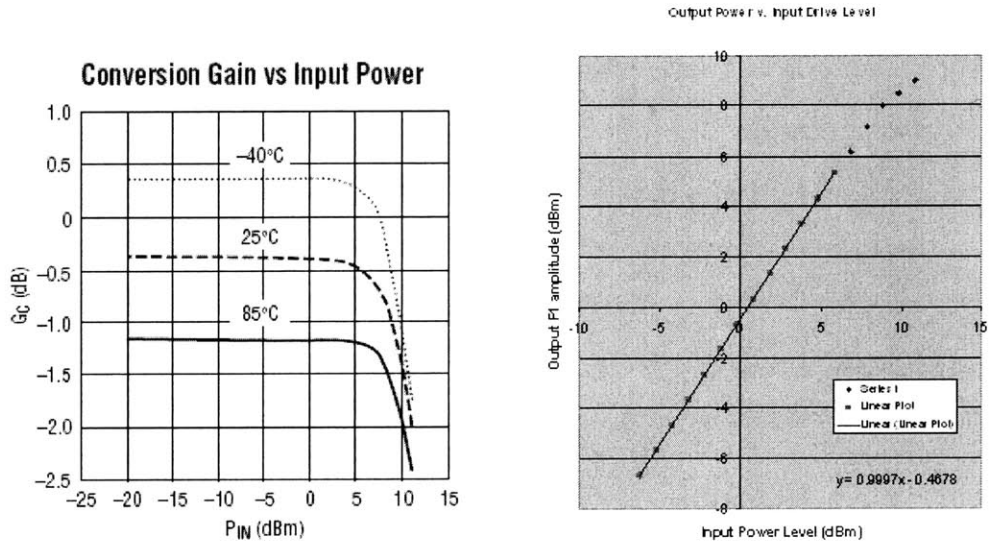
The setup for the application system was carried out in the Design Laboratory of Linear Technology in Milpitas, California under the supervision of one of the senior application engineers. Standard lab equipment was used and all components were either samples from the company or designed myself. The proprietary program PScope developed at Linear Technology was used to process the digitized signal with an 8192-point FFT and Blackman-Harris windowing function. Equipment used included signal generators from Hewlett Packard (model 8644B, 100kHz - 3.2MHz frequency range), a network analyzer from Hewlett Packard (model 8753C, 300kHz-6GHz frequency range), and a spectrum analyzer from Agilent (model 8561EC, 30Hz-6.5GHz frequency range).

This section describes some applications setup issues encountered in designing the frequency translation system. Most are standard high frequency issues not usually seen by ultrasound customers but are everyday issues for radio designers. Signal overdrive, reflected waves, impedance matching, single side-band, and double side-band are discussed here.

4.1 Signal Input Limitations

The signal level into the mixer cannot be too high. If overdriven, the mixer outputs a distorted signal compared to the lower frequency input, rather than a pure frequency-

shifted signal. For linearity, it is best to keep the input range less than 5dBm for the LT5521 [2]. A simple experiment verified datasheet specifications. Figure 4-1(a) shows that the gain falls drastically at $P_{in} > 5dBm$. The mixer input was driven from -24dBm to above 10.8dBm but the region of interest (-5 to +10 dBm) is plotted here in Figure 4-1(b). Up to 5dBm, the output fundamental amplitude and input power level have a linear relation, slope of 1 and gain approximately -0.5dBm (the intercept). Above 5dBm, the mixer reaches saturation because the points fall from the linear extrapolation, indicating that the mixer is now overdriven.



(a) Datasheet Figure, IN=250MHz and LO=1.7GHz. [2]

(b) LT5521, IN=4MHz and LO=70MHz

Figure 4-1: LT5521 Output v. Input Power

Thus, there is a minimum amount of gain required to bring the mixer output to full scale for the ADC. With a minimum 5dBm mixer input, -0.4 mixer conversion gain[1], and required +10dBm analog ADC input produces -1dBFS fullscale output, the minimum gain post-mixer is 4.67dB. The PScope plot in Figure 4-2 shows the distorted output due to an overdriven mixer. Using just one AH31 amplifier, one SAW filter (narrowband 5MHz bandwidth) and proper attenuator pads, the post-mixer gain was about 4-5dB, which is barely enough. There is significant distortion from the harmonics.

[1]Measured with Agilent 8561EC Spectrum Analyzer, with the modified LT5521 network design.

4.2 Clock Jitter

Clock jitter is a slight variation in the period of the signal, due to noise in the oscillatory system. Statistically, the period can be modeled as having a Gaussian distribution[25]. The jitter induces error in the output voltage proportional to jitter magnitude and input slew rate[26]. At higher frequencies and therefore higher slew rates, the effect of jitter is more pronounced. Since this application shifts a signal to higher frequency, clock jitter issues may arise.

With two clocks - one for the frequency translation and one for the ADC sampling, the jitter from the clocks can create an elevated noise floor or induce close in-phase noise about the fundamental signal. These effects degrade the dynamic range and the SNR of the system.

Since the upconversion will shift the signal to the IF range, which is in the range of sampling frequencies for the LTC2249, it proved advantageous to sample and shift

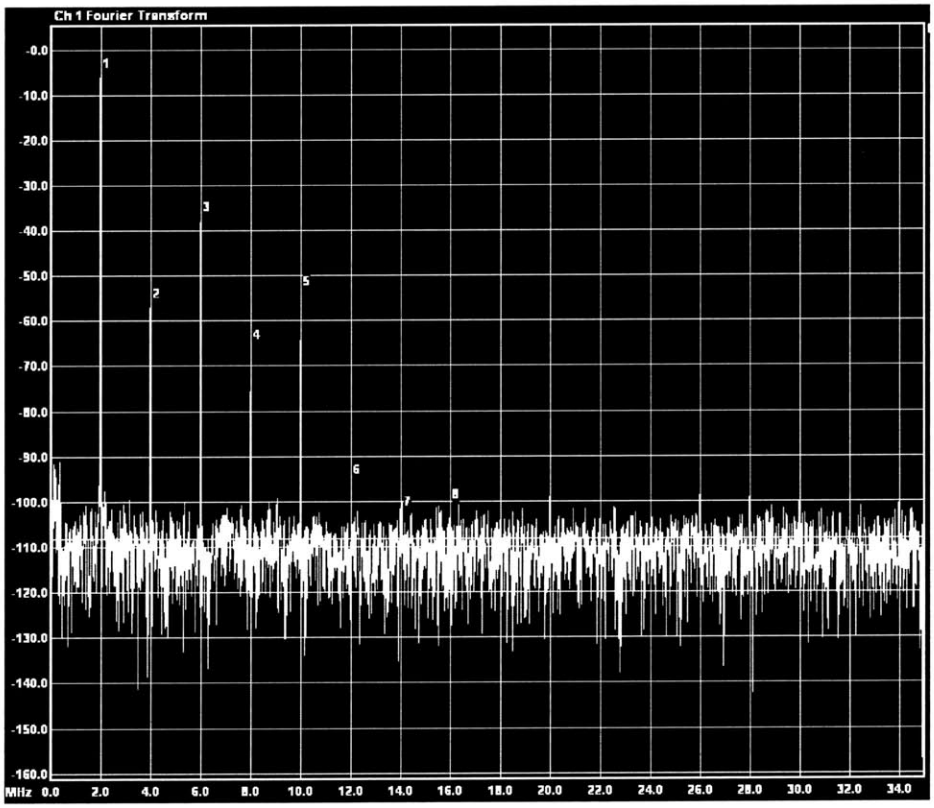


Figure 4-2: Input Overdrive System.

with the same clock source. Any oscillator fluctuation (in time or frequency) will at least be from the same source. The only difference between the two clock signals is the relative phase difference seen at the ADC, since one clock signal is at the front of the signal chain, and one clock signal samples the ADC. Jitter and random phase fluctuations should be cancelled out using the same clock source. Using the same frequency for LO and f_s in the upconversion scheme will make carrier feedthrough look as a DC offset, eliminating it from the AC spectrum.

Figure 4-3 illustrates the effects of two 70MHz clock sources used for f_s and LO, with a 2MHz input into the system. The noise floor is elevated considerably due to oscillator phase noise.

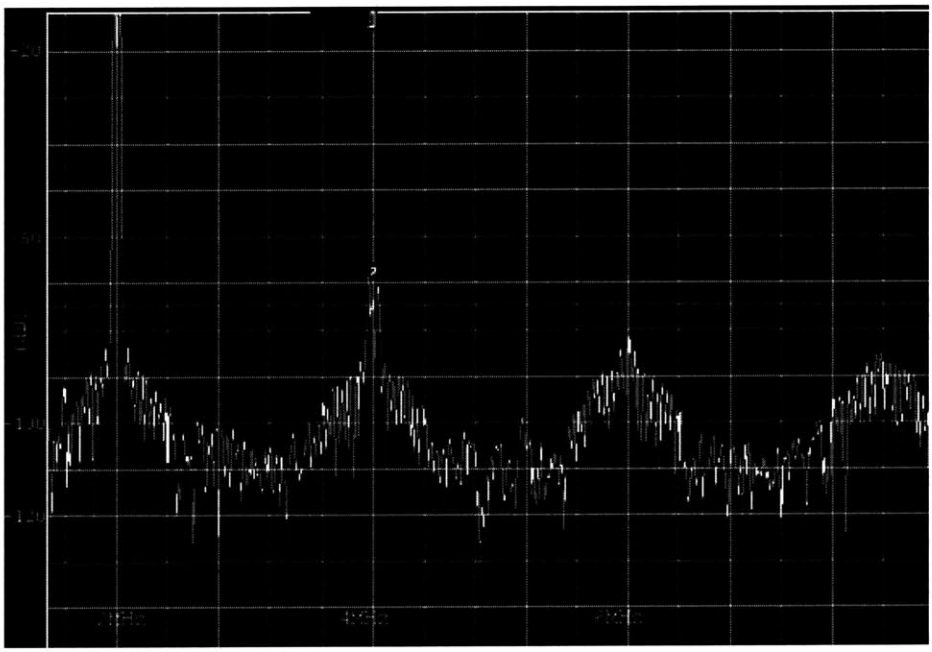


Figure 4-3: Separate Clock Sources for ADC and Mixer.

The work presented here assumes the same clock source unless otherwise indicated.

4.3 Reflected Waves

In higher frequency applications, reflections can affect the system output quality. The measurements used to determine the quality of the system in minimizing reflections are the S parameters, namely the S11 and S22 return loss parameters. Thus, it is

important to look at these parameters of each device in the signal chain. The AH31 amplifiers report S11 = S22 = -25dB and the LC bandpass filter has S11 = S22 = -16dB, which indicate there is sufficient attenuation of reflected waves. However, the SAWTEK filters do not have good S11 and S22 parameters. The data in the Figures 4-4, 4-5, and Tables 4.1 and 4.2 are from published online data from the vendor[2]. In the 5MHz bandwidth SAW, the S22 parameter in the passband is only 7-10dB attenuation. In the 20MHz bandwidth SAW, the S11 and S22 parameters are poor at about 3-5dB attenuation.

In a cascade system as in the presented application, reflected waves can compound on one another, adding undesirable signal level to the output and distorting the digitized signal. These reflections will degrade the SINAD and SFDR figures. In the case that the reflected wave is at the same frequency and phase as the incoming wave, a standing wave forms.

It was advantageous in the setup to place attenuator pads in between stages where reflections can degrade the output. Thus the mixer output, SAW input, and SAW output were all buffered by attenuator pads of 1dB to 5dB.

Freq (MHz)	S11 (dB)	S21 (dB)	S22 (dB)
65	-1.398	-58.811	-1.017
66	-2.784	-27.081	-1.299
67	-6.806	-11.631	-3.674
68	-10.530	-7.585	-7.310
69	-15.131	-7.002	-7.533
70	-16.826	-7.053	-8.945
71	-15.049	-7.036	-9.584
72	-8.065	-7.508	-8.192
73	-5.467	-13.597	-4.261

Table 4.1: SAWTEK 854660 S Parameters

[2]http://www.triquint.com/prodserv/types/filters/if/std_70mhz_family.cfm

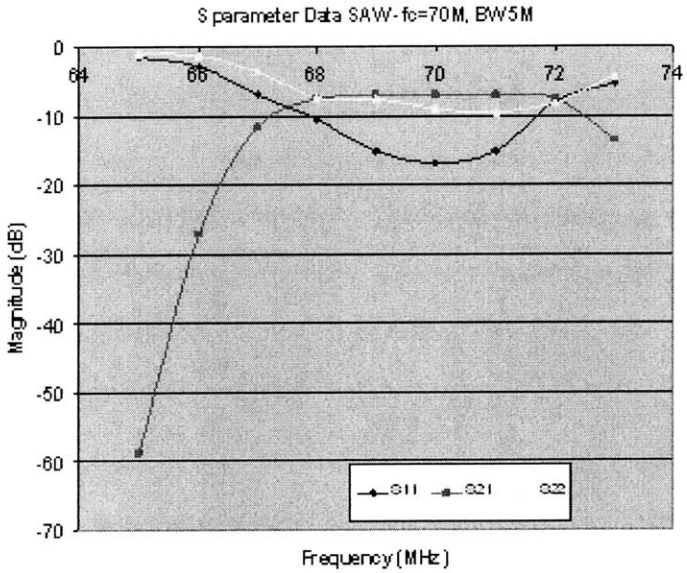


Figure 4-4: S parameter Data from SAW Filter Part 854660.

Freq (MHz)	S11 (dB)	S21 (dB)	S22 (dB)
60	-3.327	-15.791	-3.102
61	-3.728	-14.334	-3.363
62	-3.669	-14.176	-3.317
63	-3.614	-14.161	-3.323
64	-3.834	-14.237	-3.424
65	-4.095	-14.069	-3.625
66	-4.138	-14.040	-3.669
67	-3.945	-14.008	-3.581
68	-4.156	-13.991	-3.664
69	-4.302	-13.998	-3.834
70	-4.418	-14.061	-3.959
71	-4.112	-14.094	-3.757
72	-4.088	-14.051	-3.630
73	-4.428	-14.123	-3.863
74	-4.556	-14.052	-4.057
75	-4.268	-13.984	-3.796
76	-4.155	-14.040	-3.658
77	-4.256	-14.126	-3.710
78	-4.732	-13.837	-4.247
79	-4.570	-13.954	-4.181
80	-3.531	-16.773	-3.181

Table 4.2: SAWTEK 854670 S Parameters

4.4 Single Sideband v. Double Sideband

Mixers translate frequencies to signals at the sum and difference of the two input frequencies (IN and LO). One of these frequencies is the desired sideband, the other is the image sideband. In some cases the sidebands contain different information, but in most cases the desired and image sidebands represent identical information [17]. Thus only one band is necessary, and the signal is filtered as a single sideband (SSB). If both sidebands are needed, double sideband (DSB) filtering is necessary in the signal chain.

SSB and DSB offer different advantages. SSB filters are much more narrowband (they need only be half the bandwidth of a DSB filter) and can be more complex to design. SSB filters can be designed to filter out the mixer carrier frequency, making the system insensitive to LO feedthrough. As discovered in Chapter 4, the local oscillator feedthrough can be a limiting factor in system performance. Feedthrough contributes to a DC offset if the same clock source is used for sampling and upconversion. In DSB, the carrier frequency appears at the output so LO feedthrough becomes a factor. Mixer design, mainly port isolation and balanced network, is cru-

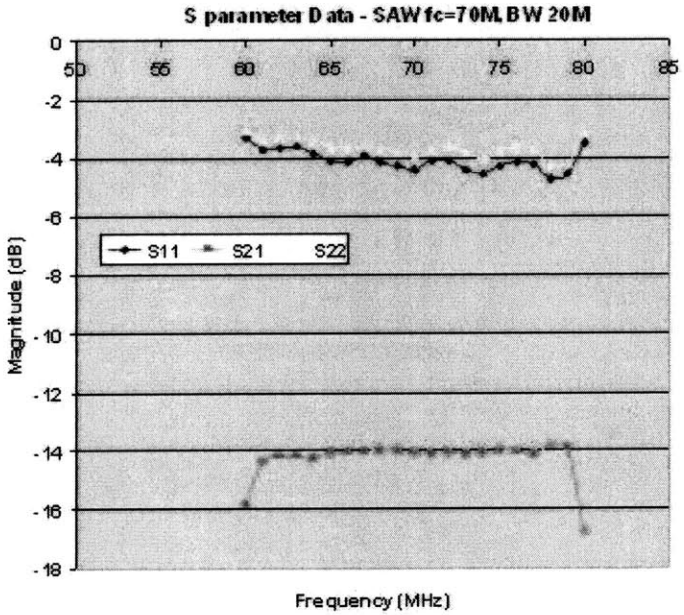


Figure 4-5: S parameter Data from SAW Filter Part 854670.

cial in DSB. Given the same input level in the system, the DSB setup should have a higher SNR and a better noise figure (NF). In DSB, there is twice as much signal, and a $\sqrt{2}$ increase in noise. Noise is measured in RMS and hence does not double like the signal level. A 2x increase is a 6dB gain and a $\sqrt{2}$ increase is a 3dB gain. Thus, the SNR increases by 3dB. With a higher SNR, the noise floor is lower and therefore the noise figure should improve with DSB. These metrics for dynamic performance will be presented in the following section and values for SSB and DSB will both be shown.

4.4.1 Phase Delay Offset

Another difference in SSB and DSB is how they are affected by a timing delay. In DSB, there are two sidebands to consider in the frequency spectrum, which means the time version of this is a signal (i.e. $\cos([\omega_i+\omega_c]t)$) that is modulated by the second (i.e. $\cos([\omega_i-\omega_c]t)$) frequency. Because of the modulation, phase delay becomes significant in sampling time. The system has two clocks traveling different signal path lengths the sampling clock directly to the ADC and the upconversion clock that has to travel the entire signal chain from mixer through amplifiers and filters all the way to the ADC input. Therefore it is important, when looking at double sideband, to ensure that the timing is such that the ADC clock is sampling at the peaks of the modulated analog input signal. Otherwise, it is possible to be sampling near the zero-crossing of the signal. The ADC would falsely output as a very low level signal even if the system is working properly, except for the timing of the clocks.

A SSB scenario has just one sideband, which is the transform of a sinusoid. When the signal is sampled, phase offset is trivial because the signal is not being modulated by another frequency[3].

Thus in the application setup, the length of the signal chain was adjusted so that proper DSB sampling could take place. This involved exchanging BNC cables of different lengths in the middle of the chain. Either the ADC sampling clock could

[3]This of course assumes that interfering signals are heavily attenuated in the signal, otherwise they are a source for modulation.

be delayed, or the signal chain can be lengthened so that the clock would sample at the next peak maxima. In a more realistic applications setting, this can be more of a nuisance than anything, so SSB may be heavily preferred over DSB. With SSB timing delay becomes a nonissue.

4.5 System Gain

Without variable components, the net system gain ranges from 15 to 23 dB. The measured gains of each component in the signal chain is listed in Table 4.3.

Part	Gain or Insertion Loss (dB)	Bandwidth
Input filters (TTE)	-3.4	Narrowband bandpass, input-frequency dependent
Butterworth Bandpass filter	-1.3	Fc=70MHz, BW=30MHz
SAW (1)	-7.25	Fc=70MHz, BW=5MHz
SAW (2)	-14.5	Fc=70MHz, BW=20MHz
AH31 (1)	+18.5	BW 44-90MHz
AH31 (2)	+19.1	BW 44-90MHz

Table 4.3: Gain and Bandwidth Values for Each Component

Throughout the system, the attenuator pads used to reduce reflections and standing waves, described in Section 4.3, sum to 6dB. Using the narrowband SAW(1) the system gain is 23dB. With the wideband SAW(2) the system gain is 15.8dB[4].

With the wideband 20MHz SAW filter care must be taken, as described in Section 4.1, not to just overdrive the system to achieve full scale. A step attenuator can be used to compensate for the 7dB difference in the insertion loss of the two SAW filters. From Section 4.4, the narrowband SAW(1) can be used for SSB filtering and the wider SAW(2) can be used for DSB filtering. To ensure consistency in testing, the same input level is configured for both tests. That level is set with the signal chain for DSB to achieve full scale output. Since the narrowband SAW(2) has a lower insertion loss,

[4]The gain of the system is defined from the filtered input, so the insertion loss of the filter is accounted for in the input level, not in the system gain. The filter is a test setup requirement, but in a real system, it is assumed that the input is well-filtered and a relatively clean signal.

a step attenuator can be used to lower the gain in the SSB chain to achieve full scale output while maintaining the same input power.

One thing to take note here is that adding PIN diodes in the system only decreases the system gain. They cannot increase the gain of the system because of the way they are implemented into the system design. PIN diodes are acting virtually as shunting resistors with increasing current bias. The maximum gain achievable for this upconversion scheme is with either no PIN diodes or reverse-biased PIN diodes.

Chapter 5

Dynamic Performance Results

The heart of this application is looking at the dynamic performance of the entire system. If the system can achieve high dynamic range without requiring the absolute top of the line components, this indicates the robustness of the application. The current application setup allows customers to determine the gain blocks of the system based on the components available at hand, the upconverting frequency, the sampling rate, and allows design room for sharp filtering for improved dynamic range. The dynamic figures of interest are Signal-to-Noise Ratio (SNR), Signal-to-Noise-and-Distortion Ratio (SINAD), Spurious-Free-Dynamic-Range (SFDR) of the entire signal chain (and ADC) as well as harmonic distortion, noise figure (NF), and output third-order intercept point (IP3).

5.1 SNR, SINAD, SFDR

The SNR of the system was generally found to be about 69-71dBFS. Different bandwidth SAW filters provided slightly varying figures, clearly the narrowband 5MHz SAW produced a higher SNR. Also, the SSB and DSB setup provided different SNR values, as anticipated in the discussion in Section 5.3. It was expected that the DSB SNR would be 3dB higher, it was found to be 1-2dB higher in most setups. Given the realistic setup on the lab bench, this is as expected. The dominant harmonics tend to be the second and third harmonics, but SINAD is typically about 62dBc and SFDR

63dBc. The system SNR comes close to the ADC LTC2249 SNR of 73dBFS, the upper limit of the expected system SNR. This suggests the method to be a low noise application, as observed with a 108dB noise floor with an 8192-point FFT. However, the SINAD and SFDR figures indicate that there is distortion in the system setup. The narrowband 5MHz SAW filter keeps higher order harmonics out, so the source of distortion lies in the components in the signal chain. Most likely the distortion arises from the mixer or amplifiers rather than the filters.

Tests were performed to look at the effects of the mixer distortion and amplifier distortion separately. In Figure 5-1 Test 1 has an IF input at 70MHz, processed through the signal chain and sampled by a 74MHz clock. Test 1 has a SNR of 69.2dBc and SINAD 67.2dBc at full scale output. Test 2 has a low frequency 4MHz input, mixed up to 74MHz, processed through the same signal chain and sampled by the same 74MHz clock. Test 2 has a SNR of 67.6dBc, and SINAD 64.8dBc.

Figure 5-1: System Distortion With and Without Mixer.
Test 1: IF input, without mixer. Test 2: LF input, with mixer.

Looking at this test, it was interesting to note that the mixer did not actually degrade the SNR or SINAD by more than a few dB. The mixer definitely contributes some noise and distortion into the signal chain, but does not seem to be the dominant factor. Therefore, the attention was shifted to the AH31 amplifiers.

If the AH31 amplifiers have poor distortion, the second AH31 which is right at the ADC input, will have the most pronounced effect at the output. The previous amplifier in the chain is followed by a narrowband SAW filter, which bandwidth limits the amplifier output.

In Figure 5-1 Test 1 has a filter in between the amplifier and ADC input network. If the order of the two parts were swapped, would the distortion change?

In Figure 5-2, a comparison was made between the order of a LC bandpass filter and AH31 amplifier in the input signal chain to the ADC. Test 1 with a cascade

of AH31-bandpass filter provides SNR = 70dBc and SINAD = 67dBc. Test 2 gives SNR=70dBc and SINAD=55dBc! Therefore, there is a large level of distortion of the AH31 when placed right before the ADC. The AH31 was designed for a bandwidth of 45MHz to 90MHz. This is greater than the Nyquist bandwidth of 35MHz, suggesting that the distortion folds back into the Nyquist zone.

The AH31 amplifiers were selected as off-the-shelf sufficient amplifiers. They are cheap and have fairly low distortion. From the two tests, it is simple to see that placing a filter after the AH31 and before the ADC will improve the SINAD and SFDR values. As long as the AH31 distortion does not affect the more realistic intermodulation test, these amplifiers are still useful components for this application.

5.1.1 SSB v. DSB

Let us compare now the difference between the figures for DSB and SSB. Comparing the two schemes is challenging, because it is hard to determine what the most equal test between the two is. The main difference in the DSB and SSB is the ease of filtering achievable. So most applications of DSB have a wider range filter than SSB. However that changes the signal gain of the post-mixer chain because the two options available are the 5MHz SAW (for SSB) and 20MHz SAW (for DSB). The other factor to consider when looking at SNR and SINAD values is the input power level. With DSB allowing both sidebands for twice the input level than in SSB, it is easy to overdrive the input in DSB. Setting the system up as described in Section 4.4 allows for a fair comparison of SSB and DSB filtering, with equal input levels an an attenuator to adjust post-mixer gain.

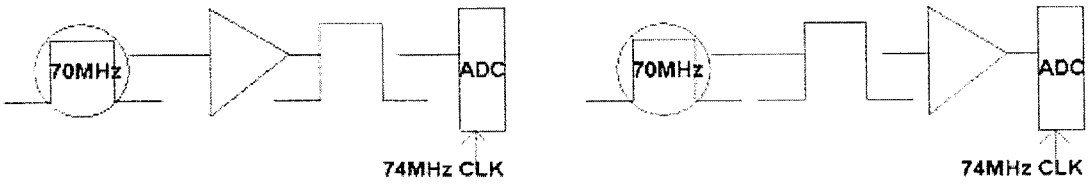


Figure 5-2: ADC Input Distortion. Having the amplifier output post-filtered improves the dynamic results.

The expected difference between SSB and DSB SNR is 3dB, as discussed previously. In the setups discussed, it was very hard to achieve a comparison where the DSB SNR is actually close to 3dB higher. The results of a DSB v. SSB test are depicted in Table 5.1:

Parameter	SSB	DSB
f_s	74MHz	70MHz
Input f	4MHz	4MHz
SAW, f_c=70MHz	5MHz BW	20MHz BW
SNR (with F1=-1dBFS)	66.7dBc	69.7dBc

Table 5.1: Double Side Band and Single Side Band Results.

5.1.2 PIN Diode Dynamic Performance

Now the attention focuses on the dynamic performance of the upconversion scheme with the PIN diodes. After all, the purpose of upconversion is to provide variable gain and filtering. It is important to measure the dynamic performance of the system with the PIN diodes in place.

With the same input level, the output amplitude dropped from full scale -1dBFS to -24dBFS at a 1V bias voltage on the PIN diodes (refer to Table 5.2). This verifies the amplitude has about 25dB gain range. The S11 parameter of the mixer with PIN diodes shows the effect of the varying output impedance matched to the 50Ω transmission line. The measurements were made with the network analyzer with 50Ω matching. In essence, the PIN diodes lower the 50Ω impedance, so that the attenuation observed at the output is due to impedance mismatch.

It is desirable to see that the SNR, SINAD, and SFDR values do not change considerably with the addition of the variable PIN diodes. In the shunt resistor configuration of the PIN diodes, it is possible that some distortion may arise. However, a comparison of SNR and SINAD values in a system with and without PIN diodes showed no change in SNR and less than 1dB change in SINAD, indicating that the distortion from PIN diodes is almost negligible.

In Ultrasound, it is possible that the gain must be adjusted depending on the input level to achieve full scale. Full scale output is desirable. To mimic the application, the PIN diodes were biased at 0.5V intervals across the gain range, and the input level was adjusted accordingly to achieve full scale at the ADC. The SFDR and SINAD values stayed consistent at 73dBFS. The SNR dropped 4dB when the PIN diode became forward biased.

5.2 Noise Figure (NF)

To validate this application of frequency translation, it is important to verify that the noise figure is acceptable. Because a mixer (which usually has a relatively poor noise figure) is in the system chain, the noise figure is not expected to be as good as a single chip VGA. Two methods of noise figure calculations were done, first with Friss' equation and second with the SNR and Gain calculation.

We are looking at noise figure, seen at the input of the system. A cascade system has an overall noise figure determined by the equation :

$$NF = F1 + \sum_{i \neq 1} \frac{F_i - 1}{\prod_{j<i} G_j}, \; where \tag{5.1}$$

F1 = First stage noise figure,

$F_i = i^{th}$ stage noise figure, and $G_j = j^{th}$ stage noise figure.

V_{bias}V	Attenuation (dB)	Return Loss S11 (dB)
5.0	-1	-18.2
4.5	-1	-13.4
4.0	-1	-2.77
3.5	-1.2	-1.83
3.0	-11	-1.41
2.5	-18	-1.30
2.0	-21.3	-1.17
1.5	-23.2	negl.
1.0	-24.47	negl.

Table 5.2: PIN Diode Attenuation and Return Loss.

As seen in Equation 5.1 the first component in the system contributes the most to the noise figure when we assume the system provides overall gain not attenuation. Here, the first component, the mixer, with the worst noise figure is expected to degrade the noise figure the most.

The table shows the noise figures and gains of each component in the system, as specified by their datasheets.

Stage	Gain (dB)	Noise (dB)
Mixer LT5521	-0.5	12.5
Bandpass Filter	-1.3	1.3
Amplifier AH31	+18.5	2.4
Amplifier AH31	+19.1	2.4
SAW filter, 5MHz	-7.5	Negligible
SAW filter, 20MHz	-14.5	Negligible

Table 5.3: Individual Stage Gain and Noise Figures.

Single sideband setup gives NF=13.02 dBFS. Double sideband setup gives NF=13.34dBFS. The difference arises from using different SAW filters for SSB And DSB.

From PScope, the noise figure can be extracted from the gain and SNR values. The relationship is shown in Figure 5-3.

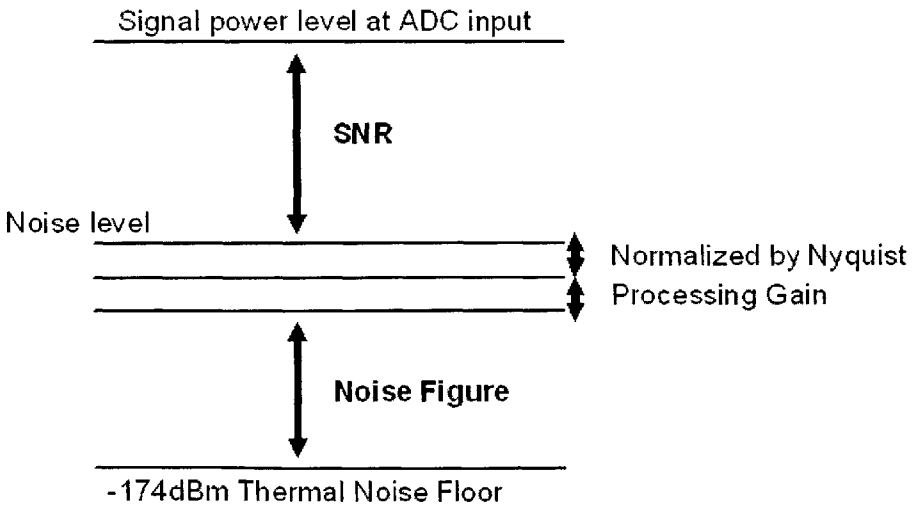


Figure 5-3: Noise Figure.

The equation is as such for a system with filter bandwidth $B < \frac{f_s}{2}$ (Nyquist):

$$NF_{out}(dB) = S_{out} - SNR - NTH - 10\log\frac{f_s}{2} - 10\log\frac{\frac{f_s}{2}}{BW} \tag{5.2}$$

$$NF_{in}(dB) = NF_{out} - Gain. \tag{5.3}$$

S_{out} = signal power level.

NTH = Thermal noise floor.

Processing Gain is $10\log\frac{\frac{f_s}{2}}{BW}$.

Nyquist Normalization is $10\log\frac{f_s}{2}$.

Essentially, the noise floor of the system is calculated, given the SNR and the output signal level. The normalization to Nyquist limits the spectrum to the Nyquist zone, or $\frac{f_s}{2}$. The processing gain scales the noise figure to the bandwidth of interest by further limiting the system to the input bandwidth, when it is less than Nyquist. In a system where the signal is bandlimited to be within Nyquist but has no additional filtering, the processing gain term is not needed. Then the difference between the noise level and the ideal -174dBm noise floor derived from ktB is the calculated noise figure of the system.

For single sideband 4MHz input upconverted to and sampled at 74MHz, the SNR was calculated to be 70dBFS, with a gain of 15. The ADC input was measured at 9.4dBm (ideally 10dBm, but slight loss to input transformer network). The noise figure at the output was 29dB, at the input (NF_{out} - Gain) was 14dB. This is comparable to the 13dB found by the cascaded gain system. The system used the 5MHz bandwidth SAW to allow for single sideband filtering, and thus the processing gain was $10\log\frac{\frac{74M}{2}}{5M}$.

5.2.1 Sources of Noise

From the equation, it is easy to see that the first component, the mixer, should be the dominant factor in the noise figure calculations. To verify whether or not this is true in the system, the mixer was replaced by a signal-generator IF frequency signal (at

the upconverted frequency). To minimize noise from the generator, a step attenuator was used, followed by a narrowband filter to block harmonics. The SNR increased by 5dB, therefore the noise figure improved by 5dB. In the Friss equation with the mixer taken out of the signal chain, the noise figure drops to 6.4dB in a single sideband system (including a -6dB loss from the step attenuator). It is important to note that the mixer plays a significant role in degrading the noise figure of the overall system. Although the amplifiers contribute noise to the system, they are very far down the signal chain. Looking at the equation, the noise figure of each component is divided by the preceding gain. Hence the overall input-referred noise figure is dominated by the mixer.

5.3 Intermodulation Test (IMD)

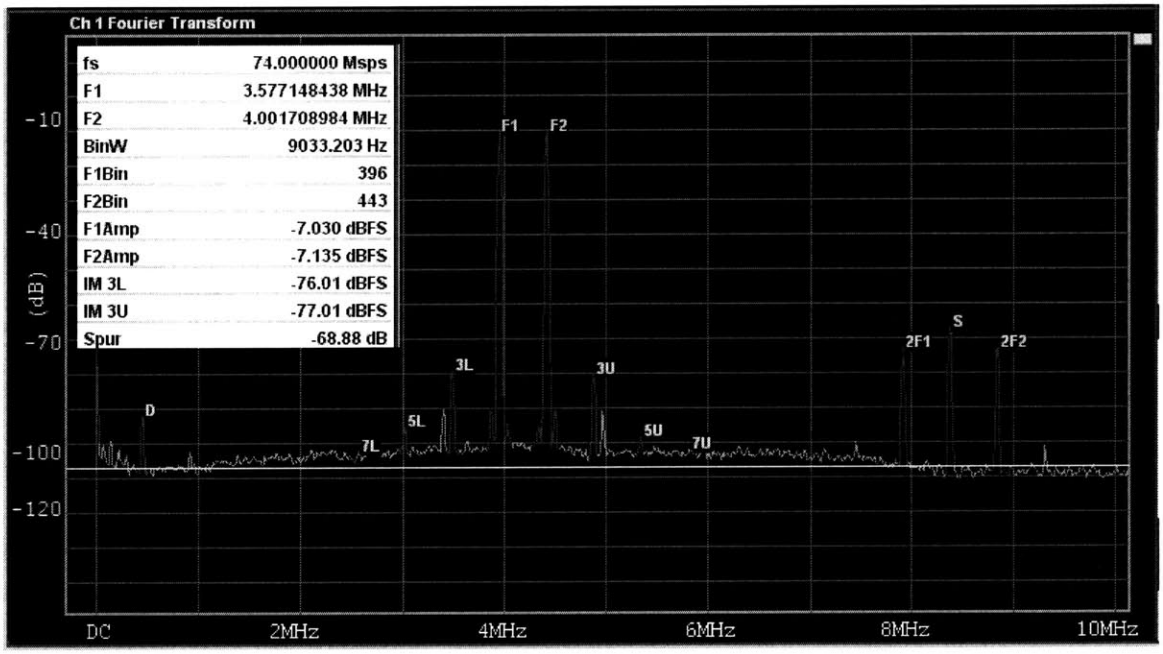


Figure 5-4: Intermodulation Test
Input signals $f_{in1} = 3.58MHz$ *and* $f_{in2} = 4MHz$, Sampling frequency 74MHz.

One of the more realistic methods of characterizing the system is to perform an intermodulation distortion test (IMD). By combining two close-in-frequency signals at the input of the system, this test shows how good the system is at rejecting interfering

signals. This measurement is extremely important in the case of ultrasound, because interfering signals arise close in frequency to the signal and require a high dynamic performing system to process the signal accurately. With a 3.58MHz and 4MHz signal in the ultrasound range, mixed up by a 74MHz clock and sampled with the same clock, 77dB was achieved for attenuation of the third order intermod signal, results in Figure 5-4. The third order IMD is a convenient measurement because it requires just two test signals, and can be set up so that the third order products are within the passband.

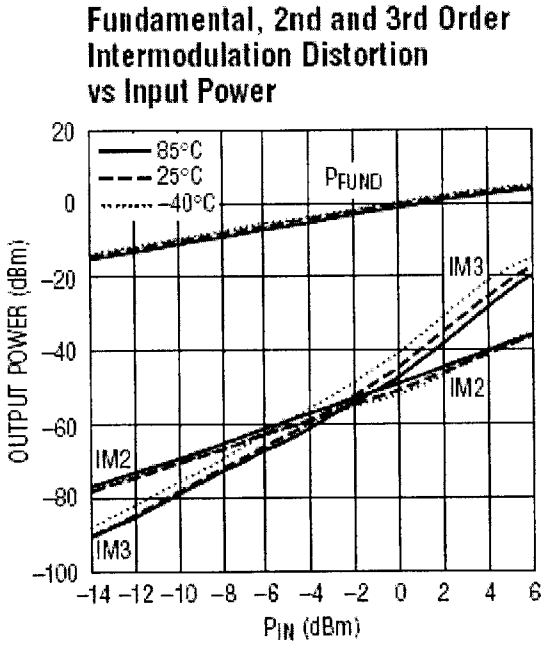


Figure 5-5: LT5521 Mixer Linearity. From Datasheet.

For linearity of the system, it is important to look at how the output fundamental and third order products change in response to input power levels. The LT5521 mixer has high linearity, given by Figure 5-5. The third order IMD gives the hypothetical OIP3 (output third order intercept point) of the system. This value gives the output power at which the third intermod signal equals the fundamental signal level. For every dB change in the fundamental, the third IMD changes by 3dB. It is hypothetical because the system would be saturated before the OIP3 point can be reached. Sweeping the input power of the system (both input signal levels were

stepped synchronously), the output F1 and IM3 amplitudes were plotted in Figure 5-6. Here, the linear portions of the plots were fitted to a line and the intersection of the two extrapolated lines gives the OIP3 point. In this test, OIP3 was found to be 44.2dBFS.

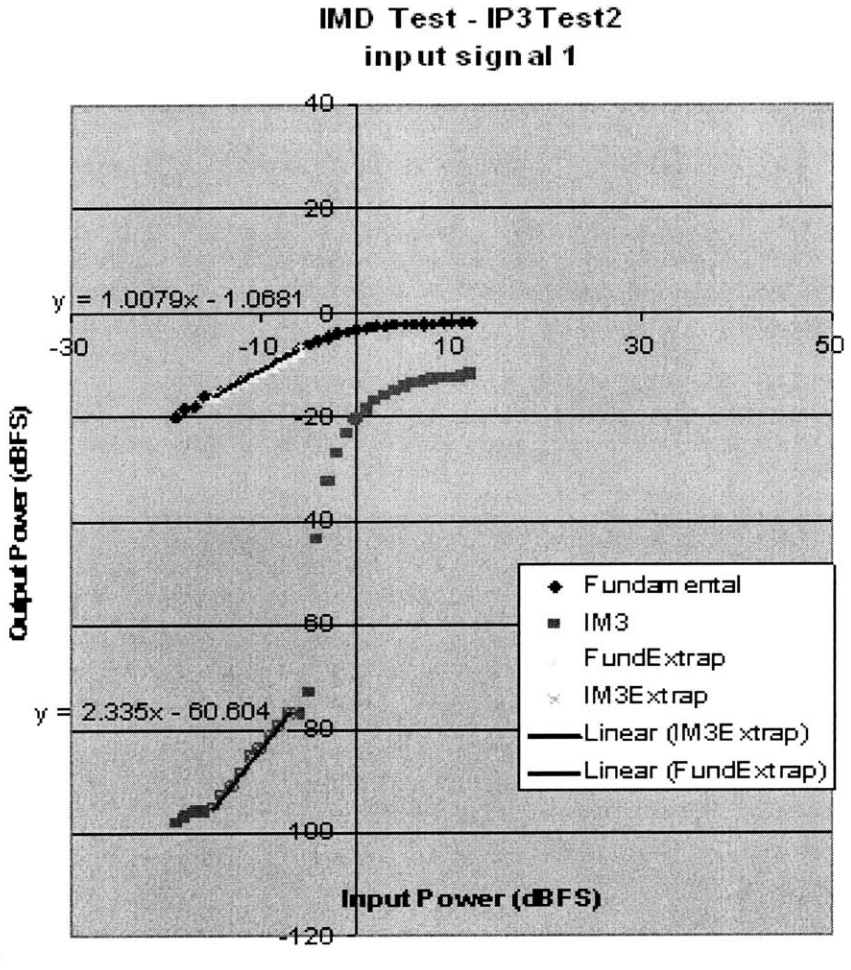


Figure 5-6: IP3 Extrapolation from Intermodulation Test.

Where is the IMD coming from?

The IMD test is performed routinely on mixers, so the LT5521 datasheet specs for +24dBFS IP3 point. This is of course, under a specific set of test parameters, but this value was used as the basic benchmark value. With a gain of 20dB post-mixer, the IP3 level is 44dBFS, which matches the extrapolated OIP3 value.

If the IP3 point and the intermodulation distortion is truly limited by the mixer, then a measurement of the IP3 of the system without the mixer would indicate such.

As in the single tone distortion test, the mixer was taken out of the equation. Two helically-filtered signals (from the signal generator) at 71MHz and 72MHz were inputs to the pre-ADC IF signal chain. The IMD test was carried out with these input signals. The results of this test showed slight improvement in IM3 values (77-80dBFS) and an IP3 improvement to 48dB. This seems to indciate that the mixer degrades the IP3 by 3dB.

However, it is highly possible that the IP3 improvement was masked by the IP3 value of the AH31 amplifier at the end of the signal chain (before the ADC). The typical datasheet OIP3 value for the AH31 is +42dBm, measured with two tones at 10dBm output power separated by 1MHz [9]. The measurements taken are already slightly higher than the typical value for the AH31. Because of the +20dB gain following the mixer, it is possible that the IP3 value of 48dB without the mixer does not really show how much the mixer actually degrades the IP3 value. In this application, it seems that the amplifier is partially responsible for limiting the IP3 value of the system. Fortunately, the system has good intermodulation distortion and attenuation of intermod products. The mixer and the amplifier both contribute to IP3 and intermod products, but the overall application is sufficient for ultrasound requirements.

Chapter 6

Conclusion

6.1 Summary

After a careful analysis of the frequency translation system designed for continuously variable gain and filtering, the performance was found to be desirable and definitely a possibility for the future of high-end ultrasound applications. With a continuous gain range up to 25dB and a 25MHz range of filtering capabilities, the upconversion scheme is palatable for ultrasound. This application is fairly straightforward to put together, and results of over 70dBFS SNR, more than 75dBFS IM3, and 44dB IP3 were achieved.

6.2 Future Work

The integration of the upconversion scheme into a working ultrasound application is challenging as is. However extensions of this thesis work can incorporate more design considerations into the application system. The following highlights possible future work.

There is no limitation in terms of sample rate and clock speed. It is possible to upconvert to a frequency higher than 70MHz, and continue sampling with the same clock source. The upper limit lies in the ADCs, with Linear's parts sampling at or more than 250MSPS.

One of the performance-limiting parts was the LT5521 mixer. Although a great part at high frequencies, it has drawbacks at 70MHz. Naturally, upconversion to higher frequencies can improve the mixer noise and distortion performance. If 70MHz is the desired translation frequency, it is possible to redesign the Gilbert-cell based mixer to improve its dynamic performance.

PIN diodes provide more than 25dB attenuation range across a bias voltage of 5V. However, the gain drops in a third-order polynomial form. It is possible to program the system to provide linear-in-dB gain control using PIN diodes to improve the user interface with the system.

There is also the option of making a module for this product. The idea of making a module out of this entire application system was discussed extensively throughout my thesis work. There are advantages and disadvantages to doing it. In the setup I have configured for my thesis work, there is sensitivity to noise and oscillation. Laying it out on a board or module will eliminate much of the ancilliary issues. However, it is important to consider the time and cost of such a project. The intended market, primarily the high-end ultrasound consumers, may not include the rapidly expanding medical ultrasound industry. In this case, it may not be economically viable to invest resources for fabricating the module. Additional market research should be done to better understand the demand for such integrated boards and/or modules for the upconversion scheme.

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