Monolithic Low Phase Noise Oscillators for Moderate Frequency Applications

by

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ABSTRACT

Low noise oscillators are critical building blocks in a wide range of commercial electronics. Increased levels of integration have created a strong need for integrated oscillator solutions despite generally inferior noise performance. The development of non-linear noise models that can accurately and efficiently predict noise in ring oscillators aids designers in optimizing noise performance in integrated oscillator solutions. Extending a piecewise constant model of noise in an oscillator and the resulting timing jitter reveals how the noise at the oscillator nodes changes during each portion of the cycle. The model can then be used to examine the effects of changing various process and design parameters such as threshold voltages and the effective stage gain. This analysis tool provides a means for designers to evaluate potential improvements of their oscillator design. In some cases approximate analytic solutions can be found that provide better insight into the timing jitter. A simple differential oscillator design illustrates the use of this analysis. The oscillator achieves an analog tuning range of 259MHz-314MHz (extendable with switched capacitors) with a normalized jitter of 102ppm.

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Chapter 1

Motivation

1.1 Introduction:

Oscillators have become an increasingly important part of a great variety of modern electronic systems, ranging from power converters to data converters to wireless and wired communication systems. In some cases, such as power converters, the performance specifications required of the oscillator are minimal and much greater emphasis is placed on features such as duty cycle control. However, in many other systems the stability and noise performance of a local oscillator can be critical to the correct operation of the circuit. With the rapid advances in the scaling of size and speed in digital circuitry, there is increased pressure placed on the capabilities of the surrounding analog circuitry as it becomes the primary bottleneck to the performance of the entire system.

The purpose of this work is to investigate the consequences of noise in integrated oscillators in various systems and find ways to improve the noise characteristics while minimizing power consumption and die area. Noise in an oscillator is typically categorized into one of three general types; amplitude noise, phase noise, and timing jitter [1]. Amplitude noise, which represents the change in the output signal's amplitude, will

not be examined in great detail in this work since the focus here is integrated ring oscillators that have heavily non-linear gain[1] and typically clip the output to one supply rail or the other. In addition, many of the electronic systems to be discussed shortly do not depend on the amplitude of the oscillator signal, with the exception of some communication systems.

The category phase noise refers to the widening of the oscillator's power spectral density in the frequency domain. Ideally the oscillator's spectrum would be a perfect impulse at its natural frequency; however the presence of phase noise causes it to have side skirts that fan out underneath it [2]. The impact of this spectral widening is particularly noticeable in communication systems, and will be discussed in the next section. The category timing jitter, on the other hand, refers to the variation of the oscillator's period. While the terms "phase noise" and "timing jitter" fundamentally represent the same noise process, distinguishing between the two aids in the analysis of frequency domain and time domain problems respectively. Timing jitter can have a large impact on the accuracy of data conversion systems, as well as the performance of large digital systems.

1.2 Communication Systems:

Phase noise performance is critical in modern communication systems where bandwidth is precious and communication channels are very tightly spaced. The increasing need for faster data transfer is forcing the use of complicated modulation

[1] The non-linear gain of most oscillators limits the output to only one stable amplitude, causing injected amplitude noise to decay quickly, although there are cases where for instance the amplitude may be set by a noisy bias current.

schemes to glean every last bit of data throughput for a given channel bandwidth. Phase noise in the local oscillator limits both the complexity of data modulation and the tightness of channel spacing [3]. In wireless communication systems base-band information is modulated up to a high frequency and transmitted through the air to a receiver some distance away. During both transmit and receive portions of the data transfer the signal is multiplied by the local oscillator, which represents a convolution of the two signals' spectra in the frequency domain. If the local oscillator is a perfect impulse in the frequency domain, then the data signal is effectively just shifted in frequency up to the carrier frequency. The presence of phase noise, however, causes distortion in the modulated signal due to the side skirts modulating the data signal in addition to the main carrier. The end result is a limit to the signal to noise ratio (SNR) of the system. Since the channel bandwidth is often set by FCC rules or some other agency out of the designer's control, the only way to send more data through the same channel is by increasing the resolution of the symbol constellation [4], however increasing the resolution beyond the limits imposed by the SNR provides no benefit as additional bits would be indistinguishable from random noise. Hence there is a limit to the effective number of bits that can be transferred at a time, which is in part set by the phase noise performance of the local oscillator.

Oscillator phase noise not only limits the SNR of the isolated channel, but also limits the spacing of channels due to inter-modulation of nearby carriers. Consider for a moment a person using a cellular phone, trying to receive a signal from a cell tower a mile away. In principle this might not be a problem as long as the tower transmits enough power and the phone has a sensitive enough receiver. Now consider that there may be

another cell tower only 10 meters away transmitting power in the adjacent channel. The signal power of the adjacent channel may be several orders of magnitude greater than the available power of the desired signal. This presents a problem when the adjacent channel is modulated by the phase noise skirts into the base-band as shown in figure 1.1.

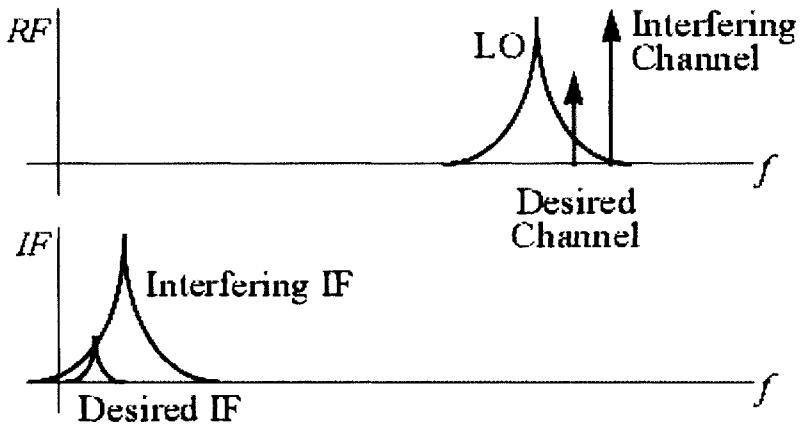

Figure 1 . 1 - Illustration of reciprocal mixing of nearby interferer with noisy oscillator [5]

The relative magnitudes in this figure are somewhat exaggerated as the phase noise power should be much smaller than the fundamental carrier power, but the disparity in signal strengths causes their product to be much closer to the received signal level, in effect lowering the available SNR again. Because of this interaction there is a limit to how closely channels can be spaced without causing degradation of the data transfer, or conversely for a given channel spacing, the oscillator phase noise limits the selectivity of the receiver in a signal rich environment.

Oscillator stability, in terms of both long term drift and short term phase noise, has become a critical limitation to the performance of narrowband communication systems. Excess phase noise can quickly reduce the total SNR and consequently the achievable data throughput. Phase locked loops (PLLs) can mitigate the problem

somewhat, but only within the bandwidth of the PLL, and ultimately a stable reference is still required for the PLL to lock on to.

1.3 Data Converters:

When considering the performance of data converter systems, it is often more convenient to represent oscillator noise as timing jitter due to the digital nature of A/D and D/A conversion. The ability to convert between digital and analog signals is predicated on the presence of a fixed timing reference at which the sampling / outputting occurs. Uncertainty in the sampling time can cause a number of subtle problems including aliasing, and distortion that is both frequency dependent and time varying [3]. Aliasing can occur if the input is not tightly band limited to less than one half the sampling frequency for Nyquist-rate converters, and variation in the sampling frequency lowers the bandwidth of the converter. The maximum bandwidth is set by the jitter in the oscillator and the minimum SNR the converter needs to maintain accuracy over its full resolution, since signals aliased by the phase noise will be small compared to the signal.

In addition to potential aliasing problems, there will be conversion errors due to the variation in the sampling time for any AC signals. For a voltage that is changing in time, a change in the sampling instant Δt, will result in a small change in the sampled voltage Δv, which in the limit of small jitter relative to the clock period (and hence signal frequency) the voltage error is approximately $\Delta v = \Delta t \cdot \frac{d}{dt} v$, illustrated here in figure 1.2:

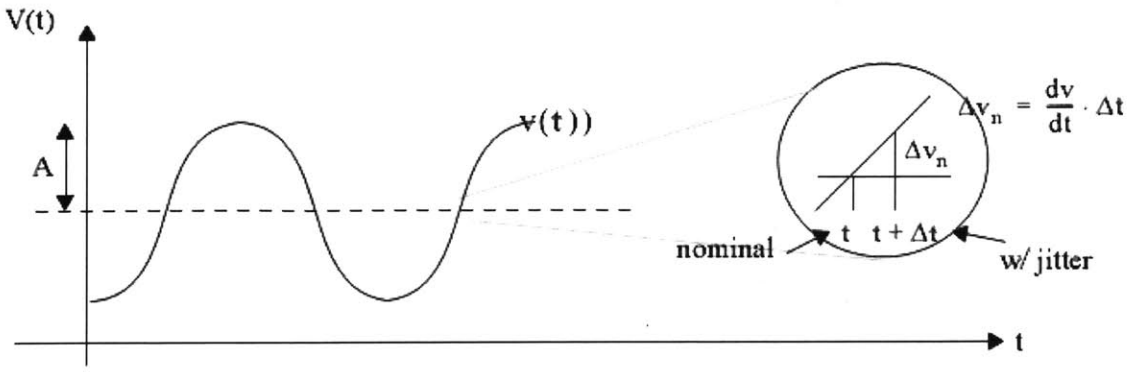

Figure 1 . 2 - Timing jitter leads to varying amplitude errors depending on the signal's slope [3]

This voltage error is particularly nasty since as a result of the dv/dt term, it is frequency dependent, amplitude dependent, and time varying. It is easy to see the creation of this error for analog to digital conversion; however it is somewhat less obvious in the case of digital to analog conversion. It may seem at first that there is no voltage error, since the DAC will output the same voltage regardless of when it is told to do so, however if one considers the fact that the analog signal being represented would have changed during the time jitter, it becomes apparent that there is an error of omission[2]. When the output is low pass filtered to restore the original band-limited signal this error will become noticeable. For large, high frequency input signals this error can add a significant amount of noise, again reducing the resolution and dynamic range of the converter. Aperture jitter, as it is often referred to in data converters, can become a big concern for high speed and high resolution converters.

1.4 Digital Systems:

[2] Note that this mainly applies to clocked digital to analog converters. In continuous time DACs there may be some error from the propagation delay of the digital switches, however this is usually less of a problem since the jitter in the propagation delay is not integrated like in an oscillator.

The last class of circuits to be discussed here involves large complicated digital systems that require very precise timing to function properly. Anytime there are sequential logic components in a digital system, there are setup and hold time conditions that must be met to ensure the correct bits are latched properly. Variation in the clock period limits the maximum operating frequency for a given allowable bit error rate (BER). Also in large systems operating at high frequencies, there may be a large amount of clock skew due to clock traces being sufficient length to introduce noticeable propagation delays. To mitigate this problem large digital chips often have multiple clocks that must be synchronized with on-chip PLLs [3]. Depending on the number of PLLs involved, care must also be taken to ensure there is no peaking in the closed loop response of the PLLs to avoid a phenomenon known as jitter peaking, where repeated 2^{nd} order PLLs can amplify phase noise at certain frequencies.

1.5 Technology Scaling:

In addition to the tightening requirements on oscillator noise performance, there is a strong push toward monolithic integration using scaled CMOS technologies to lower costs and reduce power consumption. Scaled CMOS presents a number of challenges to general analog circuit design since short channel length devices gain speed and reduce power at the cost of increased noise, reduced signal swing, and low output resistance [6,7]. The increased noise factor of short channel devices coupled with low supply voltages directly reduces the achievable SNR for a given power level. Low supply

voltages additionally restrict the use of cascodes and other stacked topologies due to insufficient headroom. As will be shown in later sections, coupling from a noisy supply can greatly affect the overall phase noise of an oscillator [8,9]. Decreased output resistance limits the power supply and common mode rejection ratios (PSRR and CMRR), and hence can reduce the noise immunity of a current biased local oscillator.

Because of their compact size and relatively simple design, integrated ring oscillators have become an attractive option for many applications. Ring oscillators are particularly useful for moderate frequency ranges where traditional LC oscillators would require bulky and expensive external components. On top of the space / cost benefit, many ring oscillator topologies are tunable over multiple decades of frequency, making them very useful for broadband communications [3]. Moreover, the same design can be scaled to perform at various power levels depending on the required noise specifications. This can be explained to first order by considering the sampling of white thermal noise onto a capacitor. It has been shown that the voltage noise on a sampling capacitor is proportional to kT/C, and since a ring oscillator is a type of relaxation oscillator that charges and discharges a capacitor, the frequency of operation is roughly determined by the available drive current and the capacitor size, where $f \alpha I/C$ [10,11]. Assuming a fixed supply voltage and frequency of operation, increasing the capacitance reduces the noise, but forces an increase in the drive current and thus power dissipation. A more detailed analysis of this tradeoff will be given later in the next chapter; however this simple analysis is enough to demonstrate the inherent tradeoff between power and noise for a typical ring oscillator.

Given the large array of circuit applications that require good low noise oscillators, and the constant push for increased integration and decreased costs, there is much incentive to find ways of improving the phase noise performance of simple ring oscillators through biasing, device sizing, and load characteristics, while maintaining flexible tuning range and good supply rejection. Additionally it is worth considering other integrated oscillator topologies such as current-mode oscillators and active inductor circuits. Chapter 2 will review the previous work conducted on LC oscillators as a background lead-in to the advantages and limitations of ring oscillators as well as lay the ground work for the noise analysis of the various ring oscillators to be studied. Chapter 3 will develop a time-domain noise analysis for single-ended ring oscillators that accommodates changing bias and load conditions. Chapter 4 will then discuss differential oscillators and apply the techniques developed in chapter 3 to determine the noise characteristics and how they are different for the differential case. Chapter 5 will close with an overall analysis of the results found during this study and potential avenues for further research.

Chapter 2

Previous Work (LC Oscillators)

2.1 Introduction:

While the focus of this work is integrated ring oscillators, it behooves us to consider the large body of previous work that has already been conducted on the properties of oscillators that utilize a resonator tank, whether LC, crystal, or cavity. Examining the characteristics of LC type oscillators serves as a reference for the comparison of various advantages or disadvantages ring oscillators may have for each application. Furthermore, it may provide valuable insight into what factors limit the achievable phase noise performance of oscillators in general.

Resonator oscillators have the potential to exhibit very good phase noise at low to moderate power levels due to their high Q values, but usually require relatively bulky and expensive external components. At RF frequencies it is becoming more common to see integrated spiral and slab inductors which have Q values in the range of 5-10, however even these on-chip inductors are still quite large relative to the active circuitry and have limited Q values as compared to external wound inductors. Also these on-chip inductors are typically only practical for operation above 1GHz and thus are not suitable for moderate frequency applications in the 100MHz - 400MHz range. LC oscillators also

typically output low-distortion sine waves, instead of square or triangle waves that are loaded with harmonics, which can be important in communication systems where overall spectral purity is important, not just nearby phase noise. Because of the size and cost of producing precision LC oscillators, ring oscillators may be an attractive alternative in many applications provided they can meet the noise specifications.

2.2 Leeson Approach:

The extensive effort that has been put into studying the properties of various types of LC oscillators provides a great deal of insight regarding general oscillator design. The first real intensive analysis of LC oscillator noise was conducted by Leeson in the 1960s. The details of the derivation will not be included here, but it follows from the linear analysis of an LC tank with some inherent loss resistance that the minimum achievable jitter is proportional to kT, P_s^{-1} and Q^{-2}, where Q is the unloaded Q of the physical tank. Considering that Q is defined as the energy in the tank over the power dissipated by the resistive loss, the phase noise is then proportional to $\frac{P_s}{(E_{tank})^2}$, suggesting we want to maximize the energy stored in the tank, while minimizing the power dissipated. Note that this is somewhat contrary to the power vs. noise tradeoff mentioned in the previous section because of the fact that increasing the Q of an LC tank reduces the power necessary to run the oscillator. While this allows for better phase noise at lower power levels, it reduces the flexibility of a design in that the designer can no longer simply scale the circuit to achieve better phase noise. Since the tank energy is in the denominator it

also demonstrates that increasing the voltage swing will also help reduce the oscillator's phase noise since the tank energy can be written as $E_{tank} = \frac{1}{2}C \cdot V^2$. This suggests that single-ended ring oscillators which typically have rail-to-rail voltage swings may be able to achieve better phase noise performance compared to ring oscillators that employ differential pairs.

2.3 Linear Time-Varying Approach:

A more thorough analysis was recently conducted by Hajimiri and Lee that takes into account that all practical oscillators have a necessary non-linearity that limits the signal amplitude and makes the oscillator "stable"[3]. The analysis conducted by Hajimiri and Lee uses a linear but time varying model to account for the changing bias conditions for various noise sources. The analysis develops an impulse sensitivity function (ISF) that maps the phase response of an oscillator to an impulse of current at the oscillator node[4] [12,13]. Since the oscillator waveforms are periodic in f_o, it follows that the ISF as a function of theta will be periodic in 2pi. Looking at the Fourier series of the ISF, there will be components at DC and at multiples of the fundamental frequency, which explains how 1/f noise gets modulated up to the carrier frequency, and gives a better approximation of the additional noise that was empirically determined as the excess noise factor F in the Leeson approximation [13]. If the noise injected into the oscillator node is

[3] Technically speaking an oscillator is never stable, however practical oscillators settle into what is referred to as a fixed limit cycle where the waveforms will be periodic.

[4] For multiple stage oscillators like ring oscillators it is usually assumed that all oscillator stages are identical, and hence the ISF will be equivalent but phase shifted. Also ISF functions can also be mapped for other nodes in the circuit; however for simplicity this discussion will be limited to a single ISF.

stationary white noise, then the excess noise factor comes from the RMS value of the ISF, however when the noise power spectral density changes for different frequencies, the texture of the ISF determines which frequency ranges contribute the most noise to the oscillator output. In addition to providing a better explanation of the modulation of noise to the oscillator spectrum, the ISF provides an easy way to account for the changing bias conditions as they affect the amount and type of noise present. The bias conditions are changing periodically as well, so the noise generated by a particular device can be modeled as a white noise source multiplied by a periodically changing envelope function, termed the noise modulation function (NMF). Multiplying the ISF by the NMF yields an effective ISF function that responds to white noise in the same manner as the original ISF responded to time varying noise [13].

Although similar in many respects to LC oscillators, ring and relaxation oscillators share two critical differences hinted at in the previous section that limit their phase noise performance. The first is that the "tank" energy in RC oscillators is discarded after every cycle, which is essentially equivalent to limiting the Q of an LC oscillator to a maximum of 1, as compared to high quality discrete LC resonators that can have Q values of 1000 or more. Considering the fact that oscillator phase noise improves as a factor of Q^{-2}, this can be a very substantial disadvantage [10]. The second difference is that from looking at the ISF functions, the restoring energy provided by the active devices in a ring oscillator is injected during the most sensitive portion of the oscillation cycle [12]. In contrast for example a Colpitts oscillator injects almost no device noise during the peak sensitivity and consequently has very good phase noise performance.

While it has yet to be proven that these two disadvantages are absolutely unavoidable, all commonly used ring oscillator topologies exhibit both of these properties. Disadvantages aside, there are still a number of important design parameters that can be used to glean the most performance out of a simple ring oscillator.

As was mentioned in the previous chapter, the amount of phase noise present in a ring oscillator can be adjusted over a very wide range by trading off die area and power consumption. Ring and relaxation oscillators at their core are essentially composed of an RC time constant, or a constant current charging a capacitor. If we consider an RC relaxation time as the oscillator core, then the frequency of operation will be proportional to the inverse of the time constant, $f_o \alpha \frac{1}{R \cdot C}$. The thermal noise current density for a resistor is $\frac{4 \cdot k \cdot T}{R}$, and the resulting voltage noise sampled onto the capacitor as a function of frequency is $(v_n)^2 = (i_n)^2 \cdot \left(\left| \frac{R}{1 + i \cdot 2\pi f \cdot R \cdot C} \right| \right)^2$ since we are dealing with variances. To find the total noise voltage at the capacitor, we then integrate the noise density over frequency as shown below:

$$(v_n)^2 = (i_n)^2 \cdot \int_0^{\infty} \left(\left| \frac{R}{1 + i \cdot 2\pi f \cdot R \cdot C} \right| \right)^2 df \rightarrow (v_n)^2 = \frac{1}{4} \cdot (i_n)^2 \cdot \frac{R}{C} \rightarrow (v_n)^2 = k \cdot \frac{T}{C}$$

The result is an equivalent noise bandwidth of $\Delta f = \frac{1}{4 \cdot R \cdot C}$ and a voltage noise variance that is independent of R. The minimum power required to charge and discharge this capacitor is $P_{min} = C \cdot (V_{dd})^2 \cdot f_o$, so for constant frequency of operation and supply voltage, power consumption and thermal noise are inversely related. Note that for typical IC

processes, increasing the capacitance will also require a proportional increase in the die area of the capacitor as the plate separation is typically fixed, although new techniques such as fractal capacitors may alleviate this trade-off to an extent [14]. Obviously there are practical limitations to the extent that power and noise can be traded-off, such as heat buildup, maximum die area[5], and minimum device dimensions; however the point is that for ring oscillators the power and area to noise efficiency, defined as the ratio of power and area over noise, is the critical figure of merit, not the absolute phase noise measurement.

2.4 Scaling Concerns:

Another growing concern in oscillator design today is the effects of CMOS device scaling on the noise properties of MOSFETs. In addition to the headroom limitations mentioned in chapter 1, CMOS scaling deteriorates the noise performance of the active devices themselves. In particular, the FET's excess noise factor[6] γ continues to increase with short channel effects, and the flicker noise corner frequency $\omega_{1/f}$ is increasing with smaller device dimensions [6,7]. Unfortunately there is little that can be done about the increase in γ from the designer's side other than using longer gate length devices, and using devices with the lowest γ in critical locations where that particular device's noise contributes greatly to the output phase noise. As far as the flicker noise corner frequency is concerned, it is important to design the oscillator for high waveform symmetry in order to reduce the DC component of the oscillator's ISF function discussed in the preceding

[5] This limitation is typically due to yield considerations, large die decrease the usable wafer area, and decrease the yield rate for a given defect density.
[6] The thermal noise current spectral density in the channel of a MOSFET is modeled as $4kTg_m\gamma$

section [12]. Ideally speaking the linear time-varying model suggests that if the ISF could be made completely symmetric about zero then there would be no up-conversion of flicker noise at all (assuming the flicker noise corner is below the oscillator frequency) [13]. In practice it is nearly impossible to completely eliminate the effects of flicker noise; however significant improvements in the flicker noise up-conversion can be made with careful design. Assuming the operating frequency is not already limited by the process capabilities, extra ring stages can be used to increase the relative waveform symmetry and thus results in a reduction of the f^3 corner frequency in the oscillator spectrum [12]. One last major area for concern is the potential effects of external noise sources, such as the supply and substrate, on the noise performance of the oscillator. While designing for very low intrinsic phase noise is still important, the trend of increasingly large scale integration of both analog and digital sub-circuits means that designers must deal with potentially large amounts of noise and voltage ripple on the supply and substrate. Large switching currents from digital sub-circuits can jerk the supply around quite a bit, especially if the supply is not properly decoupled with bypass capacitors outside the chip. Noise on the supply can affect the output noise through two of different mechanisms. The first is direct capacitive and resistive coupling, which can be reduced by reducing the supply dependence of the voltage at the oscillator node. The second is by modulating the natural frequency of the oscillator since the supply can act as an unintentional VCO tuning node [7]. The result yields both an increase in the oscillator's general phase noise, as well as the potential for spurious tones depending on the characteristics of the supply voltage ripple. Differential topologies often show much better resistance to supply and substrate noise, owing to their naturally higher power

supply and common mode rejection ratios (PSRR and CMRR), however changes in the supply still affect the oscillator frequency through the non-linear capacitances of the active devices [8,9]. As such, differential ring oscillators may be able to achieve better overall phase noise performance, despite their generally inferior intrinsic phase noise.

Chapter 3

Single-Ended Ring Oscillators

This work will begin with the analysis of single ended ring oscillators in this chapter, followed by a discussion in chapter 4 about how switching to differential architectures affects the analysis presented here, culminating in an example design which will touch on several important peripheral topics such as bias circuitry and VCO control. The flow of this chapter progresses from the simplest designs working toward more complicated ones, considering each added level of complexity one at a time. Starting with the simple designs allows for approximate analytical solutions that provide a more intuitive explanation of the factors that influence the generation of oscillator phase noise from the base-band thermal and flicker noise of various circuit elements. Furthermore, the simple designs provide a baseline for comparison so that isolated changes can be made and their effect considered without the complications of several other changes.

Section 3.1 covers the simplest design, which is a three stage linear amplifier with unity gain feedback. Section 3.2 details the large signal time domain noise analysis for the oscillator in 3.1. Following the development of a noise model for the linear amplifier oscillator is an analysis of the effects of changing device parameters. Section 3.3 covers how changes in the effective stage gain alter the oscillation frequency and jitter. Along

with the effects of stage gain variations is a look at the effects of current limiting, which leads into chapter 4's discussion of differential oscillators. The differential architectures to be examined are based on a current source biased differential pair.

3.1 Simple Amplifier Chain:

One of the simplest ways to build an oscillator is to string together three single pole amplifiers with greater than unity gain. Each of the three stages is a resistor loaded common source amplifier, with the output connected directly to the next stage's input, as shown in figure 3.1.1 below.

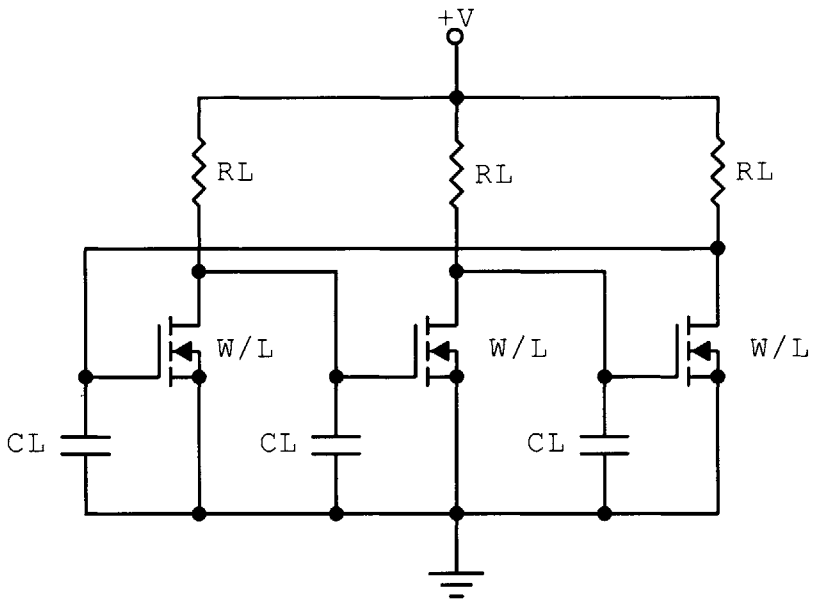

Figure 3 . 1 . 1 -- Three stage linear amplifier with unity feedback

Before delving into the precise non-linear response of this circuit, we examine the approximate linear solution as a quick first pass analysis. Following from traditional

linear analysis techniques we see that prior to closing the loop the transfer function from input to output is the product of the three single stage transfer functions. Assuming each stage is identical, the resulting input-output relation is:

$$\frac{V_o(s)}{V_i(s)} = \frac{-A^3}{(\tau \cdot s + 1)^3} = \frac{-(g_m \cdot R_L)^3}{(R_L \cdot C_L \cdot s + 1)^3} \quad \text{(Eqn. 3.1.1)}$$

Looking at the linear approximation, we get a maximum of 270 degrees of negative phase shift from the three poles, plus a net 180 degrees of phase shift from the three inversions. Under a purely linear assumption the gain must be set such that it is precisely one when the total phase becomes 360 degrees to satisfy the Barkhausen criterion, and the circuit can oscillate at any amplitude. The requisite phase shift occurs when each stage provides 60 degrees of negative phase, allowing us to solve for the frequency of oscillation.

$$\text{Total phase shift: } \phi = -3\,\text{atan}(R_L \cdot C_L \cdot \omega), \quad \text{yielding } \omega_o \approx \frac{1.732}{R_L \cdot C_L}$$

The reality is that in order to have sustained oscillations at a fixed amplitude, the gain must be amplitude dependent; greater than unity for small amplitudes, and less than unity for large amplitudes. As a result of the non-linearity, the oscillation frequency will be somewhat different from the above prediction due to the effective phase shift associated with the non-linear gain. For this oscillator, the non-linearity comes from the MOSFET entering the triode and cutoff regions for high and low inputs respectively[7]. Shown below in figure 3.1.2 is a typical drain current characteristic for a MOSFET with a constant applied drain voltage.

[7] High and low meaning near the supply and near ground indicating a large amplitude signal

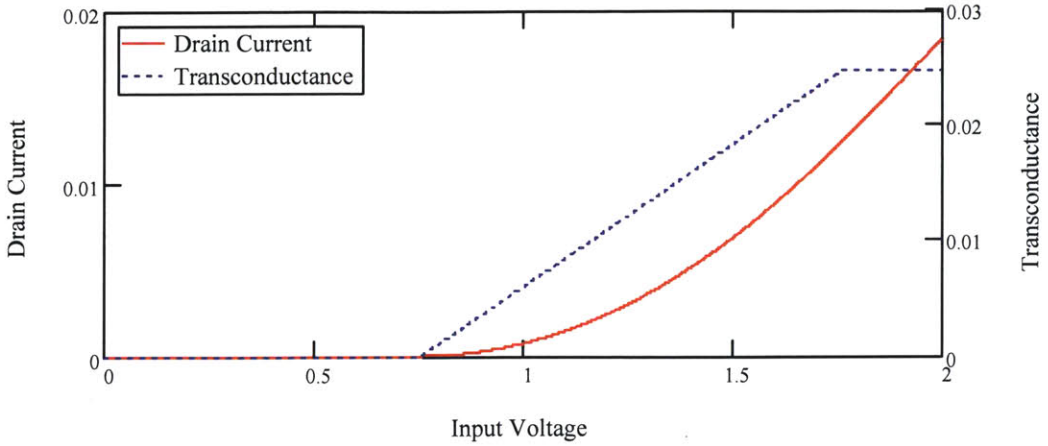

Figure 3 . 1 . 2 -- MOSFET drain current and transconductance for constant drain voltage

When in saturation the MOSFET drain current is proportional to the square of the input voltage; thus, smaller input voltages produce smaller stage gain until the voltage bottoms out at ground, shutting off the transistor completely. When the MOSFET is in the triode region the transconductance levels off to a constant for constant V_{ds}; however, in this circuit increasing the drain current reduces the drain voltage, causing g_m to decrease as demonstrated below[8] in figure 3.1.3:

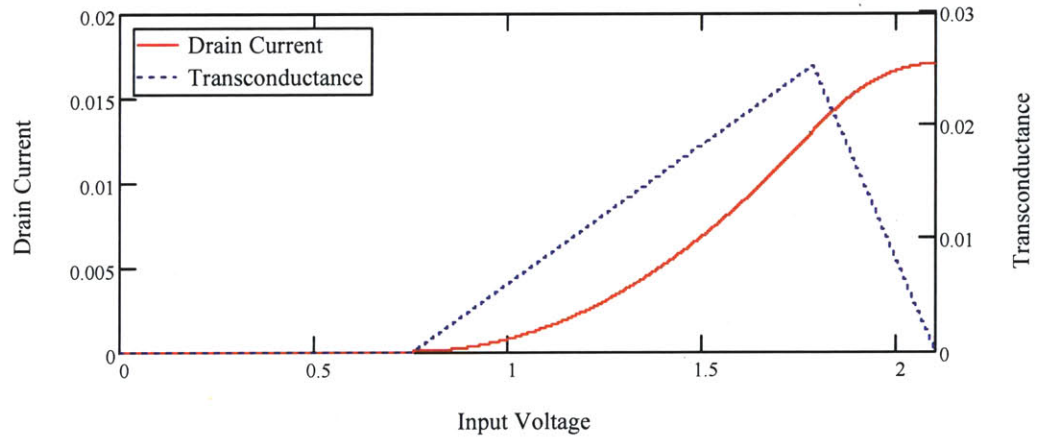

Figure 3 . 1 . 3 -- MOSFET drain current and gm with falling drain voltage

Now that we have established the basic characteristics of the individual gain stages, we move on toward determining the large signal oscillator waveform, after which we can begin the discussion of noise sources and their transformation into timing jitter. In

[8] Note this graph is only first order approximation of drain voltage for illustration, not an exact solution

this first pass, we assume the load resistor and load capacitances are linear, as well as ignore any parasitic gate to drain capacitances. When this is the case, the time evolution of the output voltage is governed by equation. 3.1.2, which is the differential equation that arises from performing KCL at the output node of a single stage,

$$C \cdot y'(t) = -h(x(t), y(t)) + \frac{V_S - y(t)}{R} \qquad \text{(Eqn. 3.1.2)}$$

where $h(V_{gs}, V_{ds})$ is the MOSFET drain current as a function of gate and drain voltage, x(t) is the input waveform, and y(t) is the output waveform, with its corresponding time derivative y'(t). The full oscillator is described by the system of three non-linear differential equations identical in form to equation 3.1.2, one for each of the three drain nodes. While there is no exact analytical solution for this entire system, particularly for more complicated MOSFET models, the system can be solved numerically to find the deterministic part of the oscillator waveform, which results in a stable limit cycle surrounding an unstable equilibrium point. Figure 3.1.4 on the next page shows several sample trajectories of one particular node voltage and its time derivative. There is an equilibrium point near the center; however, it is an unstable one, as the figure below shows how even the slightest deviation from this point will cause the trajectory to spiral outward until it reaches the stable limit cycle due to the high small signal gain and ample phase shift when the MOSFETs are biased near mid supply. If, on the other hand, the trajectory begins outside the limit cycle, the reduced small signal gain causes the signal to decay inward toward the limit cycle. This oscillator has only one stable limit cycle; however, in general, oscillators may have more than one locally stable limit cycle and may be susceptible to phenomena such as injection and harmonic locking or chaotic oscillation. Such phenomena are beyond the scope of this work, but interested readers are

encouraged to seek more information about non-linear dynamics and chaos theory in [15].

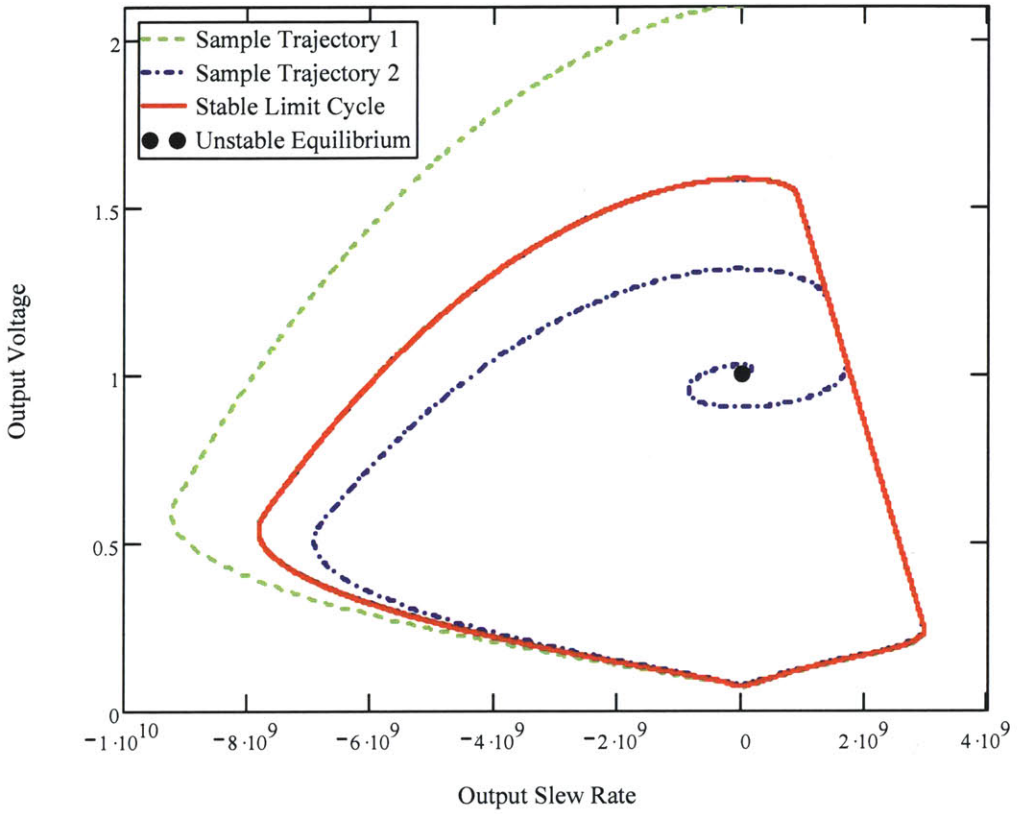

Figure 3 . 1 . 4 -- Sample oscillator trajectories, showing unstable equilibrium and stable limit cycle

The shape of the limit cycle, and hence the oscillator waveforms, is highly dependent on the gain per stage as well as process parameters such as the threshold voltage and carrier mobility[9]. For low gains, the oscillator can be treated as being weakly non-linear since only a small amount of gain compression is required to limit the oscillation amplitude. In this case the linear approximation suggested at the beginning of this chapter is a reasonable approximation to the dynamics of this system. The simulated waveform of this oscillator with a 150Ω load resistor and 4pF of added load capacitance

[9] To first order these can be thought of as simply altering the effective average gain of a stage, particularly for the mobility term. The threshold voltage has some additional effects on the DC component of the oscillator waveform.

is shown below in figure 3.1.5. The oscillation frequency of 410MHz corresponds well with the linear prediction of ~425MHz[10].

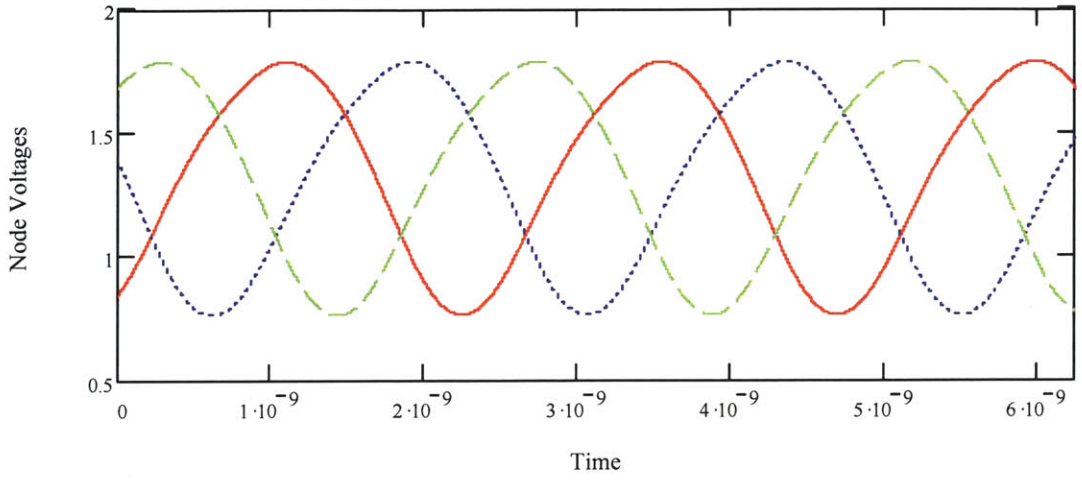

Figure 3 . 1 . 5 -- Weakly non-linear response for low gain case

The voltage waveforms are very nearly sinusoidal, consistent with the assumption that the system can be treated as only being weakly non-linear. While the linear approximation gets us a reasonably good estimate of the oscillation frequency, it does little to help us determine the amplitude, as in a strictly linear system there is no amplitude dependence. An estimate of the amplitude can be obtained using describing functions for the stage gain as a function of amplitude if so desired.

For larger gains, the system becomes less and less linear, until the gain is high enough such that the transistor essentially becomes a switch that grounds the output when on and lets the RC load relax toward the supply when off. A somewhat more accurate model is a switch with a non-zero on resistance, though it is important to remember that the noise introduced by the transistor is not simply that of a real resistor. This is due to the fact that the transistor on resistance is a function of the drain voltage, while the noise

[10] This includes approximately 300fF of capacitance from the active device in addition to the 4pF load capacitance. The device dimensions are W=200μm, L=.6μm

current density is controlled by the gate voltage and is multiplied by the excess noise factor, which can be large for short channel devices. Additionally there is added flicker noise due to various mechanisms in the transistor channel. This will be discussed in more detail in the next section when we describe the full noise analysis of this oscillator.

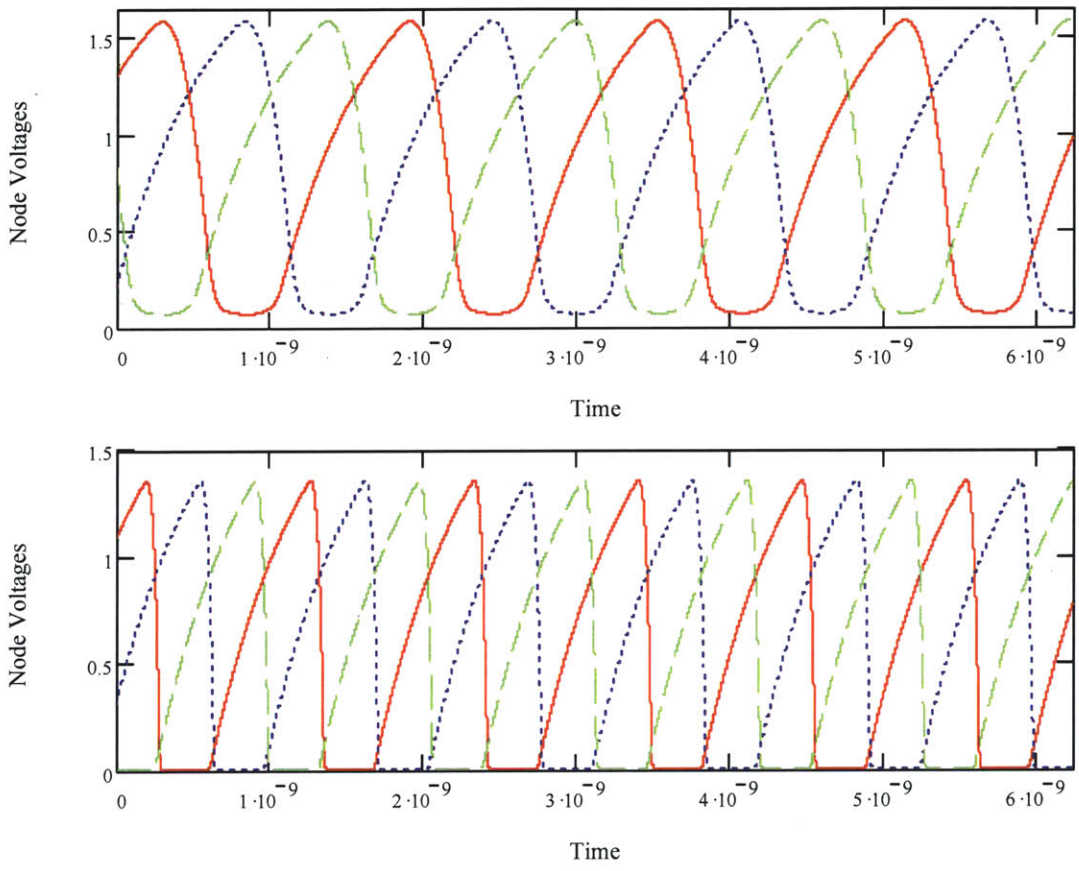

Figure 3 . 1 . 6 -- Oscillator waveforms for moderate gain (Top) and high gain (Bottom) cases

Figure 3.1.6 shows the oscillator response for increasing gain while holding everything else constant. The gain is increased by increasing the carrier mobility in the simulation, thus increasing g_m without changing the load impedance. The response, particularly in the higher gain cases, looks very similar to that of a Schmitt trigger oscillator except that the rising and falling edges have different time constants[11]. It is

[11] The other main difference is the extended time in each state, which is a result of there being multiple stages as opposed to a traditional Schmitt trigger oscillator that only has one stage.

interesting to note that as the gain increases, the oscillation amplitude increases at first, but then eventually decreases. The waveform is clipped by ground on the low end and the increasing gain requires less gate overdrive to turn on the transistor, lowering the peak voltage. This may have implications on the overall noise performance of the oscillator under different operating conditions, as is investigated in the next section.

3.2 Non-linear Noise Analysis:

Now that we have a good idea of what the waveforms look like under steady state conditions, we proceed toward determining the RMS noise voltage at the oscillator nodes, and subsequently the induced timing jitter. Since ring oscillators are typically closer to square-waves than sine-waves, this work will primarily focus on the period jitter as opposed to the precise phase noise spectrum. This section will begin by examining the noise current produced by the transistor and how it varies with the applied gate voltage. Next we look at how the noise voltage responds to the time varying noise current using a purely time domain analysis involving autocorrelation functions and impulse responses. This approach allows us to make changes in the linearity of the load resistance and capacitance without requiring major changes in the aforementioned analysis. Figure 3.2.1 on the next page illustrates the noise sources present in each stage of the ring oscillator. The noise from the load resistor is presumed to be constant for this part of the analysis, although nothing prevents it from being replaced with other loads that may have non-constant noise characteristics.

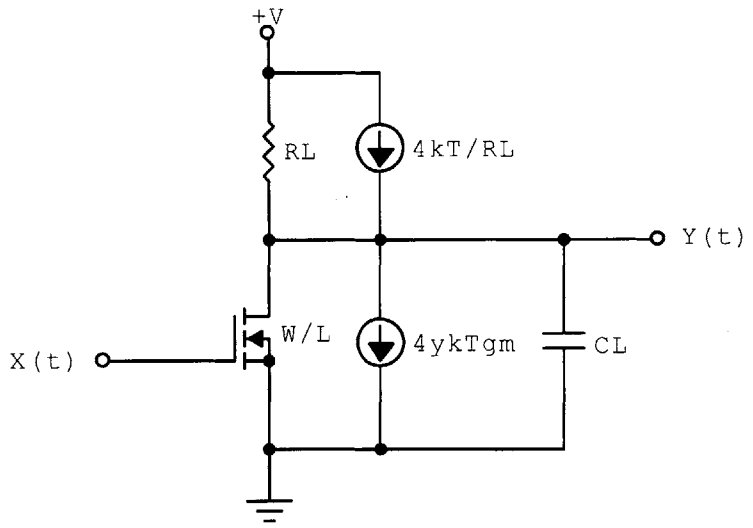

Figure 3 . 2 . 1 - Single stage with thermal noise sources shown

The noise from the transistor is dependent on both the input and output voltages as is the impulse response from current to voltage at the output. When the input voltage is below v_T the transistor is in cutoff and the noise current it produces is essentially zero.[12] Once there is sufficient overdrive the MOSFET will be in strong inversion, and produce a drain to source noise current with a uniform spectral density of $\overline{i_n^2} = 4\gamma \cdot k \cdot T \cdot g_{do}$. In terms of the gate voltage, the zero bias drain to source conductance, g_{do}, is approximately $\mu \cdot C_{ox} \frac{W}{L}(V_{gs} - v_T)$ if we ignore the back gate effect. The excess noise factor, γ, is 2/3 for long channel devices in saturation and rises to 1 when the MOSFET enters the triode region. For short channel devices γ is not as well defined, but it typically rises to around 2 or 3. The dependence on the input voltage is essentially the same whether the MOSFET is in saturation or the triode region, consistent with the presumption that the noise is related to the carrier density in the channel. The only change is in the γ term that

[12] There will be some non-zero amount of shot noise produced by the reverse biased p-n junctions, however this leakage current is very small, and the subsequent noise current should be negligible compared to the noise produced by the load resistor.

increases gradually as the channel is no longer pinched off[13], increasing the amount of charge in the channel. The above noise model is not very accurate when the MOSFET is in weak and moderate inversion; however, in this case the transistor is only in those regions for a short time. The models for weak and moderate inversion noise generation are discussed further, as part of the discussion on current limiting mechanisms at the end of this chapter.

Time Domain Noise Evolution:

To begin the time domain noise analysis we begin with a brief primer on the time evolution and decay of an isolated noise source. Using that as a foundation, a piece-wise constant model is used as a first pass, to be extended later to a nearly continuous case using the predetermined oscillator waveform[14]. While this is not the most computationally efficient method of analysis, it allows us to view the precise evolution of the RMS output noise and draw insight from that. Additionally we can try to explain the effects of non-linearities in the load impedance from the piece-wise analytic solution.

For the following analysis, we assume that the noise present in the system is small enough such that the amplifier stage's response can be treated as a linear system whose parameters vary over time. Since the object of this thesis is to aid in the design of low noise ring oscillators, the assumption seems reasonable enough and provides results consistent with full harmonic balance simulations of these oscillators. We also assume that all of the noise sources are uncorrelated since they originate from different physical

[13] In the long channel case the noise factor increases from 2/3 to 1; in the short channel case the change is less well defined.
[14] Here we make the assumption that the noise responsible for the period jitter is small enough to not alter the trajectory of the oscillator waveforms.

processes, and hence their variances will simply add and their autocorrelation functions will be scaled delta functions. The exceptions are any sources of flicker noise, which will have more complicated autocorrelation functions. However, flicker noise sources are not examined rigorously in this work.

Traditional frequency domain analysis has shown that first order RC filtering of a white noise current source results in a noise voltage variance of $\overline{i_n^2}\cdot\frac{R}{4\cdot C}$, which reduces to the well known result of $\frac{k\cdot T}{C}$ for a simple resistor where $\overline{i_n^2} = \frac{4k\cdot T}{R}\cdot\Delta f$. This analysis assumes, however, that the noise source has been constant for a long time, and consequently ignores the RC rise time associated with the output noise. In the time domain, the output voltage noise can be determined by evaluating the convolution of the noise source's autocorrelation function with the impulse response of the system.

$$R_{vv}(t_1,t_2) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} h(\tau_1)\,h(\tau_2)\,R_{ii}(t_1-\tau_1,t_2-\tau_2)\,d\tau_2\,d\tau_1 \quad \text{(Eqn. 3.2.1)}$$

Where $h(t) = \frac{1}{C_L}e^{\frac{-t}{R_L\cdot C_L}}\cdot u(t)$ and $R_{ii}(t_1,t_2) = 2\gamma\cdot k\cdot T\cdot g_m(t_1)\,\delta(t_1-t_2)$

Note that the noise current density has a factor of 2 instead of 4 because it is a double sided autocorrelation, as opposed to a single sided PSD [3]. For a constant noise source turned on at time $t = 0$, the lower limits of integration become 0 since the system is causal, i.e. $h(\tau)$ is zero for any τ less than zero. The upper limits become t since that is how much time the noise source has been on for. Since we are looking at white noise, we are only concerned with the total noise variance, not its entire autocorrelation function, hence

from now on $R_{vv}(t_1,t_2)$ will be replaced by $R_{vv}(t)$. Now equation 3.2.1 can be replaced by equation 3.2.2 shown below.

$$R_{vv}(t) = \frac{2\cdot\gamma\cdot k\cdot T\cdot g_m}{C_L^{\,2}}\cdot\int_0^t e^{\frac{-\tau_1}{R_L\cdot C_L}}\cdot\int_0^t e^{\frac{-\tau_2}{R_L\cdot C_L}}\cdot\delta(\tau_2-\tau_1)\,d\tau_2\,d\tau_1 \qquad \text{(Eqn. 3.2.2)}$$

The delta function from the noise current's autocorrelation is only non-zero when τ_2 is equal to τ_1, so the inner integral reduces to a single value, dependent on the current value of τ_1. The final result of this is a noise voltage that has a final value equal to that which would be predicted from standard frequency domain methods, but which also has a transient portion that rises from zero to the final value with an exponential time constant half that of the filter.

$$R_{vv}(t) = \frac{2\cdot\gamma\cdot k\cdot T\cdot g_m}{C_L^{\,2}}\cdot\int_0^t e^{\frac{-2\tau_1}{R_L\cdot C_L}}\,d\tau_1 = \frac{\gamma\cdot k\cdot T\cdot g_m\cdot R_L}{C_L}\cdot\left(1-e^{\frac{-2t}{R_L\cdot C_L}}\right) \qquad \text{(Eqn. 3.2.3)}$$

The halving of the time constant makes good intuitive sense when we remember that the variance is a voltage squared term, adding a factor of two in the exponent. Knowing the homogeneous response to this simple first order system, it follows that a known voltage variance will decay with time if the driving noise source is shut off. Here again the time constant will be half that of the system due to the variance being a squared term. This can be verified using equation 3.2.1 with the appropriate changes to the limits of integration; however, in the interest of saving space, the derivation is left as an exercise for the reader.

Piecewise Constant Model:

Knowing the growth and decay characteristics of an isolated noise source, we can compute the noise voltage contribution from individual segments of time one at a time. Since the noise sources are uncorrelated, the contributions from each time segment can be summed together to find the total output noise. From this we can put together a piece-wise constant model of the oscillator noise contributions. For the analysis presented in this chapter, we will use a 5 stage ring oscillator from now on for illustrative purposes due to the increased separation between operation regions. The methodology presented here remains valid for any number of stages. There are three main regions of operation for a particular stage; the first is when the input is low and the transistor is off, leaving the output to relax toward the supply; the second is when the input is high and the output is also high, keeping the transistor in saturation; and finally the third is when the input is high and the output is low, forcing the transistor into the triode region.

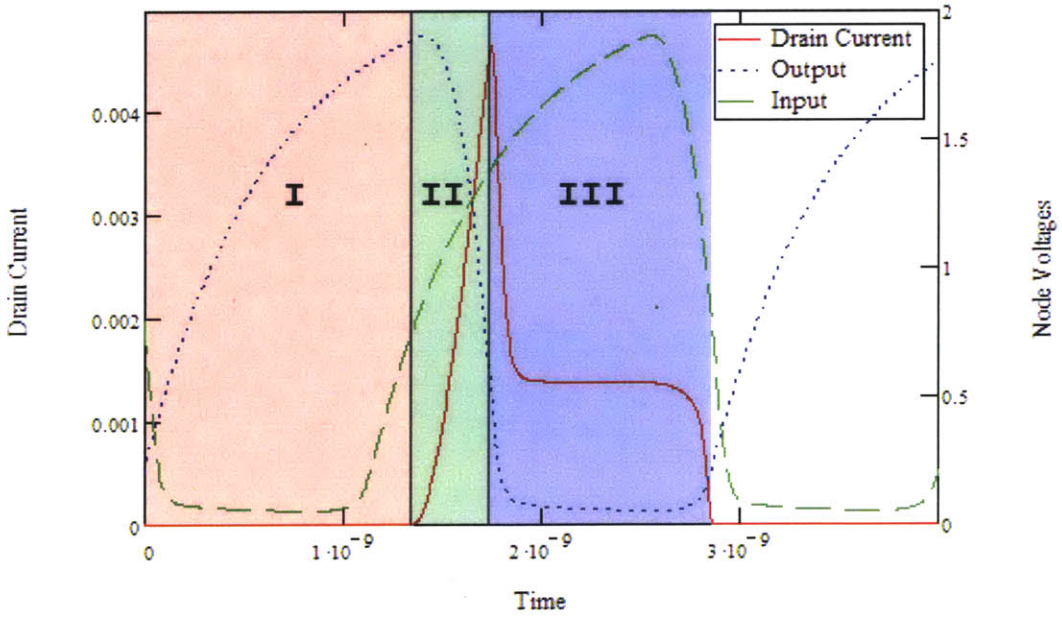

Figure 3 . 2 . 2 -- Stage waveforms and MOSFET drain current, illustrating main operating regions; I) cutoff region; II) saturation region; III) triode region

During region I the only noise source present is the thermal noise from the load resistor. For regions I and II the load impedance, and hence the impulse response, is just that of the nominal RC load[15]. Any residual noise at t = 0, will decay linearly with the time constant ½RC, as previously described. The residual noise is determined at the end of this section, but it should also be noted that the contribution of the resistor's thermal noise will not be its steady state value due to the change in effective load resistance. Considering that the low steady state voltage is approximately ground and the noise voltage is proportional to the ratio of the effective resistance over the noise resistance, the noise at t_0 from the resistor will be quite small relative to its steady state value. The noise at any time during region I can be determined by using 3.2.3, substituting 1/R for g_m and 1 for γ, and adding the residual noise decay. The noise generated from region I can be summarized as follows:

$$\overline{v_n^2}(t) = \frac{k \cdot T}{C_L} \cdot \left(1 - e^{\frac{-2t}{R_L \cdot C_L}}\right) + \overline{v_n^2} \cdot (0)\, e^{\frac{-2t}{R_L \cdot C_L}}, \qquad 0 \le t \le t_1$$

$$\overline{v_n^2}(t) = \frac{k \cdot T}{C_L} \cdot \left(1 - e^{\frac{-2t_1}{R_L \cdot C_L}}\right) e^{\frac{-2(t-t_1)}{R_L \cdot C_L}} + \overline{v_n^2} \cdot (0)\, e^{\frac{-2t}{R_L \cdot C_L}}, \qquad t_1 \le t \le t_2 \qquad \text{(Eqn. 3.2.4)}$$

Where t_1 marks the transition from region I to region II and t_2 marks the transition from region II to region III. After t_2 equation 3.2.4 is no longer valid since the small signal impulse response changes when the transistor enters the triode region. During region II, the impulse response is unchanged from region I; however the noise current is no longer constant as the gate drive of the MOSFET is increasing. We can get a first order approximation of the noise during this region if we calculate the average overdrive

[15] Technically for region II, the output resistance of the MOSFET will be in parallel with the load, however it should be quite large relative to the load resistor, especially when current limiting is involved.

voltage during this period and use it to obtain the transistor g_m.[16] Equation 3.2.5 includes both the resistor and MOSFET noise current sources in the $\left(1 + \gamma \cdot g_{m.avg} \cdot R_L\right)$ term.

$$\overline{v_n^2}(t) = \frac{k \cdot T \cdot \left(1 + \gamma \cdot g_{m.avg} \cdot R_L\right)}{C_L} \cdot \left[1 - e^{\frac{-2\left(t - t_1\right)}{R_L \cdot C_L}}\right] + \overline{v_n^2}\left(t_1\right) e^{\frac{-2\left(t - t_1\right)}{R_L \cdot C_L}}, \quad t_1 \le t \le t_2 \quad \text{(Eqn. 3.2.5)}$$

$v_n^2(t_1)$ is the noise voltage at the end of region I as calculated using the first part of equation 3.2.4. While equation 3.2.5 is not exact, it does provide a reasonable approximation to the actual noise for now. An analytic solution for the noise in this region is derived in the next section, when we extend the piecewise constant model toward the limit of continuous calculation.

In region III the small signal response is shunted by the drain to source conductance of the triode region MOSFET. For moderate to high gain configurations, the output falls very quickly, suggesting we may be able to approximate the response during region III as a constant with the zero bias drain to source conductance of the MOSFET in parallel with the load. Again we use the average overdrive voltage during this region to determine the effective drain to source resistance and noise current. The resulting noise equation for region III is then:

$$\overline{v_n^2}(t) = \frac{k \cdot T \cdot \left(\frac{1}{R_L} + \gamma \cdot g_{ds0.avg}\right) R_{eff}}{C_L} \cdot \left[1 - e^{\frac{-2\left(t - t_2\right)}{R_{eff} \cdot C_L}}\right] + \overline{v_n^2}\left(t_2\right) e^{\frac{-2\left(t - t_2\right)}{R_{eff} \cdot C_L}}, \quad t_2 \le t \le t_3 \quad \text{(Eqn. 3.2.6)}$$

where $v_n^2(t_2)$ is the noise voltage at the end of region II from equation 3.2.5, and R_{eff} is the parallel combination of R_L and g_{ds0}. R_{eff} is quite a bit smaller than R_L for any ring oscillator that swings close to ground, so the noise in region III will generally respond

[16] This will be improved upon in the next section, in fact in this case there is an analytic solution to the noise in region II

much faster since its time constant may be as much as 10 to 100 times shorter than during regions I and II. Putting all three regions together we get a first look at what the noise looks like during one cycle of oscillation. Figure 3.2.3 shows the oscillator waveforms along with the noise variance predicted from the piecewise constant model. In the figure the noise voltage at $v_n^2(T_o)$ is substituted for $v_n^2(0)$ as the waveform must be periodic, and any initial noise will have long since decayed by the end of one period. In this case it is almost entirely gone even before reaching region II, despite the fact that the significantly faster response of region III would render anything generated prior to region III insignificant by the end of the cycle.

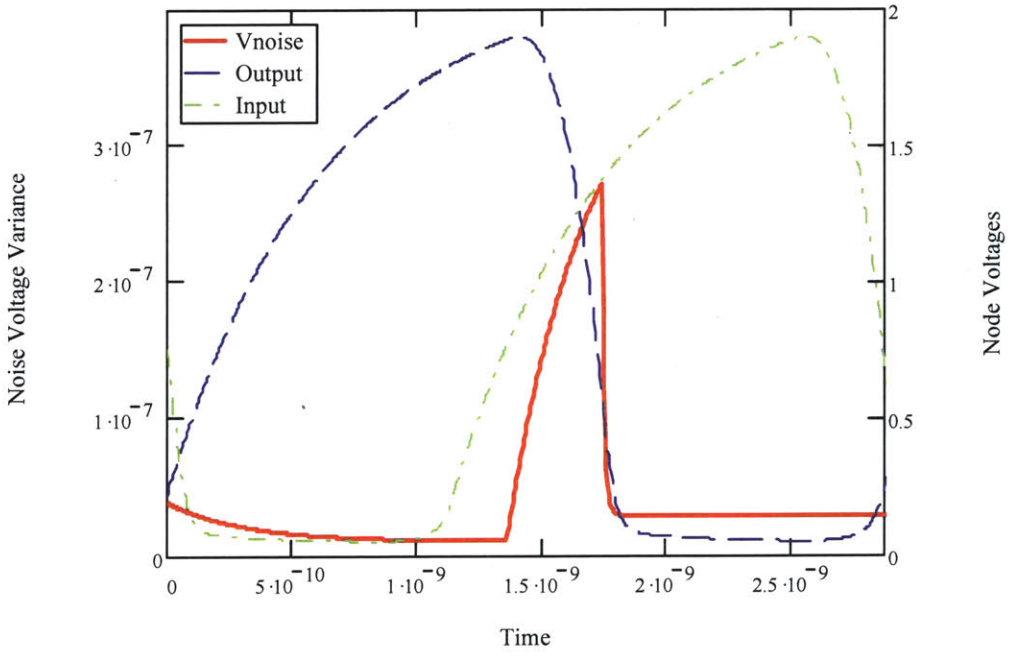

Figure 3 . 2 . 3 -- Piecewise constant noise prediction for corresponding oscillator waveforms

Near Continuous Model:

The next step in analyzing the oscillator noise is to extend the piecewise constant model toward the limit of a continuous model. Since we know how to determine the noise as a result of separate regions of time that may have varying noise currents and impulse

responses, there is no reason we can't simply break up the oscillator waveform into smaller regions until we have arbitrarily small time segments. In the limit of ever decreasing time divisions the model becomes a continuous representation of the noise evolution, and in some cases may yield an analytic result. From equation 3.2.3 we know that an isolated noise current density will generate a corresponding noise voltage variance $\frac{\overline{\left(i_n^2\right)_i}\cdot R_i}{2C_i}\cdot\left(1-e^{\frac{-2\cdot\Delta t_i}{R_i\cdot C_i}}\right)$ over a short time Δt_i of:

(Where R_i, C_i, $i_n^2{}_i$ are the effective load resistance, capacitance, and noise current at that particular time instant and Δt_i is the length of that particular segment.)

The noise variance will then decay according to the localized homogeneous system response over the course of each following time step. In this case, the noise variance is multiplied by $e^{\frac{-2\cdot\Delta t_i}{R_i\cdot C_i}}$ for each remaining time step between the current time and the final time we wish to determine the noise at. Summing the contributions from each individual time segment results in the following equation for the noise voltage after m time steps:

$$\overline{v_n^2} = \sum_{i=0}^{m}\left[\frac{\overline{\left(i_n^2\right)_i}\cdot R_i}{2C_i}\cdot\left(1-e^{\frac{-2\Delta t_i}{R_i C_i}}\right)\cdot\prod_{j=i+1}^{m} e^{\frac{-2\Delta t_j}{R_j C_j}}\right], \qquad \text{(Eqn. 3.2.7a)}$$

Which can also be rewritten in the form:

$$\overline{v_n^2} = \sum_{i=0}^{m}\left[\frac{\overline{\left(i_n^2\right)_i}\cdot R_i}{2C_i}\cdot\left(1-e^{\frac{-2\Delta t_i}{R_i C_i}}\right)\cdot e^{-2\sum_{j=i+1}^{m}\frac{\Delta t_j}{R_j C_j}}\right], \qquad \text{(Eqn. 3.2.7b)}$$

Using the predetermined oscillator waveform from any of a number of numerical integration methods, equation 3.2.7 can be used to determine the accumulated noise at

each time instant. If instead of computing the noise variance using the nested form of 3.2.7, the computation is done by iteratively scaling the cumulative noise and adding the next noise segment the computation time grows O(n) instead of $O(n^2)$, saving a significant amount of computation time. Equation 3.2.8 below shows the fundamental difference equation relating the noise variance at one time instant to the next.

$$\overline{\left(v_n^2\right)_i} = \frac{\overline{\left(i_n^2\right)_i}\cdot R_i}{2C_i}\cdot\left(1 - e^{\frac{-2\Delta t_i}{R_i C_i}}\right) + \overline{\left(v_n^2\right)_{i-1}}\cdot e^{\frac{-2\Delta t_i}{R_i C_i}} \quad \text{(Eqn. 3.2.8)}$$

After using equation 3.2.8 and the previously determined oscillator waveform, the precise noise calculation is performed and is shown below in figure 3.2.4 with the piecewise constant model for comparison.

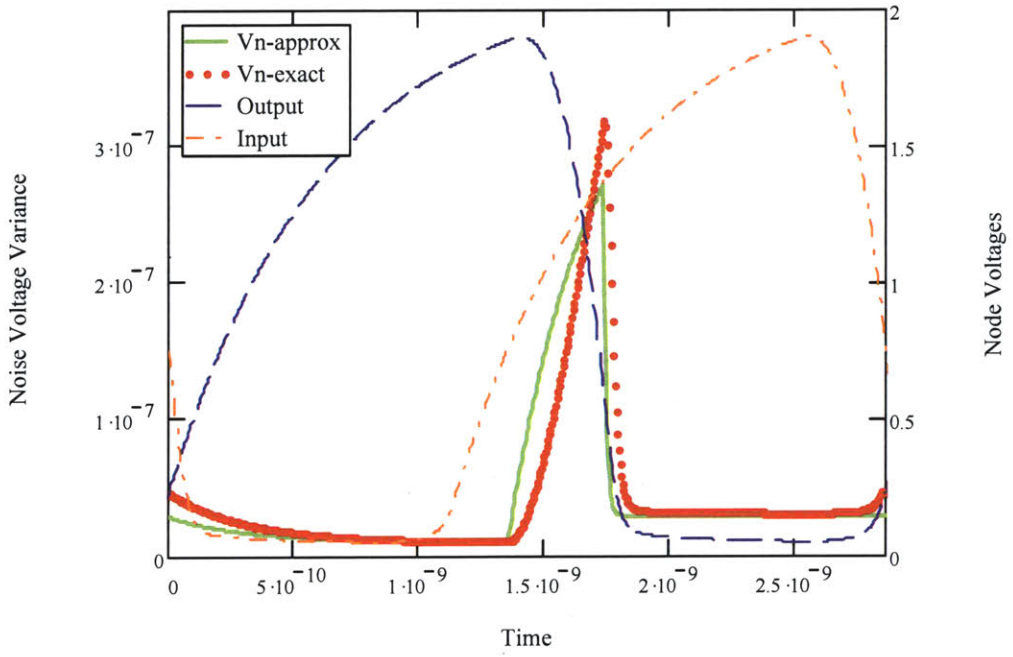

Figure 3 . 2 . 4 -- Comparison of piecewise constant noise prediction to near continuous calculation

During regions I and III, the piecewise constant model is quite close to the near continuous model, owing to the reasonably constant noise parameters during those periods. The beginning and end of region III show some disagreement, which can be

attributed to the fact that the output voltage is high enough to alter the drain-source conductance significantly from the value used in the piecewise constant model. Region II is where the most discrepancy lies since the MOSFET noise current density is changing rapidly during that time; however the piecewise model is still reasonably close and at least shows the general trends present as the oscillator progresses through each state.

The progression from a piecewise constant to a nearly continuous model can be taken one step further with a little work on equation 3.2.7. If we use a first order Taylor approximation for e^x, we can make the following substitution:

$$1 - e^{\frac{-2\Delta t_i}{R_i C_i}} \rightarrow 1 - 1 + \frac{2}{R_i \cdot C_i} \cdot \Delta t_i \rightarrow \frac{2}{R_i \cdot C_i} \cdot \Delta t_i$$

Resulting in:

$$\overline{v_n^2} = \sum_{i=0}^{m} \left(\frac{\left(\overline{i_n^2}\right)_i}{C_i^2} \cdot \Delta t_i \cdot e^{-2 \sum_{j=i+1}^{m} \frac{\Delta t_j}{R_j C_j}} \right), \qquad \text{(Eqn. 3.2.9)}$$

And finally taking the limit as Δt_i goes to zero for all i, j:

$$\overline{v_n^2}(t) = \int_0^t \frac{\overline{i_n^2}(\tau)}{C(\tau)^2} \cdot e^{\int_\tau^t \frac{-2}{R(\tau_2) C(\tau_2)} d\tau_2} d\tau, \qquad \text{(Eqn. 3.2.10)}$$

Equation 3.2.10 has the potential of giving us analytic solutions to the noise generation of any oscillator where we can determine the time dependence of the noise current density and load impedance. Unfortunately, in many cases it is infeasible to

determine the analytic time dependence[17] of those parameters and in some cases there may be no analytic solutions to the integrals in equation 3.2.10 even when the time dependences are known. For region II in our ring oscillator the load characteristics are constant and we can determine the time dependence of the noise current, hence we are able to derive an analytic solution. With R and C being constant in this region, equation 3.2.10 simplifies to

$$\overline{v_n^2}(t) = \int_0^t \frac{\overline{i_n^2}(\tau)}{C_L^2} \cdot e^{\frac{-2(t-\tau)}{R_L \cdot C_L}} \, d\tau \qquad \text{Where} \qquad \overline{i_n^2}\cdot(\tau) = 2 \cdot k \cdot T \cdot \gamma \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot \left(V_{gs}(\tau) - v_T\right)$$

Note that we are ignoring the noise contribution from the load resistor for the moment since it is constant and can be determined from the second part of equation 3.2.4. When this stage is in region II, the preceding stage driving it is in region I and the overdrive voltage relaxes toward the positive supply allowing us to replace $V_{gs}(\tau)$-v_T as follows assuming a time origin of 0 at the beginning of region II:

$$V_{gs}(\tau) - v_T = \left(V_s - v_T\right)\left(1 - e^{\frac{-\tau}{R_L \cdot C_L}}\right)$$

After performing the substitutions and working out all of the math, the end result is that the noise caused by the transistor in region II is:

$$\overline{v_n^2}(t) = 2 \cdot \frac{k \cdot T}{C_L} \cdot \gamma \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot R_L \cdot \left(V_s - v_T\right) \cdot e^{\frac{-2 \cdot t}{R_L \cdot C_L}} \cdot \left(\frac{1}{2} + \frac{1}{2} e^{\frac{2t}{R_L \cdot C_L}} - e^{\frac{-t}{R_L \cdot C_L}}\right), \quad \text{(Eqn. 3.2.11)}$$

Figure 3.2.5 below shows the noise predictions for regions I and II using the near continuous model and the analytic solution composed of equations 3.2.4 and 3.2.11.

[17] remember, simply knowing the voltage dependence of an element is not sufficient, we must also know the exact time dependence of the node voltages, which may not be continuously differentiable curves.

Ignoring the different initial conditions which are a result of the deviation of the two models at the end of region III, the two noise curves line up almost exactly, particularly in region II where we are interested the noise during switching.

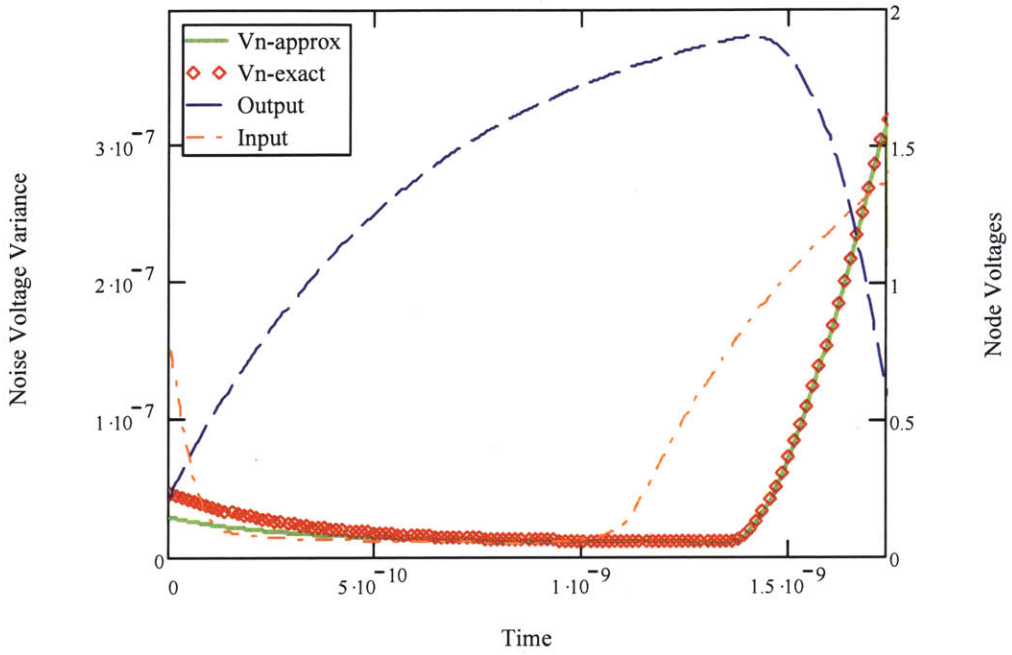

Figure 3 . 2 . 5 -- Comparison of near continuous model to analytic solution in regions I and II

Region III is much more difficult to characterize this way, as the gate voltage is not a simple function of time as it was in region I, and we don't have an analytic description of the drain voltage response which determines the noise response while the transistor is in the triode region.

The last tool we need for determining the period variation of our oscillator is a mechanism for converting the voltage noise at the output node into switching jitter. One popular method, and the method used in this work, for doing this in ring oscillators is to use the first-crossing approximation [3].

$$\overline{\Delta t^2} = \overline{v_n^2} \cdot \left(\frac{d}{dt} v \right)^{-2} , \quad \text{(Eqn. 3.2.12)}$$

The idea behind the first-crossing approximation is that the timing uncertainty at a particular point in time is related to the voltage uncertainty by the slope of the node voltage as illustrated in figure 1.2 in chapter 1. When the voltage is changing quickly large variations in the voltage result in small timing variations; suggesting that shaper transitions will result in less jitter. This is somewhat misleading however, since in order to maintain the same oscillation frequency, sharper transitions require integrating more transitions, each with their own noise.[18] As we will see in the next section, attempting to make the falling transitions excessively sharp will eventually increase the normalized oscillator jitter.

3.3 Effects of Stage Gain:

Now that we have a good idea of what the voltage noise looks like throughout the oscillator period and how that translates to timing jitter, we can begin studying the effects of changing device parameters. The first modification to be examined is the effect of changing the nominal single stage gain. The effective stage gain can be changed in several ways such as altering the transistor dimensions, using low threshold devices, changing the load resistance, or using CMOS processes with different carrier mobilities[19]. While all of these changes affect the overall gain, they also have subtle side-effects that are different for each parameter. For example, changing the transistor dimensions changes the total load capacitance which in turn changes the oscillator period and the

[18] In buffers, however, sharper transitions will indeed reduce jitter, as long as the noise voltage is not increased significantly

[19] While C_{ox} could also be changed, it affects the gate capacitance for equal sized devices, and ultimately would be equivalent to changing the transistor dimensions.

small signal noise response; while altering the transistor threshold changes the dynamics of the oscillator waveforms by altering the conditions for the MOSFET entering triode and cutoff regions. In practice designers typically do not have the luxury of choosing any carrier mobility for their devices, however the same net effect can be accomplished through changing device sizes and appropriately reducing the added load capacitance, or by altering W and L subject to the constraint that their product, and hence to first order the gate capacitance, remains constant[20]. As a result we use the carrier mobility to alter the stage gain since it provides the simplest method of doing so without significantly affecting the rest of the oscillator.

As we saw in section 3.1, increasing the gain increases the frequency in addition to deforming the oscillator waveform. This complicates matters somewhat since while 1ps of jitter may be inconsequential for an oscillator period of 1μs, it is quite noticeable for an oscillator period of 1ns. Trying to maintain the same oscillation frequency while changing the gain would require making changes to the load characteristics, which is undesirable since that will in turn affect the period jitter. So instead of trying to fix the oscillation frequency as the gain is changed, we instead focus on the normalized period jitter.

As noted in the previous section, the total period jitter is composed of the rising and falling edge jitter from each individual stage. Looking at the rising edge of the oscillator waveform, one might be tempted to assume that the rise jitter is unaffected by the stage gain as the rising edge occurs in region I where the transistor is cutoff. If we go back to equation 3.2.4, however, we are reminded that the residual noise from region III

[20] This will depend on the relative magnitudes of the oxide capacitance and overlap parasitics; this also assumes that the output resistance of the transistor is very large relative to the load resistor.

requires a finite amount of time to decay below the nominal region I noise level. Additionally, the increased gain lowers the effective switch point since less gate overdrive is required to switch the next stage. Moving the switch point down also directly affects the induced timing jitter since the rising slope will be larger at the beginning of region I, and from equation 3.2.12 we know that increasing the slope decreases the jitter for a fixed noise voltage. From combining equations 3.2.4 and 3.2.12, we have a good idea of the switching jitter on the rising edge:

$$\overline{\Delta t_r^2}(t) = \frac{k \cdot T \cdot R_L^2 C_L}{(V_s - V_{low})^2} \cdot \left(e^{\frac{2t}{R_L \cdot C_L}} - 1 \right) + \frac{R_L^2 \cdot C_L^2 \cdot \overline{v_n^2}(0)}{(V_s - V_{low})^2}, \quad \text{(Eqn. 3.3.1)}$$

Normalizing equation 3.3.1 in the general case becomes difficult as we do not have a closed form solution for the oscillator period as a function of the stage gain, and as a result, we do not know the exact dependences of the switch point and $v_n^2(0)$ either. The switch point can be reasonably approximated by the gate voltage at which the MOSFET drain current is equal to the mid-supply resistor current:

$$V_{sw} = v_T + \sqrt{\frac{V_s \cdot L}{R_L \cdot \mu \cdot C_{ox} \cdot W}}, \quad \text{(Eqn. 3.3.2)}$$

From which we get the switching time to be:

$$t_{sw} = -R_L \cdot C_L \cdot \ln\left(\frac{V_s - V_{sw}}{V_s - V_{low}} \right), \quad \text{(Eqn. 3.3.3)}$$

And substituting into equation 3.3.1 results in:

$$\overline{\Delta t_r^2}(t) = \frac{k \cdot T \cdot R_L^2 C_L}{(V_s - V_{low})^2} \cdot \left[\left(\frac{V_s - V_{low}}{V_s - V_{sw}} \right)^2 - 1 \right] + \frac{R_L^2 \cdot C_L^2 \cdot \overline{v_n^2}(0)}{(V_s - V_{low})^2}, \quad \text{(Eqn. 3.3.4)}$$

The absolute jitter deceases with increasing gain, since the switch point t occurs earlier, V_{low} is lower, and the residual noise voltage is smaller. As demonstrated at the end of this section, however, the period decreases faster than the rising edge jitter after a certain point, indicating that there will be an optimal gain point. This will be examined further after we look at the jitter caused during the falling edge.

Before we can determine the falling edge jitter, we need to derive the voltage waveform to determine the time when switching occurs. Solving equation 3.1.2 under the conditions of region II gives us the output voltage as a function of time and the initial voltage at the beginning of region II:

$$V_{out}(t) = V_s - \left(V_s - V_{out}(0)\right)e^{\frac{-t}{R_L \cdot C_L}} - \frac{\mu \cdot C_{ox} \cdot W}{2C_L \cdot L}\left(V_s - v_T\right)^2\left[R_L \cdot C_L - 2t \cdot e^{\frac{-(t)}{R_L \cdot C_L}} - R_L \cdot C_L \cdot e^{\frac{-2(t)}{R_L \cdot C_L}}\right]$$

(Eqn. 3.3.5)

There is no analytic solution to equation 3.3.5 for the switch time as a function of the switch voltage since the equation is transcendental. So again we will try to gain some insight from these equations, but will ultimately have to resort to numerical results to confirm and refine our predictions. When we combine equations 3.2.11 and 3.1.2 for

$$\overline{\Delta t_f^2}(t_{sw}) = \frac{\frac{k \cdot T}{C_L} \cdot \left[\gamma \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} R_L \cdot \left(V_s - v_T\right) \cdot \left(1 - 2e^{\frac{-t_{sw}}{R_L \cdot C_L}} + e^{\frac{-2t_{sw}}{R_L \cdot C_L}}\right) + 1\right]}{\left[\frac{V_s - V_{sw}}{R_L \cdot C_L} - \frac{\mu \cdot C_{ox} \cdot W}{2 \cdot C_L \cdot L}\left(V_s - v_T\right)^2 \cdot \left(1 - 2e^{\frac{-t_{sw}}{R_L \cdot C_L}} + e^{\frac{-2t_{sw}}{R_L \cdot C_L}}\right)\right]^2}, \quad \text{(Eqn. 3.3.6)}$$

region II as we did for the rising edge we get a fairly complicated result in equation 3.3.6. If we assume that the second term in the denominator is large relative to the first, which

seems reasonable as at the switching point the output voltage is falling, we can loosely approximate equation 3.3.6 as shown in equation 3.3.7.

$$\overline{\Delta t_f^2}(t_{sw}) = \frac{4 \cdot k \cdot T \cdot C_L \cdot \gamma \cdot L \cdot R_L}{\mu \cdot C_{ox} \cdot W \cdot (V_s - v_T)^3 \cdot \left(1 - 2 \cdot e^{\frac{-t_{sw}}{R_L \cdot C_L}} + e^{\frac{-2 \cdot t_{sw}}{R_L \cdot C_L}}\right)}, \qquad \text{(Eqn. 3.3.7)}$$

By the same token, the first term in the numerator is assumed to dominate the second. Equation 3.3.7 shows that the falling edge jitter appears to decrease for increasing gain, although we don't know the explicit dependence of t_{sw} on the stage gain.

The peak voltage and overall oscillation period can be solved for iteratively by using equation 3.3.5 to estimate the fall time, then using the fall and rise times to estimate the peak output voltage. Usually two or three iterations are sufficient to determine both the peak voltage and oscillation period.

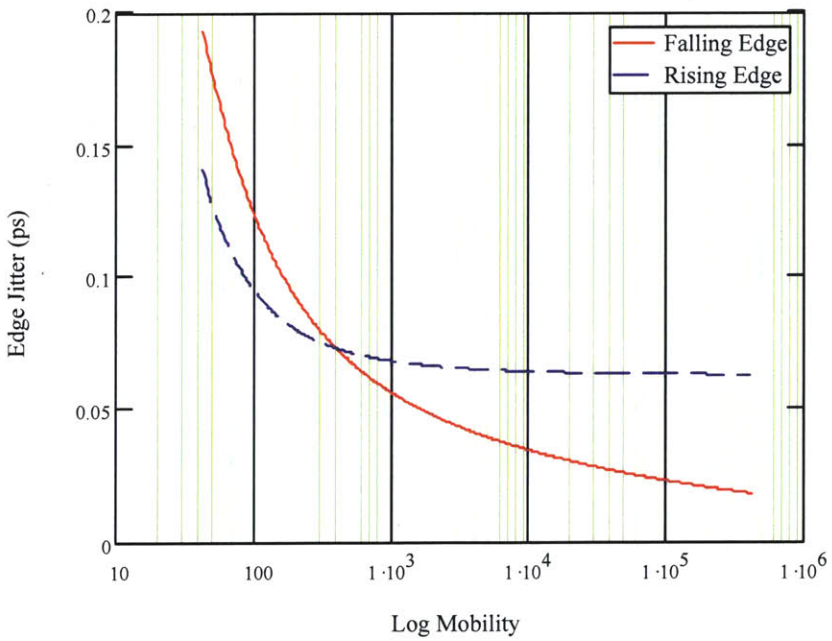

Figure 3 . 3 . 1 -- Absolute edge jitter for various values of carrier mobility

Combining that with equations 3.3.4 and 3.3.6 we can quickly solve for the normalized timing jitter for each edge for any given value of k for the pull-down

MOSFET. Figure 3.3.1 above shows the estimated absolute jitter for the rising and falling edges for our oscillator.

For low gain configurations the falling edge jitter is larger than the rising edge jitter since the two slopes are of comparable magnitude, yet the falling edge has added noise current from the MOSFET, which is not on during the rising edge. When the gain is increased enough, the falling edge is so sharp it no longer adds very much timing jitter compared to the rising edge, which levels off as the switch point cannot move below the transistor threshold voltage. Figure 3.3.2 shows the rising and falling edge jitters along with the total period jitter normalized to the oscillation period.

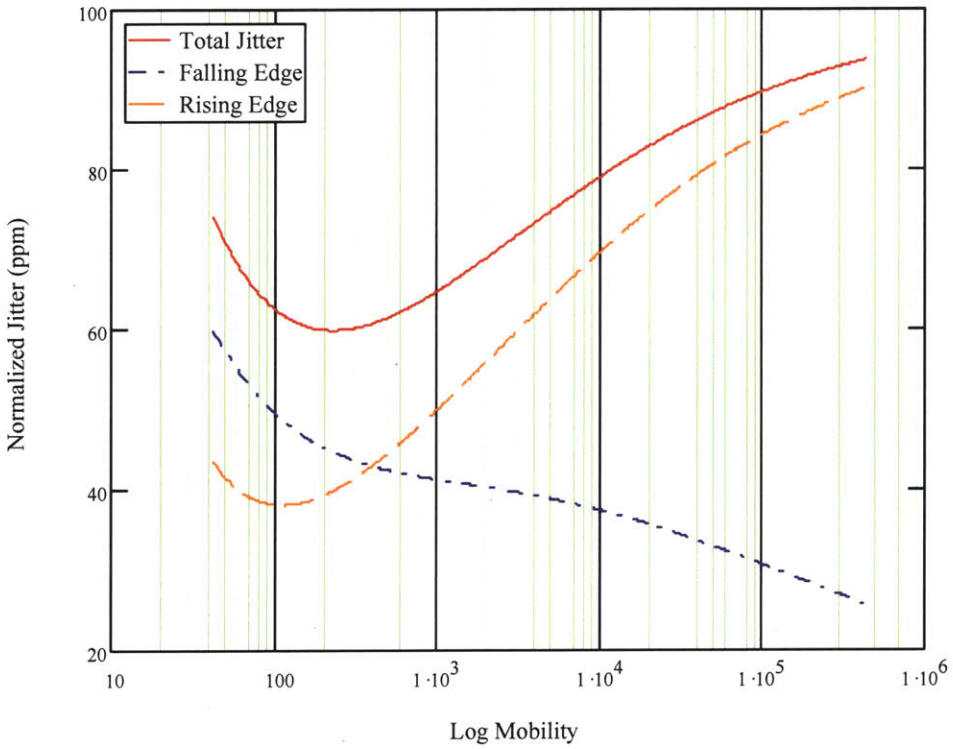

Figure 3 . 3 . 2 -- Normalized period jitter, along with rising and falling edge components

As suspected there is an optimal gain point at a carrier mobility of about $250\frac{cm^2}{V \cdot s}$, corresponding to a small signal gain of about 6 at the switch point. The falling edge jitter continues to decrease with increasing gain, even when normalized to the oscillator period.

The rising edge jitter, on the other hand, clearly levels off long before the oscillation frequency does, resulting in increasing relative jitter until the frequency also levels off. It should be noted that the predictions for very high gains are likely to be inaccurate because in those cases the transistor will be in moderate and weak inversion for significant amounts of time. Entering moderate and weak inversion requires changing the models for both the noise current density and the triode region drain conductance.

When we consider the changes in power consumption the precise optimal point may move somewhat, but keep in mind that the oscillation frequency is also changing, and for a fixed load capacitance more power is inherently required to increase the frequency of operation. The difference in efficiencies between different gain setting stems from the "static" power dissipation of each stage when it is held in the low state. While the fraction of the oscillation that a particular stage is low remains roughly constant, the power dissipation changes slightly as the low state voltage is pulled lower for higher gain, in turn pulling more current through the load resistor. The optimal efficiency point should occur at a slightly lower gain than what was predicted above due to the increasing power dissipation.

Looking back at equation 3.1.2, if we multiply through by R and hold the gain constant, whether by μ or W and L, then the RC product time scales the oscillation waveforms, but does not alter the dynamics. The noise calculation behaves similarly; it is dependent on the gain term, but not the individual g_m and R values, other than a scale factor of 1/C out front as we would expect from traditional noise analysis. As such, the optimal gain point is not dependent on the load resistance and capacitance; although it is dependent on the value of the excess noise factor γ, and the number of stages. The net

result is that we have the necessary degrees of freedom to make an optimal oscillator under arbitrary frequency and noise specifications[21]. The capacitance sets the overall noise level, while g_m and R can be traded off to get the desired frequency while maintaining the optimal gain setting.

[21] This is of course subject to the physical limitations of fabricating the oscillator such as minimum gate length, maximum die area, etc.

Chapter 4

Differential Ring Oscillators

While single-ended ring oscillators certainly have their place, designers often prefer to use differential designs for a few important reasons. Among the reasons for using differential rings in place of single-ended rings are increased common-mode rejection, trivial signal inversion, and supply independence. The common-mode rejection is particularly useful in communications and other high frequency circuits where electromagnetic interference (EMI) can couple into the oscillator causing unwanted jitter. Furthermore, the differential signal is useful for balanced mixers and digital systems where a designer may want both polarities of a control signal, as the oscillator signal can be inverted by simply swapping the positive and negative terminals. Perhaps the most important advantage as far as this work is concerned is the supply independence provided by a differential architecture. As is shown in the next section, the oscillation frequency is determined by the RC time constant of the load and the relative sizing of the switching transistors to the bias current, independent of the supply voltage[22]. This in effect greatly reduces one mechanism of incorporating supply noise into timing jitter, as compared to

[22] To first order, assuming the bias current is designed with a sufficiently large output resistance

the single-ended case where changing the supply voltage directly changes the nominal oscillation frequency. The other mechanism is direct signal coupling from the supply to the oscillator nodes; in the differential case this is also greatly reduced as the supply noise couples in the common mode, not the differential mode.

This chapter takes the noise analysis techniques developed in chapter 3 for single-ended ring oscillators and extends them for use with differential ring oscillators. As in chapter 3 we begin with a very simple design in the hopes of gaining better intuition about what aspects of the oscillator design impact the overall timing jitter the most. After investigating the differences between the single-ended rings of chapter 3 with the differential ones presented here, an example oscillator will be designed to demonstrate the use of this noise analysis. Additionally, other aspects of the oscillator design will be discussed, particularly those that may significantly affect the noise performance, such as tuning methods and biasing.

4.1 Resistor Loaded Differential Pair:

Following in the same light as chapter 3, the simplest differential oscillator to be considered is a multistage resistor loaded differential amplifier with unity feedback. Each stage of the oscillator is composed of a source coupled differential pair, biased by a current source, and loaded by equal valued resistors and capacitors. Unlike the single-ended version, this oscillator can accommodate even numbers of stages by swapping one of the outputs to add an extra inversion. The main benefit of this comes from using an

oscillator with four stages to generate quadrature signals. Figure 4.1.1 below shows one of the individual gain stages.

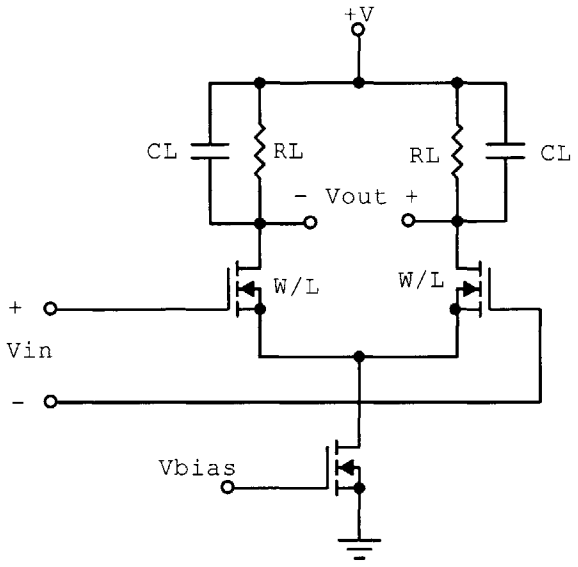

Figure 4 . 1 . 1 -- Individual differential gain cell

For the analysis presented here we assume the signal swing is not large enough to force the bias current source into the triode region, since doing so would compromise the common-mode rejection that makes the differential architecture so desirable. As a result, the load impedance characteristics are constant throughout the oscillation cycle, unlike the single-ended case, where the pull-down transistor is forced deep into the triode region. Equation 3.2.10 reduces to the same equation that was used for regions I and II in chapter 3, where only the noise current density is varying.

$$\overline{v_n^2}(t) = \int_0^t \frac{\overline{i_n^2}(\tau)}{C_L^2} \cdot e^{\frac{-2(t-\tau)}{R_L \cdot C_L}} \, d\tau \quad \text{(Eqn. 4.1.1)}$$

To make use of equation 4.1.1 we need to establish the nature of the time-varying noise current at the differential output node. Doing so requires that we first determine the

nominal output waveforms in the absence of any noise. The differential equations governing each of the output nodes are nearly the same as they were in chapter 3; however, the pull-down current depends on both input voltages. Since we are only interested in the differential mode signal at this time, we can combine the two equations for each amplifier stage by subtracting them, leaving us with equation 4.1.2:

$$C_L \cdot \frac{d}{dt} V_{diff} = \frac{V_{diff}}{R} - h\left(V_{in1}, V_{in2}, V_{out1}, V_{out2}\right), \qquad \text{(Eqn. 4.1.2)}$$

In general the differential current is a function of each input and output voltage, but if we limit ourselves to oscillators with moderate signal amplitudes that do not force the bias transistor into the triode region the differential current is only a function of the differential input voltage. Most practical differential ring oscillators adhere to this, so the assumption is not as limiting as it may sound and it greatly simplifies the analysis. For large differential inputs, the output current is limited in magnitude by the bias current source. The transition from positive to negative I_{bias} depends on the inversion level the switching MOSFETs are biased. Under the assumption that the switching transistors are in saturation, the differential output current can be solved for in terms of the input voltage as:

$$\begin{aligned} I_{out} &= I_{bias} - \frac{\mu \cdot C_{ox} \cdot W}{4L} \cdot \left(V_{in} - \sqrt{\frac{4 I_{bias} \cdot L}{\mu \cdot C_{ox} \cdot W} - V_{in}^2} \right)^2, && |V_{in}| < \sqrt{\frac{2 I_{bias} \cdot L}{\mu \cdot C_{ox} \cdot W}} \\ I_{out} &= I_{bias} \cdot sign(V_{in}), && |V_{in}| \geq \sqrt{\frac{2 I_{bias} \cdot L}{\mu \cdot C_{ox} \cdot W}} \end{aligned} \qquad \text{(Eqn. 4.1.3)}$$

Figure 4.1.2 on the next page shows an example of this transfer characteristic. Along with the exact solution, there are also two approximate solutions. The dashed line shows the linear approximation where the transconductance is treated as constant while the output current is smaller than the bias current. The dotted line uses the exponential

solution that would be exact for a bipolar switching stage, with the thermal voltage scaled to provide the same transconductance in the balanced state. The former makes the math much simpler for evaluating the differential equations governing the oscillator waveforms, while the latter may provide a more accurate prediction as the switching stage is biased closer to moderate and weak inversion.

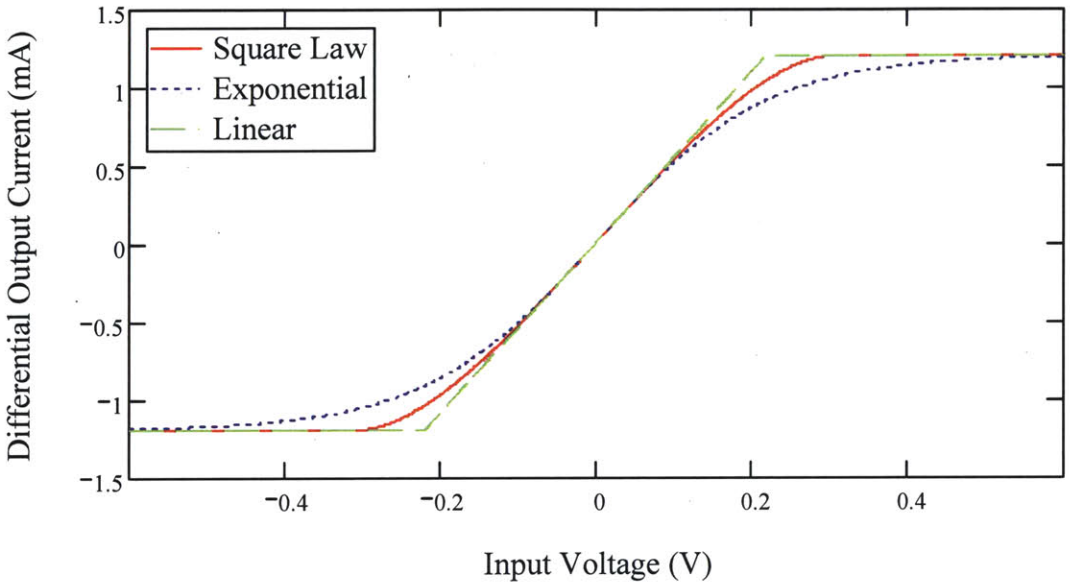

Figure 4 . 1 . 2 -- Differential I-V characteristic for current source biased differential pair

Armed with the I-V characteristic of our switching transistors, we can move forward to determining the noise current present at the output during each part of the oscillation cycle. In the differential case, there are more noise sources to consider: two from the load, two from the switching pair, and one from the bias current source. We treat the load sources as constant for this analysis just as we did in chapter 3, although for more complicated topologies they may change. The bias noise source is also treated as a constant; however, it is important to remember that its contribution to the net differential output current noise will not be constant. The two noise sources for the switching transistors are the most complicated ones to analyze, since both of their magnitudes

change and their transfer characteristics to the output noise change, depending on the input voltage. Figure 4.1.3 shows the relevant noise sources for an individual stage.

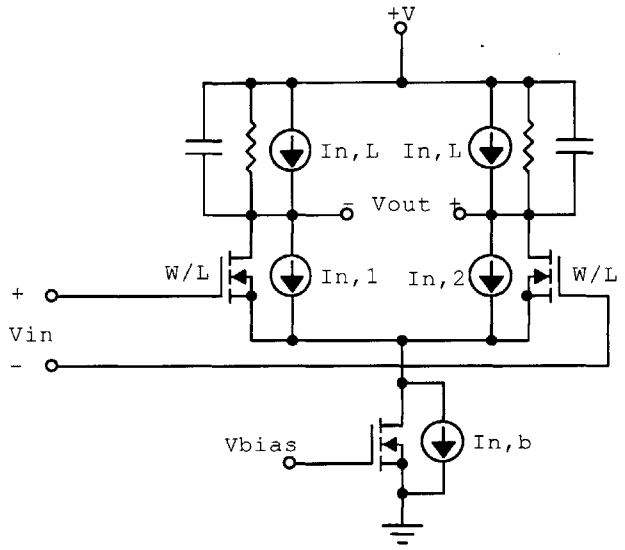

Figure 4 . 1 . 3 -- Individual oscillator stage with noise sources shown explicitly

When the input voltage is zero the differential pair is in its balanced state and each transistor carries half the bias current. In this state, any noise current from the bias transistor splits evenly between both outputs and as a result contributes nothing to the differential output current. As the input voltage deviates from zero, the bias current begins to shift more to one side than the other, and correspondingly the bias noise current will split preferentially toward that side. Now that the bias current noise splits unevenly, there will be a net differential noise current at the output. Using a linearized small signal model we can determine what portion of the bias current flows to each side of the output, and from that determine the net output current. At the drain of the bias transistor an incremental current sees the output conductance of the current source in parallel with the source conductances of the two switching transistors. In essence we have a current divider where each branch draws a percentage of the current equal to its conductance

over the total conductance. The output conductance of the bias current source will typically be much smaller than the source conductances of the differential pair, so we will treat it as zero here. For a given g_{m1} and g_{m2} the net output current contribution from the bias is[23]:

$$I_{nbo} = \left(\frac{g_{m1}}{g_{m1} + g_{m2}}\right)\cdot I_{nb} - \left(\frac{g_{m2}}{g_{m1} + g_{m2}}\right)\cdot I_{nb} = \left(\frac{g_{m1} - g_{m2}}{g_{m1} + g_{m2}}\right)\cdot I_{nb} \quad , \qquad \text{(Eqn. 4.1.4)}$$

The contribution from the differential pair transistors is a bit more complicated since the noise current generated by those transistors appears at the output both directly and indirectly through the source coupled node. The indirect contribution behaves in the same manner as the bias current noise except that its sign will be flipped since relative to the direct contribution.

$$I_{n1o} = \left(1 - \frac{g_{m1}}{g_{m1} + g_{m2}}\right)\cdot I_{n1} - \left(\frac{-g_{m2}}{g_{m1} + g_{m2}}\right)\cdot I_{n1} = \left(\frac{2g_{m2}}{g_{m1} + g_{m2}}\right)\cdot I_{n1} \quad , \qquad \text{(Eqn. 4.1.5)}$$

The equation for the second transistor is the same as 4.1.5, but with the subscripts 1 and 2 switched. An important thing to notice here is that when the differential pair is fully switched to one side, neither transistor contributes any noise to the output. For example, when all the bias current passes through the first transistor, g_{m2} is zero and all of M1's noise is cancelled out, and with g_{m2} being zero the second transistor doesn't generate any noise to begin with. Combining equations 4.1.4 and 4.1.5 and taking account of the fact that the MOSFET noise currents are dependent on their g_m's, the total differential noise current at the output due to the active devices is:

$$\overline{I_{no}^{\,2}} = 2\gamma\cdot k\cdot T\cdot\left[\left(\frac{2g_{m2}}{g_{m1} + g_{m2}}\right)^2\cdot g_{m1} + \left(\frac{2g_{m1}}{g_{m1} + g_{m2}}\right)^2\cdot g_{m2} + \left(\frac{g_{m1} - g_{m2}}{g_{m1} + g_{m2}}\right)^2\cdot g_{mbias}\right] \quad , \qquad \text{(Eqn. 4.1.6)}$$

[23] Here we are also assuming the frequency of the noise current is below the f_T of the MOSFET, which is a safe bet since the RC time constant would filter out frequencies that high anyway.

Keep in mind that we are still using the double-sided noise current density for our time domain analysis; hence, the factor of 2 appears out front instead of 4. It should also be noted that the g_{mbias} term represents the overall transconductance of the bias current source, including the effects of noise from the bias circuitry and any source degeneration. Figure 4.1.4 shows a typical breakdown of the noise contributions from each element over the course of one oscillator cycle.

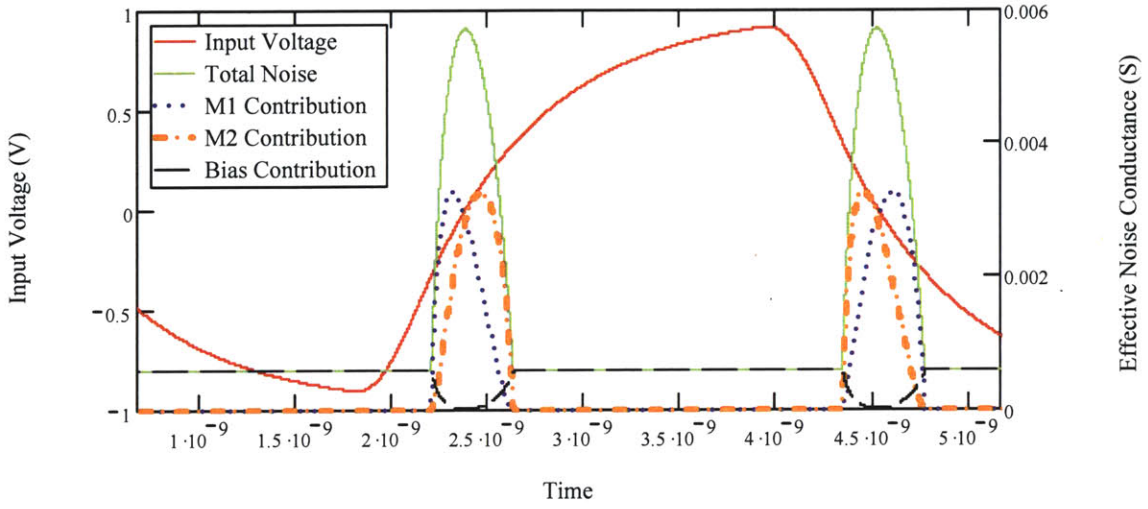

Figure 4 . 1 . 4 -- Sample oscillator waveform, with active noise current contributions

For large input voltages, the stage is fully switched to one side or the other, and the bias current noise dominates the output noise. As the input voltage crosses zero, the switching transistors take over and reject the bias noise. Increasing the gain[24] of the differential pair increases the noise current during switching, but not during times when the stage is fully switched. One might be tempted to assume this means that increasing the stage gain automatically increases the period jitter, but increasing the gain also narrows the window of input voltage where the stage is not fully switched. As a result, the effect of changing the stage gain is much more subtle. The peak noise voltage is

[24] Note that in the differential case the gain refers to transconductance relative to the bias current

roughly proportional to the area under the noise current curve[25], but the amount of time between the burst of increased noise and the next-stage-switching also changes with the stage gain. Figure 4.1.5 below shows the evolution of the noise voltage throughout the oscillator cycle. As before, the noise voltage is reset when the output switches, since under our first crossing approximation we know the voltage to be precisely zero whenever it triggers the next stage. The effect of resetting the noise voltage appears to be minimal however, since the oscillator period is several time constants long even for large gains.

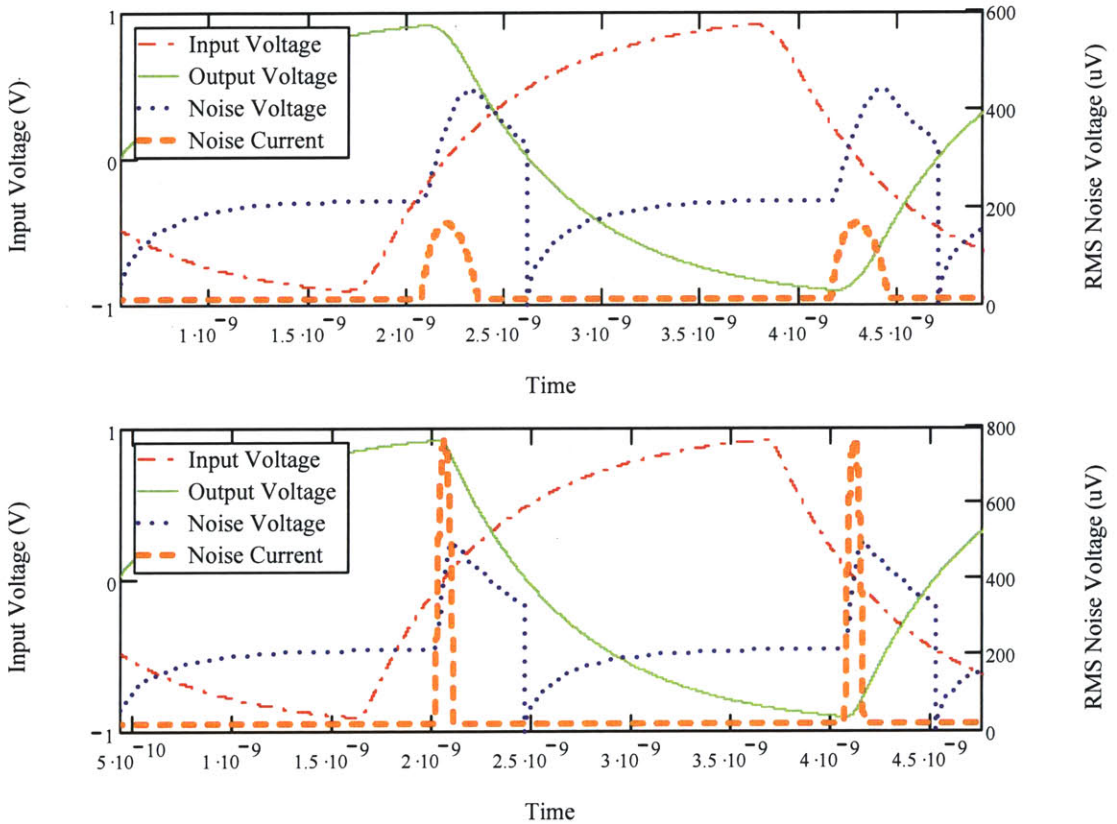

Figure 4 . 1 . 5 -- Noise current and resulting noise voltage for moderate (top) and high (bottom) gain cases

Unlike the single-ended oscillators examined in chapter 3, the switch point for the differential oscillator is not dependent on the stage gain. In all but the lowest gain cases,

[25] This is true when the integration interval is small relative to the RC load time constant, as the interval is increased the noise voltage tends toward being proportional to the height of the curve instead of the area

the stage is fully switched prior to the output switching as seen in figure 4.1.5, so the slope of the output voltage stays roughly at $\frac{I_{bias}}{C_L}$, independent of the stage gain. It is no surprise that increasing the gain results in an increase in the relative jitter for a while, and then levels off: the differential pair becomes indistinguishable from an ideal switch that introduces a fixed area impulse of noise current into the oscillator output. The area of interest to us is the low to moderate gain region where we hope to find an optimal gain setting before the signal swing begins shrinking, causing a jump in the timing jitter.

Since the output drive current is assumed to be only a function of the input voltage, the differential equation governing the output (4.1.2) is a separable equation and can be solved under piecewise constraints using the linear approximation to equation 4.1.3. As in chapter 3 the result is transcendental with respect to time, and requires using numerical methods to solve for the stage delay and RMS noise voltage.

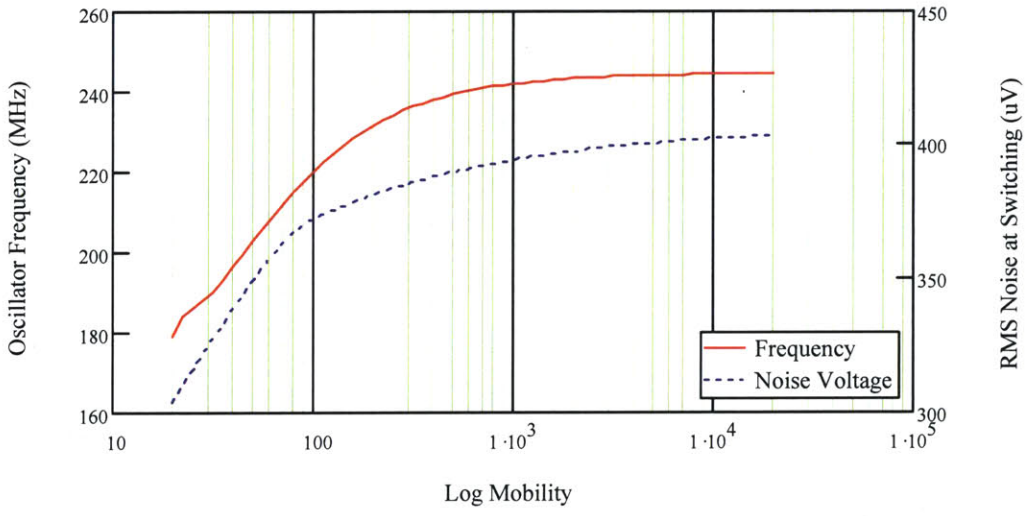

Figure 4 . 1 . 6 -- Oscillator frequency and switching noise voltage for increasing g_m but fixed I_{bias}

Despite not being able to glean much intuition from the equations themselves, we can still examine the numerical results and make sense out of any trends present. Figure

4.1.6 above illustrates how the noise and oscillation frequency change as the transconductance of the input stage is increase for a fixed bias current. For large stage gains, the output noise stays relatively stable, despite the increasing noise current from each switching transistor. For smaller gains, the bias noise is rejected by the balanced differential pair, and the switching transistors produce less noise themselves, lowering the overall noise level. As figure 4.1.7 below shows, however, eventually the decrease in the sharpness of the switching transitions catches up with the noise voltage and causes the jitter to spike back up.

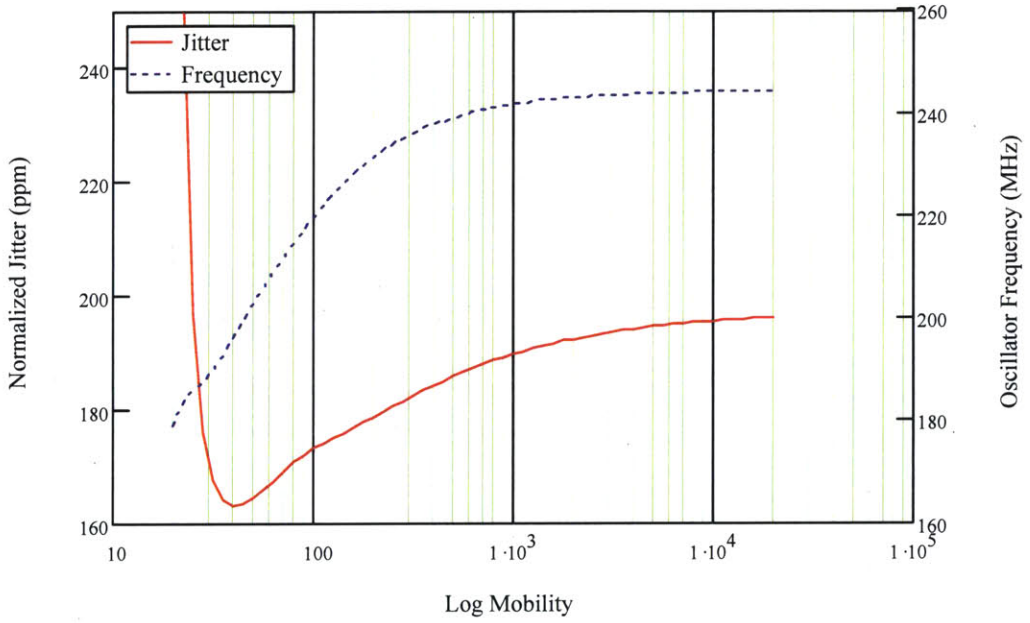

Figure 4 . 1 . 7 -- Normalized Jitter and Oscillation Frequency

The point where the normalized jitter occurs is at a mobility of $40\frac{cm^2}{V \cdot s}$, which corresponds to a ratio of .8 between the switching k and the bias k. There are a couple of important *caveats* to keep in mind here. As the gain decreases, eventually we find ourselves in a situation where the output stage begins switching the next stage before the input has fully switched the current stage. In that situation, there is amplification of noise

from one stage to the next, requiring a more complete model of the output noise than we have presented here. Further decreasing the gain lengthens the interval of overlap between active stages, but also decreases the magnitude of the effect as a direct result of the reduced gain. The tradeoff is similar in many respects to that of the noise during switching where the magnitude and duration of the noise contributions are acting opposite each other. The noise present at low gain will be somewhat higher than presented here, so the optimal gain point will likely be somewhat larger than predicted. Furthermore, when the active regions overlap, the output slope begins to decrease and causes the stage jitter to increase.

Simulations conducted on Linear Technology's .6μm CMOS process yield similar results, except that the optimal mobility point shifts upward by a factor of 2. The differences can be attributed in part to the effects of noise the amplification between overlapping stages present for low gains as mentioned before. Another important difference to account for is the effect of the back bias on the switching transistors. In the single-ended case we analyzed in chapter 3, the pull-down transistor had a grounded source, so while the body effect was still present, there was not the additional effect of having a non-zero V_{bs}. In this case the bodies of the switching transistors will be grounded, while the source node will be above ground, altering the threshold voltage.

4.2 Example Oscillator Design

At this point we will use the results of our non-linear noise analysis to design a low noise ring oscillator. This example design also provides an opportunity to discuss tuning methods and biasing, and how they can affect the oscillator's overall noise performance. We would like a differential ring oscillator with a center frequency of 225MHz and a maximum power dissipation of 7mW using a standard .6μm CMOS process and a 2.1 volt power supply. Additionally, we would like to be able to tune the oscillator across a full octave, in this case a range of approximately 150-300 MHz.

This design is limited to using a 5 stage oscillator, since the analysis performed in this study is focused mostly on 5 stage oscillators. At this time we also switch to using a PMOS switching topology. Mathematically, there is no intrinsic difference between using PMOS or NMOS in this type of oscillator; however, PMOS transistors typically have better noise performance than their NMOS counterparts. The reason for this is not entirely known, but there is speculation that it has to do with the reduced carrier mobility mitigating the short channel effects that cause excess noise [16]. With a 7mW power budget from a 2.1V supply, we can use a bias current of 660μA in each stage. In order to ensure that the bias transistor remains in saturation throughout the oscillation cycle, the bias current source transistor should be biased with a fairly low overdrive voltage. A bias voltage of .8V (1.3V below the supply) provides an overdrive of roughly 400mV, leaving enough room to have an output voltage swing of around a volt. As a result, the bias transistor should be sized with a W/L ratio of 140, however we set the ratio to 180 to account for second order effects, like the body effect, that reduce the drain current. In a complete design the bias voltage would be produced by a current mirror for better robustness over process variation, but for simplicity we use a voltage source here. The

last parameter we need to establish for the bias portion is the gate length of the bias transistor. Picking a large gate length provides us with a high output resistance, and along with that good common-mode rejection, but at the cost of increasing the die area of the circuit. In this design a gate length of 1.8μm provides sufficient output resistance, without dramatically increasing the necessary die area.

From the analysis presented in section 4.1, we see that the noise performance for this type of oscillator is optimized when the switching and bias transistors have similar W/L ratios, so the switching transistors are set to have a W/L ratio of 180. The gate length for the switching transistors is chosen to be the minimum of .6μm since this is a high speed[26] design. The total load capacitance contributed by the differential pair can be computed from the oxide and overlap capacitances and is approximately 160fF. We want to maximize the signal swing without forcing the bias transistor into the triode region, which in this case amounts to about 1 volt of swing. For the bias current of 660μA chosen, the net load resistance should be 1.5kΩ.

In order to provide a mechanism for tuning the oscillation frequency, the resistance is composed of a fixed resistor in parallel with a triode region MOSFET whose drain to source resistance can be adjusted via its gate voltage. The reason for constructing the load this way is twofold; the first part is that letting the fixed resistor dominate the load helps preserve the linearity of the load characteristic, consistent with the assumptions made during our analysis; the second is that the tuning range can be limited to keep the VCO gain small. Keeping the VCO gain small helps insulate the oscillator from noise in the control voltage, which is especially beneficial in high bandwidth PLL environments where we cannot simply increase the bypass capacitance to reduce the

[26] high speed relative to the process technology

noise because of the bandwidth requirements. The load resistance is thus formed by the parallel combination of a 2kΩ fixed resistor and an NMOS transistor with a W/L ratio of 5, biased with between 1.5 and 2.1V at the gate.

To approximate the tuning range from this setup, we use the drain-source resistance of the NFET at the midpoint of the signal swing. This gives us an estimated tuning range of 315MHz – 490MHz, however the actual center frequency will be lower due to the added load capacitance from the tuning FETs, and the range will be smaller because as the signal nears its maximum swing, the FET resistance increases quickly and the resistance is effectively that of the fixed resistor. As a result changing the bias voltage of the tuning FETs only alters the natural response for a portion of the cycle.

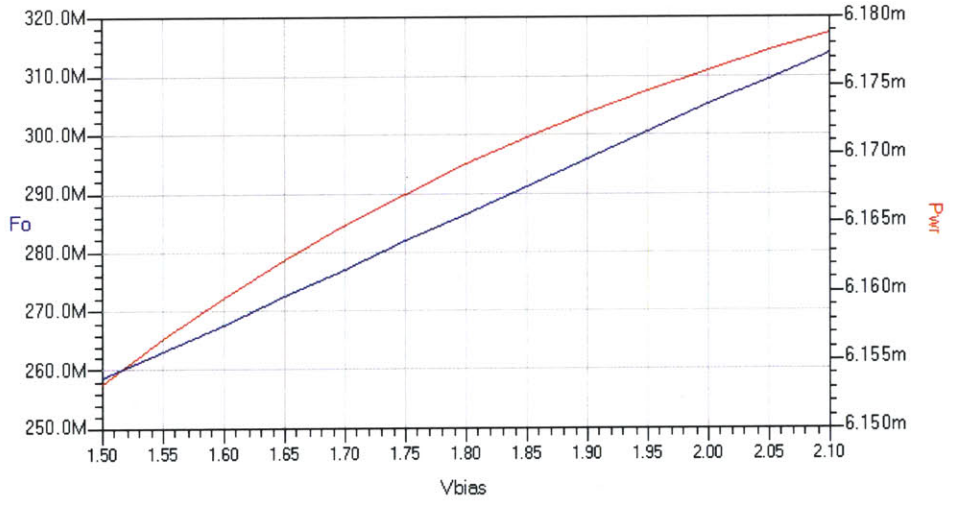

Figure 4 . 2 . 1 -- Simulated oscillator frequencies for various tuning voltages

Figure 4.2.1 above shows simulations of the actual tuning range to be 259MHz-314MHz, or 21%, for the specified tuning voltage range. In order to meet the desired overall tuning range of an octave, we can add switched capacitors at the outputs of each stage that are digitally controlled to select the local tuning range. The capacitors should

be sized such that there is sufficient overlap between adjacent digital codes to maintain continuous coverage over process and environmental variations.

Simulations of this example oscillator predict a total RMS period jitter of .394ps at the baseline frequency of 259MHz, which corresponds to a normalized jitter of 102ppm. For reference, this corresponds to a phase noise of -115.7dBc at a 1MHz offset, ignoring flicker noise contributions. This oscillator burns an average power of 6.15mW, and according to the work conducted by Navid and Lee it has a theoretical minimum phase noise of -128.6dBc at 1MHz, or a wastefulness factor of 12.9dB [17]. For a differential oscillator, this is a reasonably good result, especially for this simple oscillator design. This design highlights one of the main disadvantages in a differential oscillator design; the fixed current sources that bias each stage burn power and reduce the available signal swing, the overall result being a reduction in the available signal to noise ratio and "unused" power consumption. In comparison, single-ended ring oscillators typically have wastefulness factors around 2-6dB [17]. While this result suggests that single-ended ring oscillators are better than differential ones, it is important to remember that this analysis has only looked at the intrinsic noise performance of these oscillators. In real world circuits, supply noise, substrate noise, and EMI can all dominate the oscillator's noise performance. When all these external influences are considered, the differential oscillator will often prove to have better overall noise than the single-ended one, despite its initially higher jitter. The reader should keep in mind that the results presented for this oscillator are somewhat optimistic when comparing them to commercial solutions. In reality there are a number of noise contributors, such as bias circuitry and supply ripple, which are not intrinsic parts of the oscillator.

Chapter 5

Conclusions and Future Work

5.1 Summary and Conclusions:

This work has developed a method for determining the RMS noise voltage due to white noise sources at any time during an oscillator cycle. Beginning with a single-ended ring oscillator and simple MOSFET models in chapter 3, we derived analytic solutions for much of the oscillator period. When analytic solutions could not be found, iterative numerical approaches were taken that still provided useful results. Using this continuous noise model we were able to predict an optimal gain setting for a simple resistor loaded ring oscillator. As long as the stage gain is held constant, the oscillator waveforms are simply time scaled by the RC load constant. Consequently, the oscillation frequency and overall noise level can be set arbitrarily by trading off R and C values while maintaining the optimal gain. While only a very simple ring oscillator was used for the analysis in this work, the concept can be applied to more complicated designs. More complicated designs often will not lead to analytic solutions, but we still gain insight from observing patterns in the noise evolution. Chapter 4 took the techniques developed in chapter 3 and extended them to analyze differential ring oscillators. Again we were able to predict an optimal

bias setting for the switching pair relative to the bias current source. The differential stage is more complicated than the single-ended case since the magnitude of the bias current source noise alters the optimal gain point. When the bias noise is sufficiently small, high stage gains can be tolerated as the output noise is mostly dominated by the bias noise when the differential pair switches quickly. In cases where the bias noise is significant, lower gains (to a point) reduce the differential output noise as they spend more time in the balanced state where the bias noise is mostly rejected. Using the modifications from section 4.1, we then proceeded to walk through an example design of a differential ring oscillator which a predefined tuning range and power specification. While significantly simplified from a full on-chip oscillator design, the example provides a useful demonstration of the design process.

The noise model developed here, more than just useful for determining the overall period jitter, allows us to see how the noise voltage variance evolves over the course of an oscillation cycle. Similar to how the ISF function described by Hajimiri and Lee shows what regions of the oscillation cycle are most sensitive to injected noise [13], this model can help identify the dominant noise contributors. The advantage provided by the model developed in this work is that the noise can be determined without simulating the entire oscillator cycle for each time segment of injected impulse current. Once the oscillator waveform has been solved once, the rest of the noise calculation proceeds fairly quickly. The ability to visualize the growth and decay of output noise throughout the oscillator cycle allows designers to try to make targeted reductions in the noise response during sensitive portions of the cycle.

5.2 Recommendations for Future Work:

The nature of oscillator jitter is quite complex, and this work has only scratched the surface of this topic. There were a number of important topics touched on throughout the development and discussion of this analysis that we did not have the time to fully explore. While in our simulations in chapter 3 we altered the stage gain by changing the carrier mobility to represent changing device dimensions while maintaining a fixed RC load time constant, we did not examine the effects of changing the device threshold voltage. In practical designs, an engineer may have the option of using low threshold devices, or may adjust the effective threshold voltage by making use of the back gate effect. Decreasing the threshold voltage increases the gate overdrive, and hence small signal gain, for an oscillator stage, however recall from section 3.3 that decreasing the threshold voltage also changes the points at which the oscillator transitions from region I to II and from region II to III. The effect on the differential case appears to be more subtle since we do not enter cutoff and triode regions the same way we did in the single-ended case. Indeed in the differential case the effects of changing v_T may be identical to changing the gain as was done with the carrier mobility. Lower threshold devices for the bias current sources should, however, allow for larger signal swings and thus better noise performance, all else being equal.

Beyond simple process parameters like v_T that may not be readily controllable, it would be greatly beneficial to assess the impact of non-linearities in the load resistance and capacitance. In high speed designs where there is little or no added node capacitance, the non-linearities in the gate and parasitic capacitances may significantly alter both the

shape of the output waveform, as well as the noise response. Furthermore, most tuning methods for differential oscillators involve either a varactor diode or a triode region MOSFET whose resistance can be adjusted via a control voltage. In either case, additional non-linear characteristics are introduced into each stage's load impedance. The analysis presented here could be applied to varying degrees of load non-linearity to determine how the oscillator jitter is affected. In particular the magnitude and concavity of the non-linearity could be looked at first, before moving on to more complicated load characteristics such as that of a Maneatis load[27]. Also potentially of interest would be to consider what effects these non-linearities have on the supply dependence of both single and differential oscillators, since sacrificing a small amount of intrinsic noise performance may be acceptable if it allows the oscillator to function better in noisy real world environments.

For lower speed designs that are not at the edge of the process limits, there has often been much debate over the relative advantages and disadvantages of increasing the number of stages, increasing the load capacitance, or digitally dividing the signal to reduce the speed. A more complete investigation of the effects of increasing the number of stages would go a long way towards clarifying the pros and cons of long ring oscillators. Adding stages doesn't simply alter the oscillator time scale as changing the load capacitance does, since each stage now relaxes longer between switching times. Unlike in the case of scaling the RC time constant, the longer period results in a larger signal swing and longer delay per stage. Not only will this affect the overall period jitter,

[27] For those curious, the Maneatis load looks like an increasing resistance for small voltages, similar to a triode region MOSFET, however as the voltage increases further, it then decreases as the incremental resistance is dominated by a diode connected transistor.

it may also shift the optimal gain setting in both single-ended and differential oscillator designs.

An important point to remember is that all of the preceding analysis has been conducted under the assumption that all noise sources present are white noise sources. Flicker noise contributions are more difficult to analyze because their autocorrelation functions are not simple delta functions. Equation 3.2.2 and those subsequently derived from it are no longer valid because the inner integral must be evaluated instead of using the sifting action [3] of the delta function for white noise. While it would require a significant amount of additional work, if one could develop a similar analysis for flicker noise sources we could begin to really understand the fundamental differences between flicker and white noise in oscillators and how they are incorporated into period jitter.

References

[1] T. H. Lee, A. Hajimiri, "Oscillator Phase Noise: A Tutorial," IEEE Journal of Solid-State Circuits, vol. 35, pp. 326-336, March 2000.

[2] R Mukhopadhyay, et. al., "Reconfigurable RFICs in Si-Based Technologies for a Compact Intelligent RF Front-End," IEEE Transactions on Microwave Theory and Techniques, vol. 53, pp. 81-93, January 2005.

[3] T. Weigandt, "Low-Phase-Noise, Low-Timing-Jitter Design Techniques for Delay Cell Based VCOs and Frequency Synthesizers," Ph.D. dissertation, University of California, Berkeley, CA, 1998.

[4] O. Prator, G. P. Fettweis, "On the Spectral Efficiency of Large CDMA Systems Using Higher Order Modulation Schemes," IEEE International Symposium on Personal, Indoor and Mobile Radio Communication Proceedings, pp. 1282-1286. 2003.

[5] J. Phillips, K. Kundert, "Noise in Mixers, Oscillators, Samplers, and Logic An Introduction to Cyclostationary Noise," IEEE Custom Integrated Circuits Conference, May 2000.

[6] D. P. Triantis, A. N. Birbas, D. Kondis, "Thermal Noise Modeling for Short-Channel MOSFET's," IEEE Transactions on Electron Devices, vol. 43, pp. 1950-1955, November 1996.

[7] M. Valenza, et. al., "Overview of the impact of downscaling technology on 1/f noise in p-MOSFETs to 90nm," IEE Proceedings on Circuits Devices and Systems, vol. 151, pp. 102-110, April 2004.

[8] M. Brownlee, P. K. Hanumdu, U. Moon, K. Mayaram, "The Effect of Power Supply Noise on Ring Oscillator Phase Noise," IEEE Poster Session III: Low Power and High Performance Approaches, pp. 225-228, 2004.

[9] F. Herzel, B. Razavi, "A Study of Oscillator Jitter Due to Supply and Substrate Noise," IEEE Transactions on Circuits and Systems, vol. 46, pp. 56-62, January 1999.

[10] D. Ham, A. Hajimiri, "Virtual Damping and Einstein Relation in Oscillators," IEEE Journal of Solid-State Circuits, vol. 38, pp. 407-418, March 2003.

[11] D. Ham, A. Hajimiri, "Virtual Damping in Oscillators," IEEE Custom Integrated Circuits Conference, pp. 213-216, 2002.

[12] A. Hajimiri, S. Limotyrakis, T. H. Lee, "Jitter and Phase Noise in Ring Oscillators," IEEE Journal of Solid-State Circuits, vol. 34, pp. 790-804, June 1999.

[13] A. Hajimiri, T. H. Lee, "A General Theory of Phase Noise in Electrical Oscillators," IEEE Journal of Solid-State Circuits, vol. 33, pp. 179-194, February 1998.

[14] H. Samavati, et. al., "Fractal Capacitors," IEEE Journal of Solid-State Circuits, vol. 33, pp. 2035-2041, December 1998.

[15] S. H. Strogatz, "Nonlinear Dynamics and Chaos, with Applications to Physics, Biology, Chemistry, and Engineering" Perseus Books Publishing, LLC, Cambridge, 1994.

[16] A. Jerng, C. G. Sodini, "The Impact of Device Type and Sizing on Phase Noise Mechanisms," IEEE Journal of Solid-State Circuits, vol. 40, pp. 360-369, February 2005.

[17] R. Navid, T. H. Lee, R. W. Dutton, "Minimum Achievable Phase Noise of RC Oscillators," IEEE Journal of Solid-State Circuits, vol. 40, pp. 630-637, March 2005.

[18] R. Aparicio, A. Hajimiri, "A Noise-Shifting Differential Colpitts VCO," IEEE Journal of Solid-State Circuits, vol. 37, pp. 1728-1736, December 2002.

[19] R. Navid, T. H. Lee, R. W. Dutton,, "An Analytical Formulation of Phase Noise of Signals With Gaussian-Distributed Jitter," IEEE Transactions on Circuits and Systems, vol. 52, pp. 149-153, March 2005.

[20] S. Tedja, J. Van der Spiegel, H. H. Williams, "Analytical and Experimental Studies of Thermal Noise in MOSFET's," IEEE Transactions on Electron Devices, vol. 41, pp. 2069-2075, November 1994.