HYBRID CONSTRUCTION OF A 10MHz DC-DC CONVERTER FOR DISTRIBUTED POWER SYSTEMS

by

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ABSTRACT

This thesis describes the development of advanced multilayer copper thick film hybrid assembly techniques, specifically optimized to complement several novel circuit topologies and specially developed components, to improve the performance of high frequency switching converters. The superior power supply performance characteristics that are achieved through hybridization permit conversion at higher operating frequencies and greater power densities, without sacrificing efficiency. The resultant converters, with their improved reliability and simplified manufacturing requirements, are highly suitable for mass production in point-of-load distributed power system applications.

Several prototypes of a 50 W, 40 V-5 V DC-DC point-of-load switching converter, operating with resonant square-wave switching at a frequency of 5 MHz, have been constructed to demonstrate these concepts. Power densities of $100W/in^3$ have been achieved, with efficiencies of 85% and an output ripple frequency of 10 MHz.

Thesis Supervisor: Dr. Martin F. Schlecht
Title: Associate Professor of Electrical Engineering

ACKNOWLEDGEMENTS

This work was done as part of the high frequency switching converter research program being conducted in the Laboratory for Electromagnetic and Electronic Systems (LEES), in conjunction with the Microsystems Technology Laboratory (MTL). The project received funding in part from the MIT Collegium on Power Electronics, with additional support from the power electronics groups at Digital Equipment Corporation and at the General Electric Research and Development Center.

Many thanks are due to the companies and their sales representatives who made donations of components, chemicals, and supplies for this project. Their efforts greatly simplified the task of obtaining the small quantities of various items necessary for research and prototype development programs. The following companies are among those who made such donations in support of our research efforts: 3M Industrial Chemical Division; AAVID Engineering, Incorporated; AMP Incorporated; Chip Supply, Incorporated; DuPont Company; Heraeus Incorporated, Cermalloy Division; Johanson Dielectrics; National Semiconductor, Incorporated; Semetex, Incorporated; UTZ Engineering, Incorporated.

A special thank you is extended to Mr. Jim Mitchell of DuPont, their resident expert on copper thick film inks. His experience, expertise, and encouragement were of great assistance during the initial phases of this project. Furthermore, his personal evaluation of samples taken from our thick film facility proved invaluable in the establishment of a viable copper thick film hybrid processing facility here at MIT.

This thesis documents one facet of my graduate education which was gained outside of the traditional classroom environment, without a text book or syllabus. That it is at all coherent or meaningful is wholly due to the benevolent guidance of my research advisor, Dr. Martin Schlecht. As the visionary overseer of this and many other related projects, he was always able to suggest a new direction or an alternative approach when the problems proved intractable and the road of progress seemed at an end. At the same time, his willingness to give me the freedom to learn and try were equally conducive to my growth and education. While many of the ideas and insights presented as a part of this research were originally his, the many intermediate mistakes, wrong turns, and dead ends that delayed the completion of this document for so long are surely my own. It was through his wisdom that the successes and failures were sorted out and arranged in their present form.

I am also greatly indebted to the recently graduated Dr. Leo Casey, who proved to be a good friend as well as a wealth of technical competence. As an experienced member of the LEES laboratory, he provided me with the training and assistance crucial to management of the many mundane ordeals of everyday life. In addition, the particular circuit topology that was selected as a showpiece for this thesis concept was jointly developed by himself and Marty. I am thankful that I was able to contribute to a small part of his work by implementing a functional version of his brain-child.

The educators of this nation will undoubtedly attest to the fact that the desire to pursue an education at any level is not an inborn trait of most human beings. For my own intellectual curiousity and love of learning I must thank my wonderful parents. Their careful indoctrination successfully cultivated in me a respect and admiration for knowledge and the ability to think creatively. Through their encouragement and support, and by their example, I came to understand the priceless value of education. That I have undertaken to equal their own achievements can only attest to the success of their teachings.

Finally, I owe a great debt to my good friends Bob, George, Peter, and Laura. As fraternity brothers and housemates, the former three have provided me with a second family for most of my seven years at MIT. As my girlfriend for most of the last three years, Laura has provided invaluable emotional support, patience, and understanding. Together, they have all shared a part of my hopes, aspirations, successes, and failures at MIT; one could not ask for a better group of friends. I hope that in some way I have been able to contribute something equally precious to their lives.

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Chapter 1

INTRODUCTION

The miniaturization and integration of semiconductor components has led to rapid growth in the speed and computational ability of modern computing systems. This growth has been accompanied by increased demands for electric power, resulting in greater currents at the $5V$ logic level. At present, the technologies for conditioning this power have not kept pace with advances in computational logic circuitry, especially in the areas of power density, cost, and efficiency. As a result, the power supply in a modern computer comprises a significant fraction of the system's total size, expense, and thermal output.

Methods for advancing the technologies of power conversion are one area of research in the Laboratory for Electromagnetic and Electronic Systems (LEES). Of particular interest are the problems associated with the conversion and distribution of electric power in large computer systems. The so-called "10 MHz Project" is a research program which addresses these problems by focussing on three distinct yet interrelated power supply design issues. At the system level, techniques for fault-tolerance, load sharing, and distributed power conversion are being developed. At the module level, novel circuit topologies and integrated construction processes are being investigated. Finally, basic research at the component level is being conducted to enable the realization of converter circuits and distribution systems which cannot be fabricated with standard components and assembly techniques. This chapter describes the motivation and philosophy behind this research program, thereby providing the contextual background for this thesis.

1.1 Research on Power Conditioning Systems

The never-ending quest for faster and more powerful computers has led to the adoption of logic families with reduced supply voltage requirements to facilitate quicker level transitions

and to permit reduced device dimensions. In particular, sub-micron CMOS structures will soon be operating in the $3V$ range, while the newest current-mode logic gates (ECL) already employ supplies in the $2V$ range. Simultaneously, rapid advances in the areas of high resolution photolithography, integrated circuit packaging, and thermal management techniques are forcing power densities ever higher. Together, this decrease in supply voltage and increase in power has produced a situation in which even modest computing systems can require hundreds of amperes of load current per board.

Distribution of this low voltage, high current power requires massive copper bus bars to limit voltage drops throughout the system, thereby adding to the cost, size and weight of the distribution system. Numerous edge connections per board for power and ground lines and wide trace widths for power busses increase the size of individual boards while restricting layout options. Furthermore, resistive conduction losses grow proportionally with I^2, and localized capacitive energy storage for handling load transients becomes less efficient at low voltages due to the electrostatic energy storage density's dependence on V^2.

These and other problems associated with the distribution of high currents are increased dramatically by the physical distances separating the power conversion unit from the system being driven. They can be minimized by instead distributing the power conversion system throughout the computer, directly on the boards at the load sites [1]. In such a distributed power conversion system, the power is bussed to the boards at a higher voltage (and correspondingly lower current) and converted to the final logic voltage and higher current using point-of-load (POL) DC-DC converters. Besides addressing the problems outlined above, this approach also provides the flexibility necessary for system expansion and power supply back-up redundancy.

The concept of point-of-load conversion has existed for some time, but technological roadblocks have so far limited its realization. To permit the inclusion of power converters along side logic and memory circuitries, the converters must be both compact and efficient. Quantitatively, power densities exceeding 50 W/in^3 at efficiencies near 90% seem necessary. In contrast, present low-voltage "high density" DC supplies operate in the 5–10 W/in^3 and 80–85% efficiency range [2]. Significant advancements at the converter and device levels will therefore be necessary before distributed power conversion becomes a viable concept.

1.2 Research on Power Converters

The past decade has already brought significant improvements in the performance of power supplies for computer systems. Switching converters have almost universally replaced linear regulators as the preferable power conditioning method. Their improved efficiency, higher power density, and lower cost have made them the better option for most applications. At the same time, however, their maximum performance has been limited by switching loss mechanisms which prevent their operation at frequencies much above 1 MHz. This has proven to be an upper bound for the switching frequency of practical square wave converters, thereby limiting the maximum power densities that can be achieved.

A new class of converter topologies, capable of operating at frequencies in the 5–10 MHz range, has been proposed for DC-DC converter operation [3,4,5]. These topologies use resonant elements to significantly lower switching losses, permitting higher operating frequencies and corresponding component size reductions. A variation on one such topology, with several advantageous circuit properties including fixed frequency operation, square wave output current waveforms (rather than sinusoids), and simultaneous switch resonance, is presently under study at MIT by members of LEES [6]. This converter promises to meet the criteria for a practical distributed power conversion unit.

The first prototype of this variation, built by Leo Casey during 1986, employed a dual resonant forward converter topology, and included an open loop pre-regulation scheme. This prototype used off-the-shelf components and standard printed circuit board (PCB) assembly techniques, and demonstrated the merits of the circuit topology. However, its performance was restricted to pulsed operation and limited voltage conversion ratios. The use of standard construction and packaging techniques imposed these restrictions by contributing excessively large parasitic elements to the circuit and by precluding adequate thermal transfer. The predominant parasitic elements were inductors due to package lead interconnections, component interconnections, and transformer leakage. The major thermal concern was semiconductor device overheating due to restricted heatsink accessibility.

This thesis describes the development of hybrid circuit assembly techniques to overcome these construction-related performance restrictions. Hybrid circuits exhibit several characteristics which make them attractive for high frequency switching converter applications. Compared to standard epoxy-glass PCB's, multilayer ceramic hybrids offer a nearly

ideal component interconnection medium for low impedance circuits, with lower parasitic inductance, greater thermal conductivity, and increased mechanical stability. The ability to physically bond and electrically connect bare, unpackaged semiconductors in dice form directly onto the substrate eliminates the bulk, thermal resistance, and parasitics of semiconductor packages. These advantages of hybridization permit higher operating frequencies and greater power densities while providing improvements in reliability and simplifications in converter manufacturing.

The recognition of these merits led to the installation of a hybrid processing facility at MIT. The facility was set up for gold thick film hybrid production by Len Pitzele, a Master's student in the Mechanical Engineering Department. His work culminated in the creation of the first hybrid mock-up model of the point-of-load converter in the Fall of 1986 [7]. The following thesis is a continuation of that work, and includes the development of a new hybridization process, using a more economical copper-based multilayer thick film process, which is then used to build a succession of functional prototype converters [8].

1.3 Development of Improved Converter Components

Development of the fabrication techniques necessary to produce components, custom tailored for the dual resonant forward converter circuit topology, constitutes the third level of research being conducted within the 10 MHz Project. The full benefits of the proposed hybrid packaging techniques cannot be realized with presently available commercial components, which are manufactured by balancing many design parameters to yield a generic product that will be useful to the largest possible market. These trade-offs produce components that possess many good qualities, but few that are optimal for any particular circuit. In many cases, better circuit performance can be achieved by optimizing those component parameters which are critical for the particular circuit application, and in return sacrificing other characteristics which are less important.

At MIT, developmental programs at this level include virtually all circuit element types commonly used in power circuits. Semiconductor component fabrication programs include work on synchronous rectifiers with low parasitic capacitance [9] and high voltage FETs with integrated gate shorting switches [10]. Research on magnetics is concentrated in the area of transformer miniaturization, with emphasis on the manufacturing of low leakage windings [11] and on the characterization of magnetic core materials [12,14] and parasitic

winding capacitances [16]. Electrical and mechanical characterization studies are also being conducted on surface mount capacitors [17]. Finally, custom integrated circuits for high frequency closed-loop regulation and gate drive applications are being developed in conjunction with the government-sponsored MOSIS integrated circuit fabrication program [18].

With the exception of the high frequency magnetics, development of these components is not an integral part of this thesis. However, sucessfully optimized components from the previously described programs will be incorporated into future versions of the converter. Continuous interaction between the various research groups has enabled the evolution of optimal component designs and complementary circuit construction techniques. Together, achievements at the system, converter, and component levels will ultimately yield an advanced power distribution network, one capable of meeting the increasingly demanding applications of modern computing systems by utilizing point-of-load converters in a distributed power regulation configuration.

1.4 Thesis Overview

This thesis document is organized into five major chapters, with additional chapters serving as introductory and conclusionary summaries. The first major chapter describes one specific high frequency power conversion topology suitable for point-of-load conversion applications. The basic operating principles of the converter are first reviewed, and the effects of component parasitics are considered. The origin and effects of parasitics due to layout, construction, and component interconnection methods are then discussed. It is shown that there are fundamental limits on converter performance which cannot be overcome with standard components and conventional packaging techniques, thus motivating the development of hybrid construction as one alternative for improving converter performance.

The next chapter describes the development of an assembly process specifically optimized for high frequency power converter manufacturing applications. This assembly process employs a multilayer thick film hybrid substrate, and utilizes a more economical copper-based ink family rather than previously developed precious metal inks based upon gold, silver, and platinum conductors. Manufacturing issues, including substrate processing techniques, ink firing profiles, printing parameter variation effects, and surface oxidation control techniques are addressed, in relation to this new conductor material. The mechanical and electrical

properties of the multilayer copper hybrid process are characterized. In particular, quantitative estimates of parasitic element parameters are developed. The critical assembly issues, most notably the solder wetting and wire bond adhesion characteristics of copper conductor surfaces, are discussed. A complete assembly procedure is then presented. Finally, mechanical reliablity issues such as die bonding voids, dielectric shorts, layer adhesion failures, and thermal expansion coefficient mismatches are addressed.

Chapter 4 describes the construction of a novel high frequency power transformer with extremely low leakage inductance. The origin of leakage inductance parasitics is first described, using magnetic energy storage arguments, in the context of standard transformer construction techniques and circuit models. Methods for reducing the magnitude of these fields, and their associated leakage inductance, are then discussed. In particular, the effect of winding geometries and various interleaving configurations are described. Finally, techniques for creating low-inductance secondary-side winding terminations are demonstrated.

Chapter 5 describes the construction of a functional converter prototype, based upon the dual resonant forward converter topology presented in Chapter 2. The prototype is built using commercially available components and is assembled on a multilayer copper thick film hybrid, using the techniques described in Chapter 3 and incorporating the novel transformer design of Chapter 4. The generation of circuit layouts is discussed, emphasizing the minimization of parasitics loop inductances. A thermal analysis of the prototype is also performed, to quantify the trade-offs involved in the various construction options. The final processing parameters, specifically optimized for fabrication of the DRFC prototype, are reported in sufficient detail to facilitate reconstruction of the experimental data.

Chapter 6 describes the results of tests and measurements made on several versions of the converter prototype. Details of the experimental set-up are presented, including descriptions of the interface connections, instrumentation, and test procedures. Waveforms detailing the operation of the converter and pre-regulator sections under various operating conditions are documented. The results are interpreted and the performance enhancements afforded by hybrid construction are emphasized. Standard performance criteria, such as efficiency, power density, and load regulation are discussed.

Chapter 2

10 MHz Converter Topology

In order to achieve the power densities necessary for distributed power conversion in point-of-load (POL) applications, it is necessary to operate at switching frequencies well into the megaHertz range. However, traditional square wave converter topologies exhibit significant reductions in efficiency at frequencies above 1 MHz due to switching losses. Alternate switching topologies, particularly resonant (including "quasi-resonant") converters, offer significantly reduced switching losses through the utilization of resonant commutation elements.

One such resonant topology, the dual resonant forward converter (DRFC), was selected as the test vehicle for verifying the performance characteristics of hybrid construction. This topology, first described by Casey and Schlecht, possesses several characteristics which make it ideally suited for hybrid prototype development [6]. In keeping with the main goals of the 10 MHz project, the DRFC has great potential as a POL converter due to its high efficiency and high power density. Additionally, its resonant operation permits testing in the 5–10 MHz range, the area of interest for power conversion in the next five years. Finally, its relative simplicity, in terms of component count, reduces the overhead associated with prototype construction.

A description of the DRFC topology, and some additional advantages associated with its use as a POL converter, are presented in this chapter. This presentation will serve as an introduction to the issues associated with high frequency power conversion and converter assembly, and will provide a common reference point from which subsequent decisions for optimization tradeoffs within the hybrid design and assembly processes can be better understood.

2.1 The Resonant Forward Converter Topology

The resonant forward converter evolved from the simple down converter, motivated by the need for reduced switch stresses and improved efficiency at the higher operating frequencies necessary for power densities in the 50–100 W/in^3 range. The following section presents this evolution and calculates the associated advantages in the context of POL power conversion applications. It then describes the trade-offs that can be made to obtain fixed-frequency, push-pull operation.

2.1.1 Down Converter

The familiar down converter consists of a voltage source V_{in}, a controllable switch Q, an energy storage inductor L, a free-wheeling diode D, and an output filter capacitor C. This is shown in Fig. 2.1 with a resistive load R. The equation describing the voltage conversion ratio is

$$\frac{V_{out}}{V_{in}} = D \tag{2.1}$$

where D is the duty cycle of switch Q, expressed as the ratio of the on-time to the switching period.

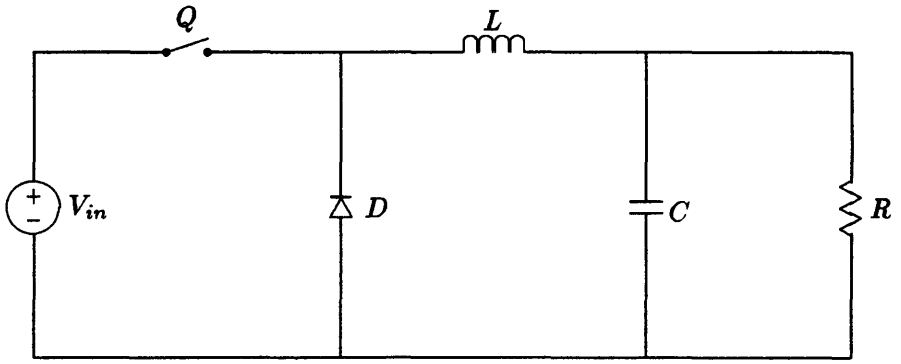


Figure 2.1: Down Converter

The VI rating of switch Q, defined as the product of the maximum off-state voltage across the switch times the maximum on-state current through the switch, is

$$VI_Q = V_{in}I_{out} = \frac{V_{out}}{D}I_{out} \tag{2.2}$$

It can be normalized to the output power to permit a design comparison which is independent of load parameters

$$\overline{VI_Q} = 1/D \tag{2.3}$$

This normalized $\overline{VI}$ rating is commonly used to compare the cost of converter designs, because the switches are typically the most expensive components in the converter. Having normalized this figure-of-merit to the output power, it becomes readily apparent that the switch stress increases as the inverse of the voltage conversion ratio. In a typical distributed power conversion system, where the POL regulator may be required to convert a nominal $40V$ input to a $5V$ output, the normalized $\overline{VI}$ rating of switch Q would be eight times the load power. Furthermore, this normalized rating becomes even higher when adjusted for conduction losses in the output rectifier D and changes in input voltage V_{in}. Because this increased rating translates directly into a larger die area for the semiconductors, the cost-per-watt for a down converter grows rapidly with decreasing conversion ratios.

2.1.2 Forward Converter

The down converter can be modified by adding a transformer, which effectively multiplies the voltage conversion ratio by the transformer's turns ratio. Such a modified down converter, called a forward converter, is shown in Fig. 2.2. This modification provides two additional benefits: 1) the drive circuitry for switch Q can be ground-referenced, and 2) the input and output of the converter can be electrically isolated. The voltage conversion ratio becomes

$$\frac{V_{out}}{V_{in}} = \frac{N_s}{N_p} D \tag{2.4}$$

where N_p/N_s is the primary-to-secondary turns ratio. By adjusting the transformer turns ratio, it is possible to operate in the 50% duty cycle range, even for small conversion ratios.

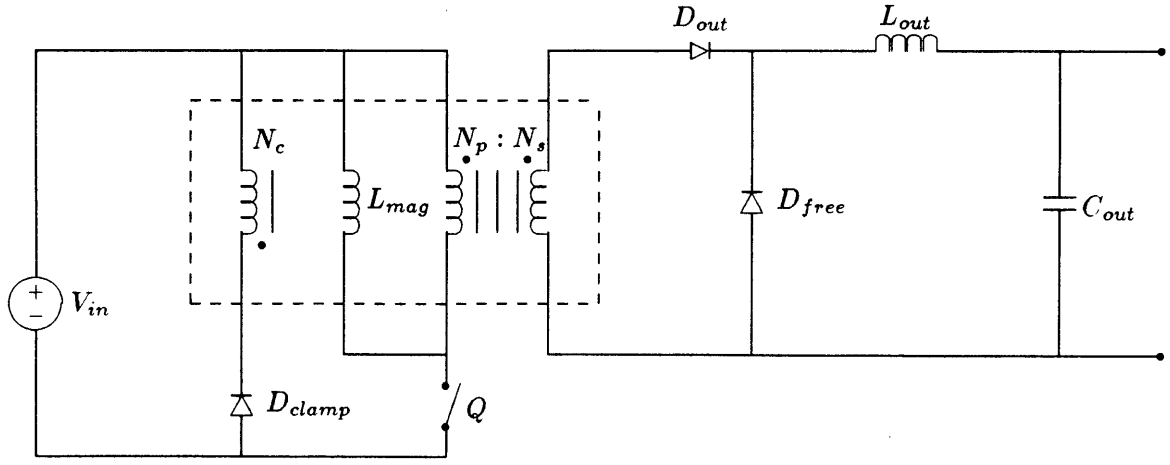


Figure 2.2: Forward Converter

The inclusion of a transformer in the down converter adds an additional parasitic element, due to the finite permeability of real transformer cores. This element, the magnetizing inductance L_{mag}, appears in parallel with the transformer. When switch Q is on, input voltage source V_{in} applies positive volt-seconds across this inductance. During steady-state converter operation, this must be balanced by an equal number of negative voltage-seconds, applied during the off-time of switch Q. These negative volt-seconds are provided by an additional clamp winding on the transformer, which simultaneously recovers the magnetizing energy from inductor L_{mag} in a "lossless" manner. When the number of turns on the clamp winding equals the number of primary turns, $N_c = N_p$, the reset voltage seen by the primary-referred magnetizing inductance L_{mag} equals the negative of the clamp voltage, which in turn equals the input voltage V_{in}. Thus, equal but opposite voltages are applied across magnetizing inductance L_{mag} during the two switch states, and, in order to assure that the core is completely reset each cycle, the maximum duty cycle of the converter is limited to 50%.

In general, the switch stress for a forward converter with an N_c-turn clamp winding, when normalized to the output power, is approximately

$$\overline{VI_Q} \approx (1 + \frac{N_p}{N_c})\frac{1}{D} \tag{2.5}$$

where the magnetizing current is assumed to be small compared to the load current. For a clamp-to-primary winding ratio of $N_c : N_p = 1 : 1$, and a transformer ratio of $N_p : N_s = 4 : 1$, a $40V$ to $5V$ forward converter would have half the normalized switch stress compared to a similar down converter. Thus, changing from a down converter topology to a forward converter can significantly reduce the switch stresses. It can be shown that a similar argument holds for the output rectifiers, which in the forward converter case see a reflection of the primary voltage that is reduced by the transformer turns ratio. For small conversion ratios, this stress savings can offset the additional cost of the transformer itself. Furthermore, the inherent isolation and switch drive flexibility advantages can make the forward converter an attractive option even when the voltage conversion ratio approaches unity.

2.1.3 Square Wave Switching Losses

Despite these advantages, the forward converter remains unsuitable for operation above 3 MHz. Like all square wave converters, energy is dissipated during every switch transi-

tion. This dissipation is due to non-idealities in the components and limitations of circuit construction which contribute unwanted parasitic elements to the circuit. These parasitics must be included when considering the operation of high frequency circuits. The most influential circuit parasitics are the junction capacitances of the switches and rectifiers and the loop inductances created by the physical spaces between the components. Figure 2.3 shows the original square wave down converter of Fig. 2.1, with the parasitic elements being represented by C_{J_Q}, C_{J_D}, and L_{loop}.

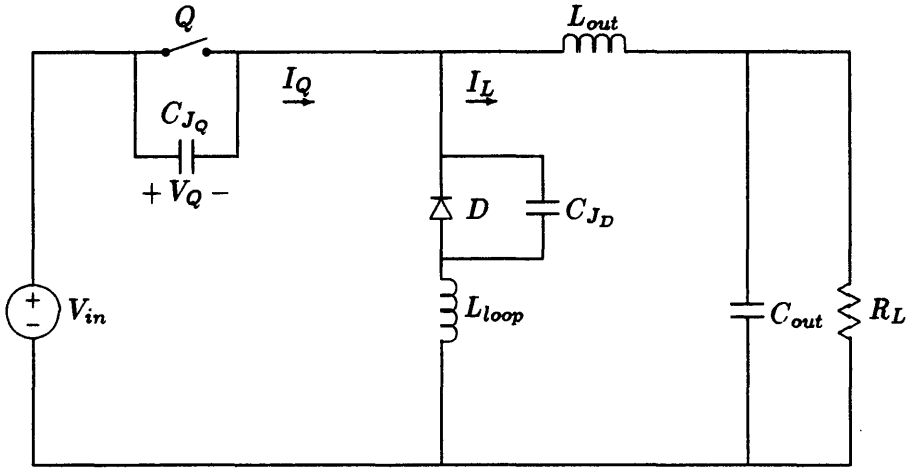


Figure 2.3: Down Converter with Parasitics

The general effect of these parasitics on the circuit operation is to slow down the switch transitions. For example, during the switch turn-on transition, the load current I_L commutates from diode D to switch Q. This situation is shown in Fig. 2.4, with switch current I_Q and switch voltage V_Q in parts a and b, respectively. Due to the non-zero turn-on time of the switch, this commutation process takes a finite period of time. During this period, labelled T_c in the figure, the diode D must remain conducting. Once the load current I_L has fully commutated to switch Q, the diode turns off and the diode parasitic junction capacitance C_{J_D} begins to charge.

During this commutation interval, the switch has both a non-zero voltage and a non-zero current, and it may for an instant support the full voltage V_{in} while carrying the full current I_L. The instantaneous power dissipated by the switch during these periods can be very high relative to the average input power. This instantaneous power is given by the VI product, and can be normalized to the input power as shown in Fig. 2.4c, where a duty cycle D of

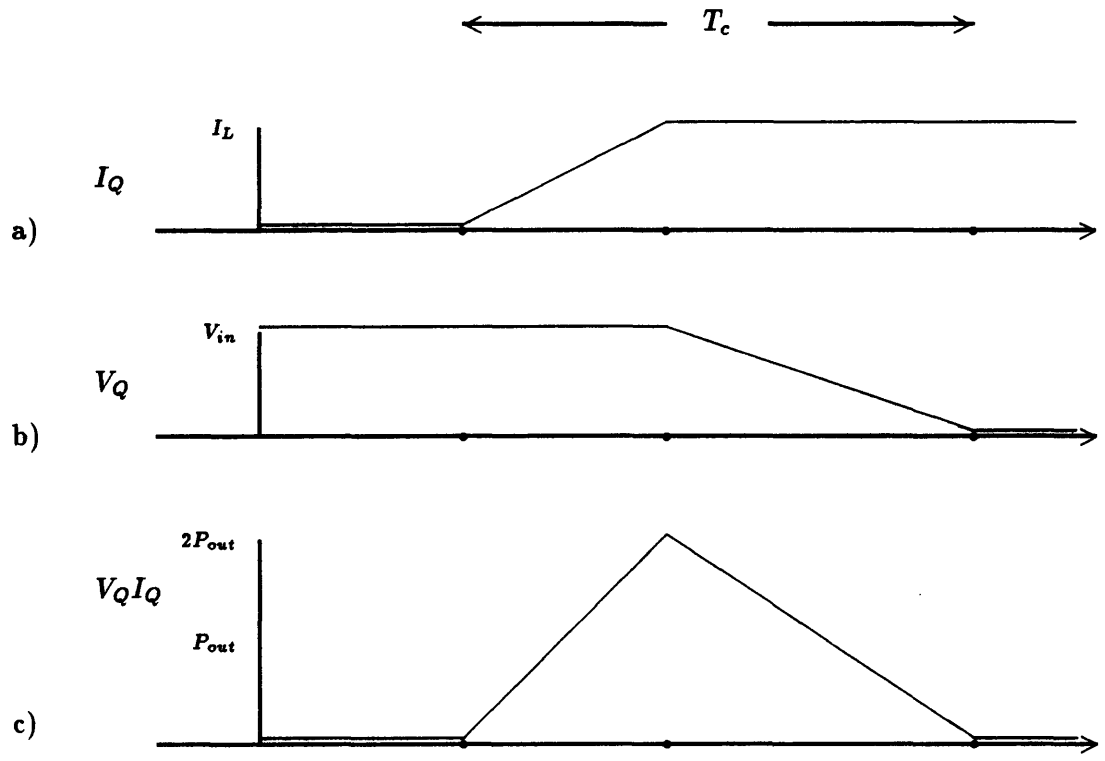


Figure 2.4: Switching Transition Waveforms

50% is assumed. The energy per switch commutation can be approximated geometrically (for straight-line transitions) as:

$$E_c = 1/2\, V_{off}\, I_{on}\, T_c \tag{2.6}$$

The power loss represented by this dissipation can be expressed as a function of the switching frequency, and normalized to the input power to yield:

$$\overline{P_c} = T_c\, f_{sw} \tag{2.7}$$

Thus, the commutation loss is directly proportional to the switching frequency. For switching frequencies in the 5–10 MHz range, and switch transitions of 5–10 nsec, these losses alone can represent a 10% decrease in conversion efficiency, dominating the switch *conduction* losses.

A second switching loss occurs in square wave converters, also during the turn-on transition, because of the non-zero voltage across the switch junction just prior to turn-on. The energy stored in the parasitic junction capacitance C_{J_Q} of switch Q is dissipated in the switch each time it turns on. When the switch is turned back off, the energy is replaced

as the capacitor is recharged. The energy lost per cycle due to this capacitive discharge is simply the energy stored in the capacitor C_{J_Q} when the switch is turned on

$$E_{cap} = 1/2\, C_{J_Q}\, (V_Q)^2 \tag{2.8}$$

where V_Q is the voltage across the switch just prior to turn-on. This energy loss can be quite significant, even in relatively low frequency (100–500 kHz) switching power supplies. For this type of power supply, the switch elements are most often MOSFETs, due to their fast transition characteristics between saturation and cutoff and the simplicity of their drive circuitry. Their output capacitance can be on the order of several hundred picofarads [20]. For off-line converters operating from input busses of $200–400V$, the energy lost in the parasitic switch capacitor each cycle becomes a significant fraction of the total input power. This limits the general use of off-line square wave down converters to the sub-megaHertz range. Even when the bus voltage is significantly lower, for example in $36V$ battery-back-up (BBU) or $40V$ distributed power supply conversion systems, the capacitive losses associated with the operation of down converters in the megaHertz range are significant. Similar arguments hold for the square wave forward converter, and most other square wave converters.

These losses create an upper bound on the practical operating frequency for square wave converters by forcing the designer to trade efficiency for power density. Eventually, a point is reached where the heatsink dominates the overall size of the converter, and further increases in frequency actually *decrease* the converter's power density. In applications such as POL converters, where the converters must operate alongside their loads, conversion efficiency and power density are critical parameters. Because it is generally impractical to implement dedicated cooling provisions for distributed converters, system thermal constraints require that the converters and their loads have comparable physical profiles and power dissipations. At present, square wave switching converters are unable to simultaneously meet the power density and efficiency requirements for POL applications. The switching losses are unacceptably high at the frequencies necessary for high power density POL converters.

2.1.4 Resonant Forward Converter

Resonant converters have been introduced to address these switching loss problems. Unlike conventional snubber circuits, which place a single energy storage element around the switch to limit the dv/dt or di/dt seen by the switch, resonant converters use an L-C tank circuit. This tank circuit becomes a self-resetting snubber in which the resonant elements absorb

energy during the switch transition, transfer it between themselves, and then return it to the circuit during the next half-cycle. The resonant ring is timed so that one of the switch co-variables is zero during each transition, insuring lossless switching. In those cases where it is the switch voltage which is zero, resonant converters provide the additional benefit of eliminating the capacitive discharge losses normally associated with the switch junction capacitance during turn-on.

The previously described square wave forward converter can be changed into a resonant forward converter (RFC) by utilizing the magnetizing inductance of the transformer as the resonant inductor, and adding a resonant capacitor in parallel with the switch. Such changes are shown in Fig. 2.5. The clamp winding was also eliminated from the transformer, because the energy in the magnetizing inductance L_{mag} is transferred to the resonant capacitor C_{res} and the switch voltage requires no clamping. This is an especially beneficial solution because it actually exploits the two main parasitics of the circuit, the transformer magnetizing inductance L_{mag} and the parasitic switch junction capacitance C_{J_Q}, rather than simply minimizing their detrimental effects. In fact, at sufficiently high switching frequencies, supplemental resonant capacitor C_{res} becomes unnecessary, and the resonant capacitance is provided exclusively by parasitics.

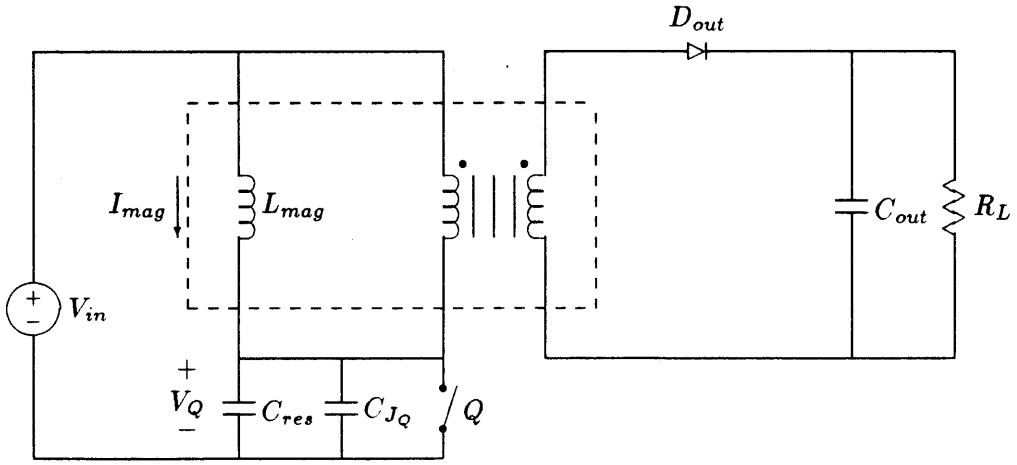


Figure 2.5: Resonant Forward Converter

As shown in Fig. 2.5, the secondary section has been modified as well as the primary. In particular, output filter inductor L and free-wheeling diode D_{free} have been removed, creating a voltage source output. The reason for this change will be explained later.

The operation of the resonant forward converter is quite different from its non-resonant

predecessor. A qualitative description can be obtained by considering the steady state ring waveforms. Typical waveforms for the voltage V_Q across switch Q and for the magnetizing current I_{mag} through the transformer parasitic inductance L_{mag} are shown in Figs. 2.6a and 2.6b respectively.

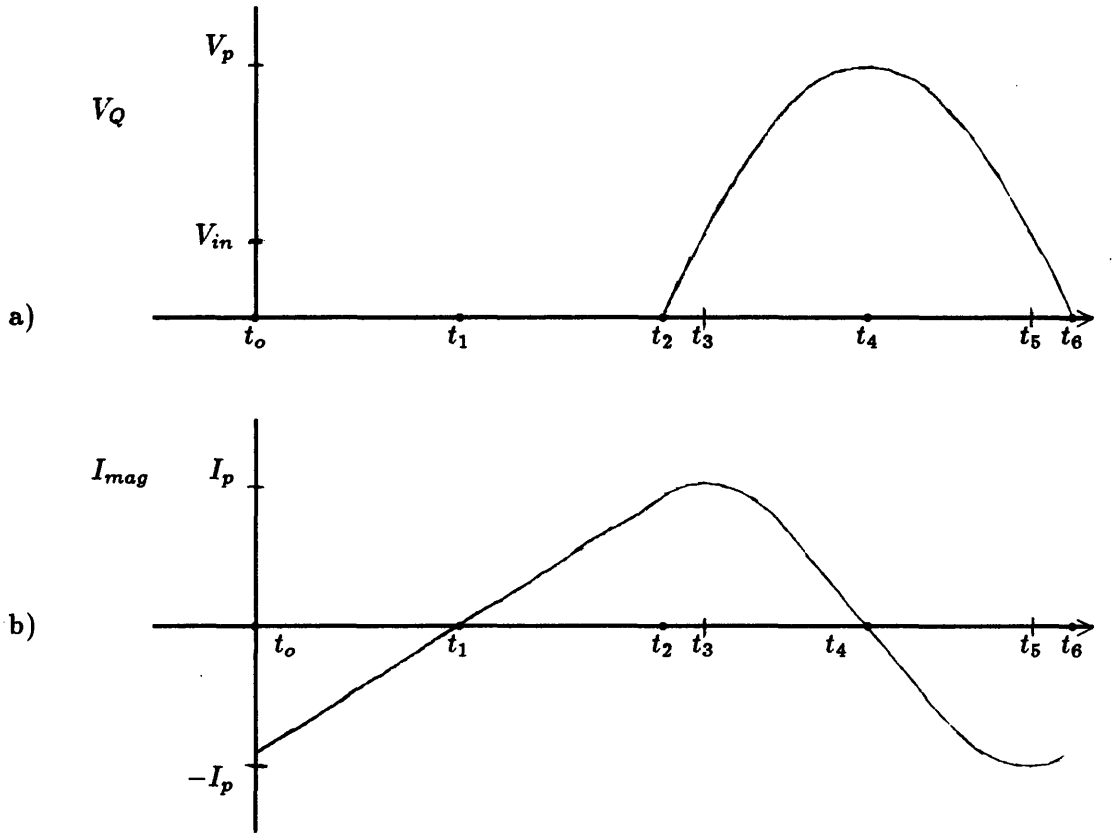


Figure 2.6: Resonant Ring Waveforms

During steady-state operation, switch Q is turned on at point t_0, while magnetizing inductance L_{mag} has a negative current and the voltage across the switch is zero. During the switch on-time, t_0 through t_2, a positive voltage is applied across the transformer, turning on output rectifier D_{out} and delivering power to the load. Simultaneously, positive volt-seconds are applied to magnetizing inductance L_{mag}, eventually reversing the magnetizing current at t_1 and storing energy for the resonant commutation operation. When the switch is turned off at t_2, the load current I_L stops flowing, magnetizing current I_{mag} commutates into resonant capacitor C_{res}, and the resonant ring begins. The magnetizing inductor and the resonant capacitor form a resonant tank circuit in series with the input source, and ring

at a frequency of

$$f_{ring} = \frac{1}{2\pi} \frac{1}{\sqrt{L_{mag} C_{res}}} \tag{2.9}$$

with the ring voltage centered around V_{in}. This ring continues through t_5, with the magnetizing current once again reversing polarity at t_4. At t_6, the resonant ring is complete, the voltage across the resonant capacitor has returned to zero, and switch Q can be turned on once more. It should be noted that the magnetizing current is quasi-triangular in shape, and has no DC component.

This description confirms that the ring waveforms are determined by the switching frequency and the duty cycle, but are independent of load. The resonant ring behavior is fixed by the initial conditions of the magnetizing current, which in turn are determined by the combination of switching frequency and duty cycle (effectively the on-time of the switch). The resonant ring period ends when the current through the parasitic MOSFET junction capacitance goes negative. At this point, the internal body diode of the MOSFET clamps the voltage, and the MOSFET can be turned on with a zero-voltage transition. The conversion frequency is thus limited by the resonant ring period, as the switch cannnot be turned on losslessly until the clamp period begins. For a given duty cycle, there is a maximum frequency above which operation with zero-voltage switch transitions is lost. Equivalently, there is a maximum duty cycle for a given operating frequency beyond which switching losses are introduced.

In many cases, it is beneficial to minimize the switching period by operating with a clamping period of length zero. In this mode, the switching frequency and duty cycle are no longer independent. Specifically, to obtain fixed frequency operation, a fixed duty cycle is required. Fixed frequency operation is desirable because it greatly reduces the noise spectrum of the converter, an important consideration in POL conversion applications where a number of converters would be operating in parallel. Because of the voltage source output, the duty cycle does not control the output voltage, so that fixing the duty cycle sacrifices nothing. In fact, operation with a 50% duty cycle is especially convenient, and permits a further modification, namely dual parallel conversion.

2.1.5 Dual Resonant Forward Converter

The many advantages of the resonant forward converter topology stem from its use in a fixed frequency, fixed duty cycle operating mode. These benefits can be further enhanced by

paralleling two such converters, and operating them 180° out of phase. Such a circuit configuration is shown in Fig. 2.7. The fundamental component of the output ripple frequency now appears at twice the switching frequency, and the magnitude of the output ripple is substantially reduced. Furthermore, the argument can be made that, to the extent that the components are ideal, input capacitor C_{in} and output capacitor C_{out} are functionally in parallel. Thus, a practical advantage of the circuit is the ability to provide output hold-up with capacitance on the primary side, where the voltage is higher and energy storage is therefore more efficient.

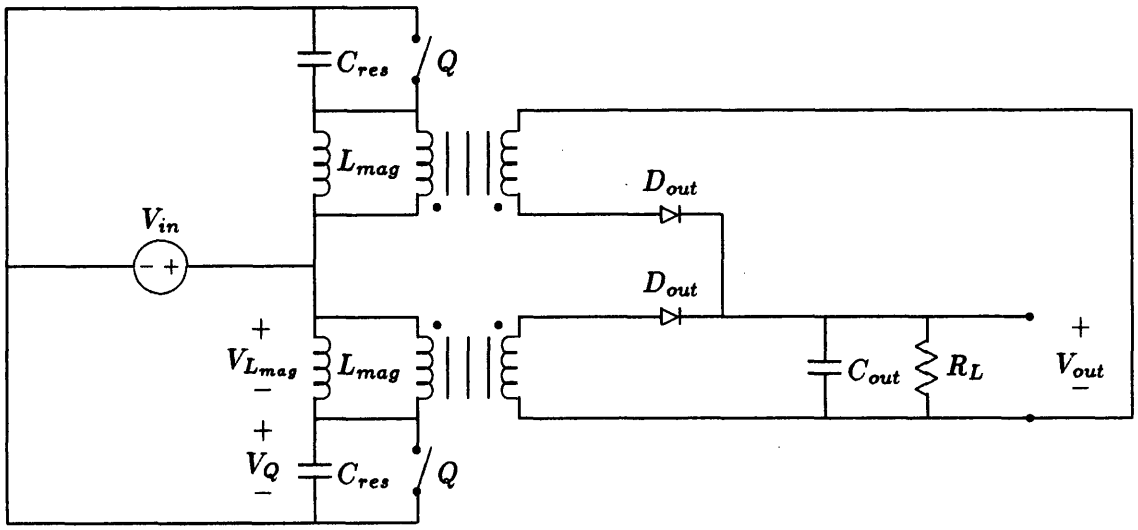


Figure 2.7: Dual Resonant Forward Converter

A quantitative analysis of the steady-state operation of the dual resonant forward converter (DRFC) topology can be performed by considering a single subcircuit operating with a fixed 50% duty cycle at a fixed frequency. During steady state operation, the total volt-seconds applied to the magnetizing inductance must be zero for each cycle. As shown in Fig. 2.8, the voltage waveform $V_{L_{mag}}$ is simply the negative of the switch voltage V_Q, offset by the input voltage.

Because the waveform shape is either DC or a sinusoid, the waveform can be formed piecewise, with solutions for each switch state

$$V_{L_{mag}} = V_{in}, \text{ for } 0 < t < \frac{1}{2f_{sw}} \tag{2.10}$$

$$V_{L_{mag}} = -V_p \cos[2\pi f_{res}(t - \frac{3}{4f_{sw}})], \text{ for } 0 < t < \frac{1}{2f_{sw}} \tag{2.11}$$

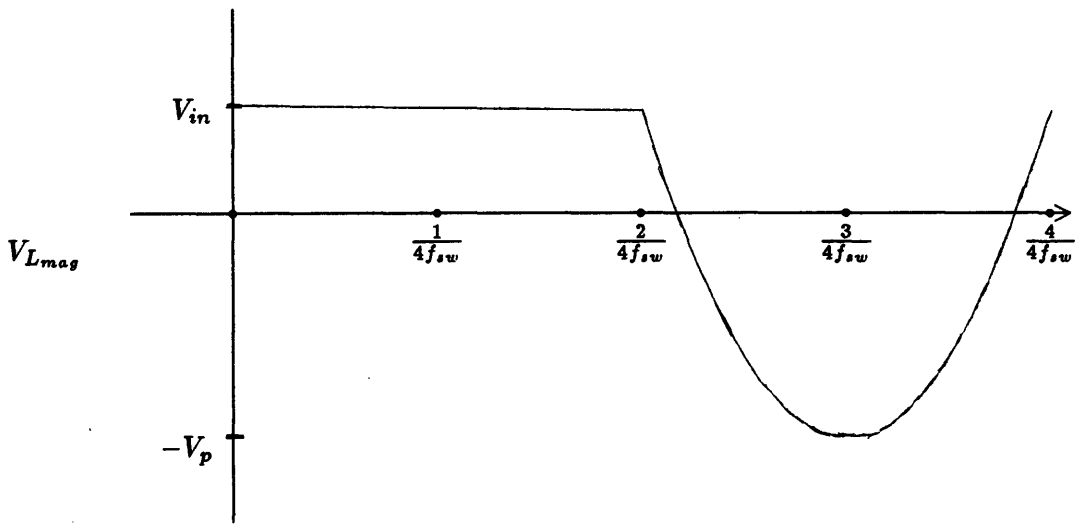


Figure 2.8: Voltage Across Magnetizing Inductance

The requirement that the two solutions intersect at their limits of validity yields a condition on the peak voltage

$$\frac{V_p}{V_{in}} = \frac{-1}{\cos(\frac{\pi}{2}\frac{f_{res}}{f_{sw}})} \tag{2.12}$$

Finally, the correct switching frequency can be determined by summing the volt-seconds applied to the magnetizing inductance during each part of the cycle. This integration, included in Appendix A, yields the result

$$\frac{f_{res}}{f_{sw}} = -\frac{2}{\pi}\tan(\frac{\pi}{2}\frac{f_{res}}{f_{sw}}) = 1.29 \tag{2.13}$$

The ratio of the resonant frequency of the tank circuit to the switching frequency, for a 50% duty cycle and zero-voltage switch transitions, is thus fixed independently of the input and output voltages and currents. When operated at this frequency, the ratio V_p:V_{in} is 2.26:1. This makes the peak voltage stress seen by switch Q equal to 3.26 V_{in}, or slightly more than three times the input voltage. This increase from twice the input voltage for the clamped forward converter has been made as a trade-off to reduce switching losses.

Dual operation of this converter is identical to single-ended operation, with complementary ring and power cycles operating 180° out of phase. This permits the continuous processing of power through the circuit, greatly reducing the input ripple currents and output ripple voltages. The DRFC topology is thus an elegant and straightforward method for processing DC power at high frequencies without incurring penalties from switching losses.

Unfortunately, this performance has been obtained at the expense of relinquishing control over the output voltage. This price can be minimal in cases where the input bus voltage is well controlled and the output voltage need not be variable. The POL converter is one such application, since the input bus voltage will be regulated to a nominal value with a small deviation range. The next section describes a simple pre-regulation scheme, applicable in such cases, which can compensate for input and load variations and provide a regulated output.

2.2 Pre-Regulation

A pre-regulation approach can be applied to the DRFC topology to restore the regulation capabilities which were traded off in favor of fixed frequency, fixed duty cycle, continuous-power-delivery operation. This approach is especially appropriate for the DRFC because, in this topology, the output bus is incrementally in parallel with the input bus, making any changes in the input voltage appear immediately at the output, scaled by the transformer turns ratio. In contrast, most other converter topologies have intervening energy storage elements which separate the input bus from the output bus, delaying the propagation of control changes through the converter and reducing the response bandwidth.

The main criteria for such a pre-regulator is that, like the DRFC itself, it must have a high power density and operate efficiently. For distributed power systems, the input power to the POL converter is typically provided by a remote off-line converter which supplies a loosely regulated ($\pm$ 10%) bus voltage in the $40V$ range. A novel floating up-converter topology, first described by Miwa and Schlecht for low cost power factor correction applications [22], exploits the limited range of the input voltage to reduce component stresses, thereby achieving conversion characteristics comparable in efficiency and power density to the DRFC itself.

2.2.1 Floating Up-Converter

The basic floating up-converter topology shown in Fig. 2.9 consists of an up-converter cell with a floating ground reference node. The voltage V_{node} at this node is held at an incremental ground by the capacitor C_{node}. Switch Q_{reg}, operated with some duty cycle D,

provides a voltage conversion ratio of

$$\frac{V_{reg} - V_{node}}{V_{in} - V_{node}} = \frac{1}{1 - D} \tag{2.14}$$

where the input and output voltages have been referred to the reference node voltage to give the familiar up-converter equation. During operation, the pre-regulator is controlled like an ordinary up-converter, providing a continuously variable output voltage as a function of duty cycle. As with standard up-converter configurations, the minimum output voltage must be at least V_{in}; for the floating converter, an additional condition for operation is the requirement that the input voltage remain greater than fixed node voltage V_{node}. This condition is easily satisfied in applications where the input voltage is a provided by a regulated source.

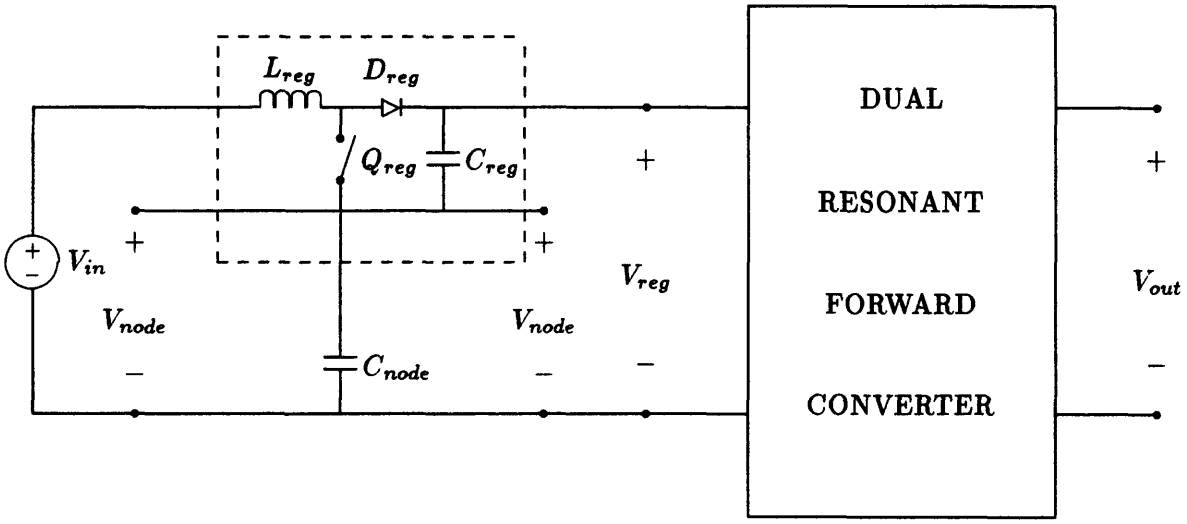


Figure 2.9: Floating Up Converter

The floating up-converter provides significant savings in terms of switch stress and switching losses. These advantages stem from a reduction in the voltage seen by switch Q_{reg}. Ordinarily, the switch would see the maximum output voltage of the converter, and would be rated accordingly. In the floating converter case, however, the switch sees only the *difference* between the maximum output voltage and reference node voltage V_{node}. For many common power conversion applications, the *range* of the input voltage is significantly smaller than the *maximum* input voltage, typically on the order of 20-30%. Reduction of the voltage rating of the switch in turn permits the selection of a switch with a larger current

rating for the same die size, permitting reductions in both conduction and switching losses. These reductions in turn permit increases in switching frequency, making the pre-regulator efficient at high power densities despite its square wave switching transitions.

To illustrate this point, consider the POL application, where a representative input voltage range might be 32–40V, and the node voltage would be fixed at 30V. The DRFC would then be configured to provide its nominal full-load output voltage for an input voltage of 42V. The function of the pre-regulator would be to hold the DRFC input voltage V_{reg} at 42V as V_{in} varied over its range. For an input of 36V, the pre-regulator would operate with a 50% duty cycle to generate the required 42V at the input to the DRFC. The ratings of an appropriate switch for 50W operation would be 200$m\Omega$ at 20V. An industry standard IRFZ24, with a Hex-2 die size and ratings of 100$m\Omega$ and 60V, has a 12V output capacitance of 350pF [20]. For such a pre-regulator, operating at 50W and 5 MHz, the combined switching and conduction losses of the pre-regulator MOSFET would represent less than 1/2% of the input power. Additional capacitive and conduction dissipation in the pre-regulator diode, a 90 mil low-voltage Schottky rectifier, would contribute further losses of 1% of the input power.

Up to this point, no mention has been made of the net charge that flows into the incremental ground node. Of course, this charge must be removed or the node voltage would change. More importantly, this charge flow represents power which must be recovered and delivered to the load, to preserve the efficiency of the converter. Fortunately, a convenient method for recovering this charge exists which simultaneously maintains a constant voltage V_{node} at the incremental ground and interfaces the pre-regulator with the DRFC.

2.2.2 Tapped DRFC with Pre-Regulation

The connection between the DRFC and the pre-regulator provides the method for charge removal at the incremental ground node by means of a tap in each of the transformer primary windings. These taps are fed through a pair of diodes D_{tap}, as shown in Fig. 2.10. The transformer taps maintain a constant ratio between V_{node} and V_{reg}, the regulated input voltage to the DRFC. This, in effect, creates a dual voltage bus across capacitors C_{node} and C_{reg}. This dual bus feeds the transformers of the forward converter, with currents splitting appropriately to maintain a bus voltage ratio equal to the transformer tap ratio. In this way, mid-point charge from the pre-regulator stage is recovered and delivered to the load.

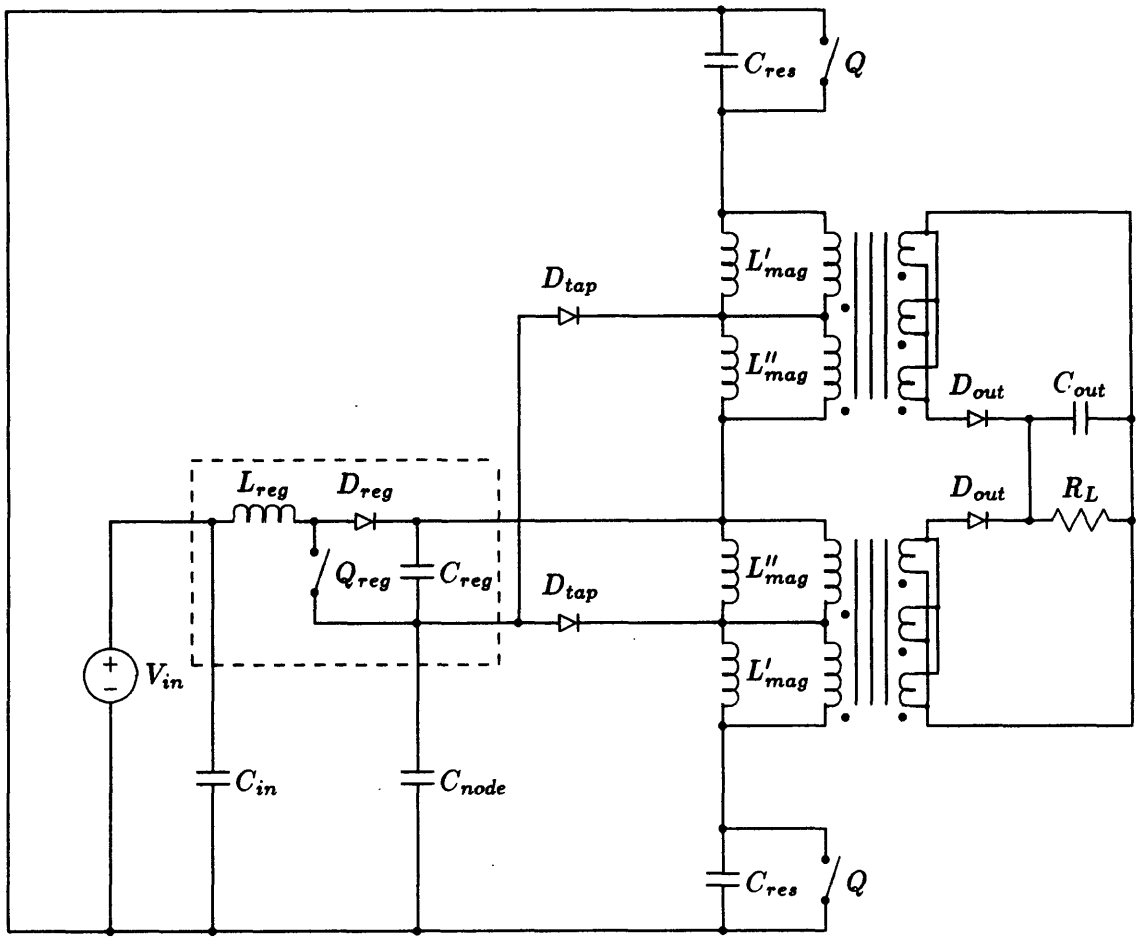


Figure 2.10: DRFC with Tapped Pre-Regulator

The addition of a floating up-converter pre-regulation stage to the DRFC topology permits closed loop control of the converter in POL applications. Output control is achieved with few additional components and with minimal loss. Operation in the upper megaHertz range without loss of efficiency is possible, suggesting that power densities in the 50-100W range are possible.

2.3 Circuit Parasitics

With the introduction of lossless resonant switch transitions, it might seem that the conversion frequency of the DRFC would be unlimited. Such is not the case, however, because the effects of parasitic circuit elements begin to dominate the circuit operation as switching frequencies are raised. For most of the preceding discussion, the components used to

construct the DRFC have been modelled as ideal elements. While such models are useful for qualitative analyses and low frequency operation simulations, the operation of high frequency switching converters is greatly affected by circuit parasitics.

In general, these parasitics can be divided into two classes, based upon their origins. The first group consists of component-inherent elements, such as transformer magnetizing and leakage inductances, and semiconductor junction capacitances. The second group of parasitics originates in the interconnections between components, and includes the component package parasitics and the effects of interconnection methods. Both parasitic types must be understoood in a quantitative manner if accurate predictions of high frequency behavior are to be made. The following sections discuss the origin and effects of the major component, package, and interconnection parasitics in the DRFC topology. In particular, they point out the inherent limits of present components and circuit construction techniques, and present the motivation behind the development of advanced hybrid construction techniques for high frequency switching power supplies.

2.3.1 Component Parasitics

The origin of component parasitics lies in the physical laws governing the materials and fabrication of electronic devices. Real components are not perfect, because the material properties are non-ideal. Conductors have resistance, energy storage elements have losses, and magnetic structures are neither infinitely permeable nor totally coupling. Finally, all components occupy a finite volume, and their three-dimensional characteristics produce parasitic interactions which affect the performance of the circuit.

The major component parasitics which affect the high frequency operation of the single RFC are included in Fig. 2.11, with the pre-regulator section removed for clarity. A majority of these parasitics are directly related to the transformer magnetics, typically the most non-ideal circuit element(s) in a power converter. The distributed parasitic winding capacitance of the transformer is modelled as having both common- and difference-mode components, indicated by C_{com} and C_{dif}. The transformer leakage inductance L_{leak} is referred to the secondary, while the magnetizing inductance is primary-referred, as before. Losses in the transformer occur due to conduction losses in the parasitic winding resistances R_{pri} and R_{sec}, and also due to hysteresis losses in the core, modelled by dissipation in core loss resistor R_{core}.

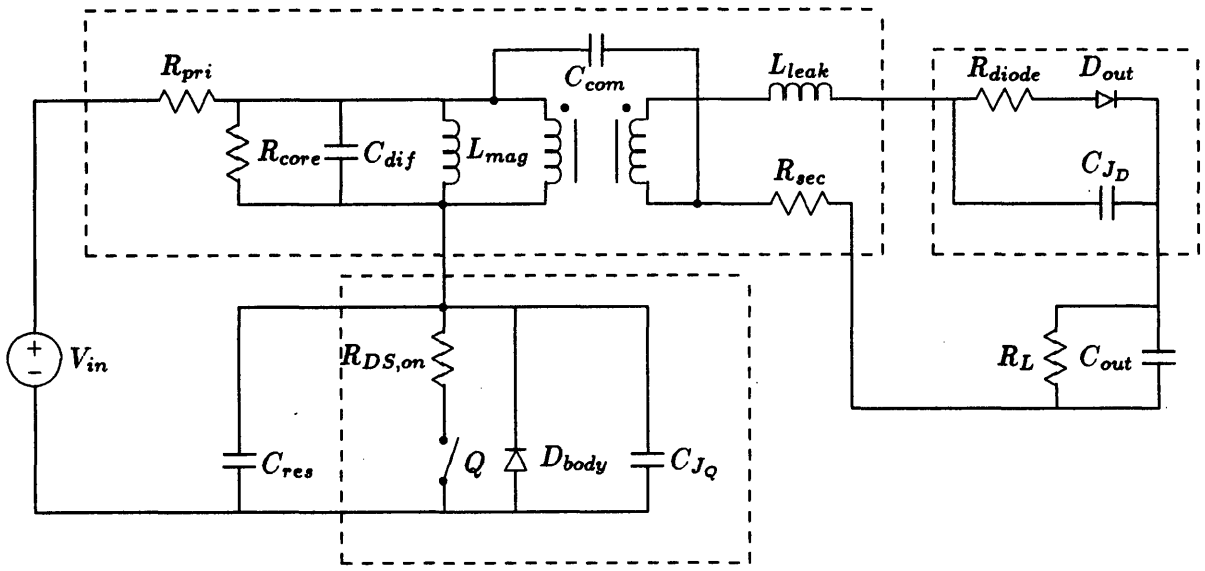


Figure 2.11: RFC with Component Parasitics

The model for switch Q, an N-channel MOSFET, consists of parasitic junction capacitance C_{J_Q} and anti-parallel body diode D_{body}. The output rectifier D_{out} is modelled as having a junction capacitance C_{J_D} and some output resistance R_{diode}. Finally, the ceramic filter capacitors are modelled as having virtually ideal energy storage characteristics. Their package and interconnection parasitics will be considered in a following section.

Transformer Magnetizing Inductance

As discussed previously, one major parasitic element in the RFC is the finite transformer magnetizing inductance. The existance of this element is due to the finite permeability of the core material used in constructing the transformer. This material, commonly a nickel-zinc ferrite for applications in the 1-10 MHz conversion frequency range, has a permeability on the order of 100 μ_o. This parasitic serves as the resonant element in the RFC. Together with the resonant capacitance, it sets the ringing frequency of the converter, as given in Eq. 2.9. Furthermore, it sets the amplitude of the AC magnetizing current, which in turn increases conduction and copper losses, without contributing to power delivery.

Ideally, the magnetizing inductance should be as large as possible, to reduce the magnetizing current. However, practical design trade-offs against higher switching frequencies

(which require a higher resonant frequency and hence a lower magnetizing inductance) and against copper and core losses (both of which increase as the magnetizing inductance is increased) tend to limit the maximum allowable magnetizing inductance. These trade-offs will be examined in detail in Chapter 4, when the design of high frequency magnetics is discussed.

Parasitic Resonant Capacitances

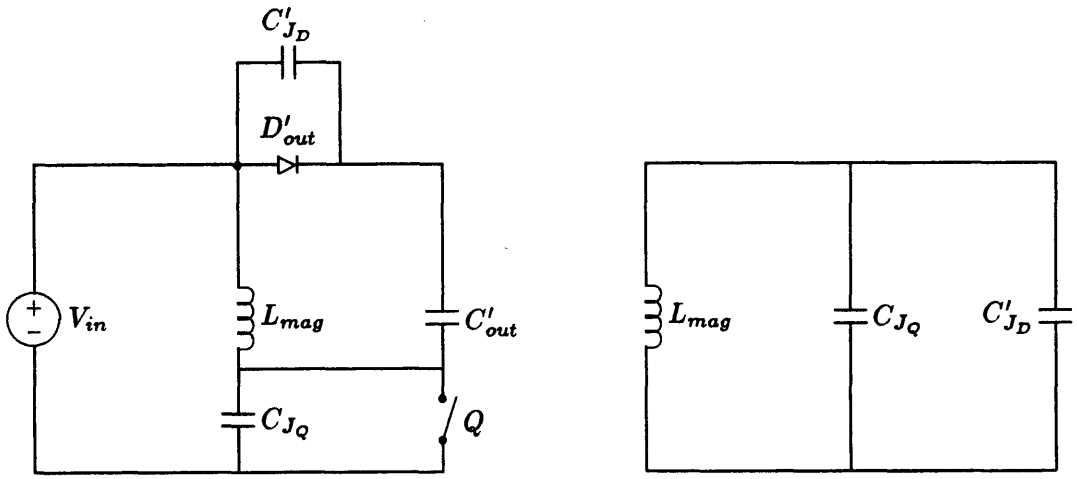
The second major parasitic element of the RFC is the output capacitance of the main MOSFET Q. This capacitance is exploited in the RFC design because it appears in parallel with the resonant capacitor C_{res} and thus reduces the size and cost of the latter. In fact, because of the power MOSFET's high output capacitance, this parasitic capacitance tends to be of sufficient or even excessive size for high frequency conversion applications, and a supplemental resonant capacitor is unnecessary. In this manner, the two major intrinsic component parasitics of the RFC are utilized as independent circuit elements to create a resonant converter, proving beneficial to the circuit operation.

Throughout the off-time of switch Q, the reflected series combination of output rectifier D_{out} and output filter capacitor C_{out} appears in parallel with switch Q. This subcircuit is shown in Fig. 2.12a, where the $'$ represents reflection through the transformer, effectively increasing the impedance of the element by the square of the transformer turns ratio.

$$C'_{out} = C_{out}(\frac{N_s}{N_p})^2 \tag{2.15}$$

Because output capacitance C_{out} is much greater than parasitic capacitance C_{J_D}, the series combination of these two elements is approximately equal to the parasitic rectifier capacitance alone. The reflected value of this capacitance, C'_{J_D}, therefore appears functionally in parallel with switch junction capacitance C_{J_Q}, as shown in Fig. 2.12b. This means that, in addition to switch Q, the output rectifier also has zero-voltage switching transitions, a highly desirable situation not normally found in discontinuous-mode resonant converters [21]. However, one side effect of this reflected capacitance is an increase in the magnitude of the total parasitic resonant capacitance, which reduces the frequency of the resonant ring.

The output capacitance of a power MOSFET is dominated by the drain-source junction capacitance, and is therefore non-linear. In particular, this capacitance is inversely



a) Full Circuit b) Incremental Subcircuit

Figure 2.12: Reflected Output Rectifier Capacitance

proportional to the square root of the voltage across it.

$$C_{DS} \approx \frac{C_{DS_o}}{\sqrt{\Psi_o + V_{DS}}} \tag{2.16}$$

The built-in junction potential Ψ_o is a constant which ranges from 0.4–$0.7V$, depending upon doping gradient profile of the semiconductor fabrication process. Similarly, the parasitic capacitance of output rectifier D_{out} is also a non-linear junction capacitance. These non-linearities cause the resonant frequency to become a function of the input voltage and distort the previously sinusoidal resonant ring waveform. The effect of this nonlinear capacitance is shown in Fig. 2.13, where non-linear capacitance and comparable linear capacitance switch voltage waveforms are superimposed. A numerical analysis reveals that in the non-linear resonant capacitor case, the ring voltage amplitude is now approximately 3.5 times the input voltage (for a 50% duty cycle), as opposed to 2.3 times for the linear case.

Another parasitic element which contributes to the magnitude of the resonant capacitance is the parasitic capacitance of the transformer. This parasitic can be modelled as a pair of capacitors, representing common- and differential-mode parasitics. The differential-mode capacitance is directly in parallel with the magnetizing inductance, and incrementally in parallel with the parasitic junction capacitances. The common-mode capacitance connects the primary and secondary windings, and can be placed across the terminals which serve as incremental grounds for the respective windings during operation, as shown in

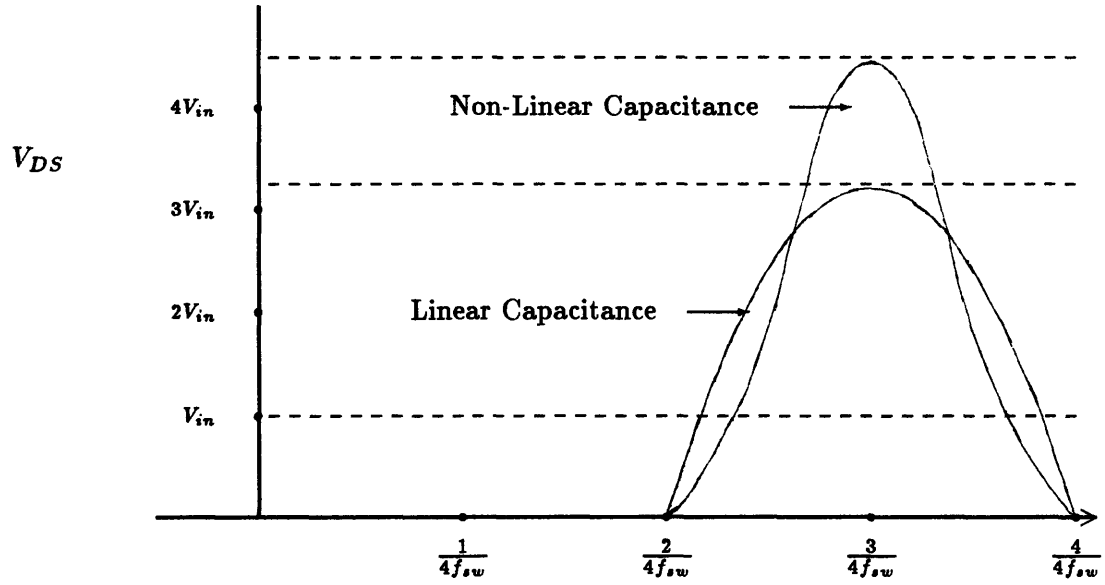


Figure 2.13: Linear and Non-Linear Resonant Ring Waveforms

Fig. 2.11. In practice, the secondary side of the converter might be shorted to the primary, or connected through some large capacitor to suppress any common mode voltages. In such cases, both parasitics effectively load the primary resonant circuit and reduce the resonant frequency. These transformer parasitics are due to interwinding capacitances, which in turn are a function of the construction geometry of the primary and secondary windings. The parasitics are therefore linear elements whose magnitudes can be calculated from the winding geometries.

Inclusion of the transformer parasitic capacitances makes the total resonant capacitance a composite of linear and non-linear elements. This complicates the circuit analysis significantly. However, the actual resonant ring waveform shape must fall somewhere in between the two waveforms shown in Fig. 2.13 for purely linear and non-linear cases, and will depend upon the relative magnitudes of the individual elements. In most cases, the capacitive parasitics cannot be estimated with sufficient accuracy to merit an exact solution, and the bounding conditions prove sufficient for design requirements.

Parasitic Loss Mechanisms

Unlike the magnetizing inductance and parasitic capacitances in the circuit, which together control the switching operation, dissipative parasitics have no circuit function in the RFC topology. These parasitics exist due to the finite conductivity of the component materials, in particular the copper transformer windings and the silicon semiconductor substrates, and due to the hysteresis of the magnetic materials. They have two major effects upon the operation of the RFC in that they lower its efficiency, and they contribute an output impedance to the converter.

The resistive parasitics are the major source of power dissipation within the converter. A great deal of effort goes into reducing the magnitude of the parasitic resistances to achieve the efficiencies necessary for POL converter applications. Because the switch transitions are made at zero volts, all of the power dissipated in the switches and output rectifiers is due to conduction losses. Oversized switches and rectifiers, with their lower $R_{DS_{on}}$ and lower forward drop, are selected despite their greater expense and higher parasitic capacitance. This increased capacitance in turn establishes a practical limit on the maximum switching frequency, as described in the previous section, forcing a trade-off between efficiency and power density.

The parasitic loss mechanisms can be modelled as resistors, as shown in Fig. 2.14. In this simplified circuit emphasizing their effect upon the output impedance, the non-linear output rectifier has been linearized to generate an incremental resistance $R_{D_{on}}$. The transformer winding resistance R_{pri} has been reflected to the secondary and combined with R_{sec} to form R_{trans}, and the switch resistance has been reflected through the transformer to become $R'_{DS_{on}}$. Furthermore, the hysteresis loss parasitic resistance R_{core}, which does not contribute to the output impedance, has been neglected and will be considered in Chapter 4. Finally, the Thevinin equivalent of the pre-regulation stage has been included in the model, and reflected through the transformer to become R'_{reg} and V'_{reg}.

These resistances form a voltage divider between themselves and the load, lowering the output voltage as the output load current $< I_{out} >$ increases. This effect, called load regulation, is minimized by making the dominant impedances as small as possible. The total output impedance due to resistive component parasitics is

$$R_{out} = [R_{reg} + R_{DS_{on}} + R_{pri}](\frac{N_s}{N_p})^2 + R_{sec} + R_{D_{on}} \tag{2.17}$$

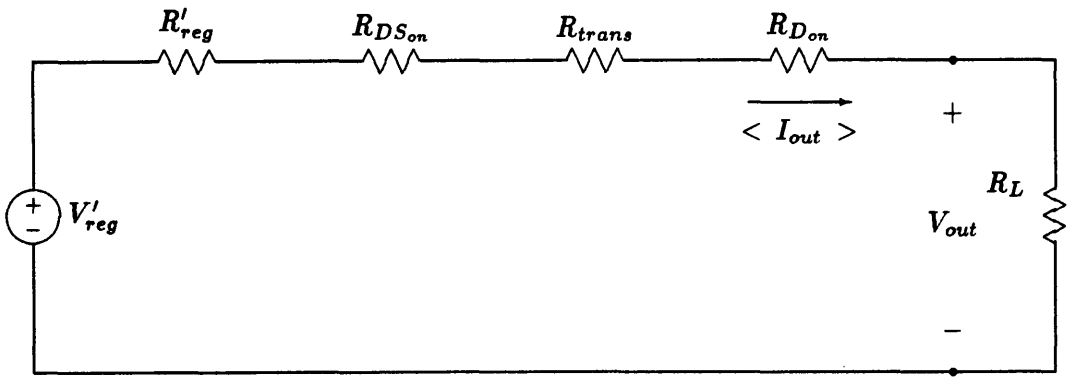


Figure 2.14: Parasitic Output Resistances

For the $50W$, $40V$–$5V$ DRFC topology discussed previously, typical parasitic element magnitudes create an output resistance of $21m\Omega$, or 4% of the minimum load resistance. Such performance might prove satisfactory as a voltage regulator in an open loop configuration, were it not for the fact that other parasitics contribute to the output impedance as well. In general, the total effect of these resistive parasitics dictates the use of a closed loop regulation scheme to control the problem of load regulation.

Transformer Leakage Inductance

One other component parasitic which can contribute greatly to the output impedance of the RFC is the transformer leakage inductance. This inductance exists due to imperfections in coupling between the primary and secondary transformer windings, which permit the fluxes to "leak" around turns rather than coupling them. Every effort is made to improve this coupling and thereby reduce the size of the leakage inductance, as will be described in Chapter 4. Nevertheless, some leakage inductance is unavoidable, and its existence proves problematic for the circuit's operation.

Leakage inductance affects the RFC in several ways. The most significant change in the circuit's operation appears in the modified shape of the load current waveform $I_{out}(t)$. This waveform is shown in Fig. 2.15, with solutions for three possible cases. These cases depend upon the relative size of the leakage inductance, specifically the L/R time constant associated with leakage inductance L_{leak} and the previously described parasitic output resistance R_{out}.

The leakage inductance prevents instantaneous changes in the load current following

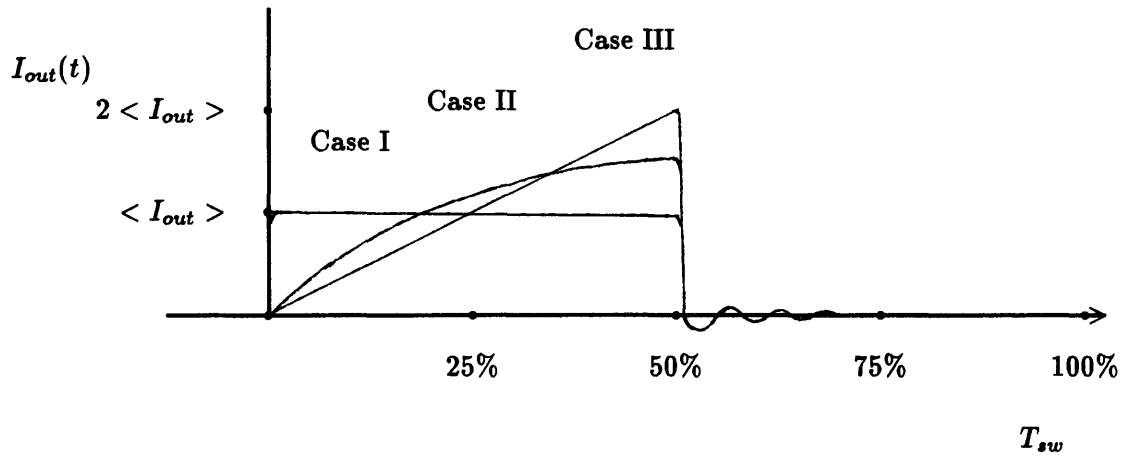


Figure 2.15: Effect of Leakage Inductance on Load Current

either transition of the switch state. Following the switch turn-on transition, the load current rises gradually, because the voltage across the leakage inductance is small. This voltage, the difference between the reflected input bus voltage V_{in}' and the output bus voltage V_{out}, is supported by large ceramic capacitors which, during steady-state operation, assume a small voltage differential just sufficient to drive the output current through the leakage inductance and parasitic resistances. This configuration is shown in Fig. 2.16. When resistive parasitics dominate the output impedance so that L_{leak}/R_{out} is short compared to the switching period, the output current waveform looks square, as shown in Case I. This is similar to the ideal waveform. However, the output voltage is reduced due to the previously described voltage division effect of the output resistance. When the leakage inductance is the dominant impedance in the output path, and the time constant is long compared to the switching period, the current rises linearly, as shown in Case III. Case II lies between these extremes, when the time constant and the switching period are comparable and neither impedance is dominant. In this case, the output current rises exponentially with the L/R time constant.

In each case, the output voltage falls from its zero-leakage magnitude to a value such that the differential voltage driving the current through the leakage inductance is sufficient to produce an average output current equal to the load current. The waveform magnitudes have been normalized so that the average load current $< I_{out} >$ is the same for each case.

Following the turn-off transition, the load current falls abruptly because the primary voltage decays rapidly once the resonant ring begins. In fact, the initial dv/dt across the

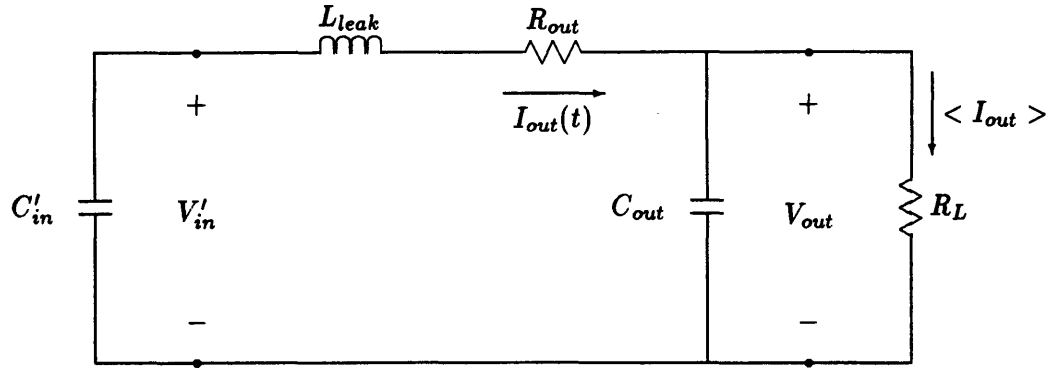


Figure 2.16: Voltage Across Leakage Inductance, Switch On

switch resonant capacitor increases with load current, because the reflected load current $I'_{out}(t)$ continues to flow in the transformer primary momentarily after switch Q turns off. This increases the total charging current into the parasitic resonant capacitors C_{res}, making it the sum of the magnetizing current I_{mag} and the reflected output current $I'_{out}(t)$. This situation is shown in Fig. 2.17, with the secondary components reflected to the primary side. As the resonant ring continues, the load current being carried by leakage inductance L_{leak} decays rapidly. The underdamped secondary loop permits the current through the leakage inductance to go negative as the leakage inductance rings with the output rectifier's parasitic junction capacitance. This high frequency ring, shown in Fig. 2.15, continues for approximately 20% of the switching period and is a source of power loss. The energy stored in the leakage inductance is eventually dissipated through damping in the transformer core and through various resistive processes.

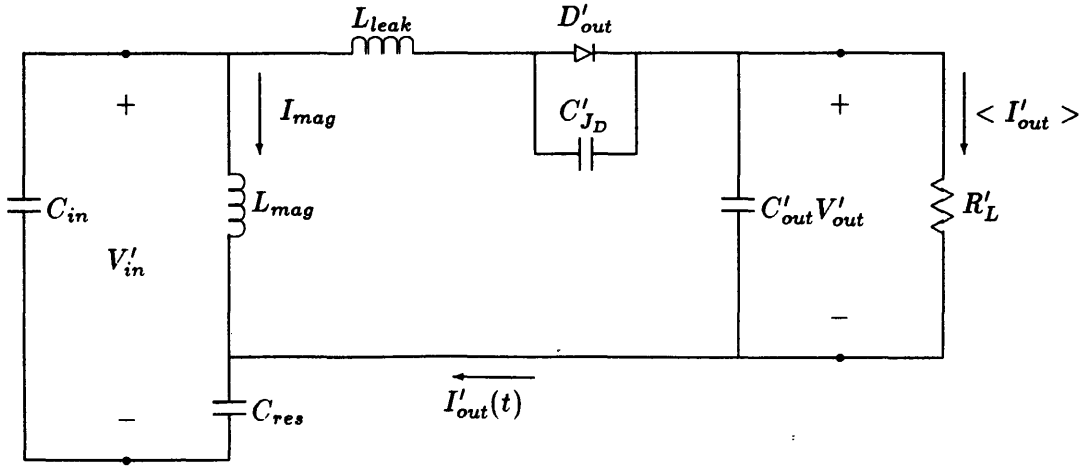


Figure 2.17: Current Into Resonant Capacitor, Switch Off

In summary, the transformer leakage inductance affects the circuit operation in four significant ways. First, it modifies the load current waveform to become less square, increasing conduction losses due to higher peak currents. Second, it introduces an additional impedance between the input and output voltage busses, contributing further to load regulation. Third, it creates a high frequency ring in conjunction with the output rectifier's parasitic capacitance, dissipating the leakage energy stored at switch turn-off. Finally, it increases the dv/dt seen by the primary side switch, and introduces a slight load dependence to the resonant ring waveform. These effects, all undesirable, provide motivation for the development of low leakage transformer designs for high freqency power conversion applications. This subject is addressed in depth in Chapter 4 of this document.

Summary of Component Parasitics

The preceding section has described a number of circuit parasitics which are due to present-day limitations in component designs. These parasitics exist independently of the package and interconnection methods selected for constructing the circuit. Some, like the transformer magnetizing inductance and interwinding capacitance, and the semiconductor junction capacitances, have been incorporated into the topology by clever circuit design. Others, like the transformer leakage inductance and the resistive parasitics, are less benevolent and must be minimized. Alternatively, the previously described component parasitics can be grouped based upon their effects upon the circuit's operation: some were shown to increase power dissipation and thereby reduce efficiency, and others tended to reduce the resonant frequency and hence power density. In both cases, selecting components and operating points involves complex trade-offs between these parasitics, requiring several iterations before an optimal combination is obtained.

2.3.2 Package and Interconnection Parasitics

In conjunction with the selection and optimization of components to minimize the effects of their parasitics on the operation of the circuit, it is necessary to consider the additional parasitics introduced by the component packages and the interconnections between these packages. These additional parasitics frequently dominate the intrinsic device parasitics, masking any performance improvements that might otherwise be gained by the selection of superior components. In most cases, these additional parasitics simply increase the

magnitude of the original parasitic. Indeed, it is often difficult to differentiate between the two types, and in some cases such separation may be unnecessary. However, when the combined effects of these parasitics begin to limit the performance of the circuit, it becomes useful to identify those elements that can be reduced or eliminated.

Because the circuit designer has significantly greater control over the selection of component packages and interconnection media than over the intrinsic characteristics of devices, understanding the origin and effects of these additional parasitics offers a significant potential for circuit performance enhancement. This selection process requires a complete understanding of the parasitics involved, and their effects upon the operation of the ciruit. The following section therefore expands the previous analysis of component parasitics and their effects to include the additional parasitics introduced when combining these components into operational systems.

Secondary Side Loop Inductance

As discussed previously, the most critical component parasitic element is the transformer leakage inductance, and various efforts are made to minimize its magnitude. Unfortunately, significant additional parasitic inductance is introduced when this transformer is connected to the secondary circuitry. Besides the transformer itself, and the secondary termination which may have an inductance comparable to the leakage inductance, the entire circuit loop adds additional parasitic inductance. This electrical loop, consisting of the transformer, the secondary termination, the output rectifier, the output capacitor, their packages, and the interconnection between these packages, adds additional inductance which appears in series with the transformer leakage inductance. Furthermore, because it is located on the secondary side of the step-down transformer, the magnitude of this additional inductance, when viewed from the primary side of the transformer, appears to be multiplied by the *square* of the turns ratio.

The magnitude of the inductance of this loop depends greatly upon the methods used to package the components, and the interconnection medium between these packages. For standard printed circuit board (PCB) construction, the packages of the rectifiers and capacitors can introduce parasitic inductances several orders of magnitude greater than the intrinsic device inductances themselves. The interconnections between components, even when made by conductive traces on opposite sides of the circuit board, can add additional

inductance on the order of the transformer's internal leakage inductance. These additional parasitics prove unacceptable for high frequency applications where the added inductance makes the output impedance unreasonably high and the leakage ring losses make the efficiency too low.

This is one of the main motivations for utilizing advanced hybrid packaging techniques to construct the DRFC. The parasitics associated with thick film hybrid interconnections are extremely small, typically less than 5% compared to traditional PCB construction. Furthermore, the use of ceramic substrates permits the reduction or elimination of component packages, greatly reducing the associated parasitics while increasing the component packing density. These advantages are presented quantitatively in the first section of Chapter 3 on multi-layer copper hybrids.

Primary Side Loop Inductance

A similar argument can be made for the loop inductance on the primary side of the transformer. While the magnitude of the parasitic inductances on this side are not multiplied by the square of the transformer turns ratio, they still contribute directly to the total apparent leakage inductance. Furthermore, the inductance associated with packages for the primary-side components, and the MOSFET switch in particular, can be significant. Again, the use of hybrid construction permits direct bonding of the unpackaged semiconductor die, greatly reducing the associated lead frame inductances.

Pre-Regulator Loop Inductance

Little mention has been made of the effect of component parasitics on the performance of the pre-regulator, apart from their contribution to its output resistance, because a square wave converter was analyzed in detail during the derivation of the DRFC, and the component parasitics in the pre-regulation stage are completely analagous to those in the RFC stages. However, it was also concluded during this derivation that, in general, square wave converter topologies are unacceptable for high frequency conversion applications. This conclusion was based upon the losses associated with the circuit's operation in the presence of both component and interconnection parasitics. Yet it is possible to operate this square-wave pre-regulation stage at switching frequencies in the megaHertz region without significant penalties in conversion efficiency. It turns out that this is made possible by

several interrelated factors.

First, the topological modification that reduces the voltage stress seen by the switch permits the selection of a switch with a much lower parasitic on-state resistance, reducing conduction losses. Furthermore, by reducing the switch voltage, the $1/2CV^2$ switching losses associated with discharging the parasitic junction capacitance of the MOSFET each time it turns on are decreased as well. Finally, careful layout and the correct choice of component packages and interconnection methods helps to reduce the parasitic loop inductances. These inductances, found in the circuit branches between which the currents must commutate during switch transitions, are the major cause of long commutation periods. Their reduction lowers the switching losses of the converter, overcoming the major impediment to the use of square wave converters at high frequencies. As was the case with the other parasitic loop inductances in the circuit, the use of hybrid construction permits the attainment of sufficiently small parasitics to enable efficient operation of the pre-regulator. Thus, by minimizing the interconnection parasitics, a very simple up-converter can provide output voltage control for the DRFC.

Resonant Drain-Source Capacitance

Like the parasitic capacitances discussed previously, the additional capacitance associated with the component packages and interconnections tend to reduce the switching frequency of the converter. The main additions to this total capacitance come from the package of the MOSFET switch and the interconnection traces at the drain node. Standard fabrication techniques produce a MOSFET which uses the bottom surface of the die as the drain contact. This surface is typically bonded to the component package, which in turn connects to the circuit. In many layouts, the source connection is brought in close proximity to this package to minimize the parasitic inductance. Unfortunately, this connection technique creates coupling between the package and the source, substantially increasing the drain-source capacitance and hence the total resonant capacitance of the circuit. In addition, interconnect traces connecting to the drain node are generally run over a ground plane, further increasing this capacitance. These capacitive parasitics can be reduced by using hybrid construction, which permits the elimination of the package and reduces the length of capacitive traces.

Gate Drive Loop Inductances

One final area in which package and interconnection parasitics greatly affect the circuit performance is the gate drive circuitry. Large parasitic inductances in the current paths of this subcircuit can greatly reduce the switching speed of the MOSFETs, which are inherently fast devices but which require substantial control charge. This charge is typically provided by a large capacitor C_{big}, and switched in and out of the gate by a driver IC U_{drive}, as shown in Fig. 2.18.

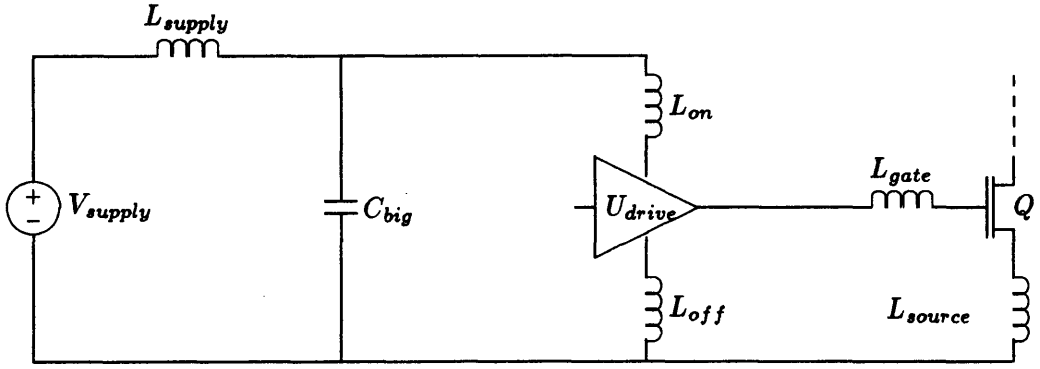


Figure 2.18: Gate Drive Loop with Parasitics

The charge and discharge times are limited by the gate drive voltage applied to the circuit, and the total loop inductance through which that charge must be forced.

$$V_{drive} = L_{loop}\frac{\Delta I}{\Delta t} = L_{loop}\frac{\Delta Q}{(\Delta t)^2} \tag{2.18}$$

$$\Delta t \propto \sqrt{\frac{L_{loop}}{V_{drive}}(\Delta Q)} \tag{2.19}$$

In practical applications, the gate drive voltage is limited by both power dissipation considerations and gate oxide breakdown safety margins. Therefore, to increase the switching speed of the MOSFET, the parasitic inductances in the loop must be reduced. This in turn means reducing the package and interconnection inductances, since the component inductance is both relatively small and inherently fixed. Once again, the use of hybrid circuit construction enables significant reduction of these parasitics, providing further motivation for the development of a viable hybrid process for the construction of high frequency power converters.

2.4 Summary of DRFC Topological Issues

This chapter has introduced the DRFC high frequency switching converter topology, explained its operation, and shown its advantages over square-wave converters and other discontinuous resonant converters. The presence of component parasitics and non-linear circuit properties have been taken into account, and their existence has been exploited wherever possible. The inclusion of additional parasitics, due to the component packages and interconnection methods commonly used for converter constructiontoday, has been shown to severely limit the performance of high frequency converters whenever both power density and conversion efficiency are critical. Finally, hybrid construction has been introduced as a possible means of addressing these limitations by reducing unwanted package and interconnection parasitics.

The following chapter will describe the development of a multi-layer copper hybrid process designed to complement the goals of high frequency power conversion. Beginning with a more quantitative comparison of hybrid circuits and PCBs, it provides the basis for confidence in hybrid circuit construction as a solution to the problems of component and interconnection parasitics. Then, following a comparison of the various thick film hybrid varieties, the chapter describes the final copper thick film hybrid process that was developed and utilized in the construction of a series of working converter prototypes. Finally, it addresses manufacturing and reliability issues, and summarizes the characteristics which differentiate hybrids and PCBs.

Chapter 3

Multilayer Copper Hybrids

Many techniques have been developed to electrically and mechanically join the numerous components which form the foundation of today's electronic circuits. For most applications, the industry standard has been the copper-clad printed wiring board (PWB). The PWB component interconnection technique has reached a maturity level which enables manufacturers to produce complex electronic systems inexpensively and with a high degree of consistency. This combination of low cost and high yield has in turn made the PWB a primary choice for a wide range of commercial electronic applications. Despite it's apparent economic advantages, however, the PWB has several limitations for power circuit construction, including poor thermal conductivity, limited operating temperature, and significant interconnection inductance. The recognition of these limits upon the achievable efficiencies and power densities of switching power converters has prompted the search for superior component interconnection and circuit construction alternatives.

Advanced hybrid circuit fabrication technologies have emerged as one such alternative. Hybrid circuits offer several options for power circuit construction which have the potential to vastly improve the state-of-the-art in switching power supplies. The thick flim conductor and ceramic substrate systems used in the construction of hybrid circuits possess superior thermal, mechanical, and electrical characteristics compared to standard phenolic or epoxy-glass PWB systems. Furthermore, the ability to bond and electrically connect bare, unpackaged semiconductors in dice form directly onto the substrate eliminates the additional size, thermal resistance, and electrical parasitics of the component packages. These advantages of hybridization permit higher operating frequencies and greater power densities, with potentially improved reliability and simplified converter manufacturing.

The first section of this chapter compares the salient characteristics of the thick film

ceramic substrate system with the PWB system, showing the benefits that can be reaped from the utilization of thick film hybrids for switching converters in applications such as the POL converter. A representative variety of thick film conductor systems are then discussed and compared, and a copper based thick film system is shown to have the greatest potential for high performance with relatively low cost. The third section provides a detailed description of a multi-layer copper thick film substrate production process, specifically developed for the POL converter application. The final section of the chapter discusses important manufacturing and reliability issues which must be addressed when considering the use of copper hybrid construction techniques for high frequency power conversion applications.

3.1 Comparison of Hybrid Substrates and PWBs

Thick film hybrids and PWBs can be compared in a number of areas, depending upon the specific interests of the user. As described previously, the greater use of PWB construction in generic circuit applications reflects the combined savings of cost and complexity over hybrid circuit construction. The use of hybrid construction is generally motivated not by economics, but by the need to overcome the performance limitations of PWBs. Because it is this issue of performance that motivates the use of hybrids, issues related to the performance of hybrid circuits will serve as the basis for the following comparisons between the two construction technologies. It is implicitly assumed that, for applications where the limitations imposed by PWB construction are not a handicap, the greater complexity and cost of present-day hybrid circuit construction processes would discourage their utilization.

There are several common materials used in the construction of PWBs. The two industry standards, CEM-3 and FR-4, are both composites of solids and resins. CEM-3, often referred to as phenolic, contains compressed cardboard-like cellulose fibers in a resin glue, while the fire-retardent FR-4 material contains glass fibers immersed in epoxy. Several hybrid circuit substrate material options exist as well, spanning a wide range of material characteristics. The most commonly used materials are alumina (Al_2O_3) and beryllia (BeO), but silicon carbide (SiC) and aluminum nitride (AlN) are rapidly gaining acceptance as alternatives. The popularity of alumina is primarily due to its low cost, its non-toxicity, and its low thermal coefficient of expansion (TCE), which closely matches that of silicon. In more demanding applications, beryllia is used because of its superior thermal conductivity, despite its greater TCE and toxic byproducts. The development of the latter two ceramics

is prompted by the growing need for materials which combine the benefits of the former materials while reducing or eliminating their weaknesses. These four substrate materials will be used in the following comparison of the physical properties of the PWB and hybrid substrate characteristics.

An evaluation of the performance of any construction media under consideration for use in an electrical interconnection system must be based upon an understanding of the functions that the media is required to execute. In the case of PWBs and hybrids, these functions can be grouped into three main categories. First, the electrical properties of the component interconnections afforded by the media are of primary importance. In addition, the mechanical characteristics of the interconnection media are an important criteria, because the components are attached to and supported by the circuit board or hybrid substrate. Finally, the heat generated by the operation of electrical circuits, and especially power circuits, must be removed to the surrounding environment, which in turn may be at an elevated temperature. Thus, the thermal properties of the media must also be considered. These three areas of mechanical, thermal, and electrical properties will serve as the basis for comparisons betweeen the hybrid circuit and the PWB construction options.

3.1.1 Mechanical Characteristics

The mechanical characteristics of interest relate to the ability of the construction media to support the weight of components without excess deformation, which tends to degrade or disrupt the electrical performance of the interconnections. This ability must remain intact, over the expected life of the system, in an environment which may induce mechanical, thermal, and chemical stresses upon the system. Thus, high mechanical strength and rigidity and environmetal stability are desirable qualities for the construction media.

The physical properties of standard PWB materials are well documented [23], and provide a base-line for comparisons. The important characteristics of CEM-3 and FR-4 are compiled in Table 3.1, along with the corresponding properties of the hybrid substrate materials [24]. The difference in flexural strength between the CEM-3 and FR-4 materials is significant, with the strength of FR-4 being comparable to that of ceramics. The lower TCE of ceramics is a distinct advantage over both PWB media, however, as is the intrinsic non-directionality (isotropy) of the ceramics. In contrast, both CEM-3 and FR-4 materials exhibit a grain orientation which causes different flexural strengths and TCEs along the two

planar axes. This can aggravate stresses and prompt board warpage with PWB construction, making component attachment difficult and less reliable. Furthermore, the chemical resistance of ceramic materials is superior, in particular their reduced tendency to absorb moisture.

	Printed Wiring Boards		Hybrid Substrates			
	CEM-3	FR-4	Al_2O_3	BeO	AlN	SiC
Flexural Strength (kg/cm^2)	740 845	3500 4200	3000	2500	3800	4500
Thermal Expansion ($ppm/°C$)	12 17	10 15	6.7	8.0	4.3	3.7
Moisture Resistance (relative)	Poor	Fair	Good	Good	Good	Good
Max Operating Temp ($°C$)	125	140	>200	>200	>200	>200
Thermal Conductivity ($W/K\,cm$)	0.0025	0.0026	0.30	2.3	1.3	2.7

Table 3.1: PWB and Hybrid Substrate Physical Properties

3.1.2 Thermal Characteristics

The thermal characteristics of the substrates are also superior compared to the PWB materials. In particular, the thermal conductivity of the various substrate materials can be several orders of magnitude greater than the PWB materials. This high conductivity permits the removal of heat directly through the substrate, eliminating the need for a separate low impedance thermal path from the components to the environment.

Together, the superior mechanical and thermal properties of the hybrid substrate media enable the connection of components directly onto the substrate, eliminating individual component packages while providing an intimate interconnection medium. The substrate provides mechanical and electrical support for the components, protects them from the environment, and removes heat from them, all without requiring the packages normally associated with the mounting of components on PCBs. This elimination of component packages provides tremendous savings in terms of size and circuit density. In addition, it virtually eliminates the electrical parasitics associated with the component packages themselves, another significant savings for applications where high frequency signals are present.

3.1.3 Electrical Characteristics

Having reviewed the physical characteristics of hybrids and PWBs, assessing their relative worth in terms of their suitability for component mounting, their functionality as electrical interconnection media will now be considered. Beyond the benefits realized by the elimination of the component packages, hybrid circuit construction provides lower impedance interconnections between these components. In the case of PWBs, the conductors which form the electrical interconnections between components are on opposite sides of the board, and the board material forms the dielectric insulator between conductor layers. The electrical properties and physical dimensions of the board are therefore critical. In contrast, typical hybrid interconnection systems utilize alternating layers of conductor and dielectric laminated to a single side of the substrate, permitting increased freedom in the selection of substrate thickness and dielectric properties. A comparison of the electrical properties of hybrids and PWBs therefore depends upon the particular characteristics of the thick film system being employed in conjunction with the hybrid substrate material.

As with the physical properties of PWBs, the electrical properties are well documented [23], and a number of formulae exist to aid in the calculation of interconnection parasitics. In general, the parasitics of interest are the inductance, capacitance, and resistance of interconnection paths between components. A generally accepted comparison method is to specify these parasitics in terms of capacitance per unit area (C/in^2), inductance per square ($L_\square$) and resistance per square ($R_\square$). For the purposes of comparison, these specifications will be made for the typical case of a single conductor over a ground plane, as shown in Fig. 3.1. The conductor is defined to have a uniform width w_c, thickness t_c, and resistivity ρ_c. For the calculation of interconnection capacitances, the conductor is further defined to have a length l_c. The spacing between conductors (the dielectric thickness) t_d is assumed to be small compared to w_c, and has a permeability μ_d and permittivity ϵ_d. The thickness t_g and resistivity ρ_g of the ground plane are equal to that of the conductor above it, while the width of the ground plane w_g is assumed to be much greater than the other dimensions.

Based upon this geometric model of the interconnection traces, a series of equations describing the parasitics can be derived. These derivations are not presented here, but can be found in most field theory textbooks [25]. The equation for the resistance of the

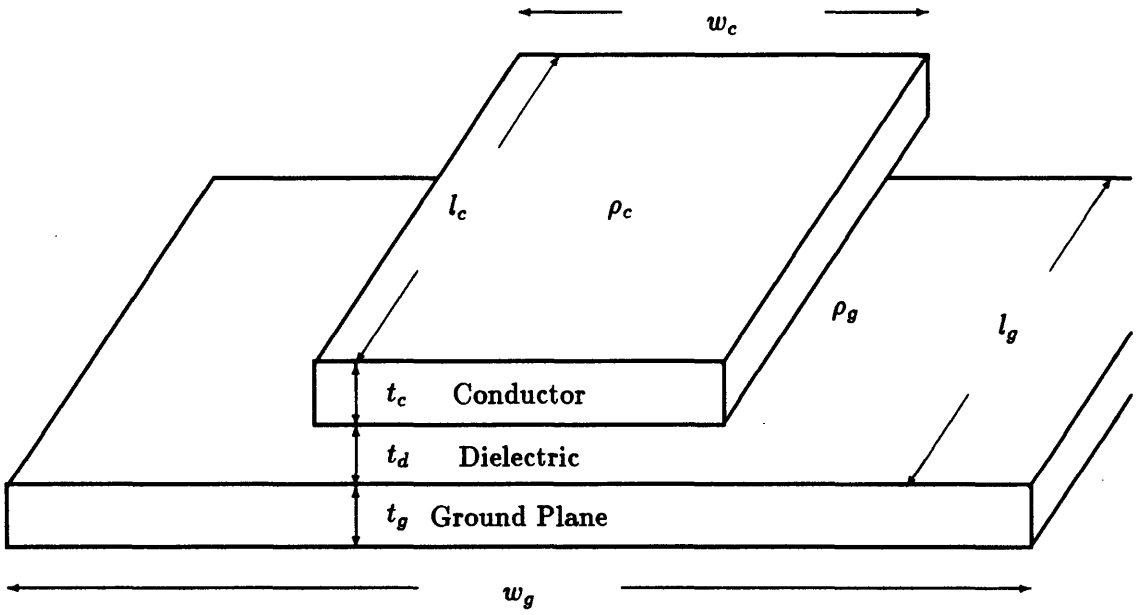


Figure 3.1: Interconnection Conductor Model

interconnection, per square, is

$$R_{\square} = \frac{\rho_c}{t_c} \tag{3.1}$$

In cases where the width of the ground plane w_g is comparable to the conductor width, or when the L/R time constant of the interconnection is long compared to the time constants of the circuit, the resistance of the interconnection loop will be the sum of the resistances of the conductor and the return path

$$R_{\square,loop} = \frac{\rho_c}{t_c} + \frac{\rho_g}{t_g} \tag{3.2}$$

effectively doubling the loop resistance. These equations suggest that the way to minimize the parasitic resistance of the interconnections is to use a conductor with the minimum resistivity and the maximum thickness. Unfortunately, limitations on the maximum usable conductor thickness are imposed by the skin effect, which limits the rate at which current can diffuse into the conductors. At high frequencies, this limited diffusion rate causes the current to flow on the surface of the conductor, with the current density decreasing exponentially with depth and thus using only a fraction of the total conductor thickness. The characteristic depth of this diffusion, called the skin depth δ, is given by

$$\delta = \sqrt{\frac{2\rho_c}{\omega\mu_d}} \tag{3.3}$$

where ω is the excitation frequency in radians per second. For a given conductor material and excitation frequency, then, minimizing interconnection resistance involves selecting a conductor thickness that exceeds the skin depth, and then minimizing the number of squares of interconnection.

Similarly, the inductance of a loop of interconnection between components is predicted by the model to be

$$L_{\square,loop} = \mu_d t_d \tag{3.4}$$

For most dielectric materials, the permeability is that of free space, μ_o. Minimization of loop inductances thus requires selection of an interconnection system with the least spacing between conductor layers. This small spacing is one of the major advantages of hybrid circuits over PCBs, as will be shown shortly.

Finally, the parasitic capacitance between conductive layers is found from the model to be

$$C/in^2 = \frac{\epsilon_d}{t_d} \tag{3.5}$$

The permittivity ϵ_d of the dielectric insulators typically used between conductor layers is between 4 and 8 times the free space permittivity, ϵ_o. Therefore, within a factor of two, the LC product of both types of interconnection sysytems remains constant, and optimizing a system to minimize one parameter can increase the other dramatically. Such is the case with hybrid circuits, which minimize parasitic inductance at the expense of the parasitic capacitance between layers.

To make a quantitative comparison between the parasitics associated with PWB and hybrid substrate interconnections, typical values are given for three interconnection methods, and the magnitudes of the parasitics are computed for each system. A double-sided FR-4 construction with 2 oz. copper (70 μm thick) is selected to represent standard PWB technology, and a copper-based thick film ink system is used to represent the hybrid circuit technologies. In addition, parameters for an advanced multi-layer PWB process are added to the comparison to show the limits of present-day PWB technology. While such processes are not generally used for power converter applications, they provide a good measure of the maximum performance achievable with PWBs.

A summary of the process parameters for these three construction/interconnection methods are given in Table 3.2, along with the associated interconnection parasitic magnitudes. In all cases, the magnetic permeability of the dielectric material was taken to be μ_o. Also,

because the effective permittivities ϵ of the dielectric materials are a function of frequency, the capacitive parasitics were compared at 1 MHz. Furthermore, the capacitance of the multi-layer PCB is doubled, because interconnection traces are normally sandwiched between two shield planes (power and ground) in this type of construction. Finally, the parasitic resistance has been given for both DC and AC conditions, to include the effects of skin depth.

	PCB		Copper	
	Standard	Multi-Layer	Hybrid	units
Conductor Resistivity	.67	.67	1.0	$\mu\Omega$ - in
Conductor Thickness	2.7	1.4	1.2	mils
Conductor Separation	63	8	1.7	mils
Dielectric Constant	4 – 5	4 – 5	6 – 7	ϵ_o
Interconnect Resistance, DC	235	470	1100	$\mu\Omega/\square$
Interconnect Resistance, 5MHz	800	800	1200	$\mu\Omega/\square$
Interconnect Inductance	2000	250	54	$pH/\square$
Interconnect Capacitance	16	260	860	pF/in^2

Table 3.2: Process Parameters and Interconnection Parasitics

The results illustrate the previously mentioned trade-off between capacitance and inductance, as a function of conductor separation. There is a significant range between the minimum and maximum parasitic inductance and capacitance magnitudes, yet the LC product in all cases is equal, within a factor of two. In addition, the combined effect of a thinner conductor and a 50% greater bulk resistivity for the hybrid interconnect system creates a significantly larger DC resistance. With the effects of skin depth at 5 MHz factored in, however, the resistivities of the pure copper and thick film copper conductors become very comparable. The dependence of skin depth upon the resistivity of the conductor increases this effect further. The greater resistivity of the thick film increases its skin depth, and hence its effective conductor thickness, as compared to the pure copper conductors of the PWB technologies.

3.1.4 Summary of Interconnection Method Comparisons

The previous section has described the important mechanical, thermal, and electrical characteristics of PWBs and hybrid substrates, in the context of circuit construction and component interconnection. The general conclusions that can be drawn, in the context of power

conversion applications, are that hybrids are significantly superior for switching power converters, in all three areas. Specifically, the combination of the mechanical strength, rigidity, and stability of ceramic substrates with their thermal conductivity permits the direct physical and electrical attachment of components. Direct component attachment eliminates the bulk of the individual packages, along with their associated parasitics. Combined with the superior electrical performance of the hybrid component interconnection system itself, the overall reduction in the electrical parasitics of the system permits greatly increased operating frequencies. This frequency increase, in combination with the elimination of component packages, will in turn reduce the size and increase the power conversion density and efficiency of the circuit. The remainder of this thesis presents the demonstration of these benefits, through the development and implementation of a hybrid process and through the construction of functional converter prototypes.

3.2 Comparison of Thick Film Systems

The development of a hybrid construction and interconnection system for assembling high frequency switching converters begins with the selection of a specific thick film ink family and a compatible substrate material. The numerous thick film inks in existence can be divided into two main groups based upon their firing atmospheres. Most thick film inks, with the exception of epoxy-based conductive adhesives, are fired at a high temperature to sinter the suspended metallic particles into a single metallic conductor. Metals that oxidize at high temperatures must be fired in an oxygen-free environment, while non-reactive metals can be fired in dry air. The air-fired, non-oxydizing conductor metals tend to contain precious metals such as gold, silver, or platinum, making them expensive, particularly for power circuits where the traces must carry large currents and the quantity of conductor metal is therefore significant. The most common nitrogen-fired conductor metal is copper, which is much less expensive compared to precious metals, and has comparable or superior electrical conductivity. However, the use of an oxidizing conductor material presents complications of its own, associated with the added complexity of maintaining a pure firing environment and preventing surface oxidation in subsequent processing and assembly steps. These complications tend to partially offset the cost advantages of copper inks, making the selection of an appropriate ink family more difficult.

The selection of inks is further complicated by the plethora of available formulations,

optimized for various applications and having restricted compatabilities. The formulation of inks is a complex process which is only beginning to be understood [46,47,39]. In addition to the base metal, most inks contain additional metal alloys, glass or ceramic frit, and screening agents to make the ink printable. Parameters such as the purity and size of the base metal particles, and the relative weight-percentage of each additive, greatly affect the conductivity, adhesion, and solderability of the inks. In the case of multi-layer applications, the compatability with dielectric and resistive inks, and the ability to withstand multiple firing cycles, must also be considered. Finally, the component assembly and interconnection methods must be considered, as most inks are not simultaneously appropriate for eutectic die bonding, soldering, gold and aluminum wire bonding, or thermal epoxy component attachment. A typical family of inks might therefore contain seven or more formulations, each one optimized for a particular function. This section discusses the various ink families, with their associated strengths and weaknesses, and addresses the issues involved in the selection of the appropriate family for power circuit applications.

3.2.1 Air-Fired Ink Systems

Air-fired inks can be subdivided into single-metal and alloy formulations. The single metal conductive inks tend to have far superior conductivities, often by an order of magnitude, compared to the alloys. For example, typical $R_{\square}$ values for silver and gold conductive inks at 0.6 mil fired thickness are 3-5$m\Omega$. Unfortunately, these formulations are both expensive and limited in their scope of applications. In particular, the single metal gold and silver formulations tend to leach badly when soldered, and are intended primarily for eutectic die bonding pads and wire bonding pads on single-layer hybrid circuits. They are generally impractical for power circuit applications, where large metallization areas and component soldering are common.

Typical alloy ink formulations intended for air-firing include various combinations of platinum (Pt), palladium (Pd), silver(Ag), and gold (Au). In the silver ink family, PdAg compositions have increased resistance to silver migration as compared to pure Ag compositions, while the PtAg and PtPdAg have increased solderability and reworkability. Similarly, PtAu and PtPdAu compositions are used with the pure Au inks for multilayer circuits with component soldering. While these alloys have the property of solderabilty which is necessary for power circuit applications, their resistivities are significantly higher, due to their

alloy nature and the presence of anti-leaching additives. Typical $R_{\square}$ values range from 10-50$m\Omega$, about an order of magnitude worse than the corresponding resistances of the pure base metals. While these values can be reduced by building up the conductor thickness, such an approach is both time consuming and costly. Furthermore, the effects of skin depth limit the improvements that can be reaped from such an approach. In power conversion applications, the low AC conductivity of the available air-fired solderable alloys effectively limits the maximum practical conversion frequencies, thereby limiting the maximum power densities of converters as well.

3.2.2 Nitrogen-Fired Ink Systems

The absence of air-firable inks which simultaneously exhibit the desirable qualities of solderability and high conductivity has prompted the development of alternate ink formulations. Copper formulations are a natural choice because copper possesses an extremely high electrical conductivity and yet costs relatively little. Furthermore, it exhibits no migration or leaching effects, and accepts both gold and aluminum wire bonds.

A minimal, low cost nitrogen fireable ink family might consist of a single copper ink for conductors and a dieletric ink to provide insulation between layers. Both inks would be fritted, i.e., they would contain glass or ceramic particles to aid the adhesion between layers. The single conductor material would provide solderable interconnection capabilities and wire bonding compatibility with an $R_{\square}$ of less than $2m\Omega$, for a typical firing thickness of about 0.6 mils. This represents a conductivity of $2.5\mu\Omega$-cm, only 50% greater than pure copper and much less than the solderable, air-fireable alloys (typically in the 10-50$m\Omega$ range).

A number of improvements can be made over such a two-ink system, by selecting additional inks which are optimized for specific functions. For instance, the surface characteristics of frit-bonded conductors are poor due to the presence of glass particles which interfere with solder wetting and wire bonding. Therefore, the use of a fritless conductor formulation can greatly improve these characteristics by providing a smooth, glass-free metal surface. This type of ink utilizes a chemical oxide bonding process which adheres well to other copper inks by creating intermetallic bonds, but it exhibits poor adhesion to the substrate or to dielectrics. A fritless overprint ink can thus be used to coat the underlying conductor layer to produce a double thickness which both adheres well and posseses excellent surface

characteristics. This approach is especially appropriate for power circuit applications where the thickness of each conductor layer is typically built up (to at least a skin depth) by successive printing and firing cycles.

Another type of ink that can improve the performance of multi-layer copper hybrid circuits is the via-fill ink. Vias are small openings in the insulating dielectric which form vertical interconnections between traces on different conductor layers. The thickness of the fired insulating dielectric layers is greater than that of a single conductive layer by a factor of three (1.7 mils vs. 0.6 mils), making connections between layers difficult and unreliable. Via-fill inks are special ink formulations that can fill these deep holes, resulting in a surface which is uniform and planarized. They have thermal expansion coefficients which are matched to the dielectric, reducing the stress in the immediate vacinity of the via opening.

In applications where components are to be soldered, a glass dielectric solder mask ink is desirable. In addition to reducing shorts due to solder bridging, the solder mask aids in the placement of components during assembly, and restricts their movement during solder reflow processing. Furthermore, the mask doubles as a hermetic seal which can be used to encapsulate the entire surface of the substrate, except where connections are to be made. This prevents exposed copper areas from oxidizing over time, and reduces the absorbtion of moisture by the dielectric.

The previously described copper ink family has the potential for providing a total thick film interconnection system for hybrid construction of high frequency power converters. It has the advantages of high conductivity, solder and wire bond compatibility, and low cost. However, it also retains the problems inherent in any interconnection system that utilizes oxidizing conductors. In particular, fabrication of the substrate and processing and assembly of the hybrid must be implemented without excessive conductor oxidation. The following section describes the fabrication process for creating multi-layer copper thick film substrates suitable for use in the construction of high frequency switching power supplies.

3.3 Multilayer Copper Thick Film Substrate Fabrication

Based upon the previous analysis, work was begun on the development of a hybrid fabrication process utilizing nitrogen-fireable copper inks. This section discusses the printing, drying, and firing (PDF) techniques used to fabricate a multilayer thick film hybrid sub-

strate. In general, it outlines an optimized version of the fabrication process, which was used to construct the experimental converter prototypes. Additional information is included to facilitate the development of a custom assembly process to fit a variety of needs and circuit applications. Descriptions are given, where appropriate, to indicate the steps leading to this optimized version of the fabrication process to eliminate any duplication of effort by others attempting to repeat this process.

3.3.1 Screen Preparation

The first step in the fabrication of thick film substrates is the preparation of the screens. Issues concerning layout techniques, including the minimization of parasitics and the observance of design rule tolerances, are quite similar to those faced when designing standard PWBs, and will be discussed in depth in Chapter 5 when the layout of the prototype converter is discussed. For now, it is assumed that photoplots of the various conductor and dielectric layers have been generated successfully. The photoplotted layouts are transferred to the screen emulsion using the familiar expose-develop-etch process. The emulsion is removed in those areas in which the ink is to be applied, leaving a bare screen mesh through which the ink can flow and deposit on the substrate. For the purposes of this research, the screens were sent to an outside agent for preparation according to specified parameters [1].

There are a number of parameters which must be determined when making screens for printing thick film inks. The screens should be oversized by 400-900% in area compared to the size of the ink pattern, to reduce the non-uniformities associated with printing near the screen borders. The screen material itself is made of stainless steel, and is specified by the thread pitch p_{thread}, measured in threads per inch. Common pitches used for printing conductor and dielectric inks are 325 and 200 t.p.i., with thread diameters d_{thread} of 0.8-1.7 mils. A knuckle gap $G_{knuckle}$, representing the space between threads at their intersections, of about 10% of the thread diameter is also standard. The percentage of the screen surface area which is not blocked by threads, A_{open}, is typically around 50%. The thickness of the wet ink print is affected by these parameters, and also by the thickness of the emulsion $t_{emulsion}$. A formula for calculating the approximate thickness of the wet print can be

[1] Special recognition is given to UTZ Engineering, Inc. of Clifton, NJ, which donated the materials, expertise, and processing labor required to prepare the screens, free of charge.

derived from these parameters.

$$t_{print} \approx [t_{emulsion} + d_{thread}(2 + G_{knuckle})]A_{open} \tag{3.6}$$

Screens are classified according to their thread pitch, rather than their thread diameter. To make use of the above formula, then, the thread diameter must first be calculated. By making use of the screen open area parameter, the thread diameter is found to be

$$d_{thread} = \frac{1 - \sqrt{A_{open}}}{p_{thread}} \tag{3.7}$$

The thread pitch determines the maximum resolution achievable from a screen, with higher thread counts producing finer lines and spaces. Offsetting the thread orientation by 45° from the print-head also improves resolution by reducing the effects of the finite thread diameter. Based upon the thread pitch required to resolve the circuit trace patterns, the desired thickness of the fired ink, and the average ink shrinkage during firing, the correct emulsion thickness can be specified.

In some cases, it is desirable to screen print solder pastes or epoxies onto the finished substrate so that the components may be mounted simultaneously or in groups. This is typically done with much coarser screens, with thread pitches of 80 t.p.i. being common. Resolution is less critical, and the larger screen openings reduce clogging due to the larger particles contained in the epoxies and solders. A much thicker emulsion is also used for the solder pastes, generally 5-10 mils as compared to the sub-mil thicknesses required for most thick film inks. This permits a greater deposition of material, as required for component attachment purposes, but limits the resolution of the print.

3.3.2 Substrate Preparation

Following the preparation of the screens, another preliminary step in the fabrication of thick film substrates is the preparation of the substrate ceramics. In some applications, it may be advantageous to have a finished hybrid with features cut into the substrate. These features might include a non-rectangular outline to fit a special package, edge notches or holes along the border for input/output connection pins, or component clearance holes in the central region of the substrate. These features can be created prior to firing the ceramic itself, while it is in a semi-pliable "green" state, by punching or stamping with templates. Feature shaping at this stage is normally performed by the ceramic manufacturer to customer specifications. If the features are to be added after the ceramic is fired, when the ceramic

is much harder and more brittle, they are made by laser cutting, abrasive jet spraying, or grinding. These procedures are more expensive and less efficient, but produce tighter tolerance features than pre-firing methods, due to the shrinkage and slight deformation that occur during firing of the green ceramic. Furthermore, they can be used after the hybrid is completely assembled and tested, permitting the handling of more convenient oversized substrates during production. When no features are required, straight line cuts can be made by scribing and breaking.

Once the substrate has been cut to shape, it must be cleaned to ensure that no contamination of the thick film conductors occurs. Cleaning is commonly performed chemically, thermally, or by using the two approaches in combination. Chemical cleaning tends to remove most contaminants, including body oils which may accumulate from excessive handling (one reason that the substrates should be handled with sterile gloves at all times, even during the cutting stages) and any dust or surface particles. The use of chemicals has several disadvantages, however. They can be expensive, and they are difficult to dispose. Furthermore, they can leave new deposits, due to reactions or impurities in the chemicals themselves. For this reason, a series of progressively weaker solvents is commonly used, with subsequent solvents removing any contamination left by the preceding ones. A recommended progression is 1,1,1 trichloroethane, followed by methanol, acetone, and finally de-ionized water. A nitrogen blow-dry between rinses can further enhance the effectiveness of chemical cleaning.

The availability of a high temperature firing furnace makes thermal cleaning much more convenient. A single pass through the firing furnace at temperatures between $800°C$ and $1000°C$ tends to burn off any impurities which might otherwise react with the inks during subsequent firings. The main disadvantages with this approach are the time involved (a single pass takes 25 to 50 minutes) and the possibility of depositing the contaminants on the interior of the furnace, from where they may later redeposit onto other substrates being fired. A thorough cleaning that uses chemical solvents to remove any gross contamination, followed by thermal cleansing to burn off any remaining particles, gives excellent results at the expense of both time and chemical resources.

The final step in the preparation of the blank substrates is the application of identification markings. These markings are especially beneficial for developmental work, when process parameters may be adjusted in mid-operation, and the effects of these adjustments

require correlation to the appropriate substrates. For common processing facilities which lack laser scribes or other exotic methods of marking the substrate itself, a simple grease pencil can be used. The mark from the pencil tends to burn off during firing, but leaves a permanent residue which remains legible after numerous firings. Care must be taken to apply the mark or label in a location which will not be obscured by subsequent layers of thick film, or by the final assemblage of components. For multi-layer hybrids, the task of marking the substrates can be postponed until after the application of the first metallization layer. At this point, the identification can be scribed into a metal conductor, exposed ground plane, or specially designated labelling area.

3.3.3 Heatsink Metallization Application

In cases where good thermal contact between the substrate and the heatsink is critical, a backside metallization is often the first layer applied to the freshly prepared substrates. This metallization layer facilitates the direct solder attachment of a heatsink or heat spreader to the substrate. The greater thermal conductivity of solders (0.2 $W/K\,cm$) compared to epoxies or other thermally conductive adhesives (0.003-0.006 $W/K\,cm$) can significantly reduce the thermal impedance between the substrate and the heatsink. In high power multilayer hybrid circuits, in which bare semiconductor dice are solder bonded to the metallized substrate, the interface between the substrate and the heatsink can represent the largest thermal impedance in the system. The availability of a solderable backside metallization can reduce the thermal rise of the junction temperatures in such a system by 50% or more. These backside metallizations are generally applied first because they are solid, featureless patterns which don't interfere with the processing of the component side.

A fritted ink formulation should be selected for the backside metallization to maximize the ink adhesion at the metal-substrate interface. The shear stresses applied at this interface can be significant when the thermal expansion coefficients of the substrate and heatsink material are not well matched, and poor metallization adhesion may cause delamination over time and thermal cycling. A second concern involves voids in the solder joint which occur due to poor solder wetting of the backside metallization surface. These voids leave air pockets between the substrate and the heatsink, creating hot spots with potentially destructive consequences. The application of a second backside metallization layer addresses this concern in two ways. First, the additional thickness enhances the metallization layer's

ability to act as a heat spreader, assisting in the conduction of heat away from these areas. Furthermore, a high purity, fritless, oxide-bonded ink formulation may be used for the second metallization, because oxide bonding yields acceptable adhesion between similar metallic conductors. The superior surface properties of fritless metallic inks greatly improve the wetting characteristics of the solder, thereby reducing the incidence of solder voids. This is especially beneficial because the backside metallization remains exposed throughout the remainder of the substrate processing and hybrid assembly steps.

Despite the care that is exercised during the application of the backside metallization layers, surface oxidation inevitably occurs during these subsequent stages. The substrate must be repeatedly dried and fired for each additional layer, often for eight or more additional cycles. Additionally, heatsink attachment is generally performed as the last step in the hybrid assembly process, following die bonding, wire bonding, component soldering, and magnetics attachment. Each of these steps is conducted at an elevated temperature, and contributes further to the oxidation and surface affinity degradation of all exposed metallized surfaces. Cleaning and oxide removal techniques intended to address these post-firing surface contamination problems are presented later in this section, along with other issues pertaining to multilayer interconnection substrate fabrication.

3.3.4 Inner Layer Metallization Application

Following the application of the heatsink metallization, the first layer of interconnect metallization is applied to the opposite side of the substrate. In cases where a solderable heatsink backing is not required, the first metal layer is immediately applied to the bare substrates. Like the first backside heatsink layer, the ink formulation for the first metal layer should include glass frit particles to aid adhesion. Furthermore, the previously discussed issues concerning surface defects and oxidation apply equally to the interconnection metallization layers. In addition, several other criteria must be met by these layers.

To begin with, the electrical properties of the interconnection metallization layers are of significant importance, especially the bulk conductivity and resistance per square. The former is generally maximized by selecting a high purity ink formulation, and then firing it at as high a temperature as possible to insure complete sintering of the metallic particles. The maximum firing temperature is limited by the additional stresses imposed on the substrate and the construction of the firing furnace. For multilayer substrates, thermal expansion

coefficient mismatches and increases in interlayer diffusion further limit this temperature. The resistance per square is minimized, for a given bulk conductivity, by applying the maximum possible metallization thickness.

Unfortunately, there are limits to the maximum conductor thickness that can be applied per PDF cycle. These limits are dictated by a number of factors related to the two important criteria of fired conductor quality and interconnection pattern resolution. For a fixed firing temperature profile and ink formulation, the conductivity of the bulk conductor material is determined by the successful removal of the ink polymers. These polymers tend to diffuse more slowly through thicker ink layers due to their reduced concentration gradients. Thicker metallization layers therefore require longer firing times, with slower ramp rates and increased burnout and firing atmosphere flow rates, to facilitate the removal of these compositions. Even with the inclusion of these process adjustments, the maximum print practical print thickness using presently available ink formulations limits the fired thickness of a single layer to about 1 mil; thicker conductors must be built up by using multiple PDF cycles.

A second criterion that must be met by the inner metallization layers is surface adhesion affinity. Unlike the heatsink metallization layers, where surface solderability was a concern, the inner metallization layers will be covered by subsequent dielectric and metallization layers. The surface adhesion characteristics of the metallization are therefore equally important. For this reason, fritless ink formulations are not recommended for inner layer applications.

A third criterion is feature resolution. This may be less of a concern for the first metallization layer, which often serves as a ground plane and therefore has few detailed layout features. However, pattern resolution is crucial to the electrical functionality of the interconnection metallization layers. To a certain extent, the size of the overall hybrid depends on the ability to resolve layout patterns down to the level required by the smallest components in the circuit. Indeed, the resolution of the interconnection medium often dictates the selection of the components themselves by requiring specific package classes which are compatible with the minimum line spacing resolution of the interconnection medium.

For miniature power circuit applications, the interconnection conductors require not only good resolution but high conductivity as well. Unfortunately, the ability to resolve thin lines and spaces diminishes rapidly as the thickness of the ink print, and hence conductivity, is

increased. Thick conductor metallizations must therefore be achieved without decreasing the pattern resolution. This requirement often precludes a single layer application of the metallization ink, and instead several thin, high resolution metallization layers may be applied in succession. These layers are applied using the same screen pattern, gradually building up the thickness of the conductors until the required thickness is achieved. For example, three layers of a single pattern, each 0.5 mils thick, might be printed, dried, and fired sequentially, to achieve an overall fired thickness of 1.5 mils and a line spacing resolution of 12 mils.

In cases where firing thickness is not limited by incomplete burnout of the ink additives, a PDPDF cycle may be used. In this process, a layer of ink is printed and dried, and then another layer is printed and dried, and finally both layers are fired simultaneously. This technique can reduce the number of substrate firings without greatly compromising either the metal conductivity or the pattern resolution, and can sometimes be extended to three or more layers if the firing process is slowed down. However, practical limits are imposed by the additional thickness of the printed layer prior to firing, which typically exceeds 50% for the metal ink formulations. The greater thickness of the unfired layers complicates the printing process because the added height of these layers increases the non-planarity of the substrate surface and reduces the intimacy of the emulsion-to-substrate contact. A recommended compromise is to PDPDF two layers of metallization ink, each with an unfired thickness of 0.9–1.4 mils, for a total fired thickness of 1.0–1.5 mils.

Despite these techniques, the final resolutions (8–10 mils) that are achieved using multiple layer metallizations are substantially less than the resolution of a single layer (4–6 mils). Problems with registration of the screens can account for a portion of this reduction, as tolerances of $\pm$ 1-2 mils are typical from layer to layer. Even when the screen position is not changed between layers, as with a PDPDF type of cycle described previously (where the evaporation of solvents from the ink on the screen between printings is minimal, and screen removal for cleaning between layer applications can therefore be eliminated), the space between lines is reduced by the second print.

In both cases, the reduction is due to the non-planarity of the substrate surface following the application of the first ink layer. During the second printing, the emulsion backing on the screen has difficulty sealing around the edges of the previous ink deposit, and the second ink layer tends to extend beyond the borders of the first layer. Thus, the spacing between

lines decreases with each printing, and the *width* of the conductors is augmented as well as its thickness. This effect is most pronounced on spaces located between lines which are oriented perpendicular to the motion of the print head. In these cases, the squeegee blade actually drags the emulsion along the substrate, smearing the ink across the surface and reducing the inter-line spacing still further. For this reason, the recommended design rule spacing between adjacent lines should be increased when multiple cycles are used to increase the print thickness.

3.3.5 Dielectric Insulation Application

The previously described problems with multiple prints and decreased resolution are also encountered when applying the dielectric insulation layers. Dielectric inks are formulated in much the same way as metallization inks, in that they contain binding agents, printing polymers, and solvents in addition to their base insulating material. The same concerns for complete polymer burnout therefore prevent the application of thick dielectric layers in a single print. In the case of dielectric inks, however, the decision to print multiple layers is not an option which improves the system performance, but a necessity to insure system functionality.

Defects left by clots in the screen mesh during printing or by the burning of dust particles in the ink during firing leave small pinholes in the dielectric surface which are filled by subsequent metallization layers. When these pinholes pass completely through the dielectric, the resultant electrical shorts destroy the functionality of the substrate. Applying multiple layers of dielectric, with a thorough cleaning of the screen between prints, greatly reduces the incidence of pinholes. Most dielectric ink formulations therefore require a minimum of two PDF cycles to insure complete electrical isolation between metallization layers. Other techniques, including double passes with the squeegee during each print cycle (PPDF or dual direction printing), also reduce pinholing but tend to smear the wet ink on the second pass and thereby reduce the print resolution by a significant amount.

A second effect, layer diffusion, also motivates the printing of multiple layers of dielectric insulation. Layer diffusion is the process of metal particle migration along concentration gradients in the thick film layers. These particles diffuse into the adjacent dielectric layers during the high temperature firing process, reducing the effective thickness of the dielectric layers. This diffusion length is typically around 0.2 mils, depending upon the fabrication and

processing details. When the combined diffusion distances of the metal particles from two adjacent metallization layers exceeds the thickness of the interceding dielectric, interlayer metallization shorting occurs. This problem is exacerbated by the repetitive firing cycles required for metallization layer buildup or for the fabrication of substrates with numerous metal layers.

In both instances, the solution to these shorting problems is to increase the total thickness of the dielectric layers. This adds additional fabrication overhead per dielectric layer, and complicates interconnection between metallization layers. Furthermore, it reduces the resolution of vias and other dielectric features. Finally, although it decreases parasitic interconnection capacitance, it increases the more harmful parasitic interconnection inductance and thermal impedance. For these reasons, a minimum dielectric thickness is recommended for low impedance circuit applications such as power supplies.

3.3.6 Via Fill Metallization Application

Electrical connections between metallization layers are made through holes, called vias, patterned in the dielectric. In some processes, the upper metal layer is simply printed over this hole, filling it in and contacting the underlying metal to form an electrical connection. There are a number of disadvantages associated with this type of an approach, however, which limit such techniques to the fabrication of relatively simple interconnection systems. To begin with, the multiple-layer fired dielectric insulation has significant thickness and sharply defined perimeters, making it difficult for screens to follow the sharp surface contours on subsequent printings. A minimum via dimension is therefore required to insure that the screen deposits ink in the bottom of the hole. This, in turn, limits the interconnect density, as the resultant via dimension is relatively large compared to the interconnect resolution capabilities of a given metallization process. Furthermore, a depression remains in the overlying metallization layer, as the same quantity of ink is deposited both in the hole and over the surrounding dielectric.

For multilayer substrates with numerous layers and interconnections between layers, the cumulative effect of filling in vias with successive layers of interconnection metallization is to produce a finished substrate with a highly non-planar surface. Such a surface is unsuitable for die bonding or wire bonding, and also complicates component soldering. Special via inks have been formulated to address these problems. These inks are more fluid during printing,

and exhibit a greater surface tackiness in the wet state, enabling them to flow into and adhere to the underlying metalization layer in the bottom of the dielectric opening. Furthermore, they contain a high percentage of solids, which minimizes ink shrinkage during firing and makes multiple via fill PDF cycles unnecessary. Finally, these ink formulations have thermal expansion coefficients which are matched to the dielectric compositions, reducing stresses at the via sites which can otherwise produce dielectric cracking and eventual electrical failure. Following via fill application, the subsequent metallization is then applied as before, making contact with the surface of the via fill metallization and establishing electrical contact. Interlayer interconnections made using this type of via fill process exhibit a much more uniform surface planarity, permitting die and wire bonding directly over via sites.

3.3.7 Top Layer Metallization Application

Following the application of the final inner layer metallization, the dielectric insulation layers, and the via fill metallizations, the top layer of metallization is added. To achieve the maximum performance potential of hybrid circuit construction, this layer must be both solderable and wire bondable. In addition, it must adhere well to the underlying thick film layers because it will support the weight of the surface components. Finally, it should have good electrical conductivity and high resolution. A layering of different ink formulations is therefore used, as in the case of the backside heatsink metallization. A frit-bonded conductor ink is first applied for maximum adhesion to the underlying metallization and dielectric layers, followed by one or more layers of oxide bonded metallization for optimal surface characteristics.

Issues described in previous discussions on metallization layers are equally applicable to the top metallization layer. Surface oxidation, polymer burnout, planarity, conductor conductivity, and line resolution are all considerations which must be addressed when adjusting the processing parameters for the final metallization application cycles. In most cases, the final firing parameters are the optimal settings for the ink family, and can be used for all of the preceding processing cycles as well. The printing parameters tend to be quite different for each layer because they depend upon the particular layout pattern and the specific ink formulation, as well as on the thickness and surface qualities of the underlying layers.

3.3.8 Glass Encapsulation Application

Following application of the final metallization layer, an optional glass encapsulation layer may be applied over the surface of the multilayer interconnect system. This encapsulation layer serves the dual purpose of a solder mask and a hermetic seal for the interconnect layers. Like the dielectric inks, the glass encapsulant is formulated from glass or ceramic particles mixed with solvents and a polymer printing vehicle. It is processed in a similar manner, and upon firing over either metallization or dielectric materials, forms a tough, hermetic, transparent coating. A PDFF (double fired) cycle is recommended to promote adhesion and to increase surface uniformity.

The presence of a solder mask is valuable in both solder- and epoxy-bonded component assembly systems. In both system types, the combination conductor-adhesive is typically screen printed onto the surface of the top metallization layer. The solder mask creates a physical boundary which assists in confining the adhesives during subsequent component attachment stages. The mask also aids in the placement and alignment of the components themselves, which is especially beneficial because hybrids lack the alignment holes which are present on standard PCB assemblies. Furthermore, the solder mask helps combat the surface tension of solder, which otherwise tends to move small components during vapor phase reflow processing. Finally, the hermeticity of the glass encapsulation protects the underlying metallization layers from corrosion, and helps seal the moisture-absorbent dielectric layers.

3.3.9 Metallization Surface Characteristics

In addition to the formulation of the ink, there are a number of processing factors which directly influence the surface characteristics of the metallization layers. The presence of oxygen in the firing furnace greatly increases the surface corrosion of the metallization layers by contributing to the formation of additional metallic oxides which alter the normal salmon-pink surface tint. Specifically, oxygen in the burnout section reacts with the copper ink particles, forming oxides which are converted to cuprous oxide during the high temperature firing stage. This type of oxidation adds a reddish-purple tint to the copper surface. In contrast, oxidation which occurs after the high temperature firing section remains as cupric oxide, which has a dark grey tint. Firing at too high a temperature causes the leaching of oxide ingredients in the ink, which are added to contribute to adhesion. One such additive,

bismuth oxide, appears as a reddish border surrounding the edges of the metallizations [29].

Bubbles and surface roughness are two other classes of surface defects which commonly occur when fabricating thick films. These defects can be caused by a number of processing errors, in any of the three PDF stages. High speed printing, the use of coarse mesh screens, and unusually thick or dried out inks all necessitate longer settling times after printing but before drying. This settling time permits the ink to flow and removes the imprints left by the screen, one source of surface roughness. Bubbling can be caused by the insufficient drying and incomplete removal of solvent additives in the ink or by the excessive drying and sealing of ink polymers beneath the print surface. The solvents maintain a constant optimal fluidity during the ink printing process and must be completely removed by oven drying before firing, or they will boil violently beneath the ink surface and cause lifting of the ink from the substrate. Excessive drying, however, can trap polymer additives beneath the ink surface. These carbonaceous polymer compounds are mixed with the particles of metal power during formulation to make the printable metallic inks thixotropic and must be removed before sintering the metal.

This second removal process occurs during the burnout stage of the firing process, when the inks reach 325-400^{o}C. Polymers mixed throughout the ink diffuse to the surface, where they are removed by the flow of the furnace atmosphere. This atmosphere is a carefully regulated by a series of valves, ports, baffles, and a venturi, which collectively provide a controlled flow of air or nitrogen to remove the volatilizing ink additives. Typical flow rates for a 5 inch belt furnace running a nitrogen atmosphere at a moderate 10% load are 50–100 lpm. These rates include flows to the end baffles which maintain positive pressure within the furnace and prevent air from entering at the substrate ports. Like excessive solvent removal, insufficient flow of nitrogen in the burn-out section or through the exhaust venturi can retard diffusion of the polymers and cause the formation of bubbles. Finally, excessive print thickness and exceedingly rapid thermal ramp rates can also cause surface bubbling by impeding the complete removal of these polymers before the substrate reaches the firing section of the furnace.

3.3.10 Multilayer Thick Film Issues

In addition to the specific processing details pertaining to the application of the various types of thick film inks, a number of additional issues arise when numerous thick film

layers are stacked to form multilayer interconnection substrates. These issues reflect the increased complexity associated with repeated PDF cycles which sets practical limits on the maximum number of metal and dielectric layers that can be assembled using thick film techniques. Several of these complications, such as the diffusion of metallization layers into adjacent dielectric layers, decreasing surface planarity, and the gradual oxidation of the backside metallization during front side layer processing, have already been addressed in their appropriate sections. Other problems peculiar to multilayer processes are now considered.

Alignment Between Layers

The simplest multilayer issue is the problem of misalignment between layers. A finite alignment error, introduced by the misregistration of screens during the printing stage, reduces the effective line-space resolution of the thick film process by requiring an additional tolerance for registration error. This error increases with the number and thickness of underlying metallization and dielectric layers, because the registration errors tend to be cumulative.

The addition of alignment targets on the first layer helps reduce the accumulation of registration errors by permitting the alignment of all successive layers to the same initial location. However, the thickness of the intervening layers tends to reduce the benefits of such an alignment system as the separation between the first layer alignment pads and the final layer screen increases. A good compromise is to first align each layer with the bottom metallization, and then adjust this alignment to compensate for any errors in the preceeding layer. Whatever the alignment procedure, several iterations of printing and adjustment are required each time a new screen pattern is used. Thus, several substrates are wasted *per layer*, adding a fixed overhead to the cost per layer.

Substrate Warpage

Another effect that becomes progressively worse as the number of thick film layers increases is substrate warpage. This warpage is caused by a mismatch in thermal expansion coefficients (TCEs) between the thick film materials, particularly the dielectrics, and the alumina substrate. Ink formulators make special efforts to match these coefficients, but the final TCE of the films is process dependent. Firing parameters such as the ramp rate in the burnout

section, the peak firing temperature, the final polymer concentration, and the cool down rate all can change the TCE, making exact matching difficult. One way to minimize the effects of this warpage is to process the thick film on oversized substrates, cutting them to final size after the thick film processing is complete. The extra substrate material provides additional support, and helps reduce the warpage that occurs as the thick film solidifies.

Metallization Surface Degradation

In discussing the back side heatsink metallization, it was noted that surface oxidation is a cumulative process that tends to continuously degrade the surface qualities of exposed metallization layers throughout the substrate fabrication and assembly processes. In addition to this oxidation, the surfaces of exposed metallization layers are contaminated by the firing of subsequent metallization and dielectric layers. During these firings, polymers and other printability vehicles are removed from the fresh inks, and deposited on the exposed portions of the underlying layers. As the number of firings grows, and the quantity of burnout material increases, the thickness of this deposition on the initial metallization surfaces becomes significant. Due to the organic nature of this contamination, it is more difficult to remove, and poses a serious obstacle to both soldering and wire bonding.

The simplest way to solve this problem is to limit surface connections to the top metallization layer *only*. In cases where a connection would ordinarily be made to an inner metallization layer, a via should be made to the surface, and an overprint of the top metal layer added. This guarantees that all connections are made to the most recently applied metallization, greatly reducing the effects of cumulative oxidation and burnout deposition. Furthermore, it assures a high degree of surface planarity, simplifying the assembly process during subsequent construction steps. In special cases where it is not practical to make connections exclusively to the most recently applied metallization layer, or when subsequent surface contamination occurs before the assembly process, the metallization surfaces must be cleaned. There are several methods that can be used to accomplish this task, depending upon the nature of the surface, the type of contamination, and the type of connection that is to be made.

The use of a mildly activated flux is appropriate for surfaces like the backside metallization, which are to be soldered. Similarly, the use of solder pastes containing such fluxes is appropriate for die bonding and component soldering onto top layer metalizations. Phys-

ical abrasion, including burnishing, sanding, and abrasive bead blasting can be employed to remove deposits left by burnout products from subsequent fired layers. This method is applicable to metallizations on either side of the substrate. Finally, chemical etching can be used to remove oxides from the surfaces of single layer interconnection substrates, or from the backside metallization of multilayer substrates. In the latter case, care must be taken to insure that no contamination of the semi-porous dielectric insulation occurs. The chemical ions in such etchants are difficult to remove from within the dielectric, and can cause electrical shorts and degradation of the interconnection structure over time. One recommended chemical cleaner is phosphoric acid, which dissolves copper oxides without attacking pure copper conductors (though it still causes dielectric shorting). The copper surfaces are wiped with a weak 5% phosphoric acid solution, then rinsed with de-ionized water, and finally oven dried.

Yield

The added complexity involved in producing multilayer interconnnection substrates tends to reduce yields significantly as the number of layers is increased. There is the previously described fixed overhead associated with the start of each new layer, as the printing and alignment parameters are adjusted. In addition, cumulative registration errors and surface non-planarity tend to reduce the incremental yield per layer as the number of layers increases. Finally, the effects of multiple firing degrade the quality of the initial layers, establishing a practical limit on the total number of layers that can be applied to a single substrate.

3.3.11 Summary of Thick Film Parameters

During the establishment of the previously outlined understanding of copper thick film substrate fabrication, a number of test substrates were generated. Their properties were measured and evaluated, and further iterations were performed. The final result of this experimentation was a thick film process suitable for the construction of a high frequency switching power supply prototype. The specifications for this process are presented in Table 3.3. Multiple table entries correspond to single and double thickness properties for each layer, while single table entries correspond to cumulative double thickness characteristics.

Excellent pattern resolution was achieved for both metallization and dielectric layers

	Inner Metal	Dielectric	Top Metal	units
Line Resolution	5 , 10	7 , 15	5 , 10	mils
Surface Characteristics	Good	...	Excellent	bondability
Substrate Adhesion	5	...	...	lbs
Fired Thickness	0.6 , 1.1	1.0 , 1.9	0.6 , 1.1	mils
Bulk Resistivity	1.04	...	1.00	$\mu\Omega$ - in
Dielectric Breakdown	...	> 300	...	V/mil

Table 3.3: Cu Hybrid Thick Film Parameters

of single thickness, with consistent line resolutions of 5-7 mils. Both inner layer and top layer metallization resolutions were limited by second print smearing, which caused shorts across perpendicularly oriented conductors with spacings of 5 mils, and required extreme processing care even with 10 mil spacings. Parallel and perpendicular spacing of 10 and 15 mils, respectively, are recommended for double thickness processes for which high yields are critical. Vias were resolved to 10x10 and 15x15 mil dimensions for single and double thickness dielectric layers, respectively. Again, 20x20 mil vias would be recommended for increased yields.

The surface characteristics of the metallization layers were subjectively measured, based upon solderability and bondability. Exposed surfaces of the inner layer metallization were solderable with solder pastes bearing mildly activated fluxes, while the top metallization was both solderable and wire bondable. Bonding was done with 1 and 3 mil aluminum wire, using a semi-automatic ultrasonic wedge bonder, with a heated stage temperature of 85^oC, in an air atmosphere. In no case was chemical or abrasive surface preparation necessary.

Substrate adhesion was measured in accordance with industry established test guidelines, using the adhesion test pattern recommended by DuPont Chemicals [30]. This pattern, shown in Fig. 3.2, also contains a 200 square resistivity test pattern used to determine bulk resistivity. In accordance with the test procedure, the patterns were printed, dried, and fired, and specially-formed pull wires were dip soldered to the test sites. The final test substrate, complete with formed wires, is shown in Fig. 3.3.

A constant-speed tensile strength test was performed, and the force-displacement curves were recorded. A representative example of a set of curves for one substrate is shown in Fig. 3.4. The average peak force required to separate the wire from the substrate was 5.1 lbs with a standard deviation of 0.4 lbs, representing a unit-area force of 510 lbs/in^2. Failure

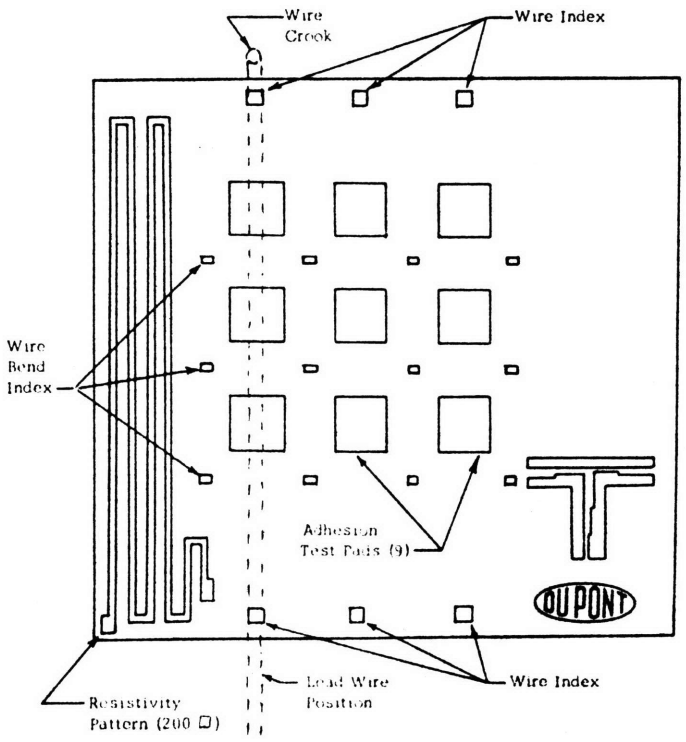


Figure 3.2: DuPont Test Pattern

modes were evenly divided between separation of the solder from the wire and peeling of the metallization from the substrate. These results generally matched the specifications quoted by the thick film ink manufacturers, and indicated satisfactory adhesion between the metallization layers and the substrate.

Substrate samples from each cycle in the assembly process were profiled to determine fired film thicknesses. The thin emulsion and fine screen pitch used for the metallization layers produced high resolution patterns with some reduction in thickness. Dielectric layers were printed using thicker emulsions on a coarser mesh screen, resulting in thicker fired films and eliminating the need for a triple thickness of dielectric between metallization layers. A sample profile, produced on a Sloan Dektak II profilometer, is shown in Fig. 3.5 for a two thickness inner metallization. The greater film thickness at the edges is caused by the emulsion, which raises the screen around the edges of the metallization pattern. The periodic ridges on the surface of the metallization correspond to the screen wire indentations left from the printing process.

The bulk resistivity was determined using the 200 square conductivity test pattern. The resistance of the conductor was determined, and the $R_{\square}$ was calculated. Using the

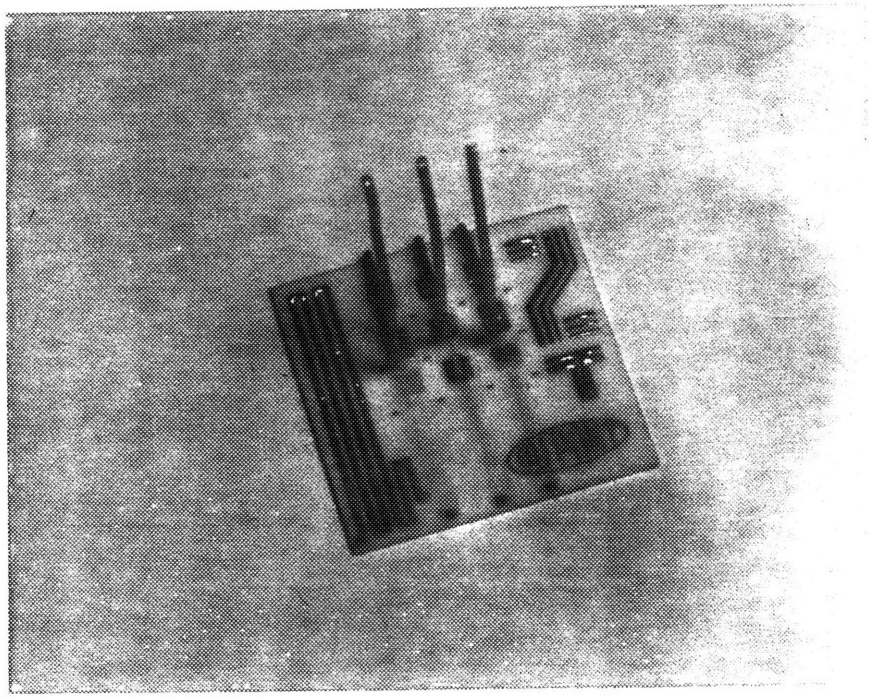


Figure 3.3: Adhesion Test Substrate

previously profiled conductor dimensions, the bulk resistivity was then determined. This resistivity was found to be 1.0 $\mu\Omega$ - in (2.6 $\mu\Omega$ - cm), or 50% greater than the 0.68 $\mu\Omega$ - in (1.724 $\mu\Omega$ - cm) of pure copper. The dielectric breakdown strength was measured and found to exceed the 300 V/mil necessary for the prevention of dielectric shorts.

The resultant magnitudes for the electrical interconnection parasitics are given in Table 3.4. These values correspond to the dimensions and characteristics of the previously described copper-based thick film system and are used throughout the following chapters as reference values.

Parasitic	Magnitude	units
$R_{\square}$	1.0	$m\Omega/\square$
$L_{\square}$	60	$pH/\square$
C_{area}	830	pF/in^2

Table 3.4: Cu Hybrid Interconnection Parasitics

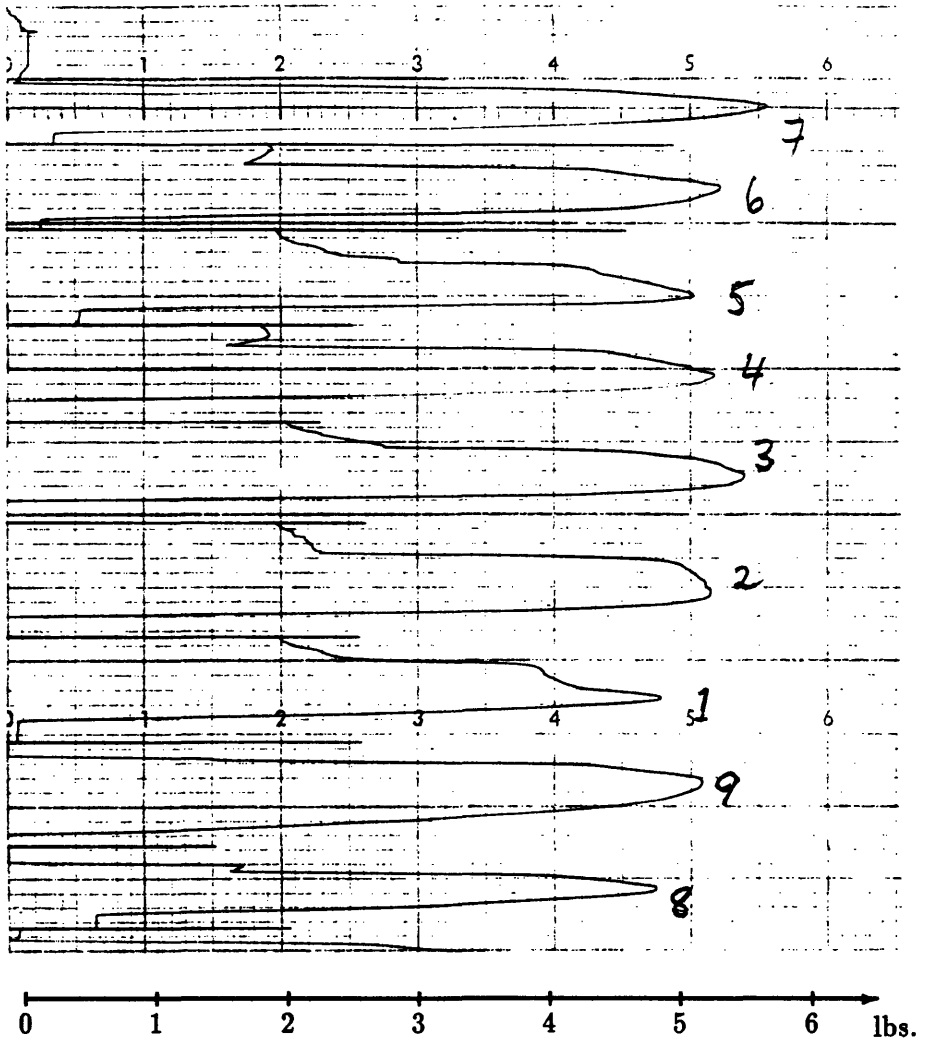


Figure 3.4: Adhesion Test Force Profile

3.4 Thick Film Hybrid Circuit Assembly

Following fabrication of the thick film substrates, components are physically attached and electrically connected to form the finished hybrid circuit. This assembly process typically involves the operations of die bonding, wire bonding, passive component attachment, magnetics assembly, and heatsink attachment. These operations are performed in a specific sequential order which is based upon their thermal processing hierarchy: steps requiring the highest processing temperature are performed first, followed by lower temperature operations. This reduces the probability that subsequent steps will disturb the quality of previously established bonds and connections. The determination of this order is based

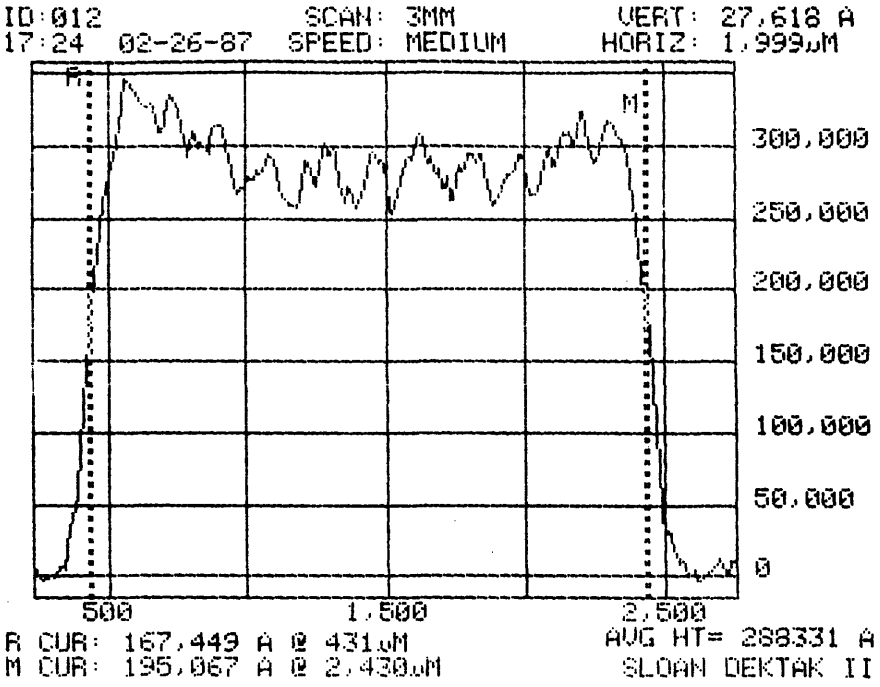


Figure 3.5: Thick Film Ink Profile

upon the selection of a particular attachment method for each operation, which in turn requires a solid understanding of the basic assembly processes. Soldering and adhesive bonding, the two most common attachment procedures, are discussed at the beginning of this section, along with processing details for each approach. The remainder of this section then describes specific steps of the assembly process.

3.4.1 Component Assembly Strategies

In the following paragraphs, two methods for attaching components to the finished thick film substrate are considered. The advantages and disadvantages of each method are described and compared. In particular, the superior electrical and thermal conductivities of solder are weighed against the complications of surface oxidation and process-induced thermal stresses. The effect of the lower conductivities of adhesives are considered both in general and in the context of the previously described POL converter application.

Solder Assembly Issues

Soldering is the accepted standard for component attachment. Solder exhibits good electrical and thermal conductivities, and high mechanical strength. It also requires high temperature processing, however, and is sensitive to surface conditions at the solder joint interface. Typical processing temperatures range from $165°C$ for low temperature solders to over $400°C$ for eutectic die bonding formulations. Table 3.5 shows several of the common alloys arranged in order of their ascending solidus temperatures. Their liquidus temperatures form a second level of ascension, with eutectic compositions being first. For example, the table indicates five solder compositions, each with a solidus temperature of $183°C$, but with liquidus temperatures ranging from $183°C$ for the eutectic composition to $238°C$ for a softer lead-tin alloy.

Solidus $°C$	Liquidus $°C$	Composition %	Trade Name	Applications and Characteristics
145	eut	50Sn,33Pb,17Cd	XM-TLC	low temp solder
178	270	Sn,Pb,Ag	XAL-45D	aluminum adhesion, organic flux
179	eut	62Sn,36Pb,2Ag	SN62	ll, db (Ag or Au to Ag)
180	209	50Pb,50In		soft, fr, db (Ag or Au backed)
183	eut	63Sn,37Pb	SN63	std electronics grade, soft
183	190	60Sn,40Pb	SN60	std general grade
183	216	50Sn,50Pb		soft
183	222	95Sn,5Pb		high strength solder
183	238	40Sn,60Pb		soft, viscous flow
187	240	35Sn,63.5Pb,1.5Sb		hard
215	eut	55In,45Pb		soft, fr, db (Ag or Au backed)
221	eut	96.5Sn,3.5Ag	SN96	ll, strong, non-toxic, sub-to-pkg
268	299	88Pb,10Sn,2Ag	SN10	soft, ll
268	302	90Pb,10Sn	XM-10/90	high temp, ceramic chips
280	eut	80Au,20Sn		hard braze, db (Au to Au)
280	eut	92.5Pb,5Sn,2.5Ag		db (Ni/Ag to Au, Cu)
296	301	93.5Pb,5Sn,1.5Ag	XM-HMP	soft, high melting point
307	eut	92.5Pb,5In,2.5Ag		soft, ht, db (Ni/Ag to Au)
309	eut	97.5Pb,1Sn,1.5Ag		ll, db (Ni/Au, Ni/Ag to Cu, Au)
356	eut	88Au,12Ge		eutectic braze, db (Si to Au)
370	940	98Au,2Ag		eutectic braze, db (Si to Au)
key: db=die bonding; fr=fatigue resistant; ht=high surface tension; ll=low leaching				

Table 3.5: Solder Characteristics

In addition to establishing solidus and liquidus temperatures, the composition of the solder greatly affects its physical properties in both the molten and solidified states. For example, solders with a significant lead (Pb) content are characterized by relatively high melting temperatures and low mechanical strength. In contrast, high tin (Sn) content formulations tend to have lower melting temperatures, superior wetting characteristics, and greater shear strength, but can sometimes exhibit brittleness or joint fatigue. Alloys containing silver (Ag) or gold (Au) dopants are typically used in low leach solder applications to prevent the migration of plating metallization materials through the solder interface. Finally, gold braze solders doped with silicon (Si) or germanium (Ge) are used to solder bare semiconductor dice to gold-metallized substrates by forming a high temperature brazed joint.

Included in the table is a brief description of the characteristics and common applications for each formulation. Besides the liquidus and solidus temperatures, the main criteria considered when selecting a solder composition are wetting and leaching characteristics and shear strength. Faced with the large number of available formulations, the usual method for selecting solders is to first determine the order of the assembly process to be used. This determination is based upon such criteria as component temperature sensitivity, component profile, and bond reworkability.

For example, bare power semiconductor dice can withstand significantly higher soldering temperatures than either plastic header interconnect pins, packaged controller ICs, or the insulating materials used in most magnetic windings. In addition, the latter components all tend to have relatively high physical profiles which restrict wire bonding access to the bare dice and substrate surface. This restriction generally forces wire bonding (and hence die bonding) to precede transformer installation. Finally, it is difficult to rework wire bonds on semiconductors after the defective components have been desoldered, because this removal process is performed manually at a high temperature and can cause significant surface oxidation in the wire bond regions. The selection of copper thick film as an interconnect metallization generally precludes reworking of the wire bonds, although the die bonds themselves are reworkable because the bond die bond sites are tinned by the first bonding cycle. For these reasons, it is advantageous to assemble the larger and more temperature sensitive components *following* die and wire bonding, using an attachment method with lower processing temperatures and improved bond reworkability.

Following the establishment of a temperature hierarchy, solder compositions are selected from within each general temperature range based upon a set of desirable characteristics for the specific application. For instance, a soft, fatigue resistant solder compatible with the appropriate component metallizations would be required for die bonding applications, while a solder with good wetting characteristics and a resistance to leaching would be desirable for soldering components with Pd-Ag terminations. Eutectic compositions are favored for most multi-temperature assembly operations, due to their inherently narrow thermal transition range, which reduces the heating margin above the solidus temperature beyond which the solder must be heated in order to guarantee complete liquidity. This in turn permits lower maximum processing temperatures for a given number of thermal tiers. Such a reduction in temperature is valuable, because high temperature soldering tends to aggravate surface oxidation problems on copper thick film metallizations, complicate subsequent soldering and assembly steps, and necessitate the use of fluxes or abrasive techniques to prepare surfaces for bonding.

Adhesive Assembly Issues

Adhesive assembly technology is developing as an alternative to standard solder assembly techniques. Most adhesives benefit from elevated processing temperatures, which provide additional energy for the chemical reactions which transform the adhesives from viscous fluids to solids. These processing temperatures are significantly lower compared to the liquidus of most solders, and can range from $50°C$ for certain thermally conductive adhesives commonly used in heatsink attachment applications, to about $200°C$ for metal-filled conductive epoxies. The majority of conductive epoxies are cured at $150°C$, where setting speed and bond uniformity are enhanced without compromising thermal stress characteristics. Once cured, the bonds can withstand significantly higher temperatures without performance degradation. Curing times can range from 10 minutes for quick-setting epoxies to over an hour for oven-cured varieties.

Once cured, the chemical changes are irreversable, making assemblies constructed using adhesives more difficult to rework than soldered constructions. While it is possible to chip off the epoxy or to apply a second layer over the first, such techniques generally compromise the integrity of the final bond interface. For this reason, the usefulness of adhesive bonding is generally limited to applications in which rework capability is not a priority. However,

it was already noted that the reworking of semiconductor dice is not presently viable with a solder-assembled copper thick film ink system (due to oxidation of the wire bond sites), so non-reworkability should not be viewed as a disadvantage of adhesives for die bonding applications in copper thick film hybrid assemblies.

A second issue that must be considered when comparing solder with conductive adhesives is the relatively poor electrical conductivity of the adhesives. Typical conductive epoxies have sheet resistances $R_\square$ of around 25 $m\Omega/\square$ at 1 mil, giving a bulk resistivity of 65$\mu\Omega$ - cm, or a factor of 25 higher than the copper thick film conductors. However, the large area and thin depth of the adhesive layer, sandwiched between the component terminal and the substrate interconnection metallizations, produces a net resistor of only a fraction of a square in length. The actual magnitude of such a resistance lies in the 10–100 $\mu\Omega$ range, making it insignificant compared to other parasitic resistances in the circuit.

The third and most important issue concerning the use of adhesives for component attachment is their *thermal* conductivity. A typical solder formulation has thermal conductivities in the range of 0.2–0.5 $W/K\,cm$, comparable to certain silver-filled fired-glass die bonding dielectrics (0.7–0.8 $W/K\,cm$). These are, in turn, up to two orders of magnitude greater than silver-filled conductive epoxies (0.017 $W/K\,cm$) or ceramic-filled insulating epoxies (0.008 $W/K\,cm$). Even a thin layer of such low thermal conductivity materials can create a dominant thermal impedance between components and the surrounding environment in well designed systems where the other thermal impedances are small. For example, a 1 mil layer of conductive epoxy under a (200 mil)^2 die would produce a 0.58 $^\circ C/W$ temperature rise.

The thermal impedances associated with such component adhesives have therefore been considered unacceptable for high power applications, including power conversion systems, which traditionally require minimal thermal impedance construction. However, the higher efficiency requirements that must be satisfied for the successful realization of POL converters in distributed power systems dictate the implementation of circuit designs that dissipate minimal power, particularly in the semiconductor components. As a result, most power semiconductors are selected to be over-rated and oversized, so that the power dissipation is small and the power dissipation *density* is even smaller. The heat flux concentration through the thermal impedance of the adhesive bond is thus reduced, and the associated temperature rise is minimal. In such applications, epoxy-based construction systems can offer an

assembly alternative using lower processing temperatures, with the associated benefits of reductions in surface oxidation and in thermal stresses, without sacrificing the thermal performance advantages of hybrid construction. A case study of such a design is presented in the fourth section of Chapter 5, where the construction of a POL converter using adhesive die bonding is described.

Processing of Solders and Adhesives

The application procedures for solders and adhesives are similar in many respects. Both are available in screen printable formulations which are compatible with thick film printing processes. This permits the uniform application of a controlled thickness across the entire contact interface area. Conductive epoxies generally contain 70–80% solids, suspended in an epoxy resin which doubles as a printing vehicle, while solder cremes require additional solvents and a dedicated printing agent to carry the metal alloy particles. These particles are relatively large compared to most other thick film ink ingredients, so printable solder cremes are specified in terms of the range of the grain size. For instance, a $-200/+325$ rating means that all the (dry) particles fit through a 200 mesh screen, but none will pass through a 325 mesh screen. Printing screens should have mesh openings one or two sizes larger than the biggest grain size, making 80 or 125 t.p.i. screen pitches appropriate in this example. Solders cremes are also available with pre-mixed flux additives to aid in surface preparation, while one major advantage of adhesive bonds it that they need no such surface preparation.

As an alternative to screen printing, both epoxies and solder cremes can be deposited manually or mechanically using a syringe-type applicator. This technique enables precise control over the volume of solder or adhesive that is applied to the connection, although the spreading distribution is less well controlled compared to screen printing. An advantage of syringe application, however, is that more than one cycle of application, component placement, and bonding can be performed, whereas with screen printing, components from the first cycle prevent further printing iterations.

Special techniques have been developed for the soldering and adhesive bonding of bare semiconductor dice. For example, solders are often applied in solid form (rather than as cremes), using preforms cut from pressed solder sheets. These solder preforms, typically 1 mil thick, are custom sized to fit the individual dice outlines and then sandwiched between

the die and the bond site prior to reflow heating. More recently, adhesive epoxies have also become available in sheet form, ranging in thickness from 1–5 mils. These sheets are typically applied to the backs of semiconductors during the final stages of the wafer fabrication process, prior to dicing. Following dicing, the individual components are applied to the die bond site, and the epoxy is cured [32].

Following the application of the solder or adhesive, by whatever method, components are placed on the bond sites. With adhesive pastes and solder cremes, the components are worked into the wet bond site by mechanical scrubbing. This motion, combined with a moderate pressure, helps insure complete wetting by removing any trapped air from between the component and the substrate metallization. The bonds are then set, both mechanically and electrically, by heating. In the case of solder, this requires melting and reflowing, while in the case of adhesives, it requires thermosetting. When the solder is applied in creme form, a preliminary drying step is also necessary to prevent the rapid volatilization of the solvents upon heating which can disturb the placement of components. As discussed previously, the use of a glass hermetic sealant helps confine the adhesive or solder during reflow and further restricts the movement of components.

Adhesive thermosetting is normally performed in a convection or infrared oven. As described earlier, typical processing parameters are $150°C$ and 30 minutes. Care must be taken to control thermal ramp rates, especially during the cool-down phase, to minimize thermal expansion stresses. Despite the extended processing at elevated temperatures required for thermosetting, the resultant surface oxidation of exposed copper metallization surfaces is minimal because the curing temperatures are relatively low. However, oxygen diffusion through the adhesives to the joint interface metallizations can cause reactions with ionic impurities in the adhesives, causing degradation of the joint properties over time.

Even more than with adhesive thermosetting, the high processing temperatures required for solder reflow can aggravate surface oxidation problems. Both soldering and adhesive curing can therefore benefit from processing in a low-oxygen environment, provided by nitrogen or some other inert gas. In adhesive processing, the gas is used to flood the oven during curing to reduce oxygen concentrations. For soldering processes, a baffled belt oven is frequently used which is similar in construction to the nitrogen firing furnace but has a lower temperature profile. They are not interchangeable, however, and a single firing furnace should *not* be used for both substrate fabrication and soldering. Deposits of

waste flux from the solder can contaminate the furnace and disrupt subsequent thick film fabrication efforts. The introduction of hydrogen-enriched nitrogen (forming gas) or some other reducing atmosphere into the oven can further limit surface oxidation and actually enhance the surface wetting performance of a solder. This can result in improved yield and reliability for soldered connections, especially die bonds.

A second method of processing solder connections incorporates vapor phase reflow techniques. Vapor phase reflow provides a highly controlled temperature bath by utilizing a two-phase thermal transfer medium. An inert liquid, with a vapor temperature 15-30^{o}C higher than the melting point of the selected solder formulation, is boiled in a confined enclosure. An external cooling coil is used to condense this vapor, maintaining a layer of suspended vapor confined between the boiling liquid and the cold coil. Hybrid assemblies with solder preforms or printed solder cremes are submerged in this vapor, which condenses upon contact, giving up the heat energy associated with the transition between liquid and vapor phases. The hybrid is heated to the liquid-vapor transition temperature, and the solder is reflowed in an oxygen-free atmosphere. Careful control of the hybrid's movement through the vapor system is required because the rapid transitions between temperature zones within the vapor enclosure can induce physical stresses on the hybrid assembly due to TCE mismatches. In general, vapor phase systems provide tightly controlled thermal baths with oxygen-free atmospheres, making them ideal for processing complex copper hybrid assemblies utilizing several solders with closely spaced melting temperatures.

3.4.2 Die Bonding

Due to the high temperature stability of semiconductor components and the need for unhindered wire bonding machine accessibility, semiconductor dice are typically the first components to be assembled onto the freshly fabricated thick film substrate. The relatively low yield of this process compared to most other assembly processes adds further incentive for early die bonding. Highest on the temperature hierarchy are solders used for the eutectic brazing of bare silicon dice. Silicon brazes are generally performed with a high gold-content solder, doped with silicon or germanium. The solder is typically applied to the substrate as a preform, as opposed to a solder creme, with 1 mil thick sheets of the solder cut 10 mils per dimension smaller than the outline of the die. The solder is then reflowed at a temperature exceeding its solidus, but well beneath its high liquidus. Molecules of silicon diffuse into

the gold, increasing the impurity level until the eutectic concentration is exceeded. This concentration is approximately 31%, and corresponds to a eutectic temperature of $370°C$ [31]. Because the eutectic temperature is higher than the original solidus, the gold solder solidifies, and the bond is formed.

Mechanical die bonding machines have been developed to simplify this die bonding procedure. These machines have individual vacuum collets to hold the dice as they are bonded. The hybrid is placed on a stage heater to provide a base temperature elevation in the range of $200–300°C$. The die bond site is selectively heated using forced air, infrared, or electrode heating, until the preform melts. The die is then mechanically scrubbed into the die site by agitation of the collet. This procedure has the advantages of removing any gasses trapped between the dice and the substrate, of distributing the solder evenly across the entire dice surface, and of greatly increasing the speed of silicon diffusion and subsequent bond formation. The end result is a superior, voidless die bond with reduced high temperature dwell time [33].

Despite the advantages of the die bonder, the high temperatures and tight processing tolerances required for successful eutectic brazing make it an impractical approach for many applications which do not require the high bond temperatures of a eutectic gold braze. A simple alternative exists in those cases where the dice are available with solderable backside metallizations. This is often the case for power semiconductors where the silicon wafer substrate constitutes a main electrical termination requiring good ohmic contact. Dice with such metallizations are solderable with standard solder formulations having lower solidus and liquidus temperatures compared to gold braze solders.

The backside metallizations are typically applied as a sandwich of several layers which are sputtered or plated as a final wafer processing step before dicing. The metal combinations of Cr-Ni-Au and Cr-Ni-Ag are most common, whereas single layer Au metallizations are typically applied for eutectic brazing applications. The inner chromium layer forms the ohmic contact with the silicon, while the nickel provides a solderable barrier and the gold or silver outer coating reduces surface oxidation and improves solder wetting.

The previously described die bonding machines are also suitable for the lower temperature die bonding of metal-backed dice, although hand application is possible with the lower temperature solders. Vapor phase reflow techniques are also used, though the bond quality is difficult to insure and solder voids can occur. The slightly better wetting characteristics

of solder cremes make them a better choice over solder preforms for reflow processes with which mechanical die scrubbing is not possible. Pretinning both the dice and the die bond sites before reflowing them together can reduce bonding voids significantly by permitting inspection of the wetted surfaces prior to assembly. Belt oven reflow in a reducing hydrogen atmosphere can also improve the wetting of the bond surfaces and reduce voids. This is especially important for copper thick film conductors which exhibit increased surface oxidation compared to air-fired precious-metal-alloy thick films.

In addition to soldering, adhesive die bonding exists as an important option for many applications. As discussed previously, the major advantage of such an approach lies in the reduced temperatures required for adhesive thermosetting compared to die bonding. Both screen printed epoxies and adhesive preforms are compatible with the die bonding process. Adhesive films can also be applied at the wafer level, prior to dicing, as an adhesive backing for the entire wafer which aids in dice processing. In cases where the passive components are to be assembled with adhesive, the further advantage of simultaneous processing enables the screen printing of adhesives for both active and passive components in a single step. In other assembly processes, where passive components are to be soldered, the surface quality of the thick film metallizations are not compromised by any previous high temperature die bonding processes. This is again beneficial in copper thick film applications, where high temperature brazing can cause serious surface oxidation. The previously mentioned inferior thermal conductivity of adhesives limits their use to low heat flux density applications. An example of an analysis comparing solder and adhesive die bonding is given in the fourth section of Chapter 5, during the description of the construction of a prototype converter.

3.4.3 Wire Bonding

Following completion of the die bonding process, wire bonding between the dice and the substrate is performed. Several different wire bonding techniques exist which use either gold or aluminum bonding wire, with thermocompression, thermosonic, and ultrasonic bonding being most common. The distinction is based upon the method in which the bond energy is supplied to the weld joint. With thermocompression bonding, a heated stage provides the majority of this energy thermally, through the bond target material. Further energy comes from compression of the bond wire, which deforms upon contact with the bond site and releases additional thermal energy. This energy causes intermetallic bonding between

the wire and the target surface, forming an electrically conductive mechanical weld. Thermocompression bonding is generally limited to applications involving gold wire, and gold or aluminum targets, due to the low bonding energy of the process.

The thermosonic and ultrasonic bonding processes differ from thermocompression bonding in that the predominant source of bonding energy is provided by a mechanical transducer. This transducer physically scrubs the wire across the bond site, imparting energy to the weld. The excitation frequency is higher for ultrasonic than for thermosonic bonding, which requires additional thermal energy in the form of substrate heating. These processes are compatable with both gold and aluminum wires and with a variety of target metallizations.

A further distinction can be drawn between ball bonding and wedge bonding. With ball bonding, the wire is fed vertically through a bonding capillary which holds it during a process called electronic flame-off (EFO). During this process, the wire tip is melted by heat generated by a spark from a high voltage discharge. Following EFO, the surface tension of the molten metal causes the formation of a ball on the tip of the wire. This ball is compressed onto the bond site by the bonding capillary, and welded onto the surface using thermosonic energy, to form an omni-directional first bond. This process is shown schematically in Fig. 3.6 with a typical bonding capillary [27]. The wire is then drawn through the capillary as the capillary is positioned over the second bond site. The bonder head descends to the bond site surface, compresses the wire and energizes the sonic welding head, and completes the second bond.

With wedge bonding, the wire is fed underneath a compressing anvil, or wedge, from the side rather than vertically down through the center. This wedge compresses the wire onto the bond site in a manner similar to that used for the second bond in a ball bonding system. This bonding format is shown in Fig. 3.7 [27]. Because the wire is fed from the side, no ball is necessary to prevent the slippage of the wire back up the wedge hole, which in turn reduces the bond pad area required for the first bond. However, the sideways orientation of the wire under the wedge restricts the direction in which the wire may be directed en route to the second bond, making the first wedge bond unidirectional. Wedge bonding thus requires significant manipulation of the substrate to achieve alignment of the bond sites prior to each bond cycle. This increased alignment is traded off against bonding pad area, which for wedge bonds is only a third the size required to accommodate the large diameter

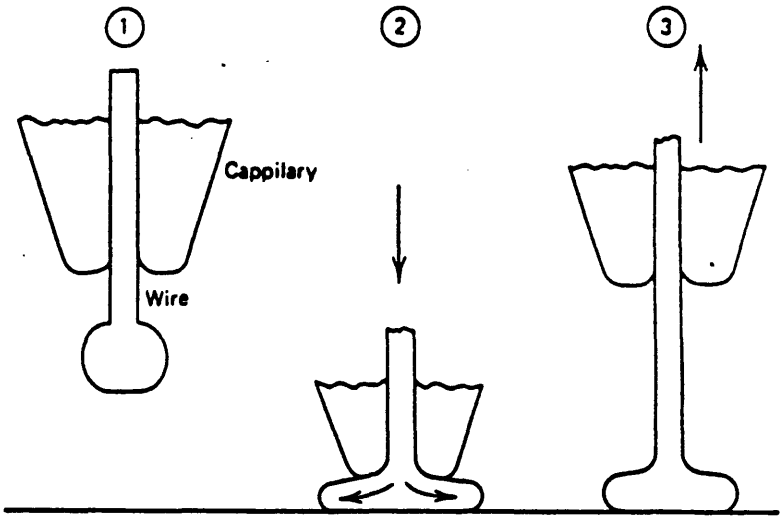


Figure 3.6: Ball Bonding Sequence

and spread of the ball bond. An additional consideration is that aluminum wire is not compatible with ball bonders, because aluminum tends to oxidize (burn) during EFO and fails to produce a bondable ball.

Due to the heavy gauge wire necessary for the current capacity required by power circuits, aluminum is generally selected as the more cost effective material for such applications. Wedge bonders, predominantly ultrasonic, are therefore used to connect most power semiconductors. The maximum current capacity of a conductor is a function of its length L, diameter D, and the temperature $T_{ambient}$ of its surroundings

$$I_{fuse} = \sqrt{\frac{K}{2\rho}} \frac{\pi D^2}{L} \sqrt{T_{melt} - T_{ambient}} \tag{3.8}$$

where the conductor resistivity ρ, thermal conductivity K, and fusing temperature T_{melt} are fixed constants of the material. More conservative estimates of current capacities for 150 mil long gold and aluminum wire bonds, based upon a $25°C$ rise, are computed in Table 3.6 for a variety of common wire diameters. Although these ratings indicate that aluminum wire has only 70% of the current capacity of gold wire, the cost savings associated with the use of aluminum makes larger wires more economical whenever additional bonding pad area is available.

A second issue associated with bonding wire diameter is inductance. As discussed in

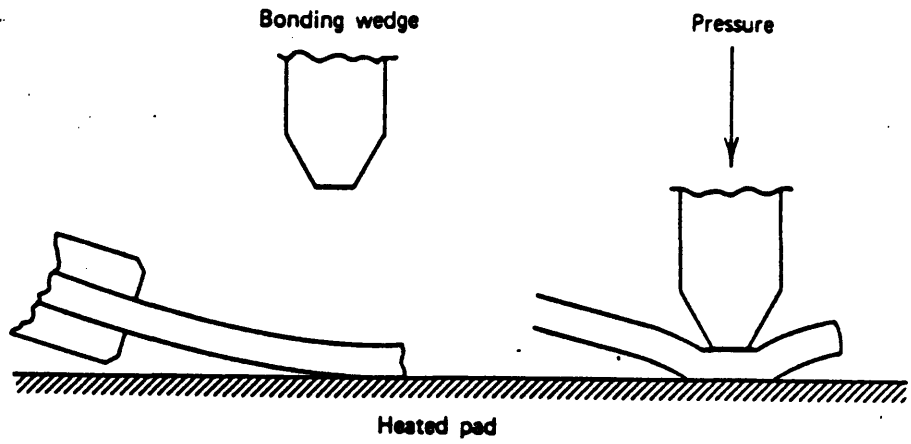


Figure 3.7: Wedge Bonding

Wire Diameter mils	Gold Wire milliamps	Aluminum Wire milliamps
0.5	55	35
0.7	110	75
1.0	220	150
1.5	500	350
2.0	880	600
3.0	2000	1350
4.0	3500	2400
5.0	5500	3750

Table 3.6: Wire Bond Current Capacities

Chapter 2, the parasitic inductances associated with the interconnections between components has proven to be a major limitation in the maximum achievable operating frequencies for power conversion circuits. The elimination of component packages and the adoption of a thick film hybrid interconnection system can reduce the magnitude of these parasitics to the point where the wire bond inductance between a component and the interconnection substrate becomes the dominant impedance. The reduction of this inductance therefore represents the final minimization of interconnection inductances. As shown in Fig. 3.8, the inductance of a single wire bond decreases with wire diameter, offering further incentive for the selection of larger bond wires. Additional reductions can be achieved by utilizing ribbon

conductors rather than circular wire. However, the additional complexity associated with such a bonding system, and the unsuitability of most commercial semiconductor bonding pads for ribbon bonding, makes such an alternative impractical in most situations.

A simple approximation to a ribbon bond, accomplished by paralleling several wire bonds in a horizontal planar orientation, can provide significant reduction in parasitic inductances compared to a single conductor. Again, the low cost of aluminum wire makes such an approach more economical. In addition to reduced inductance and greater current capacity, sheet-paralleled multiple wire bonding creates interconnections with back-up redundancy for increased wire bond reliability.

A further advantage of aluminum wire is its desensitivity to surface contamination, an important quality when bonding to copper thick film metallizations. Copper thick film inks tend to form a thin surface glaze, especially when fired over layers of dielectric (as opposed to directly on the alumina substrate). This glaze can range from less than 2 nm for fritless metallization inks fired over alumina to more than 10 nm for fritted inks over a dielectric insulation layer [26]. The greater hardness of aluminum wire compared to gold enables it to crack through this barrier to form a bond with the underlying copper metal.

3.4.4 Component Attachment

Like die bonding, component attachment can be performed using either solder or an adhesive. In cases where a conductive epoxy has been used during the die bonding process it is often convenient to simultaneously apply epoxy for attachment of the components, as mentioned during the previous discussion on die bonding. This approach assumes that the component dimensions and/or circuit layout permit wire bonding of the dice with the passive components in place. The elimination of a component soldering process stage following adhesive die bonding can greatly reduce the stress applied to the die bond interface. Furthermore, the high temperatures required for component soldering can sometimes produce outgassing in the die bonding adhesive, a potential cause of bonding voids which can cause bond failure and thermally induced component failure. Soldering of components is therefore not recommended following adhesive die bonding.

When solder is used to apply the dice, and the components are to be soldered as well, the solder must be applied as a preform or by using the syringe method. As with solder die bonding, the components are placed on top of the solder, trapped air is worked out

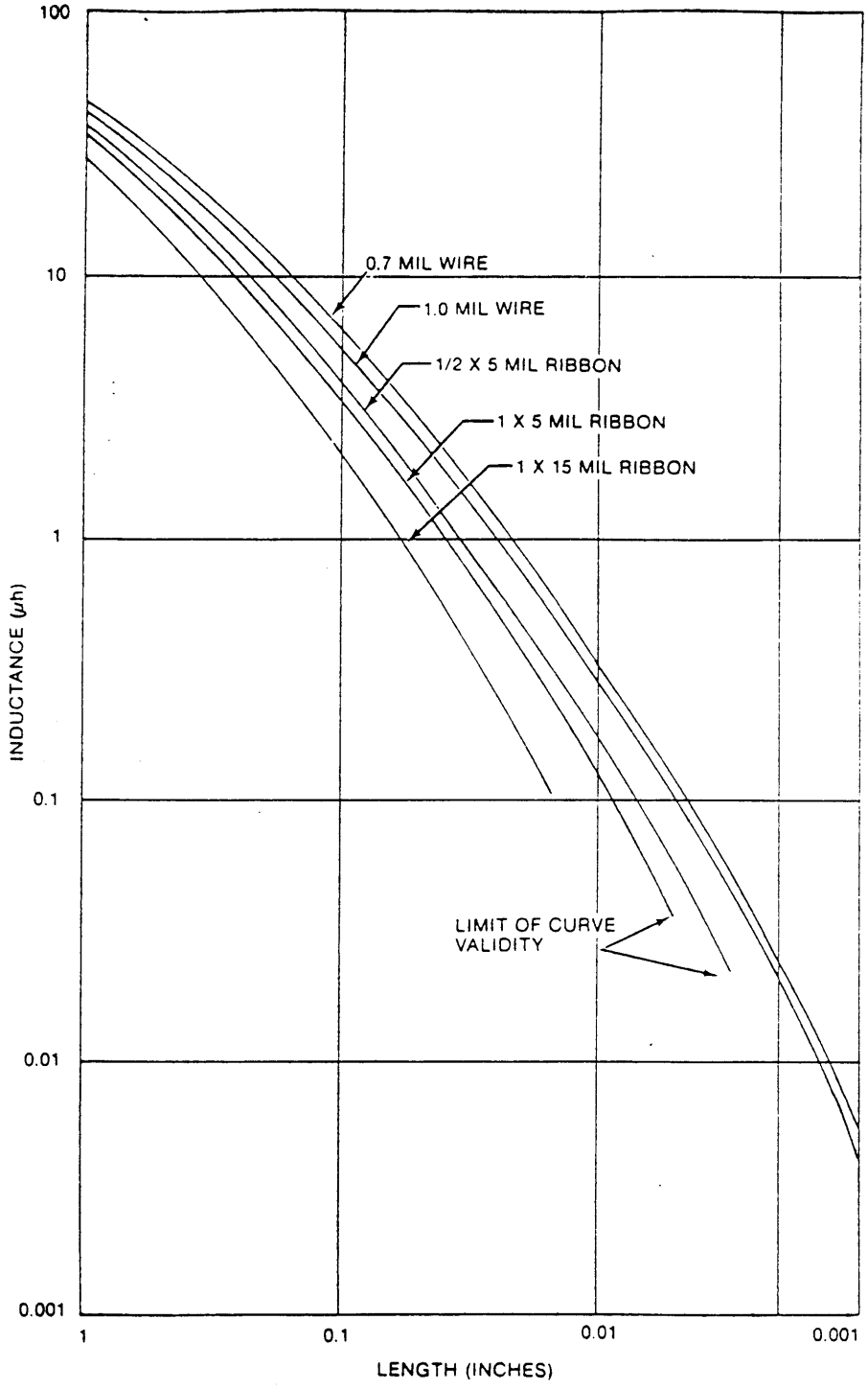


Figure 3.8: Wire Bond Inductances

by mechanical scrubbing, and (in the case of solder cremes) the solvents are dried out. The solder is the reflowed using the previously described vapor phase reflow or belt oven techniques. A simple hot plate and soldering iron can sometimes be used to manually retouch any incomplete solder joints, to replace defective passive components, or to reflow the component solder connections in cases where oxidation is no longer a concern (once wire bonding has been completed).

3.4.5 Transformer Attachment

The magnetic elements are the final electrical components to be assembled onto the hybrid circuit. In most cases, this assembly process involves the two distinct operations of electrical connection and mechanical/thermal attachment, because the wires or tabs used to make electrical connections between the hybrid substrate interconnect system and the internal windings of the magnetics cannot support the relatively large mass of the magnetic core material. A mechanical attachment system relying exclusively upon these electrical connections for the support of the magnetic cores would cause physical stresses which could result in premature failure of these combined electrical/mechanical connections. In addition, both copper (conduction) and core (hysteresis) losses in power circuit magnetics can be significant, especially when operating in the 5–10 MHz range, and the thin electrical conductors do not provide a sufficient thermal path to remove this dissipated heat energy. A separate mechanical/thermal contact between the core and the hybrid substrate is therefore provided to supplement the electrical connection.

A number of techniques exist for creating a mechanical attachment with high thermal conductivity. In this section, it is assumed that the common two-piece "pot-core" construction is used for the magnetics structures (further discussion on magnetic structures and core and winding configurations is presented in Chapter 4). Commonly used approaches for mounting lower frequency transformers (20kHz to 1MHz) include spring steel clips, which fit around the core pieces and clamp them down to the substrate, and bolts, which pass through the core center posts and into the substrate. A thin layer of thermal joint compound (typically an electrically insulating epoxy formulation) is sometimes added at the core/substrate interface to lower thermal impedances and thereby improve heat transfer. The clip and bolt methods have the advantage of maintaining intimate contact between the core halves, insuring reliable magnetic circuits with a constant gap length. These methods

are less compatible with hybrid construction than with PWB construction, however, as it is more difficult to create the slots or holes necessary to accommodate these fixtures in the hybrid substrate ceramics. Furthermore, the losses in these metallic attachments induced by the stray magnetic fields surrounding the core materials can become significant as the conversion frequency and flux densities increase.

Adhesives are therefore commonly used to attach high frequency, high power magnetics in hybrid circuit construction applications. In contrast to the epoxies used for component attachment purposes, the adhesives used to establish the mechanical and thermal connection of the magnetic cores should be electrically insulating. This helps prevent the inducement of circulating currents in the adhesive, which can cause power dissipation resulting in localized heating and reduced conversion efficiency. These adhesives are typically hand applied and uniformly distributed across the contact areas of both surfaces prior to assembly. This procedure, combined with mechanical scrubbing of the cores into the adhesive, helps reduce voids in the interface which can weaken the mechanical strength and increase the thermal impedance of the joint. Adhesives may also be used to join the various sections of partitioned core structures, to assure a fixed and uniform gap. The adhesives are then cured in accordance with standard procedures, typically by oven baking at 150°C for 30 minutes. Quick-setting, thermally conductive epoxies which harden at room temperature can also be used, reducing the stress imposed upon the magnetics and the substrate due to mismatches in TCE's.

Following mechanical assembly and attachment of the core structures, the electrical connections are made to the substrate. When a conductive adhesive is used for this purpose, it can often be cured simultaneously with the core attachment adhesive. When a solder is used, the substrate must first be heated to a moderate temperature, to facilitate soldering to the thermally conductive substrate material. Otherwise, the localized heating provided by the soldering implement is generally insufficient to insure a satisfactory solder connection, and cold solder joints can result. The substrate stage is typically 20–30°C below the lowest solder solidus used on the hybrid to insure that no reflowing occurs while the magnetics are being electrically connected.

3.4.6 Heatsink Attachment

The attachment of the heatsink to the back side of the ceramic substrate constitutes the final step in the construction of the hybrid circuit following assembly of the last electrical components. In cases where a backside thick film metallization layer has been provided to facilitate soldering of the heatsink, this attachment can follow immediately upon completion of the electrical attachment of the magnetics, prior to cool-down of the hybrid assembly. A solder must be selected which has good wetting properties to prevent voids at the heatsink-substrate interface, a relatively low melting point, and a *low* mechanical shear strength. The latter characteristics help reduce stresses on the hybrid assembly while preventing the reflow of previously soldered joints and connections.

In cases where thermal impedances are less critical and no backside metallization is provided, adhesives can be used to secure the heatsink to the hybrid circuit. In addition to reducing the complexity of the substrate fabrication process by eliminating several thick film metallization PDF cycles, the use of an adhesive for attachment of the heatsink can greatly reduce the stresses introduced by TCE mismatches between the ceramic substrate and the metal heatsink. These mismatches can cause visible deformation of the hybrid and can contribute to premature failure of the various electrical, mechanical, and thermal connections on the front side of the hybrid circuit. Adhesives tend to minimize this effect, due to their inherently lower curing temperature compared to the liquidus of most solders. One disadvantage of adhesive heatsink attachment is the permanence of adhesive bonds, which generally precludes heatsink removal for reworking or non-destructive void inspection.

3.5 Manufacturing Issues

Following completion of the various assembly stages just described, the finished hybrid circuit is ready for testing, burn-in, and operation. These processes introduce a number of additional manufacturing issues which become important when mass production and assembly automation are considered. Furthermore, the trade-offs involved in the selection of various assembly techniques and the interaction between various assembly processes must be weighed when an assembly procedure is to be devised for a new product, or when improvements or optimizations are to be made. Such considerations are the subject of this final section on hybrid circuit construction.

3.5.1 Construction Labor

One simple issue that must be considered is the quantity and types of labor that are required by the previously described assembly process. For example, the fabrication of thick film substrates is a labor-intensive process which requires tight quality control and provides little margin for error. Hybrid circuit designs which call for a large number of metallization layers or for additional complexity (resolution) in the fabrication process, in order to improve circuit performance or to achieve greater power density, generally require significantly greater hand labor, both in terms of quality and quantity, which tends to increase the cost of the product. In contrast, the placement and connection of passive components onto the fabricated hybrid substrate can be highly automated, with the processing of numerous components occurring simultaneously. Adding additional passive components to a design therefore exhibits less impact on the overall construction overhead. Similar trade-offs between circuit performance and construction labor can be found in the choices between using unpackaged components, with their associated handling restrictions and wire bonding requirements, and using packaged versions of the same components, with their additional size, thermal impedance, and electrical parasitics. While such trade-off considerations are less important for performance-driven military, aerospace, and medical applications, they can be the factor which ultimately determines practicality and marketability in cost-driven consumer product applications. Such issues must therefore be considered whenever construction labor becomes a significant fraction of the processing time or manufacturing cost.

3.5.2 Testability

Following completion of the construction of the hybrid circuit, the product must be tested for functionality. For some circuits, this can be as simple and straightforward as turning them on and running them at full power. In many cases, however, such an all-or-nothing approach can produce catastrophic destruction of the entire assembly if even one defect is present. This is especially true of power conditioning circuits, as differentiated from signal processing circuits, because the stored energy levels are significant and greater potential therefore exists to damage surrounding circuit components. A series of progressive tests, which can establish the functionality of the various subsections independently or isolate the construction defect, can be a valuable alternative approach for establishing functionality.

Such a test regimen generally requires special provisions in the design and construction

of the circuit, because the information and controls necessary to isolate and examine the various subsections are often unavailable at the input and output connections. Moreover, the physically compact nature of hybrid construction, and in particular the absence of component packages on the active devices, places additional restrictions upon the availability of connection nodes for testing. Finally, the presence of high field strengths, varying at megahertz frequencies, further complicates this testing by making low-noise, non-intrusive instrumentation more difficult. The implementation of custom instrumentation points, which provide remote access to critical nodes via extra interconnection traces, are one possible solution to the instrumentation/testing problem. Hybrid construction is particularly well suited for creating such instrumentation points, because the interconnnections are virtually parasitic-free and can be designed to achieve low noise pickup. Alternatively, designated test pads can be distributed throughout the circuit which can be probed by instrumentation and control circuits as necessary. These pads reduce the additional layout complexity associated with externalizing signals buried within the circuit, although at the expense of a reduction in circuit density. In either case, the relevant test points must be identified during the design phase, and some method of instrumentation laid out and built-in simultaneously with the construction of the rest of the circuit.

3.5.3 Reworkability

The main incentive for the development of a non-destructive, segmented testing methodology for evaluating subsystem functionality is to provide a means for identifying defective components and assemblies. In addition to indicating possible design or construction process flaws, this identification provides the information necessary for reworking and salvaging the circuit. This can be especially attractive for complex hybrids, which typically exhibit relatively low first-cut yields. Reworkability depends upon the successful identification and removal of defective parts, and their replacement with functional ones, without degradation of the surrounding components or the substrate. This in turn depends, to a great degree, upon the attachment methods used to secure the components to the hybrid substrate. In the case of epoxy adhesive attachment, the defective components can sometimes be removed by localized heating of the substrate, which helps weaken the adhesive, or by physical destruction of the components themselves. Use of the latter technique requires careful control, because the underlying substrate may otherwise be damaged.

When solder is used, the issue of temperature hierarchy once again becomes critical. In general, components must be removed in the reverse order of their assembly, in accordance with their solder liquidus temperatures. This is another reason that the heatsink is assembled last, with the lowest temperature solder: repeated soldering and desoldering of the heatsink, necessary during any reworking of the circuit, causes negligible performance degradation. Because active components are the most prone to failure, one might be inclined to install them last, for most convenient replacement. However, the wire bonding connections to these devices are best made early in the construction of the hybrid, both for component clearance reasons and to minimize surface degradation, which occurs continuously during processing and assembly. One solution to this problem is to assemble the active components first, and immediately perform functionality testing on these components. Any defective components can then be identified and reworked, before additional labor and materials are invested in the circuit. This is an especially valuable technique for minimizing losses in manufacturing processes where reworking is not possible, economical, or entirely successful.

3.5.4 Modularity

Another method for improving yields and lowering costs of production involves utilizing the inherent modularity of most circuits. In many cases, circuits (especially power circuits) can be partitioned into sections in such a way that connections between these sections are minimized, and the circuit density and low interconnection parasitics benefits of hybrid construction are not sacrificed. For example, most switching power converters exhibit DC isolation between the input and output, which is provided by a high frequency transformer. Separation of the hybrid circuit at the primary/secondary interface of the transformer is therefore one logical partitioning approach for increasing modularity of the circuit. Further separations between the control circuitry, the gate drive circuitry, the power train, or the complementary circuits in dual or push-pull converter topologies all increase circuit modularity.

The partitioning approach can be used in conjunction with, or in lieu of, the previously described construction, testing, and reworking techniques. It can often be most cost effective to use several different combinations of construction, testing, and reworking techniques on different partitioned modules within a single converter. For example, both active and passive devices in a feedback regulation control module might be attached using epoxy,

with the control chips in convenient surface mount packages. This would minimize assembly complexity by reducing processing steps and eliminating wire bonds. Meanwhile, a combined gate drive/power stage might be constructed using bare dice and unpackaged ICs, to minimize critical loop parasitics. These active devices would be soldered to the substrate to minimize thermal impedances and to facilitate reworkability. Then, using a partitioned testing routine, the cheaper controller modules might simply be discarded when non-functional, while a defective power train, with its more expensive power semiconductors, would be salvaged and reworked. Following successful testing of each completed subsection, the final hybrid circuit would then be assembled onto a single heatsink, and the modules would be interconnected.

3.5.5 Reliability

After the completed circuit is assembled and tested, it must be evaluated for reliability. This is presently an active area of research in the hybrid technologies field. Evaluations of the reliability of various thick film technologies [34] and the development of construction methods with improved reliability [35,36] are two major areas of research in the field of hybrid circuit construction. Dependable soldering to copper thick films [37,38] and long-term adhesion of thick films to various substrate materials [40,41,42] are particularly active areas of reliability research. In general, the circuit's reliability is intimately linked to the component and materials quality, the assembly techniques, the processing environment, and the final packaging or potting approach. Of these, the circuit designer and manufacturer generally have control over the latter three, with the former being limited by the state-of-the-art in component fabrication.

There are several general mechanisms for circuit failure, most commonly precipitated by over-heating of the active devices. Semiconductors are highly sensitive to temperature, with failure rates approximately doubling for every 10°C rise. Extreme temperature elevations can be caused by excessively thick adhesive or thick film dielectric layers, or by voids in die bonds or in the underlying bond between the substrate and the heatsink, all of which contribute to the thermal impedance between the device and its environment. Even when these bonds are initially satisfactory, stresses induced by thermal cycling can cause a shearing of the bonds at the joint interface, gradually reducing the effective thermal contact area and increasing the thermal impedance between the dice and the substrate [35,43].

The presence of moisture or ionic impurities can also precipitate degradation and failure of active devices. Moisture picked up during the assembly process is typically removed by oven baking prior to sealing [20]. The devices are then protected from the environment by glob-top encapsulation, potting, or hermetic packaging. Ionic contaminants in these protective coatings can react with the aluminum metallizations of the semiconductors, causing degradation over time [44]. Furthermore, moisture can diffuse through these coatings, which are typically porous epoxies, causing vapor outgassing within hermetic packages and accelerated corrosion of thick film and semiconductor metallizations.

Finally, there is an acknowledged concern over the formation of intermetallic compounds at the interfaces between layers of dissimilar metals. These compounds often have physical and electrical properties which differ significantly from those of either pure metal. In particular, these intermetallics may be much more brittle, and much poorer electrical conductors, than their pure constituents. The formation of these compounds is caused by diffusion or leaching of metallic particles between boundaries at interconnections, a process which can be accelerated by high temperatures and DC currents. Soldered interfaces, which may join two dissimilar metals using an alloy of several additional ones, are especially problematic [37]. This problem becomes acute in die bonding applications, where complete thermal and electrical contact must be maintained under conditions of shear stress imposed by TCE mismatches. The reliability of aluminum wire bonding on copper thick film is also being investigated, as the bonding of bare dice to copper hybrid substrates becomes more common [45].

3.6 Summary of Multilayer Copper Hybrid Issues

This chapter has described a multilayer copper hybrid construction process in the context of power conversion applications. It began with a characterization of hybrid circuit construction, contrasting hybrid substrates with standard PWBs. The mechanical, thermal, and electrical superiority of ceramics over phenolic and epoxy-glass materials was established, and their advantages for power circuit applications were discussed. A comparison of the various hybrid substrate construction options was then conducted. In particular, two thick film ink families, grouped according to firing atmospheres, were described. It was concluded that a copper-based ink family, although presenting some unique quality control challenges, presented the greatest potential for creating low-cost, mass-produceable power conversion

units suitable for point-of-load converters in distributed power conversion applications.

A detailed description of such a multilayer copper thick film hybrid substrate fabrication process was then presented. Details concerning the various printing, drying, and firing cycles for each of the backside, inner layer and final layer metallizations were related, including solutions to feature resolution and surface defect problems. Descriptions of a full multilayer process, complete with crossover dielectric, via fill metallization, and glass surface encapsulation were included, with a discussion of special considerations relevant to the fabrication of hybrid substrates with numerous layers (more than ten PDF cycles). Following these descriptions, various options in the component assembly process were described, with the interrelation of these options as parts of a complete and integrated assembly system being emphasized. In particular, the two distinct methods of adhesive and solder assembly were contrasted, with the strengths and weaknesses of each approach being assessed in the general context of hybrid circuit construction.

Finally, manufacturing issues such as construction labor, testability, reworkability, modularity, and reliability were addressed. These issues are becoming increasingly important in competitive, cost-driven markets where power conversion circuits are becoming increasingly popular. It is these manufacturing issues, in fact, that need further investigation, and their successful treatment will insure the feasibility of hybrid assembly as a practical method for constructing advanced power conversion circuits in the future.

The subsequent chapters report on the application of the previously described hybrid construction process in the implementation of the dual resonant forward converter circuit presented in Chapter 2. Before these results are presented, however, a special chapter is devoted to the description of a novel high frequency, high power, miniature transformer with extremely low leakage inductance. The development of such a transformer was necessary for the successful completion and testing of functional prototypes.

Chapter 4

Transformer Construction

This chapter addresses the construction and integration of high frequency magnetics in the context of hybrid power converters. The physical and electrical characteristics of the magnetics, particularly the power transformers, are critical to the successful operation of the DRFC. Presently, commercially available transformers fail to meet the numerous stringent criteria (low leakage inductance, low copper and core losses, high operating frequency, small volume) that have been established as optimal for POL applications. To overcome this failure, improved designs for high frequency power transformers have been developed. This chapter presents a novel transformer construction technique which satisfies the circuit constraints without sacrificing manufacturability.

Before considering design and construction innovations, it is first necessary to establish numerical estimates for the desired circuit parameters and tolerable parasitics. This is done in the first section, for the DRFC topology that was described in Chapter 2. These estimates are compared against corresponding magnitudes for typical commercial transformer designs and the shortcomings of the available options are highlighted.

One particular parameter, the parasitic leakage inductance, is identified as the major deficiency area in presently available commercial magnetics. As discussed in the Section 2.3, this parasitic impedes further advances in efficiency and power density and causes severe load regulation. Much of the present topological work in power conversion centers around the *exploitation* of leakage inductances in some lossless manner [19,48]. In contrast, realization of the numerous benefits of the DRFC topology depends upon the successful *minimization* of this parasitic. Both approaches require a thorough understanding of the origin of transformer parasitics in order to design magnetics with predictable, reproduceable leakage inductances. To this end, the second section describes a method for estimating the

magnitude of this parasitic in various transformer designs. This method is based upon energy storage considerations and provides valuable insight into design trade-offs for reducing transformer leakage parasitics. A number of transformer winding patterns are compared, leading to the conclusion that an interleaved parallel-planar-conductor configuration can reduce the leakage inductance by an order of magnitude.

The third section addresses the fabrication of such a winding configuration. Two possible winding orientations, barrel and planar spiral, are compared in terms of electrical performance, power density, and manufacturability. Prototypes of the resultant designs are constructed and tested, using special low-inductance secondary-side terminations compatible with hybrid construction.

4.1 Circuit Constraints on Transformer Design

In general, design specifications for the numerous transformer parameters are established as a compromise between various component imperfections. By iterating upon the process of circuit design, component selection, and performance analysis, numerical values for the turns ratio, magnetizing inductance, winding resistance, core size, and leakage inductance are derived. Such a derivation, augmented by the construction of several converter prototypes, was performed in determining the 'optimal' operating point for the DRFC. In this case, optimization was based upon the maximization of power conversion densities with efficiency factored in via heatsink size considerations. Based upon this analysis, and in conjunction with the discussions of Chapter 2 and a fore-knowledge of the achievable transformer characteristics, the following specific design parameters were established.

4.1.1 Turns Ratio

The desired turns ratio was perhaps the simplest parameter to specify. For winding patterns with a single secondary turn (to minimize leakage inductance and winding resistance), only integer ratios were acceptable. Thus, with a $40V$ in, $5V$ out system, a conservative ratio N_p:N_s of 6:1 was selected. This left ample tolerance for the output rectifier drop and for load regulation and reduced the effects of leakage inductance (which grow as the square of the turns ratio). Later iterations incorporated a 7:1 turns ratio, following improvements in transformer construction and the availability of low forward-drop schottky output rectifiers, with ratings of $0.35V$ at $10A$ for a $(125\text{ mil})^2$ die size.

4.1.2 Magnetizing Inductance

The magnetizing inductance serves as the inductive element in the resonant tank circuit which sets the resonant ring frequency. This frequency in turn sets the operating frequency of the entire converter for fixed duty-cycle operation. It is therefore beneficial to reduce this inductance, thereby increasing the conversion frequency and reducing the size of energy storage components. These gains must be traded off against increases in the magnitude of the magnetizing current, which cause additional dissipation in the transformer and thus sacrifice the overall conversion efficiency in order to increase power density.

The additional power dissipation in the primary winding due to the circulating magnetizing current was selected to be approximately 50% of the load-current-induced dissipation. For an average load current I_L being carried by a waveform which is approximately triangular[1], and a zero-centered, quasi-triangular magnetizing current[2] with peak-to-peak magnitude ΔI_{mag}, the major current components are essentially orthogonal. The average power dissipations can thus be separated and equated, giving

$$R_{pri}\frac{4}{T/4}\int_0^{T/4}(\frac{\Delta I_{mag}}{2}\frac{t}{T/4})^2\,dt = 50\%\,R_{pri}\frac{1}{T}\int_0^{T/2}(2\,I_L\frac{N_s}{N_p}\frac{t}{T/2})^2\,dt \qquad (4.1)$$

Solving these integrals yields the relationship that the peak-to-peak magnetizing current ΔI_{mag} should be equal to the average primary load current $I_L\,N_s/N_p$.

Using this relationship, the magnetizing inductance is given by

$$L_{mag} = \frac{V_{in}}{2\,f_{sw}\,\Delta I_{mag}} = \frac{V_{in}}{2\,f_{sw}}\left(\frac{1}{I_L}\right)\frac{N_p}{N_s} \qquad (4.2)$$

where the switching frequency f_{sw} is proportional to the resonant frequency f_{res}, as shown by (2.13). Using the relationship

$$f_{res} = \frac{1}{2\,\pi\sqrt{L_{mag}C_{res}}} \qquad (4.3)$$

an explicit expression for L_{mag} is derived.

$$L_{mag} = 16\,(\frac{V_{in}}{I_L}\frac{N_p}{N_s})^2\,C_{res} \qquad (4.4)$$

For a load current I_L of $10A$, a turns ratio $N_p : N_s$ of 7:1, and an equivalent linear resonant capacitance C_{res} of about $200pF$ (determined by the available selection of commercial $200V$

[1] as explained in Section 2.3.1 for $L_{leak}/R_{out} << \frac{1}{2\,f_{sw}}$.

[2] as described in Section 2.1.4, with $\Delta I_{mag} = 2I_p$.

MOSFETs), this gives a resonant frequency of 7.1 MHz. Thus, the primary-referenced magnetizing inductance is $2.5\mu H$, and the switching frequency is 5.5 MHz. This magnetizing inductance can easily be achieved with a seven turn primary wrapped around a standard commercial gapped core.

4.1.3 Core Loss

Given the previously cited magnetizing inductance, and the volt-seconds associated with a $40V$, 50% duty cycle square wave at 5.5 MHz, the energy storage of the magnetizing inductance can be calculated. In view of the fact that the circulating current has no DC component, the peak magnetizing energy is found to be

$$E_p = \frac{1}{2} L_{mag} (\frac{\Delta I_{mag}}{2})^2 = 650\ nJ \tag{4.5}$$

For high frequency operation, hysteretic core loss is minimized by using a gapped structure, implying energy storage within the gap. For the previously calculated magnetizing inductance, this gap length must be

$$2\,g = \frac{N_p^2\,\mu_o\,A_g}{L_{mag}} = 420\mu m \tag{4.6}$$

where a gap area A_g of $17mm^2$ (corresponding to an Ferroxcube size 1107 potcore) has been assumed. Finally, for such a core configuration, the peak magnetic flux density B_p will be

$$B_p = \sqrt{\frac{2\mu_o E_p}{g A_g}} = \frac{\mu_o\,N_p}{g}\frac{\Delta I_{mag}}{2} = 150G \tag{4.7}$$

High frequency magnetics which operate in the 1–10 MHz range typically require cores made from nickel zinc ferrite materials. At 5 MHz, the core loss for a 4C4 NiZn ferrite composition is approximately $1.25W/cm^3$ for the computed flux density [14]. Selecting a Ferroxcube 1107-4C4 potcore with a core volume of $0.25cm^3$ yields a core loss of approximately $300mW$ per transformer. For the dual converter configuration, operating at $50W$ load, this would result in an acceptable 1.5% reduction in efficiency.

4.1.4 Winding Resistance

The winding resistance of a power transformer can be a significant source of loss, due to the relatively large load currents and the dependence of the resistive dissipation on I^2. This loss tends to increase with frequency, as the skin and proximity effects become more pronounced. In most cases, the skin effect is minimized by keeping the conductor thickness

less than a skin depth at the operating frequency (1.1 mils at 5.5 MHz). Then, assuming that the copper is split 2:1 between the primary and secondary, and including dissipation due to the circulating magnetizing current, the total copper loss in one transformer is

$$P_{Cu} = \frac{3}{2}\left[\frac{1}{6}\,(2\,I_L\,\frac{N_s}{N_p})^2\,R_{pri}\right] + \frac{1}{6}\,(2\,I_L)^2\,R_{sec} = \frac{7}{6}\,I_L^2\,R_{sec} \tag{4.8}$$

where all losses have been referred to the secondary and written in terms of the average load current I_L. Alloting 600 mW total dissipation per transformer (i.e. equal copper and core losses of 300 mW each), which corresponds to a total reduction in conversion efficiency due to transformer losses of less than 2.5%, this requires a secondary resistance R_{sec} of $2.6m\Omega$, and a primary resistance R_{pri} of $65m\Omega$.

For the seven turn primary with each turn approximately $1in$ long, this resistance equals $111m\Omega/ft$, the DC resistance of #30 AWG copper wire (diameter = $10\ mils$). At 5 MHz, the currents only flow in the outer $1mil$ of the conductor, increasing the apparent resistance substantially. At this frequency, an effective skin depth area of $72mils^2$ is required, which would necessitate the use of #18 AWG wire (diameter = $40mils$). Multi-strand Litz wire is typically substituted for such single-conductor windings, due to its lower AC resistance and resultant economy of space within the core.

4.1.5 Leakage Inductance

The final parameter to be calculated is the parasitic leakage inductance of the transformer. The DRFC topology imposes two constraints upon this element for satisfactory converter operation. First, the energy stored in the leakage field must be small because this energy is dissipated during the turn-off transition of each power delivery cycle. Additionally, the impedance of the leakage inductance should not cause excessive load regulation.

To achieve the overall efficiencies desired for POL conversion applications, the total power lost due to leakage energy dissipation should be less than 3% of the load power P_L. For 5 MHz operation, this gives

$$L_{leak} \leq 3\%\,\frac{P_L}{4\,I_{load}^2\,f_{sw}} = 0.75nH \tag{4.9}$$

where the load current is assumed to be triangular and dual operation is taken into account.

For an *incremental* parasitic output resistance R_{out} of $15m\Omega$,[3] this gives an L_{leak}/R_{out} time constant of $50nsec$, which is comparable to the duty cycle at 5 MHz ($100nsec$). The

[3] from (2.17), with $R_{reg} \approx 0m\Omega$, $R_{DS_{on}} = 400m\Omega$, $R_{pri} = 65m\Omega$, $N_p/N_s = 7$, $R_{sec} = 2.6m\Omega$, and $R_{D_{on}} = 2.7m\Omega$

output current through the leakage inductance therefore looks more like an exponential than a ramp, and the peak current is reduced from the $2I_L$ assumed above. To more accurately calculate the leakage energy lost under these conditions, the peak current is first found by integration

$$\int_0^{2\tau} I_L \, dt \; = \; \int_0^{2\tau} I'_{L_p} \, (1 - e^{-t/\tau}) \, dt \tag{4.10}$$

where I'_{L_p} is the extrapolated final value of the exponential current waveform. From this equation, an I'_{L_p} of 1.76 times I_L is computed, corresponding to a peak current I_{L_p} of 1.5 I_L. The total power dissipated due to the two leakage inductances of $0.75nH$ each is thus 850 mW, or 1.7% of the load power.

The specified values for the magnetizing and leakage inductances give a ratio L_{leak}/L_{mag} of less than 1.5%. This small ratio, and the even smaller *absolute* magnitude of the leakage inductance itself, is difficult to achieve even when using bifilar winding construction techniques, especially within the size constraints and winding ratios specified. For example, bifilar wound #30 AWG wire has an inductance of approximately $14nH/in$. Using such wire would result in a secondary-referred leakage inductance of nearly $2nH$, more than twice the specified requirement of $0.75nH$. Unfortunately, this tight bifilar coupling is degraded as connections are made to parallel each of the seven one-turn secondaries, resulting in even greater leakage inductances. Furthermore, the total effective parasitic inductance will be much greater when the additional effects of primary- and secondary-winding interconnection inductances are factored in. For these reasons, standard transformer construction techniques were judged inadequate to achieve the low leakage inductances desired for operation of the DRFC.

4.2 Calculation of Leakage Inductances

Based upon the findings of the preceding section, it was concluded that a different construction method, specifically optimized for achieving low leakage inductances, was necessary. In order to design this winding, a simple model was created to represent the leakage fields and estimate the inductances in various designs. This model is presented in the following subsection. A series of analyses are then performed to compare various construction techniques, and some general conclusions concerning low leakage transformers are drawn.

4.2.1 General Field Model Approach

The field model approach to quantifying transformer leakage inductances exploits the fact that a transformer has two distinct energy storage mechanisms corresponding to the leakage and magnetizing inductances. Under well-defined circuit constraints, it is possible to set the magnetizing current to zero, thereby nulling the magnetizing energy as well. In this situation, all magnetic fields contribute leakage fields, and the total leakage energy is equal to the total stored magnetic energy. Once this energy is known, the leakage inductance follows from the constrained winding currents.

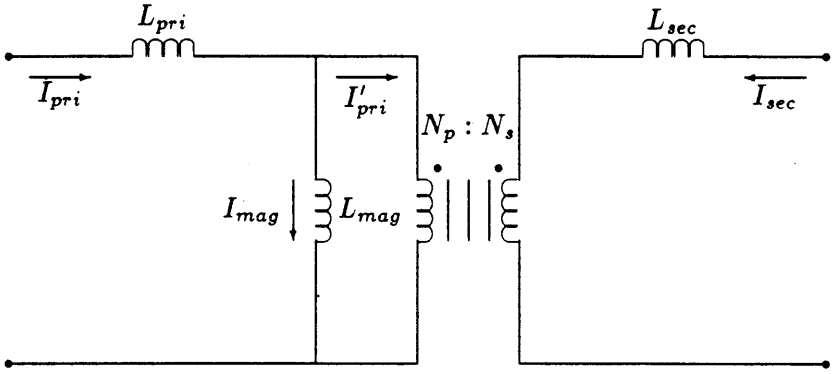


Figure 4.1: Lossless Transformer Circuit Model

The electrical model used to establish these circuit constraints is based upon the standard lossless transformer circuit representation shown in Fig. 4.1. It consists of an ideal transformer with an $N_p : N_s$ turns ratio, a magnetizing inductance L_{mag} in parallel with the primary, and a pair of leakage inductances L_{pri} and L_{sec} in series with the primary and secondary, respectively. The equations relating the indicated branch currents are

$$I_{pri} = I_{mag} + I'_{pri} = I_{mag} + \frac{N_s}{N_p} I_{sec} \tag{4.11}$$

Requiring that the stored magnetizing energy be zero establishes the current constraint

$$I_{pri} = \frac{N_s}{N_p} I_{sec} \tag{4.12}$$

Under this condition, the secondary leakage inductance can be reflected to the primary, and a total leakage inductance L_{leak} can be defined

$$L_{leak} = L_{pri} + (\frac{N_p}{N_s})^2 L_{sec} \tag{4.13}$$

The magnitude of this element is then computed by equating the energy stored in an inductor to the energy stored in the transformer magnetic fields

$$W_m = \frac{1}{2} L_{leak} I_{pri}^2 = \iiint_{VOL} \frac{\overline{B}^2}{2\mu} dV \tag{4.14}$$

In general, it may be difficult to determine such fields analytically, and a finite element approach might seem necessary. However, the extensive symmetry, periodicity, and relative simplicity of most transformer designs generally permits direct calculation of these fields under the constraint established by (4.12). The following discussion demonstrates the simplicity of this approach and provides valuable insights concerning the minimization of leakage inductances in transformer designs. Section 4.4 establishes the validity of this technique by correlating predicted and experimental values for the leakage inductances of several transformer designs.

4.2.2 Field Model Evaluation: Single-Bobbin Windings

To illustrate this analysis technique, a generic N_p:N_s transformer is first considered. Potcore construction is assumed, although the techniques are equally applicable to E-core, tape-wound, and most other co-axial winding configurations. Two possible potcore winding patterns are shown in Fig. 4.2, for lapped and butted winding configurations. The transformer windings are located in the same cavity, with distinct winding areas for the primary and secondary turns. For N_p and N_s large, the current distributions will be essentially uniform and azimuthal. The details of the windings can then be suppressed and replaced by uniform current densities $J_{\theta p}$ and $J_{\theta s}$, as shown.

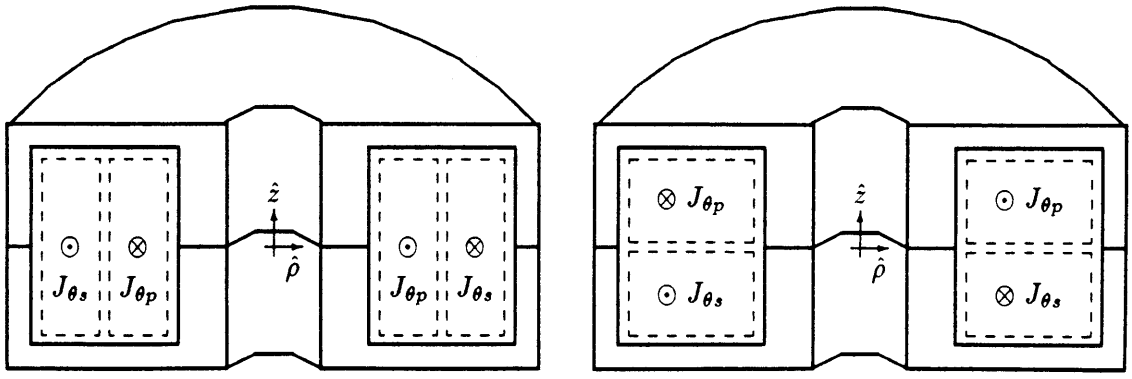


Figure 4.2: Single Bobbin Lapped and Butted Winding Configurations

For operation under the current constraint of (4.12), this gives rise to the equivalent current density constraint

$$J_{\theta p} A_p = -J_{\theta s} A_s \tag{4.15}$$

where A_p and A_s are the cross-sectional areas of the primary and secondary windings, respectively. Thus, when the winding areas are made equal, e.g. to give balanced copper losses in the primary and secondary, the current densities will also be equal (although oppositely directed).

Once the current distributions are known, the magnetic field solutions can be solved explicitly by using Maxwell's Equations. The lapped winding configuration shown in Fig. 4.3 is considered first, and an expression for the leakage inductance is derived.

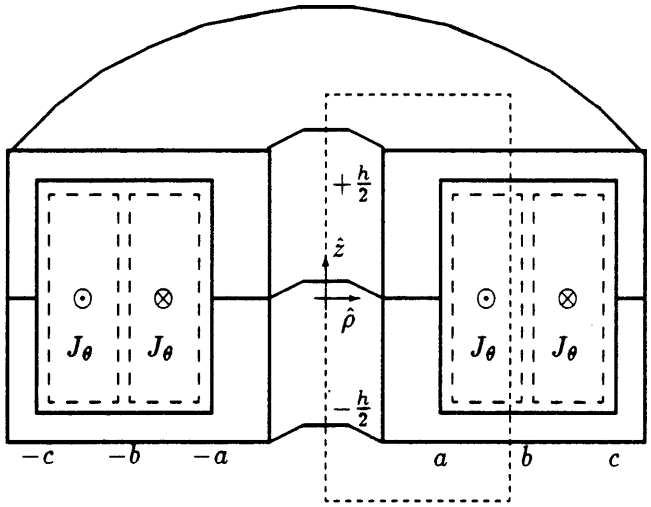


Figure 4.3: Integration Path for Lapped Winding Transformer

Using the indicated integration path, Ampère's Integral Law

$$\int \overline{H} \cdot d\bar{l} = \int \overline{J} \cdot d\overline{A} \tag{4.16}$$

is solved to determine the magnetic field as a function of ρ.

$$B_z(\rho) = \mu_o H_z(\rho) = \mu_o \frac{N_p I_{pri}}{h} \left(\frac{\rho - a}{b - a} \right) \ , \ b > \rho > a \tag{4.17}$$

$$B_z(\rho) = \mu_o H_z(\rho) = \mu_o \frac{N_p I_{pri}}{h} \left(\frac{c - \rho}{c - b} \right) \ , \ c > \rho > b \tag{4.18}$$

In performing the integrations, the fields are approximated as solenoidal within the winding volume, so that there is no variation in $\overline{B}$ along the z-axis, and contributions from $\overline{B}$ external

to the winding volume are negligible. This gives rise to a slight overestimate of $B_z(\rho)$ near $z = \pm\frac{h}{2}$, which in turn will lead to a slightly conservative overestimate of the leakage inductance.

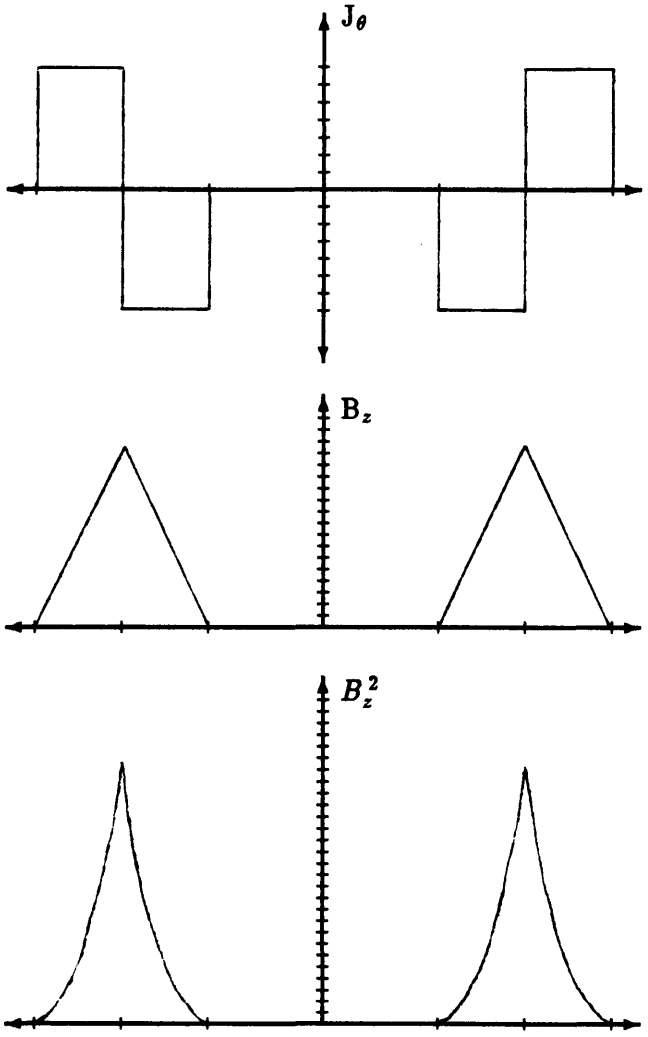


Figure 4.4: Current Density and Magnetic Field Profiles

The current density distributions $J_\theta(\rho)$ derived from (4.15) and resultant magnetic field distributions $B_z(\rho)$ from (4.17) and (4.18) are plotted in Fig. 4.4. In addition, the squared magnetic field strength $B_z^2(\rho)$, which is proportional to the magnetic energy density, is shown. As given in (4.14), the leakage inductance L_{leak} is found by integrating this density throughout the winding volume. Using the derivations in Appendix B, these integrations are reduced to simple algebraic functions of the area under the triangular B_z curves, designated

A_{ab} and A_{bc}. The leakage inductance of the structure is thus found to be

$$L_{leak} = \frac{1}{I_{pri}^2 \mu_o}\left\{2\pi h [A_{ab}]^2(\frac{b+a/3}{b-a}) + \frac{2}{3}\pi h [A_{bc}]^2(\frac{c+3b}{c-b})\right\} \quad (4.19)$$

$$= \frac{2\pi h}{I_{pri}^2 \mu_o}\left\{\left[\frac{\mu_o N_p I_{pri}(b-a)}{2h}\right]^2(\frac{b+a/3}{b-a}) + \frac{1}{3}\left[\frac{\mu_o N_p I_{pri}(c-b)}{2h}\right]^2(\frac{c+3b}{c-b})\right\}$$

When the winding dimensions a, $b-a$, and $c-b$ are all approximately equal, this expression simplifies to

$$L_{leak} \approx \frac{2\pi h}{I_{pri}^2 \mu_o}\left\{\left[\frac{\mu_o N_p I_{pri}(b-a)}{2h}\right]^2(\frac{7}{3}) + \frac{1}{3}\left[\frac{\mu_o N_p I_{pri}(c-b)}{2h}\right]^2(9)\right\}$$

$$\approx \frac{8\pi \mu_o N_p^2 a^2}{3h} \quad (4.20)$$

Thus, the estimation of the transformer's leakage inductance has been accomplished without extensive numerical integration or finite element analysis. By exploiting the inherent symmetry of the transformer, the field solutions are approximated as constant and solenoidal. The magnetic field profiles are therefore triangular, and the necessary volume integrations can be replaced by equivalent algebraic solutions. A similar analysis can be performed for the butted winding configuration by recognizing that the fields are approximately constant in ρ, and that the field quantity of interest is now a function of z, i.e. $\overline{B} = B_\rho(z)$.

In addition to the convenience afforded by this method, energy density arguments provide a highly intuitive method for identifying the sources of leakage inductance. In particular, the field and current density profiles of Fig. 4.4 suggest that a simple redistribution of the winding window areas will greatly reduce the magnitude of the peak fields, and hence lower the leakage inductance of the transformer. The following subsection explores this redistribution process, comparing two simple interleaved structures using the field model approach.

4.2.3 Field Model Evaluation: Interleaved Windings

Applying the previous field model evaluation techniques to the lapped winding transformer, two interleaved winding constructions are compared to the original single-partition winding of Fig. 4.3. These new constructions, consisting of 2- and 5-partition windings, are shown in Fig. 4.5, along with their corresponding current density and magnetic field profiles. Note that the test conditions and axis scales have been held constant to facilitate direct comparisons. In particular, the magnitude of the current density J_θ remains unchanged, and

hence the rate of change of $B_z(\rho)$ is the same. However, the interleaving process limits the peak excursions of $B_z(\rho)$, thereby reducing the *square* of the peak magnitude substantially. It is the non-linear nature of the energy storage density which makes interleaving a beneficial process in the construction of low leakage inductance transformers.

Quantitatively, the benefits of interleaving can be evaluated by first deriving expressions for the leakage inductances of the 2- and 5-partition windings. The peak field magnitude $B_{p,2}$ is first determined using Ampère's Integral Law (4.16), giving

$$B_{p,2} = \frac{\mu_o (\frac{N_p}{2}) I_{pri}}{h} \tag{4.21}$$

This magnitude is half the peak value of the single-partition winding, as given by (4.17) and (4.18) for ρ=b. Then, using the same winding dimensions assumed in the solution to (4.20), the leakage inductance of the 2-partition winding becomes

$$\begin{aligned} L_{leak,2} &= \frac{2\pi h}{I_{pri}^2 \mu_o}\left[\frac{\mu_o N_p I_{pri}\frac{a}{2}}{4h}\right]^2 \left\{(\frac{3a/2+a/3}{3a/2-a}) + \frac{1}{3}(\frac{2a+9a/2}{2a-3a/2}) + \right. \\ &\qquad \left. (\frac{5a/2+2a/3}{5a/2-2a}) + \frac{1}{3}(\frac{3a+15a/2}{3a-5a/2})\right\} \\ &= \frac{\pi \mu_o N_p^2 a^2}{32h}\left\{\frac{11}{3}+\frac{13}{3}+\frac{19}{3}+\frac{21}{3}\right\} \\ &= \frac{2\pi \mu_o N_p^2 a^2}{3h} \end{aligned} \tag{4.22}$$

This leakage inductance is precisely one-fourth the original magnitude. The peak field magnitude $B_{p,5}$ and leakage inductance $L_{leak,5}$ of the 5-partition winding are similarly found to be

$$B_{p,5} = \frac{\mu_o \frac{N_p}{3} I_{pri}}{h} \tag{4.23}$$

$$L_{leak,5} = \frac{2\pi h}{I_{pri}^2 \mu_o}\left[\frac{\mu_o N_p I_{pri}(a/3)}{6h}\right]^2 \{(48)\} = \frac{8\pi \mu_o N_p^2 a^2}{27h} \tag{4.24}$$

The leakage inductance is thus reduced by a factor of 9. This leads to the general result that, for a given winding window dimension, interleaving reduces the leakage inductance by the *square* of the reduction in area under the $\overline{B}$ field profile. This remains accurate as long as the approximations made in the derivation (negligible space between windings, uniform current densities, etc.) are appropriate. This method of leakage inductance estimation can thus be repeated for higher levels of interleaving without carrying out further calculations (which increase in length because the number of terms increases with the number of interleaved

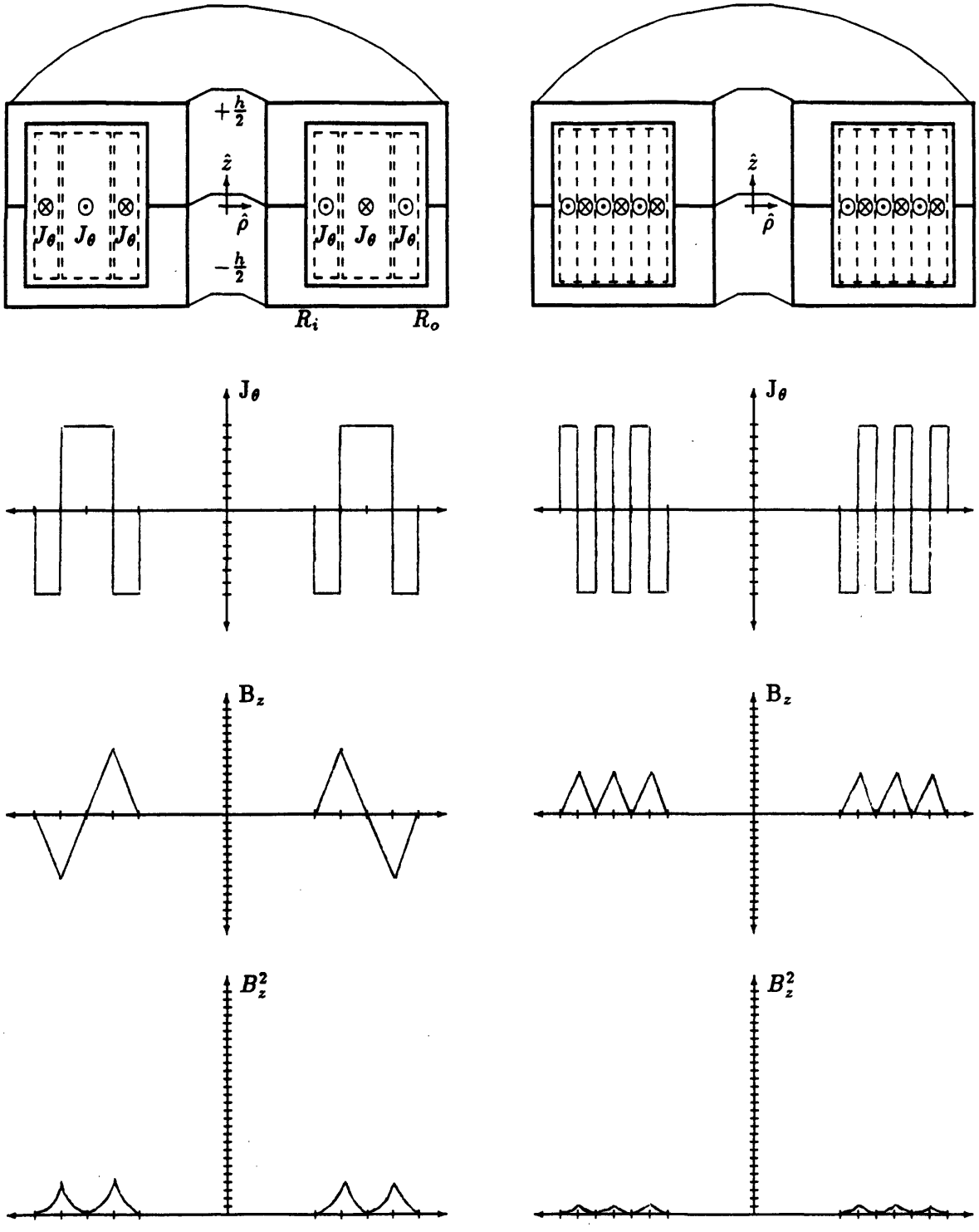


Figure 4.5: Comparison of Interleaved Windings

layers), by simply adjusting the original estimate. Finally, as with the original derivation, these examples can be extended to interleaved structures of butted windings, producing analogous results.

Bifilar Windings

By considering the limiting case of interleaved winding patterns, it is possible to understand, at least in principle, the advantages of structures made using the traditional bifilar-winding construction technique. In particular, the well-known benefit of relatively low leakage inductance attributed to bifilar construction can be interpreted in light of the preceding discussions. If one considers the current density profile of the winding window cross-section of a bifilar-wound transformer, it becomes immediately apparent that such a structure is in fact interleaved in two dimensions ($\hat{z}$ and $\hat{\rho}$ in the previous figures). While the fields are no longer solenoidal and an explicit calculation is therefore not possible using the previous field distribution approximations, it is clear that such extensive interleaving would produce a relatively weak $\overline{B}$ field with low average magnitude. The behavior of transformers constructed using bifilar winding techniques is therefore entirely consistent with the intuition provided by field model analysis.

While it might appear that unlimited reduction in leakage inductance would be possible by extending this approach, there are in fact practical limits. The field model ignores the spaces between conductor layers which are required for electrical insulation and safety isolation. As the number of interleaved layers becomes greater, this spacing becomes a significant fraction of the total core winding cross-section, and inter-conductor fields can no longer be neglected. In fact, it is precisely within these spaces between layers that the fields are greatest in magnitude, and hence these spaces become the dominant contributors to the leakage fields. Insulation between the conductors, and the inherent space between adjacent cylindrical objects dictates a minimum inductance per unit length, for a given wire diameter and insulation thickness, as discussed in Section 4.1.5.

To reduce the leakage inductance beyond this point using bifilar winding techniques, it is necessary to employ larger diameter wires or to parallel multiple windings. Both of these approaches introduce additional copper volume to the design, increasing the transformer cost. Furthermore, both solutions suffer from additional problems: at high frequencies, the utilization of larger wires provides a negligible reduction in ac resistance due to skin depth

effects, while for small transformers, interconnection difficulties complicate their construction and can introduce additional inductance which negates the theoretical advantages of paralleling multiple windings. Because the DRFC transformers are required to be compact and to operate in the MegaHertz frequency range, bifilar winding proved unacceptable as a construction approach.

Planar Conductor Windings

Based upon conclusions drawn from the previous discussions, parallel planar conductors were selected to replace the bifilar windings. Because of their flat geometry, they provide the tightest possible coupling between conductors, comparable to conductors of infinite radius, and hence a significantly lower inductance per volume. Another advantage of planar windings is that their thickness can be made comparable to the skin depth of the conductor material at the operating frequency, greatly reducing wasted space and unnecessary weight. As an added benefit, low-leakage transformers constructed with parallel planar windings are a convenient structure to design using the previously developed field model approach.

Using the circuit constraints and resultant design specifications for the DRFC transformers that were developed in Section 4.1, a 7:1 transformer with 7 series-connected single-turn primary windings and 3 parallel-connected, interleaved single-turn secondary windings was designed. This structure is shown in Fig. 4.6, along with the associated field profiles. In addition, a similar non-interleaved 7:1 transformer design is shown for comparison. Only three secondaries are used in order to overcome manufacturing difficulties, a consideration which will be discussed in the Section 4.3. Note that each primary and secondary winding area now represents a single planar conductor, rather than a conglomeration of parallel wires. The current density J_θ remains evenly distributed, however, as long as the conductor thickness is comparable to its skin depth.

Following the field model approach, the peak field magnitude $B_{p,1}$ and leakage inductance of the single-partition non-interleaved structure are found to be

$$B_{p,1} = \frac{7\,\mu_o I_{pri}}{h} \tag{4.25}$$

$$L_{leak,1} = \frac{2\pi h}{I_{pri}^2 \mu_o}\left[\frac{7\mu_o I_{pri}}{2h}\left(\frac{R_o - R_i}{10}\right)\right]^2 \left\{9\left(\frac{R_i + \frac{3}{10}(R_o - R_i) + \frac{R_i}{3}}{\frac{3}{10}(R_o - R_i)}\right) + \frac{49}{3}\left(\frac{R_o + 3[R_i + \frac{3}{10}(R_o - R_i)]}{\frac{7}{10}(R_o - R_i)}\right)\right\}$$

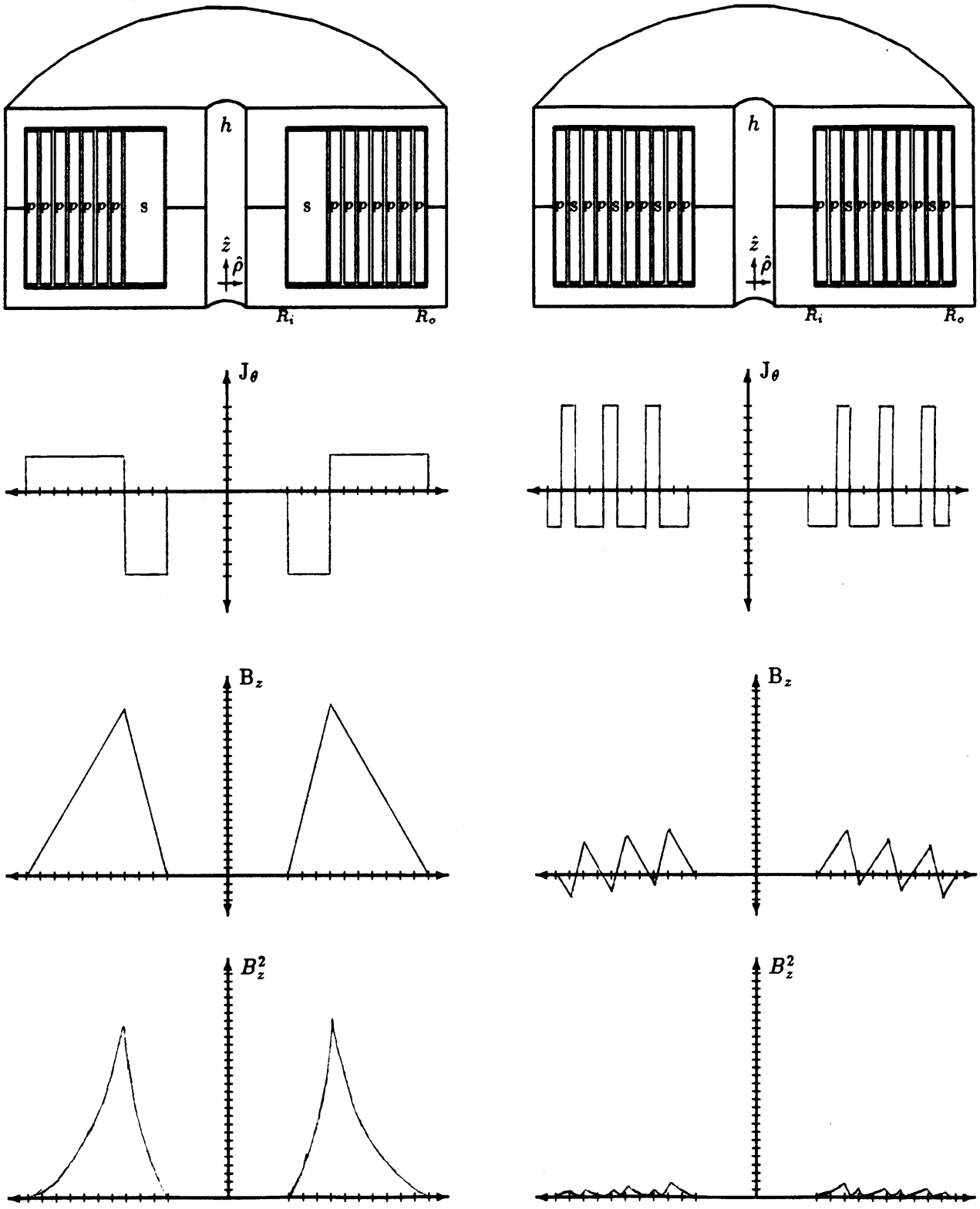


Figure 4.6: Comparison of Normal and Interleaved 7:1 Winding Structures

$$= \frac{98\,\pi\,\mu_o\,(R_o - R_i)}{400\,h}\{\frac{10}{3}(31R_i + 9R_o)\}$$
$$\approx \frac{100\,\pi\,\mu_o\,R_i^2}{h} \tag{4.26}$$

where $R_o \approx 3R_i$ has been assumed. Then, using the fact that the area under the $\overline{B}$ field profile of the interleaved structure is reduced by a factor of 5 from the non-interleaved case, the leakage inductance $L_{leak,6}$ of the 6-partition interleaved winding is

$$L_{leak,6} \approx \frac{4\,\pi\,\mu_o\,R_i^2}{h} \tag{4.27}$$

Compared to the non-interleaved 7:1 structure, the leakage inductance of this design is thus reduced by a factor of 25. Furthermore, the interleaving of the secondary reduces its ac resistance, a benefit which cannot be realized simply by increasing the thickness of a non-interleaved winding once the skin depth has been exceeded.

From these results, it is clear that the benefits provided by interleaving and the use of planar conductors are significant, in terms of reducing leakage inductance and overcoming the skin effect. Unfortunately, the manufacturabilty of such planar conductor windings is complex. The next section explores several approaches for producing these windings, and and also for integrating a low-inductance secondary termination for interconnection to the rest of the circuit.

4.3 Construction of Planar-Wound Transformers

There are two general orientations in which the windings can be placed to produce practical transformer windings. The barrel winding orientation has already been introduced; it consists of alternating layers of lapped conductors and insulation, tape-wound around a center core, as shown in Fig. 4.6. The alternative, a flat spiral winding orientation, is shown in Fig. 4.7 [15]. This section describes each of these construction approaches, emphasizing their respective advantages and shortcomings.

4.3.1 Barrel Windings

The barrel type of planar conductor winding was constructed by wrapping strips of conductor around a center bobbin or form. These conductive strips were scribed and cut by hand from sheets of copper foil, with a thickness of 1 mil for the primary and 2 mils for each of

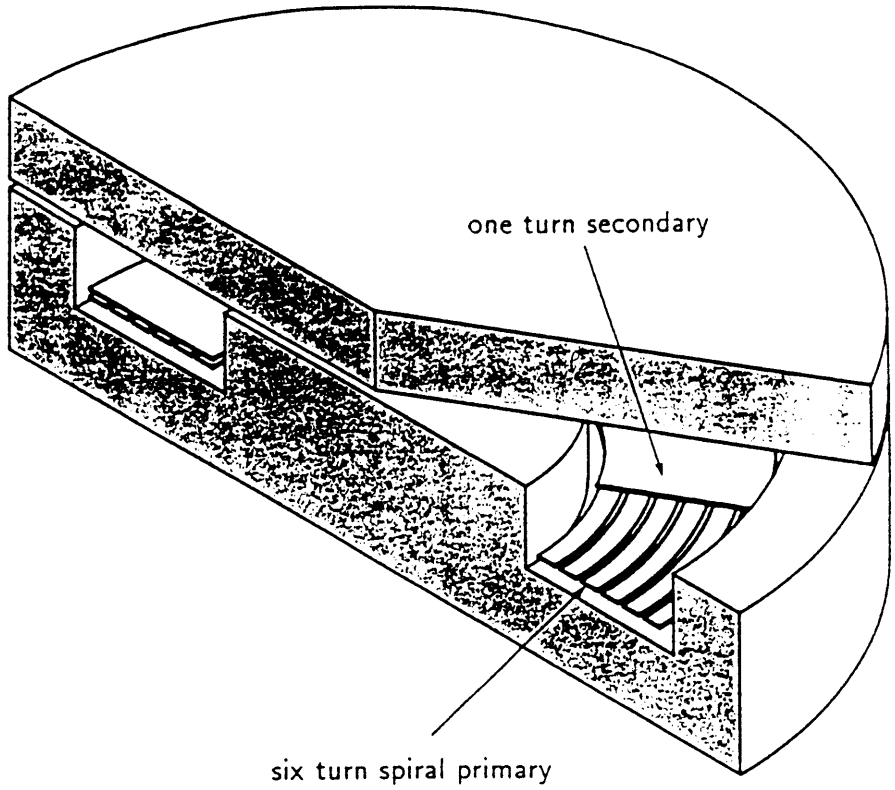


Figure 4.7: Spiral Wound Planar Conductor Transformer

the secondaries. Adhesive polyester tapes, with thicknesses ranging from 0.8–2.2 mils (including their acrylic adhesive backings), served as dielectric insulation between conductive layers. Tabs were left on each end of the primary and secondary foils to permit interconnection by soldering, with an additional tab being placed on the primary to create the tap for the pre-regulator connection. The tape was applied to these foils and trimmed around the edges, and the windings were wrapped on plastic bobbins (Ferroxcube F1D). The tabs were then bent and soldered appropriately to connect the secondary windings in parallel within the core volume, leaving two tabs for external secondary interconnection and three external primary tabs. A transformer constructed using such techniques is shown in Fig. 4.8, alongside the unwrapped primary and multiple interleaved secondary windings.

Despite the good electrical performance of the transformers produced by such a construction (see Section 4.5), there were a number of problems which prompted further investigation. To begin with, the construction method was extremely labor-intensive, requiring several hours per transformer for construction. Although portions of the manufacturing

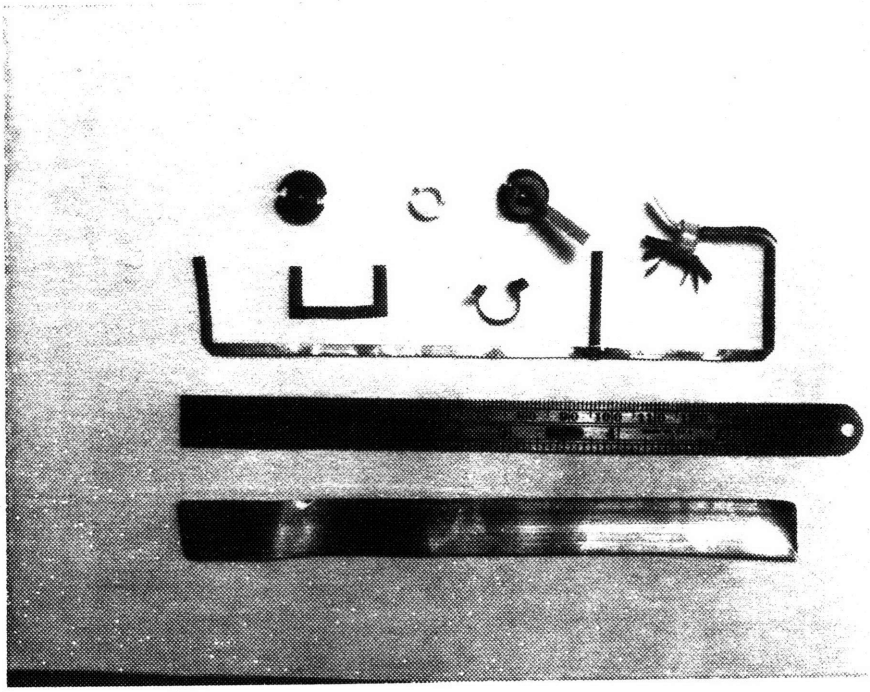


Figure 4.8: Barrel-Wound Foil-Conductor Transformers

process could be automated in a large-scale manufacturing context, the bulk of the work (particularly applying the windings to the bobbin and soldering the internal secondary tabs) would remain as hand labor. These manual steps introduce a significant reproduceablity (matching) problem, because the leakage inductance is a strong function of winding tightness, alignment, tape creasing, etc. The matching of these leakage inductances is critical to the achievement of equitable current sharing between halves of the dual converter, without which circuit performance is seriously degraded.

In addition to this consistency problem, it was determined that a lower profile transformer (i.e., reduced height h) would be sufficient for the needs of the DRFC. Since the transformers dominate the profile of the converter, any a reduction in their height would translate directly into an increase in power density, an important advantage. Unfortunately, the width of the windings (already only 120 mils wide) could not be reduced without introducing significant additional manufacturing problems in the previously described foil winding approach.

Laminated Copper/Polyimid/Copper Conductors

A flexible system of laminated copper/polyimid/copper (FLEX) was therefore adopted as the basis from which to form the planar conductors and intervening dielectric insulators. This sandwich system was originally introduced commercially for flexible printed circuit board applications. Like the conventional rigid epoxy-glass board, FLEX can be photolithographically etched to produce conductive patterns with a high degree of resolution (typically better than 5 mils).

A sample photo mask set designed to produce the primary and secondary windings simultaneously in a single two-sided exposure process is shown in Fig. 4.9. The bottom trace masks off the primary winding, in this case a 7-turn tapped primary with long tabs for the primary side connections. The top three traces are three parallel secondaries which, upon winding, end up on top of each other to form the single-turn interleaved secondary. The small tabs on the ends of these secondaries are provided to permit a parallel electrical connnection, producing a final winding structure with a triple-interleaved, single-turn secondary. Prior to photographic exposure, the primary and secondary winding masks are first aligned using the square fiducials. The photosensitive FLEX is then inserted between them and exposed in the usual manner for double-sided PCB processing.

A pair of transformer windings are shown in Fig. 4.10, following exposure between the double-sided photo-resist pattern, immersion in the developer solution, and etching to remove the undesired copper. Note that the primary windings can be seen behind the triple secondaries, through the semi-transparent polyimid insulation layer. This winding version has multiple primary tabs for testing and diagnostic purposes. After the left-over photoresist has been stripped, the windings of Fig. 4.10 are cut out along the edges of the exposed copper, coated with insulating tape, and wound around a form. Finally, the secondary tabs are soldered, and the windings are removed from the form and inserted into the core.

The FLEX windings manufactured in this manner are superior to the foil windings in several respects. First, the FLEX windings require less tape insulation than foil windings, reducing labor and inconsistency between components. Second, the single piece construction of the FLEX winding greatly simplifies the winding process and facilitates tighter, more controlled layering. This in turn permits the elimination of a coil form from the finished winding structure, thereby increasing the available winding window space (by nearly

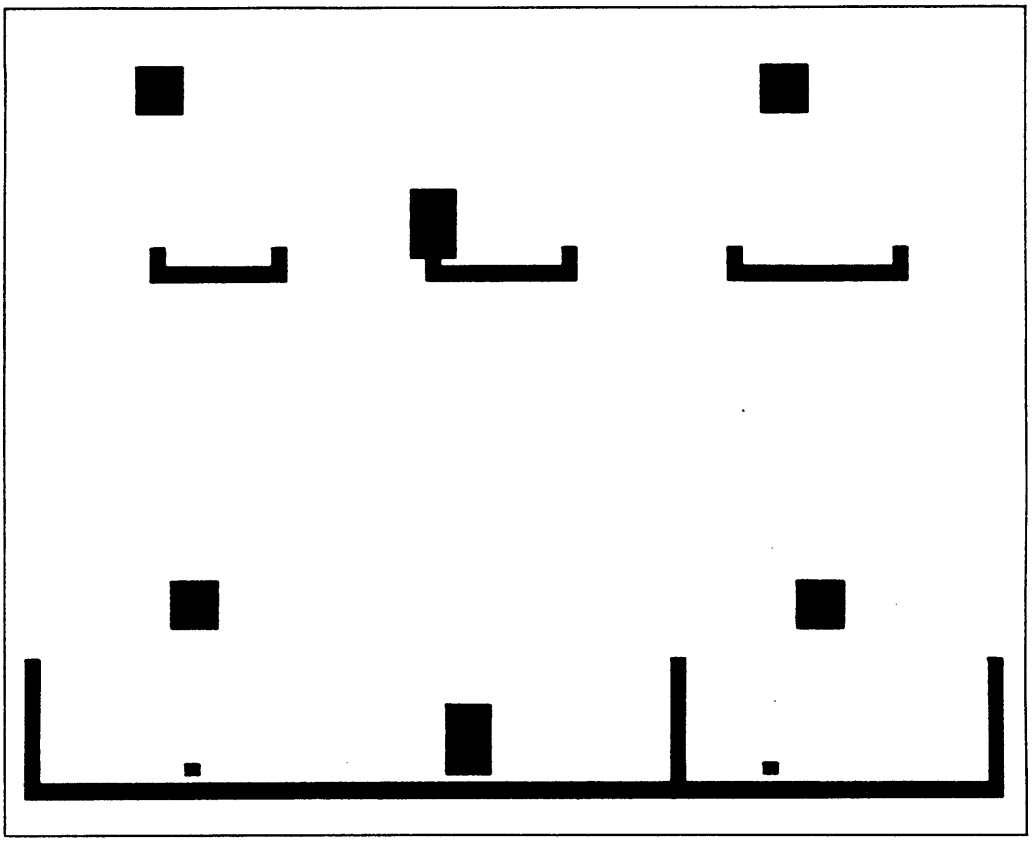


Figure 4.9: FLEX Photolithography Masks

30%). The advantage of guaranteed alignment between opposite sides of the FLEX further enhances reproduceability of the leakage characteristics. Additionally, it is possible to die punch the windings from the blank FLEX sheets prior to photo-processing, thereby eliminating hand-cutting of the polyimid layer and further streamlining the fabrication process.

Unfortunately, the FLEX winding technique as described has a major manufacturing drawback in that it still requires the soldering of internal tabs to connnect the multiple secondaries inside the transformer. This soldering, in addition to being a tedious and time-consuming process, opens up the possibility of creating internal winding shorts and once again introduces inconsistencies in the final product. Several methods for addressing this problem have been conceived which in general involve bringing the multiple secondary windings out of the core separately with multiple terminations. These methods significantly reduce the wasted space within the core previously reserved for the secondary tab solder connections, an important advantage for miniature power transformers. Once outside of

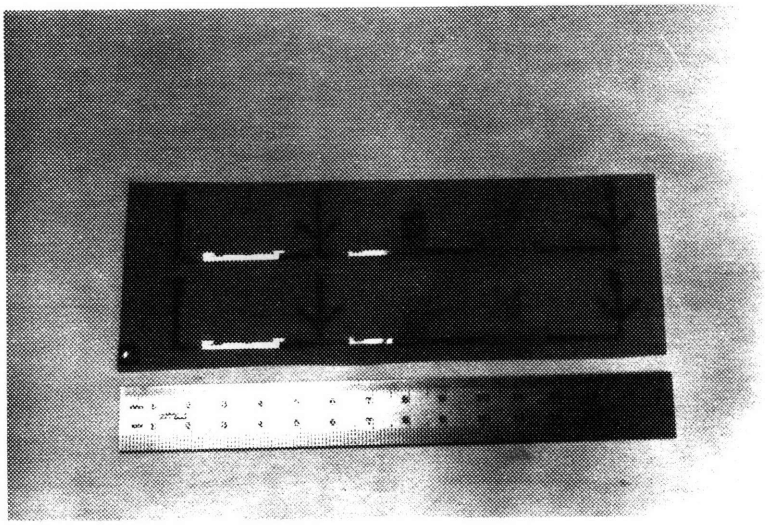


Figure 4.10: Etched FLEX Barrel Windings

the core, the terminations can either be joined together as before, or connected to multiple output rectifiers. The latter approach further reduces the inductance of the secondary loop by distributing the current path over a wider loop width.

Finally, the intrinsic height of transformers made using vertically-oriented parallel conductors is a serious impediment to further increases in power density. Because the thickness of the planar conductors is limited to a skin depth (to reduce proximity effect losses), low resistance windings require significant conductor width, which translates directly into transformer height. In contrast, the horizontally-oriented planar conductors of spiral windings tend to yield transformers with lower profiles, trading height for width to achieve low winding resistance. In most cases, such a reduction in height is preferable in order to reduce the overall height of the converter. Spirally-wound parallel planar conductor transformers were therefore investigated as a low-profile alternative to barrel windings.

4.3.2 Spiral Windings

The most convenient way to manufacture such spiral windings was to use the same FLEX material in conjunction with high resolution photo-lithography. Thus, following the same procedure used for the barrel windings, mask sets for a spiral winding were fabricated[4]. A

[4]much of the work on spiral windings was performed by Mr. David Richards as a related part of the 10 MHz Project.

6-turn primary was patterned on one side of the FLEX, with a single-turn secondary on the other side, as shown in Fig. 4.11. Note that the core is the same size as for the barrel wound transformer, i.e. 1.1 cm in diameter. Several versions were produced, and the results of electrical tests are summarized in Section 4.4.

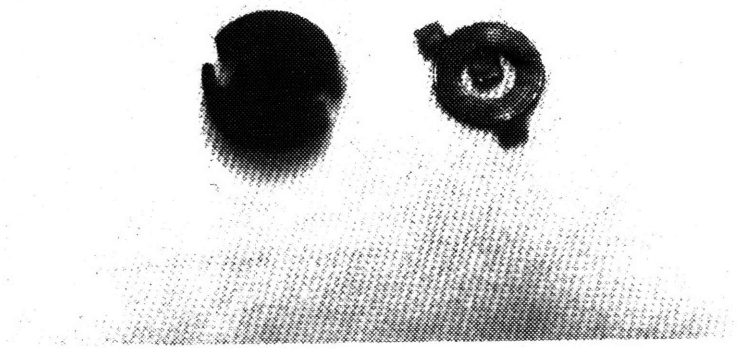


Figure 4.11: Spiral Winding on FLEX Material

There were a number of problems with this simple approach. To begin with, there was no convenient method for establishing a connection to the primary tap location. In addition, there was no mechanism for making the equivalent of a plated-through hole; thus the winding terminations had to be taken out side-by-side rather than on top of each other. This increased the secondary leakage inductance significantly, and complicated the transformer interconnection scheme. Furthermore, it was difficult to establish the necessary spacing resolution (1 mil) with the 1 oz. copper thickness (1.4 mils), as the aspect ratio of the etched slot was too great. Various solutions to these problems were tried, including hole punching and electroless plating, etching followed by electroplating, and the sandwiching of several layers of patterned FLEX spirals. In general, the results were unsatisfactory, prompting the investigation of alternative approaches for manufacturing planar spiral windings.

Thick and Thin Film Conductors

Thick and thin film construction were both considered as alternatives, the former due to its compatibility with the rest of the construction process, and the latter due to its greater resolution and multilayering capabilities. Thick film conductors have recieved considerable attention recently as a transformer winding alternative that would be compatible with hybrid power conversion [13]. Unfortunately, the relatively poor resolution of the thick film process requires that the conductors of a 6-turn transformer primary be built vertically as well as spirally (e.g. in two series-connected layers of three turns each), as shown in Fig. 4.12 [15]. The techniques for fabricating such multi-layer spirals, and in particular the process of creating interconnection vias between winding layers, have not yet been sufficiently developed. Another important problem stems from the size of the underlying ceramic substrate, which is too thick to place in the gap of a high permeability core material. Attempts to use fireable thick film magnetic materials beneath the thick film conductors, or to fire the conductors directly over magnetic materials, have so far proved less satisfactory in high power applications than the previously described barrel winding approaches.

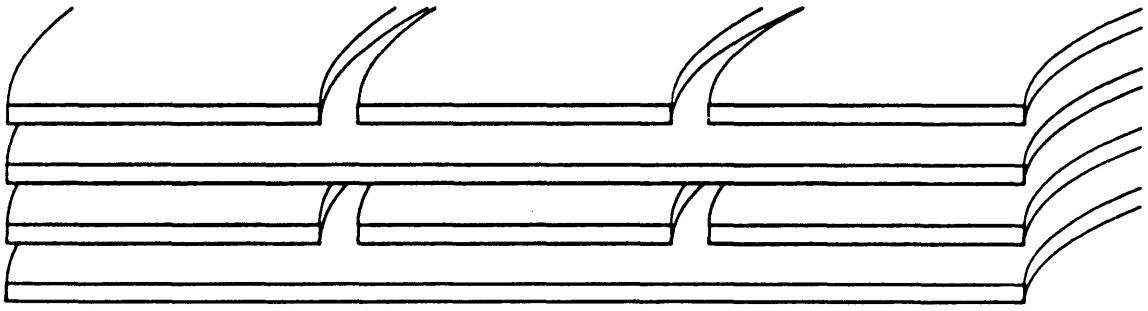


Figure 4.12: Multilayer Interleaved Spiral Winding Construction

Thin film fabrication techniques are perhaps the most promising in that they provide a high resolution, multilayer conductor interconnection medium with stable, reproduceable parasitics. The main problems with the approach seem to stem from the length and complexity of the fabrication process, which for an interleaved, tapped, 7:1 turn multilayer structure presently takes 60–80 hours (more time than is required for fabrication of the thick film substrates). Further work remains to be done in this area, however, before conclusive

results can be stated.

4.4 Tapped, Interleaved, Barrel-Wound Transformer Implementation

Based upon the results of experimentation with both types of windings, a final transformer design incorporating barrel-wound parallel-planar conductors was produced. The windings were etched and wound, and the transformers were constructed and characterized. The transformers were then incorporated into the final prototype hybrid converters.

4.4.1 Final Transformer Design

The mask set for producing the windings for the tapped, interleaved, transformer is reproduced in Fig. 4.13. This is a double mask, i.e., two transformer windings can be produced simultaneously from a single double-sided exposure. Furthermore, the mask set can be used to fabricate either full- or half-height transformers, by including or removing the extra winding widths along the bottom of each trace.

The resultant winding structure, following winding fabrication and assembly, is shown schematically in Fig. 4.14. Note that this is a half-height transformer, i.e., only the bottom half of the potcore was used in order to reduce the profile of the transformer (and hence the overall size of the converter). The upper core cover was made by sanding down a second, inverted potcore of the same type.

In accordance with the design parameters of Section 4.1, the turns ratio N_p:N_s was 7:1 and the magnetizing inductance was set at $L_{mag} = 2.5\mu$H. Maximizing the width of the copper traces within the confines of the core dimensions, the primary and secondary resistances of the design were calculated to be $R_{pri} = 60m\Omega$ and $R_{sec} = 3.15m\Omega$.

The transformer's leakage inductance was estimated using the methods of Section 4.2 during the design process. In particular, the field model techniques were used to evaluate the tradeoff between the decrease in leakage inductance and secondary resistance that is obtained with additional interleaves and the increase in manufacturing complexity that results. The effect that changing from full-height transformer cores to half-height ones had on the leakage inductance and winding resistance was also determined. These evaluations led to the adoption of the triple-interleaved, half-height secondary shown previously in Fig. 4.14. A more accurate leakage inductance calculation, taking into account the interwinding spacing,

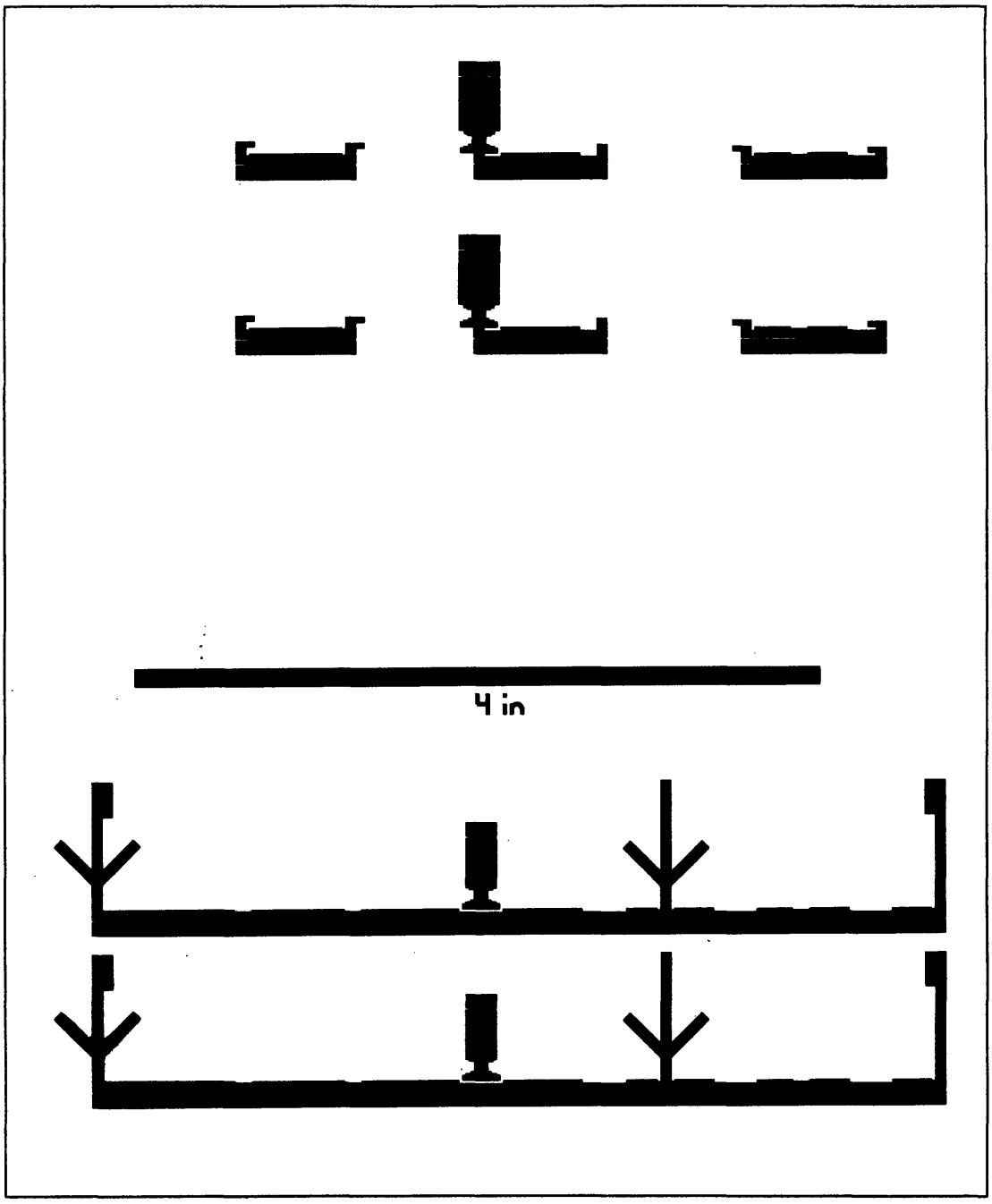


Figure 4.13: Final FLEX Barrel Winding Masks

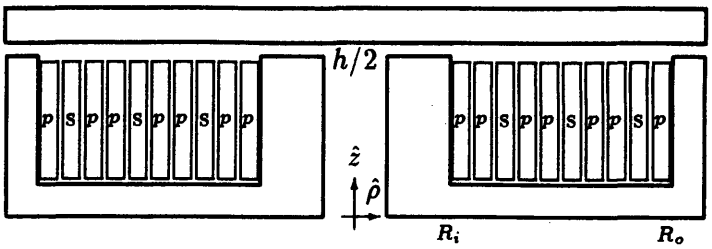


Figure 4.14: Cross-Sectional View of Transformer Showing Interleaved Windings

was then performed.

A detailed field profile of the interleaved winding configuration is shown in Fig. 4.15, where $B_o = 2\mu_o I_p/h$. The figure portrays the fields as changing linearly within conductors and remaining constant between them, which is a valid approximation when the conductors' thicknesses are equal to their skin depth.

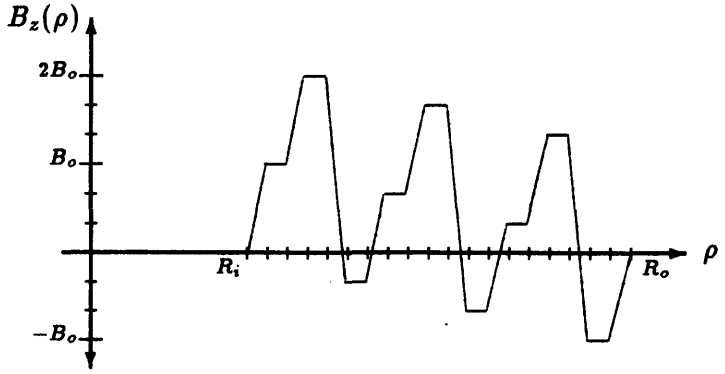


Figure 4.15: H-Field Strength in Winding Area

Using the techniques of Section 4.2, and recognizing that the volume integral of the square of a *constant* magnitude is simply the squared magnitude times the volume, the leakage inductance is found to be

$$\begin{aligned} L_{leak,final} &= \frac{2\pi h/2}{I_{pri}^2 \mu_o}\left[\frac{\mu_o I_{pri}}{h}\left(\frac{R_o - R_i}{19}\right)\right]^2 \left\{\left(\frac{R_o + R_i}{R_o - R_i}\right)\frac{6480}{5}\right\} \\ &\approx \frac{\mu_o \pi (R_o - R_i)(R_o + R_i)}{h/2}\frac{9}{5} = 30nH \end{aligned} \tag{4.28}$$

The corresponding dimensions of the winding pattern and potcore (Ferroxcube #1107-4C4) were $h/2 = 1.5$ mm, $R_o = 3.4$ mm, and $R_i = 2.3$ mm. The internal leakage inductance of the transformer was thus 30 nH, or 0.6 nH referred to the secondary. This parallel planar conductor design therefore has significantly less leakage inductance than a comparable

bifilar-wound transformer, and easily meets the leakage inductance requirements derived in Section 4.1.

4.4.2 Secondary Termination Design

In addition to minimizing the internal leakage inductance of the transformer, the winding design must also provide an equally low inductance secondary termination and component interconnection mechanism. Otherwise, the inductance of the secondary loop interconnections, which appears in series with the transformer's internal inductance, will negate any reductions in inductance afforded by the transformer design. The FLEX material is an ideal medium for performing this interconnection function, being totally compatible with the FLEX barrel winding process. By bringing the two secondary leads out of the transformer on opposite sides of the FLEX, the added inductance of this critical section is reduced to the order of fractions of a nanoHenry per square. Furthermore, it is possible to incorporate this termination into the winding mask, creating a single winding-interconnect unit and further reducing the effective leakage inductance. This integrated termination is visible in Figs. 4.9 and 4.13 as the large rectangular tab extending from the left end of the middle secondary winding and from near the center of the primary winding. Finally, the ductility of this termination helps relieve stresses in the secondary loop caused by thermal expansion mismatches between the transformer, rectifier, and capacitor materials.

A schematic view of the termination, showing the connection to the output rectifier and filter capacitors, appears in Fig. 4.16. Notice that the bottom copper layer of the FLEX termination is soldered directly onto the top (anode) of the Schottky output rectifier, producing the lowest inductance connection possible. The top copper layer is soldered to one end of the ceramic output filter capacitors; their other end is connected to a metallization on the hybrid surface. This metallization in turn completes the secondary loop, returning directly underneath the capacitors to the bottom (cathode) of the output rectifier.

The total inductance of this secondary loop can be estimated by dividing the loop into three sections, and then considering the fields in each portion. For the section consisting of the FLEX between the transformer and the rectifier, the dimensions of the FLEX are approximately 4 mm wide and 5 mm long, with a conductor separation of 0.075 mm. For a solenoidal field, the inductance of this portion is a small 120 pH.

The inductance of the rectifier and capacitor can be solved in a similar manner, by

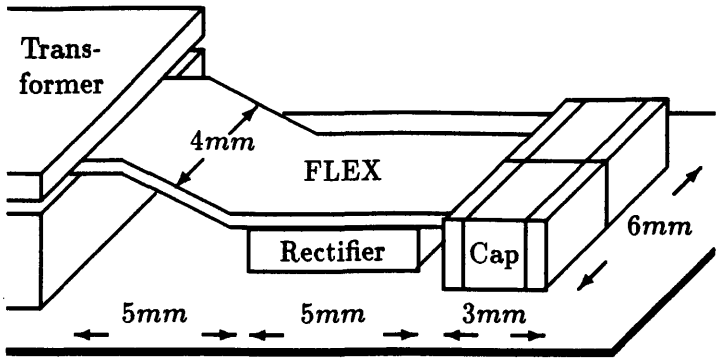


Figure 4.16: Low Inductance Secondary Interconnect

noting that their respective widths are 4 mm and 6 mm, and their lengths are 5 mm and 3 mm; their heights are 1.5 mm and 2 mm, respectively. Several assumptions are made concerning the current flow paths and the resultant fields. First, the magnetic field within the loop area is approximated as solenoidal because the width of the conductors (4–6 mm) is large compared to their separation (1.5–2 mm). Additionally, it is assumed that the rectifier's vertically directed current is distributed evenly across the die, and that the capacitors horizontally-directed current is distributed uniformly down its height. Then, using the expression for the inductance of a solenoid ($L = \mu_o A/l$) yields

$$\begin{aligned} L_{loop} &= L_{FLEX} + L_{rect} + L_{cap} \\ &= 0.12nH + \frac{\mu_o(5mm \times 1.5mm)}{3 \times 4mm} + \frac{\mu_o(3mm \times 2mm)}{3 \times 6mm} \\ &= 0.12nH + 0.8nH + 0.4nH \\ &= 1.32nH \end{aligned} \tag{4.29}$$

Note that the factor of three in the denominator of the latter two expressions in (4.25) is due to the linear decrease in magnetic field across the rectifier (from left to right) and down the capacitor. These decreasing field profiles reduce the effective inductance of the latter two geometries by a factor of three from the comparable constant-field situations.

The resultant secondary loop inductance, only 1.3 nH, is significantly lower than can be achieved with standard transformer designs and PCB construction. Combined with the internal leakage inductance of the transformers themselves, the total parasitic inductance of the design was approximately 2 nH, well below the value required for satisfactory performance of the DRFC.

4.4.3 Experimental Design Verification

Transformers were built according to these design specifications, using the previously outlined techniques. The windings were laid out on a CAD system to 10 mil resolution, photoplotted at 2 times magnification, and then reduced photographically to produce the full size negatives. Both sides of the photosensitive FLEX material (available from Universal Images, Inc.) were exposed simultaneously as a double-sided contact print for approximately 45 min under high-intensity ultra-violet light sources. This simultaneous masking technique assured proper alignment between the primary and secondary windings. Following exposure, the FLEX was then soaked in a Risolve (a 3M Co. product) photodeveloper solution for 3–4 min and the exposed resist was rinsed off in warm water.

The FLEX was dried and the copper etched using standard PCB copper etchants ($FeCl_3$) in a warm spray bath for 2 min. The extra polyimid was trimmed from the windings manually with a razor blade, and the secondaries were coated with a thin layer of insulation (0.8 mil thick polyester tape, Scotch-3M #74). The FLEX winding was wound *tightly* around a steel shaft coil form and the outer winding end was taped down, creating a single-piece winding structure. The secondary tabs were positioned and soldered appropriately onto the secondary termination, and the finished winding was then removed from the coil form and installed in the bottom potcore half (nickel-zinc core material, 11 mm diameter by 3.5 mm high, Ferroxcube #1107-A40-4C4). The top core slab was made from an inverted core half (Ferroxcube #1107-PL00-4C4). The gapped core structure was adjusted using additional tape inserted between the core halves (2.2 mil thick polyester tape, Scotch-3M #56).

Following the construction of the transformers, electrical measurements were made to confirm the validity of the designs. Specifically, the leakage inductance, magnetizing inductance, and resistance of the transformers were measured using a Hewlett Packard #4192 impedance analyzer with a rated bandwidth of 5 Hz–13 MHz. All measurements were made at a 5 MHz signal frequency. Measurements were made on a number of design constructions in addition to the final design construction outlined above, including foil and FLEX winding materials and both barrel and spiral winding geometries. While these results were used to confirm the measurement techniques and to compare the various construction approaches, only measurements from the final design are discussed in the following paragraphs.

The magnetizing inductance measurements were found to correlate well with expected

results, and exhibited good matching between components. For instance, the measured magnetizing inductances were typically 3-5% lower than predicted, an expected deviation which was due to incomplete packing of the winding volume. Furthermore, matching of the magnetizing inductances between components was typically better than $\pm 3\%$ for the final 7:1 FLEX barrel windings, improving to better than $\pm 1\%$ when the identical core sections were used with each winding. Such deviations were well within the tolerance of the DRFC, in terms of setting and matching the resonant frequencies of the complementary converter halves. Winding resistance exhibited similar agreement with the design parameters, and comparable matching between components.

Leakage inductance measurements were made with the secondary shorted at the far side of the secondary termination. The inductance of the termination strip was therefore included in the parasitic estimates. From (4.28), the predicted internal leakage inductance of the transformer was 0.6 nH; from (4.29), the additional termination inductance was 0.12 nH. The total expected leakage inductance of the transformer/termination is therefore 0.72 nH, or 35.3 nH on the primary side. The measured leakage inductances were consistently in the range of 38 nH–40 nH, well within the modelling error. Furthermore, one would expect the actual leakage inductance to be slightly higher, as the model fails to account fully for the additional inductance introduced by the internal secondary tabs. Equally as significant as the agreement between the design model and the measured performance was the *matching* between leakage inductances. This matching, better than 5%, clearly indicated the advantages of the FLEX winding approach over the original foil construction.

4.5 Summary of Transformer Construction Results

Based upon the preceding analysis, the half-height, barrel-wound, interleaved FLEX transformers were judged to be the best design for the DRFC, and were used in the construction and testing of the final prototype circuits. The salient physical and electrical characteristics of the representative construction types are summarized in Table 4.1. Two barrel and one spiral-wound constructions are included, and all numerical entries are measured results (as opposed to design predictions).

The important results can be summarized as follows. First, parallel planar conductors were found to be the only satisfactory shape for the construction of transformers meeting the numerous simultaneous constraints imposed by the DRFC topology. In particular, the

Parameter	Barrel		Spiral	units
Winding Type	Foil	FLEX	FLEX	
Turns Ratio	7:1	7:1	6:1	N_p:N_s
Interleaving	4	6	1	# Partitions
L_{mag}	2.68	2.54	3.4	μH
Core Height	0.26	0.175	0.175	in
L_{leak}	55	38.5	44	nH
R_{pri}	40	60	260	$m\Omega$
R_{sec}	1.7	3.2	7.2	$m\Omega$

Table 4.1: Summary of Transformer Parameters

low leakage inductance and low winding resistance specifications could not be met with traditional bifilar winding construction techniques, within the given volume constraints. Furthermore, it was shown that some method for interleaving layers of such parallel planar conductors was required.

Two winding orientations, the spiral and the barrel, were therefore investigated in the context of parallel planar conductors. FLEX, a copper/polyimid/copper laminate for making flexible printed circuit boards, was discovered to be an ideal medium for creating the barrel windings. It provided a mechanised method for producing consistent windings using photo-lithographic techniques, and at the same time provided a convenient, integral, low-inductance secondary termination. Furthermore, it provided a means for interleaving a limited number of conductor layers, significantly reducing the internal transformer leakage inductance and making it possible to meet the design requirements for the DRFC transformers.

Finally, no satisfactory method for constructing the spiral windings was devised. Windings using the FLEX material failed to provide the necessary copper volume, resulting in high-resistance windings. Multiple-layer interleaved structures made using thick or thin film technologies were similarly unsatisfactory, so far. However, the inherently low leakage inductance between parallel planar conductors in a spiral winding orientation continues to make it an attractive alternative. In fact, single-unit spiral windings, to be created using some mass-production method, continue to offer the greatest potential for future advances in the construction of transformers suitable for high frequency power conversion.

Chapter 5

Hybrid Prototype Construction

As explained in the introductory chapter, one of the main goals of this thesis was the development of assembly techniques which would enable the construction and eventual mass-production of dc-dc converters with high power conversion densities. These converters could then serve as POL converters in a distributed power supply system. The DRFC topology was introduced in Chapter 2 as an ideal candidate for such POL conversion applications, provided that the unwanted parasitics could be controlled during fabrication and assembly of the converter. Chapter 3 described a general construction approach, specifically the processing and fabrication of multilayer hybrid circuits using copper thick film conductors, which can aid in the control of the dominant interconnection parasitics. Finally, the minimization of parasitic leakage inductances in the transformer and in the secondary interconnection and rectification loops was described in Chapter 4.

This chapter demonstrates the application of these results to the construction of a prototype hybrid converter. Generation of the control and gate drive signals for the DRFC topology are first described, and the specific components used in the construction are discussed. The next section then presents a layout of the hybrid, focussing on the critical loops where every effort is made to minimize parasitic inductances. A thermal analysis of the converter is presented in Section 5.4, to determine the appropriate construction approach. Finally, the last section details the specific processing parameters, equipment, and materials used to fabricate this prototype.

5.1 Circuit Description

The prototype DRFC was constructed to run open loop, deriving the PWM control for the pre-regulator stage from an external clock drive signal. There were several reasons for

the selection of this mode of operation: 1) The extremely high operating frequency of the DRFC precluded the use of integrated circuit closed-loop control. While efforts have been made to develop high frequency integrated circuits which combine feedback control and gate drive capabilities [19], presently available commercial circuits are not yet capable of operating in the megaHertz range. 2) The implementation of a control circuit based upon discrete components was not a reasonable approach in light of the power density goals of a POL converter. 3) The intrinsically low output impedance of the DRFC topology permitted open loop operation without serious degradation in performance. Because of these reasons, the PWM signal was generated externally and the duty cycle was adjusted manually. The complementary clock signals for the dual converters were externally generated as well, and all of these control inputs were coupled through I/O pin connectors.

5.1.1 Power Train Hybrid

The original PCB prototypes of the DRFC built by Casey [19] included only the power train components themselves (the power semiconductors, transformers, and energy storage elements) on the board assembly. In particular, the gate drive circuitry for controlling the power MOSFET switches was mounted externally to form a 3-dimensional layered structure. One such PCB prototype is shown in Fig. 5.1. Some components, including the power MOSFET switches, were mounted on the backside of the PCB. This helped the prototype to achieve its high construction density while reducing the inductive parasitics.

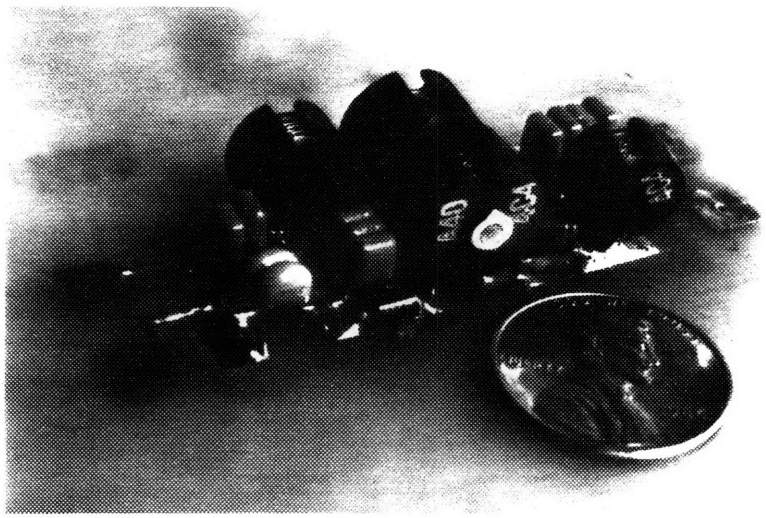


Figure 5.1: PCB Prototype Version of the DRFC

Difficulties encountered in the cooling of this structure were one of the problems which originally prompted the investigation of hybrid construction. In addition to addressing thermal concerns, hybridization facilitated the inclusion of integrated circuit gate drivers directly on the power train substrate in the close proximity to their respective MOSFETs. This inclusion, in combination with careful layout of the thick film interconnections and the use of multiple wire bonding, significantly reduced the parasitic inductances of the gate drive loops.

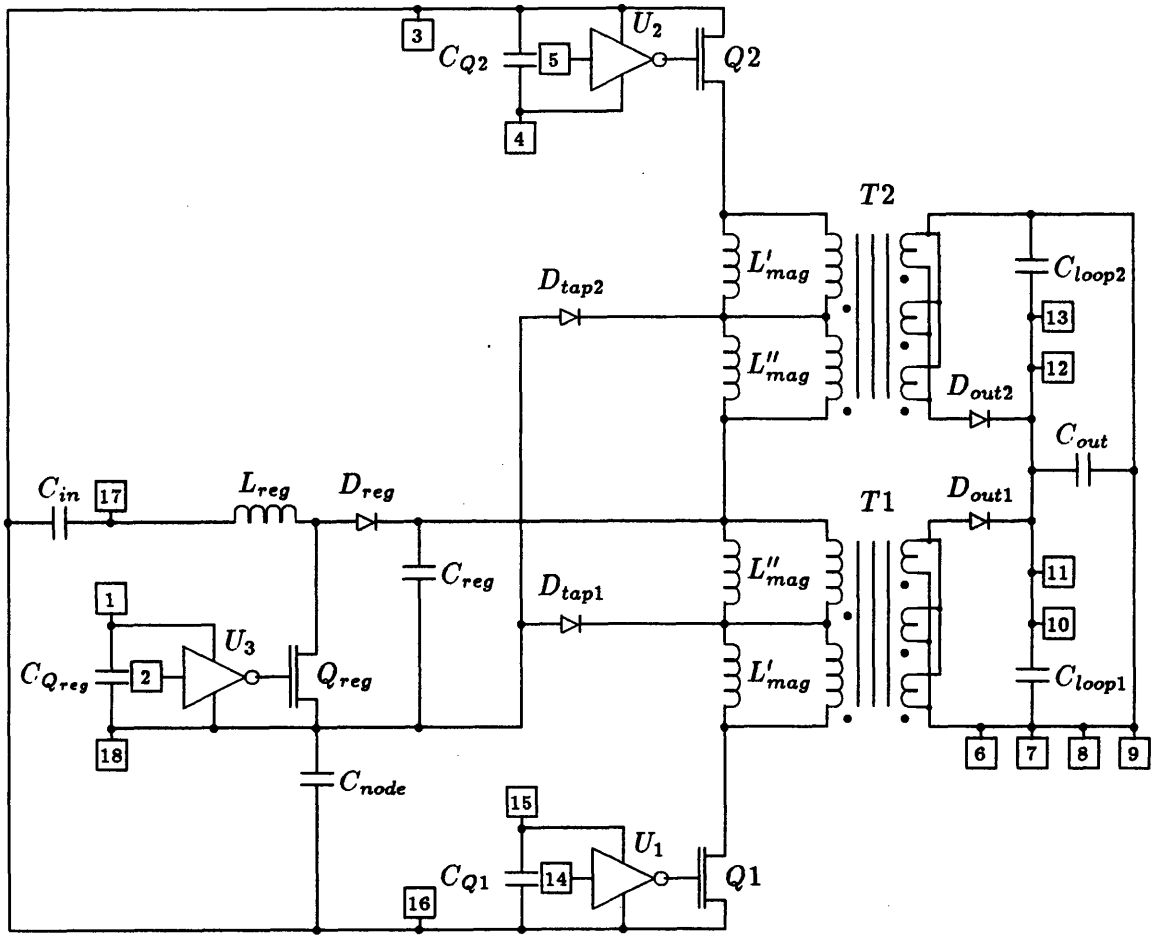


Figure 5.2: DRFC Hybrid Prototype: Power Train

The DRFC prototype topology, complete with these gate drive components, is shown in Fig. 5.2. The boxed numbers (1–18) correspond to the I/O pins of the hybrid assembly. Four pins were paralleled for each of the $5V$ output lines on the secondary side, to minimize resistive drops at full load ($10A$). Three pins were used for each of the gate drive chips,

to minimize cross-coupling between the high frequency clock signals and the large gate currents.

Components were selected in accordance with the criteria established in Chapter 3, and are listed in Table 5.1. The energy storage capacitors on the output, labelled C_{out}, were high capacitance tantalum chip capacitors. The remaining capacitors were 100nF X7R type ceramic chips, selected for their low ESR and low ESL. These were the largest-value ceramic chip capacitors available in this low-inductance package outline (#1210 125x95x65 mils), so multiple capacitors were parallelled to achieve the larger capacitances in critical AC current paths. For instance, each of the secondary rectifier loop capacitors C_{loop1} and C_{loop2} were composed of 4 ceramic chips placed side-by-side to lower the loop inductances and carry the large AC charging currents.

Component	Value	Description	Manufacturer
C_{Q1}	100nF	500S41W-104KP, 50V	Johanson
C_{Q2}	100nF	500S41W-104KP, 50V	Dielectric
$C_{Q_{reg}}$	200nF	2 x 500S41W-104KP, 50V	
C_{in}	600nF	6 x 500S41W-104KP, 50V	
C_{reg}	500nF	5 x 500S41W-104KP, 50V	
C_{node}	200nF	2 x 500S41W-104KP, 50V	
C_{loop1}	400nF	4 x 500S41W-104KP, 50V	
C_{loop2}	400nF	4 x 500S41W-104KP, 50V	
C_{out}	6.6μF	3 x 195D-225X0010B2, 10V	
$T1$	7/5:1	see text	
$T2$	7/5:1	see text	
$Q1$	HEX-3	IRF230, 200V, 400mΩ	International
$Q2$	HEX-3	IRF230, 200V, 400mΩ	Rectifier
Q_{reg}	HEX-3	IRF130, 100V, 160mΩ	
U_1	DS0026	gate drive IC	National
U_2	DS0026	gate drive IC	Semiconductor
U_3	DS0026	gate drive IC	
D_{tap1}	50 mil	SXS-50L-60, 60V schottky	Semetex
D_{tap2}	50 mil	SXS-50L-60, 60V schottky	
D_{reg}	90 mil	2-B process 30V schottky	International
D_{out1}	120 mil	2-B process 30V schottky	Rectifier
D_{out2}	120 mil	2-B process 30V schottky	

Table 5.1: DRFC Hybrid Prototype Parts List

Bypass capacitors were included near each of the gate drive ICs, with sizing based upon the gate charge required for switching the power MOSFETs. The series capacitance of the

primary-side bus capacitors C_{reg} and C_{node} was made as large as space would permit, to provide output hold-up for load transients. Their relative magnitudes were set according to the requirement that their voltage ratio match the primary winding tap ratio of the 7/5:1 transformers. Their 5:2 ratio insured that the top bus inputs and the tap inputs to the transformer would supply fixed proportions of the total output power under both steady-state and transient conditions.

The magnetics were custom made for each converter prototype. The transformers were described in detail in Chapter 4, with a summary of the electrical parameters being given in Table 4.1 and the necessary materials being listed in Section 4.4. The pre-regulator inductor was required to have low DC resistance to minimize losses, and to have minimal current ripple at switching frequencies in the 1–3 MHz range. These constraints gave a DC resistance of $100m\Omega$ and an inductance of 15μH. Construction of the input filter inductor L_{reg} was straightforward, although bobbin-wound construction was precluded by size constraints. The inductor was instead fabricated by winding 19.5 turns of #30 AWG magnet wire around a custom-made brass coil form. The wire was coated with low-loss polystyrene 'Q-Dope', a coil-forming adhesive cement, creating a solid winding structure which was then removed from the form and inserted into the magnetic core. This core was made using the same half-potcore construction as the transformers, but with smaller core halves (NiZn ferrite material, 9 mm diameter by 2.5 mm height, Ferroxcube 905-PA25-4C4). Again, the cover slab was made from a mating ungapped, inverted core half (Ferroxcube 905-PL00-4C4). Measured characteristics of the inductor were 110mΩ resistance and 14.7μH inductance.

The active devices were chosen from the severely limited number of discrete semiconductor components that were available in dice form. The main switching MOSFETs $Q1$ and $Q2$ were selected for their 200 V reverse breakdown voltage, and then for their 400 mΩ on-state resistance. The parasitic output capacitance of these HEX-3 dice, nominally 250 pF at 25 V, was extremely high, but no smaller dice with the required breakdown voltage and on-state resistance were available. Similarly, the pre-regulator MOSFET was required to meet the maximum permissable on-state resistance criterion of 200 mΩ, but required a reverse breakdown capability of only 20 V. At the time of construction, the resistance parameter could only be met by an over-rated 160 mΩ, 100 V device, as no lower-voltage devices with sufficient on-state conductivity were available in dice form. This shortage prompted

the selection of another HEX-3 die despite the resultant increase in capacitive switching losses. These active devices were supplied with back-side metallizations of Ti-Ni-Ag and with aluminum bonding pads.

Selection of the schottky rectifiers was less restricted, and appropriate sizes were eventually located. They were picked to meet the reverse voltage rating, and then to minimize conduction losses without introducing excessive junction capacitance. The 30 V rectifiers used in the pre-regulator stage (D_{reg}) and the output stage (D_{out1} and D_{out2}) were experimental products under development at a commercial semiconductor manufacturer. The goal was to produce high-speed rectifiers for power conversion applications which had extremely low forward conduction losses. Their forward drop, only 0.35 V at 10 A for a $(125\text{ mil})^2$ die, was achieved by using high-conductivity substrate materials and by relaxing the reverse leakage current constraints. Preliminary data on these developmental schottky process components are given in Appendix III. The bottom metallizations of all these rectifiers were solderable, as were the top metallizations of the 125 mil output schottkies. The smaller 60 mil and 90 mil dice had aluminum surfaces which were suitable for wire bonding.

The gate drive IC chips are industry standard bipolar-technology inverters with high current outputs (National Semiconductor DS0026). Each die has two separate inverters with common supply connections. One IC was used to drive each MOSFET gate, with the dual inputs and outputs on each die wire-bonded in parallel. This effectively doubled their switching speeds, which were generally limited by the large currents necessary to charge and discharge the input capacitances of the HEX-3 dice rather than internal inverter dynamics. The dual inverter gate drive dice were supplied without any backside metallization because wire bond pads were provided for the substrate (ground) connection and hence no electrical substrate connection was required.

5.1.2 External Clock and PWM Board

The 18 I/O pins on the hybrid were designed to plug into a PCB in a manner totally analogous to a 40-pin DIP, with the hybrid being inverted to expose the backside heatsink. The input and output power and all gate drive and PWM control signals accessed the hybrid from a socket on the PCB. Surrounding this socket were the various clock signal inputs to the gate drive circuits. This circuitry and the hybrid connector are shown in Fig. 5.3. The hybrid I/O pins are numbered from 1 to 18 in a counter-clockwise direction starting in the

top right corner.

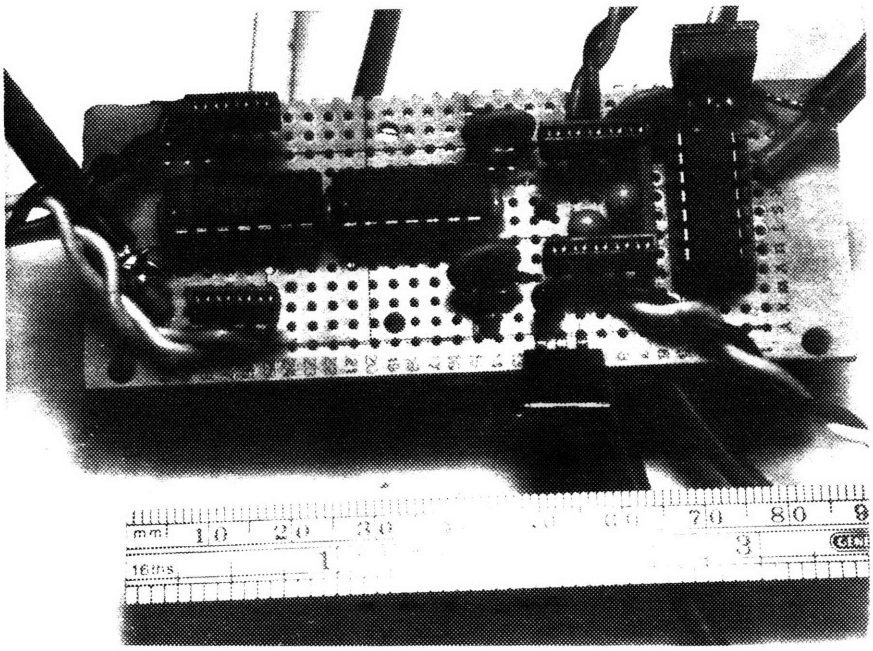


Figure 5.3: DRFC Hybrid Prototype: External Clock and PWM Board

The clock and PWM signals were generated by standard bench top function generators, and buffered by high speed TTL logic gates. The complementary, 50% duty cycle clock signals were synthesized from a 10 MHz square wave produced by an Tektronix Model FG-504 40 MHz function generator. This square wave was divided using a 74S74 dual flip-flop to produce the 5 MHz square wave with an exact 50% duty cycle, as shown in Fig. 5.4. The output from the flip-flop was sent through a series of AS-logic inverters which helped increase the level transition speeds and sourced the 10 mA currents required by the level-shifting DS0026 input stages. In addition, they provided the complementary clock phases that are required for balanced dual converter operation. The Q and $\overline{Q}$ outputs of the flip-flops could not be used to create these signals because the propagation delay through the gates produced a large timing skew between the output transitions.

The inverter strings produced complementary outputs with no more than 3 ns skew, or 1.5% of the switching period. Furthermore, their high-speed output stages gave loaded rise times of 2.5 ns (measured at the hybrid I/O pins). These gate drive signals were capacitively coupled ($C_{c1} = C_{c2} = 2$ nF) to the gate drive circuit input pins on the hybrid.

The variable duty cycle square wave for the pre-regulator MOSFET was generated in a similar manner, using a 20 MHz Hewlett Packard Pulse/Function Generator #8111A with

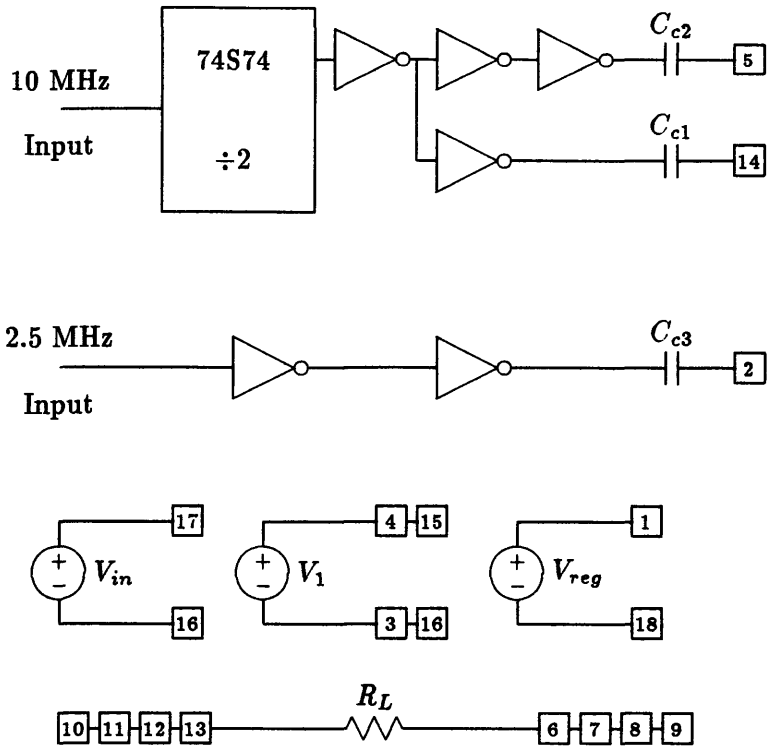


Figure 5.4: External PCB Support Circuitry

a continuously variable duty cycle output. This generator, running at 2.5 MHz (selected to be half the dual converter clock speed), in turn drove a similar string of AS-logic inverters to produce clean waveforms with rapid transitions. This signal was again capacitively coupled (C_{c3}=4nF) to the pre-regulator gate drive input.

The external PCB control board also provided the power connections between the hybrid converter and the outside world. The DC input and output lines to and from the hybrid converter run through the PCB just as they would in a normal POL configuration, permitting the hybrid converter to be treated as a generic plug-in with no additional wiring or special attachment efforts required for installation. The bias supplies for the gate drive ICs were connected to the hybrid via additional I/O pins on the external control board.

5.2 Hybrid Layout

The layout of the DRFC topology is particularly critical because the presence of layout parasitics detracts greatly from the performance of the converter. Indeed, it was the desire to reduce or eliminate these parasitics that originally prompted the investigation of hybrid

construction. The layouts for each layer were therefore done manually, as opposed to using an auto-placement or auto-routing CAD system, to insure 'optimal' interconnections.

Placement of the components was done with hand assembly and instrumentation requirements in mind. In particular, the capacitors were spaced well apart to facilitate soldering access, and space for the measurement test points and node contacts was allotted. This significantly reduced the component density of the hybrid but was necessary to produce the prototype versions. Layouts for commercial versions of the identical circuit which would likely waive such reworkability or instrumentation requirements could therefore be expected to achieve 20–30% higher packing densities with the same two-metal-layer construction technology.

As with any power circuit, conductor resistance was a prime concern. The maximum conductor thickness was fixed by the thick film process at 1.1 mils, giving an $R_{\square}$ of $1.0m\Omega$. Furthermore, in most cases the parasitic inductance of the interconnections was the other concern, rather than the capacitance. This inductance was fixed by a dielectric thickness of 1.9 mils to be $L_{\square} = 60$ pH. The hybrid was therefore laid out to maximize the trace widths, and to place the signal paths over ground planes whenever possible. The MOSFET drain connections were one important exception to this approach, as the following sections explain. Complete layout drawings of the various thick film layer masks are given in Appendix D. Detailed descriptions of two critical layout subsections are presented in the following subsections.

5.2.1 Secondary Terminations

The secondary rectification loop is perhaps the most critical construction area for the DRFC topology. The FLEX transformer termination was explained in Section 4.4, and a pictorial schematic of the resultant structure was shown in Fig. 4.14. The final prototype design called for increased loop capacitances C_{loop1} and C_{loop2} of 400 nF each, with each consisting of four 100 nF ceramic chip capacitors grouped tightly around *two* edges of the schottky rectifier dice. This layout configuration is shown in Fig. 5.5.

The secondary side of the converter consists of only four electrical nodes, as shown in the schematic of Fig. 5.2. The bottom conductor of the FLEX transformer secondary terminations were soldered directly to the anodes (top surfaces) of the schottky dice, leaving only two additional secondary-side nodes. These nodes, the $+5V$ and ground outputs of

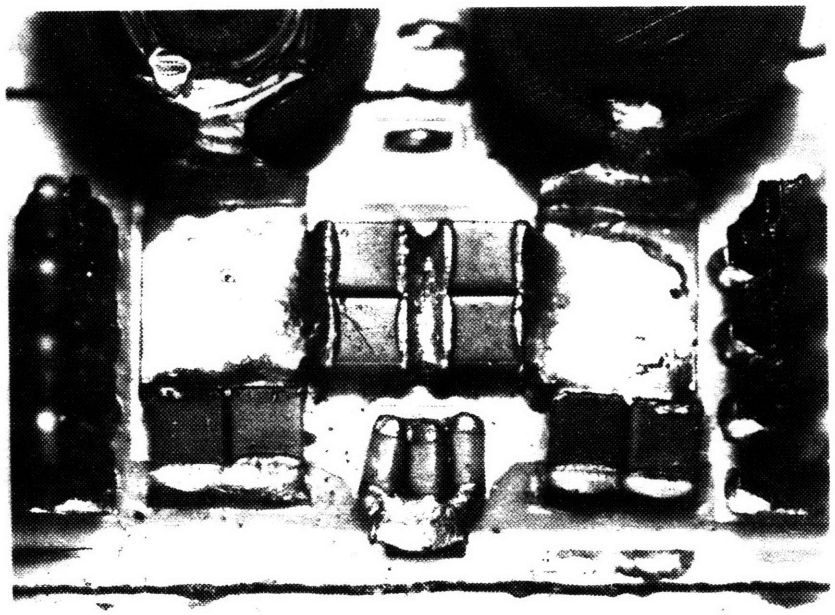


Figure 5.5: Layout of Secondary Loop Components

the converter, were fabricated from the first and second substrate metal layers respectively. This put the $+5V$ output node, which is an incremental ground in the DRFC topology, closest to the heatsink. Because the bottom metal layer on the primary side is both a dc and an incremental ground, capacitive coupling between the primary and secondary by way of the heatsink was minimized.

A side view of this structure is shown in Fig. 5.6. The cathode (bottom surface) of the output rectifier rests directly on the bottom metal layer, which extends underneath the entire secondary and in particular lies below the loop capacitors. The top conductor layer of the FLEX termination was soldered directly to the grounded ends of these loop capacitors, which were located closest to the rectifier, as shown. Finally, the opposite ends of these loop capacitors were connected to the underlying Metal 1 layer. The ac current flow path thus starts in the lower FLEX conductor, travels down through the rectifier and into the Metal 1 layer, and then across to the Via riser. From there, it continues up into the loop capacitors and finally returns to the transformer in the upper FLEX conductor.

It should be noted that this drawing is not to scale; in particular, the vertical distances separating the substrate thick film layers have been greatly exaggerated to show the interconnection detail, while the component sizes have been reduced. Because the true scale of

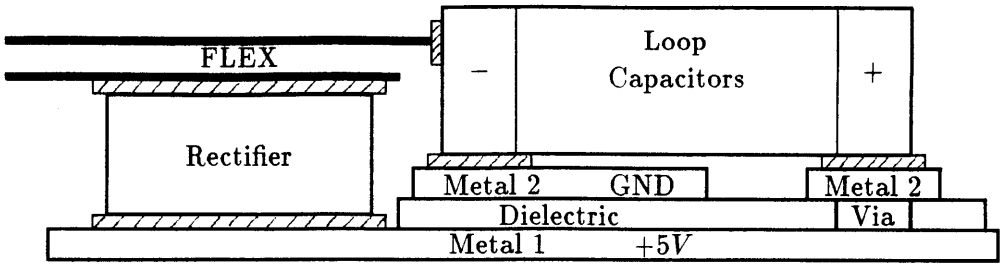


Figure 5.6: Side View of Secondary Loop Layout

the interconnection layers has a much greater depth (into the page) than height, the loop *area* of the previously described current path is much smaller than the path *width*. The inductance of the interconnection loop is therefore extremely small.

Using the techniques developed in Section 4.4, this inductance was calculated to be

$$\begin{aligned} L_{loop} &= L_{FLEX} + L_{rect} + L_{cap} \\ &= 0.12nH + \frac{\mu_o(120mils \times 20mils)}{3 \times 120mils} + \frac{1}{4}\frac{\mu_o(125mils \times 65mils)}{3 \times 90mils} \\ &= 0.12nH + 0.21nH + 0.24nH \\ &= 0.57nH \end{aligned} \tag{5.1}$$

where the one-fourth reduction factor on the capacitor inductance is due to the placement of four capacitors in parallel around each output rectifier. Combining these results with the secondary-referred transformer/FLEX leakage inductance of 0.79nH, the total effective leakage inductance of the transformer/secondary loop was calculated to be

$$\begin{aligned} L_{lk,eff} &= (L_{trans} + L_{FLEX}) + L_{rect} + L_{cap} \\ &= 0.79nH + 0.21nH + 0.24nH \\ &= 1.24nH \end{aligned} \tag{5.2}$$

The internal transformer leakage inductance thus accounts for approximately half of the total inductance, with the secondary component loop comprising the remainder.

5.2.2 MOSFET Connections

The DRFC MOSFETs also required great care in the interconnection layout. The layout of primary MOSFET switches $Q1$ and $Q2$ and pre-regulator switch Q_{reg} required the min-

imization of two critical inductances 1) in the gate drive loop and 2) in the drain-source loop.

Parasitic inductance in the gate drive loop slows down the switching transitions of the MOSFETs by limiting the peak di/dt that the drive circuitry can deliver to the gates (for a given supply voltage). This in turn increases switching losses in the pre-regulator stage and can even cause losses in $Q1$ and $Q2$ by preventing the gate drive circuitry from controlling the Miller effect (which can cause the channel to turn back on as the drain voltage rises).

Parasitic inductance in the drain source loop of the main switches $Q1$ and $Q2$ contributes directly to the apparent leakage inductance of the transformer, increasing load regulation and causing additional leakage energy losses. However, its effect is less severe than inductance in the secondary rectification loop because the transformer effectively reduces its magnitude by the square of the turns ratio. In the pre-regulator loop, this parasitic inductance contributes to turn-off transition switching losses.

To reduce these inductances and minimize their effects, careful consideration was given to the current flow paths and to techniques for minimizing their inductances. On a MOSFET die, the gate and source bonding pads are on top of the device at opposite ends, with the drain connection being a solderable metallization on the bottom surface. The gate drive loop thus includes the path from the substrate to the gate bonding pad, through the parasitic gate-source capacitance to the source bonding pad, and back to the substrate. To minimize the inductance of this path, the source connection was brought back underneath the die on the Metal 1 layer, closing the loop directly below the substrate gate connection. This interconnection approach is shown in Fig. 5.7. Again, the components and thick film dimensions have been scaled non-linearly in order to clarify the drawing.

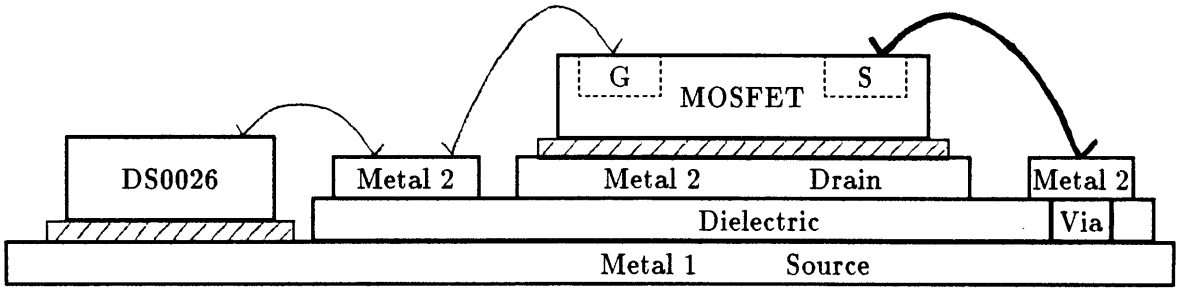


Figure 5.7: MOSFET Gate Drive Layout

Connecting the drain and source terminals of the MOSFET to different metal layers

also permitted exploitation of the inherently low interconnection inductance of hybrid construction. By placing the conductive traces on top of each other, underneath the MOSFET itself, the inductance of the *drain-source* loop is also reduced. Furthermore, by reducing the width of certain portions of the source metallization that run directly underneath the drain, the introduction of additional parasitic capacitance is minimized. This technique is clearly visible on the Metal 1 masks shown in Appendix D. Additional rectangles beneath the die sites on either side of the narrow source connection strips help keep the die bonding surface flat and simultaneously reduce the thermal impedance through the dielectric to the substrate.

Reduction of parasitic capacitance between the source and drain connections is important for both the main MOSFETs $Q1$ and $Q2$ and for the pre-regulator MOSFET Q_{reg}. In both cases, the presence of this parasitic capacitance degrades the converter's performance. In the case of the main switches, this capacitance slows down the resonant ring, which in turn reduces the switching frequency and power conversion density. Capacitance between the drain and source of the pre-regulator stage MOSFET contributes directly to switching losses, because the pre-regulator stage is a square wave converter.

Similar techniques were used throughout the converter to reduce interconnection inductances. Trace widths were maximized whenever capacitance was not a concern, and ac current loops were tightened by routing outgoing and return paths on different metal layers directly above each other.

5.3 Thermal Analysis

Concurrently with the circuit layout process, estimates of the thermal rise of each part were computed. These estimates helped insure proper thermal management of the semiconductor components during operation by preventing layout errors which might cause unnecessary thermal resistances. Specifically, the effect of separating the dice from the substrate by a thick film dielectric material with poor thermal conductivity was evaluated quantitatively and compared to the traditional approach of mounting the dice directly on the Metal 1 (bottom) interconnection layer. The estimates were also generalized to quantify the thermal advantages of solder die bonding over the use of adhesives.

This evaluation process was performed in three parts: 1) The resistance between each component and the heatsink was computed for the two cases of solder and adhesive at-

tachment. 2) Estimates of the nominal power dissipation of each component were made to determine their corresponding thermal outputs. 3) The thermal rise above ambient was computed as the product of the power dissipation times the thermal resistance. The following discussion describes these three steps in the context of the final prototype design.

5.3.1 Thermal Resistances

The thermal resistances separating the various components from the heatsink (which is assumed to be a thermal equipotential surface) can be computed from the thermal conductivities of the intervening materials. The thermal conductivities of these materials, as well as other materials commonly used in hybrid construction, are given in Table 5.2.

Thermal Conductivities of Selected Materials, in $W/^oK/cm$				
Pure Metals	Aluminum 2.37	Copper 3.98	Gold 3.15	Silver 4.29
Solder Metals	Cadmium 0.97	Indium 0.82	Lead 0.35	Tin 0.67
Solder Alloys	92.5Pb,5Sn,2.5Ag 0.25	70In,30Pb 0.38	50Sn,50Pb 0.46	63Sn,37Pb 0.66
Substrate Ceramics	Al_2O_3 0.3	AlN 1.3	BeO 2.3	SiC 2.7
Adhesive Compounds	Fired Ag-Glass Ablebond SG2001[1] 0.88	Epoxy Film Sta-Film 1400[1] 0.09	Ag Epoxy 979-1A[1] 0.017	Thermal Epoxy DeltaBond 154[2] 0.008
Thick Film Inks	Copper #9922 [3] 3.1	Dielectric #4575D [3] 0.01	Gold #5715 [3] 2.5	Dielectric #5704 [3] 0.018
key: [1]Ablestik Labs; [2]Wakefield; [3]Dupont				

Table 5.2: Thermal Conductivities of Selected Materials

Using the tabulated conductivities, the resistance of the ith layer of material under the jth component was computed using the formula

$$R_{j,i} = \frac{t_i}{\sigma_i A_j} \tag{5.3}$$

where t_i is the thickness of the ith layer, σ_i is the thermal conductivity of the layer, and A_j is the contact area of the jth component. The thermal spreading angle has been neglected by holding the thermal conduction area constant, permitting the independent solution of each component's temperature rise while making conservative design estimates. The to-

tal thermal resistance between the jth component and the heatsink is the sum of the N individual layer resistances

$$R_j = \sum_{i=1}^{N} R_{j,i} = \frac{1}{A_j}[\frac{t_1}{\sigma_1} + \frac{t_2}{\sigma_2} + \cdots + \frac{t_N}{\sigma_N}] \tag{5.4}$$

from which it is clear that the dominant resistances are due to the layers with the highest $(\frac{t}{\sigma})_i$ ratios.

For the DRFC prototype, there were j=6 different component thermal resistances of interest, and i=8 intervening thermal resistance layers between the semiconductor junctions and the heatsink. The contact areas A_j, layer thicknesses t_i, and calculated thermal resistances R_j of these six semiconductor component types are detailed in Table 5.3. The thermal conductivity of silicon was taken to be 1.14 $W/^oK/cm$, while the die bonding solder and heatsink solder thermal conductivities were 0.25 $W/^oK/cm$ and 0.5 $W/^oK/cm$, respectively. The separate cases of solder and epoxy adhesive attachment were both computed using their respective layer thicknesses. Table entries stating zero thickness correspond to specific layout circumstances in which one or more thick film layers were missing from underneath a particular die, e.g. the output rectifier die D_{out} was attached directly to the bottom Metal 1 layer.

Part	A_j	Layer Thickness t_i								R_j
		Si	Sldr/Epxy	M2	Diel	M1	Al_2O_3	M0	Sldr	sldr/epxy
Q_1	115x180	20	1.5/1.1	1.1	1.9	1.1	25	1.2	1.5	5.7/6.8
Q_3	115x180	20	1.5/1.1	1.1	1.9	1.1	25	1.2	1.5	5.7/6.8
D_{out}	125x125	20	1.5/1.1	0	0	1.1	25	1.2	1.5	2.8/4.3
D_{reg}	90x90	20	1.5/1.1	1.1	1.9	1.1	25	1.2	1.5	15/17
D_{tap}	50x50	20	1.5/1.1	1.1	1.9	0	25	1.2	1.5	47/57
U_1	55x65	20	1.5/1.1	1.1	1.9	1.1	25	1.2	1.5	33/40
	mils	mils								$^oC/W$

Table 5.3: Semiconductor Thermal Resistances

5.3.2 Component Power Dissipation and Temperature Rise

Following calculation of the thermal resistances between the components and the heatsink, the corresponding component power dissipations were computed. The dissipation in the main MOSFETs Q_1 and Q_2 was entirely due to conduction losses, and had a loss component due to the load current and one due to the magnetizing current. For the selected IRF230

MOSFET, which has a channel resistance $R_{DS,on}$ of 400mΩ, the worst-case power dissipation was calculated to be $0.7W$ per die. The IRF130 pre-regulator MOSFET, operating in a square-wave switching mode, had both conduction losses and switching losses. For an $R_{DS,on}$ of 160mΩ, an output capacitance of 240pF at $25V$, a switching commutation time of approximately 11nsec, and a switching frequency of 2.5 MHz, the total worst-case power dissipation (at low line) was estimated to be $0.8W$. For the exponential output current waveform shape discussed in Section 2.3.1 (Case II in Fig. 2.15), the power dissipation in the output rectifier D_{out} was found to be $2.2W$ per die. The pre-regulator rectifier D_{reg} had a maximum dissipation of $0.5W$ near mid-line, and the tap diodes had a maximum dissipation at low line of $0.5W$ per die. Finally, the dissipation of a DS0026 gate drive IC was measured at 5 MHz with an IRF230 dummy load and found to be composed of $200mW$ standby power plus $300mW$ switching losses.

These dissipations are summarized in Table 5.4. Their dissipation adds up to more than the expected total power loss in the converter semiconductors because these are all worst case dissipations and hence do not occur simultaneously. The table also shows the corresponding thermal resistances from Table 5.3, and the resultant thermal rise ΔT above the heatsink temperature.

Part	Dissipation	R_j		ΔT	
	W	solder	epoxy	solder	epoxy
Q_1	0.7	5.7	6.8	4.0	4.8
Q_3	0.8	5.7	6.8	4.6	5.4
D_{out}	2.2	2.8	4.3	6.2	9.5
D_{reg}	0.5	15	17	7.3	8.8
D_{tap}	0.4	47	57	20	23
U_1	0.5	33	40	17	20

Table 5.4: Worst-Case Component Power Dissipation and Thermal Rise

From the tabulated results, it is clear that the worst-case additional temperature rises due to the use of epoxy as a die bonding agent were relatively small, ranging from 0.8°C to 3.3°C. Both methods were therefore essentially equivalent from a thermal point of view. Because the gate drive ICs lacked any solderable backing metallization, epoxy was judged to be preferable in terms of assembly convenience and was used for all of the die bonds. For completeness, the solder die bonding method was used as well, with comparable converter

performance. Both assembly processes are described in the following section.

5.4 Construction Details

Following completion of the design and thermal analysis of the prototype DRFC, the substrates and transformers were fabricated and the converters assembled. The techniques and procedures outlined in Chapters 3 and 4 were used and adapted for the particular circuit and layout. This section details the specific equipment and process parameters used for the version of the DRFC prototype corresponding to the layout in Appendix D, the circuits shown in Figs. 5.2 and 5.4, and the parts list of Table 5.1.

Table 5.5 lists the major equipment items employed in the fabrication of the DRFC prototype. The furnace/controller combination was an industry standard infrared fast-firing furnace outfit. The ink drying oven was a hot air convection-heated front-opening unit with no special atmosphere-containing capabilities. The viscometer and constant temperature bath were used to measure ink viscosities, both to verify factory measurements and to monitor ink lifetimes. The vapor phase vessel and controller formed a small capacity, single-substrate reflow unit capable of handling up to 10 in. diameter substrates. The hotplate was a generic lab heater which was used for hand soldering of the transformer leads and for component reworking. The solder melting pot was a 5 cu. in. heating vessel which was used for immersion soldering of substrates for adhesion testing purposes. Finally, the wire bonder was outfitted for 1 mil aluminum ultrasonic bonding and could be modified with internal counterweights to bond up to 3 mil wire.

The specific materials used to fabricate the copper thick film substrates are listed in Table 5.6. Also included in the table are the solder and epoxy adhesives used to assemble the components, the wedges necessary for ultrasonic aluminum wire bonding, and the non-electrical prototype components. The electrical components were listed in Table 5.1, with the exception of the transformer materials, which were described in Section 4.4.3.

The final size of the DRFC prototype was 1.1 in by 2.2 in, so the 96% Al_2O_3 alumina ceramic supplied by the manufacturer required cutting. The final size of the converter was too small to process conveniently, however, so an intermediate substrate size of 2.25 in by 3.5 in was selected. A carbide-tipped scribe was used to mark and cut them. The solder pastes were formulated for screen printing and had particles ranging in size up to 5 mils. The wire solders contained rosin fluxes and were used for hand soldering and reworking.

Description	Model Number	Manufacturer
Transheat Furnace	TFF41-4-36N26GT	BTU Engineering Corp. No. Billerica, MA
Bruce Controller	7354M	BTU Engineering Corp. No. Billerica, MA
Oven	213023	Hotpack Corp. 10940 Dutton Rd. Philadelphia, PA 19154
Semi-Auto Screen Printer	SP-SA-5	de Haart, Inc. 12 Wilmington Rd. Burlington, MA 01803
Viscometer	HBT	Brookfield Engineering Labs 240 Cushing St. Stoughton, MA 02072
Constant Temp Bath	EX-200	Brookfield Engineering Labs 240 Cushing St. Stoughton, MA 02072
Vapor Phase Unit	350 Watt	Multicore Solders Cantiague Rock Rd. Westbury, NY 11590
Control Unit	PL-112	Multicore Solders Cantiague Rock Rd. Westbury, NY 11590
Hotplate	SPA 1025B	Thermolyne Corp. 2555 Kerper Blvd. Dubuque, IA 52001
Solder Melting Pot	MP4A-12-1	Waage Electric Inc. Kenilworth, NJ 07033
Al Wire Bonder	4123	Kulicke and Soffa Industries 507 Prudential Rd. Horsham, PA 19044

Table 5.5: Equipment List for Prototype DRFC Construction

Material	Part #	Description	Manufacturer
inks	4575D	dielectric	DuPont
	5681D	glass encapsulant	DuPont
	9922	outer layer	DuPont
	9924M	inner layer	DuPont
	9926D	overprint	DuPont
	9927D	via fill	DuPont
substrates		Al2O3, 25 mil, 3.5" x 4.5"	Coors Ceramics
screens		heatsink [200mesh,0.5mil emul]	UTZ Engineering
		ground plane [325,0.5]	UTZ Engineering
		dielectric [200,0.7]	UTZ Engineering
		via [200, 0.7]	UTZ Engineering
		conductors [325,0.5]	UTZ Engineering
		glass enc't [325, 0.5]	UTZ Engineering
		solder paste [80,5.0]	UTZ Engineering
solders	Sn62PRMA-B3	62Sn,2Ag,36Pb; paste	Multicore
	Sn62	62Sn,2Ag,36Pb; 24 gauge wire	Multicore
	Sn96PRMA-B3	96Sn,4Ag; paste	Multicore
	Sn63	63Sn,37Pb; 22 gauge wire	Multicore
	TLC	50Sn,33Pb,17Cd; 20 gauge wire	Multicore
vapor	FC70	215C vapor temperature	3M Indus. Prod.
phase	FC71	253C vapor temperature	3M Indus. Prod.
chemicals	PC81	hot/cold vapor degreaser	3M Indus. Prod.
epoxies	5260	silver-filled epoxy	Heraeus Cermalloy
	154	thermal epoxy	Wakefield
flux	14000	Nokorode solder paste	M. W. Dunton Co.
solvents		1,1,1 Trichloroethane	
		methanol	
		acetone	
		aerosol flux remover	SPC Technology
bonding	2131-2525-L	1 mil Al wedge	Gaiser Tool
wedges	2131-4570-L	3 mil Al wedge	Gaiser Tool
heat sink	61585	plated 6063T5 Al extrusion	AAVID
I/O pins	929835-01-14	right angle header	3M Assoc'd Elect's
test pins	50462-7	oscilloscope probe tip sockets	AMP Inc.

Table 5.6: Materials for Hybrid Substrate Fabrication

The silver-filled die bonding epoxy was premixed and required cold storage to prevent curing with age. The aluminum heatsink backside was plated with copper (0.3–0.5 mils) and tin (0.1–0.25 mils) to make it solderable, and then cut to the final prototype substrate size.

5.4.1 Thick Film Substrate Fabrication Parameters

Once the equipment and materials were gathered, the thick film substrates were fabricated. The thick film printing parameters for the specific DRFC masks shown in Appendix D are listed in Table 5.7. These numbers are optimized for the specific conditions encountered in the processing of these masks, but are representative of the settings to be used on this equipment for any multilayer copper hybrid.

	Layer					
	Heatsink A/B	Metal 1 A/B	Dielectric A/B	Metal 2 A/B	Glass	Solder
Ink	9922/9926D	9922/9926D	4575D	9922/9926D	5681D	Sn62
Mesh	200	325	200	325	200	80
Emulsion	0.5	0.5	0.7	0.5	0.5	5.0
Snap-off	25/30	25	30	25/32	30	25
Flood	10	10	10/12	10	10	5
Squeegee	-5	-5	-5	-5	-5	-5
Squ. Press.	25/20	25/30	25	25	25	30
Speed	3.6/3.5	3.6	3.4/3.45	3.4/3.8	3.5	3.3
Settle Time	5	5	7	7	10	10
Dry Time	10/12	10	12	10	15	15
Dry Temp	120	120	120	120	120	150

Table 5.7: Copper Hybrid Prototype Printing Parameters

The furnace control settings given in Table 5.8 are general and can be used without modification for a variety of copper thick film fabrication applications. A sample firing profile is shown in Fig. 5.8. The belt speed was accelerated to reduce processing time for the prototype and would normally be reduced to decrease the ramp rate and thereby permit a more complete burnout of the ink organics prior to sintering. The first firing zone heater setting would then be reduced correspondingly. The atmosphere flow rates are intended for use with a 5% belt load (corresponding to a 6 in spacing between substrates on a 5 in wide belt) and would be scaled accordingly if substrates were to be placed at a different interval.

After the final glass encapsulant layer was fired, the substrates were visually inspected

Zone Temperatures (°C)				Nitrogen Flow Rates (lpm)					Belt Speed (ipm)
975	985	985	970	15	10	20	25	15	4

Table 5.8: Furnace Control Settings

and tested for shorts between adjacent conductors and between layers. Most shorting occurred in the neighborhood of the gate drive ICs, where the resolution design rules were strained to meet the complex layout requirements. Substrates which passed the tests were considered complete and were used for prototype construction purposes.

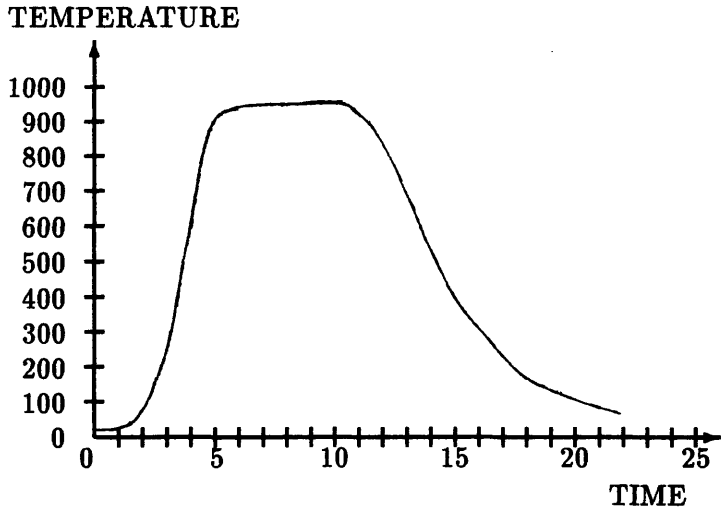


Figure 5.8: Furnace Temperature Profile

5.4.2 Component Attachment Procedures

Following completion of the substrate fabrication process, the components were attached. A low leaching solder paste (Sn62) was first printed onto the substrate, and the capacitors were hand placed in the wet solder. The solder was dried to remove the printing solvents, a necessary process to avoid their rapid evaporation during reflow. The solder was then reflowed in the vapor phase reagent (FC70), cooled, and cleaned to remove the residual fluxes.

At this time, the substrates were cut to their final size. This was judged to be the ideal

time because it followed the final step that required screen printing, and hence did not interfere with substrate alignment. Furthermore, substrate cutting (by scribing methods) is a relatively low yield process, so it was beneficial to precede adhesive attachment of the semiconductors. The soldered capacitor connections were reworkable, so broken substrates could generally be salvaged.

Following the final substrate cut, the semiconductor components were hand epoxied. A small amount of epoxy was placed on each die bond site with a syringe and the die was scrubbed in with a soft tool to minimize voids and reduce the bond thickness. Scrubbing was continued until the bond "froze", i.e. the die would no longer slide from side to side. Destructive testing revealed that consistent 1.1 mil thick, void-free bonds were achieved with this method. After scrubbing the dice into place, the epoxy was cured for 15 min at 150°C in the convection oven, and then cooled.

5.4.3 Wire Bonding

Ultrasonic wire bonding was performed immediately following die bonding, despite the consequent exposure of the fragile bonds to possible damage during subsequent assembly steps, to limit the oxidation of the wire bond sites. Large diameter 3 mil aluminum wires were paralled whenever possible to reduce both the resistance and the inductance of the bonds. Maximum arm weight (minimum counterbalance) and high ultrasonic power were used, with first/second bond settings of: force=8.0/9.2, time=8.3/9.3, power=10/9.5. Smaller diameter 1 mil wire was used for the gate drive ICs because of their limited bonding pad dimensions. The corresponding bonding machine adjustments for the 1 mil wire included the standard calibrated counterweighting with low power ultrasound and bond settings of: force=4.5/4.4, time=4.0/5.3, power=4.4/4.7. The aluminum pads on the silicon dice were bonded first for both the 1 mil and 3 mil wires. A relatively cool 85°C heated stage was used during wire bonding as a compromise to promote bond adhesion without causing excessive surface oxidation.

A close-up view of this wire bonding is shown in Fig. 5.9. The smaller 1 mil wire was used for the gate drive connections to the MOSFETs, where their greater packing density gave them a lower combined bond inductance. Current capacity was a greater concern for the source connections, so 3 mil wire bonds were paralled for these bonds. The photo also shows the 1 mil wire bonds used for the gate drive ICs and the multiple 3 mil wire bonds

used for the pre-regulator and tap rectifiers. Finally, the close proximity between the gate drive ICs and their respective MOSFETs can be seen; the total substrate area required for the combined IC/MOSFET would fit inside a standard TO-3 package.

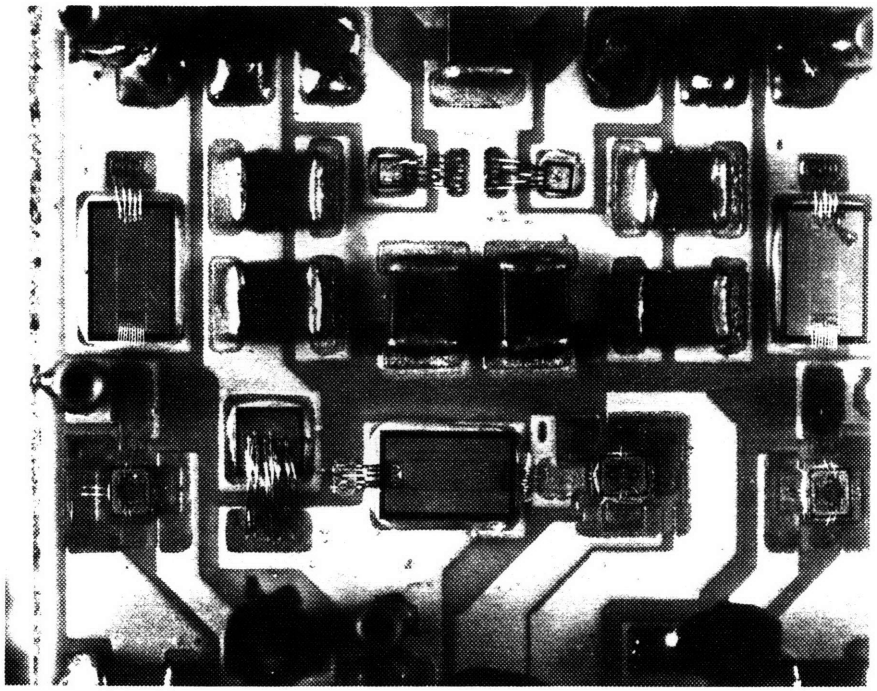


Figure 5.9: Sheet Parallelled Multiple Wire Bonding Detail

For the prototype versions made using solder for die bonding (instead of silver-filled epoxy), this assembly order was modified. Die bonding came first, followed by wire bonding and finally by capacitor attachment. A higher temperature SN96 solder paste was screen printed onto the die bond sites, the dice were gently scrubbed into the wet (tacky) solder paste, and the solder solvents were oven evaporated. The solder was then reflowed in FC71, completing the die bonds. Wire bonding was performed as before, followed by hand soldering of the capacitors with SN62 rosin core wire solder. It was necessary that wire bonding precede the capacitor soldering because the soldering process was slow and was performed in an air atmosphere. The copper would oxidize sufficiently during this time period to reduce subsequent wire bond adhesion to the point of unreliability.

Following wire bonding, the substrates were again tested for electrical functionality. During these tests, yields were high and failures were rare, because the wire bonds were done by hand and visually inspected individually. Furthermore, most wire bond connections had multiple wires, which greatly reduced the chances of open connections; careful layout

and the judicious use of overglaze encapsulant minimized the chances of shorts. Finally, all of the components were individually probed following dicing to insure their functionality before die bonding.

5.4.4 Magnetics and I/O Pin Attachment

Attachment of the larger components whose profiles would have interfered with the access of the ultrasonic bonding head was performed following the electrical tests. The bottom cores of the assembled transformers were mounted in place on the ceramic substrates using the thermal epoxy, with care being exercised to align the secondary termination tabs with the output rectifiers. The input inductor was mounted in a similar manner. The substrate was then heated briefly to a moderate temperature (approximately 150°C) to permit soldering of the transformer tabs and the I/O pins. Modified IC socket pins were also soldered to the substrate to facilitate the attachment of oscilloscope probe tips for instrumentation purposes.

5.4.5 Heatsink Attachment

The final step in the assembly of the DRFC prototype was the attachment of the heatsink. A special low-temperature soft solder was used for this purpose, to reduce thermal stresses and to prevent reflow of the previously soldered components. Both surfaces (the backside of the substrate and the plated heatsink) were first heated on the hotplate and tinned individually to insure complete wetting. The substrate was then placed on the heatsink, the excess solder was pressed out, and the joint was cooled. The resultant bond was both strong and a good thermal conductor. Following this last assembly step, the hybrid was cooled, cleaned once again, and then oven dried to remove any moisture.

5.5 Summary of Hybrid Prototype Construction

The hybrid converter was built using the copper thick film, according to the processing techniques described in Chapter 3. A two metal layer interconnection structure was used, with an additional metallization provided on the backside for heatsink attachment; details of the thick film fabrication process were recorded for reference and comparison. The converter was designed to run open loop, with a minimum of external support to aid in diagnostics and testing. Careful attention was paid to the layout details, to minimize the the critical

interconnection parasitics identified in Chapter 2. The transformers described in Chapter 4 were constructed, tested, and integrated into the hybrid design. Finally, a thermal analysis revealed that adhesive die bonding techniques could be used without significant penalties.

The resultant hybrid prototype of the DRFC is shown in Fig. 5.10, complete with heatsink and scope probe test connectors. The photo shows the dual half-height transformers and the half-height pre-regulator inductor. The photo of Fig. 5.9 is a close-up of the center portion of this converter.

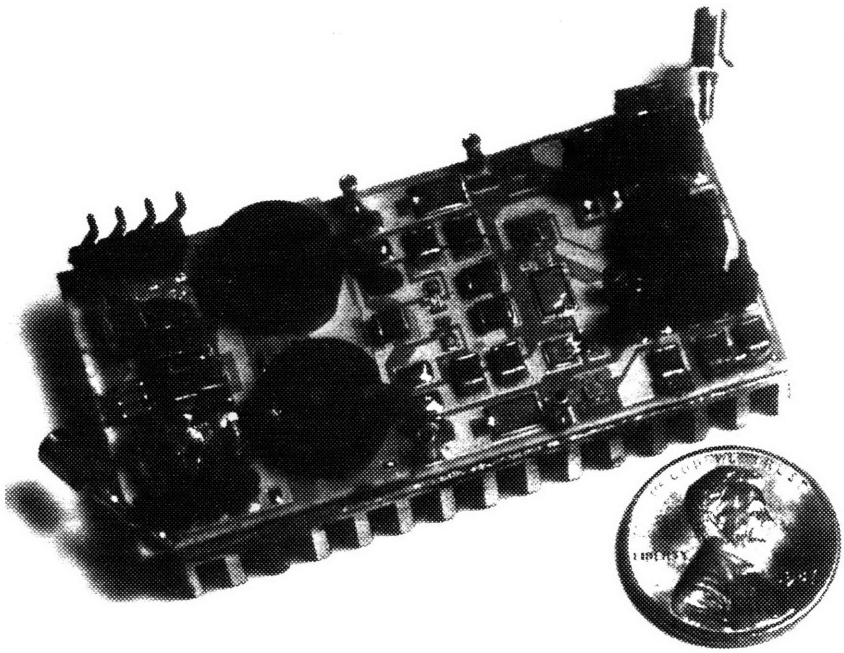


Figure 5.10: Hybrid Prototype DRFC

The dimensions of the completed hybrid, with the heatsink (but not including the scope probe connectors or the I/O pins) are: height=0.495 in, width=1.13 in, length=2.26 in. Without the heatsink, the height of the converter would be reduced by 0.29 in, while the use of full height transformers would have added 0.90 in. At $50W$, the power density of the hybrid converter is therefore $39.6W/\text{in}^3$, including the heatsink. Without the heatsink, the power density is $96W/\text{in}^3$.

Chapter 6

Experimental Results

The hybrid prototypes whose construction was described in the previous chapter were first tested for functionality at low power to confirm the operation of all components. Measurements were then performed to confirm the various design estimates. Finally, the full power performance of the converter was evaluated in terms of the standard parameters for power supplies.

This chapter first describes the measurement procedures used to characterize the converter. It then presents a summary of these measurements and documents the observed waveforms. These waveforms are interpreted and the measurements are compared to the expected theoretical performance of the converter. Additionally, estimates of the magnitudes of key parasitics are computed and the conversion efficiency as a function of input voltage is tabulated.

6.1 Instrumentation

The prototype DRFC hybrids were laid out and constructed with instrumentation in mind. Specifically, test point locations were included on the substrate, and probe tip sockets were soldered to these areas during the construction process. While the allotment of space for these probe receptacles represented a significant sacrifice in power density, they were essential for obtaining clean, accurate waveforms. These test points provided access to the drain voltages of the three MOSFETs as well as their corresponding gate voltages. These particular signals were chosen because they provide most of the pertinent information from which the converter's operation can be deduced.

Because of space limitations, it was not possible to provide room for the standard grounding jacks which usually accompany these probe tip sockets. Instead, clips affixed

to the PCB directly above the hybrid were used to ground the probe bodies. The noise pick-up due to these short ground loops was minimal, as evidenced by the clean waveforms. Additional external test probe jacks were connected directly across the input and output capacitors to measure the respective voltage ripples. Grounding jacks were used for these connections because the ripples were relatively small compared to the noise pickup and the location of the capacitors greatly simplified installation of the jacks.

The completed converter was plugged into the external clock and PWM board, and the combined assembly was turned upside-down. Oscilloscope test probes were inserted through holes in the PCB into the probe tip connectors. The PCB provided additional support to relieve the strain on the hybrid metallization, but care was required to insure that the probes did not break the connector solder joints. This test configuration is shown in Fig. 6.1. Tektronix #P6131 probes were used, which were rated at 10.8pF and 10MΩ and had a voltage attenuation factor of 10. The oscilloscope was a 300 MHz Tektronix Model #2465 with four independent display channels.

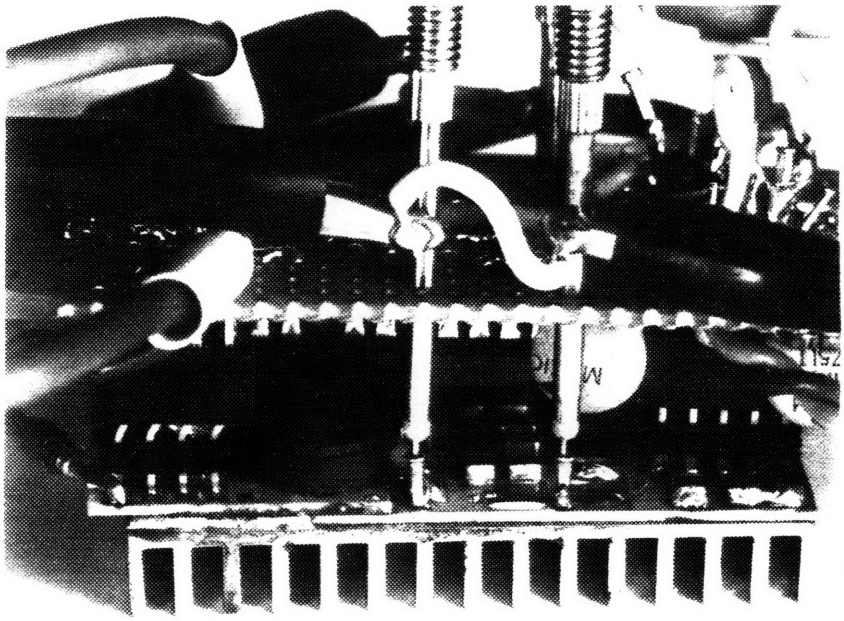


Figure 6.1: Hybrid Prototype Converter with External PCB

Additional instrumentation was used to monitor the input and output voltages and the input and output currents. Matched Fluke 77 DVMs were used for the current measurements, while Fluke 8050A DVMs were used for the voltages. A low-impedance common-mode RC filter (τ=100μsec) was added to the output voltage meter to prevent noise from

interfering with the accuracy of the measurements. These four meters were used to make simultaneous measurements for efficiency calculations.

6.2 Test Procedure

A small 'muffin' type fan was turned on and left on throughout the test sessions to simulate the cooling available in a computer mainframe. Once the appropriate probes were in place, the gate drive bias supplies were applied. These bias supplies were normally set at $10V$, but voltages as high as $15V$ and as low as $7V$ were used without incident. The function generator-synthesized clock inputs were applied next, and the gate drive waveforms were inspected. The pre-regulator clock was then turned off, with the gate of the pre-regulator MOSFET Q_{reg} held at ground.

The input voltage was applied through a switch which permitted pulse power testing. The input supply, a dual $40V$ Hewlett Packard benchtop supply wired to run in current-sharing mode, provided up to $45V$ at up to $3A$. With this voltage applied, the main clock frequency was adjusted so that the channels of MOSFETs $Q1$ and $Q2$ turned on just as their respective ring cycles ended. This timing was determined by monitoring the gate drive waveforms; for zero-voltage turn-on, the plateau regions of these waveforms were minimal. The input voltage and clock frequency were increased simultaneously, maintaining this timing relationship, until the full $42V$ input voltage was reached. The output load was then increased in increments, using tapped power resistors. Finally, the pre-regulator duty cycle was increased, and the input voltage was decreased correspondingly, so that the primary side bus voltage remained constant.

Once an operating point was reached, the converter could be turned on and off at that point simply by switching the input voltage supply in and out. The input voltage did not have to be brought up slowly, and the operating frequency remained fixed. Changes in the input voltage were compensated for (manually) by adjusting the pre-regulator duty cycle. This method of testing reflected the normal mode of operation, albeit with a controller bandwidth governed by manual reaction speeds. Similarly, the load could be switched in and out without adjusting the operating controls.

6.3 Measurements and Waveforms

Using the previously described testing approach, a number of stready-state measurements were made. The operating points were recorded, and the waveforms were photographed. In this section, a family of selected waveforms at nominal and extreme operating points are presented, along with explanations and interpretations.

6.3.1 Gate Drive Waveforms

The gate drive waveforms were observed first, before applying input power to the converter, to verify the functionality of the circuit. A pair of gate drive waveforms for the main MOSFETs $Q1$ and $Q2$ are shown in Fig. 6.2, with operation at 4.5 MHz and with a bias supply of $11V$. As expected, a small plateau region was visible during the turn-on transitions, due to the Miller effect which is present even when the drain terminals are disconnected.

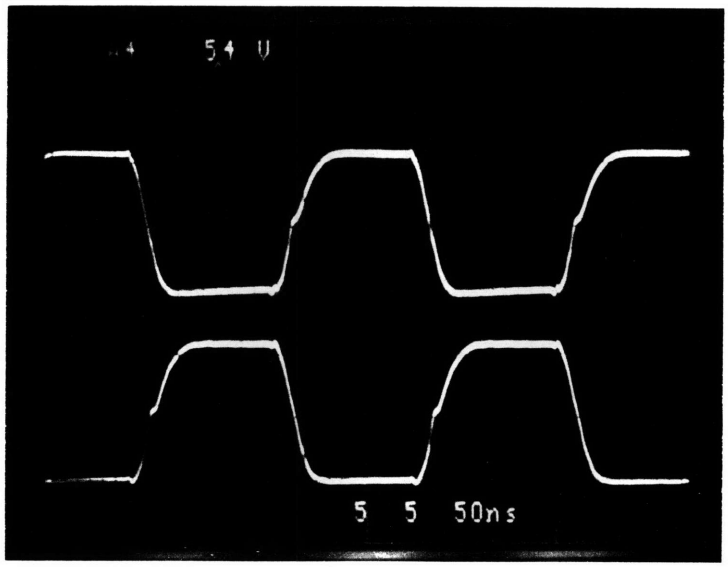


Figure 6.2: Main MOSFET Gate Drive Waveform Pair

Similar waveforms, taken at 3 MHz with a $10V$ bias supply, are superimposed and expanded in Fig. 6.3. This photo confirms the existence of a slight 2.8 nsec skew time between the two gate drive signals, corresponding to the propagation delay through the AS-logic TTL inverter.

Expanded views of the gate drive transitions, shown in Figs. 6.4 and 6.5, show the

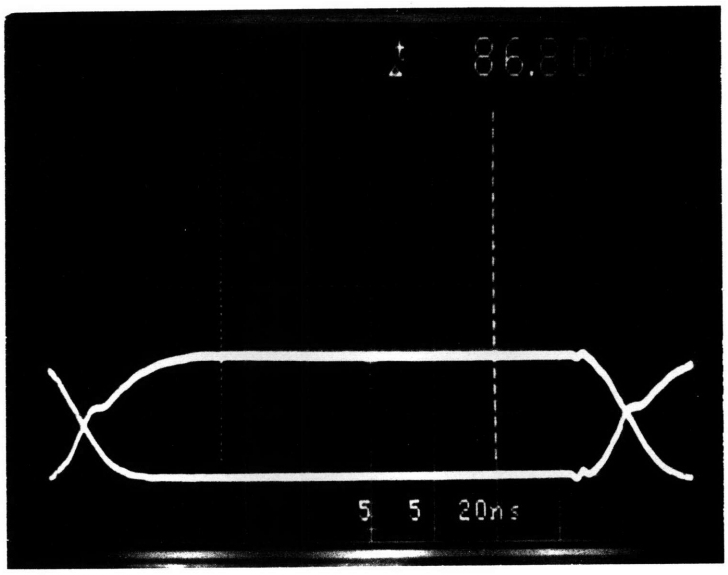


Figure 6.3: Timing Skew in Main MOSFET Gate Drive Waveforms

rise and fall times of the gate drive circuitry. The rise time was 29.8 nsec, with a plateau period (corresponding to the MOSFET switching time) of only 4 nsec. The fall time was 21.7 nsec. During normal operation, these transition times remained virtually constant regardless of the input voltage or loading conditions, because the switch transitions always occur with zero volts across the gate. However, incorrect adjustment of the conversion frequency sometimes resulted in premature switch turn-on before the drain voltage rang down to zero volts. This introduced switching losses in the converter's operation and also increased the gate drive rise times. This effect is described further in the next subsection.

6.3.2 Drain Voltage Resonant Ring Waveforms

Once the operation of the gate drive circuitry had been confirmed, the input voltage was applied and the resonant ring waveforms were observed. A typical pair of drain voltage waveforms which illustrate the non-linear nature of the resonant ring are shown in Fig. 6.6. The circuit was operated with an input of $42V$; the corresponding clock frequency necessary for zero-voltage transitions was 4.6 MHz.

As discussed in Section 2.3.1, the non-linear nature of the resonant capacitor causes the resonant frequency to change as the input voltage is varied. When the input voltage is increased, the average magnitude of the non-linear capacitor decreases, and the resonant

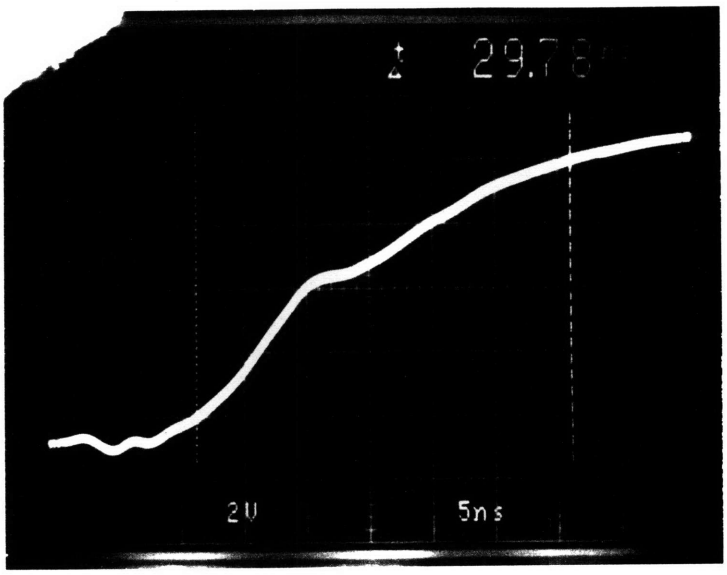


Figure 6.4: Gate Drive Waveform Showing Rise Time

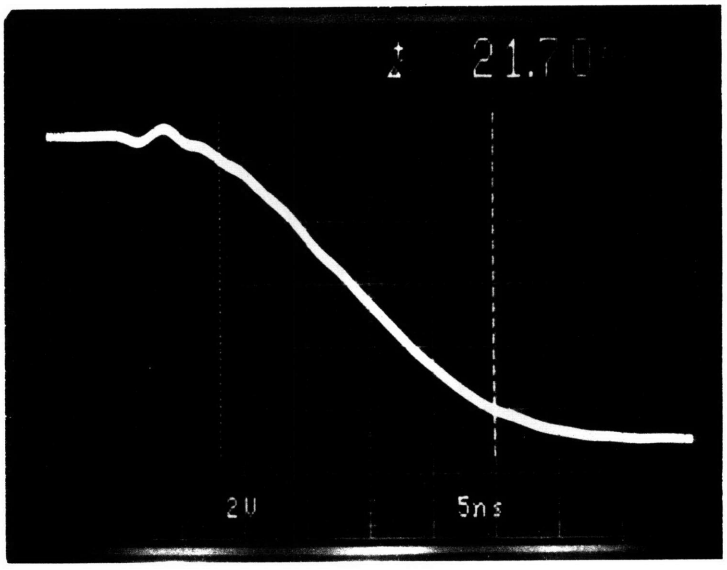


Figure 6.5: Gate Drive Waveform Showing Fall Time

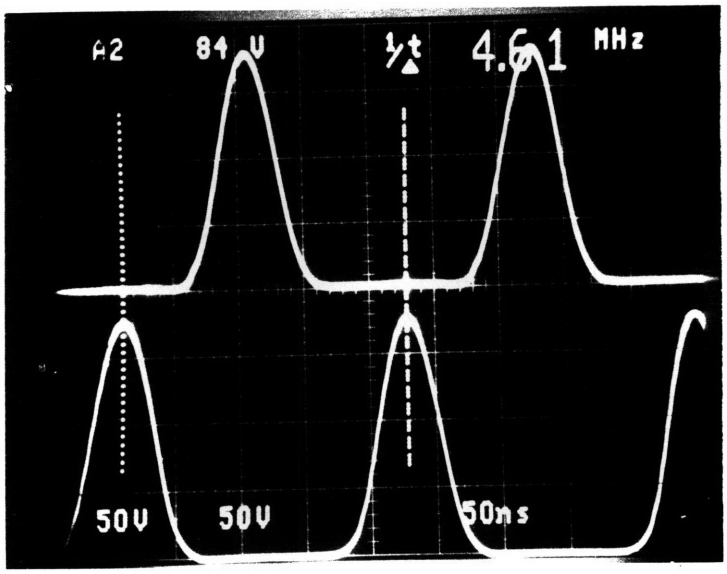


Figure 6.6: Main MOSFET Drain Voltage Waveform Pair

frequency therefore increases. This effect is shown in the series of photos in Figs. 6.7 through 6.9. The operating frequencies were 3.0 MHz, 4.0 MHz, and 4.5 MHz respectively, with corresponding input voltages of $10V$, $20V$, and $30V$.

The operating frequency of the converter was set by observing the plateau region of the gate drive waveforms. Premature turn-on, corresponding to an excessively high conversion frequency, increased the length of this period due to the Miller effect. An exaggerated example of this effect is shown in Fig. 6.10, with a $33V$ input supply and a $12.5W$ load. This condition was confirmed by the shortened drain voltage ring waveform; during the last 20 nsec, this voltage collapsed rapidly. In addition, the peak ring voltage of $136V$ was approximately $12V$ lower than would be expected for the given input voltage, when operated with zero-voltage switch transitions. This reduction is due to the shorter on-time of the MOSFET, which results in a smaller magnetizing current to drive the ring.

6.3.3 Effects of Loading on Resonant Ring Waveform

The drain voltage resonant ring waveform pairs for light ($1.5A$) and full ($10.5A$) loads are shown in Figs. 6.11 and 6.12. The fully loaded operating parameters were: V_{in}=$39.5V$, V_{out}=$5.0V$, I_{in}=$1.58A$, I_{out}=$10.6A$, and f_{sw}=4.5 MHz. The input power was therefore $62.4W$, while the output power was $53W$, giving a fully loaded conversion efficiency of

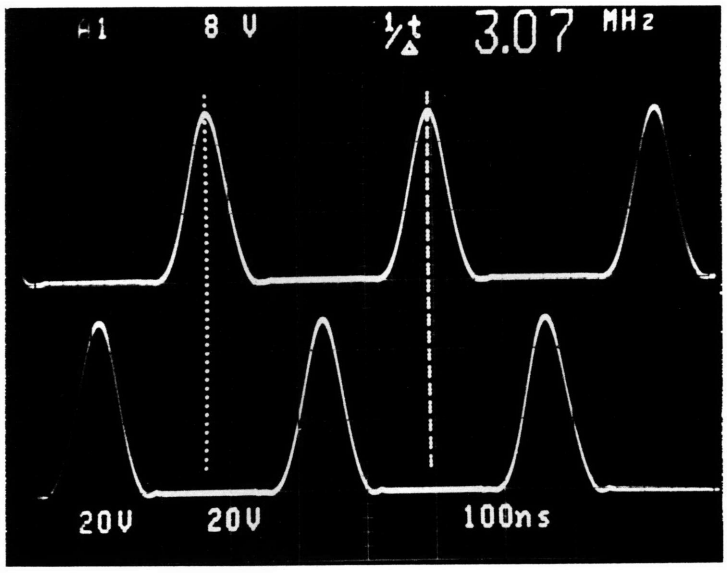


Figure 6.7: Main Switch Resonant Waveforms for 10 Volt Input

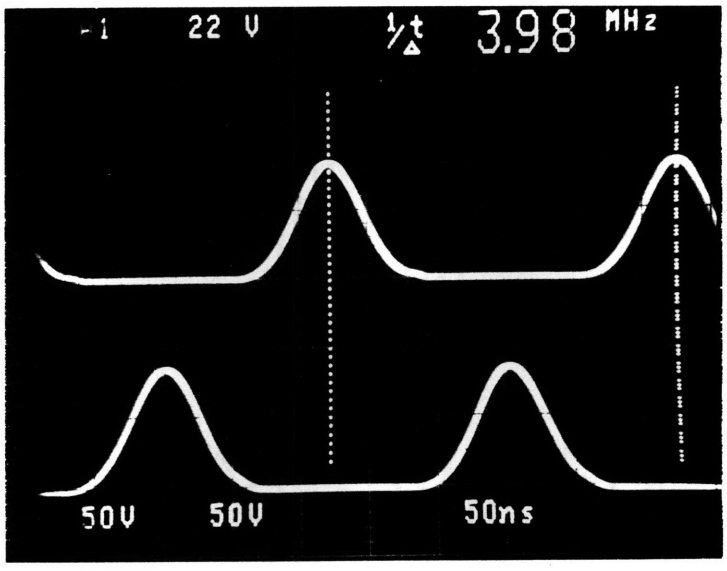


Figure 6.8: Main Switch Resonant Waveforms for 20 Volt Input

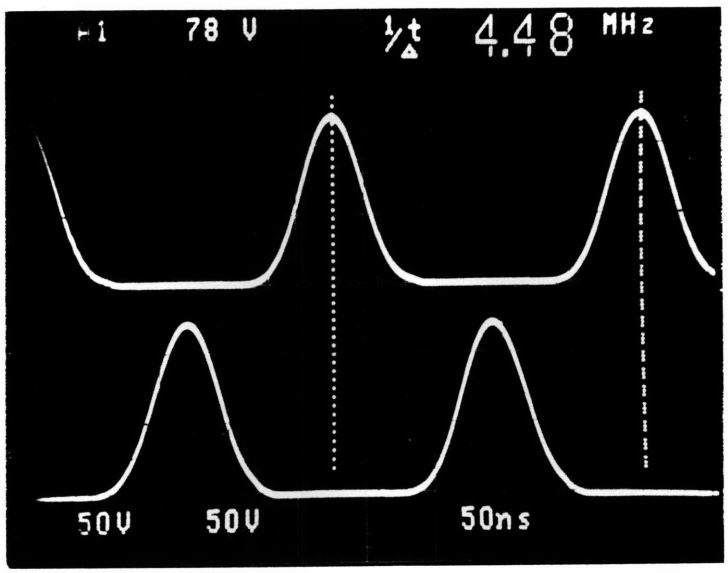


Figure 6.9: Main Switch Resonant Waveforms for 30 Volt Input

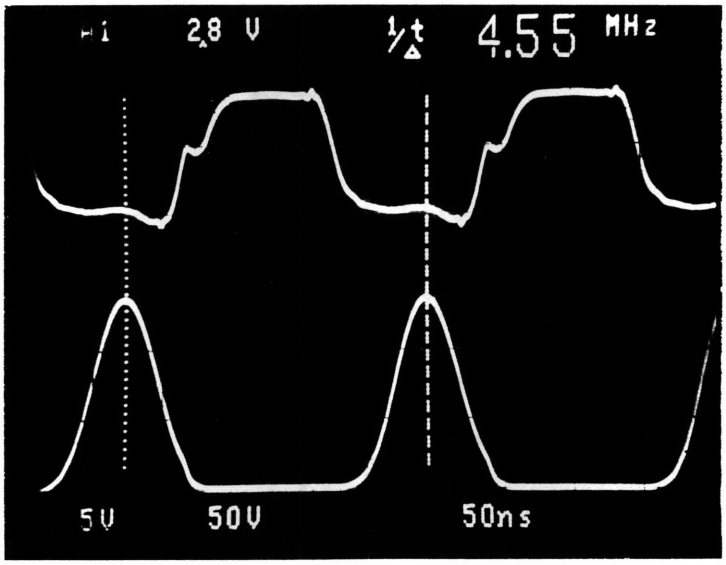


Figure 6.10: Gate and Drain Voltage Waveforms Showing Premature Switching Effects

84.9% at high line. The overall efficiency and conversion performance of the converter under various operating conditions will be discussed in Section 6.3.5.

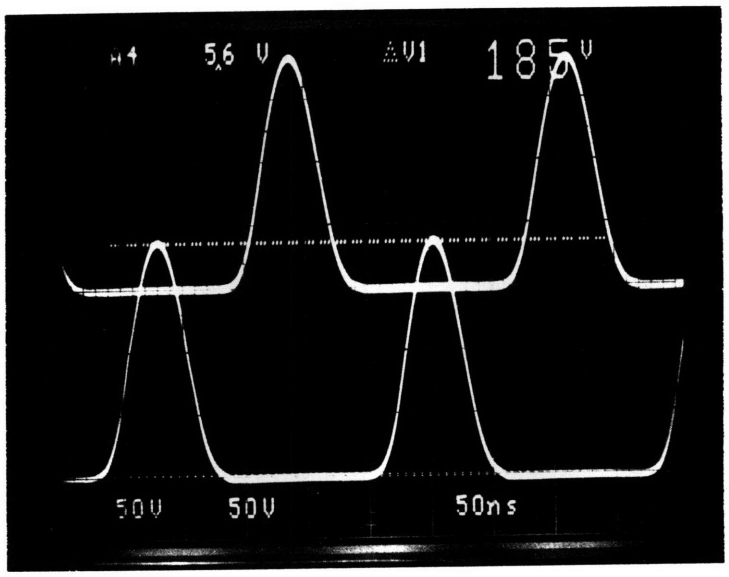


Figure 6.11: Resonant Ring Waveform Pair, Light Load

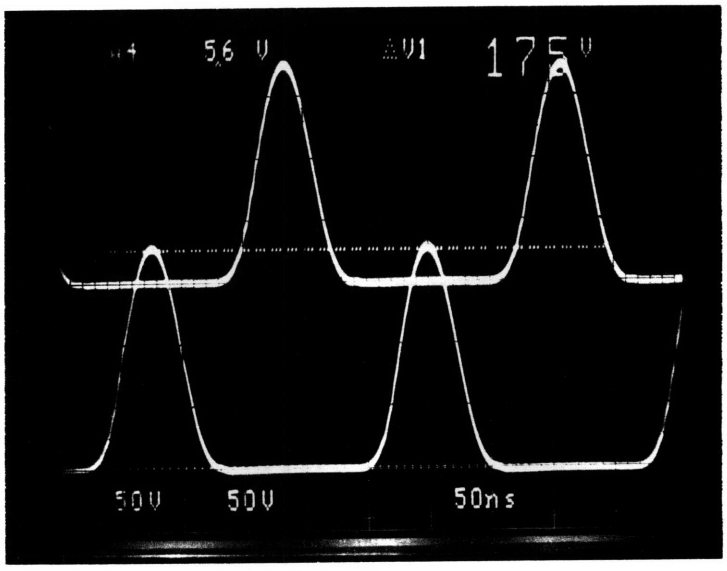


Figure 6.12: Resonant Ring Waveform Pair, Full Load

As derived in Section 2.1.5, the ideal operation of the DRFC topology is independent of loading. Specifically, the frequency and peak amplitude of the resonant ring waveforms should be functions of the input voltage and conversion frequency only. However, inherent component and interconnection parasitics in the converter caused the operation to deviate from the ideal case, and the shape of the resonant waveform became a function of the output current.

For instance, in the lightly loaded case, the resonant ring voltage reached a peak magnitude of $185V$, while at full load this peak fell to $175V$. The change is evident in Figs. 6.11 and 6.12, and was predominantly due to resistive losses in the input filter inductor and pre-regulator stages, which reduced the regulated bus voltage that was applied across the transformer primary.

Another effect of loading, the high frequency parasitic ringing of the leakage inductance with the MOSFET and output rectifier junction capacitances (see Section 2.3.1), is slightly visible in Fig. 6.12. It appears as a small waver on the leading edge of the drain voltage waveforms. An expanded view of this resonant ring waveform is shown in Fig. 6.13. This photo was taken at a higher load current ($12A$, corresponding to $62.5W$ load power) to increase the leakage energy and thereby emphasize this effect.

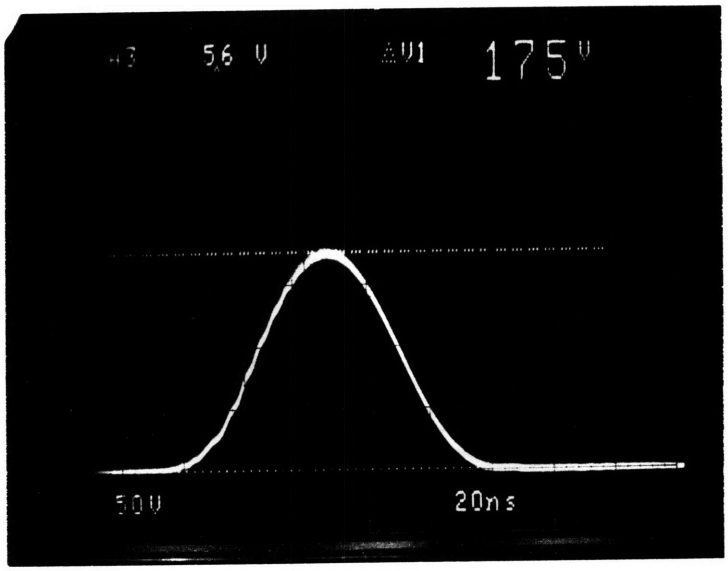


Figure 6.13: Over-Loaded Converter Resonant Ring Waveform

The asymmetric shape of the resonant ring is also notable. The dv/dt of the rising edge

was more rapid than the falling edge because the initial charging current flowing into the parasitic MOSFET resonant capacitor is the sum of the magnetizing and leakage currents, while the final current flowing out of this resonant capacitor is due to the magnetizing current alone. The amount of this asymmetry was a function of the energy stored in the leakage inductance and therefore increased with loading.

The high frequency oscillation and resonant ring asymmetry effects shown by the hybrid prototype were both relatively small (even when exaggerated by overloading the output) compared to the PCB prototype versions because the transformer leakage inductance and secondary loop inductance were much less. This is an important point, as it confirmed the benefits of hybrid construction and FLEX-wound transformer fabrication.

The high frequency ring could be seen more clearly by observing the gate drive waveforms. The resonant ring waveform pairs of Figs. 6.11 and 6.12 are repeated in Figs. 6.14 and 6.15 respectively, accompanied by their associated gate drive signals. The coupling of the high frequency ring to the gate drive waveforms was most discernable in Fig. 6.15, the fully-loaded case, where the load currents were highest and the leakage energy was greatest.

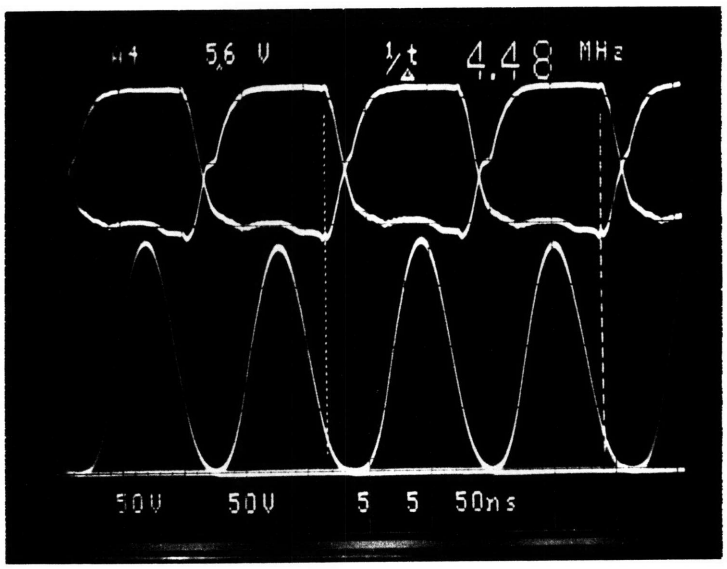


Figure 6.14: Gate Drive and Resonant Ring Waveforms Under Light Load

The high frequency ring appeared during both the on-time and the off-time of each gate drive signal because there was cross-coupling between the dual converter halves. This coupling was due to several distinct mechanisms. First, the common ground connection

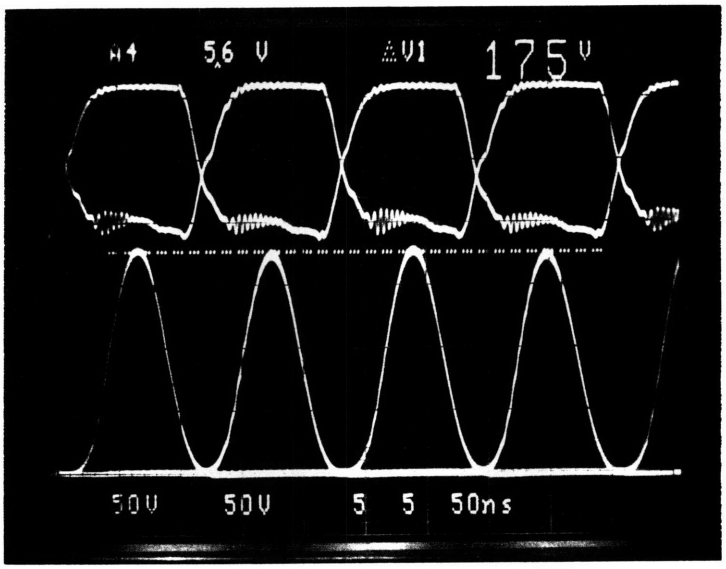


Figure 6.15: Gate Drive and Resonant Ring Waveforms Under Full Load

of the gate drive ICs and the MOSFETs introduced voltage drops on the hybrid. These drops had a common-mode component which appeared between the intrumentation ground (the ground connection to the input supply) and the bias supply ground (gate drive signal ground). In addition, EMI pickup at the ring frequency was not totally eliminated, even with the tight loops formed by the instrumentation grounding straps. Finally, a strong coupling occurred between the gate drive signal and its respective MOSFET drain voltage through the parasitic Miller capacitance.

The gate and drain voltage waveforms of Fig. 6.15 are expanded in Fig. 6.16 to clarify the nature of the high frequency ring. The parasitic ring frequency was approximately 250 MHz, and was damped in approximately 50 nsec. Also, the resonant ring frequency had a half-period of 67 nsec, corresponding to a resonant frequency f_{res} of 7.4 MHz which was quite close to the 7.1 MHz design frequency.

The lightly loaded case in Fig. 6.14 also indicated the presence of a small asymmetry between the two halves of the dual converter. The asymmetry was most visible when comparing the dwell times of the plateau regions of the two gate drive waveforms. This difference can be due to a number of causes, including differences in magnetizing inductance, differences in parasitic resonant capacitances, or large differences in leakage inductance. The latter was ruled out by noting that the energy stored in these leakage inductances was quite

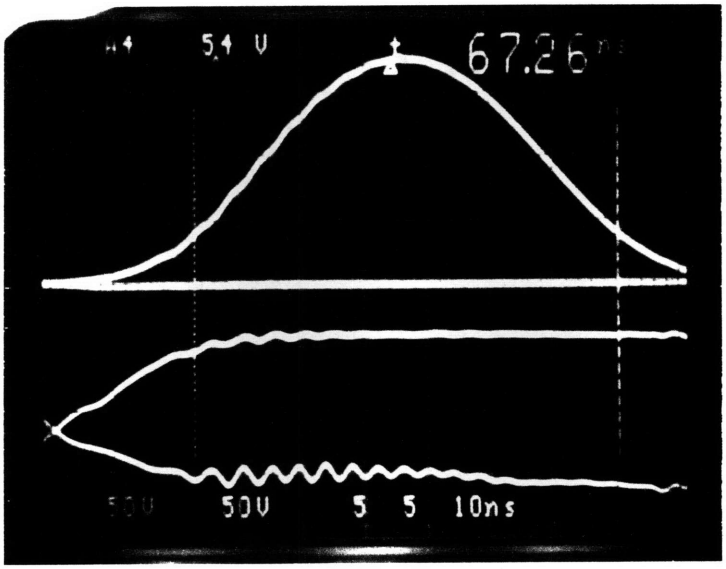


Figure 6.16: Expanded Gate Drive and Resonant Ring Waveforms Under Full Load

even, judging from the magnitude of the associated gate drive high frequency rings. The timing skew between gate drive signals also contributed to this asymmetry to a small degree. Qualitatively, the combined impact of these asymmetries upon the resonant ring behavior was small. The total plateau period (5 nsec) was only 2% of the switching period (220 nsec) and the ring period mismatch was therefore less than 1%; the difference in peak ring voltages was similarly minimal. The effect of these asymmetries upon the sharing of load currents will be investigated further when the output ripple waveforms are examined.

6.3.4 Pre-Regulator Drain Voltage Waveforms

The previously described measurements were made with the pre-regulator stage disabled (by setting the duty cycle of Q_{reg} to 0%). The gate drive and switch voltages of the pre-regulator MOSFET were then studied in a similar manner. A typical waveform pair for Q_{reg}, showing V_{DS} (above) and the gate drive IC input (below) appear in Fig. 6.17. The IC input signal was used as a reference because the gate voltage could not be instrumented.

The main converter operating parameters were: V_{in}=34.4V, V_{out}=5.0V, I_{in}=1.87A, I_{out}=10.5A, and f_{sw}=4.5 MHz. Under these conditions, the pre-regulator operating parameters were D=50% and $f_{sw,pre}$=2.25 MHz. The input power was therefore 64.3W, while the output power was 52.5W, giving a fully loaded conversion efficiency of 81.6% at mid-

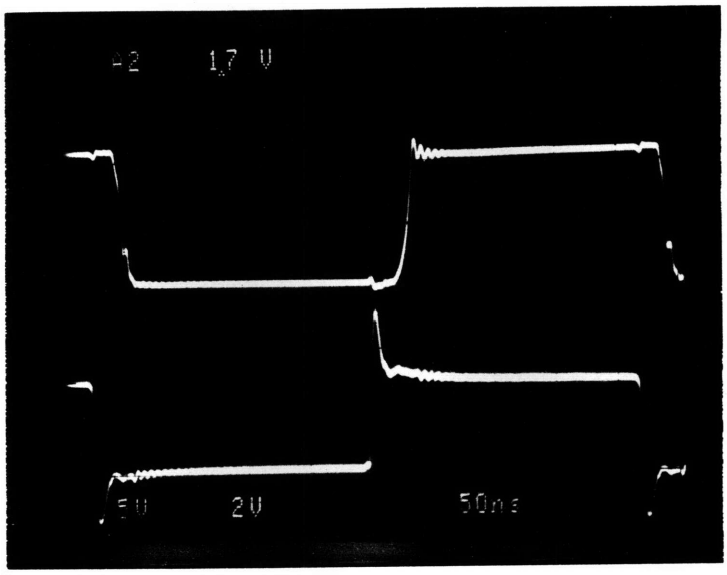


Figure 6.17: Pre-Regulator Drain Voltage and Drive Signal

line. This efficiency increased to 82.7% when the pre-regulator switching frequency was reduced to $f_{sw,pre}$=1 MHz.

Expanded views of the turn-on and turn-off switching transitions are shown in Figs. 6.18 and 6.19, respectively. The propagation delay through the DS0026 gate drive IC was approximately 12 nsec for turn-on (pull-up) and 10 nsec for turn-off (pull-down). The pre-regulator stage drain voltage waveforms were very clean, especially for square wave operation at 2.25 MHz, indicating minimal inductive parasitics in the pre-regulator stage layout. The turn-on waveform showed a switch commutation period of 14 nsec, with a short 4 nsec Miller effect plateau region. These switching times indicated the layout's successful minimization of parasitic inductance in the gate drive loop as well.

The turn-off transition period was slower than turn-on because the relatively large output capacitance of the MOSFET acted as a turn-off snubber. As the MOSFET channel turns off, the current flowing through the pre-regulator inductor L_{reg} commutates from the channel to this output capacitor, and the reverse voltage across the switch increases slowly as the capacitor charges. This transition is not a resonant ring; the increasing slope of the drain voltage waveform was due to the non-linear nature of the MOSFET junction capacitance. A low-amplitude high frequency ring then occurred as the capacitor voltage was clamped by the pre-regulator rectifier and the parasitic loop inductance of the pre-regulator

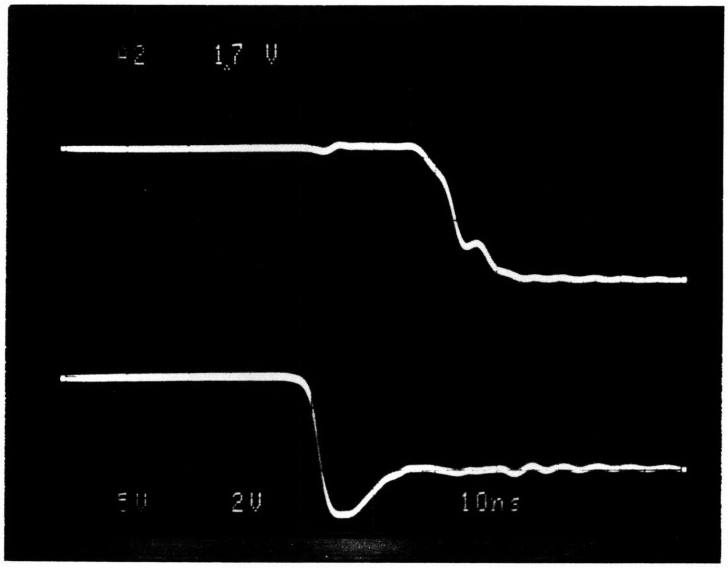


Figure 6.18: Pre-Regulator MOSFET Turn-On

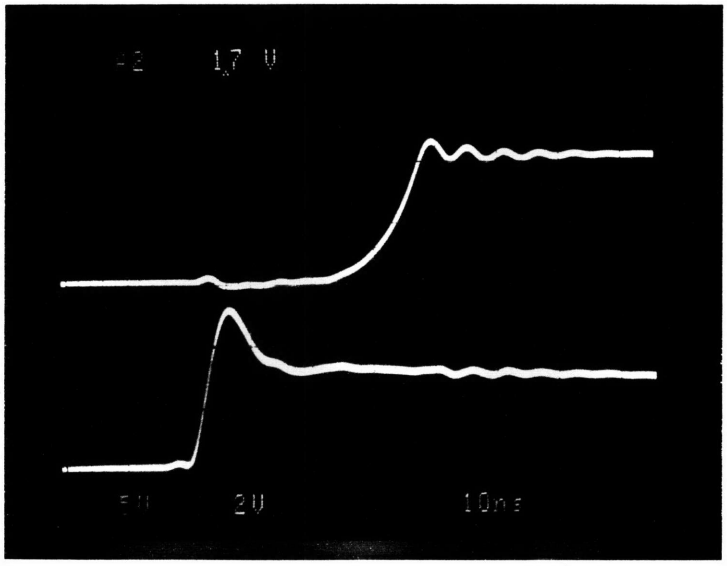


Figure 6.19: Pre-Regulator MOSFET Turn-Off

stage rang with the parasitic output capacitance.

The effect of loading upon the behavior of the pre-regulator stage is shown in Figs. 6.20 and 6.21 for the turn-on and turn-off transitions, respectively. These double-exposed photos were taken with output loads of $3.2A$ and $10.5A$, while the other operating conditions were held constant. The turn-on transition was essentially independent of loading. The turn-off transition increased in speed as loading increased, because the charging current flowing into the parasitic output capacitance of the MOSFET is a linear function of the load current. A slight decrease in the clamp voltage following the turn-off transition was also indicated, corresponding to a decrease in the primary-side bus voltage due to the parasitic resistances in the pre-regulator.

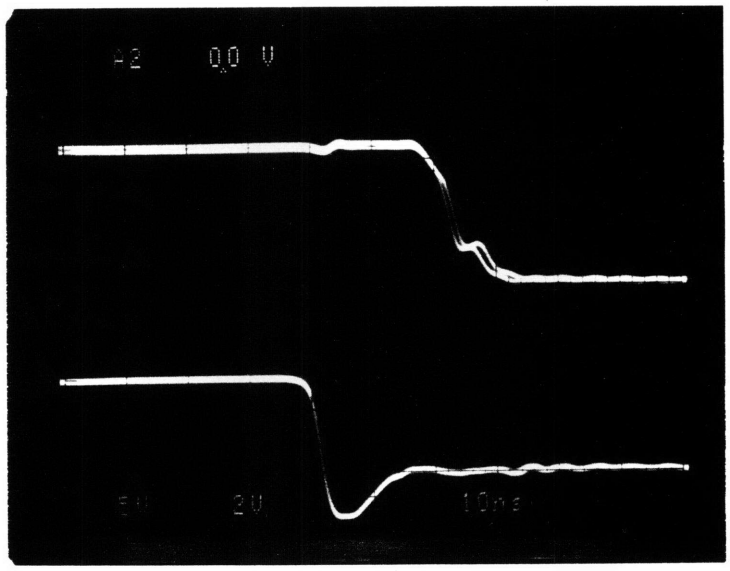


Figure 6.20: Effect of Loading on MOSFET Turn-On

6.3.5 Pre-Regulator Open Loop Control Waveforms

After the operation of the pre-regulator was observed at a 50% duty cycle, the duty cycle was swept over the entire range from 0% to 100%, under fully loaded conditions. The input voltage was adjusted to maintain a $5.0V$ output at all times. The load current was maintained at approximately $I_{out} \approx 10.5A$, and the pre-regulator switching frequency was 2.2 MHz.

The input and output measurements corresponding to operation at 100% duty cycle

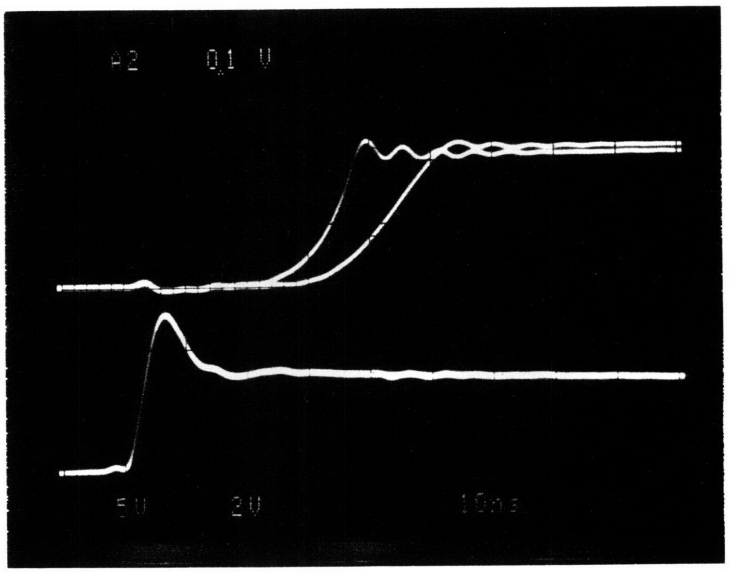


Figure 6.21: Effect of Loading on MOSFET Turn-Off

(corresponding to the pre-regulator switch Q_{reg} being continuously off) were described previously in Section 6.3.3, with reference to Fig. 6.12. Operation with 25%, 50%, and 75% duty cycles is shown in Figs. 6.22 through 6.24. The operating conditions are compiled in Table 6.1, for the range of input voltages and a $5V$ output. The resultant conversion efficiencies are also shown.

Input Voltage V_{in}	Input Current I_{in}	Output Current A	Duty Cycle D	Efficiency η
$39.5V$	1.58	10.6	0%	85%
$37.3V$	1.73	10.6	25%	82%
$34.5V$	1.87	10.5	50%	81%
$32.1V$	2.03	10.4	75%	80%
$29.9V$	2.24	10.5	100%	79%

Table 6.1: Full Power Conversion Efficiency: $5V$, $10A$

The gradual reduction in conversion efficiency was a direct result of increased I^2R losses which grew as the line voltage was lowered and the primary-side current increased. The increase in input current from the first case to the third was also evident in the greater dv/dt of the drain voltage turn-off transition and in the increased parasitic ring amplitude.

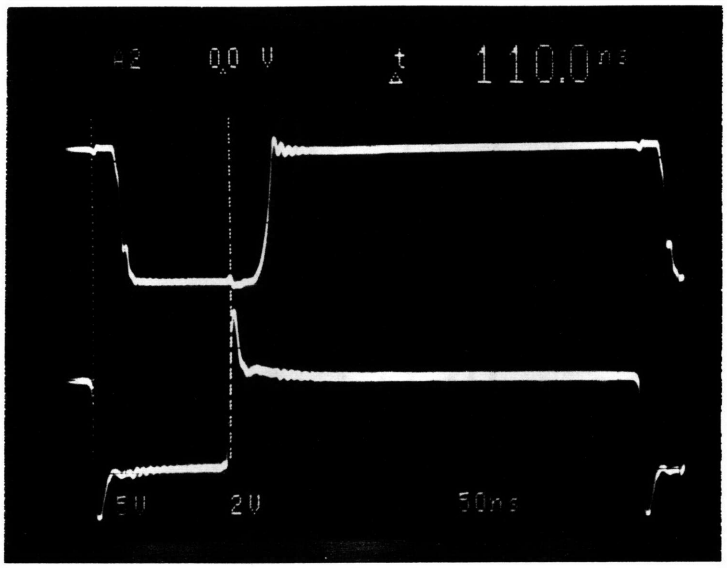


Figure 6.22: Pre-Regulator Control Input and Drain Voltage Waveforms at 25% Duty

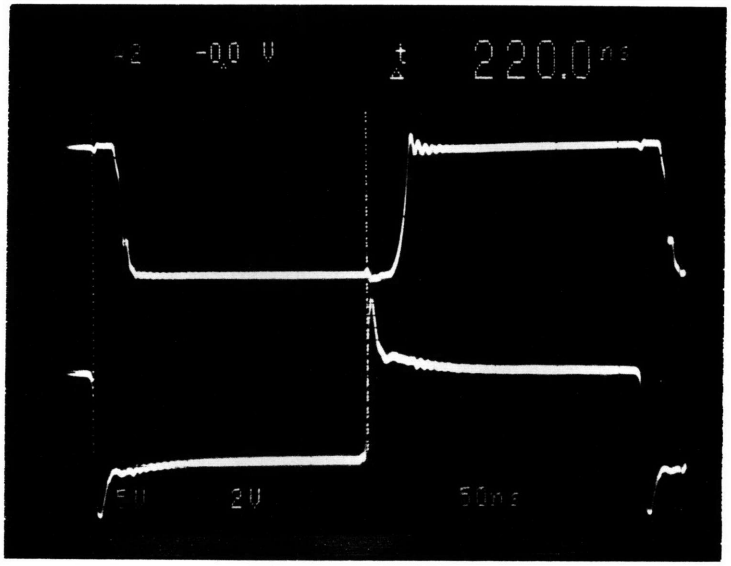


Figure 6.23: Pre-Regulator Control Input and Drain Voltage Waveforms at 50% Duty

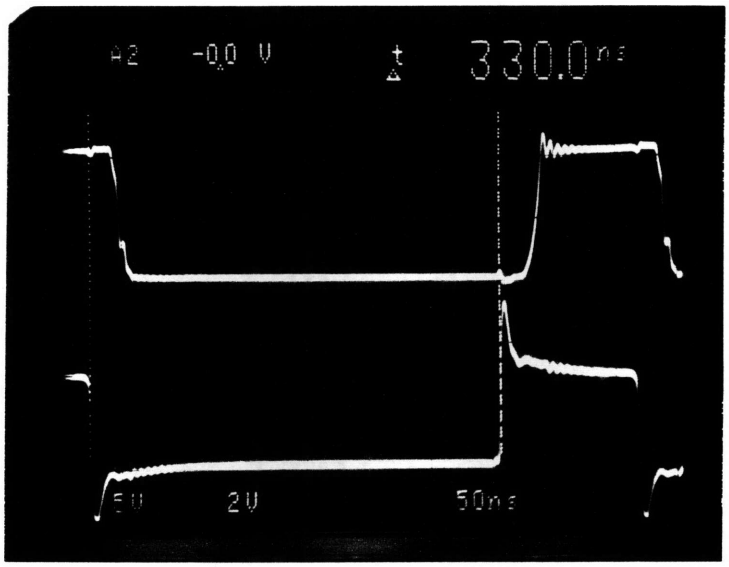


Figure 6.24: Pre-Regulator Control Input and Drain Voltage Waveforms at 75% Duty

Finally, the operation at 100% duty cycle, corresponding to the switch Q_{reg} being constantly on, is shown in Fig. 6.25. As before, the top and bottom waveform traces show the voltage across the pre-regulator MOSFET and the input to the gate drive IC, respectively. However, the trigger was synchronized to the main switches $Q1$ and $Q2$. The voltage across the pre-regulator switch thus represented the conduction drop during each half cycle of the dual converter's operation. With a $2.24A$ input current, this $300mV$ drop gave a pre-regulator MOSFET $R_{DS,on}$ of $135m\Omega$, very close to the manufacturer's specified $120m\Omega$ 'typical' rating for 25°C operation.

6.3.6 Output Ripple Waveform

The final waveform to be recorded was the output ripple. This waveform, shown in Fig. 6.26, was taken under fully loaded conditions at high line. The slight imbalance between half-cycle ripples indicated a corresponding imbalance in load current sharing between the dual converter halves, which could be caused by a number of mechanisms, including the previously discussed causes of *resonant ring* mismatch. In addition, load sharing is particularly sensitive to matching between the forward drops of the output rectifiers. These drops are in turn functions of operating temperature and device fabrication. In general, the mismatches between dual converter halves which were exhibited by these hand-constructed prototypes

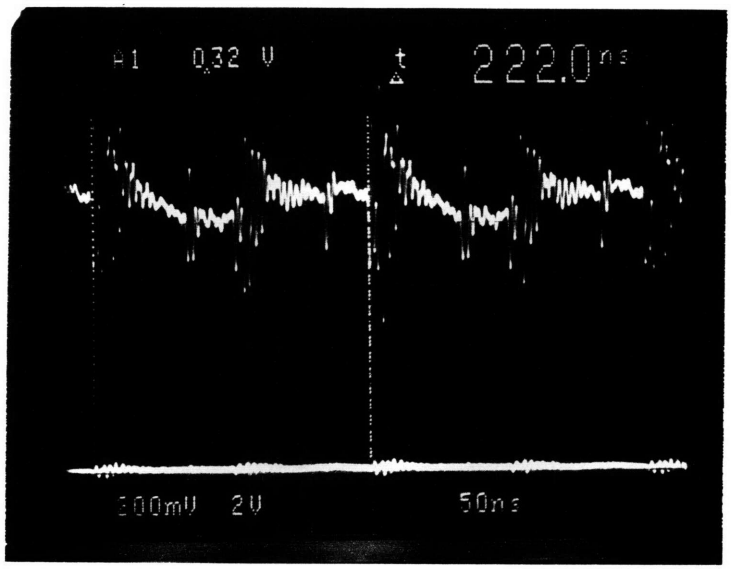


Figure 6.25: Pre-Regulator Control Input and Drain Voltage Waveforms at 100% Duty

were minimal, and would be further reduced by automated mass-production assembly techniques.

The peak-to-peak output ripple was approximately $300mV$, for a ceramic output capacitance of only 800 nF. Later converter prototypes made with triple ceramic capacitor stacks surrounding the output rectifiers increased this capacitance to 2400 nF without increasing the (half-height) converter profile; the resultant output ripple was reduced to $100mV$. A prototype DRFC made with such stacked output filter capacitors was shown in Fig. 5.10. In general, reductions in the magnitude of the output ripple were limited by the poor availability of large-valued high-density ceramic chip capacitors. The viability of stacking multiple components was shown to be one alternative for reducing this ripple; improved capacitors presently under development seem capable of reducing it still further without sacrificing power conversion density.

6.4 Summary of Measurements

Following the documentation of the various waveforms, the operating point measurements were compiled and analyzed. The conversion efficiency was already computed for a number of operating conditions ranging from low-line to high line. The results of the computations

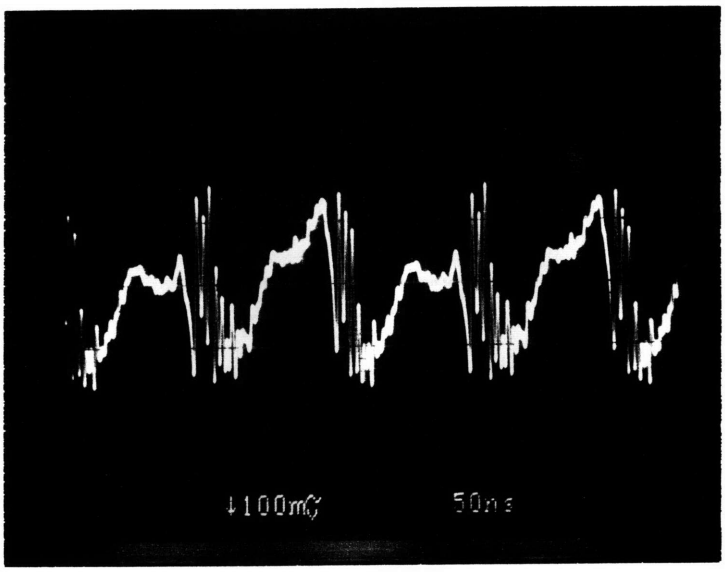


Figure 6.26: Output Voltage Ripple at Full Load

were summarized in Table 6.1, for a pre-regulator operating frequency of 2.25 MHz.

The open loop load regulation was calculated in a similar manner, using the operating point measurements from a series of test conditions. Under conditions of fixed input voltage and pre-regulator duty cycle, the output load was increased and the output voltage recorded. One such series of data points is recorded in Table 6.2. The effective output impedance $Z_{out} = \frac{\Delta V_{out}}{\Delta I_{out}}$, which includes the effects of both resistive and inductive parasitics, is also shown.

V_{out}	I_{out}	Z_{out}	V'_{out}	L_{out}
$5.38V$	$3.00A$		$5.44V$	
		$42m\Omega$		1.39 nH
$5.29V$	$5.13A$		$5.40V$	
		$41m\Omega$		1.43 nH
$5.10V$	$9.80A$		$5.31V$	

Table 6.2: Load Regulation Measurements and Estimates of Parasitics

Using these values for V_{out} as a function of I_{out}, the parasitic inductance portion of the output impedance was calculated. The output resistance of the pre-regulator stage was first computed, extrapolating the change in bus voltage from the pre-regulator MOSFET

drain-source voltage measurements of Section 6.3.4. The resistance was calculated to be

$$\begin{aligned} R_{reg} &= \frac{\Delta V_{bus}}{\Delta I_{in}} \\ &= \frac{0.4\ V}{1.87\ A - 0.64\ A} \\ &= 325m\Omega \end{aligned} \tag{6.1}$$

This value for R_{reg} was then used in (2.17) to solve for the resistive component of the output impedance.

$$\begin{aligned} R_{out} &= [R_{reg} + R_{DS_{on}} + R_{pri}](\frac{N_s}{N_p})^2 + R_{sec} + R_{D_{on}} \\ &= [325m\Omega + 400m\Omega + 65m\Omega](\frac{1}{7})^2 + 2.6m\Omega + 2.7m\Omega \\ &= 21.4m\Omega \end{aligned} \tag{6.2}$$

Using this value for R_{out}, the resistive portion of the change in output voltage was removed from the data points, according to the relationship

$$V'_{out} = V_{out} + I_{out}R_{out} \tag{6.3}$$

The resultant adjusted output voltages V'_{out} are also given in Table 6.2. Using these voltages, the secondary loop inductance component of the output impedance was then estimated as

$$L_{out} = \frac{\Delta V\ \Delta t}{1.5\ \Delta I} \tag{6.4}$$

where Δt is half the switching period at 4.5 MHz and an exponential current waveform was assumed. The load regulation characteristics of the prototype converters thus suggested a total output loop inductance of approximately 1.4 nH. This was reasonably close to the expected value predicted by the design calculations (1.24 nH).

6.5 Summary of Experimental Results

In general, the experimental results presented in the preceding sections of this chapter agreed closely with the expected performance of the prototype converters. The built-in instrumentation provisions proved sucessful in providing non-intrusive documentation of the converter's operation. High frequency performance of the gate drive circuitry was confirmed, with the low-inductance gate drive layouts producing excellent high-speed switch transitions.

The waveform characteristics (resonant frequency, resonant ring amplitude, high frequency leakage inductance ring, etc) that were observed matched the expected results. In addition, the waveforms indicated good matching between the dual halves of the converter. The operating point measurements likewise confirmed the predicted behavior characteristics of the converter, particularly its expected conversion efficiency and open loop load regulation.

The operation of the pre-regulator stage was confirmed over the full duty cycle and load ranges. Furthermore, hybrid construction was shown to be a viable method for constructing *square wave* switching cells capable of operating at frequencies above 1 MHz. The pre-regulator stage operated at 2.25 MHz with minimal loss despite the extreme overrating of the main switching MOSFET. Thus, the concept of pre-regulation was shown to be a viable method for controlling the load voltage.

Equally important, the cleanliness of the observed waveforms confirmed the significant reduction in parasitics afforded by hybrid construction. A virtual absence of ringing on the gate drive and resonant ring waveforms, even at full load, validated the layout techniques used to reduce loop inductances. Significant reductions in the load regulation of the hybrid prototypes as compared to the original PCB versions further illustrated the practicality of the copper hybrid thick film process as an alternative medium for constructing power circuits.

Finally, the successful operation of the half-height transformers illustrated the excellent compatibility between the hybrid assembly process and the barrel-wound FLEX conductor transformer fabrication process. Using these complementary construction techniques, the overall performance of the converter prototype at $50W$ was 85% efficient with a power density of $96W/in^3$.

Chapter 7

Conclusions

This thesis has described the development of a construction method for fabricating efficient high density power conversion units which are suitable for use in distributed power conversion systems. Using a copper thick film hybrid substrate fabrication process specifically developed for assembling power converters, converter operation at 5 MHz was achieved without sacrificing conversion efficiency. The resultant power conversion density of $100W/in^3$ with 85% efficiency was sufficient for point-of-load converter applications in a distributed power system.

7.1 Summary of Work

A thick film substrate fabrication process was developed which could be used in a power circuit context. By employing a copper-based thick film ink system, the prohibitively high cost of gold systems was eliminated. The additional processing complexity associated with the tendency of the copper to oxidize was shown to be manageable. The resultant component interconnection system had extremely low parasitic inductance and resistance as well as good thermal properties, making it ideal for the construction of high frequency switching power converters.

To fully exploit the low inductance characteristics of the thick film interconnection system, a novel transformer winding method was developed which permitted construction of low profile magnetics with reduced leakage inductance. An interleaved barrel winding structure with parallel-planar conductors was fabricated from flexible, double-sided PCB materials, using standard photolithographic and etching techniques. Pairs of transformers constructed with these windings mode had consistently well-matched leakage inductances in the sub-nanoHenry range. Furthermore, the compatibility of the transformer construction

and interconnection substrate fabrication methods facilitated a low-inductance secondary termination loop.

A series of prototype converters were constructed to demonstrate these fabrication methods. The prototype topology consisted of a pair of resonant forward converters operating at a fixed frequency of 5 MHz with a 50% duty cycle, raising the fundamental frequency component of the output ripple to 10 MHz. A 2 MHz square wave PWM pre-regulator was included to provide output voltage control with an associated reduction in conversion efficiency of only 2%.

7.2 Directions for Future Research

The prototype whose construction was described in this thesis was designed to demonstrate the viability of copper thick film hybrid construction as a practical alternative for high frequency power converters. While this was certainly accomplished, the resultant prototypes were not in general suitable for commercial applications. Significant work remains to be done, particularly in the area of component development, before point-of-load conversion becomes a viable commercial solution.

Improvements in capacitor manufacturing, including a few simple modifications such as changes in the package aspect ratios and increased availability of larger values, would greatly reduce their parasitic inductance while eliminating the need for multiple packages. In addition, operation at 5 MHz was accomplished by reducing the transformer's magnetizing inductance, thereby raising the resonant frequency but also increasing the circulating magnetizing currents and associated conduction losses. Far better results could be obtained from an improved MOSFET with reduced parasitic output capacitance. Most importantly, the absence of a PWM controller chip capable of operating in the megaHertz region presently precludes the implementation of closed loop feedback. High frequency controllers with integrated gate drive circuitry and low-inductance bonding pads need to be developed.

Finally, significant increases in power conversion density could be realized by simply modifying the converter layout. For the identical circuit and components, the converter could be reduced in volume by roughly 20% if the constraints imposed by instrumentation, reworkability, and hand assembly were removed. The substrate real estate saved by these reductions alone would accommodate controller/driver ICs for both the pre-regulator and main converter stages, permitting the construction of a complete closed-loop version of the

prototype within the same volume. The further elimination of bias supply and control input pins would actually permit higher power conversion densities using these control ICs. Stand-alone point-of-load power converters, operating at $100W/in^3$ with 85% efficiency, can therefore be realized today by applying existing technologies to a few specific problem areas.

Appendix A

Magnetizing Inductance Volt-Second Integration

The following section details the integration performed in solving for the relationship between the resonant frequency f_{res} of the parasitic tank elements of a resonant forward converter and the resultant switching frequency f_{sw} required for operation at a fixed, 50% duty cycle. The parasitic elements are the magnetizing inductance L_{mag} and the parasitic resonant capacitance C_{res} shown previously in Fig. 2.7.

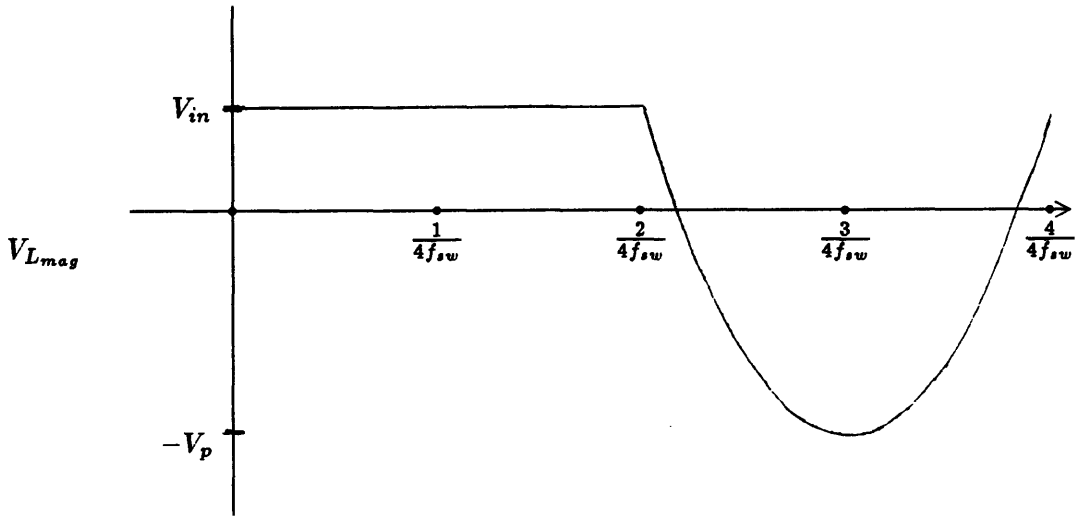


Figure A.1: Voltage Across Magnetizing Inductance

As described in Section 2.1.5, the voltage waveform of the magnetizing inductance is simply the switch voltage V_Q offset by the input voltage V_{in}, as shown in Fig. 2.8 and again here as Fig. A.1. The piecewise description of this waveform, given by (2.10) and (2.11), is

repeated here as (A.1):

$$V_{L_{mag}} = \begin{cases} V_{in} & \text{for } 0 < t < \frac{1}{2f_{sw}} \\ -V_p \cos[2\pi f_{res}(t - \frac{3}{4f_{sw}})] & \text{for } 0 < t < \frac{1}{2f_{sw}} \end{cases} \tag{A.1}$$

Requiring that the piecewise solutions be equal at their intersection, when $t = \frac{1}{2f_{sw}}$, gives the further condition:

$$V_p = \frac{-V_{in}}{\cos(\frac{\pi}{2}\frac{f_{res}}{f_{sw}})} \tag{A.2}$$

For steady-state operation, the total volt-seconds applied to the magnetizing inductance must be zero over each cycle. Using (A.1), the volt seconds during each half-cycle are summed and equated to zero:

$$\int_0^{\frac{1}{2f_{sw}}} V_{in}\, dt - \int_{\frac{1}{2f_{sw}}}^{\frac{1}{f_{sw}}} V_p \cos\left[2\pi f_{res} t - \frac{3\pi f_{res}}{2 f_{sw}}\right] dt = 0 \tag{A.3}$$

$$\frac{V_{in}}{2 f_{sw}} - \frac{V_p}{2\pi f_{res}} \sin\left[2\pi f_{res} t - \frac{3\pi f_{res}}{2 f_{sw}}\right]_{t=\frac{1}{2f_{sw}}}^{t=\frac{1}{f_{sw}}} = 0 \tag{A.4}$$

$$\frac{V_{in}}{V_p} = \frac{f_{sw}}{f_{res}} \frac{2}{\pi} \sin(\frac{\pi}{2}\frac{f_{res}}{f_{sw}}) \tag{A.5}$$

Then, using the continuity condition from (A.2),

$$-\cos(\frac{\pi}{2}\frac{f_{res}}{f_{sw}}) = \frac{f_{sw}}{f_{res}} \frac{2}{\pi} \sin(\frac{\pi}{2}\frac{f_{res}}{f_{sw}}) \tag{A.6}$$

$$\frac{f_{res}}{f_{sw}} = -\frac{2}{\pi} \tan(\frac{\pi}{2}\frac{f_{res}}{f_{sw}}) \tag{A.7}$$

Solving this transcendental equation for the ratio of the resonant frequency to the switching frequency by numerical iteration yields:

$$\frac{f_{res}}{f_{sw}} = 1.29 \tag{A.8}$$

as given in (2.13).

Appendix B

Magnetic Energy Density Integration

The magnetic energy integrations required to solve the leakage inductance estimations of Chapter 4 are described in this Appendix. It is shown that, for a general scalar function $F(\rho)$ which varies linearly between zero and some peak value F_o as a function of radius, the integral of the square of this function throughout a cylindrical volume can be described in terms of the area under the graph of the original function. The two cases of linearly increasing and linearly decreasing functions are considered separately.

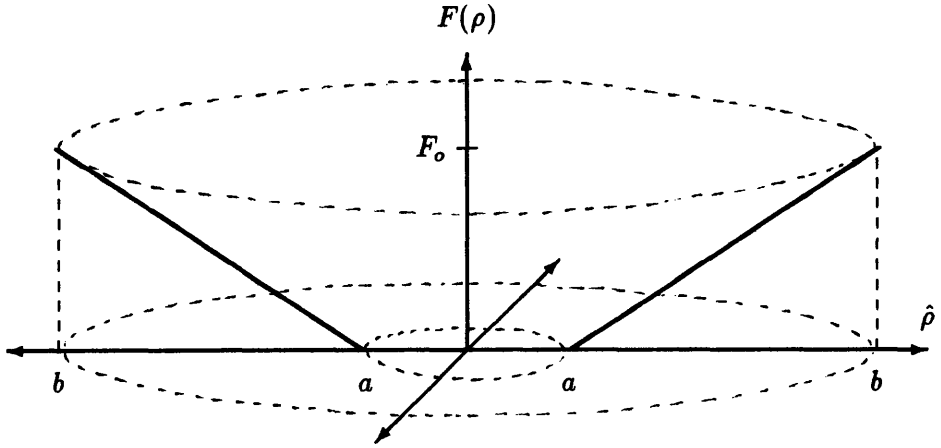


Figure B.1: Volume Integration of Linearly Increasing Function $F(\rho)$

The linearly increasing function $F(\rho)$ shown in Fig. B.1 is described by the equation

$$F(\rho) = F_o(\frac{\rho - a}{b - a}) \tag{B.1}$$

The integral of the square of this function throughout a cylindrical volume is

$$\int_V dV\,[F(\rho)]^2 = \iiint \rho\,d\rho\,d\phi\,dz\,[F_o(\frac{\rho-a}{b-a})]^2 \tag{B.2}$$

$$= 2\pi h\,\frac{F_o^2}{(b-a)^2}\int_a^b \rho\,(\rho-a)^2\,d\rho \tag{B.3}$$

$$= 2\pi h\,\frac{F_o^2}{(b-a)^2}\int_a^b (\rho^3 - 2a\rho^2 + a^2\rho)\,d\rho \tag{B.4}$$

$$= 2\pi h\,F_o^2\,\frac{3b^2-2ab-a^2}{12} \tag{B.5}$$

where h is the height of the cylinder. This solution can be written in terms of the one-dimensional integral of $F(\rho)$, i.e., in terms of the area under the graph of $F(\rho)$. This area is

$$A_{ab} = \frac{F_o(b-a)}{2} \tag{B.6}$$

The solution in terms of this area is

$$\int_V dV\,[F(\rho)]^2 = 2\pi h\,[\frac{F_o(b-a)}{2}]^2\,\frac{b+a/3}{b-a} \tag{B.7}$$

$$= 2\pi h\,[A_{ab}]^2\,\frac{b+a/3}{b-a} \tag{B.8}$$

When the outer radius of integration is much larger than the inner radius, so that $b >> a$, this solution simplifies to

$$\int_V dV\,[F(\rho)]^2 \approx 2\pi h\,[A_{ab}]^2 \tag{B.9}$$

The volume integral of the linearly increasing function $F(\rho)$ has thus been found in terms of a simple triangular area.

The solution to the linearly *decreasing* problem is solved in an analogous manner. The function $G(\rho)$ shown in Fig. B.2 is first defined to be

$$G(\rho) = G_o(\frac{c-\rho}{c-b}) \tag{B.10}$$

where the constant G_o is now the peak value. The integral of the square of this function throughout a cylindrical volume is then equal to

$$\int_V dV\,[G(\rho)]^2 = \iiint \rho\,d\rho\,d\phi\,dz\,[G_o(\frac{c-\rho}{c-b})]^2 \tag{B.11}$$

$$= 2\pi h\,\frac{G_o^2}{(c-b)^2}\int_b^c \rho\,(c-\rho)^2\,d\rho \tag{B.12}$$

$$= 2\pi h\,\frac{G_o^2}{(c-b)^2}\int_b^c (\rho^3 - 2c\rho^2 + c^2\rho)\,d\rho \tag{B.13}$$

$$= 2\pi h\,G_o^2\,\frac{c^4 - 6b^2c^2 + 8cb^3 - 3b^4}{12} \tag{B.14}$$

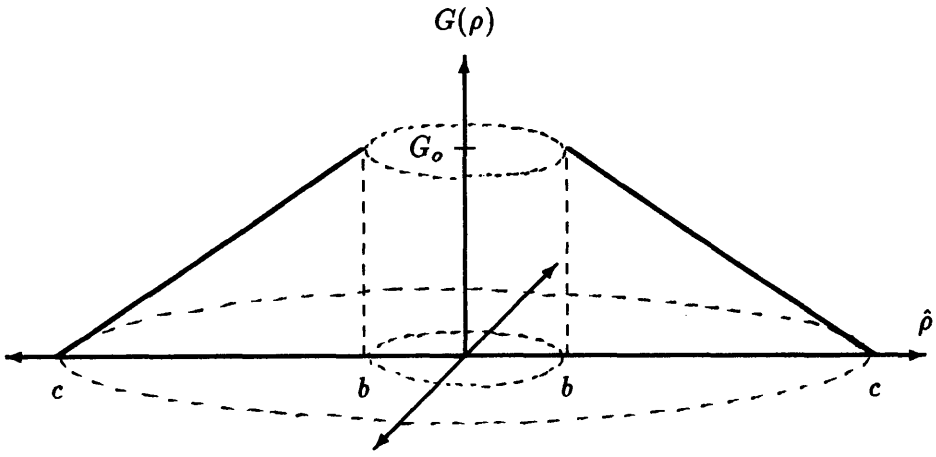


Figure B.2: Volume Integration of Linearly Decreasing Function $G(\rho)$

where h is again the cylinder height. This solution can be also be written in terms of a one-dimensional area integral. For the function $G(\rho)$, this area is

$$A_{bc} = \frac{G_o(c-b)}{2} \tag{B.15}$$

The solution in terms of this area is

$$\int_V dV\,[F(\rho)]^2 = \frac{2\pi h}{3}\,[\frac{G_o(c-b)}{2}]^2\,\frac{c+3b}{c-b} \tag{B.16}$$

$$= \frac{2\pi h}{3}\,[A_{bc}]^2\,\frac{c+3b}{c-b} \tag{B.17}$$

Again, when the outer radius of integration is much larger than the inner radius, so that $c >> b$, this solution simplifies to

$$\int_V dV\,[G(\rho)]^2 \approx \frac{2\pi h}{3}\,[A_{ab}]^2 \tag{B.18}$$

Both solutions are now in terms of the area under the function $G(\rho)$.

The particularly simple form of the solutions permits linearly changing functions to be squared and integrated in a convenient manner. When the functions are descriptions of the $\overline{B}$ field profiles within a core volume, the integration of the stored magnetic energy can therefore be performed essentially by inspection. This in turn facilitates estimation of the leakage inductance of various transformer designs. The application of these solutions in such a context was demonstrated in Sections 4.2.2 and 4.2.3.

Appendix C

2-B Process Schottky Characteristics

The inherent speed and low forward voltage drop afforded by schottky barrier devices as compared to standard junction diodes make them attractive for applications where power dissipation is a critical consideration. The schottky rectifier dice used in the construction of the final converter prototypes were specially developed for high frequency switching power converter applications as part of an industrial research program at International Rectifier. The forward drop of these rectifiers was reduced by minimizing the resistive drops which occur in the substrate bulk. A high conductivity, high purity silicon material achieved this reduction without excessive doping, which can greatly increase reverse leakage currents.

Curves showing the forward voltage drop as a function of forward current are given in Figs. C.1 and C.2. These curves were generated by the manufacturer as part of an internal process evaluation program. The graphs correspond to the 90 mil and 125 mil dice used for the pre-regulator and output rectifiers, respectively. Independent measurements verified these operating specifications for the particular components used. In addition, the reverse breakdown voltage of the devices was found to be approximately $-37V$, at knee currents of $2.4mA$ and $7.0mA$, respectively.

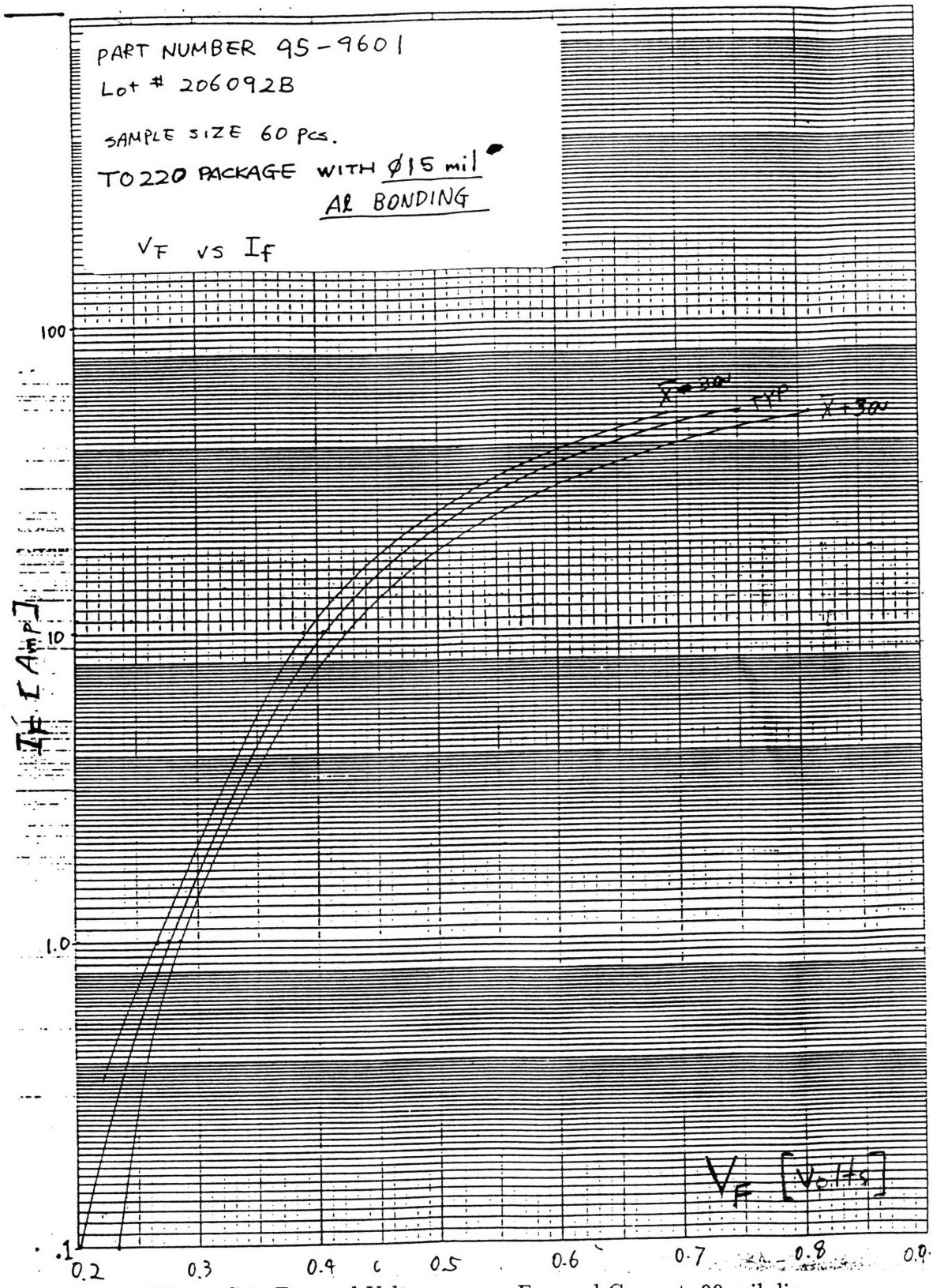


Figure C.1: Forward Voltage versus Forward Current, 90 mil die

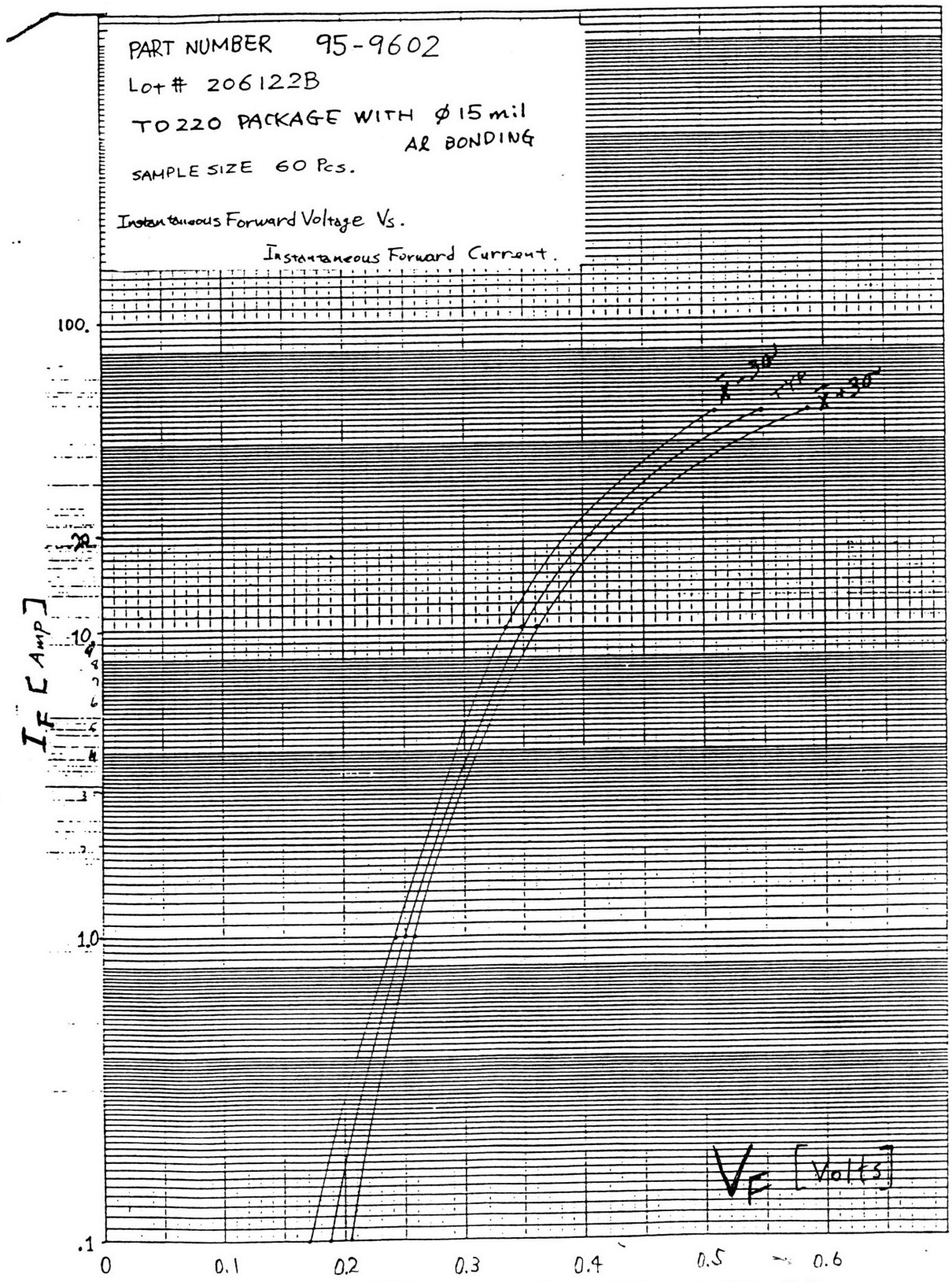


Figure C.2: Forward Voltage versus Forward Current, 125 mil die

Appendix D

Hybrid Layout Thick Film Masks

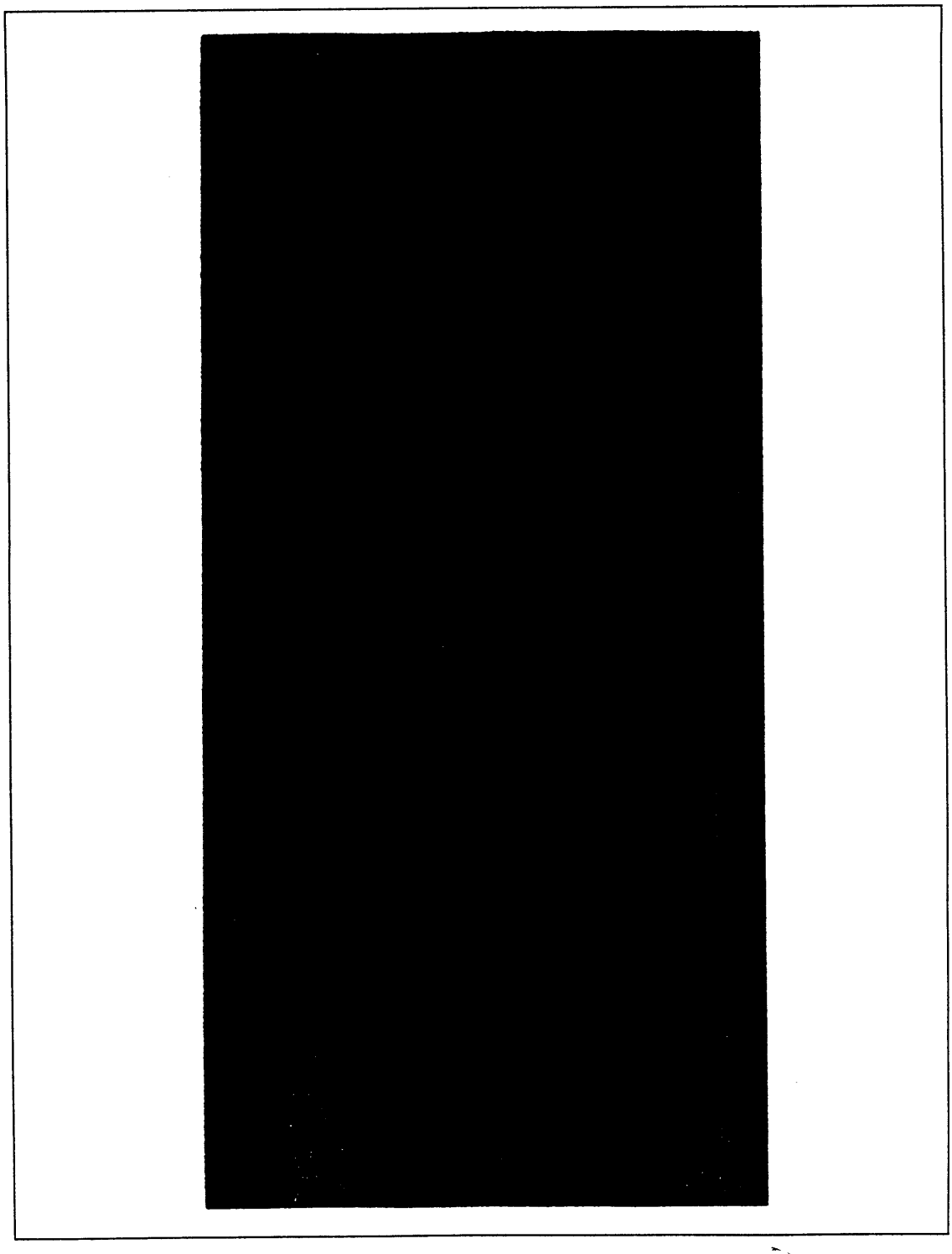


Figure D.1: Heatsink Mask

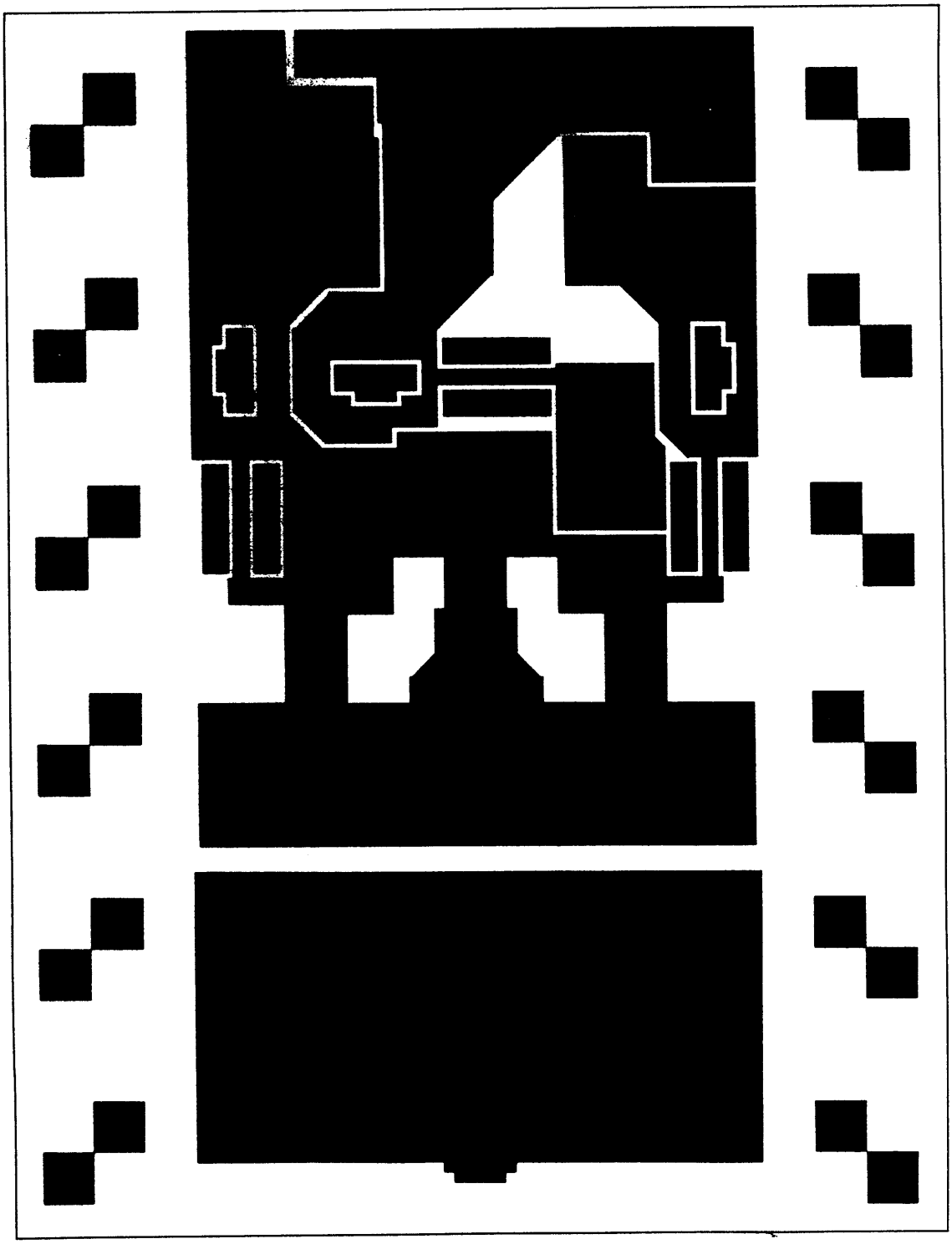


Figure D.2: Metal 1 (Ground Plane) Mask

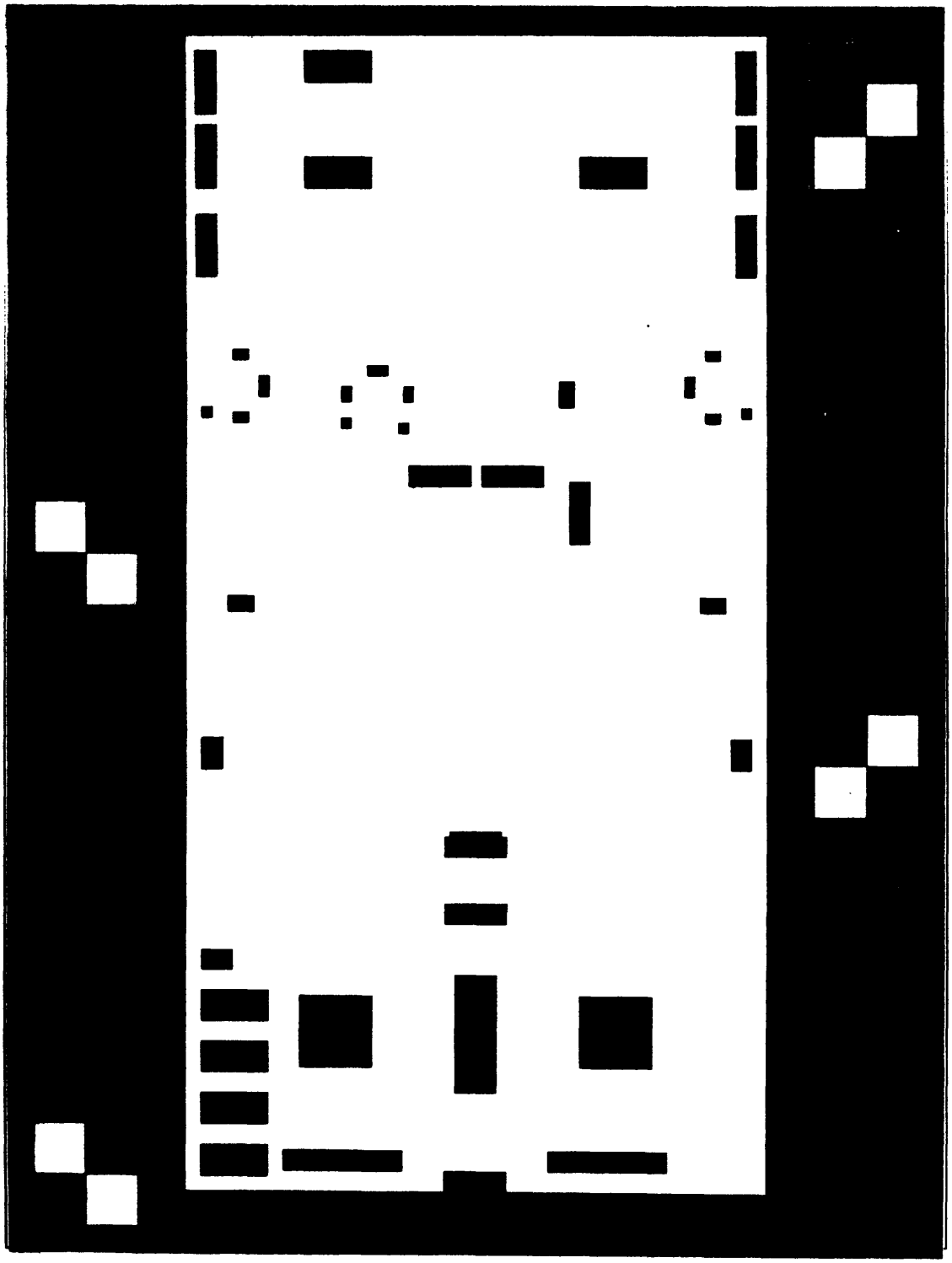


Figure D.3: Dielectric Mask

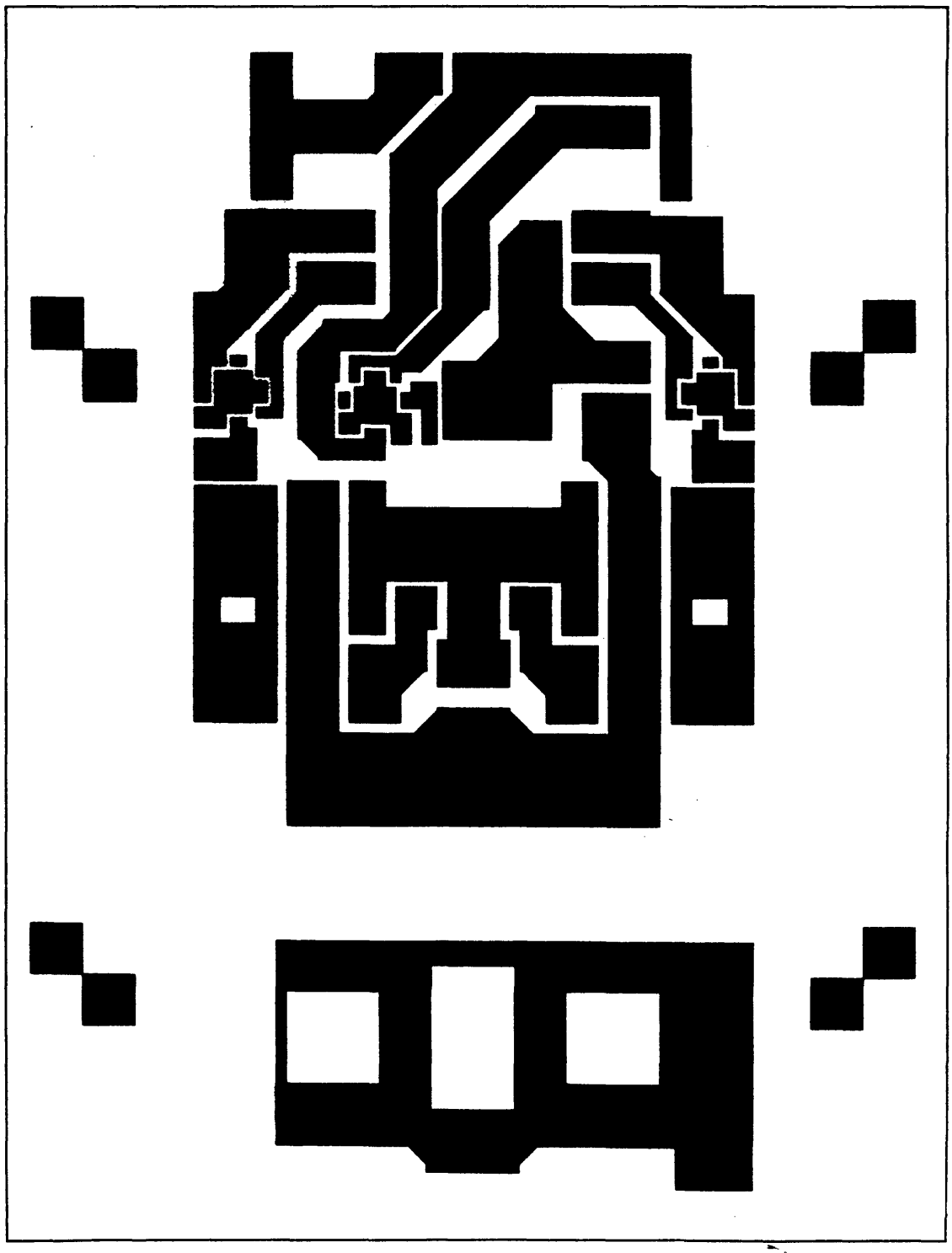


Figure D.4: Metal 2 (Interconnect) Mask

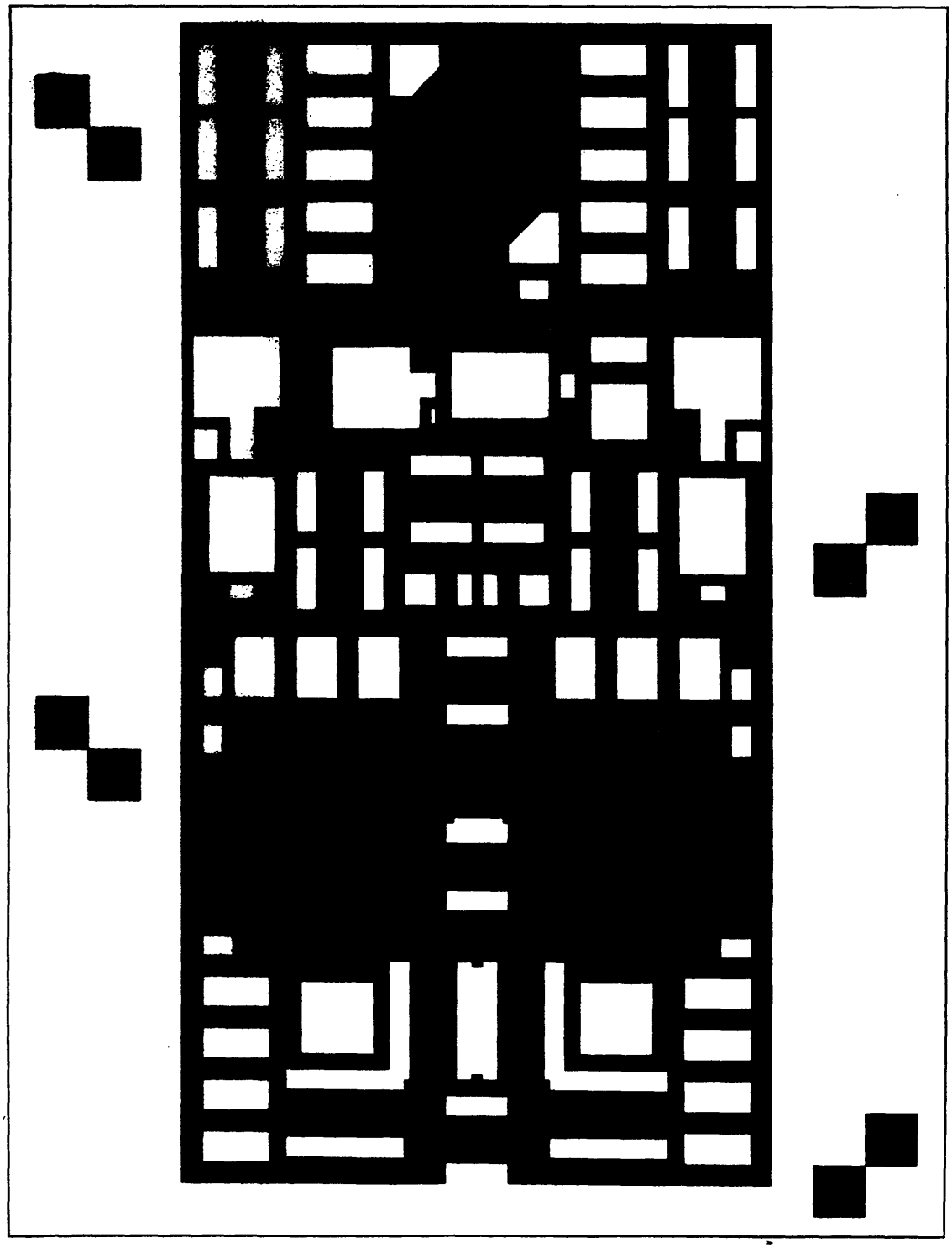


Figure D.5: Glass Encapsulant Mask

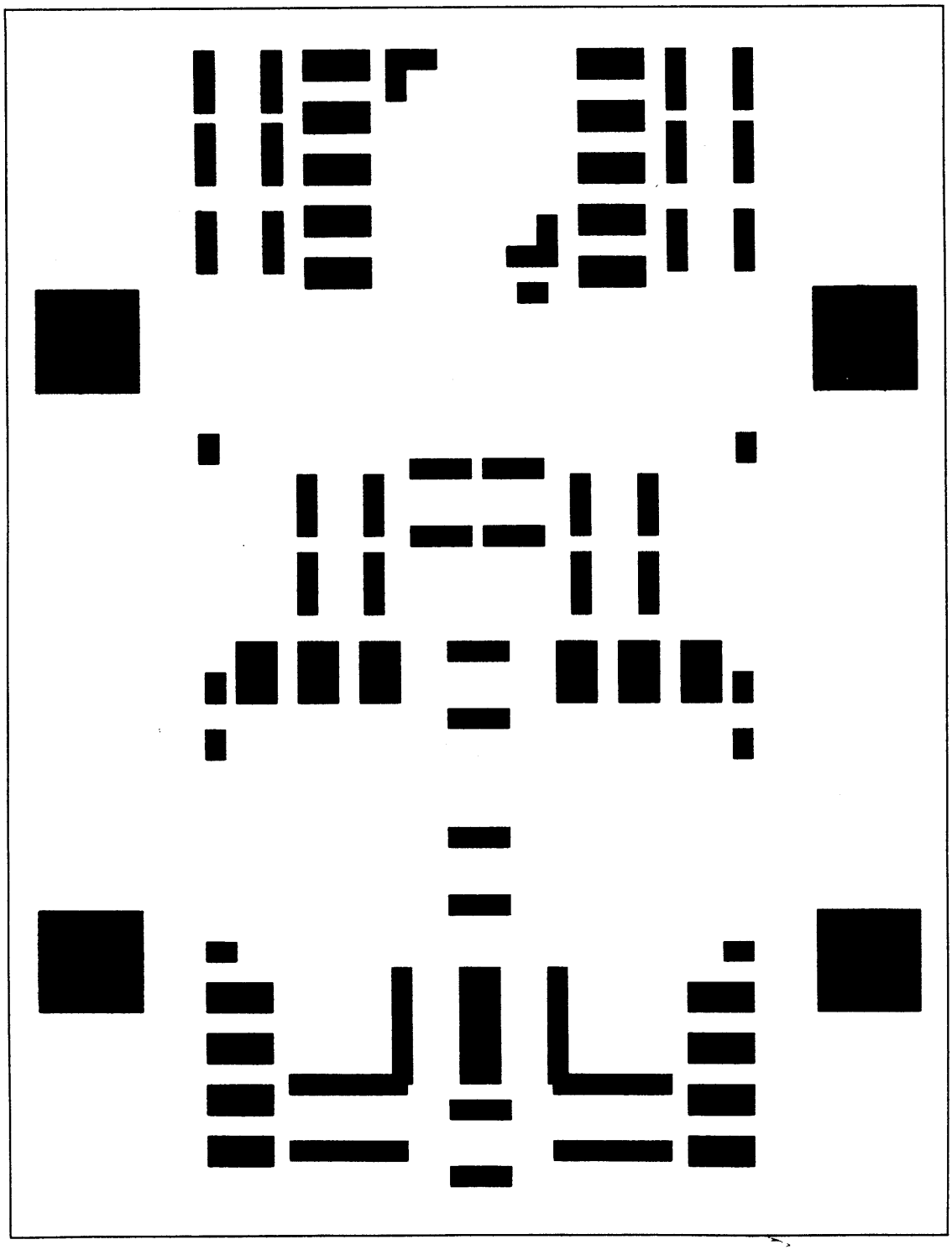


Figure D.6: Solder Mask

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