

Design and Evaluation of a Very High Frequency dc/dc Converter

by

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Abstract

This thesis presents a resonant boost topology suitable for very high frequency (VHF, 30-300 MHz) dc-dc power conversion. The proposed design is a fixed frequency, fixed duty ratio resonant converter featuring low device stress, high efficiency over a wide load range, and excellent transient performance. A 110 MHz, 23 W experimental converter has been built and evaluated. The input voltage range is 8-16 V (14.4 V nominal), and the selectable output voltage is between 22-34 V (33 V nominal). The converter achieves higher than 87% efficiency at nominal input and output voltages, and maintains efficiency above 80% for loads as small as 5% of full load. Furthermore, efficiency is high over the input and output voltage range.

In addition, a resonant gate drive scheme suitable for VHF operation is presented, which provides rapid startup and low-loss operation. The converter regulates the output using high-bandwidth on-off hysteretic control, which enables fast transient response and efficient light load operation. The low energy storage requirements of the converter allow the use of coreless inductors, thereby eliminating magnetic core loss and introducing the possibility of integration. The target application of the converter is the automotive industry, but the design presented here can be used in a broad range of applications where size, cost, and weight are important, as well as high efficiency and fast transient response.

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Introduction

POWER electronics today are facing increasing demands for miniaturization, improved efficiency, and reduced cost. In dc-dc power conversion a switched topology is often the only way to achieve reasonable efficiency. By using semiconductor switches and energy storage devices that ideally do not dissipate energy, high efficiency can be achieved. The trade-off for high efficiency is in the cost and size of the passive energy storage, which can often-time be the dominant factor for a given topology. In order to reduce the size of the passive components, it is necessary to increase the switching frequency.

The incentive to move to higher frequencies is not only given by the reduced sizes of the passive components, but also by transient performance. With smaller capacitors and inductors, less energy is stored in the converter, allowing for a faster response to a change in load. It is thus clear that much can be gained from moving to a design that enables operation at very high frequency

There is, however, a cost to be paid for moving up in frequency. Semiconductor losses increase with frequency, as do magnetic core losses. This is why the fastest conventional dc-dc converters today are switched at frequencies less than 10 MHz. Power converters that operate at above 10 MHz are often resonant topologies, which reduce switching loss and often absorb the semiconductor parasitics. The use of resonant converters for dc-dc power conversion introduces many new challenges in the areas of control, design, modeling, and layout. This thesis presents an approach to overcome those challenges, and through experimental results illustrates the substantial benefits that can be realized once those challenges are overcome.

1.1 Research Background

In conventional, hard-switched, power converters the power loss associated with each switching cycle is what often sets an upper bound on frequency of operation. During turn-on and turn-off of the semiconductor switches, the currents and voltages cannot change instantaneously. The resulting current-voltage overlap results in a power loss, which increases linearly with frequency.

One way to maintain high efficiency at high frequency is to employ a low switching-loss converter topology, incorporating Zero-Voltage-Switching (ZVS), or Zero-Current-Switching (ZCS). These techniques are also often referred to as soft switching [1–5]. Resonant converters can provide these features by using resonant elements (capacitors and inductors) to control the switch voltage and/or current during on-off transitions. Resonant topologies are frequently used in radio-frequency (rf) amplifiers, and many of the techniques used in that field can also be applied to dc-dc converters [6].

A structural design similar to that of Figure 1.1 is often employed in resonant dc-dc converters [7–12]. At the input stage a resonant inverter converts the input dc voltage to a high frequency ac voltage. A transformation stage then performs the requisite voltage transformation, and a resonant rectifier transforms the ac waveform back to dc. Not explicitly shown in Figure 1.1 are input and output filters - components that are often required to ensure that the converter meets safety and performance specifications.

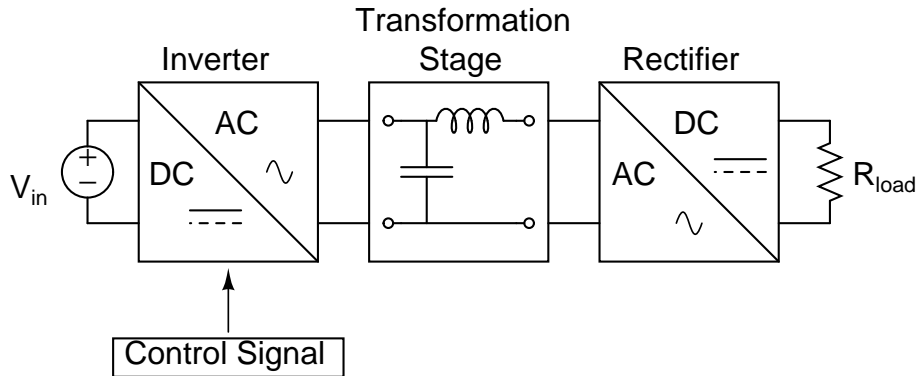


Figure 1.1: Block diagram illustrating the structure of a very high frequency dc-dc converter.

Although the use of resonant power converters enables operation at higher frequencies

than conventional hard-switched designs, it also introduces some new challenges. One example is control of the converter, which becomes more difficult as frequency increases. Frequency control is often used to regulate resonant converters. However, this typically yields poor efficiency at light load due to the many loss components that do not scale back with power, and due to the variation in circuit waveforms as frequency is adjusted. Likewise, another commonly used control strategy - pulse-width modulation, also finds limited use at very high frequency. This is because achieving duty ratio control is difficult (and typically unattractive from a gate drive loss perspective) at high frequencies, and because the performance of many resonant topologies is very sensitive to duty ratio.

In addition to being challenging to control, resonant converters often suffer from poor light load performance, as discussed in [3, 6–8, 10, 13, 14]. In some converters the resonant elements that help achieve ZVS conditions are sized for a specific load impedance. As the load impedance changes, ZVS can no longer be maintained, resulting in increased switching loss and consequently lower efficiency. Other topologies maintain ZVS conditions across the load range, but incur much higher resonant losses at light load due to increased circulating currents in the resonant elements. Because of this characteristic of resonant converters, care must be taken in our design to maintain high efficiency at light load.

One technique that has proven useful to control VHF dc-dc power converters is on-off control [12, 15, 16], also known as cell-modulation control [12, 16] or burst-mode control. In the simplest version of this approach, an rf converter cell is optimized for a narrow load range and fixed frequency and duty ratio. To control power, the entire cell is modulated on and off (bang-bang control) such that the average power delivered to the output is as needed to regulate the output voltage. Moreover, this strategy can be extended for use with multiple converter cells [12]. As the load varies, the number of cells in use is changed, allowing for efficient operation over a wide load range. This approach allows the benefits of resonant converters to be realized (high efficiency at very high frequency) while maintaining high efficiency at light load. It is important to realize that the passive elements of the converter can be made very small, as they are sized by the rf switching frequency. In addition to reducing the converter size, this approach greatly improves the transient performance, since very little energy is stored in the passives in each switching cycle. The only passive component that needs to be sized based on the modulation frequency (the frequency at which the converter cell is modulated on and off) is the output filter capacitor.

The benefits in terms of size, cost, and transient performance makes the cell-modulated architecture an attractive option.

1.2 Thesis Objectives, Contributions, and Organization

The goal of this thesis is to design and build a very high frequency (VHF, 30-300 MHz) dc-dc converter with the following specifications:

- Input Voltage: 8-16 V
- Output Voltage (selectable): 22-34 V
- Switching Frequency: 110 MHz
- Output Power Rating: 15-25 W

As Chapter 2 will illustrate, conventional power converters cannot operate at the high frequency desired while maintaining acceptable efficiency. Section 2.2 describes the common solution for high frequency dc-dc power conversion - resonant topologies. In addition to providing background and discussion of previous work, it also highlights some limitations and undesirable characteristics of conventional resonant converters.

In Chapter 3, a resonant boost topology suitable for VHF operation is introduced which overcomes many of the limitations outlined in Section 2.2. The design features a fixed frequency, fixed duty ratio highly efficient inverter stage coupled with a resonant rectifier. Detailed design procedures are presented for the inverter and rectifier stages in Sections 3.1 and 3.2, respectively.

To achieve high performance and efficiency, much care must be taken in the choice and modeling of the the main semiconductor switch. A detailed analysis of the essential parameters governing semiconductor loss is presented in Chapter 4, as well as semiconductor **SPICE** models appropriate for simulation of the complete converter. The chapter also presents a qualitative comparison between a number of possible high performance rf MOSFETs for use in VHF dc-dc power converters.

Chapter 5 introduces a low-loss resonant gate drive scheme suitable for VHF operation. This approach, which is closely related to that introduced in [16], provides rapid startup and shutdown as well as low parts count. The converter utilizes a high bandwidth hysteretic controller for on-off control, providing fast transient response and good efficiency over a wide load range. The details of the control scheme are presented in Chapter 6.

Chapter 7 discusses design and layout considerations for VHF dc-dc converters. The chapter also provides component values for the Φ_2 -based power stage, resonant gate drive circuit, and the on/off control circuitry of an experimental prototype. In addition, photographs with labelled components are presented along with schematics illustrating critical loops from a layout perspective.

Chapter 8 provides experimental measurements and evaluations of the converter. Important characteristics such as efficiency, power, output voltage ripple and transient performance are evaluated for different operating points.

Finally, Chapter 9 concludes the thesis with a summary of the contributions of this work and a discussion of possible future research directions.

Power Converter Topologies

IN the quest for higher power densities the trend in power electronics has been to operate at higher frequencies. Typically, power converters operate at the highest frequency possible for a given efficiency specification. One loss mechanism that typically limits the operating frequency of conventional dc-dc converters is switching loss, which increases linearly with frequency. Much work [1–5] has therefore focused on new topologies that mitigate the switching loss, thereby allowing an increase in switching frequency. The following section will briefly discuss hard switched converters and their limitations, followed by a treatment of resonant soft-switched converters. The chapter will conclude with a survey of a subset of resonant topologies suitable for dc-dc power conversion, along with a discussion of their respective restrictions.

2.1 Hard Switched Converters

There are many different topologies of hard switched dc-dc converters, but their switching loss mechanisms are similar. The concept of switching loss will here be illustrated by the classic buck converter, shown in Figure 2.1 [17]. The subsequent switching loss discussion makes many simplifying assumptions such as that of linear parasitic capacitors, which is certainly not the case in real devices. This analysis only aims to illustrate the *concept* of switching loss, not to give a full derivation of all subtleties involved in this loss mechanisms. For a more thorough discussion of switching loss, please refer to [?].

Figure 2.2 shows the drain-to-source voltage and current during the MOSFET’s off-to-on transition. In this example, the diode is assumed to be ideal. Initially, the MOSFET is turned off, and the diode is carrying all of the load current, I_o . Before the diode can turn off, the MOSFET current must rise from 0 to I_o . This transition is illustrated in Figure 2.2

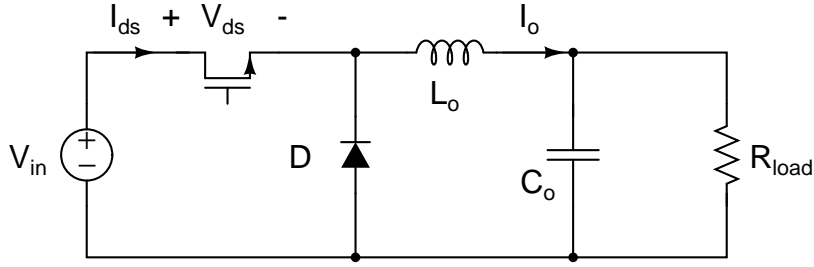


Figure 2.1: *Buck Converter - a conventional, hard switched, converter.*

as the time between t_0 and t_1 . During this time the MOSFET supports both a high voltage and a high current, which results in a power loss. At time t_1 the diode becomes reverse biased and turns off, allowing the drain-to-source voltage V_{ds} to fall to 0. The instantaneous power dissipated in the MOSFET is given by the product $V_{ds}I_{ds}$, and is shown as the shaded triangle in the lower graph of Figure 2.2. Assuming piecewise linear waveforms, the energy lost during each turn-on transition is then simply given by:

$$W_{on} = \frac{1}{2}V_{ds}I_{ds}(t_2 - t_0) \quad (2.1)$$

The transition times t_0 through t_2 are not instantaneous because of the parasitic capacitances associated with the MOSFET, and the charging and discharging of these take a finite amount of time. The parasitics of the MOSFET will be discussed further in Chapter 4. In the case of the turn-on transition, there is one additional loss mechanism. The energy stored in the parasitic drain-to-source capacitor is dissipated through the MOSFET to ground, resulting in an energy loss of $\frac{1}{2}CV^2$ (for the simplifying case of linear capacitor, which is an idealization). The energy lost in the turn-off transition, W_{off} , is similar to the one described by Equation 2.1, resulting in a total energy loss per switching cycle of $W_{sw} = W_{off} + W_{on}$. Since this happens once every switching cycle, this power loss clearly increases linearly with frequency. Although the energy lost in each cycle is relatively small, the resulting switching loss can cause a significant drop in converter efficiency as we move to high frequencies.

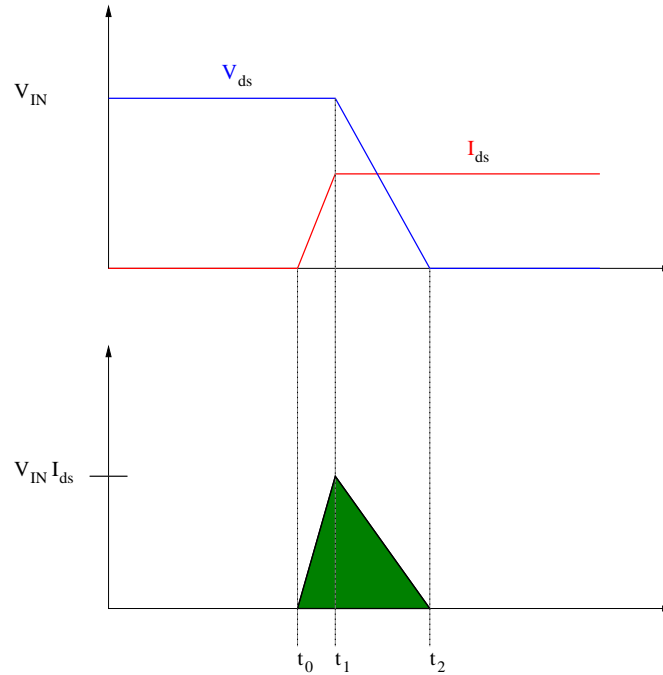


Figure 2.2: Drain-to-source voltage and current waveforms during an off-to-on transition of the buck converter of Figure 2.1.

2.2 Soft Switching Converters

In order to reduce switching loss, it is desirable to control the voltage and/or current to eliminate the overlap illustrated in Figure 2.2. By ensuring that the on/off transitions of the semiconductor devices occur at time when the waveform of interest (voltage or current) is zero, soft switching can be achieved. Resonant converters typically achieve this by using reactive networks to significantly reduce the semiconductor current or voltage during switching. Many types of soft switching converters exist [1–5], and they can be classified as zero-voltage switching (ZVS), zero-current switching (ZCS), or both. All have in common that they reduce the switching loss experienced in hard switched converters. Many of them also have the added advantage of absorbing the parasitics as part of their resonant network, and to recover the energy stored in the parasitics. If the switching frequency is sufficiently high, some discrete components of the resonant network can be completely replaced by the parasitics. Although this requires tighter control of the semiconductor parasitics than is found in conventional converters, it is nevertheless a powerful idea: exploiting the parasitics

to achieve higher performance and power density

A typical penalty for reducing switching loss in resonant soft-switched converters is the higher device stresses [2, 3, 6–10, 13, 14, 16, 18, 19], as well as higher conduction losses. Furthermore, as can be seen in [3, 6–8, 10, 13, 14], it is often difficult to maintain high efficiency over a wide load range with resonant converters. As a practical illustration the following section will examine some of these limitations seen in the Class E inverter [20], which is a common resonant topology used in dc-dc power converters [?, 7, 10, 12, 13]. Other resonant topologies exhibit similar characteristics.

2.2.1 Class E Inverter

The Class E inverter, depicted in Figure 2.3, is a highly efficient resonant topology often used in rf power amplifiers. Its successful use in resonant dc-dc power converters is also well known [6, 7, 9, 12].

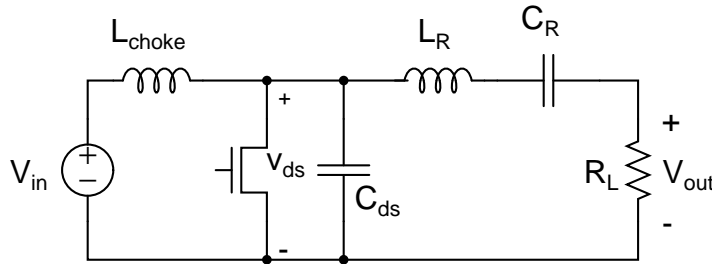


Figure 2.3: *Class E inverter. C_{ds} comprises parasitic device capacitance and possibly added discrete capacitance.*

The input inductor L_{choke} is large enough so that the current through it can be considered constant and inductor approximates an open circuit at radio frequencies. The resonant tank (L_R, C_R, R_L) is tuned in conjunction with C_{ds} to provide a switching waveform with zero voltage and zero time-derivative of voltage at turn-on. Furthermore, the switch voltage rise at turn-off is delayed until the current has decreased to zero. These conditions, which reduce switching loss by time-displacement of switch voltage and current, are known as *Class E switching conditions*.

When used in dc-dc power converters, the trade-off for low switching loss in the Class E

inverter are certain undesirable characteristics that limit miniaturization and performance:

- The RF choke inductor L_{choke} is relatively large, limiting transient performance and miniaturization.
- Voltage device stresses are high ($V_{ds_{peak}} \geq 3.6 V_{in}$), requiring the use of less efficient semiconductors.
- Output power is tightly dependent on C_{ds} .

Topologies that address some of these issues have been developed, such as the ‘Even Harmonic Resonant Class E’ [21, 22], which reduced the size of the RF choke inductor. Others, such as the Class F inverter [23, 24] use harmonic frequency resonators to shape the drain waveform to reduce device voltage stress. However, practical implementation of these types of inverters exhibit significant overlap of drain-to-source voltage and current (i.e., do not operate in “switched-mode”), thus decreasing efficiency, making them unsuitable for dc-dc converter applications.

Inverters that both reduce device stress and energy storage requirements are presented in [25, 26] (termed Class Φ for their relation to the traditional Class F). However, the proposed solutions employ high-order resonant structures requiring many passive components, which may not be realizable in all applications.

As this chapter has illustrated, resonant converters provide good efficiency for very high operating frequency due to reduction of switching loss. There is, however, a need for resonant topologies that provide reduced switch stress - enabling the use of more efficient semiconductor switches with lower device breakdown. Furthermore, in order to achieve miniaturization, and possibly integration, resonant topologies that employ small-valued passive components are highly desirable.

Resonant Boost Converter

THE limiting properties of existing resonant topologies highlighted in Chapter 2 motivates the investigation of new topologies better suited for dc-dc power conversion. This chapter introduces a new resonant boost topology that has been developed specifically to address some of the shortcomings of earlier solutions. The converter, shown in Figure 3.1 can be viewed as a special version of the Class Φ inverter, described in [25–29], coupled with a resonant rectifier. The design was developed with on-off control in mind (explained in detail in Chapter 6) and can therefore be optimized for low device stress and high efficiency at a fixed frequency and duty ratio. This enables the use of low-loss resonant gating which together with zero-voltage switching provides efficient operation in the VHF region. Section 3.1 explains the operation and design of the inverter stage, followed by details of the rectifier design and its coupling to the inverter stage in Section 3.2. Section 3.3 concludes the chapter with simulated converter waveforms and converter loss breakdown by component.

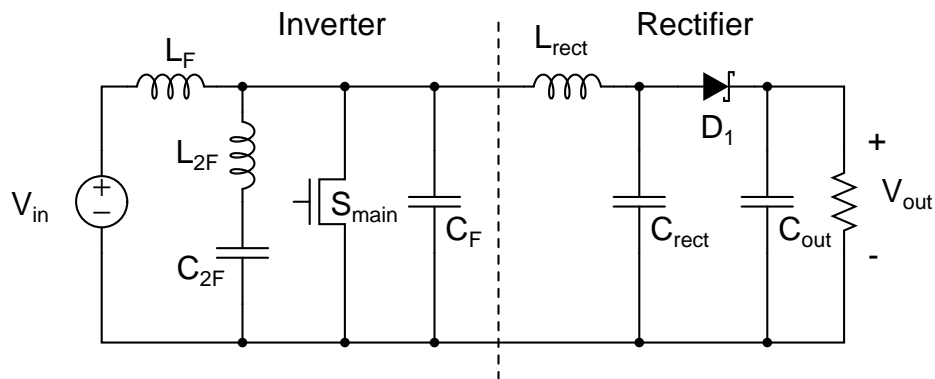


Figure 3.1: Schematic of resonant boost converter topology, consisting of a Φ_2 inverter coupled with a resonant rectifier.

3.1 Inverter Stage

3.1.1 Inverter Background

Wave-shaping Network Theory

For a transmission line of length l , characteristic impedance $Z_0 = \sqrt{\frac{L}{C}}$, where L and C are distributed inductance and capacitance (per unit length), the input impedance Z_{in} is given by [30]:

$$Z_{in} = Z_0 \frac{Z_L \cos kl + Z_0 j \sin kl}{Z_0 \cos kl + Z_L j \sin kl} \quad (3.1)$$

where $k = \frac{2\pi}{\lambda}$ is known as the wave number. For the case where the end of the transmission line is shorted (depicted in Figure 3.2), Equation 3.1 becomes:

$$Z_{in} = Z_0 j \tan kl \quad (3.2)$$

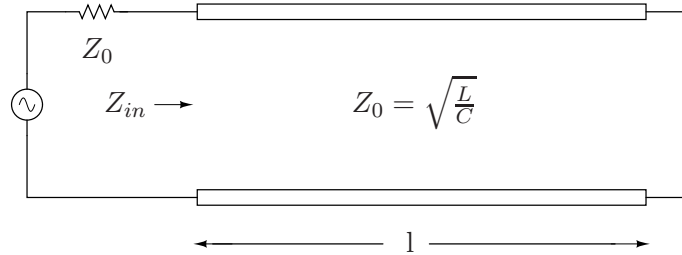


Figure 3.2: Shorted uniform, lossless transmission line of characteristic impedance Z_0 .

Figure 3.3(a) illustrates the reactance of a shorted 75Ω transmission line. For the case when the length l of the transmission line is equal to one quarter wavelength ($\lambda/4$), it can be seen that the input impedance Z_{in} has poles for frequencies:

$$f = \frac{n}{4l\sqrt{LC}} \quad \text{for } n = 1, 3, 5, \dots \quad (3.3)$$

Similarly, Z_{in} has zeros for even n (0, 2, 4...). Consequently, for an exciting waveform of frequency f_s , the shorted quarter-wave transmission line presents high impedance (peaks) at all odd harmonics, and low impedance (nulls) at all even harmonics. This is shown by the impedance magnitude plot of Figure 3.3(b). For this plot, the length l corresponds to

$\lambda/4$ for the frequency 110 MHz, and $Z_0 = 75 \Omega$. A similar analysis of a transmission line terminated by an open circuit gives the complementary result: impedance peaks at dc and even harmonics, and nulls at odd harmonics of the switching frequency.

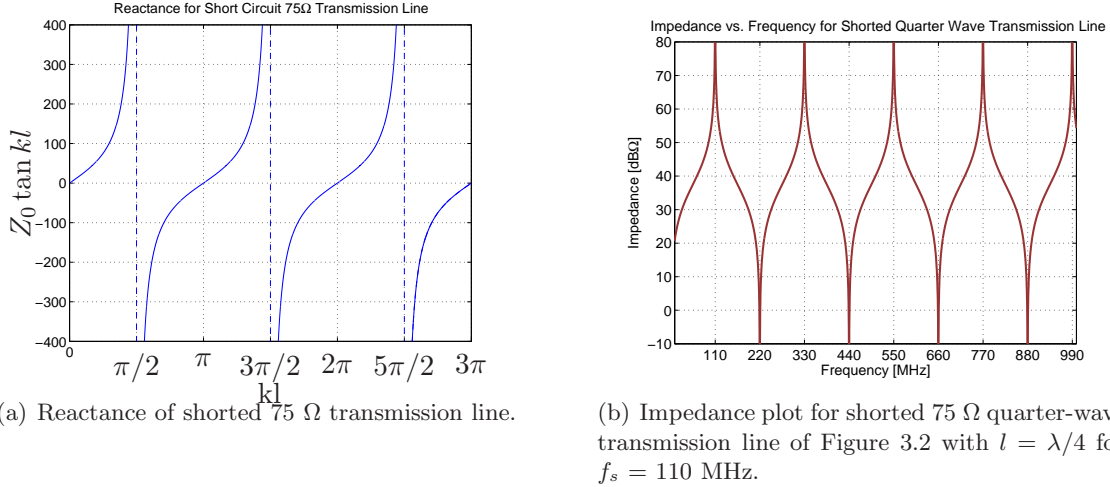


Figure 3.3: (a) Reactance of shorted transmission line. (b) Impedance for shorted quarter-wave transmission line.

These aligned peaks and nulls constrain the waveforms that can be supported by the transmission line. The impedance of the shorted quarter-wave transmission line is shown in Figure 3.3(b), and will not support voltages of even harmonics when driven by an excitation of frequency f_s . Consequently, the signal will only contain odd harmonics and will therefore be *half-wave symmetric* [31].

These characteristics of transmission lines - and their lumped element counterparts - have been used to reduce switch stress in rf power amplifiers by shaping the drain-to-source waveform [23–29, 32–36].

As is shown in [25–27], these symmetrizing properties of a quarter-wave transmission line can be used to shape the drain-to-source voltage in a resonant switching converter topology. In particular, [27] gives a detailed description of the operating principle of the Class Φ inverter, depicted in Figure 3.4. This inverter operates fully in “switched-mode”, at duty ratios somewhat less than 50%.

However, a transmission line presents practical difficulties for implementation in a VHF power converter. The added size and cost of a quarter-wave transmission line can negate

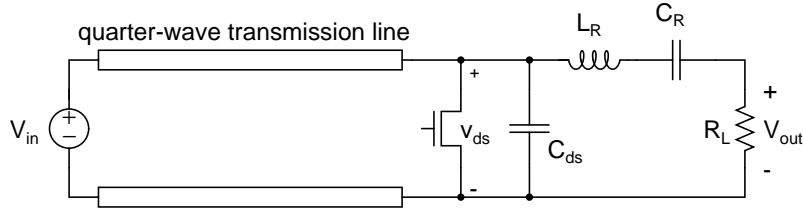


Figure 3.4: *Schematic drawing of Class Φ inverter.*

much of the benefits of switching at a high frequency, making it a less attractive solution. An alternative is the lumped transmission line analogs of [25–27], which use tapped inductors to create multi-resonant structures with symmetrizing properties similar to those of the quarter-wave transmission line. While their successful construction and implementation have been experimentally demonstrated, their fabrication requires substantial effort.

In an effort to utilize the waveshaping properties of the quarter-wave transmission line, the multi-resonant network of Figure 3.5(a) can be employed to provide a low-order approximation of the networks developed in [26]. As is seen in Figure 3.5(b), for a certain selection of components [28], the resulting input impedance mimics that of the shorted transmission line (Figure 3.3(b)) for the fundamental, second, and third harmonic of the switching frequency¹. The resonant elements C_F , C_{2F} , L_F , and L_{2F} can be made small, and as outlined in [27], can replace large bulk elements of similar topologies. Furthermore, the component C_F can comprise parasitic switch capacitance (and optional added discrete capacitance), providing parasitic absorption. Another benefit of the low-order multiresonant network is the low parts count that it offers, compared to a high-order network that attempts to more closely approximate the quarter-wave transmission line impedance at yet higher harmonics. Fewer components translates to reduced size, weight, and cost, which is always desirable. Because of these advantages, the multi-resonant network of Figure 3.5(a) is employed in the topology developed for this work.

¹Note that appropriate selections of passive component values for optimum converter operation do not typically load the network having the exact impedance peaks of a quarter-wave line, though the zero is typically selected close to the second harmonic. This will be treated subsequently.

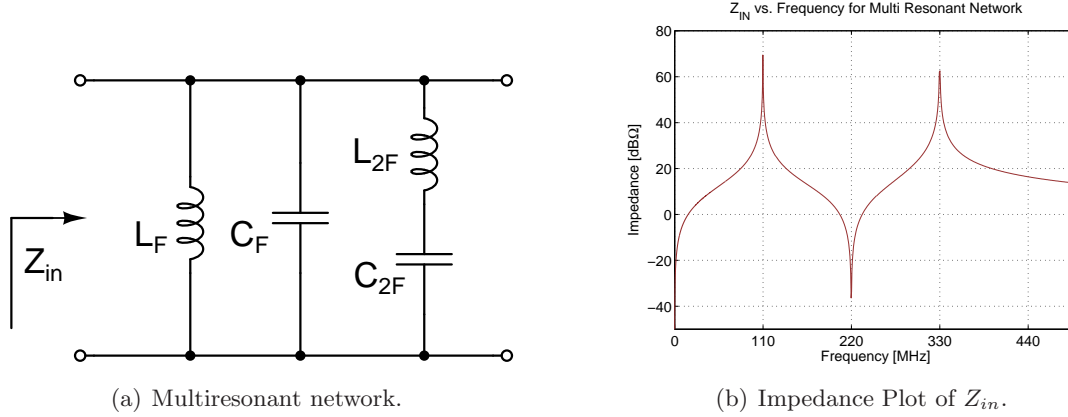


Figure 3.5: (a) Multiresonant network used to shape drain to source voltage. (b) Impedance magnitude vs. frequency for network tuned according to Equation 3.6 with $C_F = 100$ pF and $f_s = 110$ MHz.

Multi-resonant Network Implementation

By carefully controlling the impedances at a finite number of harmonics of the switching frequency, the drain-to-source voltage of a converter can be shaped to reduce overall switch voltage stress. Such a *flattening* of converter waveforms is widely used in Class F rf amplifiers [23, 24, 33–35]. Most practical Class F amplifiers, however, operate with significant voltage and current overlap (i.e., not fully “switched-mode”) which limits efficiency. Furthermore, as discussed in [24], these topologies typically use harmonic impedance control of the *load* network to shape the drain-to-source network, while still employing large bulk energy storage elements on the input.

As an example of how the drain-to-source voltage of an inverter can be controlled, consider a square wave of period T and amplitude 2. Its Fourier series is given by:

$$f(t) = 1 + \frac{4}{\pi} \sum_{n=1,3,5\dots}^N \frac{1}{n} \sin \frac{2n\pi t}{T} \tag{3.4}$$

and contains only odd harmonics. If the drain impedance can be controlled to only sustain voltage waveforms of these frequencies (with the correct amplitude), the drain voltage waveform will be that of a square wave. Often-times, however, an exact square-wave is not the objective, but instead a reduction in peak switch voltage stress. As is shown in [24], control-

ling the fundamental and third harmonic impedances is sufficient to drastically flatten the drain waveform. If the first three terms of the square-wave Fourier series of Equation 3.4 are used, the resulting equation becomes:

$$V(\theta) = 1 + V_f \sin \theta + V_{3f} \sin 3\theta \quad (3.5)$$

where $\theta = \frac{2\pi t}{T}$, $V_f = \frac{4}{\pi}$, and $V_{3f} = \frac{4}{3\pi}$. The relative weights of the first and third harmonic components of Equation 3.5 ($V_{3f} = \frac{1}{3}V_f$) produce a square wave when N of Equation 3.4 goes to infinity.² However, for a signal that only contains the first and third harmonic components of Equation 3.4, the relative weights that produce a maximally flat waveform are different, where instead $V_{3f} = \frac{1}{9}V_f$, as shown in [24]. Furthermore, this ratio is ideal if the objective is to achieve maximum waveform *flatness*. For a power converter topology - where minimum switch voltage stress is desired - the objective is to achieve minimum drain voltage, which does not correspond to maximum waveform flatness, as illustrated in Figure 3.6. For minimum drain voltage, the optimum ratio is $V_{3f} = \frac{1}{6}V_f$, as shown in Figure 3.6(b). Appendix D contains a detailed derivation of this relationship.

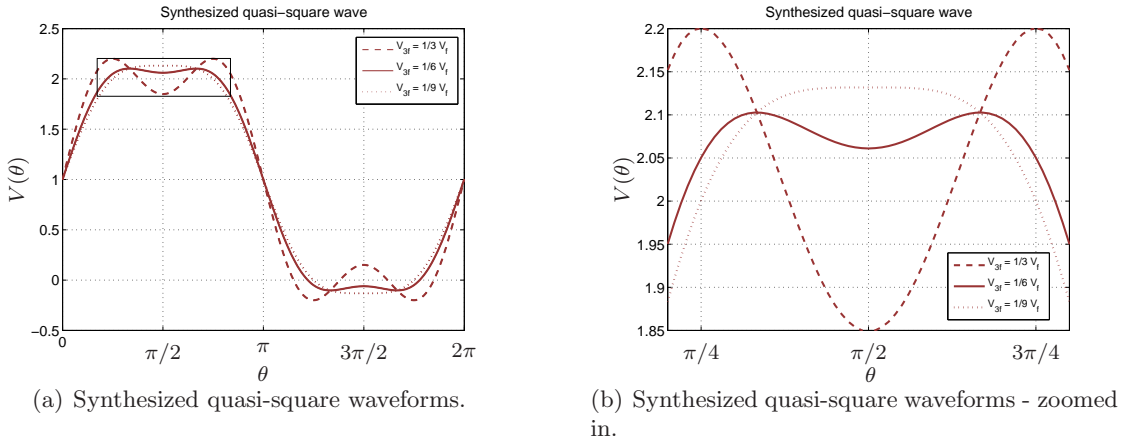


Figure 3.6: Illustration of synthesized waveforms for different ratios of V_{3f} and V_f .

The multi-resonant network of Figure 3.5(a) can then be used to significantly reduce the drain voltage as compared to other single-switch inverter structures (such as the Class

²From a strict mathematical viewpoint, the synthesized waveform for $N = \infty$ will not be an *exact* square wave. This is due to the well known Gibbs phenomenon, which describes the finite overshoot of the synthesized waveform at points of discontinuity.

E inverter). Furthermore, as shown in [28, 29], with proper tuning the network can be used to achieve zero voltage switching. The components L_F , L_{2F} , C_F and C_{2F} are tuned in the following manner: L_{2F} and C_{2F} are tuned to resonate near the second harmonic of the switching frequency, f_s , to present a low drain-to-source impedance at the second harmonic. In addition, the components L_F and C_F are tuned in conjunction with L_{2F} and C_{2F} to present a high drain-to-source impedance near the fundamental and third harmonic of f_s . The relative impedances between the fundamental and third harmonic can then be adjusted to shape the drain voltage to reduce switch voltage stress.

As a design starting point, the equation derived in [28] can be used to size L_F , L_{2F} , and C_{2F} in terms of C_F (which often comprises parasitic switch capacitance):

$$L_F = \frac{1}{9\pi^2 f_s^2 C_F}, \quad L_{2F} = \frac{1}{15\pi^2 f_s^2 C_F}, \quad C_{2F} = \frac{15}{16} C_F \quad (3.6)$$

Figure 3.5(b) illustrates the impedance of the multiresonant network when tuned according to Equation 3.6 with a C_F of 100 pF and a switching frequency of 110 MHz. The component values given by Equation 3.6 represents a good design starting point for tuning the inverter [28]. From this initial design starting point the adjustments listed below are made to achieve the desired waveforms.

In order to achieve near zero voltage switching it is desirable to tune the multiresonant network in a manner that presents an inductive impedance at the fundamental of the switching frequency. In terms of Figure 3.5(b), this corresponds to the first impedance peak (at $f_s = 110$ MHz) being moved slightly to the right. Furthermore, to reduce the peak drain voltage, the impedance at the third harmonic of the switching frequency is controlled to be lower than that of the fundamental to provide the correct ratio between first and third harmonic content of the drain voltage. To accomplish this, additional discrete capacitance can be added to C_F , and/or the relative values of L_{2F} , C_{2F} , and L_F can be adjusted.

In addition to the impedance of the multiresonant network, the impedance of the load network has an effect on the overall drain impedance, and must therefore be considered. Figure 3.7(b) shows a schematic drawing of the Φ_2 inverter coupled with a resonant load network. The resonant network is tuned as described in [28], and power is delivered to R_{load} . The impedance at the drain node is graphically split up in two components, Z_{MR}

and Z_L . Z_{MR} is the impedance looking into the inverter stage, while Z_L is the impedance looking into the resonant load network. The overall drain impedance Z_D (which is what shapes the drain voltage) is then given by the parallel combination $Z_{MR}||Z_L$.

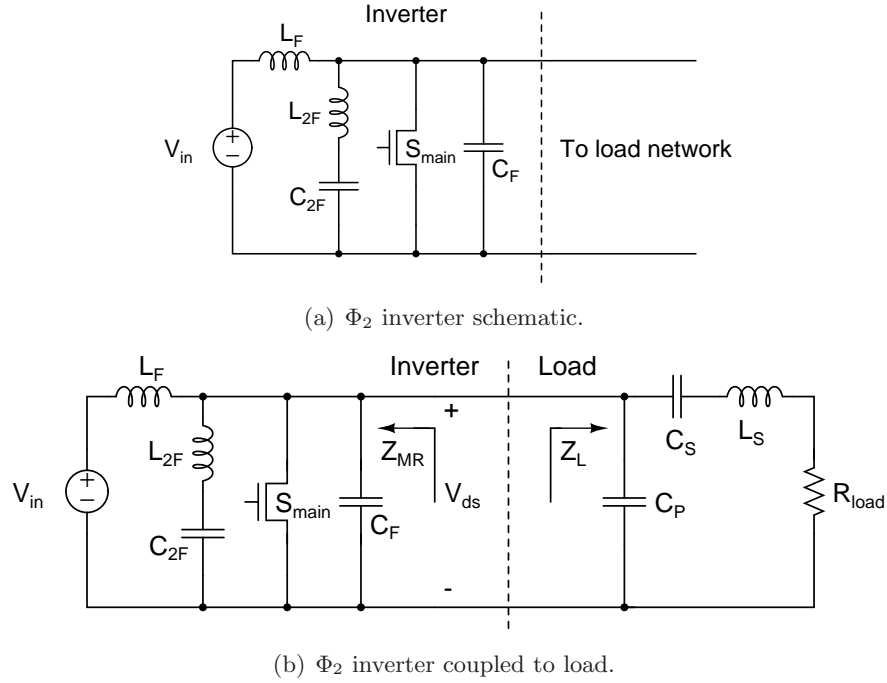


Figure 3.7: (a) Schematic of Φ_2 structure. (b) Φ_2 inverter with load network.

Plots of the impedance magnitudes of the circuit of Figure 3.7(b) are presented in Figure 3.8(a) with the corresponding time domain plot of Figure 3.8(b) showing the drain voltage for $V_{in} = 14.4$ V with S_{main} driven with a frequency $f_s = 110$ MHz. The multiresonant network component values used for the simulation are those given by Equation 3.6: $C_F = 100$ pF, $C_{2F} = 94$ pF, $L_F = 9.3$ nH, $L_{2F} = 5.6$ nH, which are the same values used to produce the impedance plot of Figure 3.5(b). The load network component values were: $C_P = 80$ pF, $C_S = 2$ nF, $L_S = 20$ nH, $R_{load} = 2.63$ Ω . Note that in this case the impedance of the output tank is selected to provide the desired drain impedance when connected together in parallel with the multiresonant network. The end result is the desired inductive impedance at the fundamental, and the proper ratio between first and third harmonic impedance.

The impedance magnitude plot of Figure 3.8(a) illustrates the 15.6 dB difference in

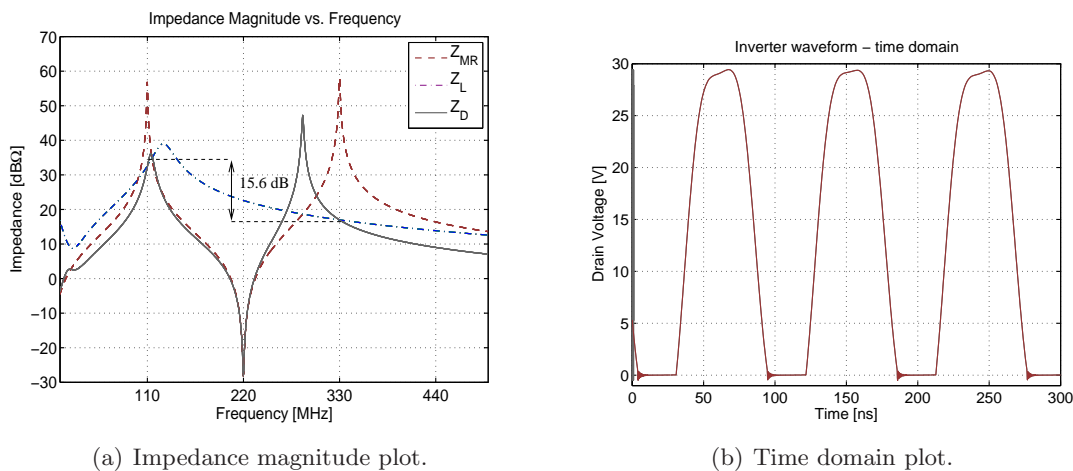


Figure 3.8: (a) Impedance magnitude plot for circuit of Figure 3.7(b). (b) Time domain simulation showing drain voltage plot for circuit of Figure 3.7(b) with $V_{in} = 14.4$ V and $f_s = 110$ MHz.

impedance at the frequencies 110 MHz and 330 MHz. Thus, the ratio of impedances is:

$$\frac{Z_D(110 \text{ MHz})}{Z_D(330 \text{ MHz})} = 10^{15.6/20} \approx 6$$

Correspondingly, if the “driving currents” at the fundamental and third harmonic were identical, the ratio of the fundamental (110 MHz) and third harmonic (330 MHz) component of the drain voltage would be:

$$\frac{V_{3f}}{V_f} \approx \frac{1}{6}$$

which is the ratio for minimum drain voltage derived in Appendix D. It should be appreciated that this is at best a qualitative relationship. There is not reason to expect the currents to be related in the stated fashion. Moreover, the waveforms under switched-mode operation are not exactly half-wave symmetric. Nevertheless, the resulting voltage does yield low device stress. As Figure 3.8(b) illustrates, the maximum drain voltage is slightly more than two times the input voltage. For comparison, the drain voltage of the Class E inverter (Figure 2.3) is - in the ideal case, and often higher in practice - 3.6 times the input voltage [37, 38].

As above analysis indicates, the Φ_2 inverter possesses many desirable properties that make it suitable for dc-dc power conversion with on-off control:

- No bulk storage elements. The multiresonant network contains small-valued resonant element (compared to the large choke inductor of the conventional Class E converter).
- Low device voltage stress.
- Output power not strongly tied to device capacitance (device capacitance is absorbed in the multiresonant network).

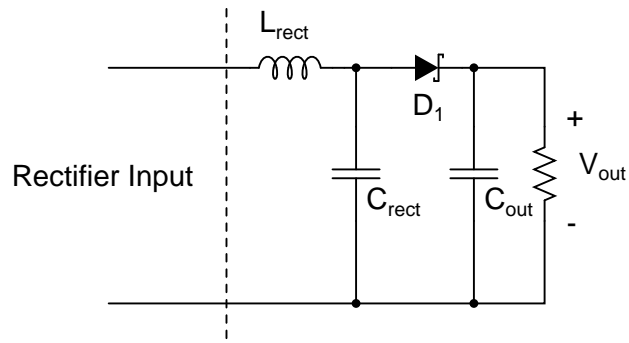
3.2 Rectifier Stage

To achieve dc-dc power transfer, the very high frequency quasi-square wave that the inverter produces needs to be rectified. At the high frequencies considered, hard-switched rectifiers exhibit substantial losses due to reverse recovery of the diode, as well as ringing due to the parasitic capacitance and package inductance associated with the discrete components. To maintain high rectifier efficiency at the frequencies of interest, a resonant rectifier topology can be coupled to the Φ_2 inverter. Many different resonant rectifier topologies have been developed [39, 40]. Two possible topologies suitable for coupling to the Φ_2 inverter are shown in Figure 3.9

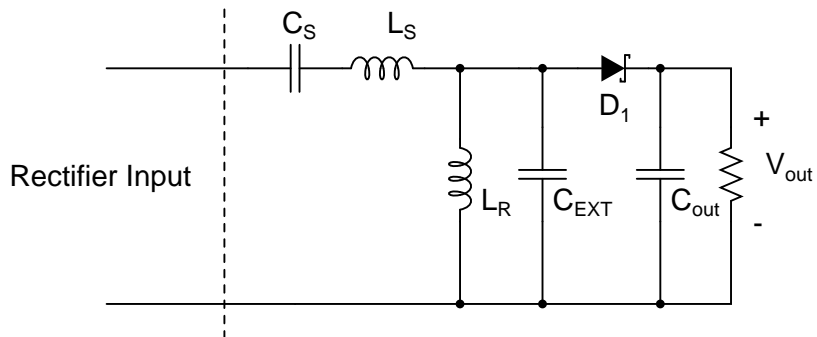
Figure 3.9(a) is a resonant rectifier topology for applications where the output voltage is higher than the input voltage (i.e. boosting). This rectifier was used in [41] where it was coupled to a Class E inverter. The dc path between input and output provides a means for a fraction of the energy to be transferred as dc power, without being subject to the resonant losses of the inverter. This topology cannot, however, be used in applications where the output voltage is lower than the input voltage (i.e. bucking) because of said dc path.

Figure 3.9(b) is another resonant rectifier topology which incorporates a resonant coupling network comprising C_S and L_S where the capacitor C_S serves as a dc block. This topology can be used in a buck or boost implementation, and provides more control over the load impedance than the topology of Figure 3.9(a). A detailed description of the design and implementation of this topology can be found in [28, 29], and is therefore not further elaborated on here.

For the target application of the converter of this work the output voltage is always above the input voltage, so the rectifier of Figure 3.9(a) can be used. The next section provides a



(a) Boost rectifier.



(b) Rectifier with dc block.

Figure 3.9: (a) Rectifier with dc path from input to output, suitable for boost applications. (b) Rectifier with blocking capacitor, suitable for buck or boost applications.

discussion of rectifier tuning and coupling to the Φ_2 inverter.

3.2.1 Rectifier Design

Figure 3.10 illustrates a method to tune the rectifier of Figure 3.9(a). In this method, the input voltage is represented as a trapezoidal waveform of amplitude $2.5 \times V_{in}$. Since the converter output voltage will be regulated to a fixed voltage, the output is modelled as a fixed voltage source. The components L_R and C_R are tuned to resonate the diode anode voltage to above the output voltage. When the diode anode voltage rises above the output voltage, the diode turns on and delivers charge to the load. The specific values of these components determine the diode current and conduction angle, which in turn determines the output power. The components L_R and C_R are thus chosen to provide a certain output power, while ensuring that the peak diode reverse voltage stays within allowed limits. Note that since the nonlinear diode parasitic capacitance C_D is - from an ac perspective - connected in parallel with C_R , the resonant behavior of the rectifier will be determined by $C_R || C_D$.

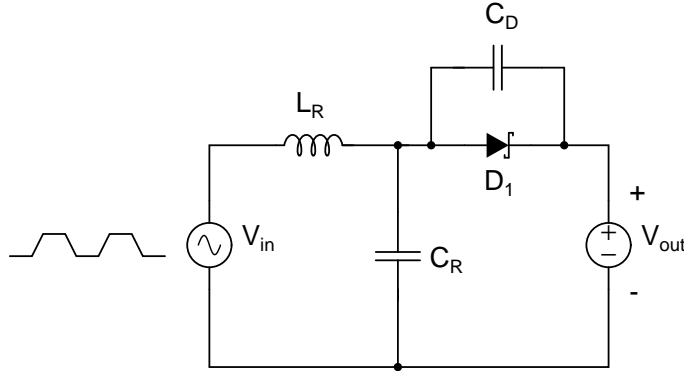


Figure 3.10: *Circuit illustrating one possible model for tuning of the resonant boost rectifier.*

The highly non-linear aspect of the rectifier circuit makes developing analytical expressions difficult. Computer simulations in SPICE was therefore heavily depended upon in the rectifier design. To achieve good performance over a wide input and output voltage range, several rectifier parameters were swept to find the best overall solution. Trade-offs included high nominal efficiency, ZVS conditions, and acceptable efficiencies across input voltage range. A more detailed discussion of these trade-offs is provided in [42], which contains,

among other things, an analysis of the effect of the diode non-linear capacitance and dc bias levels.

3.3 Simulated Converter Performance

Because of the tight dependence between converter performance and device parasitics, careful simulation was required before an experimental prototype was developed. Chapter 4 provides information regarding the semiconductor models used to accurately represent the device parasitics. In addition to semiconductor parasitics, non-idealities in inductors and capacitors must also be taken into account.

3.3.1 Converter Waveforms

Figure 3.12 illustrates converter and rectifier waveforms for a design with 14.4 V input voltage and 33 V output voltage. The switching frequency is 110 MHz. The full SPICE code for the simulation is given in Appendix A. Device parasitics are accounted for in the models as described in Chapter 4. Figure 3.11 shows the converter topology with current directions labelled. For this simulation, C_F consists entirely of the parasitic output capacitance of the MOSFET switch, as illustrated in the figure.

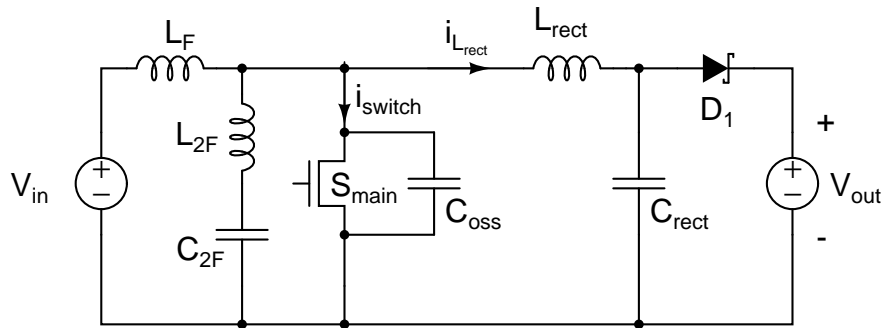


Figure 3.11: Schematic of resonant boost converter topology used for simulated waveforms of Figure 3.12.

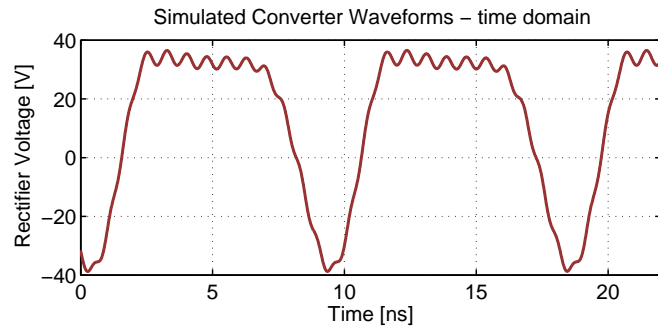
The voltage waveform of Figure 3.12(a) illustrates how the diode anode voltage is fixed at the output voltage (plus one diode drop) when the diode is turned on. When the main

switch turns on, the drain voltage is clamped at zero, forcing the current in the inductor L_{rect} to decrease, since it sees a negative voltage equal to the output voltage across its terminals. As this current further decreases, and eventually goes negative, the diode turns off, and the diode anode voltage is driven negative by the negative current in L_{rect} . When the switch is turned off, the drain voltage increases, and the positive voltage across the inductor L_{rect} causes the current through it to increase, ringing the diode anode voltage up to the output voltage, where it is clamped at that level. The cycle then repeats. The rectifier thus delivers charge to the load in each cycle through the resonant action of the inductor L_{rect} and capacitor C_{rect} .

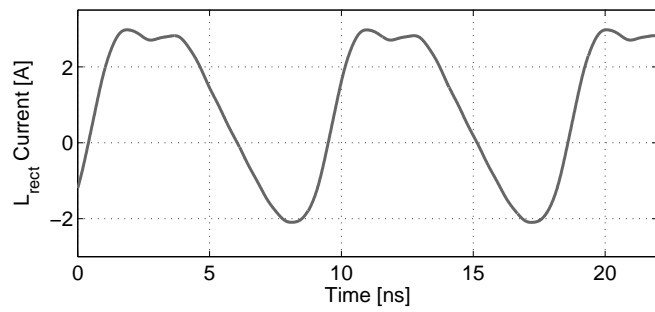
The drain voltage waveforms, shown in Figure 3.12(c) shows quite a bit of peakiness, and does not correspond to the desired smooth waveforms of the inverter simulation in Figure 3.8(b). The waveforms of Figure 3.12(c) contains too much third harmonic content, which increases the overall voltage stress. To maintain ZVS conditions for the inverter, the input impedance of the rectifier is tuned to look inductive at the fundamental. Unfortunately, this constrains the drain “impedance”, resulting in a voltage that is too high at the third harmonic of the switching frequency relative to the fundamental. (The notion of “impedances” for describing function approximations across frequency is clearly only of qualitative value.) This results in the peakiness of the drain voltage waveform of Figure 3.12(c). This highlights one limitation of the rectifier topology and values chosen. It should be noted that better waveform control has been achieved in the same basic topology in [42], albeit at much lower frequency, power, and efficiency.

3.3.2 Simulated Converter Loss Contributions by Components

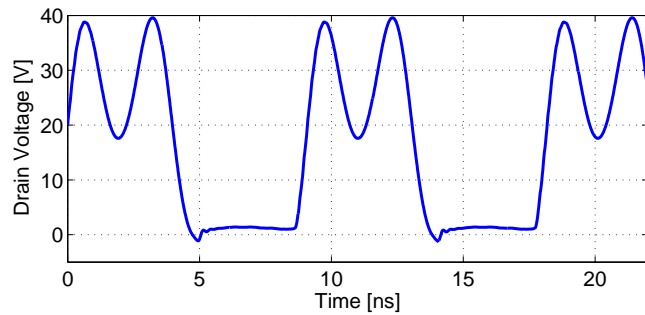
In order to improve the converter efficiency, it is important to understand what mechanisms contribute most strongly to converter power loss. With this information, component substitutions can be made to increase efficiency, and design changes can be made that reduce these losses. Figure 3.13 provides a graphical breakdown of simulated converter losses by component, and Table 3.1 provides absolute numbers. Losses in the capacitors were negligible, and as seen in the graph, the MOSFET loss dominated, contributing to more than 50% of the converter losses. The SPICE code for the simulation is provided in Appendix A. The input voltage is 14.4 V, the output voltage is 33 V, and the converter is switching at



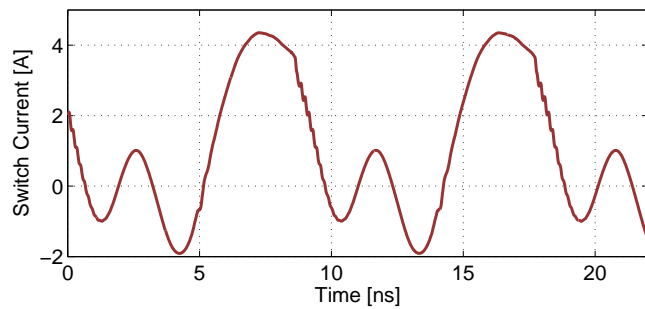
(a) Diode Anode Voltage.



(b) L_{rect} Current.



(c) Drain Voltage.



(d) Switch Current.

Figure 3.12: Simulated Converter Waveforms.

110 MHz. The simulated efficiency is 89% and the nominal output power is 25.6 W.

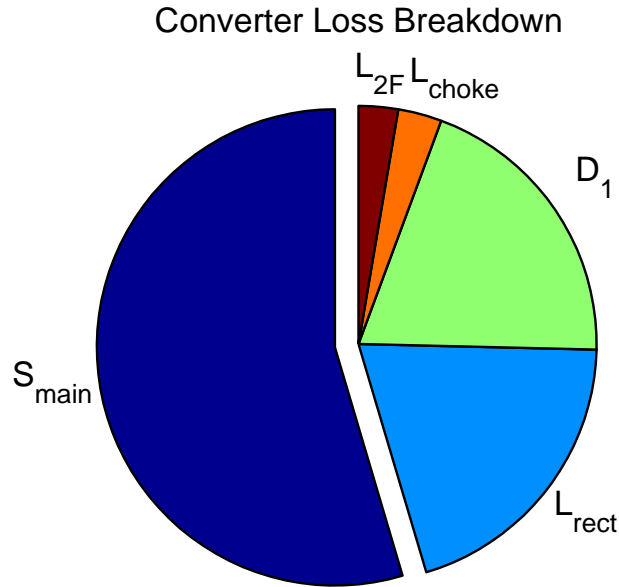


Figure 3.13: *Simulated converter loss breakdown by component.*

Component	Power Loss [W]	Percent
S_{main}	1.730	54.59
L_{rect}	0.635	20.04
D_1	0.625	19.72
L_{choke}	0.094	2.97
L_{2F}	0.085	2.68

Table 3.1: *Component loss contributions.*

Semiconductor Selection and Modeling

TO meet the goals of high efficiency dc-dc conversion at VHF, much care must be taken in the selection and modeling of the semiconductor devices. Parameters such as transistor gate capacitance and package inductance, which are of secondary importance in conventional designs operating in the hundreds of kHz, become crucial as the frequency approaches the VHF range. This chapter presents a comparison of transistors suitable for VHF operation (Section 4.1), detailed characterization of the most suitable transistor for the design considered here (Section 4.2), and presents two semiconductor models (Section 4.3) for use in computer simulation software such as SPICE.

4.1 Device Selection

For conventional dc-dc power converters, efficiency is strongly determined by the on-state resistance, $R_{ds,on}$, of the switching devices. Modern power MOSFETs can achieve values of $R_{ds,on}$ down to a few milli-Ohms, but at the expense of increased parasitic capacitance. Whereas this is an acceptable trade-off at lower frequencies, large parasitic capacitances become the limiting factor of performance when the operating frequency approaches the VHF range. Figure 4.1 shows a schematic drawing of a MOSFET with the most important parasitic elements shown as discrete components. The inductors L_d , L_s , and L_g represent the inductance of the bond-wires, packaging, and on-chip metallization. R_g represents the parasitic gate resistance, which can be several Ohms in some cases. R_{oss} is the equivalent series resistance of the parasitic capacitance between the drain and source terminals. The model of Figure 4.1 does not include the parasitic output resistance of the gate-to-drain capacitance. For the transistors covered here, C_{gd} is substantially smaller than C_{ds} , such that the effect of this resistance can be ignored for simplicity. The parasitic capacitances C_{gd} , C_{gs} and C_{ds} are often listed in device datasheets in terms of C_{iss} , C_{oss} and C_{rss} . The

relationships between the parameters are:

$$C_{iss} = C_{gs} + C_{gd} \quad C_{oss} = C_{ds} + C_{gd} \quad C_{rss} = C_{gd} \quad (4.1)$$

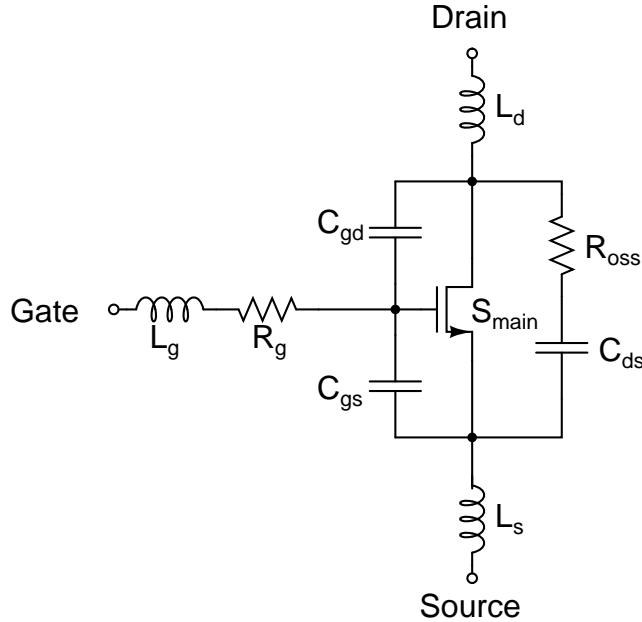


Figure 4.1: Schematic drawing of power MOSFET with key parasitic element shown as discrete components.

4.1.1 Vertical Power MOSFETs

Most traditional power converters employ vertical power MOSFETs, which can provide exceptionally low on-state resistance. To investigate the feasibility of using a vertical power MOSFET in a VHF converter, an extensive search for suitable devices was performed. Although eventually the decision was made to employ a lateral device (covered in Section 4.1.2) for the converter of this thesis, the device comparison and evaluation of vertical devices are presented here for completeness. Additionally, it is the hope of the author that the data presented in this section may be of use for future converters where different design specifications can tip the scale in favor of vertical MOSFETs. In particular, the measured device parameters that are not listed on datasheets represent a considerable amount of work. It is anticipated that their listing here will reduce the design time of future converters utilizing

similar devices.

As is shown in Chapter 5, a resonant gate drive circuit is beneficial for VHF operation. It can be shown [16,41] that the loss associated with a sinusoidal resonant gate drive is given by:

$$P_{gate} = 2R_g\pi^2 f^2 C_{iss}^2 V_{g,ac}^2 \quad (4.2)$$

Here $V_{g,ac}$ is the amplitude of the sinusoidal ac voltage, R_g is gate resistance, C_{iss} is device input capacitance, and f is switching frequency. R_g , the gate resistance, constitutes the equivalent series resistance (ESR) of the input capacitance together with any additional series resistance of the drive circuit. This is a parasitic that does not affect gating loss in hard gating, but it is an important parameter when selecting transistors used for resonant gating. Unfortunately, R_g is rarely listed on device datasheets, so this value has to be measured for each of the device candidates.

One other major device-loss of soft-switching converters is conduction loss. This is the ohmic loss due to the non-zero resistance of the transistor during its on-state, and is given by:

$$P_{conduction} = I_{RMS}^2 R_{ds,on} \quad (4.3)$$

As Equations 4.2 and 4.3 show, three important device parameters that govern power loss of VHF resonant converters using vertical MOSFETs are R_g , C_{iss} , and $R_{ds,on}$. A useful metric for evaluating vertical devices is therefore to minimize $R_g C_{iss}^2$ and $R_{ds,on}$.

Table 4.1 provides measured data for a number of 60 V vertical power MOSFETs from various manufacturers. The measurements were done in the following manner: the input capacitance C_{iss} was measured using an Agilent 16092A spring clip fixture attached to an Agilent 43961A RF impedance adapter on an Agilent 4395A impedance analyzer. For this measurement, the drain and source of the device were shorted together, and the gate and source terminals were connected to the spring clip fixture. By measuring the magnitude and phase of the DUT's response to an applied test signal, the impedance analyzer calculates the capacitance and resistance of the connection (C_{iss} and R_g for this measurement setup). This is done over a sweep of frequencies. Table 4.1 lists the values of C_{iss} and R_g measured for a frequency of 30 MHz. The on-state resistance, $R_{ds,on}$ is the temperature-adjusted resistance listed on the device datasheet for a gate-to-source voltage of 6 V. The room

temperature (25°C) value of resistance has been adjusted for an operating temperature of 135°C according to the temperature dependence from each device’s datasheet (typically an increase in $R_{ds,on}$ of 60-100%).

Device:	C_{iss} [pF]	R_g [Ω]	$R_{ds,on}^a$ [Ω]	$R_g * C_{iss}$ [Ω nF ²]
FDZ209	850	1.5	0.136	1.08
FDD5612	830	1.57	0.128	1.08
SUD23N06-31L	950	1.47	0.081	1.32
Si7850DP	1265	1.32	0.056	2.23
HUFA764	1000	2.3	0.101	2.30
FDS5690	1645	1.18	0.059	3.20
IRCZ34	2340	1.1	0.09	6.02
FDS5680	2311	1.19	0.038	6.36
FDS5672	2511	1.43	0.023	8.99
IRF7478	2635	1.51	0.053	10.5
FDS5170N7	3432	1.1	0.027	13.0
FDS5670	3572	1.26	0.031	16.1
IRF1010ES	5160	0.7	0.02	18.6

^a $R_{ds,on}$ obtained from device datasheets for $V_{gs} = 6$ V, temperature adjusted for a temperature of 135 °C

Table 4.1: *Measured device parameters for 60 V vertical MOSFETs*

Figure 4.2, a visual representation of the data of Table 4.1, shows a scatter plot of all the devices in terms of the parameters $R_g * C_{iss}^2$ and $R_{ds,on}$. The scatter plot provides a visual means of estimating the relative “goodness” of devices. Using above loss metric, one would not, for instance, choose a device whose values of R_g and $R_g C_{iss}^2$ are both larger than those of another device. This can be easily seen by the distance from the origin in the x and y direction. One cannot, however, simply use the distance from the origin as a parameter to find the best device without knowing the relative contributions of gating loss and conduction loss to converter efficiency.

In order to identify the transistor most suitable for use in the converter presented in Chapter 3, an analytic expression for converter losses is useful¹. Unfortunately, at this

¹It is possible to measure and completely characterize the parameters of *each* of the potential devices of Table 4.1. Subsequent converter design (according to the methodology outlined in Chapter 3) and computer simulation for each device would shed some light on the relative merits of the different transistors. However, this brute force approach, in addition to being hohorrendouslyime consuming, provides no design insights into the relative importance of the device parameters.

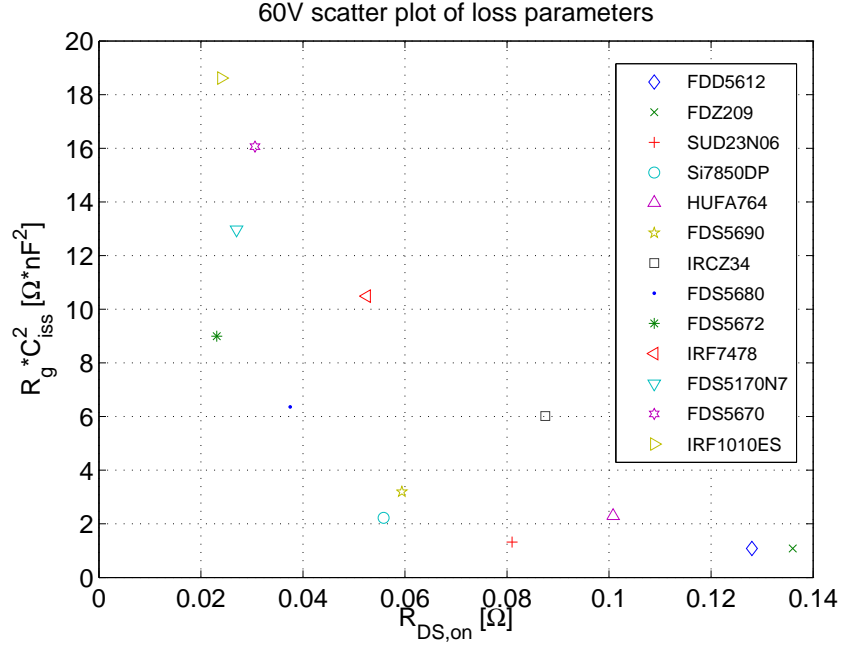


Figure 4.2: Scatter plot of potential 60 V vertical MOSFETs.

time no such expression exists for the topology presented in Chapter 3. Therefore the exact relative contribution of the parasitic parameters R_g , C_{iss} , and $R_{ds,on}$ to converter loss cannot be found. However, the inverter of Chapter 3 shares many characteristics with the well-studied Class E inverter [20]. Therefore, the analytic expressions [20, 38, 43, 44] for the Class E inverter can be used to evaluate the relative merits of the devices listed in Table 4.1 when used in a VHF resonant inverter topology similar to the Class E inverter. It has been found [38, 41] that the normalized conduction loss for the Class E converter is given by:

$$\frac{2.363R_{ds,on}}{V_{cc}^2} P \quad (4.4)$$

where V_{cc} represents the dc input voltage.

Normalizing Equation 4.2 for output power, and adding it to Equation 4.4, results in the the following expression for normalized power loss : [41]

$$P_{norm} = \frac{2.363R_{ds,on}}{V_{cc}^2} P + \frac{2R_g \pi^2 f^2 C_{iss}^2 V_{g,ac}^2}{P} \quad (4.5)$$

Taking the derivative with respect to P of above function, one finds that the minimum normalized power loss occurs when the gating loss and conduction loss are equal.

The analysis above identifies the optimum operating power level to maximize efficiency of a Class E based converter with a certain device at a *given* frequency. Since it is desirable to operate at the highest achievable frequency, a metric to compare device performance for *different* frequencies is needed. A useful comparison is to operate each device at the optimal power level as given by Equation 4.5, and calculate normalized power loss for varying frequencies. It is expected that devices with lower R_g and C_{iss} will perform better at higher frequencies, since the frequency-dependent gating loss should increase less rapidly. Figure 4.3 shows a normalized loss vs. frequency plot for selected 60V MOSFETs.

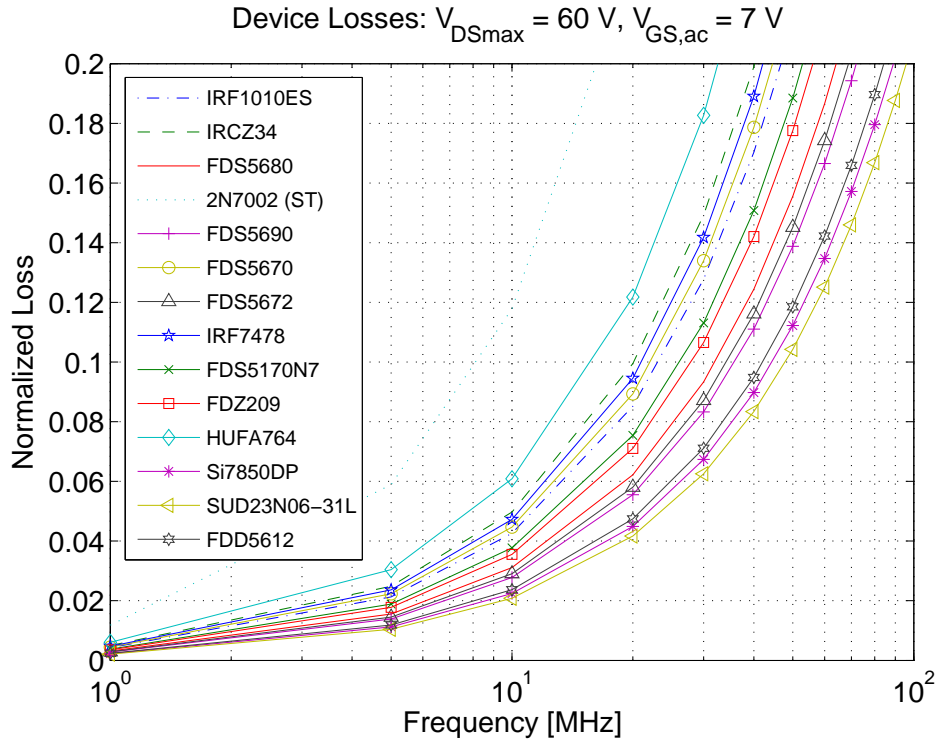


Figure 4.3: Plot of normalized power loss vs. frequency for 60 V vertical MOSFETs.

From Figure 4.3 it is evident that many devices are ill-suited for operation at VHF frequencies (30-300 MHz) due to the rapidly increasing gating loss. Considering a desired operating frequency of above 25 MHz (to achieve component miniaturization) and a desired device loss below 10% (to achieve high efficiency) it can be observed that there are a handful

of devices that meet these performance requirements. The top three (Si7850, FDD5612, SUD23N06) are selected for further consideration.

The analysis of Figure 4.3 compares each device when operating at its unique optimum power level. If this device-specific optimum power level is too low for practical use, the device might not be the best choice for use in a power converter, since, in addition to high efficiency, one typically strives to achieve the highest possible output power for a given converter area. Likewise, if the optimum power level is too high one might not be able to use the device because of heat management limitations that makes the power level impossible to realize in a practical implementation. To investigate the achievable power levels of the selected transistors, Figure 4.4 shows the normalized device loss vs. output power for the three top devices, all operating at 30 MHz.

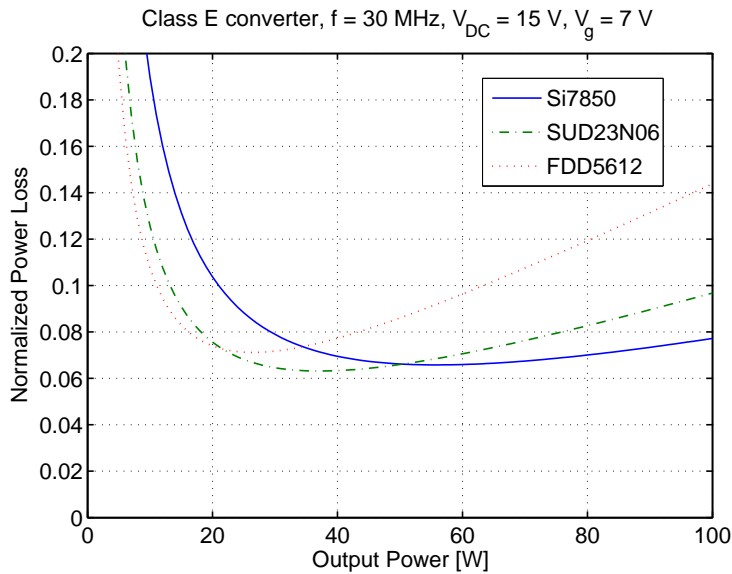


Figure 4.4: Plot of normalized power loss versus output power for the top three vertical MOSFETs.

As Figure 4.4 illustrates, all three devices have optimum power levels above 20 W. The two Siliconix devices (SUD23N06 and Si7850) are also relatively 'flat' around the optimum power level, which enables converter operation slightly above or below the optimum power level without substantially decreasing efficiency. This would be done to increase power density, or to decrease absolute power loss, if heat transfer limits are a concern. Figure 4.4 also shows that the SUD23N06 performs the best in terms of efficiency, and is therefore the

most suitable device for VHF operation according to this analysis.

It is important to note that the analysis performed above only gives an indication of the *relative* merits of each device, and that the absolute efficiency and power levels are estimates based on Class E operation with simplifying assumptions with regards to many losses. The results should therefore not be interpreted as a measurement of absolute achievable efficiency of a converter. Rather, they provide an indication of which semiconductor switches are more suitable for VHF operation than others.

Although the above analysis of vertical MOSFETs for use in VHF converters gives promising results with respect to achievable efficiency and power density, what ultimately prevents their successful implementation in a VHF converter is the limits observed in turning the devices on and off quickly. To operate efficiently in a switched-mode topology, the turn-on and turn-off transition time of the transistor must be fractions of a switching cycle. For a frequency of 30 MHz, one switching cycle is 33 ns. However, as can be seen in Table 4.1, the gate parasitic RC time constant ($C_{iss}R_g$) associated with the transistor SUD23N06 is 1.4 ns. This time constant, which does not take into account any additional resistance of the gate drive circuit (which can be substantial), is almost 5% of one switching cycle. The other vertical MOSFETs exhibit gate time constants of similar magnitudes, making their implementation in VHF converters difficult. One obvious solution to this problem is to operate the converter at a somewhat lower frequency. This will allow the designer to take advantage of the low on-state resistance of the vertical MOSFETs while keeping energy storage elements small. That approach is not taken in this work, since the main focus here is to obtain miniaturization and performance improvements of dc-dc power converters through operation at VHF (30-300 MHz). The next section treats an attractive alternative to vertical power transistors which are more suitable for VHF operation.

4.1.2 Lateral Devices

In large due to the increasing demands of the communications industry, the development of radio-frequency (rf) power semiconductor devices have progressed at a rapid pace. To reduce operating cost and heat dissipation of TV, cellular-phone, and radio broadcast systems, much work has been aimed at improving the efficiency and performance of the incorporated semiconductor devices. One area in particular - cell-phone communication, has largely

driven this development which has resulted in a tremendous improvement in performance and efficiency of semiconductor devices designed for operation at hundreds of MHz and above.

Transistors suitable for rf communication are predominantly of the LDMOS (Laterally doubly Diffused Metal Oxide Semiconductor) type, which provides inherently smaller parasitic capacitance compared to the conventional vertical power MOSFET. On-state resistance of LDMOS transistors, while typically still higher than that of vertical MOSFETs, has been continuously reduced to meet the high demands of the communications industry. The state of the art LDMOS transistors used to drive rf amplifiers in cell-phone base stations offer high efficiency and small size, parameters that are equally important for dc-dc power conversion. As [12, 16] has demonstrated, dc-dc converters utilizing LDMOS devices as their main switching elements are not only realizable, but have the potential of reducing converter size and cost while providing the desirable performance benefits associated with operation at VHF.

Since converter performance is highly dependent on the characteristics of the selected semiconductor switch, an extensive search for suitable candidates was performed. Top candidates from three semiconductor manufacturers were selected, based on the following criteria: small package size, low $R_{ds,on}$, and small C_{gs} and C_{gd} . Some high-power rf devices provide matching circuitry at the gate terminal which greatly complicates the gate drive design. For this reason only devices with unmatched gates were selected. Table 4.2 lists the top five rf devices identified as suitable for use in an experimental prototype, and therefore selected for further evaluation.

Manufacturer	Device	$V_{ds,max}$	$R_{ds,on}$ ($V_{gs} = 8$ V)	R_{oss}
Freescale	MRF6S9060	68 V	0.175	0.172
Freescale	MRF5S9070	68 V	0.193	0.191
Freescale	MRF6S9045	68 V	0.245	0.296
ST Microelectronics	SD57045	65 V	0.260	1.260
Agere	AGR09030GUM	65 V	0.375	0.486

Table 4.2: Measured data for top five LDMOS candidates selected for use in prototype resonant boost converter.

LDMOS Loss Mechanisms

As with all dc-dc power converters, $R_{ds,on}$ is an important parameter of the main switch, since it directly determines the conduction loss ($P_{conduction} = I_{RMS}^2 R_{ds,on}$). Although this parameter is listed on most manufacturers' datasheets, it was measured in the laboratory to provide a direct comparison between devices under identical conditions. $R_{ds,on}$ was measured in the following manner: a power supply, current-limited to 1 A, was connected between the drain and source terminals of the device under test (DUT). Another variable voltage source was connected between the gate and source terminals. As this voltage was swept between 0 and 10 V, a volt-meter was used to measure the voltage across the drain and source terminals. When the current delivered by the drain-connected power supply is 1 A, the voltage measured across the drain-source terminals corresponds to the on-state resistance in Ohms. This value is presented for each device in Table 4.2, column 3, for a gate voltage of 8 V.

Although still a loss mechanism, the gating loss for lateral MOSFETs is significantly smaller than that of vertical ones. This is attributed to the much smaller input capacitance C_{iss} and parasitic gate resistance R_g . As is shown in Section 4.2, C_{iss} and R_g can each be close to an order of magnitude smaller in lateral devices compared to vertical devices with similar breakdown voltages, resulting in substantially reduced gating loss.

Another loss mechanism that becomes important in lateral MOSFETs is the power dissipated each cycle in R_{oss} , the parasitic resistance of the drain-to-source junction capacitance. Each time the capacitance C_{ds} is charged and discharged (every switching cycle), some energy is lost in this parasitic resistance. Although this amount of energy is small, at sufficiently high frequencies the ensuing power loss can limit converter efficiency. For this reason R_{oss} of the five devices was measured and is listed in Table 4.2. An Agilent 4395A impedance analyzer was used to measure the output capacitance and parasitic resistance of each device. Each device had its gate and source terminals shorted together, and the drain and source terminals connected to the impedance analyzer. Table 4.2 lists the values of parasitic resistance measured at the switching frequency (110 MHz) for the selected devices. We note that this measurement actually captures loss associated with C_{gd} and C_{ds} . However, for simplicity we make the reasonable approximation that this resistance is entirely due to the drain-to-source capacitance path (i.e. through C_{ds}).

As is seen in Table 4.2, the MRF6S9060 from Freescale Semiconductors is the best device both in terms of $R_{ds,on}$ and R_{oss} , and was thus selected as the main switch for the converter.

4.2 Device Characterization

To successfully build a converter prototype, semiconductor parasitics must be carefully measured and accounted for. In this section important parasitic parameters are explained, and measured values from the MRF6S9060 are presented.

4.2.1 Non-linear Output Capacitance

One device parameter that is particularly critical to model correctly is the output capacitance of the main switch, C_{ds} (C_{gd} is sufficiently small for the selected device that C_{ds} and C_{oss} are used interchangeably for this analysis). This capacitance is highly non-linear, with the capacitance varying with drain-to-source voltage according to:

$$C_{ds} = \frac{C_{jo}}{\left[1 + \frac{V_{ds}}{V_j}\right]^M} \quad (4.6)$$

where C_{jo} , V_j , and M are device-specific parameters that are sometimes provided by the manufacturer, but more often must be found from physical measurements of the device. As indicated in Chapter 3, the resonant capacitor C_F can often be provided by C_{ds} alone. Its non-linearity must therefore carefully be modelled and accounted for in simulation to maintain ZVS waveforms. To characterize C_{ds} , the gate and source terminals of the MRF6S9060 were shorted together, and the drain and source terminals were connected to an Agilent 4395A impedance analyzer. The capacitance was measured for different drain-to-source voltages (applied by an external voltage source), and is shown in Figure 4.5. Also shown in the figure is a plot of the modelled capacitance where the parameters of Equation 4.6 have been fitted to the measured data. The plot corresponds to the parameters $C_{jo} = 157.5$ pF, $V_j = 1.163$ V, and $M = 0.446$.

For the design of the resonant gate driver (documented in Chapter 5), the gate input impedance of the MRF6S9060 must be carefully measured and modelled. To this end,

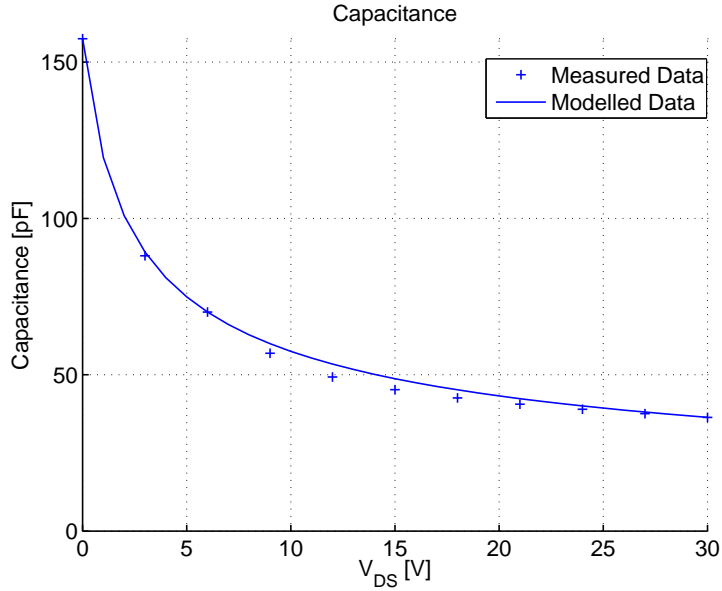


Figure 4.5: Plot of measured non-linear output capacitance of MRF6S9060.

the parameters C_{gs} and R_g were measured using an Agilent 4395A impedance analyzer. For this measurement the drain and source terminals were shorted together and the gate and source were connected to the spring clip fixture attached to the impedance analyzer. The measured values were $C_{gs} = 110$ pF and $R_g = 135$ m Ω (note that for simplicity, the variations in input capacitance with bias are ignored in this analysis, with measurements made at zero dc bias).

4.3 SPICE Modeling

In many cases, rf semiconductor manufacturers do not provide models for computer simulation software such as SPICE. In the cases where models are provided, they are often-time useful to model a small subset of the characteristics of importance, but tend to not capture all relevant information. For these reasons, the development of a SPICE model that captures the device characteristics relevant for VHF dc-dc converter operation is an important task, and it is presented in this section.² The development of the models is presented

²The development of these SPICE models build on a substantial amount of previous work done by Dr. Juan Rivas [28], which is gratefully acknowledged.

here with parameters from the devices used for the experimental prototype, but they can be easily adjusted to other devices. It is indeed the hope of the author that the general models presented here can be useful for future work using different semiconductor devices. Section 4.3.1 presents a model of a transistor that characterizes the important parameters for use in a resonant topology. Section 4.3.2 presents a model of a diode that accurately characterizes the non-linear diode capacitance, an important parameter when used in a resonant rectifier topology.

4.3.1 Transistor Model

A schematic of a transistor SPICE model is shown in Figure 4.6. It features a voltage-dependent current source used to model the non-linear drain-source capacitance according to the following rule (adapted from [45]):

$$\begin{aligned} \text{if } V_{ds} < 0 \quad \text{then} \quad & I_{ds} = C_{jo} \frac{dV_{ds}}{dt} \\ \quad \quad \quad \text{else} \quad & I_{ds} = \frac{C_{jo}}{\left[1 + \frac{V_{ds}}{V_j}\right]^M} \frac{dV_{ds}}{dt} \end{aligned}$$

The switch S_{main} and piecewise linear resistance $R_{ds,on}$ are modelled to capture how the on-state resistance varies with gate-to-source voltage. Figure 4.7 illustrates how the resistance is modelled in SPICE using a number of paralleled switches and resistors, each with different value of resistance and switch threshold. As the gate-source voltage rises, switches S_1 through S_{10} turn on and subsequently lowers the effective on-state resistance. With appropriately chosen resistance values R_1 through R_{10} , the modelled resistance can be made to match the measured resistance of the device exactly at the measured datapoints. $R_{ds,on}$ of the selected device (MRF6S9060) was measured for gate-to-source voltages between 3 and 10 V at 1 V intervals, and the resistors R_1 through R_{10} were chosen such that the modelled resistance exactly corresponds to the measured values at those points.³ To improve the accuracy of the model, on-state resistance can be measured at closer intervals, and more

³This measurement was done with the device near room temperature, $T \approx 25^\circ C$. The increase of $R_{ds,on}$ with temperature must be taken into account to properly model the device at the operating temperature (which is typically much higher than $25^\circ C$). This can be done by performing the resistance measurements at a higher device temperature, or by increasing the room temperature resistance measurement by a temperature scaling factor.

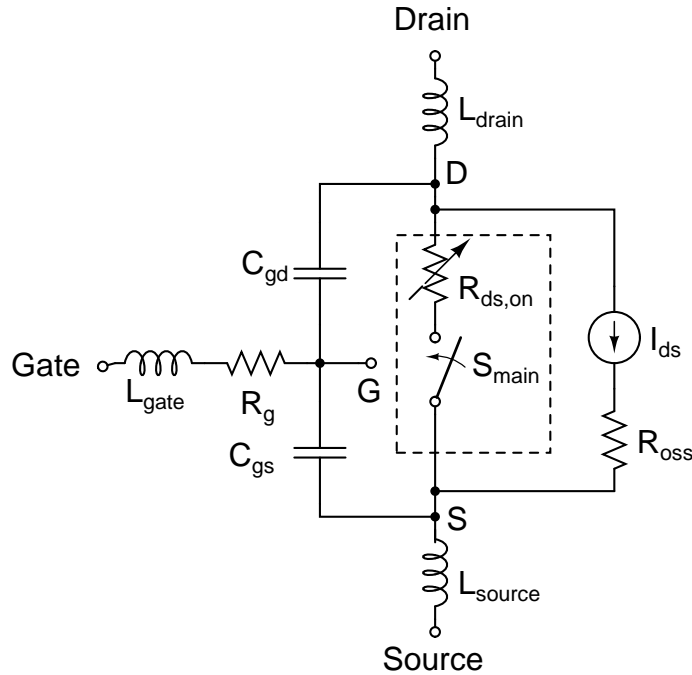


Figure 4.6: Schematic drawing of SPICE model which captures the relevant characteristic of transistors suitable for resonant dc-dc power converters.

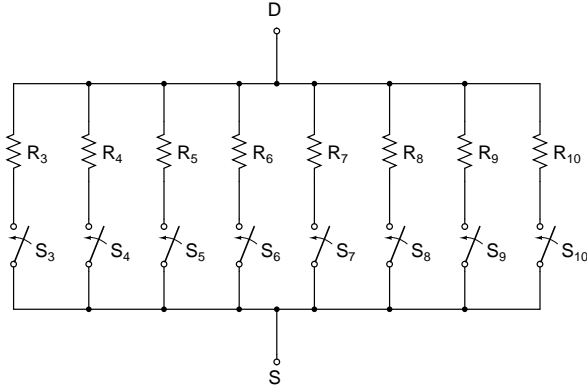
switch-resistor pairs can be incorporated in the model. This precision, however, comes at the expense of increased computation complexity.

The package and bond-wire inductances, represented by L_{drain} , L_{source} , and L_{gate} in Figure 4.6 are typically small (< 1 nH), but can nevertheless cause significant ringing at high frequencies. Because of their small size, however, they are often difficult to measure accurately. In reality it is hard to measure an exact value; an upper bound of their values is often the best one can find.

The complete SPICE code of the transistor model is provided in Appendix B.1.

4.3.2 Diode Model

The diode selected for the prototype resonant rectifier is the S310 from Fairchild Semiconductor, a 3 A Schottky diode with 100 V maximum reverse voltage. Figure 4.8 shows a schematic of the model used for simulation.



Switch	R Value	$V_{threshold}$	Total $R_{ds,on}$
S_3	1 Ω	3 V	1.000 Ω
S_4	0.31 Ω	4 V	0.238 Ω
S_5	1.34 Ω	5 V	0.202 Ω
S_6	2.71 Ω	6 V	0.188 Ω
S_7	4.23 Ω	7 V	0.180 Ω
S_8	6.3 Ω	8 V	0.175 Ω
S_9	5.95 Ω	9 V	0.170 Ω
S_{10}	9.46 Ω	10 V	0.167 Ω

Figure 4.7: Implementation of variable resistance of voltage controlled switch between nodes D and S of Figure 4.6.

Table 4.3: Resistor values and switch thresholds that provide a piecewise linear resistance model to characterize $R_{ds,on}$ of MRF6S9060.

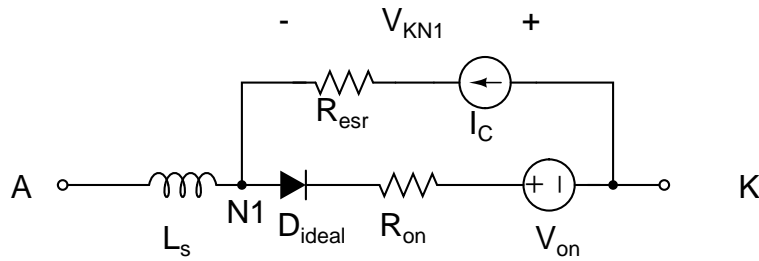


Figure 4.8: Schematic drawing of diode SPICE circuit which properly models the non-linear diode capacitance, as well as the forward voltage drop and package inductance.

The model of Figure 4.8 uses a voltage-dependent current source similar to that of the transistor model to accurately capture the non-linear behavior of the diode capacitance. The voltage-dependent current source acts like a non-linear capacitor according to the following rule:

$$\begin{aligned}
 \text{if } V_{KN1} < 0 \quad \text{then} \quad & I_C = C_{jo} \frac{dV_{KN1}}{dt} \\
 \text{else} \quad & I_C = \frac{C_{jo}}{\left[1 + \frac{V_{KN1}}{V_j}\right]^M} \frac{dV_{KN1}}{dt}
 \end{aligned}$$

Similarly to the transistor model, the parameters C_{jo} , V_j , and M are device specific parameters that can be found from measurements of the device or from the manufacturer's

datasheet. The resistor R_{esr} models the parasitic resistance of the diode capacitance, and the resistor R_{on} models the increase in forward voltage drop with increased diode current. The voltage source V_{on} represents the typical forward voltage drop at low currents. D_{ideal} acts as an ideal diode to model the fundamental behavior of the device. The parasitic lead inductance is represented by L_s .

To illustrate the accuracy with which the non-linear capacitance is characterized by the model, Figure 4.9 shows a plot of measured capacitance and modelled capacitance for the S310 Schottky diode for various voltages.

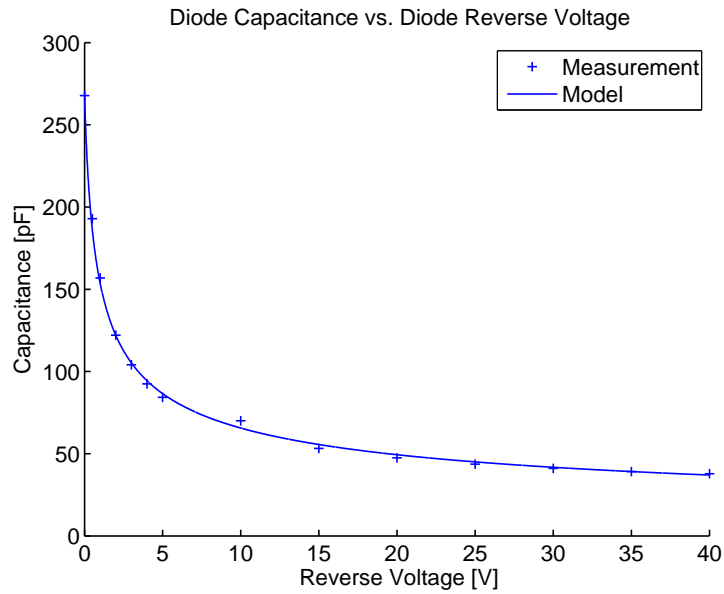


Figure 4.9: Plot comparing output capacitance of SPICE model to measured capacitance of S310 for different reverse voltages.

The code for the complete SPICE diode model is presented in Appendix B.2.

Resonant Gate Drive Circuit

ONE challenging aspect of VHF dc-dc converter design is the implementation of the gate drive circuitry. Ideally, one would like complete control over frequency, duty-ratio, and gate voltage waveforms while maintaining low loss and small size. In reality there is, as always, a trade-off between these desired characteristics. This chapter begins with a brief overview of different gate drive concepts and their relative merits for high frequency operation. A low-loss self-oscillating resonant gate drive circuit is then introduced which solves many of the problems associated with conventional gate drive circuits. Simulated results for an example 110 MHz gate drive circuit are then provided.

5.1 Resonant Gating Concepts

5.1.1 Hard Gating

In conventional converters operating at frequencies below 1 MHz, hard gating (or square-wave gating) is often employed. A two-switch implementation of this concept is illustrated in Figure 5.1.

To turn S_{main} on, S_{top} is turned on (S_{bottom} remains off) to charge the parasitic capacitance C_{gs} to a voltage V_g . To turn S_{main} off, S_{top} is turned off and S_{bottom} is turned on, discharging the capacitor C_{gs} to ground. For switching cycles much longer than the time constant $C_{gs}R_g$ (most often the case at lower frequencies), the gate voltage is approximately a square wave. If the capacitor C_{gs} is assumed to be linear (sometimes a reasonable approximation), the total energy dissipated in this transition is:

$$E_{gate} = \frac{1}{2}C_{gs}V_g^2 + \frac{1}{2}C_{gs}V_g^2 = C_{gs}V_g^2 \quad (5.1)$$

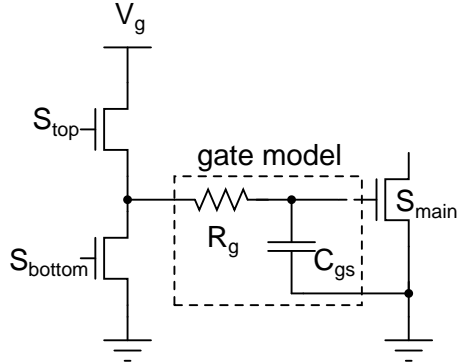


Figure 5.1: *Circuit illustrating hard gating concept.*

where an equal amount of energy is dissipated in the charging and discharging process. For a switching frequency f , the gate drive power loss is:

$$P_{gate} = C_{gs} V_g^2 f \quad (5.2)$$

Whereas this power loss is small enough to not be a major concern for frequencies in the hundreds of kHz, it can become a dominant power loss in soft-switching resonant converters operating in the VHF range [41].

Another issue complicating hard gating at VHF frequencies is the current required to deliver enough charge to C_{gs} to turn S_{main} on quickly. To prevent excessive power loss at turn-on and turn-off of the switch S_{main} , it is desirable that this charge delivery time is a small fraction of one switching cycle. Consequently, the switches S_{top} and S_{bottom} must be able to source and sink very large currents, a demand which can be difficult to meet.

For practical implementations of hard gating, care must be taken that the transistors S_{top} and S_{bottom} do not conduct simultaneously. This would cause a shoot-through current spike, which would be damaging to the transistors in addition to being detrimental to converter efficiency.

5.1.2 Resonant Gating

Figure 5.2 illustrates the concept of resonant gating [9, 19, 41, 46–51], which uses a resonant network to charge and discharge the gate.¹ In the topology of Figure 5.2, the inductor L_{res} is chosen to resonate with the parasitic gate capacitance C_{gs} at the switching frequency, providing a sinusoidal voltage at the gate.

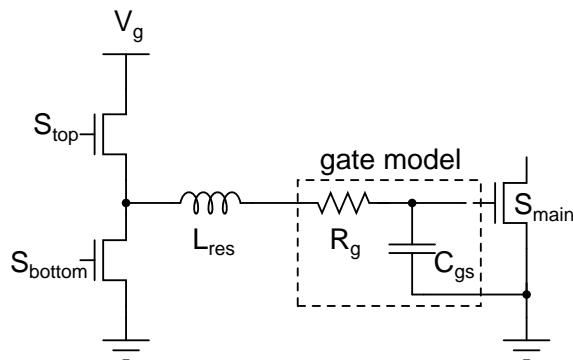


Figure 5.2: Circuit illustrating resonant gating concept.

Instead of dissipating the stored energy of the capacitor each cycle (which is done in hard gating), the energy is transferred between the capacitor (stored as electric field) and the inductor (stored as magnetic field), essentially ringing charge on and off the gate. The only energy-loss is associated with the parasitic resistance of the gate (R_g), which is typically a fraction of the energy loss that would be incurred by hard gating. It can be shown [16, 41] that the power loss for the topology of Figure 5.2, for an operating frequency f , is:

$$P_{gate} = 2R_g\pi^2 f^2 C_{gs}^2 V_{g,ac}^2 \quad (5.3)$$

Here $V_{g,ac}$ is the amplitude of the sinusoidal ac voltage. To ensure that the transistor turns fully on with a sufficiently fast transition, this voltage has to be larger than the square-wave amplitude V_g of the conventional gate drive. Nevertheless, the use of a resonant gate drive can significantly reduce gating losses in cases where the required switching time is much longer than a gate time constant, $R_g C_g$.

¹As explained in [41] this simple topology is not the most suitable implementation of resonant gating at VHF frequencies. It is displayed here only to illustrate the *concept* of resonant gating.

Resonant Gate Drive Circuit

To illustrate how this power loss compares to that of hard gating, Figure 5.3 shows the hard gating loss (Equation 5.2) and resonant gating loss (Equation 5.3) vs. frequency for the device MRF6S9060. The value for $V_{g,ac}$ is the required ac voltage to ensure that the sinusoidal gate voltage transitions from 0 V (off) to 5 V (on, as shown in Table 4.3) in a time t_s , given by:

$$V_{on} = V_{g,ac} \sin(2\pi f * t_s) \quad (5.4)$$

For a value of t_s corresponding to 5% of one switching cycle, the required $V_{g,ac}$ is 16.2 V. A desirable property of resonant converters is the relatively long switch transition-time allowed. If the transition time is instead permitted to be 10% of one switching cycle, the required value of $V_{g,ac}$ is 8.5 V. Both these values of $V_{g,ac}$ are plotted in Figure 5.3, together with the hard gating case for $V_g = 5$ V.

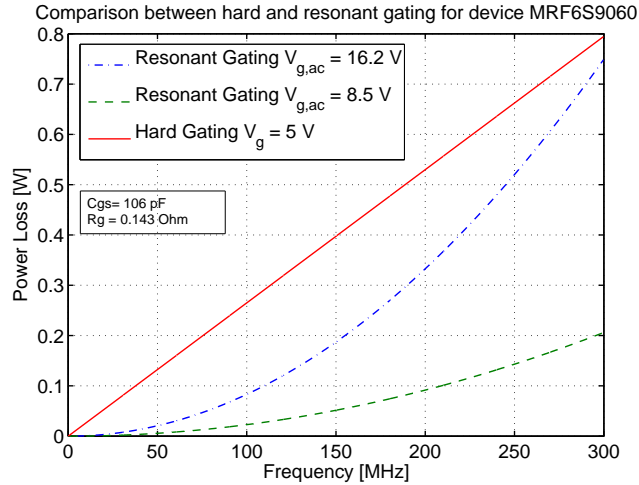


Figure 5.3: Plot of gating loss for resonant and hard gating with parameters from the MRF6S9060 rf MOSFET. Note that the MRF6S9060 cannot, in fact use sinusoidal gating for reasons discussed in the following section.

As is evident from Figure 5.3, resonant gating incurs substantially lower losses in the frequency range of interest (30-300 MHz) for the chosen semiconductor switch. Consequently, the design considered here employs a resonant gating scheme which is detailed in the following section.

5.2 Gate Drive Implementation

The semiconductor switch (MRF6S9060), identified in Chapter 4 as the most suitable device, places certain restrictions on the gate drive implementation. To protect the gate from electrostatic discharge (ESD), the manufacturer incorporated a protective diode between the gate and source terminals. This has the consequence that the gate voltage cannot be driven below -0.5 V, which in turn restricts the choice of gate drive circuits to those that provide a gate voltage above this value at all times. This excludes many designs [9, 19, 41, 46, 51] that utilize simple LC networks which provide sinusoidal waveforms at the gate.

The Φ_2 inverter, introduced in Chapter 3, provides a resonant non-negative quasi-square wave voltage across a capacitor, which is suitable to drive the gate of a MOSFET [16, 52]. As a resonant topology it provides low-loss operation, which is critical to achieving high overall converter efficiency. Figure 5.4 depicts a gate drive circuit utilizing the Φ_2 inverter, where the load network consists of the input capacitance (C_{gs}) of the switch S_{main} and its associated parasitic inductance and resistance (L_g and R_g). In the implementation developed here, the switch S_{aux} is the rf LDMOS transistor L8821P from Polyfet, chosen for its small package size, small capacitances, and its ability to sustain negative gate voltages. The switch S_{main} is the MRF6S9060 by Freescale Semiconductor, identified as the most suitable device in Chapter 4.

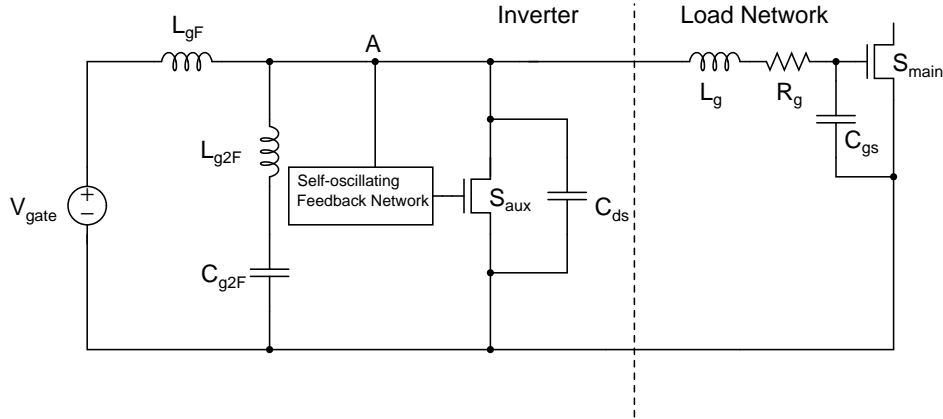


Figure 5.4: Schematic drawing of a Φ_2 -based gate drive circuit which provides quasi-square wave non-negative gate voltages.

The first step in the design of the gate drive circuit is the selection of the components

Resonant Gate Drive Circuit

L_{gF} , L_{g2F} , and C_{g2F} . These components are chosen to, together with C_{ds} of S_{aux} , ensure ZVS conditions for the (auxiliary) gate drive and to shape the drain voltage of S_{aux} . The design procedure is similar to that outlined in Chapter 3, where the drain impedance at the first, second, and third harmonic of the switching frequency are carefully selected to provide the proper waveshaping. The circuit of Figure 5.4 is initially tuned in simulation to provide the desirable voltage waveform with a sinusoidal voltage of frequency 110 MHz applied to the gate of S_{aux} (with the self-oscillating feedback network disconnected). Figure 5.5 shows the resulting S_{main} waveforms and component values. The full simulation SPICE code is presented in Appendix A.2.

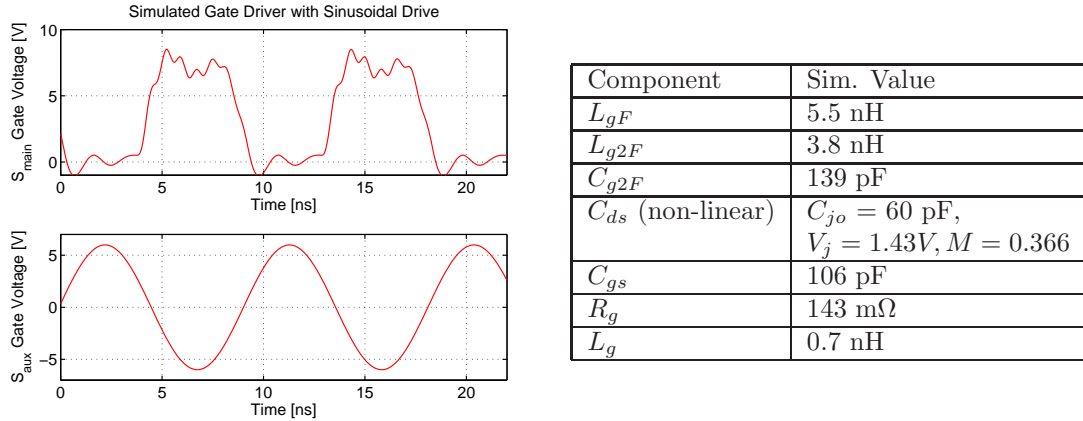


Figure 5.5: Simulated quasi-square wave gate voltages of S_{main} (top), when S_{aux} is driven with a sinusoidal voltage source (bottom). Component values as listed in table.

The S_{main} gate voltage plot of Figure 5.5 illustrates how the Φ_2 inverter can provide the requisite waveforms for resonant low-loss gating. Unlike a hard-gated design, the energy stored in the MOSFET capacitances is recycled (resonated) each cycle back to the gate drive power supply (minus the amount lost due to conduction through parasitic resistances). It can be shown that such a quasi-trapezoidal waveform is the most efficient possible for a specified transition time [16, 37, 52, 53]

To complete the design, the sinusoidal signal applied to the gate of S_{aux} in the simulation must now be replaced by a suitable self-oscillation network, as illustrated in Figure 5.4. The next section treats the synthesis of such a self-oscillation network.

5.2.1 Self-oscillating Feedback Network

The design of a self-oscillating feedback network suitable to drive the Φ_2 inverter is presented in [16, 52], and a similar feedback network is employed for the design considered here. Figure 5.6 shows a schematic of the proposed network, with the component values as listed in the accompanying table. The derivation of this network is treated in [52]. As is shown in Figure 5.7, the transfer function $\frac{V_B}{V_A}$ of the network provides a phase shift of 180° and a magnitude of approximately unity at 110 MHz.

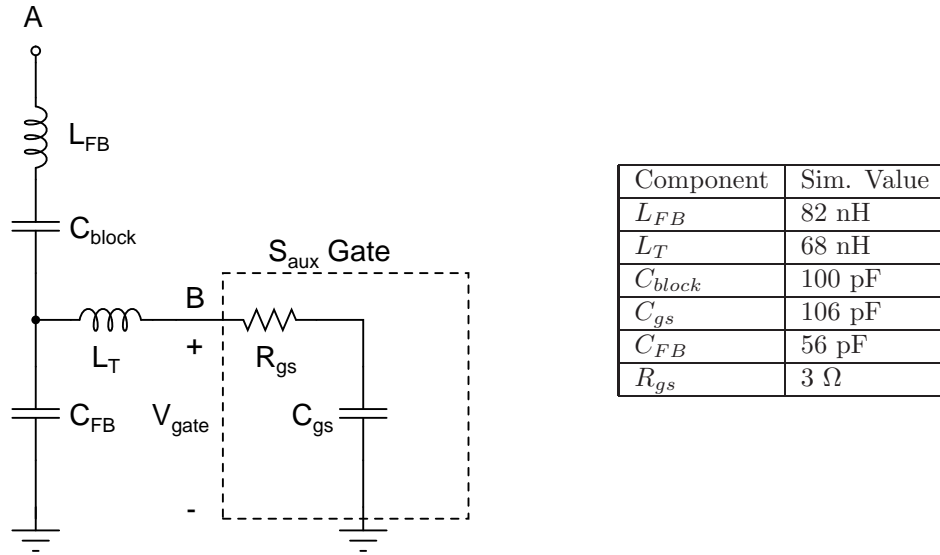


Figure 5.6: Schematic drawing of self-oscillating feedback network which provides 180° of phase shift between node A and B for component values as listed in table.

The component values to achieve the proper transfer function of the feedback network in Figure 5.6 were selected in the following manner: as a design starting point, component values similar to those in [52] were chosen. The network was then re-tuned in simulation to adjust for the higher switching frequency of the current design (110 MHz instead of 100 MHz). To reduce the physical size of the gate drive circuitry, the network was tuned to minimize the inductors L_T and L_{FB} , while maintaining the desired transfer function characteristics.

Another critical aspect of the design of the feedback network is how it affects the impedance at node A of Figure 5.4, which is the drain of the auxiliary switch, S_{aux} . Since the impedance of this node is tuned to provide the proper waveshaping of the drain voltage, care must be

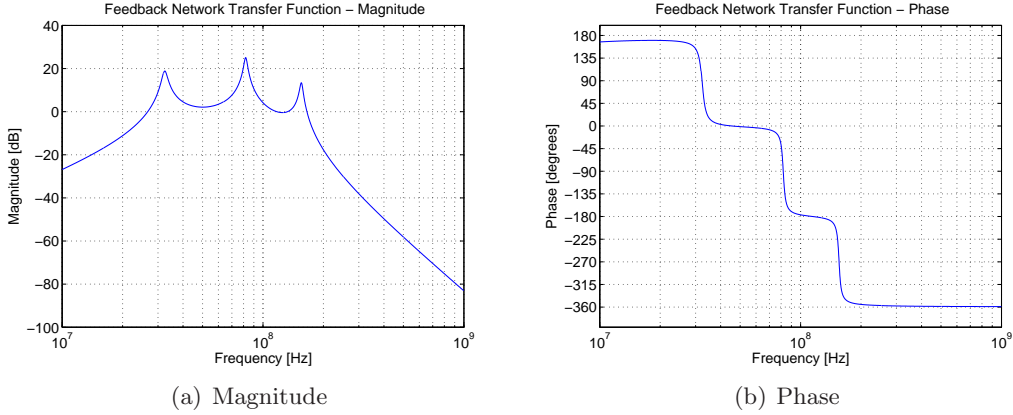


Figure 5.7: Magnitude (a) and phase (b) of the feedback transfer function $\frac{V_B}{V_A}$ of Figure 5.6.

taken to ensure that the feedback network does not improperly load this node. Figure 5.8 shows the corresponding change in magnitude of the impedance at node A (of Figure 5.4) vs. frequency when the feedback network is connected. The impedance at the fundamental of the switching frequency (110 MHz) changes somewhat, but the impedance at the second and third harmonic remain the same for both cases. Simulations and experimental measurements verify that the small change in impedance by the addition of the feedback network does not noticeably change the voltage waveforms of the gate drive circuit.

5.2.2 Simulation of Resonant Gate Drive with Feedback Network

The complete gate drive circuit is shown in Figure 5.9, where the network of Figure 5.6 has been placed to provide the feedback path between the drain (node A) and the gate of the switch S_{aux} . Figure 5.10 shows the simulated time-domain waveforms for this circuit, which illustrates the quasi-square waveforms at the gate of S_{main} and the phase-shifted sinusoidal gate voltage of S_{aux} . The full simulation SPICE code is presented in Appendix A.2

5.2.3 Gate Drive Startup

The control strategy outlined in Chapter 6 places an additional requirement on the gate drive circuit: rapid startup and shutdown. To maintain high efficiency at light load, the converter must reach steady state operation in a few cycles. This requirements necessitates

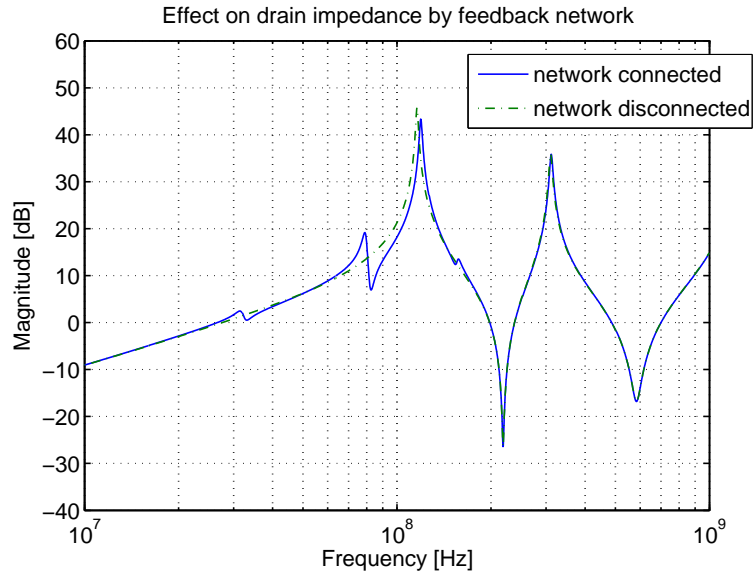


Figure 5.8: Gate drive drain impedance (node A of Figure 5.4) with feedback network connected and disconnected.

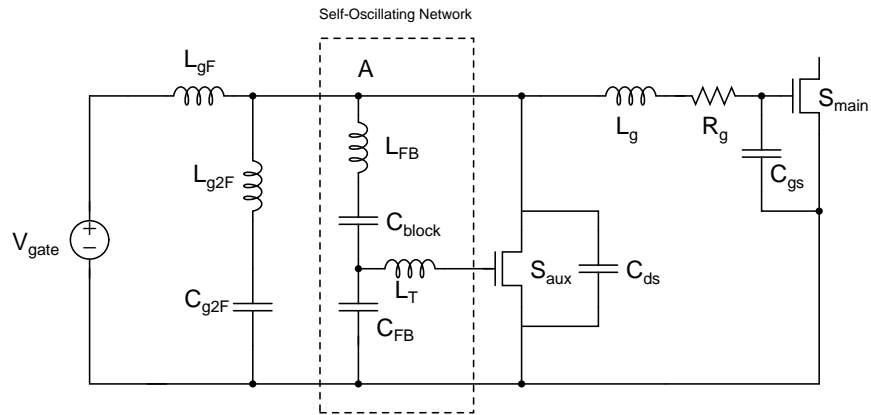


Figure 5.9: Schematic drawing of gate drive circuit with attached feedback network.

Resonant Gate Drive Circuit

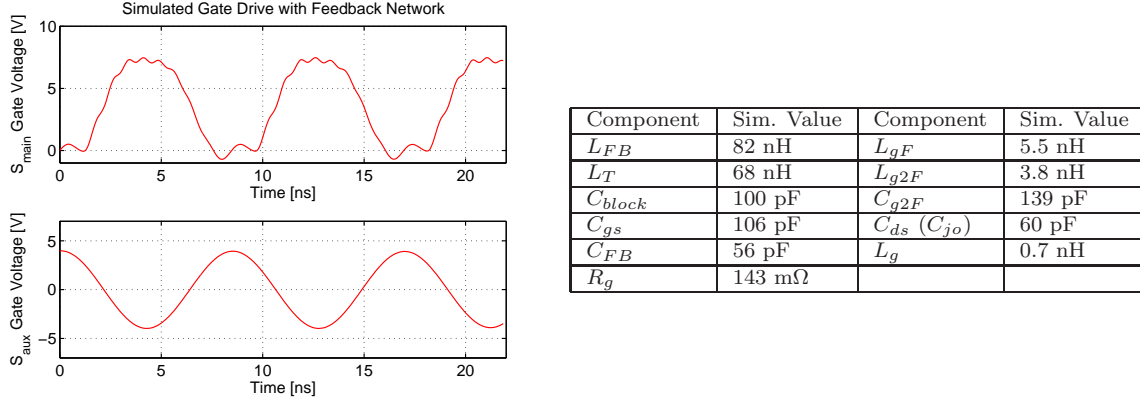


Figure 5.10: Simulated waveforms at the gate of S_{main} (top) and gate of S_{aux} (bottom) for the circuit of Figure 5.9.

a gate drive circuit with sub-microsecond startup and shutdown time.

Simulated results of the gate drive circuit of Figure 5.9 indicate that the gate voltage of S_{main} reaches steady state oscillation within a few cycles after the voltage V_{gate} is applied. However, as often is the case with oscillations, this behavior was not observed in the experimental gate drive circuit (described in Chapter 8). Although the experimental self-oscillating network started, the time for the gate voltage to reach steady state was several microseconds, rendering an unacceptable converter startup time.

To rectify this situation, a small inductor L_{start} is placed between the gate drive input node and the node connecting C_{block} , C_{FB} , and L_T , as shown in Figure 5.11. It is found (experimentally), that an inductor of 13 nH is sufficient to initiate the oscillation of the feedback network, enabling rapid startup of the gate drive circuit. One consequence of the introduction of L_{start} in the circuit is that the average gate voltage of S_{aux} is forced to be equal to V_{gate} , which can be found by the application of the principle of volt-second balance. This is an undesirable constraint, but acceptable in this case since the gate voltage (~ 3.6 V) is sufficiently close to the threshold voltage of S_{aux} (~ 2.8 V). Consequently, the gate voltage of S_{aux} is a sinusoidal waveform with a 3.6 V offset. Experimental steady-state and startup waveforms of the implemented gate drive circuit are presented in Chapter 8, along with a discussion of design layout considerations.

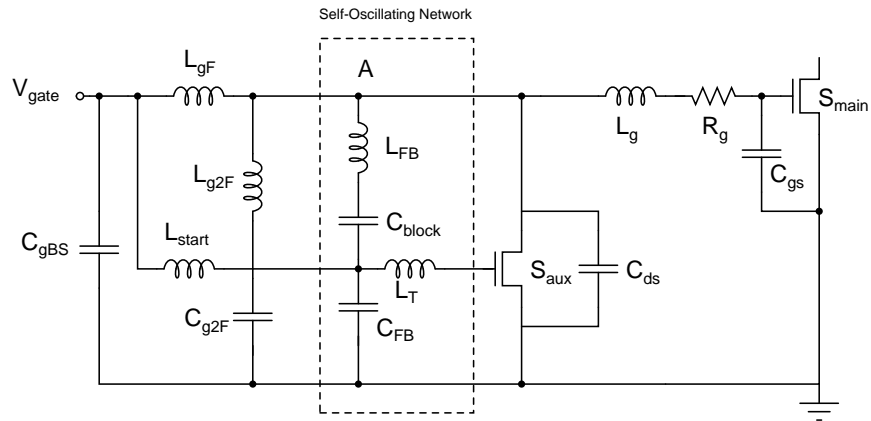


Figure 5.11: Schematic drawing of experimental implementation of the gate drive circuit with inductor L_{start} to improve startup time.

Control Architecture

AN important function of dc-dc power conversion is the ability to tightly regulate the output voltage. Many applications place strict restrictions on the allowed output voltage ripple, both in steady state and for transient events. The ability to maintain the output voltage during rapid changes of input voltage and/or load resistance is therefore a desirable property of a power converter.

As previously discussed in Chapter 1, control of resonant converters at very high frequencies can be challenging. This chapter presents a simple yet powerful control architecture particularly well suited for resonant converters operating at fixed frequency and duty ratio. The control method, which separates the control from the power processing function, allows for greatly improved transient response compared to conventional converters. In addition, high efficiency over a wide load range is made possible, something that is typically difficult to achieve with resonant converters.

6.1 General Theory

6.1.1 Resonant Converter Control Strategies

One of the more common control strategies for resonant converters is frequency modulation [2, 6, 7, 9]. One disadvantage of this strategy is the tight coupling between control functions and power processing. Since resonant converters employ reactive elements specifically chosen to resonate at certain frequencies to deliver power, any change in the operating frequency will necessarily alter the voltages and currents of the converter. Although this characteristic trait of resonant converters can be leveraged to provide output regulation (as is done in frequency modulation), a potential negative consequence is decreased efficiency

due to non-ZVS waveforms and/or increased resonant currents in the reactive elements. This is one reason for the poor light load efficiency sometimes encountered in resonant converters [3,6–8,10,13,14]. Yet other disadvantages of frequency modulation are the problems of designing good inductors over a wide frequency range, and the increased difficulty of handling conducted and generated noise compared to a fixed-frequency solution [54].

Traditional pulse-width modulation (PWM) techniques have also been applied to resonant converters [10,54–56]. However, the use of PWM techniques at VHF frequencies is complicated by the demand it places on the gate drive circuit. Low loss gating in combination with precise duty ratio control becomes challenging at higher frequencies. For instance, resonant gating schemes such as that presented in Chapter 5 cannot be used since they are designed for fixed duty ratio. Light-load efficiency can also be difficult to achieve with PWM control, since it has been observed [54] that the total power loss remains relatively constant throughout load range.

Phase-shift control [57–59] is also sometimes used in converters employing multiple switching devices. While this can be effective, it requires the use (and gating) of multiple switches, and can provide poor efficiency at light load. Other methods for constant frequency control of resonant converters include switch-controlled capacitors and inductors [60,61] which change the resonant frequency of an LC tank, thereby enabling regulation of the converter while keeping the switching frequency fixed. These methods add complexity and cost by introducing additional independent control requirement, as well as non-standard components.

6.1.2 On-off Control

The control strategy for the converter developed here is a simple on-off hysteretic control scheme [12,15,16] (also referred to as burst-mode control). That is, when the output voltage falls below a specified threshold, the converter is enabled and delivers power to the output (operating at its designed switching frequency), causing the output voltage to gradually increase. When the output rises above a specified threshold, the converter is disabled, and the output voltage gradually decreases.

This on-off control scheme realizes the advantages of separating the control from the

power processing function [19]. A particular advantage of this scheme is that the converter incurs no losses when it is disabled, and operates at a fixed high-efficiency point when it is enabled. Consequently, efficient operation can be maintained over a much larger load range than is possible with many other control strategies.

With this control method the input and output voltage ripples have components near the modulation frequency (the frequency at which the converter is modulated on and off) and its harmonics, in addition to components near the very high switching frequency. This influences the sizing of the bulk input and output capacitors. Nevertheless, the main power stage components are sized based on the very high switching frequency, enabling miniaturization and fast transient response.

The basic scheme presented in Figure 6.1 utilizes a comparator with hysteresis to generate the modulation signal, a voltage reference to set the dc level, and a voltage divider to sense the output voltage. The ripple voltage is determined by the comparator (with a small impact due to filtering of the output voltage) and is proportional to the hysteresis band. Bulk capacitance is added at the output and sized according to the desired modulation frequency range and expected load. It is important to note that the transient performance of the converter is not determined by the modulation frequency, but by the delay around the control loop and the switching frequency of the converter.

The on/off control strategy outlined in Figure 6.1 provides several benefits when used in conjunction with resonant converters: By enabling fixed switching frequency operation, the control strategy can be used together with a converter that is tuned to be highly efficient at a specific frequency. Furthermore, resonant gating can be used, providing efficient, fixed duty ratio, gate drive.

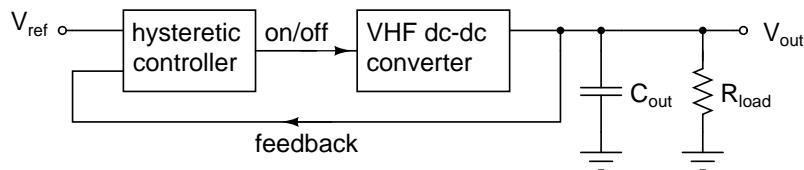


Figure 6.1: A block diagram illustrating on/off control of a VHF resonant dc-dc converter. This control strategy enables efficient operation over a wide load range and allows the converter to be optimized for a fixed frequency and duty ratio.

6.2 Example Implementation

This section discusses a possible implementation of the on-off control strategy outlined in Figure 6.1. Various design trade-offs (and their impact on converter performance) are discussed, as well as methods to increase the robustness of the hysteretic control strategy.

6.2.1 Reference Voltage

The reference voltage of Figure 6.1 is provided by the ADR390 from Analog Devices. It is a 2.048 V, micropower, low-noise precision voltage reference in a TSOT-23-5 package. In order to compare the high converter output voltage to this reference value, the output voltage is measured using a voltage divider, as shown in Figure 6.2.

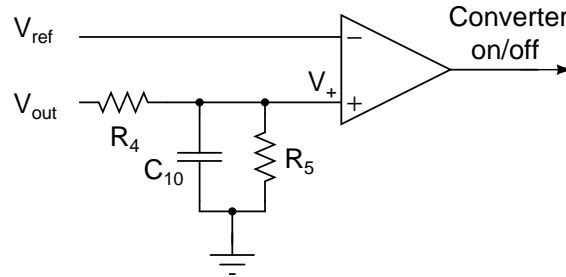


Figure 6.2: A block diagram illustrating the voltage divider network used to measure the output voltage and compare it to a desired reference voltage. The capacitor C_{10} and resistor R_4 provide high-frequency filtering of the converter output signal.

The capacitor C_{10} is sized together with the resistor R_4 to provide low-pass filtering of the high-frequency content of the output voltage. Furthermore, the resistors R_4 and R_5 are sized so that the voltage V_+ at the comparator input is equal to the reference voltage provided by the ADR390, for a desired output voltage level. As is discussed in Chapter 7, care must be taken in the board layout so that the reference voltage provided by the ADR390 is stable in the face of large high frequency signals in the surrounding power components.

6.2.2 Comparator and Hysteresis Band

The comparator of Figure 6.2 is implemented using the TLV3501 from Texas Instruments. It is a high-speed push-pull output comparator with low supply current and small package size (SOT23-6). The TLV3501 provides 6 mV of internal hysteresis for improved noise immunity. This is supplemented by an external hysteresis circuit, as illustrated in Figure 6.3.

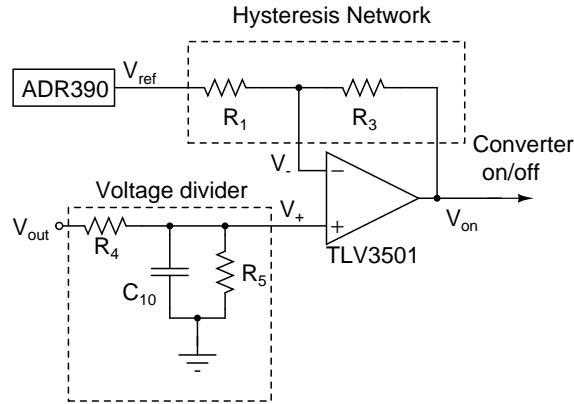


Figure 6.3: A schematic of a hysteretic control circuit, complete with voltage divider network and hysteretic feedback network. Component values for the experimental implementation are given in Table 7.3 of Chapter 7.

When the voltage V_{on} is high, the converter is enabled, causing the output voltage to gradually rise. At this point, the negative input terminal of the comparator (V_- of Figure 6.3) has a dc voltage equal to:

$$V_{-,high} = V_{on} \frac{R_1}{R_1 + R_3} + V_{ref} \frac{R_3}{R_1 + R_3} \quad (6.1)$$

Once the output voltage reaches a value where V_+ is above this value, the comparator will change state, forcing its output voltage V_{on} to 0 V. This will turn off the converter, causing the output voltage to gradually decrease. When $V_{on} = 0$ V, the negative input terminal of the comparator has a dc voltage equal to:

$$V_{-,low} = V_{ref} \frac{R_3}{R_1 + R_3} \quad (6.2)$$

The hysteresis band is then the internal hysteresis of the comparator (6 mV) plus the

difference between $V_{-,high}$ and $V_{-,low}$,

$$\Delta V_+ = 6mV + V_{on} \frac{R_1}{R_1 + R_3} \quad (6.3)$$

The peak-to-peak swing of the voltage V_+ of Figure 6.3 is equal to this hysteresis band, which in turn is directly proportional to the output voltage ripple (ΔV_{out}) of the converter. As is seen from Figure 6.3,

$$\Delta V_+ = \Delta V_{out} \frac{R_5}{R_5 + R_4} \rightarrow \Delta V_{out} = \Delta V_+ \frac{R_5 + R_4}{R_5} \quad (6.4)$$

The relative values of resistors R_5 and R_6 are typically fixed (for a given voltage reference and desired output voltage). Thus, with this on-off control strategy, the output voltage ripple is determined by ΔV_+ (which is set by the choice of the resistors R_1 and R_3). Furthermore, the minimum achievable output ripple is found for $R_1 = 0$. For an output voltage of 33 V and a voltage reference of 2.048 V, the minimum output ripple is, for this choice of comparator with 6 mV of internal hysteresis:

$$\Delta V_{out,min} = 6 \text{ mV} \frac{33}{2.048} = 96.7 \text{ mV} \quad (6.5)$$

It is also clear that a higher voltage reference would reduce this minimum achievable voltage ripple, as it reduces the required voltage divider ratio. What typically places an upper bound on the voltage reference is the available logic voltage, as well as the maximum rated input voltage of the comparator.

In a practical design, it is advisable to use some external hysteresis to mitigate problems associated with high-frequency content of the output voltage falsely triggering the comparator. When the converter is on (output voltage ramping up), the converter drain voltage contains high frequency components from the 110 MHz switching frequency and its harmonics. This unwanted signal, called pickup or hash, is detected by the comparator because of its proximity to the rapidly changing waveforms of the inverter, as well as voltage induced by the magnetic flux leakage of the inductors. It was observed experimentally that this high frequency content could be large enough to cause false triggering of the comparator. When the output voltage was very close to the maximum allowed value, this false triggering would manifest itself as a series of rapid turn-on and turn-offs of the converter, which is

detrimental to overall efficiency and regulation.

One obvious solution to this problem is just to adjust the resistors R_1 and R_3 until the hysteresis band large enough to prevent any false triggering. However, this has the effect of increasing the output voltage ripple as well, which is sometimes undesirable. Another solution then, is to add a parallel capacitor in the feedback path, as shown in Figure 6.4.

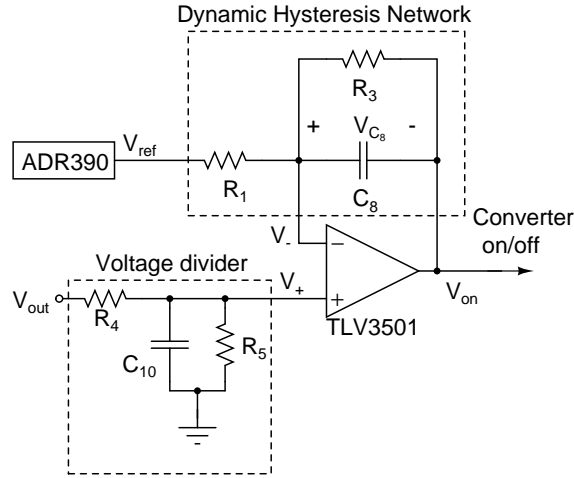


Figure 6.4: A schematic of a dynamic hysteretic control circuit, which employs a capacitor in the feedback path to mitigate problems associated with high frequency pickup. Component values for the experimental implementation are given in Table 7.3 of Chapter 7.

The use of a capacitor (C_8) in the feedback path provides *dynamic* hysteresis in the following manner: the moment before the comparator output switches from high to low ($t = 0^-$), the voltage across the capacitor is equal to:

$$V_{C_8}(t = 0^-) = V_- - V_{on} = V_{on} \frac{R_1}{R_1 + R_3} + V_{ref} \frac{R_3}{R_1 + R_3} - V_{on} = (V_{ref} - V_{on}) \frac{R_3}{R_1 + R_3} \quad (6.6)$$

At $t = 0$, the comparator output switches from high to low ($V_{on} = 0$ V). Since the voltage across the capacitor C_8 cannot change instantaneously, $V_{C_8}(t = 0^-) = V_{C_8}(t = 0^+)$, and the voltage V_- at $t = 0^+$ is given by:

$$V_-(t = 0^+) = V_{C_8}(t = 0^+) = (V_{ref} - V_{on}) \frac{R_3}{R_1 + R_3} \quad (6.7)$$

Using above initial conditions, the differential equation governing the time-dependence

of the voltage V_- can be solved to find that:

$$V_-(t)_{high \rightarrow low} = V_{ref} \frac{R_3}{R_1 + R_3} - V_{on} \frac{R_3}{R_1 + R_3} e^{\frac{-t}{R_1 || R_3 C_8}} \quad (6.8)$$

Similarly, the time-dependence for a comparator transition from low to high is found to be:

$$V_-(t)_{low \rightarrow high} = V_{ref} \frac{R_3}{R_1 + R_3} + V_{on} \frac{R_3}{R_1 + R_3} e^{\frac{-t}{R_1 || R_3 C_8}} + V_{on} \frac{R_1}{R_1 + R_3} \quad (6.9)$$

We then define a *dynamic* hysteresis band as the 6 mV of internal hysteresis, plus the difference between $V_-(t)_{low \rightarrow high}$ (Equation 6.9) and $V_-(t)_{high \rightarrow low}$ (Equation 6.8):

$$\Delta V_{+dynamic} = 6mV + V_{on} \frac{R_1}{R_1 + R_3} + 2V_{on} \frac{R_3}{R_1 + R_3} e^{\frac{-t}{R_1 || R_3 C_8}} \quad (6.10)$$

When comparing Equations 6.10 and 6.3, it can be seen that the addition of capacitor C_8 has the effect of temporarily increasing the effective hysteresis band, with the increment exponentially decaying with a time constant $R_1 || R_3 C_8$. This dynamic behavior is precisely what is needed to solve the problem of false triggering associated with high-frequency pickup.

As soon as the comparator switches from high to low (and the converter turns off) the voltage V_- drops to a value that is sufficiently low such that no high-frequency pickup can re-trigger the comparator. If this increased hysteresis band would be permanent, the overall effect would be an increased output voltage ripple, which is not desirable. Therefore, the RC time constant ($R_1 || R_3 C_8$) is selected to be much less than one period of the modulation frequency. This ensures that the exponential term of Equation 6.10 decays sufficiently fast (compared to the modulation frequency) such that the hysteresis band that governs output voltage ripple is that given by Equation 6.3. It thus follows that the RC time constant is chosen to be larger than the time-constant associated with the 110 MHz switching frequency of the converter to suppress the effects of comparator high-frequency pickup, but smaller than the modulation frequency (typically in the hundreds of kHz), to minimize output voltage ripple.

The dynamic hysteresis concept is illustrated in Figure 6.5, which shows simulated waveforms for the circuits of Figures 6.5(c) and 6.5(d). These circuit are simplifications of Figure 6.4 and characterize the change in hysteresis band of Figure 6.3, without the added

complexity of the rest of the control circuitry. As illustrated in Figure 6.5(c), the voltage V_{on} is driven by a square wave (of frequency f_{mod}) to model the behavior of the comparator output of Figure 6.4. The effect on the voltage V_- can be seen in Figure 6.6(a), which illustrates the hysteresis band with the capacitor C_8 . Figure 6.6(a) clearly illustrates the increased/decreased threshold value immediately following a transition of V_{on} when compared to Figure 6.5(b) which displays regular hysteresis waveforms.

The component values for the simulation were as follows: ¹

$$f_{mod} = 200 \text{ kHz}, C_8 = 10 \text{ pF}, R_1 = 25 \text{ k}\Omega, R_3 = 100 \text{ k}\Omega, V_{ref} = 2.048 \text{ V}, V_{on} = 3.6 \text{ V}.$$

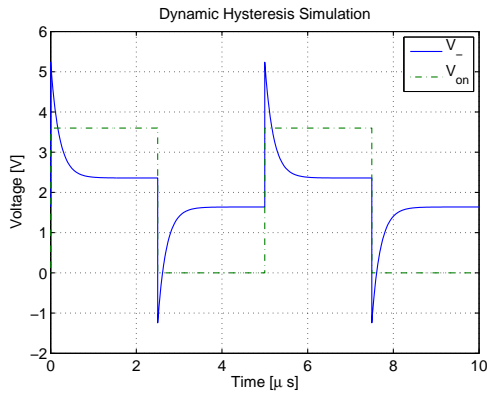
As the analysis above has shown, dynamic hysteresis is a powerful method to improve on/off control while maintaining low output voltage ripple. However, this concept can be further expanded by observing that the resistor R_3 of Figure 6.4 can be completely eliminated. The removal of R_3 from the feedback loop results in a dynamic hysteresis band that is composed entirely of the internal hysteresis of the comparator and the exponentially decaying factor contributed by the capacitor C_8 . This can be seen from Equation 6.10, by taking the limit as R_3 approaches infinity:

$$\lim_{R_3 \rightarrow \infty} \Delta V_{+dynamic} = 6mV + 2V_{on} e^{\frac{-t}{R_1 C_8}} \quad (6.11)$$

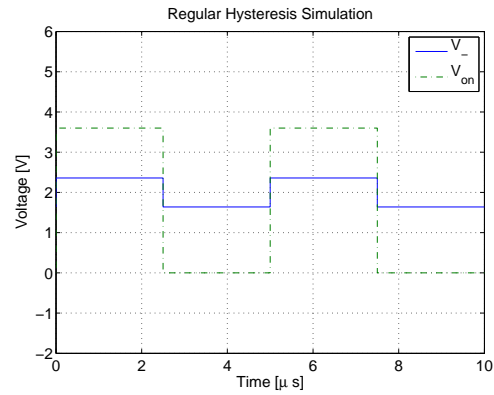
The time constant for the exponential decay is now set by R_1 and C_8 . Simulated waveforms for this case are shown in Figure 6.6.

For a system where the frequency of the disturbance (switching frequency in this case) is sufficiently high compared to the modulation frequency, the on-off control method can be made more robust by utilizing dynamic hysteresis. This has the advantage of reducing the output voltage ripple for the converter treated here.

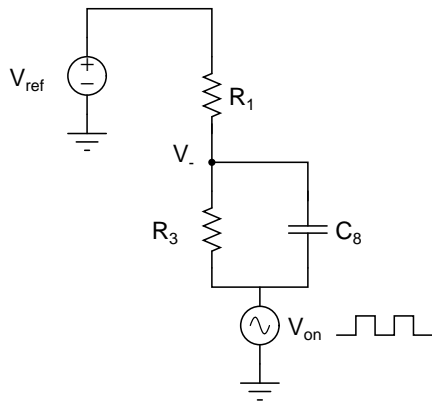
¹The values of resistors for the simulation were chosen such that the hysteresis band could be clearly identified in the graph. In a practical implementation, the selected hysteresis band would be considerably smaller.



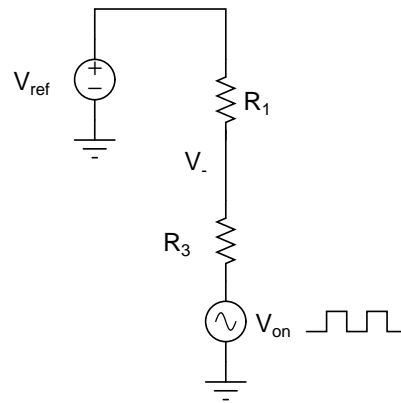
(a) Simulated waveforms for dynamic hysteresis for circuit of Figure 6.5(c) with component values: $C_8 = 10$ pF, $R_1 = 25$ k Ω , $R_3 = 100$ k Ω .



(b) Simulated waveforms for hysteresis for circuit of Figure 6.5(d) with component values: $R_1 = 25$ k Ω , $R_3 = 100$ k Ω .



(c) Simplified model of dynamic hysteresis feedback (Figure 6.3) used for simulation.



(d) Simplified model of hysteresis feedback (Figure 6.3) used for simulation.

Figure 6.5: Simulated results for dynamic hysteresis and regular hysteresis.

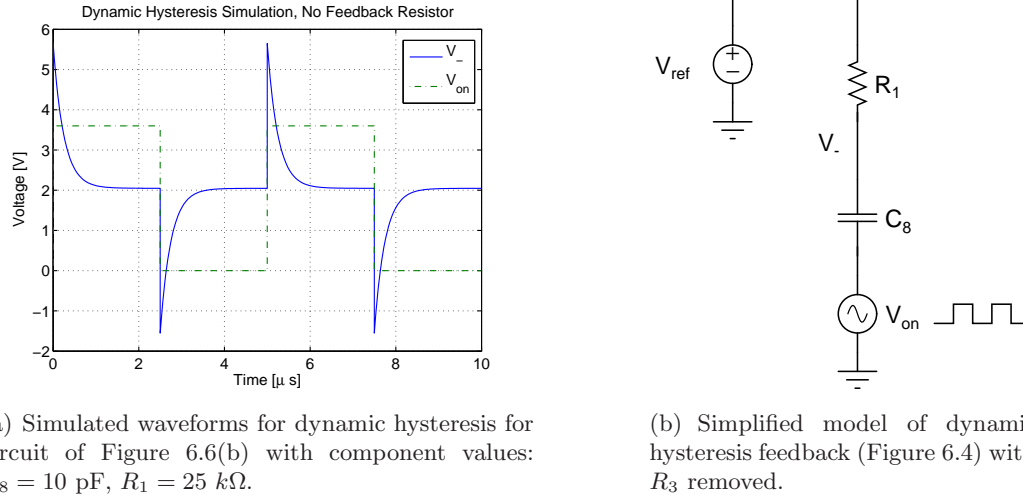


Figure 6.6: Simulated results for dynamic hysteresis with resistor R_3 removed from the feedback path.

6.2.3 Gate Drive Turn-On

When the output of the comparator TLV3501 goes high, the converter needs to start up quickly. As outlined in Chapter 5, this is accomplished by providing a voltage V_{gate} to the input of the resonant gate drive circuit (Figure 5.11). However, the TLV3501 is designed to drive high input impedance, logic-level, loads. It cannot supply the large current required to quickly charge the capacitors of the gate drive circuit of Figure 5.11. A designated gate drive chip, the LM5112 from National Semiconductor, is therefore used to turn on and off the gate drive circuit. The LM5112, which comes in a LLP-6 package, is able to source 3 A and sink 7 A, which ensures that the gate drive circuit can be turned on and off rapidly. The output of the comparator (TLV3501), is then connected to the input of the gate drive chip (LM5112). The output of the LM5112 is in turn connected to the input of the gate drive circuit (V_{gate} of Figure 5.11).

6.2.4 Powering the Logic Chips

Many of the logic chips used in the control circuitry have limitations on the maximum supply voltage which they can work from. None of them can work from a voltage as high as the converter maximum input voltage (16 V). The TLV3501, in particular, has a maximum

supply voltage of 5.5 V. In order to power the logic chips from the converter input, the TPS62110 from Texas Instruments is used to step down the converter input voltage (11-16 V) to a low-level logic voltage of 3.65 V. The TPS62110 is a high-efficiency synchronous step-down converter that can provide an adjustable output voltage between 1.2 and 16 V. It comes in a small 16-pin QFN package, but requires relatively large external inductors and capacitors.

A schematic of the complete control circuitry is presented in Figure 6.7. Chapter 7 provides, among other things, a complete listing of all the values of the control circuitry components (including bypass capacitors).

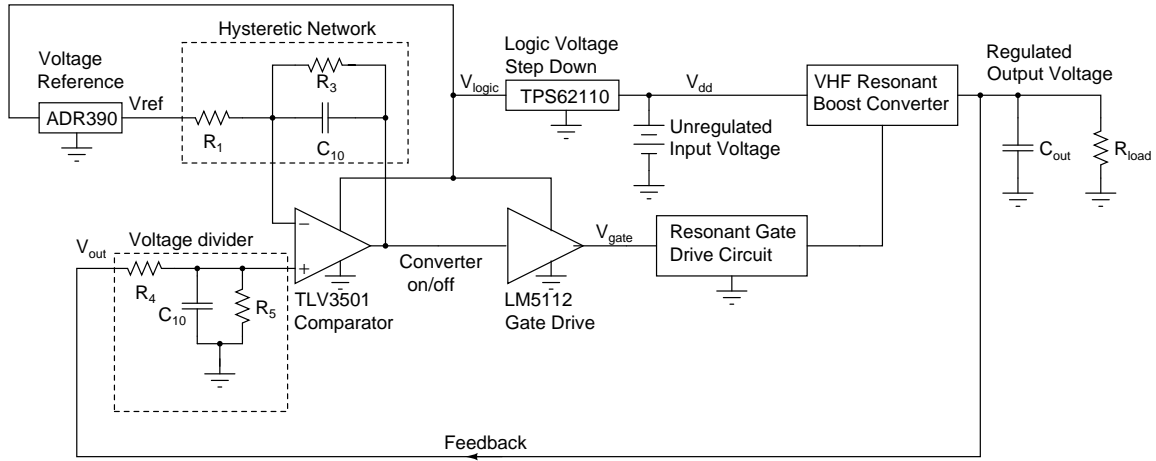


Figure 6.7: Complete schematic of converter control scheme. See Table 7.3 of Chapter 7 for component values used in the experimental implementation.

Design and Layout

PREVIOUS chapters have discussed the required parts of a dc-dc converter, beginning with the power stage of Chapter 3, the resonant gate drive circuit of Chapter 5, and finally concluding with the control circuit of Chapter 6. This chapter treats the consolidation of these pieces into an experimental implementation of a 110 MHz resonant boost converter.

For power converters operating in the VHF range, board layout is a particularly important part of the design process. Board traces must be carefully laid out to minimize undesirable inductance that can cause high frequency ringing, since such unwanted ringing can be detrimental to converter efficiency, or even worse, cause device breakdown. Furthermore, the effect of trace inductance must be adjusted for when selecting passive components, as the inductance contributed by the trace can be as large as some of the discrete inductors.

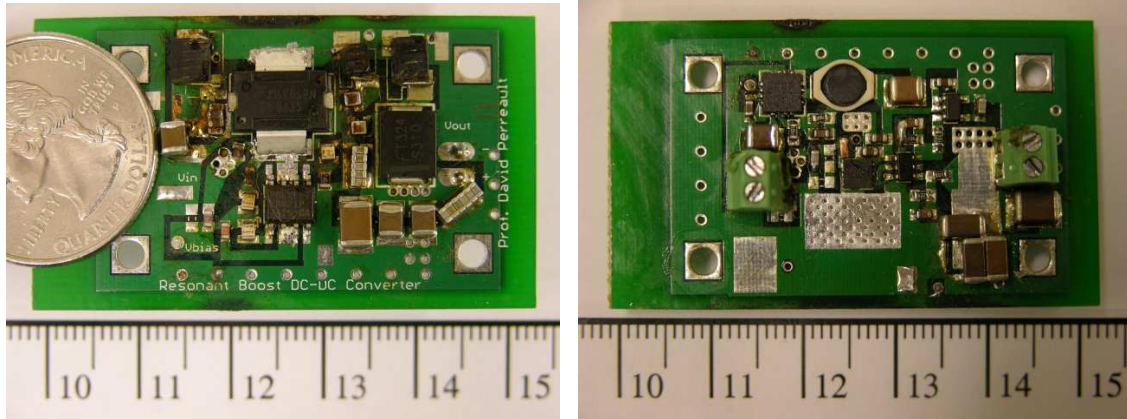
The PCB layout was made using EAGLETM Layout Editor from Cadsoft Computer, Inc. Appendix C provides the masks for selected layers used to manufacture the boards. The four layer prototype boards were manufactured by Advanced Circuits¹ with 1 oz copper. Figures 7.1(a) and 7.1(b) are photographs of the complete converter top and bottom, respectively.

7.1 Power Stage

Figure 7.2 shows a photograph of the converter with the power stage components labelled. A schematic drawing of the power stage is provided in Figure 7.3 for reference.

This schematic drawing differs slightly from Figure 3.1 of Chapter 3 by the addition of the bypass capacitor C_{IN} . This capacitor serves two purposes: it helps keep the voltage

¹www.4pcb.com



(a) Photograph of top side of converter with quarter shown for scale.

(b) Photograph of bottom side of converter.

Figure 7.1: Converter photographs of top and bottom sides with cm ruler shown for scale.

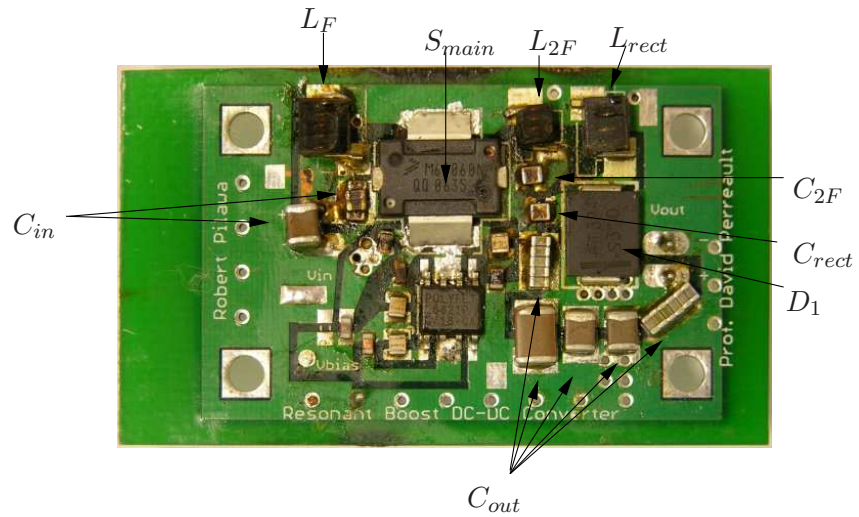


Figure 7.2: Photograph of converter with the power stage components labelled.

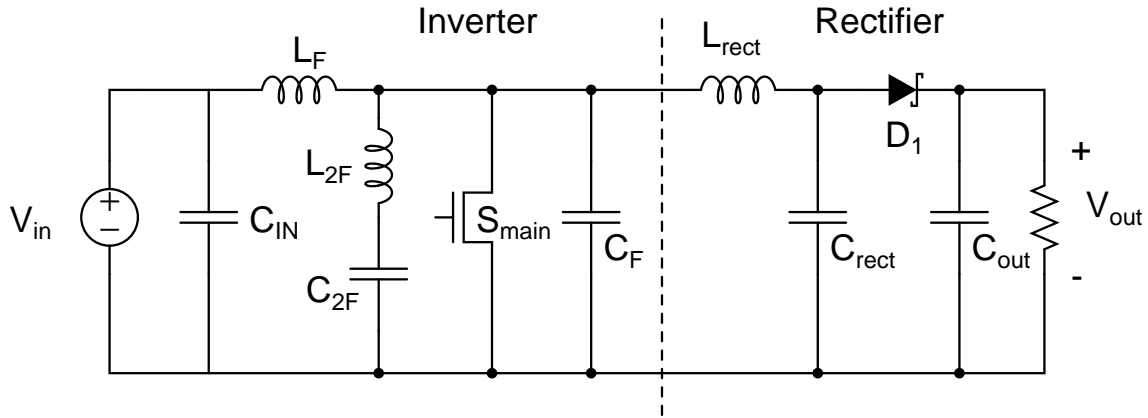


Figure 7.3: Schematic of resonant boost converter.

V_{in} stable by maintaining a buffer of charge available for the converter, and it presents an impedance at the fundamental of the switching frequency that is considerably smaller than that of L_F . The second purpose is important because, as opposed to an ideal voltage source which acts as an ac short, the power supply and meters attached to the input of the converter can present a substantial impedance at the switching frequency. Since the development of the resonant boost converter of Chapter 3 relied on a low impedance node at the input of the component L_F , the capacitor C_{IN} is sized to ensure this condition regardless of what power supply implementation is used.

7.1.1 Power Stage Board Layout

As can be seen in Figure 7.2, the components have been placed to minimize the important loop areas. It is particularly important to minimize loops that carry a large time-varying current, such as the $L_{2F} - C_{2F} - S_{main}$ loop, as outlined in Figure 7.4. Large parasitic trace inductance in this loop could cause significant induced voltages across the switch, leading to reduced efficiency and possibly device breakdown. Although it is advisable to strive for a tight layout, some loops are less critical than the loop mentioned above. For instance, the trace connecting C_{IN} , L_F and L_{2F} can be made longer, since any extra inductance in this loop will just add to the effective value of L_F . Consequently, the discrete component L_F can be made smaller to account for the inductance contributed by the trace.

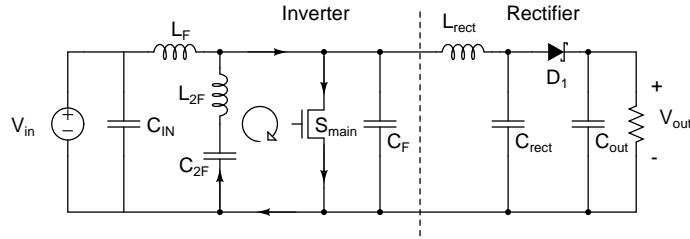


Figure 7.4: Schematic of resonant boost converter with one critical layout path highlighted.

7.1.2 Power Stage Components

Table 7.1 lists the components used for the power stage. All inductors are air-core inductors from Coilcraft. The discrete switching capacitors that are cyclically charged and discharged (C_{2F} and C_{rect}) are rf multilayer porcelain capacitors from American Technical Ceramics, specifically designed for low ESR. The input and output capacitances are provided by a mixture of discrete capacitors. The physically large (1210) capacitors provide bulk charge storage at the input and output. The bulk output capacitance is what largely determines the modulation frequency of the converter, as discussed in Chapter 6. However, the inductance associated with the large package size of these components make them unable to filter the high-frequency components of the output voltage of the rectifier. For this task, smaller (0603) capacitors are chosen which, thanks to their relatively small package inductance, present a lower impedance at the switching frequency and its harmonics.

7.2 Gate Drive Circuit

Figure 7.5 shows a photograph of the converter with the gate drive circuit components labelled. A schematic of the gate drive circuit is provided in Figure 7.6 for reference.

Similar to the case for the power stage design, the capacitor C_{gBS} is placed between the input of the inductor L_{gF} and ground to provide a low ac impedance at the input node. The input power connection is on the bottom side of the board, and the C_{gBS} is placed on that side as well. The argument for a tight layout for the loop $L_{g2F} - C_{g2F} - S_{aux}$ is identical to the argument above for the power stage counterpart loop. The inductors of the gate drive circuit are air-core inductors from Coilcraft, but since they do not process much

7.2 Gate Drive Circuit

Component	Value	Package	Manufacturer	Model Number	Spec.
L_F	33nH	1812	Coilcraft	1812SMS-33NJ	
L_{2F}	12.5 nH	A04	Coilcraft	A04TG	
L_{rect}	22 nH	1812	Coilcraft	1812SMS-22NJ	
C_F C_{board} C_{jo}	15 pF 157.5 pF			$V_j = 1.16V, M = 0.45$	Board Parasitic
C_{2F}	39 pF	ATC100A	ATC	ATC100A390JW	150V
C_{rect}	10 pF	ATC100A	ATC	ATC100A100JW	150V
C_{out}	75 μ F 4 x 10 μ F 2 x 10 μ F 5 x 1 μ F 17 x 2000 pF	1812 1210 0603 0603	Taiyo Yuden Panasonic Taiyo Yuden Murata	UMK432C106MM-T ECJ-4YF1H106Z UMK107C105KA-T GRM1885C1H202JA01D	X5S, 50V Y5V, 50V X5S, 50V C0G, 50V
C_{in}	22 μ F 4 x 2000 pF 2 x 1 μ F 2 x 10 μ F	0603 0603 1210	Mirata Taiyo Yuden Panasonic	GRM1885C1H202JA01D UMK107C105KA-T ECJ-4YF1H106Z	C0G, 50V X5S, 50V Y5V, 50V
S_{main}		TO-270-2	Freescale	MRF6S9060	
D_1		DO-214AB	Fairchild	S310	

Table 7.1: Component values for power stage.

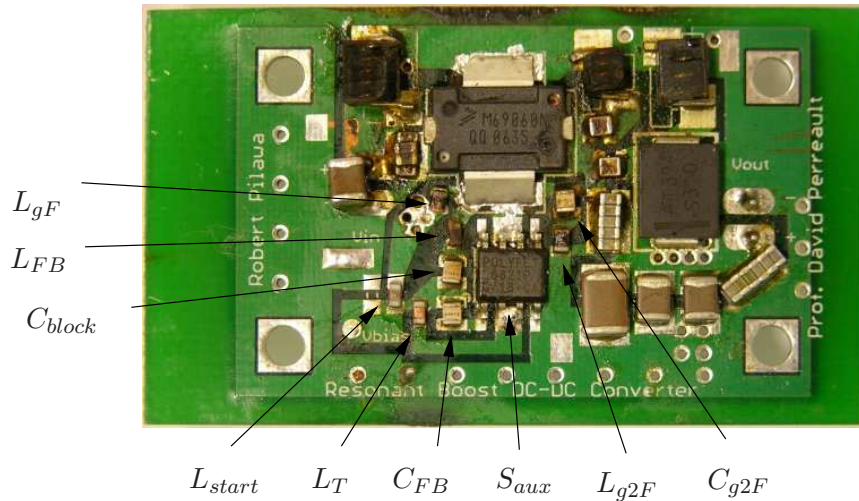


Figure 7.5: Photograph of prototype board with gate components labelled.

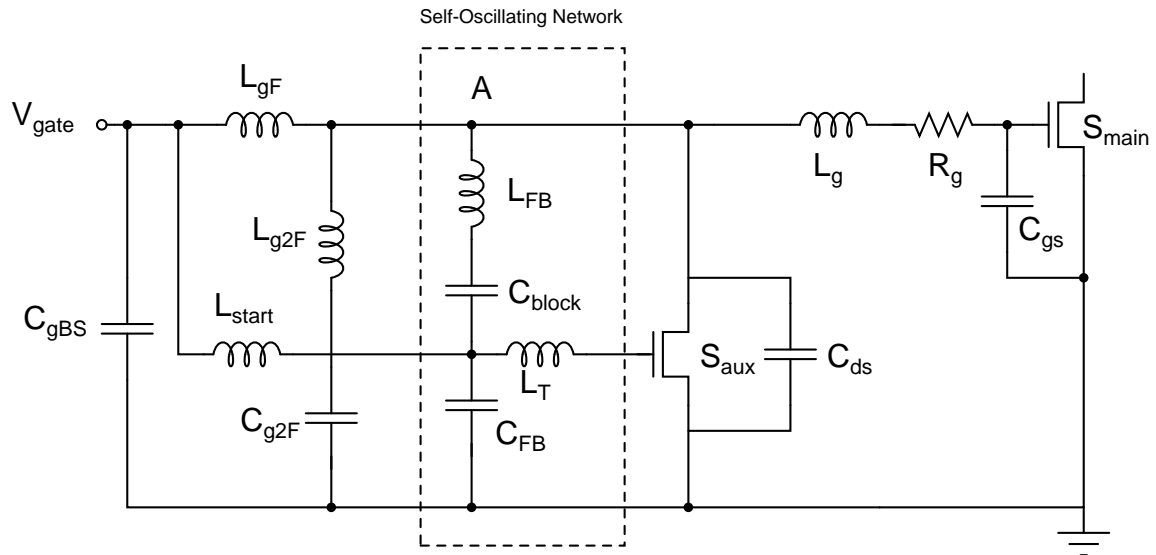


Figure 7.6: Schematic of gate drive circuit.

power, they can be substantially smaller than those of the power stage. Table 7.2 provides a listing of the components used in the gate drive circuit.

Component	Value	Package	Manufacturer	Model Number	Spec.
L_{gF}	4.5 nH	0604	Coilcraft	0604HQ-4N5XJL	
L_{g2F}	2.6 nH	0604	Coilcraft	0604HQ-2N6XJL	
L_{FB}	100 nH	0603	Coilcraft	0603CS-R10XGL	
L_T	68 nH	0603	Coilcraft	0603CS-68NXGL	
L_{start}	13 nH	0603	Coilcraft	0603CS-12NXJL	
C_{g2F}	139 pF				
	100 pF	ATC 100A	ATC	ATC100A101JW	150V
	39 pF	ATC 100A	ATC	ATC100A390JW	150V
C_{block}	100 pF	ATC100A	ATC	ATC100A101JW	150V
C_{FB}	56 pF	ATC 100A	ATC	ATC100A560JW	150V
C_{gBS}	5600 pF	0603	TDK	C1608C0G1E562J	C0G, 25V

Table 7.2: Component values for gate drive circuit implementation.

7.3 Control Circuitry

The control circuitry was placed on the bottom side of the board to help shield it from high-frequency pickup of the power components, as well as to minimize overall converter size. Figure 7.7 shows a photograph of the bottom side of the converter, with the control circuit semiconductor chips identified.

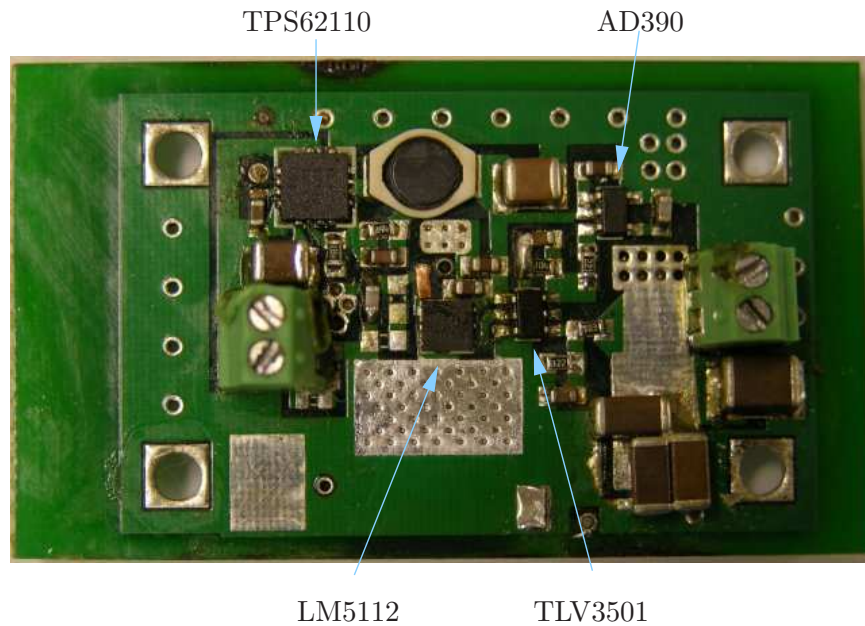


Figure 7.7: Photograph of bottom side of prototype board with the control circuit semiconductors labelled.

Figure 7.8 provides a detailed schematic of the control circuitry. A similar, but less detailed schematic was provided in Chapter 6 (Figure 6.7). The schematic presented here contains all auxiliary components such as bypass capacitors and level-setting resistors.

Component	Value	Package	Manufacturer	Model Number	Spec.
TPS62110		QFN16	Texas Instruments	TPS62110	
C_{BKIN1}	10 μ F	1210	Panasonic	ECJ-4YF1H106Z	Y5V, 50V
C_{BKIN2}	1 μ F	0603	Taiyo Yuden	UMK107C105KA-T	X5S, 50V
C_{BFB}	10 pF	0603	Panasonic	ECJ-1VC1H100D	C0G, 50V
C_{BKOUT}	22 μ F	1210	TDK	C3225X5R1A226M	X5R, 10V
L_{BUCK}	6.8 μ H	LPO1704	Coilcraft	LPO1704-682MLB	
R_{BK1}	390 k Ω	0603	Panasonic	ERJ-3GEYJ394V	1/10 W 5%
R_{BK2}	180 k Ω	0603	Panasonic	ERJ-3GEYJ184V	1/10 W 5%
ADR390		TSOT-23-5	Analog Devices	ADR390	
C_6	1 μ F	0603	Taiyo Yuden	UMK107C105KA-T	X5S, 50V
C_7					
	1 μ F	0603	Taiyo Yuden	UMK107C105KA-T	X5S, 50V
	1000 pF	0603	TDK	C1608C0G1H102J	C0G, 50V
R_1	220 Ω	0603	Panasonic	ERJ-3GEYJ221V	1/10 W 5%
R_3	100 k Ω	0603	Panasonic	ERJ-3GEYJ104V	1/10 W 5%
C_8	3 pF	0603	Panasonic	ECJ-1VC1H030C	C0G, 50V
TLV3501		SOT23-6	Texas Instruments	TLV3501	
C_9	1 μ F	0603	Taiyo Yuden	UMK107C105KA-T	X5S, 50V
C_{10}	15 pF	0603	Panasonic	ECU-V1H150KCV	C0G
R_4	18 k Ω	0603	Panasonic	ERJ-3GEYJ183V	1/10 W 5%
R_5	1.2 k Ω	0603	Panasonic	ERJ-3GEYJ122V	1/10 W 5%
LM5112		LLP-6	National Semiconductor	LM5112	
C_{GDRBP}	1 μ F	0603	Taiyo Yuden	UMK107C105KA-T	X5S, 50V

Table 7.3: *Component values for control circuitry.*

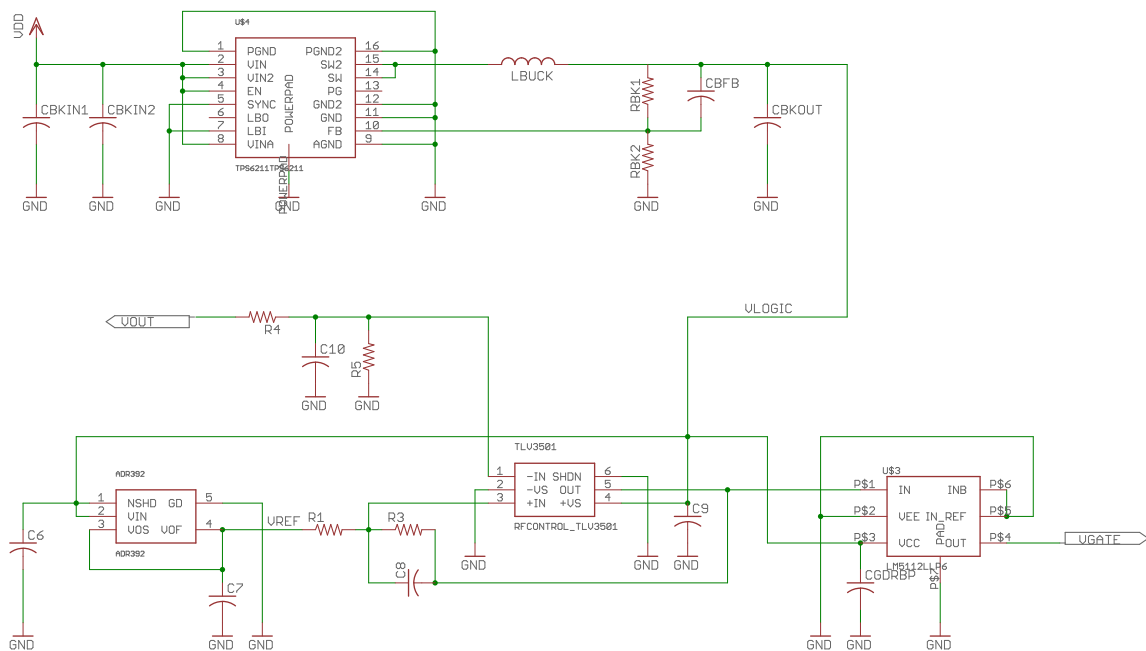


Figure 7.8: Schematic of control circuit with auxiliary components.

Experimental Results

THIS chapter presents experimental results for the converter prototype. The measurement procedure and experimental setup are discussed in Section 8.1, followed by measured converter waveforms in Section 8.2. Measurements of open and closed-loop efficiencies are presented in Sections 8.3 and 8.4, respectively. Closed-loop efficiency measurements are provided for different input voltages and different loads, illustrating the excellent light-load efficiency of the converter. Section 8.5 discusses the parameters governing output voltage ripple of the converter, and Section 8.6 concludes the chapter by illustrating the fast transient response achieved by the converter.

8.1 Measurement Setup

A block diagram of the measurement setup is shown in Figure 8.1. The input voltage is provided by a HP 6632A variable dc power supply. To measure the input current, an Agilent 34401A digital multimeter in current mode is connected between the dc power supply and the input terminal of the converter. Another Agilent 34401A (in voltage mode) is connected across the input terminals of the converter to measure the input voltage. A similar setup of two multimeters are used to measure the output current and output voltage of the converter, as illustrated in Figure 8.1. The output of the converter is connected to an electronic load (Agilent 6060B). The four Agilent 34401A multimeters are controlled by LabVIEWTM from National Instruments, through the GPIB interface of each multimeter. The software control of the instruments enables real-time measurements and display of converter efficiency and power levels (immensely useful for tuning and optimization of the converter). Appendix E shows screenshots of the software interface and a diagram of the LabVIEW code used to control the instruments. The software interface enables the recording of input and output voltages and currents to a data file at the click of a button. This greatly simplifies

the collection of data, in particular for measurements involving sweeps over input and/or output parameters. Accuracy of the measurement setup has been cross-checked against additional multimeters and mirror galvanometers. The computer-controlled measurement setup, although originally developed specifically for the converter of this thesis, is easily adapted for measurements of other power circuits, as is illustrated by its use in [28, 42]. It is the hope that this instrumentation control and data acquisition setup will simplify the experimental measurements of future power converters as well.

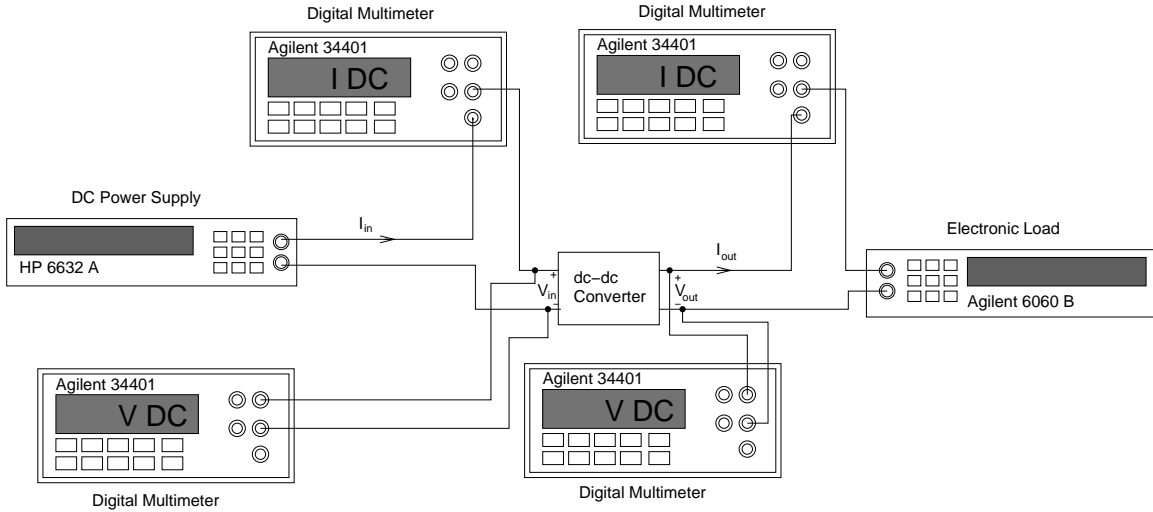


Figure 8.1: *Block diagram of measurement setup.*

In order to get true dc measurements of input and output voltages and currents, care must be taken to ensure that they contain minimum ripple. For this reason, additional capacitance is added between the input terminals of the converter in the form of two $330 \mu F$, 25 V, and one $560 \mu F$, 20 V electrolytic capacitors. This helps maintain a steady voltage at the converter input even when the converter is modulated on and off. A steady input voltage is necessary to obtain accurate measurements from the multimeters.

The converter voltage waveforms were obtained using a Tektronix TDS7254B digital phosphor oscilloscope. For gate and drain waveforms, where minimum probe capacitance was needed, the probes used were Tektronix P6158 $1k\Omega||1.5 pF$ terminated into 50Ω . These probes have a maximum input voltage of 22 V RMS, so they could not be used to measure the output voltage. For this measurement, and for the control signals, Tektronix P6139A $500 MHz$, $10 M\Omega||8.0 pF$ voltage probes were used.

8.2 Converter Waveforms

A key characteristic of the resonant boost topology developed in this thesis is the ability to reduce switch voltage stress by shaping the drain waveform. This section presents measured steady state waveforms for drain and gate voltages, as well as startup and shutdown voltages.

8.2.1 Steady State Waveforms

Converter steady state waveforms are presented in Figure 8.2, which shows measured drain and gate voltages for $V_{in} = 14.4V$ and $V_{out} = 33V$. Good zero voltage switching characteristics are observed, and the peak device voltage stress is acceptable, given the 68 V voltage rating of the transistor. As discussed in Chapter 3, the drain voltage exhibits some peakiness due to excess third harmonic content in the waveform. This inability to provide the desired load impedance is one drawback of the selected rectifier topology and component values.

The gate voltage illustrates the successful implementation of the Φ_2 inverter in a resonant gate drive circuit. The load in this case is the input capacitor of the main switch, which provides better opportunities to tune the inverter to get the desired impedance compared to the rectifier load. Here the voltage contains appropriate ratios of first and third harmonic content, providing a flatter waveform, as illustrated by the figure.

8.2.2 Startup and Shutdown Waveforms

Because of the on/off control method used to regulate the output, it is important that the converter turns on and off quickly. Rapid startup and shutdown improves transient performance, since the converter will be able to quickly respond to a change in load condition, as well as input and output voltage changes. Furthermore, the achievable modulation frequency is determined by the time needed to start up and shut down the converter. If the converter on/off transitions take too long, the modulation frequency will have to be lower to maintain good efficiency. A higher modulation frequency corresponds to lower output capacitance, which is desirable as it will reduce size, weight and cost of the converter, as well as enable faster transient performance.

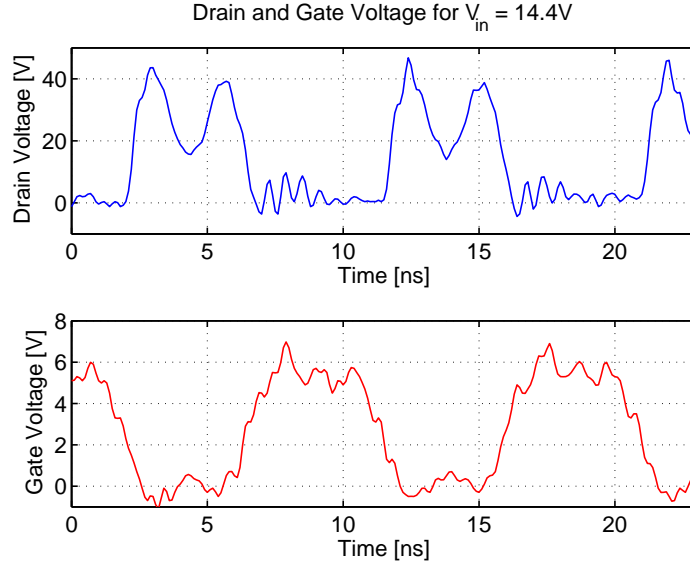


Figure 8.2: Drain and gate voltage for experimental 110 MHz converter operating with $V_{in} = 14.4 V$ and $V_{out} = 33 V$.

Figure 8.3 shows converter waveforms during startup. The initial delay between the low-to-high transition of the command signal and the rise of the gate voltage is due to the propagation delay of the LM5112 driver chip used to provide power to the gate drive. As can be seen from the figure, the converter turns on in approximately 150 ns, and takes approximately another 100 ns to reach steady state.

Another reason for wanting to minimize the time required to turn the converter fully on and fully off is to minimize converter losses, which are higher during transition times than in steady state. If the converter spends less time operating in this regime, overall efficiency will improve. As seen in Figure 8.3(c), yet another reason to limit the time the converter spends in the startup phase is the increased switch voltage stress. The drain-to-source voltage contains isolated spikes that are near the device voltage rating during converter startup.

Figure 8.4 shows the corresponding voltages for the converter at turn-off. As the figure illustrates, converter shutdown is both more rapid and less prone to dangerous drain voltage spikes.

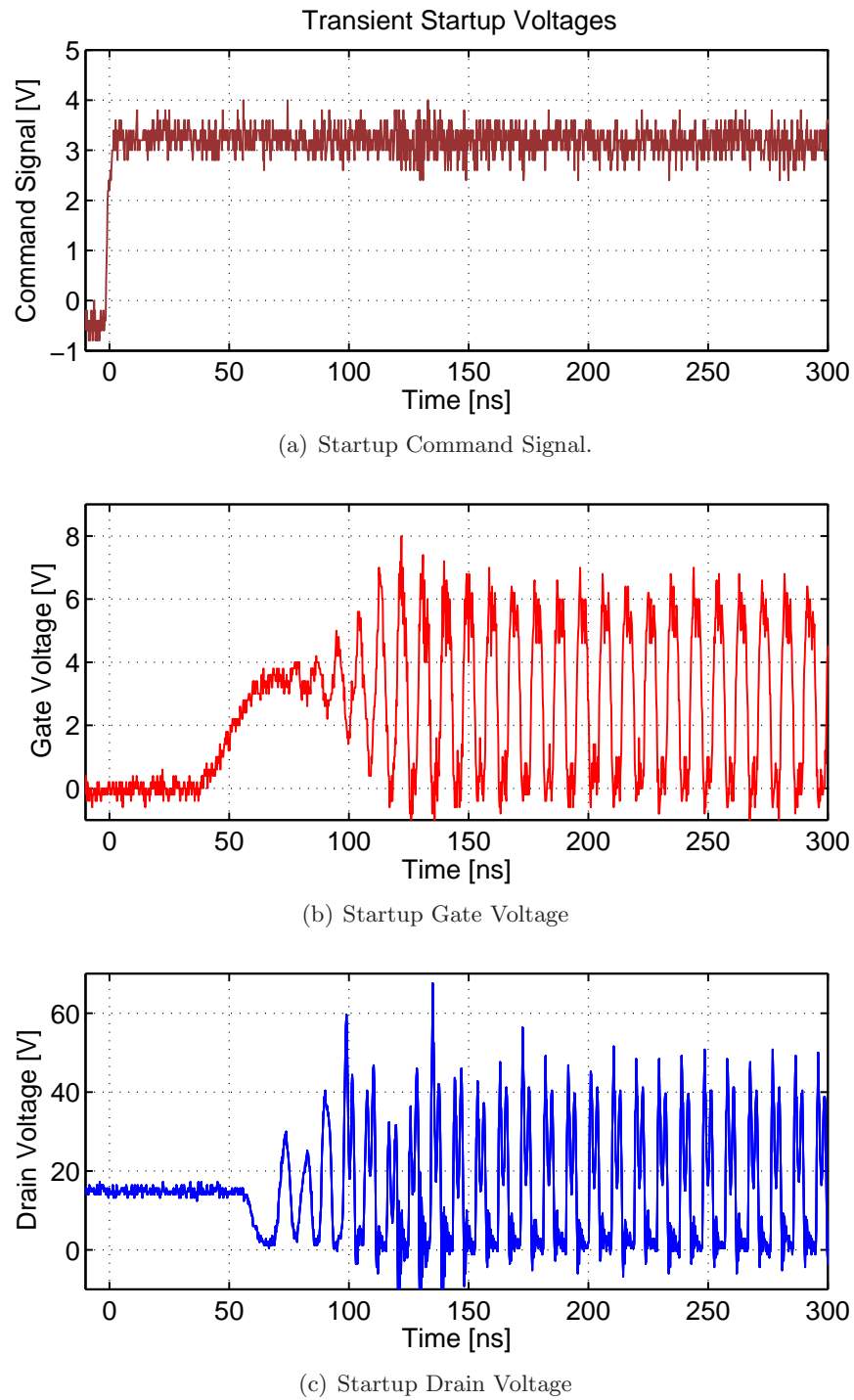
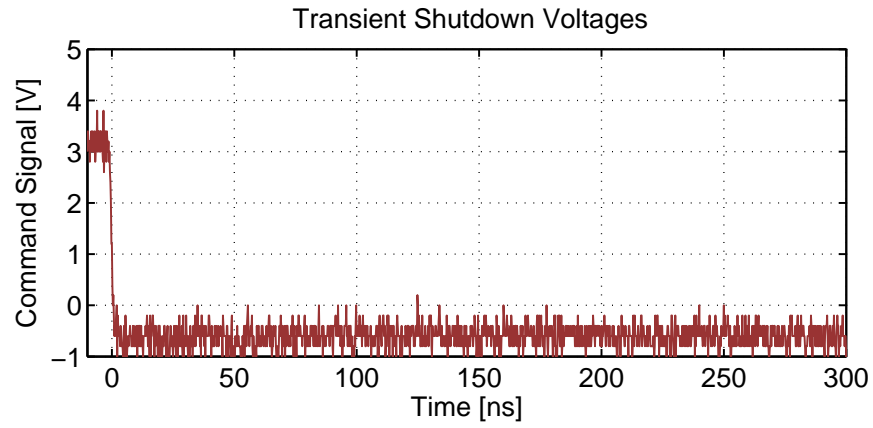
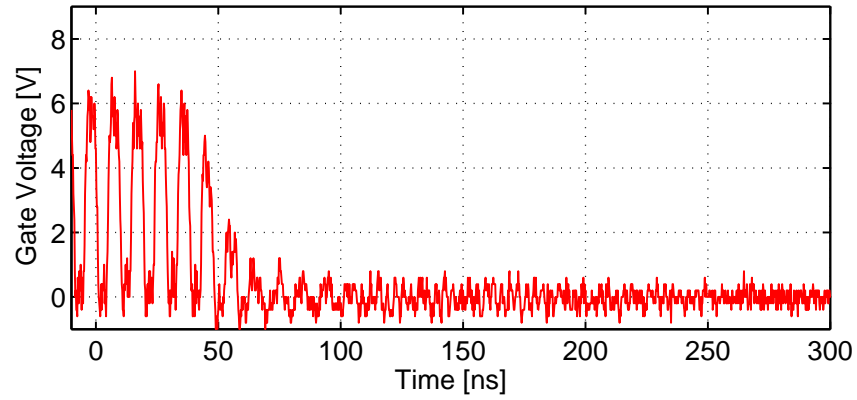


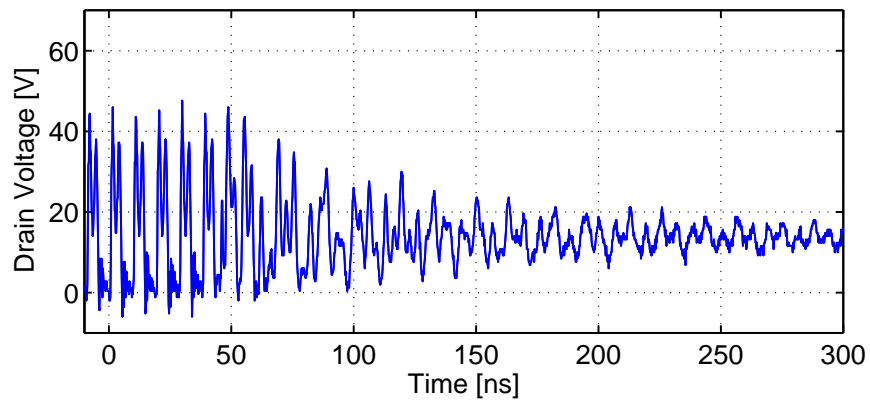
Figure 8.3: Waveforms illustrating converter startup. Operating conditions: $V_{in} = 14.4$ V, $V_{out} = 33$ V.



(a) Shutdown Command Signal.



(b) Shutdown Gate Voltage



(c) Shutdown Drain Voltage

Figure 8.4: Waveforms illustrating converter shutdown. Operating conditions: $V_{in} = 14.4$ V, $V_{out} = 33$ V.

8.3 Open-Loop Converter Efficiency

8.3.1 Continuous Operation

For the open-loop measurements, the converter output was connected to an electronic load (Agilent 6060B), setup as a constant voltage load (32 V). Since this voltage is lower than the regulation voltage (33 V), the control circuit is effectively disabled, keeping the converter on at all times. With this setup, the converter is never modulated on and off, but is constantly processing power (switching at 110 MHz) to the 32 V load. In this mode there are no losses associated with the startup and shutdown of the converter, so it is expected that the open loop efficiency will be higher than that of any closed loop operation. Figure 8.5 shows the converter open loop efficiency and power for input voltages between 8 and 16 V. This, and all following efficiency measurements, include the losses from the gate driver and control circuitry, which are powered from the converter input. It is evident from Figure 8.5 that

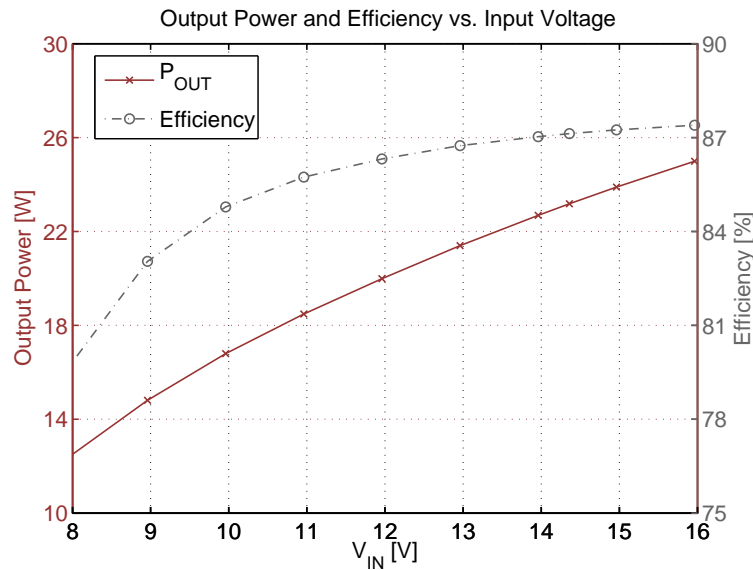


Figure 8.5: Open-loop power and efficiency over the input voltage range, with V_{out} fixed at 32 V.

the converter efficiency is better for higher input voltages (smaller conversion ratio). This is in part due to a larger fraction of the power being delivered at dc at higher input voltages.

8.3.2 Modulation Frequency

As mentioned earlier, there is a fixed power loss associated with turning the converter on and off. This places an upper limit on the practical modulation frequency, which in turns places a lower bound on the required output capacitance. Of interest, then, is a measurement of the converter efficiency as a function of modulation frequency. Figure 8.6 shows converter efficiency versus modulation frequency when the converter is driven with duty cycles of 20, 50, and 80%, for an input voltage of 14.4 V, and a fixed (through the electronic load) output voltage of 33 V.

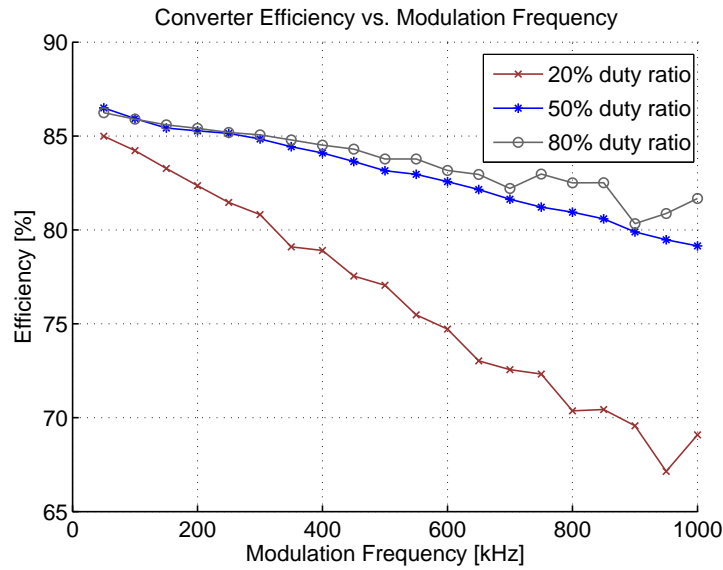


Figure 8.6: Converter open-loop efficiency vs. modulation frequency for 50% duty ratio. The input voltage is 14.4 V and the output voltage is fixed at 33 V by the electronic load.

As Figure 8.6 illustrates, the converter can be modulated at substantially higher frequencies than what is chosen for this work (20-100 kHz, depending on load), without a significant impact on overall efficiency. For designs where minimum output capacitance is desired, this trade-off can greatly reduce the size of the output capacitor at a small efficiency penalty.

8.4 Closed-Loop Converter Efficiency

An important benefit of the on/off control strategy is the high efficiency at light load. Figure 8.7 shows the closed-loop efficiency over the input voltage range parametrized by load. The converter regulates the output at 32.2 V and the load is varied from 5-90% of full load.¹

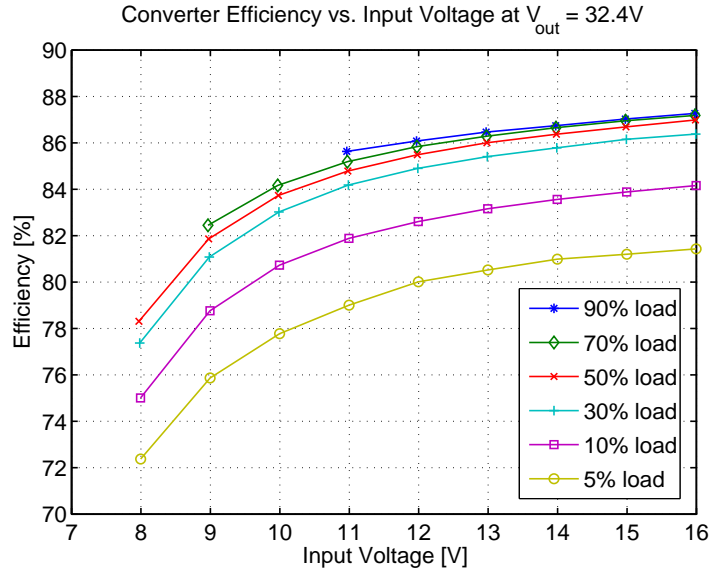


Figure 8.7: Converter efficiency over the input voltage range, parametrized by load. The output voltage is regulated at 32.4 V.

As Figure 8.7 illustrates, the converter exhibits excellent light-load performance, maintaining above 81% efficiency at nominal input voltage (14.4 V) all the way down to 5% load. This substantial improvement in light-load operation compared to typical resonant converters can be attributed to the control strategy used, which turns the converter on only for very small periods of time at light load. When the converter is turned off, it consumes no power, and for the brief time when it is turned on, it operates in a highly efficient state. There is quiescent loss of the control circuitry along with a small fixed power loss associated with turning the converter on and off, which explains why overall efficiency still decreases with lighter load. As the delivered power is reduced (lighter load), the fixed on/off power

¹For this measurement, full load is defined as the maximum power that the converter can deliver at an input voltage of 11 V, while still regulating the output voltage. Using this definition, 90% of full load corresponds to 16.3 W, and 5% to 0.9 W.

loss becomes a larger fraction of the total output power, thereby reducing efficiency.

8.5 Output Voltage Ripple

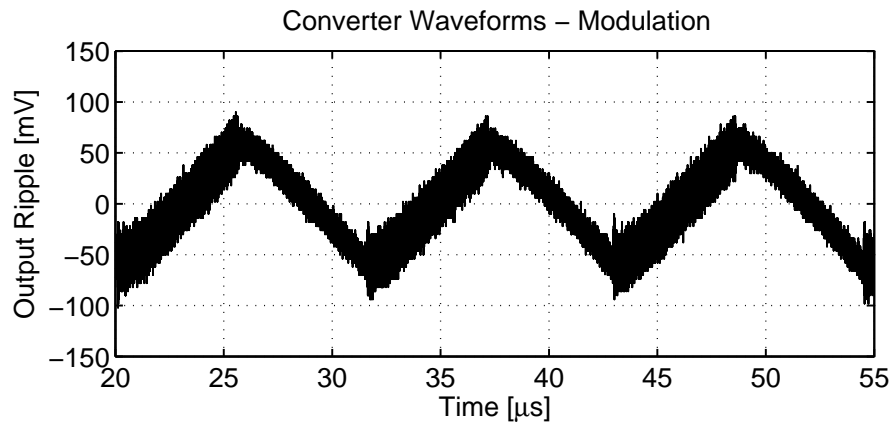
Figure 8.8(a) shows the output voltage ripple when the converter is regulating the output at 32.4 V. The approximately 200 mV ripple is set by the hysteresis band of the controller and is independent of the output capacitance of the converter. The modulation frequency (at which the converter is turned on and off) is set by the load resistance, hysteresis band, and output capacitance, and is approximately 90 kHz in the example of Figure 8.8. If a small output capacitance is desired, this modulation frequency can be set as high as several hundred kHz with a small decline in efficiency. Figures 8.8(b) and 8.8(c) show the command signal and drain-to-source voltage of the main switch, respectively, and illustrate how the converter is turned on and off as the output is regulated. It is important to note that while the on/off modulation frequency in Figure 8.8 is 90 kHz, the converter itself is operating at 110 MHz when it is turned on. In the time scale of Figure 8.8 this switching frequency is under-sampled, but its effect can be seen as the increased "hash" in the rising portion of the output voltage ripple and in the drain voltage when the converter is turned on.

8.6 Transient Performance

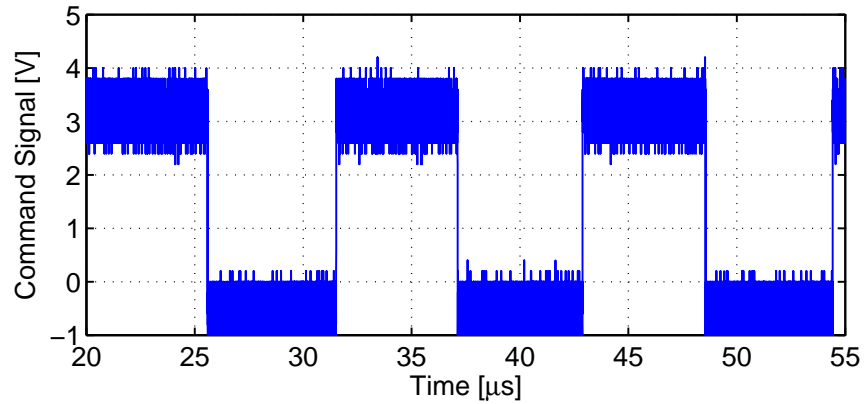
In addition to the size, weight, and cost benefits realized from smaller passive components, an increase in switching frequency also leads to improved transient performance. Because of the small amount of energy stored in the passive components in each switching cycle, the converter can quickly adjust to any changes in load conditions as well as changes in input and output voltages.

8.6.1 Output Voltage Step

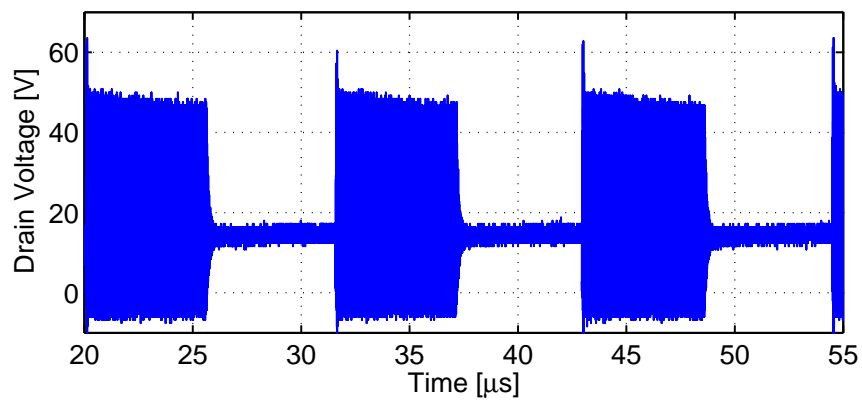
Figure 8.9 shows the converter output voltage for a transition of regulated output voltage from 22 V to 31.8 V. The slew rate (approximately 10 V/ms in Figure 8.9) is dependent on load and output capacitance in the following manner: the transition from low to high



(a) Output Voltage - AC Component



(b) Command Signal



(c) Drain Voltage

Figure 8.8: Steady state converter waveforms, illustrating output voltage ripple (a), converter command signal (b) and the corresponding drain voltage (c). $V_{in} = 14.4$ V, $V_{out} = 32.4$ V, $R_{load} = 100$ Ω .

Experimental Results

(22 V to 31.8 V in this case) will be slower for heavy load than for light load. At light load, a small amount of current is delivered to the load, and much of the rated current of the converter can be used to charge up the output capacitor, resulting in a rapid increase in output voltage. For heavy load, this transition is slower, since much of the current goes into the load, leaving less available to ramp up the output voltage.

For the output voltage transition from high to low, the situation is reversed. A heavy load will quickly bring down the output voltage, since much current will be drawn by the load, thereby reducing the voltage on the output capacitor. At light load, however, the output voltage will decrease much more slowly, since the current drawn by the load is small. If a faster slew rate is desired, an active pull-down could be utilized to improve the high to low transition, or an active pull-up for the low to high transition.

The slew rate is tightly coupled to the size of the output capacitance. Less output capacitance corresponds to a faster transition of the output voltage, as well as a higher modulation frequency. As was illustrated in Figure 8.6, converter efficiency decreases with increasing modulation frequency. Consequently, there is a trade-off between efficiency and fast slew rate.

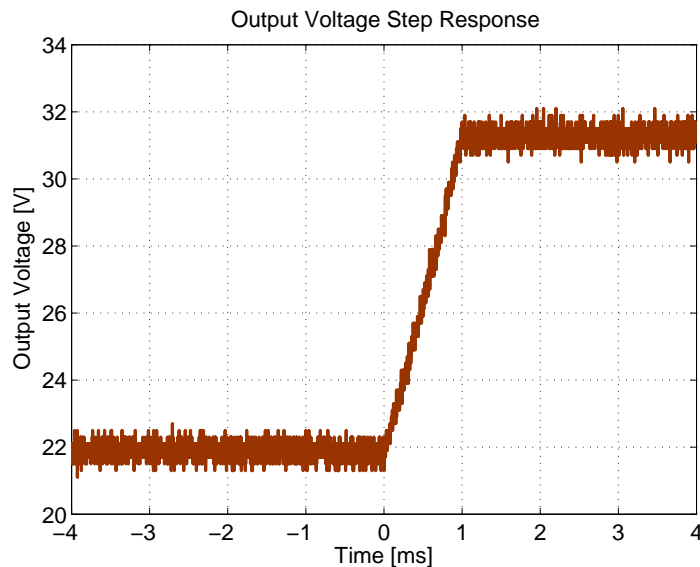


Figure 8.9: Output voltage waveform illustrating converter response to a change in regulated voltage.

To illustrate the speed of response to a reference step a simple experiment was carried out.

The modification to the voltage divider responsible for setting the regulated output voltage is shown in Figure 8.10. It is similar to the circuit used for the load step measurements (Figure 8.11), and uses an IRF540 MOSFET to change the ratio of the voltage divider. The component values are: $R_4 = 18\text{ k}\Omega$, $R_5 = 1.8\text{ k}\Omega$, $R_X = 3.9\text{ k}\Omega$, and $C_{10} = 15\text{ pF}$.

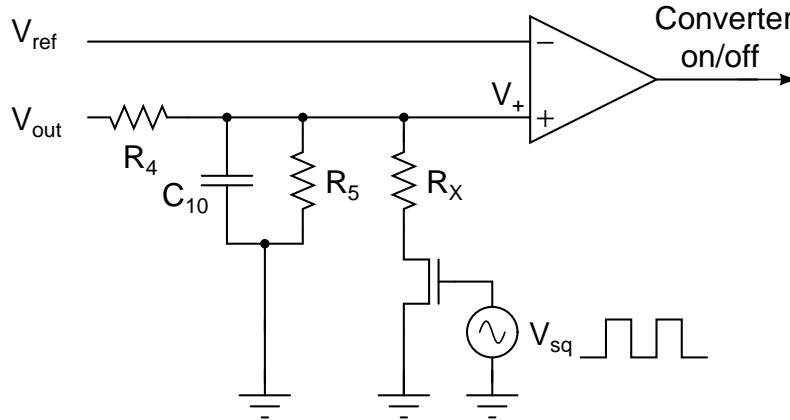


Figure 8.10: Circuit used to step the converter reference, resulting in a change in output voltage from 22 V to 31.8 V.

8.6.2 Load Step

A significant challenge in the design of power converters is to maintain a steady output voltage in the face of rapid load changes. To characterize the converter of this work in that aspect, the output voltage ripple was measured for rapid load changes from 90% to 10% and from 10% to 90% of full load. While the electronic load has the ability to provide a step change in load resistance, it cannot do so rapidly enough for the purposes of this measurement. For this reason, the circuit of Figure 8.11 was implemented. This circuit enables the characterization of the converter response to a rapid change in load conditions. An IRF540 MOSFET is driven by a 1 kHz square wave from a function generator, and alters the load resistance by connecting and disconnecting resistor R_{load1} in parallel with R_{load2} . R_{load2} consists of five 150 Ω , 1/4 Watt resistors connected as shown in Figure 8.11(b) to provide 525 Ω of total resistance while dissipating the necessary power. R_{load1} consists of two paralleled 40 Ω , 10 Watt power resistors connected in series with a third 40 Ω , 10 Watt resistor, to provide a total resistance of 60 Ω and the ability to dissipate the required power.

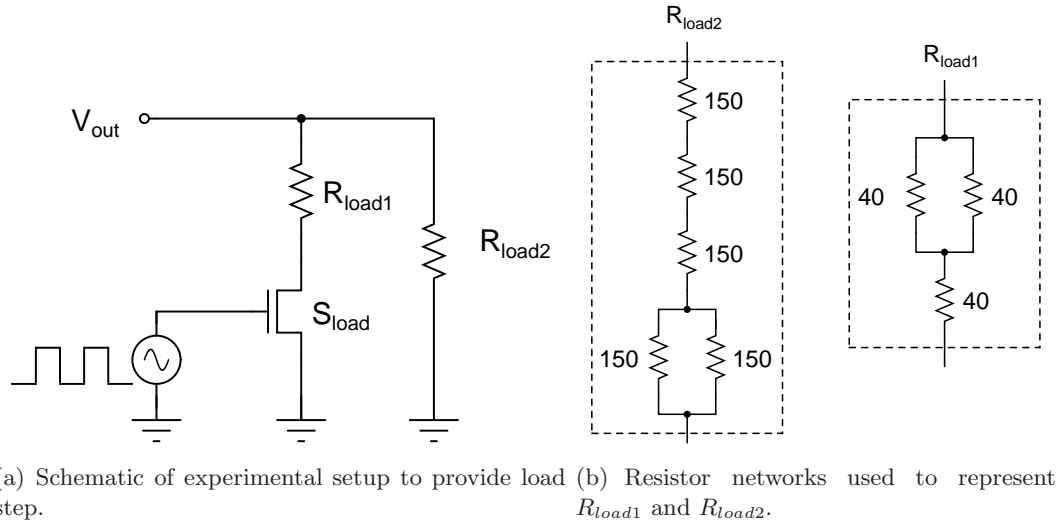
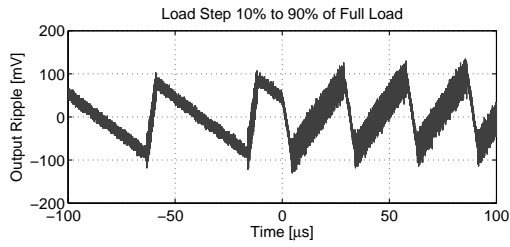


Figure 8.11: Load step circuit for characterizing transient performance of converter.

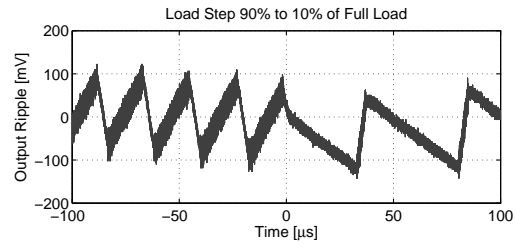
Figure 8.12 shows the measured output voltage ripple and control signal when the load is changed from 10% to 90% of full load, and from 90% to 10% of full load at time $t = 0$. It can be seen from this figure that there is an instantaneous response to the load step transient, without any voltage deviation outside the ripple range. This is in sharp contrast to most conventional converters, which can experience large deviations outside the steady-state ripple range.

This formidable transient response can be attributed to the small inductors and capacitors required for operation at 110 MHz. In addition, transient performance is improved by the resonant topology introduced in Chapter 3, which uses only small-valued resonant passive components.

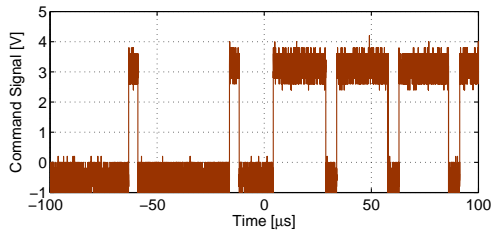
In conventional dc-dc converters, the total required output capacitance is determined by the allowed voltage ripple and the desired transient performance. It is often the latter requirement that determines the minimum capacitance, calling for a larger capacitance than what output ripple requirements alone would require in order to deal with load steps. The VHF resonant boost converter, with its inherently fast transient response, does not have this problem. The output capacitor is sized solely based on the desired on/off modulation frequency and output ripple, not by transient response limitations to changes in load. This,



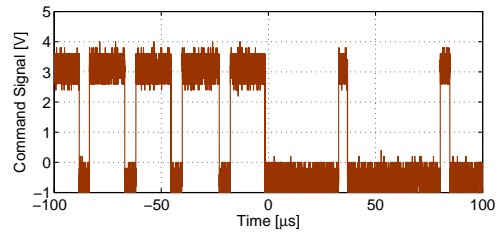
(a) Output Voltage ac Component - 10% to 90% of Full Load



(b) Output Voltage ac Component - 90% to 10% of Full Load



(c) Command Signal - 10% to 90% of Full Load



(d) Command Signal - 90% to 10% of Full Load

Figure 8.12: Converter response to load step. The converter response to a change in load is instantaneous, without any voltage deviation outside of the steady state ripple range.

in turn, frees the designer to deal with ripple through various means (e.g., linear post regulation, active filters, etc.) without constraints of transient performance limits.

Summary and Conclusions

THIS chapter provides a summary of the work of this thesis and its contributions. Areas where future work could lead to further improvements of dc-dc conversion at VHF are then discussed.

9.1 Thesis Summary and Contributions

This thesis developed a resonant boost topology suitable for VHF dc-dc power conversion. The design features a fixed frequency, fixed duty ratio highly efficiency converter cell, which is controlled using on-off control. This approach has the benefits of separating the power processing function from the control, enabling high efficiency at light load, as illustrated in the experimental evaluations of Chapter 8. The high switching frequency of the converter enables the use of small passive energy storage elements. Besides reduced weight, size, and cost, this has the advantage of providing excellent transient performance.

Numerous ancillary dc-dc converter topics are discussed. These include: low-loss resonant gate drive, effective on-off control in a high noise environment, semiconductor selection and modeling, design and layout of VHF power circuits, and details with regards to measurement and evaluation of VHF power converters.

An experimental 110 MHz prototype was built and evaluated. The converter, targeted at the automotive industry, has an input voltage range of 8-16 V, and a selectable output voltage range of 22-34 V. Nominal input and output voltages are 14.4 V and 33 V, respectively. The converter is more than 87% efficient at nominal input and output voltages where it delivers 23 W of power. Furthermore, light-load efficiency is excellent, staying above 80% for loads as low as 5% of full load at nominal input and output voltage.

9.2 Future Work

As this thesis has shown, VHF power conversion offers not only reduced size and weight of passive components, but also improved transient performance. The results achieved in this work further illustrate that high efficiency over a wide load range can be achieved, which is important in many applications. It is therefore expected that further research and development will lead to yet smaller converters operating at higher frequencies than what is done here.

The techniques developed here can find use in power electronics for portable low-voltage applications - where size, weight, and cost are of great importance. An additional challenge is then synchronous rectification at VHF frequencies, which provides better efficiency than diode-based rectifiers for low output voltage designs.

A key driving force in power electronics is the move towards fully integrated solutions. As this work has shown, the sizes of the passive components at VHF operation are small enough to make integration a possibility. The work of [42] further investigates this topic. As seen in the photograph of the power stage (Figure 7.2) of this work, the passive components are so small that it is the discrete packaging of the semiconductor devices that takes up the majority of the converter space. Designs where the passive components are integrated within the semiconductor device package provides a way to further reduce converter size and increase power density.

Another area where improvements can be made is in the semiconductor switches. Various new semiconductor materials (GaAs, SiC, etc.) promise increased performance compared to their Si counterparts. This is still an area of much research, with significantly higher device costs than conventional Si rf MOSFETs. It is expected, however, that the techniques developed here will prove useful for converters utilizing these high performance semiconductors. In addition, further improvements can be made with Si-based converters. As mentioned earlier, rf LDMOS devices exist today with substantially lower on-state resistances than the device used for this work. Issues of packaging and/or gate matching were what prevented their use in this work. Semiconductor devices specifically designed for VHF power conversion are therefore expected to further improve performance of dc-dc converters utilizing the techniques presented here.

Finally, the techniques developed here are by no means exclusive for only VHF operation. In fact, operation at *lower* frequencies may be desirable if high efficiency is the main goal. The methods used to achieve high efficiency at very high frequency in this work can be extended to provide even higher efficiency at lower frequencies. Coupled with high-performance magnetic materials, the low switching- and gating-loss topologies presented here have the possibility to provide increased efficiency in application where miniaturization is of less importance.

Appendix A

SPICE Code

A.1 Φ_2 Converter SPICE Code

```
*****
*** PHI2, written by Robert Pilawa, based on previous work
*** done by Juan Rivas, Anthony Sagneri, Olivia Leitermann
*** CAMBRIDGE,MA 1/25/2007      ***
*****
*****
*** LIST OF LIBRARIES      ***
*****
.lib "LIBS\CLASSE.LIB"
.lib "LIBS\MOSNL.LIB"
.lib "LIBS\DIODENL.LIB"
.LIB "LIBS\nlcap.LIB" ;non-linear capacitor
*****
*** SPECIAL PARAMETERS AND CONSTANTS      ***
*****
.PARAM
+ PI=3.14159

*****
* CIRCUIT PARAMETERS      *
*****

*---DESIGN PARAMETERS
.PARAM:
+FS=110MEG      ;SWITCHING FREQUENCY
+FT=110MEG
+VIN=14.4 ;INPUT VOLTAGE Spec for 25W at 11V in.
+VOUT=33 ;OUTPUT VOLTAGE
+DUTY=.5;.52;DUTY CYCLE
+QC=2k ;Q CAPACITORS
+QLCHOKE= 100 ;midi 22nH
+RDCCHOKE = 3.9m
+ QPAR= 50 ; Q of parasitic switch inductance
+C1=64.5p ; 157.5/(1+14.4/1.163)^.446 + 15
+LCHOKE=33n;{1/(9*C1*PWR((PI*FS),2))}
+CMR=40p;{15*C1/16};
+LMR=13.5n;{1/(CMR*PWR((2*PI*2*FS),2))};
+Cboard=15p
+Cbs = 8800pF
*RECTIFIER PARAMS
+QL = 100
+LREC =22.5n;19.5n;10.5n;8.5n;9.5n
+CREC =15p;50p;50p;100p
+Cblock = 100n
+Ls = 1n;4.62n
```

SPICE Code

```
+Rload = 1.595
+Qi = 140
Cboard N103 0 {Cboard}

*****CIRCUIT DESCRIPTION ***
*****
*---DC source
VIN N101 0 {VIN}
Rbig N101 0 10g
Cbs N101 0 {Cbs}
*---LUMPED MR NETWORK
VDULCHOKE N101 N101x
XLchoke N101x N103 LCHOKE ;MULTIRESONANT ELEMENT
+ PARAMS:
+ L={Lchoke}
+ QL={QLCHOKE}
+ FQ={FS}
+ IC=0
+ RDC={RDCCHOKE}

XLMR N103 N102X LQS ;MULTIRESONANT ELEMENT
+ PARAMS:
+ L={Lmr}
+ QL={Qi}
+ FQ={FS}
+ IC=0

VDULMR N102X N102 0 ;DUMMY TO MEASURE CURRENT LMR
XCMR N102 0 CQS ;MULTIRESONANT ELEMENT
+ PARAMS:
+ C={Cmr}
+ QC={Qc}
+ FQ={FS}
+ IC={Vin}

*****Non-linear MOSFET model*****
VDUSMOSALL N103 N103D 0

.PARAM
+TR={1/(10*FS)}
+PWIDTH={duty/(FS)}-TR-TR}
VGATE GATE 0 PULSE(0.1 8 0 {TR} {TR} {PWIDTH} {1/FS})

XSWITCH GATE N103D N103S MOSFETNLCINDRVAR
+ PARAMS:
+ RDSON = .267
+ RG = 143m
+ CGS = 106p
+ RCOUT = 200m;.1
+ RSHUNT = 12MEG
+ CJO = 157.5p
+ VJ = 1.163
+ M = .446
+ LS = .05n;.19n
+ LG = .15n;.48p
+ LD = .15n
+ R3 = 1.6
+ R4 = .5
+ R5 = 2.14
+ R6 = 4.34
+ R7 = 6.77
```

```

+ R8 = 10.08
+ R9 = 9.52
+ R10 = 15.14
+ QPAR = {QPAR}

VDUSMOS N103S 0 ;DUMMY TO MEASURE CURRENT MOS
Vdul N103 N103X 0
Vdur N103X N103R 0

***** RECTIFIER *****
VDREC N103R RECTIN1 0 ; DUMMY SOURCE FOR MEASURING CURRENT
VLSIN RECTIN1 RECTIN 0
*XLSIN RECTIN1 RECTIN LQS
** PARAMS:
** L={LS}
** QL={QL}
** FQ={FS}
** IC=0

XLREC1 RECTIN VREC1 LQS ; RECTIFIER INDUCTOR
+ PARAMS:
+ L={LREC}
+ QL={QL}
+ FQ={FS}
+ IC=0
VCREC1 VREC1 VREC1X 0
XCREC1 VREC1X 0 CQS ; RECTIFIER CAPACITOR
+ PARAMS:
+ C={CREC}
+ QC={QC}
+ FQ={FS}
+ IC=0

VDIODE VREC1 VREC11 0
XDREC1 VREC11 OUT DIODENL
+ PARAMS:
+ LDS=1n ;SERIES INDUCTANCE
+ VDON=0.55 ;DIODE FORWARD DROP
+ RDS=.3;0.1254 ;SERIES RESISTANCE
+ CJO=267.77p;{diodecjo}
+ VJ=0.36521670770030;0.3241
+ M=0.42044726053532 ;0.4597
+ RC=.24;.8 ;RESIST. IN SERIES WITH NON-LIN CAPACITOR
+ FS={FS}

VLOAD OUT 0 {VOUT}

.INC "MEASUREMENT.CIR"
*IAC1 0 N103X AC 1
*.AC DEC 1000 10MEG 500MEG
*.step param crec list 15p 20p 25p 30p 35p
*.step param lrec list 14.5n 18n 19n 22n 27n
*.step param lchoke list 33n 39n 47n
.TRAN 10p 3.6U 3.5U 10p UIC
.PROBE

```

A.2 Gate Drive SPICE Code

```
**gatedrive_fb.cir
**Calculations of phase and magnitude of transfer function between gate
**and drain of feedback network as well as time domain analysis

*****
*** LIST OF LIBRARIES
*****
.LIB "LIBS/CLASSE.LIB" ;LIBRARY OF CLASSE COMPONENTS
.LIB "LIBS/nlcap.LIB" ;LIBRARY OF NON-LINEAR CAPACITORS

.PARAM
+FS=110MEG ; switching frequency
+ PI=3.1416
+VIN=3.6 ;INPUT VOLTAGE
+ CG=106P ; Cgs of MRF6S9060
+ RG=0.143 ; Rg of MRF6S9060
*+ CSW=48P
+ C3=139P ; Cg2f
+ L1=5.5N ; LgF
+ L3=3.8N ; Lg2f
+ LGLEAD=0.7N; lead inductance of gate
+ VAMP = 6 ; sinusoidal gate drive amplitude
+ VOFF = 0 ; sinusoidal gate drive offset

***CIRCUIT LAYOUT***
VIN N102 0 {VIN}
*Lstart N102 CLTAP 13n
XL1 N102 N103 LQS
+ PARAMS:
+ L={L1}
+ QL=75
+ FQ={FS}
+ IC=0

XC3 N103 N10X CQS
+ PARAMS:
+ C={C3}
+ QC=1k
+ FQ={FS}
+ IC=0

XL3 N10X 0 LQS
+ PARAMS:
+ L={L3}
+ QL=75
+ FQ={FS}
+ IC=0

XCissSwitch N103 0 nlcap
+PARAMS:
+ CJO=60P
+ VJ=1.43
+ M=0.366

SIDEAL N103 0 GATE 0 SIDEAL
.MODEL SIDEAL VSWITCH(ROFF=10MEG RON=0.6 VOFF=2.7 VON=2.8)
```



```

*GATE OF MAIN MOSFET
RGATE N103 N104x {RG}
LGATE N104X N104 {LGLEAD}
CGATE N104 0 {CG} IC=0

*****
* Self oscillating structure*
*****
.PARAM:
+ CGSSMALL=30P ; Cgs of S_aux
+ RGS SMALL=3 ; Rg of S_aux
+ LT=68N
+ LF=82n
+ CF=56.8P
+ RQDAMP=10MEG ;DAMPING RESISOR
+ LBLOCK=100N
+ CBLOCK=100p;1N

VDUFLEG N103 INFED 0 ; dummy source to connect and disconnect feedback

XLF INFED CLTAPx LQS
+ PARAMS:
+ L={LF}
+ QL=80
+ FQ={FS}
+ IC=0

XCBLOCK CLTAPx CLTAP CQS
+ PARAMS:
+ C={CBLOCK}
+ QC=1K
+ FQ={FS}
+ IC=0

RDAMP INFED CLTAP {RQDAMP}

XCF CLTAP 0 CQS
+ PARAMS:
+ C={CF}
+ QC=1k
+ FQ={FS}
+ IC=5

XLBLOCK CLTAP 0 LQS
+ PARAMS:
+ L={LBLOCK}
+ QL=55
+ FQ={FS}
+ IC=0

LT CLTAP INT {LT}
* MOSFET GATE
RGATESM INT gate {RGS SMALL}
CGSSM GATE 0 {CGSSMALL}
*Vsine GATE 0 SIN({VOFF} {Vamp} {FS})

IAC1 0 N103 AC 1
.AC DEC 1000 10MEG 1000MEG

*.TRAN 0.1N 1.2u 1.1u 0.1N UIC
*.PROBE

```


Appendix B

SPICE Semiconductor Models

B.1 SPICE Transistor Model

```
.SUBCKT MOSFETNLCINDRVAR GATE DRAIN SOURCE
+ PARAMS:
+ RDSON=0.04
+ RG=0.3
+ CGS=1750P
+ RCOUT=0.08
+ RSHUNT=12MEG
+ CJO=1450P
+ VJ=0.818366
+ M=0.5049
+ LD=.5n
+ LS=.5n
+ LG=.5n
+ R3 = 1.6
+ R4 = .5
+ R5 = 2.14
+ R6 = 4.34
+ R7 = 6.77
+ R8 = 10.08
+ R9 = 9.52
+ R10 = 15.14
+ QPAR = 50

XLD DRAIN DRAINL LQS
+ PARAMS:
+ L={LD}
+ QL={Qpar}
+ FQ={FS}
+ IC=0

XLSOURCE SOURCE1 SOURCE LQS
+ PARAMS:
+ L={LS}
+ QL={Qpar}
+ FQ={FS}
+ IC=0

R3 DRAINL DRAINL3 {R3}
SW3 DRAINL3 SOURCE1 GMAIN SOURCE1 SWIDEAL3
.MODEL SWIDEAL3 VSWITCH (RON=1m ROFF=10MEG VON=3 VOFF=2.9)
R4 DRAINL DRAINL4 {R4}
SW4 DRAINL4 SOURCE1 GMAIN SOURCE1 SWIDEAL4
.MODEL SWIDEAL4 VSWITCH (RON=1m ROFF=10MEG VON=4 VOFF=3.9)
R5 DRAINL DRAINL5 {R5}
```

SPICE Semiconductor Models

```
SW5    DRAINL5  SOURCE1  GMAIN SOURCE1  SWIDEAL5
.MODEL SWIDEAL5 VSWITCH (RON=1m ROFF=10MEG VON=5 VOFF=4.9)
R6 DRAINL DRAINL6 {R6}
SW6    DRAINL6  SOURCE1  GMAIN SOURCE1  SWIDEAL6
.MODEL SWIDEAL6 VSWITCH (RON=1m ROFF=10MEG VON=6 VOFF=5.9)
R7 DRAINL DRAINL7 {R7}
SW7    DRAINL7  SOURCE1  GMAIN SOURCE1  SWIDEAL7
.MODEL SWIDEAL7 VSWITCH (RON=1m ROFF=10MEG VON=7 VOFF=6.9)
R8 DRAINL DRAINL8 {R8}
SW8    DRAINL8  SOURCE1  GMAIN SOURCE1  SWIDEAL8
.MODEL SWIDEAL8 VSWITCH (RON=1m ROFF=10MEG VON=8 VOFF=7.9)
R9 DRAINL DRAINL9 {R9}
SW9    DRAINL9  SOURCE1  GMAIN SOURCE1  SWIDEAL9
.MODEL SWIDEAL9 VSWITCH (RON=1m ROFF=10MEG VON=9 VOFF=8.9)
R10 DRAINL DRAINL10 {R10}
SW10   DRAINL10 SOURCE1  GMAIN SOURCE1  SWIDEAL10
.MODEL SWIDEAL10 VSWITCH (RON=1m ROFF=10MEG VON=10 VOFF=9.9)

*NONLINEAR CAPACITANCE EVALUATED AS A CONTROLLED CURRENT
*SOURCE
GCNL N101 DRAINL VALUE={IF((V(DRAINL)-V(N101))<0,CJO*V(201)*(1/LDER),V(201)*(1/LDER)
*(CJO/((1+(V(DRAINL)-V(N101))/VJ)**M)))}

RCOUT N101 SOURCE1 {RCOUT}

XLGATE GATE GATE1 LQS
+ PARAMS:
+ L={LG}
+ QL={Qpar}
+ FQ={FS}
+ IC=0

RG GATE1 GMAIN {RG}

CGS GMAIN 0 {CGS}

****SUBCIRCUIT TO EVALUATE THE DERIVATIVE****
*PARAMETERS AND DEFINITION FOR THIS SUBCIRCUIT
.PARAM:
+ LDER=.01U ;INDUCT FOR THE DERIVATIVE SUBCIRCUIT
+ PI=3.1416

*FUNC. FOR R OF THE DERIVATIVE SUBCIRCUIT
*.FUNC RDER(LDER,FS) {30*2*PI*FS*LDER}
.FUNC RDER(LDER,FS) {1000*2*PI*FS*LDER}
GY 0 201 VALUE={V(N101)-V(DRAIN)}
L1 201 0 {LDER}
R1 201 0 {RDER(LDER,FS)}
.ENDS MOSFETNLCINDRVAR
```

B.2 Non-ideal Diode SPICE Model

```
*Diode model that correctly models non-linear capacitance.
*Provides series inductance and diode forward drop modelling.
*Nodes: A: Anode, K: Cathode
*Parameters: Cjo, Vj, and M model non-linear capacitance
*Resr is ESR of capacitance
```

```

*Author: Robert Pilawa, based on previous model by Juan Rivas

*****
.SUBCKT DIODENL A K
+ PARAMS:
+ LDS=3.7668p
+ VDON=0.75
+ CJO=600P
+ VJ=1.7765
+ M=0.5808
+ FS=100MEG
+ Ron=.1
+ Resr=.16

*parasitic package inductance
LDS  A  101  {LDS}  IC=0

*IDEAL DIODE MODEL
DIDEAL 101 102a IDEAL
.MODEL IDEAL D(N=0.001)
Rser 102a 102 {Ron}
*FORWARD VOLTAGE DROP MODEL
VDON 102 K {VDON}

*NONLINEAR CAPACITANCE EVALUATED AS A CONTROLLED CURRENT
*SOURCE

GCNL K 101b VALUE={IF((V(K)-V(101))<0,CJO*V(201)*(1/LDER),V(201)*(1/LDER)
*(CJO/((1+((V(K)-V(101))/VJ)**M)))}
Resr 101b 101 {Resr}

****SUBCIRCUIT TO EVALUATE THE DERIVATIVE****

*PARAMETERS AND DEFINITION FOR THIS SUBCIRCUIT
.PARAM:
+ LDER=1U ;INDUCT FOR THE DERIVATIVE SUBCIRCUIT
+ PI=3.14159265

*FUNC. FOR R OF THE DERIVATIVE SUBCIRCUIT
.FUNC RDER(LDER,FS) {3000*2*PI*FS*LDER}
GY 0 201 VALUE={V(K)-V(101)}
L1 201 0 {LDER}
R1 201 0 {RDER(LDER,FS)}

.ENDS DIODENL
*****

```


Appendix C

PCB Layout

This appendix provides images of the PCB layout for the converter prototype. The PCB layout was made using EAGLE™ Layout Editor from Cadsoft Computer, Inc. Note that all images here are scaled up by a factor of 2 from their physical size.



Figure C.1: Converter PCB layout, top side.

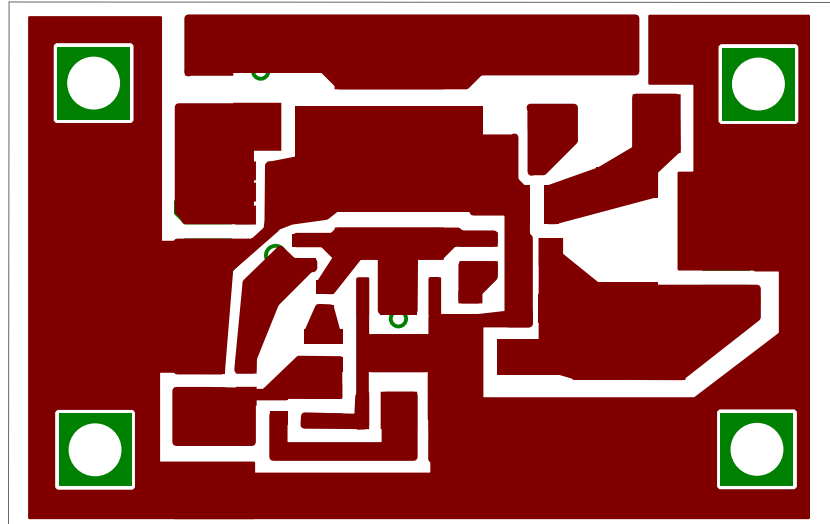


Figure C.2: Converter PCB layout, top copper layer.

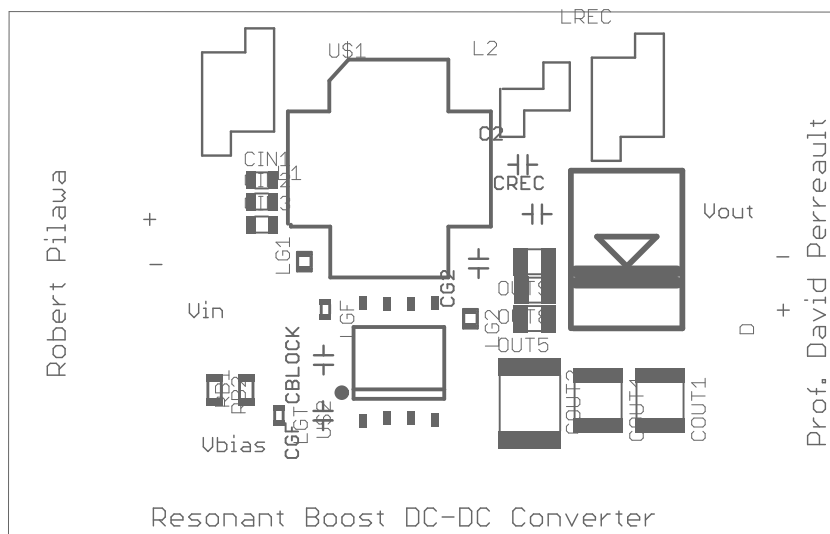


Figure C.3: Converter PCB layout, top silkscreen layer.

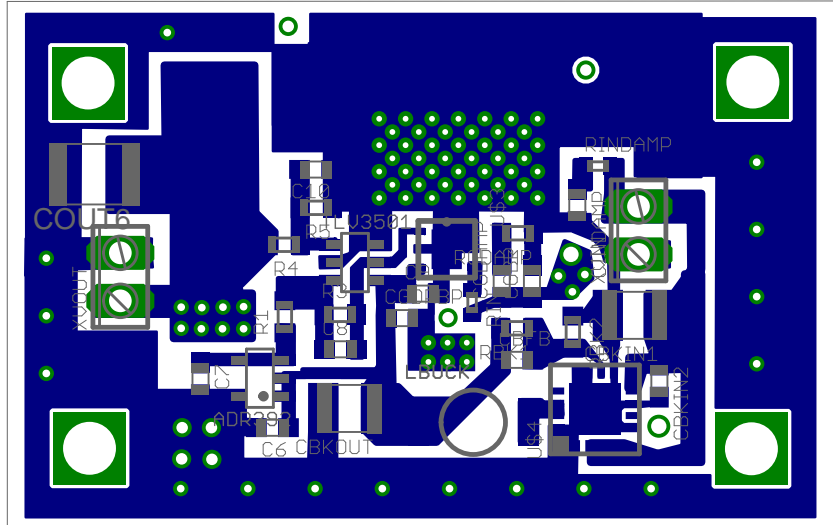


Figure C.4: Converter PCB layout, bottom side (mirrored).

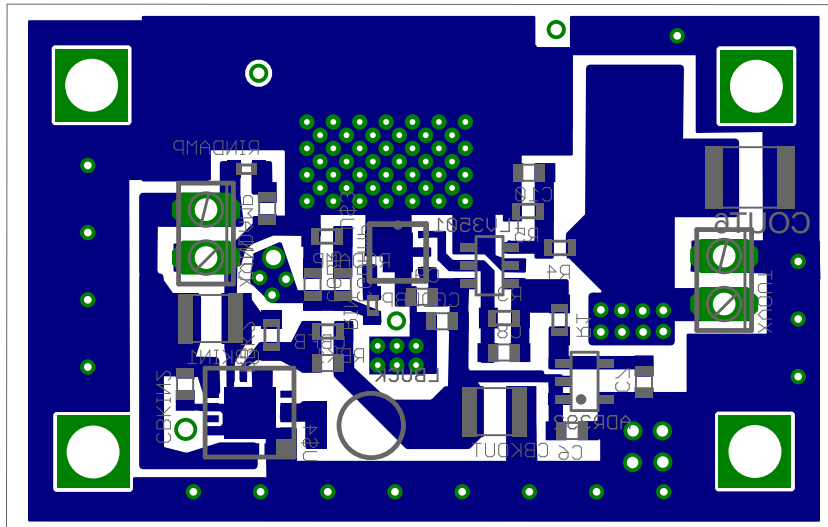


Figure C.5: Converter PCB layout, bottom side.

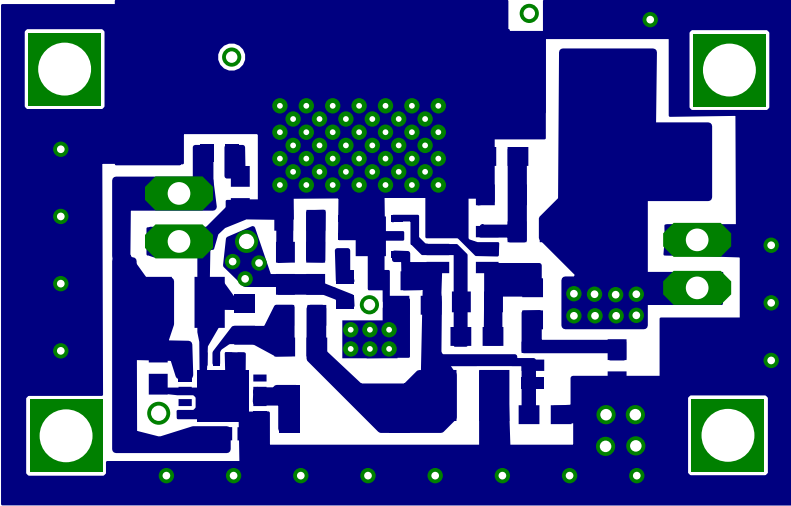


Figure C.6: Converter PCB layout, bottom copper layer.

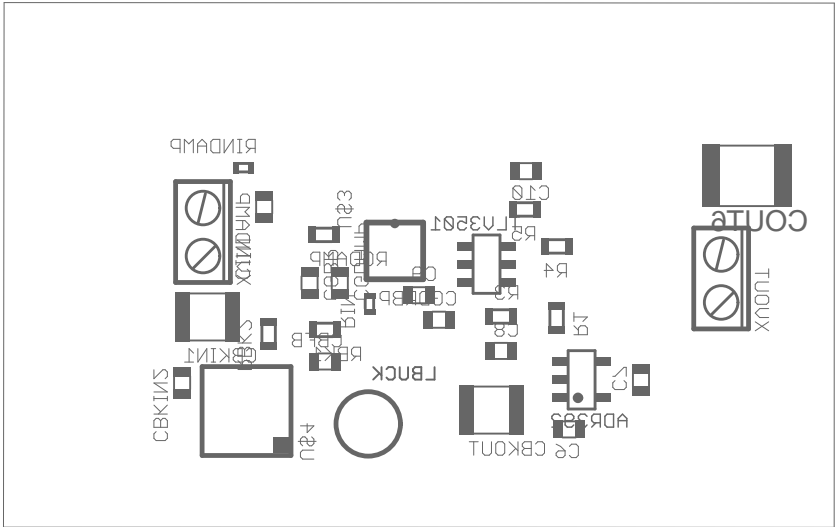


Figure C.7: Converter PCB layout, bottom silkscreen layer.

Derivation of Ideal Ratio of Fundamental and Third Harmonic Voltages for Minimum Synthesized Voltage

A square wave of period T and amplitude 2 has a Fourier series given by:

$$f(t) = 1 + \frac{4}{\pi} \sum_{n=1,3,5\dots}^N \frac{1}{n} \sin \frac{2n\pi t}{T} \quad (\text{D.1})$$

If the first three terms of Equation D.1 are used to approximate a voltage square-wave, the result is:

$$V(\theta) = 1 + V_f \sin \theta + V_{3f} \sin 3\theta \quad (\text{D.2})$$

where $\theta = \frac{2\pi t}{T}$, $V_f = \frac{4}{\pi}$, and $V_{3f} = \frac{4}{3\pi}$. We are concerned here with the ratio of V_{3f} to V_f that produces the lowest maximum value of $V(\theta)$. Note that the ratio developed in [24] is that which produces a maximally *flat* waveform, which - as will be illustrated here - is different from the waveform that has the lowest maximum value.

Figure D.1 shows the synthesized waveform of Equation D.2 for different ratios of V_{3f} to V_f . As illustrated by the figure, the value of θ which gives the maximum value of $V(\theta)$ depends on the ratio of V_{3f} to V_f . For instance, the maximum value of $V(\theta)$ occurs for $\theta < \pi/4$ for $V_{3f} = 3/5V_f$, while it occurs for $\theta > \pi/4$ when $V_{3f} = 1/20V_f$.

To find the relationship between the V_{3f} to V_f ratio and the location of maximum $V(\theta)$, Equation D.2 is re-written in the following form:

Derivation of Ideal Ratio of Fundamental and Third Harmonic Voltages for Minimum Synthesized Voltage

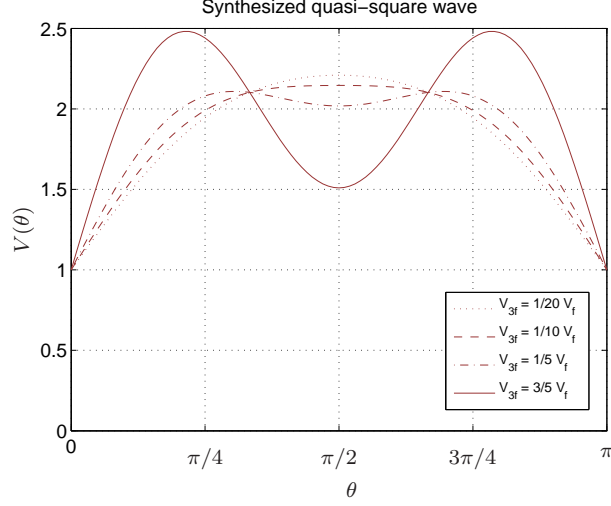


Figure D.1: Plot of Equation D.2 for various ratios of V_{3f} and V_f .

$$V(\theta, A) = \frac{1}{V_f} + \sin \theta + A \sin 3\theta \quad (\text{D.3})$$

where $A = \frac{V_{3f}}{V_f}$, and is now considered a variable. To find the location of the maxima of $V(\theta, A)$ as a function of A , we take the appropriate derivative and set it equal to zero:

$$\left[\frac{\partial V(\theta, A)}{\partial \theta} \right]_A = \cos \theta + 3A \cos 3\theta = 0$$

Using the trigonometric identity $\cos 3\theta = 4 \cos^3 \theta - 3 \cos \theta$, the above equation can be re-written as:

$$\cos \theta + 12A \cos^3 \theta - 9A \cos \theta = 0$$

A trivial solution to this equation is $\theta = \pi/2$, which is easily identified in Figure D.1 as a maxima or minima depending on the ratio of V_{3f} to V_f . A more interesting solution is that which corresponds to:

$$\theta = \cos^{-1} \sqrt{\frac{9A - 1}{12A}}$$

To find the optimum ratio of V_{3f} to V_f (captured in the parameter A), the θ found above is plugged into Equation D.3, resulting in an equation which gives the voltage (at the θ

corresponding to a maxima) as a function of the parameter A only.

$$V(A) = \frac{1}{V_f} + \sin \left[\cos^{-1} \sqrt{\frac{9A-1}{12A}} \right] + A \sin \left[3 \cos^{-1} \sqrt{\frac{9A-1}{12A}} \right] \quad (\text{D.4})$$

To find the A for which this equation is a minimum, we again take the derivative (this time with respect to A) of Equation D.5 and set it equal to zero:

$$\frac{dV(A)}{dA} = \frac{d}{dA} \left(\frac{1}{V_f} + \sin \left[\cos^{-1} \sqrt{\frac{9A-1}{12A}} \right] + A \sin \left[3 \cos^{-1} \sqrt{\frac{9A-1}{12A}} \right] \right) = 0 \quad (\text{D.5})$$

This somewhat complicated equation is most easily solved using your favorite math software, such as MathematicaTM or MapleTM. The answer¹ comes out to be $A = 1/6$, which is consistent with the graphical plot of Figure 3.6 (repeated here for reference as Figure D.2), which compares this ratio to that for maximum flatness (1/9) and that for a fourier series representation of a square wave (1/3). Figure D.3 plots the waveforms for Equation D.2 with ratios of V_{3f}/V_f of (1/6-1/60), 1/6, and (1/6+1/60) to illustrate graphically the minimum switch stress achieved with the ratio 1/6 found in above analysis.

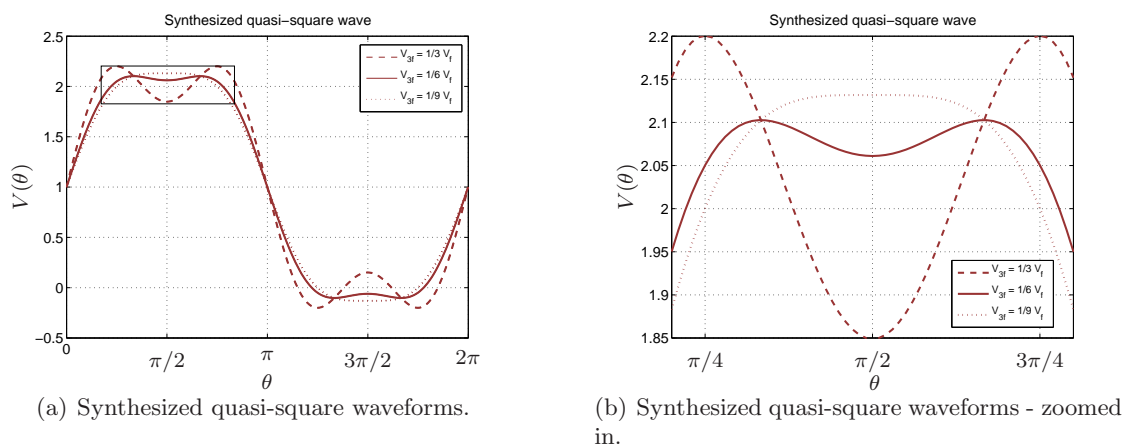
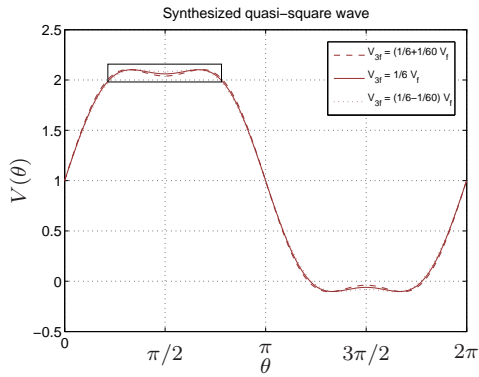


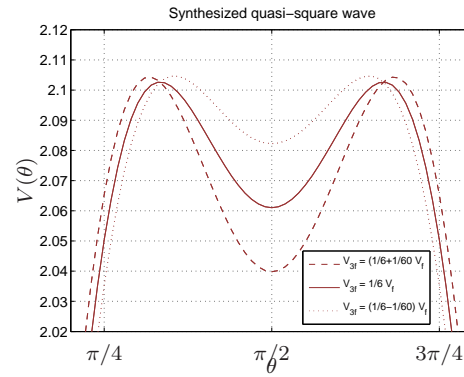
Figure D.2: Illustration of synthesized waveforms for different ratios of V_{3f} and V_f .

¹Using MathematicaTM the answer can be found with the following piece of code:
`Solve[D[Sin[u]+A Sin[3 u], u] == 0, u]`
`Solve[D[Sin[p] + A Sin[3 p], A] == 0, A] /. p->%%[[6]]`

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(a) Synthesized quasi-square waveforms.



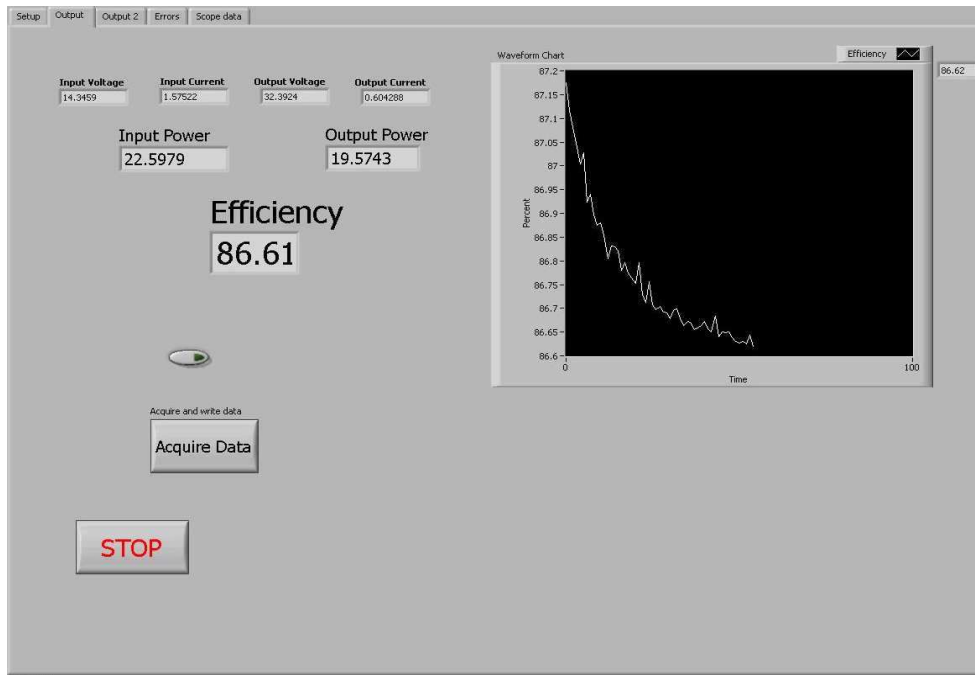
(b) Synthesized quasi-square waveforms - zoomed in.

Figure D.3: Illustration of synthesized waveforms for the value $V_{3f}/V_f = 1/6$ and small deviations above and below this ratio. Minimum voltage is achieved for the ratio $1/6$.

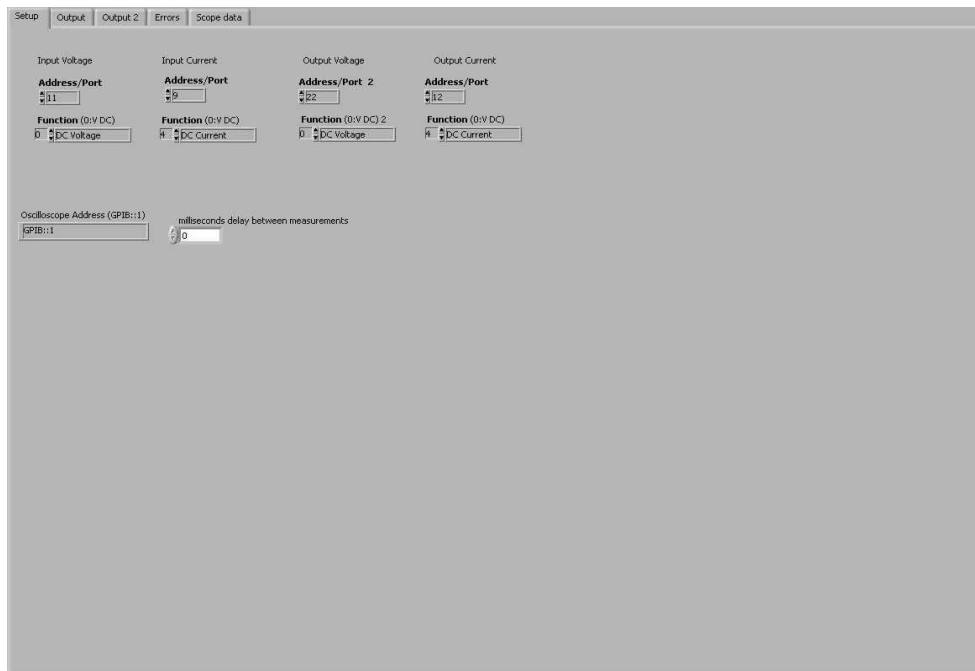
Appendix E

LabVIEWTM Interface

This appendix contains screenshots of the LabVIEWTM software interface used to control the multimeters used for the experimental evaluation of the converter (Figure E.1). Additionally, Figure E.2 shows a diagram of the LabVIEWTM code used to control the instruments.



(a) Realtime Data Display Panel



(b) Instrument Setup Panel

Figure E.1: Software interface for LabVIEW™, which is used to control the multimeters. The software enables realtime collection and display of converter efficiency and power, as well as input and output voltages and currents.

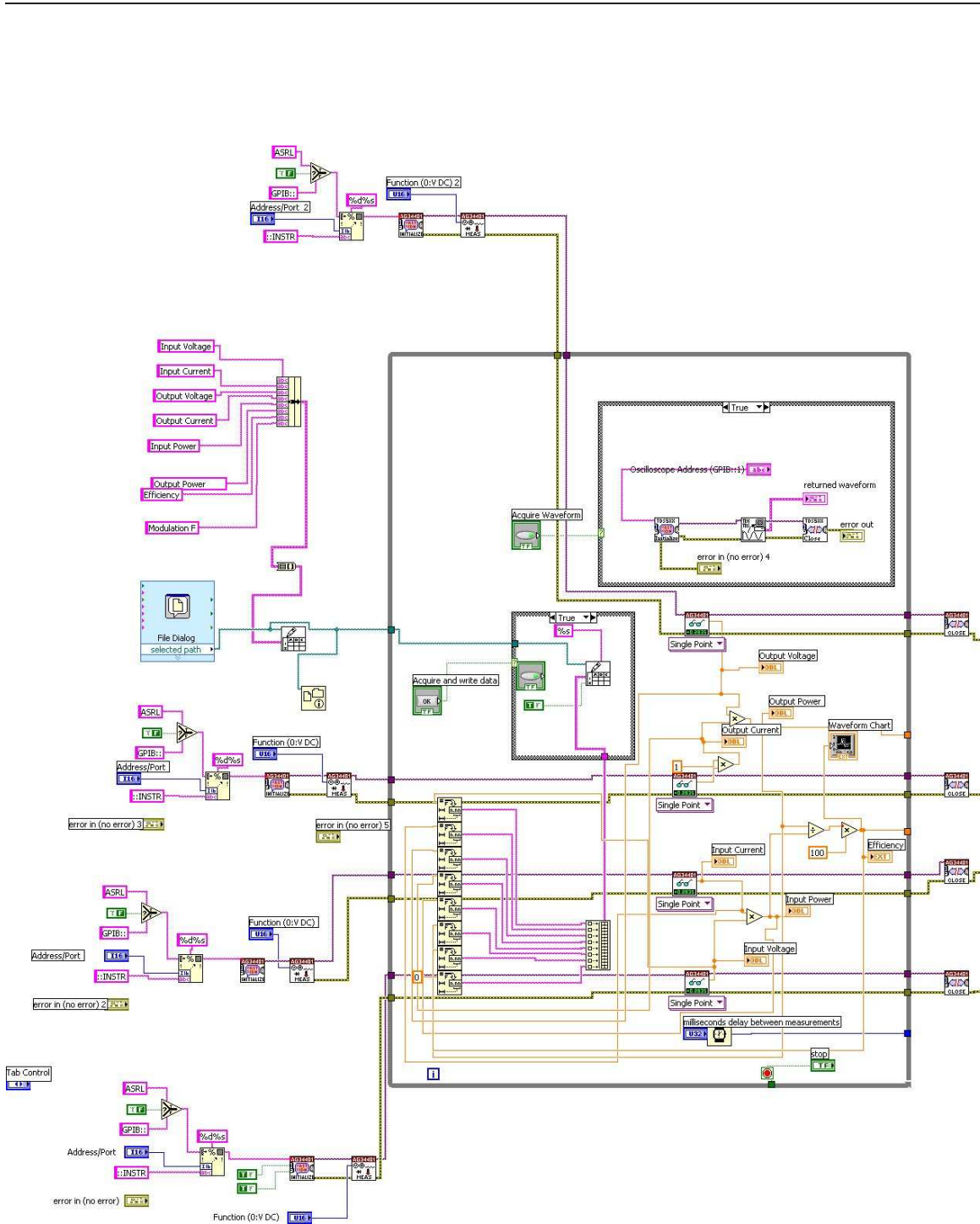


Figure E.2: Diagram of LabVIEW™ software used to control instruments.

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