Characterization of Hot-Carrier Reliability in Analog Sub-circuit Design

by

Huy X. P. Le

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Master of Engineering in Electrical Science and Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

May 1996

Author .....
Department of Electrical Engineering and Computer Science
March 8, 1996

Certified by .....
James E. Chung
Associate Professor
Thesis Supervisor

Accepted by .....
Frederic R. Morgenthaler
Chairman, Departmental Committee on Graduate Students

Characterization of Hot-Carrier Reliability in Analog Sub-circuit Design

by

Huy X. P. Le

Submitted to the Department of Electrical Engineering and Computer Science
on March 8, 1996, in partial fulfillment of the
requirements for the degree of
Master of Engineering in Electrical Science and Engineering

Abstract

The focus of hot-carrier reliability study in recent years has shifted from the modeling of the physical phenomenon at the device level toward understanding the relationship between the AC degradation and its impact on circuit performance. However, most of the effort has been targeted at digital applications, and very limited work has been done on applications requiring analog functions. Increasingly, there is a need to address the issue of hot-carrier reliability in the area of analog circuit design since the traditional lifetime prediction methodology applicable for digital circuits is no longer valid for analog circuits where the devices are not always operated in saturation and key circuit performance parameters depend on the matching properties of the devices, L_{eff}, biasing conditions, and circuit topology.

Through simulation, this thesis systematically looks at the methodology of designing for hot-carrier reliability in analog circuits. By studying hierarchically the degradation of the circuit building blocks most utilized in an operational amplifier, we first examine the existing tools and methodology for hot-carrier degradation evaluation. In a larger context and framework of evaluating the reliability of analog-circuit designs, a set of systematic steps is then proposed to be carried out in modifying, improving , and developing new algorithms and design guidelines. The end goal is to get a better understanding and insight into the trade-offs of the different designs and reliability, and more fundamentally, what it means to have a $10\%\Delta g_M$, or $10\%\Delta V_{OFFSET}$ at the circuit level.

Thesis Supervisor: James E. Chung
Title: Associate Professor

Contents

List of Figures

List of Tables

Chapter 1

Introduction

With a combination of technology scaling, architectural re-design, and creative programming, the speed and density of modern VLSI systems has increased by several orders of magnitude. One of the goals of technology scaling is to try to keep the vertical and lateral electric fields constant in a device while continually reducing the device dimensions. If these two scaling constants are severely mismatched, the device performance will degrade, and consequently fail. Such an example is when the device channel length is scaled down from $1 \sim 2\ \mu m$ into the deep submicron regime (around a one order of magnitude reduction) while the supply voltage is merely scaled down by a factor of $2 \sim 3$. The resulting high-lateral electric field causes the mobile minority-carriers in the inversion layer to accelerate and reach velocity saturation. Such highly energized carriers—also known as *hot carriers*—can cause harmful and catastrophic failures to the device.

1.1 Hot-Carrier Effects & Degradation

If device dimensions are scaled down while the supply voltage remains constant (or is not reduced as rapidly as the device dimensions), the high lateral electric field generated near the drain-end region causes the mobile carriers to reach velocity saturation. This can be seen in Figure 1-1 where the 2-D simulator MINIMOS was used to simulate the lateral electric field along the channel of an NMOS device [1]. This exponential-like dependence of

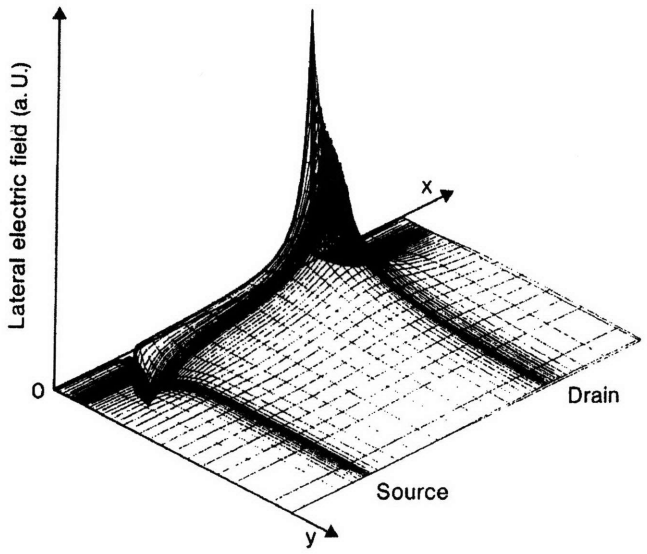

Figure 1-1: MINIMOS simulation of lateral electric field [1].

the electric field in the pinch-off region can be estimated from [3]:

$$E_{max} = \frac{V_{DS} - V_{Dsat}}{0.22\,(t_{ox})^{\frac{1}{3}} / (x_j)^{\frac{1}{2}}} \tag{1.1}$$

where t_{ox} is the gate oxide, and x_j is the source/drain junction depth. Increasing E_{max} with decreasing device dimensions causes the mobile minority-carriers to gain kinetic energy and become hot.

A hot-carrier, while traversing the channel at maximum velocity, can cause impact ionization by colliding with the silicon lattice near the drain end, generating an electron-hole pair. This electron-hole pair creation is only one manifestation of the high lateral electric field near the drain end of the device. As shown in figure 1-2, the peak E_{max} field can also affect devices in the following ways [2]:

- With sufficient energy, the initial electron-hole pair can create another electron-hole pair, and another, and another—leading to avalanche breakdown of the device (process 2 in Figure 1-2).

- In an NMOS transistor, the electrons created by the avalanche process are collected by the drain, and the holes diffuses to the substrate—constituting substrate current (process 3 in Figure 1-2). Due to high substrate resistance ($10 \sim 1000\ \Omega$), the flow of substrate current can also raise the substrate potential and forward-bias parasitic p-n

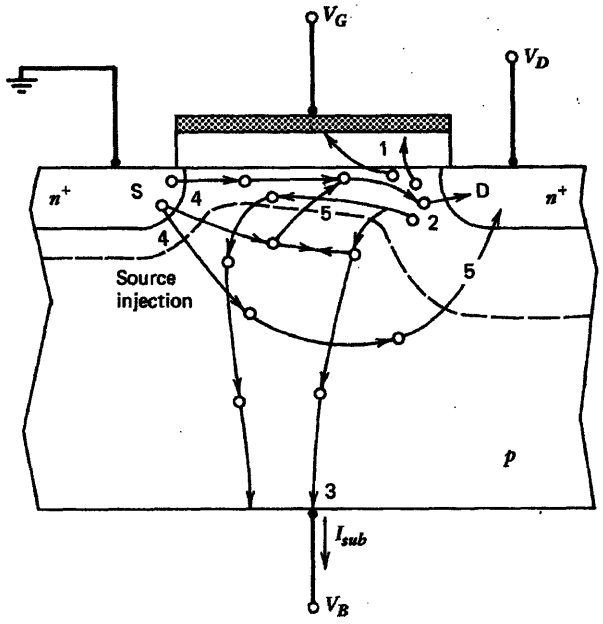

Figure 1-2: Cross section of an NMOSFET showing hot-carrier effects [2].

junctions causing the circuit to latch-up (processes 4 and 5 in Figure 1-2).

- If the electrons from the electron-hole pair creation gain sufficient energy to surmount the $Si - SiO_2$ potential barrier ($\sim 3.1eV$), they can be injected into the gate oxide to create an oxide trap or be trapped by an existing trap, giving rise to a shift in threshold voltage ΔV_T (process 1 in Figure 1-2), as can be seen through [4]:

$$V_T = \Phi_{ms} + 2\Phi_f + \frac{Q_b}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} \tag{1.2}$$

  where Φ_{ms} is the metal-silicon work-function, Φ_f is the Fermi potential, Q_b is the total charge in the inverted channel, Q_{ss} is the total interface/oxide traps in the gate oxide, and C_{ox} is the gate oxide.

- The highly energized mobile carriers can also break a silicon bond at the $Si - SiO_2$ interface to create an interface trap, resulting in decreased carrier mobility ($\Delta\mu$).

Hot-carrier degradation is not a catastrophic problem in the sense that the circuit does not fail suddenly. Rather, the device performance degrades gradually through the slow increase in threshold voltage V_T and/or the decrease in mobility μ. As a consequence, circuit performance degrades because the small signal parameters g_m, g_{ds}, and I_{Dsat} are functions of V_T and μ.

The high value of E_{max} near the drain end arises partly due to the abrupt junction between the drain and the channel, and partly due to the high drain voltage V_{ds}. To reduce this E_{max}, one can reduce the power supply voltage, or alternatively, introduce a graded doping profile junction so that the junction can absorb some of the voltage drop when $V_{ds} \geq V_{dsat}$. Such drain-engineering techniques are often used to fabricate double-diffused drains (DDD) and lightly-doped drains (LDD) devices, making them more resistive to hot-carrier degradation. When this is done, a typical reduction of $30 \sim 40\%$ of lateral E_{max} is observed which consequently reduces the the effects of hot-carrier degradation by orders of magnitude[1].

Although DDD and LDD structures have been shown to improve hot-carrier reliability, they posses drawbacks due to the increase in required process technology, and the resulting reduction in device performance. Because the source and drain have lower doping concentrations for DDD and LDD devices, there is an increase in series resistance R_d and R_s which lowers the effective V_{ds} of the device. This results in a lower current driving capability of the device.

1.2 Degradation Model

Among the different hot-carrier effects described in 1.1, interface-state generation has been found to cause significant long-term degradation in MOSFETs. To quantify the amount of degradation experienced by a device, a physical model was developed based on the lucky electron concept [6]:

$$\Delta N_{it} \propto \left[T \frac{I_d}{W} \exp(-\frac{\phi_{it}}{q\lambda E_m}) \right]^n \tag{1.3}$$

where the exponential term $\exp(-\frac{\phi_{it}}{q\lambda E_m})$ describes the probability an electron having sufficient energy to create an interface state with ϕ_{it} being the critical energy needed to create an interface state, and $q\lambda E_m$ being the kinetic energy gained by an electron while traveling along the channel. n simply describes the dynamics of ΔN_{it} generation (whether interface state generation is diffusion limited or reaction limited). To check for device degradation easily, substrate current has been proposed as a degradation monitor since it has the same

[1]Since hot-carrier degradation is an exponential function of the peak lateral electric field (see section 1.2).

functional dependence on the lateral electric field as interface state generation[2] [6]:

$$I_{sub} = \frac{A_i}{B_i} E_m l_c I_d \exp\left(-\frac{B_i}{E_m}\right) \tag{1.4}$$

In terms of I-V characteristics of the device, interface state generation results in a shift of the threshold voltage ΔV_t, shift in the subthreshold current swing ΔS, and reduction in the transconductance in the linear and/or saturation region Δg_m. Using a simple gradual-channel approximation, a linear relationship was derived between the threshold voltage shift (ΔV_T), relative transconductance reduction (Δg_m), relative mobility degradation ($\Delta \mu$), and the number of interface states generated (ΔN_{it}) [5]:

$$\Delta V_T = \left(\frac{\alpha I_D L}{\mu_0 W C_{ox} V_D} + \frac{q}{C_{ox}}\right) \overline{N}_{it} \tag{1.5}$$

$$\alpha \overline{N}_{it} = \frac{\Delta G_m}{G_{m_0} - \Delta G_m} \tag{1.6}$$

$$\mu = \frac{\mu_0}{1 + \alpha N_{it}} \tag{1.7}$$

As can be seen, Equations 1.3 and 1.4 are both related to one another through the maximum electric field E_{max} in the pinch-off region (Equation 1.1) and provide a link between the electrical characteristics of a degraded device and its physical damage (Equations 1.5, 1.6, and 1.7). Details of this particular derivation and the detailed description of the constants can be found elsewhere [5].

By generalizing the degradation of transconductance, drain current, or threshold voltage as ΔD, we can model the hot-carrier degradation as [6]:

$$\Delta D = (Age)^n \tag{1.8}$$

where

$$Age(t) = \frac{I_{ds}}{HW}\left[\frac{I_{sub}}{I_{ds}}\right]^m t \qquad \text{DC condition} \tag{1.9}$$

$$Age(t) = N\int_0^T \frac{I_{ds}}{HW}\left[\frac{I_{sub}}{I_{ds}}\right]^m dt \qquad \text{AC condition} \tag{1.10}$$

The constant m—sometimes referred to as the voltage acceleration factor—is another way

[2]Since the same mechanism E_{max} gives rise to both processes.

one can write the term $-\frac{\phi_{it}}{q\lambda E_m}$ in Equation 1.3. The larger the m value (typically from $3 \sim 8$), the harder it is for a hot-carrier to generate an interface state. The constant n, also referred to as the degradation rate coefficient, normally ranges from $0.5 \sim 1$ [6]. H is simply a technology-dependent fitting parameters.

The *age* parameter describes how much stress a device experiences and determines the number of interface states (ΔN_{it}) generated over time, for a given I_{ds}, and I_{sub} operating condition. The degradation ΔD is a power-law function of the *age*, and, for a given technology, the graph of ΔD *vs. age* should fall on a universal curve for a wide range of possible channel lengths and device operating conditions.

1.3 The Concept of Accelerated Stressing

Since device parameter degradation can be calculated by the normalized value *Age*, one can get the same age of a device by:

- Operating the device at operational conditions at low V_{DS} and V_{GS}, and hence low I_{DS} and I_{sub}, for a long time.
- Stressing the device at accelerated stress conditions at higher V_{DS}, and hence higher I_{sub}, for a shorter period of time.

Because operating voltages V_{DS}, V_{GS}, and *time* are all related through equations 1.9 and 1.10[3], one can evaluate the hot-carrier reliability of a device by doing accelerated stressing experiments. This is desirable because evaluating hot-carrier reliability at operational conditions would take a very long time. Typically, one would stress the device with a high V_{DS} to near the breakdown region in order to get a noticeable amount of degradation in a shorter time frame. One can then extrapolate back from the accelerated stress condition to the normal operating condition to predict the degradation of the device[4].

1.4 Reliability Simulation Tools

Through accurate modeling of the hot-carrier degradation mechanisms and basic understanding of how a device ages, several hot-carrier reliability simulators have been developed.

[3] A certain bias V_{DS} and V_{GS} will give rise to a fixed I_{DS} and I_{sub}.
[4] See appendix A.

One such example is the BERT tool [7], where all the major degradation mechanisms—oxide integrity, electromigration, and hot-carrier degradation—are modeled. Other hot-carrier circuit reliability simulation tools include HOTRON [8], and RELY [9].

The reliability tools BERT, RELY, and HOTRON are all built around some form of a transistor-level circuit simulator such as SPICE or HSPICE. The circuit simulation programs provide information about the device terminal voltages and currents. The reliability simulation programs then use this information to estimate the dynamic stress condition, and consequently, the aging of each transistor in the given time interval. By doing a table look-up of each transistor's calculated age, a set of aged SPICE device parameters are extrapolated for each device in order to simulate aged circuit behavior. Circuit performance analysis can then be done to predict the impact of hot-carrier degradation on such parameters as switching frequency, low frequency gain, f_T, and phase margin.

1.5 Hot-carrier Degradation & Circuit Reliability

To quantify the gradual nature of hot-carrier degradation in a circuit environment, a simple-minded approach would be to set a threshold limit for all device parameter variation and to declare a *failure* if the variation of that device's parameter exceeded the set threshold limit. This simplistic definition of failure has drawbacks impacting the general circuit performance. For example, if a device is not in a critical path, a larger parameter variation may be tolerable. However, if a transistor is in a critical path, a slight change in parameter value may have a large impact on the circuit performance. Therefore, the correct definition for circuit failure must incorporate both an understanding of device-level degradation mechanisms as well as an understanding of the impact of device degradation on circuit performance.

Work in recent years has shifted focus from trying to understand and model device-level degradation to understanding its impact on circuit performance. While some work focused on the degradation of the frequency in a ring oscillator (or τ_{pd} of an inverter) [10, 11, 12], other studies have focused on the effects of hot-carrier degradation in SRAM and DRAM performance [13, 14, 15]. With greater work and effort being spent in assessing digital-circuit reliability with respect to hot-carrier degradation, it is only worthwhile that some attention be focused on analog circuit-reliability.

Recent VLSI trends show that there is a continuing movement toward integrating digital

and analog circuits onto the same chip. Since the world is analog in nature, this not only aids digital circuits interfacing with the physical world, but also helps in improving their computational performance.

Unfortunately, the existing circuit simulation models for digital ICs are not compatible with analog-circuit simulation because:

- An incorrectly modeled slope in the saturation $I_D - V_G$ characteristics is of no consequence in most digital design. In analog design, however, it can mean an extremely inaccurate prediction of amplifier voltage gain.
- A small variation in the shape of the IV characteristics could make a big difference in the circuit sensitivity analysis.

Since the design and analysis of analog integrated circuits involves more than just a simple DC point evaluation, we need to re-examine and modify (if necessary) existing simulation models so that these models are more robust [16]. Furthermore, the most popular metrics for determining the accuracy of device models, such as RMS error of I_d current, are adequate for evaluating models for digital-circuit design. However, if these same metrics were to apply to analog device models, one would get a very different outcome, because in analog-circuits, the important device model parameters are the small signal g_m and g_{ds}, as opposed to the traditional I_{Dsat} which is important for digital circuits.

1.6 Thesis Overview

This thesis addresses the issue of hot-carrier reliability in analog circuit design based on the assumption that the existing degradation models and reliability simulators are adequate and can predict performance accurately (even for large and complex circuits). Instead of studying reliability for analog circuits in general, this study focuses particularly on the design of a differential amplifier and its subcircuit building blocks. By studying the problem hierarchically and systematically, we can get a better understanding into the trade-offs between the different circuit designs and reliability. We chose to focus on the class of amplifiers because of its frequent use in microprocessor as well as application specific ICs such as DSP chips.

This chapter presents some of the background and key issues involving in the modeling

and simulation of reliability in digital and analog integrated circuits. Chapter 2 shows the design issues involved for the particular subcircuit designs. It also explains how the circuit-simulation and reliability simulation tools are calibrated to a given technology. In Chapter 3, simulation results are presented, and discrepancies between preliminary experimental work and the simulation results will be discussed. Chapter 4 will conclude with some discussion on the ongoing efforts to verify the results from the simulations with real experimental data.

Chapter 2

Experimental Framework

2.1 Tool Calibration Issues

Several degradation models have been proposed to explain hot-carrier degradation and have been implemented in computer simulation programs. These programs can evaluate the effects of hot-carrier degradation on circuit performance quite effectively. However, appropriate procedures to calibrate these tools to a particular process have only been recently addressed as critical for the accurate prediction of lifetime [17]. Without careful calibration, these simulation tools would not be very accurate, thus limiting their overall impact and usefulness. Moreover, a typical reliability degradation simulation often relies on the voltage waveform of only the first few cycles of circuit operation ($\sim 10^{-9}$ seconds) to compute the degradation out to 10 years ($\sim 10^{+8}$ seconds). This computation would result in an extrapolation of more than 10^{+17} cycles of simulation, requiring a high degree of accuracy in the simulation parameters (both for the degraded SPICE model parameters as well as the hot-carrier degradation parameters m, n, and H.

2.1.1 SPICE Model Fitting

Since hot-carrier degradation typically alters device performance by only a few percent during typical stress measurements, SPICE parameter extraction and optimization tools cannot afford to be more than a few percent off in RMS error. If the SPICE parameter extraction tool has more RMS error than the degradation itself, one may even not be able to distinguish between the fresh SPICE parameters and the degraded ones. Therefore, high

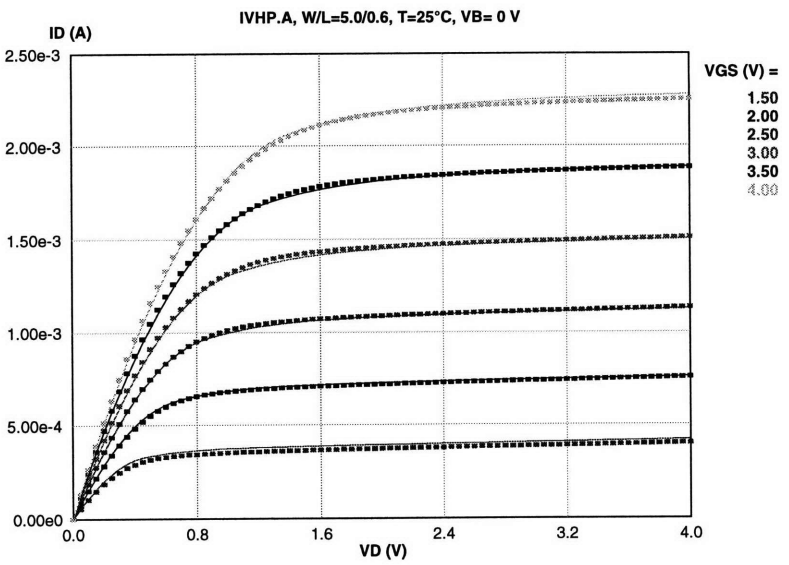

Figure 2-1: ID-VD parameter extraction of a fresh device using BSIM2 model.

performance extraction and optimizing tools must be used. Furthermore, the MOSFET models available for analog design and simulation may have addition problems that are not significant for a digital design. For example, the same specific models in various simulators may behave differently from one another due to differences in their particular implementations [16]. Poor fitting of a SPICE model could also be the result of using too simple of a model, or simply due to poor parameter extraction. For the above reasons, all SPICE simulations in this study use the BSIM2 SPICE model (model 39) to ensure proper behavior of the model in all biasing ranges.

Typical parameter extraction and SPICE fitting results for the BSIM2 model are shown in Figures 2-1 and 2-2. Only a few example of parameter fittings are shown here, and even with one the most advanced MOSFET models (BSIM2), the fit of the drain current and output resistance is still poor at the 'knee' region where the transistor changes from the linear to the saturation region. Recent improvements in the MOSFET model BSIM3 greatly rectify this problem, but the model has yet be implemented in the currently-available design tools.

Notice that the ID-VD curves show a much better fitting than Ro-VD curves. In Figure 2-1, we were able to achieve less than 2% RMS error, but with Figure 2-2, the best we could do was a 40% RMS error. This is an illustration of how models and tools are traditionally optimized for digital-circuit simulation rather than analog-circuit modeling since in digital circuits, one is only concerned with saturation current drive rather than small-signal

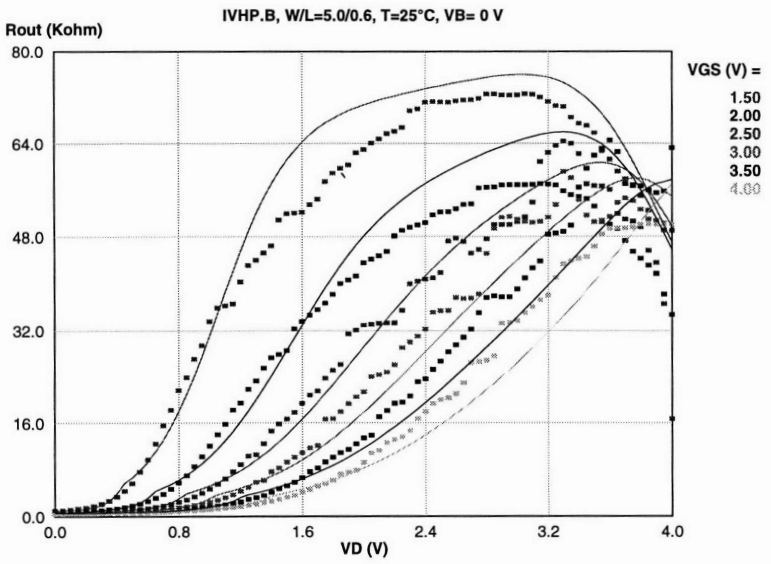

Figure 2-2: R_{out}-VD fitting of an degraded device using BSIM2 model.

parameters such as r_o for analog circuits.

2.1.2 Hot Carrier Degradation Model Parameters

Almost all AC hot-carrier degradation models and reliability simulation tools are based on the general concept of hot-carrier 'AGE' as described in the previous chapter. This abstract quantity, as defined by Equation 1.9, has an inversely-proportional relationship to H and an exponential relationship to m; any small error in extracting these quantities could result in large error in predicting degradation. Furthermore, the stress-bias dependence of the hot-carrier degradation rate n has been shown to cause poor lifetime prediction if not properly taken into account [18].

As mention previously and also noted in Appendix A, reliability simulation often requires large extrapolations based a few initial data points using model fitting parameters that can vary by orders of magnitude (Figure 2-3-b). In this study, to improve model accuracy, a large number of devices were stressed, from which degradation model parameters were extracted, in order to account for any statistical and experimental variations. The hot-carrier degradation parameters m, n, and H for NMOSFETs have been extracted based on a 10 percent linear-current degradation lifetime definition, and modeled as a quadratic function of V_{gd}. The model fitting of these parameters is shown in Figure 2-3, and the

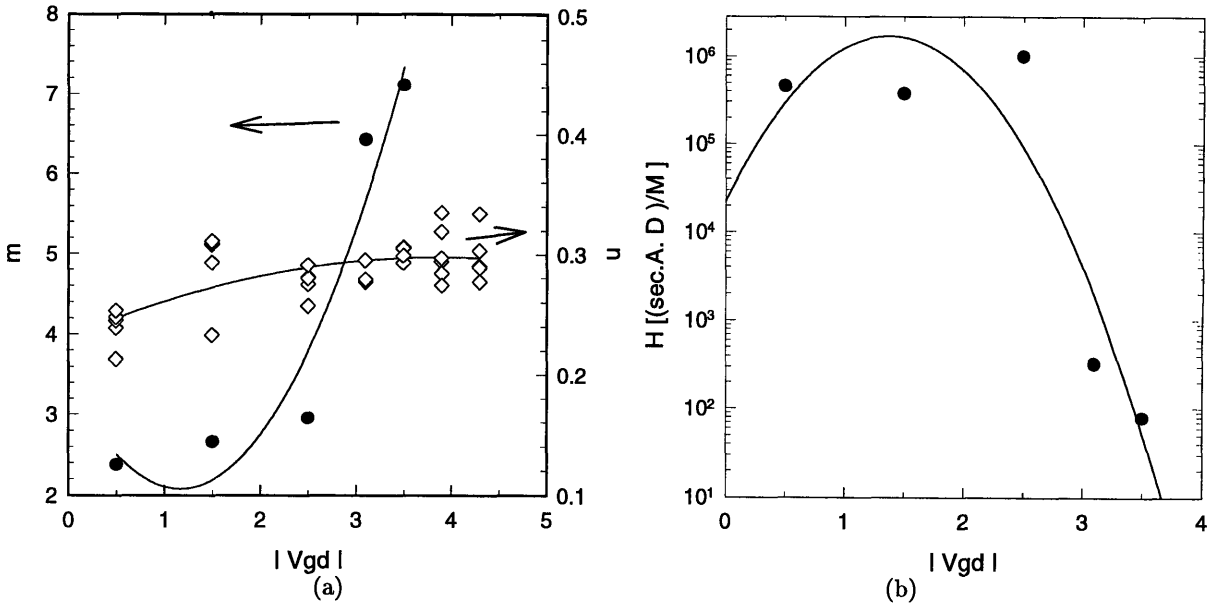

Figure 2-3: Hot-Carrier parameters fitting for use in this thesis.

quadratic function modeling these parameters was found to be:

$$m = \quad 3.376 - 2.233\ V_{gd} + 0.96\ V_{gd}^2 \tag{2.1}$$

$$n = \quad 0.230 - 0.0424\ V_{gd} - 0.0044\ V_{gd}^2 \tag{2.2}$$

$$\log H = \quad 4.346 + 2.743\ V_{gd} - 0.998\ V_{gd}^2 \tag{2.3}$$

2.2 Analog Design Space

The performance of digital circuits may not depend as critically as analog circuits on such circuit parameters as biasing conditions, matching properties of the devices, or on device parameters such as and threshold voltage shift (ΔV_t). As can be seen in the following two equations, whereas the digital circuit parameter τ_{pd} of an inverter is quite insensitive to device variation, the transconductance G_m of a differential pair can vary significantly with device variation [4, 19]:

$$\tau_{pd} \propto \quad \frac{1}{(V_{dd}-V_t)^2} \tag{2.4}$$

$$G_m = g_m \propto \quad (V_{gs} - V_t) \tag{2.5}$$

This can be seen more clearly if one differentiate these two equations for the circuit parameters τ_{pd} and G_m with respect to the device parameter V_t and evaluating them at V_{t_0}:

$$\left.\frac{\delta \tau_{pd}}{\delta V_t}\right|_{V_{t_0}} \propto \frac{2}{(V_{dd} - V_{t_0})^3} \tag{2.6}$$

$$\left.\frac{\delta G_m}{\delta V_t}\right|_{V_{t_0}} \propto -1 \tag{2.7}$$

The denominator of Equation 2.6 will always be greater than one, hence the sensitivity of τ_{pd} (Equation 2.6) with respect to V_t would always be smaller than the sensitivity of G_m (Equation 2.7) with respect to V_t. Furthermore, the sensitivity of an analog circuit parameters depends a lot on perturbations in the SPICE parameters as well as the particular circuit operating environment. Thus, the circuits in this thesis have been designed to span many dimensions to study the different dependencies and sensitivities of circuit performance.

Ranging from basic biasing circuits to basic gain stages, the circuits designed in this thesis serve as the building blocks of more complex analog functions and subsystems. Although implementations may vary from design to design, the circuits presented here show the simplest way one could implement the given function. Beginning with analog subcircuit blocks such as differential pairs, current mirrors, bias voltage generators, gain stages, and output stages, models and understanding will build upon the analysis and experimental data gathered from stressing each of these subcircuit blocks. Instead of the traditional device lifetime plots, we will concentrate on a set of analog hot-carrier design curves based on the simulation of the 'composite' amplifiers using simulation tools such as HSPICE and BERT.

One may question the methodology we take in evaluating the degradation and reliability of the subcircuits since, after all, the device degradation and its interaction among the subcircuits may not be as valid and well behaved as we have assumed it to be. Whether it is valid to 'break up' the circuits in this manner and model degradation as a black box with terminals that can interact across each of the subcircuits remains unclear. However, from our previous experience, one can model the performance behavior of an operational amplifier this way, and since hot-carrier degradation is directly related to circuit performance and behavior, the assumption that degradation can be modeled as a series of connected black boxes is a good one. The validity of this assumption will be verified with experimental data.

These circuits were designed to maximize the V_{DS} on each transistor—and to enhance

	M1	M2	M3	M4	M5	M6	M7	M8
Figure 2-4	100/0.6	100/0.6	33/0.6	33/0.6	50/0.6	50/0.6	—	—
Figure 2-5	100/0.6	100/0.6	33/0.6	33/0.6	50/0.6	50/0.6	25/0.6	25/0.6
Figure 2-6	100/0.6	100/0.6	33/0.6	33/0.6	50/0.6	50/0.6	25/0.6	25/0.6
Figure 2-7	20/0.6	20/0.6	—	—	—	—	—	—
Figure 2-8	10/0.6	40/0.6	40/0.6	40/0.6	40/0.6	40/0.6	—	—
Figure 2-9	50/0.6	50/0.6	50/0.6	—	—	—	—	—
Figure 2-10	25/0.6	25/0.6	25/0.6	25/0.6	—	—	—	—
Figure 2-11	100/0.6	50/0.6	—	—	—	—	—	—
Figure 2-12	50/0.6	50/0.6	—	—	—	—	—	—

Table 2.1: W/L of transistors used in figure 2-4 to 2-12 (in micron).

hot-carrier degradation—especially those devices that are 'stacked' between power and ground rails. Unlike digital circuits where a typical transistor sees a full V_{dd} across the drain and source terminals, a transistor in an analog circuit will only see a fraction of V_{dd} in a typical operating condition. Therefore, all transistors have minimum feature size to accelerate the hot carrier degradation, with the exception of a few channel-length variations of some circuits to verify the channel length dependence of hot-carrier degradation in analog circuits.

The dimensions of the transistors are listed in Table 2.1[1]. A variant of these subcircuits are the sister-class of circuits where PMOS and NMOS devices substitute for one another. The following figures capture most the ideas of this project, and provide a brief explanation for what we would hope to see from each subcircuit block. In each figure, the NMOS flavor is shown in (a), and its corresponding PMOS sister is shown in (b).

2.2.1 Low Frequency Differential Pair

This represent a broad class of circuits whose basic function is to amplify the difference between the two input signals. The bias level and gain of such a stage depend on the symmetry between the two branches of the circuit making it an ideal gain block in most integrated circuits. The differential pair is attractive for its ability to be cascaded without requiring either DC level shifters or coupling capacitors. A typical configuration may have a passive (resistive) load or an active (current mirror) load. The active-load differential pair can provide higher gain because the output impedance of a current source is (theoretically)

[1]Variant of figure 2-4 includes fixing the PMOSFETS and varying NMOSFETS channel length to 0.8 and 1.0 μm, and fixing the NMOSFETS and varying the PMOSFETS channel length to 0.8 and 1.0 μm

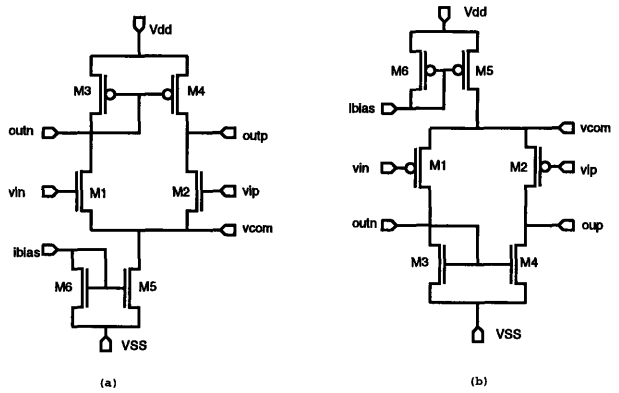

Figure 2-4: Schematic of differential pair with emphasis on accessibility of the internal nodes.

infinite. Normally, a differential pair would have a differential output where the signal voltage is taken between the two output nodes. Shown in Figure 2-4 is the differential to single-ended conversion implementation of the differential pair circuit.

Figure 2-4 shows the schematic of a simple differential pair where each of the individual transistor within the subcircuit can be probed and monitored for degradation, or individually be stressed in order to study how the asymmetrical degradation of the devices affects the matching properties of the differential input pair. Because of the probing pads present at the AC nodes *outp*, *outn*, and *vcom*, the bandwidth performance of this circuit is expectedly poor and simulated to be no more then $10MHz$. If we take the output at node *outp* and the input at node *vin*, the gain of the differential pair can be calculated as:

$$A_v = \frac{v_{outp}}{v_{vin}} = g_{m2} \times g_{ds4} \tag{2.8}$$

where g_{m2} and g_{ds4} can be found by differentiating

$$I_{ds} = \mu\, C_{ox}\, \frac{W}{2\,L}\, (V_{gs} - V_t)^2 \tag{2.9}$$

and evaluating it at the appropriate bias condition. Looking at this circuit by grounding *vip*, the input *vin* to output *outp* can be seen as a common gate amplifier. The DC node voltages of each transistor can be found by evaluating equation for $I_D = \frac{1}{2}\, i_{bias}$.

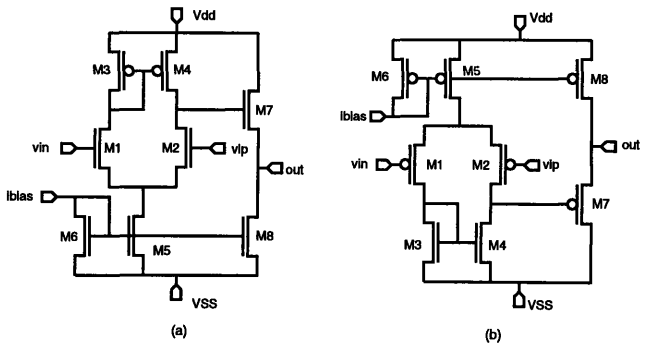

Figure 2-5: Schematic of differential pair with emphasis on high frequency testing.

2.2.2 High Frequency Differential Pair

One limitation of the low-frequency differential pair is the large output load capacitance at node *outp* that prevents the signal from achieving high bandwidth. By incorporating the source follower, we can achieve a higher bandwidth without sacrificing gain as shown in Figure 2-5. With this configuration, we hope to study hot carrier effects at a higher frequency at the cost of losing the capability of internal probing to characterize the individual transistors. Figure 2-5 shows the schematic of a simple differential pair with a source follower simulating the realistic operating condition of a typical amplifier. Because there is minimal loading capacitance in the internal nodes, the frequency response is expected to be superior to that of Figure 2-4. However, we cannnot monitor/stress the individual transistors from within the subcircuits.

From this circuit we can only measure how the frequency response behaves as the subcircuit is stressed over time. By cascading the source follower with the differential pair, we have effectively trade the increase in bandwidth of the circuit for the effective gain, since the gain of a source follower is not quite unity [2].

2.2.3 Mixed Frequency Differential Pair

The low-frequency and high-frequency differential pairs present the two extreme cases of testability in our designs. On the one hand, the design in Figure 2-4 provides for accessibility to the internal nodes of the circuits at the expense of frequency limitation. On the other hand, the design of Figure 2-5 allows the testing frequency to go higher but at the cost of internal-node probing and monitoring. A good compromise between these two designs is

[2]See section 2.2.9

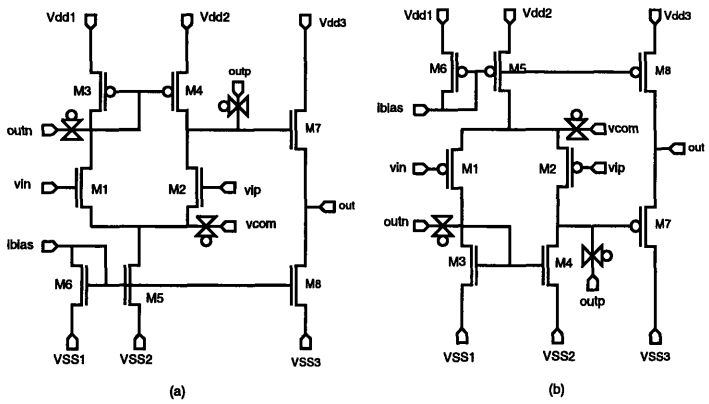

Figure 2-6: Schematic of differential pair compromising between accessibility and high frequency testing.

shown in Figure 2-6 where CMOS pass-gate transistors were added to the high-frequency differential pair. With this design, one still can individually monitor each device in the subcircuit as it degrades, but the complexity of the test setup has increased by one order of magnitude. The presence of parasitic junction-capacitances of the pass-gate transistors is minimal as compared to the large gate-capacitances of each of the transistors, thus not limiting the circuit bandwidth significantly.

2.2.4 Simple Current Mirror

In order for the differential pairs to work properly, appropriate current biasing conditions must be established to keep the input transistor pair *m1* and *m2* in saturation. Another way to look at the basic differential-pair is a pair of source-coupled NMOS transistors in cascode with 2 current sources (one PMOS type, and one NMOS type). The goal of a current mirror is to establish a DC node that is capable of sourcing or sinking current, and with a high small-signal impedance to ground. One simple-minded way to do this is shown in Figure 2-7. Output resistance in this configuration is limited by the channel-length modulation coefficient, and in sub-micron dimensions, this coefficient can be quite large.

The purpose of this subcircuit is to study how the mismatch in current mirrors due to hot-carrier degradation can affect the circuit-level performance. The symmetry of the device and design layout would be reduced when one of the transistor's V_t is shifted due to hot-carrier degradation. We want to explore how degradation tracks the current matching behavior of the circuit. For completeness, we have included the PMOS class of the current mirror, while in practice, the NMOS current mirror alone is sufficient.

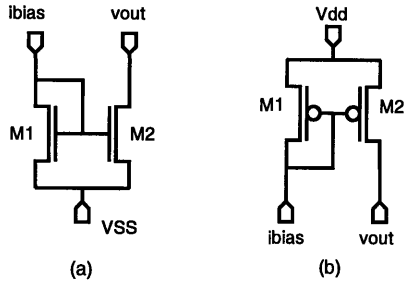

Figure 2-7: Schematic of simple current mirror.

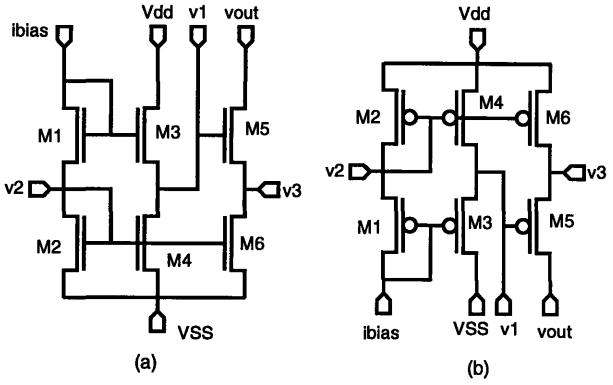

Figure 2-8: Schematic of cascode current mirror.

2.2.5 Cascode Current Mirror

A cascode configuration, such as one shown in Figure 2-8, can achieve a much higher output resistance. Since this is a desirable characteristics in a current source, a cascode current mirror is often used in circuits where the power supply is greater than a few volts. In low power supply design, it is more difficult to use a cascode circuit such as the one shown here since the 'head-room', or swing voltage at the output node, is limited as the transistors are stacked up. In the cascode design, a minimum voltage must be maintained at the output terminal to keep transistors M5 and M6 in saturation. Hot-carrier degradation may cause the node voltages to drift, thus driving some of the transistors out of saturation and into linear region—reducing the effectiveness of the cascode configuration.

2.2.6 Wilson Current Mirror

Another method to improve the output resistance of a current source is to use negative feedback in the manner known as the Wilson current mirror as shown in Figure 2-9. By employing negative feedback through transistor M2, the effective output resistance seen at

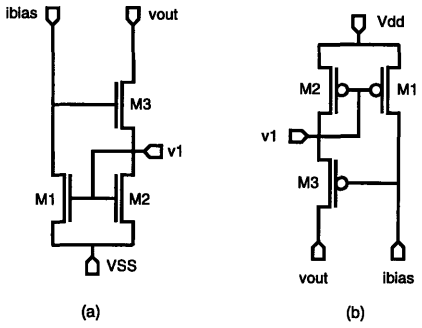

Figure 2-9: Schematic of Wilson current mirror.

vout is found to be [4]:

$$r_{out} \sim (2 + g_{m3}\, r_{o1})\, r_{o3} \tag{2.10}$$

The feedback action works as follow. As I_{out} decreases slightly, node *v1* decreases, and in order to maintain the fixed I_{bias}, the V_{ds} of M1 would have to increase. As a result, the effective V_{gs} of M3 is increased making I_{out} larger. The Wilson current mirror also suffers from similar problems as other current mirrors, and any threshold voltage deviation (due to hot-carrier degradation) will lead to drain-current mismatch.

2.2.7 Bias-Voltage Generator

In a variety of circuit applications, it is necessary to establish a low-impedance point within the circuit which can serve as an internal voltage supply. Ideally such a voltage reference point is required to have both a very low AC impedance, and a very stable DC voltage level which is insensitive to power supply and temperature variations. Such circuits are known as voltage sources or references. A simple way of implementing a bias-voltage reference is to cascode the diode-connected transistors between the power and ground rails as shown in Figure 2-10. The reference voltage generated at nodes *v1*, *v2*, and *v3* can be controlled by varying the device dimensions $\left(\frac{W}{L}\right)_1$, $\left(\frac{W}{L}\right)_2$, and $\left(\frac{W}{L}\right)_3$.

Many circuits have been proposed to generate DC voltages that are independent from power supply voltage or temperature. However complex these circuits may be, hot-carrier degradation would inevitably cause the voltage reference to drift over time.

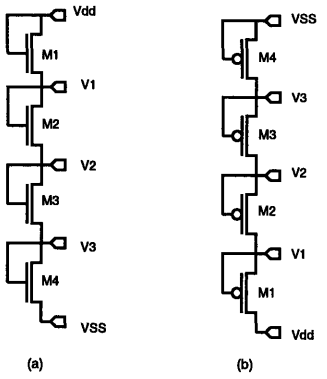

Figure 2-10: Schematic of bias voltage generator.

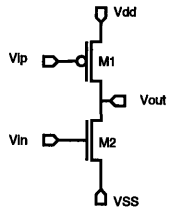

Figure 2-11: Schematic of common source amplifier.

2.2.8 Common-Source Amplifier

The common-source amplifier is commonly used in operational amplifiers for second-stage gain. As an amplifier in itself, hot-carrier degradation of the common source amplifier may not be as interesting as if it was used for second-stage gain. In a Miller-compensated configuration, the common-source amplifier is directly in the feedback path, and, depending on the design, f_T may be a function of g_{m2} where g_{m2} is the second stage gain. Hot-carrier degradation resulting in a reduction in g_{m2} may lead to circuit instabilities when f_T shifts or the phase margin decreases. With this configuration (shown in Figure 2-11), one can achieve very high gain with low biasing current as a single gain stage since it is a common source amplifier with an active (current source) load [3].

2.2.9 Source Follower

Sometimes known as a level shifter, this class of subcircuit insures the DC level of one part of the circuit is compatible with another part of the circuit. Such a circuit is needed, for example, when common-source gain stages are cascaded, and the output DC level of one

[3]It would be a (digital circuit) inverter if *vip* and *vin* are tied together.

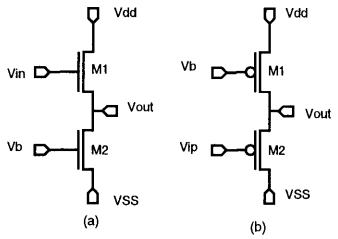

Figure 2-12: Circuit schematics for the source follower.

stage is higher than the input DC level of the next stage. Due to its high input-impedance and low output-impedance nature, this kind of circuit is often used as a unilateral buffer between successive gain stages to prevent loading. It is also sometimes used at the output stage where small output impedance is required. The schematics are shown in Figure 2-12.

When used as an output stage, it is the simplest technique to achieve large output current swing, low output impedance, low signal distortion, and excellent frequency response. The gain of this stage is approximately [19]:

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m1}}{\frac{1}{g_{ds1}+g_{ds2}} + g_{m1} + g_{mb1}} \tag{2.11}$$

where, in the limit of $g_{m1} \gg g_{mb1}$ or $\frac{1}{g_{ds1}+g_{ds2}}$, the gain approaches unity.

Depending where the input signal is applied and where the output signal is taken, Figure 2-12 can also be configured as a common-gate amplifier. For example, if the input signal is applied at *vb*, and the output is taken at *vdd*, with *vin* biased at a DC voltage, the amplifier could be used as a current buffer, or a very high gain voltage amplifier without sacrificing bandwidth due to the missing coupling capacitance from input to output.

2.2.10 Design Verification

Using the data to be gathered from each subcircuit blocks, a 'composite' operational amplifier will be simulated using circuit simulators such as HSPICE and reliability tools such as BERT. By doing so we hope to gain further insight into the relationship between circuit reliability and performance in analog circuit design. Upon the completion of this study, it may be worthwhile to re-assemble these subcircuits into a complete Miller-compensated operational-amplifier and verify the degradation mechanisms and their interaction among the subcircuits by using the two-port model of the amplifier and measuring the Y-parameters.

Using the layout tool MAGIC, the above circuits were laid out using techniques such as common centroid to minimize device mismatch. The circuits were each SPICE extracted into net lists for hot-carrier degradation simulation. Processing parameters such as interconnect and device parasitics were included to simulate the realistic circuit environment.

Chapter 3

Simulation Result & Discussion

As outlined in previous chapters, there are several important issues involved in the simulation of hot-carrier reliability. One important issue is the accurate extraction of the fresh device and degraded device SPICE parameters. It is also important that the SPICE models behave 'normally' in all regions of operation. By *normal* we mean that there is no discontinuity in the plots of the small signal parameters g_{ds} or g_m. Another important issue is the accuracy of the degradation model as well as the device SPICE models implemented in the simulators. In this chapter, we will examine the accuracy of the degradation as well as the SPICE models and point out some of the subtle issues in simulating the hot-carrier degradation of analog circuits.

3.1 NMOS Device Simulation

During the process of SPICE parameter extraction, one would not expect to achieve a perfect fitting to the I-V data after just the first pass (or trial). Typically, one would need to adjust various SPICE parameters until the desired accuracy goal is achieved. Depending on the application for which the SPICE parameters are to be used, one would have to optimize the fitting of SPICE parameters to the data for different parts of the I-V curve. This is often due to inaccuracies or limitations of the device models. For our experiments, we extracted the SPICE parameters for the BSIM2 model with an emphasis on the fitting of analog small-signal parameters r_{out} and the optimization of the I-V curve locally in the low V_{gs} region.

Though this technique seems to work well for one particular set of I-V curves and a

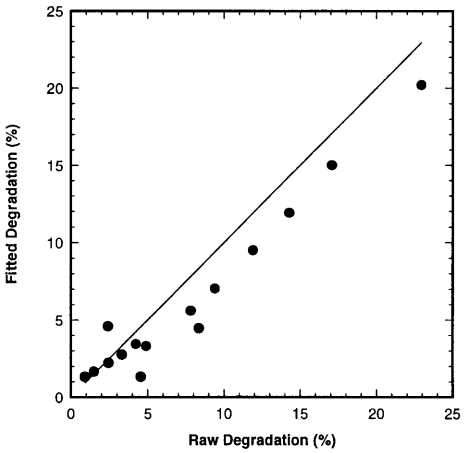

Figure 3-1: Simulated degradation vs. raw degradation for a single NMOSFET.

corresponding SPICE parameter file, it is much more difficult to get a consistent set of SPICE parameter files for a set of I-V curves which degrades over time. To illustrate this problem, we look at a set of degraded I_{ds} vs V_{ds} curves labeled IV_0, IV_1, IV_2, ... IV_i with the corresponding SPICE parameter files $model_0$, $model_1$, $model_2$, ... $model_i$. The subscript *0, 1, 2, ... i* describes the order in time when the I-V characteristics were taken at various stress time intervals. Although each I-V and SPICE model file correlate well with each another at any particular stress time, if we superimpose all the SPICE model files together, we find that the SPICE models at time $(i+1)^{th}$ will *not* necessarily be consistent with the SPICE model at time i^{th} even though their corresponding raw data I-V files are consistent[1].

As shown in figure 3-1, the degradation of a single NMOSFET is simulated under DC stress conditions and compared with the real experimental degradation of the device under the same stressing condition. The labels on the axis corresponds the subscript *0, 1, 2, ... i* above, and the interpretation of the plot is as follow:

- For smaller degradation values of the transistor, we get a near perfect correlation between the simulated degradation and the raw degradation. These correspond to the dots that are on or very close to the solid line.

- For other small degradation values (at a later time interval $i+1 > i$), we may over-predict the degradation of the device as compared to the real degradation. This corresponds to the dots that are above the solid line.

- For degradation values above a certain threshold ($\sim$ 3%), we consistently under-

[1]By *consistent*, we mean that the $(i+1)^{th}$ drain current is smaller than the i^{th} drain current as expected since at the $(i+1)^{th}$ time, the device should have more degradation than at time i^{th}.

estimate the degradation as compare to the real degradation (corresponding to the dots below the solid line).

- If we trace the simulated degradation of the device as a function of (stress) time, we will notice that errors in the SPICE model and parameter extraction procedure cause the current drive of the device to increase at some future time, and then decrease monotonically for subsequent stress time. While these kind of effects have been often observed in ring-oscillator degradation, it has rarely ever seen in device degradation. The simulated degradation exhibits this behavior because there is a lack of *global optimization* with respect to time in the optimization algorithm of the SPICE parameters even though each SPICE parameter file is *locally* optimized.

The circuit performance degradation can be accurately predicted only if the SPICE and degradation models along with the parameter extraction techniques are of sufficient accuracy.

3.2 PMOS Device Simulation

Not withstanding the issues pointed out previously, NMOSFET device and degradation models are relatively quite robust and have been developed over the years to model a wide range of circuit environments, and be able to scale across most technologies. The NMOSFET degradation mechanisms have also been thoroughly examined and demonstrated to correlate well with substrate current. For PMOSFETs, however, the degradation mechanisms and its effects on performance have not been so thoroughly investigated to the same extent as NMOSFETs'. It has been shown that PMOSFET degradation in conventional devices can be modeled as a combined function of both gate current as well as substrate current [20]. As the channel length of the devices approaches submicron dimensions and device technology becomes more advanced, however, the degradation models developed for PMOSFETs in the early days for long channel-conventional devices may not be as applicable.

According to the traditional understanding of the PMOSFET degradation mechanisms and their effects on the I-V characteristics, one would expect that when the PMOS device degrades, the V_t increases in the direction such that its magnitude is decreased. As a result,the drain current is increased in *both* the linear and saturation regime. With such degradation behavior, one would expect the I-V of a fresh and degraded PMOSFET to be

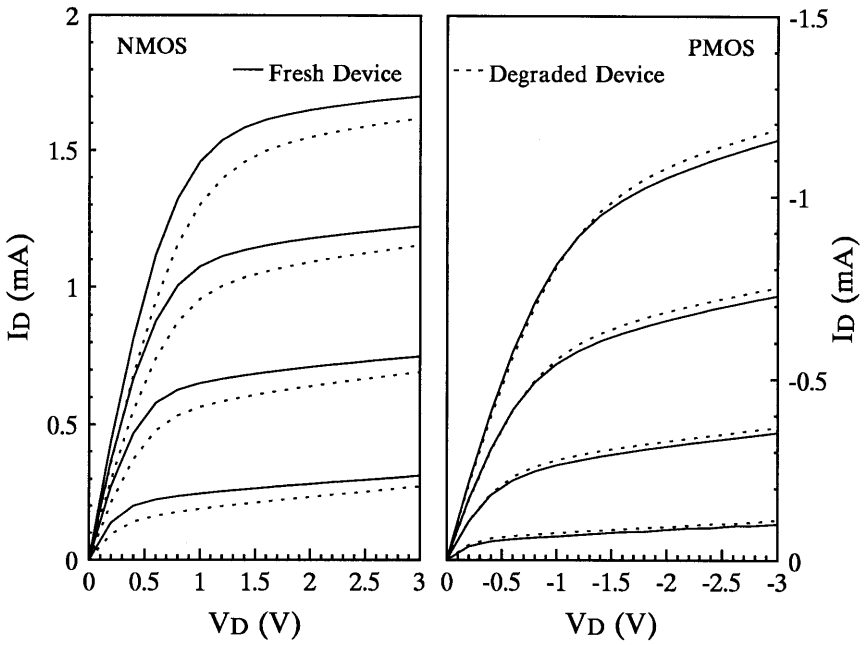

Figure 3-2: Experimental fresh and degraded IV for both N and PMOSFETs [10].

opposite to that of the NMOSFET. The degraded PMOS drain current should be larger than the fresh drain current for all bias regimes. However, as can be seen in Figure 3-2 (b), hot-carrier degradation of the PMOS device results in a decrease rather than an increase in drain current in the linear region. The explanation for this is that when the device is in linear region, the hot-carrier induced series resistance as a result of $\Delta\mu$ has a larger impact on the drain current than does the shifted threshold voltage [10]. In the saturation region, the drain current increases as expected. This demonstrates that the PMOSFET degradation model is not as quite robust as that of the NMOSFET's. For purposes of comparision, Figure 3-2 (a) shows the behavior of a fresh and degraded NMOSFET.

3.3 Differential Pair Simulation

Because PMOSFET degradation results in an increased current drive, its manifestation in a digital circuit such as an inverter is a shifted degradation curve (or performance curve) opposite to that of the NMOSFETs. Such a rule of thumb for digital-circuit design has been shown to predict reasonably accurate degradation in ring-oscillators [21]. This technique is possible because in a digital-circuit environment, most transistors are either in cut-off, or in *weak* saturation ($V_{gs} = V_{ds}$). The transition time where the gate voltage changes from low

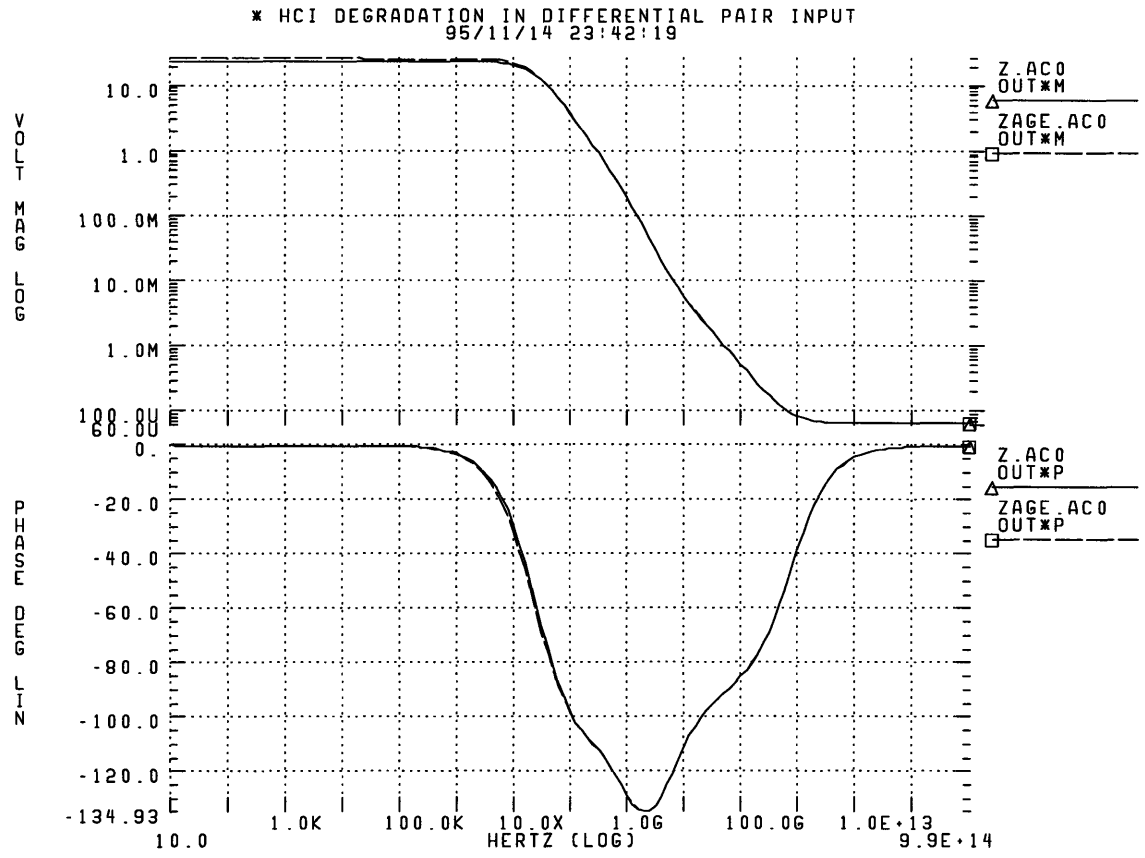

Figure 3-3: Simulation of the fresh and degraded Bode plots for a differential pair.

V_{gs} to high V_{gs} is typically smaller than one microsecond. Thus, the total degradation seen by the transistors when $V_t \leq V_{gs} \leq V_{ds}$ is small comparing to transistors in analog circuits.

In a typical analog circuit, different transistors may see different biasing conditions and degrade differently, especially those that are biased in *strong* saturation ($V_{gs} \leq V_{ds}$). One would not expect the rule of thumb as describe above to be applicable in accounting for PMOSFET degradation. If one does a full simulation of an analog circuit using existing tools and degradation models, the resulting simulated degradation would be inaccurate as shown in Figure 3-3 and 3-4. Using the existing degradation and SPICE models to simulate the differential pair of Figure 2-4, we plot the fresh and degraded Bode curves after ten years of operation in Figure 3-3.

As can be seen, the unity gain f_T of the differential pair and the phase margin change negligibly both before and after 10 years. However, the low frequency gain increases from 27.45 dB to 28.22 dB, which corresponds to a gain increase from 23.59 to 25.76. This contradicts the experimental results from earlier work where it was shown that the degradation

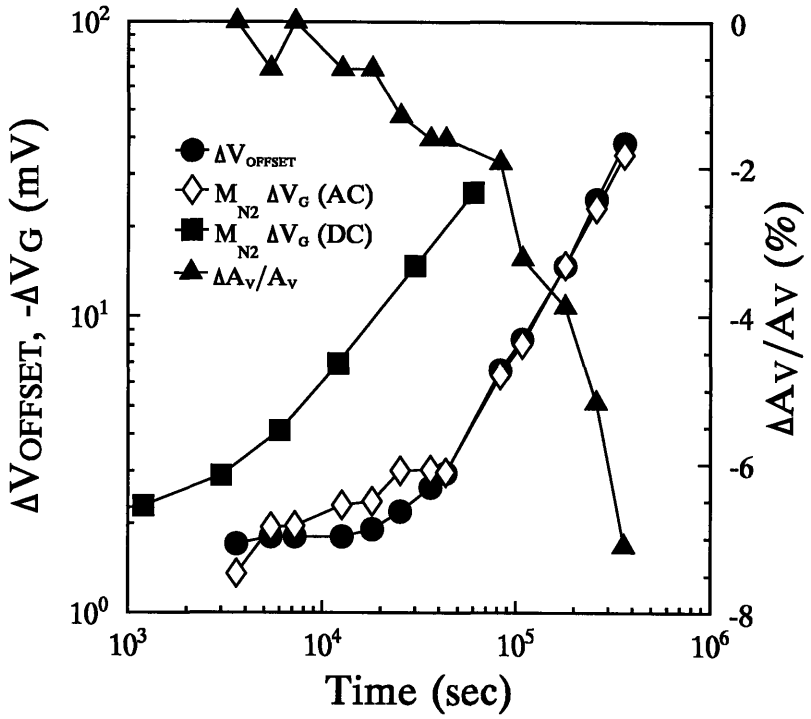

Figure 3-4: Experimental data of the differential pair stressing [22].

of a differential pair actually decreases with increasing stress time as shown in Figure 3-4 [22]. Clearly, the degradation and device simulators need improvement both in terms of model calibration, and modifying the models to be more sensitive to small-signal parameter degradation due to hot-carrier damage.

Chapter 4

Conclusion

This thesis intends to show that analog reliability simulator tools and models need several improvements. In contrast to the traditional data-fitting of digital circuits, where I_{Dsat} was the major concern, analog hot-carrier reliability models, both in BERT, and SPICE extraction programs, need to be more sensitive to small-signal parameters such as g_m and g_{ds}. Furthermore, the optimization algorithm of the SPICE parameters needs modifying to be able to *optimize globally* across several SPICE and I-V files *independent* of the algorithms already used in the existing extraction tool. Finally, new degradation models and design guidelines must be developed in light of the recent need for insuring analog circuit reliability.

The problems are not so easy to solve. While some of the issues such as model inconsistency among the simulators can be cured by simply modifying the necessary codes, others such as SPICE modeling and optimization of the model parameters may take a little more work, especially to satisfy stringent requirements for consistency in the degraded small-signal parameters such as g_m and g_{ds}. To this end, we must make a conscious effort to improve the SPICE models as well as develop new degradation models and design guidelines. Promising work is already in progress in improving the SPICE models, such as the current work going on at the University of California at Berkeley.

What we are proposing is to develop new models and algorithms that are applicable to the framework of evaluating the reliability analog-circuit designs. The traditional methodology, techniques, and benchmarks for evaluating hot-carrier degradation in digital circuit design, as we have shown, are no longer applicable to mixed-mode signal simulation. As of the writing of this thesis, we have already designed and implemented the circuits proposed

in this thesis for hot-carrier evaluation. Shown in appendix C are the actual layout of these circuits transfered to industry for fabrication.

Appendix A

BERT: Limitations of HCI Reliability Simulation

Degradation simulators such as BERT assume that the degradation of each transistor in the circuit is independent from one another, and is only a function of the terminal voltages and current of each transistor. All degradations behavior of a device is captured in the quantity called AGE that provides the means to compare the amount of degradation experienced by the device in operation with a fresh device. AGE is described by [21]:

$$Age = \int \frac{I_{ds}}{HW}\left[\frac{I_{sub}}{I_{ds}}\right]^m dt \qquad \text{NMOSFET} \qquad \text{(A.1)}$$

$$Age = W_g \int \frac{1}{H}\left[\frac{I_g}{W}\right]^m dt + W_b \int \frac{I_{ds}}{HW}\left[\frac{I_{sub}}{I_{ds}}\right]^m dt \qquad \text{PMOSFET} \qquad \text{(A.2)}$$

where W_g and W_b are weighting factors that take into account both the gate and substrate current in PMOSFET degradation mechanisms. The DC version of AGE is defined by Equation 1.9.

During circuit simulation, the "AC" AGE is calculated for each device and at each time step using the terminal voltages and currents. It is then integrated to obtain the total AGE over the simulated operation time of the circuit. After the AGE of each transistor in the circuit is computed by this 'quasi-static' method, it is compared to the list of "DC" ages stored in a separate files called the "agetable" to generate the aged SPICE models using the methods of regression or interpolation [23]. Graphically, the steps are shown in Figure A-1.

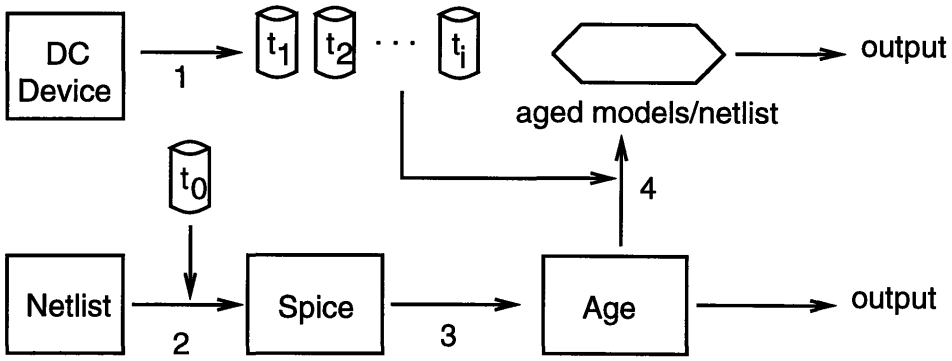

Figure A-1: Inner working of BERT.

1. SPICE extraction of a device is done at time t_0 (fresh), and at subsequent t_1, t_2, ... t_i (after DC stress for t_1, t_2, ... minutes). A reference SPICE file is extracted and generated at various stressed times with the associated DC age computed by Equation 1.9. Substrate current is also measured to extract the appropriate substrate current parameters.

2. The SPICE netlist for the fresh device (t_0) is fed into circuit simulator (such as SPICE) to get terminal voltage and current waveforms.

3. The age of each transistor is calculated according to equation A.1 and A.2. Substrate current I_{sub} is calculated based on the SPICE output and using equation [6]:

$$I_{sub} = \frac{A_i}{B_i} E_m l_c I_d \exp - \frac{B_i}{E_m} \tag{A.3}$$

where

$$E_m \approx \frac{(V_{ds} - V_{dsat})}{l_c} \tag{A.4}$$

4. Regression / Interpolation between the reference SPICE files is used to calculate the appropriate aged SPICE models for each transistors to produce an 'aged' netlist file. This file can be simulated again to predict the performance of the circuit after it degrades.

Once the SPICE model files and BERT parameters (m, n, and H) are calibrated, the above process can be repeated to get accurate prediction of circuit performance at different future times under a particular operating conditions. The tools (SPICE, BERT)

have been shown to simulate digital-circuits degradation—namely ring-oscillators frequency degradation—to within a few percent. It will be shown here that, the same methodology may not apply for analog circuits.

Since most of the digital circuit parameters are encapsulated by variables such as τ_{pd}, a slight perturbation in the device parameters such as V_t, or MU_0 will not affect the circuit parameters. However, small variations in V_t or V_{FB} will have enormous impact on analog circuit parameters such as g_m or g_{ds}. These small variations in V_t and V_{FB} come about, not only from the hot-carrier degradation itself, but also from the regression / interpolation step during the circuit aging simulation process as described above.

The difficulties in achieving (interpolating) an accurate degraded SPICE parameter file involves two parts. The first part begins with the extraction and optimization of a degraded device's I-V characteristic. The second part involves the interpolation step carried at during the circuit aging calculation.

1. Traditionally, we have understood the mobility degradation to be dependent on the stress time as shown in previous chapters. As a consequent, when one does parameter extraction for a degraded device, one would typically 'lock' all the SPICE parameters except for the mobility term itself, and by optimizing the low field mobility term (MU_0 in BSIM2 model), one would expect to get a nice fit to the data. However, as can be seen in figure A-2, the SPICE parameter $U1_0$—high drain field (velocity saturation) mobility reduction factor—also has a dependence on the degradation, and if one makes the mistake of locking such a parameter, one would not be able to get a good fit. The difficulty is in deciding which parameters to lock and which not to lock since most of the parameters in BSIM2 model are empirical fitting parameters.

2. The second part involves the implementation of the circuit aging calculation algorithm in BERT. Because the method of calculating a particular parameter P_i can either be the *linear* interpolation or regression (see Figure A-3), it is applied to all the parameters. As we can see from figure A-2 however, some of the SPICE parameters have a *quadratic* dependence on the age rather a linear one. We have found that, across all SPICE parameters, some parameters have a linear dependence on the age where as others have a quadratic one.

Due to these issues, and others as noted in previous chapters, the circuit aging calculating

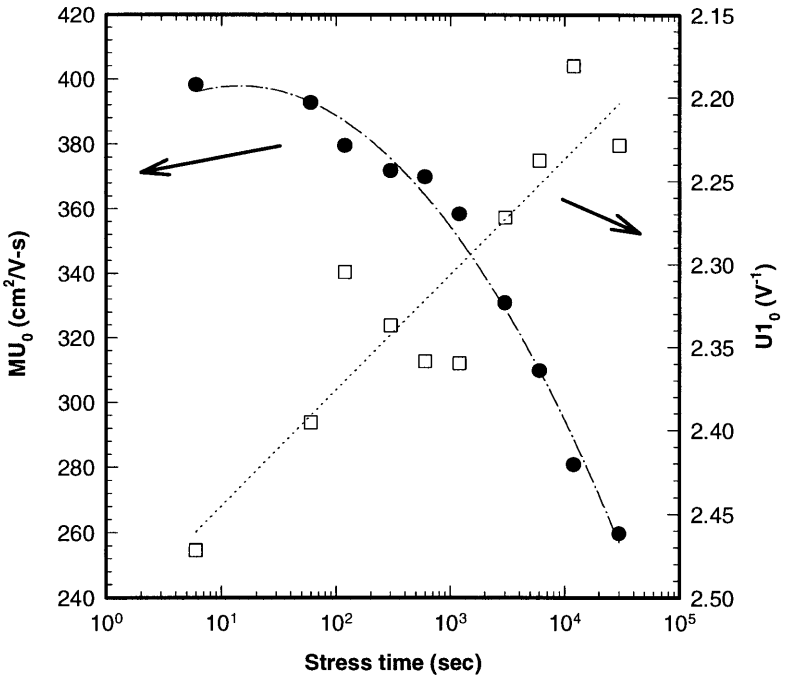

Figure A-2: Linear and quadratic dependency of MU_0 and $U1_0$ in linear scale.

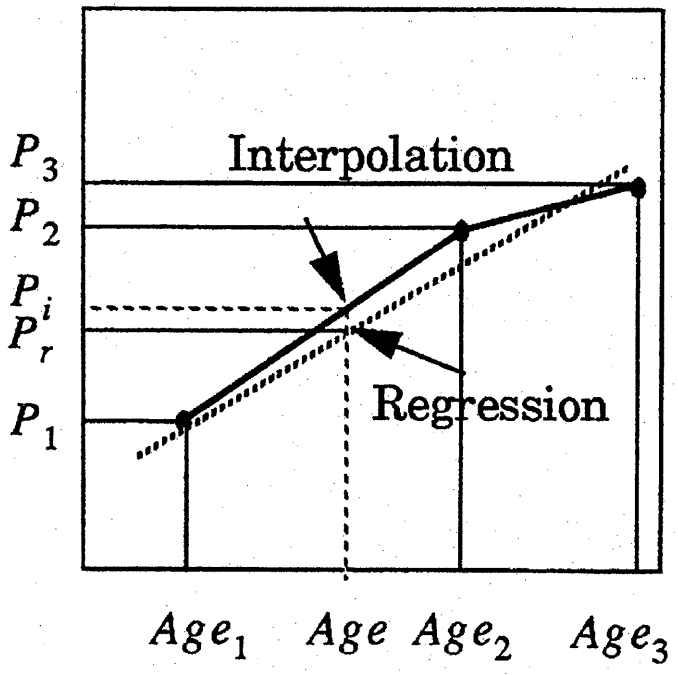

Figure A-3: How BERT calculate degraded SPICE parameter [24].

algorithm implemented in BERT sometimes returns an unexpected, out-of-range value for a particular SPICE parameter that, when it is fed to HSPICE, gives an error. This usually happens when the interpolation point is not in between any two degraded SPICE reference files, thus requiring the simulator to extrapolate outside the AGE range available. One way to get around this is to insure the maximum-aged SPICE reference file be larger than the largest degradation experience by any transistor in the circuit being simulated.

Appendix B

SPICE & BERT Simulation Input Files

Shown here in this appendix are the SPICE netlist files and BERT command files used for the hot-carrier reliability simulation. Notice that all the parasitic capacitances in the SPICE files have been removed. Only the nodal connection of the main elements are shown.

B.1 BERT Command File

Typical BERT commands are shown here in this file. For simulations where iterative runs were required, we changed the corresponding variable in this command file and repeatedly ran the simulation.

```
* hci degradation simulation

.option nomod noelck post
.param power=3.0 ibias=3e-3
.param vout=1

* spice files and input wave forms
.include '~/fig4a.spice'

* spice model files
.include '~/model0.n'

* BERT commands
* 3.14496e7 sec/yr
```

```
.age 3.155e8
.agemethod interp linlog
.ageproc nmos files= ~/model0.n
+  ~/model1.n ~/model2.n ~/model3.n ~/model4.n
+  ~/model5.n ~/model6.n ~/model7.n ~/model8.n ~/model9.n
.degprint all
.degsort
.deltad 10.0000e-02
.minage  0.00e+00
.plotisub all
.spicetype 7 4
.scale  1.0000e+00
.scalm  1.0000e+00

.END
```

B.2 SPICE Netlist for MOSFET Simulation

```
m1 vd vg vs vb nmos w=100.0u l=1.0u

vd vd 0 6.3
vg vg 0 5.8
vs vs 0 0
vb vb 0 0

* lv9  : vt lv10 : vdsat
* lx2  : vgs lx3  : vds lx4  : Drain current
* lx7  : gm lx8  : gds

*.dc vd 0 power 'power/100' vg 1.0 power 'power/8'
*.dc vg 0 power 'power/100'
.tran 10e-12 100e-9

.plot dc lx4(m1) lx7(m1) lx8(m1)
```

B.3 Netlist for Differential Pair Simulation

```
****** top level cell is ./fig1a.ext
m3 outn outn vdd nwell pmos w=33.0u l=0.6u
m4 vdd outn outp nwell pmos w=33.0u l=0.6u
m1 vcom vin outn psub nmos w=100.0u l=0.6u
m2 vcom vip outp psub nmos w=100.0u l=0.6u
```

```
m6 ibias ibias vss psub nmos w=50.0u l=0.6u
m5 vss ibias vcom psub nmos w=50.0u l=0.6u

cin    vin  0 1.42p
cip    vip  0 1.42p
coutn  outn 0 1.42p
coutp  outp 0 1.42p
css    vss  0 1.42p
cpsub  psub 0 1.42p
cdd    vdd  0 1.42p
cbias ibias 0 1.42p
cwell nwell 0 1.42p
com    vcom 0 1.42p

vin vin 0 dc 0 ac 1
vip vip 0 dc 0
.ac dec 10 1e2 1e14
*.pz v(outn) vin
*.tf v(outn) vin

*vin vin 0 sin (0 0.1 150e6)
*vip vip 0 dc 0
*.tran

vss vss 0 '-power'
vdd vdd 0 power
vwell nwell 0 power
vsub psub 0 '-power'
ibias ibias 0 '-ibias'
```

Appendix C

Layout of The Figures in Chapter 2

Shown here in this appendix are the layout of the subcircuits in Figures 2-4 to 2-12. Notice that only the (a) versions of each subcircuits are showned here.

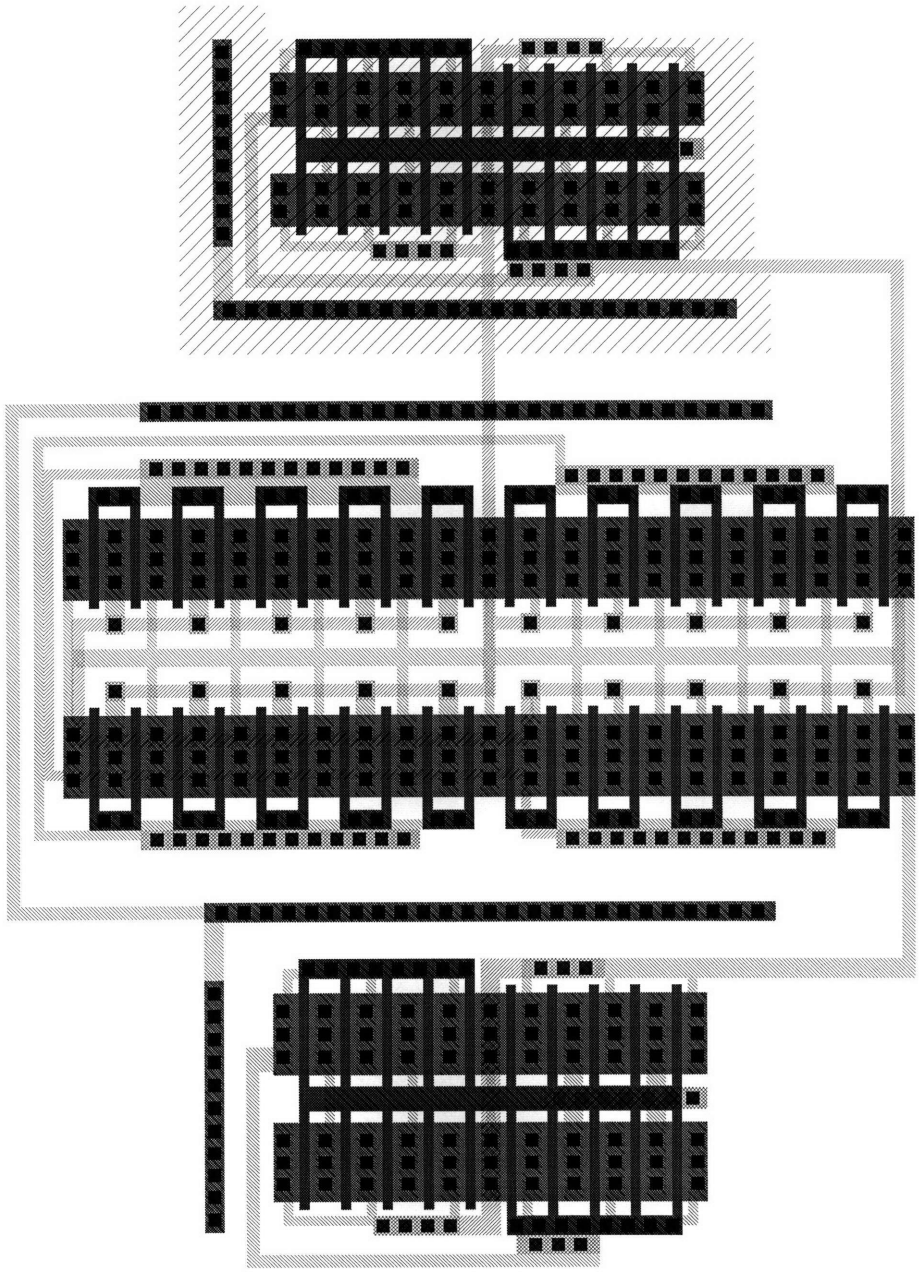

Figure C-1: Layout of the test circuit of the low-frequency differential pair (Figure 2-4).

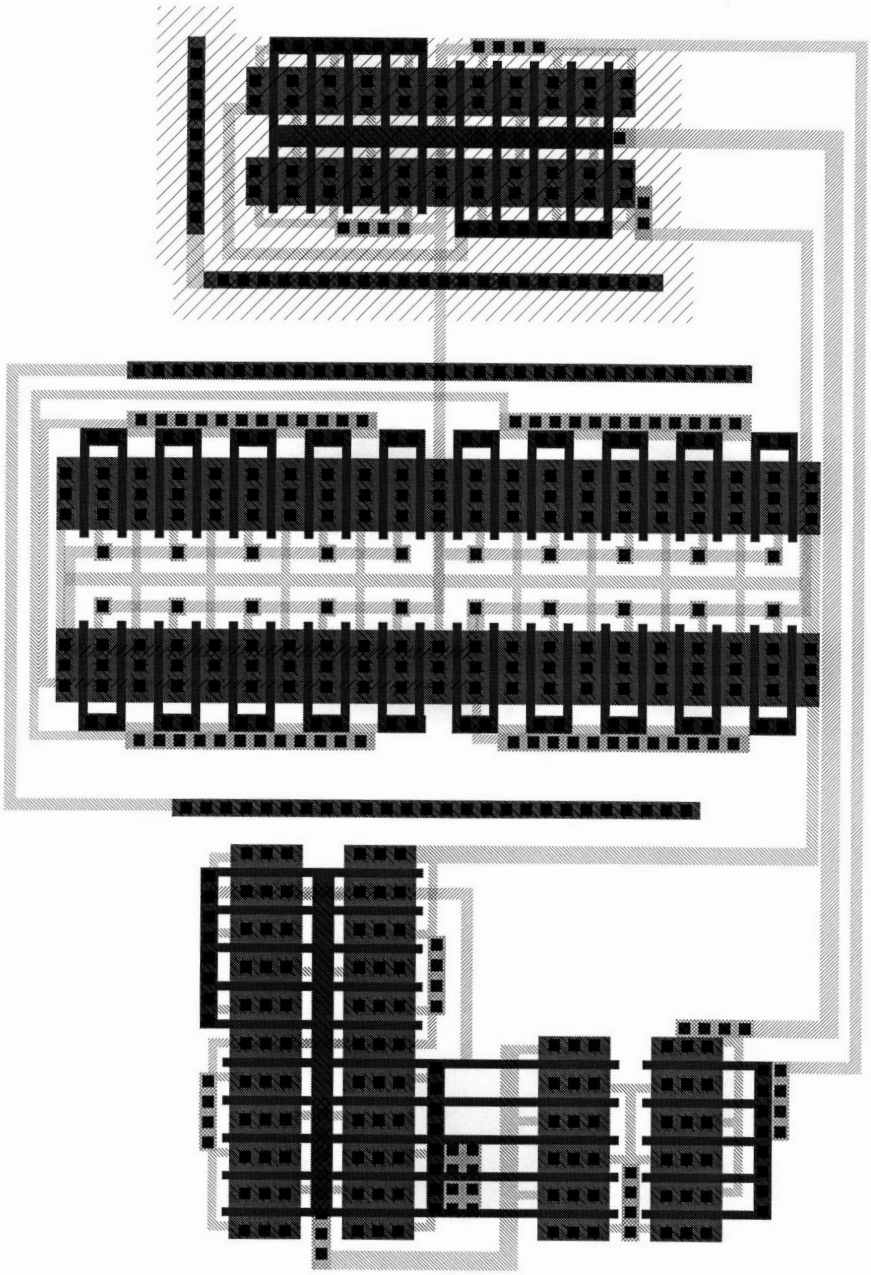

Figure C-2: Layout of the test circuit of the high-frequency differential pair (Figure 2-5).

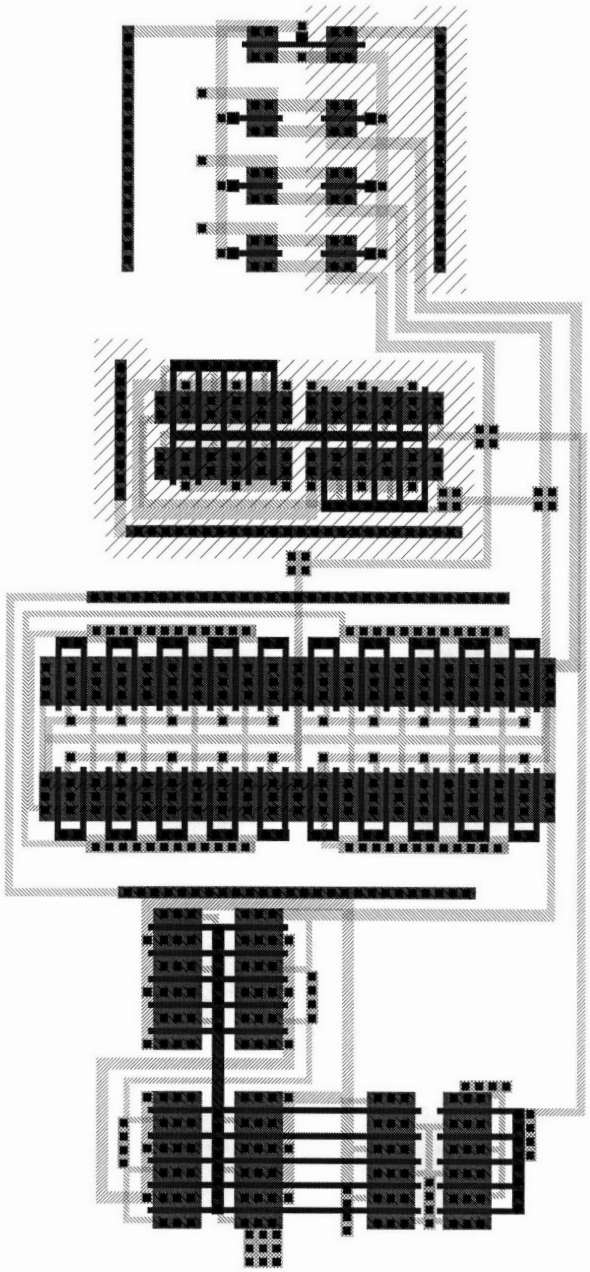

Figure C-3: Layout of the test circuit of the mixed-frequency differential pair (Figure 2-6).

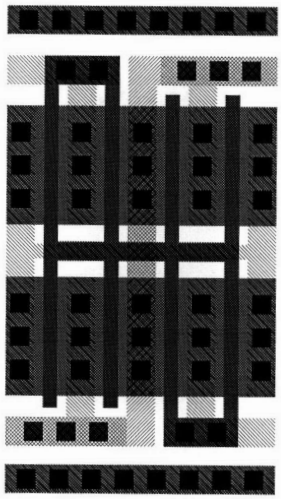

Figure C-4: Layout of the test circuit of the simple current mirror (Figure 2-7).

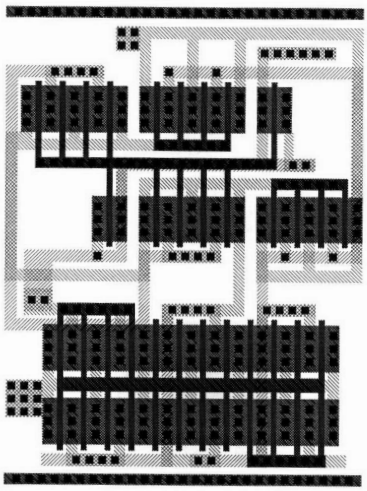

Figure C-5: Layout of the test circuit of the cascode current mirror (Figure 2-8).

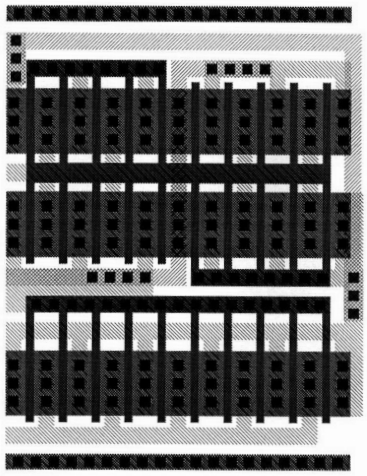

Figure C-6: Layout of the test circuit of the Wilson current mirror (Figure 2-9).

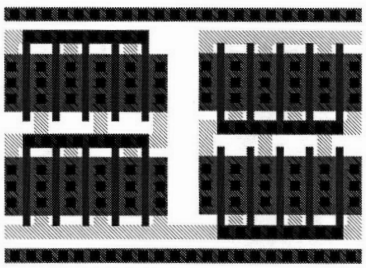

Figure C-7: Layout of the test circuit of the bias-voltage generator (Figure 2-10).

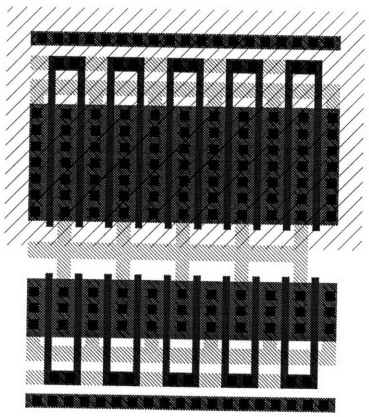

Figure C-8: Layout of the test circuit of the common-source amplifier (Figure 2-11).

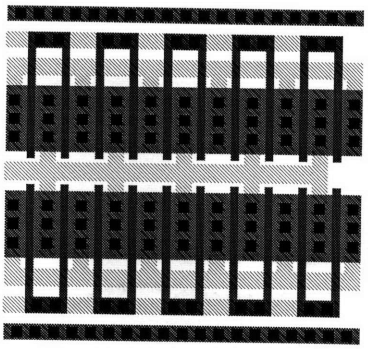

Figure C-9: Layout of the test circuit of the source follower (Figure 2-12).

Bibliography

[1] Cheng T. Wang. *Hot Carrier Design Considerations for MOS Devices and Circuits.* Van Nostrand Reinhold, 1992.

[2] Richard S. Muller and Theodore L. Kamins. *Device Electronics For Integrated Circuits.* John Wiley & Sons, second edition, 1986.

[3] Stanley Wolf. *Process Integration*, volume 2 of *Silicon Processing for the VLSI Era.* Lattice Press, Lattice Press, 1990.

[4] Paul Gray and Robert Meyer. *Analysis and Design of Analog Integrated Circuits.* John Wiley & Sons, third edition, 1993.

[5] F.C. Hsu and S. Tam. Relationship between mosfet degradation and hot-electron-induced interface-state generation. In *Electron Device Letters*, number 2 in EDL-5. IEEE, February 1984.

[6] Chenming Hu, Simon C. Tam, Fu-Chieh Hsu, Ping-Keung Ko, Tung-Yi Chan, and Kyle W. Terrill. Hot-electron-induced mosfet degradation-model, monitor, and improvement. In *Transaction on Electron Devices*, number 2 in ED-32, pages 375–385. IEEE, February 1985.

[7] Robert H. Tu, Elyse Rosenbaum, Wilson Y. Chan, Chester C. Li, Eric Minami, Khandker Quader, Ping Keung Ko, and Chenming Hu. Berkeley reliability tools—bert. In *Trans. on Computer Aided Design of Integrated Circuits and Systems*, number 10 in Vol. 12, pages 1524–1534. IEEE, October 1993.

[8] Shian Aur, Dale E. Hocevar, and Ping Yang. Hotron—a circuit hot electron effect simulator. In *International Conference Computer-Aided Design*, CH2469, pages 256–259. IEEE, May 1987.

[9] Bing J. Sheu, Wen-Jay Hsu, and Bang W. Lee. An integrated-circuit reliability simulator—rely. In *Journal of Solid-State Circuits*, Vol. 24, pages 473–477. IEEE, April 1989.

[10] Vei-Han Chan, Thomas E. Kopley, Paul J. Marcoux, and James E. Chung. High-frequency ac hot-carrier degradation in cmos circuits. In *International Electron Device Meeting*. IEEE, 1994.

[11] Khander N. Quader, Peng Fang, John T. Yue, Ping K. Ko, and Chenming Hu. Hot-carrier-reliability design rules for translating device degradation to cmos digital circuit degradation. In *Transaction on Electron Device*, number 5 in 41, pages 681–691. IEEE, May 1994.

[12] W. Weber, L. Risch, W. Krautschneider, and Q. Wang. Hot-carrier degradation of cmos-inverters. In *International Electron Device Meeting*, CH2528, pages 208–211. IEEE, 1988.

[13] C. Duvvury, D. Redwine, H. Kitagawa, R. Haas, Y. Chuang, C. Beydler, and A. Hyslop. Impact of hot carriers on dram circuits. In *International Reliability Physical Symposium*, CH2388, pages 201–206. IEEE, 1987.

[14] Anant G. Sabnis and James T. Nelson. A physical model for degradation of drams during accelerated stress aging. In *International Reliability Physical Symposium*, number 5 in CH1846, pages 90–95. IEEE, April 1983.

[15] Jacob A. van der Pol and Jan J. Koomen. Relation between the hot carrier lifetime of transistors and cmos sram products. In *International Reliability Physical Symposium*, CH2787, pages 178–185. IEEE, 1990.

[16] Y. Tsividis and K. Suyama. Mosfet modelling for analog circuit cad: Problems and prospects. In *Custom Integrated Circuits Conference*, pages 14.1.1–14.1.6. IEEE, March 1993.

[17] Vei-Han Chan, Jeffery S. Kim, and James E. Chung. Parameter extraction guidelines for hot-electron reliability simulation. In *International Reliability Physical Symposium*. IEEE, 1993.

[18] SeokWon A. Kim, Beniyam Menberu, Thomas E. Kopley, and James E. Chung. Oxide-field dependence of the nmos hot-carrier degradation rate and its impact on ac-lifetime prediction. In *International Electron Device Meeting.* IEEE, 1995.

[19] Roger T. Howe and Charles G. Sodini. *Microelectronics: An Integrated Approach.* MIT 6.012 Course Note, second edition, 1995.

[20] Tong-Chern Ong. *Hot-Carrier Effects in P-MOSFETs.* PhD dissertation, University of California, BERKELEY, Department of Engineering, January 1988.

[21] Khandker N. Quader, Ping K. Ko, and Chenming Hu. Simulation of cmos circuit degradation due to hot-carrier effects. In *International Reliability Physical Symposium,* CH3084, pages 16–23. IEEE, 1992.

[22] Vei-Han Chan and James E. Chung. The impact of nmosfet hot-carrier degradation on cmos analog subcircuit performance. In *Journal of Solid-State Circuits,* number 6 in Vol. 30, pages 644–649. IEEE, June 1995.

[23] Peter M. Lee, Mary M. Kuo, Koichi Seki, P. K. Ko, and C. Hu. Circuit aging simulator (cas). In *International Electron Device Meeting,* CH2528, pages 134–137. IEEE, 1988.

[24] BTA Technology, Inc., Santa Clara, CA. *BTABERT User's Manual,* 1.01 edition, October 1993.

[25] Meta-Software, Inc., Campbell, CA. *HSPICE User's Manual,* h92 edition, 1992.