Design of Resonant-Tunneling Diodes for a GaAs Integrated SRAM

by

Rajni J. Aggarwal

S.B., S.M., Massachusetts Institute of Technology (1990)

Submitted to the
Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

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Abstract

The resonant-tunneling diode (RTD) has frequently been cited as a potential building block for high speed, low complexity circuits. This work investigates the application of RTDs in a SRAM. The effects of six design parameters on memory switching speed and static power are evaluated and design rules for a two-RTD one-EFET SRAM cell are established. A novel integration technique, Epitaxy-on-Electronics (EoE), enables the integration of high performance relaxed-buffer $In_xGa_{1-x}As/AlAs$ RTDs on commercial GaAs circuits. A variety of relaxed buffers and relaxed-buffer RTD (RBRTD) structures were investigated. We conducted a study of several grading methods at MBE growth temperatures suitable for EoE and found that the threading dislocation density of the RBRTDs is relatively immune to the indium grading profile. RBRTDs grown on integrated circuits (IC) and epi-ready substrates (ERS) were compared. Greater relaxation was observed in the material grown on the IC. RTDs integrated on the IC had lower current densities than those grown on the ERS. This reduction is attributed to the presence of misfit dislocations in the RTD barrier/well interfaces which are depleting the RTD, effectively reducing the RBRTDs electrical area. Integrated RBRTD-EFET SRAM cells were designed, fabricated, and a proof-of-concept SRAM cell was successfully demonstrated.

Thesis Supervisor: Clifton G. Fonstad, Jr. Title: Professor of Electrical Engineering

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Despite the frustrations of research and the climate and atmosphere of New England, I can honestly say that I did enjoy some parts of this experience. The enjoyment has come from my interactions with the people around me. I appreciate all of their efforts toward my continued success. A few, in particular, deserve special thanks.

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Contents

1 Introduction **15**
1.1 Monolithic RTD-based SRAMs . . . 16
1.2 Thesis Organization . . . 17

2 RTD-EFET SRAM **19**
2.1 Operation of an RTD-EFET SRAM . . . 19
2.2 Static Power of an RTD-EFET SRAM . . . 23
2.3 Switching Current of an RTD-EFET SRAM . . . 26
2.4 Switching Speed of an RTD-EFET SRAM . . . 27
2.4.1 SRAM Model Description . . . 28
2.4.2 Effects of PVCR . . . 31
2.4.3 Effects of Current Density . . . 34
2.4.4 Combined Effects of PVCR and Current Density . . . 36
2.5 Desired RTD Characteristics for an RTD-EFET SRAM . . . 38

3 RTD-MESFET Circuit Design and Fabrication **41**
3.1 Epitaxy-on-Electronics Integration Technique . . . 41
3.1.1 RTD-MESFET Circuit Design . . . 43
3.1.2 MESFET Circuit Fabrication . . . 43
3.1.3 MBE Heterostructure Growth . . . 44
3.1.4 RTD Fabrication . . . 45
3.2 Well Array . . . 46
3.3 SRAM Cells . . . 48
3.4 Memory Array . . . 55
3.5 Circuit Summary . . . 62
3.6 MIT-OEIC-3 Features . . . 63
3.6.1 Conversion Errors . . . 64
3.6.2 Implanted vs. Nonimplanted DGWs . . . 64
3.6.3 DGW Cleaning Problems . . . 65

4 Relaxed-Buffer RTDs **67**
4.1 Relaxed-Buffer RTD Materials 67
4.2 Mechanisms of Strain Relief in Relaxed Buffers 73
4.3 Relaxed-Buffer Demonstrations 75
4.4 EoE-Compatible Relaxed Buffer Quality 76
4.4.1 Effect of Grading Method on Relaxation 78
4.4.2 Effect of Grading Method on Dislocation Density 85
4.5 High-PVCR RBRTD 96
4.6 Series Resistance of RBRTDs 98

5 Characterization of Monolithically Integrated RBRTDs **105**
5.1 Material Characterization of Integrated RBRTDs 106
5.1.1 IC Substrate Quality 106
5.1.2 IC Epitaxial Material Quality 107
5.2 Degradation of IC Electronics 113
5.3 Electrical Characterization of Integrated RBRTDs 115
5.3.1 Effect of Substrate on RBRTD Performance 116
5.3.2 Performance of Well Array RBRTDs 124

6 Characterization of RTD-EFET SRAM Circuits **127**
6.1 Monolithic RTD-EFET SRAM Circuits 127
6.2 Hybrid RTD-EFET SRAM Circuits 130

7 Conclusions **137**
7.1 Accomplishments 137
7.2 Future Work 140
7.2.1 Integration Studies 140
7.2.2 Materials Studies 141
7.2.3 Electrical studies 141

A RTD-EFET SRAM Analytic Model **143**

B Documentation for RTD-OEIC-1 **149**

C Integrated RTD Process Flow **161**

D RTD-EFET Ring Oscillator **165**

E X-ray Diffraction **169**

List of Figures

2-1 Circuit schematic of the RTD-EFET SRAM cell. 19
2-2 Operation of the RTD-EFET SRAM cell. 21
2-3 Load line characteristics as a function of V_{RTD}. 24
2-4 Measured voltage bistability of an RBRTD storage element. 25
2-5 Measured $I_{switch,min}$ requirements for an RTD storage element. 26
2-6 Load line schematics of minimum required switching current. 27
2-7 RTD-EFET SRAM switching model. 29
2-8 Effects of RTD PVCR on cell performance. 32
2-9 Storage element load lines as a function of V_{RTD} and PVCR. 33
2-10 Effects of RTD current density on cell performance. 34
2-11 Storage element load lines as a function of V_{RTD} and current density. 35
2-12 Effects of RTD PVCR and current density on cell performance. 36
2-13 Effects of node capacitance on cell performance. 37

3-1 Integrated RTD-EFET SRAM process flow. 42
3-2 Thermal stability of IC metals. 43
3-3 RTD-OEIC-1 mask layout. 45
3-4 Layout of well array. 47
3-5 Circuit schematics of the RTD-EFET SRAM cells. 48
3-6 Layout of one-bit memory cells with a shared S/D implant. 49
3-7 Layout of one-bit memory cells without a shared S/D implant. 50
3-8 Simulated operation of a 100 μm^2 RBRTD. 51
3-9 Simulated operation of cell RJA1A: voltage nodes. 52
3-10 Simulated operation of cell RJA1A: currents. 53
3-11 Circuit schematic of 4×1-bit memory array. 56
3-12 Layout of 4×1-bit memory array. 57
3-13 Simulated operation of bits 11 and 00 of the memory array. 58
3-14 Simulated operation of bits 10 and 01 of the memory array. 60
3-15 MIT-OEIC-3 prior to MBE growth. 63
3-16 AFM profile of DGW substrate. 65

4-1 Conduction bands of RTD-barrier materials. 68
4-2 Performance of GaAs/Al_xGa_{1-x}As resonant-tunneling diodes. 69
4-3 In_xGa_{1-x}As/AlAs RTD material features. 70
4-4 Performance of In_xGa_{1-x}As/AlAs RTDs. 71
4-5 Calculated energy states for a RBRTD. 72
4-6 Schematic of pseudomorphic and relaxed epitaxial layers. 73
4-7 Defect nucleation and propagation. 74
4-8 Relaxed-buffer epitaxial structures. 77
4-9 X-ray rocking curve of a single-step RBRTD. 78
4-10 Cathodoluminescence spectrum of a single-step RBRTD. 79
4-11 X-ray rocking curves of a multiple-step RBRTD with a thick cap. 80
4-12 X-ray rocking curves of a multiple-step RBRTD with a thin cap. 81
4-13 Cathodoluminescence spectra of multiple-step RBRTDs. 81
4-14 X-ray rocking curves of a linearly graded RBRTD. 82
4-15 Cathodoluminescence spectrum of linearly graded RBRTD. 83
4-16 Surface maps of a single-step RBRTD. 86
4-17 X-TEM of a single-step RBRTD. 86
4-18 PV-TEM of a single-step RBRTD. 87
4-19 Surface maps of a multiple-step, thick cap RBRTD. 88
4-20 X-TEM of a multiple-step, thick cap RBRTD. 88
4-21 PV-TEM of a multiple-step, thick cap RBRTD. 89
4-22 Surface maps of a multiple-step, thin cap RBRTD. 90
4-23 X-TEM of a multiple-step, thin cap RBRTD. 91
4-24 PV-TEMs of a multiple-step, thin cap RBRTD. 92
4-25 Surface maps of a linearly graded RBRTD. 93
4-26 X-TEM of a linearly graded RBRTD. 93
4-27 PV-TEM of a linearly graded RBRTD. 94
4-28 I–V Characteristics of a high-PVCR RBRTD. 96
4-29 X-ray rocking curve of a high-PVCR RBRTD. 97
4-30 10 K PL spectrum of a high-PVCR RBRTD. 98
4-31 X-ray rocking curve of RBRTD doping series. 99
4-32 I–V characteristics of RBRTD 7089. 100
4-33 I–V characteristics of RBRTD 7090. 101
4-34 I–V characteristics of RBRTD 7091. 101

5-1 AFM 3-D surface map of DGW substrate. 106
5-2 PL spectra comparison of IC and ERS epitaxial material. 107
5-3 Cl spectra as a function of position in an IC DGW: lattice-matched material. . . . 108
5-4 Cl spectra as a function of position in an IC DGW: MQW sample. 109
5-5 CL spectra of a linearly graded RBRTD. 110

5-6 Cl spectra of a linearly graded RBRTD as a function of position in an IC DGW. . 111
5-7 Surface maps of a linearly graded RBRTD. 112
5-8 I–V of a 10×1.2 μm EFET before and after thermal cycling. 113
5-9 Fully processed MIT-OEIC-3 IC with RBRTDs. 115
5-10 RBRTD numbering scheme. 116
5-11 RBRTD uniformity across IC–N003. 117
5-12 RBRTD uniformity across IC–S032. 118
5-13 Comparison of integrated and non-integrated RBRTD I–Vs. 121
5-14 Schematic of EoE IC and ERS misfit dislocations. 122
5-15 Schematic of defect created depletion region. 123
5-16 I–V characteristics of well array RBRTDs. 125

6-1 Photograph of a fully integrated RTD-EFET SRAM cell. 128
6-2 Photograph of a fully integrated 4-bit RTD-EFET SRAM. 128
6-3 Schematic of the hybrid memory cell measurement configuration. 130
6-4 RTD-EFET SRAM cell write operation: 5×5 μm RTDs, 350 nsec SELECT pulse. 131
6-5 RTD-EFET SRAM cell write operation: 5×5 μm RTDs, 100 nsec SELECT pulse. 132
6-6 RTD-EFET SRAM cell write operation: 10×10 μm RTDs, 100 nsec SELECT pulse.133

D-1 Schematic of an RTD-EFET ring oscillator. 165
D-2 Schematic of 23-stage RTD-EFET ring oscillator. 166
D-3 Layout of 23-stage RTD-EFET ring oscillator. 167
D-4 Simulated operation of 23-stage RTD-EFET ring oscillator. 168

E-1 Schematic of the rocking curve reflection angles. 169

List of Tables

1.1 Partial summary of resonant-tunneling device applications reported in recent literature. 15

2.1 Calculated RTD-EFET SRAM performance for a variety of RTDs. 38

3.1 Summary of one-bit memory-cell parameters. 48

4.1 Summary of RTDs grown on relaxed buffers. 76
4.2 Experimental bandgap energies of RBRTDs. 83
4.3 TDD of RBRTDs. 95
4.4 Epitaxial structure of the RBRTD doping series. 99
4.5 RBRTD doping series device statistics. 102

5.1 Effects of temperature on EFET performance. 113
5.2 Effects of temperature on IC resistor performance. 114
5.3 Performance of multiple-step RBRTDs on a MIT-OEIC-3 IC. 119
5.4 Performance of multiple-step RBRTDs on an ERS. 119
5.5 Performance of linearly graded RBRTDs integrated on an MIT-OEIC-3 IC. 119
5.6 Performance of linearly graded RBRTDs on an ERS. 120
5.7 Comparison of integrated RBRTDs: discrete vs. well array. 126

6.1 Partial summary of SRAM cell performance. 134
6.2 Comparison of simulated and experimental SRAM performance. 135

7.1 Comparison of GaAs and RTD-EFET SRAM cell performance. 138
7.2 Comparison of recent GaAs SRAMs. 139

B.1 Standard RTD dimensions. 149
B.2 Well-array device sizes. 150
B.3 Laser array device sizes. 151

1

Introduction

The resonant-tunneling diode (RTD) is one device which has considerable potential to make the transition from research labs to commercial applications. First introduced by Tsu and Esaki [1], the distinguishing feature of the RTD is its region of negative-differential resistance. The device has shown promise for uses ranging from oscillators to high-speed circuits [2, 3]. One of the greatest challenges engineers face today is bringing developmental devices from research labs into commercial production. Along these lines, considerable effort has been expended to realize the promise of RTDs in practical applications. Table 1.1 provides a partial summary of recent RTD circuit efforts.

Application	Research group	References
InAs/GaSb/AlSb interband-RTD-based SRAM	Shen @ Motorola	[4, 5]
InAlAs/InGaAs double-emitter RHET SRAM	Mori @ Fujitsu	[6]
InGaAs/InAlAs RTD/HEMT SRAM	Watanabe @ Fujitsu	[7]
InGaAs/AlAs RTD-based multiple input logic gates	Takeyoshi and Maezawa @ NTT	[8, 9]
Multidimensional multiple-state SRAM	Shieh @ Univ. of Maryland	[10]
RTD-based multivalued SRAM	Wei @ Univ. of Maryland	[11]
RTD/depletion mode MESFET multivalued memory	Yan @ Simon Frasier Univ.	[12]
GaAs/AlAs RTD MESFET logic gates	Lear @ Stanford Univ.	[13]
RHET-based logic circuits	Takatsu @ Fujitsu	[14]
RTD-based A/D converter	Wei @ Univ. of Maryland	[15]
RTD/HBT logic circuits	Seabaugh @ Texas Instruments, Inc.	[16]
GaAs/AlAs RTD broad-band trigger circuit	Yang @ Hewlett Packard	[17]

Table 1.1: Partial summary of resonant-tunneling device applications reported in recent literature.

RTDs offer potential advantages for circuits in four areas: switching speed, reduced circuit complexity, small device sizes for high density circuits, and compatibility with III-V optical

materials. Recently, researchers at NTT demonstrated an $In_{0.53}Ga_{0.47}As/AlAs$ RTD with a valley-to-peak, i.e., *off* to *on*, switching time of 1.5 psec [18]. The multivalued nature of the RTD I–V characteristics can be used to reduce the number of elements in logic and memory circuits. The RTD is a scalable device, and thus its I–V characteristics are maintained with a reduction in size. A very small device size offers the potential for high density circuits. And finally, the materials and processing used for RTDs are compatible with those used for III-V based optical devices. There is a great deal of interest in optoelectronic integrated circuits (OEICs). A RTD circuit technology will provide a high speed electronic counterpart to III-V photonic devices, enabling one form of OEICs.

1.1 Monolithic RTD-based SRAMs

We are particularly interested in an RTD-based static random access memory (SRAM). Three approaches have been discussed in the literature: a single-transistor, two-RTD architecture; a double-emitter resonant hot-electron transistor (RHET) architecture; and a multipeaked RTD architecture. Fujitsu initially proposed a single-transistor, two-RTD SRAM cell using $In_xGa_{1-x}As/In_xAl_{1-x}As$ HEMTs and $In_xGa_{1-x}As/AlAs$ RTDs [7]. The RTDs serve as the storage element and the transistor provides read and write access to the memory cell. The transistor and RTDs were grown in a single MBE run. Because the HEMT did not have current gain, it was not the appropriate device to build the necessary addressing circuitry for a large-scale memory. Fujitsu abandoned the architecture in favor of one incorporating double-emitter RHETs [6]. Fujitsu had previously demonstrated a variety of logic circuits built with similar RHETs [14]. This architecture has been adopted by Motorola, with the exception of using a tunnel diode with two resonant-interband-tunneling diodes (RITDs) to create a similar band-structure profile as the double-emitter RHET. Motorola is implementing the memory in the $In_xGa_yAl_{1-x-y}Sb$ material system [4, 5]. The third approach uses RTDs to create a multivalued SRAM cell. Wei [11] and Yan [12] proposed versions of this cell. Both use series combinations of RTDs to create a multipeaked I-V characteristic. Yan uses a depletion-mode FET as a load while Wei uses another set of RTDs. Wei's approach has been further developed by Shieh to utilize multiple-well RTDs to create the multipeaked I–V characteristic, and to use these RTDs as both driver and load devices in a multistate memory [10].

Our approach builds on the single-transistor, two-RTD SRAM architecture. We utilize MBE growth on commercial circuits to combine a proven GaAs MESFET technology with RTDs. We use the Vitesse HGaAs3 process to fabricate high-performance GaAs DCFL circuits on which we epitaxially grow RTDs. In this fashion, we take advantage of the lower cost, volume production, and stable process of the transistor technology and yet maintain a monolithic SRAM.

The RTD-EFET SRAM can conceivably provide performance gains over present GaAs SRAMs. The standard GaAs DCFL SRAM cell uses six transistors. At its minimum, an

RTD-EFET SRAM cell will require the area of a single transistor. Since the power dissipation and access time of an SRAM are heavily influenced by addressing circuitry design, the savings in cell area will translate into shorter word and bit lines which reduce parasitic capacitance and therefore increase the speed of the memory. At the cell level, the read/write speed of the RTD-EFET SRAM cell will be determined by the propagation delay through the access transistor and the RTD storage element switching speed. If the cell takes advantage of the diode switching speed, reading from and writing to the RTD-EFET SRAM cell could be faster than for a standard DCFL SRAM cell. Finally, the static power of the RTD-EFET SRAM cell is dependent on the the I–V characteristics of the RTDs. A memory composed of low resonance voltage and low current density RTDs can possibly have a lower static power than GaAs SRAMs.

This thesis presents the design and implementation of a monolithically integrated RTD-EFET SRAM. Our design goal is to determine the best RTD for a high speed, low power, and high density integrated RTD-EFET memory that is compatible with OEICs. Because memory performance is heavily influenced by circuit layout and fabrication, we are not explicitly trying to build the fastest, smallest, and lowest power memory. We use the Epitaxy-on-Electronics (EoE) technique [19, 20] to combine RTDs with a commercial MESFET technology. EoE is a development technology which allows a researcher to focus on a heterostructure device and its role in a particular circuit or system. Because it is a development technique, EoE is not optimized for small circuit area or high-speed circuit performance. The circuits built as part of this thesis are intended as proof of concept demonstrations.

1.2 Thesis Organization

The development of an RTD-EFET memory technology can be broken down into integral parts: design of SRAM cell-compatible RTDs, demonstration of SRAM cell-compatible RTDs, and demonstration of an RTD-EFET SRAM cell. Chapters 2 and 3 review the design phase. Chapter 2 begins with a brief review of the basic operation of a RTD-EFET SRAM cell. The role of six cell design parameters are analyzed to produce a set of general design rules for a RTD-EFET SRAM. Chapter 3 introduces the EoE integration technique. RTD-EFET monolithic SRAM circuits were designed as part of a larger OEIC effort. The designs of test circuits, as well as their associated experimental purposes are reviewed. HSPICE simulations with parasitics extracted from the layout are presented for all RTD-EFET memory circuits. The chapter concludes with a brief review of features particular to the MIT-OEIC-3 IC.

Chapter 4 reviews the development of an SRAM-compatible RTD growth technology. The constraints of the EoE integration technique necessitated the development of a low temperature, relaxed-buffer RTD (RBRTD) growth technology. Section 4.1 reviews the choice of a material system for SRAM cell-compatible RTDs. Section 4.2 gives a brief introduction to relaxed buffers and Section 4.3 reviews prior work on relaxed-buffer structures. The material characterizations performed to evaluate the epitaxial quality of RBRTDs are documented in

Section 4.4. Sections 4.5 and 4.6 present the electrical characterization of RBRTDs.

Chapters 5 and 6 present the integrated RTD-EFET circuit results. Chapter 5 focuses on the evaluation of discrete devices on the integrated circuit. The epitaxial quality of material grown on the integrated circuit is presented in Section 5.1. Electrical characterization of the IC circuit components and discrete integrated RBRTDs are presented in Sections 5.2 and 5.3. Chapter 6 reviews the fabrication, Section 6.1, and operation, Section 6.2, of the integrated RTD-EFET memory.

2

RTD-EFET SRAM

This chapter documents the design of an RTD-EFET SRAM cell. It begins with a review of the operation of the memory, Section 2.1. The designer has six variables available in the design of an RTD-EFET memory: the RTD storage element supply bias, the EFET current, and the peak and valley voltages and currents of the RTDs. The following sections address the impact of each of these parameters. Section 2.2 focuses on the static power of the SRAM. Section 2.3 reviews the switching current requirements of the SRAM. Section 2.4 reviews the effects of the six parameters on the write speed of the memory. And finally, the chapter concludes with a discussion of the optimum RTD design for a RTD-EFET SRAM, Section 2.5.

2.1 Operation of an RTD-EFET SRAM

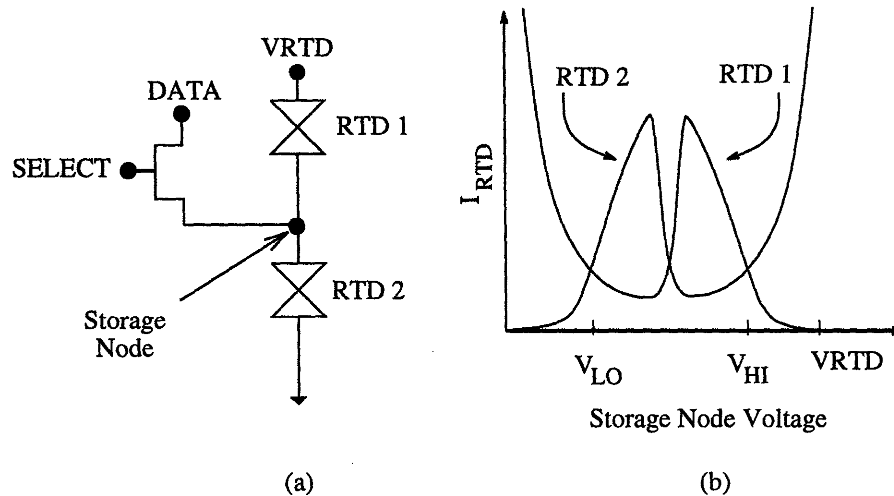


Figure 2-1: Circuit schematic of the RTD-EFET SRAM cell. (a) Schematic of the memory cell; (b) Load line graph of the RTD storage element.

The SRAM cell is composed of two RTDs and a single EFET. Figure 2-1a shows the cell architecture. The two RTDs form the storage element of the cell and the EFET provides access

to the storage node. Figure 2-1b shows the load line graph of the RTD storage element. The storage element supply voltage is V_{RTD}. The voltage at the storage node will be held at either V_{LO} or V_{HI}.

Figure 2-2 shows the activity occurring in the storage element during the WRITE HI and WRITE LO operations. This is a load line analysis where current is the variable. Thus the I–V characteristics of the RTDs move vertically with respect to each other. To write a HI to the cell, the gate of the EFET is turned on (SELECT HI) while the DATA node is high. In the load line analysis, this is represented by summing the EFET and the load RTD (RTD1) currents, resulting in a vertically shifted RTD1 load line. When writing a HI from a LO (Figure 2-2b–c), as the EFET is turned on current will flow into the storage node. The storage node will rise as the injected current charges the storage node capacitance. The exact node current and voltage will be determined by the characteristics of the two diodes, and will rise following the intersection of the load and driver RTDs. If enough current is added to the node, the only allowed operating point for the storage element/EFET system will be a high voltage operating point. The storage node will "switch", charging up to this WRITE HI voltage. When the EFET is turned off, the storage node will relax to V_{HI}. When writing a HI from a HI, the storage node will increase in voltage when the EFET is sourcing current, and relax to V_{HI} when the EFET is off.

To write a LO to the cell the EFET gate is turned on (SELECT HI) after a low voltage is established at the DATA node (Figure 2-2b–d). This can be represented in the load line analysis by offsetting the RTD2 I–V characteristic. When writing a LO from a HI, current will flow out of the storage node, discharging it. If enough current is drawn from the node, the only allowed operating voltage for the storage element/EFET system will be a low voltage. The storage node will "switch" to this WRITE LO voltage. When the EFET is turned off, the storage node will relax to V_{LO}. When writing a LO from a LO, the storage node will decrease in voltage when the EFET is sourcing current, and relax to V_{LO} when the EFET is off.

In the WRITE HI operation, the storage node serves as the source contact of the EFET. As the storage node rises in voltage, V_{GS} and V_{DS} of the EFET decrease. As the switch occurs, the amount of current that the EFET supplies to charge the node will decrease. If $V_{GS} = V_{SELECT\,HI} - V_{node} < V_{threshold}$, the EFET will turn off. If the EFET turns off before the storage node has charged to the point where the load RTD can charge the node, the storage node voltage will relax to V_{LO}. If the EFET turns off before the node has reached $V_{WRITE\,HI}$, but after the load RTD starts charging the node, the voltage at the storage node will rise to V_{HI}. The operating currents and voltages at the gate, source, and drain of the EFET, as well as the voltages V_{HI} and V_{LO} must be set such that the EFET will push the storage node high enough that the cell will switch states.

When writing a HI from a HI, the drain voltage of the EFET is the DATA voltage, the gate voltage of the EFET is the SELECT voltage, and the source voltage of the EFET is V_{HI}. If $V_{SELECT\,HI} - V_{HI} < V_{threshold}$, the EFET will not be on. If $V_{DATA\,HI} > V_{HI}$ and $V_{SELECT\,HI} - V_{HI} >$

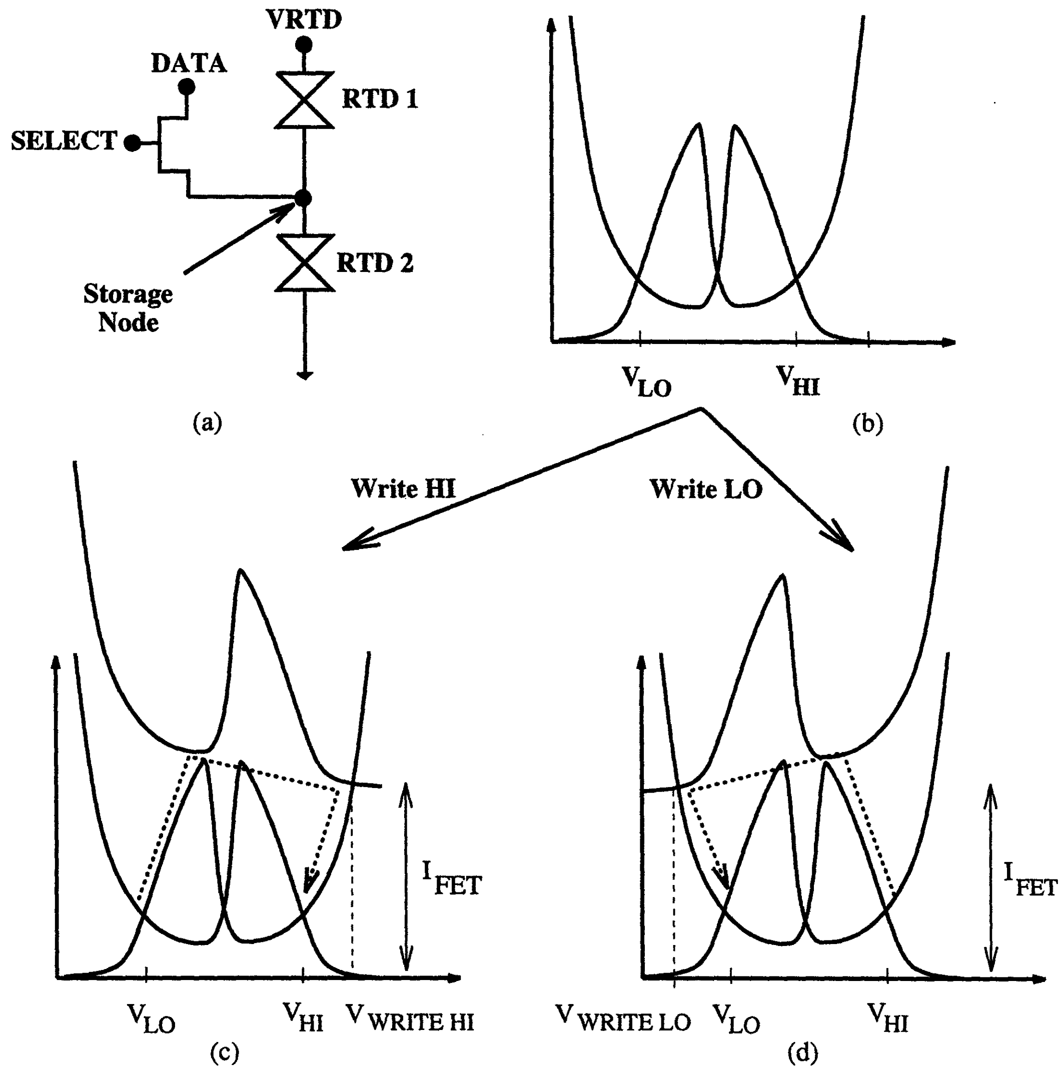


Figure 2-2: Operation of the RTD-EFET SRAM cell. (a) Cell schematic; (b)–(c) WRITE HI operation; (b)–(d) WRITE LO operation.

$V_{threshold}$, the EFET will supply current to push the storage node higher. If $V_{DATA\,HI} < V_{HI}$ and $V_{SELECT\,HI}$ - $V_{DATA\,HI} > V_{threshold}$, the EFET will draw current, pulling down the storage node voltage. To maintain a high state under these conditions, the EFET must not pull enough current to reach a situation where the driver RTD can discharge the node. In situations where the DATA and source node voltages are greater than the select voltages, the gate/source diode of the EFET will be reverse biased, and will draw gate current.

When writing a LO from a HI, V_{HI} is the drain voltage, the SELECT voltage is the gate voltage, and the DATA is the source voltage. The EFET is turned on by the difference between the data and select lines. The initial V_{DS} equals V_{HI} - $V_{DATA\,LO}$, and will draw current from the node. As the node voltage drops, V_{DS} of the EFET will drop, and thus the current pulled

by the EFET will decrease. V_{GS} is established by the SELECT and DATA lines, and thus will remain constant. The EFET current will decrease as the EFET moves from the saturation to linear regimes. However, the EFET will not automatically shut off because its gate will remain higher in voltage than its source and drain. The EFET must sink enough current for the storage node to discharge to a point where the driver RTD (RTD2) can discharge the node. Otherwise, the storage node will charge to V_{HI} when the EFET is turned off. Once again, the operating currents and voltages at the gate, source, and drain of the EFET, as well as the voltages V_{HI} and V_{LO} must be set such that the EFET will push the storage node low enough that the cell will switch states. Because the EFET is always on, this is the less stringent of the writing conditions. However, the voltages should be chosen so that the EFET is operating in the saturation regime for the critical part of the switch.

When writing a LO from a LO, V_{LO} is the drain voltage of the EFET, the SELECT voltage is the gate voltage, and the DATA voltage is the source voltage. Current will flow to equalize the voltages at the source and drain of the EFET. If $V_{\mathrm{DATA\,LO}} < V_{\mathrm{LO}}$, the storage node will be pulled lower in voltage. If $V_{\mathrm{DATA\,LO}} > V_{\mathrm{LO}}$, the storage node will rise to $V_{\mathrm{DATA\,LO}}$. In this case, the EFET must not source enough current for the load RTD to be able to charge the node, or the state of the memory will switch HI.

The choice between the read and write operations will be made in the access circuitry of the cell. To read the contents of the memory, the SELECT line will be activated and the DATA line will be left floating. Current will flow from the storage node to charge or discharge the DATA node, forcing the voltage at this node to change to reflect the voltage at the storage node. During the READ operations, the voltage at the storage node will be affected as the node provides current to charge the SELECT and DATA lines. If a HI is read, current will flow from the storage node to charge the READ DATA node. In a load line analysis, this operation is the same as writing a LO. The voltage at the storage node will decrease as the load RTD provides current to charge the READ DATA node. The READ operation will be destructive if enough current is drawn from the storage node such that the only allowed operating point for the storage element is a low voltage. This maximum current is the minimum current necessary to write a LO to the cell. As the voltage on the READ DATA node approaches that of the storage node, the EFET will possibly shut off, depending on the exact SELECT and storage node voltages. To read a LO, the voltage at the READ DATA node will be discharged through the READ EFET and the driver RTD. To prevent a destructive READ, the current sourced by the READ EFET cannot result in a single, high-voltage operating point for the storage element. This maximum current is the minimum current necessary to write a HI to the cell. Because the drain and source of the READ EFET are low while the gate is high, the READ EFET will possibly sink gate current during the read operation. In both the read LO and HI cases, the amount of current flowing to charge or discharge the DATA node will decrease as the node approaches the storage node voltage.

In a practical application of the memory, the READ DATA node will be the word line for a

particular column in the memory array. During the read operation, the storage node will be seeing the capacitance of the entire word line of the memory. The capacitances of the access lines must be such that the charge drained from the storage node does not flip the state of the cell. Large capacitances will slow the speed of the read operation. To reduce the chance of a destructive read and to increase the speed of the READ operation, the READ DATA node (word line) can be precharged to a voltage halfway between V_{LO} and V_{HI}. If the voltage at the storage node were to actually reach this voltage, a destructive READ could occur. However, precharging the READ DATA line will actually reduce the amount of current necessary to charge or discharge the READ DATA node. The smaller V_{DS} present on the READ EFET will reduce the current sunk or sourced by the storage node, reducing the voltage change at the node. Since the storage node acts as a source or a drain depending on the value being read, the read HI and read LO operations will have different speed, with the read HI being the slower of the two operations. The precharge voltage can be adjusted to make the read operations symmetric.

2.2 Static Power of an RTD-EFET SRAM

The static power of the SRAM cell is the product of the bias voltage of the RTD storage element and the static current of the individual states, either V_{LO} or V_{HI}. There is a finite range of bias voltages for which the diode chain will be bistable. Figure 2-3 shows schematically the different bias situations resulting in single, double, and triple operating points. For low bias voltages, Figure 2-3a, the operating point of the diode chain will occur where the pre-resonance rising legs of both diodes intersect. At a certain voltage, the valley of the load (driver) device will intersect the rising edge of the driver (load) device. For asymmetric diodes, i.e., where the load and driver have different I–V characteristics, the two events will not occur at the same voltage. Bistability occurs when either or both of these intersections occur, but the desired condition for a memory cells happens when both intersections exist, Figure 2-3b. For biases beyond the bistability range, the operating point will occur at the intersection of the post-resonance rising leg of both diodes, Figure 2-3c. For some diodes, three stable intersections can occur, Figure 2-3d. This is an undesirable situation because the middle voltage state is stable, and can be switched into. Figure 2-4 shows the measured voltage bistability range of a relaxed-buffer RTD (RBRTD) storage element.

The range of bistability is related to the peak and valley voltages and currents of the RTD. The peak and valley voltages and currents of the RTDs are V_P, V_V, I_P, and I_V, respectively and are shown in Figure 2-3c. (The peak and valley current densities of the RTD are J_P and J_V, respectively.) For bistable operation, the minimum bias voltage is twice the maximum of the peak voltages of the two RTDs in the storage element, $V_{P,max}$. For a given peak-to-valley voltage ratio, a diode with a lower valley current will also extend this range because the valley of the load (driver) device will overlap the rising edge of the driver (load) device for a larger supply

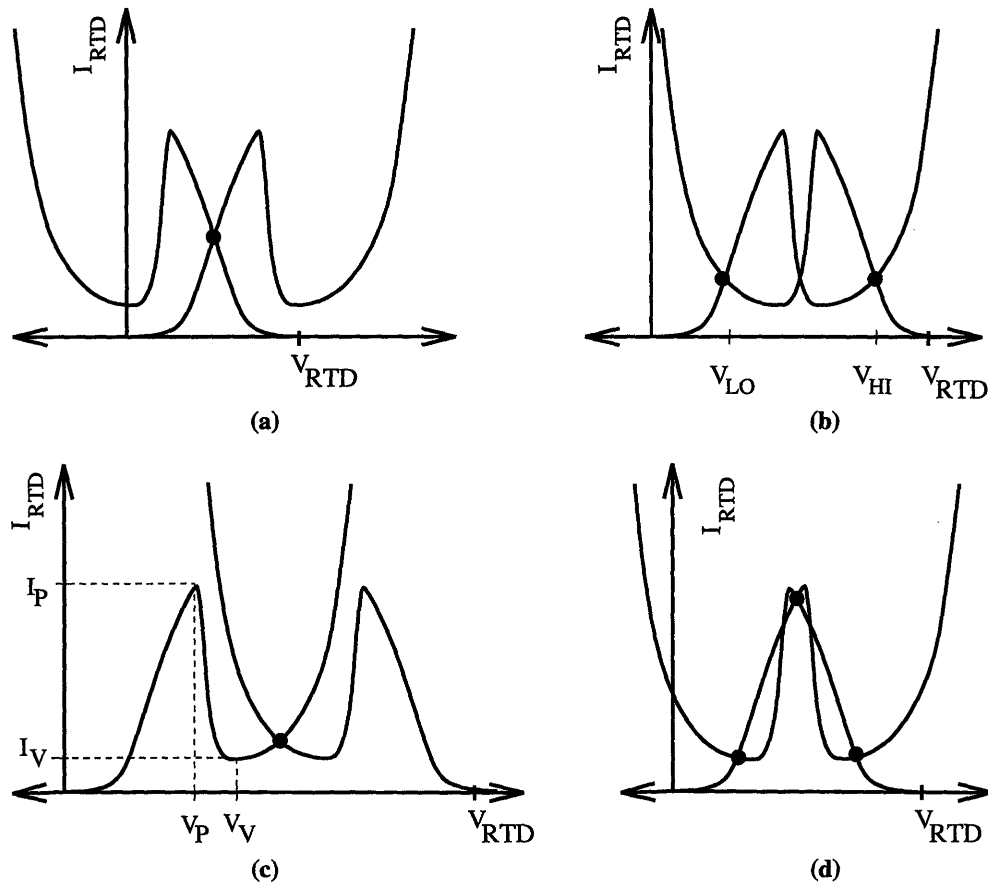


Figure 2-3: Load line characteristics as a function of V_{RTD}: (a) V_{RTD} below bistability range; (b) V_{RTD} in bistability range; (c) V_{RTD} beyond bistability range; (d) V_{RTD} resulting in tristable situation. Stable operating points are marked with filled circles. V_P, V_V, I_P, and I_V are marked in (c).

voltage. The static current of both V_{LO} and V_{HI} will increase with increasing bias voltage. For asymmetric diodes, the currents of these two states will be different. The dependence of the static current will be proportional to the post-resonance valley current. The lower the valley current of the devices, the lower the static power of the cell will be. In addition, a broad, low-current valley is desirable to accommodate variations in RTD peak and valley voltages without substantially varying the static power across an array of diodes.

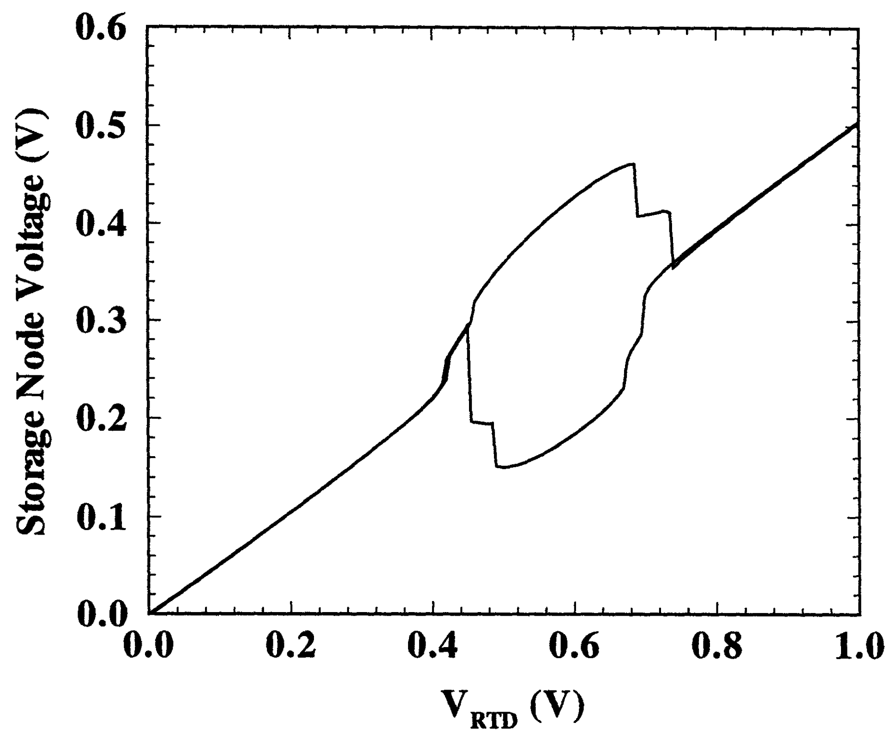


Figure 2-4: Measured voltage bistability of an RBRTD storage element. The device areas are 25 μm^2 and $V_{P,max}$ is 0.344 V.

2.3 Switching Current of an RTD-EFET SRAM

Figure 2-5 shows the measured minimum required switching current, $I_{switch,min}$, for an RTD storage element. This is the current that an EFET must supply to write a HI or LO to this storage element. For biases below 1.1 V, the RTD storage element is in a region of tristability. For completeness, a description of the minimum required current to switch the chain is included. However, this is not a preferred region of operation for the memory.

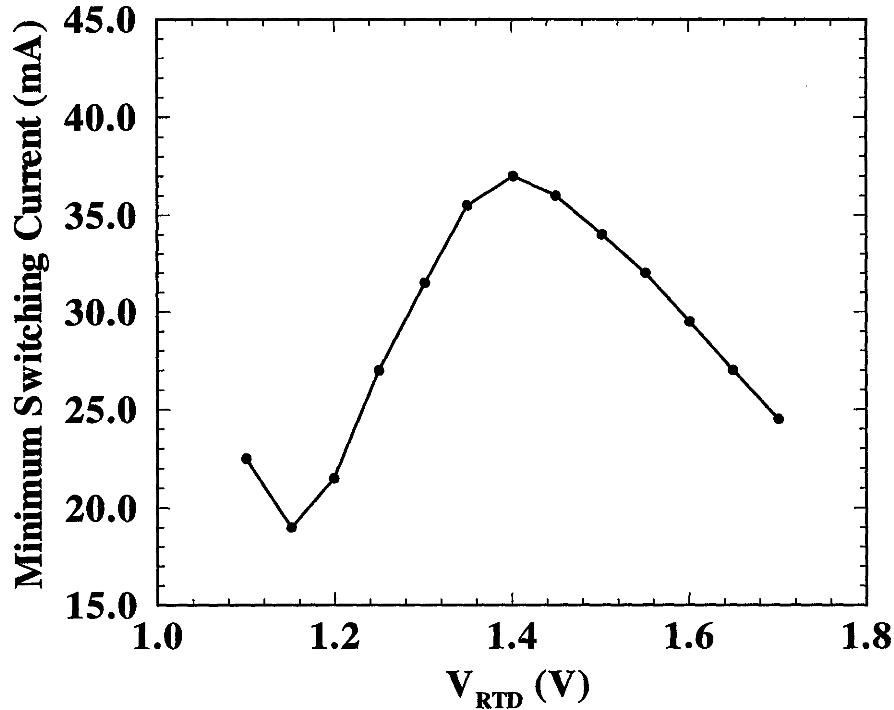


Figure 2-5: Measured $I_{switch,min}$ requirements for a pseudomorphic RTD storage element with device areas of 100 μm^2 and a maximum peak current density of 9.09 kA/cm^2.

For bias voltages $V_P < V_{RTD} < 2V_P$, the memory element is in a region of tristability. In this situation, shown in Figure 2-6a, there are 4 currents to consider. When switching from LO to HI, currents b and c set the minimum, and when switching from HI to LO, currents a and d set the minimum. For biases in this range, current must be added (subtracted) from the storage node such that the sum of the added (subtracted) current and the valley current of the load (driver) no longer intersects the pre-resonance rising leg of the driver (load), and the peak current of the driver (load) is less than the sum of the injected (subtracted) current and the pre-resonance rising leg of the load (driver). In the case of symmetric RTDs, $I_{switch,min}$ will occur at the bias where $b = c$ and $a = d$. For asymmetric diodes, the minimum current will be the maximum of the two. Because there is a stable middle storage node voltage for this bias

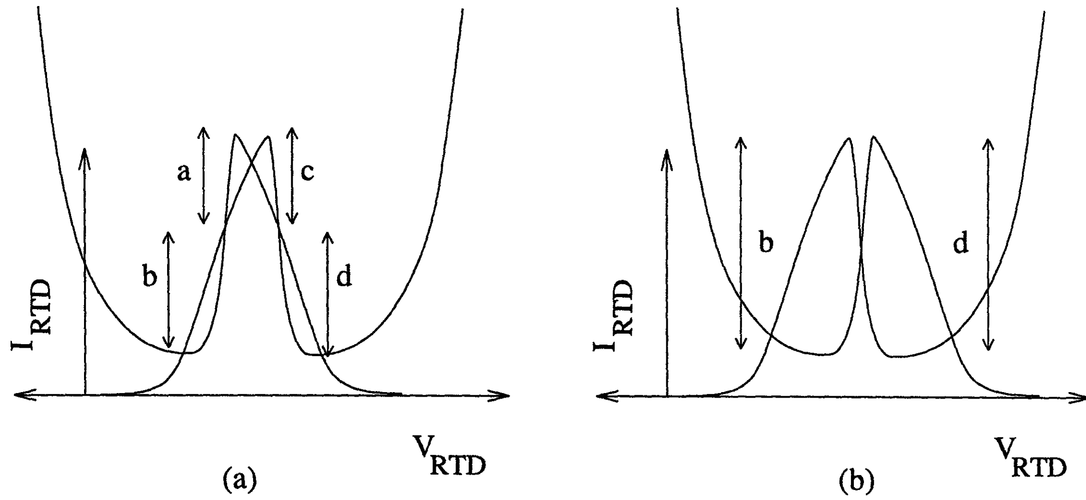


Figure 2-6: Schematics showing $I_{switch,min}$ (a) in tristable region (b) in bistable region.

range, however, the $I_{switch,min}$ is not practical for a memory cell.

For biases $V_{RTD} > 2V_{P,max}$, Figure 2-6b, currents *b* and *d* establish the switching current requirement. The maximum $I_{switch,min}$ needed, in magnitude, will be $(I_P - I_V)_{max}$. To change the state of the memory, the EFET must be able to supply this magnitude of current. For a given EFET, designing the memory to require lower switching current will result in a cell with higher static power. When switching the cell, the EFET is doing the initial charging of the storage node. For a given V_{RTD}, the more current beyond $I_{switch,min}$ that the EFET can supply, the faster the switch will be.

V_{GS} and V_{DS} of the EFET will change during the write operations. Care must be taken that the EFET design accounts for the reduction in current. Specifically, the EFET must be large enough to supply at least $I_{switch,min}$ as long as there are two stable operating points for the storage element. (Another way to think of this, described in Section 2.4, is that the EFET must supply current as long as the storage node voltage is in a range where the RTDs cannot push the switch. For symmetric RTDs, this voltage will be $V_{RTD}/2$.) To account for the reduction in current, the EFET will have to be "oversized."

2.4 Switching Speed of an RTD-EFET SRAM

Most of the investigations in the literature of tunnel-diode switching speed have focused on the use of diodes in logic circuits, initially using Esaki tunnel diodes and later RTDs. Many investigations specifically looked at the time necessary for a diode to switch from its peak to valley voltage and vice versa [21, 22, 23]. In all cases, the speed of the diode voltage switch was determined by the ability of the diode to charge its depletion capacitor. Likewise, the speed of the memory cell will be determined by the ability of the EFET and the RTDs to charge and discharge the storage node capacitance. The major differences are that the voltage switch

happens over a much greater voltage region than the previous investigations, the load is no longer a simple resistor, and the node capacitance includes that of an additional RTD and an EFET. This section focuses on the effects various RTD-EFET SRAM cell parameters have on the switching speed.

2.4.1 SRAM Model Description

Figure 2-7 shows the evolution of the RTD SRAM model. Equations 2.1– 2.3 describe the dynamics of the memory cell:

$$I_{RTD1} + C_{RTD1}\frac{dV_{RTD1}}{dt} + I_{EFET}(V_{GS}, V_{GD}) = I_{RTD2} + C_{RTD2}\frac{dV_{RTD2}}{dt} + C_S\frac{dV_{RTD2}}{dt} \quad (2.1)$$

where I_{RTD} is the current in an RTD and C_{RTD} is the RTD capacitance. The capacitance of the EFET source contact is C_S. Writing V_{RTD1} in terms of V_{RTD2} and combining terms gives

$$\frac{dV_{RTD1}}{dt} = \frac{dV_{RTD}}{dt} - \frac{dV_{RTD2}}{dt} = -\frac{dV_{RTD2}}{dt} \quad (2.2)$$

$$I_{RTD1} - I_{RTD2} + I_{EFET}(V_{GS}, V_{GD}) = [C_{RTD1} + C_{RTD2} + C_S]\,\frac{dV_{RTD2}}{dt} \quad (2.3)$$

The EFET source node capacitance can be combined with the capacitances of the two RTDs to form the storage node capacitance, C_{node}. Recognizing that V_{RTD2} is the storage node voltage yields

$$I_{RTD1} - I_{RTD2} + I_{EFET}(V_{GS}, V_{GD}) = C_{node}\frac{dV_{node}}{dt}. \quad (2.4)$$

To analytically solve for the storage node voltage as a function of time, Equation 2.5 is solved for the piecewise-linear regions of the switch and the switching times for each region are then summed to calculate the total switching time.

$$t = \int dt = \int \frac{C_{node}\, dV_{node}}{I_{RTD1} - I_{RTD2} + I_{EFET}} \quad (2.5)$$

For a complete listing of the analytical solutions to Equation 2.5 the reader is referred to Appendix A. Because the intent of this model is to focus on the role of the RTD in the memory, further assumptions are made:

- The RTDs used are symmetric with respect to voltage.
- Load and driver RTDs are identical. The pre-resonance conductance of the RTDs is G_1 and the post-resonance conductance of the RTDs is G_2.
- The RTD negative differential resistance (NDR) region is modeled as a finite, linear resistor with conductance G_{N}.
- All capacitances are constant as a function of voltage.

- To simulate the EFET turning off during the switch, the EFET current is modeled as constant for $V_{node} < V_{RTD} - V_P$. This will only simulate the slowest of the write actions: WRITE HI when the EFET cuts off. The current is actually on longer than the minimum time (t_{min} occurs when $V_{node} = V_{RTD}/2$), but is assumed to be zero for $t > t_{min}$ for simplicity and to account for noise margins for the switch.

- $V_{RTD} \geq 2V_P$ to insure that there is no stable middle voltage node.

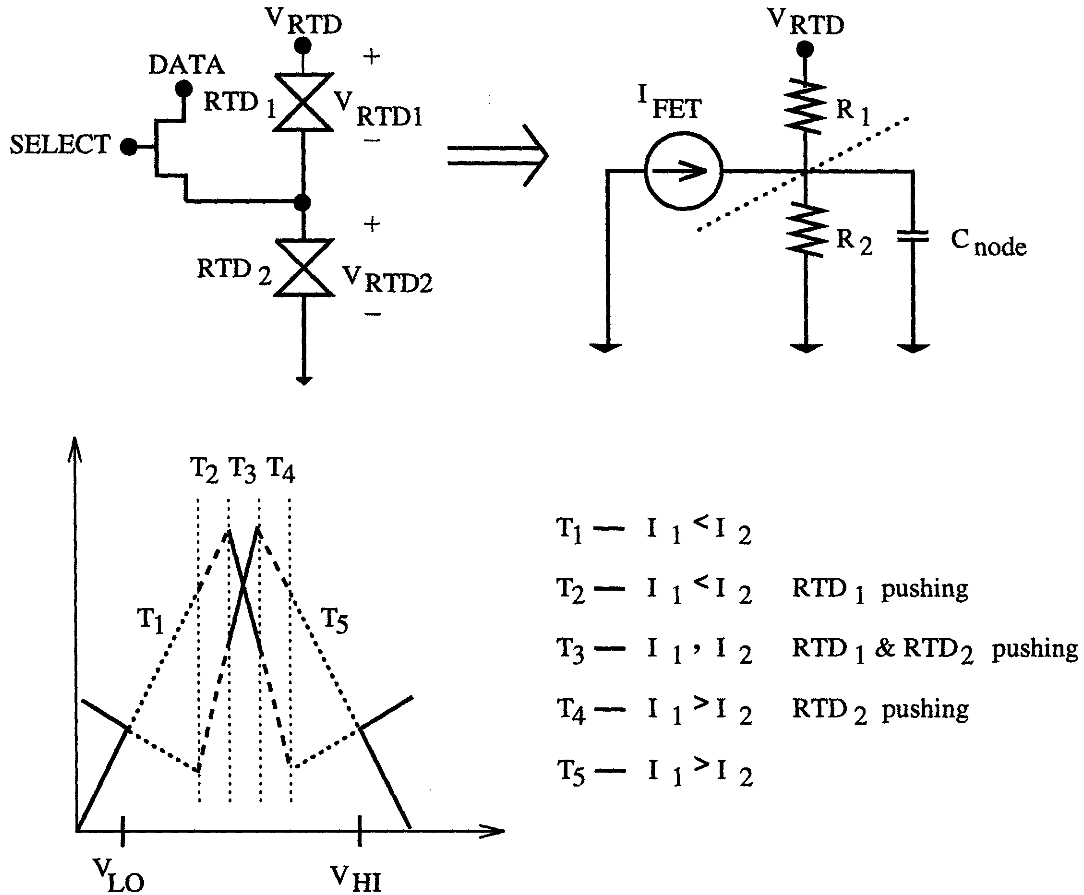


Figure 2-7: Evolution of the RTD-EFET SRAM switching model. The circuit elements are reduced and combined to form a simplified circuit architecture. Current and voltage continuity at the storage node are used to describe the action of the cell. The transition from V_{LO} to V_{HI} is broken into 5 regions. Case 2, $V_{RTD} > 2V_P$ and $V_{RTD} < V_P + V_V$, is shown in this figure.

Four different bias cases are considered:

- Case 1: $V_{RTD} = 2V_P$

- Case 2: $V_{RTD} > 2V_P$ and $V_{RTD} < V_P + V_V$

- Case 3: $V_{RTD} > 2V_P$, $V_{RTD} > V_P + V_V$ and $V_{RTD} < 2V_V$

- Case 4: $V_{RTD} > 2V_P$ and $V_{RTD} > 2V_V$

For Cases 2 to 4, there are 5 distinct regions in the voltage switch. For Case 1, there are four distinct regions.

Region 1: Current is being supplied to the storage node via the EFET and the load RTD. Without the added EFET current, the load RTD cannot charge the storage node. For all cases, as the voltage at the storage node rises, the current injected into the storage node decreases because the load RTD is pushed closer to its valley. This is a standard RC charging situation where $\tau_1 = C_{node}/(G_1 + G_2)$. As the storage node rises in voltage, it becomes harder to charge the storage node.

Region 2: Current is being supplied to the storage node via the EFET and the load RTD. Without the added EFET current, the load RTD cannot source the current to charge the storage node. For Cases 1 and 2, as the voltage at the storage node rises, the current injected into the storage node increases because the load RTD is pushed through its NDR region towards its peak. For these cases, $\tau_2 = C_{node}/(G_1 + G_N)$, and the load RTD is pushing the storage node higher in voltage. For Cases 3 and 4, as the voltage at the storage node increases, the current demand of the driver RTD decreases because it is being pushed through its NDR region. Simultaneously, the current supplied by the load RTD is decreasing as it is pushed towards its valley. In these cases, $\tau_2 = C_{node}/(G_2 + G_N)$, and the voltage at the storage node is pushed higher by the driver RTD.

Region 3: This region is specific to Cases 2 to 4. Current is being supplied to the storage node via the EFET and the load RTD. When $V_{node} < V_{RTD}/2$, the load RTD cannot source the current to charge the storage node without the added EFET current. However for $V_{node} > V_{RTD}/2$, the load RTD sources more current than the driver RTD demands. Here, $\tau_3 = C_{node}/2G_N$. Both RTDs are in their respective NDR regions and both push the storage node higher in voltage. As the storage node voltage rises, the load RTD supplies, and the driver RTD demands, less current. This allows more charge to build up on the storage node capacitor, forcing the storage node even higher.

Region 4: The model assumes that the EFET has been turned off in this region. For Cases 1 and 2, the load RTD sources more current than the driver RTD demands. The driver RTD is in its NDR region, and as the storage node voltage increases, the driver RTD will demand progressively less current. Though the load RTD will supply decreasing amounts of current with the increasing storage node voltage, its rate of decline is much less than the driver RTD demand decline, and thus "surplus" current will be available to charge the storage node. For these cases, $\tau_4 = C_{node}/(G_1 + G_N)$, and the driver RTD is pushing the storage node. For Cases 3 and 4, the load RTD is supplying increasing amounts of current as it is pushed through its NDR region and the driver RTD is demanding increasing amounts of current as it is pushed beyond it valley. The rate of increase in the load current supply will exceed the driver demand increase, and once again, "surplus" current will be available to charge the storage node. For these cases, $\tau_4 = C_{node}/(G_2 + G_N)$, and the load RTD is pushing the storage node.

Region 5: For all cases, in this region the load RTD current supply is decreasing and the driver RTD current demand is increasing, but the load supply is always greater than or equal to the driver demand. Because the load is supplying more current than the driver demands, the storage node will rise, but neither diode is driving the storage node because as the the voltage rises, less current is available to charge the storage node capacitance. In this region, $\tau_5 = C_{\text{node}}/(G_1 + G_2)$, and it once again looks like a standard RC charging problem.

For the following discussions, the RTD and EFET are based on devices that experimentally have been fabricated and integrated. This "reference" RTD has a peak voltage of 0.2888 V, a valley voltage of 0.4195 V, a peak current density of 1.01 kA/cm^2, and a peak-to-valley current ratio, PVCR, of 2.3:1. The diode area is 25 μm^2. Using a parallel plate assumption, the depletion capacitance of the RTD is calculated to be 10 fF. The EFET used in the integration was 10×1.2 μm. Its source node capacitance, 20 fF, was calculated using capacitance per unit area numbers supplied by Vitesse as part of their HSPICE models. Interconnect capacitances are included by increasing the source node capacitance. Series resistances in the RTDs are not included. This particular RTD-EFET combination was chosen to correspond to an experimental demonstration present later in the thesis. However, the results are general in nature, and the effects of changes in RTD and EFET size will be discussed for each analysis.

2.4.2 Effects of PVCR

To assess the effect of changing the PVCR of the RTDs on the switching time, the valley current of the RTD was decreased and the peak current of the RTD was held constant. Figure 2-8 shows the effect of changing the PVCR on the 10–90 rise time to write a HI and on the cell static power, both as a function of bias voltage. In this calculation, interconnect capacitances are ignored. G_1 and G_2 are obtained from the reference diode, and are held constant as I_V, and hence G_N are changed. For these calculations the switching current was 0.4 mA.

For a given V_{RTD}, the variation of PVCR has different effects. Consider first the case V_{RTD}= 0.6 V. As the PVCR increases the amount of current the load RTD contributes (the dotted line in Figure 2-9a and b) in the initial part of the switch decreases. Therefore, the time spent in regions T_1 and T_2 of the switch increases. However, since the EFET is the dominant current source in these regions of the switch, the effects of the PVCR changes are not significant. For situations where $|G_N| \approx G_1$ and $I_{\text{RTD1}} \approx I_{\text{RTD2}}$, the driver RTD is sinking most of the current available to charge the node. As the PVCR is increased, the corresponding reduction in I_V increases $|G_N|$, and thus the RTDs drive the switch harder. In the latter half of the switch, increased PVCR leads a decrease in the time spent in regions T_4 and T_5. The reduction in switching time is due to an increase in the difference between supply and demand current. The extra charge is dumped on the capacitor. The reduction in time spent in regions T_4 and T_5 outweighs the increase in regions T_1 and T_2, and thus the overall switching time is reduced.

As the PVCR gets increasingly bigger, the effects of the increase in PVCR become less

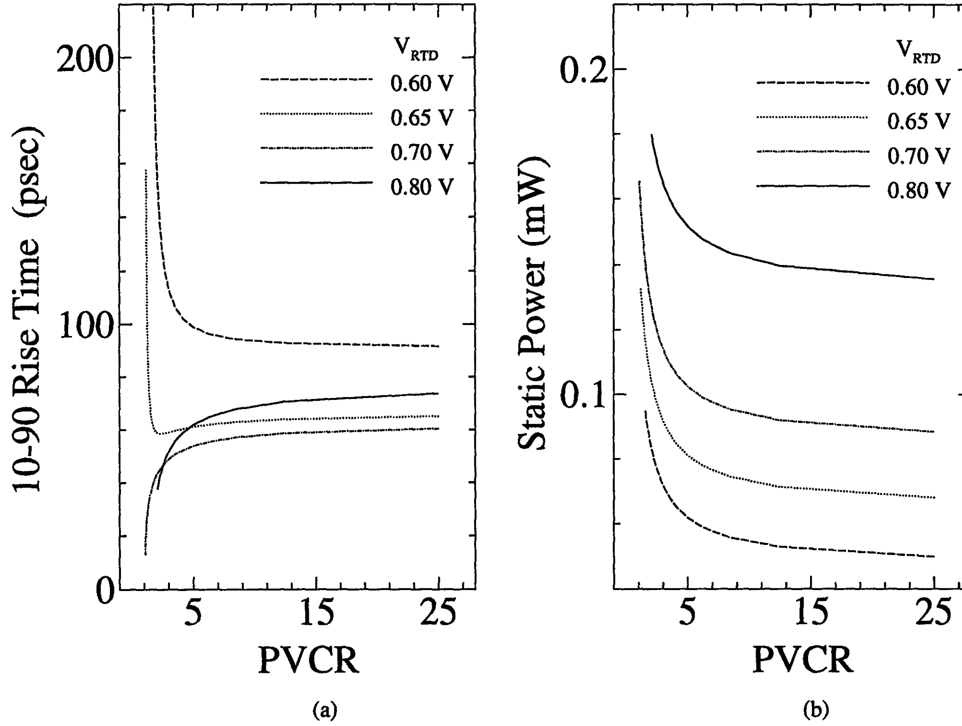


Figure 2-8: Effects of changing RTD PVCR on (a) 10-90 switching time and (b) cell static power as a function of V_{RTD} with constant current density.

substantial. This can been seen in the time constants of the switch. For regions T_2 and T_4, $\tau = C_{node}/(G_1 + G_N)$. For $|G_N| \gg G_1$, $\tau = C_{node}/G_N$. The minimum required switching current that must be supplied by the EFET will increase with PVCR, but for this bias case the required current is still far below that being supplied by the EFET. Thus, the switching time continues to slowly decrease with increased PVCR.

For $V_{RTD} = 0.7$ V, the ratio of supply/demand current decreases in regions T_1 and T_2 and increases in regions T_4 and T_5. However, this bias has the highest $I_{switch,min}$ of those considered. As the PVCR increases, $I_{switch,min}$ also increases. The "surplus" current left to charge the node decreases, and thus the speed of the overall switch decreases. Once again, for $|G_N| \gg G_1$, $\tau = C_{node}/G_N$. In this case the effects of the increase in minimum switching current required outweigh the effects of a larger $|G_N|$, and the speed slowly continues to decrease. For $V_{RTD} = 0.8$ V, the dependence on PVCR is the same as that for $V_{RTD} = 0.7$ V. $V_{RTD} = 0.7$ V has the greatest surplus current, and therefore is the fastest bias case.

Across a memory array, there will be variations in RTD J_P, J_V, V_P, and V_V. This set of parameters explicitly accounts for the current variations. Variations in RTD voltages can be represented by assuming a spread of V_{RTD}. It is desirable to design in tolerance for these variations. Of the two SRAM figures of merit considered here, it is preferable to have the variations

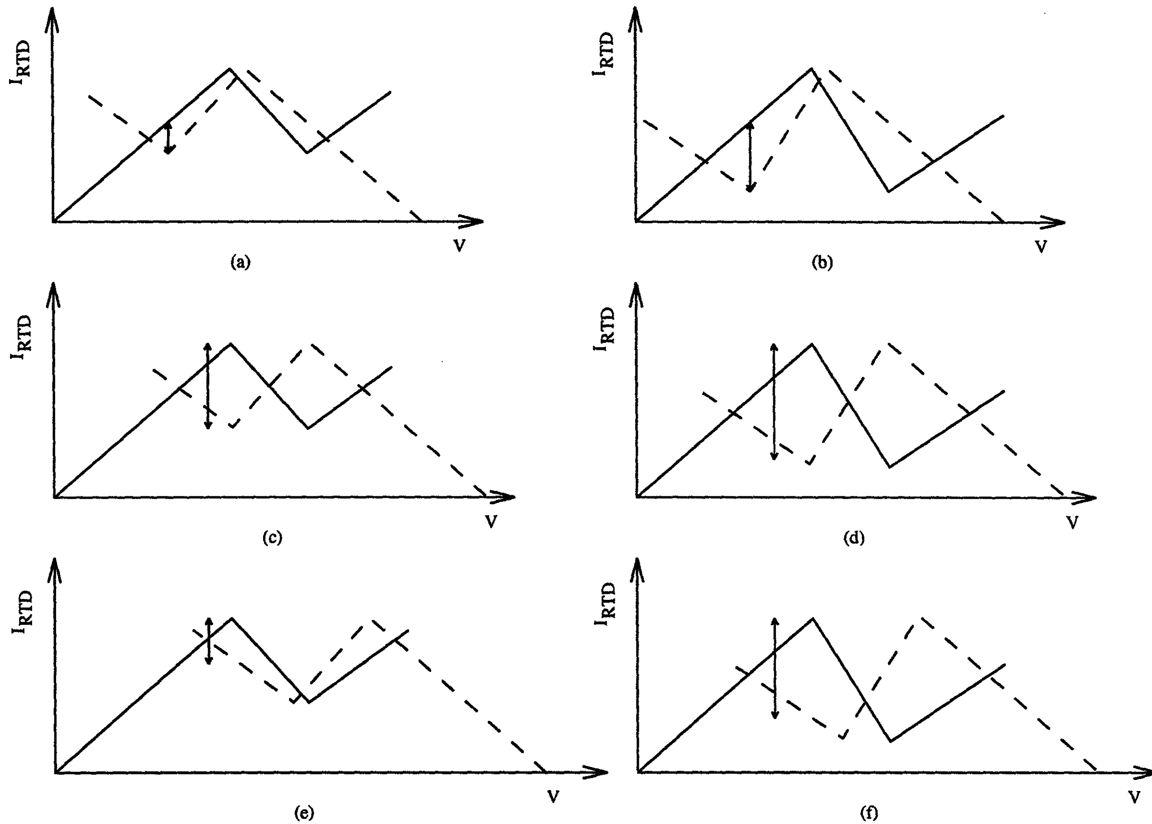


Figure 2-9: Storage element load lines as a function of V_{RTD} and PVCR: (a) V_{RTD} = 0.6 V, low PVCR; (b) V_{RTD} = 0.6 V, high PVCR; (c) V_{RTD} = 0.7 V, low PVCR; (d) V_{RTD} = 0.7 V, high PVCR; (e) V_{RTD} = 0.8 V, low PVCR; (f) V_{RTD} = 0.8 V, high PVCR. In each situation, the minimum required switching current is indicated with an arrow.

in RTD characteristics manifest themselves as variations in the static power dissipated in a cell. In addition, one would like to maintain a low static power. Both of these constraints can be satisfied by designing RTDs with high PVCR. High is a relative term. Exactly how high the PVCR should be will be determined by the EFET. The PVCR cannot result in a $I_{switch,min}$ that is beyond the capacity of the EFET. In this example, because this EFET can supply enough current to switch this RTD storage element regardless of RTD PVCR, a design with a very high PVCR, 25:1, should be used to minimize static power. In addition, the RTDs should be designed such that the $V_P + V_V \approx V_{RTD}$, where V_{RTD} is the supply bias of the storage element.

For a given EFET size, reduction in RTD area will decrease the storage node capacitance and increase the surplus current supplied by the EFET to charge to storage node. These factors will lead to an increase in switching speed. Reduction of EFET size for a given RTD size will decrease the storage node capacitance. However, the resulting gains in speed will be offset by the reduction in the current sourcing capability of the EFET, which will reduce the speed.

2.4.3 Effects of Current Density

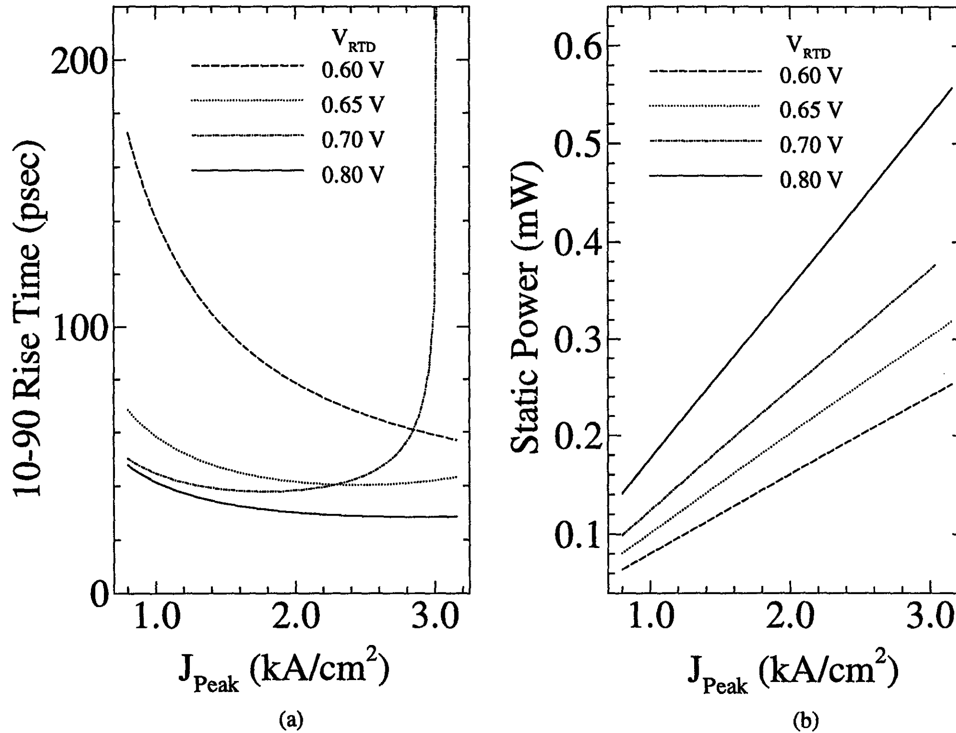


Figure 2-10: Effects of RTD current density on (a) 10-90 switching time and (b) cell static power as a function of V_{RTD} and with constant PVCR.

To assess the effect of changing the current density of the RTD, the PVCR was held constant (at the reference RTD PVCR) while the peak and valley currents were changed. The performance of the cell was again evaluated at a number of RTD bias voltages. In this study, G_1, G_N, and G_2 all are changing.

Figures 2-10 and 2-11 show the performance of the cell and the load line characteristics of the memory element, respectively. The performance effects of varying the current density are similar to those of varying the PVCR. For V_{RTD} = 0.6 V, as current density increases the difference between the demand and supply currents increases. For regions T_1 and T_2, there is an increasing deficit of current which must be supplied by the EFET. Because the EFET is supplying well beyond the $I_{switch,min}$, the effects of the reduced supply current are not substantial. In regions T_4 and T_5 there is an increase in the surplus current available to charge the storage node, and the time spent in these regions of the switch is reduced. This effect is stronger than the time increase in regions T_1 and T_2, and thus the overall switching time will be reduced as the current density of the RTDs is increased.

For V_{RTD} = 0.7 V the same increase in T_1 and T_2 and decrease in T_4 and T_5 occur. However, for this bias voltage, as the current density increases the minimum switching current increases

to values close to that supplied by the EFET. For higher current densities, there is less surplus current to charge the storage node. This effect is the dominant one and therefore there is an increase in the overall switching time as the RTD current density increases.

Two factors contribute to the overall speed of $V_{RTD} = 0.8$ V: very little switching current is necessary for all current densities, and the majority of the switch occurs over regions where one of the RTDs is pushing the switch forward. The same general trends apply with respect to increasing current density, and thus the speed of the switch increases for higher current density devices.

As expected, the static power dissipated in a cell increases with increasing bias voltage. In addition, the static power increases with increasing current density. This is primarily due to the increase in valley current density. Switching speeds are overall faster than for the previous

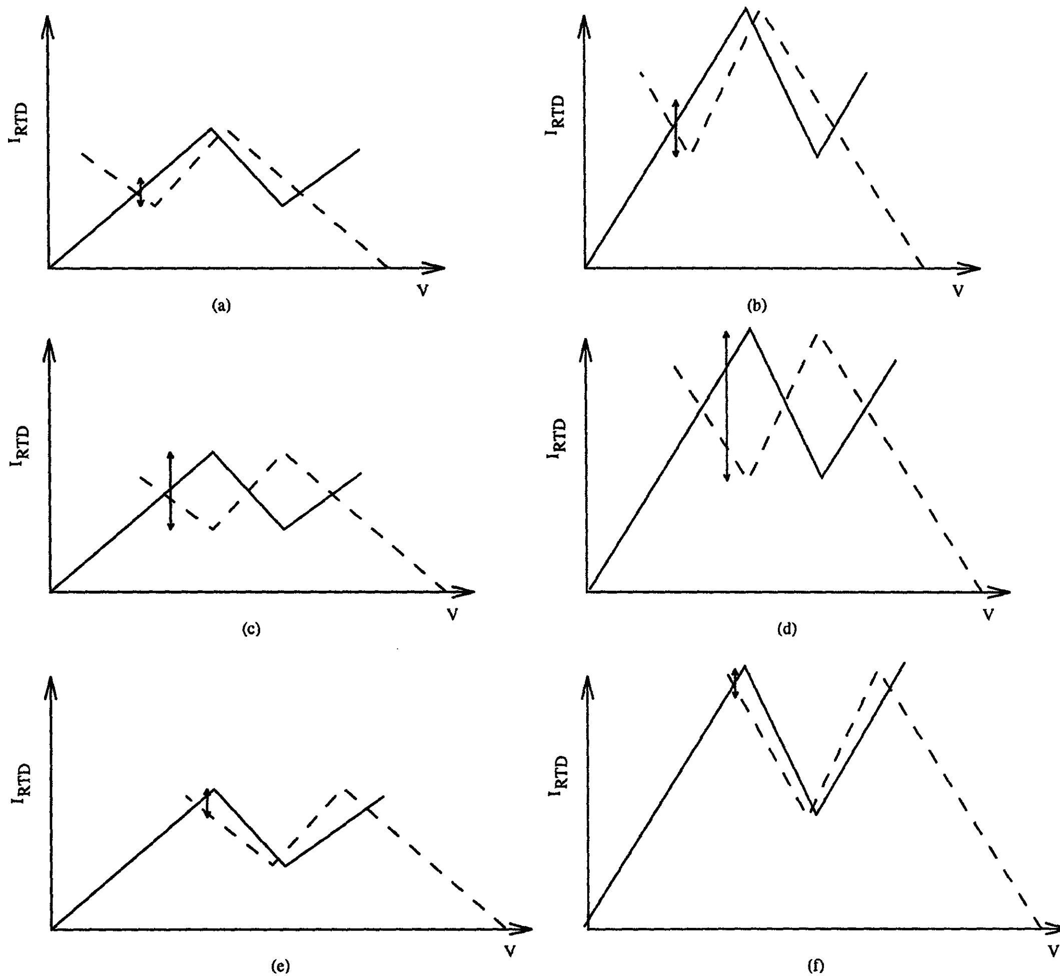


Figure 2-11: Storage element load lines as a function of V_{RTD} and current density (CD): (a) $V_{RTD} = 0.6$ V, low CD; (b) $V_{RTD} = 0.6$ V, high CD; (c) $V_{RTD} = 0.7$ V, low CD; (d) $V_{RTD} = 0.7$ V, high CD; (e) $V_{RTD} = 0.8$ V, low CD; (f) $V_{RTD} = 0.8$ V, high CD. In each situation, the minimum required switching current is indicated with an arrow.

case because more current is available to charge the storage node.

To design for robustness, once again, the RTD current density should be such that changes in current density and supply voltage have a minimal effect on the 10–90 rise time of the cell. The RTDs should be designed such that the bias voltage is greater than $V_P + V_V$ to accommodate variations in current density. In addition, for this EFET, current densities in the 1–2 kA/cm^2 range are preferable.

The general area trade-offs are the same as for the previous analysis. Reductions in RTD area for a given EFET will increase the speed of the switch. Reduction in EFET size for a given RTD area will lead to a reduction in the cell switching speed.

2.4.4 Combined Effects of PVCR and Current Density

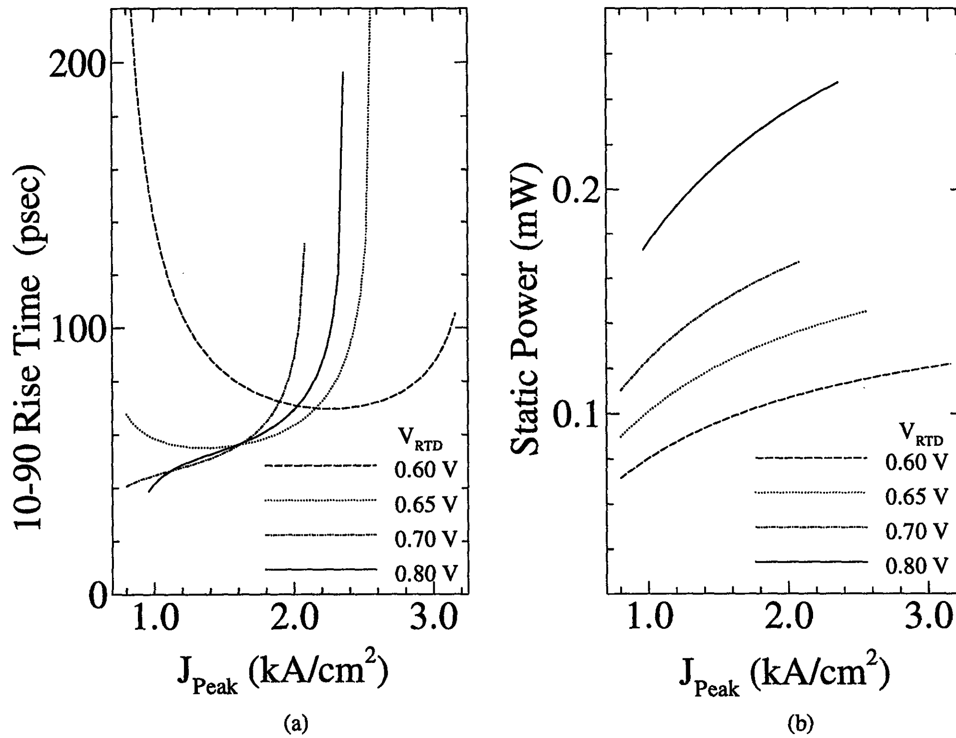


Figure 2-12: Effects of RTD peak current density and associated PVCR on (a) 10–90 switching time and (b) cell static power as a function of V_{RTD} for constant J_V.

The previous two analyses demonstrate the low power advantages of high PVCR and the speed advantages of higher current density. By designing RTDs with thin, wide-bandgap barriers, it may be possible to combine these advantages. Thus, a study of the combined effects of PVCR and current density was performed. The valley current of the RTD was held constant and the peak current of the RTD was increased. As the peak current density increases, there is an associated increase in the PVCR of the RTD. In this study, G_1 and G_N change, but G_2 is

held constant.

Figure 2-12 shows the performance as the RTD peak current density and associated PVCR are increased. For all bias voltages, the trends follow those established in the previous two analyses. At low current densities, where the EFET is providing more than enough switching current, the increase in surplus current with increased V_{RTD} in regions T_4 and T_5 increases the speed of the switch. For high current densities, the speed is limited by the lack of switching current being supplied by the EFET.

Combining increased current density and PVCR actually improves the tolerance of the cell. For $J_P = 1.6$ kA/cm^2, the cell can handle a 0.15 V variation in V_{RTD} without changing the 10–90 rise time of the cell. For J_P = 1–2 kA/cm^2 and PVCR = 2.3–4.5, the EFET is still supplying enough switching current. In this range, the speed of the cell is somewhat slower than the case of varying current density only. However, for higher V_{RTD} there is approximately a 1/3 reduction in power. For this same current range, increasing the PVCR by reducing the valley current will produce lower static current. Manipulation of the valley current substantially reduces the tolerance of the cell to RTD parameter variations.

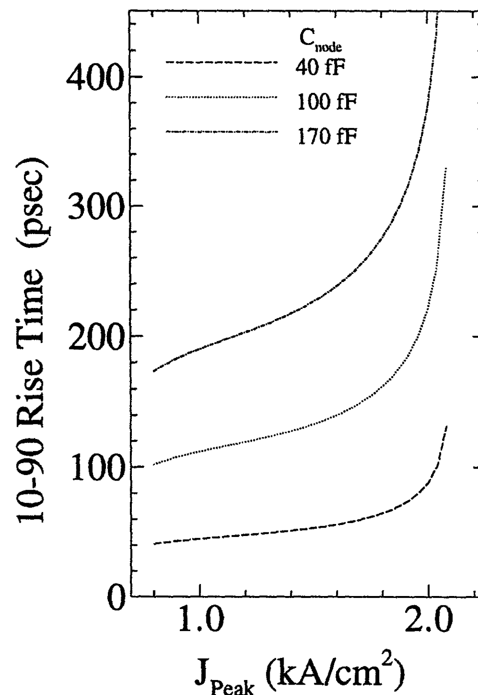


Figure 2-13: SRAM 10–90 switching time as a function of peak current density (and associated PVCR) with node capacitance as a parameter and V_{RTD} = 0.7 V.

Figure 2-13 shows the effect of changing the node capacitance for V_{RTD} = 0.7 V. As expected, increased capacitance slows the charging of the storage node. The case C_{node} = 170 fF

is representative of a hybrid implementation, with a 75×75 μm bond pad, 45 fF of interconnect capacitance, 20 fF source capacitance, and 10 fF RTD capacitance. Not only does extra capacitance slow the speed of the memory, it also reduces the array tolerance to variations in RTD parameters.

2.5 Desired RTD Characteristics for an RTD-EFET SRAM

RTD	J_P (A/cm^2)	PVCR	I_{FET} (mA)	V_{RTD} (V)	τ_R (psec)	P_{static} (mW)
NTT	6.8×10^5	2.59	50	4.79	16.1	229
RJA–7089	1.23×10^5	4.80	25	2.45	21.0	45.8
RJA–6141	20.8×10^3	13.0	5.0	5.0	95.2	11.2
RJA–9037	1.01×10^3	2.25	0.40	0.70	44.8	0.124
RJA–9080	0.287×10^3	2.27	0.05	0.56	273.0	0.0259

Table 2.1: Calculated RTD-EFET SRAM performance for a variety of RTDs: NTT is a device reported by NTT [18] and the others were grown as part of this thesis. The EFET source node capacitance was calculated using Vitesse design curves for 1.2 μm gate length EFETs that would source the listed switching current.

An RTD designed explicitly for speed will not be a good device for an RTD-EFET memory cell. Table 2.1 lists the calculated performance for a number of different RTDs. RTD NTT has a reported valley-to-peak switching time of 1.5 psec [18]. Obviously, this RTD was not grown with memory applications in mind. However, it explicitly demonstrates the speed/power trade-off. Even if the SRAM storage element bias voltage was reduced to 2 V (the RTD characteristics were compressed in voltage), one cell would still dissipate 95.5 mW of power. Comparison of the NTT diode to RJA–6141, another diode not grown specifically for memory applications, shows the effects of PVCR on static power and current density on speed. RJA–6141 has about a factor of thirty lower current density, which helps reduce the power of the cell, but increases the 10–90 rise time by approximately five. The increase in PVCR reduces the cell power dissipation by a factor of about twenty. RTDs RJA–9037 and RJA–9080 were both integrated with 10×1.2 μm EFETs. To accommodate the EFET, the current densities of both RTDs were reduced. They show further reductions in speed and static power dissipation because of this.

The best RTD for the RTD-EFET SRAM cell will be one tailored to a specific EFET technology, as well as to larger speed, power, and size constraints of the overall memory. However, for all situations, a few general statements can be made with regards to the most desirable RTD.

- The RTDs should have the highest allowable peak current density that will not exceed the switching current capabilities of the EFET. This will improve the ability of the RTDs to charge the storage node in the latter part of the switch.
- The RTDs should have the highest PVCR that will not exceed the switching current

capabilities of the EFET. This will reduce the static power of the cell and improve the memory's tolerance to RTD variations.

- The RTDs should have broad, low current valleys. This will reduce the static power of the cell as well as improve the uniformity in switching time and static power across a memory array.
- The RTDs should have peak and valley voltages such that the storage element can be biased $V_{\mathrm{RTD}} \geq V_P + V_V$ to best utilize the pushing power of the RTDs.

Given these guidelines, the choice of an RTD design, specifically with its current density, will be coupled with a choice of RTD area. In general, the RTD area should be minimized to reduce node capacitance. Ultimately, the final area choices will be determined by the current sourcing capabilities of the EFET.

3

RTD-MESFET Circuit Design and Fabrication

The second part of the design phase involves taking the lessons learned in Chapter 2 and applying them to a SRAM circuit. The integration technique affects the EFET performance and therefore places constraints on the circuit design. In addition, practical fabrication limitations must be taken into consideration. Section 3.1 provides an introduction to the Epitaxy-on-Electronics (EoE) integration technique, and reviews the additional design limitations the technique imposes. Sections 3.2, 3.3, and 3.4 describe the individual circuits designed to characterize the integration process and the RTD-EFET SRAM circuits. The RTD-EFET SRAM circuits are part of the multiepitaxy optoelectronic circuit MIT-OEIC-3. The atomic force microscopy measurements presented in this chapter were performed in collaboration with J. L. Pan of the MIT Department of Electrical Engineering and Computer Science.

3.1 Epitaxy-on-Electronics Integration Technique

Epitaxy-on-Electronics (EoE) is a novel technique used to combine III-V heterostructures with GaAs VLSI MESFET circuits. This technique, developed at MIT [19, 20], was originally designed to integrate photonic devices with electronics to form optoelectronic integrated circuits (OEICs). The technique leverages the considerable development of commercial GaAs MESFET circuits, allowing the focus of the user to remain on the photonic device and the circuit/system under study. For a complete review of the EoE technique, the reader is referred to [24]. EoE is by no means restricted to optoelectronic circuits, and in this thesis has been utilized to study the potential of RTD-based circuits.

The basic EoE process flow (Figure 3-1) has been successfully demonstrated in six generations of optoelectronic integrated circuits, including a winner-take-all LED-FET neural circuit [20]. The RTD circuits will be fabricated using the EoE flow. There are four steps to the EoE process: RTD-MESFET circuit design, MESFET circuit fabrication, MBE heterostructure growth, and heterostructure processing.

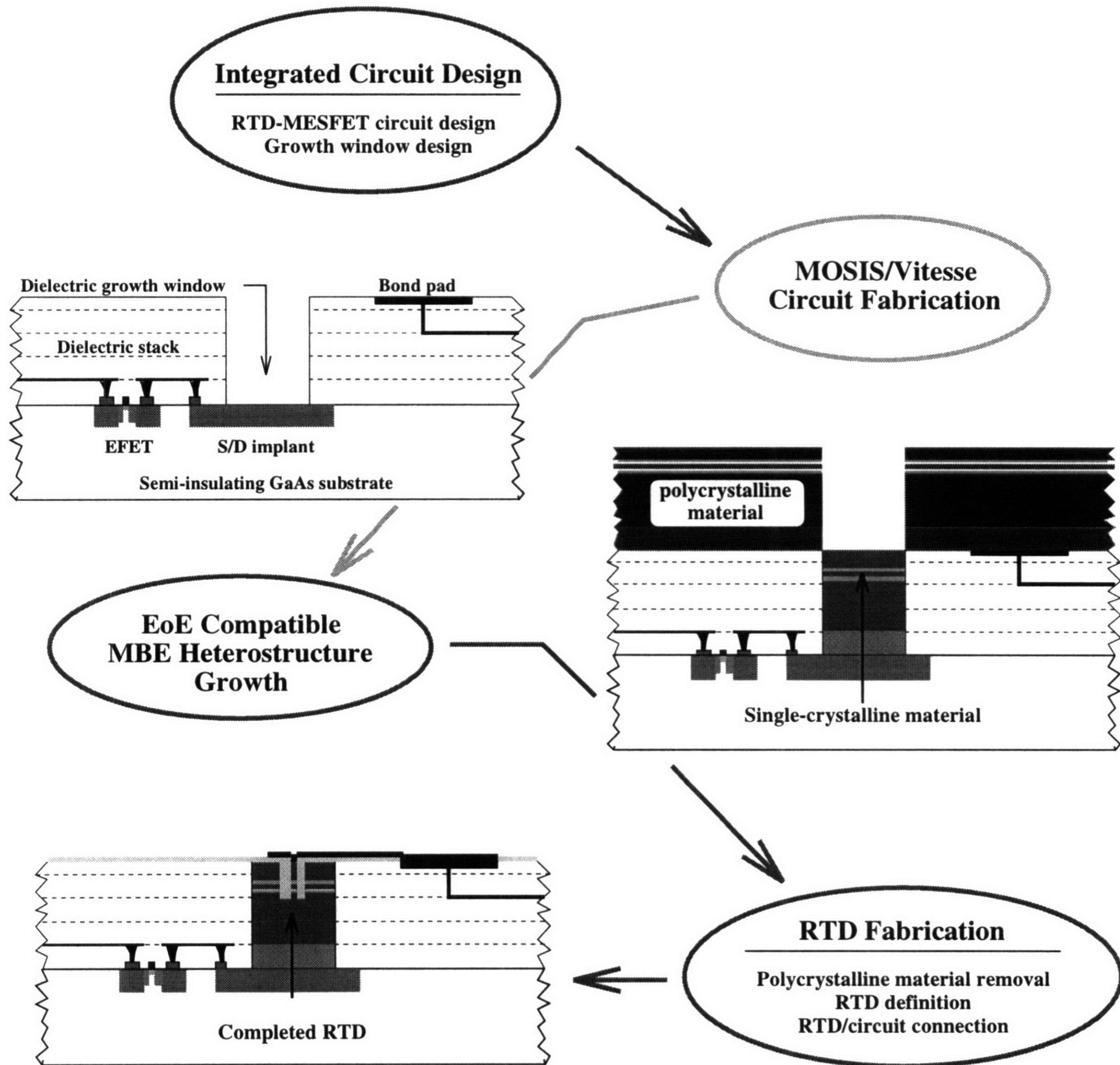


Figure 3-1: Integrated RTD-EFET SRAM process flow: circuits are designed at MIT; GaAs MESFET circuits are fabricated at Vitesse via the MOSIS service; the IC GaAs substrate is exposed in the dielectric growth windows (DGWs); an RTD heterostructure is grown in the DGW using MBE; standard processing techniques are used to remove the polycrystalline material and fabricate the RTDs.

3.1.1 RTD-MESFET Circuit Design

The first step in the EoE process is the design of a RTD-MESFET circuit. HSPICE modeling is an integral part of the initial design. HSPICE FET models are supplied by Vitesse [25]. The RTD is modeled as a voltage-controlled current source in parallel with a capacitor. Both polynomial and piecewise-linear fits to experimental RTD characteristics were used. During circuit layout, area is reserved for the RTDs. These regions, termed dielectric growth windows (DGWs), are where the heterostructure devices will eventually be fabricated. At this stage in the design process, however, they are just regions of the circuit where only interlevel dielectric will be placed. Final design checks are made using layout-extracted HSPICE elements, to which the RTDs are explicitly added.

3.1.2 MESFET Circuit Fabrication

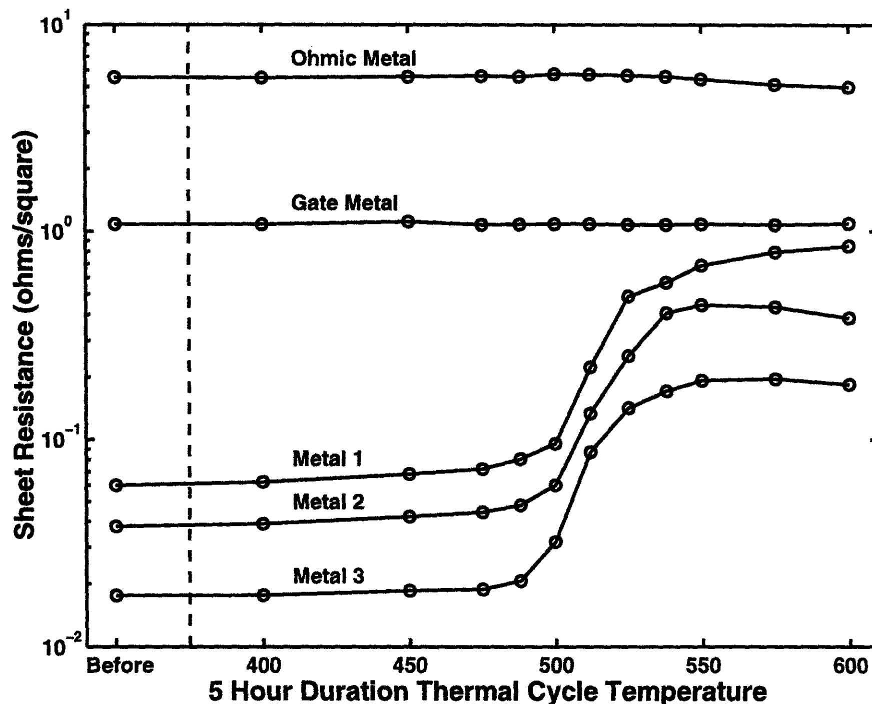


Figure 3-2: Thermal stability of IC metals.

Vitesse Semiconductor Corporation is the GaAs circuit vendor used by the ARPA/NSF MOS Implementation System (MOSIS). Vitesse uses a refractory-metal-based gate and ohmic contact process. This process is critical to the EoE integration technique, specifically the heterostructure growth step. These refractory metals can withstand the extended thermal cycles the circuits must undergo during heterostructure growth. The thermal stability of the circuit

metal places limits on the heterostructure growth. The upper-level interconnect metal is the most sensitive to thermal exposure and sets a thermal budget of five hours at 470°C for the MBE growth (Figure 3-2). If the thermal budget is exceeded, the sheet resistance of the interconnect metal increases leading to degraded circuit performance. The thermal stability of the circuits has been extensively studied as part of EoE development [19, 26]. For a full review of this topic, the reader is referred to [24, 27].

Vitesse also performs a 45° rotation of the crystal substrate. The RTD fabrication process uses wet etches, and the effect of this rotation on the fabrication process will be discussed in Subsection 3.1.4. As part of the Vitesse fabrication process, a scribe line etch is used to remove a substantial portion of the interlevel dielectric in the DGWs. Early integration projects used this etch to thoroughly clean the DGW, revealing the underlying GaAs substrate. More recently, the etch has been used to only partially cut through the dielectric stack in an effort to protect the GaAs IC substrate surface.

3.1.3 MBE Heterostructure Growth

When the fully processed integrated circuits are returned by MOSIS, the DGWs are partly filled with dielectric. This dielectric is removed in-house using a CF_4/O_2 reactive-ion etch (RIE) followed by a buffered-oxide etch (BOE) dip.

All heterostructures are grown in a Riber Model 2300 solid-source MBE. The IC is mounted on a molybdenum block with a quarter wafer of epi-ready substrate. This substrate serves as a growth monitor for reflected high energy electron diffraction (RHEED) and temperature calibrations. Once loaded into the growth chamber, the first step in a heterostructure growth is the removal of the native oxide present on the substrate. This is accomplished by baking the sample at 580°C until a 2×4 surface reconstruction is visible using RHEED, normally 5–10 minutes. The thermal desorption procedure does not lie within the budgeted thermal exposure for the chip. Hydrogen passivation for low temperature in-situ surface preparation is presently being incorporated as part of the standard EoE growth procedure. However, it was not utilized in any of the growths performed for this thesis. For every growth in this work, the performance of the integrated circuit is expected to be degraded.

After the surface oxide is removed, the growth is initiated and the substrate temperature is reduced to fall within the thermal budget. Epitaxial material is grown such that the entire DGW is filled. After removal of the polycrystalline material deposited on the IC, the surface of the filled DGW will match the IC surface. Completely filling the DGW provides a planar surface for high-resolution contact lithography in the DGW and reliable metal step coverage from the RTDs in the DGW to MESFET bond pads of the IC. The choice of substrate temperature must take into account both the material being grown and the total length of the growth. It is appropriate to comment here that the total growth thickness necessary to fill the DGW is 6.5 μm. This is substantially greater than the DGW depth of the two previous MIT-OEIC generation chips. The difference is due to an additional level of interconnect metal, metal 4,

in the Vitesse fabrication process. To comply with the thermal budget, the epitaxial growth rate would have to be greater than 1 μm/hour, or the growth temperature further reduced. Both options compromise epitaxial material quality. The maximum growth rate used in this thesis was 1 μm/hour. This growth rate-substrate temperature combination is expected to cause additional circuit degradation.

3.1.4 RTD Fabrication

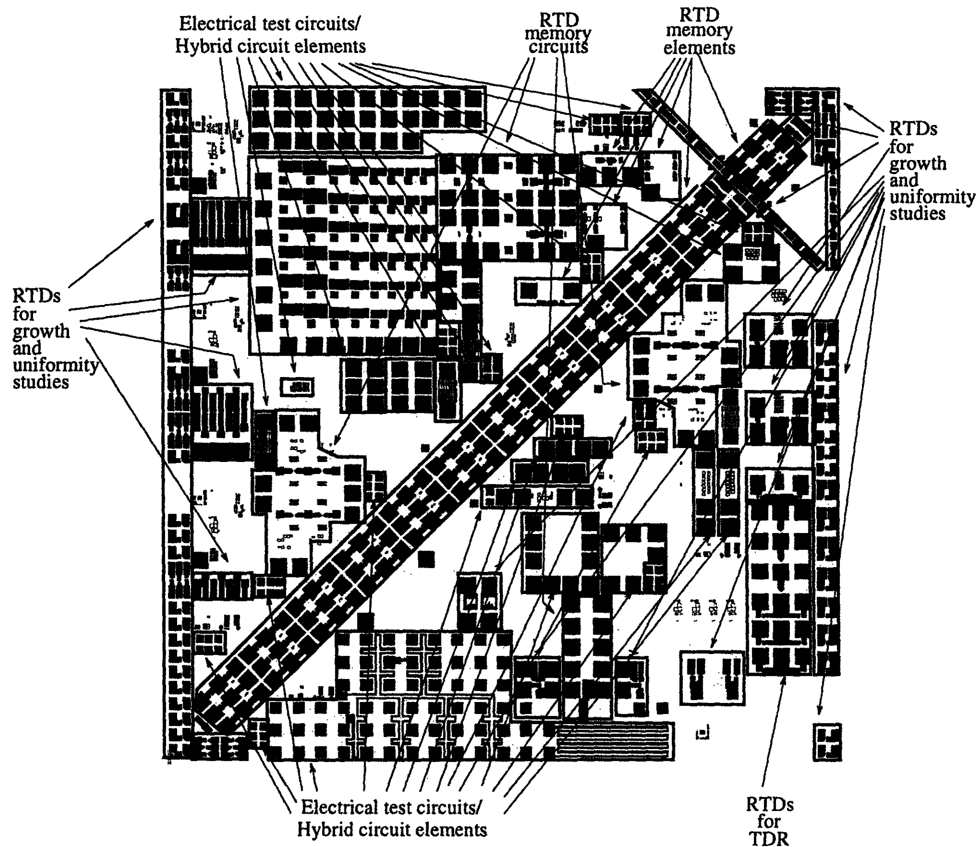


Figure 3-3: RTD-OEIC-1 mask layout.

Standard processing techniques are used to remove the polycrystalline material from the IC and to fabricate the RTDs within the DGW. A mask set, RTD-OEIC-1, was designed specifically to process the circuits associated with MIT-OEIC-3. This mask set utilizes every available DGW, not just those intended for RTD-based circuits, to provide characterization of device as well as circuit performance. As part of this mask set three general purpose mask layers, to be used in any implementation of MIT-OEIC-3 were designed. Figure 3-3 shows the various RTD circuits of RTD-OEIC-1. Complete documentation of the RTD-OEIC-1 mask set and the exact process details for RTD fabrication can be found in Appendices B and C.

To accommodate the Vitesse substrate rotation, all RTDs on the mask are oriented at a 45^0 angle with respect to the square mask, so that wet etches proceed on crystallographic planes. In addition, mesas are also oriented at the same angle. Upper-level metal must travel over the discontinuities in height formed by the device and mesa layers. Where ever possible, these contacts traverse both the V-groove and dove-tail edge profiles created by the wet etch, to insure that the contact traverses an edge suitable for metallization.

3.2 Well Array

Four basic circuits are used to demonstrate the RTD-MESFET integration. The first, shown in Figure 3-4, is an array of 48 growth wells (6 rows of 8 wells each). Each row has a variety of growth-well sizes: 100×100 μm, 75×75 μm, 50×50 μm, 40×40 μm, 30×30 μm, 20×20 μm, 10×10 μm, and 5×5 μm. In addition, the sidewall profile of the growth well is varied. Three of the rows have vertical sidewalls and three have sidewalls approximately 45^0 off vertical. The wells are implanted with the n-type source/drain (S/D) implant. The growth-well area is fully implanted for four of the rows, and roughly 25% implanted for two of the rows.

The wells are suitable for testing any two-terminal device, in this case RTDs. Electrical contact to each diode is made through a "column bus" and a "row bus". Each "row bus" is connected to the growth well via the S/D implant. Connection to the "column bus" will be made during post-growth processing. An additional pad has been included to allow post-growth connection to the substrate side of each well if necessary. Both the "row bus" and "column bus" bond pads are large enough to accommodate ball bonds. This will allow low-temperature studies of the diodes.

The primary purpose of this array is to study the growth of resonant-tunneling structures in DGWs. We specifically address the following issues:

- How does growth-well size affect the quality of RTDs? Is there a minimum size necessary?
- How does growth-well sidewall profile affect the quality of RTDs?
- Is there any difference in the quality of material grown on implanted crystal as opposed to nonimplanted crystal?

Electrical characterization and visual characterization will be the methods used to answer these questions. The electrical characterizations will also be used to choose appropriate supply voltages for the memory circuits.

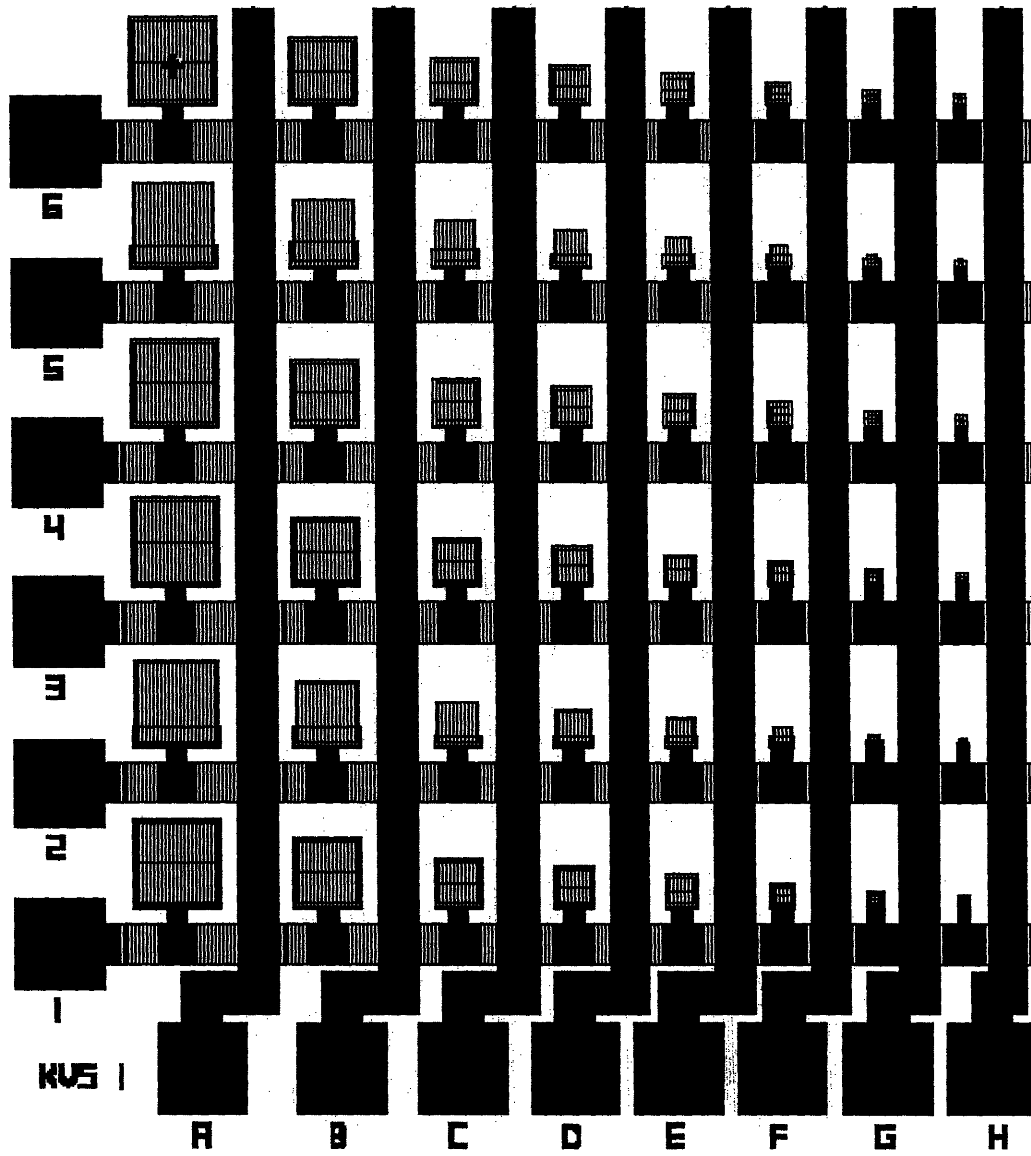


Figure 3-4: Layout of well array.

3.3 SRAM Cells

The second series of circuits is comprised of one-bit memory cells. These cells study the effects of RTD parameters such as size, doping, and peak-to-valley current and voltage ratios on the basic operation of the SRAM cell. These issues were raised in the the theoretical studies of the SRAM. The integration of EFETs and RTDs will allow the studies to be made on the actual cell.

Cell Name	EFET Gate	Growth Well	RTD size
RJA1A	240×1.2 μm	Implanted	10×10μm, 7.5×7.5 μm
RJA1B	84×1.2 μm	Implanted	5×5 μm, 7.5×7.5 μm
RJA2A	240×1.2 μm	Nonimplanted	10×10 μm, 7.5×7.5 μm
RJA2B	84×1.2 μm	Nonimplanted	5×5 μm, 7.5×7.5 μm

Table 3.1: Summary of one-bit memory-cell parameters. Two different RTD sizes are available for each memory cell.

Each cell contains two identical EFETs and a 100×100 μm growth well. The parameters varied in this circuit series are EFET size, RTD size, and growth-well implant. Table 3.1 identifies each of the memory cells and its associated EFET, RTD, and growth-well parameters. The addition of a second EFET, the READ EFET, is made to simplify testing of the memory cell. The READ and WRITE functionality can be evaluated without additional addressing circuitry. Figure 3-5 shows the schematics of the cells and Figures 3-6 and 3-7 show their layout.

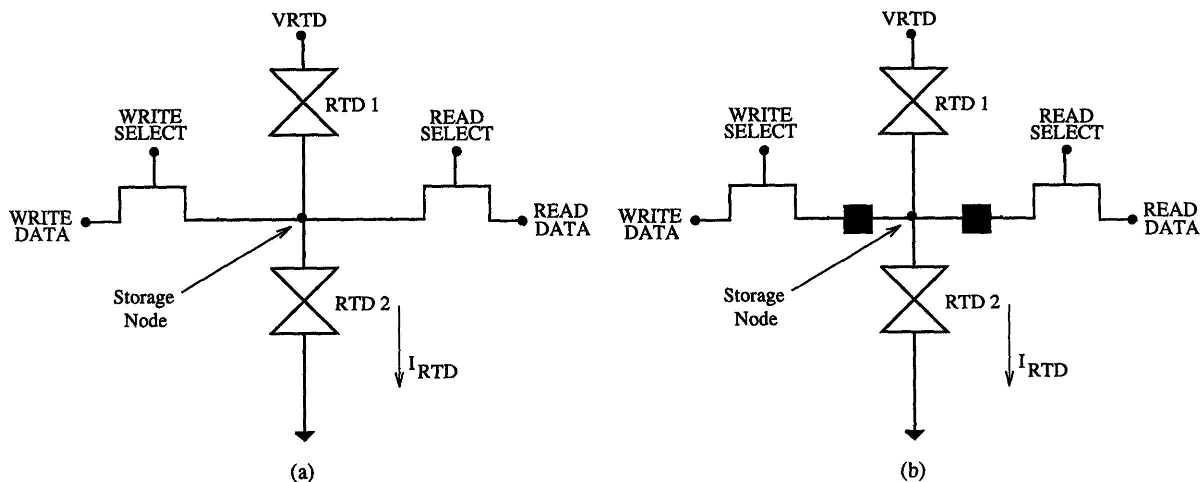


Figure 3-5: Circuit schematic of the RTD-EFET SRAM cells. (a) Implanted substrate: the connection between the EFETs and the RTDs is made via the source/drain implant exposed in the DGW; (b) Nonimplanted substrate: the connection between the EFETs and the RTDs is made by routing RTD upper-level metal between the EFET bond pads and the RTD node contact.

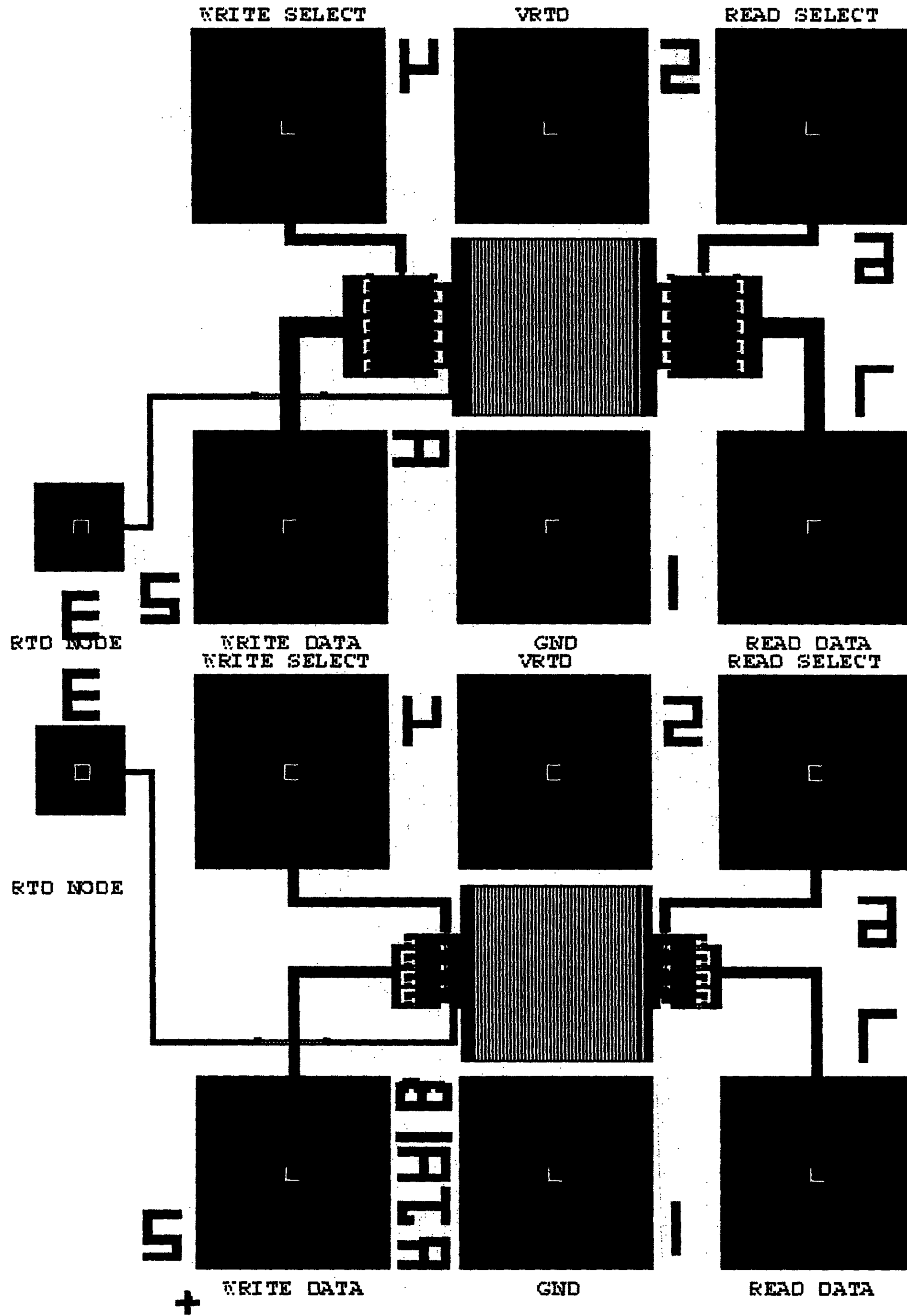


Figure 3-6: Layout of one-bit memory cells with a shared S/D implant.

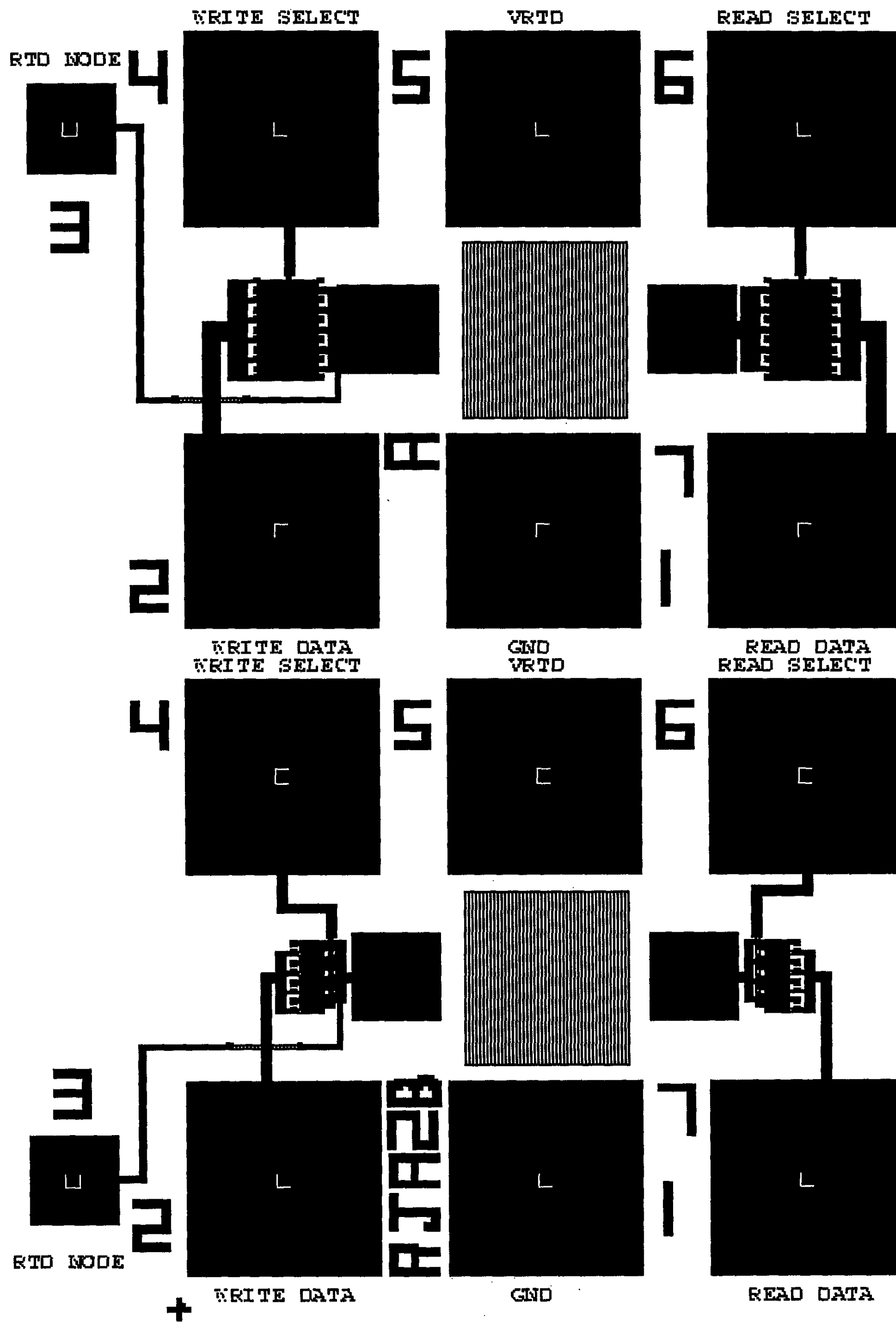


Figure 3-7: Layout of one-bit memory cells without a shared S/D implant.

The EFETs within the SRAM cells have been sized based on the performance of a 5×5 μm relaxed-buffer RTD (RBRTD) with a peak voltage of 0.6 V and a peak current of 30 mA. This particular diode has very thin barriers, and the EFETs were sized assuming a factor of ten reduction in current density for the RBRTDs. Figure 3-8 shows the HSPICE generated I–V characteristics for a 100 μm^2 RBRTD used in the circuit design simulations. To ensure manufacturability, the RTD sizes are large. The EFETs have been designed to compensate for the expected degradation of the electronics as well as to allow for some variation in RTD peak current density. The design should allow a wide variety of diodes to be integrated into the memory cell. Because there is no addressing circuitry involved, it will be possible to use non-DCFL levels at gates and drains of the WRITE and READ EFETs if necessary.

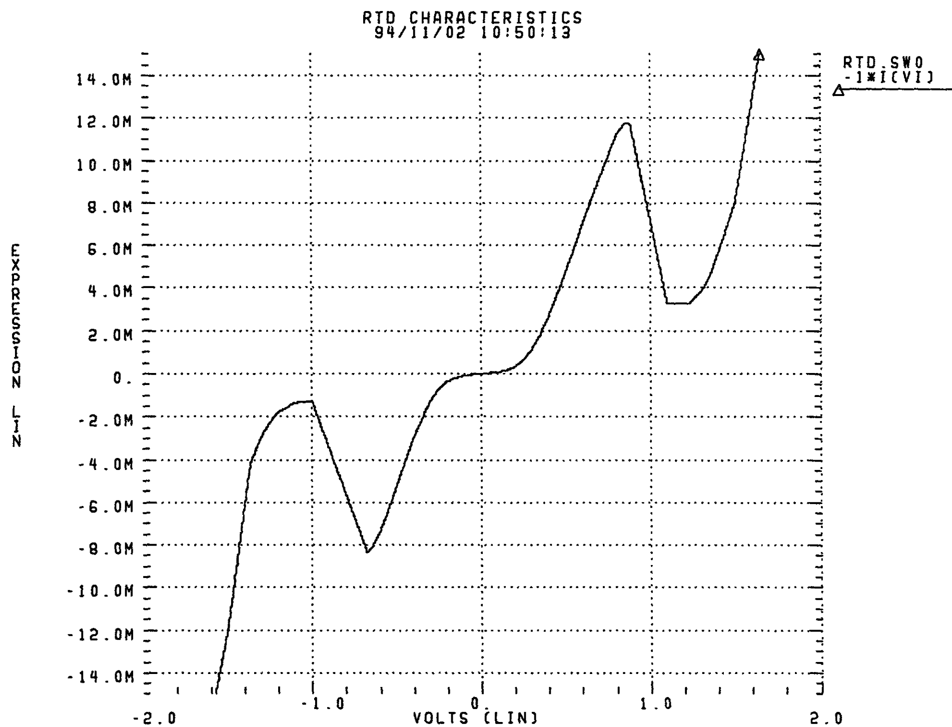


Figure 3-8: Simulated operation of 100 μm^2 RBRTD.

The cells are designed primarily for testing in the memory-cell configuration. Bond pads (100×100 μm) provide access to the WRITE SELECT, READ SELECT, WRITE DATA, READ DATA, VRTD (RTD storage element power supply), and GND (ground) nodes of the cell. In the case of the nonimplanted growth wells, there are two 50×50 μm bond pads to connect the RTDs with the EFETs. To test the memory cell operation, function generators are connected

to the WRITE SELECT, READ SELECT, and WRITE DATA nodes. The state of the cell can be read at the READ DATA node using an active probe.

Each cell has a 50×50 μm bond pad at the memory-cell storage node. This pad is a capacitive load on the cell. However, it allows for individual characterization of the discrete elements within the cell. Because of the limited number of cells available, the presence of a process monitoring node was considered essential.

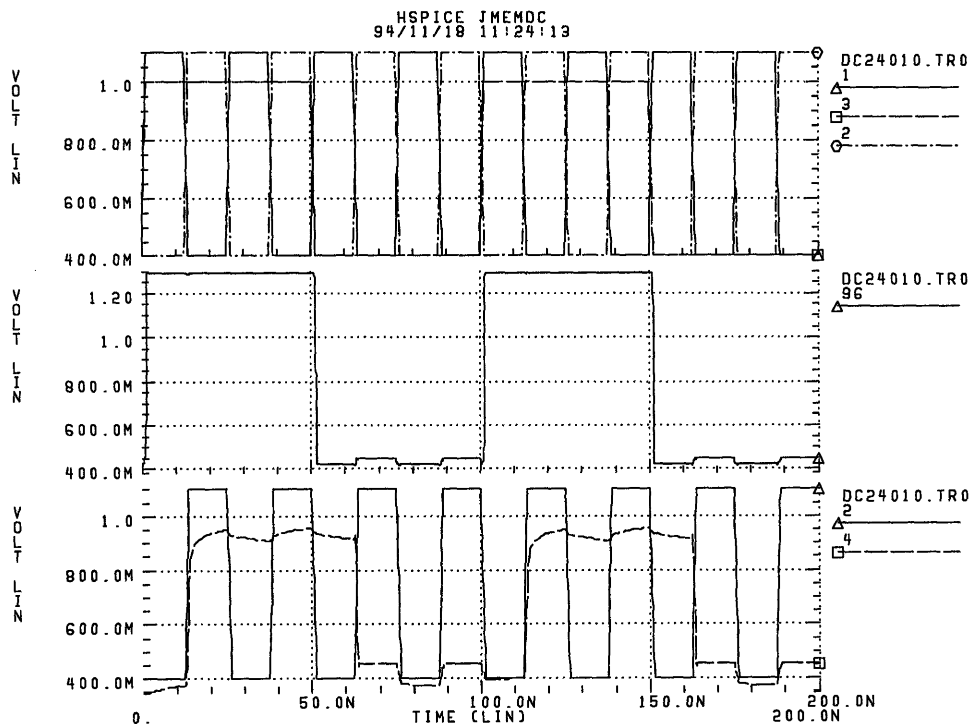


Figure 3-9: Simulated operation of cell RJA1A. Panel 1 shows the voltages at the WRITE DATA and WRITE and READ SELECT nodes. Panel 2 shows the voltage at the storage node. Panel 3 shows the voltages at the READ SELECT and DATA nodes. Details of the panels are described in the text.

Figure 3-9 shows the simulated operation of cell RJA1A. (The performance of cells RJA1B, RJA2A, and RJA2B are similar to those of RJA1A.) The parameters for the simulation are extracted from the layout of cell RJA1A. RTDs with areas of 100 μm^2 are used. The simulation assumes that a Picoprobe active probe (R = 1 M, C = 100 fF) is used to sense the READ DATA node. The sequence shown is WRITE HI from HI, READ HI, WRITE HI from LO, READ HI, WRITE LO from HI, READ LO, WRITE LO from LO, READ LO.

The first panel shows the WRITE DATA (dot-dash), WRITE SELECT (solid), and READ

SELECT (dashed) lines. The bias voltage for the RTDs, V_{RTD}, is 1.7 V. Both SELECT lines run between 0.4 and 1.1 V. The WRITE DATA line operates between 0.4 and 1 V.

The second panel shows the voltage at the storage node. Initially, V_{node} was set to 0.38 V. V_{HI} is 1.29 V and V_{LO} is 0.43 V. The storage node voltage is solid during the entire WRITE sequence. During the READ LO operations, the storage node rises to 0.45 V, but does not switch.

The third panel shows the voltage at the READ SELECT and READ DATA nodes. The solid line is the READ SELECT and the dashed line is the voltage at the READ DATA node. The READ DATA is valid only when the READ SELECT is HI. The READ DATA levels are ≈ 0.90 V for a HI and ≈ 0.45 V for a LO. During the READ HI operation, the storage node and the READ SELECT voltages are almost the same. The READ SELECT and READ DATA nodes establish V_{GS} for the READ EFET.

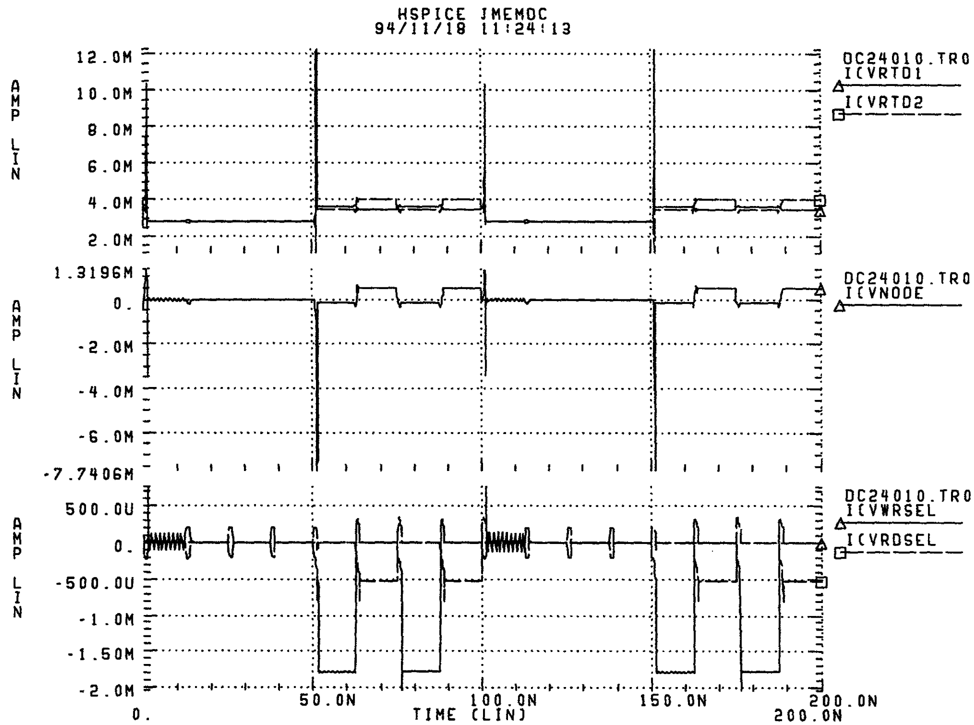


Figure 3-10: Simulated operation of cell RJA1A. Panel 1 shows the currents flowing in the two RTDs. Panel 2 shows the current flowing out of the storage node. Panel 3 shows the current flowing out of the gates of the WRITE and READ EFETs. Details of the panels are described in the text.

Figure 3-10 shows the currents flowing in the cell during the WRITE/READ sequence. The

first panel shows the currents flowing through the two RTDs, the solid line is the load RTD (RTD1), and the dashed line is the driver RTD (RTD2). The second panel shows the current flowing out of the node. The asymmetry of the RTDs is evident in these panels. Writing a HI requires the EFET to supply $\approx$ 8 mA but writing a LO requires $\approx$ 4 mA. The static power dissipated in the cell is 1.6 mW for the HI state and 1.4 mW for the LO state. During the WRITE LO operation, the WRITE EFET does not turn off. The voltages on the EFET are V_S = 0.40 V, V_G = 1.0 V, and V_D = 0.43 V. During this operation, the gate-to-source diode of the EFET is on. The EFET gate is drawing 1.78 mA, most of which is sunk by the DATA LO voltage source.

During the READ operation, the current flow in the circuit changes the voltage at the storage node. When reading a HI from a LO, V_{GS} of the READ EFET is established by the voltage difference between the READ SELECT and READ DATA nodes. Initially, V_{GS} is approximately 1 V. Current flows from the storage node, charging the READ DATA node. As the READ DATA node increases in voltage, V_{GS} of the READ EFET decreases. In addition, as the READ DATA node increases in voltage, V_{DS} of the READ EFET decreases. Therefore, the current flowing in the READ EFET decreases as the READ DATA node charges. In this simulation, the READ DATA node does not reach the storage node voltage before the READ EFET stops supplying current. However, the READ DATA node does make a rapid transition up in voltage over a range of approximately 0.5 V, which can be properly measured by a differential sense amplifier.

In the case of reading a LO from a HI, current flows into the storage node as the READ DATA node discharges. In this situation, V_{GS} of the READ EFET will be determined by the difference between the storage node and READ SELECT voltages. Current will flow into the storage node, discharging the READ DATA node. The addition of current to the storage node will cause its voltage to rise. Because the SELECT pulse is on after the READ DATA node has discharged to a voltage close to that of the storage node, the READ EFET has a high voltage on its gate and low voltages on its source and drain. As a result, the current flowing in the READ EFET changes from drain-source current to gate current. This current is divided bewteen the READ DATA and storage nodes, and increases the voltage at both nodes. This current is not enough to corrupt the voltage at the storage node. Once the READ SELECT is turned off, the storage node returns to its stable V_{LO} voltage, and the READ DATA node begins to discharge.

In these simulations, the READ DATA node is not precharged. These simulations are the worst-case scenario for the read operation because the voltage at the READ DATA node must switch over its full range. However, because these simulations are extracted from the layout of a single memory cell, they do not account for the capacitance of a full access line.

3.4 Memory Array

The third circuit cell is a 4×1-bit memory array. There are two identical arrays located in different regions of the chip. Each array is comprised of four one-bit memory cells identical to RJA1A, two sets of decode circuitry, and power and data lines. The circuits are designed to study the effects of RTD variation on memory performance. A schematic of the array is shown in Figure 3-11, and the layout of the circuit is shown in Figure 3-12.

The read and write operations have separate input and output circuitry. For the write operation, two control lines, S0 WRITE and S1 WRITE, are used to choose one of the four memory locations. The data to be written is input on the WRITE data line. For the read operation, two control lines, S0 READ and S1 READ, are used to choose one of the four memory locations. The read operation output is the READ data line. There are separate power supplies for the decode logic (VTT) and the RTDs (V_{RTD}.) All of the array components share a common ground node. The array is not designed to allow testing of internal nodes. A schematic of the array is shown in Figure 3-11.

Because the intent of this thesis is to focus on the operation of the memory cell, the addressing circuitry used in the array is very simple. In a commercial memory array, the exclusive selection of the READ or WRITE operation would be controlled by additional circuitry. We have not included any circuitry to prevent writing and reading to the same cell at the same time. The test operator will control these operations. Another consequence of our decode design is that one of the four cells is always selected. Memory location 00 has been selected as the "trash" location. To write a value to a specific bit, the value to be written is established on the WRITE data line, and the cell address is selected. For example, to write a HI to bit 10, S1 WRITE is LO, S0 WRITE is HI, and the WRITE data line is HI. Likewise to read from bit 01, the READ data line is sensed, S1 is LO and S0 is HI.

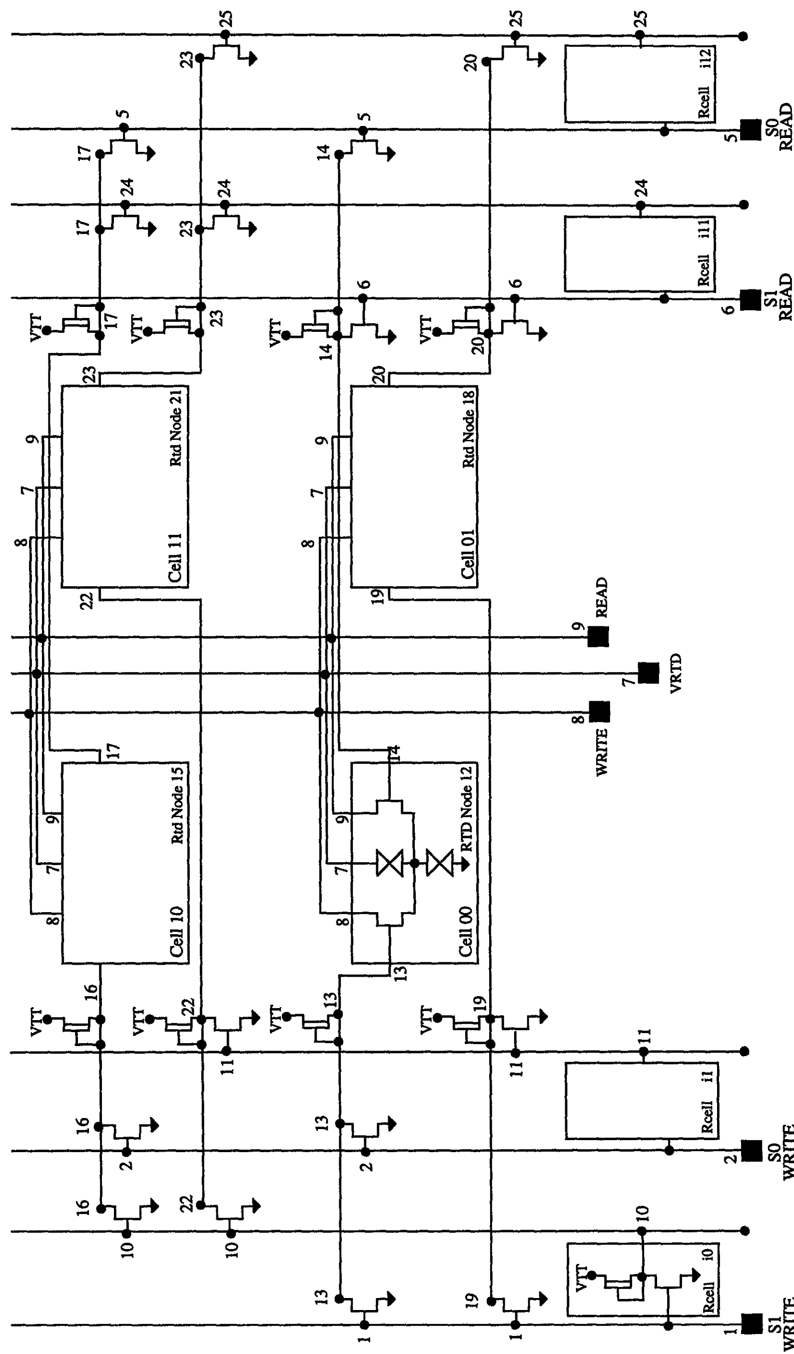


Figure 3-11: Circuit schematic of 4×1-bit memory array. HSPICE nodes are numbered.

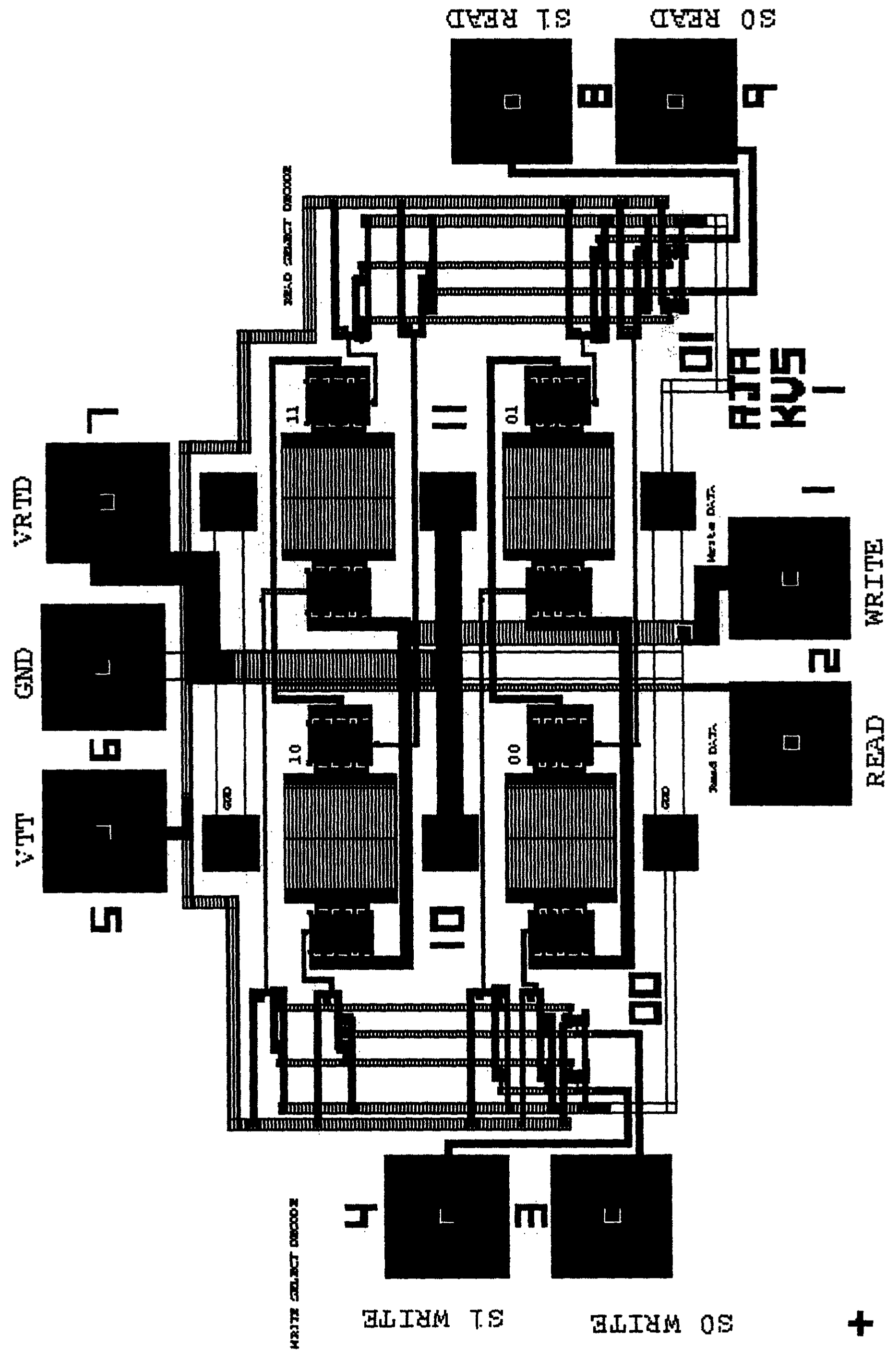


Figure 3-12: Layout of 4×1-bit memory array.

The parameters for the simulation of the memory array are extracted from the layout of cell RJA_KVS1. RTDs with an area of 100 μm^2 are used. The simulation assumes that a Picoprobe active probe (R = 1 M, C = 100 fF) is used to sense the READ data line. The basic test sequence is WRITE HI, READ HI, WRITE LO, READ LO.

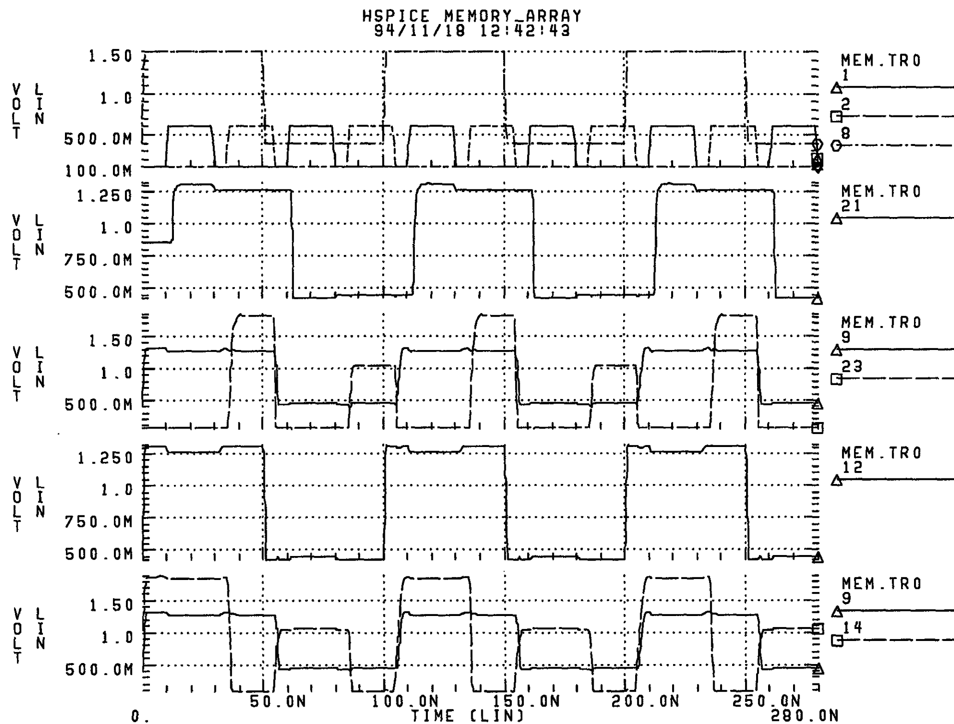


Figure 3-13: Simulated operation of bits 11 and 00 of the memory array. Details of the panels are described in the text.

Figure 3-13 shows the operation of memory locations 11 and 00 of the array. Panel 1 shows the WRITE data line (dot-dashed line), WRITE S1 SELECT (solid line), WRITE S0 SELECT (solid line), READ S1 SELECT (dashed line), and READ S0 SELECT (dashed line). The WRITE data line operates between 0.4 and 1.5 V, and the SELECT lines operate between 0.1 and 0.6 V. For this figure, the test sequence is WRITE HI 11, READ HI 11, WRITE LO 11, READ LO 11. Because one cell is always being addressed, the read and write functions overlap. Writing to location 11 and reading location 00 will occur simultaneously. Thus a READ LO 00, WRITE HI 00, READ HI 00, WRITE LO 00 sequence is also occurring.

Panel 2 shows the voltage at the storage node of location 11. When the WRITE data line and both WRITE SELECT lines are HI, the storage node at location 11 charges to $V_{\mathrm{WRITE\,HI}}$ =

1.31 V. When the WRITE SELECT lines go LO, the storage node relaxes to V_{HI} = 1.26 V. When the WRITE data line is LO and both WRITE SELECT lines are HI, the storage node at location 11 discharges to $V_{WRITE\,LO}$ = 0.42 V. When the WRITE SELECT lines go LO, the storage node relaxes to V_{LO} = 0.45 V. Panel 3 shows the internal READ SELECT 11 node (dashed line) and the voltage on the READ data line (solid line). When the internal READ SELECT 11 node is HI, the READ data line reflects the state of location 11. For t = 35–55 nsec, the state is a HI with a voltage of 1.25 V and for t = 85–105 nsec, the state is a LO with a voltage of 0.45 V.

Panel 4 shows the voltage at the storage node of location 00. When the WRITE data line HI and both WRITE SELECT lines are LO, the storage node at location 00 charges to $V_{WRITE\,HI}$ = 1.31 V. When the WRITE SELECT lines go HI, the storage node relaxes to V_{HI} = 1.26 V. When the WRITE data line and both WRITE SELECT lines are LO, the storage node at location 11 discharges to $V_{WRITE\,LO}$ = 0.42 V. When the WRITE SELECT lines go HI, the storage node relaxes to V_{LO} = 0.45 V. Panel 5 shows the internal READ SELECT 00 node (dashed line) and the voltage on the READ data line (solid line). When the internal READ SELECT 00 node is HI, the READ data line reflects the state of location 00. For t = 0–35 nsec, this is a HI and for t = 55–85 nsec, this is a LO. The HI and LO voltages, 1.25 and 0.45 V, respectively, are consistent with the READ values for location 11.

Figure 3-14 shows the operation of memory locations 01 and 10 of the array. Panel 1 shows the WRITE data line (dot-dashed line), WRITE S1 SELECT (solid line), WRITE S0 SELECT (solid line), READ S1 SELECT (dashed line), and READ S0 SELECT (dashed line). The WRITE data line operates between 0.4 and 1.5 V, and the SELECT lines operate between 0.1 and 0.6 V. For this figure, the test sequence is WRITE HI 10, READ HI 10, WRITE LO 10, READ LO 10. Because one cell is always being addressed, the read and write functions overlap. Writing to location 10 and reading location 01 will occur simultaneously. Thus a READ LO 01, WRITE HI 01, READ HI 01, WRITE LO 01 sequence is also occurring.

Panel 2 shows the voltage at the storage node of location 01. When the WRITE data line is HI, WRITE S1 SELECT is LO, and WRITE S0 SELECT is HI, the storage node at location 01 charges to $V_{WRITE\,HI}$ = 1.31 V. When the WRITE SELECT lines flip, the storage node relaxes to V_{HI} = 1.26 V. When the WRITE data line is LO, WRITE S1 SELECT is LO, and WRITE S0 SELECT is HI, the storage node at location 01 discharges to $V_{WRITE\,LO}$ = 0.42 V. When the WRITE SELECT lines flip, the storage node relaxes to V_{LO} = 0.45 V. Panel 3 shows the internal READ SELECT 01 node (dashed line) and the voltage on the READ data line (solid line). When the internal READ SELECT 01 node is HI, the READ data line reflects the state of location 01. For t = 40–60 nsec, this is a HI with a voltage of 1.25 V and for t = 80–100 nsec, this is a LO with a voltage of 0.45 V. The initial READ 01 operation, t = 0–20 nsec, reflects the simulation initial condition of location 01. The LO and HI voltages are consistent with those for states 00 and 11.

Panel 4 shows the voltage at the storage node of location 10. When the WRITE data line is HI, WRITE S1 SELECT is HI, and WRITE S0 SELECT is LO, the storage node at location 10

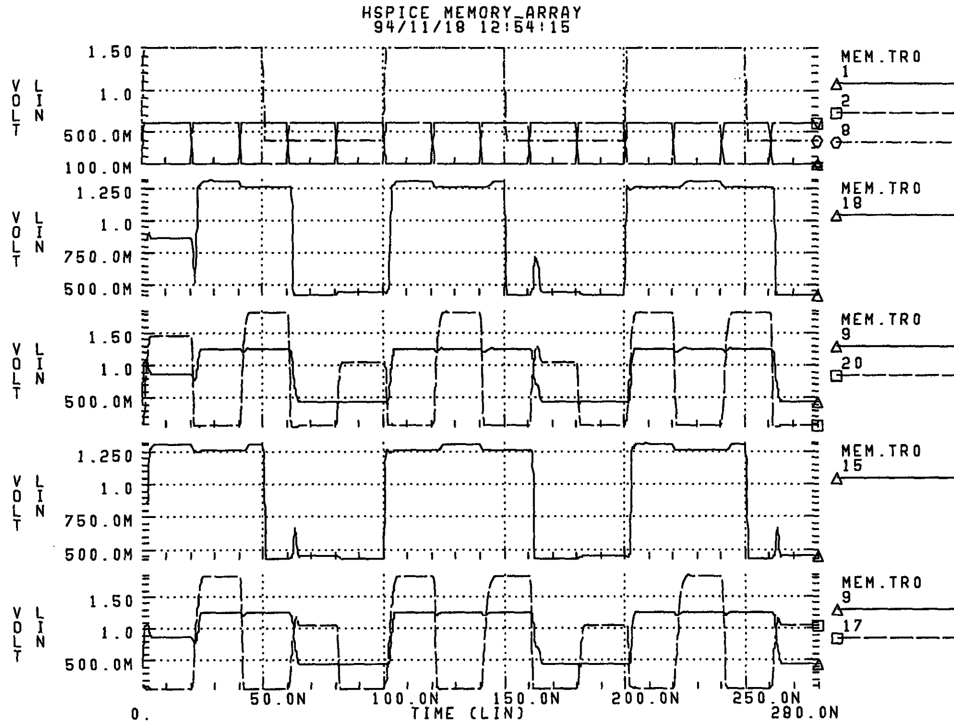


Figure 3-14: Simulated operation of bits 10 and 01 of the memory array. Details of the panels are described in the text.

charges to $V_{\mathrm{WRITE\,HI}}$ = 1.31 V. When the WRITE SELECT lines flip, the storage node relaxes to V_{HI} = 1.26 V. When the WRITE data line is LO, WRITE S1 SELECT is HI, and WRITE S0 SELECT is LO, the storage node at location 10 discharges to $V_{\mathrm{WRITE\,LO}}$ = 0.42 V. When the WRITE SELECT lines flip, the storage node relaxes to V_{LO} = 0.45 V. Panel 5 shows the internal READ SELECT 10 node (dashed line) and the voltage on the READ data line (solid line). When the internal READ SELECT 10 node is HI, the READ data line reflects the state of location 10. For t = 20–40 nsec this is a HI and for t = 60 – 80 nsec, this is a LO. The HI and LO voltages, 1.25 and 0.45 V, respectively, are consistent will all the other states of the memory array.

The storage nodes of both 01 and 10 memory cells show glitches when one cell select switches from a WRITE LO to READ LO operation and the other is simultaneously transitioning from a READ HI to WRITE LO operation. In both cases, the storage node of the cell in the WRITE LO to READ LO transition rises to approximately 0.75 V, but drops during the READ operation. The glitch is not destructive, and is a result of poor timing of the SELECT line transitions.

These simulations represent a worst-case scenario for the read operation of this memory array. The READ data line is not precharged, and therefore the memory element and READ EFET must drive the entire READ data line over the full output voltage range. In addition, this layout is not optimized for minimum signal line lengths and therefore has extra capacitance due to its length. The voltage swing of the READ data line is 0.8 V, from 0.45 to 1.25 V. This output voltage range is larger than that for a single memory cell, primarily due to the larger SELECT voltage (1.5 V for the array vs. 1.2 V for a single cell) at the individual memory cells of the array. (The individual select voltages of the array memory cells are higher because of the large voltage swing of the select decode circuitry.) Increases in the size of the memory will increase the size of the READ data line, and will reduce the speed of the read operation. A large enough READ data line will cause corruption of the voltage at the individual cell storage nodes. The size of the memory at which this happens will be dependent on the layout and processing issues that determine the capacitance of the READ data line, as well as the choice of a precharged voltage value for the line. But, these simulations indicate that for the purposes of this thesis, the memory cell is design is robust and that an array composed of these cells should operate under worst-case scenario conditions.

3.5 Circuit Summary

Characterization of EoE integrated RTD circuits must occur both at the device and circuit level. Electronic test circuits will be used to track the performance of the Vitesse circuit elements. The RTD-OEIC-1 mask has been designed to provide a wealth of information on discrete integrated RTDs. Additional device information will be extracted from the well-array circuits. The one-bit SRAM cell and four-bit SRAM array are designed primarily for functionality. Both the EFETS and RTDs are large to ensure proper circuit operation and manufacturability. All the circuits have been fully simulated, including layout extracted parasitics, in HSPICE.

3.6 MIT-OEIC-3 Features

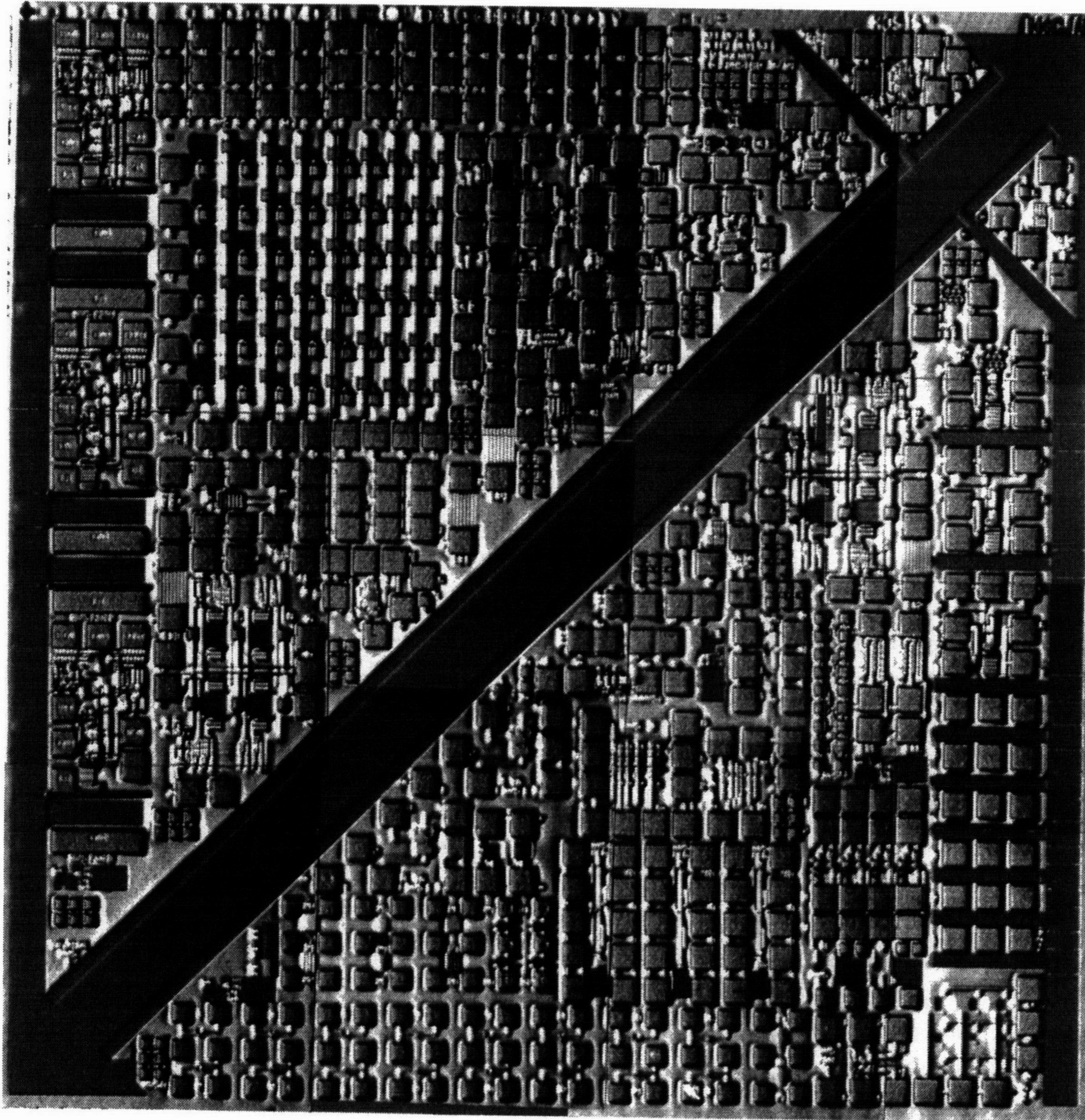


Figure 3-15: MIT-OEIC-3 prior to MBE growth. The picture is a collage of photographs taken at 50×. The smooth, dark areas are the exposed GaAs substrate.

MIT-OEIC-3, as indicated by its name, is the third in a series of OEICs. It is the first multiepitaxy chip of the series. This chip contains LED, laser, SEED, RTD, modulator, electrical testing, and process monitoring circuits. The chip measures 4.7 mm on a side. Figure 3-15 is a photograph of a chip ready for MBE growth. The picture is a collage of photographs taken at 50×. The smooth, dark areas are the exposed GaAs substrate. Complete documentation of MIT-OEIC-3 can be found in "MIT-OEIC-3/NCIPT-OEVLSI-1 Optoelectronic VLSI GaAs Chip

Design and Testing Manual" [25].

MIT-OEIC-3 is the first OEIC to involve a complex variety of different-sized DGWs. It is also the first chip to investigate the effects of implanted and nonimplanted substrates in the DGWs. This section review features and problems specific to this OEIC, some of which have ramifications for this thesis.

3.6.1 Conversion Errors

A file conversion error occured in the process of flattening the hierarchical integrated circuit design. The use of a Mentor Graphics GDT flattening flag, -gdsmerge, did not merge abutting features, but rather deleted elements in the design. The error occurred when the merge was required to combine multiple rectangles. MIT-OEIC-4 and future generations do not use the merge flag, and do not suffer from this problem.

As a result of the merge error, both 4-bit memory arrays and three of the 1-bit memory cells are nonfunctional. In addition, none of the large, discrete EFETs suitable for hybrid implementations of the memory circuits are functional. Because the focus of this thesis was on dc, not high speed operation, the original goals of the project are still applicable. The demonstration however, shifted from a monolithically integrated SRAM cell to a hybrid version, with both components on-chip. In addition, the lack of large EFETs necessitated a change in the desired RTD characteristics. To accommodate the reduction in available switching current, RTDs with lower current density and lower resonance voltages were designed and grown.

3.6.2 Implanted vs. Nonimplanted DGWs

MIT-OEIC-3 was the first of the MIT-OEIC series to have dielectric growth wells which exposed both implanted and nonimplanted regions of the IC substrate. There are three types of wells: fully implanted, partially implanted, and nonimplanted. These structures are included to determine which substrate, implanted or nonimplanted, provides the highest quality substrate for subsequent epitaxial growth. Surprisingly, it was discovered that there was a height differential between the implanted and nonimplanted substrates. Figure 3-16 shows the profile of a partially implanted well, revealing implanted material surface to be about 12.5 nm lower than the nonimplanted. It is suspected that during the initial Vitesse implant masking steps, substrate material is being removed as the field oxide implant mask is removed. In addition, it is suspected that there is a reaction between the crystal and the Si_3N_4 Oxide 0 during the activation anneal, consuming additional substrate. The reacted material is also removed during the DGW cleaning process. The combination of etches results in a depressed implant region. The depression does not pose a problem if the well is fully implanted or nonimplanted. However, in partially implanted wells, the implant/nonimplant height differential is transferred to the epitaxial material grown above it. Critical quantum well layers cannot be grown across the transition region.

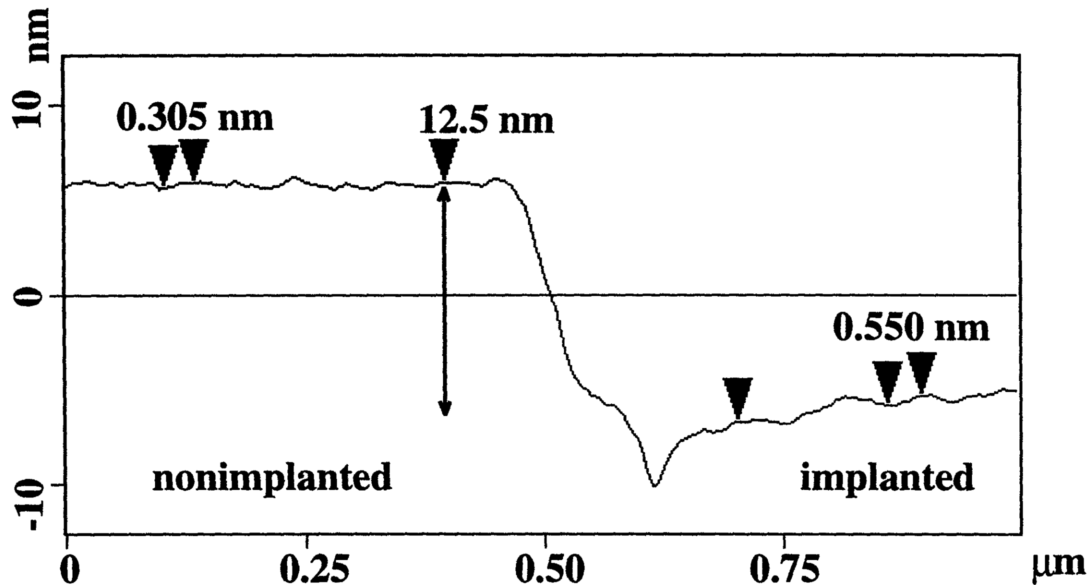


Figure 3-16: AFM Profile of implanted to nonimplanted DGW substrate transition.

3.6.3 DGW Cleaning Problems

Originally, the majority of the dielectric in the DGWs was to be removed at Vitesse using their scribe-line etch. This particular etch did not occur during the fabrication of MIT-OEIC-3. When received, the chips averaged 4.5 μm of dielectric in the DGWs, that had to be cleaned prior to MBE growth. Earlier generations of ICs had successfully been cleaned with a combination of unmasked RIE and wet etching. To avoid any possible damage to the substrate caused by the RIE, the mask set for this particular chip was designed for wet etching alone. A 3 μm overhang was provided to account for the lateral spread of an isotropic BOE etch. However, this proved unsatisfactory. The presence of two substrates, implanted and nonimplanted, exacerbated the cleaning problems. To expose the nonimplanted DGW substrate regions, an additional 0.3800 μm of dielectric, SiO_2 and Si_3N_4, has to be etched through. During this additional etch, the lateral spread of the etch seemed to be traveling along the interfaces of different dielectric materials within the stack. The lateral creep of the BOE exceeded the 3 μm margin provided by the overhang and eventually reached and began to destroy the circuits. An RIE process was developed to clean the DGW without destroying the electronics. Photoresist can be used as an RIE mask; however, the duration of the etch, 4.5 hours, would eat away the resist. Protection could be obtained by repeated photoresist mask and etch steps. Instead a metal mask RIE procedure was used clean the DGWs. In this process, aluminum was evaporated directly on the integrated circuit and then patterned to open the DGWs. The metal mask provided single-step protection of the integrated circuits during the RIE etch. The end of the RIE etch was visually determined, and a short BOE dip was used to remove any oxide left in the DGWs. BOE etches aluminum, and therefore the last BOE etch can generate particulates in the DGWs. An

additional masking step was used to protect the metal mask from the BOE. The metal mask could either be left on or removed for the MBE growth. An HCL etch removes the mask without damaging the GaAs crystal. Prior to MBE growth, a thorough ultrasound solvent clean was performed.

The lack of a scribe-line etch combined with the metal-mask cleaning procedure negated the angled sidewalls designed into the well array. In addition, the cleaning procedure seemed to create a substantial particle count in the DGWs, which resulted in many defects in the heterostructure epitaxy. Substrate exposed by the RIE etch showed higher defect densities than that exposed by the BOE etch. It is believed that the RIE etch is damaging the IC substrate. To alleviate these cleaning problems, a new DGW structure is being implemented in MIT-OEIC-4.

4

Relaxed-Buffer RTDs

This chapter describes the design and fabrication of RTDs compatible with SRAM circuits. The first section reviews the choice of a material system for the RTDs. The next section reviews prior work both on relaxed $In_xGa_{1-x}As$ on GaAs buffers as well as relaxed-buffer RTDs (RBRTDs). The following sections then detail the experimental results of this thesis: the demonstration of high-performance RTDs, RTDs suitable for circuit integration, and characterization of the relaxed buffer. The x-ray measurements reported in this chapter were made by J.L. Pan of the MIT Department of Electrical Engineering and Computer Science. The x-ray data analysis was performed by the author. All other reported material studies on relaxed buffers presented in this chapter were performed in collaboration with Prof. E.A. Fitzgerald and M.T. Bulsara of the MIT Department of Materials Science and Engineering. Both the cathodoluminescence and etching measurements and data analysis were a collaborative effort. The transmission electron microscopy sample preparation and measurements were performed by M.T. Bulsara. The transmission electron microscopy data analysis was a collaborative effort.

4.1 Relaxed-Buffer RTD Materials

The EoE integration scheme requires that the component RTDs be compatible with GaAs substrates. Given our present epitaxial facilities, this restriction limits our choice of RTD materials to the $In_xGa_yAl_{1-x-y}As$ quaternary system. Within this quaternary system, there is a wide range of choices for both barrier and well material. The three most popular barrier materials for GaAs substrate RTDs are $Al_xGa_{1-x}As$, $In_xAl_{1-x}As$, and AlAs. Figure 4-1 shows the conduction band position of these materials with respect to the GaAs conduction band as a function of aluminum mole fraction. Unstrained values are calculated based on the work of Van de Walle [28] and the strained values are calculated based on the work of Krijn [29]. AlAs provides the largest gamma-band offset of the three. However, it also has the lowest lying X-band minimum. A number of studies have been reported in the literature which evaluate the effects of gamma- and X-band barrier height on the peak-to-valley current ratio (PVCR) and peak current density (J_P) of RTDs [30, 31, 32]. The peak current of an RTD is composed of

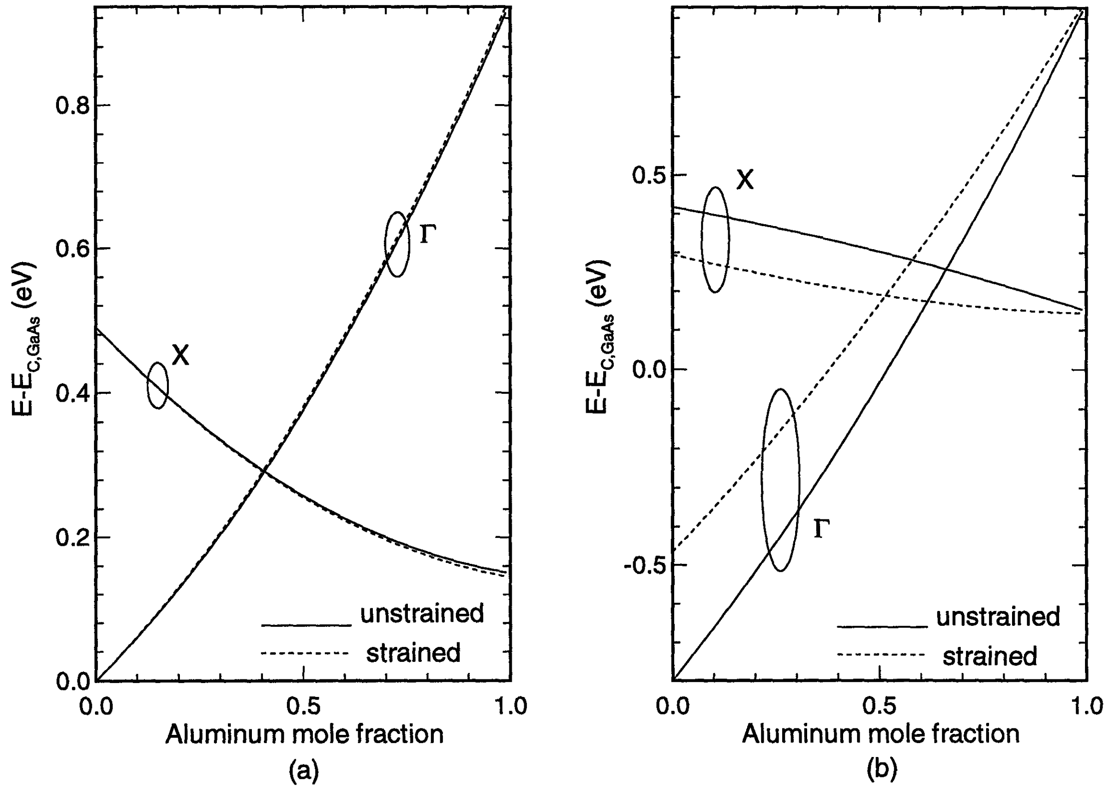


Figure 4-1: Conduction bands of RTD-barrier materials as a function of aluminum mole fraction. The bands are plotted relative to the gamma-conduction band of GaAs. (a) Gamma- and X-bands of $Al_xGa_{1-x}As$; (b) Gamma- and X-bands of $Al_xIn_{1-x}As$. Calculations are based on the work of Van de Walle [28] and Krijn [29].

a resonant-tunneling component and a component due to electrons scattering through lower-lying valleys in the barriers. The resonant-tunneling component current is dependent on the transmission coefficient of the double-barrier structure. The transmission coefficient is a highly peaked function whose value depends on the barrier height, barrier thickness, and well thickness of the RTD. For diodes of the same barrier and well width, a lower barrier height will lead to broader peaks in the transmission coefficient, causing a larger resonant-tunneling current. The valley current of the diode is also dependent on the transmission coefficient. Lower barrier heights will reduce the confinement of the RTD quantum-well state and lead to a larger valley current. The effect on the valley current is much stronger than on the peak current. Therefore, an increase in barrier aluminum mole fraction, leading to a more peaked transmission coefficient, will lead to an increase in PVCR [30].

The X-band barrier height will drop with increasing aluminum mole fraction. As a result, the "scattering" component of both the peak and valley currents will increase. Figure 4-2

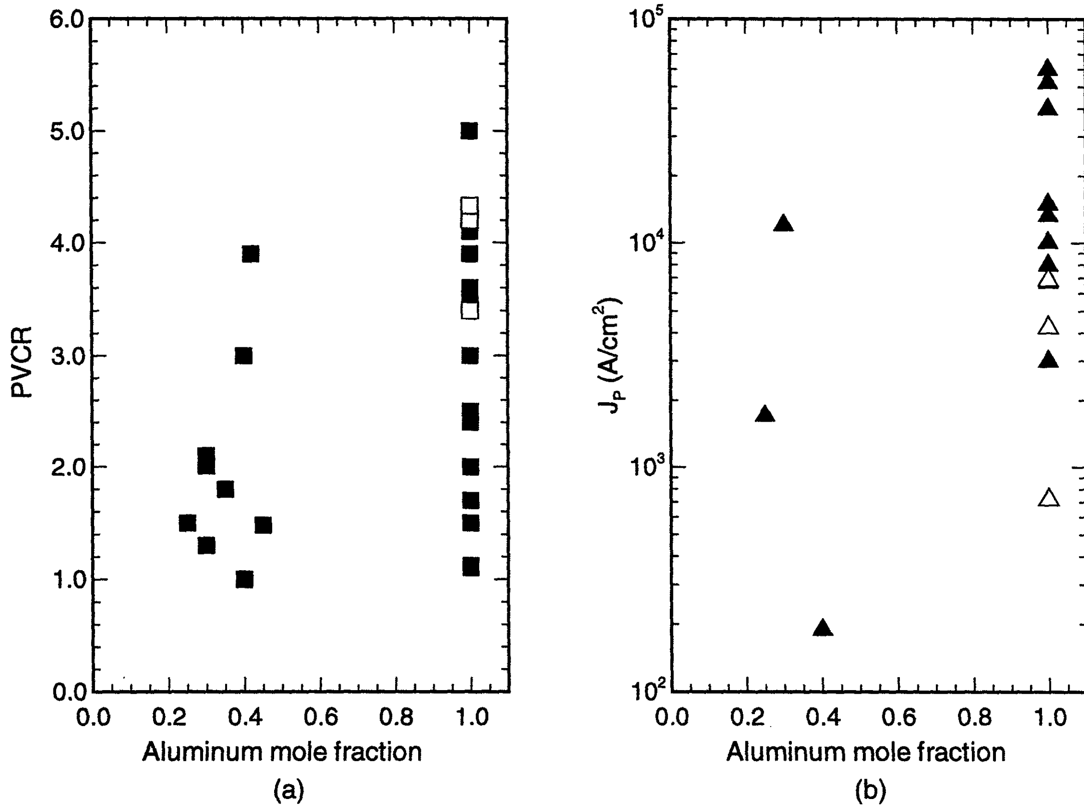


Figure 4-2: Performance of GaAs/$Al_xGa_{1-x}As$ resonant-tunneling diodes reported in the literature (solid) and grown as part of this thesis (open). (a) PVCR and (b) J_P as a function of barrier aluminum mole fraction. These diodes have a variety of barrier widths.

summarizes the performance of some RTDs reported in the literature, as well as some grown in the early phase of this thesis. For a given aluminum mole fraction, the variance in the performance of the diodes can be attributed to differences in barrier thickness and epitaxial material quality. Experimentally, higher PVCRs have been attained using AlAs rather than $Al_xGa_{1-x}As$ as a barrier material, suggesting that the gamma-band barrier is the critical barrier in these structures. Because the current density of diodes can be adjusted by varying diode barrier widths, we feel that PVCR is the critical figure of merit for the choice of barrier material. Therefore, we have chosen AlAs as the barrier material for our diodes.

The choice of a well material within the ternary $In_xGa_{1-x}As$ system involves a trade-off between the advantages of larger conduction band discontinuities and the disadvantages of smaller critical thicknesses. Figure 4-3a shows the conduction band offset of $In_xGa_{1-x}As$ to AlAs on a GaAs substrate. Figure 4-3b shows the critical thickness limits of $In_xGa_{1-x}As$ on GaAs. Once again, the bandstructure calculations are based on the work of Van de Walle [28]

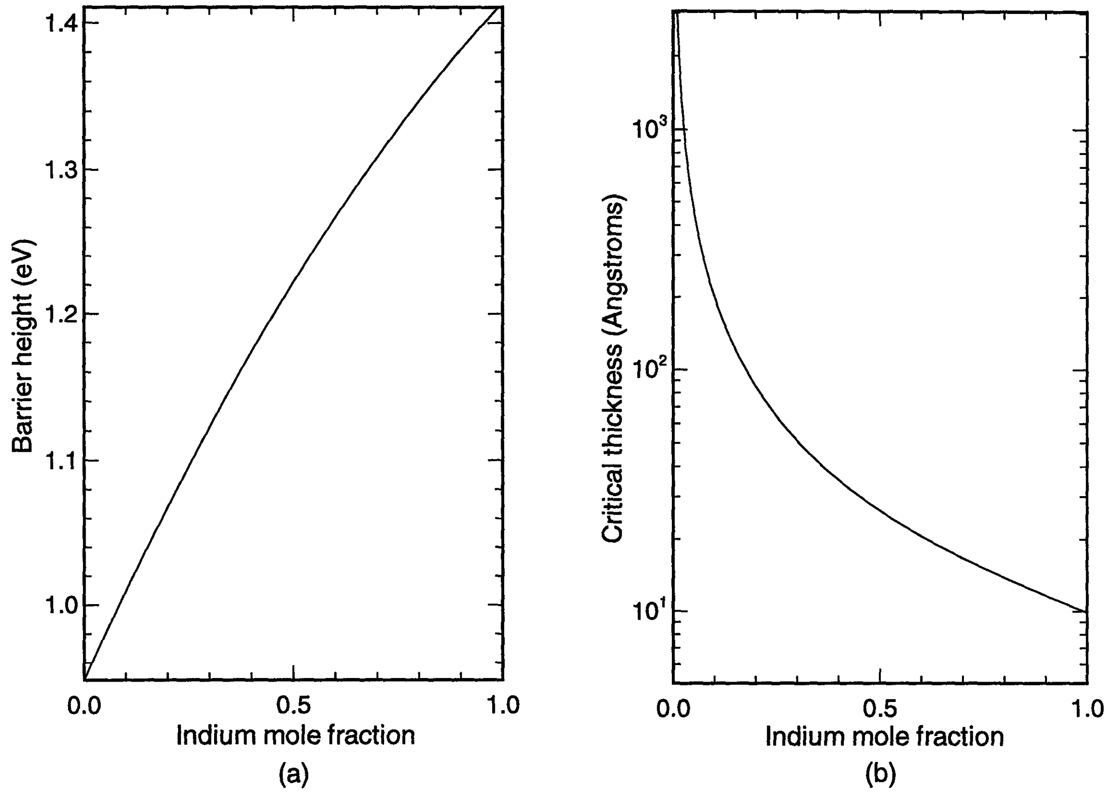


Figure 4-3: $In_xGa_{1-x}As/AlAs$ RTD material features. (a) The barrier height of $In_xGa_{1-x}As$ compared to AlAs when grown on GaAs as a function of indium mole fraction. (b) The critical thickness limits of $In_xGa_{1-x}As$ on GaAs as a function of indium mole fraction. The bandstructure calculations are based on the work of Van de Walle [28] and Krijn [29] and the critical thickness calculations are based on the work of Bennett [33].

and Krijn [29]. The critical thickness calculations are based on the work of Bennett [33]. Consider a double-barrier structure with a GaAs anode and cathode, AlAs barriers, and an $In_xGa_{1-x}As$ well. The smaller bandgap of $In_xGa_{1-x}As$ compared to GaAs allows the design of a structure in which the first state of the quantum well lies close to the cathode band edge while maintaining relatively large separation between the first and second energy states. For increasing indium content, the conduction band offset between $In_xGa_{1-x}As$ and AlAs will lead to greater confinement of the quantum-well state. This will decrease the full width at half maximum (FWHM) of the tunneling structure transmission coefficient, leading to a sharper diode current turn-off and a lower valley current.

To further improve the PVCR, $In_xGa_{1-x}As$ pre-wells ($In_xGa_{1-x}As$ wells before the AlAs barrier) can be added to $In_xGa_{1-x}As/AlAs$ double-barrier structures. Electrons injected through the barriers from an $In_xGa_{1-x}As$ pre-well will see a higher X-band barrier than those injected

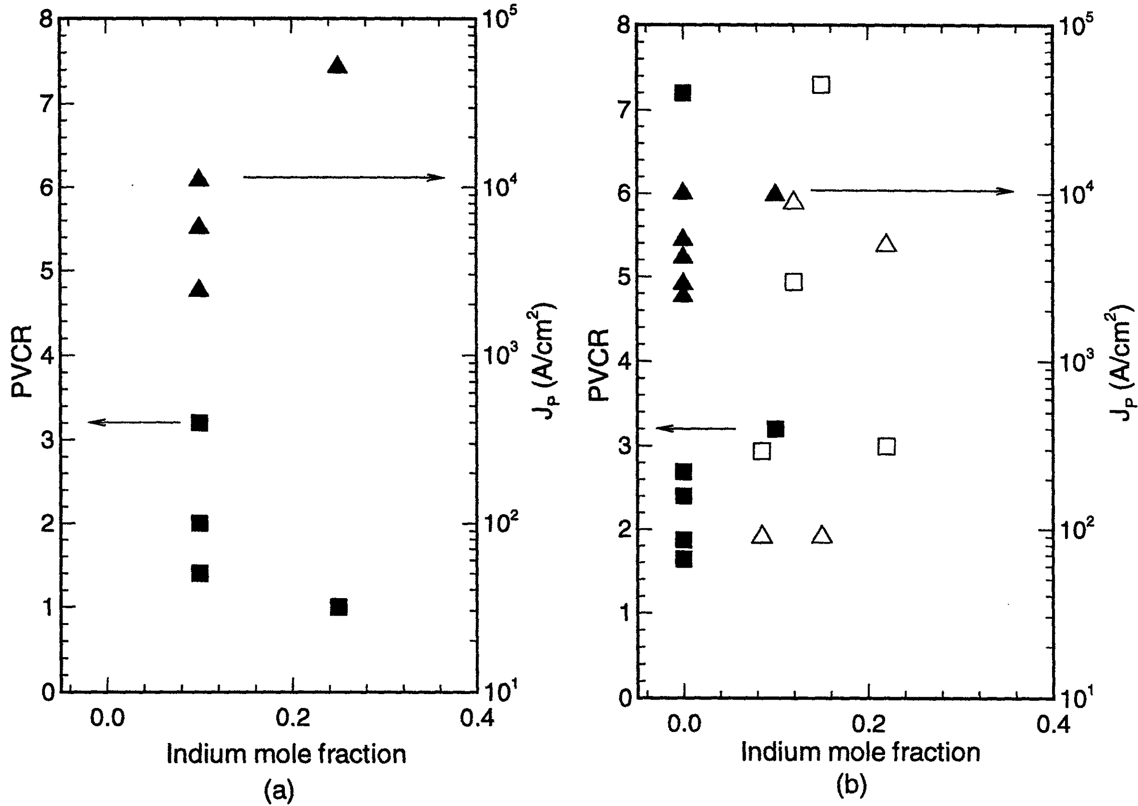


Figure 4-4: Performance of $In_xGa_{1-x}As/AlAs$ RTDs reported in the literature (solid) and grown as part of this thesis (open) as a function of well indium mole fraction. PVCR is shown with squares and J_P is shown with triangles. (a) $In_xGa_{1-x}As$ well RTDs (b) $In_xGa_{1-x}As$ pre-well and well RTDs. These diodes have a variety of barrier widths.

from GaAs. Figure 4-4 shows a partial summary of the performance of $In_xGa_{1-x}As$ well RTDs, both with and without $In_xGa_{1-x}As$ pre-wells, as reported in the literature and grown in the early phases of this thesis, as a function of the well indium mole fraction. Variations in diode performance for the same well indium mole fraction are attributable to differences in barrier widths and epitaxial material quality. An additional factor for the $In_xGa_{1-x}As$ pre-well and well devices is the indium fraction of the pre-well.

Because of the increasing amount of lattice mismatch as the indium fraction is increased, growth of a pseudomorphic structure will require that the width of a high-indium-percentage layer be less than its critical thickness. For $In_xGa_{1-x}As$ well structures, this may force the tunneling state of the well to lie at a higher energy than desired. The cumulative strain in $In_xGa_{1-x}As$ pre-well and well structures will preclude the use of wide, high-indium-percentage pre-wells and wells.

One method of overcoming these problems is to grow a strain-relieved epitaxial buffer

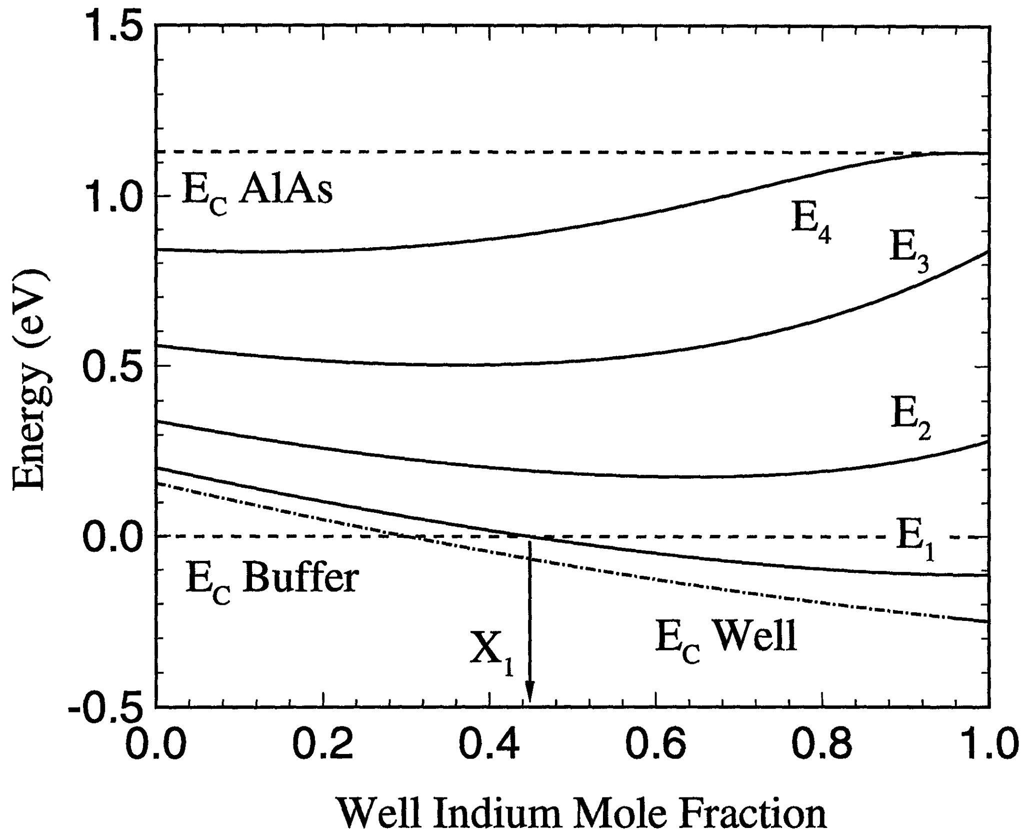


Figure 4-5: Calculated energy states for a RBRTD with a 10 nm well. $E = 0$ corresponds to the buffer conduction band edge. At X_1, state E_1 is no longer available for tunneling.

layer on which the tunnel diode is then grown, effectively changing the lattice constant of the substrate. The new "substrate" can be custom tailored to match the lattice constant of the diode well material. The lattice mismatch between the substrate and the RTD wells can be eliminated. As the relaxed-buffer indium percentage increases, the strain between the "substrate" and the AlAs barriers will increase. However, the barriers will be the thinnest layers in the double barrier structure, and can be designed to remain within critical thickness limits despite the change from a GaAs substrate.

Figure 4-5 shows the calculated energy states for a RBRTD. The "substrate" is $In_{0.30}Ga_{0.70}As$ and the barriers are AlAs. The well width is held at 10 nm and the energy states of the well are calculated for well materials ranging from GaAs to InAs. The model assumes that the RTDs are pseudomorphic, and the effects of strain on the band offsets and the variation in effective mass with indium percentage are included. The reference energy for the plot is the $In_{0.30}Ga_{0.70}As$ conduction band. For well indium mole fractions beyond $X_1 \approx 0.42$, the first energy state in the quantum well lies below the buffer conduction band edge, and is no longer

accessible for tunneling. When using a relaxed buffer, the designer has the choice of relaxed buffer, well material, and well width to control the position of the first tunneling state of the RTD quantum well, and thus the RTD resonance voltage.

4.2 Mechanisms of Strain Relief in Relaxed Buffers

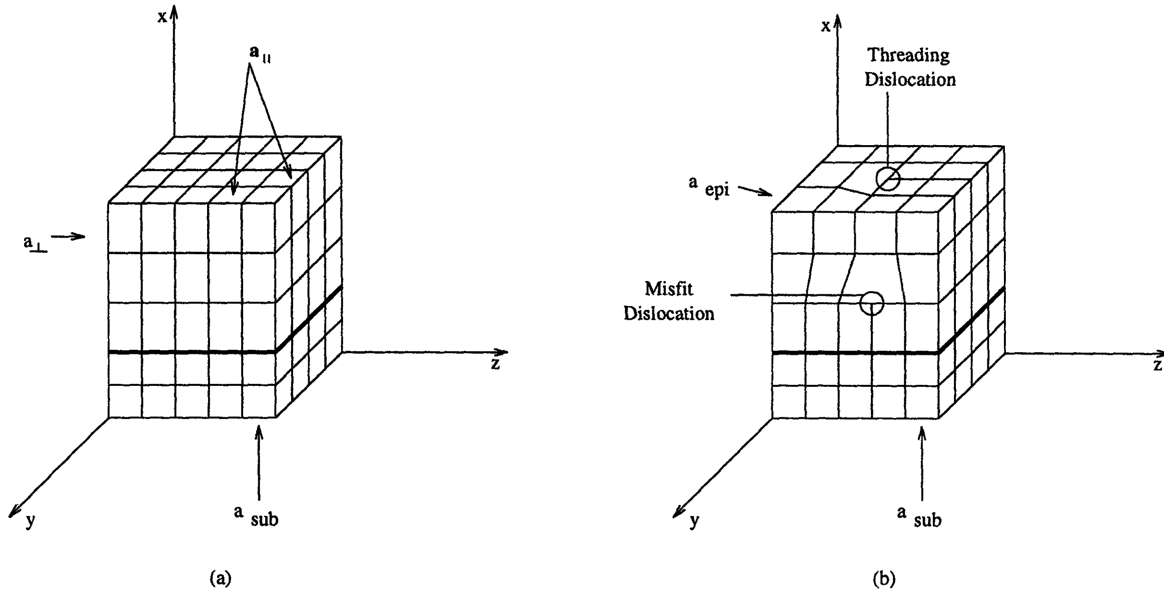


Figure 4-6: Schematic of crystal structures: (a) pseudomorphic, (b) relaxed.

In pseudomorphic epitaxial structures, Figure 4-6a, the in-plane lattice constant of the epitaxial layer, $a_{||}$, is the same as the substrate lattice constant, a_{sub}. (For the substrate, $a_{\mathrm{sub}} = a_{\perp} = a_{||}$.) The epitaxial layer elastically deforms perpendicular to the growth interface to accommodate the strain. When the crystal relaxes, Figure 4-6b, dislocations relieve the strain by changing the in-plane lattice constant. Dislocations lying parallel to the growth interface are misfit dislocations. Those that travel from inside the crystal to its top surface are threading dislocations. In $\mathrm{In}_x\mathrm{Ga}_{1-x}\mathrm{As}$, the relaxation is not necessarily equal in the two in-plane directions. In such situations, the crystal undergoes orthorhombic distortion.

Dislocation nucleation will occur when the strain relief provided by a dislocation, E_ϵ, balances or exceeds the energy required to generate that dislocation, E_l. Once initiated, the radius of a nucleation will increase until reaching an interface (Figure 4-7a). The dislocation will then have misfit and threading segments (Figure 4-7b). As the dislocation propagates, the threading segments will travel through the crystal and the misfit segment will have a corresponding increase in length. The number of nucleations per unit time and volume, N, can be written as [34]

$$N = A\eta\, exp\left(-\frac{E^*}{kT}\right), \tag{4.1}$$

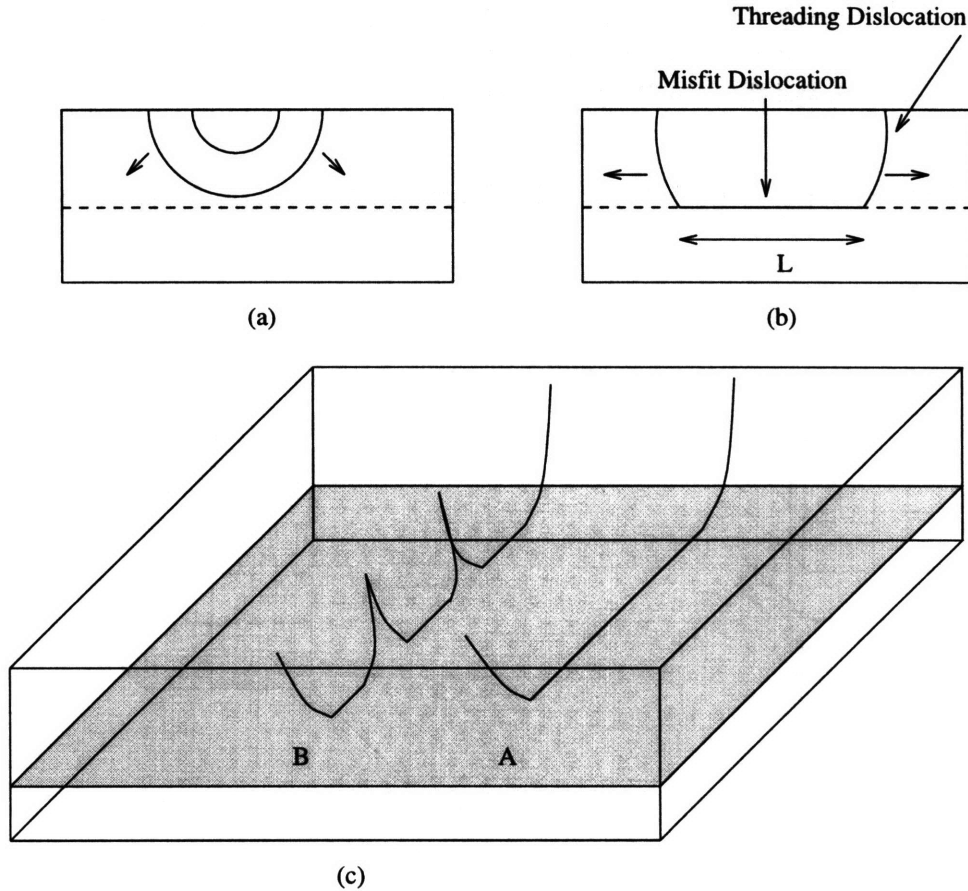


Figure 4-7: Defect nucleation and propagation. Dislocation nucleation occurs when energy required to generate a dislocation is balanced or exceeded by the strain relief provided by that dislocation. (a) Radial growth of a half-loop nucleation. (b) Creation of one misfit and two threading dislocations from the half-loop nucleation. (c) A long misfit, A, provides more efficient strain relief than a series of short misfits, B. Figure adapted from [34, 35].

where A is a constant with units of sec^{-1} and η is the atom density in cm^{-3}. The activation energy of the dislocation, $E^* \approx E_l - E_\epsilon$, is dependent on the nucleation source and proportional to the strain of the system. The velocity of a dislocation, $v = dL/dt$, can be expressed as [35]

$$v = B\,\tau_{res}^{m}\,exp\left(-\frac{U}{kT}\right), \tag{4.2}$$

where B is a constant with units of sec^{-1}, τ_{res}^{m} is the resolved shear stress with units of cm, and U is the activation energy for dislocation glide. Also, $m \approx 1.1$, and τ_{res}^{m} is linearly proportional to the strain of the system.

The strain relief provided by a misfit dislocation is proportional to its length. For a given total misfit length, the situation with the fewest threading dislocations is the most efficient. In Figure 4-7c, misfit A will more efficiently relax the buffer than misfit B. The optimal relaxation

conditions will balance the strain and temperature of a system to provide enough nucleation sites to generate strain-relieving misfits and allow those dislocations to propagate through the system. Too high a strain or too low a growth temperature can enhance nucleation. A low growth temperature will also reduce dislocation velocity. Both situations can lead to less efficient strain relief and increase the threading dislocation density of a buffer.

The cumulative strain fields from the misfit dislocations far below the surface will appear as a surface pattern. In relaxed $In_xGa_{1-x}As$, the pattern is a crosshatch in the $\langle 110 \rangle$ directions. An optically smooth surface is not an indication of good material quality. The surface view is a cross-sectional view of features perpendicular to the surface. Therefore, it is a view down the long axis of a threading dislocation. The cross-sectional area of a thread is difficult to view, even under magnification, without the aid of a defect revealing technique. An optically smooth surface could actually be one filled with threading dislocations. The presence of a crosshatch indicates that misfit dislocations are relieving the strain in a relaxed buffer.

4.3 Relaxed-Buffer Demonstrations

A variety of relaxed-buffer structures, single-step, multiple-step, and linearly graded, have been used to grade from GaAs to an arbitrary $In_xGa_{1-x}As$. A single-step buffer will introduce the largest initial strain. Using double-crystal x-ray diffraction, Westwood *et al.* have studied the relaxation of 2.8 μm thick, single-step $In_xGa_{1-x}As$ layers on GaAs, $x = 0.0 - 1.0$. Residual strain was measured in all samples, with particularly poor material quality noted for $x \approx 0.5$. Studies have shown that for $x = 0.0 - 0.18$, the yield strength of $In_xGa_{1-x}As$ vs. GaAs can cause the dislocations generated at such interfaces to propagate into the GaAs substrate rather than the epitaxial layer [36, 37]. This notion of engineering the strain in subsequent epitaxial layers to direct the propagation of the strain relieving dislocations, i.e., grading the buffer, has the additional advantage of limiting and/or reducing the strain present at an interface. The reduction of strain will lead to a reduction in dislocation nucleation rate. If coupled with conditions appropriate to high dislocation velocity, this method will promote efficient strain relief in a buffer. Sacks *et al.* have demonstrated an $In_{0.4}Ga_{0.6}As$ metal-semiconductor-metal (MSM) photodetector on GaAs using a two-step relaxed buffer [38]. $In_xGa_{1-x}As$ step-graded buffers have been studied for use in MODFET structures as well [39, 40, 41].

Slow grading rates combined with high growth temperatures can be used to reduce the threading dislocation density (TDD) of relaxed buffers [48]. The slow grading rate limits the accumulation of strain and therefore the dislocation nucleation rate, and the high temperature allows a high dislocation velocity. $In_xGa_{1-x}As$/GaAs quantum wells grown on slow, linear grades have superior optical properties to those grown on single- and multiple-step buffers [49]. In addition, linear grades have produced very low TDD $In_xGa_{1-x}As$ epilayers [50].

RBRTDs have been reported on single-step, multiple-step, and linearly graded buffers. Early work on single-step buffers demonstrated GaAs/AlAs RTDs on a silicon substrate [42].

Buffer Structure	Diode Description	PVCR	J_P (kA/cm^2)	Source
Single Step	GaAs/AlAs on Si	2.9	1.6	[42]
Single Step	$In_{0.53}Ga_{0.47}As/AlAs$ on GaAs	9.3	17	[43]
Single Step	InAs/AlSb on GaAs	4.13	186	[44]
Three Step	$In_{0.3}Ga_{0.7}As/In_{0.3}Al_{0.7}As$ on GaAs	7.6	2.6	[45]
Linearly Graded	$In_{0.2}Ga_{0.8}As/In_{0.2}Al_{0.8}As$ on GaAs	4.7	12.8	[46]
Linearly Graded	$In_{0.34}Ga_{0.66}As/In_{0.34}Al_{0.66}As$ on GaAs	2.7	26	[46]
(6141) Two Step	$In_{0.22}Ga_{0.78}As/AlAs$ on GaAs	13	22.8	thesis, [47]
(7085) Two Step	$In_{0.22}Ga_{0.78}As/AlAs$ on GaAs	3.97	89.3	thesis
(7089) Two Step	$In_{0.27}Ga_{0.73}As/AlAs$ on GaAs	6.4	133	thesis
(7090) Two Step	$In_{0.27}Ga_{0.73}As/AlAs$ on GaAs	4.85	73.4	thesis
(7091) Two Step	$In_{0.27}Ga_{0.73}As/AlAs$ on GaAs	2.33	60.0	thesis
(9037) Two Step	$In_{0.27}Ga_{0.73}As/AlAs$ on GaAs	3.27	2.28	thesis
(9080) Linear Grade	$In_{0.205}Ga_{0.795}As/AlAs$ on GaAs	2.6, 4.98†	0.822, 17.5†	thesis

Table 4.1: Summary of RTDs grown on relaxed buffers. Devices below the double line are reported in this thesis; all others are from the literature. †Data from first, second resonance.

More recent work has concentrated on high-performance $In_xGa_{1-x}As$-based RTDs on GaAs substrates. Table 4.1 describes the performance of reported RBRTDs and compares them to those grown in this thesis. There is a wide variety in the performance of the devices. Much of this variety can be attributed to differences in the RTD structures. It is not clear how differences in the relaxation and defect structure of the relaxed buffers contribute to the differences in RTD performance.

4.4 EoE-Compatible Relaxed Buffer Quality

The growth conditions used in RBRTD growth for EoE integration purposes must conform with those established by the EoE process flow. Specifically, the MBE thermal cycle must not exceed 5 hours at 470°C and the total growth thickness must be 6.5 μm. Though compatible with relaxed-buffer growth, these conditions are not necessarily the optimal conditions for efficient strain relief. For these growth conditions, we need to determine the the best relaxed-buffer structure for our application. The ideal relaxed buffer would fully relieve the strain incurred in grading from GaAs to an arbitrary $In_xGa_{1-x}As$, as well as provide a defect free "substrate" on which to grow the RTD.

Any residual strain in the buffer will change the bandgap of the $In_xGa_{1-x}As$, changing the conduction band profile of the RTD. The ultimate effect of this strain will be in the position of the resonance voltage of the RTD. In addition, any residual strain will impact the critical thickness limits for the AlAs barriers of the RTD. The effect of defects on the performance of the RTD is unclear. Both misfit and threading dislocations are nonradiative recombination centers. Misfit dislocations lying deep in the relaxed buffer should not have any effect on the RTD. The

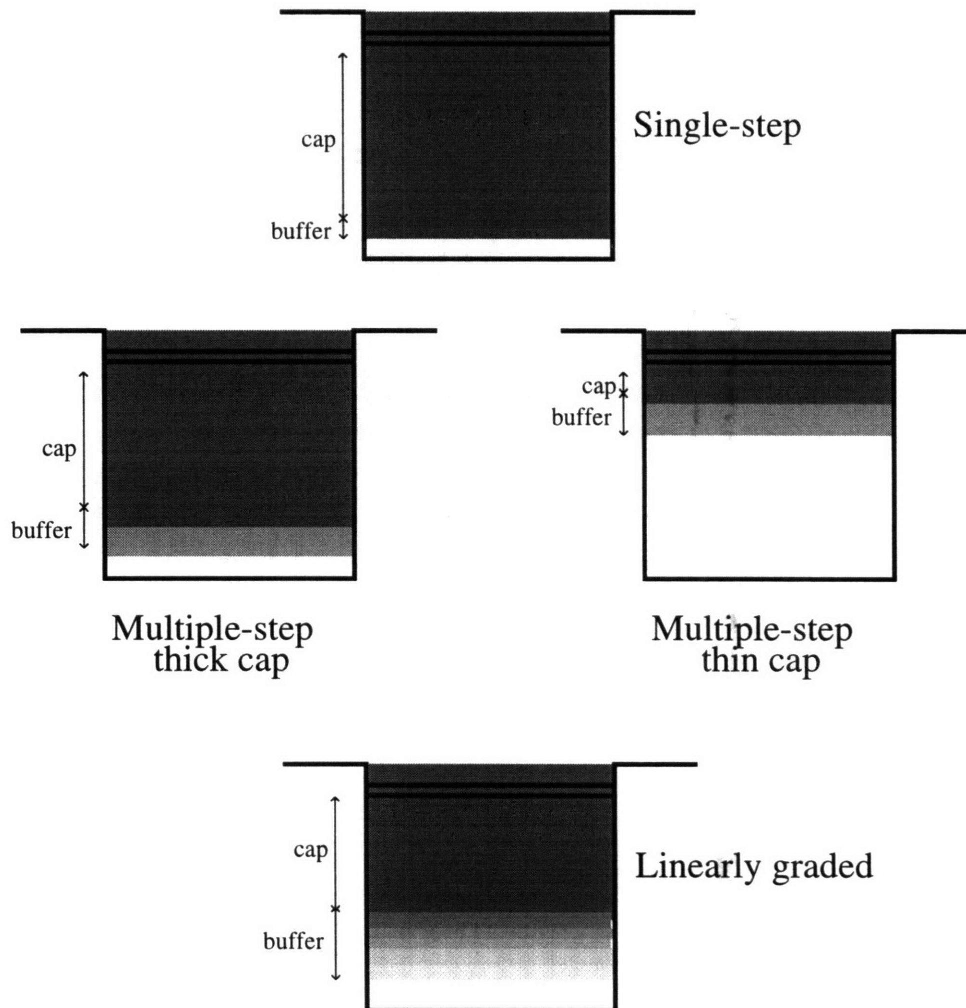


Figure 4-8: Epitaxial layer structure of relaxed buffers used to evaluate material quality.

electrical activity of misfit and threading dislocations in the RTD active layers is unknown; i.e., it is not possible to say whether threads short the RTD. The presence of threading dislocations will disrupt the RTD layer thicknesses, and a high TDD is expected to reduce the uniformity of the devices across a wafer. Practically, we would like to maximize the relaxation occuring in the buffer and minimize the number of defects propagating out of the buffer structure.

Figure 4-8 shows the basic RBRTD structure. After a thin GaAs buffer, the relaxed-buffer layer is grown. This is followed by a constant indium $In_xGa_{1-x}As$ layer, the cap, and the RTD active layers. We investigated three types of buffer grading structures: single step, multiple step, and linear. In addition, the multiple-step grade was performed both early and late in the growth to study the effect of cap thickness on buffer quality. For each relaxed-buffer structure we must evaluate both the relaxation of the structure and the TDD. To determine the relaxation of the buffers, a combination of x-ray diffraction and cathodoluminescence was used.

Cathodoluminescence (CL), etching studies, and transmission electron microscopy (TEM) were used to obtain the buffer TDD.

4.4.1 Effect of Grading Method on Relaxation

We use double crystal x-ray diffraction to characterize the relaxed-buffer material. To determine the amount of relaxation as well as the epitaxial layer composition, both symmetric and asymmetric rocking curves must be measured. The symmetric, (004) reflection, gives information on the out-of-plane lattice constant of the epilayer and the asymmetric, (224) reflection, gives information on the in-plane lattice constant of the epilayer. To fully characterize an orthorhombically distorted layer, six x-ray scans are required. This is a time consuming endeavor that is desirable to avoid. To reduce the number of required x-ray scans, assumptions can be made as to the degree of relaxation in the epitaxial layer. There are three possible states for the epilayer to be in: fully relaxed, partially relaxed, and pseudomorphic. In these studies, full relaxation was assumed. The x-ray results are compared to CL studies to determine the validity of this assumption.

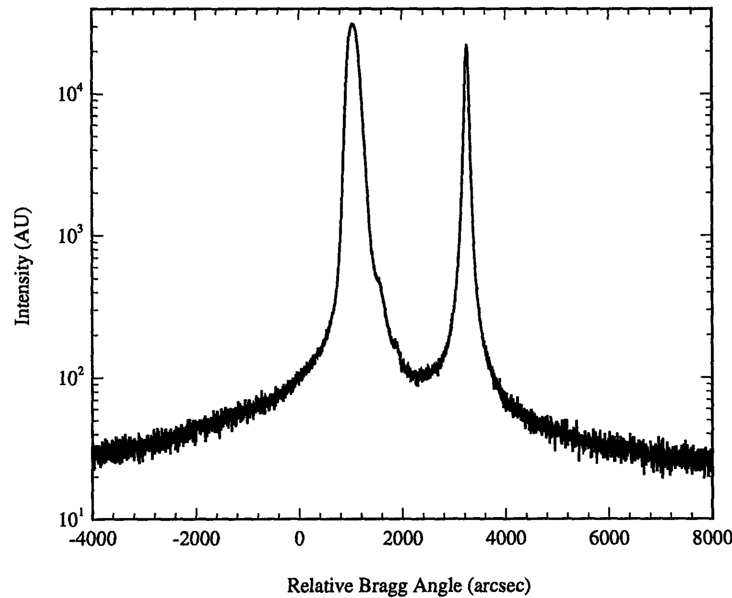


Figure 4-9: X-ray rocking curve of a single-step RBRTD. Epitaxial layer tilt was not included in this analysis.

Because complete relaxation was assumed, only symmetric rocking curve measurements were made. As an epitaxial layer relaxes, a tilt component will contribute to the measured peak separation. To eliminate the effects of the tilt, which is dependent on the rotational angle of the sample, two reflections 180^{0} apart were used. The reflections were taken parallel to the majority of misfit dislocations. A derivation of the analysis used in obtaining material

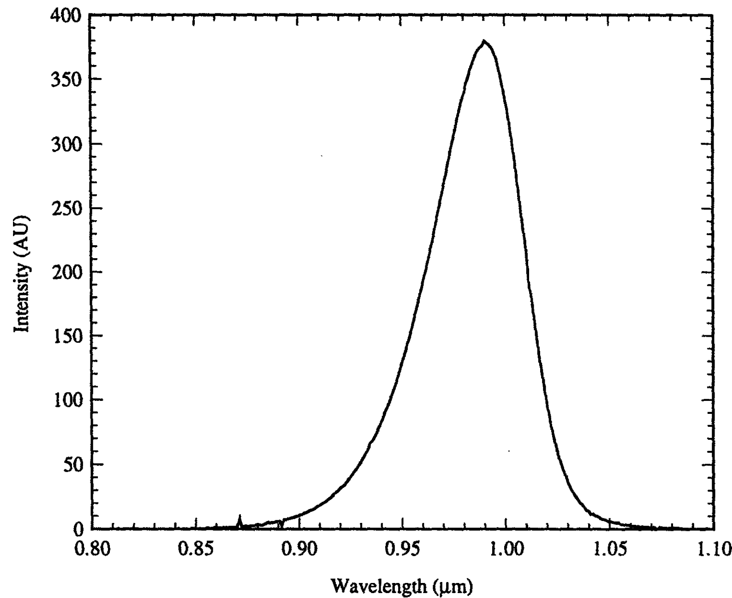


Figure 4-10: Cathodoluminescence spectrum of a single-step RBRTD. The peak wavelength is 0.99 μm. The spectrum was taken at 10 kV and 1000×.

composition from the x-ray rocking curves is included in Appendix E. For a complete review of x-ray diffraction, the reader is referred to [51, 52].

The single-step relaxed-buffer sample consists of 0.35 μm of GaAs, 3.18 μm $In_xGa_{1-x}As$, the RTD layers, and a 0.3363 μm top contact. The RTD consists of symmetric 10 nm undoped spacers, 2.1 nm AlAs barriers, and a 6.5 nm well. To facilitate the growth of multiple structures during one day, this structure was grown assuming a DGW depth of ≈ 4 μm. Following standard thermal oxide desorption, the substrate temperature was held at 470°C throughout the growth.

Figure 4-9 shows an (004)-reflection x-ray rocking curve for the single-step RBRTD. The narrow peak is the response from the substrate and wider peak from the relaxed buffer. Under the assumption of full relaxation, the x-ray data indicates a buffer indium mole fraction of 0.2309, corresponding to a bandgap of 1.108 eV. Figure 4-10 shows a cathodoluminescence spectrum of the material taken at 10 kV and 1000×. The peak wavelength is 0.99 μm. If we take E_G (eV) $= 1.242/\lambda\,(\mu\text{m})$, this corresponds to a bandgap of 1.255 eV. Part of the discrepancy between the x-ray and CL results can be assigned to the fact that for this sample, tilt of the epilayer was not included in the x-ray calculations. However, the effects of tilt cannot fully account for the differences in composition. Strain increases the bandgap of a material, therefore a partially relaxed $In_{0.23}Ga_{0.77}As$ layer could have the same CL response as a fully relaxed layer of lower indium content. The combination of the CL and x-ray spectra indicate that this buffer is not completely relaxed.

The multiple-step buffer structures were grown on the same day with identical cell temperatures. To accommodate the growth of two structures on one day, these samples were also

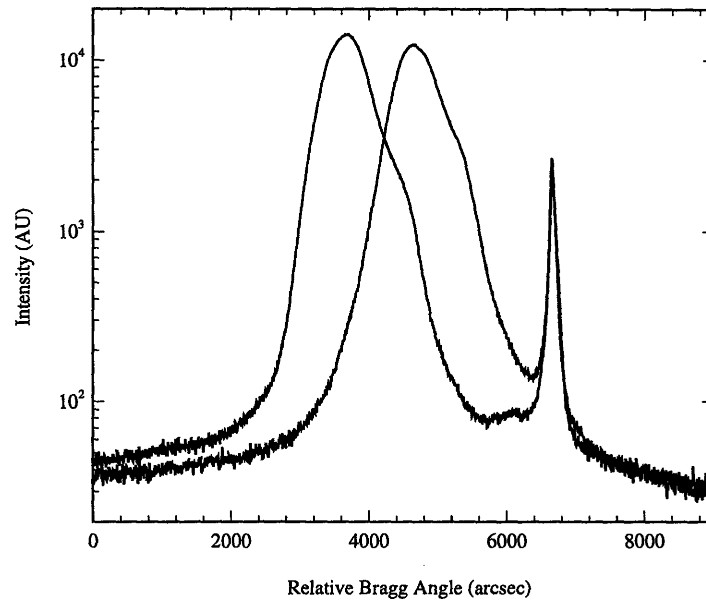


Figure 4-11: X-ray rocking curves of multiple-step, thick cap RBRTD. The two curves are measured 180$^{\text{O}}$ apart.

grown assuming a DGW depth of $\approx$ 4 μm. Following standard thermal oxide desorption, the substrate temperature was held at 470$^{\text{O}}$C throughout each growth. The thick cap structure consists of 0.4455 μm GaAs, 0.1939 μm $In_yGa_{1-y}As$, 2.908 μm $In_xGa_{1-x}As$, the RTD layers, and 0.3554 μm $In_xGa_{1-x}As$. The thin cap structure consists of 2.6 μm GaAs, 0.1939 μm $In_yGa_{1-y}As$, 0.3554 μm $In_xGa_{1-x}As$, the RTD layers, and 0.3554 μm $In_xGa_{1-x}As$. Both RTDs have symmetric 10 nm undoped spacers, 2.1 nm AlAs barriers, and a 8.1 nm well.

Figure 4-11 shows the (004)-reflection x-ray rocking curves for the multiple-step thick cap RBRTD sample. The smaller sharp peaks are the responses from the substrate and the larger broad peaks are from the epilayer. The shoulder on the right hand side of the epilayer peak is due to the intermediate $In_yGa_{1-y}As$ layer. If we assume complete relaxation, the x-ray data indicate an intermediate step indium mole fraction of y = 0.1899 and a final buffer indium mole fraction of x = 0.2601, corresponding to a bandgap of 1.060 eV.

Figure 4-12 shows the (004)-reflection x-ray rocking curves for the multiple-step thin cap RBRTD sample. Only one of the two orientations shows the contributions of intermediate $In_yGa_{1-y}As$ and final $In_xGa_{1-x}As$ layers. This feature is a result of residual strain in the sample as well as possible sample misalignment during the measurement. For the case of fully relaxed material, the x-ray data indicate an intermediate step indium mole fraction of y = 0.1997 and a buffer indium mole fraction of x = 0.2268, corresponding to a bandgap of 1.113 eV.

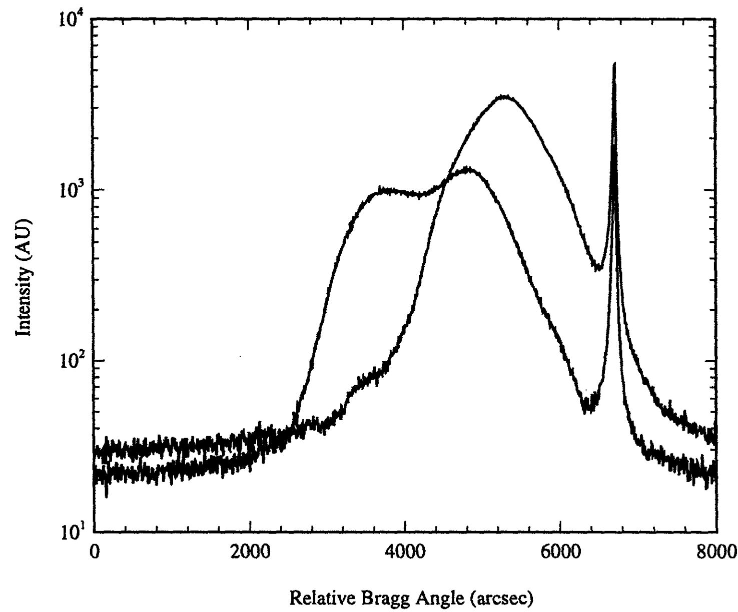


Figure 4-12: X-ray rocking curves of multiple-step, thin cap RBRTD. The two curves are measured 180° apart.

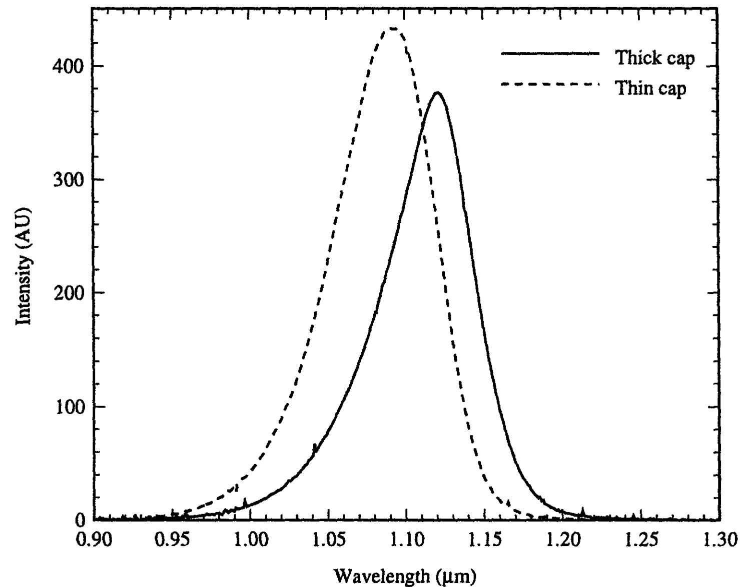


Figure 4-13: Cathodoluminescence spectra of multiple-step RBRTDs. The peak wavelength of the thick cap sample (solid line) is 1.12 μm and the peak wavelength of the thin cap sample (dashed line) is 1.095 μm. The spectra were both taken at 10 kV and 1000×.

Figure 4-13 shows the cathodoluminescence spectra of both multiple-step structures. For the thick cap sample the peak wavelength is 1.120 μm (1.109 eV), and for the thin cap the peak wavelength is 1.095 μm (1.134 eV). Identical cell temperatures were used for both structures, and therefore the indium content of the intermediate and final buffer layers should be the same for the structures. The lack of correspondence between the x-ray and CL for the individual samples as well as the differences between the two samples indicate a lack of relaxation in both samples. For the thick cap sample, the CL spectrum indicates a material with a larger bandgap, indicating residual strain in the material. Both the CL and x-ray results indicate that if fully relaxed, the thin cap structure would have a lower indium content than the thick cap. Since this is not feasible, we can assume that the thin cap layer is also strained. Because the cell temperatures were the same for both samples, we assume that the thin cap indium mole fraction should be $x = 0.2601$. The CL spectra indicate that the thin cap sample has a greater residual strain than the thick cap sample.

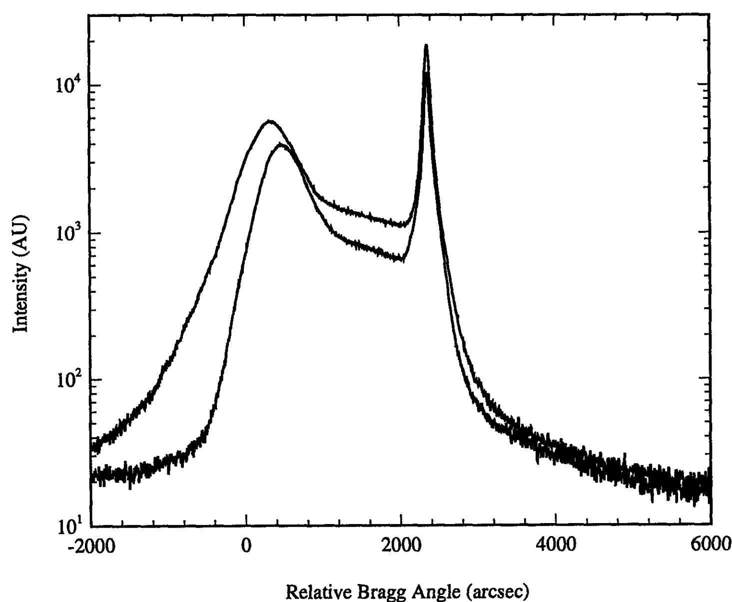


Figure 4-14: X-ray rocking curves of a linearly graded RBRTD. The two curves are measured 180^0 apart.

The linearly graded RBRTD consists of 0.5 μm GaAs, 3.0 μm linearly graded from GaAs to $In_xGa_{1-x}As$, 2.6 μm $In_xGa_{1-x}As$, the RTD layers, and 0.3 μm $In_xGa_{1-x}As$. The RTD consists of symmetric 10 nm undoped spacers, 2.1 nm AlAs barriers, and a 7.5 nm well. This structure completely fills the MIT-OEIC-3 DGWs. This sample was also grown at 470^0C.

Figure 4-14 shows the (004)-reflection x-ray rocking curves for the linearly graded RBRTD sample. The narrow peaks are the response of the substrate. The broad peaks correspond to $In_{0.2055}Ga_{0.7945}As$, with a bandgap of 1.140 eV. The presence of all indium percentages between 0% and 20.55% causes the slow rise in x-ray intensity with decreasing Bragg angle between

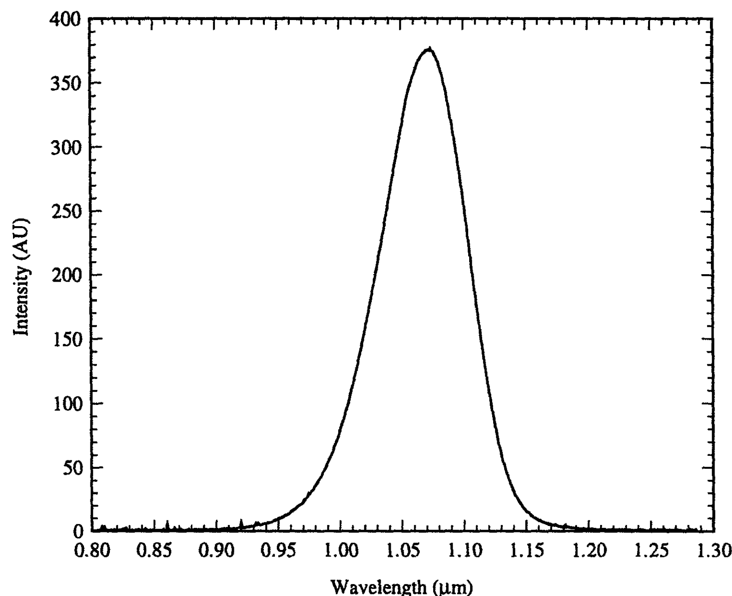


Figure 4-15: Cathodoluminescence spectrum of a linearly graded RBRTD. The peak wavelength is 1.075 μm and the spectrum was taken at 10 kV 1000×.

the substrate and $In_{0.2055}Ga_{0.7945}As$ peaks. This sample has very little epitaxial layer tilt.

Figure 4-15 shows the cathodoluminescence spectrum of the linearly graded RBRTD. The peak wavelength is 1.075 μm, corresponding to a fully relaxed bandgap of 1.155 eV. The x-ray and CL results for this sample shows the closest agreement of all the samples. The slightly larger bandgap of the CL response indicates that there is still a very small amount of residual strain left in the sample.

Sample	X-ray E_G (eV)	CL E_G (eV)	δE (eV)	$\epsilon_{residual}$
Single-step	1.108	1.255	0.147	-0.0411
Multiple-step, thick cap	1.060	1.109	0.049	-0.0141
Multiple-step, thin cap	1.060†	1.134	0.074	-0.0213
Linearly Graded	1.140	1.155	0.015	-0.0041

Table 4.2: Comparison of the experimental bandgap energies of RBRTDs obtained from x-ray and CL spectra. Compositions are calculated assuming complete relaxation of the buffer. The residual strain is derived from the difference between the x-ray and CL energies. Negative residual strain indicates that the strain is compressive. †Identical compositions are assumed for the multiple-step buffers.

Table 4.2 summarizes the bandgap energy values obtained for the four relaxed-buffer structures using the x-ray and CL spectra. Both values have been calculated assuming complete relaxation of the buffer, and therefore neither value is accurate. A six-scan orthorhombic x-ray analysis is necessary to get an accurate composition of the buffer layer. However, if the x-ray

determined composition is the correct one, the difference in energy can be related to the residual strain in the material. Though not wholly accurate, this analysis will yield a qualitative assessment of the relaxation capability of the various buffer structures.

The difference in bandgap of a relaxed and strained layer can be related to the residual strain in a layer by [53]

$$\delta E_{strain} = \left[2a\left(\frac{C_{11}-C_{12}}{C_{11}}\right) - b\left(\frac{C_{11}+2C_{12}}{C_{11}}\right)\right]\epsilon_{residual}, \tag{4.3}$$

where a is the hydrostatic deformation potential constant, b is the shear deformation potential constant, and C_{11} and C_{12} are the stiffness coefficients of the epitaxial material. Table 4.2 also summarizes the residual strain in each sample. Values for a, b, C_{11}, and C_{12} are taken from [29].

Residual strain in the layers will reduce the validity of the assumption that the buffers are fully relaxed, and will produce incorrect composition values. The x-ray and CL results indicate that none of the samples is completely relaxed. The residual strain calculations indicate that the samples with gradual increases in indium content, and hence gradual increases in strain, showed more relaxation. The single-step buffer was the least relaxed, followed by the multiple-step thin cap and the multiple-step thick cap, with the linearly graded enabling the greatest buffer relaxation. Equations 4.1 and 4.2 indicate a linear reduction in dislocation velocity with a decrease in strain and an exponential reduction in nucleation rate with a decrease in strain. The reduction in nucleation rate is the stronger of the two effects. In these samples, the reduction in nucleation rate is allowing the creation of longer misfit dislocation segments. Therefore, samples with lower strain are relaxing more.

4.4.2 Effect of Grading Method on Dislocation Density

Three techniques were used to measure threading dislocation density (TDD): transmission electron microscopy, defect revealing etches, and CL topographical maps. TEM is useful for studying high dislocation density structures. Both plan-view and cross-sectional transmission electron microscopy (PV-TEM and X-TEM) were used to evaluate the dislocation densities of the relaxed buffers. Because of the small sample size used in TEM, if no threading dislocations are observed, it can only be concluded that the TDD is less than $10^8 - 10^9$ cm^{-2}. Both etching studies and CL topographical maps are useful for studying low defect density structures, of the order of $10^5 - 10^6$ cm^{-2}.

In CL, an electron beam is used to generate electron/hole pairs within a sample. These carriers will nonradiatively recombine at a defect. Mapping the light emitted from the samples effectively maps the location of the defects. Because they have a direct bandgap, III-V materials are well suited to this technique. The generation depth of the electron/hole pairs is a function of sample material and beam energy. For these studies, the maximum generation depth is $\approx$ 1.6 μm. In the CL maps, threading dislocations appear as circles. Dark circles are most likely clusters of dislocations, and faint spots are single dislocations. Determination of TDD from the CL topographical maps required correlation with the TEM results for that particular sample. The X-TEM pictures were examined to find regions where multiple threads reach the surface of the epitaxial layers. A local TDD was calculated by multiplying the distance between the threads and the sample thickness, 300 nm. The CL e-beam spot size is $\approx$ 1 μm. From the local TDD, a threads/spot density was calculated. This value was then used as the dark spot TDD. The cumulative errors from the X-TEM and subjective count of the CL spots, this technique will only give an order of magnitude estimate of the TDD and is used to provide a qualitative estimate of the TDD.

Chromium trioxide and 1:8:160 H_2SO_4:H_2O_2:H_2O etching solutions were used to reveal the threading dislocations of the buffers. For each solution, the RTD active layers and some cap material were etched off. After etching, threading dislocations appear as pits. The pits were counted using an optical microscope. Neither etch proved to be a good defect-revealing etch. The chromium trioxide etch had been successfully used in p-type $In_xGa_{1-x}As$ samples, but had a much lower etch rate for the present n-type samples. The sulfuric acid based etch seemed to reveal more dislocations. It is reasonable to suspect that clusters of threading dislocations will appear as a single pit. Again, a "local" TDD can be calculated, and used to get a more accurate count of the threading dislocations in the sample. However, because of the difficulty in obtaining a good etch-pit sample, the validity of the etching data is questionable and therefore the local TDD calculations were not performed.

In X-TEM, the TDD was calculated by measuring the dislocation line length per unit volume. The measurements assumed a sample thickness of 3000 nm. In the PV-TEM studies, the TDD was calculated by counting the dislocations in the viewed area. Of the two TEM methods, PV-TEM is expected to give a more accurate TDD. Because of the limited sample size of X-TEM

as well as the uncertainty in the sample thickness, the error bars on the TDD obtained from X-TEM are large. X-TEM serves as a litmus test as to the presence of dislocations.

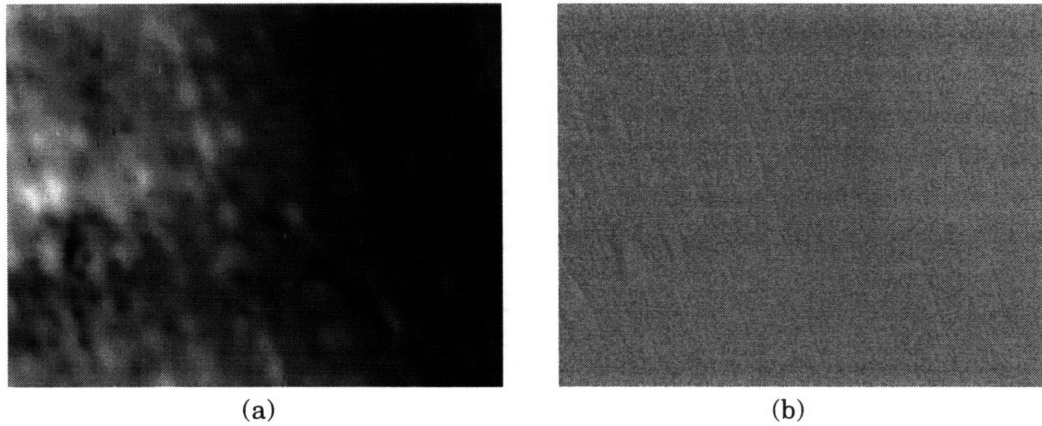


Figure 4-16: Surface maps of a single-step RBRTD. (a) CL map taken at 10 kV, 2500×, and a wavelength of 0.9980 μm. The map area is 36×46 μm^2. (b) SEM image of the same area taken at 2500×.

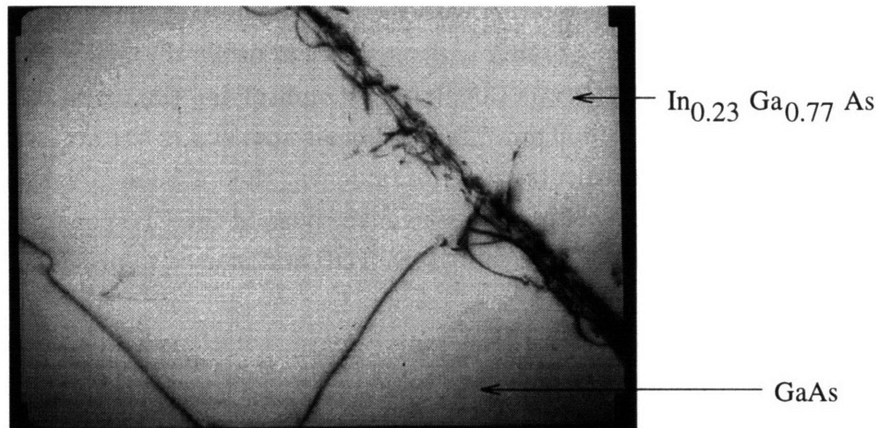


Figure 4-17: X-TEM of a single-step RBRTD. The dark lines are defects. The magnification is 60,000× and $\overline{G} = \langle 220 \rangle$.

Figure 4-16a shows the cathodoluminescence topographical map of the single-step RBRTD and Figure 4-16b shows an SEM of the same area. The CL map was taken at a beam energy of 10 kV, 2500× magnification, and at a wavelength of 0.998 μm. The SEM image was taken at a magnification of 2500×. The map was taken at the edge of the optimal spatial collection range and therefore there is a decrease in signal intensity at the edge of the map. Variations in intensity indicate relative differences in the dislocation density. The dark regions are probably clusters of threads. The mottled appearance of the sample indicates a high overall threading dislocation density. The SEM does not show the deformation expected with the presence of long misfit dislocations, further supporting the theory that relaxation in this sample is obtained

through short misfit dislocations and a high threading dislocation density.

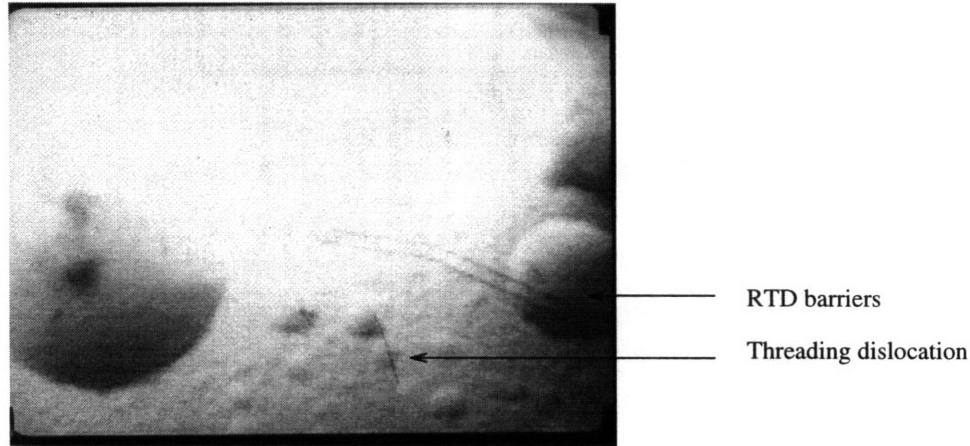


Figure 4-18: PV-TEM of a single-step RBRTD. The RTD barriers and a threading dislocation can be seen. The magnification is 20,000× and $\overline{G} = \langle 220 \rangle$. The bubbles are from localized differences in milling rates.

Figure 4-17 shows an X-TEM of the GaAs to $In_xGa_{1-x}As$ transition region. The magnification is 60,000× and $\overline{G} = \langle 220 \rangle$. X-TEMs reveal substantial numbers of misfit and threading dislocations in the step grade as well as dislocations penetrating both the RTD layers and the GaAs substrate. Figure 4-18 shows a PV-TEM of a single-step RBRTD. The magnification is 20,000× and $\overline{G} = \langle 220 \rangle$. PV-TEM samples are made by milling the sample from the substrate side. $In_xGa_{1-x}As$ and AlAs mill at different rates. AlAs mills faster, and as a result, rings are visible in the PV-TEMs. The outer ring is the substrate-side AlAs barrier and the inner ring is the surface-side AlAs barrier. In this PV-TEM, only part of a set of rings is seen. The bubbles present in the sample are also due to thickness variations which result from nonuniform milling. Figure 4-18 shows one threading dislocation. The thread appears as line because it rises from the substrate at an angle and its projection is visible from the top surface. Both the X-TEM and PV-TEMs of this sample showed a high number of heterogeneous nucleation sites at the surface of the sample. It is unclear what caused the nucleations. However, they do create large, complex tangles of dislocations.

The X-TEM results indicate that the TDD for this sample is 2.36×10^8 cm^{-2}. The lower and upper bounds on the X-TEM TDD are 6.14×10^7 and 6.14×10^9 cm^{-2}, respectively. Using PV-TEM, the calculated TDD is 1.2×10^7 cm^{-2}. The lower and upper bounds on the PV-TEM TDD are 5.15×10^6 and 2.09×10^7 cm^{-2}, respectively. The CL, CrO_3, and H_2SO_4 etching TDDs calculated without accounting for clusters of threads are 10^6, 10^5, and 10^6 cm^{-2} respectively. The TDDs obtained from the TEMs indicates that the CL and etching values are low. Unfortunately, an appropriate X-TEM sample to get a "local" TDD for the dark spots on the CL does not exist. The dislocations generated at the surface nucleations were too tangled to count and therefore were not included in the TEM TDD calculations. Thus the overall TDDs for this

sample are expected to be low.

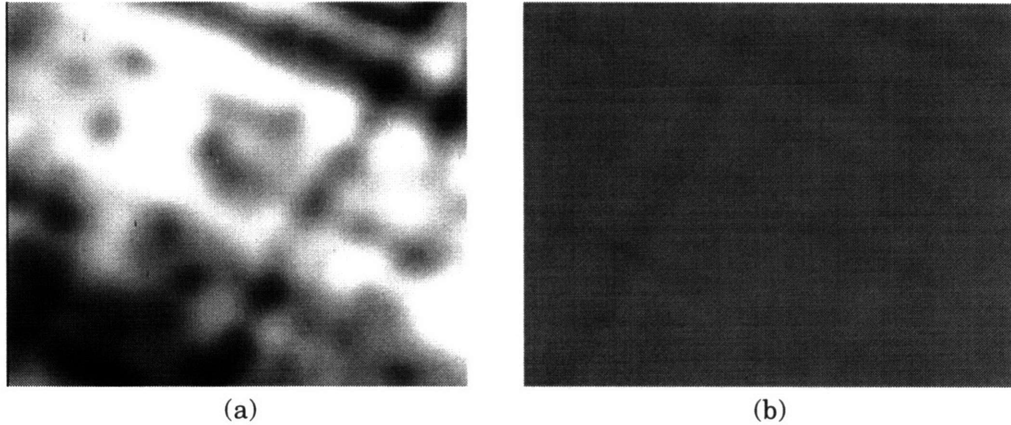


Figure 4-19: Surface maps of a multiple-step thick cap RBRTD. (a) CL map taken at 10 kV, 2500×, and a wavelength of 1.130 μm. The map area is 36×46 μm^2. (b) SEM image of the same area taken at 2500×.

Figure 4-19 shows the CL topographical map of the multiple-step, thick cap RBRTD and its associated SEM image, both at 2500×. The CL map e-beam energy was 10 kV. The expected generation depth of the injected carriers is 1.6 μm. Therefore, only features present half-way through the cap and higher should be seen in the CL. Very dark features in the CL map indicate that the defect lies close to the surface of the sample. A crosshatch pattern is visible in both images. In addition, there are small sharp dark spots, large diffuse dark spots, and dark bands visible on the CL map. The crosshatch pattern can be attributed to misfit dislocations, most likely occurring at the $In_xGa_{1-x}As$/AlAs interfaces of the RTD. Dark bands are probably multiple misfit dislocations in close proximity of one another. Dark spots are the CL signature of threading dislocations. In this sample, the sharp spots are most likely individual threads and the large, diffuse spots clusters of threads.

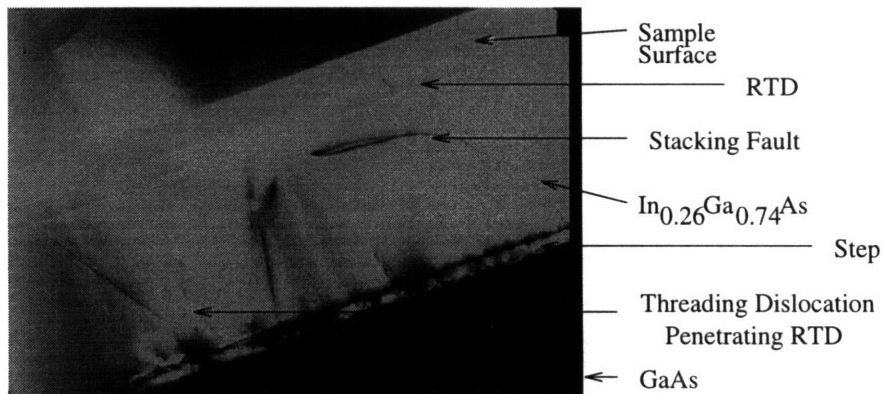


Figure 4-20: X-TEM of a multiple-step, thick cap RBRTD. The magnification is 12,000× and $\overline{G} = \langle 220 \rangle$.

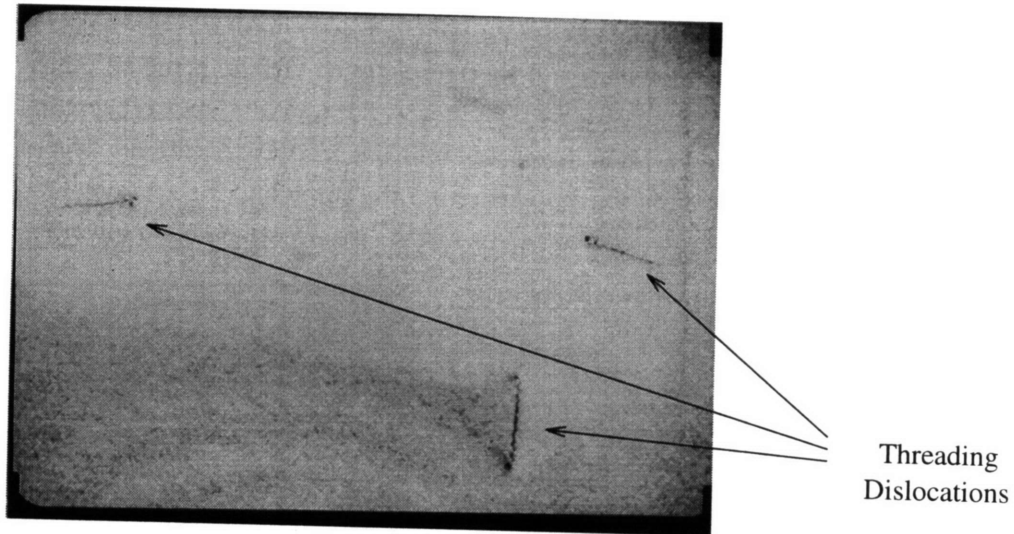


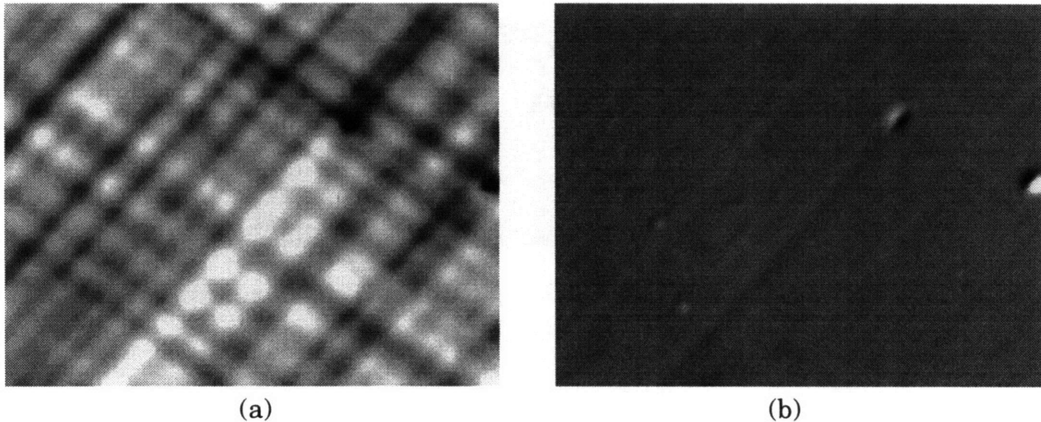
Figure 4-21: PV-TEM of a multiple-step, thick cap RBRTD. The magnification is 29,000× and $\overline{G} = \langle 220 \rangle$.

Figure 4-20 shows an X-TEM of the multiple-step, thick cap relax-buffer RTD at 12,000× magnification. The dark area on the lower right-hand corner of the picture is the GaAs substrate. Misfit dislocations are visible at the GaAs/$In_{0.19}Ga_{0.81}As$ and $In_{0.19}Ga_{0.81}As$/$In_{0.26}Ga_{0.74}As$ interfaces. Threading dislocations can be seen throughout the cap layers, including one which penetrates the RTD layers. Threading dislocations cause localized disruption of the RTD interfaces. Two phenomena are seen. In one situation, the RTD active layers will remain parallel, but strain fields will cause the RTD layers to wave. In the other, the RTD barrier and well layers on either side of a thread will not be aligned. The first situation should not affect the I–V characteristics of the RTD. The second can cause a localized difference in the RTD energy states, leading to a broadened RTD resonance. Figure 4-21 shows a PV-TEM of the multiple-step, thick cap RBRTD at 29,000× magnification. This particular PV-TEM shows only threading dislocations.

The TDD calculated using X-TEM is 2.56×10^8 cm^{-2}. The lower and upper bounds on the X-TEM TDD are 6.66×10^7 and 6.66×10^9 cm^{-2}, respectively. The TDD obtained from PV-TEM is 6.2×10^7 cm^{-2}. The lower and upper bounds on the PV-TEM TDD are 4.3×10^7 and 7.3×10^7 cm^{-2}, respectively. A "local" TDD of 66 threads/μm^2 was also obtained from X-TEM. Incorporating the effects of clusters of threads, a TDD of 10^7 cm^{-2} was obtained from the CL map. TDDs obtained from the CrO_3 and H_2SO_4 etches were 10^4 and 10^5 cm^{-2} respectively. There is some overlap in the X-TEM and PV-TEM TDD ranges. In addition, an order 10^7 cm^{-2} density is corroborated by the CL data.

Figure 4-22 shows the CL topographical map of the multiple-step, thin cap RBRTD and its associated SEM image, both at 2500×. A crosshatch pattern is clearly visible in both images. In this sample, the relaxed-buffer step interfaces lie 0.7358 and 0.9297 μm below the

sample surface. Misfit dislocations generated in the relaxed buffer regions will be within the penetration depth of the CL e-beam and therefore will be visible in the CL map. The darker lines are probably misfits lying at the RTD barrier/well interfaces and the gray lines are misfits in the relaxed buffer. Wide bands are probably multiple misfit dislocations. The response from the misfit dislocations obscures the response from the threading dislocations. In this sample, threading dislocations are predominantly seen at the intersection of two misfits.



(a) (b)

Figure 4-22: Surface maps of a multiple-step, thin cap, RBRTD. (a) CL map taken at 10 kV, 2500×, and a wavelength of 1.090 μm. The map area is 36×46 μm^2. (b) SEM image of the same area taken at 2500×.

Figure 4-23 shows an X-TEM of the multiple-step, thin cap buffer. The sample magnification is 60,000× and the strain conditions are optimized to show defects in the material. A large number of misfit dislocations are visible at the GaAs/$In_{0.19}Ga_{0.81}As$ interface, and threads propagate both into the epilayer and substrate from this interface. Misfits are also seen at the $In_{0.19}Ga_{0.81}As$/$In_{0.26}Ga_{0.74}As$ interface. A misfit can be seen running along the RTD active layers. The transition from misfit to threading dislocation can be seen at two places along the RTD. This figure also shows threading dislocations propagating to the surface of the sample.

Figure 4-24a shows a PV-TEM of the multiple-step, thin cap buffer. This sample includes the relaxed buffer, the cap, and the RTD layers. Both misfit and threading dislocations can be seen in the photograph. The proximity of the relaxed buffer to the surface made it difficult to distinguish threading dislocations from those that loop down towards the substrate – both appear as projections on the PV-TEM. Figure 4-24b shows a sample which has been further thinned. This sample contains only the cap and RTD layers. The nonuniform milling of the sample has created the previously mentioned ring structure. Misfits can be seen on both AlAs barriers. There is also a pair of dislocations that could cause the band response that is seen in the CL maps. The TEMs confirm the presence of misfit dislocations lying at the $In_{0.26}Ga_{0.74}As$/AlAs interfaces of the RTD.

A TDD of 6.8×10^8 cm^{-2} and a "local" TDD of 100 threads/μm^2 are obtained from the X-TEM. The lower and upper bounds on the X-TEM TDD are 1.8×10^8 and 1.8×10^9 cm^{-2}, respectively.

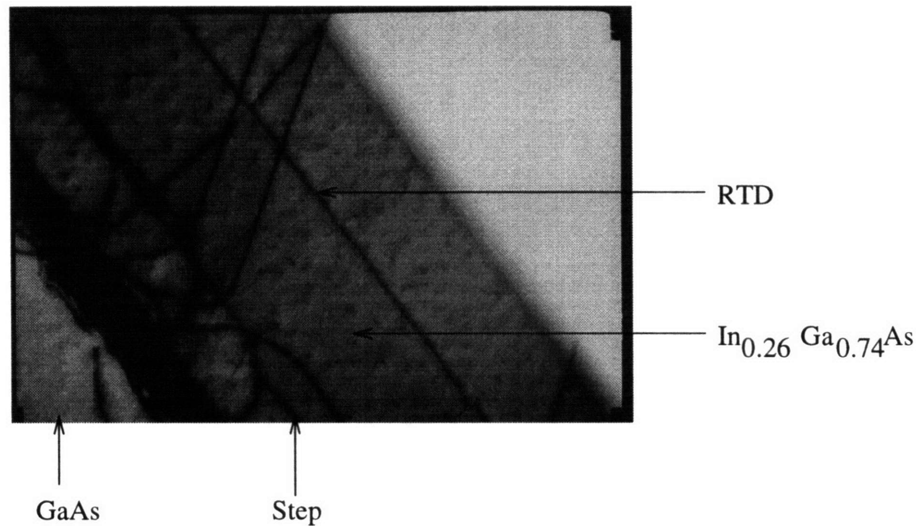


Figure 4-23: X-TEM of a multiple-step, thin cap RBRTD. The picture shows a large number of dislocation occurring at the initial GaAs/In_xGa_{1-x}As interface. The picture also shows a misfit lying along the RTD layers. Because the TEM strain conditions are optimized to show defects, the RTD layers are not visible. The magnification is 120,000× and $\overline{G} = \langle 220 \rangle$.

A TDD of 1.2×10^{7} cm^{-2} is obtained from the PV-TEM. The lower and upper bounds on the PV-TEM TDD are 5.2×10^{6} and 2.1×10^{7} cm^{-2}, respectively. A TDD of 10^{7} cm^{-2} is obtained from the CL map. The thin cap layer prevented the preparation of an etch-pit sample for this buffer. The X-TEM results indicate that this sample should have a high TDD. The CL and PV-TEM values are consistent with each other, but are an order of magnitude lower than the X-TEM. However, in both the PV-TEM and CL analyses, response from the misfit dislocation array obscures responses from threading dislocations. It would not be unreasonable to suspect that the PV-TEM and CL TDDs are low.

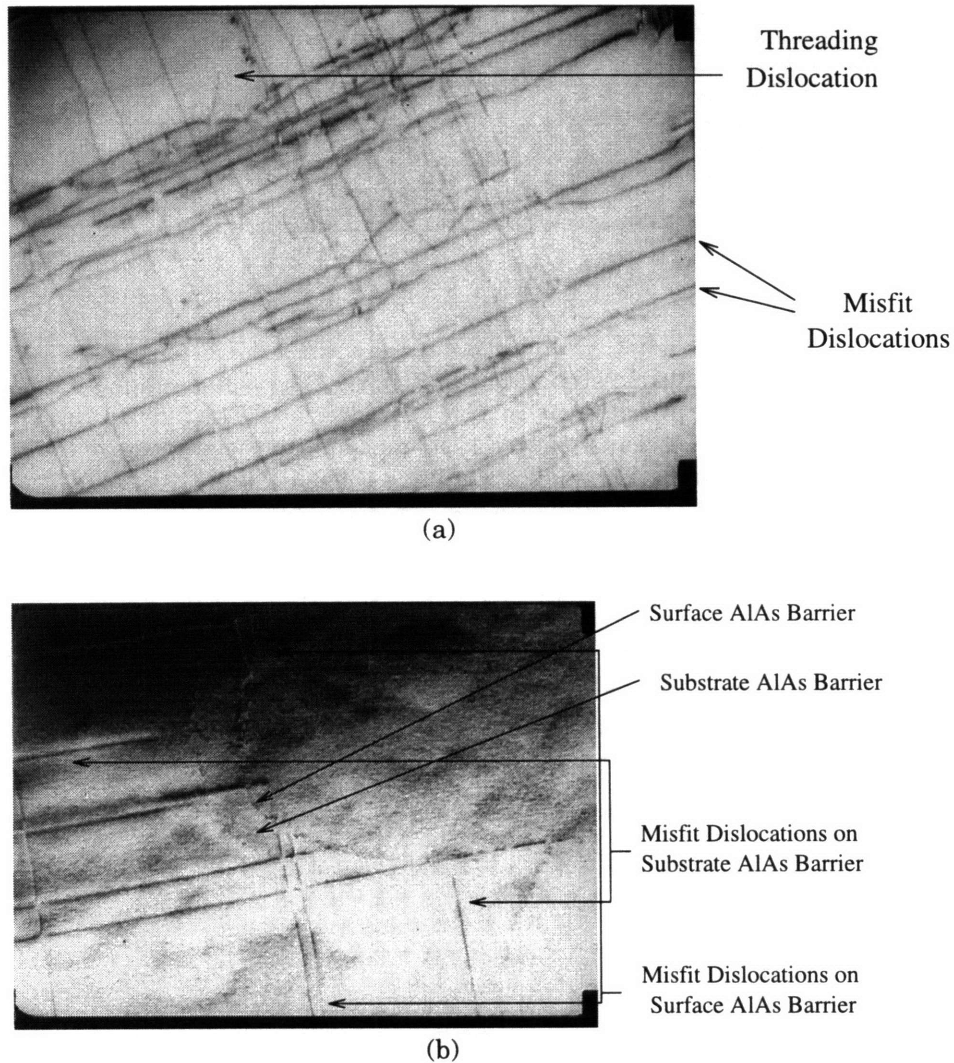


Figure 4-24: PV-TEMs of a multiple-step, thin cap RBRTD. In (a), the sample contains the relaxed buffer, cap, and the RTD layers. Both misfit and threading dislocations can be seen. The magnification is 29,000× and $\overline{G} = \langle 220 \rangle$. In (b), the sample has been further thinned and only contains the cap and RTD layers. Misfits lying on both RTD barriers can be seen. The magnification is 40,000× and $\overline{G} = \langle 220 \rangle$.

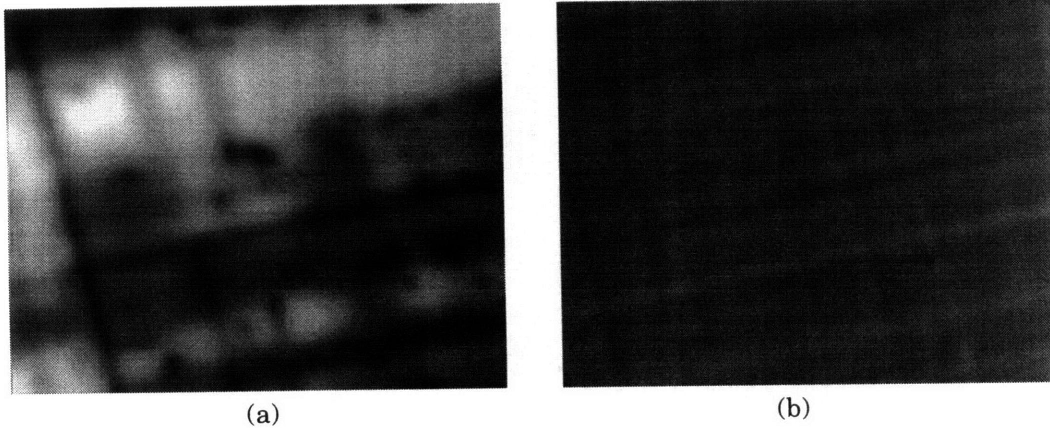


Figure 4-25: Surface maps of a linearly graded RBRTD. (a) CL map taken at 10 kV, 2500×, and a wavelength of 1.075 μm. The map area is 36×46 μm^2. (b) SEM image of the same area taken at 2500×.

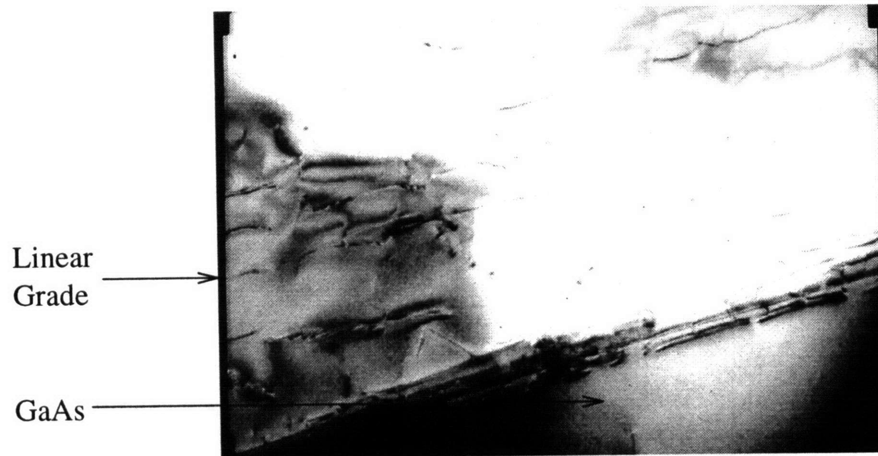


Figure 4-26: X-TEM of a linearly graded RBRTD. The picture shows misfit dislocations occurring throughout the graded layer. The magnification is 20,000× and $\overline{G} = \langle 220 \rangle$.

Figure 4-25 shows the CL topographical map of the linearly graded RBRTD and its associated SEM image, both at 2500×. Similar to the multiple-step thick cap sample, the linearly graded CL maps shows the presence of individual and clustered threads and RTD-layer misfit dislocations. A crosshatch pattern is visible in the SEM of the sample. This sample has extended areas of low background response, indicating a locally low TDD. The CL maps shows misfit dislocations ending in threading dislocations.

Figure 4-26 shows an X-TEM of the linearly graded region of the buffer. There is a high density of misfit dislocations at the initial GaAs/$In_xGa_{1-x}As$ interface. Both misfit and threading dislocations are visible throughout the graded region of the buffer. X-TEM pictures reveal a surprisingly high number of threading dislocations within the $In_xGa_{1-x}As$ cap layer as well. Figure 4-27 shows a PV-TEM of the linearly graded RBRTD. Two of the misfit dislocations are

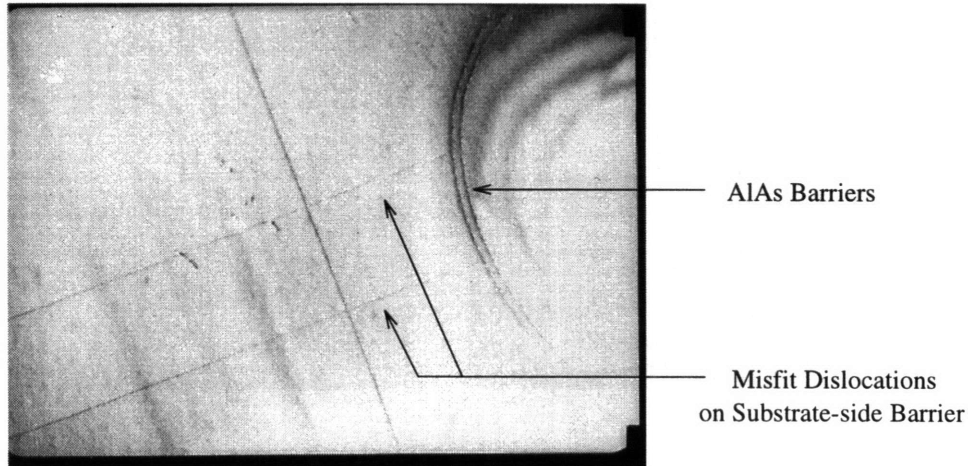


Figure 4-27: PV-TEM of a linearly graded RBRTD. The picture shows misfit dislocations lying on the substrate-side RTD barrier as well as some threading dislocations. The magnification is 14,000× and $\overline{\mathrm{G}} = \langle 220 \rangle$.

located at the substrate-side AlAs barrier.

A TDD of 7.73×10^{7} cm^{-2} and a "local" TDD of 71 threads/μm^2 are obtained from X-TEM. The lower and upper bounds on the X-TEM TDD are 2.0×10^{7} and 2.0×10^{8} cm^{-2}, respectively. The PV-TEM TDD is 1.8×10^{7} cm^{-2}. The lower and upper bounds on the PV-TEM TDD are 1.0×10^{7} and 2.8×10^{7} cm^{-2}, respectively. TDDs of 10^7, 10^4, and 10^5 cm^{-2} were obtained from the CL map, CrO_3 etch, and H_2SO_4 etch, respectively. For this sample, there is relatively good correlation between the adjusted CL, PV-TEM, and X-TEM TDD values.

Both the etching and CL techniques used to count the threading dislocations in the samples are of limited use. Selective chemical etching is useful to determine the TDD in low defect density samples. The spatial resolution of the technique is limited, and therefore it is difficult to distinguish single dislocations from tightly clustered multiple dislocations. Cathodoluminescence maps reveal both misfit and threading defects. In relaxed-buffer structures where a thick cap separates the strain relieving misfits from the e-beam generated carriers, the technique is useful to map threading dislocations. However, in these samples, the misfit dislocations present at the RTD active layer interfaces lie within range of the CL probe and obscure the response from the threading dislocations. In addition, the subjective nature of the "local" TDD reduces the accuracy of this method. For these structures, PV-TEM is the most reliable method to count the TDD. However, even PV-TEM can suffer from poor signal (threads) to noise (misfits) ratios, and can be misleading. The results of the PV-TEM, X-TEM, and CL calculations together provide an educated estimate of the TDD of each sample.

Table 4.3 summarizes the TDDs calculated using the different techniques. All samples show a higher TDD using X-TEM than PV-TEM. The PV-TEM TDDs of the single-step and multiple-step thin cap samples are considered low because of the difficulties involved in counting the threads in these samples. The multiple-step thin cap sample showed the highest X-TEM TDD.

Sample	X-TEM (cm^{-2})	PV-TEM (cm^{-2})	CL (cm^{-2})	CrO_3 (cm^{-2})	H_2SO_4 (cm^{-2})
Single-step	2.36×10^8	$1.2\times10^{7\dagger}$	10^6	10^5	10^6
Multiple-step, thick cap	2.56×10^8	6.2×10^7	10^7	10^4	10^5
Multiple-step, thin cap	6.8×10^8	$1.2\times10^{7\dagger}$	10^7	NA	NA
Linearly Graded	7.73×10^7	1.2×10^7	10^7	10^4	10^5

Table 4.3: Measured TDD of RBRTDs. A TDD could not be obtained for the multiple-step, thin cap sample using the etching techniques. † These numbers are low because of difficulties counting the threading dislocations.

The three thick-cap samples had comparable TDDs. The high TDD of the multiple-step thin cap sample is not surprising. A dislocation cannot end within a crystal. As a misfit dislocation increases in length, the threading segments associated with it move toward the edges of the crystal. If the movement is unimpeded, eventually the threading segments will be pushed out of the crystal leaving only a misfit dislocation. For thin epitaxial layers, the misfits have not had the time to grow in length, and therefore their associated threading segments are still stuck in the crystal.

The lack of substantial difference in the TDDs (both X-TEM and PV-TEM) of the single-step, multiple-step thick cap, and linearly graded samples is surprising. The three samples, in that order, have decreasing strain during the course of the buffer growth. This should lead to a corresponding reduction in defect nucleation in the samples, allowing those defects which do nucleate to maximize their misfit dislocation segment lengths. The experimentally obtained TDDs indicate that the effect of temperature on dislocation nucleation and propagation must also be considered. For a given nucleation activation energy, a reduction in temperature will increase the nucleation rate. That same reduction in temperature will decrease the dislocation velocity.

The experimental results corroborate the exponential vs. linear effects of temperature and strain on velocity in Equation 4.2. The effects counteract each other in altering nucleation rate. The beneficial effect of a slightly lower nucleation rate for linearly graded samples is reduced by the decrease in dislocation velocity. For these growth temperatures, our results indicate that there is no advantage to any particular buffer grading method.

4.5 High-PVCR RBRTD

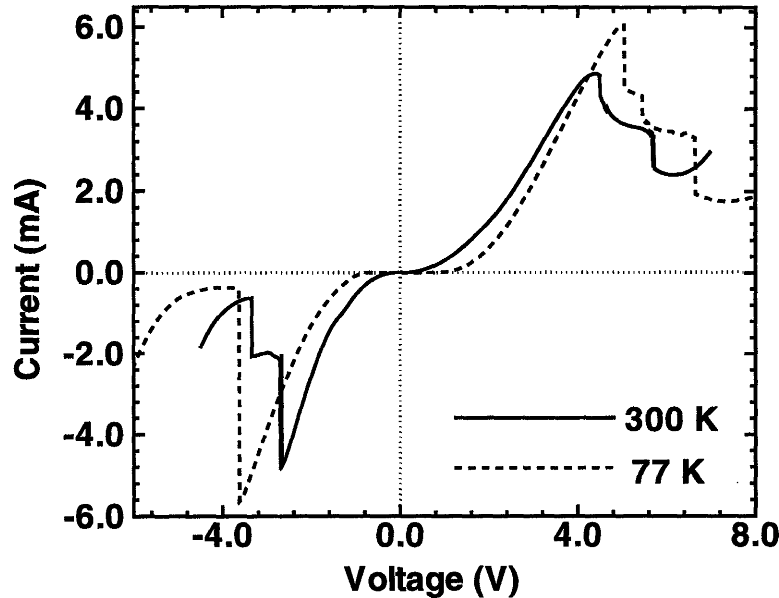


Figure 4-28: I–V Characteristics of a high-PVCR RBRTD.

Initial RBRTD growths used step buffers to grade from GaAs to $In_xGa_{1-x}As$. The step buffer structure was chosen to confine the dislocations formed at the GaAs/$In_xGa_{1-x}As$ interface to a small region close to the interface. Figure 4-28 shows the I–V characteristics of a $In_{0.22}Ga_{0.78}As$/AlAs RBRTD [47]. The buffer structure consists of four layers: 0.57 μm of n^+ GaAs (n = 1×10^{18} cm^{-3}), 0.55 μm of n- $In_{0.17}Ga_{0.83}As$ (n = 8×10^{17} cm^{-3}), 0.21 μm of n-$In_{0.22}Ga_{0.78}As$ (n = 8×10^{17} cm^{-3}), and 0.12 μm of n- $In_{0.22}Ga_{0.78}As$ (n = 6.5×10^{16} cm^{-3}). The diode consists of undoped, symmetric 6.2 nm $In_{0.22}Ga_{0.78}As$ layers, 2.1 nm AlAs barriers and a 5.0 nm $In_{0.22}Ga_{0.78}As$ well. The structure is capped with 0.2 μm of n- $In_{0.22}Ga_{0.78}As$ (n = 6×10^{16} cm^{-3}), 62.5 nm of n- $In_{0.22}Ga_{0.78}As$ (n = 8×10^{17} cm^{-3}), and 62.5 nm of n^+ $In_{0.22}Ga_{0.78}As$ (n = 8×10^{18} cm^{-3}). The GaAs buffer and the epilayers were grown at a substrate temperature of 580°C and 480°C, respectively. The V/III flux ratio was approximately three. The $In_{0.17}Ga_{0.83}As$ and $In_{0.22}Ga_{0.78}As$ layers were grown at 0.5 and 0.77 μm/hr, respectively. Mesa diodes with areas ranging from 25 to 900 μm^2 were processed using standard photolithography and wet etching techniques.

X-ray diffraction and low-temperature photoluminescence (PL) were performed on the sample. Figure 4-29 shows the (004)-reflection x-ray rocking curve. Because the two steps have very similar indium compositions, two distinct peaks for the buffer are not visible. The position of the broad peak corresponds well to simulated x-ray results assuming total relaxation of the $In_{0.17}Ga_{0.83}As$ and $In_{0.22}Ga_{0.78}As$ buffer layers. The 10 K PL data, shown in Figure 4-30 has a strong peak at 1.2 eV. If complete relaxation is assumed, the PL peak corresponds

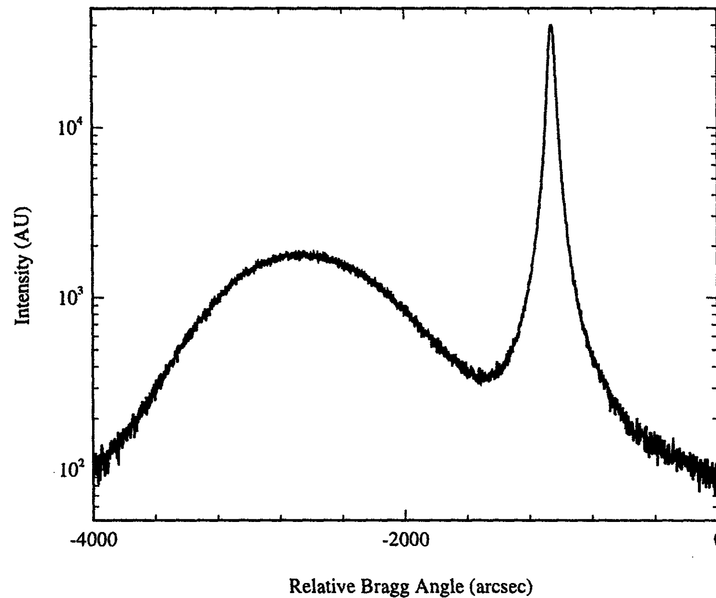


Figure 4-29: X-ray rocking curve of a high-PVCR RBRTD.

to $In_{0.21}Ga_{0.79}As$, in good agreement with the x-ray data. The discrepancy between the two characterizations indicates that there is still some residual strain in the buffer. Both material characterizations confirm the composition and relaxed nature of the buffers.

The I–V characteristics of the devices were measured at 300 and 77 K. Smaller resonance voltages and higher PVCRs were measured for negative applied biases. The asymmetry in I–V characteristics can be attributed to the difference in widths of the contact regions adjacent to the double-barrier structure. Consistent measurements of the positive resonance were difficult because the high power required to reach the resonance often destroyed the device. The maximum peak current density was 22.8 kA/cm^2. The maximum PVCR measured was 13:1 at 300 K and 27.5:1 at 77 K.

Dislocations can be optically observed in the upper epitaxial layers. The good intrinsic performance of the devices indicates that resonant-tunneling structures are robust and can withstand the presence of some dislocations within the active layers. It is possible that the dislocations are serving as electron traps, and that the presence of dislocations combined with low doping densities increases the resistivity of the contact layers. Similar effects have been observed in optical detectors in which carrier transport was perpendicular to the buffer/substrate interface [38]. The PVCR and current density of this RBRTD are suitable for circuit integration. However, the resonance voltages far exceed those necessary for RTD-EFET SRAM applications. An increase in doping density of the contact layers is expected to reduced the series resistance of the structure. This structure demonstrates the need to elucidate the effects of relaxed buffers on the series resistance of RTDs.

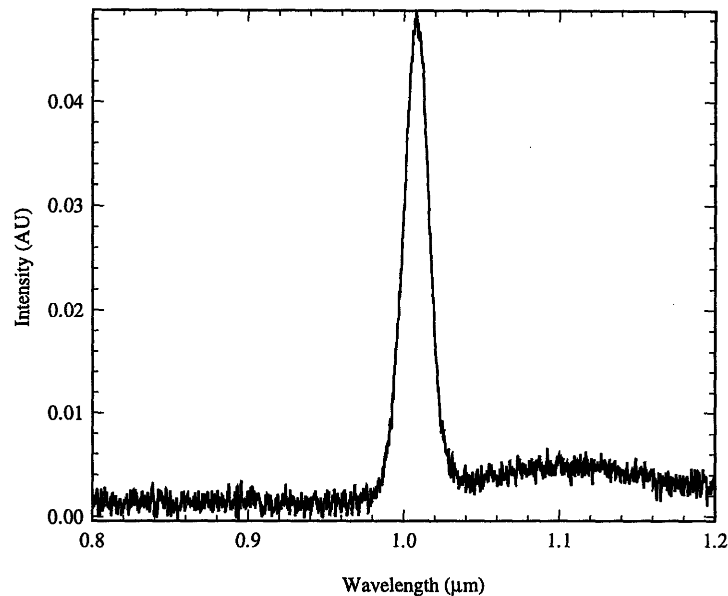


Figure 4-30: 10 K PL spectrum of a high-PVCR RBRTD.

4.6 Series Resistance of RBRTDs

Integration of RTDs with commercial GaAs circuits will require that the device current flow perpendicular to the growth interface. The location of the substrate side contact to the RTD will determine whether current will flow through the relaxed buffer. In situations where the contact lies on the substrate, current will flow through the buffer and in situations where the contact lies on a layer between the buffer and the active device layers, it will not. If the relaxed buffer adds substantial series resistance to the RTD, the latter contact scheme must be used. The purpose of this study is to assess the effect of transport through a relaxed buffer on RTD performance with specific focus on identifying the optimum contact topology for RBRTD-EFET integration.

A series of RTDs was grown in which the only material parameter varied among devices was the doping of the contact immediately adjacent to the diode. The indium content of the epitaxial layers as well as their total widths were held constant. The series consists of a 0.12 μm n^+ GaAs buffer (n=2×10^{18} cm^{-3}), 0.2 μm of n^+ $In_{0.11}Ga_{0.89}As$ (n=2×10^{18} cm^{-3}), 0.2 μm of $In_{0.27}Ga_{0.73}As$ with variable doping, undoped resonant-tunneling structure, and 0.23 μm $In_{0.27}Ga_{0.73}As$ with variable doping. The resonant-tunneling structure consists of undoped, symmetric 4.14 nm $In_{0.27}Ga_{0.73}As$ spacer layers, 1.2 nm AlAs barriers and a 3.39 nm $In_{0.27}Ga_{0.73}As$ well. Table 4.4 lists the individual doping for each sample. For all samples the GaAs buffers were grown at a substrate temperature of 580°C and all other layers were grown at 480°C. As with previous relaxed-buffer growths, the surface of all samples were crosshatched, with striations in the $\langle 110 \rangle$ directions.

7089	7090	7091
		83.3 nm 3×10^{18} cm^{-3}
0.23 μm 3×10^{18} cm^{-3}	0.146 μm 3×10^{18} cm^{-3}	73.3 nm 1.5×10^{17} cm^{-3}
	73.3 nm 1.5×10^{17} cm^{-3}	73.3 nm 1.5×10^{16} cm^{-3}
RTD	RTD	RTD
	66.7 nm 1.5×10^{17} cm^{-3}	66.7 nm 1.5×10^{16} cm^{-3}
0.2 μm 3×10^{18} cm^{-3}	0.133 μm 3×10^{18} cm^{-3}	66.7 nm 1.5×10^{17} cm^{-3}
		66.7 nm 3×10^{18} cm^{-3}
0.32 μm 3×10^{18} cm^{-3}	0.32 μm 3×10^{18} cm^{-3}	0.32 μm 3×10^{18} cm^{-3}
n$^+$ substrate	n$^+$ substrate	n$^+$ substrate

Table 4.4: Epitaxial structure of the RBRTD doping series.

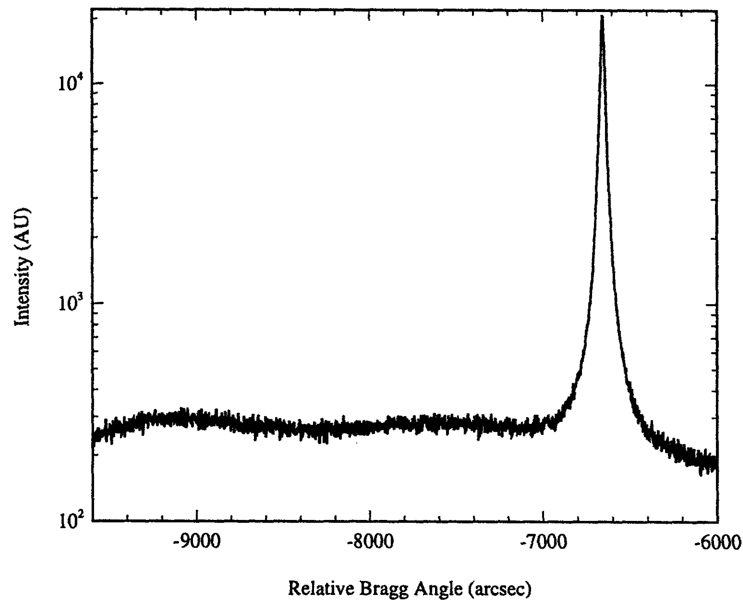


Figure 4-31: X-ray rocking curve of sample 7089. The sharp peak is the response from the substrate and the two smaller peaks indicate relaxed-buffer step compositions of 11% and 27% indium.

X-ray diffraction was performed to determine the indium compositions listed above. The x-ray rocking curves were measured for the (004) reflection and did not account for epitaxial layer tilt. The x-ray results from 7089 are fairly weak. This is probably due to a sample alignment problem. The peaks in the x-ray data indicate an intermediate $In_{0.11}Ga_{0.89}As$ layer and a final $In_{0.27}Ga_{0.73}As$ buffer. Based on the relaxation data obtained previously, we expect this sample to be underrelaxed because it has thin epitaxial layers.

Mesa diodes ranging from 25 to 900 μm^2 were processed using standard photolithography

and wet etching techniques. Alloyed AuGe/Ni/Au was used to contact the RTDs. Samples were measured using a HP4145B configured for a four-point probe method. To identify the contribution of the buffer to the total voltage drop across the structure, two measurements were made. In the first, method A, current was forced from the emitter contact to the backside substrate contact, and the voltage was monitored at these same points. In the second measurement, method B, the current was forced from the emitter contact to the backside substrate contact, but the voltage was monitored at the emitter and surface substrate contact. Comparison of the resonance voltages for these situations will reveal how much of the resonance voltage of the first measurement is dropped across the buffer.

All three samples in the series showed resonances for negative voltages. Only sample 7089 showed a positive resonance. Figures 4-32, 4-33, and 4-34 show I–V characteristics of 25 μm^2 devices on samples 7089, 7090, and 7091, respectively, for both measurement methods. As expected, the negative resonance voltage of sample 7090 is higher than sample 7089. Sample 7090 was substantially less stable than 7089, and only 25 μm^2 devices reliably showed the resonance. Sample 7091 showed an additional increase in resonance voltage. This sample was not robust at all. Table 4.5 summarizes the performance of all the samples.

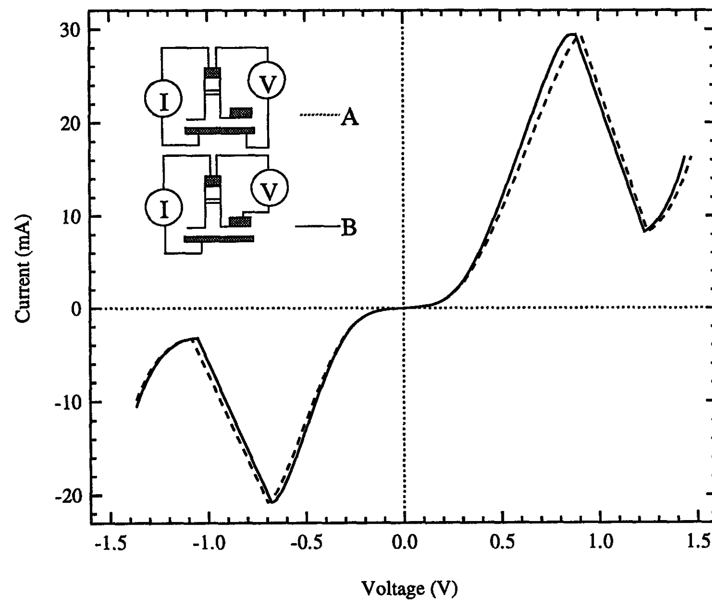


Figure 4-32: I–V characteristics of a 25 μm^2 sample 7089 RBRTD showing the series resistance of the buffer. Method A (dashed line) includes the effects of the relaxed buffer and method B (solid line) does not. This sample has peak voltages compatible with SRAM circuit applications.

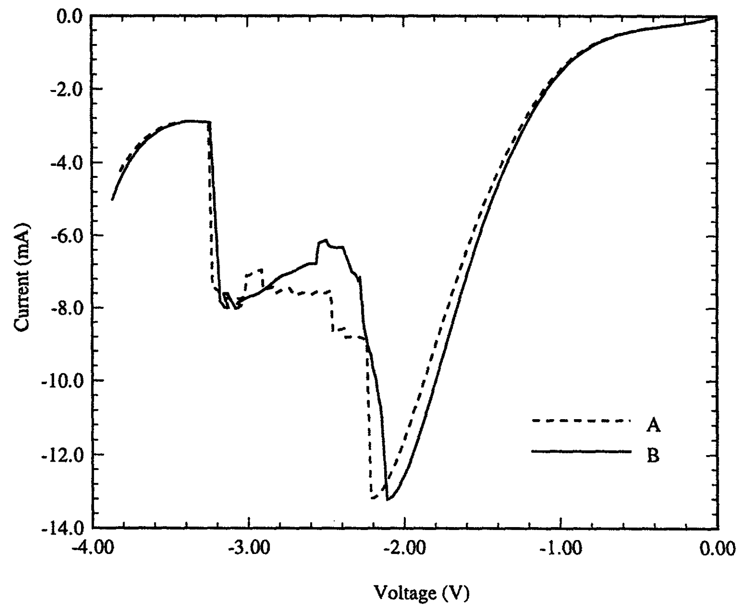


Figure 4-33: I–V characteristics of a 25 μm^2 sample 7090 RBRTD showing the series resistance of the buffer. Method A (dashed line) includes the effects of the relaxed buffer and method B (solid line) does not.

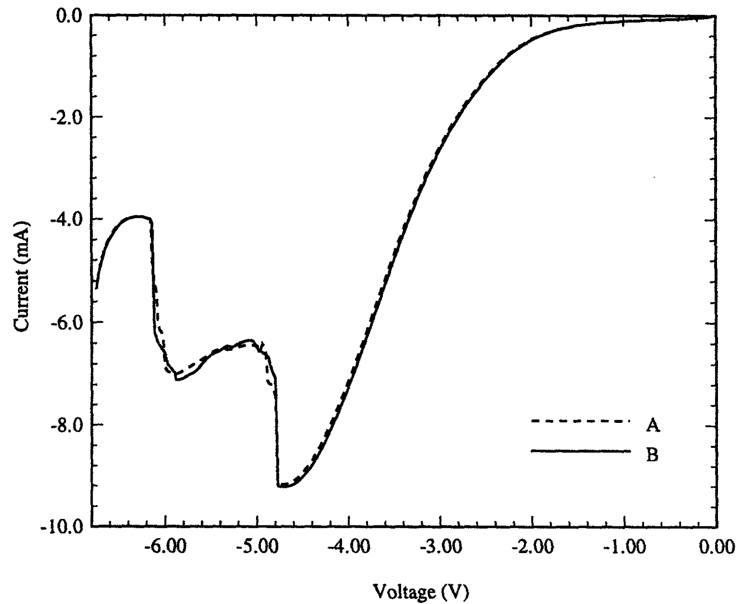


Figure 4-34: I–V characteristics of a 25 μm^2 sample 7091 RBRTD showing the series resistance of the buffer. Method A (dashed line) includes the effects of the relaxed buffer and method B (solid line) does not.

Sample	Test Method	V_{peak} (V) Ave.	V_{peak} (V) Min.	J_{peak} (kA/cm^2) Ave.	J_{peak} (kA/cm^2) Max.	PVCR Ave.	PVCR Max.
7089	A	-0.807	-0.678	-1.01×10^5	-1.33×10^5	4.28	6.31
7089	B	-0.723	-0.678	-1.01×10^5	-1.33×10^5	4.33	6.40
7089	A	0.892	0.842	1.16×10^5	1.22×10^5	2.96	3.54
7089	B	0.871	0.811	1.21×10^5	1.34×10^5	2.45	3.56
7090	A	-2.18	-2.01	-5.18×10^4	-7.30×10^4	3.57	4.84
7090	B	-2.13	-1.98	-5.19×10^4	-7.34×10^4	3.58	4.85
7091	A	-4.71	-4.55	-4.34×10^4	-5.07×10^4	2.21	2.32
7091	B	-4.71	-4.67	-5.13×10^4	-6.00×10^4	1.67	2.33

Table 4.5: RBRTD doping series device statistics. Method A includes the effects of the relaxed buffer and method B does not.

The lack of symmetry in the electrical characteristics of the series indicates that despite original intentions, the epitaxial structures of the samples are not entirely symmetric. The low PVCR and high peak current density of these structures can be attributed to thinner than intended AlAs barriers. Of the three sample, only sample 7089 has peak voltages compatible with SRAM circuit applications.

The voltage drop across the entire structure, V_{app}, is the sum of voltage drops across the emitter accumulation region, V_{acc}, the undoped tunneling structure, V_{RTD}, the collector depletion region, V_{dep}, and voltage drops due to the resistance of the buffer layer, V_{buffer}, and the contacts, V_{contact}.

$$V_{app} = V_{acc} + V_{RTD} + V_{dep} + V_{buffer} + V_{contact} \tag{4.4}$$

The I–V characteristics of the samples indicates that there is a small amount of voltage dropped across the relaxed buffer. In all cases, the voltage drop difference was less than 100 mV, and in most less than 50 mV. The only differences in V_{app} for measurement methods A and B could be due to a difference between the back-side substrate and top-side substrate contacts and the relaxed buffers. Because the cell temperatures and growth times for the samples were the same and the samples were processed at the same time, V_{RTD} and V_{contact} should be the same for all of the samples. V_{acc} and V_{dep} will change from sample to sample. (Values for V_{acc}, V_{dep}, and V_{RTD} can be calculated using a self-consistent Poisson solver to calculate the potential as a function of position for each structure.)

The structures studied all had heavily-doped relaxed buffers. The experimental results indicate that there will be a certain amount of voltage dropped across the relaxed buffer in a RBRTD. However, in the three samples studied, this voltage was consistently less than 100 mV. Such a voltage differential can be designed into the memory cell, allowing contact to the RTD to occur below the relaxed buffer [54]. This simplifies the EoE process flow because it enables the use of implanted DGWs. In implanted DGWs, contact to the RBRTD is made

through the S/D implant of the dielectric growth well. This simplifies the design of the MESFET circuits because an extra bond pad to provide access between the MESFETs and the RTDs is not necessary. In addition, it eliminates the metallization step required to make a second contact, in the SRAM case the storage node contact, to the RTDs. Based on these results, RBRTDs used in the integrated memory cells will have heavily-doped relaxed buffers. The designs for RBRTD-based circuits will included margins for the buffer voltage drop and the desired contact topology for RBRTDs will require current flow through the buffer. The capacitive parasitic element of this contact structure will be evaluated as part of the integrated memory cells. But, these results indicate that the resistive parasitic element of this simplified contact topology can be tolerated. It should be noted, however, that these studies were done on bulk RTDs, not integrated RTDs. This analysis does not include the parasitics contributed by the integrated circuit.

5

Characterization of Monolithically Integrated RBRTDs

Multiple-step and linear grade relaxed-buffer structures were grown on MIT-OEIC-3 ICs. Both electrical and material characterizations were performed on the ICs and their associated epi-ready substrate (ERS) samples to evaluate the quality of the epitaxial material grown on both substrates. The specific issues addressed were:

- Is there a difference in epitaxial material quality between the IC and the ERS?
- Is there a difference in epitaxial material grown on implanted and nonimplanted regions of the IC?
- How much variation is there in RBRTD performance across the IC?
- Is there any difference in RBRTD performance between the IC and the ERS?

In addition, the IC circuit degradation resulting from the extended MBE growth time-temperature cycle was also evaluated. These issues have implications for the design of RTD-EFET SRAMs, primarily in ensuring a robust cell design and in handling RTD variations across an SRAM. Sections 5.1.1 and 5.1.2 evaluate the quality of IC and ERS material. Section 5.2 reviews the degradation in the electronics suffered during MBE growth. The performance of integrated RBRTDs is covered in Sections 5.3.1 and 5.3.2. The atomic force microscopy measurements presented in this chapter were performed in collaboration with J.L. Pan of the MIT Department of Electrical Engineering and Computer Science. The relaxed buffer cathodoluminescence measurements and data analysis presented in this chapter were performed in collaboration with Prof. E.A. Fitzgerald and M.T. Bulsara of the MIT Department of Materials Science and Engineering.

5.1 Material Characterization of Integrated RBRTDs

5.1.1 IC Substrate Quality

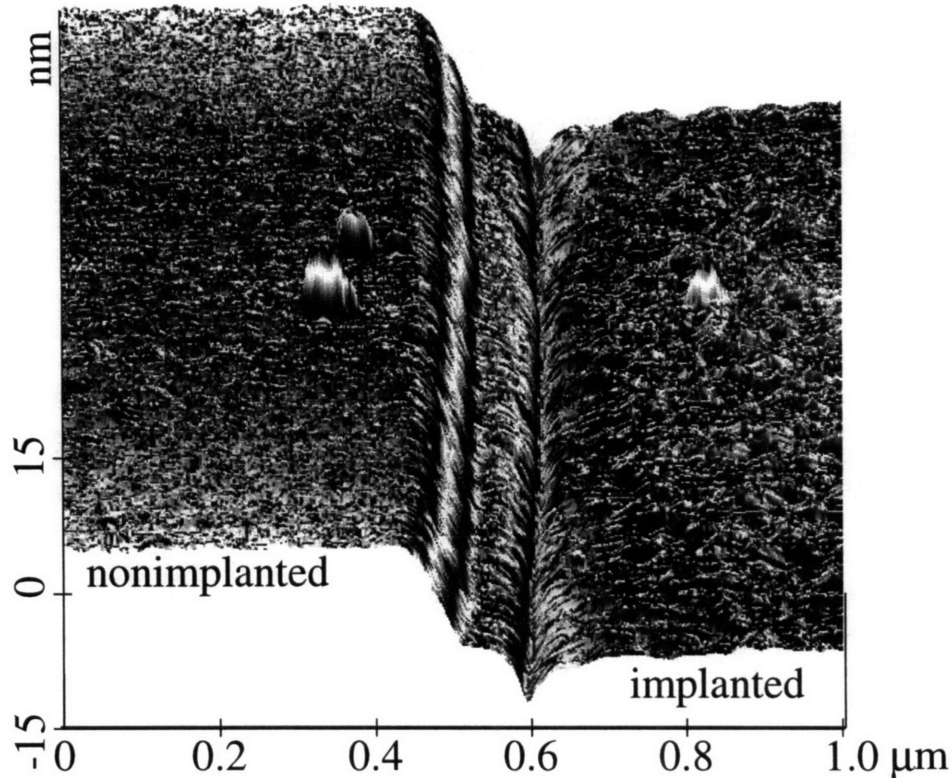


Figure 5-1: AFM 3-D surface map of implanted and nonimplanted DGW substrates.

The quality of an epitaxial layer is very dependent on its substrate. Because the IC substrate has seen repeated implantation and etching steps, it is reasonable to suspect that the growth surface in the DGWs could be rougher than typical ERS wafers. Figure 3-16 showed the profile of the IC substrate. The nonimplanted and implanted material have median height variations of $\approx$ 0.3 and 0.5 nm respectively. Figure 5-1 is an atomic force micrograph of the surface of both regions. The trench in the transition from the nonimplanted to implanted regions is an artifact generated by the convolution of the atomic force microscope (AFM) needle and the sample step. Both regions have seen a light p-type implant. The implanted regions have seen further n-type implantations. The nonimplanted surfaces have only seen one etch and fewer implantations, and therefore are smoother than the implanted surfaces. Monolayers for the $In_xGa_{1-x}As$ system range from 0.2827 to 0.3029 nm. A typical epi-ready substrate has height variations on the order of 0.3 nm, about 1 monolayer. The surface of the implanted IC substrate is definitely rougher than that of an epi-ready substrate.

The threading dislocations present at the surface of a wafer will serve as nucleation sites for dislocations in subsequent epitaxial layers. The threading dislocation density (TDD) of wafers

is specified in terms of an etch pit density (EPD). We use two-inch, epi-ready GaAs substrates with EPDs of less than 100 cm^{-2} for n^+ and less than 1500 cm^{-2} for semi-insulating wafers. Vitesse uses four-inch semi-insulating substrates with an average EPD of 100,000 cm^{-2}. The higher EPD of the IC substrates will lead to higher TDDs in the IC epitaxial material. The rougher starting surface and higher TDD of the IC substrates are expected to reduce the quality of the epitaxial material grown on the ICs as compared to material grown on epi-ready substrates.

5.1.2 IC Epitaxial Material Quality

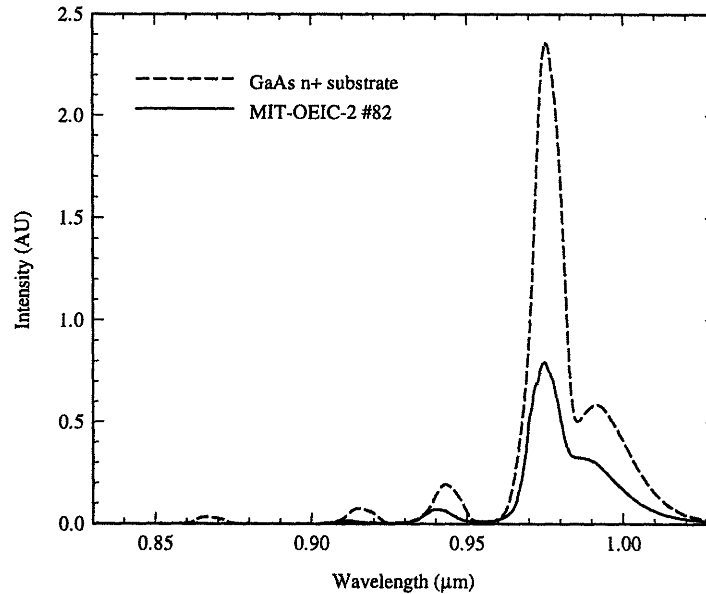


Figure 5-2: Comparison of the 10 K PL spectra of an $In_{0.2}Ga_{0.8}As/GaAs$ multiple-quantum well structure grown on an MIT-OEIC-2 chip and an ERS. Because the PL spot size was larger than the IC DGW, the intensities are not comparable. Data from [24].

Relaxed buffers complicate the evaluation of material quality by introducing additional misfit and threading dislocations. Therefore, initial characterization of the quality of the epitaxy grown on the ICs was performed on lattice-matched structures. Figure 5-2 shows the 10 K PL spectra of an $In_{0.2}Ga_{0.8}As/GaAs$ multiple-quantum well structure grown on an MIT-OEIC-2 chip and an ERS [24]. Because the PL spot size was larger than the IC DGW, the intensities are not comparable. The structure has quantum wells of 3.0, 5.6, 8.3, and 16.7 nm. The well width increases with distance from the substrate. Both spectra show the response of three of the four quantum wells. The highest wavelength peak corresponds to the bandgap of $In_{0.2}Ga_{0.8}As/GaAs$. The IC spectra is taken in a 100×400 μm silicon-doped DGW.

Figure 5-3 shows the room-temperature cathodoluminescence (CL) spectra of the same IC

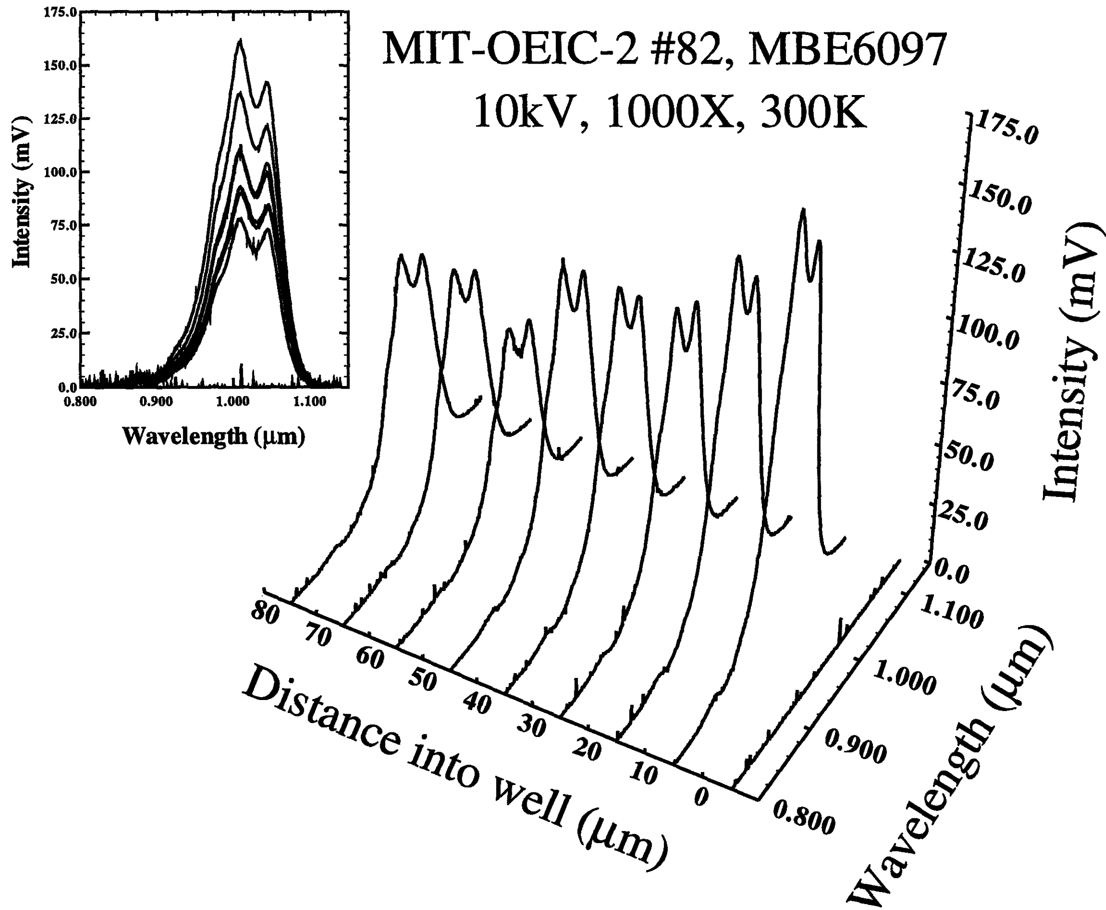


Figure 5-3: Comparison of the room-temperature CL spectra of an $In_{0.2}Ga_{0.8}As/GaAs$ multiple-quantum well structure grown on an MIT-OEIC-2 chip as a function of position within a 100×400 μm DGW. The inset compares the peak wavelengths of all of the spectra.

as a function of position across a 100×400 μm DGW. The spectra show the response from all four quantum wells (λ = 0.8750, 0.9025, 0.9750, and 1.005 μm) and the $In_{0.2}Ga_{0.8}As$ bandgap (λ = 1.040 μm). The strongest responses are from the bandgap and the widest quantum well. The inset shows that the peak wavelengths of the spectra do not vary as a function of position within the DGW. The spectra indicate that the material is not varying in composition within the DGW. However, the difference in intensity of the spectra indicates a variation in defect density within the DGW. In addition, the spectra indicate that good material exists within 5 μm of the DGW edge. The spectrum at -5 μm is a reference taken on the dielectric 5 μm outside the DGW.

Figure 5-4 shows the room-temperature CL spectra of an $In_{0.1}Ga_{0.9}As/GaAs$ multiple-quantum well structure grown on an MIT-OEIC-3 chip as a function of position within a 100×100 μm DGW and within the photonic IC DGW (the large stripe across the chip). The

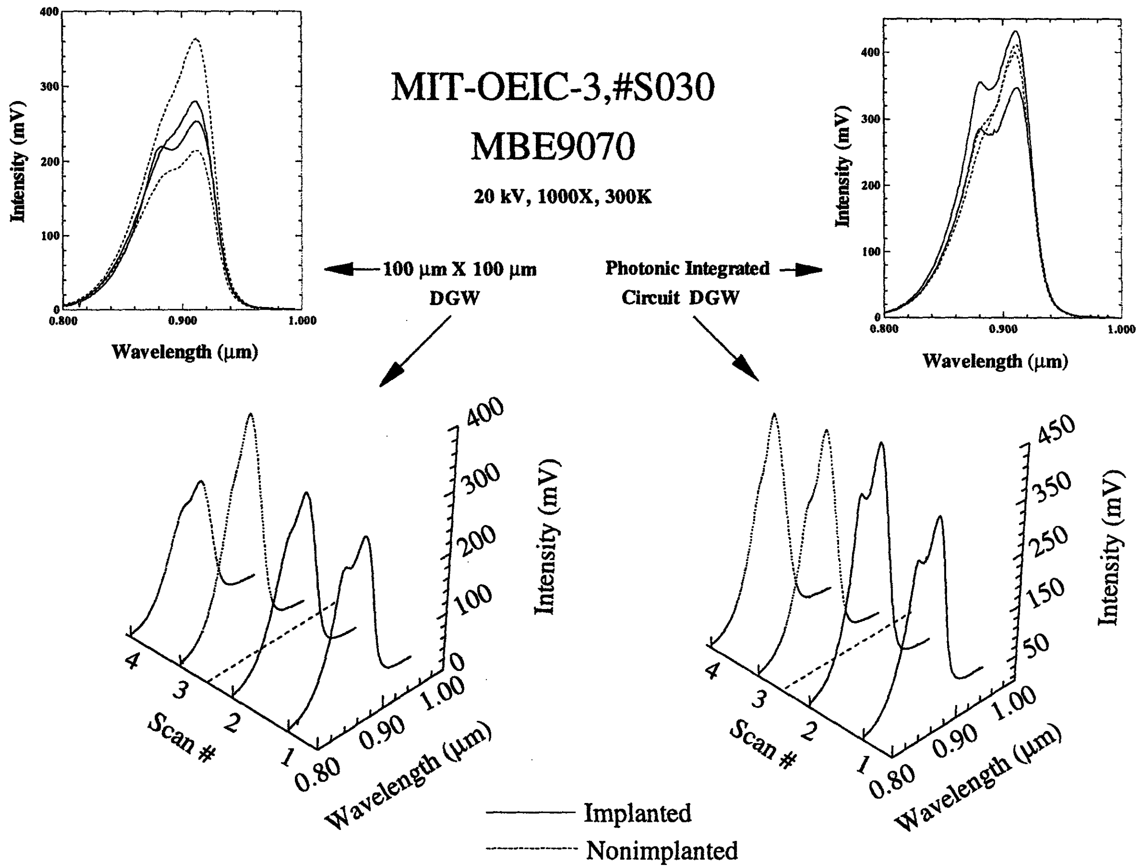


Figure 5-4: Comparison of the room-temperature CL spectra of an $In_{0.1}Ga_{0.9}As/GaAs$ multiple-quantum well structure grown on an MIT-OEIC-3 chip as a function of position within a 100×100 μm DGW and the photonic IC DGW. Both insets compare the peak wavelengths of spectra taken within the same DGW.

responses from the $In_{0.1}Ga_{0.9}As$ bandgap (λ = 0.8800 μm) as well as the first state in the quantum well (λ = 0.9100 μm) are seen. For this chip, the spectra are compared as a function of substrate doping. For both DGWs, scan 1 is 5 μm from the edge of the DGW. The scans are spaced $\approx$15 μm apart. The peak wavelengths do not shift as a function of substrate doping. As with the $In_{0.2}Ga_{0.8}As/GaAs$ sample, the spectra vary in intensity as a function of position and substrate doping, but not consistently. Again, this indicates a variation in defect density as a function of spectrum position.

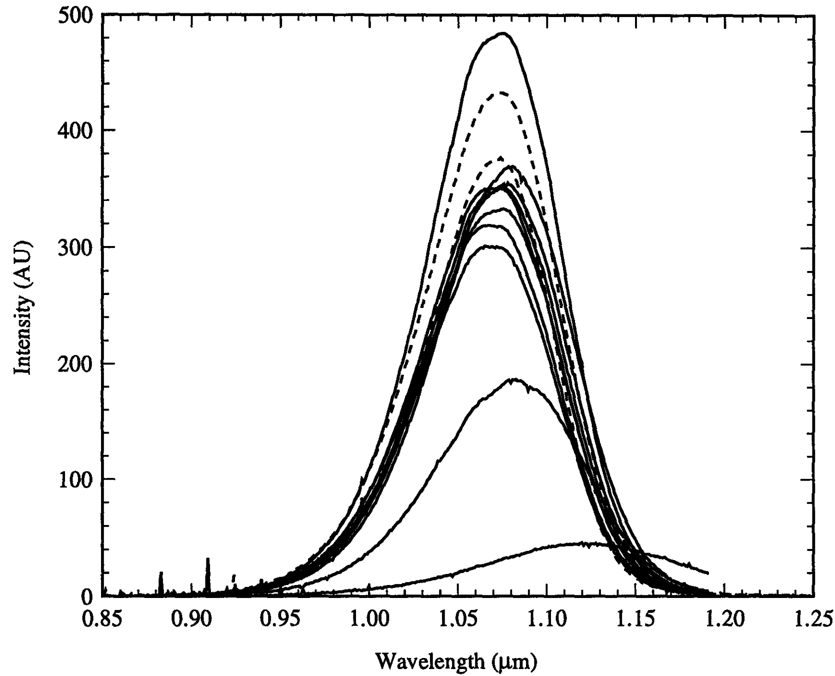


Figure 5-5: CL spectra of a linearly graded RBRTD grown on an ERS (dashed lines) and a MIT-OEIC-3 IC (solid lines). The scans were taken at a number of positions, and are overlapped here for comparison of the peak wavelengths. There is a difference in the peak wavelength of the scans on the two substrates. The spectra are taken at 10 kV and 1000×.

Figure 5-5 shows the room-temperature CL spectra of a linearly graded RBRTD grown on an MIT-OEIC-3 and n-type ERS. The solid lines are spectra from the IC and the dashed lines are the spectra from the ERS. The scans compare the peak wavelength of the spectra taken at different positions. Comparison of the spectra shows that there is a difference in the peak wavelengths of the material grown on the IC and the ERS. The ERS material peak wavelength is $\lambda = 1.075$ μm. The IC material peak wavelength is slightly higher at $\lambda = 1.085$ μm. Figure 5-6 shows the variation in CL spectra as a function of substrate and position within a DGW. There is no difference in peak wavelength between the implanted and nonimplanted regions of the IC. However, there is a large variation in intensity as a function of position. In addition, in this sample, degradation of material quality is seen 5 μm from the DGW edge.

The CL topographical maps and corresponding SEMs of the ERS and IC material are shown in Figures 5-7a and 5-7b and Figures 5-7c and 5-7d, respectively. Both CL maps show responses from threading dislocation clusters and misfit dislocations near the surface. The misfit bands are broader in the IC material. The SEMs show that both samples have the expected crosshatch, but the surface of the IC material reflects the broad misfit bands, and appears to have a more featured surface.

The difference in wavelengths of the CL spectra indicates a difference in the relaxation of

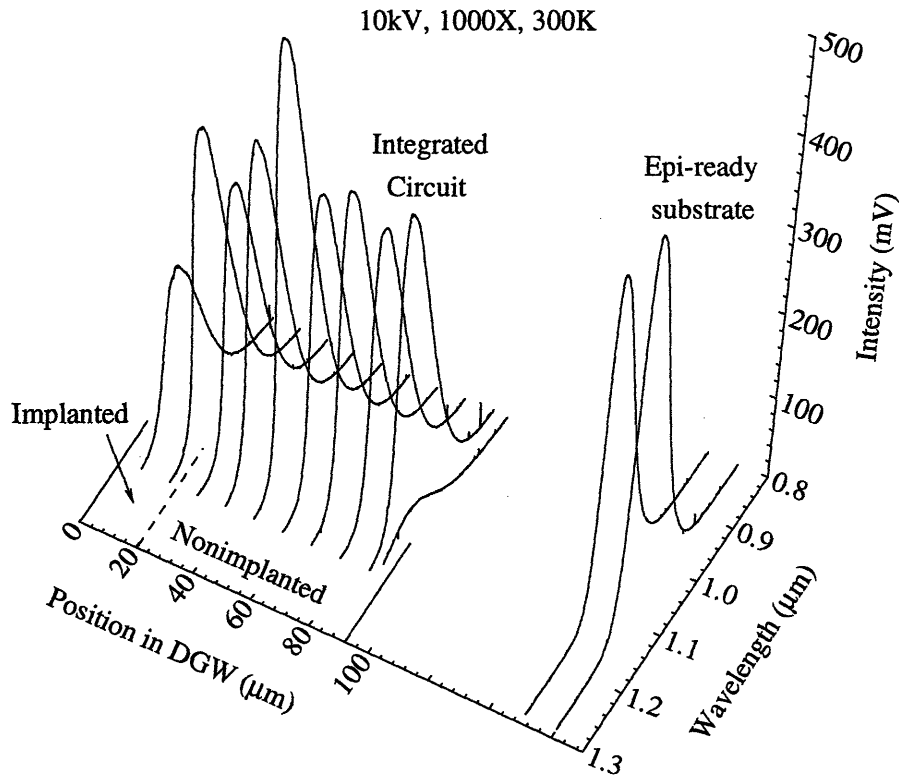


Figure 5-6: Comparison of the room-temperature CL spectra of a linearly graded RBRTD as a function of position and substrate.

the ERS and IC material, with the IC material being slightly more relaxed. A difference in substrate quality is the most plausible explanation for the difference in relaxation of the IC and ERS material. The IC has a higher number of heterogeneous nucleation sites than the ERS because of the high TDD of the IC substrate. In addition, the DGW sidewalls can serve as nucleation sites. A higher number of nucleation sites will translate into a larger threading and misfit dislocation density. The CL maps indicate that the IC material has a larger misfit dislocation density, which also corresponds to greater relaxation of the IC material.

Our results indicate that there is a difference between the epitaxial material grown on the ICs and that grown on a standard epi-ready substrate. The difference is in material quality, not composition. There is a variation in quality due to the variation in defect density in the epitaxial material as a function of position within the DGW. The variation is not correlated with the doping of the IC substrate. In relaxed-buffer structures, material grown on an IC has

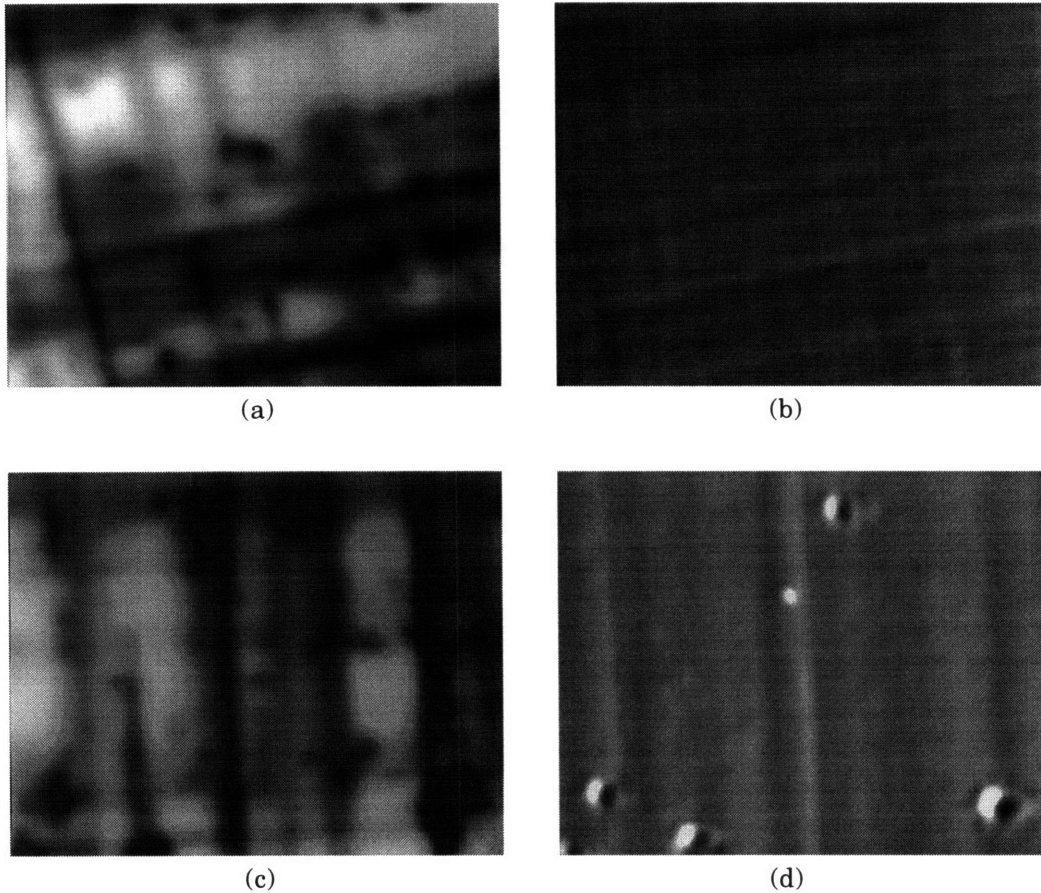


Figure 5-7: Surface maps of a linearly graded RBRTDs. (a) CL map of the ERS material taken at 10 kV and 2500× and (b) its corresponding SEM. (c) CL map of the IC material taken at 10 kV and 2500× and (d) its corresponding SEM. The area of the CL maps is $36 \times 46\ \mu m^2$.

shown a higher degree of relaxation than that on an ERS. This is attributable to the difference in defect density of the IC and ERS epitaxial material.

5.2 Degradation of IC Electronics

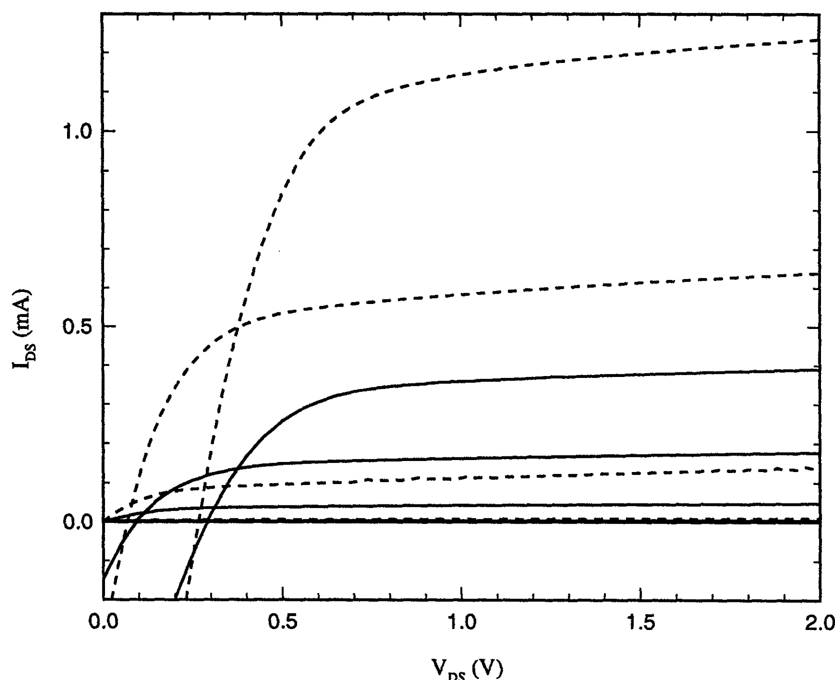


Figure 5-8: I–V of a 10×1.2 μm EFET before (dashed line) and after (solid line) a 6.5 hour RBRTD growth. V_{GS} = 0.0–1.0 V in steps of 0.25 V.

	Avg. V_T (V)	V_T σ (V)	Avg. R_E (kOhm)	R_E σ (kOhm)	Ave. g_m (μS)	g_m σ (μS)
Before	0.328	0.0140	20.9	1.48	942.8	84.14
6.5 hr. 470°C	0.360	0.0284	41.1	13.6	186.3	69.50

Table 5.1: Effects of temperature on 10×1.2 μm EFET performance. The 6.5 hour data includes the effect of thermal desorption of the native surface oxide. "Before" V_T and g_m data from [24].

As documented in Section 3.1.3, the total thermal cycle necessary to grow epitaxial material to completely fill the DGW will exceed the limits set to avoid degradation of the IC electronics. In particular, increases in the resistance of the MESFET S/D ohmic contacts and interconnect metals, increases in MESFET threshold voltage, and increases in the MESFET output resistance will have consequences on RTD circuit design. Figure 5-8 shows the I–V characteristics of a 10×1.2 μm EFET before and after a 6.5 hour RBRTD growth. The native oxide was desorbed at 580°C, and the substrate temperature during the 6.5 hour growth was 470°C.

Table 5.1 summarizes the performance of 13 EFETs across a MIT-OEIC-3 IC. The thermal exposure causes an increase in threshold voltage and a reduction in drain current. A higher V_T

Resistor	Before (Ohm)	6.5 hr. 470°C (Ohm)
Gate metal resistor snake	1.77×10^3	2.24×10^3
Metal 1 resistor snake	47.4	549
Metal 2 resistor snake	26.8	169
Metal 3 resistor snake	11.3	31.0
5×50 μm S/D resistor	2.41×10^3	3.19×10^3
20×5 μm S/D resistor	98.4	3.36×10^3

Table 5.2: Effects of temperature on IC resistor performance. "Before" data from [24].

and lower g_m reduce the amount of current that the EFET will provide for a given V_{RTD}, V_{HI}, and V_{LO}. Therefore, these changes will reduce the ability of the EFET to kick start a write to the SRAM. To accommodate the degradation of the EFETs, the SRAM cell must be designed with a larger EFET and a higher V_{RTD}. For V_{GS} = 1.0 V, V_{DS} = 0.7 V, the thermal exposure causes approximately a factor of three reduction in current: I_{before} = 1.064 mA and I_{after} = 0.3323 mA. Therefore, a corresponding EFET width increase of a factor of three will be required to account for the degradation. A higher V_{RTD} is required to maintain the V_{GS} and V_{DS} biases on the EFET. Table 5.2 shows the increase in MESFET and interconnect resistances with thermal exposure. These increases will reduce EFET performance and increase the parasitic resistances in the addressing circuitry of RTD SRAMs.

The degradation in the S/D ohmic contact is believed to be due to an interaction between the ohmic metal (70 nm Ni-Ge/100 nm WN_x) and metal 1 (150 nm WN_x/800 nm $AlCu_x$/ 100 nm WN_x) [24, 27]. Thermal exposure causes aluminum penetration through the WN_x barrier into the Ni-Ge, resulting in a new phase nucleation and the growth of a high-resistivity compound. The degradation in the interconnect metals is believed to be due to a solid-state reaction between $AlCu_x$ and WN_x [27]. The expected interconnect degradation can be simulated and must be incorporated in future SRAM circuit designs, particularly in the addressing circuitry. The degradation of the electronics caused by thermal desorption of the native oxide and the extended growth time are problems general to any EoE integration on the MIT-OEIC-3 ICs. A reduction in the degradation will be obtained with a low-temperature oxide removal process. Reductions in the degradation due to the length of the growth can possibly be obtained by further lowering the epitaxial growth temperature.

5.3 Electrical Characterization of Integrated RBRTDs

Both multiple-step and linearly graded RBRTDs were grown on ICs. For each sample, a corresponding piece of ERS was simultaneously processed for device comparison. Figure 5-9 shows a fully processed MIT-OEIC-3 IC with a linearly graded RBRTD heterostructure.

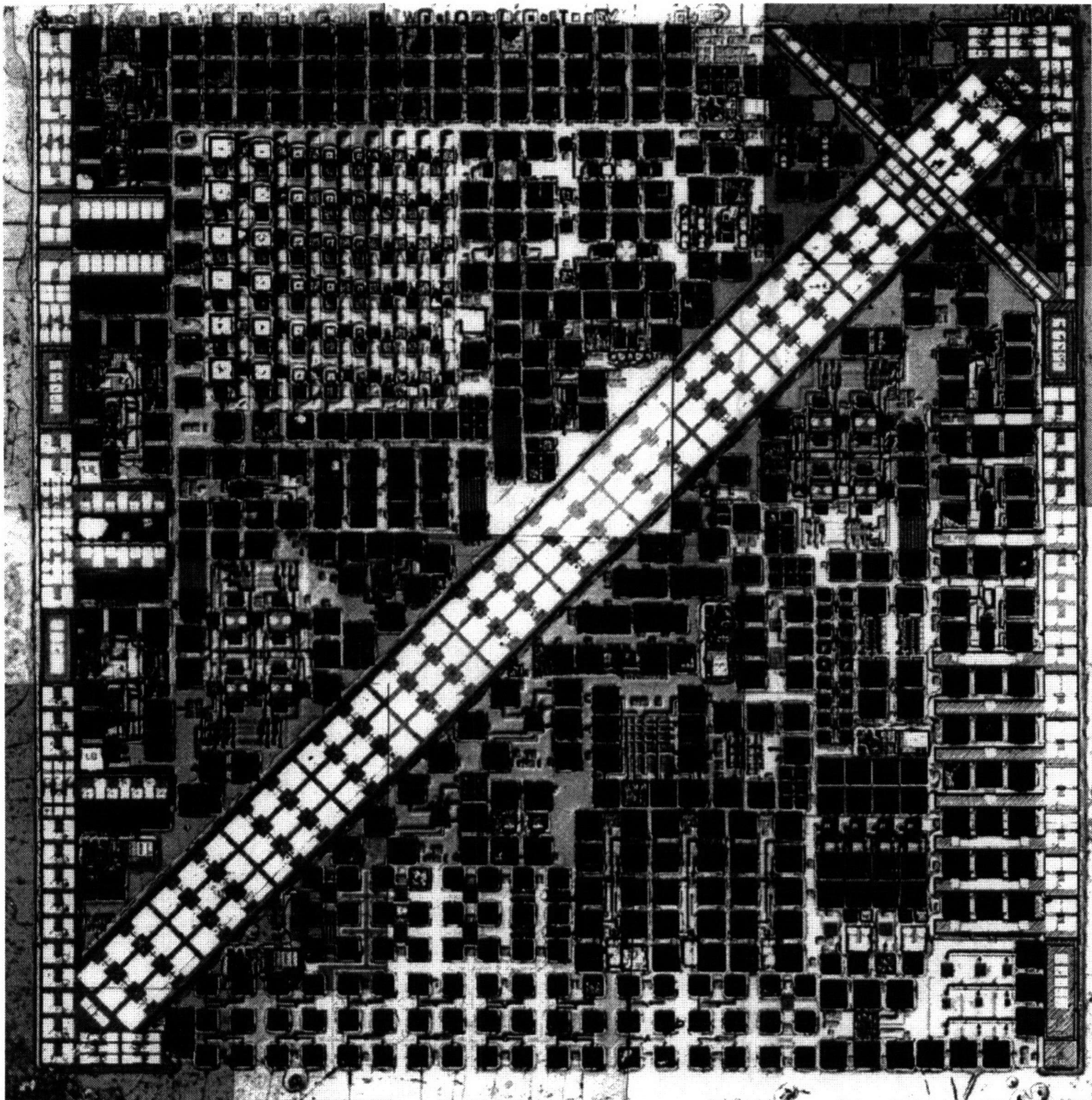


Figure 5-9: MIT-OEIC-3 IC with linearly graded RBRTDs processed using the RTD-OEIC-1 mask set.

5.3.1 Effect of Substrate on RBRTD Performance

To evaluate the uniformity of RTD performance across the integrated circuit, devices of different sizes were measured across the IC. To compare the IC device variation to that of RTDs grown on an epi-ready substrate, both types of samples were processed using the RTD-OEIC-1 mask set and identically positioned devices on each sample were measured. Figure 5-10 shows the RTD numbering scheme associated with the RTD-OEIC-1 mask set.

Figures 5-11 and 5-12, respectively, show the variation in the performance of two structures, a multiple-step and linearly graded RBRTD, across two different integrated ICs and their

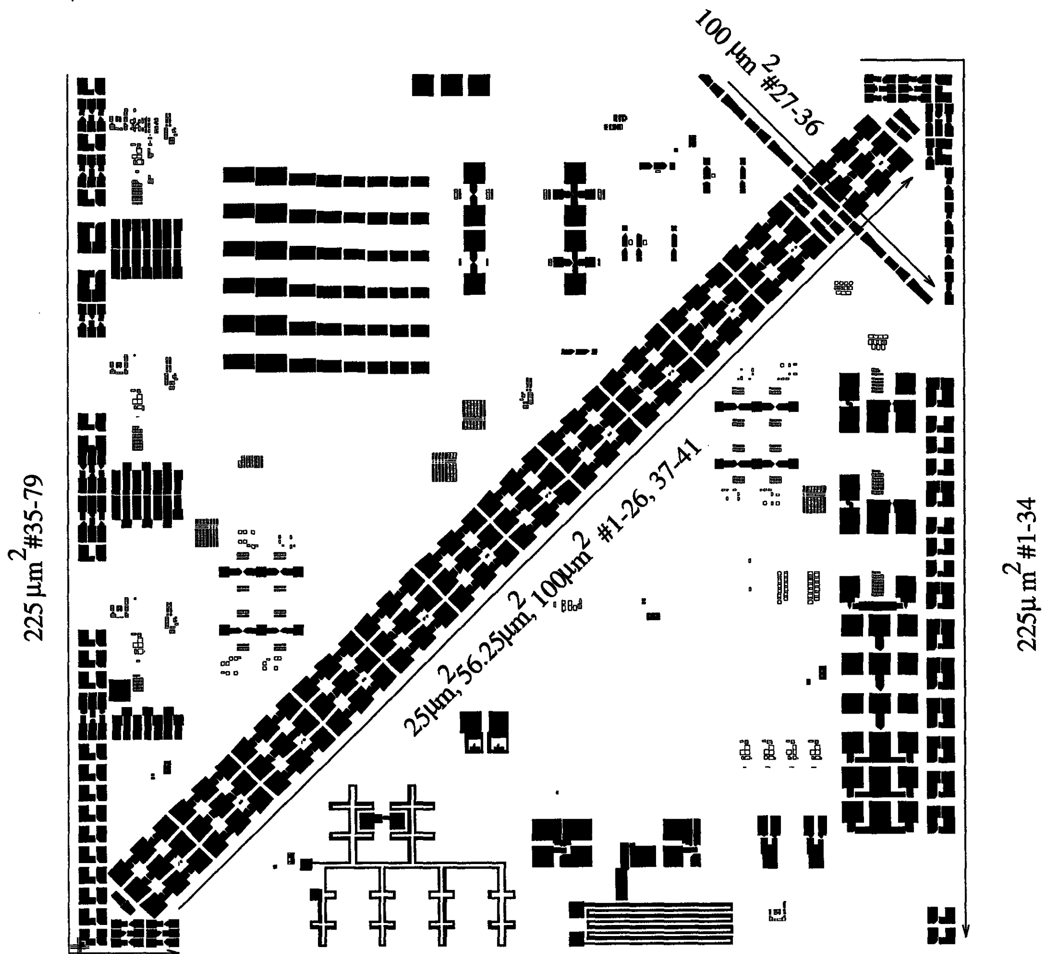


Figure 5-10: Numbering scheme associated with the RTD-OEIC-1 mask set.

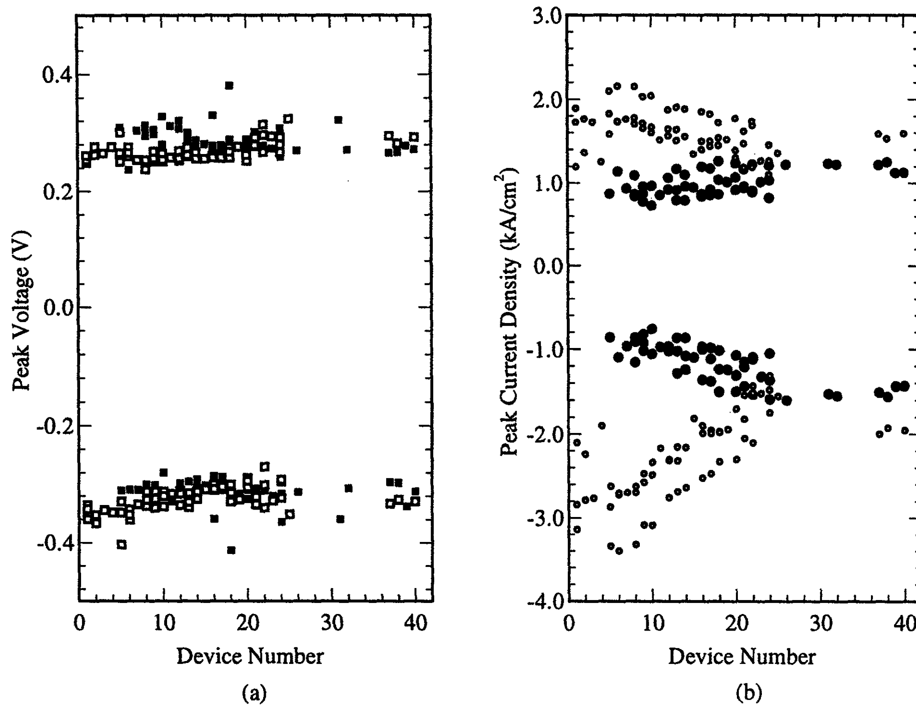


Figure 5-11: Uniformity of multiple-step RBRTD performance across a MIT-OEIC-3 IC (solid) and its associated ERS (open) for both polarities. (a) Variation in resonance voltage and (b) variation in peak current density. This IC had epitaxy grown only in the photonic IC DGW.

associated ERS samples. The multiple-step RBRTD in Figure 5-11 had epitaxy grown only in the photonic IC DGW (the large stripe across the chip). Both structures show variation as a function of position across the chip. For both, the variations were strongest in the peak current density, J_P, of the devices. In addition, for both structures, the material on the ERS showed a greater variation than that on the IC. The multiple-step ERS sample shows a gradual reduction in J_P moving from the lower-left to upper-right hand corner of the IC. The multiple-step IC sample showed a smaller magnitude increase in J_P for the same progression across the chip. For the linearly graded RBRTDs, neither sample showed much variance as a function of position for the $n = 1$ resonance. For the $n = 2$ resonance, the IC samples showed some scatter, but no consistent trend as a function of position. However, the $n = 2$ resonance of the linearly graded RBRTDs on the ERS showed substantial variance. Devices along the edges of the IC in general showed lower current densities than those in the middle of the IC (across the stripe). Tables 5.3, 5.4, 5.5, and 5.6 list the statistics of all the devices measured.

The variance in the performance of the integrated RBRTDs indicates the critical RTD parameters to be considered during design of a SRAM array. While all the parameters show variation, the peak and valley current densities consistently show greater percentage variation than the peak and valley voltages. The important current density to consider is the peak current density. The sizes of the RTDs and EFET should be chosen such that the EFET supplies more

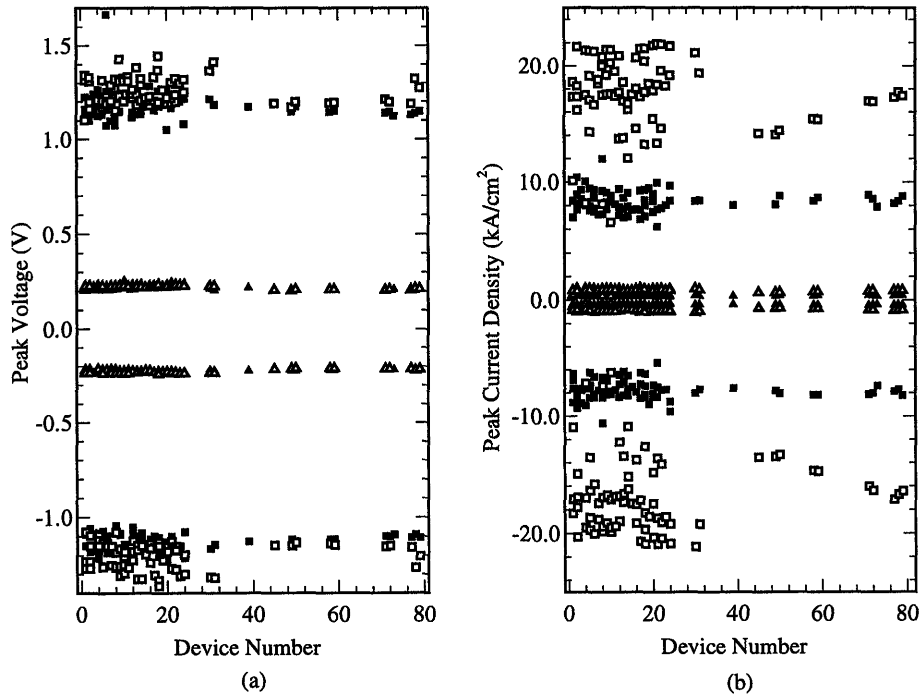


Figure 5-12: Uniformity of linearly graded RBRTD performance across an MIT-OEIC-3 IC (solid) and its associated ERS (open) for both polarities. (a) Variation in resonance voltage and (b) variation in peak current density. The triangles are the response for the $n = 1$ resonance, and the squares are for the $n = 2$ resonance. Not all of the devices on the samples were measured.

than the peak current of the RTDs. This will mitigate the effects of the variation in valley current, and most importantly, all cells of the SRAM will operate. For the linearly graded sample, RTD and EFET sizes must be chosen so that the EFET can handle a 11% variation in peak current (for the $n = 2$ resonance), and for the multiple-step sample, a 20% variation in peak current.

Parameter	Avg.	σ	max	Parameter	Avg.	σ	max
V_P (V)	-0.3122	0.02308		V_P (V)	0.2888	0.02288	
J_P (kA/cm^2)	-1.176	0.2350		J_P (kA/cm^2)	1.008	0.1511	
V_V (V)	-0.4250	0.01209		V_V (V)	0.4195	0.01380	
J_V (kA/cm^2)	-0.5712	0.1028		J_V (kA/cm^2)	0.4449	0.08119	
PVCR	2.062	0.1928	2.320	PVCR	2.303	0.3401	2.709

Table 5.3: Performance of multiple-step RBRTDs on an MIT-OEIC-3 IC. A total of 51 devices were measured.

Parameter	Avg.	σ	max	Parameter	Avg.	σ	max
V_P (V)	-0.3249	0.02188		V_P (V)	0.2681	0.01664	
J_P (kA/cm^2)	-2.279	0.5104		J_P (kA/cm^2)	1.614	0.2443	
V_V (V)	-0.4485	0.01931		V_V (V)	0.4134	0.009786	
J_V (kA/cm^2)	-0.9604	0.1907		J_V (kA/cm^2)	0.5832	0.07654	
PVCR	2.367	0.1387	2.849	PVCR	2.771	0.2346	3.272

Table 5.4: Performance of multiple-step RBRTDs on an ERS. A total of 60 devices were measured.

Parameter	Avg.	σ	max	Parameter	Avg.	σ	max
V_P (V)	-1.127	0.04590		V_P (V)	1.183	0.07968	
J_P (kA/cm^2)	-7.790	0.8416		J_P (kA/cm^2)	8.368	0.9283	
V_V (V)	-1.179	0.03230		V_V (V)	1.197	0.04382	
J_V (kA/cm^2)	-2.729	1.095		J_V (kA/cm^2)	2.634	0.9382	
PVCR	3.136	0.8260	5.050	PVCR	3.447	0.8844	5.140
V_P (V)	-0.2288	0.006501		V_P (V)	0.2220	0.007988	
J_P (kA/cm^2)	-0.3689	0.05847		J_P (kA/cm^2)	0.3572	0.05940	
V_V (V)	-0.3530	0.01237		V_V (V)	0.3436	0.01284	
J_V (kA/cm^2)	-0.1989	0.05904		J_V (kA/cm^2)	0.2063	0.05767	
PVCR	1.926	0.3067	2.332	PVCR	1.792	0.2826	2.264

Table 5.5: Performance of linearly graded RBRTDs integrated on a MIT-OEIC-3 IC. A total of 74 devices were measured.

Parameter	Avg.	σ	max	Parameter	Avg.	σ	max
V_P (V)	-1.201	0.07010		V_P (V)	1.251	0.07023	
J_P (kA/cm^2)	-16.84	3.189		J_P (kA/cm^2)	17.49	0.07023	
V_V (V)	-1.232	0.05182		V_V (V)	1.261	0.6402	
J_V (kA/cm^2)	-4.491	1.003		J_V (kA/cm^2)	4.724	1.075	
PVCR	3.821	0.6420	4.830	PVCR	3.791	0.7153	4.975
V_P (V)	-0.2280	0.007808		V_P (V)	0.2213	0.007884	
J_P (kA/cm^2)	-0.8219	0.1584		J_P (kA/cm^2)	0.7765	0.1457	
V_V (V)	-0.3602	0.01267		V_V (V)	0.3536	0.01261	
J_V (kA/cm^2)	-.3748	0.6548		J_V (kA/cm^2)	0.3843	0.06740	
PVCR	2.191	0.2145	2.598	PVCR	2.019	0.1729	2.325

Table 5.6: Performance of linearly graded RBRTDs on an ERS. A total of 75 devices were measured.

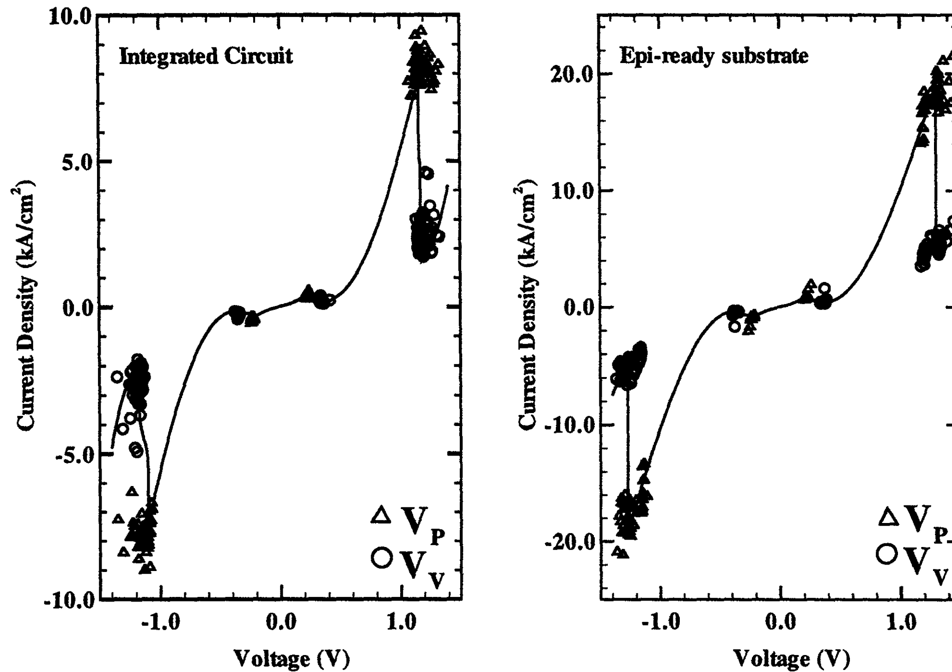


Figure 5-13: Comparison of the I–V characteristics of a linearly graded RBRTD on (a) an MIT-OEIC-3 IC and (b) an ERS. Fifty devices are plotted in each graph. An I–V curve is included to help guide the eye. The only difference in performance between the two substrates was lower peak and valley current densities for the RBRTDs on the IC.

Figure 5-13 is a scatter plot of the performance of the larger-sized linearly graded RBRTDs. An I–V is shown to help guide the eye. For the $n = 1$ and $n = 2$ resonance voltages, the differences between the two substrates are minimal. In addition, the PVCR for all the resonances are similar. What is substantially different is the current density. RBRTDs grown on the IC have almost a factor of two lower peak and valley current densities than those grown on the ERS. The peak (valley) current density of a device is the ratio of its peak (valley) current and its geometric area. The phenomenon seen is consistent with the IC devices having an electrically smaller area than their geometric area. For the $n = 2$ resonance, the data would then imply that the average reduction in area is 46.2% for the negative resonance and 47.8% for the positive resonance. For the $n = 1$ resonance, the reduction in area would have to be 44.9% for the negative resonance and 46.% for the positive resonance. The same area reduction phenomenon can be seen in the multiple-step RBRTD sample.

The presence of misfit dislocations in the active device layers might explain the reduction in active area of the EoE devices, as well as the variation in performance of the ERS and EoE devices as a function of position. Figure 5-14 schematically illustrates the location of the misfits in the two samples. The dark misfit bands in the CL maps of the ERS and IC linearly graded RBRTD samples, Figure 5-7, indicate that the misfits lie close to the sample

Figure 5-14: Schematic of difference in the misfit dislocation density of the EoE IC and ERS material.

surface. The junctions between the $In_xGa_{1-x}As$ and AlAs layers provide interfaces on which misfit dislocations can form and glide. PV–TEMs of the ERS linearly graded sample showed that misfit dislocations exist at the barrier/well interfaces of the RTD.

There are two types of misfit dislocations generated in relaxed $In_xGa_{1-x}As$. The first, called α dislocations, occur when the underbonded atoms along a dislocation are gallium atoms. They have a $[1\bar{1}0]$ direction. The second, called β dislocations, occur when the underbonded atoms along a dislocations are arsenic atoms. They have a [110] direction. Watson *et al.* have shown that α dislocations act as n-type majority carrier traps in relaxed $GaAs/In_{0.06}Ga_{0.94}As$ structures, 0.58 eV below the $In_{0.06}Ga_{0.94}As$ conduction band edge [55]. In addition, a number of studies have shown that a depletion region exists at the $GaAs/In_xGa_{1-x}As$ interface of n-type relaxed buffers [56, 57].

The majority of misfit dislocations in the IC material have a $[1\bar{1}0]$ direction, indicating the predominance of α dislocations. Based on the results presented in the literature, let us assume that misfit dislocations at the RTD active layers act like a majority carrier trap and deplete a region of semiconductor around them. For simplicity we also assume that the entire structure is heavily doped. We can estimate the width of the depletion layer using

$$W = \left[\frac{2\epsilon_s\phi}{qN_D}\right]^{\frac{1}{2}}. \quad (5.1)$$

If we assume ϕ = 0.58 eV, the depletion region for $N_D = 10^{18}$ cm^{-3} is 29.3 nm. In this situation, the depletion region around each dislocation will be a cylinder, as shown in Figure 5-15, with a radius of 29.3 nm. This radius is almost equal to the total width of the tunneling layers, 31.7 nm. Given that the RTD layers are unintentionally doped, the actual depletion region cross section will be elliptical with its major axis parallel the growth plane. The minor axis of the ellipse (the one parallel to the electron conduction path) will be substantially larger than 29.3 nm. Thus, a single dislocation can deplete the entire electron path through the RTD structure. If the unintentionally doped layers of the RTD are n-type 10^{15} cm^{-3}, the major axis of the ellipse will be 0.9260 μm.

The average area reduction experimentally observed in the linearly graded RBRTD on the

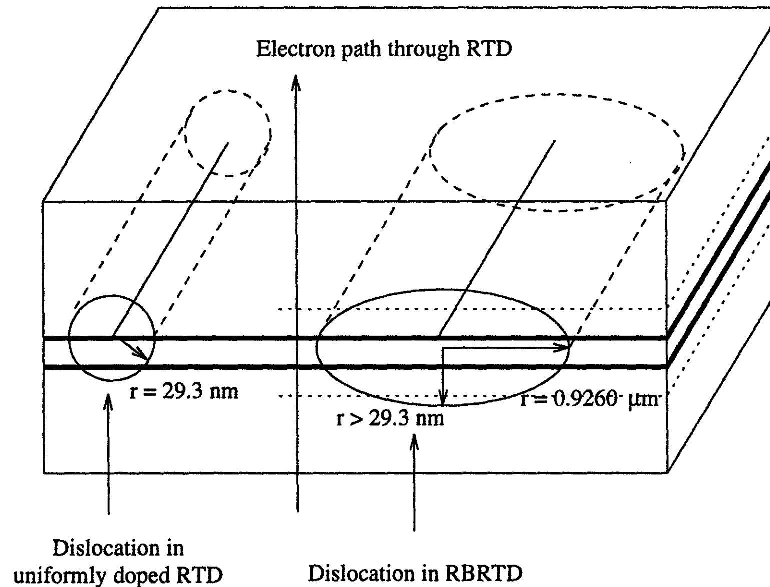


Figure 5-15: Schematic of the depletion region created by a misfit dislocation. On the left is the depletion region assuming uniform doping in the RTD layers. On the right is the depletion region for unintentionally doped RTD layers with doped contacts.

IC was 46.23%. If each dislocation laterally depletes the RTD 1.85 μm (twice the radius of the major axis of the dislocation ellipse) 1.25 misfit dislocations/5$\times$5 μm RTD are needed to account for the reduction in area.

From the PV-TEMs of the linearly graded RBRTD, we obtain a misfit dislocation density of 3.83×10^3 cm^{-1} for material on an ERS. This dislocation density corresponds to 1.92 misfits dislocations/5$\times$5 μm RTD. There are two corrections that need to be made to this number. Not all of the dislocations are α dislocations. And, in addition, an α misfit dislocation density is not available for the linearly graded RBRTD grown on the IC. Unfortunately, the information necessary to make these corrections cannot be obtained. We can expect the two corrections to offset each other. The reduction in dislocation number due to the elimination of the β dislocations will be compensated by the increase in α dislocations present in the IC material. Despite its limitations, the experimentally obtained misfit dislocation density corresponds reasonably well to that necessary to cause the reduction in active area seen in the linearly graded RBRTDs on the IC.

Further corroboration, albeit in a somewhat qualitative sense, can be obtained from the CL topographical maps of the linearly graded RBRTD. The dark regions on the CL map indicate regions of low minority carrier lifetime. If we assume that majority carriers are being eliminated at these regions, we can estimate the misfit dislocation depletion area from the CL maps. There are 7 α bands that occur in the map width of 46 μm and the average width of a misfit band is 2.9 μm. From this we can calculate a "depletion ratio" of 0.441 μm depleted material/μm of material. If we assume that electrons cannot tunnel through the RTD layers

anywhere there is a misfit dislocation at the RTD active layer interfaces, this ratio of depleted to undepleted material per unit length will correspond to a 44.1% reduction in active area for a specific device size. This number correlates well with those experimentally obtained.

These results help to explain the variation of the devices as a function of position. The performance of a device will be dependent on whether or not it contains a misfit dislocation. For both RBRTD structures grown on the ICs, the variation in the devices on the IC was less than that of devices grown on the ERS. If the IC has a greater density of misfit dislocations, there will be a more uniform distribution of misfit dislocations among devices. The variance of the ERS devices reflects the nonuniformity in misfit dislocation distribution among devices.

The reduced current densities of the integrated RBRTDs was a benefit in this thesis. Given the limited size and number of EFETs available for integration, the reduced current density ensured that at least the smaller RBRTDs would be compatible with the available EFETs. However, under normal circumstances, the reduction in current density is a detriment. If the reduction is not accounted for, the EFET will be oversized. An oversized EFET wastes area and adds capacitance to the circuit. Presently, only rough estimates of the area reduction are known. A systematic study of the electrical activity of misfit dislocations in the active layers of RTDs must be performed to accurately predict the reduction in current, and thus properly size the SRAM EFET.

5.3.2 Performance of Well Array RBRTDs

The problems encountered in cleaning the DGWs limited the use of the well array. Many times, the smaller wells were not successfully cleaned. The procedure that was used to successfully clean some of the well array DGWs did not reproduce the angled DGW sidewalls originally incorporated in the well array design. These difficulties negated the experiments designed to assess the effect of DGW edge profile on material quality and device performance. The smallest DGWs that RTDs were successfully fabricated in were 30×30 μm.

RBRTD performance was severely limited by series resistance. Transmission line measurements structures were used to obtain a contact resistivity of $\rho_c = 1.6 \times 10^{-6}$ ohm/cm^2 for the top contact (alloyed AuGe/Ni/Au) of the RTD, indicating that this contact should not be adding series resistance to the devices. The RBRTDs were electrically characterized by probing at the well array bond pads as well as at the well array probe pads. Comparison of these I–Vs revealed little difference, indicating that the connection from the epitaxial material through the DGW S/D implant and ohmic contact was adding the resistance. Comparison of fully and partially implanted DGW devices did not show any trends. Both these results are consistent with previous studies of the thermal degradation of the S/D ohmic contacts which concluded that the S/D ohmic contact resistance increase could be as large as several orders of magnitude and was highly unpredictable [27].

Figure 5-16 shows the I–V characteristics of 7.5×7.5 μm linearly graded RBRTDs grown in fully and partially implanted DGWs. Because of the erratic behavior of the ohmic contacts,

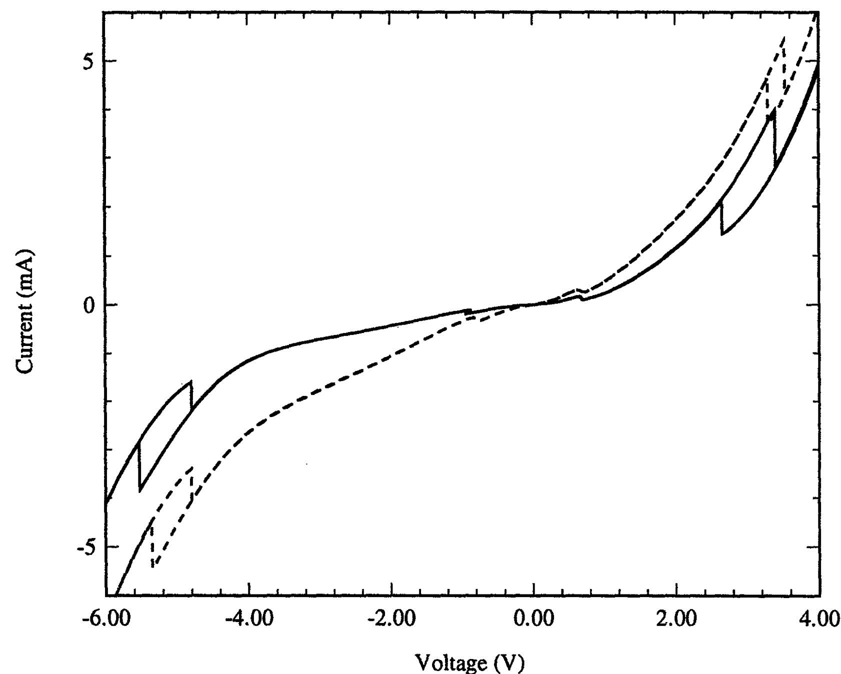


Figure 5-16: I–V characteristics of 7.5×7.5 μm RBRTDs grown in fully implanted (solid, well 6E) and partially implanted (dashed, well 5E) DGWs.

these I–Vs cannot be considered typical. However, they do demonstrate the character of the degradation in RTD performance. The hysteresis present indicates that there is a series resistance component to the devices. This component is more prominent in the $n = 2$ resonance. These devices have the same epitaxial structure as those shown in Figure 5-13a. Table 5.7 compares the performance of the devices shown in Figure 5-16 with the average values for discrete devices with the same epitaxial structure. The well array devices show substantial increases in peak voltage for all resonances. The $n = 2$ peak voltages of the well array devices are not compatible with those necessary for proper SRAM operation. Current densities are comparable for all three samples. However, the reduction in PVCR will change the switching current requirements as well as reduce the noise margins of an SRAM cell made with the well array devices. Furthermore, the erratic nature of the ohmic contact degradation will reduce the uniformity in cell performance across a SRAM array.

In the previous chapter, studies of the series resistance of RBRTDs was determined to be small enough to enable the use of an implanted DGW contact scheme. This contact topology simplifies both the layout and fabrication of RTD circuits. However, the degradation in the performance of the well array devices indicates that a contact topology that utilizes the S/D ohmic contact is not feasible. The thermal exposure experienced during the MBE growth substantially increases the ohmic contact resistance, and thus increases the resonance voltage

RTD description	resonance	V_P (V)	J_P (kA/cm^2)	PCVR	V_P (V)	J_P (kA/cm^2)	PVCR
fully implanted	$n = 2$	-5.348	-9.689	1.600	3.525	9.431	1.444
partially implanted	$n = 2$	-5.523	-6.825	2.395	3.390	7.116	2.776
discrete	$n = 2$	-1.127	-7.790	3.316	1.183	8.368	3.447
fully implanted	$n = 1$	-0.7700	-0.6014	1.238	0.6300	0.5609	1.154
partially implanted	$n = 1$	-0.9420	-0.3390	1.715	0.6600	0.3120	1.653
discrete	$n = 1$	-0.2288	-0.3689	1.926	0.2220	0.3572	1.792

Table 5.7: Comparison of the performance of fully and partially implanted well array 7.5×7.5 μm linearly graded RBRTDs (wells 6E and 5E, respectively) with the average performance of discrete integrated devices.

of the RBRTDs. The majority of the contact degradation can be attributed to the thermal oxide desorption procedure [27]. These results further emphasize the need for a low-temperature oxide removal procedure. Otherwise, the ohmic contact degradation will limit all circuits utilizing implanted growth wells to connect heterostructure devices with the IC electronics.

6

Characterization of RTD-EFET SRAM Circuits

Because of the conversion error during the circuit layout, both four-bit memory arrays and three of the one-bit memory cells have nonfunctional EFETs. The largest discrete EFET available, at a quantity of 1/chip, was a 20×1.2 μm EFET. A larger supply, 17/chip, of 10×1.2 μm EFETs were available. Therefore, the RBRTDs grown on the integrated circuits had lower resonance voltages and current densities than those used in the circuit designs of Chapter 3. This enabled hybrid implementations of the memory cells using discrete RBRTDs and 10×1.2 μm EFETs for dc evaluation of the circuit.

The monolithic SRAM circuits were fabricated as part of the standard RTD process flow. Though none of these circuits functioned as planned, they provided valuable information regarding the heterostructure fabrication part of the EoE process flow. Section 6.1 describes the fully fabricated circuits. The demonstration of the RTD-EFET SRAM was made using a hybrid implementation of the circuit. Section 6.2 describes the circuits and their performance.

6.1 Monolithic RTD-EFET SRAM Circuits

Figure 6-1 shows a fully processed one-bit memory cell at a magnification of $200\times$. The DGW measures 100×100 μm. The two RTDs, measuring 5×5 μm, are the two round dots in the DGW. Two vertical fingers connect the RTDs to power, V_{RTD}, and ground. The horizontal contact in the DGW connects the storage node to the EFET source nodes via 50×50 μm bond pads. This cell, RJA2B, has 84×1.2 μm EFETs.

Figure 6-2 shows a fully processed memory array at a magnification of $50\times$. There are four 100×100 μm DGWs, each with two 10×10 μm RTDs. The connections between the RTDs and their respective power and ground bond pads appear as short, vertical lines. These DGWs are implanted, and therefore explicit connection between the RTDs and the EFETs is not necessary. The EFETs in this circuit are 240×1.2 μm. Crossing the upper right-hand corner of the photograph is the photonic integrated circuit DGW, which is filled with RTD storage

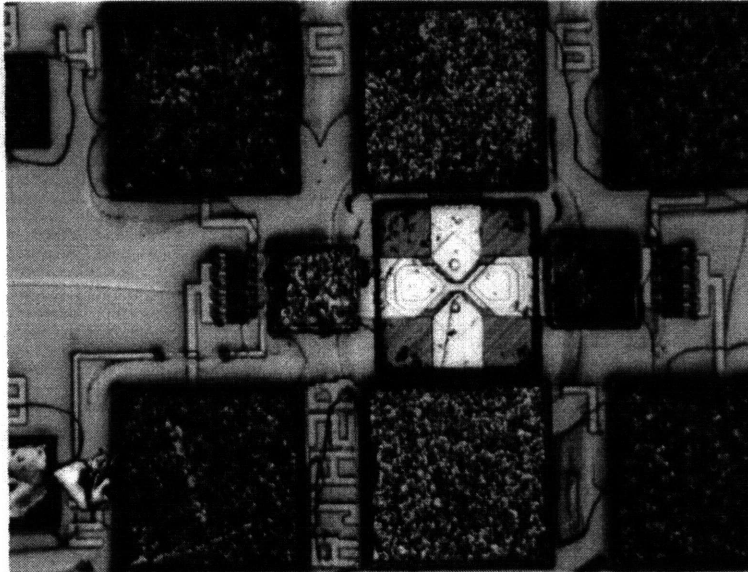


Figure 6-1: Photograph of a 1-bit RTD-EFET SRAM cell at 200×.

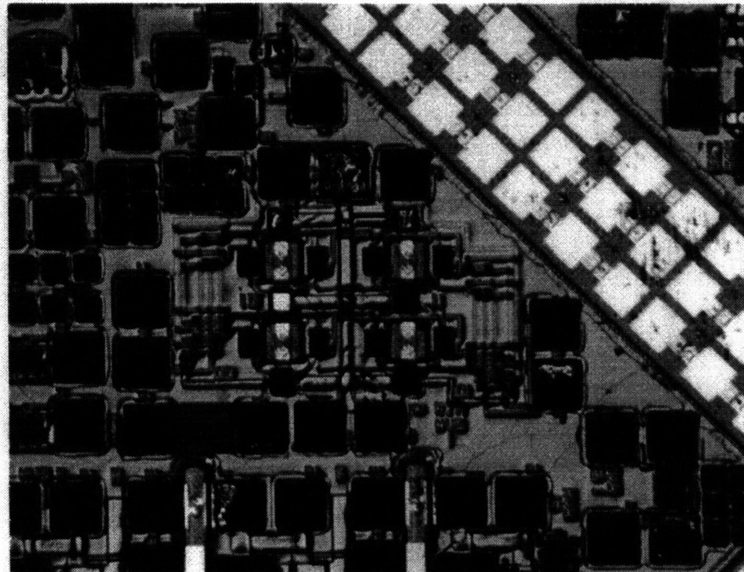


Figure 6-2: Photograph of a 4-bit RTD-EFET SRAM array at 50×. The array is in the middle of the photograph. The photonic IC and its associated RTDs can be seen crossing the upper-right hand corner of the photograph.

elements.

Though not functional, these circuits were extremely useful in evaluating the present DGW and overall chip design, and the heterostructure process flow. The border around the chip proved valuable in providing area to handle the inevitable edge-buildup of photoresist during the lithography process. The combination of a 0.5 mm border and a simple edge-bead removal process improved contact during lithography without the loss of devices in DGWs at the edges of the chip. The accuracy of the alignment steps was, as expected, dependent on the height differentials present across the chip. To accommodate the large lips at the edges of the electronics bond pads, two different resists were used. A thin resist, which provided better feature definition, was used in all etching steps, where a lack of resist coverage over the lip would not affect the circuit. A thick resist process was successful for metallizations within the DGWs. The thick resist provided the lip with enough protection that extraneous metal did not adhere to the edges of the circuit bond pads. The issue of metal step coverage from the DGW and over the bond pad lip remained a problem. A lack of bond metal coverage over the lip prevented successful connection between the RTDs in the DGWs and the IC bond pads. This problem was not solved in this thesis. However, the new bond pad design utilized in MIT-OEIC-4 addresses, and hopefully solves, the problem.

There is one memory cell/chip that is properly connected on each MIT-OEIC-3 IC. Unfortunately, in all of the integrations, the RBRTDs in this cell failed before the memory action of the cell was successfully demonstrated.

6.2 Hybrid RTD-EFET SRAM Circuits

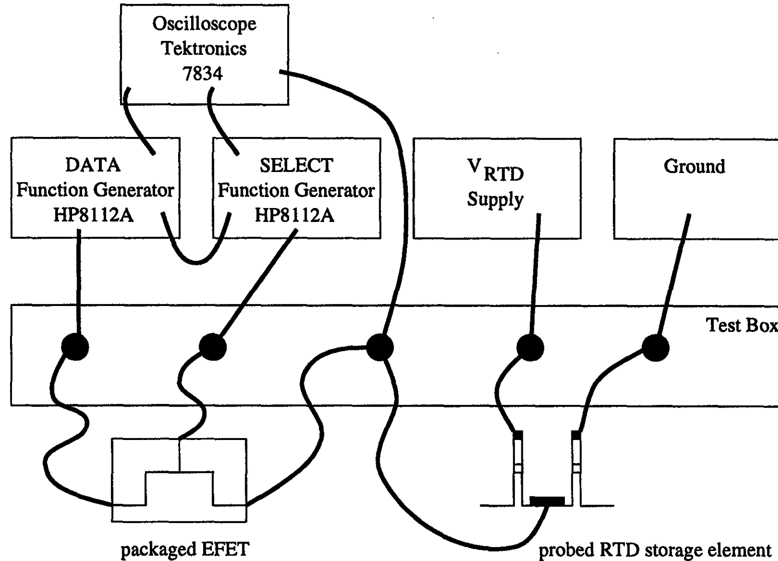


Figure 6-3: Schematic of the hybrid memory cell measurement configuration. The EFET was contacted via a standard dual-in-line package and the RTDs were probed.

Figure 6-3 shows the experimental configuration for the hybrid memory cell measurements. The EFET is packaged and the RTDs are probed. The EFET used in the demonstrations was from an IC that had not been thermal cycled. (None of the thermally cycled EFETs could provide enough current to write to the SRAM.) The two devices are connected via a test box. The SELECT function generator is triggered off of the DATA signal. The connection between the EFET and the RTDs (package to coaxial cable to dc needle probes) and to the oscilloscope (probes to coaxial cable, through the test box to more coaxial cable) adds a large capacitance to the storage node. This measurement configuration eliminates the possibility of useful switching time measurements of the cell. The DATA line has 100 nsec rise and fall times to help reduce oscillations in the circuit. Wherever possible, i.e., at the nonstorage node coaxial connections, 50 ohm terminations were used. However, impedance mismatches still exist within the circuit and are visible in the oscilloscope traces. The RTDs used in the following demonstrations are linearly graded RBRTDs with an average V_P of 0.23 V, V_V of 0.36 V, and J_P of 290 A/cm^2. The EFET is 10×1.2 μm.

Figure 6-4 shows the performance of a hybrid RTD-EFET SRAM cell that uses 5×5 μm RTDs and a V_{RTD} of 0.56 V. The top trace is the SELECT line operating at 1 MHz. The select voltage ranges from 0–1 V with a 350 nsec pulse width. The second trace is the DATA line and ranges from -0.25–0.75 V. The circuit demonstrates the basic functionality of an SRAM. When the SELECT and DATA lines are high, the state of the DATA line is "written" to the storage node. When the SELECT line goes LO, i.e., the EFET turns off, the storage node holds the voltage most recently written to it. For this RTD bias, V_{HI} = 0.46 V and V_{LO} = 0.16 V. The

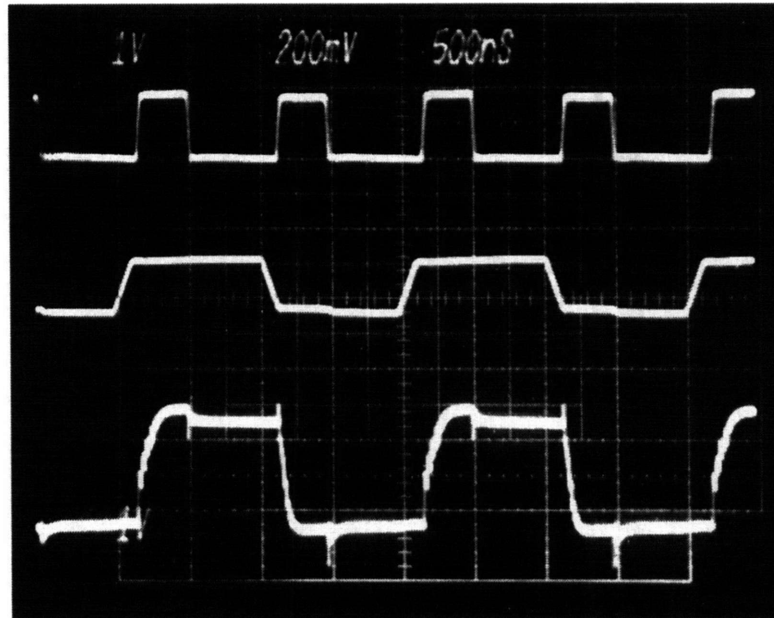


Figure 6-4: Write operation of a hybrid RTD-EFET SRAM cell using 5×5 μm RTDs and a 10×1.2 μm EFET. The top, middle, and bottom traces are the SELECT, DATA, and storage node, respectively. The SELECT pulse width is 350 nsec.

static powers for the LO and HI states are 0.032 and 0.0.34 mW, respectively. The minimum switching current requirements for V_{RTD} = 0.56 V are approximately 0.033 mA to write a HI and 0.035 mA to write a LO.

During the WRITE HI operation, the EFET V_{GS} = 0.84–0.54 V and V_{DS} = 0.59–0.29 V. In this demonstration the SELECT pulse is long enough for the storage node to charge to the WRITE HI level, $V_{\mathrm{WRITE,\,HI}}$ = 0.5 V. Once the EFET is turned off, the storage node relaxes to V_{HI} = 0.46 V. Comparison of these values with the I–V characteristics of the EFET, Figure 5-8, shows that in this implementation the EFET sources much more than the minimum required switching current.

During the WRITE LO operation, the EFET V_{GS} = 1.25 V and V_{DS} = 0.75–0.41 V. The V_{GS} of the WRITE LO operation exceeds the Schottky barrier height of 0.7 V for the gate-source diode of the EFET. When the gate-source diode is on, the gate is drawing current. This causes the voltage at the DATA node to rise $\approx$ 10 mV during the write operation, and pins the voltage at the storage node. As the SELECT line drops in voltage and the EFET stops pulling gate current, there is a momentary drop in the storage node voltage. This occurs when the EFET is still on and the low value of the DATA line draws additional current from the storage node. When the EFET is fully off, the node voltage charges to a stable V_{LO} = 0.16 V.

Figure 6-5 shows the performance of the same hybrid circuit with a reduced SELECT pulse width. In this situation, the EFET is not on long enough to charge the storage node to $V_{\mathrm{WRITE,\,HI}}$. However, the EFET is on long enough to raise the storage node past $V_{\mathrm{RTD}}/2$, at

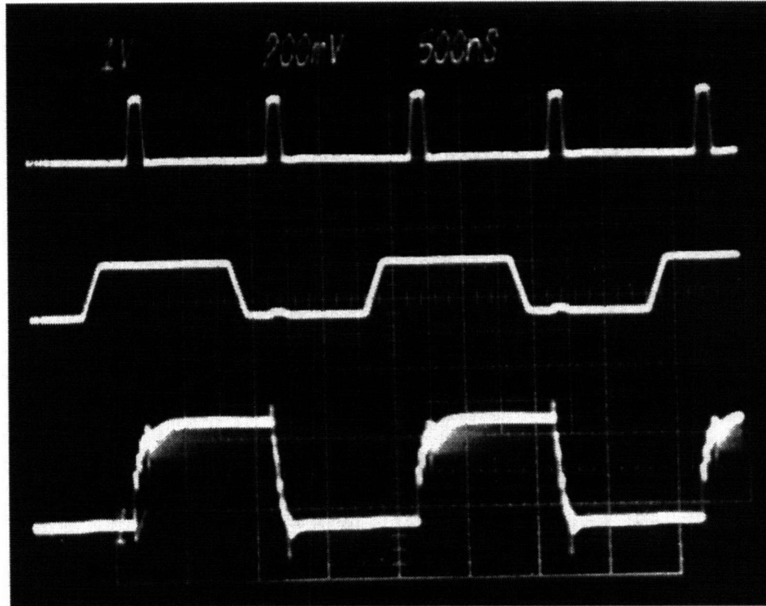


Figure 6-5: Write operation of a hybrid RTD-EFET SRAM cell using 5×5 μm RTDs and a 10×1.2 μm EFET. The top, middle, and bottom traces are the SELECT, DATA, and storage node, respectively. The SELECT pulse width is 100 nsec.

which point the RTDs take over the switch. (This is the situation simulated in the analytic cell performance curves of Chapter 2.) This demonstration foreshadows one design trade-off in a RTD-EFET SRAM memory array: access line charging vs. cell switching speed. A higher voltage SELECT pulse will translate into a larger delay time for a write or read propagation through the addressing circuitry. If the EFET is turned off sooner, i.e., before the EFET establishes $V_{\mathrm{WRITE,HI}}$, the delay is incurred because the RTDs must charge the storage node without additional charge supplied by the EFET.

The performance of the circuit was monitored as increasing capacitance was added to the storage node. The RTD storage element was able to establish V_{LO} and V_{HI} despite the addition of 2.5 nF to the storage node. When the DATA function generator was disconnected, the storage node retained its value, either a V_{HI} of 0.46 V or a V_{LO} of 0.16 V depending on the last value written to the node. This voltage was maintained indefinitely. The memory failed when 10 nF were added to the storage node.

Our results indicates that the RTD storage element is capable of charging a substantial capacitance. As mentioned previously, this capacitance was a result of the hybrid implementation of the memory cell. During a read operation of a single cell, the capacitance of the READ EFET, the READ DATA bond pad, and a high impedance probe, (under 300 fF) will be added to the storage node. For a memory array, the added capacitance will be larger. Our simulations indicated that the memory cell read operation will work under worst-case scenarios, Sections 3.3 and 3.4. Though this demonstration does not explicitly show the read functionality

Figure 6-6: Write operation of hybrid RTD-EFET SRAM cell with 10×10 μm RTDs and a 10×1.2μm EFET. The top, middle, and bottom traces are the SELECT, DATA, and storage node, respectively. The SELECT pulse width is 100 nsec.

of the cell, it indicates that the storage element will be capable of charging the access lines of a memory.

In the previous demonstrations, the EFET was substantially oversized in relation to the RTDs, and thus supplied much more than the minimum required switching current. Figure 6-6 shows the performance of a hybrid cell using a 10×10 μm RTD and V_{RTD} = 0.55 V. The SELECT and DATA lines once again range from 0–1 V and -0.25–0.75 V, respectively. For this RTD bias, V_{HI} = 0.44 V and V_{LO} = 0.16 V. The static powers for the LO and HI states are 0.1436 and 0.1209 mW, respectively. The minimum switching current requirements for V_{RTD} = 0.55 V are approximately 0.05 mA to write a HI and 0.025 mA to write a LO.

During the WRITE HI operation, the EFET V_{GS} = 0.84–0.56 V and V_{DS} = 0.59–0.31 V. The DATA line voltage can be reduced to -0.25–0.55 V (V_{DS} = 0.39–0.11 V) and maintain proper operation of the cell. The reduction in drain voltage reduces the EFET's ability to charge the storage node. Comparison of the initial V_{DS} and V_{GS} values with the EFET characteristics of Figure 5-8 shows that initially the EFET must source more than the minimum required switching current. This is because the EFET is not a constant current source. As the storage node rises, the EFET current will decrease. In this circuit, the EFET must initially provide over ten times the minimum switching current to kick start the write operation. Then, as the storage node drops in voltage, the EFET will still source the required current to charge the storage node. The short pulse width turns the EFET off before the storage node has charged to the WRITE HI level. When the HI DATA voltage is reduced below 0.55 V, the EFET can no longer supply the current necessary to charge the storage node.

RTD	RTD Area (μm^2)	V_{SELECT} (V)	V_{DATA} (V)	V_{RTD} (V)	V_{HI} (V)	P_{HI} (mW)	V_{LO} (V)	P_{LO} (mW)
RJA–9080 (LG)	100	0.0–1.0	-0.25–0.75	0.550	0.42	0.121	0.16	0.144
RJA–9080 (LG)	56.25	0.0–1.0	-0.25–0.75	0.573	0.48	0.103	0.18	0.074
RJA–9080 (LG)	25	0.0–1.0	-0.25–0.75	0.560	0.46	0.034	0.16	0.032
RJA–9037 (MS)	56.25	0.0–1.2	0.0–1.0	0.676	0.50	0.172	0.20	0.213
RJA–9037 (MS)	56.25	0.0–1.0	-0.5–1.0	1.119	0.58	0.448	0.24	0.468
RJA–9037 (MS)	25	0.0–1.2	-0.25–0.55	0.700	0.52	0.085	0.20	0.103

Table 6.1: Partial summary of hybrid integrated RBRTD SRAM cell performance. All use a 10×1.2 μm EFET. LG – linearly graded RBRTD, MS – multiple-step RBRTD.

During the WRITE LO operation, the EFET V_{GS} = 1.25 V and V_{DS} = 0.69–0.41 V. Again, the EFET must initially supply substantially more than the minimum required switching current for the switch to occur. The proper WRITE LO operation will not occur for DATA LO voltages higher that -0.25 V, because the V_{DS} of the EFET is not large enough to provide the necessary kick start for the switch.

For this implementation, the cell will not operate if V_{SELECT} < 0–1 V. For V_{SELECT} = 0–1 V, the smallest V_{DATA} range is -0.25–0.55 V. For these SELECT and DATA voltages, V_{RTD} can range from 0.5 V to 0.835 V, and the SRAM cell will operate using the n = 1 resonance.

Table 6.1 shows a partial summary of the performance of hybrid integrated RTD-EFET SRAM cells using both linearly graded and multiple-step RBRTDs. The multiple-step RBRTDs have an average V_P = 0.2888 V, V_V = 0.4195 V, and J_P = 1.01 kA/cm^2. Cells using the multiple-step RBRTD show the possible trade-off between SELECT, DATA, and RTD supply voltages. The same cell will work for V_{SELECT} = 0.0–1.2 V, V_{DATA} = 0.0–1.0 V, and V_{RTD} = 0.676 V as well as V_{SELECT} = 0.0–1.0, V_{DATA} = -0.5–1.0 V, and V_{RTD} = 1.119 V. In the second case, the increase in V_{RTD} raises the V_{HI} and V_{LO} values and is coupled with an increase in the V_{DATA} range. These changes increase V_{DS} to compensate the reduction in V_{GS}, maintaining the necessary EFET current to complete the write operations.

Table 6.2 compares the predicted and experimentally measured performance of RTD-EFET SRAM cells. Because of a lack of experimental data, we cannot evaluate the predictions of SRAM speed. In addition, by design, the model does not accurately predict the switching current ranges necessary for proper cell operation. However, for dc performance parameters, the simulated and experimental results are in good agreement. This indicates that a simple, piecewise-linear model is a good tool for the basic design of the memory. It accurately predicts the dc voltage levels of the storage element. Knowledge of V_{LO} and V_{HI} in turn gives accurate predictions of the input voltage ranges of the EFET. With this knowledge, the EFET can be appropriately sized such that it will supply enough current to switch the cell. For example, the EFET should be sized such that when the storage node is half-way through its transition, the resulting V_{GS} and V_{DS} will force the EFET to supply the necessary switching current. The

RTD	V_{SELECT} (V)	V_{DATA} (V)	I_{EFET} (mA)	V_{RTD} (V)	V_{HI} (V)	P_{HI} (mW)	V_{LO} (V)	P_{LO} (mW)
RJA–9080 (LG)	0.0–1.0	-0.25–0.75		0.560	0.46	0.034	0.16	0.032
RJA–9080 (LG)			0.05	0.56	0.410	0.026	0.150	0.026
RJA–9037 (MS)	0.0–1.2	-0.25–0.55		0.7	0.52	0.085	0.20	0.103
RJA–9037 (MS)			0.4	0.7	0.495	0.124	0.205	0.124

Table 6.2: Comparison of simulated and experimental SRAM performance. The results are for 5×5 μm RTDs and a 10×1.2 μm EFET. For the experimental results, the input voltage ranges of the EFET are listed. For the simulated results, the EFET was assumed to be a constant current source and the node capacitance is 40 fF. LG – linearly graded RBRTD. MS – multiple-step RBRTD.

overall design will be iterative in nature, with repeated adjustments to the storage element and EFET parameters to assure self-consistency.

These are first-generation demonstrations verifying the concept of a RTD-EFET SRAM. They exposed flaws in the manufacturing process. The value of these circuits as learning tools for EoE-based OEIC fabrication cannot be underestimated. The lessons learned from these circuits will be incorporated both in future RTD circuits as well as any circuit utilizing the EoE integration technique. The information gained led to the redesign of the DGWs and bond pads, and confirmed the edge-bead border layout concept.

Experimentally, we have demonstrated the write functionality of the RTD-EFET memory circuit. Our measurements indicate that the cell will be capable of a non-destructive read operation. The circuits are robust; they operate despite substantial parasitic capacitance and impedance mismatches. The dc operation of the memory is close to that analytically simulated. Cells with and without oversized EFETs were measured. Both types operate under a variety of bias conditions. The wide operating range is a function of the six-parameter design space alloted the RTD-EFET SRAM designer. By showing the operation of the cells under various bias conditions, we demonstrate both design trade-offs mentioned earlier in this thesis and the memory's ability to handle RTD variations.

7

Conclusions

7.1 Accomplishments

The Epitaxy-on-Electronics (EoE) integration technique has been used to successfully demonstrate an integrated RTD-EFET SRAM cell. This thesis covers all phases of the development of the memory technology: design, device demonstration, and circuit demonstration.

The cell design phase of the work, Chapter 2, focused on identifying the optimum RTD parameters for a RTD-EFET SRAM. A set of four guidelines for RTD design were presented. A high current density and moderate peak and valley voltages will contribute to the cell write speed. A broad, low current valley and high peak-to-valley current ratio RTD will reduce cell power dissipation and increase cell speed and power uniformity across an array. Limits on the RTD parameters are ultimately established by the EFET's current sourcing capabilities. In Chapter 3, designs for SRAM cells and a four-bit SRAM array were presented. The circuit designs were fully simulated, including the effects of layout generated parasitics, in HSPICE. These circuits were fabricated as part of the optoelectronic integrated circuit MIT-OEIC-3.

The first experimental phase of the thesis, Chapter 4, concentrated on developing the MBE growth techniques for relaxed-buffer RTDs (RBRTDs) and evaluating their epitaxial quality. The growth techniques were developed within the constraints of the EoE integration process. X-ray diffraction, cathodoluminescence, and transmission electron microscopy were used to characterize the relaxed-buffer material. We demonstrated that the constraints of the EoE integration technology limit the effectiveness of relaxed-buffer grading techniques. Electrical characterization was performed on a variety of RBRTDs. We demonstrated high-PVCR RBRTDs and RBRTDs that were suitable for use in circuits.

The last experimental phase of the thesis, presented in Chapters 5 and 6, evaluated the performance of integrated RBRTDs and RTD-EFET SRAM cells. We have shown that there is a difference in the material quality of RBRTDs grown on an epi-ready substrate (ERS) and on an integrated circuit (IC). RBRTDs on the IC show a higher misfit dislocation density and corresponding greater relaxation. The higher dislocation density is not surprising given the high IC substrate threading dislocation density (TDD) as well as the additional heterogeneous

nucleation sites provided by the DGW walls. Comparison of RBRTDs with different misfit dislocation densities indicates that the misfit dislocations are reducing the electrical area of the RBRTDs. The variation in RTD performance both across a sample and between samples can be related to the dislocation density of the sample.

The expected degradation of the integrated circuits was monitored. The degradation was severe and consistent with previous studies. Evaluation of RTDs utilizing the S/D ohmic contact indicate that the degradation will preclude the use of this contact scheme unless a low-temperature native oxide desorption procedure is adopted.

Monolithic integrated RTD-EFET SRAM cells and four-bit SRAM arrays were fabricated using the MIT-OEIC-3 ICs. The circuits were not functional due to circuit design conversion problems. However, they provided information on the manufacturability of the MIT-OEIC-3 design. A cleaning procedure was developed to enable utilization of the MIT-OEIC-3 circuits. New DGW and bond pad designs were developed based on these results. The fabrication validated the edge-bead border concept first implemented on MIT-OEIC-3.

The culmination of the thesis was a demonstration of a first-generation, functional RTD-EFET SRAM cell. Hybrid SRAM cells were made using integrated RTDs and EFETs. Because of the hybrid nature of the circuit, experimental evaluation of SRAM switching speed was not possible. The hybrid circuits demonstrate the expected memory action for the write operation. Our results indicate that the cell will be capable of a non-destructive read operation. The wide operating range that results from a six-parameter design space was experimentally mapped. The circuit dc parameters show good correspondence with earlier analytic models.

Technology	Cell Size (μm)	Cell τ_{rise} (psec)	Cell P_{diss} (mW)	Ref.
GaAs MESFET DCFL	42.0×28.5	200	0.036	[58]
RTD-EFET (MS)	10×9.8	44.8	0.124	thesis
RTD-EFET (LG)	10×9.8	273.0	0.026	thesis

Table 7.1: Comparison of GaAs and RTD-EFET SRAM cell performance. The RTD-EFET cell assume 5×5 μm RTDs stacked on a 10×1.2 μm EFET according to the Vitesse HGaAs3 design rules. MS – mulitple-step RBRTD, LG – linearly graded RBRTD.

This study began by citing the potential of the RTD-EFET memory. The RTD-EFET SRAM has a very simple cell architecture and the potential to be a very high speed, high density, and low power memory. Table 7.1 compares two simulated RTD-EFET SRAM cell performances to that of a GaAs SRAM cell [58]. The RTD-EFET cells assume 5×5 μm RTDs stacked on a 10×1.2 μm EFET according to the Vitesse HGaAs3 design rules. The performance of the linearly graded RTD-EFET SRAM cell has speed and power performance specifications that are very close to those of the GaAs DCFL SRAM. The RTD-EFET SRAM achieves this performance with a much smaller cell area. Because of this reduction in cell area, the same size memory implemented in the RTD-EFET technology will have smaller bit and word line lengths than

if the memory was implemented in the GaAs DCFL technology. For the same addresssing circuit design, the reduction in bit and word line lengths should correspond to a reduction in access time. Or, the reduced cell area of the RTD-EFET SRAM could be utilized to increase the density of the memory for a given total memory IC area. For either of these cases, the RTD-EFET SRAM technology should exhibit advantages over the GaAs SRAM.

Technology	Memory Size	Cell Area (μm^2)	Supply Voltage (V)	Access Time (nsec)	Memory P_{diss} (mW)	Ref.
CGaAs	4K	278	0.9	15.0	0.36	[59]
CGaAs	4K	278	1.5	5.3	16.2	[59]
Current Mirror	1K	350	2.0	1.4	800	[60]

Table 7.2: Comparison of recent GaAs SRAMs. CGaAs is a complementary heterostructure GaAs technology.

The GaAs DCFL memory cell cited in Table 7.1 was demonstrated in 1987. Since that time, considerable work has gone into increasing the overall speed and reducing the total power dissipation of GaAs SRAMs. Table 7.2 reviews two recently published GaAs SRAMs. One approach, geared towards very low voltage applications, uses a complementary heterostructure GaAs logic family [59]. The other approach uses a novel current mirror memory cell to increase the speed of the memory [60]. An RTD-EFET memory must successfully compete against these types of technologies to be a viable commercial memory.

The RTD-EFET technology presented in this thesis uses the EoE integration technology, and therefore is not optimized for speed or power performance. Any commercial implementation of the memory will see substantial reductions in RTD area as well as reductions in EFET sizes. Given production fabrication facilities, RTD areas of 1 μm^2 are achievable. Vitesse presently has available a 0.6 μm gate length GaAs technology. Two 1$\times$1 μm RTDs fit with a 3.0$\times$0.6 μm EFET, giving a cell area of approximately 11.4 μm^2. This cell area is substantially smaller than those listed in Table 7.2. The reduction in the RTD and EFET areas will contribute to a reduction in the storage node capacitance, which in turn will help to reduce the RTD-EFET cell rise time. For given RTD and EFET areas, increases in RTD current density can further reduce the cell rise time at the expense of increased cell power dissipation.

A factor of twenty-five reduction in the linearly graded RBRTD area will reduce the static power of its SRAM cell to approximately 1 μW. The memory cells of a 1K SRAM will then have a power dissipation of 1 mW, less than the simulated 288 mW total cell power dissipation for the current mirror SRAM technology [60]. However, the RTD-EFET SRAM will not have a lower power than the lower supply voltage CGaAs SRAM. The total power dissipated in the RTD memory will be dependent on the addressing circuitry used. The access time of the RTD-EFET memory will also be dependent on the addressing circuitry of the memory. An added complication to the RTD-EFET technology is the necessity of an additional voltage supply

for the addressing circuitry. The storage element supply bias, 0.56 V for the linearly graded RBRTD-EFET SRAM cell, is not suitable to drive DCFL GaAs addressing circuits.

A true comparison of the performance of GaAs and RTD-EFET SRAMs will require that an optimized RTD-EFET SRAM be built. The RTD-EFET technology is best positioned to compete as a high speed memory. An aggressive addressing circuit is necessary to utilize the speed of the RTD-EFET SRAM cell. Reductions in RTD and EFET areas as well as increases in RTD current density will increase the speed of the memory. However, if the access time delay incurred in the addressing circuitry is much larger than the cell rise time, improvements in the cell rise time will have little consequence on the overall performance of the memory. An RTD-EFET SRAM must handle variations in RTD I–V characteristics across a memory. A limited memory size will reduce access time as well as RTD parameter variations across an array. An RTD-EFET memory will be useful in applications where speed is the ultimate goal, and the power dissipation requirements of the memory are sacrificed for that speed.

7.2 Future Work

The first, and most obvious next step in the development of the RTD-EFET SRAM is a monolithic demonstration of the cell. Corrected SRAM designs were submitted to MOSIS in July of 1995 as part of MIT-OEIC-4, the next generation optoelectronic integrated circuit. Given that submission, future work can be divided into three categories: integration studies, materials studies, and circuit studies.

7.2.1 Integration Studies

This thesis emphatically reinforces the necessity of a low-temperature thermal oxide desorption procedure. The present method degrades the S/D ohmic contacts to unacceptable levels. Without such a procedure, the simplified contact topology of the implanted dielectric growth windows is nullified.

A related problem is the length of the epitaxial growth. Presently, 6.5 μm of epitaxy are required to completely fill the DGW. The resulting MBE growth time also degrades the circuits. There are two possible MBE growth solutions: development of a high growth rate relaxed buffer technique or the development of a low-temperature relaxed buffer technique similar to present low-temperature GaAs buffers. Both of these however, threaten to reduce the relaxation and increase the TDD of the relaxed buffers. Another solution is to forgo planarity, and only fill a small portion of the DGW. The step coverage requirements created by an incompletely filled DGW can be addressed with sputtered metal interconnects. The problems associated with contact lithography will be minimal for large devices. However, for smaller devices such as a typical 5×5 μm RTD, projection lithography will be necessary for accurate device definition.

7.2.2 Materials Studies

This thesis demonstrated the difference in epitaxial material quality grown on an ERS and an IC. The presence of misfit and threading dislocations prevented accurate counts/comparisons of the threading dislocation density for the different substrates. Minimization of TDD is desirable for all heterostructures grown on the ICs, whether they are lattice matched or not. Cathodoluminescence studies of lattice-matched structures on an ERS and an IC will yield information on the epitaxial TDD of the two samples. This information is especially critical for minority-carrier devices, where the TDD is expected to have a greater effect on device performance.

This thesis demonstrated that misfit dislocations along the tunneling layers of an RTD can reduce the electrical area of an RTD. These studies were qualitative in nature. A systematic study of the electrical activity of misfit dislocations in RTDs will be necessary to accurately model the reduction in RTD current for future RBRTD applications.

7.2.3 Electrical studies

This thesis demonstrated the basic memory action of the RTD-EFET SRAM. The second generation of cell circuits should experimentally evaluate the effects of RTD, interconnect, and parasitic capacitances on the cell speed. The RTD capacitance is varied by adjusting the contact doping of the RTDs. The interconnect capacitance is varied by changing the contact topology of the SRAM. Parasitic effects can be measured by externally loading the monolithic circuit. Given a monolithic circuit, a more representative demonstration of the read and write operations of the memory can be made. The second generation of full memory circuits must also begin to incorporate realistic addressing schemes for the memory. The combination of speed and full circuit measurements are necessary to properly evaluate the commercial position/potential of RTD-EFET memories.

A

RTD-EFET SRAM Analytic Model

The analytic model solves for the voltage at the storage node as a function of time. The starting point of the model is Equation A.1

$$I_{RTD1} + C_{RTD1}\frac{dV_{RTD1}}{dt} + I_{EFET}(V_{GS}, V_{GD}) = I_{RTD2} + C_{RTD2}\frac{dV_{RTD2}}{dt} + C_S\frac{dV_{RTD2}}{dt}, \quad \text{(A.1)}$$

which is derived using Kirchoff's Current Law at the storage node. I_{RTD} is the current in an RTD and C_{RTD} is the RTD capacitance. The capacitance of the EFET source contact is C_S. Writing V_{RTD1} in terms of V_{RTD2} and combining terms gives

$$\frac{dV_{RTD1}}{dt} = \frac{dV_{RTD}}{dt} - \frac{dV_{RTD2}}{dt} = -\frac{dV_{RTD2}}{dt} \quad \text{(A.2)}$$

$$I_{RTD1} - I_{RTD2} + I_{EFET}(V_{GS}, V_{GD}) = [C_{RTD1} + C_{RTD2} + C_S]\frac{dV_{RTD2}}{dt}. \quad \text{(A.3)}$$

The EFET source node capacitance can be combined with the capacitances of the two RTDs to form the storage node capacitance, C_{node}. Recognizing that V_{RTD2} is the storage node voltage yields

$$I_{RTD1} - I_{RTD2} + I_{EFET}(V_{GS}, V_{GD}) = C_{node}\frac{dV_{node}}{dt}. \quad \text{(A.4)}$$

To analytically solve for the storage node voltage as a function of time, Equation A.5 is solved for the piecewise-linear regions of the switch and the switching times for each region are then summed to calculate the total switching time.

$$t = \int dt = \int \frac{C_{node}\, dV_{node}}{I_{RTD1} - I_{RTD2} + I_{EFET}} \quad \text{(A.5)}$$

Because the intent of this model is to focus on the role of the RTD, further assumptions are made:

- The RTDs used are symmetric with respect to voltage.
- Load and driver RTDs are identical. The pre-resonance conductance of the RTDs is G_1 and the post-resonance conductance of the RTDs is G_2.
- The RTD negative differential resistance (NDR) region is modeled as a finite, linear resistor with conductance G_{N}.
- All capacitances are constant as a function of bias.

- To simulate the EFET turning off during the switch, the EFET current is modeled as constant for $V_{\text{node}} < V_{\text{RTD}} - V_{\text{P}}$. This will only simulate the slowest of the write actions: WRITE HI when the EFET cuts off. The current is actually on longer than the minimum time (t_{min} occurs when $V_{\text{node}} = V_{\text{RTD}}/2$), but is assumed to be zero for $t > t_{\text{min}}$ for simplicity and to account for noise margins for the switch.
- $V_{\text{RTD}} \geq 2V_{\text{P}}$ to insure that there is no stable middle voltage node.

There are four possible bias cases. The solutions for each case will be presented region by region.

Case 1: $\mathbf{V_{RTD} = 2V_P}$

Region 1

$$\tau_1 = \frac{C_{node}}{G_1 + G_2} \tag{A.6}$$

$$K_1 = -(G_1 + G_2)V_{LO} + G_2(V_{RTD} - V_V) + I_V + I_o \tag{A.7}$$

$$t_1 = -\tau_1 \, ln \left[\frac{-G_1(V_{RTD} - V_V) + I_V + I_o}{K_1} \right] \tag{A.8}$$

$$V_1(t) = \frac{G_2(V_{RTD} - V_V) + I_V + I_o - K_1 exp\left(\frac{-t}{\tau_1}\right)}{G_1 + G_2} \tag{A.9}$$

Region 2

$$\tau_2 = \frac{C_{node}}{G_1 + G_N} \tag{A.10}$$

$$K_2 = exp\left(\frac{t_1}{\tau_2}\right) \left[-G_1(V_{RTD} - V_V) + G_N(V_V - V_P) + I_P + I_o\right] \tag{A.11}$$

$$t_2 = -\tau_2 \, ln \left[\frac{-G_1 V_P + G_N(V_{RTD} - 2V_P) + I_P + I_o}{K_2} \right] \tag{A.12}$$

$$V_2(t) = \frac{G_N(V_{RTD} - V_P) + I_P + I_o - K_2 exp\left(\frac{-t}{\tau_2}\right)}{G_1 + G_N} \tag{A.13}$$

Region 3

$$\tau_3 = \frac{C_{node}}{G_1 + G_N} \tag{A.14}$$

$$K_3 = exp\left(\frac{t_2}{\tau_3}\right) \left[G_1(V_{RTD} - V_P) - I_P + I_o\right] \tag{A.15}$$

$$t_3 = -\tau_3 \, ln \left[\frac{G_1(V_{RTD} - V_V) + G_N(V_P - V_V) - I_P + I_o}{K_3} \right] \tag{A.16}$$

$$V_3(t) = \frac{G_1 V_{RTD} + G_N V_P - I_P + I_o - K_3 exp\left(\frac{-t}{\tau_3}\right)}{G_1 + G_N} \tag{A.17}$$

Region 4

$$\tau_4 = \frac{C_{node}}{G_1 + G_2} \tag{A.18}$$

$$K_4 = exp\left(\frac{t_3}{\tau_4}\right)\left[G_1(V_{RTD} - V_V) - I_V + I_o\right] \tag{A.19}$$

$$V_4(t) = \frac{G_1 V_{RTD} + G_2 V_V - I_V + I_o - K_4 exp\left(\frac{-t}{\tau_4}\right)}{G_1 + G_2} \tag{A.20}$$

Case 2: $\mathbf{V_{RTD} > 2V_P, V_{RTD} < V_P + V_V}$

Region 1

$$\tau_1 = \frac{C_{node}}{G_1 + G_2} \tag{A.21}$$

$$K_1 = -(G_1 + G_2)V_{LO} + G_2(V_{RTD} - V_V) + I_V + I_o \tag{A.22}$$

$$t_1 = -\tau_1 \, ln\left[\frac{-G_1(V_{RTD} - V_V) + I_V + I_o}{K_1}\right] \tag{A.23}$$

$$V_1(t) = \frac{G_2(V_{RTD} - V_V) + I_V + I_o - K_1 exp\left(\frac{-t}{\tau_1}\right)}{G_1 + G_2} \tag{A.24}$$

Region 2

$$\tau_2 = \frac{C_{node}}{G_1 + G_N} \tag{A.25}$$

$$K_2 = exp\left(\frac{t_1}{\tau_2}\right)\left[-G_1(V_{RTD} - V_V) + G_N(V_V - V_P) + I_P + I_o\right] \tag{A.26}$$

$$t_2 = -\tau_2 \, ln\left[\frac{-G_1 V_P + G_N(V_{RTD} - 2V_P) + I_P + I_o}{K_2}\right] \tag{A.27}$$

$$V_2(t) = \frac{G_N(V_{RTD} - V_P) + I_P + I_o - K_2 exp\left(\frac{-t}{\tau_2}\right)}{G_1 + G_N} \tag{A.28}$$

Region 3

$$\tau_3 = \frac{C_{node}}{2G_N} \tag{A.29}$$

$$K_3 = exp\left(\frac{t_2}{\tau_3}\right)\left[-2G_N V_P + G_N V_{RTD} + I_o\right] \tag{A.30}$$

$$t_3 = -\tau_3 \, ln\left[\frac{-G_N(V_{RTD} - 2V_P) + I_o}{K_3}\right] \tag{A.31}$$

$$V_3(t) = \frac{G_N V_{RTD} + I_o - K_3 exp\left(\frac{-t}{\tau_3}\right)}{2G_n} \tag{A.32}$$

Region 4

$$\tau_4 = \frac{C_{node}}{G_1 + G_N} \tag{A.33}$$

$$K_4 = exp\left(\frac{t_3}{\tau_4}\right)[G_1V_P - G_N(V_{RTD} - 2V_P) - I_P + I_o] \tag{A.34}$$

$$t_4 = -\tau_4\, ln\left[\frac{G_1(V_{RTD} - V_V) + G_N(V_P - V_V) - I_P + I_o}{K_4}\right] \tag{A.35}$$

$$V_4(t) = \frac{G_1V_{RTD} + G_NV_P - I_P + I_o - K_4exp\left(\frac{-t}{\tau_4}\right)}{G_1 + G_N} \tag{A.36}$$

Region 5

$$\tau_5 = \frac{C_{node}}{G_1 + G_2} \tag{A.37}$$

$$K_5 = exp\left(\frac{t_4}{\tau_5}\right)[G_1(V_{RTD} - V_V) - I_V + I_o] \tag{A.38}$$

$$V_5(t) = \frac{G_1V_{RTD} + G_2V_V - I_V + I_o - K_5exp\left(\frac{-t}{\tau_5}\right)}{G_1 + G_2} \tag{A.39}$$

Case 3: $V_{RTD} > 2V_P$, $V_{RTD} > V_P + V_V$, $V_{RTD} < 2V_V$

Region 1

$$\tau_1 = \frac{C_{node}}{G_1 + G_2} \tag{A.40}$$

$$K_1 = -(G_1 + G_2)V_{LO} + G_2(V_{RTD} - V_V) + I_V + I_o \tag{A.41}$$

$$t_1 = -\tau_1\, ln\left[\frac{-V_P(G_1 + G_2) + G_2(V_{RTD} - V_V) + I_V + I_o}{K_1}\right] \tag{A.42}$$

$$V_1(t) = \frac{G_2(V_{RTD} - V_V) + I_V + I_o - K_1exp\left(\frac{-t}{\tau_1}\right)}{G_1 + G_2} \tag{A.43}$$

Region 2

$$\tau_2 = \frac{C_{node}}{G_2 + G_N} \tag{A.44}$$

$$K_2 = exp\left(\frac{t_1}{\tau_2}\right)[G_2(V_{RTD} - V_P - V_V) + I_V - I_P + I_o] \tag{A.45}$$

$$t_2 = -\tau_2\, ln\left[\frac{-G_N(V_{RTD} - V_V - V_P) + I_V - I_P + I_o}{K_2}\right] \tag{A.46}$$

$$V_2(t) = \frac{G_2(V_{RTD} - V_V) + G_NV_P + I_V - I_P + I_o - K_2exp\left(\frac{-t}{\tau_2}\right)}{G_2 + G_N} \tag{A.47}$$

Region 3

$$\tau_3 = \frac{C_{node}}{2G_N} \tag{A.48}$$

$$K_3 = exp\left(\frac{t_2}{\tau_3}\right)\left[G_N(2V_V - V_{RTD}) + I_o\right] \tag{A.49}$$

$$t_3 = -\tau_3\, ln\left[\frac{G_N(V_{RTD} - 2V_V) + I_o}{K_3}\right] \tag{A.50}$$

$$V_3(t) = \frac{G_N V_{RTD} + I_o - K_3 exp\left(\frac{-t}{\tau_3}\right)}{2G_N} \tag{A.51}$$

Region 4

$$\tau_4 = \frac{C_{node}}{G_2 + G_N} \tag{A.52}$$

$$K_4 = exp\left(\frac{t_3}{\tau_4}\right)\left[G_N(V_{RTD} - V_P - V_V) + I_P + I_o\right] \tag{A.53}$$

$$t_4 = -\tau_4\, ln\left[\frac{G_2(V_V + V_P - V_{RTD}) + I_P + I_o}{K_4}\right] \tag{A.54}$$

$$V_4(t) = \frac{G_N(V_{RTD} - V_P) + G_2 V_V + I_P + I_o - K_4 exp\left(\frac{-t}{\tau_4}\right)}{G_N + G_2} \tag{A.55}$$

Region 5

$$\tau_5 = \frac{C_{node}}{G_1 + G_2} \tag{A.56}$$

$$K_5 = exp\left(\frac{t_4}{\tau_5}\right)\left[G_1 V_P + G_2(V_V + V_P - V_{RTD}) - I_V + I_o\right] \tag{A.57}$$

$$V_5(t) = \frac{G_1 V_{RTD} + G_2 V_V - I_V + I_o - K_5 exp\left(\frac{-t}{\tau_5}\right)}{G_1 + G_2} \tag{A.58}$$

Case 4: $\mathbf{V_{RTD} > 2V_P, V_{RTD} > 2V_V}$

Region 1

$$\tau_1 = \frac{C_{node}}{G_1 + G_2} \tag{A.59}$$

$$K_1 = -(G_1 + G_2)V_{LO} + G_2(V_{RTD} - V_V) + I_V + I_o \tag{A.60}$$

$$t_1 = -\tau_1\, ln\left[\frac{-V_P(G_1 + G_2) + G_2(V_{RTD} - V_V) + I_V + I_o}{K_1}\right] \tag{A.61}$$

$$V_1(t) = \frac{G_2(V_{RTD} - V_V) + I_V + I_o - K_1 exp\left(\frac{-t}{\tau_1}\right)}{G_1 + G_2} \tag{A.62}$$

Region 2

$$\tau_2 = \frac{C_{node}}{G_2 + G_N} \tag{A.63}$$

$$K_2 = exp\left(\frac{t_1}{\tau_2}\right)\left[G_2(V_{RTD} - V_P - V_V) + I_V - I_P + I_o\right] \tag{A.64}$$

$$t_2 = -\tau_2\, ln\left[\frac{-G_N(V_V - V_P) - G_2(2V_V - V_{RTD}) + I_V - I_P + I_o}{K_2}\right] \tag{A.65}$$

$$V_2(t) = \frac{G_2(V_{RTD} - V_V) + G_N V_P + I_V - I_P + I_o - K_2 exp\left(\frac{-t}{\tau_2}\right)}{G_2 + G_N} \tag{A.66}$$

Region 3

$$\tau_2 = \frac{C_{node}}{2G_2} \tag{A.67}$$

$$K_3 = exp\left(\frac{t_2}{\tau_3}\right)\left[G_2(V_{RTD} - 2V_V) + I_o\right] \tag{A.68}$$

$$t_3 = -\tau_3\, ln\left[\frac{G_2(2V_V - V_{RTD}) + I_o}{K_3}\right] \tag{A.69}$$

$$V_3(t) = \frac{G_2 V_{RTD} + I_o - K_3 exp\left(\frac{-t}{\tau_3}\right)}{2G_2} \tag{A.70}$$

Region 4

$$\tau_4 = \frac{C_{node}}{G_2 + G_N} \tag{A.71}$$

$$K_4 = exp\left(\frac{t_3}{\tau_4}\right)\left[G_N(V_V - V_P) + G_2(2V_V - V_{RTD}) + I_P + I_o\right] \tag{A.72}$$

$$t_4 = -\tau_4\, ln\left[\frac{G_2(V_V + V_P - V_{RTD}) + I_P + I_o}{K_4}\right] \tag{A.73}$$

$$V_4(t) = \frac{G_N(V_{RTD} - V_P) + G_2 V_V + I_P + I_o - K_4 exp\left(\frac{-t}{\tau_4}\right)}{G_N + G_2} \tag{A.74}$$

Region 5

$$\tau_5 = \frac{C_{node}}{G_1 + G_2} \tag{A.75}$$

$$K_5 = exp\left(\frac{t_4}{\tau_5}\right)\left[G_1 V_P + G_2(V_V + V_P - V_{RTD}) - I_V + I_o\right] \tag{A.76}$$

$$V_5(t) = \frac{G_1 V_{RTD} + G_2 V_V - I_V + I_o - K_5 exp\left(\frac{-t}{\tau_5}\right)}{G_1 + G_2} \tag{A.77}$$

B

Documentation for RTD-OEIC-1

This document is a guide to the mask RTD-OEIC-1. It describes the purpose and critical dimensions of each set of structures on the mask. It is organized to follow the circuit flow (cell name flow) presented in the MIT-OEIC-3/NCIPT-OEVLSI-1 Optoelectronic VLSI GaAs Chip Design and Testing Manual [25].

Device Specifications

All the RTDs and their respective mesas are oriented at 45° to the mask so that the mesa etch proceeds on crystallographic planes. Upper metal level must travel over the discontinuities in height formed by the device and mesa layers. Whenever possible, these contacts traverse both 45° planes, one of which should have a dove-tail profile suitable for metallization. If possible a large collector contact is made in nonimplanted growth wells. Table B.1 lists the standard device sizes used in this mask.

Name	Device Area (μm^2)	Diagonal (μm)	Via Area (μm^2)	Via Diagonal (μm)
4HS	22.5×22.5	32	12×12	8.5
5□	15×15	21	7×7	10
4□	10×10	14	5×5	7
3□	7.5×7.5	10	3.5×3.5	5
2□	5×5	7	2×2	2.8
1□	2×2	2.8	1×1	1.4
collector	20×20	28	12×12	8.5

Table B.1: Standard RTD dimensions.

The mask layout follows a few other layout rules. Where possible, the mesas extend 15 μm beyond the RTD. An attempt is made to keep all activity in the well, mesa included, 5 μm into the well.

In general, bond pads are HUGE to assure that metal can get back over the mesa and over any lip left at the edge of the well after the polycrystalline material removal. However, there are a few "aggressive contacts" in regions space is limited or where parasitics are of concern. For devices with adjacent collector contacts, the bond pad metal extends 5 μm beyond the diode and there are 6 μm between adjacent bond-metal-to-device contacts.

In cells where the underlying circuitry is utilized, vias are made in the RTD oxide to contact the Vitesse bond pads. At the time this mask was designed, it was not know how well the RTD

bond metal would adhere to the Vitesse pads during bonding. The Vitesse pads are left exposed (not overlaid with RTD bond metal) in these circuits. In the future, these Vitesse pad should be overlaid with bond metal [24]. Many of the RTDs utilize growth wells intended for other devices. The RTD bond pads are deposited on top of the Vitesse pads to take advantage of the pad layout and planarity. However, in these instances, vias are not made down to the Vitesse pads.

PCM

This process control monitor bar exists for qualification of discrete devices. Certain devices within this bar are exposed to serve as possible discrete devices for hybrid RTD-EFET circuits. An aggressive two-contact RTD is placed in the PCM growth well to evaluate the feasibility of utilizing small, nonimplanted growth wells.

The FETs exposed are: EFET 1 – 20×20 μm, EFET 2 – 20×10 μm, EFET 3 – 20×5 μm, EFET 4 – 20×1.2 μm, EFET 5 – 3×20 μm, EFET 5 – 3×2.6 μm, EFET 7 – 3×2 μm, EFET 8 – 3×1.2 μm, DFET 9 – 20×20 μm, DFET 10 – 20×10 μm, DFET 11 – 20×5 μm, DFET 12 – 20×1.2 μm. The metal snakes, resistors, and TLM structures are also exposed.

There is one nonimplanted 50×50 μm growth well in the PCM. A 3□ with collector contact is placed there. The contacts are aggressive. There are no vias to the Vitesse pads in this RTD structure.

There are two metal snakes to measure the RTD bond metal sheet resistance. The wire is 10 μm wide. The first one traverses a number of bond pads, and has a length of 640 squares. The second snake does not traverse any ridges of any kind and has a total length of 912 squares.

Well_array

This structure enables the study of the growth of single-crystal material in growth wells of different sizes, sidewall profiles, and implantation schemes.

Rows 1, 2, and 3 have angled sidewalls. Rows 4, 5, and 6 have straight sidewalls. Rows 1, 3, 4, and 6 are fully implanted. Rows 2 and 5 are implanted for approximately 25% of the well area on the row side of the well. Diodes are centered in the wells. In columns G and H, the 5 μm border rule is violated. The diode sizes are listed in Table B.2.

	A	B	C	D	E	F	G	G
6	5□	5□	4□	4□	3□	2□	1□	1□
5	5□	5□	4□	4□	3□	2□	2□	1□
4	4HS	4HS	5□	5□	4□	3□	2□	1□
3	5□	5□	4□	4□	3□	2□	1□	1□
2	5□	5□	4□	4□	3□	2□	2□	1□
1	4HS	4HS	5□	5□	4□	3□	2□	1□

Table B.2: Well-array device sizes.

Laser_array

These circuits provides RTDs for Time Domain Reflectometry (TDR).

Rows 1, 2, and 3 are nonimplanted wells with a S_1GS_2 pad configuration. These devices can also be measured with a GSG probe, in which case there would be two identical diodes in parallel. Rows 4, 5, and 6 are implanted wells with a GS_1G pad configuration. All the diodes have minimum bond pad overlap to reduce parasitics for microwave measurements. The diodes are centered in the y-direction in the wells.

Rows 4, 5, and 6 have vias down to the Vitesse pads. The ground connection is formed through the well implant. The signal pad is not connected. A via is made to this pad to keep the final pad heights at the same level for better wear on the microwave probes. In Rows 1, 2, and 3, vias are not made to the Vitesse pads. Table B.3 lists the sizes of the RTDs in this cell.

	RTDMET1			RTDMET2		
Row	S_1	S_2	Edge	S_1	S_2	Edge
6	2□	–	5□	3□	–	5□
5	3□	–	5□	4□	–	5□
4	4□	–	5□	4□	–	5□
3	2□	2□	5□	3□	3□	5□
2	3□	3□	5□	4□	4□	5□
1	4□	4□	5□	4□	4□	5□

Table B.3: Laser array device sizes.

Opfet_array

This cell characterizes optical EFET geometry dependent responsivity and frequency response. The Vitesse bond pads for this structure are exposed to provide discrete optical FETs for RTD circuits.

MSM_TI_array

These structures study the quality of devices grown in the corners of wells. This will qualify the types of wells necessary for integration. They will help determine if large diodes can be processed close together.

MSM_TI pair C has 2□ and 3□ diodes in it. MSM_TI pair D has 4□ and 5□ diodes in it. The bond pads are big in this structure, and vias are not made to the Vitesse pads.

Align_poly_strip

This cell is used to align the PSTRIP mask. It is also used to align the first metal mask (RTDMET1 or RTDMET2) to the cleaned growth wells. During the polycrystalline material removal, stripes (and fish) will be etched into the single-crystal material in this cell's growth wells. The emitter metal will later be aligned to these features.

Align_upper_layers

This cell contains an instance of align_poly_strip as well as a 150×100 μm growth well. Alignment marks will be deposited in this growth well. A vernier structure and a cross are

used. The vernier fingers are 3 μm wide with the center finger aligned. Finger misalignment increases by 0.5 μm with each finger out from the middle, to a maximum of 2 μm. The squares are 9×9 μm. The crosses inside are 3 μm wide and fit 1 μm away from the edges of the squares.

LED_mirrors

These structures study RTD quality in growth wells with and without mirrors. This quality has implications if you want to combine RTDs with optical devices in the same well: for example quantum well detectors, lasers, and RTD circuits.

Pads 1 and 3 are the collector contact pads and have vias to the Vitesse bond pads. Pads 2 and 4 do not have vias. Identical 4□ devices are in both wells. The well associated with Pad 2 does not have a mirror and the well associated with Pad 4 has a mirror. The bond pads have been designed to allow optical access to the RTD tunneling layers.

Laser_and_driver

These structures provide RTD storage elements for measurements pertaining to the RTD-based SRAM bitcell. Diodes are also placed at the edge of the well to determine the feasibility of growing and processing devices at the edge of the chip.

In these chains the substrate is the storage node, and current flows in different directions in the load and driver RTDs.

Cell A has a nonimplanted growth well. Two 4□ diodes occur here in both RTDMET1 and RTDMET2. Vias are not made to Vitesse Pads A1 and A7. Cell B has an implanted growth well. A 2□ chain in RTDMET1 and a 3□ chain in RTDMET2 are connected to Pad B1 and A3. A 3□ chain in RTDMET1 and a 4□ chain in RTDMET2 are connected to pads A4 and A5. Pad B7 is the collector contact to the Cell B growth well. Only pad B7 has a via to the Vitesse bond pad. Single 5□ RTDs occur on the edges of the growth wells. All diodes are centered in the y-direction in the wells. To reduce parasitics in the storage element measurements, the bond pads on these devices are aggressive.

Optical_clock

These structures provide RTD storage elements for measurements pertaining to the RTD-based SRAM bitcell. Diodes are also placed at the edge of the well to determine the feasibility of growing and processing devices at the edge of the chip.

In these chains the substrate is the storage node, and current flows in different directions in the load and driver RTDs.

This cell is located directly above Laser_and_driver (LaD)and essentially continues the Laser_and_driver cell. A 2□ chain in RTDMET1 and a 3□ chain in RTDMET2 are connected to Pad 1 and pad LaD-B3. A 3□ chain in RTDMET1 and a 4□ chain in RTDMET2 are connected to pads LaD-B4 and LaD-B5. Pad 5 provides the collector contact to LaD well B, and is the only pad with a via to the Vitesse pads. All diodes are centered in the y-direction in the wells. To reduce parasitics in the diode chain measurements, the bond pads on these devices are aggressive.

Fet_uniformity

This cell is an EFET and DFET pair "sprinkled" around the chip to serve as uniformity monitors.

It is possible to string the FETs together to simulate a bigger FET. The EFETs are 10×1.2 μm and the DFETs are 2.8×3.4 μm. Vias have been opened to all of the Vitesse pads.

D_flip_flop

This will serve as a GaAs memory cell for comparison to RTD memory cells.

Vias have been opened to all of the Vitesse pads.

Vcro

This is a voltage controlled, frequency tunable right oscillator serving as a voltage tunable high-speed DCFL source.

Vias have been opened to all of the Vitesse pads.

Mwavedev

These FETs were originally intended for microwave characterization. They will be used as elements for hybrid RTD-EFET circuits.

There are 4 FETs: A – 10×1.2 μm EFET, B – 90×1.2 μm EFET, C – 10×3.6 μm DFET, and D – 40×3.6 μm DFET. (Tragically, EFET B is missing a connection.) Vias have been opened to all of the Vitesse pads.

Mwavedum

To test the resistances of the bond pads with and without gold on top of the pads, six of the microwave dummy pads have been opened. The probe will be put horizontally across a set of 3 pads. Pads A1, A4, and B1 have gold on top of the pad, and A1 and A4 are shorted together. Pads A2, A5, and B2 do not have gold on the Vitesse pads, and pads A2 and A5 are shorted together.

Seed_rec

These circuits will be used to study RTD storage elements that have RTDs in separate growth wells. The current flows in the same direction through the RTD load and driver devices. These circuits can also be used for optical RTD circuits. RTDMET1 and RTDMET2 device sizes are the same.

Identical 2□ devices are centered in each well. Pad SEED1–P provides the emitter contact to RTD–1. Pad SEED–COMMON connects the collector contact of RTD–1 to the emitter contact of RTD–2. Pad SEED2–N provides the collector contact to RTD–2. In the event that the circuitry might be useful, all of the full sized bond pads have vias down to the Vitesse pads. Only the SEED1–P pad is isolated from the circuit (no vias to Vitesse pad) to allow a bias to be applied to the RTD chain. To help in probing, gold is placed on top of all the smaller SEED access pads.

The RTD bond pads are small, and are only intended to be probed. To reduce parasitics in the storage element measurements, the bond pads on these devices are aggressive.

Seed_nor

This is a two input NOR constructed from DCFL circuitry.
Vias have been made to all Vitesse bond pads.

Seed_trans

These circuits will be used to study RTD storage elements that have RTDs in separate growth wells. The current flows in the same direction through the RTD load and driver devices. These circuits can also be used for optical RTD circuits. RTDMET1 and RTDMET2 device sizes are the same.

Identical 3□ devices are centered in each well. Pad SEED1–P provides the emitter contact to RTD–1. Pad SEED–COMMON connects the collector contact of RTD-1 to the emitter contact of RTD-2. Pad SEED2–N provides the collector contact to RTD–2. Bond pads 1 and 5 provide access to SEED1–P and SEED2–N respectively, and have vias to the Vitesse pads. Other bond pads are left covered. All SEED access pads have vias to the Vitesse pads, and are covered with gold.

The RTD bond pads are small, and are only intended to be probed. To reduce parasitics in the storage element measurements, the bond pads on these devices are aggressive.

Seed_rectrans

These circuits will be used to study RTD storage elements that have RTDs in separate growth wells. The current flows in the same direction through the RTD load and driver devices. These circuits can also be used for optical RTD circuits. RTDMET1 and RTDMET2 device sizes are the same.

There are two sets of SEED regrowth wells in this cell. Identical 2□ devices are centered in the well located between pads 2 and 3. Identical 3□ devices are centered in the well located between pads 1 and 4. Pad SEED1–P provides the emitter contact to RTD–1. Pad SEED–COMMON connects the collector contact of RTD–1 to the emitter contact of RTD–2. Pad SEED2–N provides the collector contact to RTD–2. This circuit is missing wires, and therefore only the SEED-contact pads are useful, but a via has been made to pad SEED1–P to connect it to bond pad 2. All SEED access pads have vias to the Vitesse pads, and are covered with gold.

The RTD bond pads are small, and are only intended to be probed. To reduce parasitics in the storage element measurements, the bond pads on these devices are aggressive.

Seed_recnortrans

These circuits will be used to study RTD storage elements that have RTDs in separate growth wells. The current flows in the same direction through the RTD load and driver devices. These circuits can also be used for optical RTD circuits. RTDMET1 and RTDMET2 device sizes are the same.

There are three sets of SEED regrowth wells in this cell. Identical 2□ devices are centered in the well located above pads 2 and 3. Identical 3□ devices are centered in the well located between pads 2 and 3. Identical 4□ devices are centered in the well located between pads 1 and 4. Pad SEED1–P provides the emitter contact to RTD–1. Pad SEED–COMMON connects the collector contact of RTD–1 to the emitter contact of RTD–2. Pad SEED2–N provides the collector contact to RTD–2. This circuit is missing wires, and therefore only the SEED-contact

pads are useful, but a via has been made to pad SEED1–P to connect it to bond pad 2. All SEED access pads have vias to the Vitesse pads, and are covered with gold.

The RTD bond pads are small, and are only intended to be probed. To reduce parasitics in the storage element measurements, the bond pads on these devices are aggressive.

Efet_oe_inv

Originally intended as an optical-electrical inverter, this cell can be used to study RTD-FET logic. In addition, it can be adapted to form a 1-bit RTD SRAM memory cell. Unfortunately, the growth well is not connected to the circuit. Therefore, this circuit will be used to study RTD storage elements offset in larger wells. An additional diode provides information on large devices grown in large wells. RTDMET1 and RTDMET2 device sizes are the same.

A 2□ diode chain is connected between pads 4 and 7. A 5□ single diode is connected to pad 6. Pad 5 is the contact to the implanted well and serves as the storage node contact for the diode chain and the collector contact for the single device. Because of a missing wire, this pad is metalized in post-growth processing. There are no vias to Vitesse bond pads. To fit 3 diodes in the well, the bond pads on these devices are aggressive.

Dfet_oe_inv

Originally intended as an optical-electrical inverter, this cell can be used to study RTD-DFET logic. In addition, it can be adapted to form a 1-bit RTD SRAM memory cell using a DFET.

A 2□ load RTD (RTDMET1) is connected to pad 6. Pad 5 is the storage node of the cell. A second 2□ RTD (RTDMET1) is connected to a bond pad made during RTD processing. In RTDMET2, the devices are both 3□s. The diodes are positioned close to the implant connection to reduce access resistance. All 10 original circuit bond pads have vias opened to the Vitesse pads.

Dcfl_oe_inv

Originally intended as an optical-electrical inverter, this cell can be used to study RTD-FET logic. In addition, it can be adapted to form a 1-bit RTD SRAM memory cell. Unfortunately, the growth well is not connected to the circuit. Therefore, this circuit will be used to study RTD storage elements offset in larger wells. An additional diode provides information on large devices grown in large wells. RTDMET1 and RTDMET2 device sizes are the same.

A 2□ diode chain is connected between pads 4 and 7. A 5□ single diode is connected to pad 6. Pad 5 is the contact to the implanted well and serves as the storage node contact for the diode chain and the collector contact for the single device. Because of a missing wire, this pad is metalized in post-growth processing. There are no vias to Vitesse bond pads. To fit 3 diodes in the well, the bond pads on these devices are aggressive.

ORODERED1

It is conceivable that the epitaxial heterostructures can be confined to central regions of a circuit. This structure simulates such an environment. Multiple devices are fabricated within a large well. The performance will be compared to devices fabricated individually in a well. In this cell, the devices are centered in the y-direction within the well. These devices will also

be compared to ones staggered within a well. RTDMET1 and RTDMET2 device sizes are the same.

There are 7 devices fabricated in each well. The upper well contains 2□ devices and the lower well contains 3□ devices. The edges of the wells contain single 5□ devices that are also staggered. Both wells are implanted. The upper well is contacted through the pad LASER BIAS and the lower well is contacted through the lower most large bond pad. Both of these pads have vias to the Vitesse layers. The diode emitters are contacted through 35×40 μm pads located between the wells. The pads are 15 μm apart and 10 μm from the edge of the underlying Vitesse pad. These pads are intended for probing purposes only.

ORODERED2

It is conceivable that the epitaxial heterostructures can be confined to central regions of a circuit. This structure simulates such an environment. Multiple devices are fabricated within a large well. The performance will be compared to devices fabricated individually in a well. In this cell, the devices are centered in the y-direction within the well. These devices will also be compared to ones staggered within a well. RTDMET1 and RTDMET2 device sizes are the same.

There are 7 devices fabricated in each well. The upper well contains 2□ devices and the lower well contains 3□ devices. The edges of the wells contain single 5□ devices that are also staggered. Both wells are implanted. The upper well is contacted through the pad LASER BIAS and the lower well is contacted through the lower most large bond pad. Both of these pads have vias to the Vitesse layers. The diode emitters are contacted through 35×40 μm pads located between the wells. The pads are 15 μm apart and 10 μm from the edge of the underlying Vitesse pad. These pads are intended for probing purposes only.

ORODERED3

It is conceivable that the epitaxial heterostructures can be confined to central regions of a circuit. This structure simulates such and environment. Multiple devices are fabricated within a large well. The performance will be compared to devices fabricated individually in a well. In this cell, the devices are staggered in the y-direction within the well. These devices will be compared to ones centered within a well.

There are 7 4□ devices fabricated the well. The edge of the well contains single 5□ devices. The well is contacted through the pad LASER BIAS, which has a via to the Vitesse layers. The diode emitters are contacted through 35×40 μm pads, located between the wells. The pads are 15 μm apart and 10 μm from the edge of the underlying Vitesse pad. These pads are intended for probing purposes only.

Array4×1_4

This cell is used to extract the ohmic contact resistance dependence on the ohmic contact size and metal 1 via size. Comparisons will be made between pre- and post-growth values.

Vias are made to all Vitesse pads.

Array4×3_0

This cell is used to extract the ohmic contact resistance dependence on the ohmic contact size and metal 1 via size. Comparisons will be made between pre- and post-growth values.
Vias are made to all Vitesse pads.

Array2×1_4

This cell is used to extract the ohmic contact resistance dependence on the ohmic contact size and metal 1 via size. Comparisons will be made between pre- and post-growth values.
Vias are made to all Vitesse pads.

Array2_4×1_4_nometl

This cell is used to extract the ohmic contact resistance dependence on the ohmic contact without metal 1 via. Comparisons will be made between pre- and post-growth values.
Vias are made to all Vitesse pads.

Ringosc

This cell is used to extract the ring oscillator inverter delay with MESFET source and drain ohmic contacts having metal 1 interconnections. Comparisons will be made between pre- and post-growth values.
Vias are made to all Vitesse pads.

Ringosc_nometl

This cell is used to extract the ring oscillator inverter delay with MESFET source and drain ohmic contacts having gate metal interconnections. Comparisons will be made between pre- and post-growth values.
Vias are made to all Vitesse pads.

Inverter

This cell is used to extract inverter I–V characteristics with MESFET source and drain ohmic contacts having metal 1 interconnections. Comparisons will be made between pre- and post-growth values. The inverter is also available for integration with RTD circuits.
Vias are made to all Vitesse pads.

Inverter_nomet

This cell is used to extract inverter I–V characteristics with MESFET source and drain ohmic contacts having gate metal interconnections. Comparisons will be made between pre- and post-growth values. The inverter is also available for integration with RTD circuits.
Vias are made to all Vitesse pads.

Inverter_fets

These FETs were intended for extraction of the corresponding ring oscillator FET I–V characteristics. Comparisons will be made between pre- and post-growth values. They are available for integration with RTD circuits.

Vias are made to all Vitesse pads.

Inverter_fets_nometl

These FETs were intended for extraction of the corresponding ring oscillator FET I–V characteristics. Comparisons will be made between pre- and post-growth values. They are available for integration with RTD circuits.

Vias are made to all Vitesse pads.

Memdc

This is a series of single-bit RTD SRAM cells. The cells are designed to study the effects of RTD parameters such as size, doping, and peak-to-valley current and voltage ratios on the basic operation of the SRAM.

The growth wells in this cell are implanted. Circuit A has 2 4□ diodes (RTDMET1) spaced as close to the center as possible. Circuit B has 2 2□ diodes (RTDMET1) spaced as close to the center as possible. In RTDMET2 both sets of diodes are 3□. The storage node contact is the implanted well, which is directly connected to the FETs in the cell.

Vias are made to all FET pads in both cells, but not to the VRTD and VGND pads. The bond pads are aggressive.

Memdcnoimp

This is a series of single-bit RTD SRAM cells. The cells are designed to study the effects of RTD parameters such as size, doping, and peak-to-valley current and voltage ratios on the basic operation of the SRAM.

The growth wells in this cell are not implanted. Circuit A has 2 4□ diodes (RTDMET1) spaced as close to the center as possible. Circuit B has 2 2□ diodes (RTDMET1) spaced as close to the center as possible. In RTDMET2 both sets of diodes are 3□. Contact to the storage node is made as close to the RTDs as possible and brought out to pads which connect to the FETs in the circuit.

Vias are made to all FET pads in both cells, but not to the VRTD and VGND pads. The bond pads are aggressive.

Mem_array

This is a 4-bit RTD SRAM. It is designed to study density issues such as the effects of RTD nonuniformity on SRAM performance. In addition, it examines the effects of line capacitance on individual cell performance.

There are 4 identical growth wells. In each well, 2 4□ diodes (RTDMET1) are spaced as close to the center as possible. In RTDMET2 all four sets of diodes are 3□. Vias are made to all pads. Gold only covers RTD access bond pads.

Stripe

This is a large growth area that will be used to evaluate the performance of RTDs grown on GaAs VLSI circuits. The area extends diagonally across the chip and is ideal for uniformity studies. There are also growth regions lining the edges of the chip and large devices will be fabricated in these regions. Parameters that will be evaluated are: growth quality, implant quality (doping effects), the manufacturability of different regions of the chip. In addition, this area will be used for alignment marks and RTD process monitors. There are numerous subcells used within this cell and they will be addressed in turn.

TLM_top

This is a TLM structure designed to evaluate the contact resistance of the RTD emitter contact. The TLM structures occur in nonimplanted regions of the stripe. During the polycrystalline material removal processing step, the TLM regions will be isolated from the rest of the stripe. The mesa etch step will be used to further restrict the current flow in this TLM structure. The TLM structure has 5 40×60 μm^2 pads separated by 5 μm, 7.5 μm, 10 μm, and 15 μm. These are the upper-right and lower-left TLM structures on the mask.

TLM_bottom

This is a TLM structure designed to evaluate the contact resistance of the RTD collector contact. The TLM structures occur in nonimplanted regions of the stripe. During the polycrystalline material removal processing step, the TLM regions will be isolated from the rest of the stripe. During the mesa etch, the substrate side RTD contact will be exposed. The TLM structure has 5 40×60 μm pads separated by 5 μm, 7.5 μm, 10 μm, and 15 μm. These are the lower-right and upper-left TLM structures on the mask.

Edge_5_single

This is a 5□ device with an adjacent collector contact. It will fit in narrow regions on the edge of the chip. These devices are meant to be probed.

Edge_5_square

This is a 5□ device with an adjacent collector contact. It is designed to fit in a laser growth well edge extension. Some of these have pads which extend into adjacent growth wells. If contact to the pad is not made, these devices can still be probed.

Edge_5_staggered

This is a series of three 5□ devices staggered following the layout of RTDs in the ORODERED series. These will be used to evaluate how closely edge RTDs can be placed.

Angled_3_square

This is a 3□ RTD designed to fit in the smaller of the two diagonal stripes. These RTDs are designed to be probed only.

RTD_block

This is a block of 6 RTDs designed to fit in the large growth well that crosses the chip. There are 2 2□, 2 3□, and 2 4□ RTDs in RTDMET1 and 2 3□, 2 4□, and 2 5□ RTDs in RTDMET2. Each RTD has an associated collector contact. The bond pads for the collector contacts are shared so that current flows in opposite directions through the devices. These diodes can easily be tested individually or in diode chains. This cell also has the RTD fine alignment marks. These are copied from earlier group RTD masks and consist of a partial cross and a box. The cross is made from 2, 4, and 6 μm steps, each 3 μm long. The box at the cross intersection is 2×2 μm. A space of 0.5 μm is given for alignment of the upper layers. The squares in the box are also 2×2 μm. The box is 8×8 μm.

RTD_block

This is a block of 6 RTDs designed to fit in the large growth well that crosses the chip. There are 2 2□, 2 3□, and 2 4□ RTDs in RTDMET1 and 2 3□, 2 4□, and 2 5□ RTDs in RTDMET2. Each RTD has an associated collector contact. The diodes are connected so that current flows in the same direction in each device. These diodes can easily be tested individually or in diode chains. This cell also has the RTD fine alignment marks. These are copied from earlier group RTD masks and consist of a partial cross and a box. The cross is made from 2, 4, and 6 μm steps, each 3 μm long. The box at the cross intersection is 2×2 μm. A space of 0.5 μm is given for alignment of the upper layers. The squares in the box are also 2×2 μm. The box is 8×8 μm.

C

Integrated RTD Process Flow

There are two basic process flows used in the fabrication of integrated RTD-EFET circuits. Both of these flows are supported by the RTD-OEIC-1 mask set. The first is the process used to clean the DGWs. The second is the process used to fabricate the RTDs. The RTD-OEIC-1 mask set also has provisions for a test metalization. There are copies of the mask available for both positive and negative resists. One caveat: the masks, and thus the alignment marks, were made for positive resist.

DGW Cleaning Flow

1. Solvent clean: Perform an ultrasound clean in TCA, acetone, and methanol to remove any black wax left on the chips from the sawing process. Times for the clean will vary from chip to chip.

2. Aluminum mask deposition: Evaporate at least 400 nm, of aluminum for a mask. We use the aluminum evaporator in the Microlab. You will need 14 clips to get at least 400 nm. You might get substantially more depending on the amount of aluminum left in the filament, but more aluminum is OK. Use a silicon monitor during the evaporation for thickness tests as well as etch monitors.

3. Pattern the metal mask: This step uses mask level WCLEAN. This mask level was designed for a positive resist. Ultimately, we used Futurex NR8-3000 to pattern the mask. This is a thick NEGATIVE resist. If you use a negative resist, make sure you have the inverted mask. Develop and asher following normal parameters of the resist of your choice.

4. Etch the mask: The aluminum is etched using PAN etch: 10% water, 80% Phosphoric, 5% Nitric, and 5% Acetic acid. The acid needs to be at 45°C for best results. Test the etch on a dummy aluminum sample. At this point, the chip is masked and ready for etching. DO NOT strip the resist.

5. BOE clean: BOE dip with ultrasound for 1 minute. This will remove the residue left by Vitesse in the growth wells.

6. RIE: This etch will take approximately 4.5 hours. You need to use the Ardel plate with 3-inch silicon wafers in the holes. The parameters are 45 sccm CF_4 and 10 sccm O_2 at 50 mTorr and 200 watts. Use the power regulated mode. You will need to etch through about 3 μm of dielectric. Monitor the etch visually. The implanted regions will clear first. Over etching will damage the crystal surface. At this point, you can choose to remask the

chip and finish the etch with BOE. Depending on how much dielectric is left in the DGW, the BOE may or may not damage the electronics.

7. Post etch clean: Do a thorough solvent clean in ultrasound (at least 15 minutes/solvent) and then asher the chips to remove any organics left from the cleaning process.

8. Pre-MBE clean: Immediately before mounting the chip for MBE growth, another ultrasonic solvent clean is recommended. Following that, a short BOE dip is used to remove surface oxide.

Test Metalization

The mask level TESTMET is used to test the integrity of the n+ implant by evaporating a number of ohmic contacts in the well. This step WILL NOT be performed on chips to be used for epitaxial device integration purposes. This level was designed for a standard positive resist process.

RTD Process Flow

1. Polycrystalline material removal: Remove the polycrystalline material from the chip. Mask PSTRIP is used here. This mask has reverse polarity from all the others on the chip. The growth wells plus a 5 μm buffer will be protected. Since the etch of the polycrystalline material is isotropic, the etch will come under the resist. The buffer is designed to protect the single crystal material in the well. Use 1:1:5 H_3PO_4:H_2O_2:H_2O as the etchant. The time of the etch will vary depending on the epitaxial thickness. Over etch approximately 30 seconds to insure that all the polycrystalline material is removed. The standard positive resist process is:

   (a) Spin HMDS
   (b) Spin Shipley 1400-27, 5000 RPM, 40 sec.
   (c) Softbake, 90°C, 30 minutes.
   (d) Remove the edge bead with acetone sprayed on a foam swab. Run the swab along the side of the chip. The acetone will creep around the edge. If you wipe the swab on the top of the chip, you will remove too much resist.
   (e) Expose 7 seconds (45 seconds) for the standard (high-resolution) aligner. Warning, this number will change with differing process environments. Adjust this time to make the development time one minute.
   (f) Develop in MF-319. The development time should be one minute.
   (g) Asher 100 watts for one minute.

   Because of the mask design, edge bead removal is not necessary for this step.

2. RTD emitter contacts: Evaporate the surface RTD contacts, referred to as emitter contacts. There are two different masks for the emitters. These are identical with the exception of sizes for the RTDs in the SRAM cells. They are RTDMET1 and RTDMET2. These masks were designed for positive resists. AuGe/Ni/Au ohmic contacts are used for the emitters. The topology of the chip required a thick resist, and therefore Futurex NR8-3000, was used for the lift-off. The standard negative resist process is:

   (a) Spin HMDS

(b) Spin Futurex NR8-3000, 5000 RPM, 40 seconds.

(c) Softbake, 90°C, 30 minutes.

(d) Expose 20 seconds on the standard aligner. Warning, this number will change with differing process environments.

(e) Develop in Futurex D2 developer, 2.5 minutes.

(f) Asher 100 watts for one minute.

3. Mesa etch: The RTD mesas are etched using a self-aligned process. However, the surrounding circuit regions must be protected. Mask RTDMESA is used in this step. 1:8:160 H_2SO_4:H_2O_2:H_2O will be used as the etchant. Use the standard positive resist process.

4. RTD collector contacts: Substrate contacts to the RTDs, referred to as the collector contacts, will be made using standard lithography and lift-off techniques using mask RTD-MET3. Again, AuGe/Ni/Au will be used for the ohmic.

5. Contact alloy: Rapid thermal anneal the contacts at 375° for 15 seconds.

6. Passivation: SiO_x will be deposited for isolation between the diode material and the bond pads. Deposit 200 nm of dielectric. Run dummy samples during the deposition to serve as etch monitors.

7. Via etch: The RTDVIA mask will open vias in the oxide for contact between the bond pads and the emitter and collector contacts. Use the standard positive resist process and the RTDVIA mask. Etch the vias in BOE using a time determined by the etch monitors.

8. Bond pads: Evaporate Cr/Au bond pads using mask RTDBOND. This mask was designed for a positive resist. Use the inverted version of the mask and the standard negative resist process.

Bond Pad Protection

If the bond pad protection process is desired, a layer of dielectric is deposited over the entire chip before cleaning the wells. The well cleaning, growth, and polycrystalline material strip proceed as above. Then, the RTDVIA mask is used to open vias in the top dielectric down to the Vitesse pads. This is done in the same manner as the via etch. Because there is no oxide over the DGWs, the device vias in the RTDVIA mask will only expose the grown crystal to BOE and will not be a problem.

ERS RTD Processes

When the RTD process is used on material grown on an ERS, a positive resist lift-off process can be used. Chlorobenzene is used to create resist profile more suitable for lift-off. The standard positive resist lift-off lithography process is:

1. Spin HMDS

2. Spin Shipley 1400-27, 5000 RPM, 40 sec.

3. Softbake, 90°C, 30 minutes.

4. Remove the edge bead with acetone sprayed on a foam swab. Run the swab along the side of the chip. The acetone will creep around the edge. If you wipe the swab on the top of the chip, you will remove too much resist.

5. Expose 7 (45) seconds on the standard (high-resolution) aligner. Warning, this number will change with differing process environments. Time this so that the development time is 1 minute without chlorobenzene.

6. Soak 8 minutes in chlorobenzene. This number will change with differing process environments. The time is chosen such that there is a 15 second delay in the appearance of a pattern during developing.

7. Softbake 5 minutes to drive off the chlorobenzene.

8. Develop in MF-319. The development time should be 1 minute 15 seconds with the chlorobenzene dip.

9. Asher 100 watts for one minute.

10. Evaporate contacts.

D

RTD-EFET Ring Oscillator

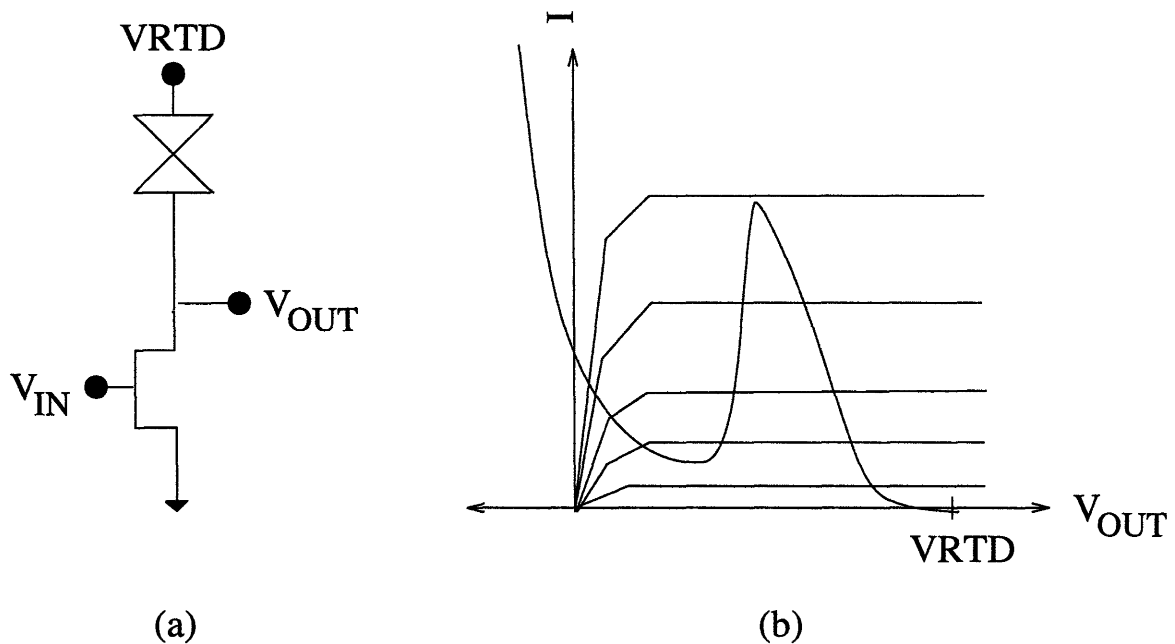


Figure D-1: (a) Schematic of a RTD-EFET inverter. (b) Load line characteristics of a RTD-EFET inverter.

Many of the performance studies that the RTD-EFET SRAM cells are designed for are applicable to RTD logic circuits as well. The basic element of RTD logic circuits is an RTD-EFET inverter. Figure D-1 shows the RTD-EFET inverter topology and load line characteristics. The speed of an RTD-based inverter is limited by the RTDs inability to charge the inverter output node. There is a substantial difference in the rise and fall times of an RTD-EFET inverter. When the output of the inverter falls, the RTD current rises, discharging the output node capacitance. When the inverter output rises, the RTD must charge the capacitor. However, because the RTD is in its valley region it cannot supply much current until the node voltage rises such that the RTD is in its NDR region.

MIT-OEIC-4 includes a 23-stage RTD-EFET ring oscillator. This circuit will be used to

evaluate the effect of RTD parameter variations on logic circuits. The ring oscillator will also be compared to a DCFL ring oscillator to provide an experimental evaluation of the two logic families.

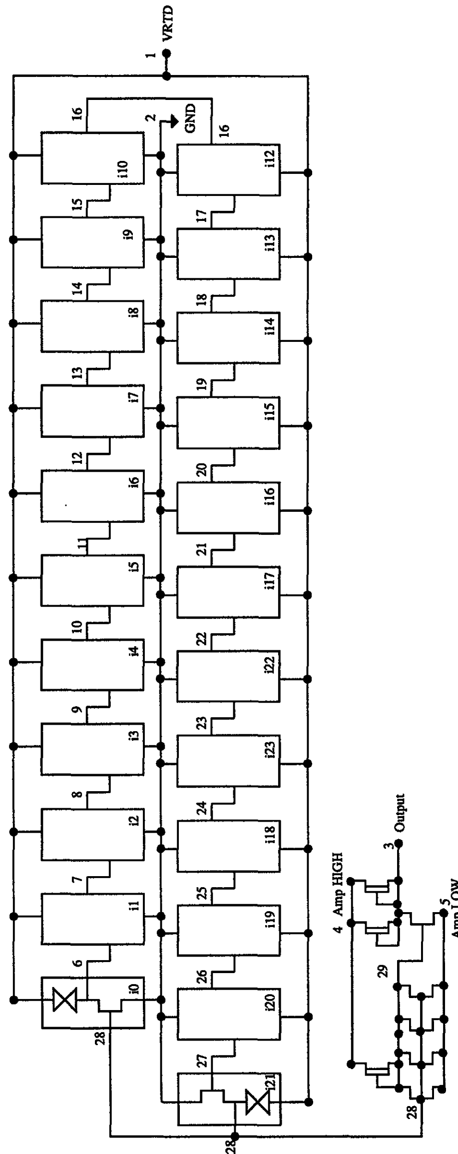


Figure D-2: Schematic of 23-stage RTD-EFET ring oscillator. HSPICE nodes are numbered.

Figure D-2 is a schematic of the ring oscillator circuit. Individual inverters are comprised of an EFET loaded by a RTD. There are two output stages to buffer and amplify the output. Figure D-3 shows the layout of the circuit. The three implanted growth wells will house the RTDs. The wells are electrically connected to each other and to a bond pad. Therefore, the substrate contact of the RTDs will be the supply connection. The top-side RTD contact will be the inverter stage output node, and will be connected to the EFETs in upper-level RTD bond

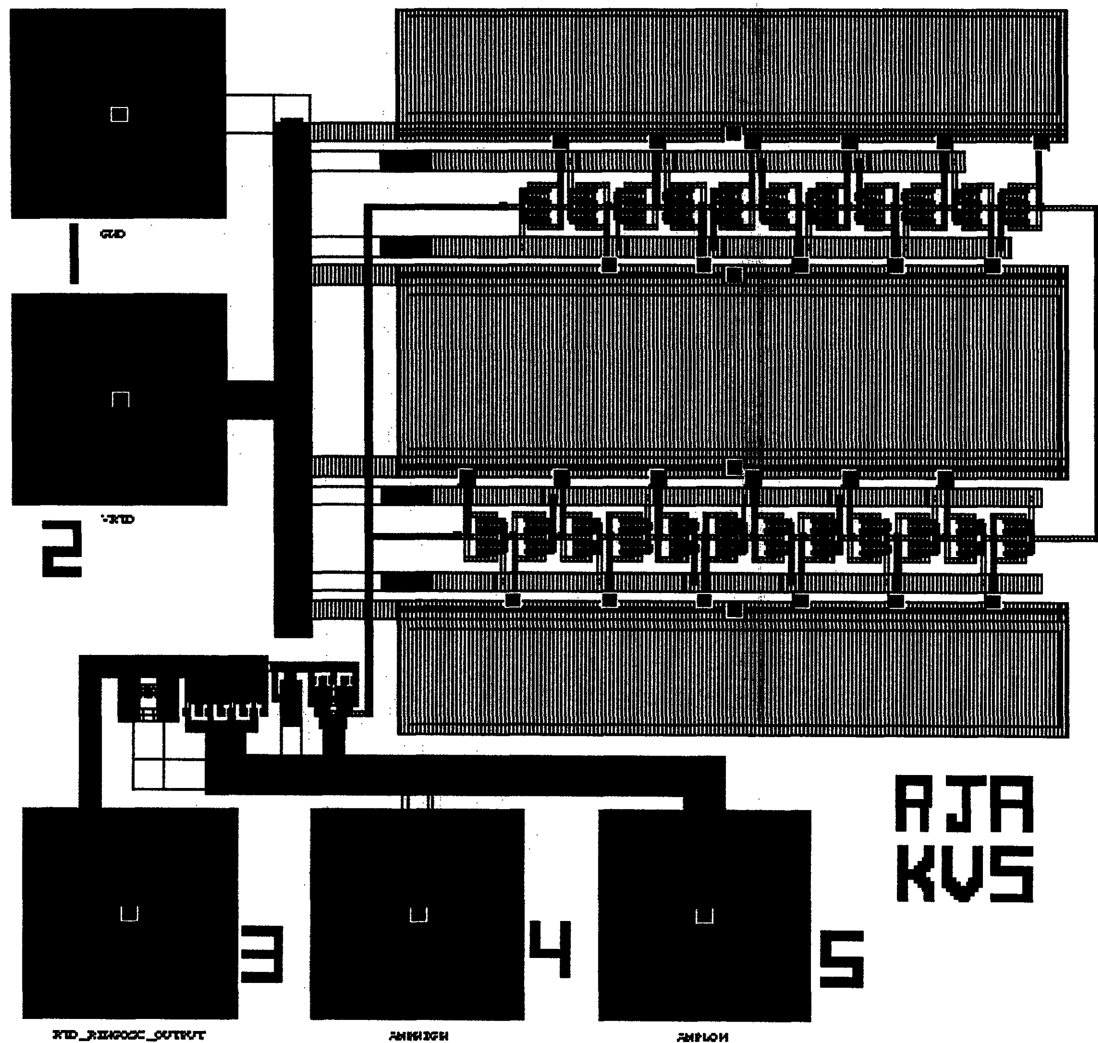


Figure D-3: Layout of 23-stage RTD-EFET ring oscillator.

pad metal. The inverter EFETS and the first buffer stage EFET are 40×1.2 μm. The second buffer stage EFET is 84×1.2 μm. The output stage DFETs are 10×3 μm.

Figure D-4 shows the simulated operation of the ring oscillator. The HSPICE elements are extracted from the layout of the cell. The RBRTDs have areas of 9 μm^2. The first panel shows the input (dashed line) and output (solid line) node voltages for an inverter stage. The second panel shows the voltage at the output of the buffer stage. As expected, there is a difference between the rise and fall time of the output node.

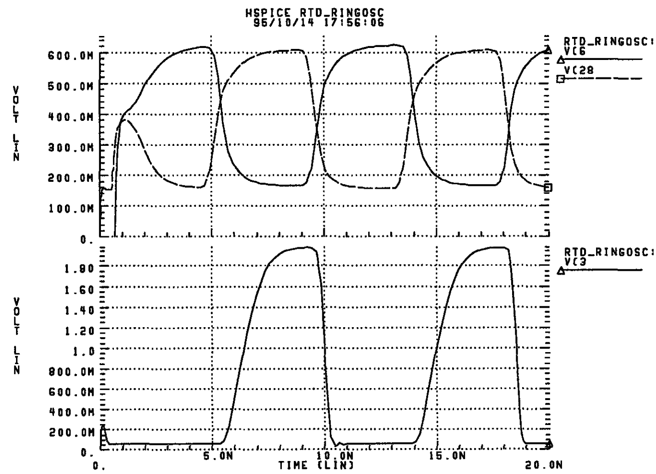
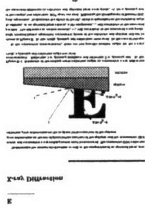


Figure D-4: Simulated operation of 23-stage RTD-EFET ring oscillator. Details of the panels are described in the text.



X-ray Diffraction

To determine the amount of relaxation as well as the composition of an epitaxial layer, symmetric and asymmetric x-ray rocking curves must be measured. The symmetric (004) reflection gives information on the out-of-plane lattice constant of the epilayer and the asymmetric (224) reflection gives information on the in-plane lattice constant of the epilayer.

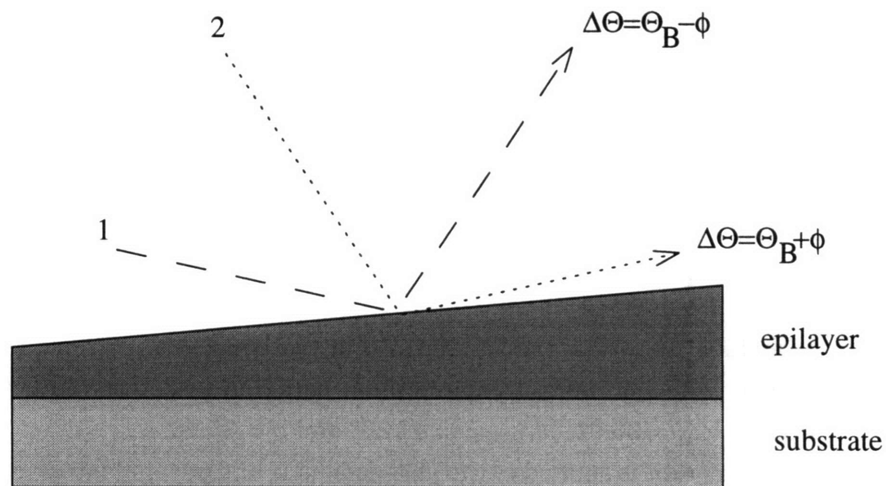


Figure E-1: Schematic of the rocking curve reflection angles in asymmetric x-ray diffraction measurements. Reflection 1 is glancing incidence and reflection 2 is glancing exit. In this study, a glancing exit reflection angle was used.

In the asymmetric measurements, there are two possible incident angles for the x-rays, shown in Figure E. In this study, glancing exit reflections were used. In the case of

measurement is:

$$\delta\theta_1 = \delta\theta_B - \delta\phi + \omega\,, \tag{E.1}$$

$$\delta\theta_2 = \delta\theta_B - \delta\phi - \omega\,, \tag{E.2}$$

$$\frac{\delta\theta_1 + \delta\theta_2}{2} = \delta\theta_{ave} = \delta\theta_B - \delta\phi\,, \tag{E.3}$$

where $\delta\theta_B$ is the difference in Bragg angles of the substrate and epilayer. Equation E.3 can be written in terms of the perpendicular and parallel lattice constant differences:

$$\delta\theta_B = -\left[\left(\frac{\delta a}{a}\right)_{\perp}\cos^2\phi + \left(\frac{\delta a}{a}\right)_{\|}\sin^2\phi\right]\tan\theta_B\,, \tag{E.4}$$

where θ_B is the Bragg angle of the substrate and ϕ is the angle between the surface and the diffracting plane, and

$$\delta\phi = \left[\left(\frac{\delta a}{a}\right)_{\perp} - \left(\frac{\delta a}{a}\right)_{\|}\right]\sin\phi\cos\phi\,. \tag{E.5}$$

Substitution of Equations E.4 and E.5 into Equation E.3 gives

$$\delta\theta_{ave} = \left(\frac{\delta a}{a}\right)_{\|}\left(-\sin^2\phi\tan\theta_B + \sin\phi\cos\phi\right) + \left(\frac{\delta a}{a}\right)_{\perp}\left(-\cos^2\phi\tan\theta_B - \sin\phi\cos\phi\right)\,. \tag{E.6}$$

For the symmetric reflection $\delta\phi = 0$, and Equation E.6 reduces to

$$\delta_{ave} = -\left(\frac{\delta a}{a}\right)_{\perp}\tan\theta_B\,. \tag{E.7}$$

In the case of orthorhombic distortion the two parallel lattice constants are unequal, and thus two sets of asymmetric reflection measurements must be taken to determine $\left(\frac{\delta a}{a}\right)_{\|,[1\bar{1}0]}$ and $\left(\frac{\delta a}{a}\right)_{\|,[110]}$. For GaAs, $\theta_{B,(004)} = 33.01^o$, $\theta_{B,(224)} = 41.86^o$ and $\phi = 35.26^o$.

The relaxed lattice constant is related to the perpendicular and parallel lattice constants by

$$\left(\frac{\delta a}{a}\right)_R = \frac{1-\nu}{1+\nu}\left(\frac{\delta a}{a}\right)_{\perp} + \frac{\nu}{1+\nu}\left[\left(\frac{\delta a}{a}\right)_{\|,[1\bar{1}0]} + \left(\frac{\delta a}{a}\right)_{\|,[110]}\right]\,, \tag{E.8}$$

where ν is Poisson's ratio for the epilayer, and is also a function of indium mole fraction. The relaxed lattice constant can then be related to the indium content of the layer by Vegard's law:

$$\left(\frac{\delta a}{a}\right)_R = \frac{a_{epi} - a_{sub}}{a_{sub}}\,, \tag{E.9}$$

$$= \frac{[x a_{InAs} + (1-x)a_{GaAs}] - a_{GaAs}}{a_{GaAs}}\,, \tag{E.10}$$

$$= x\frac{a_{InAs} - a_{GaAs}}{a_{GaAs}}\,, \tag{E.11}$$

$$13.995\left(\frac{\delta a}{a}\right)_R = x\,. \tag{E.12}$$

To fully characterize an orthorhombically distorted layer, six x-ray scans are required. This is a time consuming endeavor that is desirable to avoid. To reduce the number of required x-ray scans, assumptions can be made as to the degree of relaxation in epitaxial layer. There are three possible states for the epilayer to be in: fully relaxed, partially relaxed, and psuedomorphic. For a fully relaxed epilayer

$$\left(\frac{\delta a}{a}\right)_{\|,[1\bar{1}0]} = \left(\frac{\delta a}{a}\right)_{\|,[110]} = \left(\frac{\delta a}{a}\right)_{\perp} = \left(\frac{\delta a}{a}\right)_R\,. \tag{E.13}$$

For a partially relaxed epilayer

$$\left(\frac{\delta a}{a}\right)_{\|,[1\bar{1}0]} \neq \left(\frac{\delta a}{a}\right)_{\|,[110]} < \left(\frac{\delta a}{a}\right)_R < \left(\frac{\delta a}{a}\right)_{\perp}\,. \tag{E.14}$$

And, for a pseudomorphic epilayer

$$\left(\frac{\delta a}{a}\right)_{\|,[1\bar{1}0]} = \left(\frac{\delta a}{a}\right)_{\|,[110]} = 0\,, \tag{E.15}$$

$$\left(\frac{\delta a}{a}\right)_R \approx \frac{1}{2}\left(\frac{\delta a}{a}\right)_{\perp}\,. \tag{E.16}$$

If we assume that the layer is fully relaxed, only the perpendicular lattice constant need be evaluated at a cost of two x-ray scans. If we assume tetragonal distortion, i.e. $\left(\frac{\delta a}{a}\right)_{\|,[1\bar{1}0]} = \left(\frac{\delta a}{a}\right)_{\|,[110]}$, four scans must be taken. And if orthorhombic distortion is assumed, the full six scans must be made.

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5224-6