Environmentally Benign Manufacturing of Three Dimensional Integrated Circuits

by

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Submitted to the Department of Materials Science and Engineering
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

at the

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Abstract

Along with scaling down in size, novel materials have been introduced into the semiconductor industry to enable continued improvements in performance and cost as predicted by Moore's law. It has become important now more than ever to include an environmental impact evaluation of future technologies, before they are introduced into manufacturing, in order to identify potentially environmentally harmful materials or processes and understand their implications, costs, and mitigation requirements. In this thesis, we introduce a methodology to compare alternative options on the environmental axis, along with the cost and performance axes, in order to create environmentally aware and benign technologies. This methodology also helps to identify potential performance and cost issues in novel technologies by taking a transparent and bottoms-up assessment approach.

This methodology is applied to the evaluation of the MIT 3D IC technology in comparison to a standard CMOS 2D IC approach. Both options are compared on all three axes – performance, cost and environmental impact. The "handle wafer" unit process in the existing 3D IC technology, which is a crucial process for back-to-face integration, is found to have a large environmental impact because of its use of thick metal sacrificial layers and high energy consumption. We explore three different handle wafer options, between-die channel, oxide release layer, and alternative low-temperature permanent bonding. The first two approaches use a chemical handle wafer release mechanism; while the third explores solid liquid inter-diffusion (SLID) bonding using copper-indium at 200°C. Preliminary results for copper-indium bonding indicate that a sub-micron thick multi-layer copper-indium stack, when bonded to a 300 nm thick copper film results in large voids in the bonding interface primarily due to rough as-deposited films. Finally, we conduct an overall assessment of these and other proposed handle wafer technologies. The overall assessment shows that but the oxide release layer approach appears promising; however, each process option has its strength and weaknesses, which need to be understood and pursued accordingly.

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Chapter 1: Introduction

This chapter emphasizes the importance of environment, safety and health (ESH) assessment for emerging silicon technologies. These emerging technologies are at a key stage in the development pipeline where they can still be modified or selected, and large environmental, performance or cost impacts on the fast-paced semiconductor industry can be avoided or minimized. In Section 1.2, we introduce the concept of three-way evaluation of several novel technologies on cost, performance and ESH impacts.

Our goal in this thesis is to develop this assessment methodology, and demonstrate its application on an important example, emerging three-dimensional integrated circuit (3D IC) technology. In Section 1.3, 3D IC process technology is introduced. Several integration and bonding methods used to fabricate 3D ICs are reviewed in Section 1.4, and other enabling technologies for 3D ICs are summarized in Section 1.5. In Section 1.6, we describe our thesis objectives and scope, and describe the organization of the rest of the thesis.

1.1 Motivation for ESH Assessment

According to the International Technology Roadmap to Semiconductors (ITRS) [1], the semiconductor industry must make significant strides in the performance of future technology nodes. Due to the increasing demand for greater device performance, scaling alone will not achieve the required performance levels, and therefore there is a need to introduce novel materials and process technologies. Figure 1 illustrates the extent to which novel materials currently are tested and used in the semiconductor industry,

compared to two decades ago [2]. The industry began using a limited number of elements including silicon, oxygen, aluminum, and a number of dopant elements; these were the workhorse elements in the 1980s. Figure 1.1 highlights the next set of elements, such as copper, titanium and tungsten, which were introduced in the 1990s, primarily to improve interconnect performance. More recently, the industry has begun using and evaluating a large number of additional elements in an effort to improve both transistors and interconnect. While Figure 1.1 simply illustrates the additional elements, if we take a look at the compounds used, we notice there has been further order of magnitude increase in both the organic and inorganic varieties of compounds, or combination of these elements that are being used or explored for future IC technology.

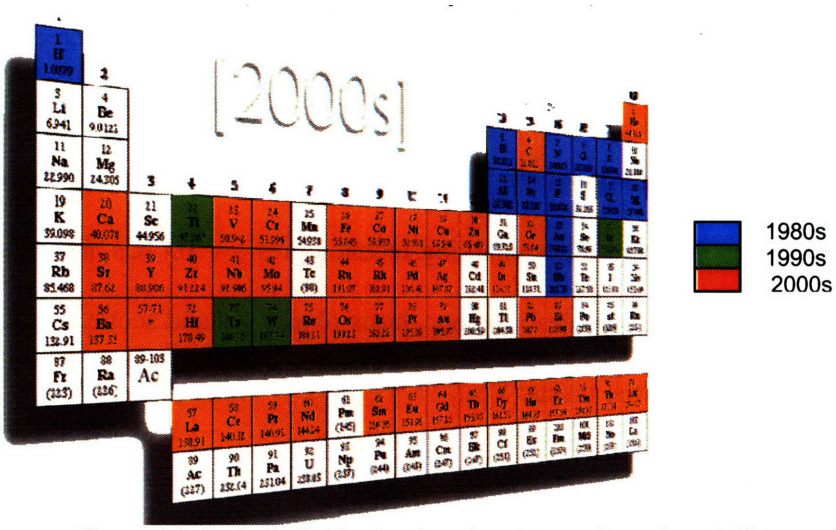


Figure 1.1: Periodic Table showing elements used per decade [2].

In addition to the increasing number of compounds, the manufacturing processes used to manipulate materials at smaller length scales have increasingly higher energy demands. The energy demands of nano-manufacturing processes, including energy used in the manipulation (addition or removal) of material at the nanometer scale, has been the subject of recent research [3]. Gutowski et al. [4] have examined the "specific

manufacturing energy", or the energy consumed per unit volume of addition or removal of material (MJ/mm^3), for a range of manufacturing processes operating at different lengths. They observed that the specific manufacturing energy increases dramatically at the nano-scale; a log-log inverse trend is observed between specific manufacturing energy and rate of material removal. Besides an increase in energy consumption, different emissions such as global warming gases (GWGs), volatile organic compounds (VOCs), and hazardous air pollutants (HAPs), pose another escalating problem. All emissions are directly proportional to the increasing number of layers in advanced ICs. In the coming years, as the industry continues to follow Moore's law [5] and produce increasingly complex and more highly integrated multilayer chips, these trends in energy and emissions will become a significant challenge.

The semiconductor industry is striving to counter the above mentioned environmental concerns. In order to make unit process more environmentally benign, the industry has proposed methods to reduce the emission of global warming gases from chamber cleaning [7] and dielectric etch [8], reduction in the use of photoresist [9],[130], approaches for copper removal from CMP waste [10], and other reduction, replacement or treatment options. Although there have been numerous success in reducing the environmental footprint of unit semiconductor processes, guidelines and methodologies for environmentally benign technology development are required. In particular, there is a need to consider environment, safety, and health (ESH) early on, in the research phase, to impact and assist the decision making process for future technologies.

1.2 Background and Introduction to ESH Assessment

Currently, there exist conventional models, which deal with performance metrics such as RC delay or power consumption, and the relationship of these metrics to new materials or novel processes. Cost models also exist to evaluate new materials and novel processes. The interplay between cost and performance determines the choice of a future technology path. This interplay is illustrated in Figure 1.2, which provides a conceptual plot of various technology options on performance and cost axes. Performance has multiple parameters, which can be either measured or modeled. Each of these performance metrics has an associated dollar-value depending on the revenue, which enables the evaluation of tradeoffs against the corresponding manufacturing cost.

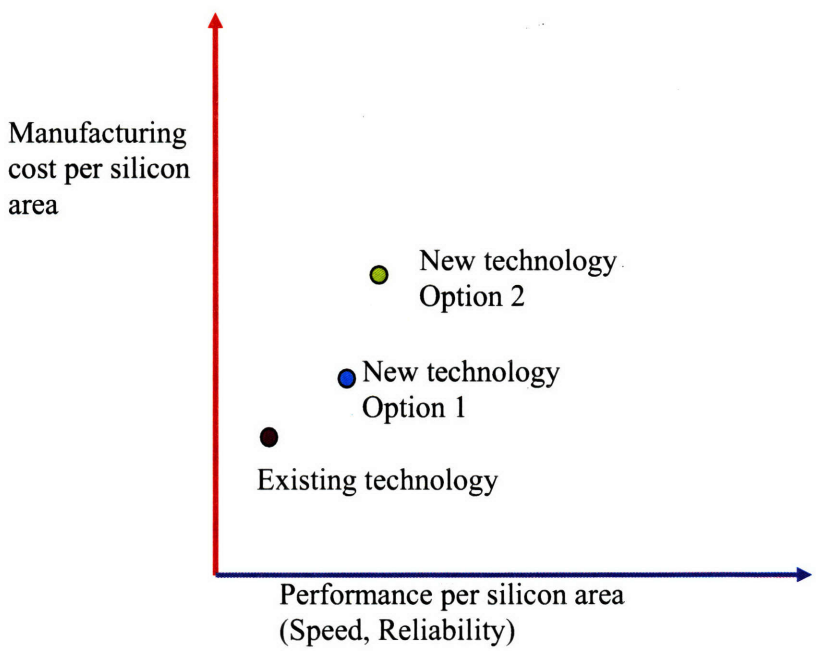


Figure 1.2: Trade-off between performance and manufacturing cost.

If ESH issues are not factored into the decision making process right from the start, significant time and financial investment loss may result. When the industry is

proactive, it can better deal with or avoid crises, such as the lead (Pb) banning scare in July 2006. In the 1990s, lead had become one of the most integral elements used in the electronics industry; in particular, lead was used as solder material along with tin (Sn) in virtually all packaging and printed circuit board (PCB) technologies. According to World Semiconductor Council (WSC) reports in 2001 [6], regulations introduced to ban lead affected an estimated 200,000 electronic products, as well as 200,000-plus sub-assemblies. Due to the widespread collaborative nature of the worldwide semiconductor industry, there are few alternative compounds presently available, which are environmentally preferable to lead, resulting in a significant cost in identifying and retrofitting alternative technologies. These kinds of regulations or sanctions on the use of specific materials can have a huge impact on the industry monetarily.

It is evident that future process technology development must involve an approach to assess the ESH impacts of new technologies early in the research and development cycle. We envision that future technologies should not be optimized solely on the cost-performance plane, but rather in the three-dimensions of cost, performance and ESH as shown in Figure 1.3. ESH is pictured as a third axis; it also has multiple variables as does the performance dimension. The key idea is that one should be able to quantify different environmental parameters for newer process technologies and existing technologies, at least comparatively if not absolutely. Health and safety issues are especially difficult to quantify, and much research is needed in this direction. As a first step toward ESH assessment of new technologies, in this research we will focus on environmental issues related to semiconductor processing. Like cost and performance, environmental issues can and should become an integral part of the technology

development and decision-making process. In Chapter 2, we will further elaborate on environmental impact evaluation studies conducted in the semiconductor manufacturing across both academia and industry, and present our proposed environmental assessment methodology in more detail. As motivation, however, we would like to further discuss some of the benefits of earlier consideration of ESH issues in the semiconductor technology development.

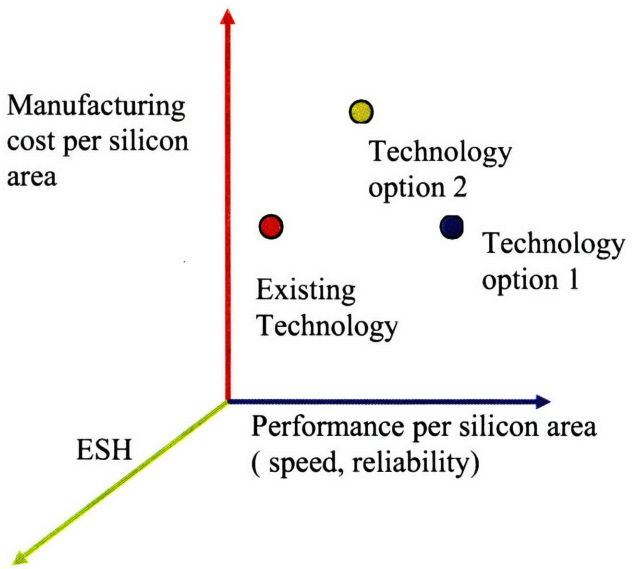


Figure 1.3: Three axes to manufacturing: Cost, performance, and ESH performance.

An early focus on ESH issues can provide the semiconductor industry with significant advantages, besides contributing to the environment in a positive way. It can prepare companies for future regulations and sanctions, and protect the industry from law-suits. Nowadays, "green" marketing is one of the best ways to advertise, and specifically in developed nations, it has enormous value. Another significant near-term benefit is that environmentally benign manufacturing includes the principle of

optimization and minimization of resources, which is a win-win solution for the industry as it decreases the cost of production, along with creating better ESH conditions.

It is essential to relate the third axis – environmental impacts - back to the dollar cost and value, as that will make the case stronger for the mapping and trade-off of future technologies on all three dimensions, rather than on cost and performance alone (both of which are very well correlated with dollar amount). Thus, it is important to build a total cost-of-ownership (CoO) model in order to understand the complete impact of environmentally benign manufacturing technologies. Such a model is difficult to make, because usually the environmental cost is shared by the community and it is challenging to relate costs back to individual manufacturer's viewpoint. Nevertheless, the industry has made some progress toward such a model.

In 1996, Sematech initiated the project entitled, "Design for Environment, Safety and Health (DFESH)" [11]. The environmental concerns and CoO were integrated with existing input-output models of the semiconductor wafer fabrication processes, in order to help engineers make better decisions early in the design phase. Lashbrook et al. [12] applied the ESH cost model and CARRI ™ on three different lithography processes to illustrate the evaluation process between different unit process technologies. Krishnan et al. [13] quantified the environmental footprint of various exhaust systems used after the CVD process, using the EnV-S method. All of the current CoO models are unit process focused and subjective. Further research is needed to make the CoO model more objective and quantitative, which will help in providing cleaner assessment.

It is a common belief that environmental evaluation will slow down the growth of fast-paced semiconductor industry. To avoid this, we propose to conduct an

environmental evaluation of novel technologies, which have already passed the first phase of fundamental research and are just entering into the second phase of integration (Figure 1.4). However, postponing environmental assessment further than this is no longer appropriate. After integration studies are conducted and technology is proven to enhance the performance and cost, it becomes very difficult for the highly competitive semiconductor industry to change their product and process. Thus, the critical point for environmental evaluation is during the early development and integration of new and novel technologies, as highlighted in Figure 1.4.

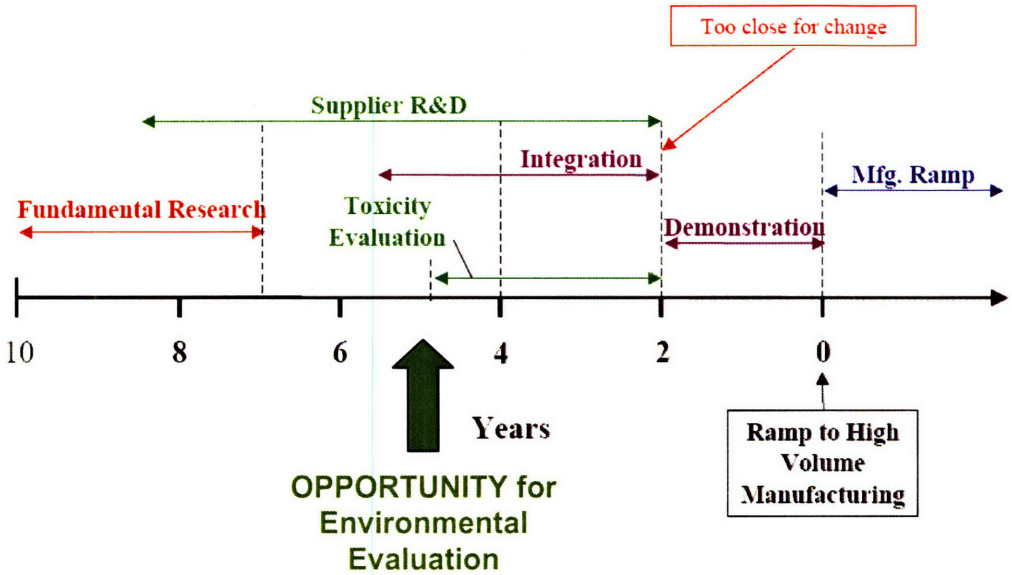


Figure 1.4: Technology development path indicating time where environment evaluation can be conducted (Timeline from [14]; opportunity notation added).

In this thesis, we introduce a methodology which will help in environmental impact evaluation of future technologies. This methodology will assist in plotting the technology on all three axes of performance, cost and environmental impact, as shown in Figure 1.3, which will help us make informed decisions about different technologies. To illustrate and demonstrate this methodology, we select a future silicon based technology

which is still in the research phase, and consider multiple options at the process and design-level. Three dimensional integrated circuits (3D ICs) is one such technology option the semiconductor industry is currently exploring. Goals of this option include solution to the interconnect delay problem, enablement of heterogeneous integration, and reduction of the packaged form-factor to sustain growth according to Moore's law [5]. In this current work, we examine possible 3D IC design options, including the MIT back-to-face wafer level bonding approach. In the next section, we discuss the background and motivation for 3D IC technology.

1.3 Background and Motivation for 3D IC

For the past four decades, higher computing power was achieved through rigorous scaling of device dimensions. Throughout this period, integrated circuits (ICs) essentially remained single device layer structures. As performance enhancement through device scaling is becoming more challenging and the demand for higher functionality increases, there is tremendous potential to explore the third spatial dimension, i.e., the vertical dimension of integrated circuits in addition to exploring newer materials.

With feature size scaling, there has been consistent improvement in device performance in terms of gate switching delay, but with an adverse effect on global interconnect latency [15]. The global interconnect RC delay has increasingly become a circuit performance limiting factor, especially in the deep sub-micron regime. Even though Cu/low-κ material systems have been introduced to improve interconnect RC delay, these are not long-term solutions. When chip size continues to increase to accommodate more functionality, the total interconnect length increases at the same time. In addition to latency impact, this also causes a tremendous amount of power dissipation

in the interconnects. Implementation of system-on-a-chip (SoC) technology using the planar IC process will result in larger chip size, longer interconnects, and longer manufacturing time as each functional block is fabricated sequentially using separate sets of technology.

Recently, there has been research interest in advanced three-dimensional integrated circuits (3D ICs) in the form of a stack of interconnected active layers, which have many performance, integration and cost advantages [16]. Three-dimensional ICs can be defined as a stack of several device layers (with interconnects) that are electrically interconnected by vertical interlayer vias. Figure 1.5 schematically shows the concept of multi-layer 3D ICs. In principal, one can stack as many device layers as the technology and the economics allow. In the following, advantages offered by 3D integration will be discussed and potential applications will be highlighted. In Section 1.4, we will review more in detail a particular scheme of integration for 3D ICs, focusing on wafer bonding technology.

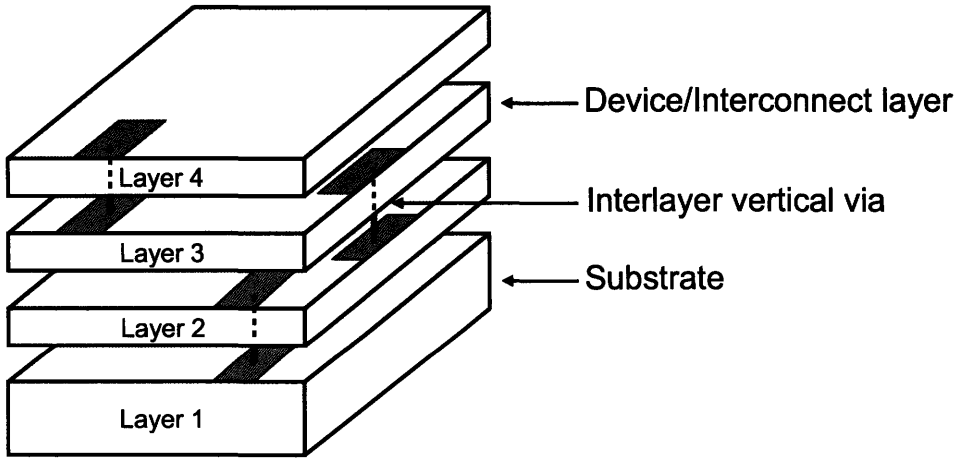


Figure 1.5: A conceptual multi-layer three-dimensional integrated circuit.

Interconnect Bottleneck

Today, as the device dimensions continue to shrink and the chip area continues to increase, the circuit performance has shifted from device dominated to interconnect dominated. As a result of scaling, global interconnects become slower due to increased resistance and capacitance. Total interconnect length also increases as the complexity of the chip increases, which results in higher interconnect latency and power consumption.

One solution to the interconnect problem is to partition a large chip into smaller blocks, followed by thinning, stacking, and interconnecting them with vertical vias on a common substrate, as shown in Figure 1.5. Instead of traveling across the entire chip, inter-block communication is now shunted through vertical vias which are much shorter. With a 3D implementation, one ends up with shorter global and semi-global interconnects (for clock, power, and signal connections). To seek a long-term solution to the interconnect bottleneck, the ITRS has identified 3D interconnects as one of the promising options [1]. Some of the benefits of 3D IC technology are discussed below.

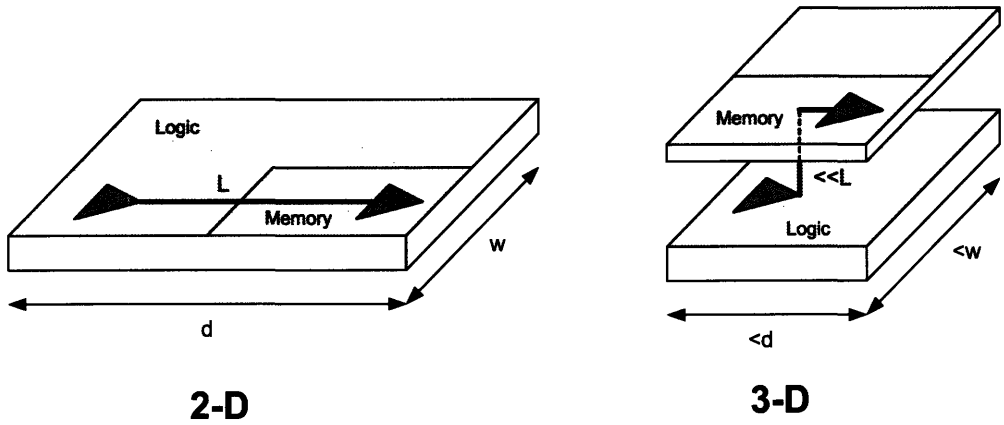


Figure 1.6: 3D integration can replace long global and semi-global wires with shorter vertical interconnects.

Chip Form Factor

By stacking a few device layers in a vertical fashion, more compact integrated circuits can be realized. Packing density, in terms of number of devices or functionalities per unit area will increase, and this reduced chip form factor might have cost advantages in applications where area is a primary consideration.

Enable Heterogeneous Integration

System-on-a-chip (SoC) is a potential solution to the mounting demand for multiple functionalities on a single chip. There are several challenges associated with planar implementation of SoC on a single substrate. Each functional block has to be built on the same technology base, and it is challenging to optimize and to integrate each functional block on the same substrate. In addition, performance may be limited if constrained to a single substrate. For example, substrate coupling might cause signal corruption between functional blocks [17]. 3D integration is an attractive choice for SoC implementation, as it allows integration of the various functional blocks in a vertical fashion. In this way, each block can be optimized independently, fabricated using optimal process technology for that functionality and then stacked to form a 3D system. Since there is no shared substrate in this type of implementation, noise between blocks is expected to improve compared to a planar implementation.

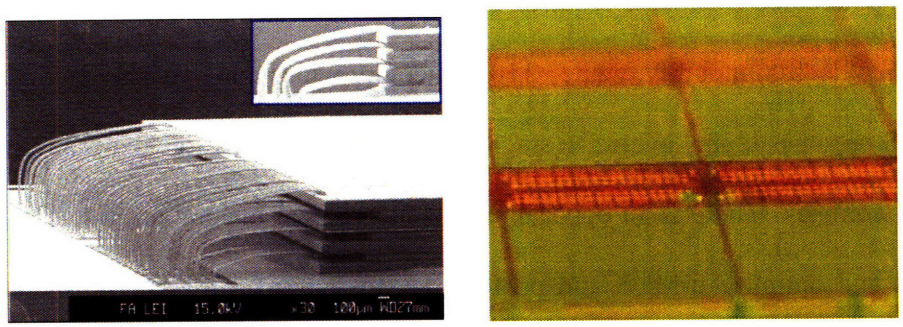
Enable Hybrid CMOS

Another attractive possibility enabled by stacking active device layers in a vertical fashion is the implementation of hybrid CMOS. While the n-MOSFETs and p-MOSFETs in CMOS inverters have remained largely identical in terms of materials selection in the past, MOSFET technology in state-of-the-art CMOS inverters have increasingly diverged. For example, a tensile strained channel is required for n-MOS, while a

compressive strained channel is required for p-MOS [18]. In addition, <100> orientation has a higher electron mobility, while <110> silicon provides a higher hole mobility [19]. As CMOS becomes more "hybrid" a single substrate implementation and processing can be highly complex. There is an opportunity for 3D vertical integration in this area: one can build and optimize n-MOS and p-MOS devices on two different substrates, with individually optimized materials and processes, then bond and thin back to form stacked CMOS.

1.4 3D IC Fabrication Approach

Three-dimensional integrated circuits can be achieved in several ways. 3D ICs can be attained at various levels such as die-to-die, die-on-wafer and wafer-to-wafer bonding. Die-to-die integration is already in existence, and various companies including Intel already stack multiple chips to attain a compact form factor. Figure 1.7 (a) illustrates an example of four DRAM dies stacked by a packaging company, *STATS ChipPAC* [39]. The dies are connected to each other using flip chip bumps, and thus the interconnection density is low. Another way to achieve 3D integration is bonding die-on-wafer. This method is becoming more popular in the industry because of its use of known good dies (KGD), where good dies can be selected and bonded to another wafer, reducing potential yield loss. Die-on-wafer approaches can be very useful in bonding dissimilar dies which are different in size and shape, avoiding the need to match chip size, as in wafer-to-wafer bonding. Figure 1.7 (b) illustrates 10 μm thin dies bonded to a wafer using Cu-Sn bonding at IZM Fraunhofer [38]. Die-level bonding and integration suffer, however, from low throughput and interconnect density limitations. For this reason, wafer-level integration is of particular interest as a 3D IC option.



a b

Figure 1.7: a) Four DRAM die stack with two spacers [39]. b) Chip-to-wafer stacks - 10 μm thin chip bonded to 200 mm wafer [38].

In general, there are two primary fabrication schemes for wafer scale integration of integrated circuits. To form a stack of active device layers, one can either build a 3D IC sequentially, using a "bottom-up" approach, or do it in parallel, and assemble the finished device layer using an "assembly" method. Both approaches are described below and examples are given based on reports in the literature. Comments on each technology will be given where appropriate.

1.4.1 Bottom-Up Approach or Epitaxy

In the bottom-up approach, devices in each active layer are processed sequentially starting from the bottom-most layer. Devices are first built on a substrate wafer by mainstream process technology. After proper isolation, a second device layer is formed in which devices are processed by an alternative technology in the second layer. This sequence of isolation, layer formation, and device processing can be repeated to build a multi-layer structure. This bottom-up approach has the advantage that precision alignment between layers can be accomplished. However, it suffers from a number of drawbacks, due to the need to grow the upper level devices using different technology than that used in the substrate wafer. The deposition of upper device layers can be achieved by laser beam crystallization [21], seeding [22], or selective epitaxial growth

[23]. However, the crystallinity of deposited upper semiconductor material layers is usually low and imperfect. As a result, high performance devices cannot be built in the upper layers. Thermal cycling during upper layer crystallization and device processing can degrade underlying devices, and therefore a tight thermal budget must be imposed. Also, due to the sequential nature of this method, manufacturing throughput can be low. Despite all these challenges, a 3D stacked memory cell has come into production recently [20].

1.4.2 Assembly Approach or Wafer Bonding

While the recrystallization technique finds specific applications in memory devices, it is not suitable for applications where high performance devices are required. This has opened up the opportunity for an "assembly" method. This method allows one to fabricate individual 2D circuits using conventional high performance planar fabrication technology. These 2D circuits can then be tested and assembled to form 3D circuits. While it is possible to stack high performance devices, new challenges exist for this method. Precision alignment between layers can impose a limit on the density of vertical interconnects. Low temperature layer transfer techniques are also needed, though recent progress in low temperature wafer bonding has been encouraging [24]. Since device layers can be fabricated in parallel, and optimized using their respective technologies prior to layer stacking, higher throughput can be expected. This is an attractive approach to realize true heterogeneous integration of materials and functionalities.

In wafer-level bonding, thin device layers can be added to a substrate to form a vertical stack of device layers in two different orientations, i.e., "face down" or "face up" integration of device layers. The face down orientation adds the device layer face-to-face

with the substrate wafer. In this method, a donor wafer is permanently bonded to a substrate and thinned back to the desired thickness. On the other hand, the face-up orientation adds device layers back-to-face with the substrate wafer. In this method, a donor wafer first must be temporarily bonded to a handle wafer, thinned back to the desired thickness, and then permanently bonded to the substrate wafer. The transfer is completed by removing the handle wafer. A permanent bond between active layers can be formed either by insulating or conducting materials. Examples for each of these bonding mediums are reviewed below. Another categorization of 3D IC integration approaches can be identified, based on making electrical contacts between layers either before permanent bonding or after permanent bonding, denoted as via first or via last approaches, respectively. The choice of the formation of contacts before or after bonding is dominated by alignment issues.

Dielectric Bond

When the bonding medium between active layers is insulating, a "via last" sequence is followed. Device layers are first bonded and vertical vias are etched through the bonding interface. Therefore, high aspect ratio vertical vias are needed. Examples of such bonding media include polyimide adhesive, polymeric adhesive, and silicon oxide.

Ramm et al. [25] pioneered what is termed a "vertically integrated circuit (VIC)" by stacking thinned processed device wafers using an aligned bonding process with polyimide adhesive and vertical interconnects. Lu et al. [26] used a face down approach, hence avoiding the use of a handle wafer. Wafers were bonded using polymeric glues such as benzocyclobutene (BCB). Warner et al. [27] demonstrated two-layer SOI CMOS circuits with operational ring oscillators using low-temperature oxide bonding. Guarini et

al. [28] designed a back-to-face donor layer transfer to substrate wafer using oxide fusion bonding. A glass handle wafer was used to assist in wafer alignment, and bonding between donor wafer and glass handle was done using polymeric glue. It was shown that the intrinsic electrical characteristics of the thinned layer were preserved.

Metallic Bond

Device layers can also be bonded with a conductive metallic layer. This is an attractive choice because it allows a "via first" approach for fabricating 3D ICs. When metal is used as a bonding medium, vias can be formed in both pairing device layers prior to bonding, hence the requirement for a very large interlayer via aspect ratio can be relaxed. Vias are electrically connected by bonding landing pads at the end of the vias. Dummy pads are also bonded to provide mechanical strength to the stack. Since metal is a conductive medium, bonding of a continuous surface film would not allow for patterned features; bonding of segmented or patterned metal must be accomplished and proper dielectric filling between metal pads is needed for a reliable bond. Thermo-compression bonding of metals such as Cu [29] and Au [30] has been demonstrated.

Using a similar flow described in [31], Ramm et al. replaced the bond between active layers with a metallic bond formed by solid liquid interdiffusion of Cu and tin (Sn). Cu pads were formed on both top and bottom wafers and Sn was deposited on the top Cu pads. Under a pressure of 5 bar and temperature of 260-300°C, Sn starts to melt and intermixing of Sn and Cu will take place. A stable eutectic alloy, Cu_3Sn, forms between the remaining Cu layers. This is an attractive choice because the alloy is stable up to 600 ^{o}C, hence providing a temperature window to stack additional layers on the stack using a similar technique.

Tan et al. [32] stacked ultra-thin silicon layers in a face-to-face fashion having Cu as the bonding medium. Fabrication of a double-layer stack was demonstrated, and by repeating the stacking with two double-layer stacks, a four-layer stack was successfully built.

Table 1 summarizes the various approaches explored in industry or academia. The table presents different characteristics of each process including their bonding scheme (die-to die, die-on-wafer or wafer-to-wafer), bonding material, via density, design, and material. It also notes whether a handle wafer is required in the process, and if so, then what kind of material is used to make the sacrificial bond.

	Bonding scheme	Bonding material	SOI or bulk	HW/ material?	Via depth (μm)	Via array/ peripheral	Via etch process	Supervia metal	Electrical results
RPI	W2W	BCB	SOI	No	2 X (7 to 8)	Array	oxide-BCB etch	Cu	unknown
MIT	W2W	Cu	SOI	Yes/ Al or oxide	2	Array	Oxide	Cu	Yes
Fraunhoffer	D2W	Cu-Sn	Bulk	Yes/ polyimide BCB to porous Si	10 to 30	Array	Si etch	W or Cu	Yes
Infineon	D2W	Cu-Sn		No	unknown	unknown	unknown	unknown	Yes
ASET Japan and Zycube	D2D	Cu-Sn	Bulk	Yes/unknown	50	peripheral	Si etch	Cu	unknown
Toshiba	W2W	Bumps	Bulk	unknown	50 to 70	peripheral	Si etch	Cu	unknown
Tokohou Univ	W2W	In/Au bumps		Yes/unknown	50 to 55		Si etch	poly Si-W	unknown
Intel	W2W	Cu	SOI	Yes/unknown	?	Array	Oxide	Cu	Yes
IBM	W2W	Oxide	SOI	Yes/ magical polymer	7 to 8	Array	Oxide	Cu	Yes
MIT-LL	W2W	Oxide	SOI	No	2 X (7 to 8)	Array	Oxide-IMD etch	Cu	Yes
Ziptronix	D2W	Cu/ unknown		No	unkown	Array		Cu	unknown
Tezzaron	W2W	Cu		No	6	Array	IMD-Si etch	Cu	Yes
MCNC-RDI	D2W/ D2D	Polymer or bumps	Bulk	No	unknown	Array	unknown	Cu	unknown

Table 1-1: Summary of 3D IC process approaches [141].

This table has been compiled based on information in the literature [141] and is by no means complete. The table is meant to provide a sampling of the different schemes and materials that have been explored for 3D ICs.

1.5 Enabling Technologies for 3D IC

In this section, we focus more narrowly on the challenges presently faced by the semiconductor industry in order to make 3D ICs at the wafer-level. These challenges are the basis for ongoing research into 3D ICs. In this thesis, we will explore handle-wafer and bonding technologies that both address these performance and manufacturing issues, and which have benefits from an environmental impact perspective.

Wafer Bonding

In the previous section, we have described several bonding methods using both dielectric and metal bonding interfaces. There are several promising ways in which bonding can be achieved, but one still needs to make the bonding process more reliable and repeatable. A further need is to decrease the bonding temperature to provide a larger process window with minimum thermal stress. In addition, high throughput bonding is desired, and can be enhanced with lower temperature bonding. In this thesis, we will investigate indium based low-temperature bonding conducted at 200°C, as discussed in Chapter 6.

Alignment

Alignment can be the key which determines the viability of a 3D IC technology because it determines the pitch and inter-wafer via density. Suss MicroTec [40] and Electronic Vision Group [41] are the two major companies developing equipment for 3D IC alignment. With regards to wafer-to-wafer stacking, both companies promise to

provide sub-micron alignment technology, but another concern is the time consumed to achieve the desired alignment. For chip-to-wafer stacking, KGD need to be placed on the substrate wafer and then bonded. In this case, the speed in which chips can be placed precisely and in alignment is important. In general, the ability to align, and the corresponding manufacturing cost, will be an important constraint as we explore alternative bonding technologies later in this thesis.

Through Silicon Via (TSV)

When 3D ICs have more than two layers, one needs through wafer vias, which can conduct signals from one device layer to another device layer. This can be one of the most challenging aspects of 3D IC technology development, as it requires composite etch across a thinned silicon wafer. After etch, through silicon vias need to be filled by a conductive metal, like Cu or W. In this case, the thickness of the thinned wafer will determine the size of the via, as there is a limit on the aspect ratio (depth-to-width) one can etch and fill with conductive metal successfully. Thus, the thickness of the active device layer is an important parameter in the development and assessment of the alternative bonding (and temporary bonding) approaches. In Chapter 5, we explore the constraints on layer thickness in a novel oxide channel bonding approach.

Handle Wafer (Layer Transfer Technology)

Handle wafer or layer transfer technology is an important aspect of the back-to-face integration. The handle wafer process involves making a temporary bond, then thinning and transferring the thinned layer from the support wafer to another device wafer using a permanent bond. Later in this thesis, we will focus on this technology and describe it in more detail, as we will see that this as a critical step from an environmental, as well as performance and cost, perspective.

Packaging

Last but not least, in order to make 3D ICs feasible, packaging for a bonded stack needs to be determined. In the case of existing stacked die technology, die are wire bonded using an interposer between each layer as shown in Figure 1.7 (a). To gain the maximum benefit of 3D IC technology, one needs to identify what is the best packaging method. While packaging is important from performance, cost, and environmental perspectives, in this thesis we limit our scope to the 3D integration technology. Future work should consider the interplay of 3D IC processes and packaging technology from all three perspectives.

1.6 Thesis Objectives and Scope

The primary objective of this thesis is to develop a comparative methodology and framework to evaluate the environmental impact of emerging silicon technologies. This methodology helps to identify unit processes which are not environmentally benign and to ascertain if they have any other issues or concerns regarding cost and performance. This methodology will be demonstrated by comparing existing planar (2D) single device layer technology, to multiple layer technology using a 3D IC approach. Handle wafer or layer transfer technology is identified as the key process to be improved upon from both performance and environmental viewpoints. Our goal is to further develop and compare different handle wafer process options to existing handle wafer processes. We also investigate low-temperature copper indium bonding as permanent bonding option which could change the constraints for handle wafer and dramatically increase the performance, cost and environmental tradeoffs in future 3D IC technology.

In Chapter 2, we introduce the comparative environmental assessment methodology. We apply it to the analysis of existing planar technology against 3D IC technology, using the previously developed MIT 3D IC process flow. An outcome of this analysis is identification of the handle wafer process as needing improvement, from both environmental as well as performance perspectives. In this chapter, we also conduct an overall comparison of 3D and 2D technologies by on performance, cost and environmental impact axes. In the subsequent four chapters, alternative handle wafer and bonding technologies are explored and further developed.

In Chapter 3, the goals and requirements of the handle wafer process are discussed. These requirements are the basis of new approaches explored in this thesis, detailed in Chapter 4 through 6.

In Chapter 4, the first novel approach for the handle wafer process is discussed. A between-die channel approach, inspired by a singulation technique called dicing-before-grinding (DBG), is proposed. The main idea behind this approach is to increase the access of release or etching fluids to the sacrificial bond interface materials by creating channels. We explore this approach using Al as a release layer, but other release layers can be used.

In Chapter 5, we discuss a second novel approach for the handle wafer process using low-temperature oxide bonding as a temporary bond. We propose to undercut oxide using an HF based chemistry in order to release the wafer. To evaluate the performance of this approach, the effects of patterning on the interface toughness of oxide fusion bonds are measured using a chevron structure.

In Chapter 6, we investigate copper-indium bonding using various characterization techniques, including scanning electron microscope (SEM), and scanning tunneling electron microscopy (STEM). Multilayer stacks of copper and indium are investigated to understand more about the low-temperature bonding. While this technology remains of substantial interest as a way to achieve low-temperature bonding, further research is needed to overcome void formation issues.

With further development and exploration of 3D IC handle wafer and bonding approaches, as described in Chapters 4 through 6, we make comparisons and assess different handle wafer options on all three of the performance, cost and environmental axes in Chapter 7.

In Chapter 8, we summarize the contributions of this thesis and present suggestions for future research.

Chapter 2: Methodology for Environmental Impact Evaluation

In this chapter, we first briefly review , different environment evaluation methods used in the semiconductor industry, starting from life cycle analysis (LCA), moving to new methods including life cycle inventory (LCI) (Section 2.1). A comparative methodology is proposed in Section 2.2, for environmental impact evaluation of emerging silicon-based technologies. This methodology enables identification of unit processes that do not perform or have environmental issues in the novel technology. The key steps in the proposed comparative methodology are presented in detail, emphasizing the importance of creating and updating an inventory database for all semiconductor manufacturing unit processes. Section 2.3 further details the approach of evaluating new elements, inspired by Klee and Graedel [49], which are being pursued by the industry. In Section 2.4, the proposed framework is applied to the comparison of existing planar technologies (single device layer) and MIT's 3D IC technology, to generate its environmental footprint of each technology. An outcome of this analysis is the identification of the handle wafer process as a key step needing further development to reduce environmental impact. This motivates the technology development that follows in Chapter 4 through 6, after which comparison of handle wafer options can be made in Chapter 7, on all three axes of performance, cost and environmental issues. In Section 2.5, several previous works have been outlined to conduct performance and cost comparison of 3D IC to 2D IC.

2.1 Background for Environmental Impact Evaluation

In this section, we describe two different existing environmental impact evaluation methods and summarize various attempts to apply these methods in the semiconductor industry. We consider strength and weaknesses of these existing approaches.

2.1.1 Life Cycle Analysis

Environmental impact evaluation can be quite tedious and challenging, because a product can impact the environment in different stages of its life cycle and in numerous ways. Impact analysis is also challenging because of its interdisciplinary nature. The traditional approach is to do a complete a life cycle analysis (LCA), an integrated "cradle to grave" approach, to assess the environmental performance of a product. An LCA is divided into various stages including materials extraction (upstream), product manufacturing, product use/reuse, repair and maintenance, and finally disposal. However, LCAs are product specific and often are not completed until the product is already in the market due to the time required to complete an LCA. LCAs have been performed for a limited number of electronic products, like desktop computers [42] and mobile phones [43], which are standardized functional units being used by typical end consumers. These electronic products are made up of highly specialized assemblies of components including microprocessors and DRAMs, but the LCA loses that specificity because of its very broad and comprehensive nature. As a result, LCAs are not transparent and lack chemical specificity, particularly to guide decision making in process technology development. Although LCA is an excellent tool for comparative study of products and

technologies, it does not provide guidelines about improving further technology generation.

2.1.2 Recent Efforts

A more focused approach has been proposed by the industry to counter problems with LCA. Life cycle inventory (LCI) is an accounting of the energy, materials, by-products and waste associated with the creation of new products. Unlike LCA's top-down and all-encompassing approach, LCI can be a bottom up approach scoped to particular processes or product components of interest. It also can be used to quickly evaluate processes with more chemical and material specificity. This inventory approach can be applied to either an integrated process flow or to individual unit processes, making it widely applicable. An extensive materials and energy inventory for a 32 MB DRAM was conducted by Williams et al. [44], which shows that fabrication and packaging are by far the most energy and materials expensive stages in IC products and processes. Murphy et al. [46] developed parametric models for environmental impacts to provide the flexibility needed for predictive LCI for a range of fabrication process steps. Various researchers are developing the IZM-toolbox [47],[50], which seeks to integrate the environmental assessment with product design, along with creating an energy and materials inventory for different semiconductor processes. This is a notable effort, as this tool-set does a quantitative rather than qualitative estimation, unlike previous methods. The toolbox has various indicators, such as those for toxicity, energy and recycling at different life phases. Still, as in other LCI methods, although the toolbox is helpful when conducting a comparative analysis, it does not provide guidelines or design rules to improve upon future technology.

Taiariol et al. [52] also report a within-fab (gate-to-gate) semiconductor manufacturing inventory. In another vital study, Yao et al. [48] compared the manufacturing and consumer use of two generations of semiconductors. This investigation identified several major environmental impacts, including perfluorocompounds (PFCs), volatile organic compounds (VOCs) and hazardous air pollutants (HAPs) emissions, as well as water and energy consumption in semiconductor manufacturing. Unfortunately, this study lacks chemical specificity. For example, the toxicity of the VOC benzene is different from other VOCs such as methyl ethyl ketone; the Yao study does not consider these distinctions.

As a part of this thesis research, we have conducted a full-scale, transparent LCI of a CMOS chip [54]. This LCI will be discussed in more detail in Section 2.4.2. Our effort, in collaboration with UCB and Applied Materials, contributes gate-to-gate input and output models for the fabrication of a semiconductor logic device (CMOS processor, 6-layer Cu metallization, 130 nm node, 300 mm wafer) using detailed, bottom-up process data to form inventories of energy and material demands and individually speciated emissions. The impact assessment methodology proposed in the next section strongly depends on the availability of such an LCI database, as most semiconductor process technologies consist of multiple instances of approximately forty different kinds of unit processes.

2.2 Proposed Methodology

In this effort, we pursue a comparative methodology to evaluate the environmental impact of emerging silicon based technologies. One should be able to locate novel options, as well as existing technology options, in a space spanned by cost,

performance and ESH as previously depicted in Figure 1.3. Our methodology primarily focuses on environmental concerns along the third axis, rather than the generalized concerns of environment, safety and health (ESH). For this current approach, wafer fabrication unit operations and packaging are defined as the system boundary, as depicted by dashed line in Figure 2.1. Eventually, material flows from start to finish, e.g. from mining to post disposal environment cycling, could be considered, once LCI databases are available with this scope. This methodology uses a bottom-up approach for estimating environmental impact, based on aggregation of all unit processes.

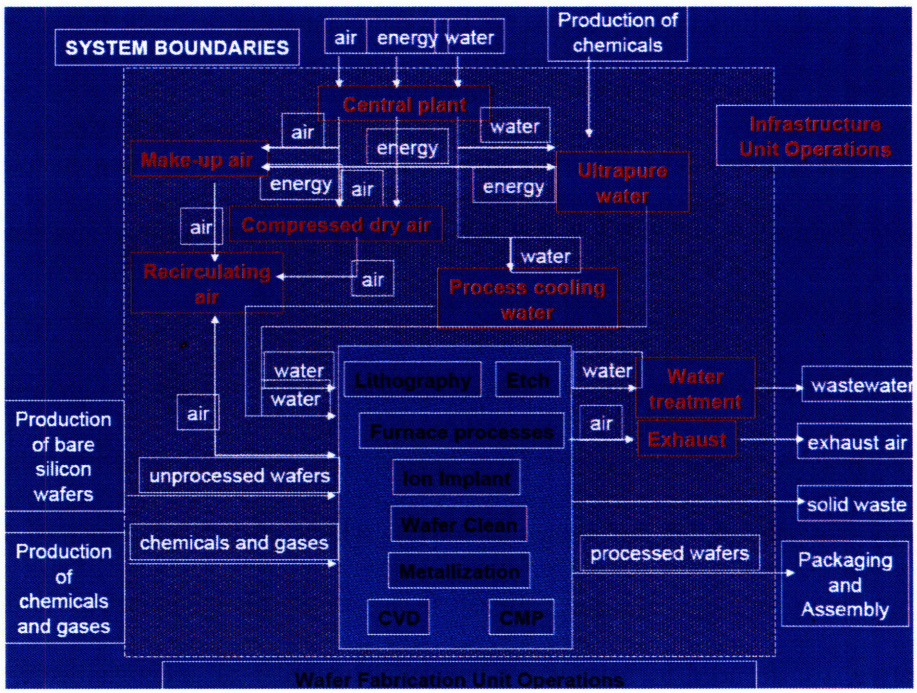


Figure 2.1: Illustrating system boundaries [45].

A novel process technology must be considered as a whole, rather than simply evaluating alternative options for a single specific unit operation. Because individual unit process alternatives typically have an effect on multiple upstream or downstream unit steps in manufacturing, it is important to compare the total environmental, performance, and cost impact of the integrated technology. Once the aggregate assessment has been

performed and problematic unit steps identified, then we focus on the critical alternative unit process steps, which also have significant impact from an environmental perspective. A set of more detailed and refined environmental assessment techniques can then be applied to these critical unit steps, appropriate for use while these new emerging unit processes are still in the research phase. The six steps in the proposed methodology can be summarized as follows:

1. Identify novel process technologies that need to be evaluated. The selected process technology should still be in a research phase and not yet fully developed; however, the technology also should be not be too premature or far in the future, as it will become hard to obtain the requisite data and information about the various processes involved. Most appropriate is the technology, which is 3-5 years from implementation or at the point industry is already contemplating different process options, and evaluating performance, yield and cost issues (Figure 1.4).

2. Identify the state-of-the-art technology that will be replaced or augmented by the novel process technology under investigation. For example, current 65 nm node technology is replacing 90 nm node technology, which in turn had replaced 130 nm technology two years ago. The most important aspect of this methodology is that it is comparative, so we need to have a good baseline in order to understand the relative change of a new technology option. To fulfill this requirement, we need to generate or have available the environmental footprint for a standard manufacturing technology.

3. Define functional unit for comparison. In any comparative analysis, one needs to define how one technology or process can be fairly compared to another. For example, to compare a system-on-a-chip (SoC) to a standard CMOS technology, great care must be

taken because the SoC might provide more functionality compared to any individual CMOS chip. One needs to define the functional unit, e.g. an integrated memory/process function, in order to provide the basis for comparison between two distinct integration approaches.

4. Design the prototypical flow for the functional unit with all the process technologies under investigation. For this particular step, one needs to investigate the relevant literature to understand differences between various alternative process technologies and their respective limitations and advantages. Further, one needs to identify the new or additional unit processes that make the novel process technology different from the standard process. For example, in the case of strained silicon technology using Si-Ge on insulator, when compared to standard SOI technology, the additional and new process is epitaxial deposition of Si-Ge thin films in the fabrication of substrates.

5. Assess the environmental impact of the alternative technologies, compared to the standard IC technology, for the functional unit identified above. Energy, water and chemical data for standard unit processes can be generated using input-output models. For processes which are not novel and have no standard input-output model, quantities must be estimated using approximations. Research data must be scaled to describe full-scale manufacturing. At the outset, inventory of different process technologies under investigation are compared to the standard or state-of-the-art technology (step 2), in order to see if there are any "red flags" in the novel technology in terms of energy, water, or chemical usage. The critical unit processes are identified, which are challenging from the

environmental, performance and cost standpoints. In this methodology, we maintain chemical specificity as much as possible.

6. Design alternative approaches for these critical unit processes and compare these alternatives on all three axes of cost, performance and environment. The performance will act as a screening option for alternative approaches; and once an option satisfies some criterion for performance, the option can be evaluated on the environment axis.

The idea behind the methodology is to create environmentally conscious technologies and, at the same time, to avoid sacrificing performance or increasing cost. Thus, evaluating the options early in a research phase is preferred. Along with an environmental impact evaluation, technologies should be evaluated on cost and performance metrics to complete this methodology.

2.3 Evaluating Materials/Chemicals

In addition to concerns arising from energy and water usage, specific materials or reagent chemical choices may give rise to environmental concerns. Williams et al. [44] conducted an inventory of the twenty most used chemicals in the semiconductor industry. Process data for specialty chemicals and materials is difficult to collect due to competitive and confidential forces, but such data is critically important. Middendrof et al. [50] at IZM present a modular assessment system for the environmental impact evaluation of electronics. The different modules are based on product and process specific data. In the product based module, the toxicity and recycling potential are assigned to the materials present in the product; in the process specific module, the process toxicity screening and emission potential is assigned to the materials used. This

method is quite dependent on toxicity data, but such availability is limited in a rapidly evolving industry.

At the research stage, one needs to have a quick screening system, with the ability to advance in tandem with technological development. Here, we briefly describe an approach for screening elements. If a material's industrial usage is greater than its corresponding natural fluxes on either local or global scales, problems may arise, especially when the chemical compositions of the air we breathe, the water we drink, and the media sustaining the growth of the food we eat substantially changes. Past soil, water or air compositional changes, e.g., Pb or Hg, arising from human usage of metals have already been deemed hazardous, and we can avoid a repeat of such mistakes if we choose, utilize, and dispose of such materials in our products and processes wisely. Klee and Graedel [49] have published a seminal work summarizing the geochemical cycle information for 77 elements (leaving out noble gases and short-lived radio active elements). They compared the anthropogenic and natural fluxes to identify elements which, potentially, might be of concern in the near future (Figure 2.2). While human-generated changes in natural fluxes are not necessarily harmful, the potential for such changes can serve as an early warning indicator highlighting that special attention and care may be needed.

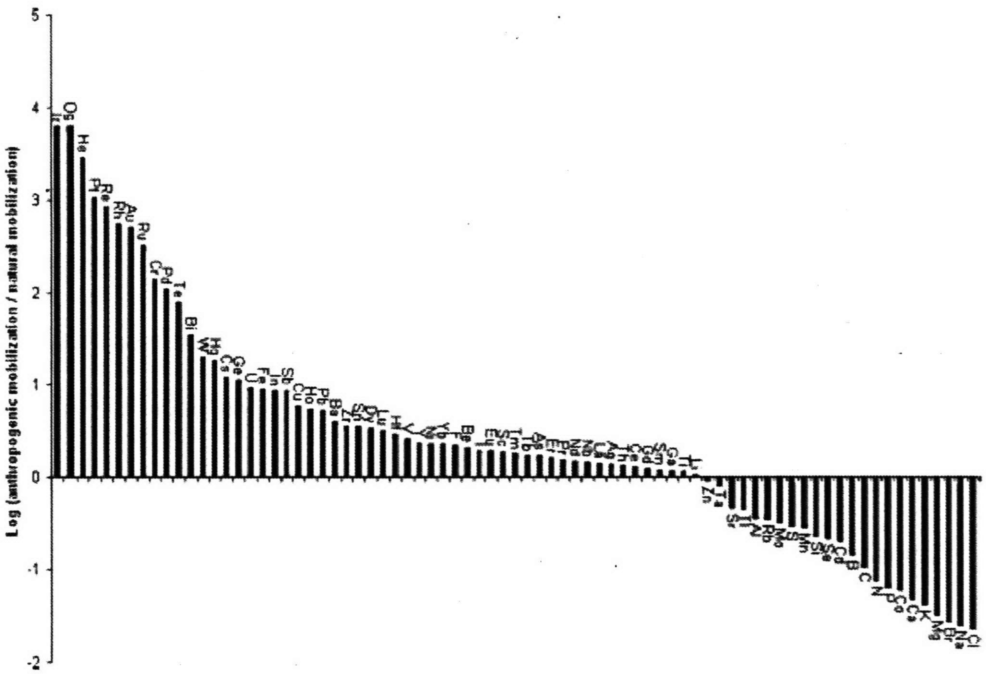


Figure 2.2: Graphic representation of anthropogenic and natural mobilization flows. Elements in the left are mobilized by human beings more when compared to their natural mobilization rates while those to the right are not affected by human mobilization [49].

To identify risk associated with material choices, from an ESH point of view, one should ask the question: could material fluxes associated with semiconductor manufacturing cause changes in the concentration of environmental media? Obviously, this is automatically true for xenobiotic substances, so materials must be evaluated relative to limits set by toxicity testing, global warming potential, or other disruption criteria. To assess fluxes of natural materials, we must consider the corresponding natural cycles establishing those chemicals' ambient concentrations in a simple way. This involves a mass balance treatment for all environmental compartments of interest. Consider the following model:

$$V\, dC/dt = \sum inputs - V \sum k\, C$$

where V is the volume (m^3) of the environmental compartment of interest, dC/dt is the time rate of change of the chemical concentration of interest (mol/m^3 sec), $\sum inputs$ is the sum of all inputs of the material to the environmental compartment (mol/sec), and $\sum kC$ is the sum of first order removal rates of the material from the environmental compartment depending on rate coefficients, k (sec^{-1}) reflects various removal mechanisms, and C (mol/m^3) is the concentration of the material in the compartment. Following is a summary analysis for one element used in semiconductor manufacturing, tantalum (Ta), which has been compiled as a part of this thesis research in collaboration with White and Gschwend.

Examining the state for Ta (Figure 2.3), we see that mining currently mobilizes approximately 8×10^8 kg/yr in support of all industrial applications, and the semiconductor fabrication industry uses only a fraction of this. The natural fluxes for Ta are calculated using literature [56]. Interestingly, fossil fuels (especially coal burning) are responsible for inputs roughly comparable in size to mining (Figure 2.3). Judged in the context of the natural weathering rates, the semiconductor usage may well be benign. However, the total anthropogenic mobilization is comparable to natural inputs implying that steady state exposures to Ta may already be doubled.

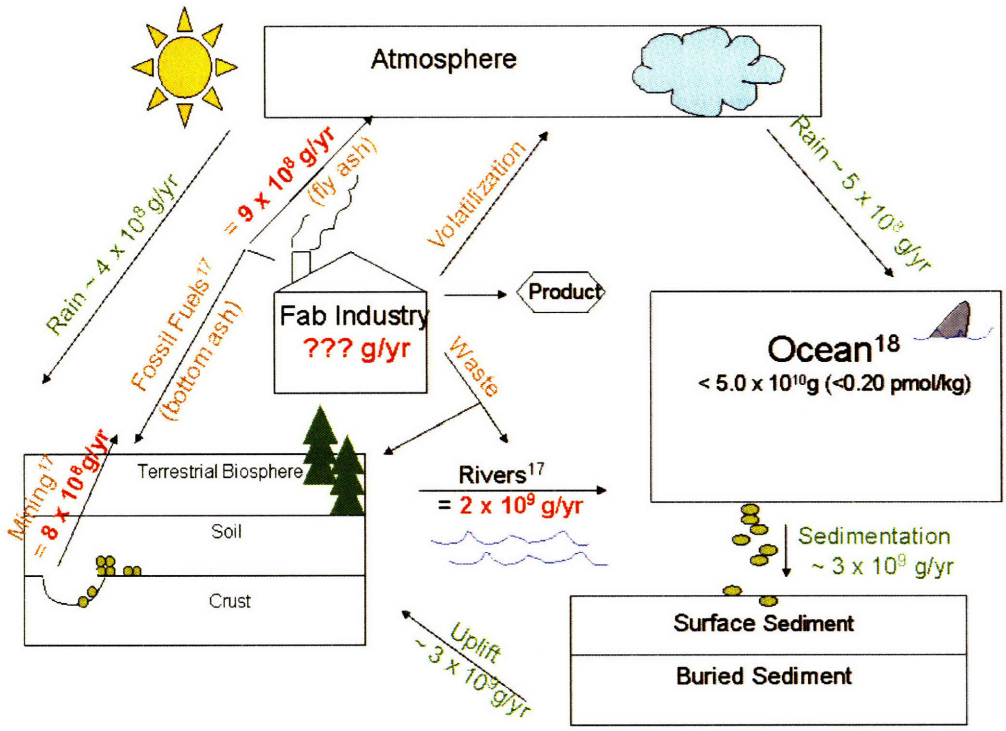


Figure 2.3: Tantalum geochemical cycle (steady-state assumption) [55].

In summary, a preliminary material evaluation for Ta raises a flag that this metal industrial usage will change ecosystem/human exposures. While the semiconductor industry may prove to make-up only a small part of this usage, the prospects for an overall material ban, e.g., as Freon, and PFOS, appear real. Thus, this environmental evaluation suggests that CMOS manufacturing design options might well be served by avoiding Ta use, or to prepare for Ta discharge controls (effective effluent treatment, product recycle) so as to promote longevity of the CMOS technology. More work needs to be done to accurately quantify tantalum's natural weathering rates, its current ambient concentrations, and the changes that we should consider "safe" in an ESH context.

2.4 Case Study 2D vs. 3D

In this section, we illustrate and apply the proposed methodology using a case study comparison between standard (2D) ICs and 3D ICs. Each of the six steps described in Section 2.2 2 will be considered in turn.

2.4.1 Novel Technology Selection – 3D IC

The proposed methodology is applied to an emerging technology: Three-dimensional (3D) integrated circuits (ICs). This technology is currently under active research, further motivating our desire to understand potential environmental issues concurrently with performance and cost optimization. As discussed in Chapter 1, 3D ICs can be fabricated in two ways, by using the epitaxial or bonding approach. Here, wafer-to-wafer bonding is considered, primarily because of its high throughput. In particular, we will focus our analysis on a 3D integration process based on Cu thermo-compression bonding.

This analysis considers a 3D integration process based on substantial prior work on Cu thermo-compression bonding, previously conducted by several researchers at MIT [57],[58],[59],[60]. In this approach, two active device wafers are stacked back-to-face and bonded by means of low temperature Cu-to-Cu thermo compression. Interlayer vertical vias electrically interconnect the device layers. Low temperature wafer bonding is necessary since the pre-bonding device layers already have aluminum metal interconnect lines. This is an attractive scheme because it allows lower aspect ratio interlayer vertical vias and thinner bonding layers. The process sequence in the MIT 3D integration approach is illustrated in Figure 2.4.

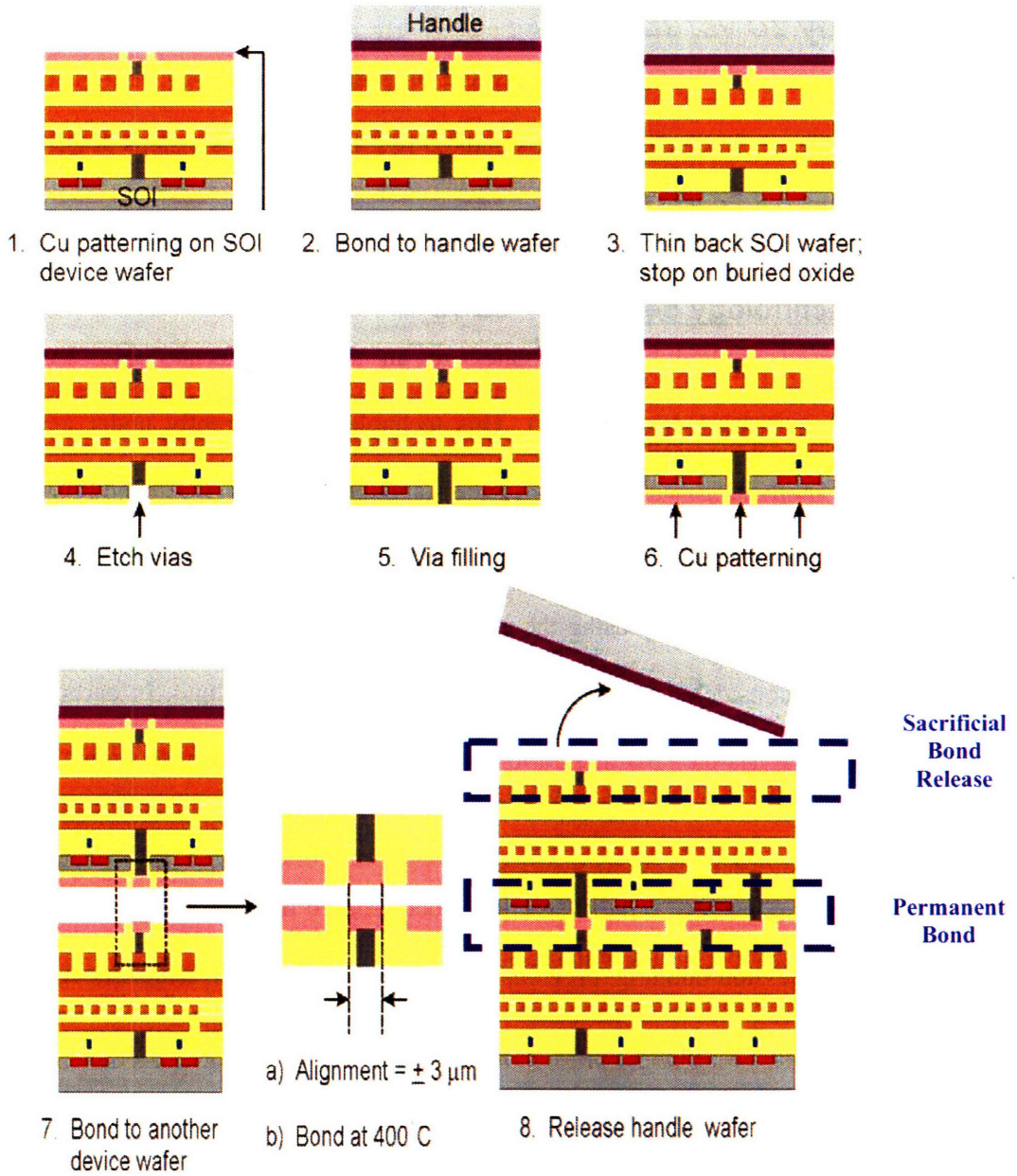


Figure 2.4: MIT 3D IC process flow [58].

In step 1, an SOI wafer is fully processed up to the passivation layer; using a temporary bond, it is bonded face down to the handle wafer in step 2. The SOI wafer is ground back and TMAH wet etched until the buried oxide (BOX) layer is reached in step 3. In steps 4, 5 and 6, through-wafer vias are etched and filled, and copper pads are

formed on the back side of the SOI wafer. In step 7, another fully processed device wafer with a redistribution layer and copper pads is bonded to the thinned wafer stack. Finally, the handle wafer is released in step 8 in order to attach more layers to the two-layer stack.

2.4.2. Environmental Footprint of Standard 2D IC CMOS

As the second step in our assessment methodology, the environmental footprint for a typical 2D IC CMOS logic device process flow using SOI substrates is estimated by breaking each module in the flow down to its constituent unit operations as shown in Figure 2.5. A modular and hierarchical approach is used to generate this environmental footprint. An LCI for each unit step is required, in order to estimate the gate-to-gate inventory. A CMOS process flow repeats the given unit processes multiple times to attain a working device, and thus the full process footprint is estimated by aggregating the unit process impacts.

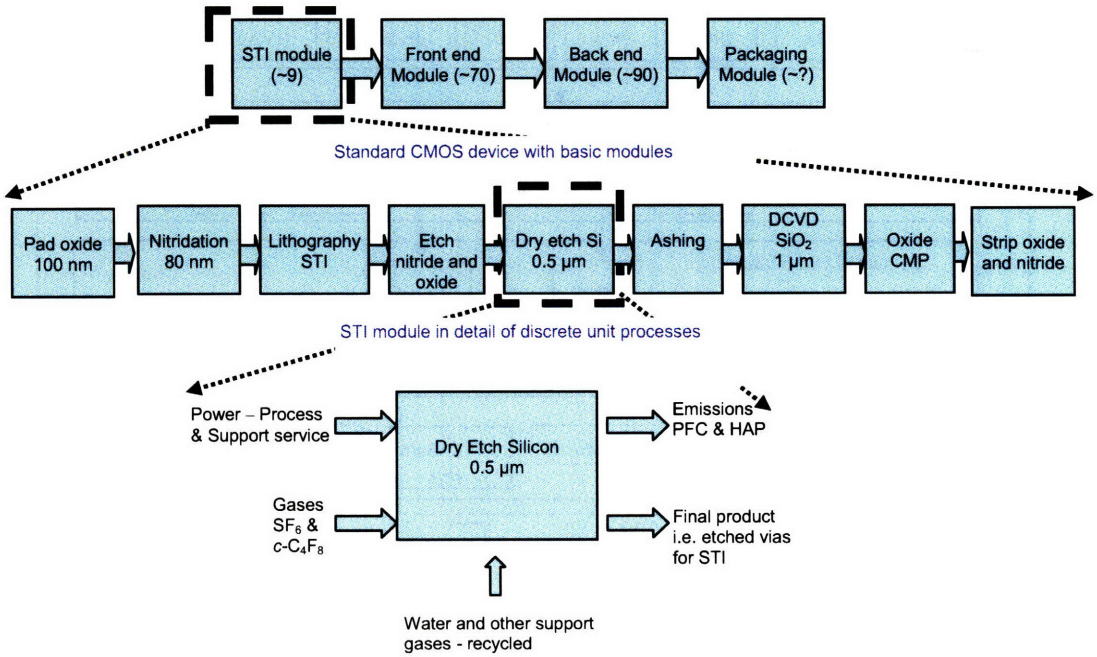


Figure 2.5: Illustration of environmental footprint of a standard 2D CMOS technology.

A hybrid LCI for CMOS based logic devices is used for our analysis; the LCI was developed as part of this thesis research, in collaboration with Krishnan and Boyd, at Applied Materials. Firstly, we develop a bottom-up, within-fab life cycle inventory. Secondly, we perform an approximate evaluation of impacts of upstream chemicals and materials. The within-fab inventory is divided into three layers: process based, point of use abatement, and facilities, as shown in Figure 2.6. The data was collated from several sources including an Applied Materials emission and energy measurement program, TSMC energy measurement data. The process recipes used in this work are not optimized and it is possible that the inventory may differ across manufacturing lines, although other fabs are likely to use similar chemicals and result in approximately similar inventories.

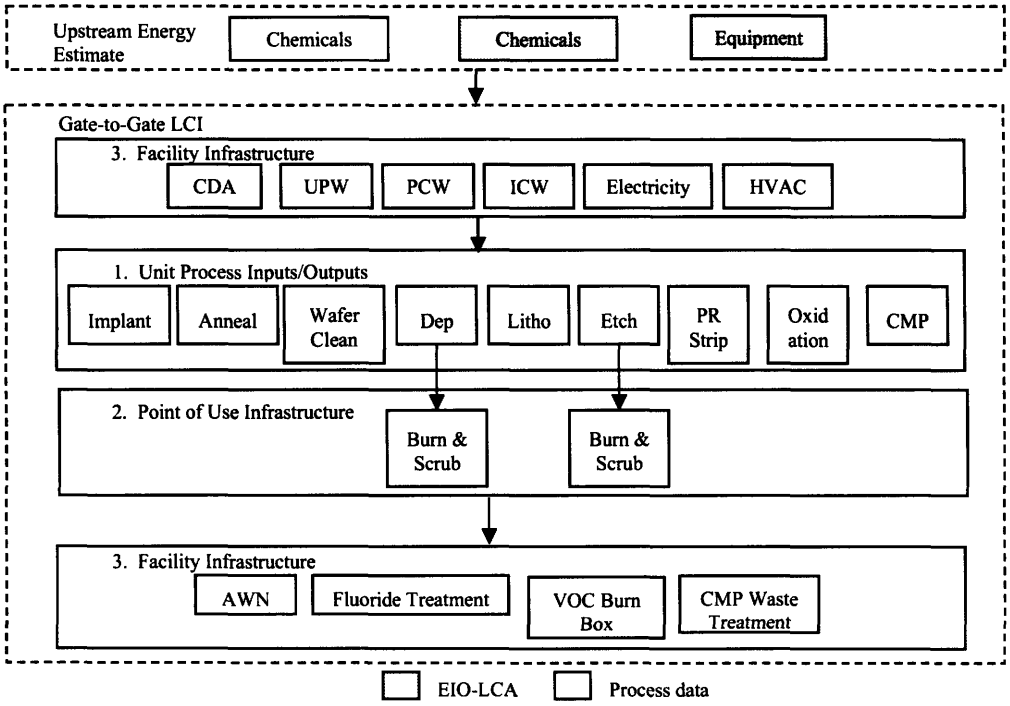


Figure 2.6: Hybrid LCA approach for semiconductor manufacturing [54].

The LCI for a "standard" 2D CMOS logic device with six metal layers is next calculated using the unit process database. A standard "textbook" CMOS process flow is used [61],[62] is used consisting of approximately 200 unit process steps drawn from approximately 40 kinds of unit processes. The first order environmental impact estimation is performed by grouping unit processes based on a broad classification, e.g., LPCVD nitride deposition, DCVD oxide or thermal oxidation, photo step at front end, and so on. Important parameters of each unit process are tracked, such as material deposition thicknesses. For example, a 1-μm film deposition will consume approximately four times the energy and material of a 0.25-μm thick film. The result of this analysis is the environmental footprint of a baseline process, against which we can compare the new technology. Table 2.1 shows the breakdown in unit steps of our 2D process flow. Appendix A summarizes the corresponding environmental footprint for our baseline 2D CMOS technology.

2.4.3 Define Functional Unit

Three-dimensional technology can be used to bond multi-functional ICs (e.g., those incorporating both logic and memory), and thus it can be difficult to compare with a 2D technology that does not necessarily integrate all components on one chip. For this reason, it is necessary to define an integrated system explicitly (including packaging) to make a meaningful comparison. Many modern electronic systems such as computers and PDAs include logic, SRAM, and external DRAM components.

We use an integrated chip consisting of logic and SRAM device areas, as our functional unit, in order to compare 3D to 2D ICs. SRAM is typically fabricated on the same die as logic, as it uses CMOS technology with a 6T memory cell. Therefore, in both

the 2D and 3D IC, we will assume that our logic device has an integrated SRAM cache. In the 3D flow, our functional unit will be assumed to use a two layer structure. This might enable one layer to be used for logic and another for distributed SRAM. In both 2D and 3D systems, however, we will assume that DRAM is accessed externally (i.e. not integrated in the 3D case either). This assumption implies that both 2D and 3D technologies have similar packaging. Thus, our basis for comparison between 3D and 2D CMOS technologies does not consider the potential impact or issues in packaging. Further research is needed to understand the potential environmental, cost and performance improvements which might be achieved by elimination of the package in an integrated 3D logic, SRAM and DRAM system. Such an analysis should consider the potential changes required for 3D packaging technologies. The emerging technology assessment methodology proposed in this thesis could be applied to the packaging module; re-examination of the 2D versus 3D tradeoffs for an expanded functional unit (e.g., including external DRAM in 2D vs. integrated DRAM in 3D) would then be possible.

2.4.4 Design 3D IC Prototype Flow

The fourth step requires design of a process flow for the emerging technology under consideration. The MIT 3D process flow is used here. The wafer bonding module in the MIT 3D IC approach is inserted between the back-end and packaging modules in the standard 2D flow as shown in Figure 2.7. Following our comparative methodology, the processes up to and including the back-end module, are comparable as they are similar in both process flows under consideration.

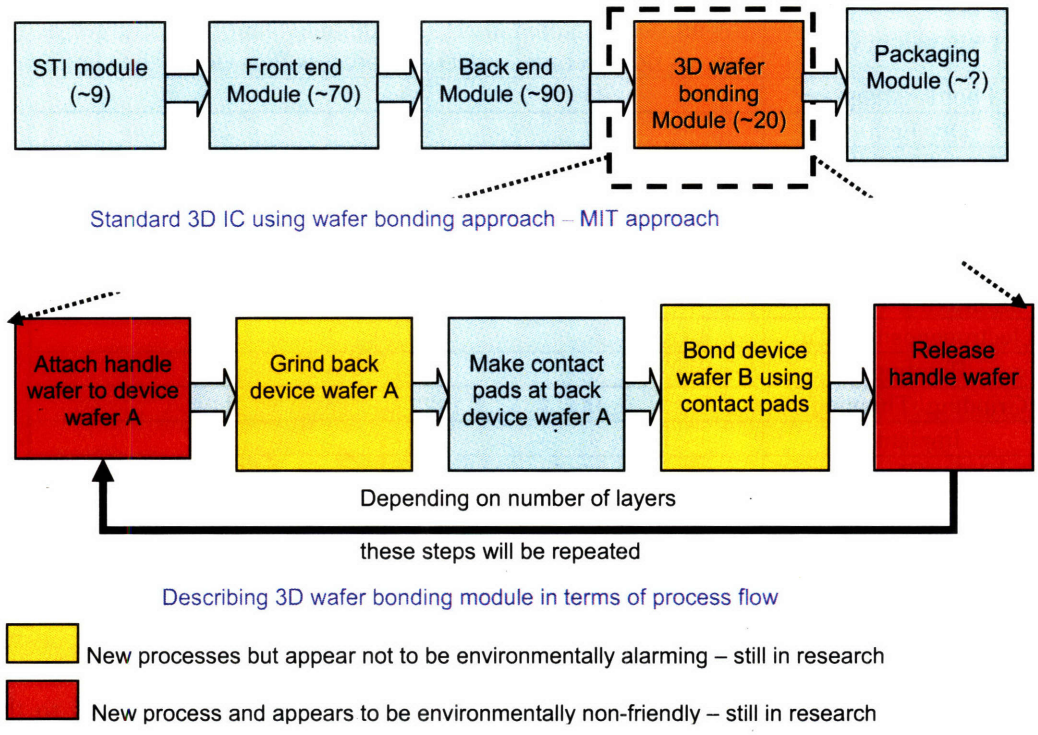


Figure 2.7: Illustration of MIT 3D IC process in terms of module.

The unit process summaries for both 2D and 3D process technologies are compared in Table 2.1. We see that bonding and grinding are the two novel unit process steps injected by the 3D flows, and that twice 20 μm thick deposition of aluminum is used in making a temporary bond and releasing. The remaining process steps added by 3D processing can be approximated as fabricating one additional layer of interconnect stack as they are very similar in scale and number of steps.

Unit operation	# Unit steps required in 2D process flow (for one wafer)	# Additional unit steps required in 3D process flow (to add one layer)
Photo/Ashing	25	1
Dry Etch	17	2
Wet etch/Clean	31/14	3/ 4
CVD	11	1
CMP (Cu and Oxide)	14	2
Sputtering Al	**1 (0.5 μm for metal 1)**	**2 (20 μm)**
Sputtering Ta/Cu	6	1
Electrodeposition Cu	6	1
Bonding	0	2
Grinding/ Thinning	0	1
Implant	9	0
Oxidation/ Annealing	4/7	0/2

Table 2-1: First-order unit process comparison between 2D and 3D IC flows.

2.4.5 Environmental Impact – Identify Critical Unit Processes

The fifth step in our assessment methodology is to identify those unit processes which may be problematic from an environmental point of view, in comparison to the baseline technology. Here, we consider several aspects to the environmental footprint of our 3D IC process, including energy and water consumption along with chemical specific data. In the following sub-sections, we provide a first-order estimation of energy, water and chemical consumption. The environmental impact of new 3D technology steps including thinning and bonding can be approximated using similar existing 2D IC steps and process knowledge or the available literature. The approximations made here are assuming that unit process steps are carried out on 300 mm wafers with state-of-the-art equipment in manufacturing settings.

Energy and Water Consumption

First, we review the energy consumption required in our baseline 2D IC technology, using the LCI database. According to our inventory, the energy for a 300 mm wafer with 0.13 μm technology and six levels of interconnect is 540 KWh/wafer. Our inventory appears consistent with the published literature. Murphy et al. [46] did an

energy inventory for a 200 mm wafer using 0.13 μm technology. They report that 408KWh/wafer is required for an eight-metal layer microprocessor. Another energy inventory conducted recently by Boyd et al. [53] reports that 360 KWh/wafer is required for a similar technology node for 200-mm wafer.

Considering the new process steps introduced in the 3D process flow, next we examine the grinding or thinning steps. We estimated that energy consumption will lie in the range of 25-30 KWh, while water usage will be approximately 5 m^3 per thinning process. This estimate is based directly on a study presented by Schischke et al. [51], who conducted an environmental assessment of flexible passive transponder tags. Their study shows that wafer thinning consumes negligible energy (4%) and toxic chemicals (with TPI 4%) as compared to wafer processing to fabricate the passive transponder, but requires substantial water (19%). Their results are summarized in Figure 2.8 below.

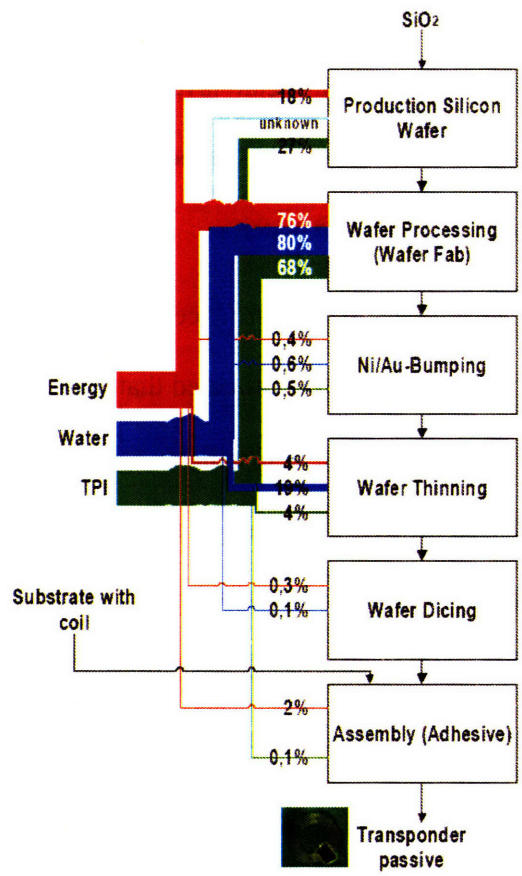


Figure 2.8: Sankey Chart for ProTox (Input TPI), energy, and water using IZM EE-Toolbox [51].

Next, we can estimate energy, water and material consumption for the Cu-Cu bonding step. First, we approximate the energy required for the bond annealing step as being comparable to that used in a conventional thermal process at 350°C for an hour, followed by annealing at 400°C in N_2 ambient for another hour. The conventional furnace is a batch process unlike bonding; thus the energy required for the bonding process is approximately 10-15 KWh for an hour long bonding step followed by batch annealing. Second, we consider the energy consumed in aligning one wafer to another wafer. We approximate this as being equivalent to aligning a mask during photolithography, which

is 2.6 KWh. In terms of water, the wafer bonding annealing step uses process cooling water (PCW) primarily for maintaining the temperature, requiring approximately 1 m^3.

The handle wafer bonding and releasing steps are not present in the standard 2D CMOS process. As summarized in Table 1, we see that the MIT 3D process flow includes a step in which a 20 μm Al layer is deposited on both handle and device wafers; this layer later is etched away selectively using HCl to release the handle wafer. The MEMS community has used Al as sacrificial etch material [63]. As a rough estimate, 1 μm of Al deposition using sputtering requires energy approximately 5-7 KWh. Thus, 40 μms of Al deposition will require as much as 200-280 KWh. The energy consumption of this temporary bond and release process is thus of the same order of magnitude as the energy required for fabricating the rest of the device wafer, i.e. 540 KWh/wafer. The thick aluminum deposition also requires approximately 13.6 m^3 of PCW, in order to maintain the desired substrate and chamber temperature.

As mentioned above, the remaining processes can be approximated as adding one more layer of conventional interconnect, which requires 40 KWh electric energy, and consumes approximately 2 m^3 of PCW and 0.04 m^3 of ultra-pure water (UPW).

Chemical Assessment

We next consider the chemical consumption of 3D flow, compared to the 2D flow. Mechanical grinding can be approximated as a two step process. The first grinding step is purely mechanical, and will only use substantial water and energy. The second step is a polishing step, and can be approximated as a conventional chemical mechanical polishing step conducted for a few minutes. The wet etch mixture used in thinning

process, which follows polishing step, can be recycled a number of times, which means that it requires relatively little consumption per wafer.

Bonding is similar to annealing, using no chemicals, other than nitrogen gas. 20 μm deposition of Al will use substantial Al material and process cooling water, along with argon gas for sputtering. For the release step, HCl acid will be required; however, this steps adds little load compared to the number of cleans used in the normal processing.

In summary, the MIT 3D IC approach requires and addition of roughly 350-KWh electric energy and 14.7 m^3 of PCW to add one more device layer (Table 2.2). This *additional* consumption is quite comparable to the process energy and water requirement for the entire six-layer 0.13 μm technology, which needed 540 KWh and 26.7 m^3 of PCW. In terms of chemical consumption, the 3D process is not alarming, as it used mostly standard chemicals such as N_2, Ar, Al and other chemicals as used for fabricating one additional layer of interconnect. We see that most of the additional energy and water in the 3D process flow is consumed by thick sacrificial metal deposition during temporary bonding, which will be etched away during the subsequent handle wafer release step. With our first order estimation, the thick sacrificial metal deposition for the handle wafer process appears to have an undesirable, large environmental footprint. Therefore, in step 6 of the proposed methodology, alternative and improved options for the handle wafer process must be explored.

	Energy Consumption (KWh)	Water Consumption (m3)			Chemical Consumption
		PCW	UPW	ICW	
Adding 1 layer to 3D Stack	350 +	14.7 +	0.6 +	0.1 +	Equivalent to adding 1 more interconnect layer
2D CMOS, 300 mm wafer, 130 nm technology, 6 metal layers	540	26.6	0.96	0.65	Summarized in thesis Appendix A

Table 2-2: First-order comparison between 2D CMOS and additional processes to add one device layer using Al release layer handle wafer approach.

2.4.6 Alternative Approaches

Step six of the proposed integrated environmental, performance, and cost assessment methodology involves the exploration of improvements to identified problematic steps. As discussed in Section 2.4.5, the existing MIT 3D handle wafer process is by no means environmentally benign. In addition, to environmental concerns, this research prototype unit process also has substantial yield concerns. Fan [58], details several processing issues related to the handle wafer technology. Primarily because of etchant transport issues, Fan was not able to release a 150 mm wafer. With increasing wafer size, it seems unlikely that the HCl release of a thick Al layer will be pursued in manufacturing. The rationale behind the thick Al deposition was to reduce the problem of diffusion; thicker layers were desired to provide the wider channels with less surface tension. Despite the extremely thick Al layer, the release process has poor yield and thus high cost.

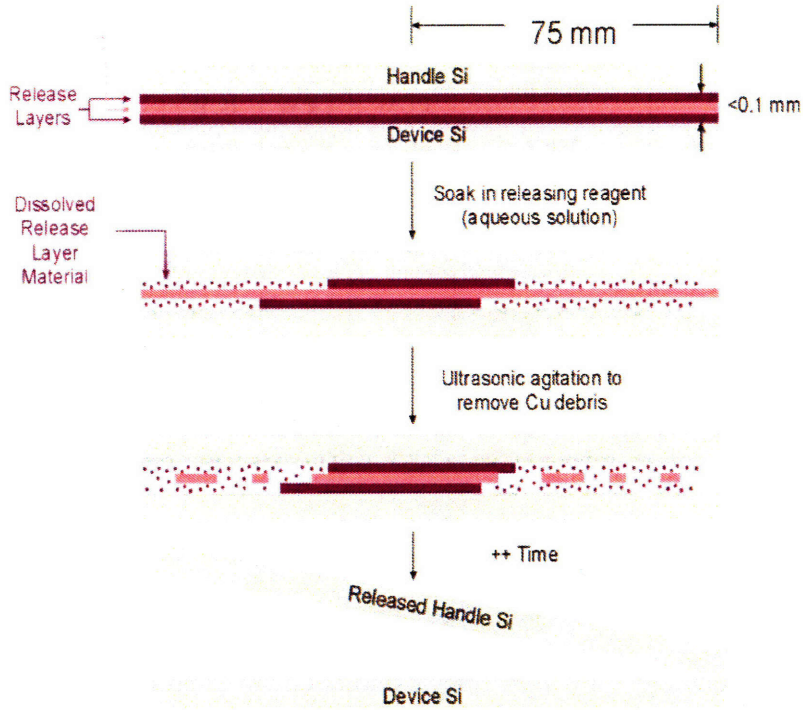


Figure 2.9: Releasing handle wafer using wet-etch in Cu-Cu bonding [58].

Due to combined environmental, performance, and cost concerns as revealed by the combined assessment methodology, the handle wafer step merits deeper study. In Chapters 3 through 6, we propose alternative options for the handle wafer unit process, or including an approach for solving the etchant diffusion or transport problem.

2.5 Performance and Cost Comparison 3D IC vs. 2D IC

As mentioned earlier, to make the assessment of two technologies complete, the technology options need to be compared on all three axes of performance, cost and environmental impact. In this section, we briefly review the performance comparison between generic 3D and 2D IC technologies, and provide a structure for cost comparison between these options.

2.5.1 Performance Comparison

As detailed in Chapter 1, there are several motivations for pursing 3D ICs. After form-factor improvement, 3D IC technology's main advantage is that it significantly enhances interconnect resources. These performance benefits have been studied extensively in the literature, and are generally well understood. Used correctly, 3D IC technology provides improved bandwidth and communication throughput, and reduced wire length. In the best-case scenario, if we ignored the inter-tier vias, we would expect the average wire length to drop by a factor of $(N_{tiers})^{1/2}$. Both wire resistance and capacitance would drop proportionately; that is, power would drop by a factor of $(N_{tiers})^{1/2}$ and wire (RC) delay would drop by a factor of N_{tiers} [112]. Wires with repeaters would see a greater reduction in power and lesser reduction in delay, since repeaters are generally inserted so that delay increases linearly with wire length. Thus, for interconnect- dominated architectures, we would expect a significant reduction in energy per operation.

Various researchers have performed thorough investigations to determine the reduction in average and maximum wire-length. Zhang et al. [110] used stochastic estimates based on Rent's rule to show a roughly 40% reduction in length of the longest wires but only 30% reduction for average wires. Das et al. [111] developed a 3D placer and global router and applied them to the ISPD 98 benchmark circuits. Their results showed an 11% reduction in average wire length when minimizing inter-tier cuts, and a 41% reduction when minimizing wire length. Black et al. [109] at Intel applied 3D to a real *x*86 deeply pipelined high-performance microprocessor, and in initial results, they have shown a 15% improvement in performance along with 15% decrease in power.

Davis et al. [112] at North Carolina State University in collaboration with MIT Lincoln Laboratories (MIT LL), did a full case-study where they designed a three tier 3D IC using a 180 nm SOI process developed at MIT LL, and compared to a 2D IC. They demonstrated 26% reduction in average wire length and 33% reduction in maximum average length. In this study, they further calculated that using three-tiers provided an increase in speed of only 2.4%, which means that this design continues to be limited by the gate delay. Total power was decreased by 23%, which is a combination of the effects of reduced wire capacitance, clock power and short circuit power (this design did not use any repeaters).

Aside from decreasing wire-length, 3D enables disparate technologies across strata. Suntharalingam et al. [113] at MIT LL developed CMOS image sensors combining CMOS with photodiode sensors. Bowers et al. at University of California Santa Barbara, along with Intel Corp, [115], were able to integrate photonic devices on SOI wafers using wafer bonding. Similarly Koyanagi et al. [142] at Tokohou University has been working on creating an artificial retina chip using 3D integration technology. The exploration of this application space has just started.

The heat removal or thermal dissipation is one of the biggest challenges for 3D ICs, along with technology development. Thermal management in 3D ICs is a critical issue that requires solutions beyond the conventional 2D circuit heat-sinking technology. In a 3D wafer or die stack, there are multiple device layers, therefore a multiplication of the power that needs to be dissipated and removed. For circuits operating in saturation, the mobility degradation with temperature tends to be the dominant effect, and each 10°C increase in operating temperature increases delay by almost 5% [116].

Researchers are pursuing some interesting solutions. Rajappa et al. [59] studied the feasibility of liquid-phase cooling in integrated microchannels to dissipate heat in 3D circuits. Wong et al. [117] and Goplen et al. [118] studied effective thermal planning using thermal vias. It has been shown that this can be an effective way to remove heat from the device layers.

3D ICs also present challenges in terms of developing new technology, such as through silicon via (TSV), bonding, and thinning-back. These challenges are summarized in Chapter 1 as enabling technologies required for the success of 3D integration. When a new process technology is introduced in silicon manufacturing, it must go through intensive yield enhancement and process development stages, which have huge costs associated with it. At the same time, one requires a manufacturing infrastructure for all of these new processes. All of these issues can have a substantial impact on cost, as described next.

2.5.2 Cost Comparison 3D vs. 2D

Cost can be divided into fixed and variable parts. The fixed cost can be further divided into two factors: independent and dependent. By independent factors, we mean that it is related to the capital investment in the infrastructure, such as maintenance of the clean room environment. The dependent fixed cost factor denotes the costs related to a particular tool. This might become important in cases where we introduce new technologies that may require new equipment. In 3D IC technology, one needs bonder and high-aspect ratio DRIE silicon etcher equipment. The variable cost per function of an IC depends on the equipment productivity, manufacturing yield, and number of chips

available per wafer [119]. The productivity and yield are tied strongly to the manufacturing process complexity.

Yield can be the most important aspect in determining the cost. For example, 1% assembly yield losses for the Intel Pentium microprocessors cost over $42 million annually [120]. Yield can be affected by several parameters, such as wafer size, die size, number of processing steps, complexity of steps and feature size. Unit step yield becomes more important when the step is conducted late in the manufacturing cycle. In the 3D IC flow, wafer integration takes place after BEOL and before packaging, as shown in Figure 2.6. Thus, the 3D process step yield is a critical cost factor.

Cost will play an important role in the final decision as to whether or not any technology option is viable. In this section, we identify factors that will help determine the cost of 3D IC technology, based on yield, and on new tools and processes that need to be developed.

In our methodology, we focus on comparison between two options. In Section 2.4, we identified processes that make the two process flows different. Unfortunately, there are no process-based cost models publicly available, which make it difficult to calculate the cost difference between the two options. Rahman et al [114] illustrated a very basic cost comparison approach by estimating the cost of bonding another device layer as being equivalent to adding one more interconnect metal layer. In the following, we use that approach, enhanced by consideration of the cost of the handle wafer as identified in Section 2.4.

By examining the 3D IC processing steps necessary for the MIT 3D wafer bonding approach, we find that the complexity associated with the wafer bonding process

is comparable to the complexity for integrating an additional interconnect level per device layer, with the additional cost of the handle wafer process. Therefore the variable fabrication cost (v.c.f.) will be proportional to $(mI+n_b(I+h))$, where m is the number of interconnect levels per device layer, $n_b = N_z - 1$, number of inter-device bonding steps, I is the cost of one interconnect layer for that particular technology, and h is the cost of handle wafer process. In Chapter 7, following the consideration of new handle wafer and bonding process approaches, we will return to make a comparison of these approaches, including the analysis of the cost of these alternatives. The cost function for 3D ICs also depends on the chip area. If we want to have the same number of chips or wafers processed, then the device layer chip area for any one wafer layer will be reduced by factor of $1/N_z$.

Akraguld [121] presented Sematech's preliminary cost comparison of 3D interconnects with its two other competing technologies, 2D SOC and chip stack. He determined that 3D interconnects provide the best performance value when normalized with cost. The results are summarized in Figure 2.11 which shows that 3D interconnects are a low cost solution with high performance levels. Sematech further evaluated different 3D integration process options using the CRM model [122], and those results are available to Sematech member companies.

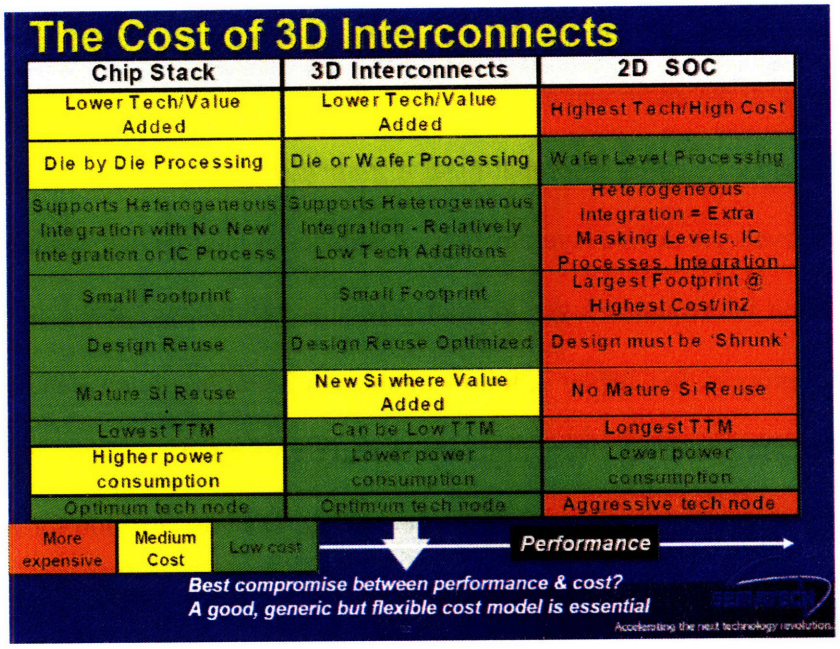


Figure 2.10: Preliminary results of a cost study conducted by Sematech, comparing 3D interconnects with two other competing technologies - chip stack and 2D SOC [121].

2.6 Summary

A new environmental assessment methodology is proposed, to enable evaluation and comparison of technology options early in the development cycle. The methodology includes analysis of performance, cost and environmental issues associated with an emerging technology.

This new methodology is applied to the analysis of the MIT 3D IC approach, in comparison to a standard 2D IC technology. The environmental footprint of a conventional 2D CMOS process flow for a 130 nm technology node, 300 mm wafer with six metal layers is generated, using a process based inventory. The wafer bonding back-to-face integration approach can be modularized and compared to the 2D flow; the bonding module, which comes in between interconnect and packaging modules, introduces 22 additional unit process steps. Seventeen of these steps are standard CMOS based unit process steps, which can be approximated as adding process costs and

environmental impact equivalent to one additional conventional CMOS metal layer. The remaining five steps comprised of grinding/thinning back, two thermo-compression bonding and two thick deposition of sacrificial aluminum metal layer. The environmental load of the five unit processes are estimated using process-based knowledge and existing literature data. Based on analysis of the sacrificial metal deposition, this step is found to be highly energy and water consuming, with high environmental impact and low yield. This process is part of the handle wafer process, a critical process for back-to-face 3D integration. Due to its combined environmental, performance, and cost concerns, the handle wafer step merits deeper study and further development. On the performance axes, 3D IC has several advantages while on the cost dimension, the additional cost can be approximated as the sum of one more interconnect layer and the handle wafer.

Our application of the proposed environmental, performance and cost assessment methodology thus successfully identifies one critical process step that needs improvement. In Chapter 3, we overview the potential handle wafer process options. Chapters 4 and 5 then pursue further development of two alternatives. Chapter 6 considers a means to change the constraint on handle wafer step, by also improving the permanent bonding process. Thus, Chapters 3 through 6 can be considered a demonstration of the sixth step in our proposed assessment methodology, where we explore alternatives for the most problematic step in our 3D IC case.

Chapter 3: 3D IC Handle Wafer Options

As established in the previous chapter, the handle wafer process has substantial environmental, performance and cost concerns, thus requires more in-depth study to understand the alternative options available. Section 3.1 details the purpose of the handle wafer step for 3D integration, and explains the key requirements for this unit process. Section 3.2 briefly reviews different handle wafer options pursued by various researchers, including those at MIT. Section 3.3, summarize what we learned from these process options and previews our new approaches for the handle wafer process.

3.1 Motivation and Requirements for Handle Wafer

In this first part of this section, we describe the motivation for pursuing handle wafer process improvements and the significance of this step in the 3D IC flow. In the second part of this section, various issues related to handle wafer process are discussed, and we review the requirements and goals of an ideal handle wafer or support wafer process. These criterions will also serve as the basis for performance comparison of our new approaches, presented later in Chapter 7.

3.1.1 Motivation for the Handle Wafer Process

Two different kinds of integration are possible in wafer bonding for 3D ICs at the wafer-level, i.e., face-to-face or back-to-face. Face-to-face integration does not require any support or handle wafer, because one device wafer can act as the base wafer on which all other device layers are mounted. In the back-to-face approach, however, a handle wafer is essential, as it provides mechanical support for a thinned wafer. If we bond only two layers, face-to-face integration has fewer steps and is easier in terms of

alignment than a back-to-face approach. The face-to-face approach, on the other hand lacks stability: when one needs to bond more than two layers, multiple face-to-face bonding is not possible, and would require development of both back-to-face and face-to-face processes.

The handle wafer process is a critical step in back-to-face 3D IC integration, and is the preferred method used in the MIT 3D IC process flow. The handle wafer acts as a transfer wafer for the thinned layer, and provides support during the device layer grinding and thin-back steps. The handle wafer process is crucial in determining the thickness to which the device wafer can be thinned, which in turn dictates the density of interconnects between the two device layers, in addition to alignment. The interconnect density between two device layers is one of the most important factors in determining the viability of 3D ICs. For the reasons stated above, there is an increasing focus on back-to-face integration with both via first and via last approaches. Various handle wafer options are reviewed in this chapter, based on the information in literature. All have issues with their yield (performance), cost or manufacturability.

3.1.2 Requirements for the Handle Wafer Process

The handle wafer step is a critical unit process needed in future 3D IC technologies that involve back-to-face bonding. The function of the handle wafer is to provide mechanical support during grind back and TMAH etch-back, and to enable transfer of the thinned device layer to another device wafer. In the MIT 3D technology, the release must be selective to the permanent Cu-Cu bond and must not affect integrated device performance. Ideally, the handle wafer step, as a unit process, should not impact any performance characteristics of the final product, and should have minimal negative

impact on the overall yield of 3D ICs. In this section, various characteristics required by the handle wafer and by the temporary bonding layer used in the handle wafer step are outlined.

Bond strength of temporary-bond: The temporary-bond should possess high bonding strength to support wafers during subsequent harsh processes, including back-grinding and polishing.

Void-free bonding: The final performance of the bonded pair requires a strong and void-free bond, even though the bond layer is sacrificial. Even if the bond is strong and planar across the wafer, very small voids (~1 mm) can still cause issues in steps following back-grinding, such as metallization. Small voids can burst under the conditions of the metallization process and leave defect points in the thinned substrate.

Chemical resistance: The temporary bonding material intended for wafer bonding applications must withstand strong acids, alkalis, and solvents at high temperatures during various processes including etching and metallization. This can be particularly challenging given that layer is also sacrificial and must enable easy release at a later point in time.

Thinning-back capability: There are various kinds of wafer-thinning processes available. In our experiments, we have used a combination of back-grinding followed by wet isotropic silicon etch using tetra-methyl ammonium hydroxide (TMAH). The handle wafer structure should show integrity to the thinning back process.

Thermal properties: The handle wafer and temporary bond to the high processing temperatures at various stages of wafer-thinning, and processes after wafer-thinning such

as dielectric deposition and metallization. Therefore, it is important for the temporary bonding material to perform well over a wide range of temperatures, particularly to avoid degradation and delamination.

Debonding or release of thinned wafer: Last but not least, the ease of transferring the device layer to the base wafer or bonded stack is very important for the success of the handle wafer process. Most of the handle wafer requirements are aligned and mutually beneficial, and can be satisfied with a number of temporary bonding materials. In contrast, the need to release the handle wafer selectively enforces substantial limitations on the selection of bonding material and process approaches. In Section 3.2, we describe several existing approaches taken by researchers for designing handle wafer process.

3.2 Various Approaches for the Handle Wafer Process

Before 3D IC technology, support carrier or handle wafers have been used primarily for wafer thinning, to achieve thin dies required in specialized applications such as smart card and die-stacking. Another technology which uses a layer transfer step is silicon-on-insulator (SOI) manufacturing, In this section, we describe various approaches for handle wafer processes that have been previously explored at MIT and elsewhere.

3.2.1 Handle Wafer Approaches at MIT

At MIT, there are primarily two handle wafer process approaches that have been investigated: 1) use of a metal as a release layer which can be etched later [58]; and 2) oxide to oxide bonding with release of the bond at a later point using a smart cut process, i.e., by annealing implanted hydrogen [57].

Al Release Layer

For the first approach, metals such as zirconium and aluminum have been used to act as the release layer. Fan [58] proposed to use a laminate structure, a schematic of which is illustrated in Figure 3.1. The concept is to break down the problem into multiple layers for specific purposes. First, there is one permanent bonding material that can withstand mechanical grinding and corrosion. There is a second cladding material which will be destroyed using a specific reagent to facilitate the separation of the handle wafer and 3D stack. Copper was chosen as the material for permanent bonding because of its resistance to non-oxidizing acids and alkaline solutions up to 120°C. At the same time, it can form bonds below 400°C with good strength. Aluminum was chosen as the cladding material because it can be removed easily using hot hydrochloric acid (HCl).

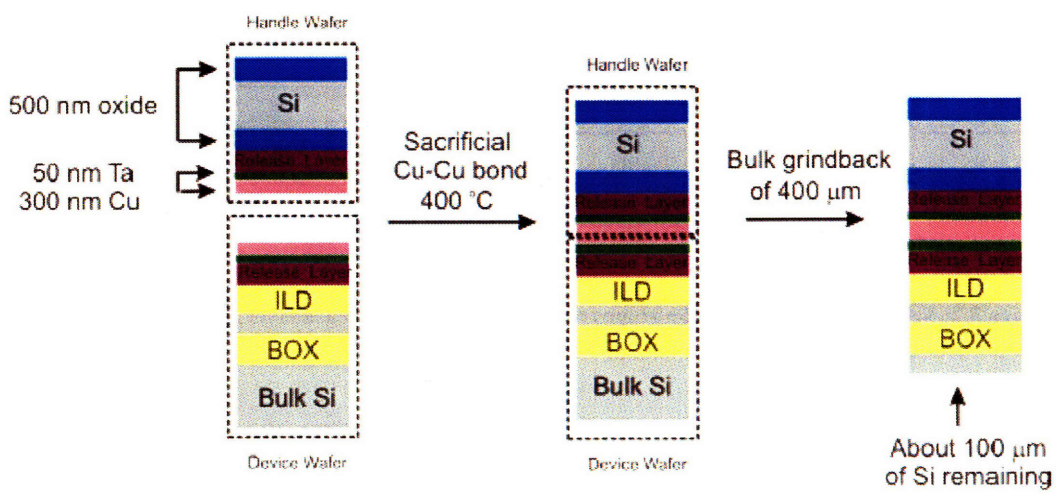


Figure 3.1: Laminate structure used for the handle wafer [58].

The primary challenge in this approach is the mass transfer in the release cavity, as it requires by-products to be removed and fresh reactants to reach the exposed and moving Al surface. Providing agitation using ultra-sound can assist in the mass transfer. The acid penetration problem is exemplified in Figure 3.2. As illustrated, small H_2

bubbles coalesce to form bigger bubbles, which can create a blockage. Such bloackages will affect release in two ways, by decreasing the concentration of acid at the reaction site and by increasing the level of by-products of the etched Al increase which together can stop the release process [58].

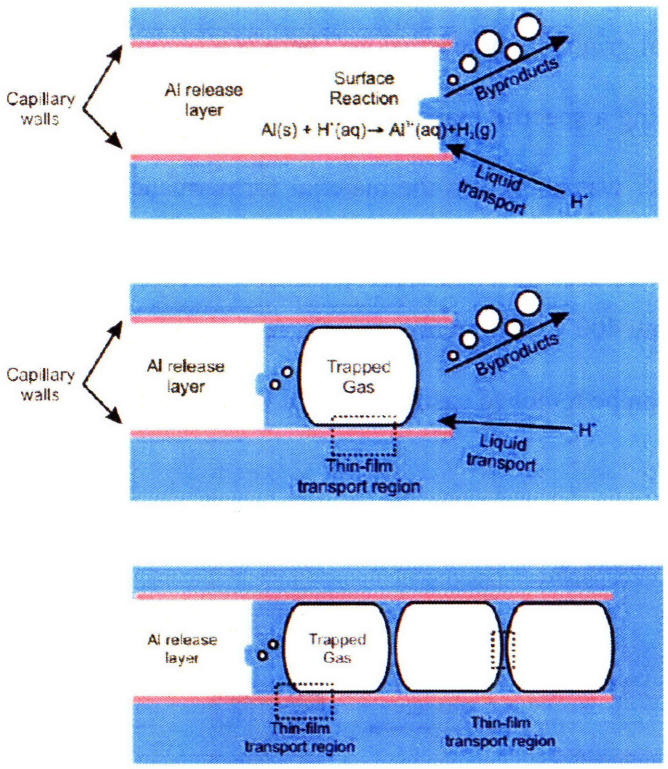


Figure 3.2: Schematic of the reaction stages of Al etching of the release layer, in which H_2 bubbles can become trapped in the release channel [58].

The main lessons learned from this prior work are the need to find etch mechanisms not constrained by gaseous by-products, and the need for the multiple channels to improve accessibility of reactants and removal of products.

Smart Cut

In the second approach previously explored at MIT, the smart-cut process is used to release the handle wafer which is bonded with low-temperature oxide bonding as

shown in Figure 3.3 (a) [33],[36],[57]. H_2^+ ions at a dose of 5 x 10^{16} cm^{-2} are implanted at 150 keV into the handle wafer prior to wafer bonding. Upon heating at the appropriate temperature, lateral micro-cracks induced by hydrogen will release the handle wafer at the location around the peak of the hydrogen implant profile. Figure 3.3 (b) shows the SIMS profile of the implanted hydrogen with a peak about 300 nm into the silicon handle wafer from the oxide-silicon interface. To achieve successful bonding, it is important to ensure that the hydrogen implant does not increase the surface roughness of the oxide handle wafer excessively.

This process is temperature sensitive; all heat treatments prior to layer splitting are kept at 300°C or below. Therefore, this handle wafer approach requires a permanent bond to be made at a temperature below 300°C, which is a challenge with present copper bonding which requires at least 350°C for one hour. Hydrogen induced wafer splitting was achieved with annealing at 300°C for 1 hour. This process has the potential to perform satisfactorily, provided that there is a technology which can enable low-temperature conductive bonding. An important drawback, however, is that the process can be very expensive. The cost of wafers made by Soitec, which produces SOI staring wafers, for device manufacture using smart cut technology, is substantially higher than SOI wafers made by using SIMOX technology. H_2 implantation makes the silicon wafer cost 5-10 times more than bulk silicon wafer.

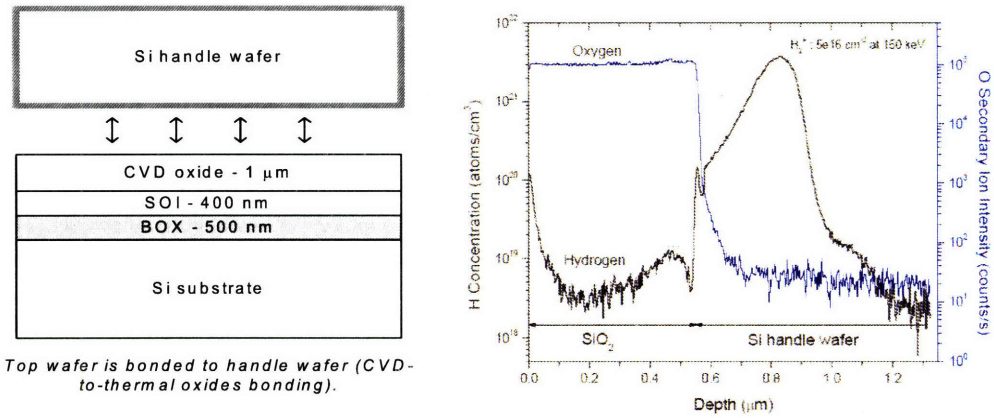


Figure 3.3: a) Implanted handle wafer bonded to device wafer using low-temperature bonding. b) SIMS profile of implanted H_2^+ ions in handle wafer [36].

3.2.2 Other Handle Wafer Approaches

Several organizations are pursuing various handle wafer approaches. Selections of these are reviewed in this section.

IZM Fraunhoffer [34] uses a porous Si-handle wafer and bonds with layers of polymide and BCB. These can be dry etched through the porous wafer for releasing (Figure 3.4). This appears to be an expensive option for two reasons. To make the silicon wafer with micro holes will require special fabrication process. Secondly, processing of handle wafers with micro holes will require different tools, as standard vacuum handling on the conventional fabrication equipment will not work.

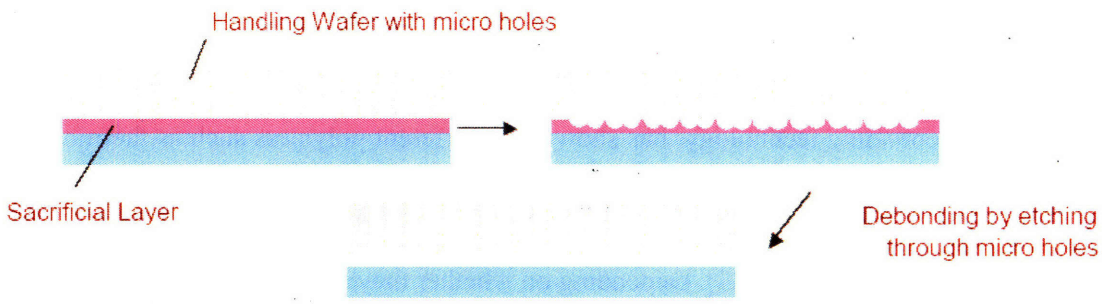


Figure 3.4: IZM handle wafer approach [34].

IBM [28] uses a schott glass handle wafer that can be bonded with a polymer to a Si-device wafer (Figure 3.5). The glass wafer also aids in alignment, as it can be used with standard lithography, whereas other flows may need IR alignment or another sophisticated alignment approach. Pogge et al. [35] detail the IBM handle wafer bonding approach, in which they coat PTFE on a schott glass and bond it using polyimide located on the handle wafer. Laser illumination, transparent to the glass, is used to burn off and release the polymer. This is an interesting approach, although little data about performance and manufacturability is available.

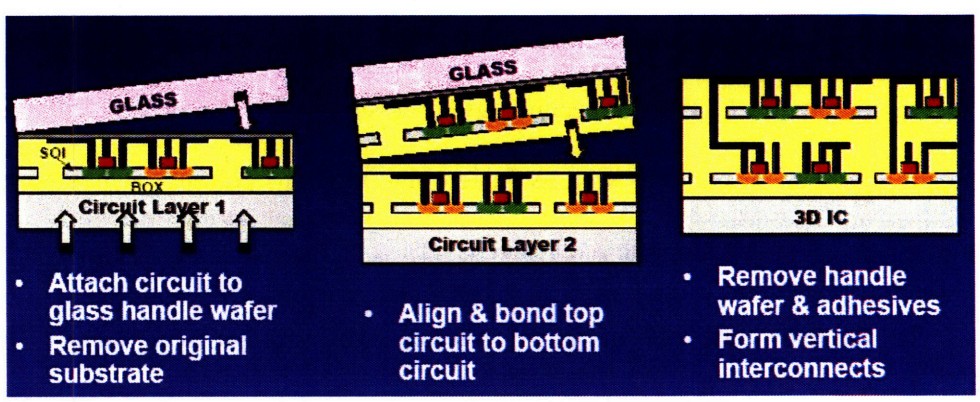


Figure 3.5: IBM's 3D integration handle wafer approach [28].

Another common method used to bond wafers temporarily is to use an organic polymer, which can later be thermally decomposed at temperatures such as 200-350°C.

Polymers suffer from the problem of low modulus, creating problems during grind back as shown in Figure 3.6 [97]. Electronics Vision Group (EVG), a company actively pursuing debonding technology, has shown that different polymers such as thermosetting and thermoplastic polymers, can be used to make a temporary bond, followed by etch back of the device layer [123]. Depending on whether they are thermoplastic or thermoset polymer, the temporary layer can be debonded at 200°C or 350°C.

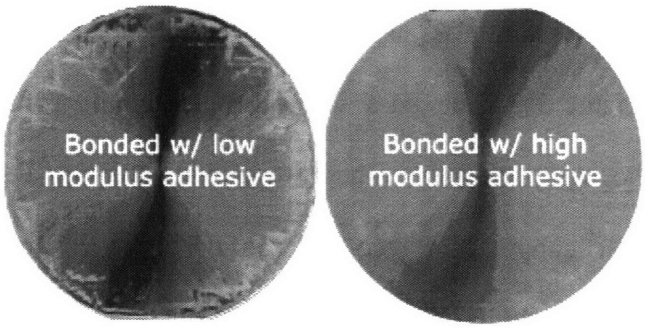


Figure 3.6: Silicon grind quality using low modulus adhesive and high modulus adhesive [97].

The problem with this approach, besides suffering from a low-modulus, limiting grind-back options, is the degradation of temporary bond with temperature. The thermoplastic materials are stable up to 200°C, while the reversible thermoset materials start outgassing at 275°C. For this technology to be successful, one needs to find a low-temperature permanent bond, as well as design high modulus adhesive which are stable through to release of the temporary adhesive layer.

In summary, the use of an Al release layer together with copper for the permanent bonding layer works well with respect to all the required characteristics, as mentioned in Section 3.1.2, with the major exception of the release or debonding requirement. Smart cut and adhesive bonding seems to satisfy several criteria, but has poor thermal properties, as the bonding layers degrade with high temperature processing.

There is not much known about the IBM and IZM handle wafer approaches, making it difficult to comment in detail on the strengths and weaknesses of these technologies. Table 3.1 summarizes the performance characteristics of the three different handle wafer options.

Handle Wafer Approaches	Bond strength	Void Formation	Chemical Selectivity	Thinning-back Capability	Temperature range	Time to debond
Al Release Layer	3 J/m2 ✓	No ✓	Probably with TMAH ↔	Good ✓ < 1 μm	Good ✓	Does not release in finite time ✗
Smart Cut	2 J/m2 ✓	Few ↔	Good ✓	Good ✓ < 1 μm	Requires processing temp. less than 250oC ✗	Good, released in 60 min ✓
Temporary Adhesive	Do not have information	No ✓	Good ✓	Poor, Requires 80 μm ⌋	Requires processing temp. less than 250oC ✗	Good release in 30 min ✓

Table 3-1: Performance comparison of three different handle wafer options. An ✓ indicates good, an ↔ indicates it can be improved while an ✗ indicates that particular option does not work because of this particular requirement.

3.3 Our Approach

In this section, we describe our approach to the environmentally conscious design of the handle wafer process for back-to-face integration of 3D ICs. One line of attack is to overcome the performance and environmental problems inherent in the previous MIT aluminum release layer approach. The other line of attack is to consider alternatives for the permanent bonding layer which might enable or support higher temperature processing. If such a permanent bonding layer could be found then attractive handle wafer approaches such as smart cut and adhesive bonding may become feasible.

Two ideas are explored to solve the diffusion problem for chemical release of the handle wafer. The processes and materials used in these approaches are CMOS

compatible, using processes available in BEOL technology. In both new approaches, channels for facilitating mass diffusion are created, either etched in the device wafer or in the handle wafer. In the device wafer, the channels can be etched only at the die-saw line, as this is the only place where there are no product devices. In the handle wafer, channels can be etched anywhere.

In Chapter 4, we describe the handle wafer approach in which channels are etched in the device wafer. The temporary bond is made using the same stack structure as in the Al release layer process.

In Chapter 5, we demonstrate another approach, where channels are etched in the handle wafer. This approach use low-temperature oxide bonding, with oxide serving as the release layer.

In Chapter 6, we consider the use of copper-indium to make the permanent conductive bond, using a solid liquid inter-diffusion (SLID) bonding approach. The main idea is to create a permanent bond at temperatures, as low as 200°C, in order to enable handle wafer approaches like temporary adhesive bonding and smart cut.

The approach used for consideration of these new handle wafer involve proof of concept, followed by comparison of performance, cost and environmental concerns of the alternative options. Chapter 7 discusses the overall comparison of four handle wafer process options. As mentioned earlier, the performance of the handle wafer process isis considered to be the yield of 3D process integration. The handle wafer process is also evaluated using the comparative methodology proposed in Chapter 2, including analysis of the environmental footprint of the whole handle wafer process module.

3.4 Summary

The handle wafer process is fundamental for back-to-face 3D IC technologies. Key requirements include temporary bond strength, void-free bonding, chemical resistance, thermal properties and debonding or release abilities. Various approaches for handle wafer were reviewed. Approaches involving an Al release layer, which use a subsequent chemical release step, are diffusion limited. Methods such as smart cut and temporary adhesive bonding have poor thermal characteristics, and can only tolerate temperatures up to 200-250°C. In order to improve and enable the alternative approaches for the handle wafer process, three technology improvements are explored in the following chapters. First, channels in the device wafer are considered in Chapter 4, to overcome mass transport and diffusion limitation in the Al release step. Second, channels in the handle wafer, using oxide as the release layer are considered in Chapter 5 to overcome limitations in the between-die channel approach. Third, an alternate copper-indium SLID approach is explored in Chapter 6, with the goal of enabling low-temperature permanent bonding. After discussing these new approaches, we return to our assessment methodology in Chapter 7, where we analyze and compare the various handle wafer process alternatives.

Chapter 4: Between-Die Channel Approach for the Handle Wafer Process

Based on our comparative environmental impact evaluation study between the MIT 3D IC and standard 2D IC, we established that the handle wafer process in the MIT 3D IC flow requires deeper study because of its environmental and performance concerns. In Chapter 3, after surveying different handle wafer integration technologies, we found that there is no single process to satisfy all the concerns and requirements for the handle wafer. In this chapter, we describe a novel approach that uses channels in between die the device wafer, together with the same laminate structure used by Fan [58], consisting of an Al release layer and copper permanent bonding layer. Section 4.1 presents background information and introduction to this new approach. Section 4.2 describes the fabrication used for this work, including extensions for channel formation; processing concerns are also identified. Section 4.3 presents the results, and discusses modifications for more effective release.

4.1 Background and Introduction

The proposed approach is inspired by Fan's [58] work on 3D IC technology. He uses a laminate structure, a schematic of which is shown in Figure 3.1. The concept is to break down the problem into two parts, so there is one permanent bonding material that can withstand mechanical grinding and corrosion, and another material to enable handle wafer release. With the proposed laminate structure, Fan could not release a six inch bonded wafer stack, but was able to demonstrate that square dies of area 1 cm^2 can be released effectively. Die-scale release succeeds because the required penetration length

for the liquid etchant becomes smaller, easing diffusion of both reactants and products. This result is significant and valuable as 1 cm^2 is approximately the size of today's functional die. However, Fan's existing process does not support wafer-level bonding and release, motivating the need for an improved process.

The release concept proposed below maintains wafer-level integration and provides channels for chemical release, utilizing the fact that the laminate structure, with an Al release layer, succeeds for 1 cm^2 dies. Our approach also borrows the ideas from a singulation technique called dicing before grinding (DBG) [125], which has gained attention in the last few years because of its damage free singulation (cutting of wafer into individual die) of thinned wafers.

The notion of DBG [125] is explained briefly with the help of the schematic flow in Figure 4.1. In the existing DBG technology, the wafer is initially half-cut with a special dicing saw. After tape lamination to hold the die, singulation is achieved when the wafer is thinned below the level of this cut. Afterward, the wafer then goes to the in-line DBG mounter, which gently peels off the protective grinding tape, completing the process. In the DBG process, thinned wafers are never transported, thus wafer-level breakage is greatly reduced. In addition, because die separation occurs during the grinding process, the backside chipping associated with thin-wafer dicing is kept to a minimum. DBG also offers exceptionally high die strength.

In the new proposed handle wafer and release approach we form channels between-die in the device wafer, for fluid transport rather than for the purpose of die singulation. This DBG inspired approach also takes advantage if the thinning concept, in our case to release the handle wafer rather than to separate die.

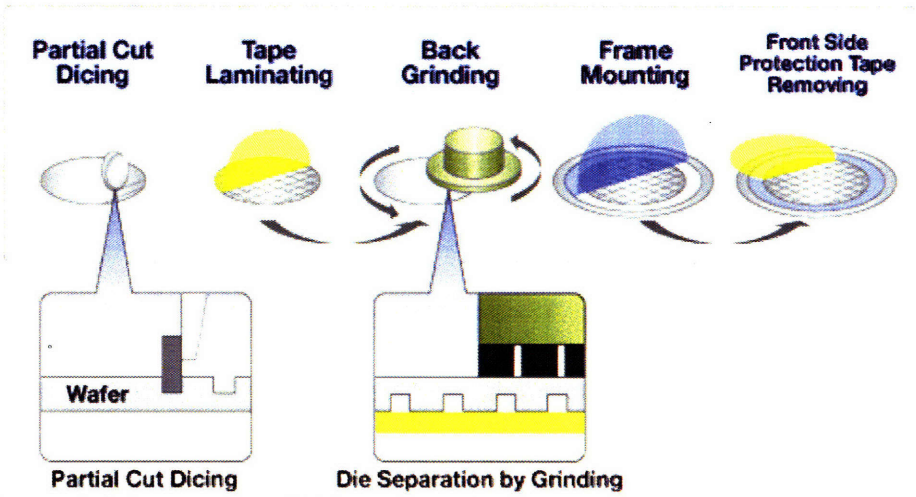


Figure 4.1: Schematic flow of dicing before grinding (separation by wafer thinning) [125].

4.2 Experimental Procedure

This section first describes, with figures, a prototypical flow for the proposed between-die channel handle wafer process. Concerns regarding this approach are noted. The fabrication procedure is described to prove the feasibility of the concept. In our demonstration, there are no active devices formed; rather a dummy device wafer is created by depositing blanket layers, followed by channel patterning, bonding, thinning and release. Each of the unit process steps and process parameters are described in detail.

4.2.1 Prototype Flow

In this section, we describe the back-to-face wafer-level integration approach using between-die channels formed in the device layer. This approach uses a similar laminate structure for the handle wafer to that developed by Fan. This approach is illustrated in Figure 4.2, and consists of the following steps:

1. Once the SOI device wafer A is ready for 3D stacking, between-die channels are printed using a thick resist.

2. Using the between-die mask, deep channels are etched in the inter-level dielectric (ILD) and inter-metallic dielectric (IMD) material, through other etch stop layers and into the silicon, then finally through to the buried oxide layer (BOX).

3. Any chemical release layer is deposited on the front of the device wafer A. Subsequent to the release layer, the bonding layer is deposited on both the device wafer and the handle wafer.

4. Device wafer A and the handle wafer are bonded using thermo-compression bonding.

5. The device wafer is thinned using grind back and wet etch. Dies remain affixed to the handle wafer but are only separated from each other. The BOX layer acts as an etch stop during etch back.

6. Contacts are made from the back side, using conventional lithography since the dies are very thin. An alternate is to use the "Cu-nail" technology described by IMEC [64], in which one integrates the 3D IC in the front-end by forming Cu or W vias before M1 in STI.

7. Using the handle (transfer) wafer, thinned dies are bonded to another device wafer B, again using same thermo compression bonding as described in step 3.

8. The last step is to release the die from the handle wafer using a selective chemical etch. In this step, the etched between-die channels help in effective chemical release of the handle wafer.

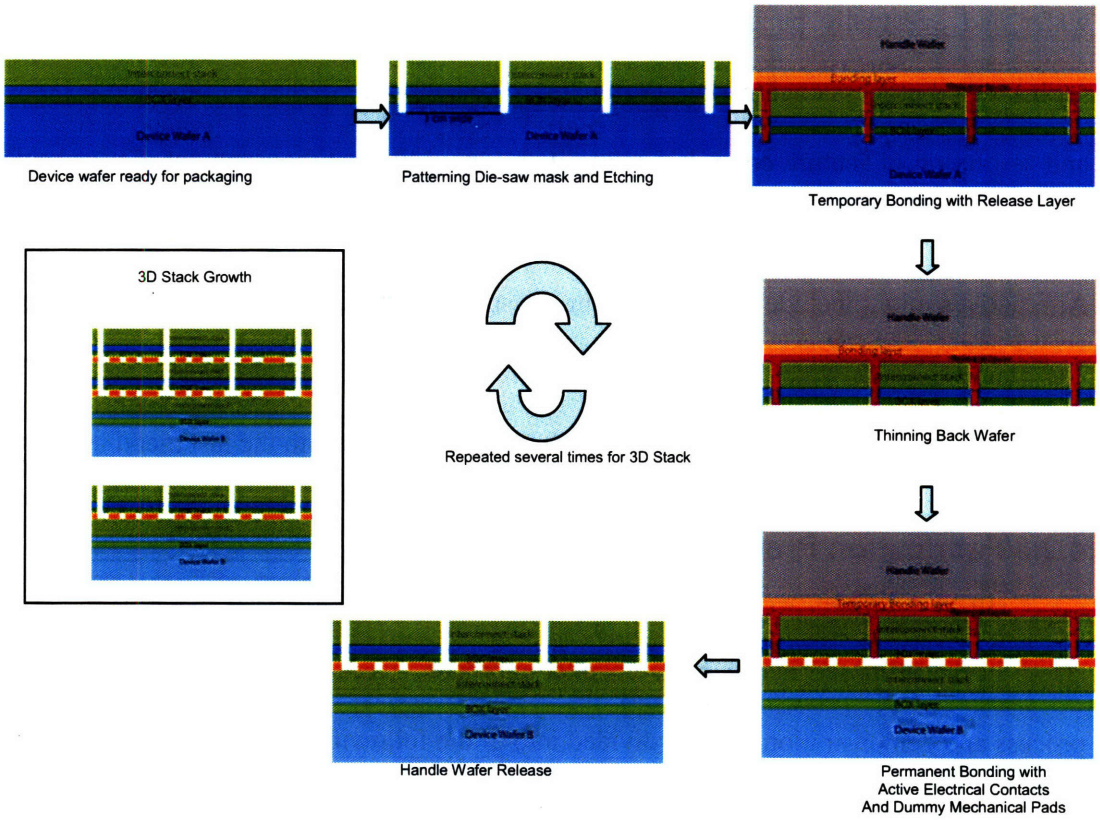


Figure 4.2: Integrated handle wafer process flow using a DBG-inspired approach. Box at the left shows the creation of a multi-layer 3D stack using the proposed DBG-inspired approach.

4.2.2 Additional Concerns

This section presents concerns or issues about the proposed integration approach. Die-saw streets do not contain any product devices or interconnects, given that this portion of the silicon wafer is destroyed during dicing. However, these die-saw street areas often contain test and monitoring devices, which are tested during fabrication and prior to packaging. If die-saw streets are etched before final test as we do in this approach, one might have to re-design or forego the dummy devices on the die, potentially leading to wastage of silicon area.

Another challenge concerns the development of a deep composite etch, in which several layers of dielectric are etched (Mn to M1) followed by etching into the silicon

wafer and eventually punching through to the buried oxide layer. This may require sophisticated process engineering. Fortunately, the lateral dimension of this etch is large, and resolution of feature control in non-critical. In addition, lithography at the backside of the wafer can be quite complex, as there is likely to be significant topography present. Alternatives might include Cu-nail structure as suggested by IMEC [64], or to etch super-vias (large through-wafer vias) at the same time as between-die channels. One can fill these super-vias with copper in step 2, and then connect them with the last metal layer.

4.2.3 Fabrication Procedure at MIT

In this section, we describe in detail the series of steps used to fabricate a 3D stack, in the proposed between-die channel approach. The fabrication of our prototype process and demonstration stack is divided into of the following steps:

(1) Fabrication of dummy device wafer

a. Dummy BOX layer and interconnect stack

b. Patterning and etching of between-die channels

c. Release layer deposition

(2) Fabrication of handle wafer

(3) Sacrificial bond formation

a. Deposition of bonding layer

b. Bonding

(4) Thinning

(5) Permanent bond

(6) Handle wafer release

(1) Dummy device wafer

Device wafer fabrication can be divided into three parts: deposition of dummy SOI layer interconnect stack fabrication, patterning and etching of the between-die channels, finally, the thick metal sacrificial layer is also deposited.

Dummy BOX layer and Interconnect stack

150 mm Si (100) wafers are cleaned using an RCA bath. The RCA clean can be divided into three steps, SC1 (5:1:1 H_2O:H_2O_2:NH_4OH solution for 10 minutes at 80°C) to remove organic contaminants (such as dust particles, grease or silica gel) from the wafer surface; HF dip (using a diluted 50:1 H_2O:HF solution for 1 minute) removing any oxide layers that may have built up; and finally SC2 (6:1:1 H_2O:H_2O_2: HCl solution for 15 minutes at 80°C) to remove any ionic or heavy metal contaminants. The RCA clean is a batch process in which 50 wafers can be cleaned at once. A 500 nm thick SiO_2 layer is then grown on the cleaned silicon wafer using a wet oxidation process. A mixture of H_2, O_2, and N_2 is used in an atmospheric tube furnace for 90 minutes at 1000°C.

LPCVD poly-silicon is deposited on the thermal oxide to complete the dummy SOI wafer. A 250 nm thick poly-silicon layer is deposited in a tube furnace at 625°C by pyrolysis of silane (SiH4) gas flowing at 150 sccm at 200 mTorr, with a deposition rate of 10 nm/min. In order to simulate the interconnect stack, 4 μm oxide is deposited using an Applied Materials Centura, which is a high density plasma CVD tool. The oxide is deposited using silane and nitrous oxide at high pressure, with a substrate temperature around 400°C. The deposition rate is approximately 1 μm/min.

Patterning and etching of between-die channels

The between-die channel mask is a simple grid mask with dimension of 1 cm x 1 cm, with 200 μm wide channels. A soda-lime glass mask is prepared in-house using chrome plates. In this case, we have assumed that scribe or between-die channels are 200 μm wide; but in reality these channels should match scribe line or die-saw street dimension which are same in size. The thick positive resist AZP 4620 (Clariant) is coated on the dummy device wafer stack using a manual coater at the speed of 3.5K rpm, which yields an 8 μm thick resist, which was followed by an hour bake at 90°C. An EV620 Mask Aligner is used to expose the coated wafers using the between-die channel mask. The exposure system uses a 350 watt high pressure mercury lamp with wavelengths ranging from 365-405 nm at constant power (10-mW/cm^2/sec). Because it is the first mask, no alignment is required. Wafers are exposed for 20 seconds in soft contact mode. The pattern is developed using AZ 440 (Clariant) in under 3 minutes and then rinsed vigorously in water. This was followed by post-bake of 30 minutes. Patterning is one of the most critical unit-steps to ensure the success of handle wafer release.

The oxide is etched in a magnetically enhanced reactive ion etcher, Applied Materials P5000, using CHF_3 (45 sccm), CF_4 (15 sccm) and Ar (100 sccm) at pressure of 200 mTorr with 600 watts and 30 gauss. The etch rate is approximately 400 nm/min; thus it requires 10 minutes to etch 4 μm oxide (dummy interconnect stack). LPCVD poly-Si was etched using Cl_2/HBr (20/20 sccm) at 200 mTorr and 350 watts with 50 gaussand requires three minutes to etch 250 nm poly-Si. Buried oxide is etched again with the same recipe described above. The surface technology system (STS) mutiplex ICP tool is used to etch 4-5 μm silicon, using the Bosch process of time multiplexed deep etching (TMDE) to achieve high aspect ratio etches. This process utilizes an etch cycle flowing

of only SF_6, then switching to a sidewall passivation cycle using only c-C_4F_8. During the subsequent etch cycle, the passivating film is preferentially removed from the bottom of the trenches using ion bombardment. A constant pressure recipe is used to obtain more repeatable and uniform results. After etch, the remaining photoresist and polymer deposited during etch is stripped in a barrel asher at 1000 watts for 4 hours. This is followed by a piranha (H_2O_2:H_2SO_4 in1:3 volumetric ratio) for 10 minutes, to make sure that all organic material is removed.

Deposition of release layer

After the clean, 100 nm thick titanium film is deposited, followed by an 8-10 μm aluminum layer, follows using the Applied Materials Endura sputter system. In order to deposit 8 μm thick Aluminum, a 1 μm deposition recipe is used multiple times without breaking the vacuum. Sputtering can heat the substrate and the wafer chuck in the chamber, so it is desired to include a cooling down period in between consecutive Al deposition runs. In our design, Al is sputtered over the device wafer instead of the handle wafer, because the release layer needs to be exposed to a chemical reagent after thinning and after the permanent bond is formed.

(2) Handle wafer fabrication

In our initial prototype experiment, the handle wafer is a blanket wafer with no pattern. The handle wafer is a 150 mm test quality silicon wafer with 0.5 μm wet oxide grown on the surface. In experiments here, the handle wafer oxide is grown at the same time as the dummy device wafer oxide growth.

(3) Sacrificial bond formation

The sacrificial bond formation is accomplished in two steps. The first is bonding layer deposition, and the second is copper thermo-compression bonding.

Deposition of bonding layer

Both the handle wafer and the dummy device wafer are mounted in an electron beam (e-beam) deposition system (Temescal / BOC Edwards) using a planetary configuration to deposit 50 and 100 nm of tantalum followed by copper, at a pressure below than $2x10^{-6}$ Torr. The usual deposition rate for Ta is around 12-nm/min, while Cu is deposited at approximately 18-20 nm/min.

The e-beam deposition is not very conformal because it can only deposit in a line of-sight fashion from the target. It is very much desired to have conformal deposition, as we do not want the aluminum beneath the copper to be exposed during TMAH etch back, which attacks Al vigorously. Thus, 250 nm copper is deposited on both the handle wafer and the dummy device wafer, using the Perkin-Elmer sputter system at a pressure less than $3x10^{-6}$ Torr and 2 KW. The sputter usually has a very high deposition rate (70 nm/min), and because of the high pressure during deposition it gives a more conformal deposition covering the edges of the patterned channels. The Perkin-Elmer deposits metal using a DC magnetron to strike Argon plasma and which sputters the target material onto wafers, which are placed on a rotating table for better uniformity. It has been found that thermo-compression copper bonding is dependent on the technique is used to deposit copper. Ideally, both bonding substrates should have a similar copper film, in order to match the grain size and the roughness of the deposited copper and facilitate bonding.

Copper bonding

Thermo-compression copper bonding has been the core of MIT's 3D IC technology. The copper-bonding work reported in this thesis, as well as earlier works performed at MIT, has been conducted on Electronic Vision Group (EVG) EV 501. The schematic and image of the wafer bonder is shown below in Figure 4.3. An early work by Fan, [58], reported that a 100 mm wafer with 300 nm thick Cu can be bonded to another 100 mm wafer with 300 nm thick Cu layer at 400˚C in 30 minutes, with applied pressure of 4000 N. Chen et al. [60] further studied the morphology and bond-strength of copper wafer bonding, by investigating the bonding interface using of transmission electron microscopy (TEM). Chen studied the bonding temperature and annealing time, establishing 300˚C as the minimum temperature required for bonding. Fan realized that to ensure reliable and repeatable thermo-compression bonding, there are more than just two parameters, including wafer-bow, and tool parameters such as dialed distance and diffuser calibration, that are important.

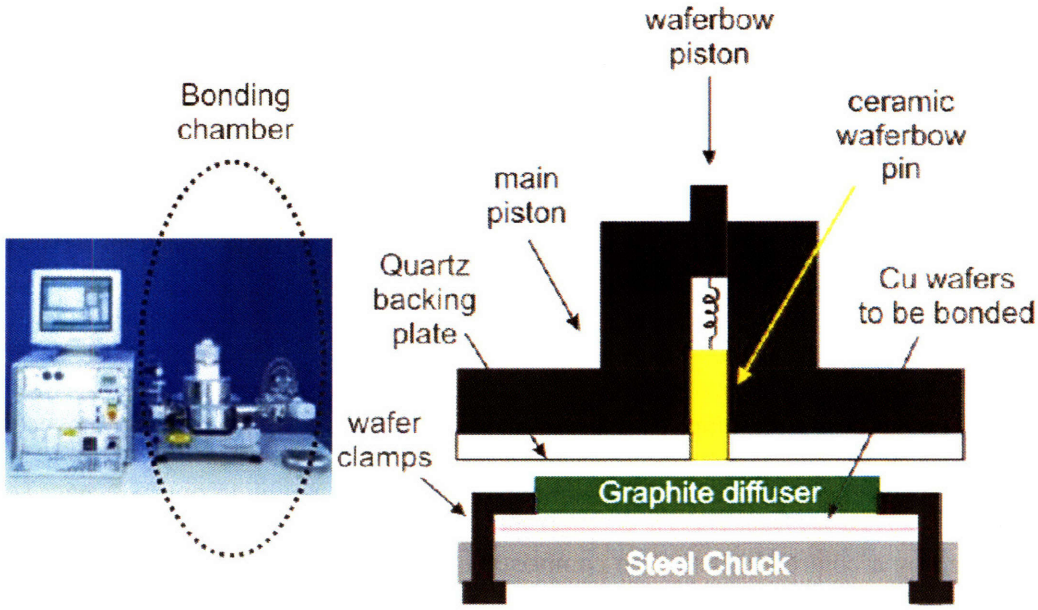


Figure 4.3: Photo of EVG 501 bonder, and schematic cross-section [58].

In this thesis, thermo compression bonding for a 150 mm wafer is carried out at 350°C for one hour with an applied force of 6000 N. In all experiments, we use a graphite diffuser to achieve uniform and repeatable bonding. In this case, wafers need not be aligned, so the wafers are stacked and inserted in the chamber, as show in the Figure 4.3, with metal clamps in between the two wafers. The wafers are then purged cleaned with N_2 and pumped down to 1 mTorr, followed by the removal of the clamps and application of a higher force of 3000 N. At this stage, the heater is turned on to reach the desired top and bottom chuck temperature (heating up to 40°C/min), at which point the piston is pushed further down with 6000 N for one hour. The bonded stack is removed from the bonder once it cools down to room temperature and is annealed in a furnace for one hour at 400°C. Figure 4.4 shows a schematic of the bonded stack, with the aluminum release layer buried beneath the copper bonding layer.

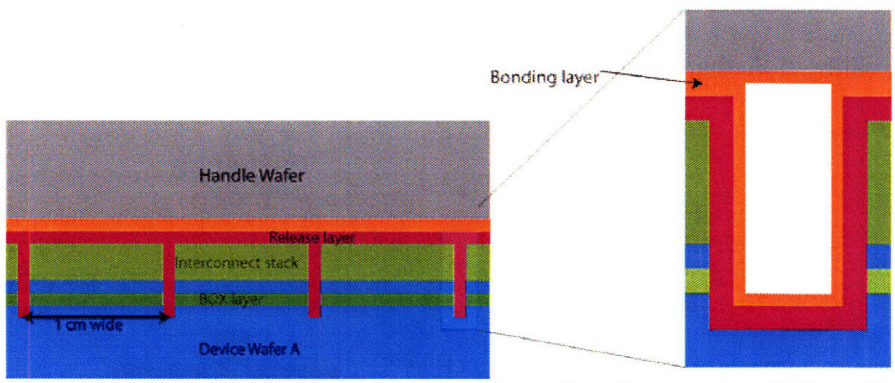


Figure 4.4: Schematic of handle wafer bonded with device wafer using copper and Al as release layer with between-die channel lines.

(4) Thinning of bond stack

For in-house thinning, back-side poly and thermal oxide layers are removed from the dummy device wafer in the STS etcher using isotropic etch with only SF_6 gas. This is followed by a controlled bath etch comprised of 1:2 tetra-methyl ammonium hydroxide: water (TMAH: H_2O) maintained between 80-90°C. The approximate etch rate for this

mixture is 1 μm/min. This chemistry has a very good selectivity for oxide and nitride films, and this etch stops at buried thermal oxide layer. The between-die channels are exposed and the device wafer now consists of individual dies with 200 μm wide channels between each die. The aluminum layer is protected by the conformal copper deposition until the dies have been thinned back. Once the dies have been thinned, the aluminum layer is exposed, as shown in Figure 4.5 (a). Figure 4.5 (b) shows the schematic cross-section of three layer bonded stack with handle wafer and two-device layers bonded with permanent bond and die-channel.

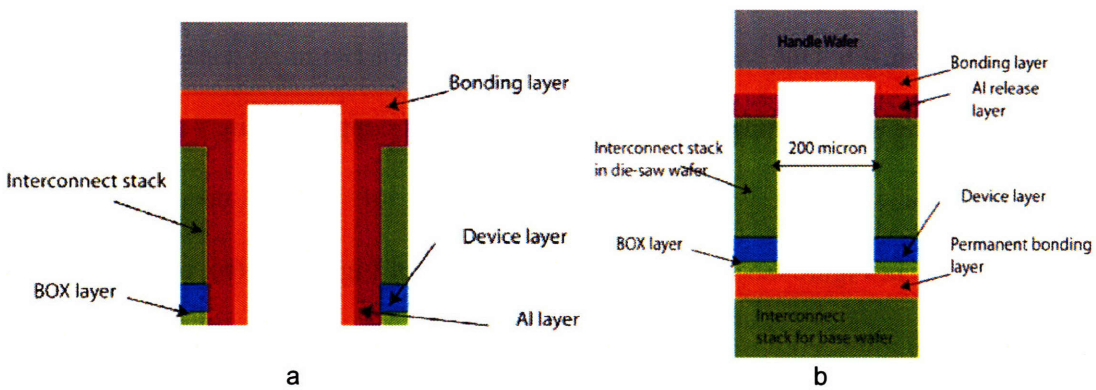
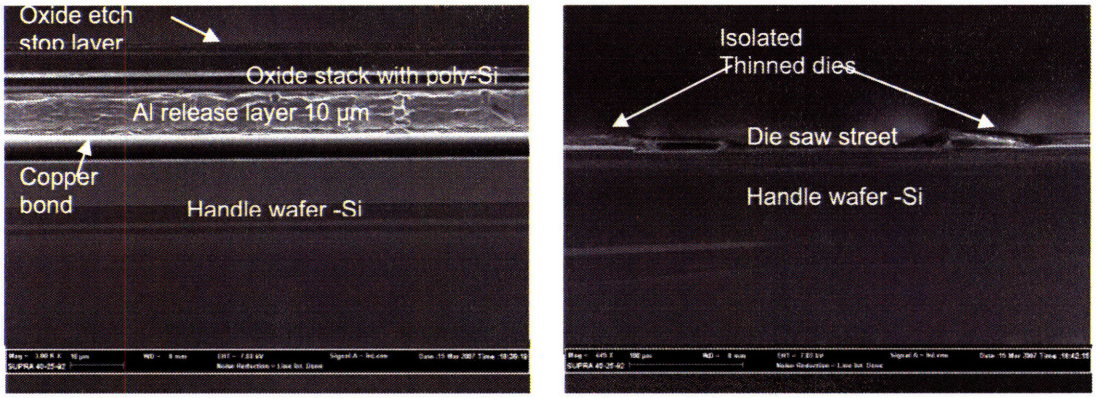


Figure 4.5: a) Schematic of thinned wafer. b) Schematic of three layer bonded wafer with between-die channels.

The back-side silicon is observed to etch etched non-uniformly because of the non-uniform heating of the bath. This causes widening of some of the between-die channels as part of the wafer still has some silicon remaining, while other parts are over-etched. After back-side silicon etch wafer is cleaned extensively using a spin dryer, followed by an organic clean using acetone, methanol and iso-propanol, so that no TMAH marks are left on the oxide. Figure 4.6 shows a photo of etch back using TMAH, depicting the problem resulting from non-uniform etch back. The wafer was cleaved to obtain a cross-sectional SEM sample.

Figure 4.6: Non-uniform partial etch back of dummy device wafer using TMAH.

Figure 4.7 (a) shows a cross-sectional SEM obtained from the thinned wafer shown in Figure 4.6. One can observe a thinned die with a 10 μm Al release layer and a 5 μm thick oxide stack, bonded to the handle wafer with copper. Figure 4.7 (b) illustrates the between-die channels and shows the isolation of thinned dies as illustrated schematically in Figure 4.5 (a). By close examination of Figure 4.7 (b), one can observe the under-etch of the Al release layer at the edges of the between-die channel.



a b

Figure 4.7: Cross-sectional SEM of thinned wafer a) Thinned dies with Al release layer bonded to handle wafer using copper. b) Between-die channels and isolation of dies by thinning.

(5) Permanent bond using copper

At this stage, a real device wafer would undergo contact and via patterning and formation. In our experimental demonstration, there are no active circuits so no

lithography is needed. The blanket tantalum followed by copper layers, 50 and 300 nm thick respectively, are deposited on the back-side of the dies using an e-beam system. The dummy device wafer B is also deposited with the same stack. At permanent bonding stage, it is desired not to have a conformal copper layer, since the handle wafer needs to be released in a later step.

The back-side of the thinned dies (5-8 μm thick), which are stacked on the handle wafer is bonded to the front-side of dummy device wafer B, using EV 501 with the same recipe as described earlier. The three-layer stack is annealed at 400°C in a batch furnace for half an hour, in order to make sure that the permanent copper bond between die and device wafer B is strong.

(6) Handle wafer release

The dies can now be transferred to the device wafer B, and the handle (transfer) wafer is released. Aluminum can be etched very selectively with hydrochloric acid (HCl) if the temperature is less than 80°C. A mixture of H_2O: HCl in a 1:1 ratio is heated to 60°C using a hot-plate, and the wafer stack is submerged in the release bath. The 200 μm wide between-die channels aid in the release process. As soon as aluminum starts reacting with HCl, hydrogen is released and many bubbles are visible as they come to the surface. Ultrasonic agitation is employed periodically to remove copper debris, and to aid in removing H_2 bubbles so as to create pathways for incoming acid.

Characterization

For characterization purposes, wafers are visually inspected to see if the device dies are transferred or not, and then cross-sectional SEM is conducted using a focused ion beam-SEM (FIB-SEM) technique [126] or in-house e-SEM for more detailed analysis of

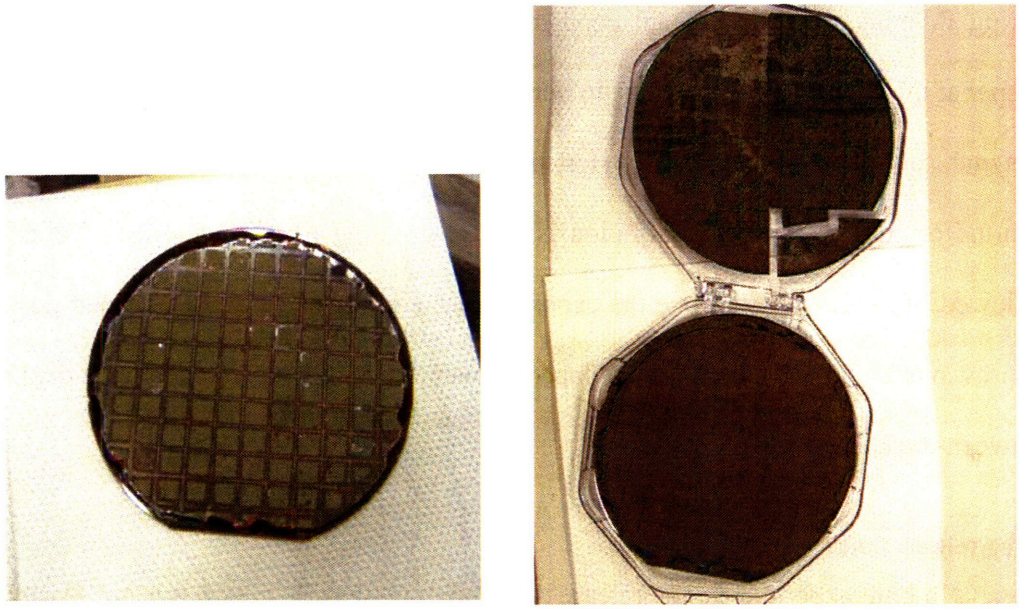
film stacks. FIB-sample shown here are prepared at Materials Analytical Services, in Raleigh, NC.

4.3 Results and Discussion

In this section, we first will prove that creating channels in the laminate structure helps and improves the release process. It is followed by observations and explanations. Secondly, we will conduct a full process flow to observe the integrity of the structure, along with providing some concerns. Then we will discuss the change in design to make this whole process more efficient and robust.

4.3.1 Initial Results

In the first phase, the concept was proven by following the full process described in section 4.2.3. The dummy stack was not fabricated to reduce the complexity and processing time. Figure 4.8 (a) shows an image of thinned dies bonded to a handle wafer. The bright shiny areas are aluminum beneath 0.5 micron buried oxide layer, which is an effective die area. Next, the wafer shown in Figure 4.8 (a) was bonded to another blanket wafer with Ta/Cu (50/300 nm) stack on 0.5 μm oxide, using the copper bonding recipe. The bonded wafer stack was soaked in a $HCl:H_2O$ with 1:1 solution at 60°C, and required approximately three days (72 hours) for this handle wafer to be released. An ultrasound bath was not used, but the glass container was manually agitated from time-to-time in order to help remove the copper debris and H_2 bubbles trapped inside the channels. The released wafer can be seen in Figure 4.9 (b), which was cleaved in order to extract the sample for cross-sectional SEM.



a b

Figure 4.8: a) Thinned dies on the handle wafer. This wafer was reflecting because of 10 μm of Al . b) Pair of released wafers: bottom is the handle wafer, and top is the wafer with thinned dies.

4.3.2 Observations and Discussion

In this section, the initial results are summarized in order to understand what are the primary achievements and limitations of the between-die channel approach and what can be done in order to further improve this approach. The initial experiments demonstrated that Al can be used as a release layer, using the suggested laminate structure with the patterned between-die channels and also enabled us to make additional observations as discussed below.

Widening of between-die channel streets

In Figure 4.8 (a), one can observe that the between-die channels have become broader than desired 200 μm, which consumes more silicon device area than desired. Another trend is that the channels are far wider at the edge of the wafer than at the center. These two facts can be attributed to TMAH attacking the Al release layer. In this experiment, conformal copper was not deposited, which is capable of protecting Al

during thinning than the e-beam deposited copper layer used here. The channels are deeper at the edges of the wafer due to non-uniform DRIE etching as well as non-uniform wet etch. In addition the TTV of wafers used here was 15 micron which results in more non-uniformity. One possible solution is to use grinding for the majority of thinning, followed by wet etch, to reduce the exposure of the wafer to TMAH. A second possible improvement is to use a conformal copper deposition along with a smaller etch depth for between-die channels.

Long release time

In both experiments, the release required more than 24 hours. It is not feasible to have a unit process in manufacturing that takes this much time, so we need to optimize the recipe to improve the release time. The release time can be a function of the number of channels, how wide they are, and how deep they are. It can also be argued that if we change the chemistry or add some surfactants to decrease the surface tension of the solution, then we may be able to decrease the release time. In previous release work, Fan found that H_2 bubbles and copper debris are two major bottlenecks for handle wafer release. We also found that defect free lithography, is important to ensure that all channels are open and the aluminum is exposed to the HCl solution. In the next set of experiments discussed later in Section 4.3.3 and 4.3.4, an ultrasound bath was applied intermittently, and, at the same time increased channel depths are explored.

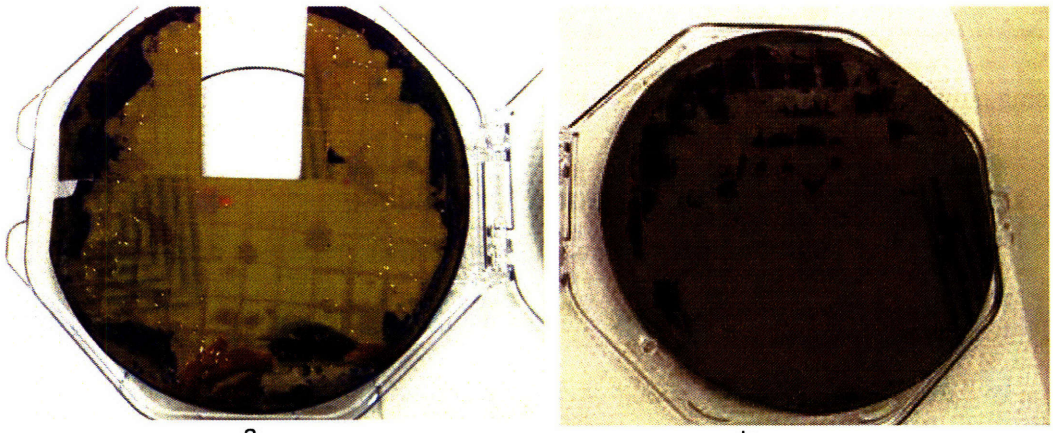
Low yield at wafer edges

It can be perceived in Figure 4.8 (a) that, after thinning down in TMAH the edge dies on the wafer are lost. After bonding and releasing, the overall yield for edges is very low as shown in Figure 4.8 (b). The primary reason for low yield is long exposure to the

TMAH and HCl acid bath. The solution is again to reduce the exposure to TMAH by using a mechanical grind back and reduce the release time by using other approaches.

4.3.3 Ultrasound Agitation Results for Release

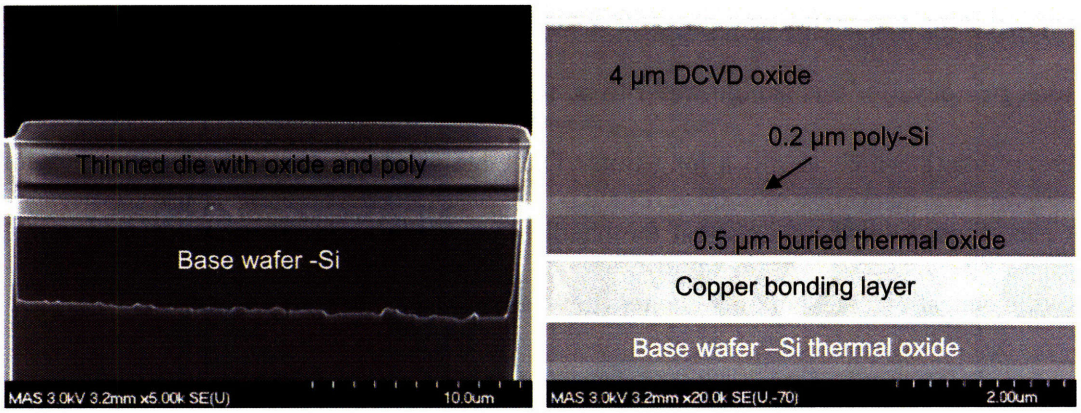
In the second set of experiments, full fabrication process as described in 4.2.3 is applied; the poly-Si layer is also deposited on the dummy device wafer. In Figure 4.9 (a), one can see dies bonded to a second device wafer, and Figure 4.9 (b) shows the released handle wafer. The dies were successful transferred to the substrate wafer (as indicated by the green color in Figure 4.9 (a)). In this experiment, we monitored and agitated wet etch more actively in order to obtain a more uniform etch by changing the orientation of the wafer and by stirring the TMAH solution, from time to time during the etch. There was no over-etching thus we prevented the widening of between-die channels. During this release process, we also employed ultrasound intermittently. The ultrasound bath did not have any active heating, so it was never applied for more than 5 minutes, to avoid reducing the temperature below 60°C which would lower the reaction rate drastically. It took two days for this handle wafer to be released (compared to three days in the second experiment), which is still a long time. The edge yield appears better than in previous cases. Figure 4.9 (b) shows that the handle wafer is left with Ta thin film and thermal oxide beneath it. The bonding copper film was removed along with aluminum.



a b

Figure 4.9: Successful handle wafer release of full dummy wafer stack. a) Released wafer with dies. b) Released handle wafer.

The device wafer stack with die in Figure 4.9 (a) was cleaved for cross-sectional SEM. Figure 4.10 (a) shows the FIB cross-section of the released die on the base wafer, where we see back-to-face dies bonded to the base wafer using copper. The poly-silicon layer and 4 μm thick oxide stack was intact, indicating that process is robust and stable (Figure 4.10 b).



a b

Figure 4.10: FIB- SEM of cleaved sample from Figure 4.9(a). a) Thinned die bonded to base wafer with copper which has been released from the handle wafer. b) Layer transfer depicting oxide and poly layers using FIB.

4.3.4 Between-Die Channels in Both Device and Handle Wafers

The release time is a primary concern and, as discussed earlier, the channel depth is a major factor affecting this time. In the above approach, the channel depth is set by the thickness of Al and oxide interconnect stack (10-15 μm). This section, we explore a modification enabling deeper channels by creating channels in the handle wafer that are a mirror to the between-die channels formed on the device wafer. These handle wafer channels will provide the option of increasing the channel depth, as illustrated in Figure 4.11.

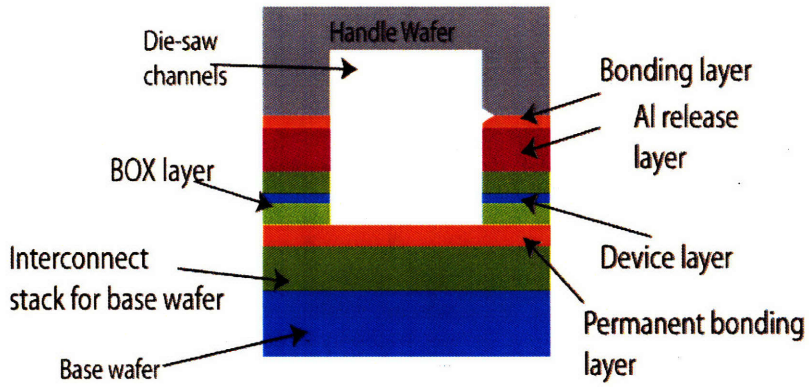


Figure 4.11: Modified stack with between-die channels also formed in the handle wafer.

The process flow remains the same as before for the device wafer. The pattern and etch of the handle wafer channels is done by using a mirror mask to the device channel mask (in our case, the same mask is used since it is symmetrical). Channels are etched and then cleaned with piranha rigorously, followed by RCA for wet oxidation to form a 0.5 μm thick oxide. At this stage, the handle wafer can be integrated with the previous process flow. One now needs to align the handle wafer and the device wafer, so that the channels overlap. Aligning the device wafer with 10 μm thick aluminum layer becomes challenging, as this film has a high tensile stress, which causes high wafer bow.

The wafer bow was measured to be 117.25 μm by Fan [58] for a 6 inch PMOS wafer with 10 μm Al laminate structure.

Figure 4.12 describes the operation of the EV 620 aligner. It aligns the computer generated physical marks to the top wafer which is facing down, and then those marks are aligned to the back-side of the bottom wafer, which should be a dual-side polished (DSP) silicon wafer. Because of the large bow in the device wafer, the vacuum of the EV 620 is not able to hold the wafer; thus mounting the handle wafer on top, with the device wafer on bottom, is necessary.

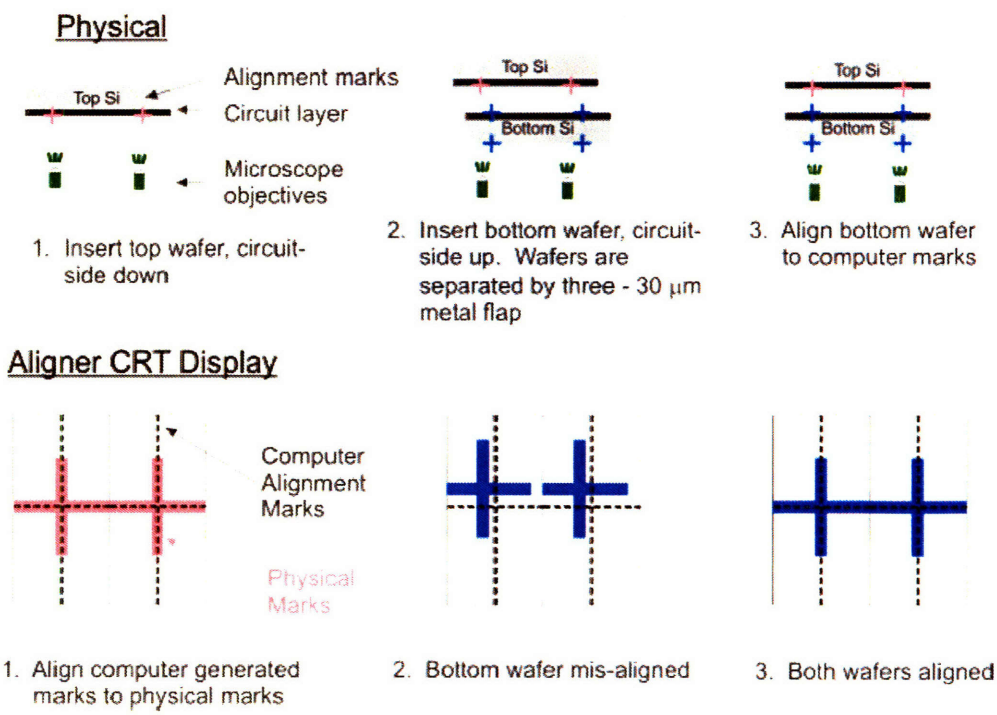


Figure 4.12: Wafer-wafer aligning protocol for EV 620 [58].

The handle wafer was etched for 15 minutes in STS resulting in 30 μms etch depth. The device wafer had 8 μm Al release layer above buried oxide 0.5 μm thick. The device wafer was etched shallow in silicon (1 μm), to avoid widening of between-die

channel streets. The stack was soaked in HCl: H2O (1:1 solution) and was immersed in ultrasound bath intermittently. The handle wafer was released in 8 hours. Figure 4.13 shows the photo of the released handle wafer (left) and dies transferred to base wafer (right). Both wafers have copper remaining, but upon inspection, it is found that dies were transferred as desired. Figure 4.14 shows the FIB-SEM of dies bonded to thinned wafer. It shows that the 0.5 μm thick oxide dummy device layer was successfully transferred using copper bonding to the base wafer. The copper bond has few voids at the bonding interface, probably because of the uneven etch back.

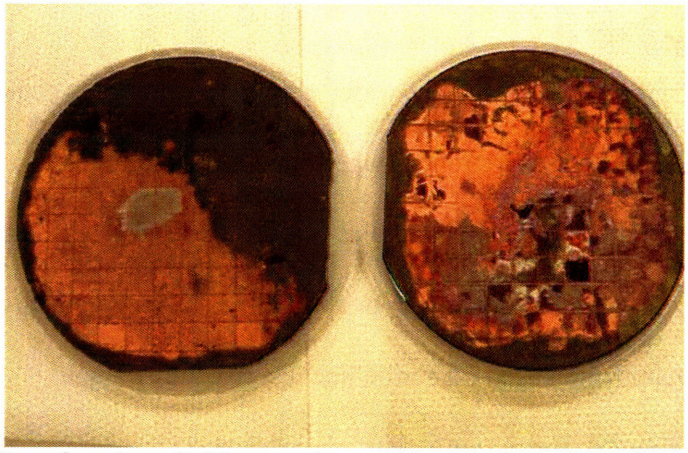


Figure 4.13: Handle wafer release in 8 hours using combined device and handle wafer channels. The wafer on the left is the released wafer; the wafer on the right is the substrate wafer with transferred dies.

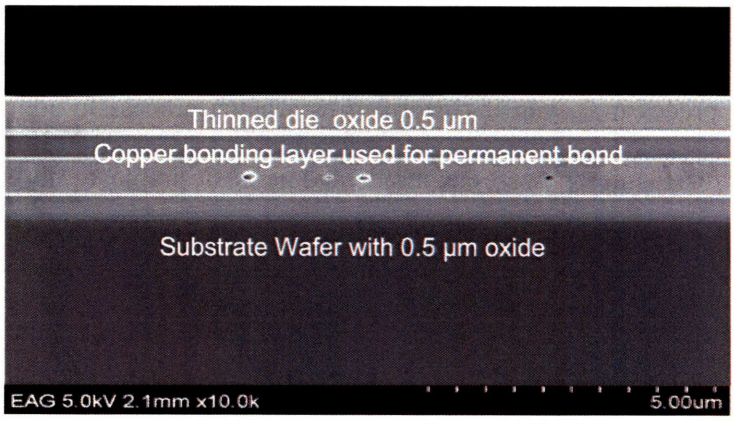


Figure 4.14: FIB-SEM of thinned die bonded to base wafer, released in 8 hours using the combined device and handle wafer channels.

The release using the combined handle and device wafer channel appears to be better and quicker than in the previous experiments. This integration approach can be optimized further, such as by using surfactants, increasing the soak temperature (up to 80°C) or adding some H_2O_2 or oxidizing chemistry which can reduce H_2 gas [63]. Another approach which may further decrease the release time is to increase the number of channels and the channel depth on the handle wafer. Besides decreasing the release time, another variable that requires optimization is the aluminum (release layer) thickness; the 8 μm thick is still very expensive in terms of energy.

4.4 Summary

In this chapter, a novel handle wafer approach using between-die channels has been demonstrated. By using a strong copper bond and an aluminum release layer with high modulus, thinning is very reliable and repeatable. Using between-die channels in location typically occupied by a die-saw or scribe lines has a potential drawback; in that kerf area is lost that is often used for scribe line test structures.

Results for the proposed handle wafer release were presented. The shortest time required to release the handle wafer from thinned is approximately 8 hours, using the combined device and handle wafer between-die channels. This is a long time in terms of semiconductor processing, even if performed as a batch process In addition, aluminum thicknesses of 8-10 micron were required, and it is desirable to further reduce this thickness to minimize manufacturing cost and environmental impact.

Chapter 5: Handle Wafer Release: Oxide Release Layer

This chapter introduces a second sacrificial bond and release approach for use in the handle wafer release process. This approach is modeled after a MEMS approach that uses silicon oxide as the sacrificial layer. In the previous chapter, we illustrated an approach inspired by dicing before grinding (DBG), to resolve the problem of etchant diffusion for the handle wafer release steps by introducing between-die channels at the sacrificial bond interface. Even though between-die channels showed tremendous improvement as compared to a blanket aluminum release layer, the approach still takes eight hours to release the handle wafer. In the approach proposed in this chapter, deeper micro-fluidic channels are incorporated in the temporary bonding layer, and smaller spacing is used to further decrease the release time. In order to form channels with decreased spacing, the channels must be etched in the handle wafer alone.

The main objective of this chapter is to present a feasibility study for this novel approach, and to determine its environmental footprint. As in the previous chapter, a dummy SOI wafer is fabricated and used to demonstrate and evaluate the approach. In section 5.1, we provide an overview of the process in six steps, outlining the fabrication process steps for the proposed, oxide release layer, handle wafer approach. In section 5.2 through 5.7, we then present details and experimental results for each step of the process. Section 5.8 discusses the results of the integrated process, and finally, we will summarize the approach in Section 5.9.

5.1 Oxide Release Layer – Process Overview

The proposed handle wafer design discussed in this chapter uses a single material for both bonding and releasing. In this approach, we propose to use oxide-to-oxide bonding as the sacrificial bond, which can be selectively etched using hydrofluoric (HF) acid. Low-temperature oxide bonding developed by Chuan-Seng [57] will be employed, as this process will be performed in the BEOL and the maximum permissible temperature is 400°C. The bonding process involves cleaning and bonding at room-temperature, and then annealing at 250-300°C. Silicon oxide sacrificial layer etching has become a major MEMS surface micromachining method used to fabricate microsensors [131] and microactuators [132] often made of poly-Si. The various oxide etchants are based on HF such as concentrated HF, diluted HF, buffered HF, HF and HCl, vapor HF, pad etch and many others. Selectivity is the most important factor which enables one to choose among different possible etchants. The review article by Buhler et al. [89] contains a compilation of etch rates for different kinds of oxide using different possible etchants, along with their selectivity data.

For our study, the proposed handle wafer process can be divided into six steps as shown in Figure 5.1, and summarized below.

(1) Fabrication of handle wafer

(2) Fabrication of dummy device wafer

(3) Low-temperature plasma activated oxide bonding

(4) Wafer thinning

(5) Permanent bonding

(6) Handle wafer release

The first step of the process is to fabricate the handle wafer, which requires etching channels, and the second is to fabricate the dummy device wafer. These steps may be done in parallel. This is followed by temporary bonding of the oxide layers. The fourth step is thinning the device wafer using the support wafer (using grinding/wet etching). In the fifth step, a permanent bond is made between the back-side of the thinned wafer and the face side of another device wafer. In step 6, the handle wafer or the support wafer is released.

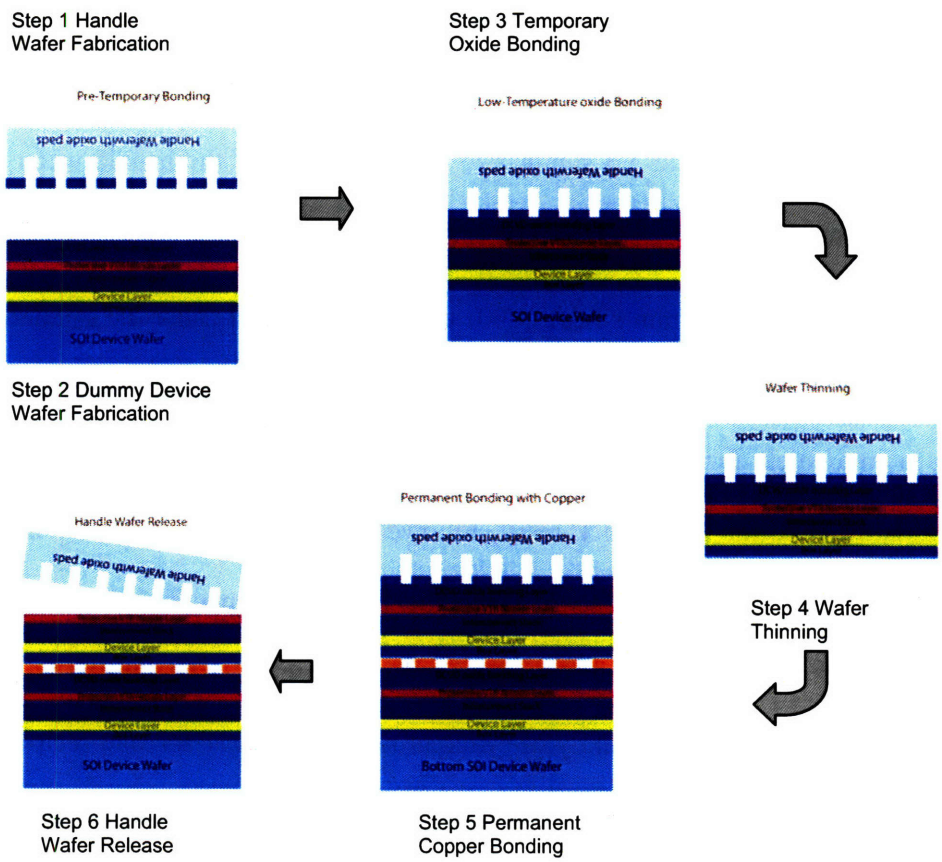


Figure 5.1: Six steps for oxide release layer approach.

In Section 5.2 through 5.7, we explore each step in detail, report an experimental evaluation, and identify concerns related to each step such as bond strength, stability during grinding, release time, and interconnect stack protection from HF acid.

As discussed in Chapter 3, there are six characteristics that determine the performance of the handle wafer process: bond strength, void formation, thinning capability, chemical stability, thermal stability and ease of debonding or releasing. These six characteristics are discussed in our analysis below, as appropriate.

5.2 Handle Wafer Fabrication

The key idea in the proposed approach is to fabricate many channels in the oxide bonding layer of the handle wafer, to provide the access for etchants in the later oxide release step. Figures 5.2 and 5.3 summarize the parameters of the handle wafer design and fabrication.

To begin with 150 mm silicon (100) wafers are cleaned using the standard RCA clean (as described previously in Section 4.2.3). A 0.5 μm thick wet thermal oxide is grown in an ambient furnace at 1000°C. Thick positive AZP 4620 resist is coated using the standard recipe for 8 μm thick resist, followed by prebake for one hour in a 90°C oven. The coated wafers are exposed using the EV 620 aligner to obtain the desired pattern of continuous micro-channels as depicted in Figure 5.2. The channel widths and spacing are varied to obtain a family of different mask. A similar EV 620 recipe is used as described in Chapter 4 to obtain the pattern. Figure 5.2 (b) shows a schematic of the top view of a wafer which has been developed using the mask shown in Figure 5.2 (a). In this study, we explore different mask sets with different pad and channel sizes, in order to observe how these parameters affect bonding and releasing. Five different mask-sets are

used: 80 μm pads with 40 μm channels; 40 μm pads with 20 μm channels; 30 μm pads with 30 μm channels, with 1 cm relief layer at the edge; 500 μm pads with 100 μm channels; between-die channel mask (200 μm wide channels with die-size of 1 cm).

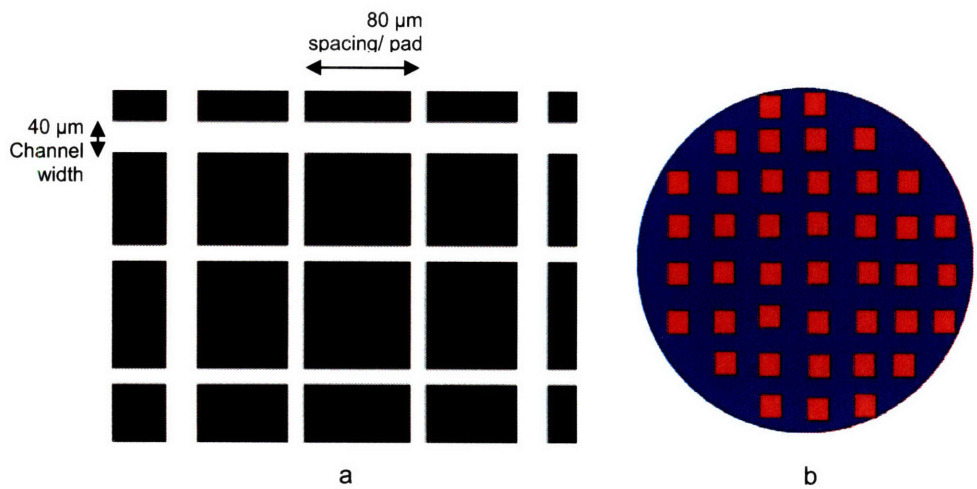


Figure 5.2: a) Magnified image of mask file. b) Illustration depicting mask on oxide wafer.

Resist-patterned wafers are immersed in buffered oxide etch (BOE) for 10 minutes to etch thermal oxide from the channels, and at the same time to remove the oxide from the back side of the handle wafer (Figure 5.3a). Patterning and wet etching using BOE is one of the crucial steps in determining the time of the release of the handle wafer process; this will be discussed in Section 5.8. The wafers are dump rinsed for at least 15 minutes and then spin dried to make sure that there is no HF remaining.

Following oxide etch, silicon channels are etched in a multiplex inductively coupled plasma (ICP) Surface Technology Systems (STS) etcher using standard Bosch process using SF_6 and c-C_4F_8. The recipe used for channel etching is the same as the recipe for etching between-die channels (described in section 4.2.3). The in-situ channel etch depth cannot be measured, therefore it was difficult to obtain a prescribed exact etch depth. Etch was timed, however, in order to achieve the same approximate etch depth for

each set of experiments. Even though the recipe is tuned in an effect to achieve a uniform etch rate across the wafer, the etch rate at the edge of wafer is almost 1.2 times greater than the etch rate at the center of the wafer.

The Bosch etch process for silicon uses alternating steps of etch and deposition, in order to obtain straight side walls, leading to large polymer deposition. The remaining photoresist and deposited polymer is stripped in a barrel asher at very low power (1 KW) for two hours. To enable oxide bonding surface cleanliness is imperative, so asher stripping is followed by a double piranha clean (3:1 H_2SO_4:H_2O_2). The handle wafer with its patterned oxide pads and open channels is then ready for bonding (Figure 5.3b).

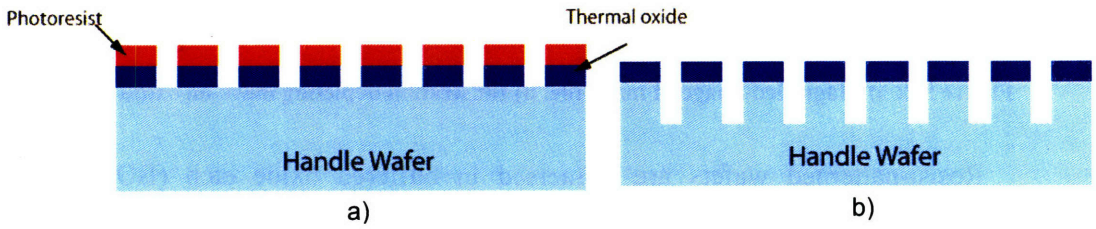


Figure 5.3: a) Patterned handle wafer with thermal oxide etched with BOE. b) Handle wafer after channel formation, ready for bonding.

5.3 Fabrication of Dummy Device SOI Wafer

A dummy device SOI wafer is fabricated by depositing 0.25 μm of LPCVD poly-Si at 625°C, on a top of 0.5 μm thick thermal oxide. The buried thermal oxide acts as the BOX and etch-stop layer. A 4 μm thick high density plasma chemical vapor deposition (HDP CVD) oxide is deposited on the dummy SOI wafer using an Applied Materials Centura 5200, which acts as a dummy interconnect stack for the device wafer. LPCVD silicon-rich-nitride (SiN) is deposited using a vertical furnace (VTR) at 600°C, which is again followed by oxide deposition of 2 μm by HDP CVD. The SiN layer acts as a sacrificial layer for the interconnect stack when the handle/support wafer is released

using HF. A 1 μm SiN layer can withstand concentrated HF acid for approximately 45-50 minutes [93].

The dummy SOI wafer is next polished using chemical mechanical polishing (CMP) for 60-120 seconds on a Strasbaugh (Model 6EC) polisher for 150 mm wafers. The slurry used is Cabot Microelectronics Semi-Sperse 25 E on Rohm & Hass CMP pads. The polish rate is approximately 20-30 nm/min. After CMP, the wafers are cleaned using piranha to (Figure 5.4) as oxide bonding requires a smooth and clean surface. The dummy device SOI stack is summarized in Figure 5.4, ready for bonding in the next step.

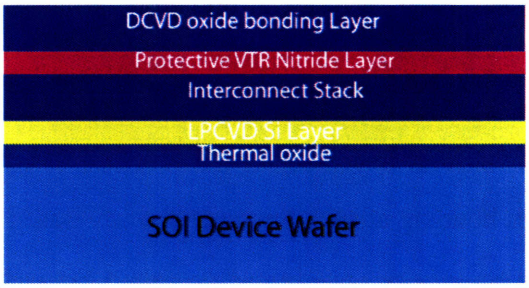


Figure 5.4: Dummy SOI wafer after CMP and ready for bonding.

The CMP step is included in our process flow to improve surface micro-roughness, which is a local, microscopic parameter of wafer surface quality and that is critical in wafer bonding. It is usually characterized by an RMS (root mean square) value measured using atomic force microscopy (AFM). It has been demonstrated experimentally that RMS less than 0.5 nm is adequate for oxide bonding [72],[86]. The average roughness of the 0.5 μm thick blanket thermal oxide used in this work is 0.16 nm calculated on 5 μm x 5 μm area. However, the blanket deposited films used to fabricate the dummy SOI wafer also adds to the roughness. A 2 μm DCVD oxide film deposited using the Applied Materials Centura 5200 has an RMS roughness value of 3.4 nm. Micro-roughness of these as-deposited wafers is too high for oxide bonding, thus

chemical mechanical polishing is employed for 60 seconds, which reduces the micro-roughness of a DCVD 2 μm thick oxide film to 0.4 nm, an acceptable number.

5.4 Low Temperature Plasma Activated Oxide Bonding

As mentioned earlier, temporary bonding will be used after BEOL processing in device wafers, so the processing temperature needs to no greater than 400 °C. Different chemical activation [57],[65],[140] has been reported to activate the oxide surface before bonding, but plasma has been the most effective. Numerous plasma processes have been reported for bond strengthening. The bond-strengthening influence of short plasma activation is clear and has been reported in numerous articles [65],[68],[69],[70],[71]. However, the mechanism behind this effect is still unclear. There are different explanations but one coherent observation is that plasma makes surface more hydrophilic [71],[73], which enables bonding at such low temperature. Based on the literature [57], it is known to be advantageous to have a short wet cleaning step between activation and bonding, and bonding can be achieved at room-temperatures and in an ambient atmosphere. The bonded stack is generally annealed afterward to strengthen the bond. Another set of factors that dominates the bondability is roughness of the bonding surface (as mentioned earlier), TTV and wafer bow [72],[83],[86].

In this section, we describe the process and parameters used in our bonding experiments. In this work, we bond pattern films to blanket films; patterned wafer bonding can be a concern because the bonded area is considerably less than in blanket to blanket wafer bonding. Therefore, we measure bond-strength for a variety of patterned oxide films.

5.4.1 Experimental Procedure for Oxide Bonding

We use a plasma activation process with the piranha clean process developed by Tan [[57]], using H_2SO_4: H_2O_2 (2:1). Oxygen plasma is used for 20 seconds in an Applied Materials P5000, magnetically enhanced reactive ion etcher, at 200 mTorr with 200 watts (DC bias voltage -200 V). O_2^+ ions and O_2 radicals interact with the oxide surface to make it more active [57]. Hydrogen peroxide-rich piranha has two purposes: first, is to clean any organic contaminants from the surface of oxide, and second, is to attach OH^- ions to the active surface to aid in formation of oxide bonds during wafer bonding.

All wafers used in this experiment are bonded in the Electronics Vision Group EV 620 under ambient atmosphere at room temperature. We find that bonding in a vacuum (pressure < 10^{-3} torr) has the same results as bonding in ambient. The wafers are pressed together using a waferbow pin, which pushes them together from center; pressure (1100 mbar) is then applied using a piston for two minutes. The bonding front moves from the center of the wafer radially outwards. The bonded stack is annealed in N_2 atmosphere at 250-300°C for 2-3 hours; this is based on the experience of Tan [[57]], who used a razor blade test to measure the bond strength determined that three hours allows enough time for the bond strength to saturate. Figure 5.5 shows a cross-sectional SEM of our bonded wafers.

The ability to bond patterned oxide pads is critical to our oxide release layer approach, because the oxide-oxide bond serve as temporary bond. For this reason, we have taken additional care to characterize the quality of our bonding step. In Section 5.4.2, we examine void possible formation using IR transmission imaging. In section

5.4.3, we perform bond strength measurements using chevron testing, for a range of oxide pads and channel sizes.

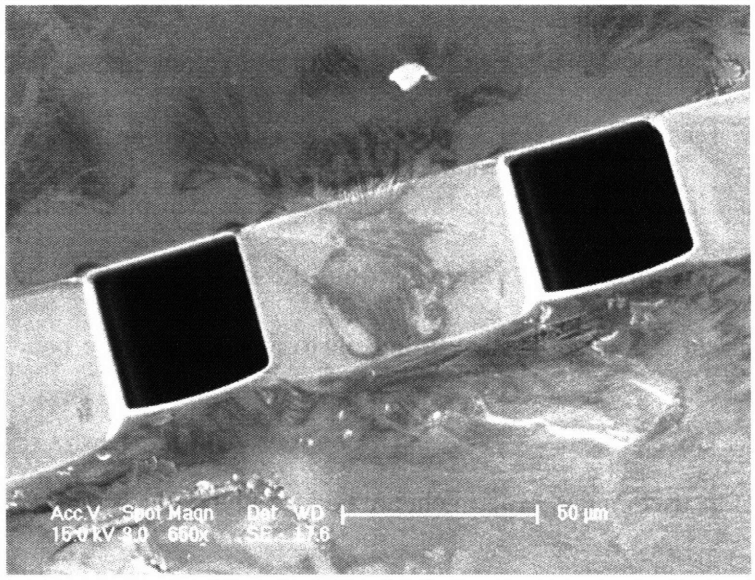


Figure 5.5: SEM cross-section of the oxide-bonded wafer with 80 µm pads and 40 µm channels. The handle wafer was etched for one hour to attain a channel etch depth of 45 µms.

5.4.2 Void Detection Using IR Transmission

For rapid investigation of the bonding quality, optical transmission is the most popular method. In principle, if the energy of incident radiant photons is less than the band gap energy of the material under the irradiation, then the photons can travel through the material without being absorbed. Areas that are not in contact form Newton rings, due to the interference of light reflected on the internal surfaces. The shape of the rings shows the shape of the delamination, and light and dark rings enable determination of the distance between unbonded surfaces [85].

If at least one of the bonded wafers is transparent, for instance glass, quartz, or sapphire, voids can be observed with the naked eye. For cases involving two silicon wafers, IR light ($\lambda > 1.1$ µm) and an IR camera are required. Heavily doped silicon,

however, is not transparent to IR light and therefore IR transmission is not suitable for wafer pairs with at least one highly doped counterpart. Figure 5.6 (a) shows an IR image of a bonded 150 mm silicon wafer pair with both wafers covered by blanket thermal oxide, a large void in the middle and edges is clearly seen with some small voids in other locations. To detect a void with IR transmission imaging, the void separated surfaces must be at least one fourth of a wavelength apart, and the lateral resolution typically is limited to about 1 mm. Figure 5.6 (b) shows a bonded pair composed of a wafer with pads bonded to a blanket oxide wafer. This bonded pair does not have any voids because of the presence of the pattern oxide channels, which help water and air molecules move out from the bonding interface during the bonding process.

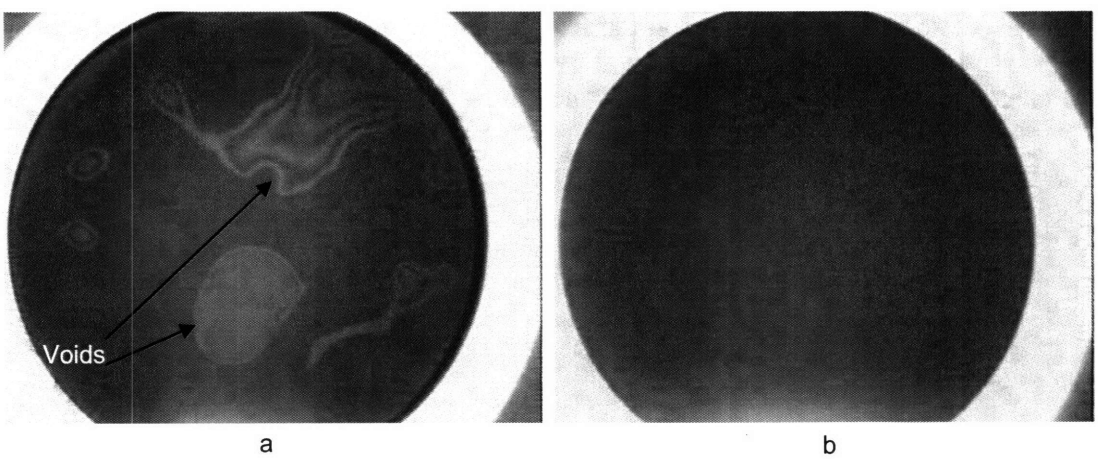


Figure 5.6: a) IR transmission image of a blanket thermal oxide bonded pair. b) Perfectly bonded oxide pair with pads on one wafer and the other wafer is having a blanket oxide layer.

5.4.3 Bond Strength Measurement

A common measure of bond quality is the mode I (tensile) fracture toughness, K_{Ic}, which is typically reported in the form of interface fracture energy, G_c. There are several methods available to measure bond strength including razor blade test [74],[75], blister test [75], tensile test [76],[79], and four point bend test [80],[81],[82]. In this work, we

utilize a novel chevron testing method, used by Bagdahn et al. for measuring directly bonded silicon wafers [77],[78].

The mode I interface toughness of SiO_2 fusion bonds is examined experimentally using a chevron test specimen, as pictured in Figure 5.7 (a). The surface of one wafer, or the interlayer, is patterned in the form of a V-shaped notch prior to bonding. The specimen is glued between two stubs that allow the specimen to be gripped and loaded in tension during the test. The sharp chevron tip serves as a stress-concentration point and enables characterization of both weak and strong bonds. Figure 5.7 (b) shows the top view of the chevron specimen. The loading line is different from the specimen edge due to the finite area along which the stubs are glued. This method is considered to be the most accurate measurement method for determining the bond strength. The measurement of maximum force is more accurate than measuring the crack length.

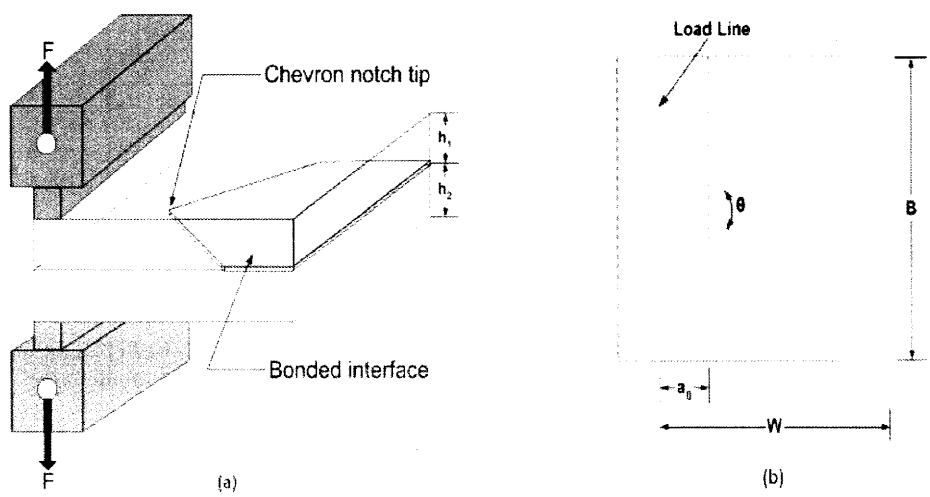


Figure 5.7: a) Schematic of chevron test specimen for bonded interface characterization. b) Plan view of a chevron specimen showing the geometry.

Fabrication of Chevron Structures

The fabrication of our chevron structure is quite simple. The process for fabricating our handle wafers is followed, but in this case at patterning step, handle wafer is double exposed with the chevron mask as shown in Figure 5.8 (a). When positive resist is exposed to UV light, it will clear the resist wherever light is exposed, resulting in patterned oxide pad structures remaining only under the chevron region. Since the primary goal is to understand the patterning effects, all other processing conditions, such as etch depth of channels and other bonding parameters are kept constant. The wafers are bonded to simplified device wafer, consisting of a silicon wafer with a 0.5 μm thick wet oxide grown on it. Figure 5.8 (b) shows the IR transmission image of a 150 mm bonded wafer. Each wafer is die-sawed using the Disco auto die-saw model DAD-H 6T into individual chevron structures, by dicing within the die-saw streets made on the mask. Care is taken not to damage the bonding interface.

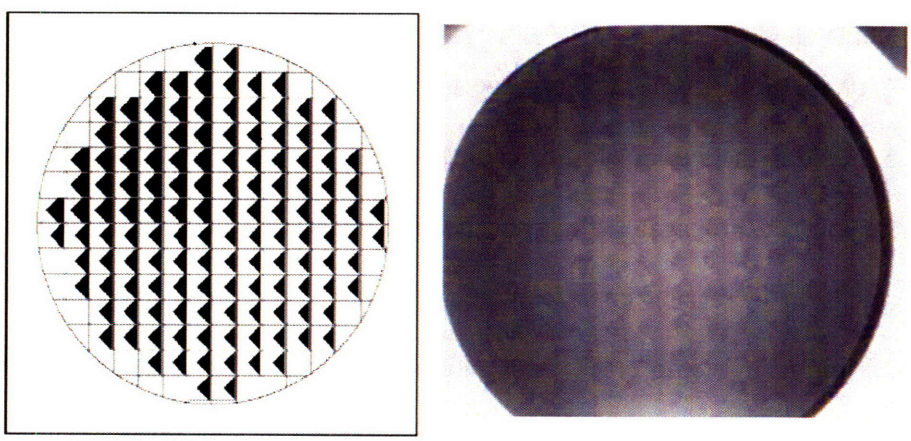


Figure 5.8: a) Schematic of 7" chevron mask for 6" wafer. b) IR transmission image of 6" wafer exposed to the chevron mask, along with 80 μm pads, and bonded.

Measurement

Test specimens from the bonded wafer pair are glued onto aluminum stubs using high-viscosity glue. Care is taken to prevent seepage of the glue into the bonded interface. Three different kinds of masks are used to understand the pattern size dependency, and approximately 12 specimens are tested for each geometric configuration. The specimens are selected to sample various regions on the bonded wafer. The glued specimens are then tested under tension in an Instron™ 8848 electromechanical universal testing apparatus. The specimens are loaded at a constant displacement rate of 0.12 mm/min. The load-displacement behavior is digitally recorded. After debonding, the specimens are dismounted from the stubs using acetone and the stubs are reused. Optical microscopy, scanning electron microscopy, and in some cases atomic force microscopy (AFM), and profilometry are used to characterize the fractured surfaces [84].

Results and Discussion

A typical load-displacement curve for a chevron-notched specimen is shown in Figure 5.9. After the initial elastic loading of the specimen, a crack initiates at the chevron notch and propagates along the bonded interface. The triangle-shaped bonded area provides an increasing interfacial area with increasing crack length and load, and initially resulting in stable crack propagation. At some crack length, the propagation becomes unstable and catastrophic failure of the sample occurs; this coincides with the point of maximum load in Figure 5.9.

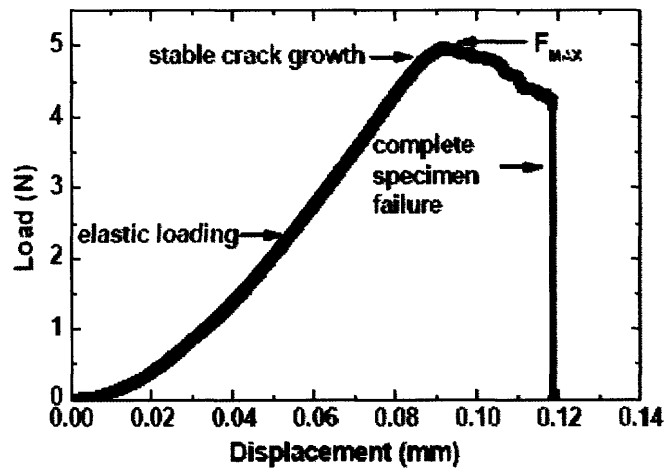


Figure 5.9: Typical load-displacement behavior from a bonded chevron test. The maximum force/load is used to calculate fracture toughness.

The critical stress intensity factor, K_C, at which failure occurs can be calculated from the maximum load in the test, F_{max}, using

$$K_c = \frac{F_{\max}}{B\sqrt{W}} Y_{\min} \qquad (1)$$

where Y_{min} is the minimum value of the geometry function, and B and W are the width and length of the specimen, respectively (as defined in Figure 5.7 b). Y is a dimensionless coefficient that varies with the crack length and is a function of the specimen geometry. Unstable propagation and catastrophic failure occur at maximum load, F_{max}, and the crack length that corresponds to the minimum value of the geometry function, Y_{min}. For plane strain the interface toughness, G_C, is related to the critical stress intensity factor by

$$G_c = \frac{1-\nu^2}{E} K_c^2 \frac{1}{A} \qquad (2)$$

where E and ν are the Young's modulus and Poisson's ratio of Si, respectively; and A is the area fraction of the chevron specimen that is bonded. It can be seen from Equations

(1) and (2) that the calculation of interface toughness from a chevron test requires the maximum load as from the experiments, as well as knowledge of the geometry and elastic properties of the specimen. Finite element (FE) analysis from [129] is used to determine the minimum value of the geometry function, which is dependent on the thickness of the bonded layers and crack geometry.

The correction factor is applied to all measurements depending on their pad size and spacing. As the crack is supposed to propagate in a straight line across the chevron structure, pattern density across the line serves as the basis for the correction factor, i.e,. (pad+spacing)/pad.

The results are tabulated in Table 5.1, summarizing the interface toughness for both center and edge regions of the wafer for different oxide pad patterns. At least four samples are tested from each part of the wafer to assess variabilities. In addition, 80 μm pad interface toughness is measured on three different wafers, to give us information about the wafer-to-wafer variance. We note that the patterned pads are smaller than designed, perhaps because of over exposure; the observed pad size and spacing is also shown in Table 5.1.

Pattern type	Designed Pads/ Spacing (μm)	Observed Pads/ Spacing (μm)	Area fraction (bonded)	Gc (corrected) ±sigma center (J/m^2)	Gc (corrected) ±sigma edge (J/m^2)
Blanket			**1**	**3.35 ± 0.19**	**1.94 ± 0.20**
Pads	**500/100**	**450/ 100**	**0.81**	**2.35 ± 0.35**	**1.94 ± 0.86**
Pads	**80/40**	**70/ 50**	**0.34**	**1.7 ± 0.22**	**1.64 ± 0.15**
Pads	**40/20**	**32/ 28**	**0.28**	**1.64 ± 0.26**	**1.53 ± 0.37**

Table 5-1: Interface toughness of different patterns measured using chevron test.

The edge value of bond strength for the blanket wafer is seen to be significantly different from the center value. To understand why the edge bonds are weaker than the

center bonds in the blanket films, we need to revisit how the oxide bond is formed in the first place. As described earlier in the EV 620 the center of the wafer is pressed first, then the whole piston is pushed with 1100 mbar pressure for two minutes. This means that bonding is initiated at the center, and the bonding front moves radially outwards. The edge can be weaker because, as the oxide bond forms water molecules are released, perhaps during annealing, and the water molecules from the center must travel towards the wafer edge, leading to additional moisture in the wafer edge. According to this theory, if we anneal the sample longer, the edge bond should become stronger; indeed we observe that the bond becomes tougher after annealing overnight. This observation contradicts the data from Tan [57], which showed that bond strength saturates. This can be explained by the difference in razor blade test and chevron test, the later has high resolution and can differentiate between smaller differences in bond strength.

In contrast to the blanket wafer bonding case, we see in Table 5.1 that the wafer center and wafer edge bond strengths are not (statistically) significantly different in all of our patterned pad cases. This suggests that the pad channels may provide a substantial benefit from the release of moisture or trapped gases during the bonding process leading to better within wafer uniformity

Another clear trend is the decrease in wafer center bond strength with deceasing bond area fraction. This drop in bond strength does not appear to be directly proportional to bond area; the 20% reduction in bond area from the blanket wafer to the 500 micron pad case corresponds to a 50% reduction in bond strength. This might be due to the patterning introducing sub-critical flaws proportional to the total perimeter around patterned features. The total perimeter per unit wafer is inversely proportional to the pad

feature size. Thus, flaws increase with decreasing pad size, resulting in lower bond strength. This result is quite significant, as it determines the minimum pad size that can be used for temporary bonding, as the wafer must provide a minimum bond strength to survive the mechanical grind back and post-thinning process.

Wafers with nominally zero bow (< 5 μm) are created by patterning the SiO_2 using a plasma (dry) etch rather than the wet etch in our normal flow, thereby ensuring that the backside of the wafers are covered by SiO_2. The bond toughness of wafers as a function of wafer bow is summarized in Table 5.2. The results show that wafer bows up to 30 μm over the 150 mm wafers did not have any effect on the bond toughness.

Wafer Bow (μm)	Bond Toughness (J/m^2)
5	2.77 ± 0.65
30	2.79 ± 0.59
Wafer thickness = 675 μm, Wafer diameter = 150 mm	

Table 5-2: Toughness as function of wafer bow.

Another set of experiments is conducted; in which patterned wafers are etched for 90 minutes instead of our standard 30 minutes etch, to yield 50 μm deep channels as compared to our standard 15 μm. For these experiments, all the 80 μm pad and 40 μm pad spacing (for channels) mask is used. The deeper channel wafers are found to have similar bond strength, i.e., 1.60 ± 0.2 J/m^2, as for shallower channels. This is significant result, as it shows that bond strength is independent of channel depth between 15 and 50 μm deep channels, and thus the handle wafer can be etched deeper for better and more effective wafer release in our later step.

Finally, both parallel and orthogonal line bond strengths have been studied to understand more about oxide bond toughness. Failure loci have been studied as well

using SEM to further understand details of crack propagation. The results and discussion pertaining to these studies can be found in [84], which details experiments conducted as part of this thesis research in collaboration with Rajappa and Thompson, at Department of Materials Science and Engineering, at MIT.

Trends Observed

Based on our experiments and characterization of plasma-assisted, low temperature oxide-oxide bonding, we can summarize the observed trends. Wafers with bow to 30 μm bow do not have significant effect on the bond strength. The channel etch depth between 15 and 50 μm does not significantly change the bond strength. There is a strong pattern size dependency, even after the correction factor is applied; this can be explained by the increasing number of crack initiation flaws with increasing perimeter for small pad sizes. Finally, the wafer center and edge bond strength is statistically different in the case of blanket films, but not in patterned films.

5.5 Wafer Thinning

In this section, we describe the thinning process proposed for our oxide release layer handle wafer process. Based on our experiments, we characterize two critical aspects of our thinning process, the chemical selectivity, and the thinning capability based on the mechanical stability of thinned films.

5.5.1 Experimental Thinning Procedure

In this study, our main objective is to thin the device wafer reliably, and to stop at the buried oxide layer. One of the main concerns in this experiment is stress-strain generated during and after thinning back. Wafer thinning is conducted in two stages: 1) mechanical grinding [88], and 2) selective thinning using chemical methods.

Our oxide-oxide bonded wafers are sent to an outside vendor named Silicon Valley Microelectronics, for grind back. Dummy device wafers are usually thinned to 100 μm ± 2 μm. We found that more aggressive grind-back can lead to far deeper silicon damage and can result in chipping. In severe cases, grind back may lead to debonding. Grinding back to 100 μm is a good compromise; the grind back serves as a good test for bond strength and, at the same time, is an effective way to remove substantial silicon prior to chemical thinning.

For the tinning step, two approaches were explored. In the first approach, we applied conventional fluorine-based dry etching in an STS ICP chamber using the buried oxide layer as an etch stop. The results were not promising, as the dry-etch is found to be selective to oxide but not selective enough because argon ions during silicon etch can sputter the oxide. In addition, the etch rate at the wafer edge is found to be far greater than at the wafer center. Because of non-uniformity and selectivity concerns, a second approach was developed using a TMAH wet etch. TMAH is mixed with water in the ratio of 1:2 and then heated to 80-90°C using a hot-plate. The bonded wafers are immersed in the heated bath. The etch rate is 1 μm/min for a 6-inch wafer, and the temperature needs to be monitored because selectivity decreases drastically at high temperature. The chemical selectivity for this process is a critical parameter, and is discussed in more detail next.

5.5.2 Chemical Selectivity

In the case of wet etch for wafer thinning, TMAH can enter into the release layer channels and start etching the sidewalls of the channels, as illustrated in Figure 5.10 (a). This can cause the thin wafer to start delaminating at the wafer edge, because that is most

affected by TMAH encroachment. To counter this problem during wafer thinning, we modify our handle wafer to be covered with an additional protective oxide layer as shown in Figure 5.10 (b).

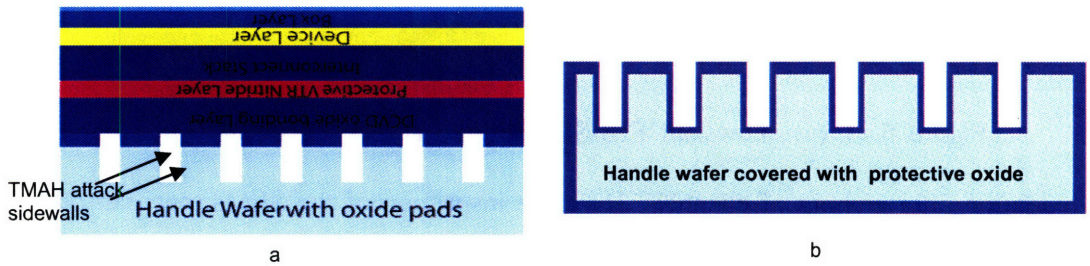


Figure 5.10: a) During wafer thinning, TMAH attacks the channel sidewalls. b) Silicon handle wafer with etched channels and covered with oxide.

To achieve this, our process flow for the handle wafer is changed in small way. Lithography is conducted as before on the bare silicon handle wafer. After channels are etched, the wafers are cleaned, then a 0.5 μm thick silicon oxide is grown on using wet oxidation furnace process.

The changed process flow for the handle wafer is applied to the various pad size and spacing mask sets those defined in Section 5.2 with the exception of the 30 μm pad size and 30 μm spacing. Bonding experiments revealed that wafers with 500 μm pads and 100 micron channels, and between-die channels, can be bonded, but the wafers with smaller pad sizes do not bond successfully.

As described earlier, there can be two reasons for oxide bonding not to occur: chemical limitations (the surface is not hydrophilic enough) and mechanical limitations (there can be an issue with local roughness, wafer bow and total thickness variation (TTV)). It is found that the wafers with 500 μm and larger pads, can be bonded, as mentioned earlier, which suggests that chemical issues are not the source of bonding

problem. To determine the local roughness, an AFM study was conducted on the oxidized pads, which reveals that roughness is the same as when thermal oxide is grown on the blanket wafers in both cases being about 0.2 nm. Wafer bow is measured for all wafers used for this bonding experiment, using KLA Tencor instrument; the bow is less than 25 μm in all cases.

Figure 5.11 (a) shows an FIB-SEM of the corner of a pad which underwent oxidation after etching of channels. By close inspection of the SEMs, one can observe that there is bump approximately 5-10 nm with width of 2-3 μm, near the corner of the channel. Suni et al. [66] present experimental results that also match with our observation shown in Figure 5.11 (b) taken by Dektak surface profilometery. These results are also consistent with observations made by other MTL researchers [133]. This bump formation likely occurs due to different thermal oxidation rates for convex and concave corners, compared to flat surfaces.

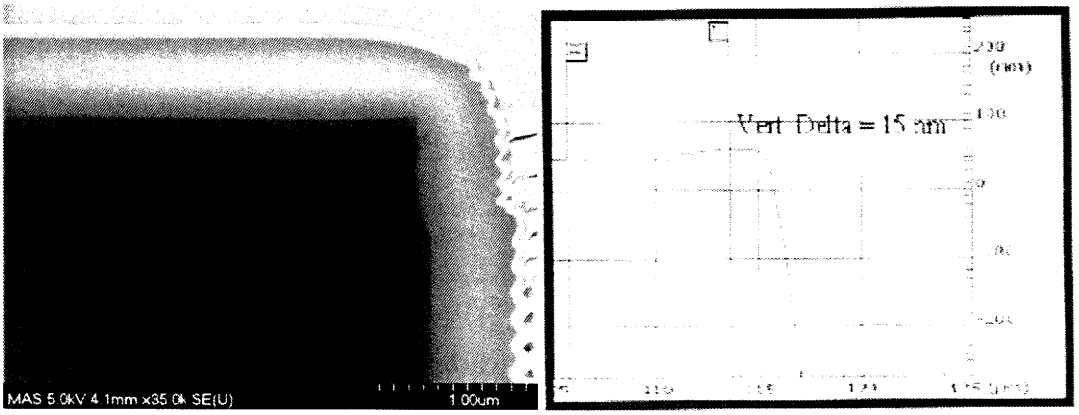
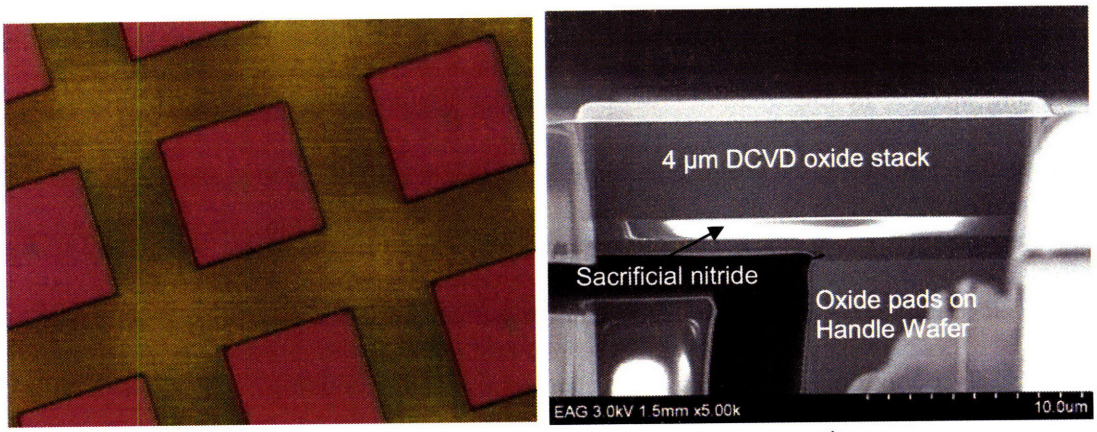


Figure 5.11: a) FIB-SEM of corner of silicon pad which is oxidized after etching. b) Profile of pads showing a bump of order of 15 nm [66].

To understand the impact of the raised bump at the corner of the pads, we turn to bonding studies in the literature which consider requirements for closing small gaps during wafer bonding. According to Tong and Gösele [86], the gap closing can occur at the bonded interface if the condition $h < 2.6(R\gamma/E)^{1/2}$ is fulfilled, where h is height of the bump, R is the lateral extension of the gap (in our case it is the size of pad), γ is surface energy at room temperature (0.1 J/m^2 for oxide–oxide bonding), and E is Young's modulus. Based on this equation, the gap between our pad and a planar blanket wafer will not be able to close given typical bump and pad dimensions. When pad size is very large, as in our 500 μm or 10,000 μm (full 1 cm die) cases, then the bump is too small enough in relation to the dimensions that it does not hinder the bonding process. When the bump becomes comparable in size to the pads, however, then bonding is not possible.

For the reasons above, we change the oxidation thickness for the patterned wafer to 200 nm instead of 500 nm, which leads to a reduction in the height of the bump. With this oxidation thickness, 80 μm pads can be successfully bonded to the dummy device stack. Figure 5.12 (a) shows an optical image of 80 μm pads with a thin device stack. Figure 5.12 (b) shows an FIB-SEM of the same wafer, demonstrating that the wafer can be bonded and thinned successfully.



a b

Figure 5.12: a) Optical microscope image of 200 nm oxide bonded to the dummy device wafer and thinned back to BOX layer. b) FIB-SEM of the same thinned wafer.

5.5.3 Mechanical Stability of Thinned Films

Another major concern in the oxide release layer approach is the stress-strain induced on the device layer, not only during thinning, but also the residual stress and deflection after thinning. Given the presence of the handle wafer channels, the thinned device wafer is only supported periodically by the oxide pads, and thus there can be deflection or surface bowing and, in extreme cases, buckling of the device layer.

In order to understand this issue and establish a constraint on pad size and spacing, we turn to studies conducted previously in the literature. The MEMS community, in particular, has long been interested in free standing films or membranes bonded to a cavity. Recently, wafer bonding has been used to fabricate membranes on the cavity, rather than the more traditional sacrificial etch, because of bonding ability to form different sizes and shapes of cavities at the same time. Huang et al. [87] fabricated capacitive ultrasonic transducers using wafer bonding technology, and in that work, different membrane thicknesses are investigated for various cavity sizes to understand the

deflection characteristics of the membrane. Table 5.3 summarizes their results, for a square silicon membrane bonded to a cavity.

Membrane Size (μm)	Thickness (μm)	Ansys Result (μm)	Wyco Result (μm)
600	4.2	6.24	6.1
650	4.2	7.34	7.4
700	4.2	8.13	8.2
750	4.2	9.3	8.8
150	0.34	2.7	2.29-2.33
100	0.34	1.56	1.69-1.79
50	0.34	0.54	0.54-0.57
40	0.34	0.34	0.32-0.34
35	0.34	0.15	0.21-0.23
30	0.34	0.15	0.21-0.22
20	0.34	0.016	0.033-0.038
10	0.34	0.01	0.014

Table 5-3: Deflection of different membrane sizes and thickness [87].

Figure 5.13 (a) shows a cross-sectional image of our thinned device wafer bonded to 80 μm pads and 40 μm wide channels, etched to a depth of 30 μm. The bonded stack is thinned using grind-back followed by the wet TMAH process. In this case the dummy device wafer was simply 0.5 micron thick oxide, thus resulting in a 1 μm oxide layer bonded to the oxide support pads. As seen in Figure 5.13 (a), a large deflection of about 2-3 μm exists. Figure 5.13 (b) shows another structure, in which the thinned device wafer has been bonded to 80 μm pads; in this case, the wafer was thinned using grind back followed by STS plasma etch for one hour and wet TMAH etch for 10 minutes.. In this case, the thinned device wafers consists of 10 μm of silicon, together with a 0.5 μm thick oxide layer, which is bonded to oxide pads in the handle wafer. The 10 μm thick membrane does not shows any signs of deflection or residual stress.

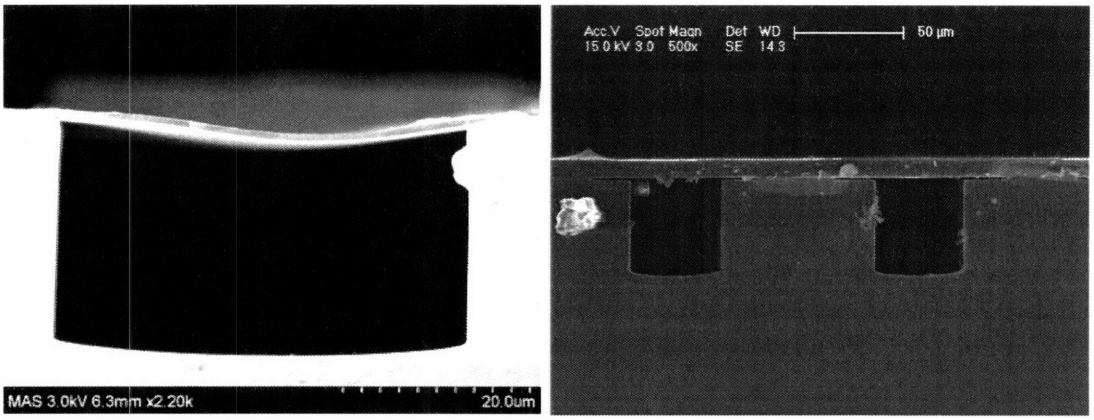


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Figure 5.13: a) FIB-SEM of 1 µm thin membrane on 40 µm wide channel. The image depicts large defelction and residual stress. b) SEM of a wafer thinned using plasma etch, followed by wet etch. A 10 µm thick silicon layer remains on the 80 micron oxide pads with 50 micron channel depth.

Figure 5.14 is another cross-sectional SEM image of the same thinned wafer shown earlier in Figure 5.12. In this structure, a full dummy device stack is emulated and the resulting thinned membrane shows good integrity with no noticeable deflection. Because of the wet-etch using TMAH, residue can be seen at the surface; in the image, the left pad was cleaved using FIB, which also causes an imaging artifact in the channel.

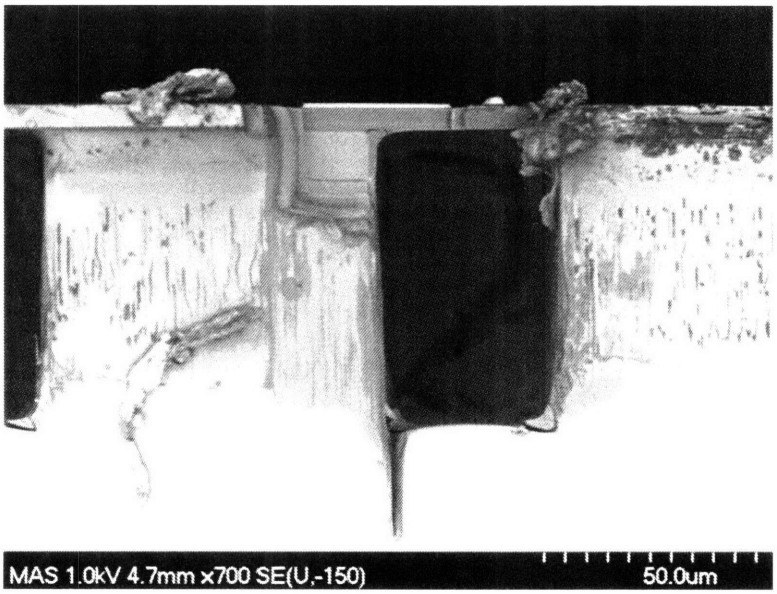

Figure 5.14: FIB-SEM of thinned wafer with a 5 µm thick membrane on 40 µm wide channels.

5.4.4 Wafer Thinning Summary

Based on our wafer thinning studies, an important observation is that for reliable thinning using a wet alkaline silicon etch (TMAH), the channels and sidewalls must be covered with a protective oxide layer. To form these protective coatings, one needs to perform oxidation of pads, after channel etch; unfortunately, pad oxidation can create bumps at the edges of pad to prevent wafer bonding (depending upon pad size). However, with the reduction of the oxidation thickness, it becomes possible to bond successfully.

Our studies also show that after wafer thinning, the device layer membrane can deflect if thinned below the thickness of 1-2 μm. This is certainly not desirable for devices on thinned wafers. We find that thinned wafers with the thickness greater than 5 μm and with 40 μm channels do not show any deflection. Further simulation and measurement is recommended in future work to measure the exact deflection and calculate the corresponding stress.

5.6 Permanent Bonding

In the proposed handle wafer release method, the temporary bonded oxide layer needs to be released at a later stage using an HF-based wet-etch chemistry. Therefore we need a metal that can withstand concentrated acid for a long duration. Copper fares well against acids that are not oxidizing in nature or do not have oxidizing chemistry present along with them. Diffusion and adhesion barrier metals also need to have good resistance to HF-based chemistry. Ti reacts vigorously with HF, but TiN and TiW are believed to be stable compounds [93]. Due to lack of source of TiW and reactive sputtering for TiN, Ta is chosen as the adhesion and diffusion barrier for copper. Thus, the same stack composition is used for permanent bonding as described in Chapter 4. Blanket copper

films are used for permanent bonding, with tantalum as the diffusion and adhesion barrier on the oxide. The permanent bond is dependent on wafer thinning and how smooth a surface can be achieved; therefore, it is required that the wafer thinning step stop on the BOX layer with high selectivity.

A thinned dummy device SOI layer/membrane is dump-rinsed and cleaned with great caution. If not cleaned properly, TMAH leaves residue on the back side of the thinned wafers and can cause problems in copper bonding. A tantalum/copper (Ta/Cu) 50/300 nm stack is deposited on both the back side of the thinned wafer and the front side of a new dummy SOI device wafer using e-beam deposition (as described in Chapter 4). In real devices, one would need to perform a dual damascene process to form copper contacts on the back side of the thinned wafer and on the second device wafer in order to have a mirror image of the copper pads for bonding, but in our experiment we bond blanket copper layers. The wafers are bonded using the EV 501 at 350°C for 60 minutes, with applied down force of 6000 N. The copper bonding process is the same as that used in Chapter 4 and is based on the previous work by Fan [58], Tan [57], Chen [60] and Tadepalli [59]. Figure 5.18 (a) shows the stack schematic after the permanent bond has taken place. Figure 5.18 (b) shows an FIB-SEM of the three-layer stack, demonstrating that reliable copper bond can be formed on the thinned substrate supported on oxide pads.

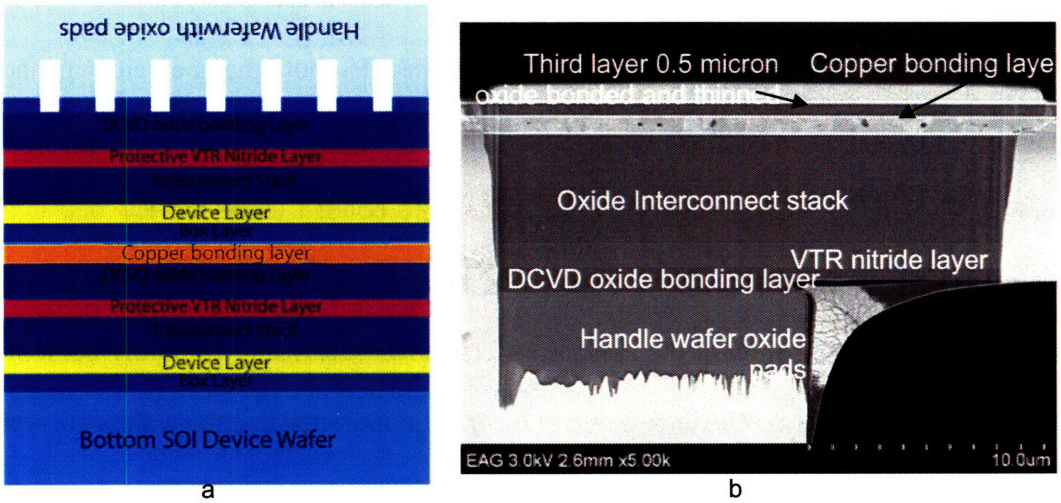

Figure 5.15: a) Schematic representation of three-layer stack with permanent bond formed using copper. b) FIB-SEM of three layer bonded stack with copper bond.

5.7 Handle Wafer Release

In this section, we seek to demonstrate the feasibility and manufacturability of the proposed oxide release layer approach. Two alternative chemistries are explored: 49% HF and a buffered oxide etch (BOE). The motivation for the use of concentrated HF and BOE chemistries for sacrificial oxide removal comes from experience in the MEMS community, where substantial study of various etchants and processes have been explored [89],[90],[91],[94]. We study a key characteristic for the handle wafer process, namely, the ease of releasing or debonding. The ease of release or debond is characterized by the time required to release the handle wafer, and the selectivity of the release chemistry. In this section, we primarily focus on the time required to release while in Section 5.8, integrated release results, we will comment on the chemical selectivity.

5.7.1 HF Release

The first set of oxide release experiments utilizes 49% HF as etchant. Handle wafers with oxide pads are bonded to a 2 μm thick blanket CVD oxide film on the

acceptor silicon device wafer. The handle wafer is fabricated using 30 μm pads and 30 μm channels. The wafer is etched for 10 minutes in the STS tool, giving an etch channel depth of 8 μm at the center of the wafer. The blanket CVD oxide film is polished for 60 seconds to overcome local roughness. The wafers are bonded using the EV 620 with plasma activation as previously described. The bonded wafers are annealed for three hours. Infra-red examination of the bonded wafers shows successful temporary bonding, as seen in Figure 5.16 (a). The dark circle in the middle indicates that the wafers are well bonded with no air trapped in the center, although some air is trapped at the edge of the wafer.

The bonded pair is then immersed in a Teflon container having 500 ml of 49% concentrated HF. The infra-red image of the bonded pair is shown in Figure 5.16 (b) after three hours of a soak time in the 49% HF bath. It is apparent that the wafer is released at the edges of the wafer, but is still bonded in the center of the wafer. This indicates that the process is in a etchant diffusion limited regime. HF encroaches from the wafer edge and travels through the channels, and at the same time undercuts the bonded pads. In this experiment, no ultrasound was used. With continued soaking, the bonded pair finally releases after five hours.

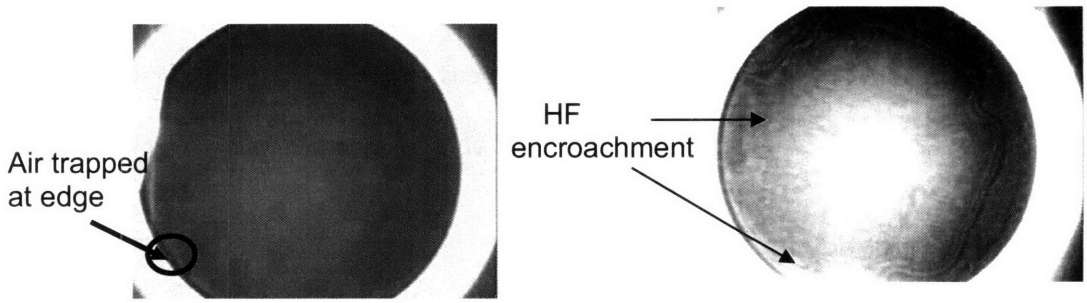

Figure 5.16: a) IR transmission image of a well bonded oxide wafer with air trapped at the edge. b) Partially released wafer after three hours of soak time in concentrated 49% HF. HF encroachment can be seen.

This experiment demonstrates the feasibility of the concept, channel-based oxide release layer and shows that wafers can be successfully released. However, release time is one of the most important characteristics in determining the manufacturability of this approach and a reduced release time is desirable. Low stress silicon rich nitride (SiN) has been proposed to act as a sacrificial layer in a 49% HF bath, and it is known that 1 μm nitride can withstand 49% HF for 45 minutes [93]. Several release studies are described next in an effort to understand the effect of channel depth, and channel and pad pattern size on release time. In these studies, the ultrasound agitation is also introduced to increase the penetration of HF, which helps to further reduce the release time. In addition, other methods to reduce release time are explored, including etching of between-die channels (200 μm wide), and as well as mechanical cleaving using a water-jet.

In the first release experiment, the handle wafer is exposed twice, using the pads/channels mask first and between-die channel mask second. The idea behind creating between-die channels is to provide etchants greater access to the center of wafer. Figure 5.17 illustrates a handle wafer which is exposed twice using the 40 μm pad mask and the between-die channel mask.

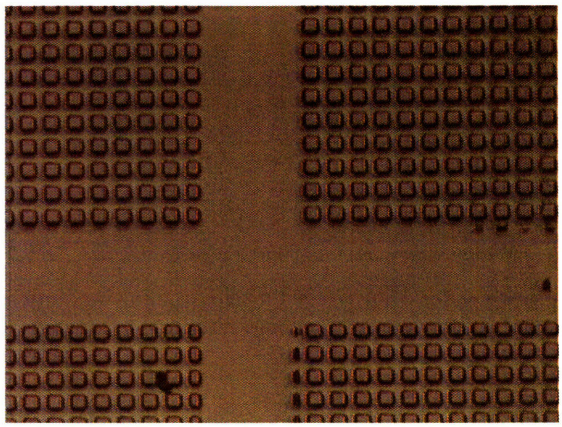

Figure 5.17: Optical microscope image of 40 μm pads, double exposed, with between-die channel mask (200 μm wide) after release using HF.

In the second enhancement explored, a water jet technique is used in which the jet is forced in between bonded wafers. The bonded wafers can be successfully cleaved by forcing the water-jet into the bonding interface for 1 minute. Although water or moisture reportedly reduces the strength of the oxide bond [72], we believe this technique primarily provides the mechanical force to drive the wafer separation. Figure 5.18 (a) shows a blanket wafer with a 0.5 μm thick oxide when bonded to a handle wafer with 80 μm pads. When forced with the water jet, oxide pad marks remain on the wafer after cleaving. Figure 5.18 (b) provides an enlarged image of the marks on the blanket wafer, which depicts pads remaining from the handle wafer. This suggests that mechanical force has overcome the original pad/device interface strength fracturing the pads rather than enabling chemical release at the temporary oxide bond interface. It appears that the water jet helps to release the handle wafer, when etch driven release becomes diffusion limited, such as in the middle of the wafer or during the last part of the release.

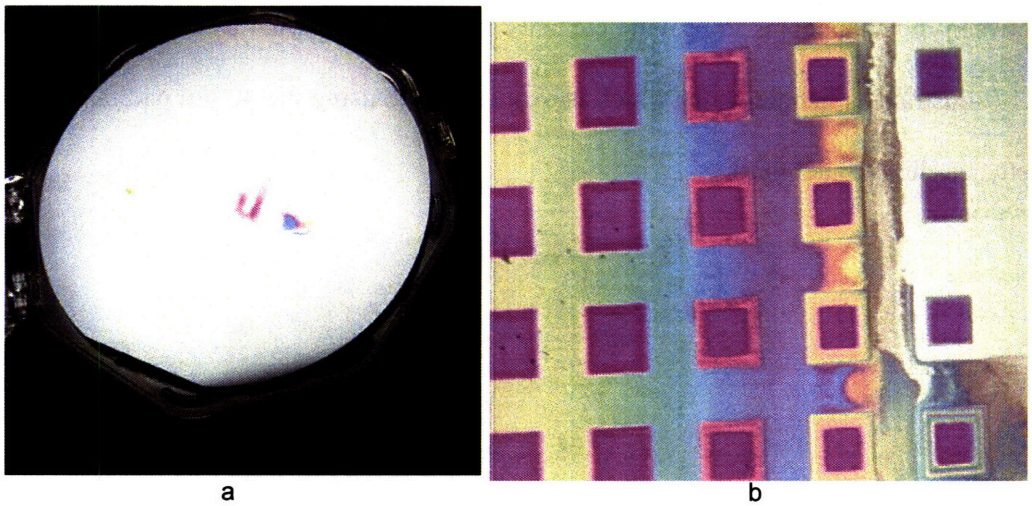

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Figure 5.18: a) Blanket oxide wafer after water jet release, showing imprints of oxide pads from the handle wafer. b) Optical microscope image of remaining oxide pads on the blanket wafer.

Three additional sets of experiments are conducted to gain an understanding of the dependence of release time on feature size (pad/channel) and etch depth, and the

effect of patterned between-die channels. In the first set of experiment, three different mask sets with pad size/ spacing of 80/40, 40/20 and 30/30 are used to make three different kinds of handle wafers. The bonded area fraction for the first two masks is designed to be 4/9, while the third mask had a lower bonded fraction of ¼. The handle wafers are etched using an STS ICP chamber, as described previously to approximately the same etch depth. Table 5.4 summarizes the results, showing approximate channel depth (±2 micron) and the corresponding release time in 49% HF with ultrasonic agitation. The observed pad size is smaller than the designed pad size, primarily because of over exposure during lithography; the observed bond area fraction is reported in the Table 5.4. It shows that release time decreases with decreasing bonded area fraction for approximately same etch depth.

Pattern size (pads/spacing) (μm)	**Etch depth center/edge (μm)**	**Real area fraction**	**Release time (min)**
80/40	**~50/ 58**	**0.34**	**55**
40/20	**~48/ 60**	**0.28**	**35**
30/30	**~ 45/55**	**0.18**	**25**

Table 5-4: Pattern size effect on release time.

The second set of experiments is conducted to analyze the channel depth effect and water-jet on release time. The mask with 80 μm pad and 40 μm channels is used to fabricate handle wafers with different etch depths. The handle wafer release times for handle wafer, with or without water-jet forcing are detailed in Table 5.5. An ultrasound bath is used for all the releases in Table 5.5.

Center Etch depth (μm)	Water jet used or not	Release time (min.)
~60	No	< 80
~51	Yes	45
~42	Yes	55
~23	Yes	90
~8	No	< 240

Table 5-5: Release time vs. etch depth and effect of water-jet. For this experiment 80 μm pad and 40 μm channel mask was used.

It appears that the use of water-jet reduces the release time substantially, comparing the 60 and 51 micron deep channel results. A substantial portion of the wafer needs to be released before applying the water-jet. If applied too early, it can damage or possibly break the device wafer.

In the third set of experiments, we assess the effect of between-die channel on the release time along with etch depth. The mask with 80 μm pad and 40 μm channels mask was double exposed with between-die channel and etched for different depth. The results are tabulated in Table 5.6 and like all the previous experiments ultrasonic agitation is used.

~Etch depth (micron)	Release time (min.)
~40	45
~50	35
~ 95	25

Table 5-6:: Release time for handle wafers with between-die channels and 80 μm pads and 40 μm channels mask was used.

The release time is function of the channel etch depth as it can be seen from both Table 5.5 and 5.6, which shows that release time decreasing with increasing etch depth.

Although, it can be said that dependence becomes weak at the larger etch depth such as 90 micron in Table 5.6.

It can be very well said that introducing between-die channel is the most effective to reduce release time if we compare across the table for 80 μm pad and 40 μm channels with or without water-jet and with or without die-saw line for the same etch depth. We find that 80 μm pad and 40 μm channels without between-die mask and no water jet takes 55 minutes to release, while with water jet it takes 45 minutes to release, and with die-saw mask, it took 35 minutes.

5.7.2 BOE Release

The concentrated HF can be very corroding to metals and other silicon based compounds depending upon the impurity levels. Because of this concern, buffered oxide is investigated very briefly for release. The handle wafer had 80 μm pads and 40 μm channels (mask-set 1) and die-mask is superimposed for effective release. It is etched for one hour in an STS etch tool, i.e. approximately 45 μm center etch depth, and is bonded to the device wafer, which had die-saw lines etched on it. The die-saw lines facilitate the release process, by increasing the pathways for etchant to access the center of wafer.

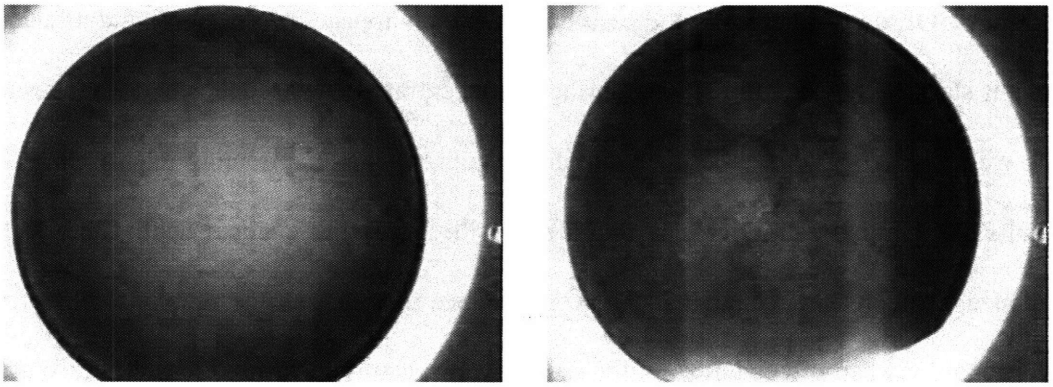


Figure 5.19: a) IR transmission image of bonded pair after 45 minutes. b) IR transmission image of same pair after 4 hours.

Above are the infra-red images of the bonded pair (Figure 5.19) immersed in BOE with an ultrasound bath for 40 minutes and 4 hours respectively in (a) & (b). The images show that the bonded pair, which is immersed for 40 minutes, released at the edges only, indicating penetration is really slow. Even when the wafer is left in BOE for 4 hours, the pair is not released, as one can see from the bonded area in the center.

Another significant observation is the corrosion and roughness appearing on the silicon surface. It has been reported in several studies that silicon shows signs of roughness when left for a long time in BHF solutions. Miyamato et al. [92] suggested that by suppressing the NH_4F concentration, one can suppress micro-roughening and pitting caused by BOE and he also proposed hydrocarbon additives which can help achieve that.

5.7.3 Summary of Handle Wafer Release Results

Different oxide and chemicals are reviewed, which are used as sacrificial layer and its etchants. In the interest of time, we only explored concentrated HF and BOE on thermal oxide bonded wafers. It will be interesting to see how different surfactants and additives suggested in the literature [91] can modify the conclusions we derived.

The results of our HF and BOE oxide release investigations can be summarized as follows. BOE does not yield good results, as the etch appears to self stop, and after one hour it starts to corrode the silicon surface. Concentrated HF produces excellent results and we explored various experiments to understand the factors affecting release time and results are summarized here. It is found that with increasing channel depth, decreasing pad size, or, increasing channel size, one can reduce the release time. The introduction of additional between-die channels in the handle wafer can reduce the release time. Water-

jet separation also helps to reduce the release time by mechanically cleaving the remaining bonded oxide in the center, but care must be taken to avoid damages.

5.8 Integrated Oxide Release Layer Process Results

In this section, experiments are described in which a thinned device wafer, bonded to pads using low-temperature plasma assisted oxide bonding, is transferred to another silicon wafer. This constitutes a test of the integrated oxide release layer concept. The back-side of the thinned wafer is bonded to the front of another silicon wafer using thermo-compression bonding, as illustrated in Figure 5.15. As shown in earlier sections, concentrated hydrofluoric acid is the fastest oxide etchant for the release the sacrificial layer; however, HF is very corrosive and not very selective, and integrated flow assessment is needed. For this set of experiments, the three layer bonded stack is immersed in concentrated HF, using a Teflon boat, and provided with ultra-sound energy for better penetration. We demonstrate successful release, and then summarize our learning from these oxide release layer process flow experiments.

Figure 5.20 shows the first successful release of the full handle wafer. In this case, we did not thin the wafer using TMAH, but instead bonded it immediately after grinding because the handle wafer was fabricated using a preliminary handle wafer process flow. The back-side of the wafer was not smooth, and the thinned device wafer was approximately 50 μm thick. Therefore, the permanent bond was not strong, but this experiment does demonstrate the full-scale release of the handle wafer. The permanent bond is made using copper at 400°C for 30 minutes, and annealed at 400°C for 60 minutes. The wafer edge yield was poor, and the copper was corroded at the wafer edges after wafer release because oxide beneath the Ta/Cu stack was attacked. The handle

wafer had the channels that are 40 μm deep with between-die channels and the 80 μm pad mask. The wafer release required about 80 minutes, with help of the water jet. Because the release took more than 45 minutes, it is expected that all of the sacrificial nitride as well as the dummy interconnect stack was etched.

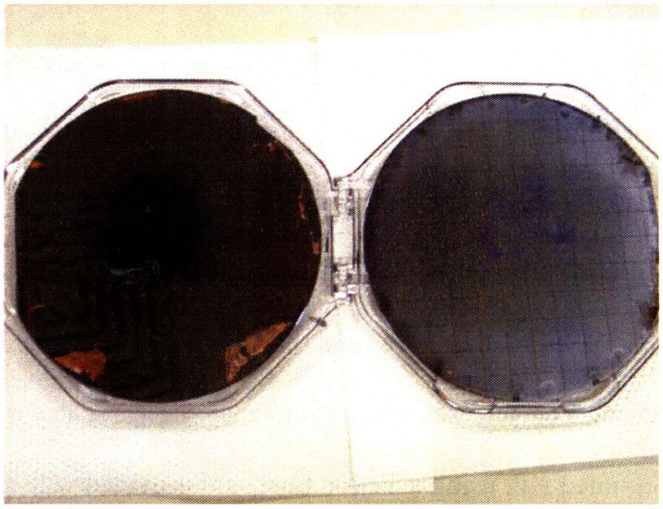


Figure 5.20: First full wafer release using concentrated HF. The release required 80 minutes, so that sacrificial nitride was also etched.

As discussed in Section 5.5, our handle wafer fabrication process is enhanced to include protective oxide on the sidewalls. A full integrated handle wafer process experiment with the enhanced protective oxide shows successful release using concentrated HF, as pictured in Figure 5.21. The oxide stack beneath the nitride is unharmed; the surface of the transferred device wafer is still covered by nitride as confirmed with Nanospec. The handle wafer in this case uses 80 μm pads with 40 μm spacing and channels etched to a depth of 60 μm. Copper bonding for permanent bond is performed at 350°C for one hour. With the protective oxide on the handle wafer, the dummy device wafer can be thinned using the standard procedure; the device wafer is thinned using mechanical grinding followed by a wet TMAH etch. In this case, it took

approximately 45 minutes for the handle wafer to be released from the bonding stack. In this full integrated handle wafer process flow experiment, the handle wafer can be released and the thin membrane device layers are successfully transferred.

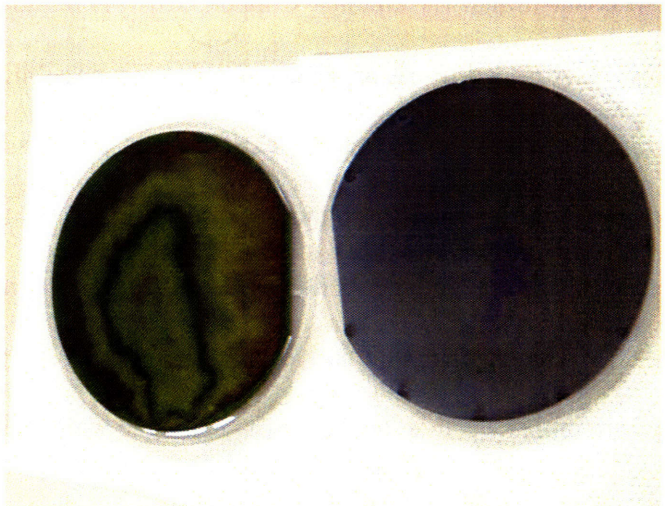


Figure 5.21: Successful release with 49% HF in 45 minutes. Remaining nitride layer can be seen.

Based on our investigations, several additional observations can be made regarding the proposed oxide channel release layer handle wafer process. We find that the release time is not only dependent on channel depth, presence of between-chip channels or wide channels and bonding defects, but also on the processing temperature during subsequent processing. We found that that oxide bond becomes tougher if it is annealed at higher temperatures but this also results in longer release times. This observation is consistent with reports by Suni et al. [67], which suggests that HF under-cut etch rate is inversely proportional to bond strength. Thus, it becomes important to make a permanent copper bond at a low-temperature. This also helps explain the long release time required for our first release experiment, in which the permanent bond is formed at 400°C and also annealed at the same temperature.

In terms of chemical selectivity, we find that HF acid release raises some concerns. The concentrated HF attacks tantalum and the oxide layer beneath the tantalum. The sacrificial nitride has a finite etch rate, so that the 1 μm nitride can only withstand about 45 minutes of concentrated HF etching. Copper, which is immune to concentrated HF, can nevertheless be corroded if it is oxidized, and this is a possibility during bonding and subsequent annealing steps. In the above experiments, the handle wafers can be released without damaging the permanent bond because of the use of the blanket copper layers, but in the case of patterned copper pads, corrosion may be a concern. Thus, future work is suggested to evaluate other alternative etch chemistries, such as vapor HF or buffered HF, which are more selective, for better oxide handle wafer release.

5.9 Summary

In this chapter, low-temperature oxide bonding is used to form a sacrificial bond, which can be released using concentrated HF acid with the help of channels etched between oxide pads in the handle wafer. A new oxide release layer process flow is proposed, and then modified to include a protective oxide layer on the sidewalls of channel, to enable wet-etch using TMAH.

Several important parameters of the handle wafer process are characterized. Bond strength is measured using a chevron structure, showing that normalized bond strength decreases with smaller pad size. The release time is found to increase with larger pad size, which creates a trade off between bond strength and release time. We find that there are far fewer voids in the low-temperature bonding of handle wafer with patterned pads compared to blanket wafer bonding because of the presence of channels that help remove water molecule from the bonding interface.

It is also established that thick oxidation of etched pads is not suitable for fusion bonding at low-temperature, because of the presence of bumps near the edges of the pads. Thinner oxidation layers can be used to achieve successful bonding. In terms of thinning-back, the proposed approach has some concerns because of presence of encapsulated channels, which require that thinned device wafer be free floating over these spaces. It is shown that the device wafer can be thinned to a 5 μm thick stack remaining, and this layer can be reliably bonded to another wafer using permanent copper bonding. However, further evaluation is needed to optimize the device layer thickness, and to understand the stress relationship between etch-back thickness and channel size.

A thin membrane device wafer has been transferred using this process flow successfully, and the handle wafer release time was studied showing that release time depends on pattern, channel depth, presence of additional wide between-die channels, presence of defects and processing temperature. However, concentrated HF raises concerns for manufacturing purposes, primarily because of its high corrosive nature, creating a need to explore other oxide etchants to make this process more manufacturable. The proposed oxide release layer with channels has been successfully demonstrated, and appears to be a promising handle wafer technology meriting further research and development

Chapter 6: Low Temperature Permanent Metallic Copper – Indium Bonding

This chapter deals with the investigation of a low-temperature permanent bonding technique, as an alternative approach to enable handle wafer integration. The primary objective is to form a good quality bond at the lowest temperature possible, so that handle wafer approaches such as smart cut and temporary adhesive bonding can be realized. In Chapters 4 and 5, we investigated different chemical release methods using micro-channels in the device wafer and in the handle wafer, respectively. In this chapter, we investigate a novel system Cu-In, for making a permanent bond at 200°C which will be stable at higher temperature. This will enable an expanded menu of handle wafer methods; including those requiring thermal decomposition for release at temperatures above 200°C.

As described in Chapter 1 (Table 1.1), there is a multitude of bonding materials (metals and dielectrics) under investigation in industry and academia. In Section 6.1, we will provide a brief motivation for low-temperature bonding. Section 6.2 follows with an overview of different metallic bonding systems, and we describe a concept called solid liquid inter-diffusion (SLID) bonding, which was introduced by Bernstein in 1966 [95],[96]. In Section 6.3 we describe the bonding experiments performed using copper-indium. The bonding interface was characterized using SEM and STEM and the results are presented in Section 6.4. Section 6.5 presents further characterization results of multi-stack copper-indium films using SEM and XRD, to identify different phases formed in the as-deposited and annealed films. Section 6.6 discusses the source of observed void

formation and Section 6.7 suggests alternatives that might reduce or eliminate the formation of voids in the bonding interface. Finally in Section 6.8 we present a summary of our understanding of these thin films and the bonding interface.

6.1 Motivation for Low-Temperature Bonding

As mentioned above, the most important motivation for making a permanent bond at low-temperatures is that it provides expanded flexibility to 3D IC processing. For example, Tan [33] proposed a smart-cut approach for releasing the handle wafer. H_2 cracking is very sensitive to temperature, and its temperature activation range is between 250-300°C. Therefore, one needs to bond at a temperature lower than 250°C for robust processing. Similarly, EVG [123] has proposed various thermoplastic polymers for use in handle wafer processes which debond at 250°C. If we can make a permanent conductive bond at a low temperature, it becomes possible to consider these handle wafer alternatives. We are already limited by temperature at the high end, as 3D integration is conducted at the BEOL, requiring all processing temperatures are be less than 400°C.

Another motivation is to reduce misalignment in bonding. The difference in thermal expansion coefficients for materials used in CMOS makes it is very difficult to obtain sub-micron alignment when the bonding process requires high temperatures.

Lowering the bonding temperature can also increase throughput. It usually takes about one hour in a bonding chamber under pressure to make a reliable bond. In addition, it usually takes an hour for the ramping up and down of the temperature. Being a single wafer process, the long bonding process times can be a concern.

6.2 Solid Liquid Interdiffusion (SLID) Bonding

Bernstein, in 1966 [95], proposed solid liquid interdiffusion (SLID) bonding for semiconductors, and explored various indium and tin based system. The main idea behind SLID bonding is that low-melting point metals diffuse rapidly into a parent metal and form intermetallic compounds which are then stable at higher temperatures. Bernstein described the process in the following five distinct stages:

Wetting: During this stage, a low-melting point component melts and covers the high melting point metal or component. The conventional surface free energy plays a primary role in achieving optimal wetting.

Alloying: Alloying between the liquid and the high melting point component. This stage terminates when the liquid is completely saturated, according to the appropriate phase diagram.

Liquid Diffusion: The liquid and solid components begin to interdiffuse to form high melting compounds. This stage determines the effectiveness of the bonding mechanism.

Gradual Solidification: The quantity of the liquid phase diminishes and the bond gradually solidifies until all liquid disappears.

Solid Diffusion: During the preceding two stages, diffusion in the solid state is also taking place, but after complete solidification, this is the only mechanism to drive this reaction to equilibrium. This stage usually happens during annealing.

Bernstein et al. [96] not only studied the binary system combination of gold, silver and copper with indium and tin, but also looked at the ternary systems. Various

samples were bonded at 300°C for one hour under N_2, H_2, or Ar is added to the environment to minimize oxidation. In their study, tensile testing was conducted in the bonded samples at the temperature range of 200-450°C. Few copper-indium bonds were ruptured, even at a low-temperature, without even forming the higher temperature phase. This anomalous behavior was attributed to poor wetting, unsatisfactory mating of parts and other factors. The research concluded that the bonding is good and there are no voids, cracks or non-wetted areas present. The thickness of the metallic films in Bernstein studies were on the order of 25 μm. In the next two sub-sections, we present two examples of SLID bonding from recent literature.

6.2.1 Copper Tin Bonding

In recent years, the copper-tin system has been explored by IZM Fraunhofer [38] and Infineon [98] for their 3D IC process flow. IZM proposes to use copper-tin in back-to-face integration using the via-first approach at the wafer-level, while Infineon uses this in the face-to-face approach for die-to-wafer integration (SOLID).

The Infineon approach involves electroplating an 8 μm thick copper/tin bilayer, then bonding it to electroplate copper at 260-300°C as illustrated in Figure 6.1 (a). Figure 6.1 (b) shows an FIB of a 3D integrated test structure after bonding. During the bonding step at a temperature of approximately 300°C while applying pressure, the liquid Sn is interdiffused by Cu, finally forming the intermetallic phase Cu_3Sn. This so-called ε-phase is thermodynamically stable with a melting point above 600°C as seen in the phase-diagram of Cu-Sn (Figure 6.2). Using appropriate film thicknesses, tin is consumed and the solidification is completed within a few minutes, with copper on both sides. The tin film should always be in the range of 20-30 atomic percent in the total stack (marked

in Figure 6.2), so that the reaction can be driven to phase where Cu_3Sn is formed along with copper as shown in Figure 6.1 (b).

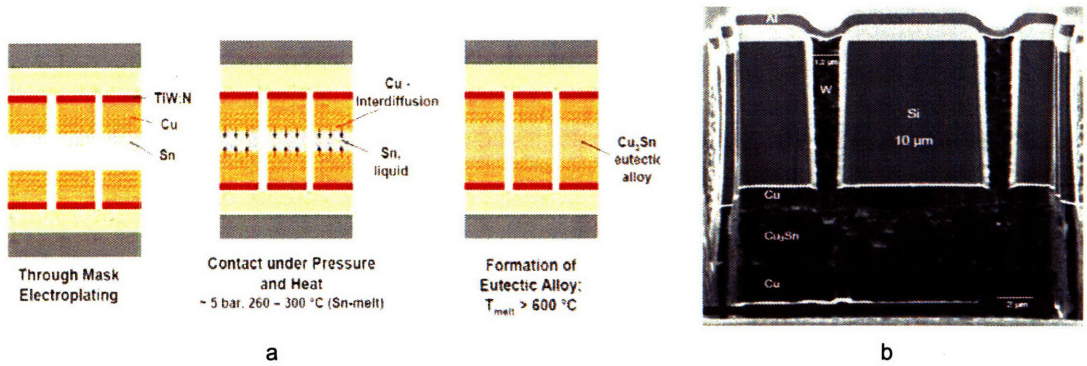


Figure 6.1: a) Schematic process for Cu-Sn bonding followed by IZM [[31]]. b) FIB-SEM of copper indium bonded silicon wafer with through silicon via filled with tungsten [[38]]. Indicating a stable form of Cu_3Sn in between the Cu layers.

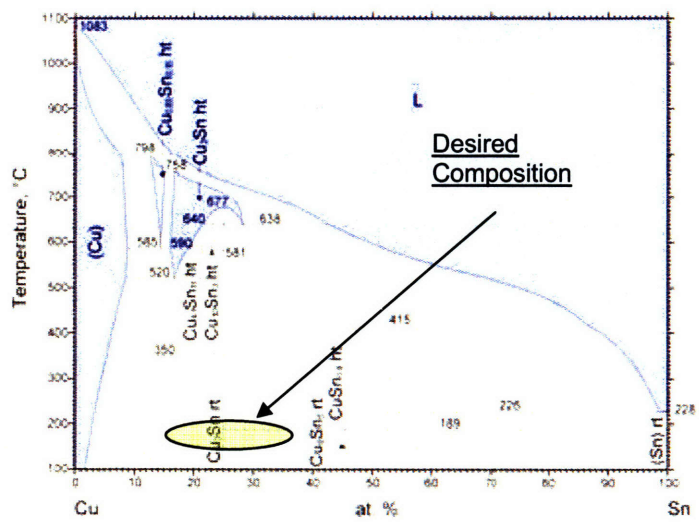


Figure 6.2: Cu-Sn phase diagram [144]. The arrow indicates the composition or percentage of Sn desired in the multi-layer.

Copper-tin bonding has several advantages. It can be bonded at 260°C and it requires less time under pressure (i.e. in a bonder) which increases throughput. It also helps in conformal and repeatable bonding, reducing the bonding variation due to pressure and topography issues.

There are a number of issues or concerns with copper-tin bonding. First, tin has a problem of whisker growth [134]. Second, the process currently developed by IZM is good for the stacking of 50 μm dies, as it uses very thick metallic stacks, unlike sub-micron thick copper bonding. Therefore, the pitch for inter-wafer vias is on the order of 50 μm, compared to 5 μm, which can be achieved in wafer-level integration using copper bonding.

In the next section, we introduce copper indium bonding using the SLID concept. The primary previous work with this system has been reported by C. Chen and C. Lee [99], for electronic packaging.

6.2.2 Copper Indium Bonding

Besides tin based solders, indium has often been used as a soft solder for bonding delicate devices that need a low process temperature. Indium is extremely malleable with excellent fatigue resistance. Its use is appropriate when a large plastic strain of the joint is required to release stresses induced by thermal expansion mismatch. Besides the aforementioned reasons, copper-indium is of interest for our study for the following reasons: 1) lower melting temperature of 157°C, but not as low as gallium which can be difficult to handle; 2) it forms a self-passivating oxide and adheres well with copper; and, 3) copper-indium has a very similar phase diagram, as seen in Figure 6.3 [143], to form intermetallic compounds such as $Cu_{11}In_9$, Cu_7In_4.

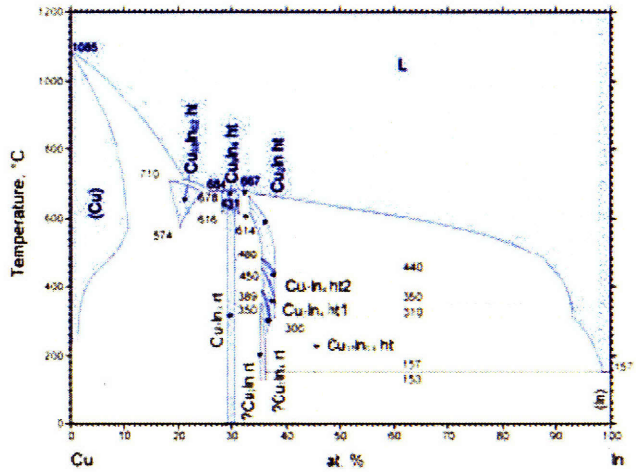


Figure 6.3: Cu-In phase diagram obtained from ASM [143]. A range of intermetallic compounds can be stable up to 600°C.

Indium was used in conjunction with several other metals like gold, silver and copper for use as a solder metal [99],[100],[135]. C. Lee et al. [99],[100] at University of California Irvine, have explored fluxless bonding technology using a similar concept to SLID bonding, primarily for electronic packaging. Low-melting point metals, such as In are capped with a high temperature metal like Cu, Ag, or Au and then bonded to another sample which has a high temperature metal as shown in Figure 6.4. The main idea behind fluxless bonding technology is to protect low-melting point and reactive metals from being oxidized, by forming an intermetallic compound. During bonding, the low-melting point metal will diffuse through the intermetallic compound layer to react with remaining metals and form a void-free joint as illustrated in Figure 6.4. The bond was formed at 200°C under a hydrogen environment in 10 minutes.

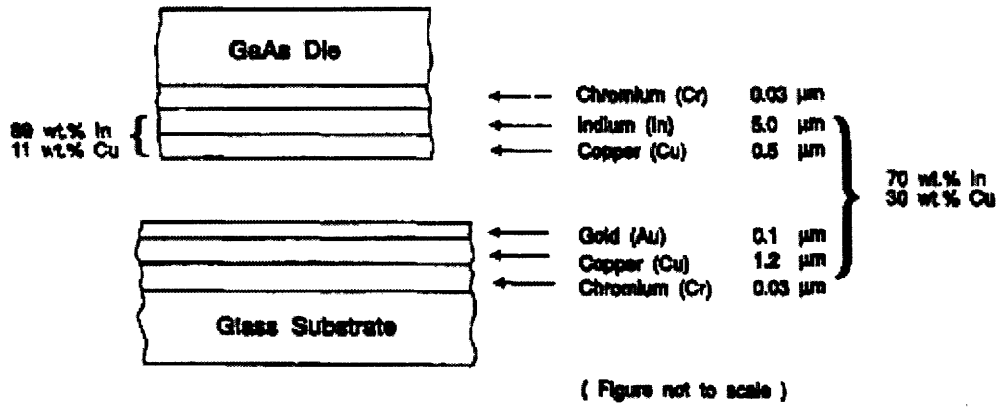


Figure 6.4: Dies with multi-layer structure used by Chen et al. [99].

Previous work has examined copper-indium bonding, showing that it functions well for the films that are several micron thick [95],[99]. In the coming section, we describe the low-temperature copper-indium bonding experiments conducted at MIT, using sub-micron thick films. The goal is to evaluate whether or not a copper-indium bond can be used for wafer-level bonding in 3D IC with a 3D contact pitch less than 5 µm. For this reason, multi-metal stack used in these experiments is less than 1 µm.

6.3 Experimental Procedure

The aim of these experiments is to evaluate the feasibility of bonding copper-indium at 200-250°C. All experiments are conducted on 150 mm Si (100) wafers. A 0.5 µm of wet oxide is grown on the wafers for all experiments. The metal films are deposited using electron beam deposition, which is a form of physical vapor deposition. The deposited films are bonded using an EVG 501 bonder (description in Chapter 3) and then annealed in a diffusion tube. There are no active circuits present on the wafer. Blanket films are bonded, since the main objective is to investigate the bonding interface and determine if a reliable bond can be made. Two different kinds of film stacks are considered and described in this section.

6.3.1 Fabrication of Bonded Pairs

Our experiments can be divided into two parts. The first involves film deposition and the second involves bonding. 150 mm silicon wafers (100) are cleaned in RCA using SC1 and SC2 with an HF dip in between. A 0.5 μm thermal oxide is grown on cleaned wafers using wet oxide recipe in a furnace as explained earlier in Chapters 4 and 5.

E-beam Deposition

Electron beam deposition is used to deposit multi-stack blanket metallic thin films, at pressure below $2x10^{-6}$ Torr. The desired metal is purchased from vendors such as Kurt J. Lesker, in the form of small pellets with 99.99% purity. Four different kinds of metals can be deposited using the apparatus without exposing wafers to the atmosphere; this enabled multi-layer metal stacks to be developed.

Two kinds of stacks are deposited. In one, indium is deposited last, with thickness in the range of 300-550 nm. In the other stack, the indium layer is capped with copper in order to prevent indium from oxidizing and to investigate fluxless bonding. Figure 9 illustrates the two different stacks used for this experiment; these are referred to as the TCI and TCIC stacks. The TCI stack consists of tantalum/ copper/ indium with thickness of 50/100/300 nm as shown in Figure 6.5 (a). The TCIC stack comprises tantalum/ copper/ indium with 50/200/520/80 nm thickness as shown in Figure 6.5 (b).

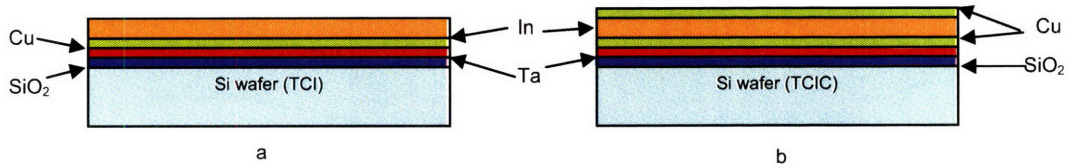


Figure 6.5: a) Ta/Cu/In stack (TCI). b) Ta/Cu/In/Cu stack (capped with copper) (TCIC).

Thermo-compression Bonding

In the second part of the experiment, the wafer with the copper-indium layer is bonded to another wafer that has a tantalum/copper layer only. For bonding, the EVG 501 is used as discussed in Chapter 4 (see Figure 4.3).

Thermo-compression bonding has various parameters, such as temperature, time and pressure. In this work, we focus only on bonding temperature, which is determined by bonding pairs at different temperatures, starting from 160°C to 250°C, with incremental increase of 10°C. We find that 200°C is the lowest temperature at which the two wafers can bond successfully.

6.3.2 Sample Preparation for Bonding Interface Characterization

The bonding interface is characterized using cross-sectional SEM images. The images are usually taken with the help of FIB-SEM. The advantage of using FIB-SEM is that one can obtain a freshly cleaved surface with minimal film damage. The FIB-SEM samples must be thinned to obtain good images; we use grind back followed by wet silicon etch using either TMAH or plasma silicon etch, as described in Chapter 5. Figure 6.6 show a schematic of a thinned wafer bonded to another full-thickness wafer, using a copper-indium stack.

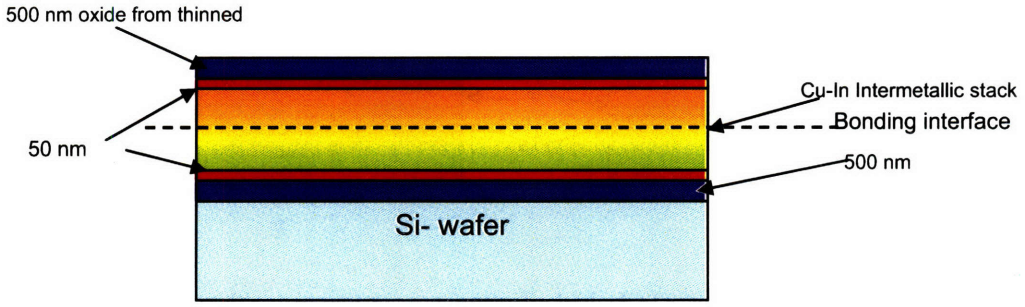


Figure 6.6: Schematic of thinned copper-indium bonded wafers

The main objective is to evaluate differences in microstructure because of composition or copper capping. The 150 mm wafers are bonded at 200°C for one hour with 6000 N down force and annealed for four hours at 230°C in a tube furnace in an N_2 environment. Figure 6.7 (a) and (b) shows a photo of the thinned-back wafer stopping on the thermal oxide. The thinning back is uniform with minor delamination on the TCIC bonded stack.

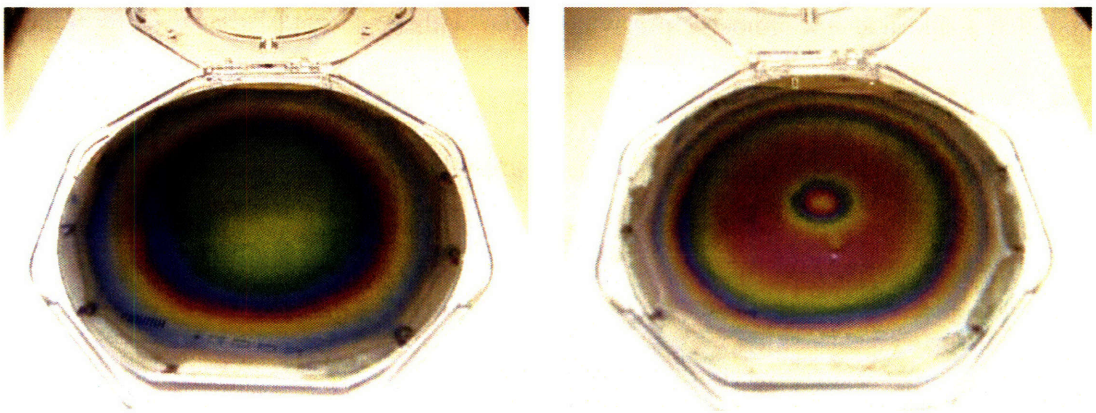


Figure 6.7: Thinned back wafer using mechanical grind back followed by dry-etch using SF_6. Wafers are bonded at 200°C and annealed at 230°C. a) TCI film bonded to TC stack b) TCIC stack bonded to TC.

TMAH is not very selective to indium. Thus, for this experiment plasma etch (SF_6 etch in STS) is used. The wafer is thinned to 100 μms using mechanical grind back (by Silicon Valley Microelectronics). The total stack thickness is reduced to 775 μm, where wafer thickness is 675 μm. For the removal of remaining silicon, STS plasma-etch is used for this etch process. It is not very selective to oxide, especially at the edge of the wafer, so metallic layers are exposed at the wafer edge.

6.4 Bonding Interface Characterization

In order to characterize the bonding interface, bonded pairs are thinned as shown in Figure 6.7. The structural integrity of bonding interface is characterized using FIB-

SEM. Chemical analysis of bonded interface is conducted using scanning transmission electron microscopy (STEM).

6.4.1 Structural Characterization

The cross-sectional FIB-SEM (Figure 6.8 a) shows that there are large voids present along with some small voids, in the TCI bonded stack. These voids can be an issue for bonding reliability and repeatability. Some of the voids span across the whole bonded stack, and are almost 2 μm wide. Even with these voids, the wafer is thinned successfully to 0.5 μm thick oxide remaining. All grains are seen to be as wide as the bonding interface, with grains beginning to grow horizontally because of annealing as shown in Figure 6.8 (b). There is no apparent bonding interface.

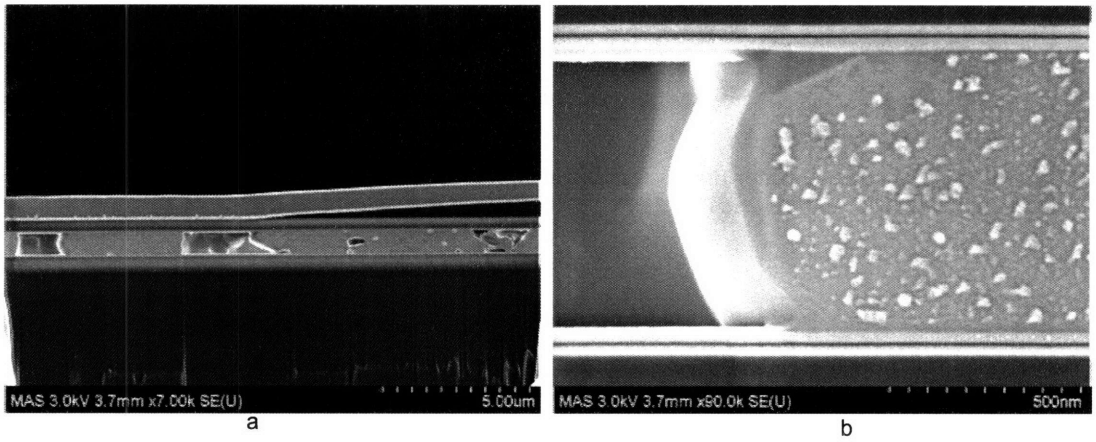


Figure 6.8: TCI bonded to TC a) overview of FIB-SEM. b) Void across 600-nm wide bonding interface and single grain is present across the whole bonding interface. Nano-particles observed in FIB-SEM are because of gallium milling, as gallium likes to attach itself to indium.

Figure 6.9 shows the cross-sectional SEM of TCIC films bonded to a Ta/Cu (TC) stack. Figure 6.9 (a) shows a long-range cross-section, providing a 20 μm long view. Figures 6.9 (b) provides a closer view of the bonding interface. This interface also has many voids, but, the voids are different in nature as compared to those in the TCI-TC. There are no voids that span the whole bonding interface; rather voids are predominantly

located on the thinned wafer, i.e., the wafer on which we had the Ta/Cu stack. In this sample again, no interfaces that marks the bonding junction. The grains spanned across the entire bonded region from one wafer to the other.

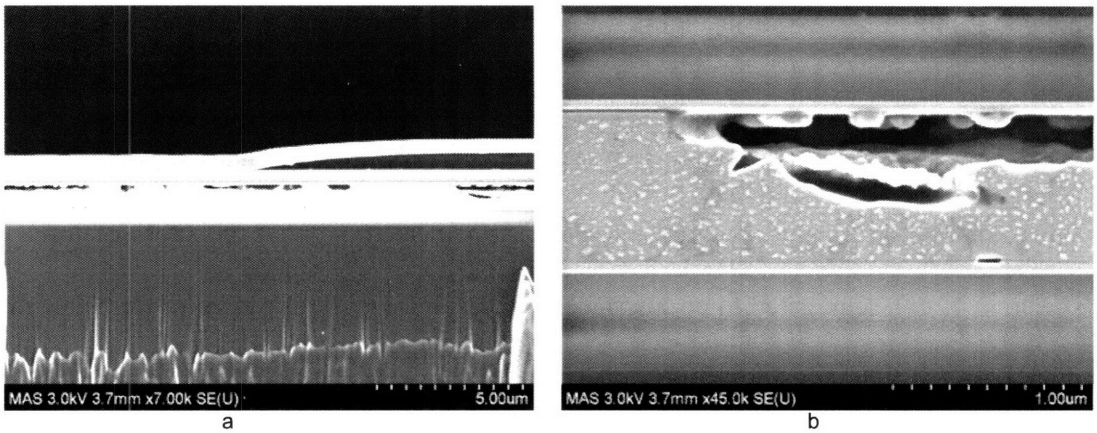


Figure 6.9: Bonded TCIC film to TC at 200°C. a) Overview of FIB-SEM. b) Voids are located on the TC wafer, and are almost 2-3 μm wide. Grains are also large, and appear to have grown in the horizontal direction.

Both bonded sample FIB images show nano-sized particles on their surface. On further analysis, we found gallium metal stuck to indium layer during milling to form a Cu-In-Ga compound.

In the previous studies reported by Bernstein [95] and Lee [99], they never reported voids in the copper indium bonding interface. Both of these studies were conducted with larger film thicknesses.

6.4.2 Chemical Characterization

The bonding interface is characterized using SIMS and STEM. SIMS provides depth profiles of each of the elements using mass spectrometry during sputtering of the bonded film. STEM also provides elemental information, by analyzing the characteristic

x-rays produced by the sample. The goal of our characterization is to identify intermetallic compounds formed during bonding.

SIMS did not yield good results, primarily because of the porous nature of these bonded samples, as shown in Figure 6.8 and 6.9. It appears that copper and indium are well distributed within the stack. To gain more knowledge about the chemical segregation of copper and indium, STEM can be used for microanalysis on an exquisitly fine scale, and is capable, theoretically at least, of detecting about one atom of foreign specie in 1,000, segregated to an interface. The computer system can generate elemental maps of samples, illustrating the distribution of elements. Our STEM analysis is conducted at the Center for Materials Science and Engineering, at MIT with the help of Dr. Anthony Reed. VG HB603 STEM, an advanced analytical electron microscope operating at 250KV, that a field-emission electron gun, large angle x-ray detector and a parallel-detection EELS system (PEELS).

In terms of sample preparation, STEM requires a thin membrane (70-80 nm thick) attached to a copper grid for analysis. To prepare this sample, a piece from a thinned wafer is obtained and milled using focused ion beam, to form a thin membrane of 70 nm thick and 8 μm wide. This sample preparation was conducted at the Center for Nanoscale Systems at Harvard University with the help of Dr. Richard Schalek. Once the membranes are formed, they are attached to the copper grid and elemental maps are produced using the STEM, along with a high resolution image of the bonded stack. Energy dispersive x-ray spectroscopy permits elemental identification and compositional analysis. We are going to publish the elemental maps produced using the VG STEM

(Figure 6.10 and 6.11). The main objective, as mentioned earlier, is to understand if micro-segregation of indium in the bonding interface exists.

Figure 6.10 shows the elemental maps of the TCI bonded film. In these maps, each point represents copper, indium and tantalum atomic species. This technique has a resolution of 0.1 nm, which is fairly precise. These maps are populated by acquiring data over a period of 10 minutes (this is a long time to remove the noise). Figure 6.11 shows elemental maps and annular dark field image of the TCIC bonded stack.

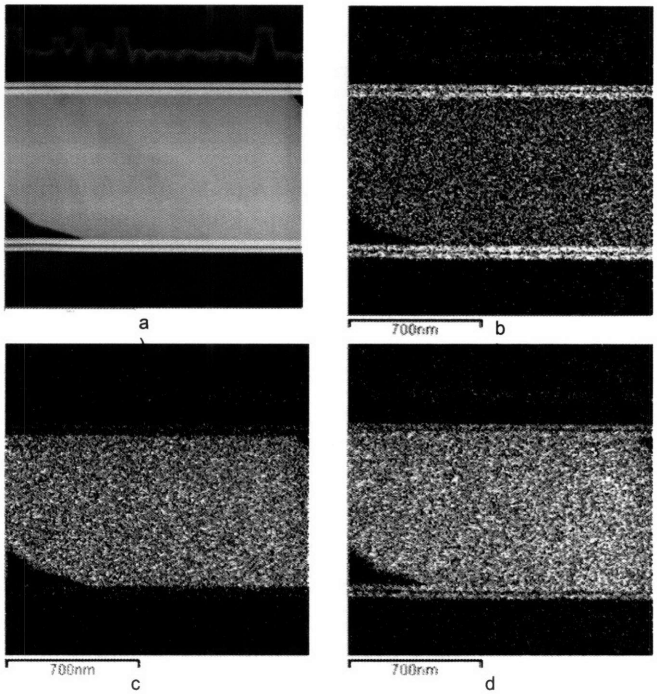


Figure 6.10: STEM images of TCI bonded sample. a) Annular dark field image of bonded stack which shows three different grains from one layer to another. b) Elemental map of Ta. c) Elemental map of indium. d) Elemental maps of copper.

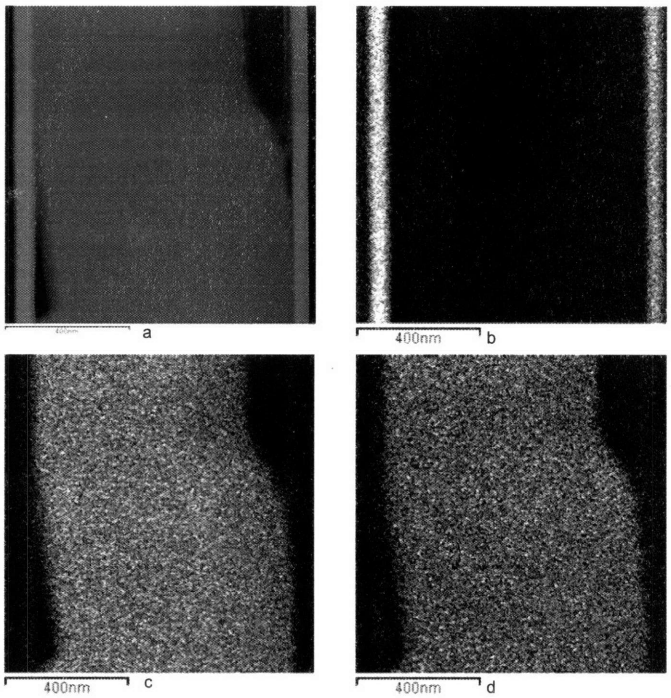


Figure 6.11: STEM images of TCIC bonded stack. a) Annular dark field image of bonded stack. b) Elemental map of Ta. c) Elemental map of In. d) Elemental map of Cu.

Elemental maps of copper and indium in both bonded samples indicates that these films are homogeneous. This data agrees with what we have observed in SIMS. Even along the grain boundaries, there is no apparent change in composition. Line scans are conducted, as shown in Figure 6.12 for both bonded samples to understand if segregation along the grain boundaries occurs. If one looks at the high resolution image of the TCI bonded sample, it appears that there may be some ordering present, since a laminar kind of structure is observed (Figure 6.12 a). But if we look at the concentration line on the right graph (Figure 6.12 b), it appears that only noise is present, but no pattern.

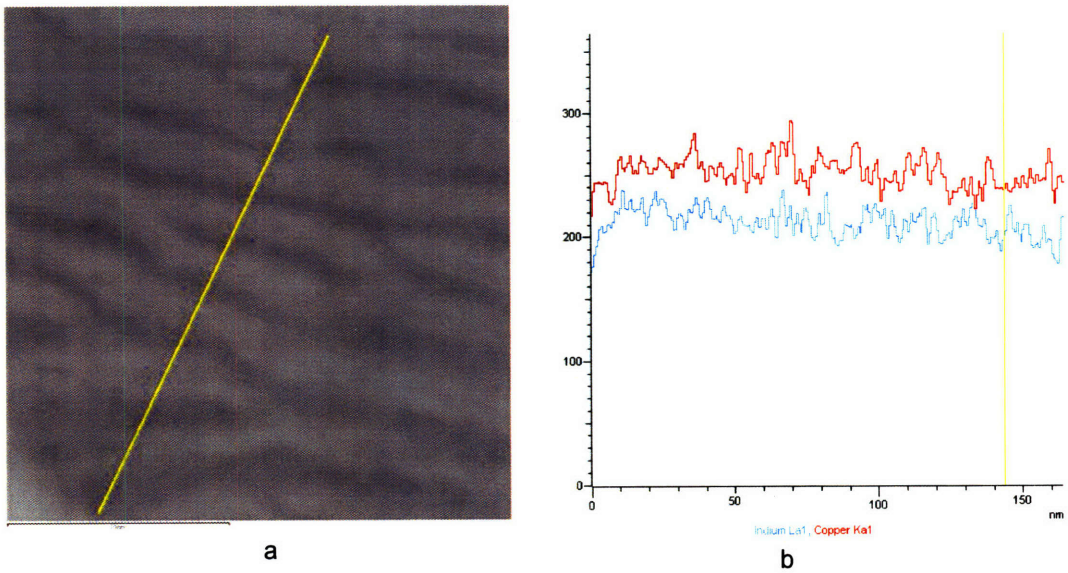


Figure 6.12: a) High resolution image of TCI bonded sample. Yellow line shows the points at which the scan is conducted, resulting in the graph at the right. b) Concentration profile of copper and indium atoms across that line shown in (a).

The only location where one can observe a change in the relative composition between copper and indium is at the surface of the voids. Figure 6.13 shows an example of the dimensional measurement obtained from various points in the area of interest of the TCIC bonded sample. Table 6.1 presents the normalized atomic concentrations present at each site, denoted in Figure 6.13. To our surprise, no oxygen, only sulphur is found in all of the films. This may be due to contamination during sample preparation, or may be due to the external environment. Spectrum 4 is the only outlier in the four different spectra collected. All others lie in a range where copper is between 60-50 atomic percent and indium is 40-50 atomic percent. Spectrum 4 is from a spatial location that lies very near to the Ta layer (of the TC stack) and at the surface of voids in the specimen.

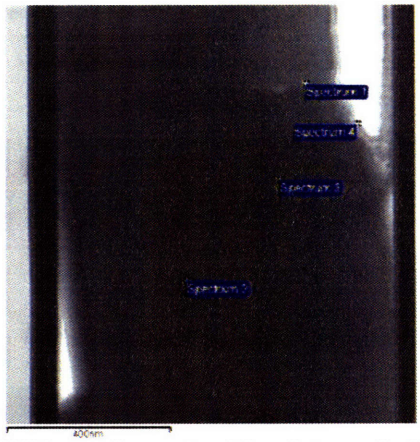


Figure 6.13: ADF image of TCIC bonded sample with points marked which are quantified in Table 6.1.

Points of interest as marked on the map	S (at%)	Cu (at %)	In (at %)
Spectrum 1	1.63	52.96	45.41
Spectrum 2	2.43	57.79	39.77
Spectrum 3	0.9	51.73	47.36
Spectrum 4	3.25	80.13	16.62

Table 6-1: Normalized atomic concentration of respectively marked points in Figure 6.13.

STEM element maps show that Ta is a good diffusion barrier because there is no copper and indium found in the oxide stack beneath Ta. Copper and indium are distributed evenly across the bonding stack. There is no segregation, in agreement with SIMS results. Copper and indium are present in the ratio of 11:9, which suggests either $Cu_{11}In_9$ or perhaps CuIn is formed. Another important observation is that there is no oxygen found in the bonding interface indicating that indium oxidation is not an issue. This result is in agreement with both SIMS and STEM.

To enhance our understanding of the bonding process, we next consider multi-layer films of copper and indium using different characterization techniques.

6.5 Characterization of Multi-Layer Copper-Indium Stack

Thin films of Cu-In alloys have been of substantial interest to industry because the chalcogenization of this alloy produces chalcopyrite semiconductors ($CuInSe_2$, $CuInS_2$, and so on) that are suitable for photovoltaic applications (solar cells). A two-step technique for this application invloves deposition of precursor Cu-In (1:1) film, and then chalconegization, has been very well-studied since the late 1980s [101],[102]. This system is still attracting interest because it is a good candidate for the low-cost production of large area devices.

Since the technique was discovered, there have been several studies in the literature to understand the microscopic uniformity and growth of the intermetallic phase. There are various ways in which these films can be deposited, such as evaporation [102], electrodeposition [102] and sputtering [103]. The roughness and morphology of the films are dependent on the deposition process [103], composition [104],[105] and deposition temperature [104]. Even though, Chen et al. [103] have shown that sputtering is able to provide microscopically smooth films, evaporation has been the major deposition method, primarily because of the ease of deposition.

In our experiments presented below, the evaporation technique is used, as described earlier in Chapter 4. In our set-up, we are unable to control the substrate temperature. The maximum temperature observed for this PVD technique, as reported by Tan, is 70°C, particularly for this specific tool. Our films are deposited without breaking the vacuum. For our study, we explore two different stacks, TCI and TCIC, which are used previously in our bonding experiments. Later, other films are evaluated to probe for any difference if another diffusion/adhesion barrier, such as Cr, is used instead of Ta in

Section 6.7. The different characterization techniques such as SEM, XRD and XPS, along with SIMS, are used to understand the film morphology and composition.

6.5.1 Structural Characterization

Figure 6.14 (a) and (b) shows cross-sectional FIB-SEM images of our TCI and TCIC films conducted at Materials Analytical Services, Rayleigh. Form visual inspection of the wafer we observe that both films are very rough, and in agreement with SEM images. TCI films forms hillocks with a maximum width of about 2 μm. TCIC film forms hillocks which also have voids in them; these hillocks can be as wide as 5 μm.

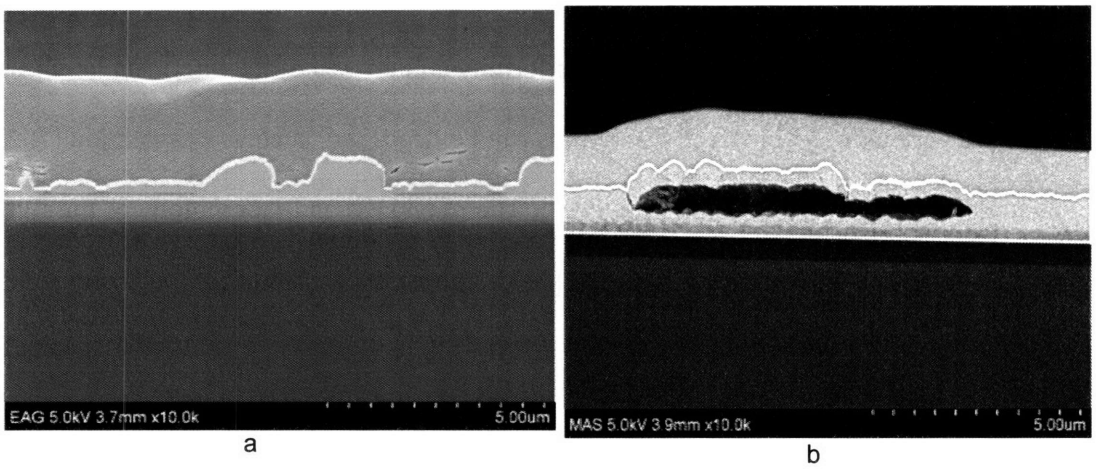


Figure 6.14: Cross-sectional FIB-SEM images of a) TCI film. b) TCIC film.

Other researchers have noticed roughness in Cu-In films, and have sought to understand and find ways to reduce the roughness. Nakano et al. [105] studied the roughness evolution of thin copper-indium films with varying concentrations of indium, compared to copper, and also the roughness dependency on substrate temperature during deposition. They showed that roughness increases with increasing indium concentration with a constant slope until the In:Cu ratio becomes two, then at which point is sudden increase in roughness because of the formation of $CuIn_2$ islands. Basol et al. [107] found

a roughness dependence on the interface, and introduced a new element, Te, to form less Cu-In films.

The general understanding of the morphology evolution of copper-indium films, so far, is that when indium is deposited on copper using evaporation with a deposition rate somewhere between 10-20 nm/min, indium atoms diffuse through copper grain boundaries and form copper intermetallic compounds, such as $Cu_{11}In_9$, CuIn, and other copper rich compounds. This mechanism has been proposed by Basol [107] and Roy [108]. Nankano et al. [105] proposed that copper atoms also need to diffuse, otherwise all intermetallic compounds will be limited by the supply of copper from the underlayer. According to this theory, the way to achieve smooth films is to either reduce the mobility of indium atoms by decreasing the temperature, or to reduce grain boundaries in the underlying copper film. Gossla et al. [104] has demonstrated that if one reduces the substrate temperature to -175°C, it is possible to attain a really smooth film by evaporation. The other possible approach is to anneal the copper film before depositing the indium layer which can minimize the copper grain boundaries. Sputtering also enables to form smooth films primarily because it does not provide enough time for mobile indium atom to diffuse because of its high deposition rate.

6.5.2 Chemical Phase Identification

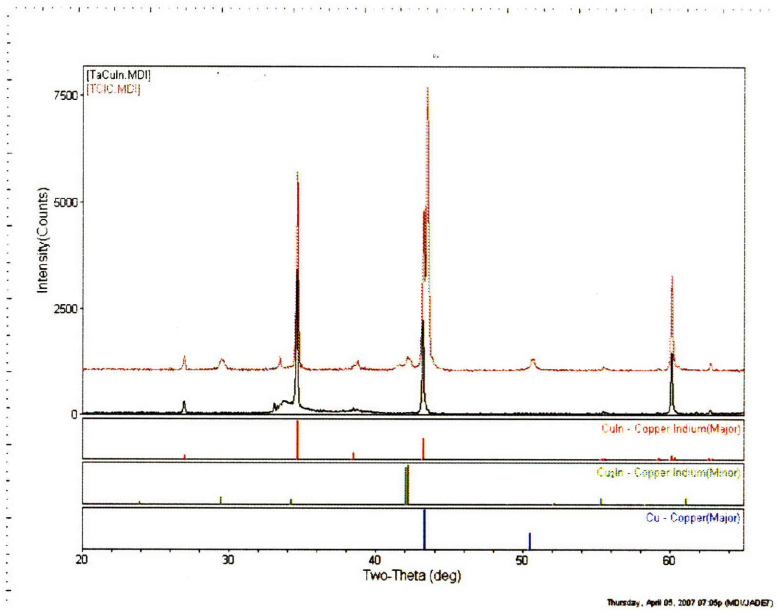
Several efforts have been reported in the literature to characterize copper-indium multilayer stacks. For solar cells applications using a two-phase process, copper-indium precursor films are required with a Cu:In ratio close to one and, uniform in chemical composition. In 1980 Simic and Markinovic [106] identified a new phase CuIn, which does not exist in the phase diagram, and several researchers since then reported

observation of this phase [105],[107],[108]. Roy et al. [108] used electrical resistance measurements to study phase evolution from room temperature to 432 K, and identified CuIn as a primary phase for the configuration, in which indium is on the top of copper. Lindhal et al. [136] completed a quantitative investigation of copper-indium multilayer thin film reactions using differential scanning calorimetry (DSC) along with other characterization techniques to understand phase reactions.

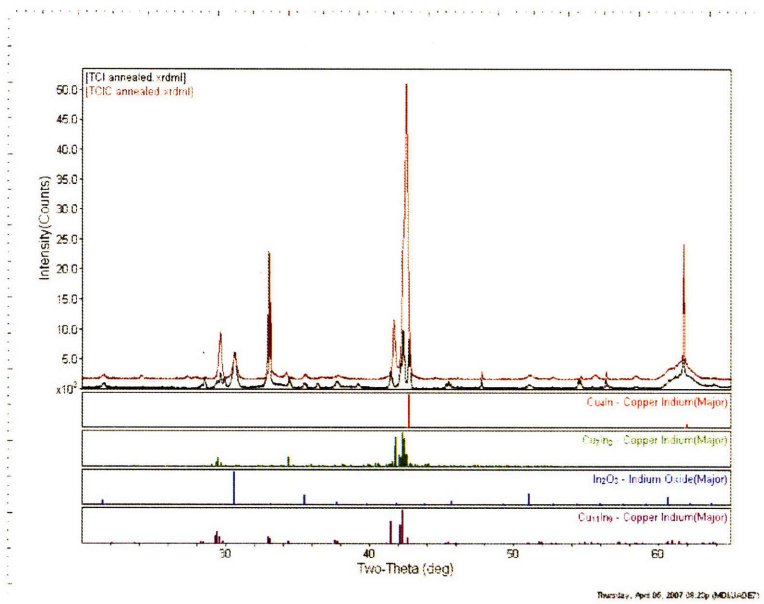
X-ray Diffraction

In our study, we used x-ray diffraction (XRD) to identify different phases in the copper-indium as-deposited and annealed films. The Rigakau RU 300 XRD tool is used to characterize the films. SIMS and XPS were used for depth profiling. Because of a lack of copper-indium XPS data, we could not identify chemical composition.

X-ray diffraction analysis of our two films deposited film stacks, both before and after annealing, is preferred to identify the identical phase in each case. Figure 6.15 (a) shows the XRD pattern of both as-deposited TCI and TCIC stacks while Figure 6.15 (b) shows the pattern for films annealed in a forming gas environment for 250°C for 4 hours.



a



b

Figure 6.15: XRD pattern of TCI and TCIC stacks. a) As-deposited film. b) Annealed for 4 hours in forming gas environment at 250°C.

In the case of as-deposited films (Figure 6.15 a), CuIn is the only phase found in the TCI film, while the TCIC film has traces of Cu and Cu_2In. The results appear to be in agreement with cross-sectional SEM analysis which shows that the TCI film is homogeneous. While TCIC SEM image confirms the presence of more than one

compound in the sample which can be confirmed by XRD which shows presence of copper and copper-rich phases such as Cu_2In.

In annealed films (Figure 6.15 b), CuIn which is the meta-stable phase appears to have dissolved. Many small peaks are observed which could not be identified. $Cu_{11}In_9$ and In_2O_3 is present in both films, while the TCIC stack has more copper rich compounds such as Cu_7In_3 and Cu_4In in small traces which is consistent with as-deposited stack.

6.6 Void Formation

The TCI film does not have any voids but is very non-uniform and rough, as observed in the SEM image (Figure 6.14 a). The In:Cu raio for this film is around 1.4, meaning the indium is approximately 60 atomic percent. According to Nakano et al. [105], at 60 atomic percent, the copper indium film should be filling the valleys between the islands.

In the case of our TCIC film, because of the further deposition of copper as a cap layer, care must be taken to interpret our images. If one observes the FIB-SEM of the TCIC film (Figure 6.14 b) closely, two different layers can be seen. It appears that two different compositions are present, as confirmed by XRD. The copper deposited as a cap layer in TCIC appears to have been annihilated by indium interdiffusion. Another interesting observation is that a crack is present on the left side of the void in Figure 6.14 (b). After much discussion with FIB-SEM specialist, we come to the conclusion that this crack is not an artifact produced FIB. This suggest that there can be substantial stress induced either during the deposition of the capped layer, which might result in voids. Therefore, it does not appear to be a good idea to deposit copper for the capping layer, especially when there is no oxygen found in the bonding stack.

Two different kinds of voids are formed in the TCI and TCIC bonded samples. The TCI film has regular islands and valleys as seen in Figure 6.14 (a). It is proposed that CuIn islands or hillocks will react with other copper layers and will grow, depleting the valley and resulting in voids which span across the entire bonding interface. The TCIC bonding stack has large voids present, similar to those in its as-deposited stack, which suggests that copper has diffused from the other wafer (TC stack) into the bonding layer. In this hypothesis, there is an assumption that not only does indium diffuse into copper, but also copper diffuses into indium, at a very fast diffusion rate at bonding temperature of 200°C. This explains the absence of copper on the thinned TC wafer in the TCIC bonded stack.

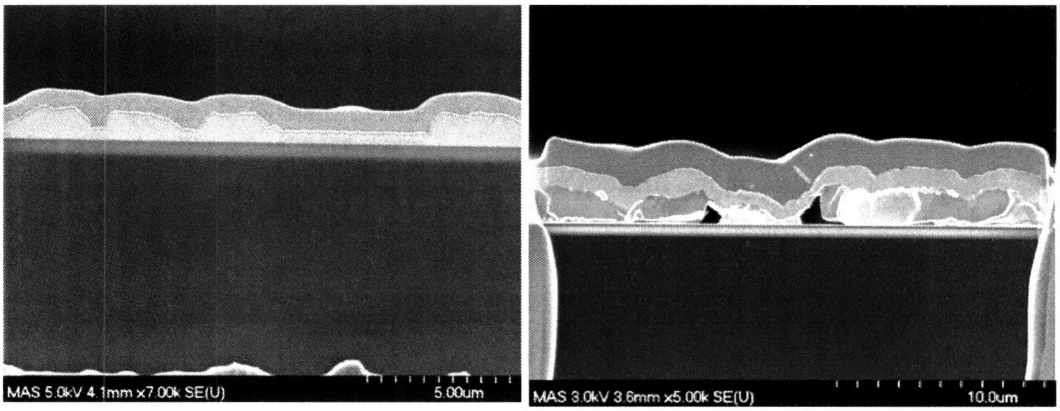
Another possible explanation for the large voids in the TCI film, is that the film melts completely during bonding. Once the film melts, the constituents will diffuse into the copper film and also melt the copper stack. Both become completely molten, and during solidification large voids may form because of the interfacial energy. In the case of TCIC films, even though the In:Cu ratio is similar to that in the TCI film, its relatively large mass (thick) makes two-layers possible, such that diffusion is not complete. Thus, during bonding the films may be diffusing rather than melting.

6.7 Other Alternatives

In this section, we describe other approaches we explored in an attempt to obtain smooth deposited films of copper-indium. First, we consider an approach using chromium instead of tantalum as a diffusion barrier. Second, we electrodeposit indium films on copper rather than use e-beam evaporation.

6.7.1 Chromium –Diffusion Barrier

Lee et al. [99] reports the use of chromium as the diffusion barrier with good bonding results. Basol [107] has shown that having Te over Mo helps to smooth films. Our study we use the same TCI stack as described in Section 6.3 but instead of using tantalum, we use chromium resulting Cr/Cu/In stack with 50/100/300 nm thick films. However, no improvement in morphology, as seen in Figure 6.16 (a). The bonded sample is still full of voids (Figure 6.16 (b)). One additional stack was tried, with a thicker indium film (1200 nm) deposited on chromium; in this case we deposit Cu on the top by sputtering using a Perkin-Elmer tool. Using this composition, it is hard to obtain a continuous film. Figure 6.16 (b) shows that sputtered copper is continuous over discontinuous indium. Bonded stack of both composition demonstrate bonding interface full of voids.



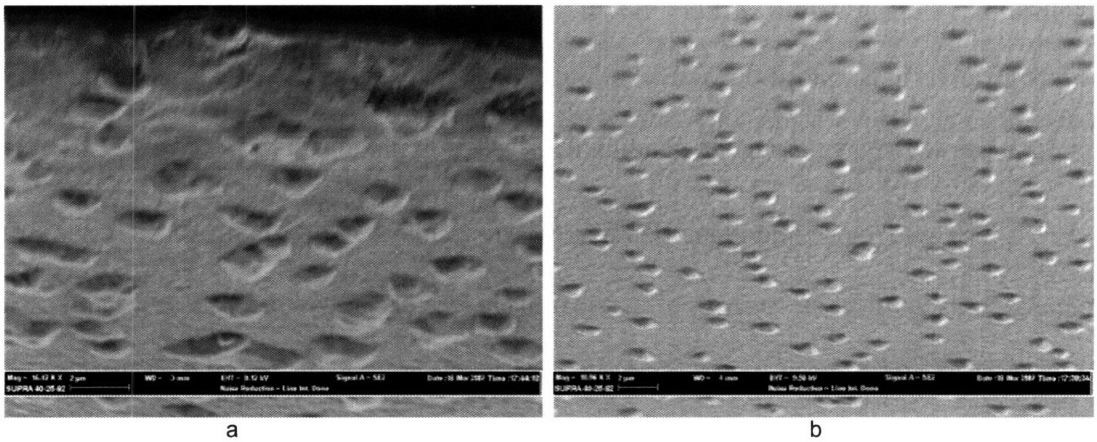
a b

Figure 6.16: FIB-SEM of Cr/Cu/In stack (50/100/500 nm). b) FIB-SEM image of Cr/In/Cu stack with 50/1200/200 nm.

6.7.2 Electro-deposition Indium

In order to obtain a continuous smooth surface, we also investigate electro-deposition of indium on copper using a sulfamic acid bath. The electroplating kit is obtained from Indium Corporation [127], which contains the solution and anodes. DC

settings are used to deposit the indium film. Figure 6.17 (a) shows an SEM of a thick deposition of indium on a 3.5 μm copper film, while Figure 6.17 (b) shows an SEM image of a thin deposition of indium on a 300 nm thick copper film. Both images are similar, with the same kind of hillocks structures as observed using e-beam deposition.



a b

Figure 6.17: a) SEM of thick indium deposition on 3.5 μm copper layer. b) Thin indium deposition on a 300 nm copper.

6.8 Summary

With the goal of lowering the permanent bond temperature to enable alternative handle wafer approaches such as smart cut and adhesive bonding, we investigated copper indium SLID bonding using sub-micron stack thicknesses. We find that copper stack can be bonded to a multi-stack copper indium film, at 200°C in an EV501 bonder using 6000N force for one hour, with blanket films on 150 mm wafers. The bonded wafers were successfully thinned using grind back followed by TMAH etch. On careful inspection, however we find that the interface contains several voids, where the void size can be on the order of film thickness. The presence of these voids pose a problem for reliability, and are not acceptable.

Thin copper-indium stacks are further studied to understand void formation. We find that indium, when deposited on copper using an e-beam or other PVD technique, result in a rough film, which contributes to voids in our films. At the same time, indium diffuses into copper quickly, sub-micron stacks even in as-deposited form prior to annealing form a CuIn solid solution. STEM analysis shows that the films are homogeneous in composition, and with low oxygen content, with no evidence that copper indium has segregated along the bonding interface or grain boundaries.

The two most important requirements to achieve good bonding using a SLID approach is to deposit smooth films that have the desired copper and indium rich composition. Both are believed to be achievable with sputtering, which has a faster deposition rate, and in turn, provides a less time limiting diffusion of the indium during deposition. Future work should thus examine the opportunity for solid liquid interdiffusion of sputter-deposited indium and copper thin films, given their potential to substantially reduce the temperature required for permanent bonding in 3D IC technology.

Chapter 7: Overall Comparison of Handle Wafer Options

This chapter presents an overall comparison of the different handle wafer options described earlier in this thesis. By overall comparison, we mean assessment of combined performance, cost and environmental considerations. The main objective of this chapter is to demonstrate this comparative methodology, presented in Chapter 2, in the next case of 3D IC handle wafer options.

In Chapter 2, we compared the MIT 3D integration approach and process flow with an existing standard 2D CMOS flow, and established that the handle wafer process is the critical technology which requires deeper study because of its performance, cost and environmental concerns. In Chapter 3, we reviewed existing handle wafer options, and discussed the requirements for improved handle wafer solutions. Two distinct handle wafer release methods were discussed in Chapters 4 and 5; in Chapter 6, we discussed an alternate permanent bonding technology to enable greater thermal process flexibility in handle wafer integration. Now, in this chapter we assess and compare two previously developed handle wafer approaches, together with two new approaches described in Chapter 4 and 5; this comparison is on all thee aces of environmental impact, perfomance and cost in order to understand the strengths and weakness of each approach.

7.1 Introduction

Handle wafer options described earlier in thesis are compared with two other options proposed by Fan [58] and Tan [33],[57] at MIT. We consider these two previously existing options in part because we have process information available for these two processes, and the assessment methodology used is highly dependent on

process data. The four handle wafer processes are scaled to a full-scale manufacturing model in order to understand the impact. Most of the analysis considers different handle wafer options that are still at the proof of concept stage, so it can be difficult to comment about final yield. However, we use the different factors and requirements for the handle wafer process outlined earlier in Chapter 3, together with knowledge gathered during processing and experimentation, to help estimate yield and performance. Performance comparison for the four handle wafer options are presented in Section 7.2.

In absence of publicly available process-based cost models, it is difficult to estimate the cost for our different options. Nevertheless, we provide the key factors and a framework to make a rough estimate about the cost of the different options. In particular we will see that cost depends on the number of new processes and new infrastructure needed for the new technology, and the expected wafer throughput. Cost comparison for the handle wafer options are discussed in Section 7.3.

To assess the environmental impact, different handle wafer options are assessed using our comparative methodology. All approaches are considered at the unit process level, enabling us to ignore those steps that are common to all four options, such as thinning. The remaining unit processes are divided into three groups depending on whether they performed on the handle wafer, the device wafer or on the bonded and thinned stack. These processes are either estimated using process based knowledge or using out environmental inventory database. Results for energy and water consumption, along with trends in chemical and effluents, are summarized in Section 7.4.

Finally, an integrated comparison of the strengths and weaknesses of the four handle wafer options is summarized in Section 7.5.

7.2 Performance Comparison

The handle wafer or support wafer's main function is to enable the transfer of the thinned device layer to a 3D stack, as explained earlier. Ideally, the handle wafer process, should not affect or impact any electrical performance characteristics of the final product. But this process can impact the overall yield of 3D ICs. Here, yield can be defined as the number of wafers that can be thinned and transferred successfully without any defects. Potential defects include: mechanical defects, such as delamination and voids; chemical defects, such as low selectivity; and functional defects, such as failure to release.

All of these defects can be characterized with the help of six factors mentioned in Chapter 3. The factors are bond strength, void formation, chemical selectivity, thinning capability, thermal tolerance and ease of release. For all of the chemical release methods, ease of release parameter can be further divided into chemical selectivity for release and time for release.

In this section, we present a brief discussion of these six factors under three categories, mechanical, chemical and functional, for the different handle wafer options. The mechanical aspects include bond strength, void formation, and thinning capability, while the chemical aspects consist of chemical selectivity and thermal characteristics. Functional aspects will focus on effectiveness of the handle wafer release. In the end of the section, results are tabulated to bring together perspectives about the different processing options.

Aluminum Release Layer

Fan [58] proposed a laminated structure for the handle wafer with a 20 μm Al release layer on both handle wafer and device wafer, as described in Chapter 3

(Figure3.1). The aluminum release layer approach suffers from mass transfer problems and is not able to release 150 mm wafers, therefore it will be hard to project that it will be possible to achieve any substantial yield on 300 mm wafers.

Mechanical: Copper-copper bond toughness is approximately 3 J/m^2 depending upon surface conditions and deposition technique [[59]]. The thermo-compression copper bond is insensitive to surface contamination and has few voids. The bond works well, and SOI device wafers can be thinned down to a buried oxide layer, e.g. with 200 nm of silicon remaining without any delamination. Potentially, problems may arise because of the large wafer bow associated with 20 μm thick layers of aluminum [58].

Chemical: The process benefits from a large processing window in terms of temperature operating range. The strong metallic bond and high modulus metallic release layer results in easier thinning. There is no loss in yield during grind-back, but during wet-etch using TMAH, the Al release layer needs to be protected as it is easily attacked.

Functional: Even after five days of soak time, 150 mm wafers are not released successfully; only die-size of 10 mm have been shown to release successfully [58].

Between-Die Channels

The between-die channel handle wafer approach has been discussed in Chapter 4. This is a modified version of the aluminum release approach just described. In this approach, the mass transfer problem is solved by introducing wide channels in the device wafer. This process option can be scaled to 300 mm wafers, as the release time is limited by the die-size rather than the wafer size.

Mechanical: Copper is used for the temporary bond, and as mentioned earlier, achieves high bond strength and few voids in bonded layers. Device wafers can be

thinned to the buried oxide layer without any problem. This approach uses a laminate structure for the temporary bond using only one 8-μm of aluminum on the device wafer, which induces a large wafer bow (130 μm for 150 mm wafers) which can cause difficulty in alignment.

Chemical: As mentioned earlier, this stacking method has a wide temperature range, and is very selective to chemicals used in electroplating and etching. However, minor problems can arise when wafers are exposed to TMAH for a long time such as ten hours, in the case of prototype demonstration.

Functional: The handle wafer can be released successfully from the bonded stack, although it requires at least eight hours for the wafers to be released. The release time is limited by the undercut etch rate, which is around 500 μm/hr in an HCl: H_2O (1:1) solution [63]. This method can be enhanced using ultrasound, increasing the release temperature and adding surfactants or oxidizers. It can be potentially implemented as a batch process, operating on 25-50 wafers at the same time with limited additional cost.

Smart Cut

As described earlier in Chapter 2, Soitec currently uses a smart cut method to manufacture SOI wafers. Tan proposed to use smart cut as a handle wafer release method for back-to-face 3D integration [57]. Since the smart cut process is already being used in the industry for other purposes, it is definitely scalable to manufacturing.

Mechanical: Low-temperature oxide bonding is used as the temporary bond in smart cut approach. As measured on blanket films, the bond energy can be as high as 2 J/m^2 depending upon annealing temperature. The bond is quite strong and can help in thinning of the device wafer. However, bonding also requires surface roughness less than

1 nm, which is a challenge for the whole processed wafer. Plasma-assisted oxide bonding is also sensitive to particles and trapped moisture, and leaves voids, unlike thermo-compression bonding.

Chemical: The smart cut handle wafer option has a small process window in terms of temperature. H_2 activation can take between 250-300°C which can create some issues and constraints for subsequent processes such as permanent bonding. Our preliminary investigation of low-temperature permanent bonding using Cu-In SLID approach has shown that bonding may be possible at 200°C, which is promising result to enable the smart cut handle wafer. Chemicals used in further processing have no effect on bonding and releasing.

Functional: Smart cut release requires thermal activation and can be done in a furnace within 30 to 60 minutes. It is independent of wafer and die-size, unlike the previous two approaches. It is also a batch process.

Oxide Release Layer

Oxide release layer approach is described in Chapter 5. In this approach, channels are etched into the handle wafer to enable the transfer of etchants to the center of the wafer from the bulk. And at the same time, the channels also facilitate the products from the center of wafer back to the bulk bath.

Mechanical: As in the smart cut approach, in this we also use low-temperature plasma assisted oxide bonding. In this option, a blanket oxide film (device wafer) was bonded to the handle wafer with a pad structure encapsulating the channels, and it was shown in Chapter 5 that the bond strength decreases with pad size. In this approach, there is a critical thickness to which wafer can be thinned without any stress and buckling (as

discussed in Section 5.5). There are fewer voids as compared to smart cut which involves bonding without channels because water molecules can diffuse out through the patterned channels.

Chemical: The temperature at which the temporary oxide bond is exposed can affect the release time. Concentrated HF acid does not act as a selective etch chemistry, although it does have a slower etch rate for the sacrificial nitride layer. HF also corrodes metal when exposed for a long time. Concentrated hydrofluoric acid was used in each handle wafer release experiment, with 1 μm thick silicon rich nitride present as a sacrificial layer to protect the oxide interconnect stack. In this thesis, we have only explored concentrated hydrofluoric acid as the etchant (release chemical) in order to show proof of concept, but other more benign chemistries such as buffered oxide etch along with vapor HF, can be used to make this option more viable.

Functional: The handle wafer with 80 μm pads and 40 μm channels, if etched to a depth of 45 μm or greater, can be released within 45 min. In Chapter 5, there are two sets of experiments are tabulated showing the effect of etch depth and pattern size on the release time. Besides these two factors, the release process is sensitive to lithography defects and the temperature at which the oxide release layer is annealed. The handle wafer release yield is low because of the use of concentrated HF and the other issues listed above (as discussed in Chapter 5).

Table 1 summarizes the performance, based on six factors, of the four different handle wafer options.

Handle Wafer Approaches	Bond strength	Void Formation	Chemical Selectivity	Thinning-back Capability	Temperature range	Ease of debonding
Smart Cut	~2 J/m^2 ↑	Few ↔	Good ↑	Good ↑ < 1 µm	< 250°C, Cu-In bonding at 200°C ↔	Good, released in 60 mins ↑
Al Release Layer	~3 J/m^2 ↑	No ↑	Probably with TMAH ↔	Good ↑ < 1 µm	Good ↑	Do not release in finite time ↓
Between-Die Channel	~ 3 J/m^2 ↑	No ↑	Probably with TMAH ↔	Good ↑ < 1 µm	Good ↑	Released in 8 hours ↔
Oxide Release Layer	~1.6 J/m^2 ↑	No ↑	HF acid highly corrosive ↔	Minimum thickness 5-10 µm ↑	High temp. difficult to release ↔	Release in 45 mins but not selective ↔

Table 7-1: Performance comparison of different handle wafer options under consideration. An ↑ indicates relatively good performance, likewise ↓ indicates poor performance and ↔ suggests that performance is okay and can be improved.

7.3 Cost Comparison

In this section, because of a lack of readily available process-based (input–output) cost models for individual unit processes, we detail a strategy and provide relative estimates for different process options as compared to the cost of the standard 2D CMOS. Cost is a strong function of the number of process steps and mask-sets, process complexity and yield. By process complexity, we mean that if the process is new to the semiconductor industry, much process engineering needs to be conducted to achieve acceptable yield. A second factor relates to equipment cost; if one observes the trend in the Sematech CRM model [122], it can be seen that tool depreciation and maintenance costs are the two major costs for almost all processes. Throughput can also become a factor, if processing takes too long to process one wafer at one particular station (especially in the case of single wafer processes).

To estimate the relative variable cost of each handle wafer option as compared to standard 2D CMOS, we make a number of assumptions made about the cost of each fully processed wafer, number of wafer-starts and equipment cost. All these assumptions are outlined below, along with the method which is used to estimate the cost of each process option.

The cost of a fully processed 2D CMOS, 6 metal layers, 300 mm wafer with 130 nm technology node is $4000. In this technology, it is assumed that there are 200 unit process steps including 25 masking steps. Each mask process costs 2% of the total cost. The price for the additional needed equipment including the DRIE etcher, sputterer and bonder, are assumed to be approximately $1M. It is also assumed that they depreciate fully in four years with constant rate. The number of wafer starts will be 2000 per week. There is an underlying assumption in this approach that all handle wafer process options will be developed to an acceptable yield level, so we do not discount any process for its bad yield in the research prototype. Using the above assumptions and our estimated throughput values, we can estimate the relative price for each handle wafer option. The relative value will be the capital expense plus cost of mask and processes.

Al Release Layer

The Al release layer approach requires a 20 μm thick deposition of Al on both the handle wafer and the device wafer, which is later etched away in the release step. In terms of complexity, the process steps are simple, but 20 μm of Al deposition is very expensive in terms of throughput, and can increase the cost of this process by becoming a manufacturing bottleneck. Furthermore, this process is not feasible because the release

process is mass transfer limited; thus this process will not be discussed in the cost comparison.

Between-Die Channels

In the between-die channel handle wafer process, in addition to the deposition of 5-8 μm of Al on the device wafer, one needs to etch through the whole interconnect stack (6-7 layers) to form the between-die channels on the wafer. In addition, the handle wafer also needs 50-60 μm deep channels to be etched. The thermo-compression bonding can cause some throughput concerns. In terms of equipment needs, the 60 μm etching will certainly require a deep silicon etcher, which is not part of the typical CMOS fab, thus requiring additional capital expense. Considering low throughput for 2000 wafers per week, one needs approximately 20 sputter chambers and 20 bonder chambers, each, while 10 DRIE etchers should be sufficient. This process is thus capital intensive as it might require $40M of additional equipment, which will account for 2.5% increase in cost. There are two mask-sets used and 13 unit process-steps, which will contribute to 4% and 6.5% increase in cost, respectively. In terms of process complexity, this approach is relatively simple, and the handle wafer can be reused. Even though releasing has a high yield and can be performed as a batch process, release time is long, requiring 8-10 hours.

Smart Cut

Smart cut is already is use by Soitec to make SOI wafers with low defects, but it is a very expensive process. SIMOX, another way of making SOI wafers using oxygen implantation, has become more successful because of its lower cost. Chediak et al. [137] published in 2002 that the cost for a 300 mm SOI wafer manufactured from SIMOX and smart cut is $1300 and $1800, respectively, for orders less than 1000 wafers. Even if we

assume that high volume manufacturing can reduce the smart cut cost almost in half, the final price for SOI wafers using smart cut will be 6 to 8 times more than the average price of 300 mm bulk silicon wafers which are used in all of the other handle wafer options.

In this process, H_2 implantation is required along with bonding oxide at low-temperature, requiring CMP and plasma activation. The process complexity is relatively modest, as these unit processes are already in the manufacturing stage. Handle wafer release promises high yield and, at the same time, is a batch process that can be conducted in one hour.

For our relative estimate, we will assume high volume implantation of H_2 and assume this will drive the price down to $1000 per wafer. This implies that cost of this option is approximately 25% of the fully processed bulk technology wafer.

Oxide Release Layer

In the oxide release layer approach, channels are etched in a handle wafer up to 50 μm deep using a silicon etcher, which can be an additional capital expense. Wafers are bonded using low-temperature plasma-assisted oxide bonding, a high throughput process. The process is highly complex, requiring a sacrificial layer to protect the oxide in the interconnect stack. This requires substantial process engineering and development. Release is promising, but does not have a high yield in demonstration so far. This handle wafer option needs additional engineering in order to be considered a robust process option. The handle wafer can be reused, however, making this process attractive from cost view point. This process would require an order of ten silicon DRIE etcher and five bonding chambers along with two more nitride chambers for the device wafer. In terms of capital expense, it is not extreme as this option might require approximately $20M

additional capital equipment which will contribute to 1.25% additional cost. There is only one mask-set used and 8 unit process-steps, which will contribute to 2% and 4% increase in cost, respectively.

Table 6.2 summarizes the issues that affect cost, including the need for a new infrastructure, wafer throughput, process complexity, number of steps and masks required. An aggregate cost factor is included, which gives an estimated relative cost of the various handle wafer options. The cost factor clearly illustrates that smart cut is the most expensive process option, followed by between-die channel, and while the oxide release layer approach adds the least additional cost of the options considered.

Handle wafer options	New infrastructure	# of process steps with extra masks	Throughput	New processes/ Process complexity	Cost factor
Between-die channel	Bonder, Sputterer for Al, Si-etcher	13 with two extra mask	Low	8 µm thick Al deposition, copper bonding, silicon etch	1.13
Oxide release layer	Bonder, Si-etcher	8 with one extra mask	Moderate	Silicon etch, oxide bonding	1.08
Smart cut	Oxide Bonder, H2 implanter	6 with no extra mask	Moderate	Oxide bonding, H2 implantation	1.25

Table 7-2: Summary - cost comparison of different handle wafer options.

7.4 Environmental Comparison of Handle Wafer Options

There can be several ways to report an environmental assessment. Yao et al. [[48]] grouped different chemicals as GWG, VOCs, and HAPs. The IZM Tool box [[50]] uses a toxicity potential indicator (TPI), recycle potential indicator (RPI), and other parameters, to show the environmental characteristics of the product. As we discussed in Chapter 2, in our approach we seek to maintain as much chemical specificity as possible, so that we can report the particular chemicals used. In this section, the environmental footprint of the different handle wafer options are calculated, either using standard data or

an estimation for novel processes. This is followed by comparison of energy and water consumption. Finally, the trend in materials consumption and effluents production will be discussed.

7.4.1 Approach and Assumptions

The unit process based comparative environmental impact evaluation described in Section 2.2, can be applied to the current assessment. There does not exist any standard process, so the four different handle wafer options are compared among themselves. The functional unit for this analysis is the addition of a single layer to an already existing 3D IC stack. Each prototype flow is summarized in Table 7.3, dividing the flow into three process modules: 1) handle wafer fabrication, 2) device wafer fabrication, and 3) stack bonding (Table 7.3).

Using the comparative approach, unit processes which are identical across all four process options are eliminated; these include thinning, back-side vias formation, contacts fabrication using copper pads and permanent bond formation. The environmental footprint is generated for the remaining processes, using process based knowledge or our inventory database. The inventory is generated for 300 mm wafers, with a 130 nm technology node. This data set is obtained from tools which are used in high volume manufacturing. Eighty chemicals, including gases and liquids are listed, in this inventory. The database generated for all these unit process steps can be found in Appendix B-E of this thesis.

Different Modules	Al Release Layer	Smart Cut	Between-Die Channels	Oxide Release Layer
Handle Wafer Fabrication	Clean wafers, Oxidation, Barrier deposition, Al deposition, Barrier deposition, Copper deposition	Clean wafers, Oxidation, H_2 implantation, Plasma Activation, Piranha	Clean wafers, Oxidation, Photo – mask #1, Wet etch oxide, Dry etch Si, Remove Photo, Barrier, Copper deposition	Photo -mask #1, Dry etch Si, Remove Photo, Clean wafers, Oxidation, Plasma Activation, Piranha
Device Wafer Fabrication	Barrier deposition, Al deposition, Barrier deposition, Copper deposition	Oxide Deposition, CMP oxide, Plasma Activation, Piranha	Photo – mask #2, Etch dielectric, Etch silicon, Remove Photo, Barrier, Al deposition, Barrier deposition, Copper deposition	Sacrificial nitride deposition, Oxide Deposition, CMP oxide, Plasma Activation, Piranha
Stack Bonding	Temporary Cu bond, Thinning, Making vias, Making Cu contacts, Permanent Cu bond, HCl release	Temporary oxide bond, Thinning, Making vias, Making Cu contacts, Permanent Cu bond, Anneal release	Temporary Cu bond, Thinning, Making vias, Making Cu contacts, Permanent Cu bond, HCl release	Temporary oxide bond, Thinning, Making vias, Making Cu contacts, Permanent Cu bond, HF release

Table 7-3: Unit processes for different handle wafer options.

Two kinds of abatement systems are used specifically for processes described in the handle wafer options. The first is combustion and water scrubbing, which is used for gases that are toxic and flammable in nature. These devices consume methane, air and electricity, and significantly reduce toxicity. The second kind of abatement system is plasma abatement, which destroys perfluorocarbon emissions and reduces the global warming impact of etch and deposition processes. These systems are located before the pump, at sub-atmospheric pressure (one per process chamber). Based on standard

process conditions, for a one minute recipe, plasma abatement would utilize about 0.05 kWh/wafer pass and 200 g water/wafer pass.

The water consumption can be divided into three main categories, depending on where the water is consumed. Ultra-pure water (UPW) is used in the process itself and, as the name suggests, it is high grade deionized water. Ultra-pure water is produced in the fab through continuous cycling of water through a sequence of filter chambers and a reverse osmosis system. Typically, 14 Whr of electricity is required per liter of UPW [54]. Process cooling water (PCW) is utilized in all processes which involves high temperature processing, and is usually recycled by passing through a heat exchanger. Process cooling water is recycled upon return from the process equipment. During recycling, PCW is cooled using a chiller, and cleaned, usually through ion exchange. A typical PCW chiller capacity is approximately 6,000 gpm, and requires 0.91 Whr/liter of PCW supplied [128]. Industrial city water (ICW) is used in all of the abatement processes.

As mentioned earlier, our process inventory maintains an extensive list of approximately 80 chemicals that have been reported as used in approximately 40 unique processes in CMOS processing. In this study, the chemical specificity is maintained, but the chemicals are also identified in six different categories: global warming gases, hazardous chemicals, criteria air pollutants, volatile organic compounds, flammables and other chemicals. During our discussion about chemicals for each handle wafer option, all six categories are addressed.

The data set is compiled for the standard 2D CMOS processes, but the handle wafer options discussed in this thesis utilize require novel processes. Therefore, we need a number of assumptions and approximations as summarized below.

If the desired thickness to be etched or deposited is different from the standard process listed in the database, then process inputs and outputs are linearly scaled with time, depending upon etch and deposition rate.

Some processes are novel, such as bonding and thinning, and are not present in the inventory of a 2D logic device. In that case, these processes are approximated using the knowledge gathered during processing.

It is assumed that each unit process has a point of use abatement system installed along with it, wherever applicable. The energy, water and materials consumption reported here include point of use abatement data. In the same way, effluents stated are after the abatement system.

Wet bench and oxidation are considered to be batch processes, and it is assumed that the batch size is 50 wafers. These processes can often be scaled to 150 wafers, if needed, which essentially means less energy consumption. Wet bench processes include wafer cleaning (RCA, Piranha) and acid release.

In all of the handle wafer options, it is assumed that the device wafer was completed to the last layer, then covered with passivating oxide and polished using CMP so that roughness and global flatness are suitable for oxide bonding.

The energy consumption values are based on the power measurement for that particular tool, along with peripheral equipment such as vacuum pumps. The energy

consumption data also includes the process power, idle power, as well as the power consumed in point of use abatement.

7.4.2 Estimation

In this section, all of the novel unit processes used in the four different handle wafer options which are not part of the gate-to-gate inventory database are estimated, either by finding an analogous unit process, or by extrapolating from research data.

Bonding Oxide and Copper

Two methods are used for bonding of copper and oxide layers. The first method is thermo-compression copper bonding, followed by annealing, and the second method is low-temperature fusion bonding using oxide layers followed by annealing. Bonding is a single wafer pair process. More energy is required in the case of thermo-compression copper bonding, where a single wafer pair is under pressure and high temperature for one hour, than in the low-temperature oxide bonding case which takes place in 2 minutes at room-temperature.

The energy and water consumption for the thermo-compression bonding method can be approximated as being similar to that needed in the copper annealing process requiring 300-400°C for one hour. In terms of material and chemical consumption, this method uses only process N_2 and process cooling water (PCW).

Silicon Etch – Bosch process

In 2D CMOS, the etch depth is usually on the order of a few microns to obtain small features. Etching silicon as deep as 50 μm using the Bosch process in an ICP chamber is a concept borrowed from MEMS. Thus, we do not have any inventory data available for this particular process. Etch rate in deep reactive ion etching (DRIE) is

highly dependent on the loading area. For the between-die channel mask (with exposed area ~1%), the etch rate is approximately 2.0 μm/min, while for the oxide pad mask with loading area as large as 60%, the etch rate is approximately 1.0 μm/min. Thus, the energy consumption is twice as great for oxide-release layer approach as for the between-die channel for similar etch depth.

The power requirement for the Centura chamber to etch silicon, during conventional STI module, is approximately 60 KW. We assume that the power requirement for the ICP chamber is near this level on average. Another assumption is that the ideal energy required will be around 2 KWh, and abatement will not be more than 3 KWh. This makes the total energy around 30 KWh for the between-die channel to be etched 50 μms deep. For etching of 50 μm deep channels using the handle wafer pad mask, the electrical energy consumption will be approximately 55 KWh/wafer.

The bosch process is time multiplexed, using a two stage process with alternating etch and deposition cycles. During the etch cycle it uses SF_6 gas flowing at almost 400 sccm, while in the deposition cycle c-C_4F_8 gas flows at as much as 100 sccm. The time is divided in the ratio of 60:40 between etch and deposition. Using these values, one can calculate the total flow required to etch 50 μm deep channels. The effluents generated by the etch process go through an abatement system which burns high potential GWG using methane and oxygen. In this particular etch, we have assumed that, SF_6 has high plasma destruction efficiency of 90% while c-C_4F_8 has a comparatively low plasma destruction efficiency of 80 %.

Al deposition - Sputtering

The given inventory is based on a 130 nm technology node which uses a copper interconnect backend, so there is no standard process for aluminum. The standard way to deposit Al is DC sputtering. A recipe for Al deposition is estimated using a Ti deposition process. It has been assumed that Al can be sputtered at a rate of 1 μm/min. But for deposition thickness greater 1 μm, one needs to cool the wafer. Therefore, after every 1 μm deposition there is cooling period of 1 min. Energy consumption is estimated by assuming that the energy required to deposit 50 nm of Ti is similar to that required to deposit 50 nm of Al. In terms of chemical and materials, mostly Argon is used for sputter deposition, and there is a large amount of cooling water and N_2 used in this process.

Chemical release

All handle wafer options except smart cut use a wet chemical release. The release etch is approximated using other wet bench processes such as wet etch, which require relatively little electrical energy per wafer. However, the release steps requires substantial amount of ultra pure water along with acids. The chemical release in manufacturing can be a batch process, which makes the chemical use per wafer relatively small. The chemicals usage estimates here are based on research data. The effluents produced are estimated using the chemical reactions. It is assumed that an Acid Waste Neutralization (AWN) system is attached to the chemical release unit process.

Plasma Activation

Oxygen plasma activation, used for low-temperature oxide bonding can be estimated as a plasma step for 20 seconds. The power for plasma etch can be approximately 30 KW, this low power case. Therefore, the energy consumed during plasma activation is 0.5 KWh. The energy required for other peripherals amounts to

another 0.5 KWh. The total energy consumption is 1 KWh/wafer. In terms of material consumption, this process only uses oxygen gas, and the effluents are primarily composed of oxygen gas. Therefore, there is no need for a point of use abatement system in this process.

H_2 Implantation

The H_2 implantation process was used in the smart cut handle wafer approach. Even though this process is not novel and exists in industry, a little data is available to estimate the environmental footprint of this particular process. The state of the art implant equipment can have throughput somewhere between 20-40 wafers/hr. The energy consumption for implantation is around 2.5 KWh/wafer. If we use this as an estimate and assume that the voltage required is twice and the throughput is half of that needed for well implantation, then the energy requirement will be quadrupled. An upper bound on the electrical energy consumption is 12 KWh/wafer. The water and material consumption are estimated in the same way, in comparison to the inventory data for the well implantation process.

Wet Oxidation

In 2D CMOS, all of the oxidation steps use dry oxidation and the thickness is not more than 40 nm. For different handle wafer options explored, all require 0.5 μm thick thermal oxide growth. The recipe was created using our lab process which has N_2, H_2 and O_2 gases flowing for 90 minutes at 1000°C to grow the 0.5 μm wet oxide film. Energy consumption remains the same as for dry oxidation as the tube is maintained at the same temperature as in case of dry oxidation step available in our database.

In Appendices B through E, inventories for each of the different handle wafer options are detailed, listing the different chemicals for each unit process step. For the sake of clarity in the appendices, the handle wafer options are split into the three distinct modules as shown in Table 7.3, i.e. handle wafer fabrication, device wafer fabrication and stack bonding. The process inventory results are summarized in Section. 7.4.3 through 7.4.6.

7.4.3 Energy Consumption Comparison

According to environmental footprint generated using our process inventory database, a full 2D process flow using 130 nm technology node, with six metal layers, and 300 mm wafers requires 540 KWh/wafer (in processing alone). Each interconnect layer consumes approximately 40 KWh energy. Our 3D IC process flow is approximated as requiring the equivalent of one additional interconnect layer, in addition to the handle wafer process. The energy requirements results for the different handle wafer options are summarized in Table 7.4; these needs are discussed further below.

The handle wafer option proposed by Fan [[58]] as part of MIT's 3D IC approach has the highest energy consumption, i.e., 296 KWh. DC sputtering of 40 μm of Al is a very expensive process in terms of energy, as it requires approximately 6 KWh/wafer to deposit 1 μm of Al. Energy consumption numbers for this approach may be overestimated, depending upon the energy required to deposit aluminum.

The between-die channel approach requires 240 KWh to make a temporary bond and release using HCl acid. Besides deposition of 8 μm of Al, the other two processes that require the largest amount of energy are the etching of six layers of ILD and 50 μms

of silicon on the handle wafer. This approach needs to be further optimized to reduce Al thickness, as well as between-die channel depth, which might consume less energy.

The smart cut handle wafer is the most energy benign process; it only consumes energy approximately 21 KWh. The reason is that it requires the smallest number of steps and does not use extensive etching or deposition as do most of the other options. The energy usage may be under estimated, as there may be far more energy required to implant H_2, which is a small ion, as compared to implantation of larger ions like BF_2^+ as used in well implantation.

The oxide release layer approach consumes energy of around 60 KWh. The primary contribution comes from the 50 μm deep silicon etch with 60% open area, which requires approximately 50 KWh. This option also requires future optimization in terms of etch depth, which can potentially reduce the energy requirement.

7.4.4 Water Consumption Comparison

Ultra pure water required is approximately 500 liters in each of the different handle wafer options. Table 7.4 summarizes the water requirements for each option. The UPW requirement is comparable to the amount consumed by 300 mm wafer processing with six layers of interconnect, which is 1042 liters. The primary cause is that all wet bench processes are batch processes and our CMOS process inventory assumes the batch size of 150 wafers, while for handle wafer options, the batch size is 50 wafers. Another reason is that all of the handle wafer options require at least two wet bench processes, including wafer cleaning before oxidation of the handle wafer, and releasing /activation before bonding. All of these processes are heavily water intensive.

The Al release layer process uses approximately 14,000 liters of PCW, which is enormous. A full 300 mm wafer flow with six levels of, interconnect uses 30,000 liters of PCW. The reason for this large number is the 40 μm thick Al deposition using sputtering. Sputtering is a high energy process which requires cooling of the wafer. In the same way, H_2^+ implantation also requires a lot of cooling, and it is estimated that the smart cut process will require 4000 liters of water. The oxide release layer and between-die channel approaches need PCW for the extensive etch processes.

Handle Wafer Approaches	Energy Consumption (KWh)	Ultra pure water (m^3)	Process Cooling Water (m^3)	Waste water generated (m^3)
Al Release Layer	296, thick Al deposition 40 μm	0.5, acid release	14.7, deposition and oxidation	~1,Acid release, generate acid water containing $AlCl_3$
Between-Die Channel	240, thick Al deposition, All 6 layers of IMD and 50 μm silicon etching	0.62, acid release and clean	10.7, oxidation, deposition and etching	~1,Acid release, generate acid water containing $AlCl_3$
Oxide Release Layer	60, 50 μm of silicon etching	0.73, acid release, activation	2.9, oxidation and etching	~1, waste water from acid and activation
Smart Cut	20, assumed H_2 implantation is similar to other implantation process	0.43, activation	4.71, oxidation and implantation	~0.5, waste water from activation

Table 7-4: Comparing energy and water consumption for four handle wafer options.

Industrial city water (ICW) is used in small amounts by point of use abatement systems. All three options, which employ a wet release process, generate water mixed with either $AlCl_3$ or SiF_4. There is also water mixed with acids produced by the abatement system, which is sent to an acid waste neutralization (AWN) system followed by a house scrubber to neutralize.

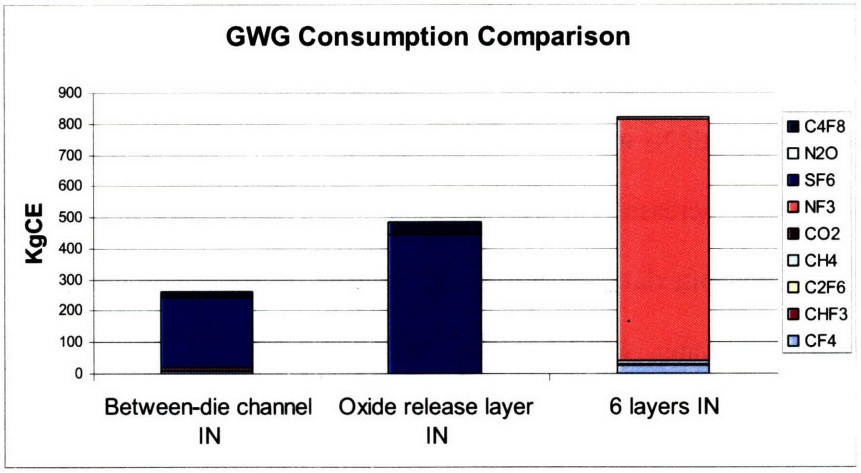
7.4.5 Trends in Chemical Use and Effluents Output

All of the results corresponding to chemical use and effluents produced are listed in detail in Appendix B through E. Here we summarize some key points about these different processes. Unlike electricity and water consumption, it is very hard to compare the chemicals used and effluents for each handle wafer option. Therefore, here the comparison is conducted in comparison to 2D CMOS based on our process inventory. The idea behind this is to assess the relative change in the composition of incoming materials and chemicals, and of the outgoing effluents.

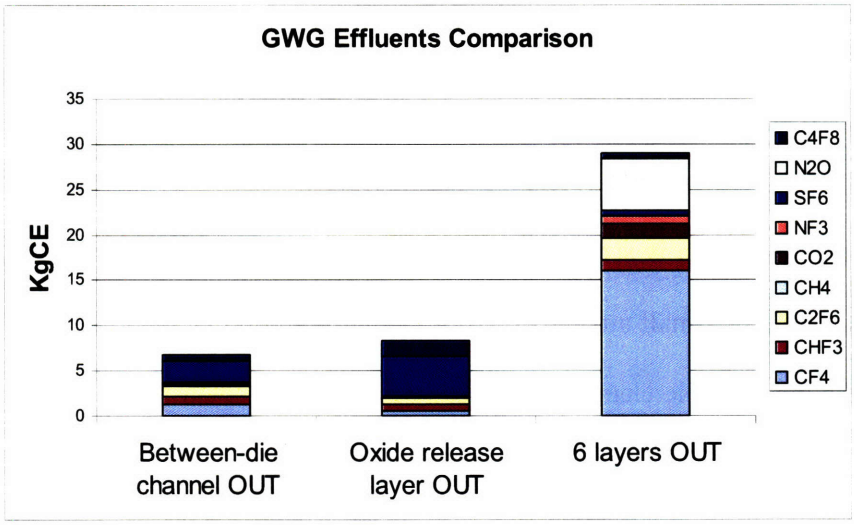
Global Warming Gases

The oxide release layer and between-die channel approach both employ the Bosch process for creating channels in handle wafer to enable the release process. The Bosch process uses SF_6 and c-C_4F_8, and both these gases have large GWP, 23900 and 8700 respectively, and both are very long-lived and can stay in the atmosphere for 3200 years [[138]]. A 50 μm etch depth was required, which need plasma on times of 20 minutes to 40 minutes depending on the loading area. Thus, large amounts of SF_6 and c-C_4F_8 are required as seen in the table in Appendix D and E.

The between-die channel approach also etches deep channels in the device wafer which requires etching six levels of inter-level dielectric. This process will also contribute to GWG. Figure 7.1 compares the GWP of different handle wafer options both in intake and effluents. The resulting handle wafer GWP is comparable to the six metal layer 2D CMOS logic device.



a



b

Figure 7.1 Global warming potential compared for two handle wafer options, and compared with a six metal layer 2D CMOS process using a 130 nm technology node and 300 mm wafers. a) Intake of GWG. b) Effluents generated and emitted out in the air.

Volatile Organic Compounds

The oxide release layer and between-die channel requires patterning or lithography while other two options do not. However, they are relatively modest additions compared to the thirty litho step conducted in six levels of metal processing in a conventional full CMOS process flow.

Flammable

H_2 has been used in wet oxidation in conjunction with N_2 and O_2 gas. But H_2O can be used along with N_2 instead. As compared to a full-scale CMOS process, there is approximately 10% increase in H_2 consumption. In a CMOS process, the two main steps which use H_2 are epitaxial deposition and tungsten CVD. Hydrogen can be burned completely to give water, which makes it benign in effluents. At the same time, the consumption of *c*-C_4F_8 has increased the flammable gases used in the oxide release layer and between-die approach. This flammable gas can be burn in the combustion chamber to yield either CO_2 or COF_2.

Hazardous Air Pollutants

In case of the oxide release layer, silicon is etched using a Bosch process, resulting in SiF_4 which is scrubbed using water, then sent to the house scrubber to be removed efficiently. Small amounts of F_2 are emitted during etching of both silicon and oxide in the between-die channel approach, which is very small when compared against release in a deposition process. In the case of the between-die channel approach, silicon is etched using an HBr/ Cl_2 recipe which is standard for STI etching, thus Br_2 is produced as an effluent which needs to be scrubbed.

Criteria Air Pollutants

Interestingly, there are no criteria gases used as inputs, but they are formed as by-products during some processes. In our case, in silicon etching using the Bosch process, large amounts of SF_6 gas are used, resulting in a different kind of SO_xF_y by products when cleaned with oxygen plasma periodically. The stable forms of the clean by-products are primarily SO_2 and F_2. SO_2 is generally scrubbed using water to form acid and remove from the system.

7.4.6 Uncertainty

There can be various sources of error in the analyses presented here. Some of these errors source are identified and listed below.

Measurement error – The inventory database, which is used as the basis for our estimation, can have some measurement issues on the exhaust side. The inventory data was collected using residual gas analyzer (RGA) to the exhaust pipe, and there can be errors related to the RGA measurement such as ionization efficiency, heavy mass species being less present, or human errors.

Estimation error – Poor assumptions may be present in our estimates. For example, we extrapolate data from 150 mm to 300 mm wafers. Effluents can be very dependent on processing conditions, for example loading area, leading to estimation errors.

Obsolete – The chemicals and recipe used in our inventory may not be equivalent to an optimized recipe used in manufacturing, but may be generic or obsolete version.

Batch process – It is assumed that all batch processes have 50 wafers as the standard size. It is quite possible that in manufacturing, the batch size may be much larger than this. In that situation, our estimates especially for water consumption can be reduced by that factor.

7.5 Overall Assessment of Handle Wafer options

The four different handle wafer options have been analyzed and compared with respect to performance, cost and environmental footprint. No single process option is optimal on all three axes. Figure 7.2 aggregates and compares, in a qualitative summary,

all four handle wafer options on our three axes. These qualitative comparisons can be summarized as follows.

	Al Release Layer	Between-Die Channel	Smart Cut	Oxide Release Layer
Performance	✗	✓	✓	○
Cost	○	○	✗	✓
Environmental Concerns	✗	✗	✓	○

Figure 7.2: Overall comparative assessment of handle wafer options. A ✓ indicates acceptable, a ○ indicates further work is needed, an ✗ indicates an area of high concern.

Smart cut, which seems the best in terms of environmental impact and performance in spite of having voids, can be improved further with process development. It is the most expensive option

The oxide release layer approach seems to be fair on the environmental and cost axes (because of its reuse nature). In performance, it has low selectivity, and presents challenging issues in terms of thinning and releasing.

The between-die channel approach has good performance; it offers good selectivity and a wide process window with good yield. However, it has a large environmental footprint along with low throughput, which can also be cause for concern in terms of cost. The Al release layer approach does not have acceptable yield, and has the largest environmental footprint.

Chapter 8: Contributions and Conclusions

This chapter summarizes the key contributions of this work and identifies issues which require further research. The prime purpose of this research is to enable environmentally benign or environmentally conscious semiconductor manufacturing, which can be achieved by integrating environmental impact evaluation in the research phase of emerging technology development. An environmental assessment methodology is developed, and applied to the MIT 3D IC technology, resulting in identification of the handle wafer process as being alarming from both environmental and performance perspectives. Three different approaches were explored for improving the handle wafer process. Different handle wafer process options were then compared on three axes including cost, performance and environmental impact.

In Section 8.1, we summarize our findings about the environmental assessment methodology. In Section 8.2, we recapitulate the technology development and assessment of 3D ICs contributed in this thesis. We also discuss another key enabling technology low-temperature bonding using copper-indium is explored in this thesis as a potential approach which could changes the constraints on 3D handle wafer technology. Finally, Section 8.3, we suggest future directions for both the environmental assessment methodology, and for technology development of 3D IC.

8.1 Environmental Assessment Methodology

This research contributes methodology to enable comparative environmental assessment of emerging silicon technologies. The primary motivation of the assessment methodology is to provide a quick comparison of the environmental footprints of

alternative technologies under consideration, along with cost and performance. The evaluation will enable environmental factors to be part of the decision making process early in the technology development cycle and will provide guidelines to researchers about how to make future technologies more environmentally conscious.

The methodology identifies a novel technology and a state-of-the-art technology, which is going to be augmented or replaced. Then, a functional unit for comparison is defined between two or more technologies. Using a prototype flow for the novel technology, the proposed approach is compared with existing technology to identify new and additional unit processes. With the help of a process-based input-output inventory database and estimation, key environmental parameters are evaluated against each other. Because of its transparent and bottom up approach, it is possible to identify unit processes that have environmental issues, and research can be focused on making those unit processes more environmentally benign. The possible drawback of this methodology is that it is very dependent on updated input-output process based inventory or models. A gate-to-gate inventory is contributed for a CMOS based logic device in a 130-nm technology node on 300 mm wafers, in collaboration with other researchers from Applied Materials. This inventory database is quite comprehensive, and listing of eighty different chemicals (both from consumption and effluents viewpoints). This is a significant contribution, as before this study data was only available for approximately twenty chemicals identified by SIA and Sematech, based primarily on consumption and cost. The inventory also details process energy, water consumption and waste generated for a substantial number of unit processes.

8.1.1 Case Study 3D vs. 2D

The environmental assessment methodology was applied to upcoming three dimensional integrated circuit (3D IC) technology. The standard state-of-the-art integrated circuit (2D IC) technology will be augmented by 3D ICs; thus the two technologies are compared to each other on all three axes of performance, cost, and environmental impact, providing an overall assessment. 3D ICs can be implemented in various ways, as reviewed in Chapter 1. To apply this methodology, we need to be specific about the process flow. Therefore, the methodology was applied to a previously developed 3D IC developed at MIT that employs back-to-face wafer bonding using copper bonding layers.

3D IC technology provides advantages in terms of reducing wire length, which can not only enhance the speed, but also reduce power consumption. There are significant challenges, in terms of heat removal and technology integration, which need to be solved before 3D ICs can become viable.

On the cost axis, 3D ICs appears to be more expensive than 2D ICs, due to the number of processes involved. 3D ICs also require the development of new technologies, tool acquisition, and tool maintenance, and therefore it is likely to be more expensive than existing 2D technology. Using a very simple approach, it is determined that the variable cost for adding one device layer in a 3D stack can be approximated as equal to that of adding one layer of interconnect, plus the cost of handle wafer process. On the other hand, we believe that significant cost savings will result from a reduction in package size; further analysis of 3D vs. 2D packaging benefits and cost is needed.

With an initial environmental assessment using our comparative methodology, we ascertained that there are 22 additional unit processes, including novel and standard, for adding one more device layer using the MIT 3D IC approach. As with cost, the environmental impact of the addition of one more device layer can be approximated as equivalent to that generated by adding one more interconnect layer, together with the environmental cost of the handle wafer, grinding and bonding processes. Grinding and thermo-compression bonding processes were estimated using existing literature and estimation from the CMOS inventory. The handle wafer process was identified as an environmentally expensive process, especially from an energy viewpoint. It was also shown that the handle wafer process has a low functional yield in its current form, and thus new processes for 3D handle wafer technology were investigated in the second half of the thesis.

8.2 Handle Wafer Options

The handle or support wafer is an essential technology for enabling back-to-face integration (MIT's approach) in 3D ICs. Various handle wafer options in the literature were examined, but none of these are yet satisfactory in terms of performance or cost. Thus, we explored new approaches for an environmentally conscious handle wafer process. Broadly, three technological approaches are proposed for the handle wafer process: between-die channels in the device wafer to improve handle wafer release, micro-channels in an oxide bonded handle wafer to accelerate chemical release, and enabling low-temperature permanent metallic bonding for options such as smart cut.

8.2.1 Chemical Release with Micro-Channels in the Device Wafer

The between-die channel approach is improved version of the Al release layer stacked structure previously developed by Fan. The between-die channel approach is inspired by existing dicing before grinding (DBG) technologies. The channels are introduced to solve the diffusion limitation and to enable undercutting the aluminum release layer. This method is very selective with a wide process window and high yield. However, it has an important limitation in terms of process throughput, as it requires 8 hours to release the handle wafer. The between-die channel approach also consumes a large amount of energy, because it requires deposition of 8 μm thick layers of Al, as well as etching of 50 μm of silicon, which requires long plasma etch time. This approach presents a unique way for releasing the handle wafer using chemical methods, by providing a deep channel in the kerf area between chips, where the die-saw line is later formed; the channels enables more effective and better transfer of reactants and products across the wafer.

8.2.2 Chemical Release Using Channels in an Oxide Release Layer

An oxide release layer is a second proposed handle wafer option, employing chemical release of a stack in which the temporary bonding and releasing material are the same. In this approach, silicon handle wafers are etched with channels, which are bonded to a device wafer using low-temperature plasma assisted oxide bonding. Encapsulated channels are used for effective and improved chemical release. Oxide bond strength is measured for different patterns using chevron structure. We find that bond strength has an inverse relation with channel spacing or pad size. Thermal oxidation of the pads structure can lead to bumps at the pad edges, which pose a challenge for low-temperature oxide bonding, and result in a constraint on oxide thickness. Handle wafers can be released

using concentrated hydrofluoric acid; the release time is inversely proportional to etch depth, smaller pads can be released more efficiently. A dummy device wafer was successfully transferred to another substrate wafer, demonstrating the feasibility of the proposed approach. Silicon nitride can be used as a sacrificial layer to protect underlying oxide from the hydrofluoric acid, overcoming some of the concerns with the use of HF.

8.2.3 Low-Temperature Bonding – Copper-Indium

A third approach for the handle wafer is to enable low-temperature permanent bonding using copper-indium SLID bonding. Temporary adhesive bonding and smart cut handle wafer options require processing temperature below 250°C, in order to be manufacturable. In this thesis, low-temperature copper indium bonding was explored as a means to reduce the permanent bonding temperature from 350°C (as used in copper bonding) to 200°C using solid liquid interdiffusion (SLID) bonding. In our preliminary explorations, we demonstrate that sub-micron copper-indium stacks can be bonded to copper stacks at 200°C, and the stacks can be thinned reliably. When examining the stack using cross-sectional SEM, however we find that there are large voids present in the bonding interface, which is not satisfactory for 3D circuit use.

Thin films in various copper-indium stacks were studied to understand the void formation. Indium, when deposited on copper using e-beam or any PVD technique, is found to result in a very rough film, which may result in voids in bonded stack. Additionally, indium diffuses quickly into copper and, because of the sub-micron copper stack dimensions, as-deposited films form a CuIn solid solution, as confirmed when analyzed using XRD. STEM was conducted on the bonding interface to understand if there is indium or copper segregation along the bonding interface and grain boundary;

results show that the films are homogeneous in composition, with very low oxygen content and no apparent bonding interface.

The two most important requirements to achieve good, reliable bonding in this approach is to deposit smooth films having copper and indium rich composition. Future work should consider sputtering, which can deposit smooth films and which has a faster deposition rate to limit the diffusion time for indium atom.

8.2.4 Overall Assessment of Handle Wafer Options

A final contribution of this thesis is the assessment of handle wafer process options, including the newly developed and extended approaches proposed in this thesis on all three axes of performance, cost and environmental impact. The functional yield is a key parameter used to evaluate the performance of different options. We find that the between-die channel and smart cut approaches have higher yield compared to the oxide release layer, and the Al release layer approach has very low yield. In terms of cost, the between-die channel has low throughput because of long handle wafer release time. Smart-cut is also an expensive process, because of the high cost involved in H_2 implantation. Even though the oxide release layer approach has lower yield than between-die channel and smart cut process, it has a lower cost and environmental footprint, primarily because the handle wafer and etch chemistry can be reused with very little additional cost and processing.

Various parameters, such as energy and water consumption along with chemicals consumption and effluents creation, are evaluated on the handle wafer option. All of these options were compared to each other in terms of energy and water consumption. For chemicals and effluents, options are evaluated in terms of use or emissions of global

warming gases, volatile organic compounds, hazardous, flammable and criteria pollutants. Using the unit process inventory database, each process option is quantified and compared against a 130 nm technology node using 300 mm wafers, and 6 metal layers.

8.3 Future Work

As mentioned previously, our environmental assessment methodology is heavily reliant on the inventory database. It is an ongoing process to make this database complete not only in terms of including different processes but also to have multiple data points for each kind of process step in order to make estimates less prone to error. A data set for MEMS and III-V semiconductor processing is needed, in order to evaluate hybrid technologies which will become more prevalent in the future

Packaging needs to be considered, and should be added to the comparison between 3D ICs and 2D ICs. 3D ICs have several performance advantages and is likely to be deployed in the future; thus, it is important to compare and improve the integration options to achieve a 3D IC, from an environmental perspective as well as from performance and cost points of view.

Based on our results and experience, the following future work is recommended focused on the 3D IC handle wafer process. In terms of technology development, the between-die channel approach shows promise. Chemical release methods can be optimized further using as the aluminum release layer by increasing temperature and changing chemistry, such as adding surfactants and peroxide. The oxide release layer approach suggests a number of potential avenues for further research. The etchant chemistries which are selective than concentrated HF should be explored, such as HF

vapor [139], or buffered oxide with some additives. Another avenue for further research is to change the oxide bonding layer to BPSG which can be etched much faster than thermal oxide in an HF based chemistry [90]. It is also important to study thinning limitations; by finite element simulations and experiments can help to understand stress in thin device wafers bonded to pads having encapsulated free-floating channels. Another very interesting approach for future study might be a hybrid handle wafer approaches combining micro-channel structures with aluminum release layers.

Copper-indium bonding should be further characterized with sputtered indium, and potentially with thicker films, to see if Cu-In stack can be bonded reliably, without voids. This remains a promising approach which could substantially change the temperature constraints in 3D IC handle wafer technology by making it possible to reduce the bonding temperature to 200°C as compared to the 300°C needed for Cu-Sn bonding.

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Appendix

In this section we present four appendix detailing process inventories which has been developed as part of this thesis with the help of Nikhil Krishnan and Sarah Boyd at Applied Materials.

Because the data is huge the excel sheets are broken into several pieces. The data is organized by the emissions and consumption data as the row and unit process steps as the column. Each process step has three columns saying: process in, process out, Post point of use abatement.

Appendix A summarizes the result of environmental footprint of 2D CMOS with six layer device, for 130 nm technology node, 300 mm wafer.

Appendix B is the unit process steps which are unique for Al release layers are tabulated.

Appendix C is the unit process steps for the smart cut approach.

Appendix D for the Oxide release layer approach.

Appendix E is for the between-die-channel approach.

Appendix A
CMOS 6 layer metal 130 nm, 300 mm wafer

UNITS in g/wafer wherever possible			
	130 nm node 300 mm wafer 6 layer wafer		
Film Thickness (A)		Total Time	
Time (s)	22508.70787	45936.13851	
	IN	OUT	postPQU
GWG			
CF4	15.98128683	17.38392932	9.389958571
CHF3	1.041828794	0.607741395	0.338129903
C2F6	0	0.863	0.72
CH4	1643.479613	0.338	0.228
CO2	0	763.7275313	4892.913741
NF3	353.2381958	8.254029167	0.543286339
C4F6	0.650892857	0.05	0.0001
SUM	2014.391817	0.791224231	4.904133216
HAZARDOUS			
F2	0	152.5651262	2.863993695
HF (gas)	0	10.75409715	1.112148455
SiF4	0.045	78.25875778	3.280799596
C4F8	0.33	0.03	0.0003
C2F4	0	0.54354	0.54354
COF2	0	3.646823061	0.43222975
HCl (gas)	28.84285714	22.21101786	18.65621786
Cl2	0.474	0.648	0.037569091
SiCl4	0	2.22	0.037045455
PH3	1.205811956	0.226003812	0.226000152
Bis Tertiary-Butylamino Silane	1.0675	0.84182	0.84182
AsH3	0.018928202	0.000566397	0.150022656
BCl3	0	0	0
Pb	0.056110416	0.055549311	0
WF6	13.57528571	5.982428571	5.982428571
HBr	23.606	2.409	1.42
Br2	0	39.2	39.2
SUM	69.22149343	319.5927302	74.78411528
CRITERIA			
CO	0	4.878867108	6.258728767
NO	0	3.829367108	7.05
NO2	0	4.8	4.58
SO2	0	0	0
N2O	91.77209821	68.43651429	68.19591429
SUM	91.77209821	81.9447485	86.08464305
VOC			
DMA	0	0.007453125	0.007453125
MMA	0	0.17146875	0.17146875
TDMAT	3.528158333	0	0
TMS	43.9985	24.876	0.0174
TEOS	0	0	0
Formaldehyde (CH2O)	54.81945	53.723061	49.24613925
m-Cresol	34.7625	34.06725	31.2383125
p-Cresol	34.425	33.7365	30.925125
polypropylene glycol monomethyl ether a	132.2690625	130.95	120.0375
SUM	303.8026708	277.5317329	231.6433986
FLAMMABLE			
SiH4	9.4845	1.330755238	0.770814571
H2	65.84443452	16.35172143	2.385029464
DCS	5.65	4.06	0.000736364
B2H6	0.00498	0.00183	0
C4F8	0	0.24	0.22
SUM	80.98391452	21.98430667	3.376580399

Appendix A
CMOS 6 layer metal 130 nm, 300 mm wafer

UNITS in g/wafer wherever possible			
	130 nm node 300 mm wafer 6 layer wafer		
Film Thickness (A)		Total Time	
Time (s)	22508.70787	45936.13851	
	IN	OUT	post-POU
OTHER CHEMICALS			
O2	11464.82704	111.6377117	22.73765616
Ar	194.2855858	95.28915723	84.78915723
N2	2264.139267	2122.76097	2122.76097
EP-C5003, Cabot	14436.69855	13846.05939	13846.05939
H2O2 100%	5885.324886	2439.325	2439.325
CUS silica slurry A	437.5	437.5	437.5
CUS silica slurry B	437.5	437.5	437.5
BTA, Aldrich	18.00095299	18.00095299	18.00095299
Sumiwash	463	463	463
ElectraClean,Ashland	294.6666667	294.6666667	294.6666667
Semi-Sperse W2000	2307.676565	2307.676565	2307.676565
Al	0	7.353E-07	7.353E-07
As	0	9.9693E-09	9.9693E-09
Cu	0.698093304	0.349046667	0.349046667
Pt	2.6125	2.612500001	2.612500001
Ti	0.188493792	0.164217864	6.48866E-09
He	432.33	0.005	0.00005
NH3	14.83047994	13.74263214	3.066372143
CuSO4	12.46012665	12.46012665	12.46012665
ArH	0	0	0
100% HF liquid	21.13142947	13.8537726	13.8439726
H2SO4	64397.33107	64297.8	64297.8
HCl	1096.2	0	0
NH4OH	1470.785308	1465.459096	1465.459096
IPA	0	0	0
Oxide CMP Slurry& chemicals	4428	4428	4428
BF3	0.024820471	0.020600991	0.00082404
ethyl lactate	139.05	136.269	136.269
Cr	0	0	0
Au	0	0	0
Sn	0.015501404	0.01534639	0.01534639
Co	0.026212664	0.010485065	0.010485065
polyimide laminate	5.625	5.5125	5.5125
laminate solvent	213.9377113	213.8218363	213.8218363
utility N2	71687.26534	71538.46024	71687.26534
Silicon	0	0	0
H3PO4	558.6	446.88	446.88
CuCl2	0	0.00713943	0.00713943
W	0	0	0
METAL OXIDE POWDER (Fe2O3)	1.396259045	1.396259045	1.396259045
SUM	182686.1279	165150.2562	165188.7863
OTHERS per wafer			
Process Electricity (KWh)	540.0295791	0	0
UPW	961640.9362	0	0
Industrial City Water	609522.6342	0	0
PCW	26683587.93	0	5263650.323
Fluoride Wastewater (H2O)	0	0	368266.2316
Industrial Wastewater (H2O)	0	83806.36319	935731.7044
Cu CMP wastewater	0	0	134238.7904
dissolved solid Cu to CMP waste	0	0	0.0039525
Ammonia Waste (NH3) to AWN	0	0	19.38
HF liquid waste to Fluoride treatment	0	4.291535321	4.291535321
SiF4 liquid waste to Fluoride treatment	0	0.356047904	0.356047904
NH4OH waste	0	4.68	4.68
H2O2 liquid waste	0	5.53	5.53
H2O2 to CMP waste	267778	441.6698857	441.6698857
liter/wafer			OTHERS (liter/wafer)
UPW	961.6409362	0	0
Industrial City Water	609.5226342	0	0
PCW	26683.58793	0	5263.650323
Fluoride Wastewater (H2O)	0	0	368.2662316
Industrial Wastewater (H2O)	0	83.80636319	935.7317044
Cu CMP wastewater	0	0	134.2387904
dissolved solid Cu to CMP waste	0	0	3.9525E-06
Ammonia Waste (NH3) to AWN			0.01938

Appendix B
Al Release Layer

Al releas layer - Handle wafer option	Device Wafer Preparation					
UNITS in g/wafer wherever possible		Al deposition			Bonding layer	
		Sputtering			TiN/ Cu PVD	
Film Thickness (nm)		20000			50/300	
Time (s)	2400					
	in	process out	post-POU	in	process out	post-POU
GWG						
CF4	0.000	0.000	0.000	0.000	0.000	0.000
CHF3	0.000	0.000	0.000	0.000	0.000	0.000
C2F6	0.000	0.000	0.000	0.000	0.000	0.000
CH4	0.000	0.000	0.000	0.000	0.000	0.000
CO2	0.000	0.000	0.000	0.000	0.000	0.000
NF3	0.000	0.000	0.000	0.175	0.003	0.003
C4F6	0.000	0.000	0.000	0.000	0.000	0.000
SF6	0.000	0.000	0.000	0.000	0.000	0.000
HAZARDOUS						
F2	0.000	0.000	0.000	0.000	0.102	0.102
HF (gas)	0.000	0.000	0.000	0.000	0.000	0.000
SiF4 (gas)	0.000	0.000	0.000	0.000	0.035	0.035
C4F8	0.000	0.000	0.000	0.000	0.000	0.000
C2F4	0.000	0.000	0.000	0.000	0.000	0.000
COF2	0.000	0.000	0.000	0.000	0.000	0.000
HCl (gas)	0.000	0.000	0.000	0.000	0.000	0.000
Cl2	0.000	0.000	0.000	0.000	0.000	0.000
SiCl4	0.000	0.000	0.000	0.000	0.000	0.000
PH3	0.000	0.000	0.000	0.000	0.000	0.000
Bis Tertiary-Butylamino Silane	0.000	0.000	0.000	0.000	0.000	0.000
AsH3	0.000	0.000	0.000	0.000	0.000	0.000
BCl3	0.000	0.000	0.000	0.000	0.000	0.000
Pb	0.000	0.000	0.000	0.000	0.000	0.000
WF6	0.000	0.000	0.000	0.000	0.000	0.000
HBr	0.000	0.000	0.000	0.000	0.000	0.000
Br2	0.000	0.000	0.000	0.000	0.000	0.000
CRITERIA						
CO	0.000	0.000	0.000	0.000	0.000	0.000
NO	0.000	0.000	0.000	0.000	0.000	0.000
NO2	0.000	0.000	0.000	0.000	0.000	0.000
SO2	0.000	0.000	0.000	0.000	0.000	0.000
N2O	0.000	0.000	0.000	0.000	0.000	0.000
VOC						
DMA	0.000	0.000	0.000	0.000	0.001	0.001
MMA	0.000	0.000	0.000	0.000	0.024	0.024
TDMAT	0.000	0.000	0.000	0.504	0.000	0.000
TMS	0.000	0.000	0.000	0.000	0.000	0.000
TEOS	0.000	0.000	0.000	0.000	0.000	0.000
Formaldehyde (CH2O)	0.000	0.000	0.000	0.000	0.000	0.000
m-Cresol	0.000	0.000	0.000	0.000	0.000	0.000
p-Cresol	0.000	0.000	0.000	0.000	0.000	0.000
polypropylene glycol monomethyl ether acetate	0.000	0.000	0.000	0.188	0.000	0.000
FLAMMABLE						
SiH4	0.000	0.000	0.000	0.000	0.000	0.000
H2	0.000	0.000	0.000	0.000	0.000	0.000
DCS	0.000	0.000	0.000	0.000	0.000	0.000
B2H6	0.000	0.000	0.000	0.000	0.000	0.000
C4F8	0.000	0.000	0.000	0.000	0.000	0.000

Appendix B
Al Release Layer

Al releas layer - Handle wafer option	Handle Wafer Preparation					
UNITS in g/wafer wherever possible		Wafer Clean			Oxidation	
		RCA Batch process		Furnace Batch process wet oxidation		
Film Thickness (nm)					500	
Time (s)				8100		
	in	process out	post-POU	in	process out	post-POU
GWG						
CF4	0.000	0.000	0.000	0.00	0.00	0.00
CHF3	0.000	0.000	0.000	0.00	0.00	0.00
C2F6	0.000	0.000	0.000	0.00	0.00	0.00
CH4	0.000	0.000	0.000	0.00	0.00	0.00
CO2	0.000	0.000	0.000	0.00	0.00	0.00
NF3	0.000	0.000	0.000	0.00	0.00	0.00
C4F6	0.000	0.000	0.000	0.00	0.00	0.00
SF6	0.000	0.000	0.000	0.00	0.00	0.00
HAZARDOUS						
F2	0.000	0.000	0.000	0.00	0.00	0.00
HF (gas)	0.000	0.000	0.000	0.00	0.00	0.00
SiF4 (gas)	0.000	0.000	0.000	0.00	0.00	0.00
C4F8	0.000	0.000	0.000	0.00	0.00	0.00
C2F4	0.000	0.000	0.000	0.00	0.00	0.00
COF2	0.000	0.000	0.000	0.00	0.00	0.00
HCl (gas)	0.000	0.000	0.000	3.52	0.35	0.35
Cl2	0.000	0.000	0.000	0.00	0.00	0.00
SiCl4	0.000	0.000	0.000	0.00	0.00	0.00
PH3	0.000	0.000	0.000	0.00	0.00	0.00
Bis Tertiary-Butylamino Silane	0.000	0.000	0.000	0.00	0.00	0.00
AsH3	0.000	0.000	0.000	0.00	0.00	0.00
BCl3	0.000	0.000	0.000	0.00	0.00	0.00
Pb	0.000	0.000	0.000	0.00	0.00	0.00
WF6	0.000	0.000	0.000	0.00	0.00	0.00
HBr	0.000	0.000	0.000	0.00	0.00	0.00
Br2	0.000	0.000	0.000	0.00	0.00	0.00
CRITERIA						
CO	0.000	0.000	0.000	0.00	0.00	0.00
NO	0.000	0.000	0.000	0.00	0.00	0.00
NO2	0.000	0.000	0.000	0.00	0.00	90.00
SO2	0.000	0.000	0.000	0.00	0.00	0.00
N2O	0.000	0.000	0.000	0.00	0.00	0.00
				0.00	0.00	0.00
VOC						
DMA	0.000	0.000	0.000	0.00	0.00	0.00
MMA	0.000	0.000	0.000	0.00	0.00	0.00
TDMAT	0.000	0.000	0.000	0.00	0.00	0.00
TMS	0.000	0.000	0.000	0.00	0.00	0.00
TEOS	0.000	0.000	0.000	0.00	0.00	0.00
Formaldehyde (CH2O)	0.000	0.000	0.000	0.00	0.00	0.00
m-Cresol	0.000	0.000	0.000	0.00	0.00	0.00
p-Cresol	0.000	0.000	0.000	0.00	0.00	0.00
polypropylene glycol monomethyl ether acetate	0.000	0.000	0.000	0.00	0.00	0.00
FLAMMABLE						
SiH4	0.000	0.000	0.000	0.00	0.00	0.00
H2	0.000	0.000	0.000	8.35	3.06	0.00
DCS	0.000	0.000	0.000	0.00	0.00	0.00
B2H6	0.000	0.000	0.000	0.00	0.00	0.00
C4F8	0.000	0.000	0.000	0.00	0.00	0.00

Appendix B
Al Release Layer

Al releas layer - Handle wafer option						
UNITS in g/wafer wherever possible		**Al deposition**			**Bonding Layer**	
		Sputtering			TiN/Cu PVD	
Film Thickness (nm)		20000			50/300	
Time (s)	2400.00					
	in	process out	post-POU	in	process out	post-POU
GWG						
CF4	0.000	0.000	0.000	0.000	0.000	0.000
CHF3	0.000	0.000	0.000	0.000	0.000	0.000
C2F6	0.000	0.000	0.000	0.000	0.000	0.000
CH4	0.000	0.000	0.000	0.000	0.000	0.000
CO2	0.000	0.000	0.000	0.000	0.000	0.000
NF3	0.000	0.000	0.000	0.175	0.003	0.003
C4F6	0.000	0.000	0.000	0.000	0.000	0.000
SF6	0.000	0.000	0.000	0.000	0.000	0.000
HAZARDOUS						
F2	0.000	0.000	0.000	0.000	0.102	0.102
HF (gas)	0.000	0.000	0.000	0.000	0.000	0.000
SiF4 (gas)	0.000	0.000	0.000	0.000	0.035	0.035
C4F8	0.000	0.000	0.000	0.000	0.000	0.000
C2F4	0.000	0.000	0.000	0.000	0.000	0.000
COF2	0.000	0.000	0.000	0.000	0.000	0.000
HCl (gas)	0.000	0.000	0.000	0.000	0.000	0.000
Cl2	0.000	0.000	0.000	0.000	0.000	0.000
SiCl4	0.000	0.000	0.000	0.000	0.000	0.000
PH3	0.000	0.000	0.000	0.000	0.000	0.000
Bis Tertiary-Butylamino Silane	0.000	0.000	0.000	0.000	0.000	0.000
AsH3	0.000	0.000	0.000	0.000	0.000	0.000
BCl3	0.000	0.000	0.000	0.000	0.000	0.000
Pb	0.000	0.000	0.000	0.000	0.000	0.000
WF6	0.000	0.000	0.000	0.000	0.000	0.000
HBr	0.000	0.000	0.000	0.000	0.000	0.000
Br2	0.000	0.000	0.000	0.000	0.000	0.000
CRITERIA						
CO	0.000	0.000	0.000	0.000	0.000	0.000
NO	0.000	0.000	0.000	0.000	0.000	0.000
NO2	0.000	0.000	0.000	0.000	0.000	0.000
SO2	0.000	0.000	0.000	0.000	0.000	0.000
N2O	0.000	0.000	0.000	0.000	0.000	0.000
VOC						
DMA	0.000	0.000	0.000	0.000	0.001	0.001
MMA	0.000	0.000	0.000	0.000	0.024	0.024
TDMAT	0.000	0.000	0.000	0.504	0.000	0.000
TMS	0.000	0.000	0.000	0.000	0.000	0.000
TEOS	0.000	0.000	0.000	0.000	0.000	0.000
Formaldehyde (CH2O)	0.000	0.000	0.000	0.000	0.000	0.000
m-Cresol	0.000	0.000	0.000	0.000	0.000	0.000
p-Cresol	0.000	0.000	0.000	0.000	0.000	0.000
polypropylene glycol monomethyl ether acetate	0.000	0.000	0.000	0.188	0.000	0.000
FLAMMABLE						
SiH4	0.000	0.000	0.000	0.000	0.000	0.000
H2	0.000	0.000	0.000	0.000	0.000	0.000
DCS	0.000	0.000	0.000	0.000	0.000	0.000
B2H6	0.000	0.000	0.000	0.000	0.000	0.000
C4F8	0.000	0.000	0.000	0.000	0.000	0.000

Appendix B
Al Release Layer

Al releas layer - Handle wafer option	Bonded Stack					
UNITS in g/wafer wherever possible	Copper Bonding and annealing				HCL release	
		(modeled on coper annealing)			Acid bath -wet bench	
Film Thickness (nm)				(36% by wt in 1:1 solution with H2O)		
Time (s)	10800			Not determined		
				in	process out	post-POU
GWG						
CF4	0.000	0.000	0.000	0.000	0.000	0.000
CHF3	0.000	0.000	0.000	0.000	0.000	0.000
C2F6	0.000	0.000	0.000	0.000	0.000	0.000
CH4	0.000	0.000	0.000	0.000	0.000	0.000
CO2	0.000	0.000	0.000	0.000	0.000	0.000
NF3	0.000	0.000	0.000	0.000	0.000	0.000
C4F6	0.000	0.000	0.000	0.000	0.000	0.000
SF6	0.000	0.000	0.000	0.000	0.000	0.000
HAZARDOUS						
F2	0.000	0.000	0.000	0.000	0.000	0.000
HF (gas)	0.000	0.000	0.000	0.000	0.000	0.000
SiF4 (gas)	0.000	0.000	0.000	0.000	0.000	0.000
C4F8	0.000	0.000	0.000	0.000	0.000	0.000
C2F4	0.000	0.000	0.000	0.000	0.000	0.000
COF2	0.000	0.000	0.000	0.000	0.000	0.000
HCl (gas)	0.000	0.000	0.000	0.000	0.000	0.000
Cl2	0.000	0.000	0.000	0.000	0.000	0.000
SiCl4	0.000	0.000	0.000	0.000	0.000	0.000
PH3	0.000	0.000	0.000	0.000	0.000	0.000
Bis Tertiary-Butylamino Silane	0.000	0.000	0.000	0.000	0.000	0.000
AsH3	0.000	0.000	0.000	0.000	0.000	0.000
BCl3	0.000	0.000	0.000	0.000	0.000	0.000
Pb	0.000	0.000	0.000	0.000	0.000	0.000
WF6	0.000	0.000	0.000	0.000	0.000	0.000
HBr	0.000	0.000	0.000	0.000	0.000	0.000
Br2	0.000	0.000	0.000	0.000	0.000	0.000
CRITERIA						
CO	0.000	0.000	0.000	0.000	0.000	0.000
NO	0.000	0.000	0.000	0.000	0.000	0.000
NO2	0.000	0.000	0.000	0.000	0.000	0.000
SO2	0.000	0.000	0.000	0.000	0.000	0.000
N2O	0.000	0.000	0.000	0.000	0.000	0.000
	0.000	0.000	0.000			
VOC	0.000	0.000	0.000			
DMA	0.000	0.000	0.000	0.000	0.000	0.000
MMA	0.000	0.000	0.000	0.000	0.000	0.000
TDMAT	0.000	0.000	0.000	0.000	0.000	0.000
TMS	0.000	0.000	0.000	0.000	0.000	0.000
TEOS	0.000	0.000	0.000	0.000	0.000	0.000
Formaldehyde (CH2O)	0.000	0.000	0.000	0.000	0.000	0.000
m-Cresol	0.000	0.000	0.000	0.000	0.000	0.000
p-Cresol	0.000	0.000	0.000	0.000	0.000	0.000
polypropylene glycol monomethyl ether acetate	0.000	0.000	0.000	0.000	0.000	0.000
	0.000	0.000	0.000			
FLAMMABLE						
SiH4	0.000	0.000	0.000	0.000	0.000	0.000
H2	2.902	2.902	2.902	0.000	0.000	0.000
DCS	0.000	0.000	0.000	0.000	0.000	0.000
B2H6	0.000	0.000	0.000	0.000	0.000	0.000
C4F8	0.000	0.000	0.000	0.000	0.000	0.000

Appendix B
Al Release Layer

Al releas layer - Handle wafer option	Totals		
UNITS in g/wafer wherever possible			
Film Thickness (nm)			
Time (s)			
	in	process out	post-POU
GWG			
CF4	0.000	0.000	0.000
CHF3	0.000	0.000	0.000
C2F6	0.000	0.000	0.000
CH4	0.000	0.000	0.000
CO2	0.000	0.000	0.000
NF3	0.350	0.007	0.007
C4F6	0.000	0.000	0.000
SF6	0.000	0.000	0.000
HAZARDOUS			
F2	0.000	0.203	0.203
HF (gas)	0.000	0.001	0.001
SiF4 (gas)	0.000	0.069	0.069
C4F8	0.000	0.000	0.000
C2F4	0.000	0.000	0.000
COF2	0.000	0.000	0.000
HCl (gas)	3.520	0.352	0.352
Cl2	0.000	0.000	0.000
SiCl4	0.000	0.000	0.000
PH3	0.000	0.000	0.000
Bis Tertiary-Butylamino Silane	0.000	0.000	0.000
AsH3	0.000	0.000	0.000
BCl3	0.000	0.000	0.000
Pb	0.000	0.000	0.000
WF6	0.000	0.000	0.000
HBr	0.000	0.000	0.000
Br2	0.000	0.000	0.000
CRITERIA			
CO	0.000	0.000	0.000
NO	0.000	0.000	0.000
NO2	0.000	0.000	90.000
SO2	0.000	0.000	0.000
N2O	0.000	0.000	0.000
VOC			
DMA	0.000	0.002	0.002
MMA	0.000	0.049	0.049
TDMAT	1.008	0.000	0.000
TMS	0.000	0.000	0.000
TEOS	0.000	0.000	0.000
Formaldehyde (CH2O)	0.000	0.000	0.000
m-Cresol	0.000	0.000	0.000
p-Cresol	0.000	0.000	0.000
polypropylene glycol monomethyl ether acetate	0.377	0.000	0.000
FLAMMABLE			
SiH4	0.000	0.000	0.000
H2	11.252	5.962	2.902
DCS	0.000	0.000	0.000
B2H6	0.000	0.000	0.000
C4F8	0.000	0.000	0.000

Appendix B
Al Release Layer

Al releas layer - Handle wafer option	Device Wafer Preparation					
UNITS in g/wafer wherever possible		Al deposition			Bonding layer	
		Sputtering			TiN/ Cu PVD	
Film Thickness (nm)		20000			50/300	
Time (s)	2400					
	in	process out	post-POU	in	process out	post-POU
OTHER CHEMICALS						
O2	0.000	0.000	0.000	0.000	0.000	0.000
Ar	40.796	40.796	40.796	0.327	0.327	0.327
N2	0.000	0.000	0.000	178.922	161.697	161.697
EP-C5003, Cabot	0.000	0.000	0.000	0.000	0.000	0.000
H2O2 (100%)	0.000	0.000	0.000	0.000	0.000	0.000
CUS silica slurry A	0.000	0.000	0.000	0.000	0.000	0.000
CUS silica slurry B	0.000	0.000	0.000	0.000	0.000	0.000
BTA, Aldrich	0.000	0.000	0.000	0.000	0.000	0.000
Sumiwash	0.000	0.000	0.000	0.000	0.000	0.000
ElectraClean,Ashland	0.000	0.000	0.000	0.000	0.000	0.000
Semi-Sperse W2000	0.000	0.000	0.000	0.000	0.000	0.000
Al	2.124	0.000	0.000	0.000	0.000	0.000
As	0.000	0.000	0.000	0.000	0.000	0.000
Cu	0.000	0.000	0.000	0.349	0.175	0.175
Pt	0.000	0.000	0.000	0.373	0.373	0.373
Ti	0.000	0.000	0.000	0.016	0.000	0.000
He	0.000	0.000	0.000	0.000	0.000	0.000
NH3	0.000	0.000	0.000	0.000	0.027	0.027
CuSO4	0.000	0.000	0.000	0.000	0.000	0.000
ArH	0.000	0.000	0.000	0.000	0.000	0.000
100% HF liquid	0.000	0.000	0.000	0.000	0.000	0.000
H2SO4	0.000	0.000	0.000	0.000	0.000	0.000
HCl	0.000	0.000	0.000	0.000	0.000	0.000
NH4OH	0.000	0.000	0.000	0.000	0.000	0.000
IPA	0.000	0.000	0.000	0.000	0.000	0.000
Oxide CMP Slurry& chemicals	0.000	0.000	0.000	0.000	0.000	0.000
BF3	0.000	0.000	0.000	0.000	0.000	0.000
ethyl lactate	0.000	0.000	0.000	0.000	0.000	0.000
Cr	0.000	0.000	0.000	0.000	0.000	0.000
Au	0.000	0.000	0.000	0.000	0.000	0.000
Sn	0.000	0.000	0.000	0.000	0.000	0.000
Co	0.000	0.000	0.000	0.000	0.000	0.000
polyimide laminate	0.000	0.000	0.000	0.000	0.000	0.000
laminate solvent	0.000	0.000	0.000	0.000	0.000	0.000
utility N2	100.036	100.036	100.036	132.797	132.797	132.797
silicon	0.000	0.000	0.000	0.000	0.000	0.000
H3PO4	0.000	0.000	0.000	0.000	0.000	0.000
CuCl2	0.000	0.000	0.000	0.000	0.000	0.000
AlCl3	0.000	0.000	0.000	0.000	0.000	0.000
OTHERS						
Electricity (KWhr)	137.354	0.000	0.000	0.762	0.000	0.000
UPW	0.000	0.000	0.000	0.000	0.000	0.000
Industrial City Water	0.000	0.000	0.000	0.000	0.000	0.000
PCW	4825396.825	0.000	0.000	98713.294	0.000	0.000
Fluoride Wastewater (H2O)	0.000	0.000	0.000	0.000	0.000	0.000
Industrial Wastewater (H2O)	0.000	0.000	0.000	0.000	0.000	0.000
Ammonia Waste (NH3)	0.000	0.000	0.000	0.000	0.000	0.000
HF liquid waste to Fluoride treatment	0.000	0.000	0.000	0.000	0.000	0.000
SiF4 liquid waste to Fluoride treatment	0.000	0.000	0.000	0.000	0.000	0.000
NH4OH waste	0.000	0.000	0.000	0.000	0.000	0.000
H2O2 to ammonia waste	0.000	0.000	0.000	0.000	0.000	0.000

Appendix B
Al Release Layer

Al releas layer - Handle wafer option	Handle Wafer Preparation					
UNITS in g/wafer wherever possible		Wafer Clean			Oxidation	
		RCA Batch process		Furnace Batch process wet oxidation		
Film Thickness (nm)					500	
Time (s)				8100		
	in	process out	post-POU	in	process out	post-POU
OTHER CHEMICALS						
O2	0.000	0.000	0.000	106.00	26.35	9.49
Ar	0.000	0.000	0.000	0.00	0.00	0.00
N2	0.000	0.000	0.000	2250.00	2250.00	2250.00
EP-C5003, Cabot	0.000	0.000	0.000	0.00	0.00	0.00
H2O2 (100%)	688.500	688.500	688.500	0.00	0.00	0.00
CUS silica slurry A	0.000	0.000	0.000	0.00	0.00	0.00
CUS silica slurry B	0.000	0.000	0.000	0.00	0.00	0.00
BTA, Aldrich	0.000	0.000	0.000	0.00	0.00	0.00
Sumiwash	0.000	0.000	0.000	0.00	0.00	0.00
ElectraClean,Ashland	0.000	0.000	0.000	0.00	0.00	0.00
Semi-Sperse W2000	0.000	0.000	0.000	0.00	0.00	0.00
Al	0.000	0.000	0.000	0.00	0.00	0.00
As	0.000	0.000	0.000	0.00	0.00	0.00
Cu	0.000	0.000	0.000	0.00	0.00	0.00
Pt	0.000	0.000	0.000	0.00	0.00	0.00
Ti	0.000	0.000	0.000	0.00	0.00	0.00
He	0.000	0.000	0.000	0.00	0.00	0.00
NH3	0.000	0.277	0.277	0.00	0.00	0.00
CuSO4	0.000	0.000	0.000	0.00	0.00	0.00
ArH	0.000	0.000	0.000	0.00	0.00	0.00
100% HF liquid	1.216	0.000	0.000	0.00	0.00	0.00
H2SO4	0.000	0.000	0.000	0.00	0.00	0.00
HCl	469.800	0.000	0.000	0.00	0.00	0.00
NH4OH	582.750	582.473	582.473	0.00	0.00	0.00
IPA	0.000	0.000	0.000	0.00	0.00	0.00
Oxide CMP Slurry& chemicals	0.000	0.000	0.000	0.00	0.00	0.00
BF3	0.000	0.000	0.000	0.00	0.00	0.00
ethyl lactate	0.000	0.000	0.000	0.00	0.00	0.00
Cr	0.000	0.000	0.000	0.00	0.00	0.00
Au	0.000	0.000	0.000	0.00	0.00	0.00
Sn	0.000	0.000	0.000	0.00	0.00	0.00
Co	0.000	0.000	0.000	0.00	0.00	0.00
polyimide laminate	0.000	0.000	0.000	0.00	0.00	0.00
laminate solvent	0.000	0.000	0.000	0.00	0.00	0.00
utility N2	0.000	0.000	0.000	1491.43	1491.43	1491.43
silicon	0.000	0.000	0.000	0.00	0.00	0.00
H3PO4	0.000	0.000	0.000	0.00	0.00	0.00
CuCl2	0.000	0.000	0.000	0.00	0.00	0.00
AlCl3	0.000	0.000	0.000	0.00	0.00	0.00
OTHERS						
Electricity (KWhr)	0.106	0.000	0.000	6.13	0.00	0.00
UPW	251419.090	0.000	0.000	0.00	0.00	0.00
Industrial City Water	0.000	0.000	0.000	0.00	0.00	0.00
PCW	0.000	0.000	0.000	3908571.43	0.00	0.00
Fluoride Wastewater (H2O)	0.000	0.000	0.000	0.00	0.00	0.00
Industrial Wastewater (H2O)	0.000	0.000	251419.090	0.00	0.00	0.00
Ammonia Waste (NH3)	0.000	0.000	0.000	0.00	0.00	0.00
HF liquid waste to Fluoride treatment	0.000	1.216	1.216	0.00	0.00	0.00
SiF4 liquid waste to Fluoride treatment	0.000	0.000	0.000	0.00	0.00	0.00
NH4OH waste	0.000	0.000	0.000	0.00	0.00	0.00
H2O2 to ammonia waste	0.000	0.000	0.000	0.00	0.00	0.00

Appendix B
Al Release Layer

Al releas layer - Handle wafer option						
UNITS in g/wafer wherever possible		**Al deposition**			**Bonding Layer**	
		Sputtering			TiN/Cu PVD	
Film Thickness (nm)		20000			50/300	
Time (s)	2400.00					
	in	process out	post-POU	in	process out	post-POU
OTHER CHEMICALS						
O2	0.000	0.000	0.000	0.000	0.000	0.000
Ar	40.796	40.796	40.796	0.327	0.327	0.327
N2	0.000	0.000	0.000	178.922	161.697	161.697
EP-C5003, Cabot	0.000	0.000	0.000	0.000	0.000	0.000
H2O2 (100%)	0.000	0.000	0.000	0.000	0.000	0.000
CUS silica slurry A	0.000	0.000	0.000	0.000	0.000	0.000
CUS silica slurry B	0.000	0.000	0.000	0.000	0.000	0.000
BTA, Aldrich	0.000	0.000	0.000	0.000	0.000	0.000
Sumiwash	0.000	0.000	0.000	0.000	0.000	0.000
ElectraClean,Ashland	0.000	0.000	0.000	0.000	0.000	0.000
Semi-Sperse W2000	0.000	0.000	0.000	0.000	0.000	0.000
Al	2.124	0.000	0.000	0.000	0.000	0.000
As	0.000	0.000	0.000	0.000	0.000	0.000
Cu	0.000	0.000	0.000	0.349	0.175	0.175
Pt	0.000	0.000	0.000	0.373	0.373	0.373
Ti	0.000	0.000	0.000	0.016	0.000	0.000
He	0.000	0.000	0.000	0.000	0.000	0.000
NH3	0.000	0.000	0.000	0.000	0.027	0.027
CuSO4	0.000	0.000	0.000	0.000	0.000	0.000
ArH	0.000	0.000	0.000	0.000	0.000	0.000
100% HF liquid	0.000	0.000	0.000	0.000	0.000	0.000
H2SO4	0.000	0.000	0.000	0.000	0.000	0.000
HCl	0.000	0.000	0.000	0.000	0.000	0.000
NH4OH	0.000	0.000	0.000	0.000	0.000	0.000
IPA	0.000	0.000	0.000	0.000	0.000	0.000
Oxide CMP Slurry& chemicals	0.000	0.000	0.000	0.000	0.000	0.000
BF3	0.000	0.000	0.000	0.000	0.000	0.000
ethyl lactate	0.000	0.000	0.000	0.000	0.000	0.000
Cr	0.000	0.000	0.000	0.000	0.000	0.000
Au	0.000	0.000	0.000	0.000	0.000	0.000
Sn	0.000	0.000	0.000	0.000	0.000	0.000
Co	0.000	0.000	0.000	0.000	0.000	0.000
polyimide laminate	0.000	0.000	0.000	0.000	0.000	0.000
laminate solvent	0.000	0.000	0.000	0.000	0.000	0.000
utility N2	100.036	100.036	100.036	132.797	132.797	132.797
silicon	0.000	0.000	0.000	0.000	0.000	0.000
H3PO4	0.000	0.000	0.000	0.000	0.000	0.000
CuCl2	0.000	0.000	0.000	0.000	0.000	0.000
AlCl3	0.000	0.000	0.000	0.000	0.000	0.000
OTHERS						
Electricity (KWhr)	137.354	0.000	0.000	0.762	0.000	0.000
UPW	0.000	0.000	0.000	0.000	0.000	0.000
Industrial City Water	0.000	0.000	0.000	0.000	0.000	0.000
PCW	4825396.825	0.000	0.000	98713.294	0.000	0.000
Fluoride Wastewater (H2O)	0.000	0.000	0.000	0.000	0.000	0.000
Industrial Wastewater (H2O)	0.000	0.000	0.000	0.000	0.000	0.000
Ammonia Waste (NH3)	0.000	0.000	0.000	0.000	0.000	0.000
HF liquid waste to Fluoride treatment	0.000	0.000	0.000	0.000	0.000	0.000
SiF4 liquid waste to Fluoride treatment	0.000	0.000	0.000	0.000	0.000	0.000
NH4OH waste	0.000	0.000	0.000	0.000	0.000	0.000
H2O2 to ammonia waste	0.000	0.000	0.000	0.000	0.000	0.000

Appendix B
Al Release Layer

Al releas layer - Handle wafer option	Bonded Stack					
UNITS in g/wafer wherever possible	Copper Bonding and annealing				HCL release	
		(modeled on coper annealing)			Acid bath -wet bench	
Film Thickness (nm)				(36% by wt in 1:1 solution with H2O)		
Time (s)	10800			Not determined		
				in	process out	post-POU
OTHER CHEMICALS						
O2	0.000	0.000	0.000	0.000	0.000	0.000
Ar	0.000	0.000	0.000	0.000	0.000	0.000
N2	281.250	281.250	281.250	0.000	0.000	0.000
EP-C5003, Cabot	0.000	0.000	0.000	0.000	0.000	0.000
H2O2 (100%)	0.000	0.000	0.000	50.000	50.000	50.000
CUS silica slurry A	0.000	0.000	0.000	0.000	0.000	0.000
CUS silica slurry B	0.000	0.000	0.000	0.000	0.000	0.000
BTA, Aldrich	0.000	0.000	0.000	0.000	0.000	0.000
Sumiwash	0.000	0.000	0.000	0.000	0.000	0.000
ElectraClean,Ashland	0.000	0.000	0.000	0.000	0.000	0.000
Semi-Sperse W2000	0.000	0.000	0.000	0.000	0.000	0.000
Al	0.000	0.000	0.000	0.000	0.000	0.000
As	0.000	0.000	0.000	0.000	0.000	0.000
Cu	0.000	0.000	0.000	0.000	0.000	0.000
Pt	0.000	0.000	0.000	0.000	0.000	0.000
Ti	0.000	0.000	0.000	0.000	0.000	0.000
He	0.000	0.000	0.000	0.000	0.000	0.000
NH3	0.000	0.000	0.000	0.000	0.000	0.000
CuSO4	0.000	0.000	0.000	0.000	0.000	0.000
ArH	0.000	0.000	0.000	0.000	0.000	0.000
100% HF liquid	0.000	0.000	0.000	0.000	0.000	0.000
H2SO4	0.000	0.000	0.000	0.000	0.000	0.000
HCl	0.000	0.000	0.000	469.800	440.000	440.000
NH4OH	0.000	0.000	0.000	0.000	0.000	0.000
IPA	0.000	0.000	0.000	0.000	0.000	0.000
Oxide CMP Slurry& chemicals	0.000	0.000	0.000	0.000	0.000	0.000
BF3	0.000	0.000	0.000	0.000	0.000	0.000
ethyl lactate	0.000	0.000	0.000	0.000	0.000	0.000
Cr	0.000	0.000	0.000	0.000	0.000	0.000
Au	0.000	0.000	0.000	0.000	0.000	0.000
Sn	0.000	0.000	0.000	0.000	0.000	0.000
Co	0.000	0.000	0.000	0.000	0.000	0.000
polyimide laminate	0.000	0.000	0.000	0.000	0.000	0.000
laminate solvent	0.000	0.000	0.000	0.000	0.000	0.000
utility N2	0.000	0.000	0.000	0.000	0.000	0.000
silicon	0.000	0.000	0.000	0.000	0.000	0.000
H3PO4	0.000	0.000	0.000	0.000	0.000	0.000
CuCl2	0.000	0.000	0.000	0.000	0.000	0.000
AlCl3	0.000	0.000	0.000	0.000	63.000	63.000
OTHERS						
Electricity (KWhr)	13.974	0.000	0.000	0.106	0.000	0.000
UPW	0.000	0.000	0.000	251419.090	0.000	0.000
Industrial City Water	0.000	0.000	0.000	0.000	0.000	0.000
PCW	1020625.000	0.000	0.000	0.000	0.000	0.000
Fluoride Wastewater (H2O)	0.000	0.000	0.000	0.000	0.000	0.000
Industrial Wastewater (H2O)	0.000	0.000	0.000	0.000	0.000	251419.090
Ammonia Waste (NH3)	0.000	0.000	0.000	0.000	0.000	0.000
HF liquid waste to Fluoride treatment	0.000	0.000	0.000	0.000	0.000	0.000
SiF4 liquid waste to Fluoride treatment	0.000	0.000	0.000	0.000	0.000	0.000
NH4OH waste	0.000	0.000	0.000	0.000	0.000	0.000
H2O2 to ammonia waste	0.000	0.000	0.000	0.000	0.000	0.000

Appendix B
Al Release Layer

Al releas layer - Handle wafer option	Totals		
UNITS in g/wafer wherever possible			
Film Thickness (nm)			
Time (s)			
	in	process out	post-POU
OTHER CHEMICALS			
O2	106.000	26.350	9.489
Ar	82.245	82.245	82.245
N2	2889.093	2854.643	2854.643
EP-C5003, Cabot	0.000	0.000	0.000
H2O2 (100%)	738.500	738.500	738.500
CUS silica slurry A	0.000	0.000	0.000
CUS silica slurry B	0.000	0.000	0.000
BTA, Aldrich	0.000	0.000	0.000
Sumiwash	0.000	0.000	0.000
ElectraClean,Ashland	0.000	0.000	0.000
Semi-Sperse W2000	0.000	0.000	0.000
Al	4.248	0.000	0.000
As	0.000	0.000	0.000
Cu	0.698	0.349	0.349
Pt	0.746	0.746	0.746
Ti	0.032	0.000	0.000
He	0.000	0.000	0.000
NH3	0.000	0.332	0.332
CuSO4	0.000	0.000	0.000
ArH	0.000	0.000	0.000
100% HF liquid	1.216	0.000	0.000
H2SO4	0.000	0.000	0.000
HCl	939.600	440.000	440.000
NH4OH	582.750	582.473	582.473
IPA	0.000	0.000	0.000
Oxide CMP Slurry& chemicals	0.000	0.000	0.000
BF3	0.000	0.000	0.000
ethyl lactate	0.000	0.000	0.000
Cr	0.000	0.000	0.000
Au	0.000	0.000	0.000
Sn	0.000	0.000	0.000
Co	0.000	0.000	0.000
polyimide laminate	0.000	0.000	0.000
laminate solvent	0.000	0.000	0.000
utility N2	1957.095	1957.095	1957.095
silicon	0.000	0.000	0.000
H3PO4	0.000	0.000	0.000
CuCl2	0.000	0.000	0.000
AlCl3	0.000	63.000	63.000
OTHERS			
Electricity (KWhr)	296.546	0.000	0.000
UPW	502838.179	0.000	0.000
Industrial City Water	0.000	0.000	0.000
PCW	14777416.667	0.000	0.000
Fluoride Wastewater (H2O)	0.000	0.000	0.000
Industrial Wastewater (H2O)	0.000	0.000	502838.179
Ammonia Waste (NH3)	0.000	0.000	0.000
HF liquid waste to Fluoride treatment	0.000	1.216	1.216
SiF4 liquid waste to Fluoride treatment	0.000	0.000	0.000
NH4OH waste	0.000	0.000	0.000
H2O2 to ammonia waste	0.000	0.000	0.000

Appendix C
Smart Cut

Oxide release layer	Device Wafer Preparation			Handle Wafer Preparation					
UNITS in g/wafer wherever possible	Activation Plasma + Piranha				Wafer Clean			Oxidation	
	Oxygen plasma followed by Piranha				RCA Batch process		Furnace Batch process wet oxidation		
Film Thickness (nm)								500	
Time (s)	30+120						8100		
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
GWG									
CF4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CHF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C2F6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CH4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SF6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HAZARDOUS									
F2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HF (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiF4 (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F8	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C2F4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
COF2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HCl (gas)	0.00	0.00	0.00	0.00	0.00	0.00	3.52	0.35	0.35
Cl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiCl4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Bis Tertiary-Butylamino Silane	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AsH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pb	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
WF6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HBr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Br2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CRITERIA									
CO	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NO	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	90.00
SO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
N2O	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
VOC									
DMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TDMAT	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TMS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TEOS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Formaldehyde (CH2O)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
m-Cresol	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
p-Cresol	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
polypropylene glycol monomethyl ether ace	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
FLAMMABLE									
SiH4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2	0.00	0.00	0.00	0.00	0.00	0.00	8.35	3.06	0.00
DCS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
B2H6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F8	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

Appendix C
Smart Cut

Oxide release layer							Bonded Stack		
UNITS in g/wafer wherever possible	Hydrogen Implantation			Activation Plasma + Piranha			Oxide Bonding and Annealing		
				Oxygen plasma followed by Piranha					
Film Thickness (nm)									
Time (s)	200-300			30+120			120+ 10800		
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
GWG									
CF4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CHF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C2F6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CH4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SF6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HAZARDOUS									
F2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HF (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiF4 (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F8	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C2F4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
COF2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HCl (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiCl4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Bis Tertiary-Butylamino Silane	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AsH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pb	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
WF6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HBr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Br2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CRITERIA									
CO	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NO	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
N2O	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
VOC									
DMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TDMAT	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TMS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TEOS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Formaldehyde (CH2O)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
m-Cresol	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
p-Cresol	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
polypropylene glycol monomethyl ether ace	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
FLAMMABLE									
SiH4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2	0.50	0.45	0.00	0.00	0.00	0.00	0.12	0.12	0.12
DCS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
B2H6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F8	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

Appendix C
Smart Cut

Oxide release layer				Totals		
UNITS in g/wafer wherever possible		Annealing				
	Anneal in furnace at 300C					
Film Thickness (nm)						
Time (s)	3600					
	in	process out	post-POU	in	process out	post-POU
GWG						
CF4	0.00	0.00	0.00	0.00	0.00	0.00
CHF3	0.00	0.00	0.00	0.00	0.00	0.00
C2F6	0.00	0.00	0.00	0.00	0.00	0.00
CH4	0.00	0.00	0.00	0.00	0.00	0.00
CO2	0.00	0.00	0.00	0.00	0.00	0.00
NF3	0.00	0.00	0.00	0.00	0.00	0.00
C4F6	0.00	0.00	0.00	0.00	0.00	0.00
SF6	0.00	0.00	0.00	0.00	0.00	0.00
HAZARDOUS						
F2	0.00	0.00	0.00	0.00	0.00	0.00
HF (gas)	0.00	0.00	0.00	0.00	0.00	0.00
SiF4 (gas)	0.00	0.00	0.00	0.00	0.00	0.00
C4F8	0.00	0.00	0.00	0.00	0.00	0.00
C2F4	0.00	0.00	0.00	0.00	0.00	0.00
COF2	0.00	0.00	0.00	0.00	0.00	0.00
HCl (gas)	0.00	0.00	0.00	3.52	0.35	0.35
Cl2	0.00	0.00	0.00	0.00	0.00	0.00
SiCl4	0.00	0.00	0.00	0.00	0.00	0.00
PH3	0.00	0.00	0.00	0.00	0.00	0.00
Bis Tertiary-Butylamino Silane	0.00	0.00	0.00	0.00	0.00	0.00
AsH3	0.00	0.00	0.00	0.00	0.00	0.00
BCl3	0.00	0.00	0.00	0.00	0.00	0.00
Pb	0.00	0.00	0.00	0.00	0.00	0.00
WF6	0.00	0.00	0.00	0.00	0.00	0.00
HBr	0.00	0.00	0.00	0.00	0.00	0.00
Br2	0.00	0.00	0.00	0.00	0.00	0.00
CRITERIA						
CO	0.00	0.00	0.00	0.00	0.00	0.00
NO	0.00	0.00	0.00	0.00	0.00	0.00
NO2	0.00	0.00	0.00	0.00	0.00	90.00
SO2	0.00	0.00	0.00	0.00	0.00	0.00
N2O	0.00	0.00	0.00	0.00	0.00	0.00
VOC						
DMA	0.00	0.00	0.00	0.00	0.00	0.00
MMA	0.00	0.00	0.00	0.00	0.00	0.00
TDMAT	0.00	0.00	0.00	0.00	0.00	0.00
TMS	0.00	0.00	0.00	0.00	0.00	0.00
TEOS	0.00	0.00	0.00	0.00	0.00	0.00
Formaldehyde (CH2O)	0.00	0.00	0.00	0.00	0.00	0.00
m-Cresol	0.00	0.00	0.00	0.00	0.00	0.00
p-Cresol	0.00	0.00	0.00	0.00	0.00	0.00
polypropylene glycol monomethyl ether ace	0.00	0.00	0.00	0.00	0.00	0.00
FLAMMABLE						
SiH4	0.00	0.00	0.00	0.00	0.00	0.00
H2	0.00	0.00	0.00	8.97	3.63	0.12
DCS	0.00	0.00	0.00	0.00	0.00	0.00
B2H6	0.00	0.00	0.00	0.00	0.00	0.00
C4F8	0.00	0.00	0.00	0.00	0.00	0.00

Appendix C
Smart Cut

Oxide release layer	Device Wafer Preparation			Handle Wafer Preparation					
UNITS in g/wafer wherever possible	Activation Plasma + Piranha				Wafer Clean			Oxidation	
	Oxygen plasma followed by Piranha				RCA Batch process		Furnace Batch process wet oxidation		
Film Thickness (nm)								500	
Time (s)	30+120						8100		
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
OTHER CHEMICALS									
O2	0.13	0.13	0.13	0.00	0.00	0.00	106.00	26.35	9.49
Ar	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
N2	0.00	0.00	0.00	0.00	0.00	0.00	2250.00	2250.00	2250.00
EP-C5003, Cabot	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2O2 (100%)	1377.00	275.40	275.40	688.50	688.50	688.50	0.00	0.00	0.00
CUS silica slurry A	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CUS silica slurry B	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BTA, Aldrich	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sumiwash	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ElectraClean,Ashland	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Semi-Sperse W2000	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Al	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
As	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cu	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pt	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Ti	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
He	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH3	0.00	0.00	0.00	0.00	0.28	0.28	0.00	0.00	0.00
CuSO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ArH	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
100% HF liquid	0.00	0.00	0.00	1.22	0.00	0.00	0.00	0.00	0.00
H2SO4	23814.00	23814.00	23814.00	0.00	0.00	0.00	0.00	0.00	0.00
HCl	0.00	0.00	0.00	469.80	0.00	0.00	0.00	0.00	0.00
NH4OH	0.00	0.00	0.00	582.75	582.47	582.47	0.00	0.00	0.00
IPA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Oxide CMP Slurry& chemicals	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ethyl lactate	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Au	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sn	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Co	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
polyimide laminate	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
laminate solvent	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
utility N2	2974.86	2974.86	2974.86	0.00	0.00	0.00	1491.43	1491.43	1491.43
silicon	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H3PO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CuCl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AlCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
OTHERS									
Electricity (KWhr)	0.56	0.00	0.00	0.11	0.00	0.00	6.13	0.00	0.00
UPW	75844.39	0.00	0.00	251419.09	0.00	0.00	0.00	0.00	0.00
Industrial City Water	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PCW	0.46	0.00	0.00	0.00	0.00	0.00	3908571.43	0.00	0.00
Fluoride Wastewater (H2O)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Industrial Wastewater (H2O)	0.00	0.00	76945.99	0.00	0.00	251419.09	0.00	0.00	0.00
Ammonia Waste (NH3)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HF liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	1.22	1.22	0.00	0.00	0.00
SiF4 liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH4OH waste	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2O2 to ammonia waste	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

Appendix C
Smart Cut

Oxide release layer							Bonded Stack		
UNITS in g/wafer wherever possible	Hydrogen Implantation			Activation Plasma + Piranha			Oxide Bonding and Annealing		
				Oxygen plasma followed by Piranha					
Film Thickness (nm)									
Time (s)	200-300			30+120			120+ 10800		
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
OTHER CHEMICALS									
O2	9.49	3.49	0.00	0.13	0.13	0.13	0.00	0.00	0.00
Ar	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
N2	85.03	85.03	85.03	0.00	0.00	0.00	11.25	11.25	11.25
EP-C5003, Cabot	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2O2 (100%)	0.00	0.00	0.00	1377.00	275.40	275.40	0.00	0.00	0.00
CUS silica slurry A	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CUS silica slurry B	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BTA, Aldrich	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sumiwash	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ElectraClean,Ashland	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Semi-Sperse W2000	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Al	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
As	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cu	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pt	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Ti	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
He	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CuSO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ArH	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
100% HF liquid	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2SO4	0.00	0.00	0.00	23814.00	23814.00	23814.00	0.00	0.00	0.00
HCl	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH4OH	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
IPA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Oxide CMP Slurry& chemicals	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ethyl lactate	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Au	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sn	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Co	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
polyimide laminate	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
laminate solvent	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
utility N2	1457.64	1457.64	1457.64	2974.86	2974.86	2974.86	0.00	0.00	0.00
silicon	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H3PO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CuCl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AlCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
OTHERS									
Electricity (KWhr)	11.73	0.00	0.00	0.56	0.00	0.00	0.56	0.00	0.00
UPW	0.00	0.00	0.00	75844.39	0.00	0.00	0.00	0.00	0.00
Industrial City Water	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PCW	567508.31	0.00	0.00	0.46	0.00	0.00	240825.00	0.00	0.00
Fluoride Wastewater (H2O)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Industrial Wastewater (H2O)	0.00	0.00	0.00	0.00	0.00	76945.99	0.00	0.00	0.00
Ammonia Waste (NH3)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HF liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiF4 liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH4OH waste	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2O2 to ammonia waste	0	0	0	0.00	0.00	0.00	0.00	0.00	0.00

Appendix C
Smart Cut

Oxide release layer				Totals		
UNITS in g/wafer wherever possible		Annealing				
	Anneal in furnace at 300C					
Film Thickness (nm)						
Time (s)	3600					
	in	process out	post-POU	in	process out	post-POU
OTHER CHEMICALS						
O2	0.00	0.00	0.00	115.76	30.11	9.76
Ar	0.00	0.00	0.00	0.00	0.00	0.00
N2	840.00	840.00	840.00	3186.28	3186.28	3186.28
EP-C5003, Cabot	0.00	0.00	0.00	0.00	0.00	0.00
H2O2 (100%)	0.00	0.00	0.00	3442.50	1239.30	1239.30
CUS silica slurry A	0.00	0.00	0.00	0.00	0.00	0.00
CUS silica slurry B	0.00	0.00	0.00	0.00	0.00	0.00
BTA, Aldrich	0.00	0.00	0.00	0.00	0.00	0.00
Sumiwash	0.00	0.00	0.00	0.00	0.00	0.00
ElectraClean,Ashland	0.00	0.00	0.00	0.00	0.00	0.00
Semi-Sperse W2000	0.00	0.00	0.00	0.00	0.00	0.00
Al	0.00	0.00	0.00	0.00	0.00	0.00
As	0.00	0.00	0.00	0.00	0.00	0.00
Cu	0.00	0.00	0.00	0.00	0.00	0.00
Pt	0.00	0.00	0.00	0.00	0.00	0.00
Ti	0.00	0.00	0.00	0.00	0.00	0.00
He	0.00	0.00	0.00	0.00	0.00	0.00
NH3	0.00	0.00	0.00	0.00	0.28	0.28
CuSO4	0.00	0.00	0.00	0.00	0.00	0.00
ArH	0.00	0.00	0.00	0.00	0.00	0.00
100% HF liquid	0.00	0.00	0.00	1.22	0.00	0.00
H2SO4	0.00	0.00	0.00	47628.00	47628.00	47628.00
HCl	0.00	0.00	0.00	469.80	0.00	0.00
NH4OH	0.00	0.00	0.00	582.75	582.47	582.47
IPA	0.00	0.00	0.00	0.00	0.00	0.00
Oxide CMP Slurry& chemicals	0.00	0.00	0.00	0.00	0.00	0.00
BF3	0.00	0.00	0.00	0.00	0.00	0.00
ethyl lactate	0.00	0.00	0.00	0.00	0.00	0.00
Cr	0.00	0.00	0.00	0.00	0.00	0.00
Au	0.00	0.00	0.00	0.00	0.00	0.00
Sn	0.00	0.00	0.00	0.00	0.00	0.00
Co	0.00	0.00	0.00	0.00	0.00	0.00
polyimide laminate	0.00	0.00	0.00	0.00	0.00	0.00
laminate solvent	0.00	0.00	0.00	0.00	0.00	0.00
utility N2	0.00	0.00	0.00	8898.79	8898.79	8898.79
silicon	0.00	0.00	0.00	0.00	0.00	0.00
H3PO4	0.00	0.00	0.00	0.00	0.00	0.00
CuCl2	0.00	0.00	0.00	0.00	0.00	0.00
AlCl3	0.00	0.00	0.00	0.00	0.00	0.00
OTHERS						
Electricity (KWhr)	0.56	0.00	0.00	20.21	0.00	0.00
UPW	0.00	0.00	0.00	403107.88	0.00	0.00
Industrial City Water	0.00	0.00	0.00	0.00	0.00	0.00
PCW	240825.00	0.00	0.00	4957730.65	0.00	0.00
Fluoride Wastewater (H2O)	0.00	0.00	0.00	0.00	0.00	0.00
Industrial Wastewater (H2O)	0.00	0.00	0.00	0.00	0.00	405311.08
Ammonia Waste (NH3)	0.00	0.00	0.00	0.00	0.00	0.00
HF liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	1.22	1.22
SiF4 liquid waste to Fluoride treatment	0	0	0	0.00	0.00	0.00
NH4OH waste	0	0	0	0.00	0.00	0.00
H2O2 to ammonia waste	0	0	0	0.00	0.00	0.00

Appendix D
Oxide Release Layer

Oxide release layer	Device Wafer Preparation			Handle Wafer Preparation					
UNITS in g/wafer wherever possible	Activation Plasma + Piranha				Lithography			Etch Silicon	
	Oxygen plasma followed by Piranha			Die-saw mask Thick positive resist				Bosch process	
Film Thickness (nm)								50000	
Time (s)	30+120			120			3000+300		
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
GWG									
CF4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	1.86	0.02
CHF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.24	0.18
C2F6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.24	0.24
CH4	0.00	0.00	0.00	0.00	0.00	0.00	198.21	0.00	0.00
CO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.24	544.71
NF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F6	0.00	0.00	0.00	0.00	0.00	0.00	0.36	0.03	0.03
SF6	0.00	0.00	0.00	0.00	0.00	0.00	68.02	6.80	0.68
HAZARDOUS									
F2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.60	0.00
HF (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.60	0.00
SiF4 (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	15.24	12.19
C4F8	0.00	0.00	0.00	0.00	0.00	0.00	17.85	3.57	0.71
C2F4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	3.34	0.54
COF2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.06	0.04
HCl (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiCl4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Bis Tertiary-Butylamino Silane	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AsH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pb	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
WF6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HBr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Br2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CRITERIA									
CO	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.24	0.24
NO	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	32.85
N2O	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
VOC									
DMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TDMAT	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TMS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TEOS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Formaldehyde (CH2O)	0.00	0.00	0.00	2.28	2.24	2.24	0.00	0.00	0.00
m-Cresol	0.00	0.00	0.00	1.45	1.42	1.42	0.00	0.00	0.00
p-Cresol	0.00	0.00	0.00	1.43	1.41	1.41	0.00	0.00	0.00
polypropylene glycol monomethyl ether ac	0.00	0.00	0.00	5.46	5.46	5.46	0.00	0.00	0.00
FLAMMABLE									
SiH4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
DCS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
B2H6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F8	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

Appendix D
Oxide Release Layer

Oxide release layer									
UNITS in g/wafer wherever possible	Strip PR + Piranha			Wafer Clean			Oxidation		
	Striping resist in oxygen plasma			RCA Batch process			Furnace Batch process wet oxidation		
Film Thickness (nm)	Followed by wet bench batch process						200		
Time (s)	60+120			120			5400		
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
GWG									
CF4	0.12	0.34	0.34	0.00	0.00	0.00	0.00	0.00	0.00
CHF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C2F6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CH4	0.39	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CO2	0.00	0.15	0.15	0.00	0.00	0.00	0.00	0.00	0.00
NF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SF6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HAZARDOUS									
F2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HF (gas)	0.00	0.02	0.02	0.00	0.00	0.00	0.00	0.00	0.00
SiF4 (gas)	0.00	0.02	0.02	0.00	0.00	0.00	0.00	0.00	0.00
C4F8	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C2F4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
COF2	0.00	0.88	0.88	0.00	0.00	0.00	0.00	0.00	0.00
HCl (gas)	0.00	0.00	0.00	0.00	0.00	0.00	2.35	0.23	0.23
Cl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiCl4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Bis Tertiary-Butylamino Silane	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AsH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pb	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
WF6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HBr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Br2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CRITERIA									
CO	0.00	0.15	0.15	0.00	0.00	0.00	0.00	0.00	0.00
NO	0.00	0.15	0.15	0.00	0.00	0.00	0.00	0.00	0.00
NO2	0.00	0.20	0.20	0.00	0.00	0.00	0.00	0.00	60.00
SO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
N2O	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
VOC									
DMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TDMAT	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TMS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TEOS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Formaldehyde (CH2O)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
m-Cresol	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
p-Cresol	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
polypropylene glycol monomethyl ether ac	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
FLAMMABLE									
SiH4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2	0.00	0.00	0.00	0.00	0.00	0.00	5.57	2.04	0.00
DCS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
B2H6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F8	0.00	0.01	0.01	0.00	0.00	0.00	0.00	0.00	0.00

Appendix D
Oxide Release Layer

Oxide release layer				Bonded Stack						Totals		
UNITS in g/wafer wherever possible	Activation Plasma + Piranha			Oxide Bonding and Annealing				HF release				
	Oxygen plasma followed by Piranha							Acid bath -wet bench				
Film Thickness (nm)							49% by wt HF (concentrated)					
Time (s)	30+120			120+ 10800			2400					
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
GWG												
CF4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.12	2.20	0.36
CHF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.24	0.18
C2F6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.24	0.24
CH4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	198.60	0.00	0.00
CO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.39	544.86
NF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.36	0.03	0.03
SF6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	68.02	6.80	0.68
HAZARDOUS												
F2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.60	0.00
HF (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.62	0.02
SiF4 (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	15.26	12.21
C4F8	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	17.85	3.57	0.71
C2F4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	3.34	0.54
COF2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.94	0.92
HCl (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	2.35	0.23	0.23
Cl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiCl4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Bis Tertiary-Butylamino Silane	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AsH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pb	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
WF6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HBr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Br2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CRITERIA												
CO	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.39	0.39
NO	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.15	0.15
NO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.20	60.20
SO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	32.85
N2O	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
VOC												
DMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TDMAT	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TMS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TEOS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Formaldehyde (CH2O)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	2.28	2.24	2.24
m-Cresol	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	1.45	1.42	1.42
p-Cresol	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	1.43	1.41	1.41
polypropylene glycol monomethyl ether ac	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	5.46	5.46	5.46
FLAMMABLE												
SiH4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2	0.00	0.00	0.00	0.12	0.12	0.12	0.00	0.00	0.00	5.68	2.16	0.12
DCS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
B2H6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F8	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.01	0.01

Appendix D
Oxide Release Layer

Oxide release layer	Device Wafer Preparation			Handle Wafer Preparation					
UNITS in g/wafer wherever possible	Activation Plasma + Piranha			Lithography				Etch Silicon	
	Oxygen plasma followed by Piranha			Die-saw mask Thick positive resist				Bosch process	
Film Thickness (nm)								50000	
Time (s)	30+120			120			3000+300		
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
OTHER CHEMICALS									
O2	0.13	0.13	0.13	0.00	0.00	0.00	642.86	15.00	15.00
Ar	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
N2	0.00	0.00	0.00	0.00	0.00	0.00	1.87	1.87	1.87
EP-C5003, Cabot	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2O2 (100%)	1377.00	275.40	275.40	0.00	0.00	0.00	0.00	0.00	0.00
CUS silica slurry A	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CUS silica slurry B	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BTA, Aldrich	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sumiwash	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ElectraClean,Ashland	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Semi-Sperse W2000	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Al	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
As	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cu	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pt	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Ti	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
He	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CuSO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ArH	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
100% HF liquid	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2SO4	23814.00	23814.00	23814.00	0.00	0.00	0.00	0.00	0.00	0.00
HCl	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH4OH	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
IPA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Oxide CMP Slurry& chemicals	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ethyl lactate	0.00	0.00	0.00	5.79	5.68	5.68	0.00	0.00	0.00
Cr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Au	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sn	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Co	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
polyimide laminate	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
laminate solvent	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
utility N2	2974.86	2974.86	2974.86	125.00	125.00	125.00	249.89	249.89	249.89
silicon	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H3PO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CuCl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AlCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
OTHERS									
Electricity (KWhr)	0.56	0.00	0.00	2.82	0.00	0.00	50.00	0.00	0.00
UPW	75844.39	0.00	0.00	61.88	0.00	0.00	0.00	0.00	0.00
Industrial City Water	0.00	0.00	0.00	0.00	0.00	0.00	43149.00	0.00	0.00
PCW	0.46	0.00	0.00	200000.00	0.00	0.00	170325.00	0.00	170325.00
Fluoride Wastewater (H2O)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	43149.00
Industrial Wastewater (H2O)	0.00	0.00	76945.99	0.00	0.00	0.00	0.00	0.00	0.00
Ammonia Waste (NH3)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HF liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiF4 liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH4OH waste	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2O2 to ammonia waste	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

Appendix D
Oxide Release Layer

Oxide release layer									
UNITS in g/wafer wherever possible	Strip PR + Piranha			Wafer Clean			Oxidation		
	Striping resist in oxygen plasma			RCA Batch process			Furnace Batch process wet oxidation		
Film Thickness (nm)	Followed by wet bench batch process							200	
Time (s)	60+120			120			5400		
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
OTHER CHEMICALS									
O2	32.00	12.00	12.00	0.00	0.00	0.00	70.67	17.57	6.33
Ar	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
N2	0.00	0.00	0.00	0.00	0.00	0.00	1500.00	1500.00	1500.00
EP-C5003, Cabot	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2O2 (100%)	1377.00	275.40	275.40	688.50	688.50	688.50	0.00	0.00	0.00
CUS silica slurry A	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CUS silica slurry B	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BTA, Aldrich	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sumiwash	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ElectraClean,Ashland	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Semi-Sperse W2000	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Al	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
As	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cu	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pt	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Ti	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
He	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH3	0.00	0.00	0.00	0.00	0.28	0.28	0.00	0.00	0.00
CuSO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ArH	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
100% HF liquid	0.00	0.00	0.00	1.22	0.00	0.00	0.00	0.00	0.00
H2SO4	23814.00	23814.00	23814.00	0.00	0.00	0.00	0.00	0.00	0.00
HCl	0.00	0.00	0.00	469.80	0.00	0.00	0.00	0.00	0.00
NH4OH	0.00	0.00	0.00	582.75	582.47	582.47	0.00	0.00	0.00
IPA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Oxide CMP Slurry& chemicals	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ethyl lactate	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Au	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sn	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Co	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
polyimide laminate	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
laminate solvent	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
utility N2	0.00	0.00	0.00	0.00	0.00	0.00	994.29	994.29	994.29
silicon	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H3PO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CuCl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AlCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
OTHERS									
Electricity (KWhr)	1.00	0.00	0.00	0.11	0.00	0.00	4.08	0.00	0.00
UPW	76015.73	0.00	0.00	251419.09	0.00	0.00	0.00	0.00	0.00
Industrial City Water	9087.31	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PCW	10408.75	0.00	0.00	0.00	0.00	0.00	2605714.29	0.00	0.00
Fluoride Wastewater (H2O)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Industrial Wastewater (H2O)	0.00	0.00	86204.64	0.00	0.00	251419.09	0.00	0.00	0.00
Ammonia Waste (NH3)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HF liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	1.22	1.22	0.00	0.00	0.00
SiF4 liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH4OH waste	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2O2 to ammonia waste	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

Appendix D
Oxide Release Layer

Oxide release layer				Bonded Stack						Totals		
UNITS in g/wafer wherever possible	Activation Plasma + Piranha			Oxide Bonding and Annealing			HF release					
	Oxygen plasma followed by Piranha						Acid bath -wet bench					
Film Thickness (nm)							49% by wt HF (concentrated)					
Time (s)	30+120			120+ 10800			2400					
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
OTHER CHEMICALS												
O2	0.13	0.13	0.13	0.00	0.00	0.00	0.00	0.00	0.00	745.79	44.83	33.59
Ar	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
N2	0.00	0.00	0.00	11.25	11.25	11.25	0.00	0.00	0.00	1513.12	1513.12	1513.12
EP-C5003, Cabot	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2O2 (100%)	1377.00	275.40	275.40	0.00	0.00	0.00	50.00	50.00	50.00	4869.50	1564.70	1564.70
CUS silica slurry A	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CUS silica slurry B	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BTA, Aldrich	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sumiwash	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ElectraClean,Ashland	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Semi-Sperse W2000	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Al	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
As	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cu	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pt	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Ti	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
He	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.28	0.28
CuSO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ArH	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
100% HF liquid	0.00	0.00	0.00	0.00	0.00	0.00	287.75	280.00	280.00	288.97	280.00	280.00
H2SO4	23814.00	23814.00	23814.00	0.00	0.00	0.00	0.00	0.00	0.00	71442.00	71442.00	71442.00
HCl	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	469.80	0.00	0.00
NH4OH	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	582.75	582.47	582.47
IPA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Oxide CMP Slurry& chemicals	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ethyl lactate	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	5.79	5.68	5.68
Cr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Au	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sn	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Co	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
polyimide laminate	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
laminate solvent	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
utility N2	2974.86	2974.86	2974.86	0.00	0.00	0.00	0.00	0.00	0.00	7318.90	7318.90	7318.90
silicon	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H3PO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CuCl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AlCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
OTHERS												
Electricity (KWhr)	0.56	0.00	0.00	0.56	0.00	0.00	0.11	0.00	0.00	59.81	0.00	0.00
UPW	75844.39	0.00	0.00	0.00	0.00	0.00	251419.09	0.00	0.00	730604.57	0.00	0.00
Industrial City Water	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	52236.31	0.00	0.00
PCW	0.46	0.00	0.00	240825.00	0.00	0.00	0.00	0.00	0.00	3227273.95	0.00	170325.00
Fluoride Wastewater (H2O)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	43149.00
Industrial Wastewater (H2O)	0.00	0.00	76945.99	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	491515.72
Ammonia Waste (NH3)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HF liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	251419.09	0.00	1.22	251420.31
SiF4 liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	587.50	0.00	0.00	587.50
NH4OH waste	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2O2 to ammonia waste	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

Appendix E
Between-Die Channel

Between-Die Channel	Device Wafer Preparation								
UNITS in g/wafer wherever possible		Lithography		Etch 6 layers stack + silicon 0.5 micron				Strip PR + Piranha	
	Die-saw mask Thick positive resist			Using die-saw mask make die-saw marks			Strip resist is single wafer. Piranha is batch		
Film Thickness (nm)									
Time (s)	120			1800			60+120		
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
GWG									
CF4	0.00	0.00	0.00	3.72	1.86	0.02	0.12	0.34	0.34
CHF3	0.00	0.00	0.00	0.60	0.24	0.18	0.00	0.00	0.00
C2F6	0.00	0.00	0.00	0.00	0.24	0.24	0.00	0.00	0.00
CH4	0.00	0.00	0.00	198.21	0.00	0.00	0.39	0.00	0.00
CO2	0.00	0.00	0.00	0.00	0.24	544.71	0.00	0.15	0.15
NF3	0.00	0.00	0.00	3.75	0.07	0.07	0.00	0.00	0.00
C4F6	0.00	0.00	0.00	0.36	0.03	0.03	0.00	0.00	0.00
SF6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HAZARDOUS									
F2	0.00	0.00	0.00	0.00	0.14	0.00	0.00	0.00	0.00
HF (gas)	0.00	0.00	0.00	0.00	0.06	0.08	0.00	0.02	0.02
SiF4 (gas)	0.00	0.00	0.00	0.00	1.10	1.06	0.00	0.02	0.02
C4F8	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C2F4	0.00	0.00	0.00	0.00	0.54	0.54	0.00	0.00	0.00
COF2	0.00	0.00	0.00	0.00	0.06	0.04	0.00	0.88	0.88
HCl (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiCl4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Bis Tertiary-Butylamino Silane	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AsH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pb	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
WF6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HBr	0.00	0.00	0.00	21.40	1.42	1.42	0.00	0.00	0.00
Br2	0.00	0.00	0.00	0.00	39.20	39.20	0.00	0.00	0.00
CRITERIA									
CO	0.00	0.00	0.00	0.00	0.24	0.24	0.00	0.15	0.15
NO	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.15	0.15
NO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.20	0.20
SO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
N2O	0.00	0.00	0.00	0.00	0.02	0.00	0.00	0.00	0.00
VOC									
DMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TDMAT	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TMS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TEOS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Formaldehyde (CH2O)	2.28	2.24	2.24	0.00	0.00	0.00	0.00	0.00	0.00
m-Cresol	1.45	1.42	1.42	0.00	0.00	0.00	0.00	0.00	0.00
p-Cresol	1.43	1.41	1.41	0.00	0.00	0.00	0.00	0.00	0.00
polypropylene glycol monomethyl ether acet	5.46	5.46	5.46	0.00	0.00	0.00	0.00	0.00	0.00
FLAMMABLE									
SiH4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
DCS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
B2H6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F8	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.01	0.01

Appendix E
Between-Die Channel

Between-Die Channel							Handle Wafer Preparation		
UNITS in g/wafer wherever possible		Al deposition			Bonding layer			Wafer Clean	
	process	Sputtering			TiN/ Cu PVD			RCA Batch process	
Film Thickness (nm)		8000			50/300				
Time (s)	960						120		
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
GWG									
CF4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CHF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C2F6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CH4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NF3	0.00	0.00	0.00	0.18	0.00	0.00	0.00	0.00	0.00
C4F6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SF6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HAZARDOUS									
F2	0.00	0.00	0.00	0.00	0.10	0.10	0.00	0.00	0.00
HF (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiF4 (gas)	0.00	0.00	0.00	0.00	0.03	0.03	0.00	0.00	0.00
C4F8	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C2F4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
COF2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HCl (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiCl4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Bis Tertiary-Butylamino Silane	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AsH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pb	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
WF6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HBr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Br2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CRITERIA									
CO	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NO	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
N2O	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
VOC									
DMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MMA	0.00	0.00	0.00	0.00	0.02	0.02	0.00	0.00	0.00
TDMAT	0.00	0.00	0.00	0.50	0.00	0.00	0.00	0.00	0.00
TMS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TEOS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Formaldehyde (CH2O)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
m-Cresol	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
p-Cresol	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
polypropylene glycol monomethyl ether acet	0.00	0.00	0.00	0.19	0.00	0.00	0.00	0.00	0.00
FLAMMABLE									
SiH4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
DCS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
B2H6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F8	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

Appendix E
Between-Die Channel

Between-Die Channel									
UNITS in g/wafer wherever possible		Oxidation			Lithography			Wet oxide etch	
	Furnace Batch process wet oxidation			Die-saw mask Thick positive resist			Batch process		
Film Thickness (nm)		500						500	
Time (s)	8100			120			120		
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
GWG									
CF4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CHF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C2F6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CH4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SF6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HAZARDOUS									
F2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HF (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiF4 (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F8	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C2F4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
COF2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HCl (gas)	3.52	0.35	0.35	0.00	0.00	0.00	0.00	0.00	0.00
Cl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiCl4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Bis Tertiary-Butylamino Silane	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AsH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pb	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
WF6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HBr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Br2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CRITERIA									
CO	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NO	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NO2	0.00	0.00	90.00	0.00	0.00	0.00	0.00	0.00	0.00
SO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
N2O	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
VOC									
DMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TDMAT	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TMS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TEOS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Formaldehyde (CH2O)	0.00	0.00	0.00	2.28	2.24	2.24	0.00	0.00	0.00
m-Cresol	0.00	0.00	0.00	1.45	1.42	1.42	0.00	0.00	0.00
p-Cresol	0.00	0.00	0.00	1.43	1.41	1.41	0.00	0.00	0.00
polypropylene glycol monomethyl ether acet	0.00	0.00	0.00	5.46	5.46	5.46	0.00	0.00	0.00
FLAMMABLE									
SiH4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2	8.35	3.06	0.00	0.00	0.00	0.00	0.00	0.00	0.00
DCS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
B2H6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F8	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

Appendix E
Between-Die Channel

Between-Die Channel									
UNITS in g/wafer wherever possible	Etch Silicon			Strip PR + Piranha			Bonding Layer		
	Bosch process						TiN/Cu PVD		
Film Thickness (nm)	50000						50/300		
Time (s)	1500+300			60+120					
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
GWG									
CF4	0.00	0.93	0.01	0.12	0.34	0.34	0.00	0.00	0.00
CHF3	0.00	0.12	0.09	0.00	0.00	0.00	0.00	0.00	0.00
C2F6	0.00	0.12	0.12	0.00	0.00	0.00	0.00	0.00	0.00
CH4	99.11	0.00	0.00	0.39	0.00	0.00	0.00	0.00	0.00
CO2	0.00	0.12	272.36	0.00	0.15	0.15	0.00	0.00	0.00
NF3	0.00	0.00	0.00	0.00	0.00	0.00	0.18	0.00	0.00
C4F6	0.00	0.01	0.01	0.00	0.00	0.00	0.00	0.00	0.00
SF6	34.01	3.40	0.34	0.00	0.00	0.00	0.00	0.00	0.00
HAZARDOUS									
F2	0.00	0.30	0.00	0.00	0.00	0.00	0.00	0.10	0.10
HF (gas)	0.00	0.30	0.00	0.00	0.02	0.02	0.00	0.00	0.00
SiF4 (gas)	0.00	0.12	0.10	0.00	0.02	0.02	0.00	0.03	0.03
C4F8	8.95	1.79	0.36	0.00	0.00	0.00	0.00	0.00	0.00
C2F4	0.00	0.27	0.27	0.00	0.00	0.00	0.00	0.00	0.00
COF2	0.00	0.03	0.02	0.00	0.88	0.88	0.00	0.00	0.00
HCl (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiCl4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Bis Tertiary-Butylamino Silane	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AsH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pb	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
WF6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HBr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Br2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CRITERIA									
CO	0.00	0.12	0.12	0.00	0.15	0.15	0.00	0.00	0.00
NO	0.00	0.00	0.00	0.00	0.15	0.15	0.00	0.00	0.00
NO2	0.00	0.00	0.00	0.00	0.20	0.20	0.00	0.00	0.00
SO2	0.00	0.00	16.43	0.00	0.00	0.00	0.00	0.00	0.00
N2O	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
VOC									
DMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.02	0.02
TDMAT	0.00	0.00	0.00	0.00	0.00	0.00	0.50	0.00	0.00
TMS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TEOS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Formaldehyde (CH2O)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
m-Cresol	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
p-Cresol	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
polypropylene glycol monomethyl ether acet	0.00	0.00	0.00	0.00	0.00	0.00	0.19	0.00	0.00
FLAMMABLE									
SiH4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
DCS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
B2H6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F8	0.00	0.00	0.00	0.00	0.01	0.01	0.00	0.00	0.00

Appendix E
Between-Die Channel

Between-Die Channel	Bonded Stack						Totals		
UNITS in g/wafer wherever possible		Copper Bonding			HCL release				
		(modeled on coper annealing)			Acid bath -wet bench				
Film Thickness (nm)				(36% by wt in 1:1 solution with H2O)					
Time (s)	10800			Not determined					
				in	process out	post-POU	in	process out	post-POU
GWG									
CF4	0.00	0.00	0.00	0.00	0.00	0.00	3.96	3.47	0.71
CHF3	0.00	0.00	0.00	0.00	0.00	0.00	0.60	0.36	0.27
C2F6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.36	0.36
CH4	0.00	0.00	0.00	0.00	0.00	0.00	298.10	0.00	0.00
CO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.66	817.37
NF3	0.00	0.00	0.00	0.00	0.00	0.00	4.10	0.07	0.07
C4F6	0.00	0.00	0.00	0.00	0.00	0.00	0.36	0.04	0.04
SF6	0.00	0.00	0.00	0.00	0.00	0.00	34.01	3.40	0.34
HAZARDOUS									
F2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.64	0.20
HF (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.40	0.13
SiF4 (gas)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	1.33	1.26
C4F8	0.00	0.00	0.00	0.00	0.00	0.00	8.95	1.79	0.36
C2F4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.81	0.81
COF2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	1.85	1.82
HCl (gas)	0.00	0.00	0.00	0.00	0.00	0.00	3.52	0.35	0.35
Cl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiCl4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Bis Tertiary-Butylamino Silane	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AsH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pb	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
WF6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HBr	0.00	0.00	0.00	0.00	0.00	0.00	21.40	1.42	1.42
Br2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	39.20	39.20
CRITERIA									
CO	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.66	0.66
NO	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.30	0.30
NO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.40	90.40
SO2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	16.43
N2O	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.02	0.00
	0.00	0.00	0.00						
VOC	0.00	0.00	0.00						
DMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MMA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.05	0.05
TDMAT	0.00	0.00	0.00	0.00	0.00	0.00	1.01	0.00	0.00
TMS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
TEOS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Formaldehyde (CH2O)	0.00	0.00	0.00	0.00	0.00	0.00	4.57	4.48	4.48
m-Cresol	0.00	0.00	0.00	0.00	0.00	0.00	2.90	2.84	2.84
p-Cresol	0.00	0.00	0.00	0.00	0.00	0.00	2.87	2.81	2.81
polypropylene glycol monomethyl ether acet	0.00	0.00	0.00	0.00	0.00	0.00	11.29	10.91	10.91
	0.00	0.00	0.00						
FLAMMABLE									
SiH4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2	2.90	2.90	2.90	0.00	0.00	0.00	11.25	5.96	2.90
DCS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
B2H6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
C4F8	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.02	0.02

Appendix E
Between-Die Channel

Between-Die Channel	Device Wafer Preparation								
UNITS in g/wafer wherever possible		Lithography		Etch 6 layers stack + silicon 0.5 micron				Strip PR + Piranha	
	Die-saw mask Thick positive resist			Using die-saw mask make die-saw marks			Strip resist is single wafer. Piranha is batch		
Film Thickness (nm)									
Time (s)	120			1800			60+120		
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
OTHER CHEMICALS									
O2	0.00	0.00	0.00	643.65	0.27	0.00	32.00	12.00	12.00
Ar	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
N2	0.00	0.00	0.00	1.87	1.87	1.87	0.00	0.00	0.00
EP-C5003, Cabot	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2O2 (100%)	0.00	0.00	0.00	0.00	0.00	0.00	1377.00	275.40	275.40
CUS silica slurry A	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CUS silica slurry B	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BTA, Aldrich	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sumiwash	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ElectraClean,Ashland	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Semi-Sperse W2000	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Al	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
As	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cu	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pt	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Ti	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
He	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CuSO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ArH	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
100% HF liquid	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2SO4	0.00	0.00	0.00	0.00	0.00	0.00	23814.00	23814.00	23814.00
HCl	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH4OH	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
IPA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Oxide CMP Slurry& chemicals	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ethyl lactate	5.79	5.68	5.68	0.00	0.00	0.00	0.00	0.00	0.00
Cr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Au	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sn	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Co	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
polyimide laminate	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
laminate solvent	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
utility N2	125.00	125.00	125.00	1170.26	1170.26	1170.26	0.00	0.00	0.00
silicon	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H3PO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CuCl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AlCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
OTHERS									
Electricity (KWhr)	2.82	0.00	0.00	42.48	0.00	0.00	1.00	0.00	0.00
UPW	61.88	0.00	0.00	7366.26	0.00	0.00	76015.73	0.00	0.00
Industrial City Water	0.00	0.00	0.00	50515.26	0.00	0.00	9087.31	0.00	0.00
PCW	200000.00	0.00	0.00	274879.78	0.00	274879.78	10408.75	0.00	0.00
Fluoride Wastewater (H2O)	0.00	0.00	0.00	0.00	0.00	43149.00	0.00	0.00	0.00
Industrial Wastewater (H2O)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	86204.64
Ammonia Waste (NH3)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HF liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiF4 liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH4OH waste	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AlCl3 containing water	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

Appendix E
Between-Die Channel

Between-Die Channel							Handle Wafer Preparation		
UNITS in g/wafer wherever possible		Al deposition			Bonding layer			Wafer Clean	
	rocess	Sputtering			TiN/ Cu PVD			RCA Batch process	
Film Thickness (nm)		8000			50/300				
Time (s)	960						120		
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
OTHER CHEMICALS									
O2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Ar	40.80	40.80	40.80	0.33	0.33	0.33	0.00	0.00	0.00
N2	0.00	0.00	0.00	178.92	161.70	161.70	0.00	0.00	0.00
EP-C5003, Cabot	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2O2 (100%)	0.00	0.00	0.00	0.00	0.00	0.00	688.50	688.50	688.50
CUS silica slurry A	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CUS silica slurry B	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BTA, Aldrich	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sumiwash	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ElectraClean,Ashland	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Semi-Sperse W2000	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Al	2.12	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
As	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cu	0.00	0.00	0.00	0.35	0.17	0.17	0.00	0.00	0.00
Pt	0.00	0.00	0.00	0.37	0.37	0.37	0.00	0.00	0.00
Ti	0.00	0.00	0.00	0.02	0.00	0.00	0.00	0.00	0.00
He	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH3	0.00	0.00	0.00	0.00	0.03	0.03	0.00	0.28	0.28
CuSO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ArH	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
100% HF liquid	0.00	0.00	0.00	0.00	0.00	0.00	1.22	0.00	0.00
H2SO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HCl	0.00	0.00	0.00	0.00	0.00	0.00	469.80	0.00	0.00
NH4OH	0.00	0.00	0.00	0.00	0.00	0.00	582.75	582.47	582.47
IPA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Oxide CMP Slurry& chemicals	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ethyl lactate	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Au	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sn	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Co	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
polyimide laminate	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
laminate solvent	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
utility N2	100.04	100.04	100.04	132.80	132.80	132.80	0.00	0.00	0.00
silicon	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H3PO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CuCl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AlCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
OTHERS									
Electricity (KWhr)	137.35	0.00	0.00	0.76	0.00	0.00	0.11	0.00	0.00
UPW	0.00	0.00	0.00	0.00	0.00	0.00	251419.09	0.00	0.00
Industrial City Water	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PCW	4825396.83	0.00	0.00	98713.29	0.00	0.00	0.00	0.00	0.00
Fluoride Wastewater (H2O)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Industrial Wastewater (H2O)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	251419.09
Ammonia Waste (NH3)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HF liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	1.22	1.22
SiF4 liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH4OH waste	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AlCl3 containing water	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

Appendix E
Between-Die Channel

Between-Die Channel									
UNITS in g/wafer wherever possible		Oxidation			Lithography			Wet oxide etch	
	Furnace Batch process wet oxidation			Die-saw mask Thick positive resist			Batch process		
Film Thickness (nm)		500						500	
Time (s)	8100			120			120		
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
OTHER CHEMICALS									
O2	106.00	26.35	9.49	0.00	0.00	0.00	0.00	0.00	0.00
Ar	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
N2	2250.00	2250.00	2250.00	0.00	0.00	0.00	0.00	0.00	0.00
EP-C5003, Cabot	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2O2 (100%)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CUS silica slurry A	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CUS silica slurry B	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BTA, Aldrich	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sumiwash	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ElectraClean,Ashland	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Semi-Sperse W2000	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Al	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
As	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cu	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pt	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Ti	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
He	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CuSO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ArH	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
100% HF liquid	0.00	0.00	0.00	0.00	0.00	0.00	1.48	0.00	0.00
H2SO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HCl	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH4OH	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
IPA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Oxide CMP Slurry& chemicals	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ethyl lactate	0.00	0.00	0.00	5.79	5.68	5.68	0.00	0.00	0.00
Cr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Au	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sn	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Co	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
polyimide laminate	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
laminate solvent	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
utility N2	1491.43	1491.43	1491.43	125.00	125.00	125.00	0.00	0.00	0.00
silicon	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H3PO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CuCl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AlCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
OTHERS									
Electricity (KWhr)	6.13	0.00	0.00	2.82	0.00	0.00	0.04	0.00	0.00
UPW	0.00	0.00	0.00	61.88	0.00	0.00	748.50	0.00	0.00
Industrial City Water	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PCW	3908571.43	0.00	0.00	200000.00	0.00	0.00	0.00	0.00	0.00
Fluoride Wastewater (H2O)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	748.50
Industrial Wastewater (H2O)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Ammonia Waste (NH3)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HF liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiF4 liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH4OH waste	0.00	0.00	0.00	0.00	0.00	0.00	0.00	1.34	1.34
AlCl3 containing water	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.18	0.18

Appendix E
Between-Die Channel

Between-Die Channel									
UNITS in g/wafer wherever possible		Etch Silicon			Strip PR + Piranha			Bonding Layer	
		Bosch process						TiN/Cu PVD	
Film Thickness (nm)		50000						50/300	
Time (s)	1500+300			60+120					
	in	process out	post-POU	in	process out	post-POU	in	process out	post-POU
OTHER CHEMICALS									
O2	321.43	0.00	0.00	32.00	12.00	12.00	0.00	0.00	0.00
Ar	0.00	0.00	0.00	0.00	0.00	0.00	0.33	0.33	0.33
N2	0.93	0.93	0.93	0.00	0.00	0.00	178.92	161.70	161.70
EP-C5003, Cabot	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2O2 (100%)	0.00	0.00	0.00	1377.00	275.40	275.40	0.00	0.00	0.00
CUS silica slurry A	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CUS silica slurry B	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BTA, Aldrich	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sumiwash	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ElectraClean,Ashland	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Semi-Sperse W2000	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Al	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
As	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cu	0.00	0.00	0.00	0.00	0.00	0.00	0.35	0.17	0.17
Pt	0.00	0.00	0.00	0.00	0.00	0.00	0.37	0.37	0.37
Ti	0.00	0.00	0.00	0.00	0.00	0.00	0.02	0.00	0.00
He	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.03	0.03
CuSO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ArH	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
100% HF liquid	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2SO4	0.00	0.00	0.00	23814.00	23814.00	23814.00	0.00	0.00	0.00
HCl	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH4OH	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
IPA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Oxide CMP Slurry& chemicals	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ethyl lactate	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Au	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sn	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Co	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
polyimide laminate	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
laminate solvent	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
utility N2	289.00	283.00	283.00	0.00	0.00	0.00	132.80	132.80	132.80
silicon	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H3PO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CuCl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AlCl3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
OTHERS									
Electricity (KWhr)	30.00	0.00	0.00	1.00	0.00	0.00	0.76	0.00	0.00
UPW	0.00	0.00	0.00	76015.73	0.00	0.00	0.00	0.00	0.00
Industrial City Water	21574.50	0.00	0.00	9087.31	0.00	0.00	0.00	0.00	0.00
PCW	85162.50	0.00	85162.50	10408.75	0.00	0.00	98713.29	0.00	0.00
Fluoride Wastewater (H2O)	0.00	0.00	21574.50	0.00	0.00	0.00	0.00	0.00	0.00
Industrial Wastewater (H2O)	0.00	0.00	0.00	0.00	0.00	86204.64	0.00	0.00	0.00
Ammonia Waste (NH3)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HF liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
SiF4 liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH4OH waste	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AlCl3 containing water	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

Appendix E
Between-Die Channel

Between-Die Channel	Bonded Stack						Totals		
UNITS in g/wafer wherever possible		Copper Bonding			HCL release				
		(modeled on coper annealing)			Acid bath -wet bench				
Film Thickness (nm)				(36% by wt in 1:1 solution with H2O)					
Time (s)	10800			Not determined					
				in	process out	post-POU	in	process out	post-POU
OTHER CHEMICALS									
O2	0.00	0.00	0.00	0.00	0.00	0.00	1135.08	50.62	33.49
Ar	0.00	0.00	0.00	0.00	0.00	0.00	41.45	41.45	41.45
N2	281.25	281.25	281.25	0.00	0.00	0.00	2891.89	2857.45	2857.45
EP-C5003, Cabot	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H2O2 (100%)	0.00	0.00	0.00	50.00	50.00	50.00	3492.50	1289.30	1289.30
CUS silica slurry A	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CUS silica slurry B	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BTA, Aldrich	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sumiwash	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ElectraClean,Ashland	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Semi-Sperse W2000	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Al	0.00	0.00	0.00	0.00	0.00	0.00	2.12	0.00	0.00
As	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Cu	0.00	0.00	0.00	0.00	0.00	0.00	0.70	0.35	0.35
Pt	0.00	0.00	0.00	0.00	0.00	0.00	0.75	0.75	0.75
Ti	0.00	0.00	0.00	0.00	0.00	0.00	0.03	0.00	0.00
He	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.33	0.33
CuSO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ArH	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
100% HF liquid	0.00	0.00	0.00	0.00	0.00	0.00	1.22	0.00	0.00
H2SO4	0.00	0.00	0.00	0.00	0.00	0.00	47628.00	47628.00	47628.00
HCl	0.00	0.00	0.00	469.80	440.00	440.00	939.60	440.00	440.00
NH4OH	0.00	0.00	0.00	0.00	0.00	0.00	582.75	582.47	582.47
IPA	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Oxide CMP Slurry& chemicals	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
BF3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
ethyl lactate	0.00	0.00	0.00	0.00	0.00	0.00	11.59	11.36	11.36
Cr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Au	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Sn	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Co	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
polyimide laminate	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
laminate solvent	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
utility N2	0.00	0.00	0.00	0.00	0.00	0.00	3566.32	3560.32	3560.32
silicon	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
H3PO4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
CuCl2	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AlCl3	0.00	0.00	0.00	0.00	63.00	63.00	0.00	63.00	63.00
OTHERS									
Electricity (KWhr)	13.97	0.00	0.00	0.11	0.00	0.00	239.31	0.00	0.00
UPW	0.00	0.00	0.00	251419.09	0.00	0.00	662359.64	0.00	0.00
Industrial City Water	0.00	0.00	0.00	0.00	0.00	0.00	90264.38	0.00	0.00
PCW	1020625.00	0.00	0.00	0.00	0.00	0.00	10732879.63	0.00	360042.28
Fluoride Wastewater (H2O)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	64723.50
Industrial Wastewater (H2O)	0.00	0.00	0.00	0.00	0.00	241419.09	0.00	0.00	665247.46
Ammonia Waste (NH3)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
HF liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	1.22	1.22
SiF4 liquid waste to Fluoride treatment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
NH4OH waste	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
AlCl3 containing water	0.00	0.00	0.00	0.00	0.00	1000.00	0.00	0.00	1000.00