# The Connection Machine RAM Chip

## by

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## Abstract

This document describes the three transistor NMOS dynamic ram circuit used in the connection machine. It was designed and implemented by Brewster Kahle, with the assistance of Jim Cherry, Danny Hillis and Tom Knight. Prototypes were fabricated through the APRA MOSIS facility, using both four and three micro design rules. Jim Li and I tested both runs this fall. They work. This document describes how.

# The Connection Machine RAM Chip

The dynamic RAM for the Connection Machine contains an array of memory cells forming 16 registers, 24 bits long. They are arranged in 16 horizontal rows and 24 vertical columns. Each row of cells has associated with it, circuitry consisting of a precharge stage, a decoding stage, and driver stage, used for refreshing the dynamic RAM. The circuit diagram of these stages is shown in Figure 1. The whole block of 16 x 24 cells also has associated with it one common driver circuit for controlling the ALU's option of writing new data back into the RAM. Figures 2-4 illustrate this section with a circuit diagram, a functional diagram and a topological layout.

The basic RAM cell consists of three transistors with READ and Write control lines gating two of those transistors. A four phase clock is used to produce the read and write cycles (Figure 7). PC (precharge) is the OR of PC1 and PC2. As Figure 1 shows, when phi-1 goes high, PC precharges the bit line to a "one". This way, the bit line need not be pulled up when writing a one is desired, but only pulled down when a zero is written. The line is always precharged before a read or a write operation.

During a WRITE, phi-4, charge is stored on the transistor gated by the WRITE line. During the READ cycle, the transistor gated by READ is turned on, creating a possible path to ground, depending on the state of the storage transistor gated by the WRITE line. If a one had been written, the third transistor, gated by the source of WRITE's storage transistor will have been turned on and during a READ, a path to ground will have been created. This forces the bit line low. Therefore, the "one" written onto the bit line during the WRITE cycle is transformed into a zero during the READ cycle. This inverted bit is reinverted in the next stage, the driver stage.

The driver stage is needed to refresh the bit line of the dynamic RAM because bit storage is accomplished by keeping a charge on a capacitor and this charge tends to leak off after a period of time. The drivers refresh the bit line either by rewriting the inversion of the bit presently on the line, or else if selected for ALU operation, by writing a new bit onto the line.

If the bit line is not selected for ALU operation, refreshing is accomplished similarly to the initial writing of a bit into the cell. Assume a zero is on the bit line. On phi-2, when READ goes high, the READ transistor passes a zero which gates another transistor, turning it off. During phi-3, REFRESH and WRITE goes high turning on a transistor connected in series to the one with a zero on its gate. Thus a path to ground from the bit line is not formed and the bit line is pulled high. It's pulled high during phi-4's WRITE because the line had just been precharged during phi-3. Consequently, the zero on the bit line has been reinverted back to a one, the original datum.

If the bit line has been selected for ALU operation, that is, if the pass transistor for that line in the decoder has been turned on, the data on that line will be sent to the ALU for processing. However, even if the line has been selected, this option can be controlled by the control signal NOP-bar. If NOP-bar is low, then no operation is performed by the ALU and the bit is just refreshed by the RAM drivers. If NOP-bar is high then the bit is sent to the ALU. Figure 3 illustrates the ALU driver circuit. If NOP-bar is low, then on phi-2, READ goes high and the bit on the selected line is inverted and sent to the superbuffers and the AOUT pad. AOUT is the same sense as the bit actually stored in the cell. Since NOP-bar is low, the transistor gated by NOP-bar and an inverter is turned on but the transistor gated just by NOP-bar is turned off. Therefore, the bit does not get sent to the ALU, but gets rewritten onto the bit line through the circuitry on the upper loop of Figure 3. During phi-3, PC2 is high, opening possible paths either to ground or VDD during phi-4, depending on the sense of the bit. If AOUT is one, a path to ground is made and a zero is written onto the bit line. Since entering

this stage, this bit has been inverted twice and so is written back the same way it was read out.

If NOP-bar is high, the transistor gated by NOP-bar and an inverter is turned off, not allowing the bit passed by the READ transistor to pass through. However, the transistor gated only by NOP-bar is turned on and whatever bit is input there from the ALU will be sent around the upper loop circuitry of Figure 3 and written back into the RAM cell. Timing diagrams for various cases of NOP-bar and ALU-IN are shown in Figures 5 and 6. BOUT is an output pad connected directly to the bit line and hence reads out the inversion of the bit written in. AOUT, as mentioned earlier, is of the same sense as the bit stored in the cell.
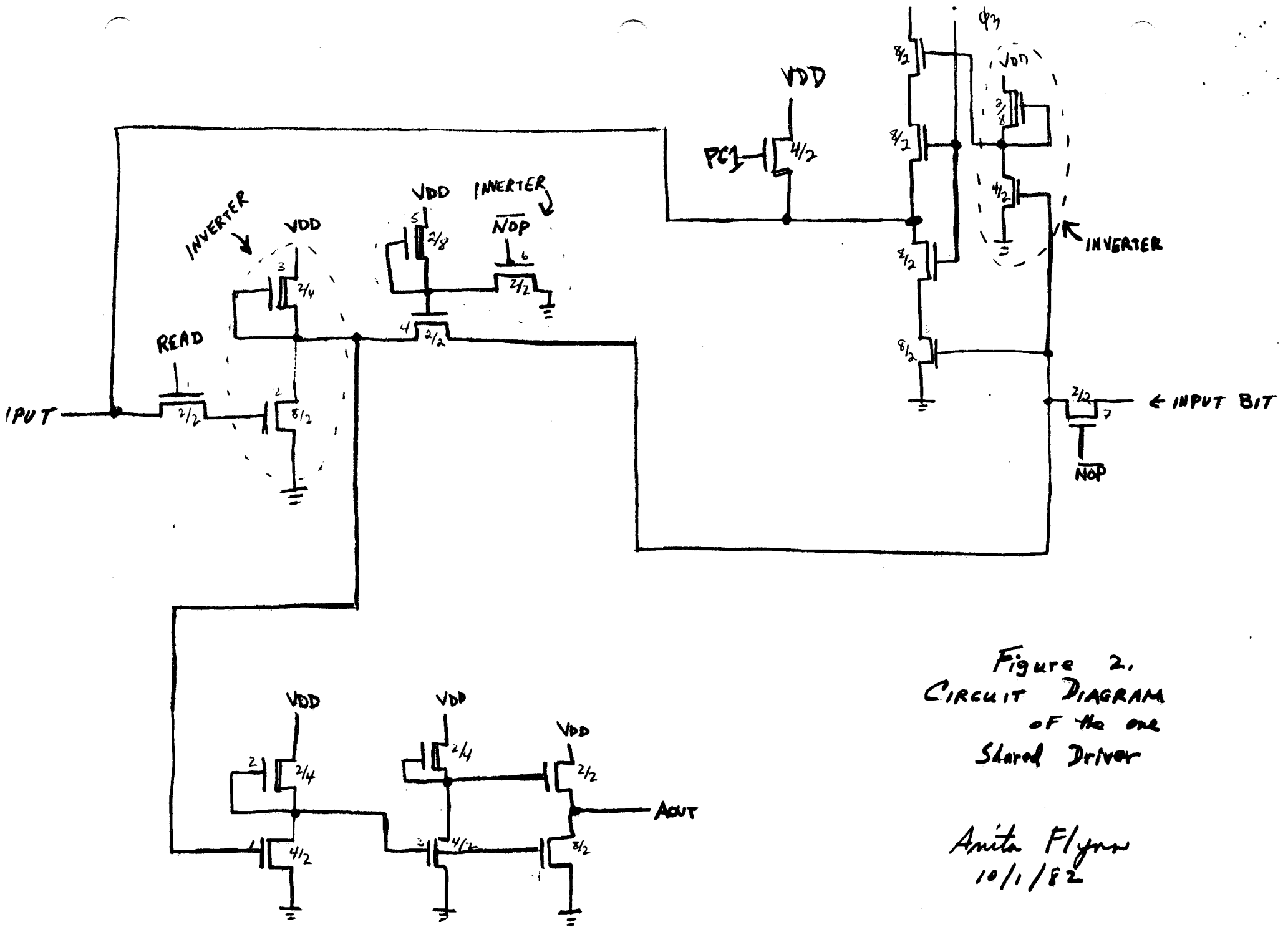
Figure 2.
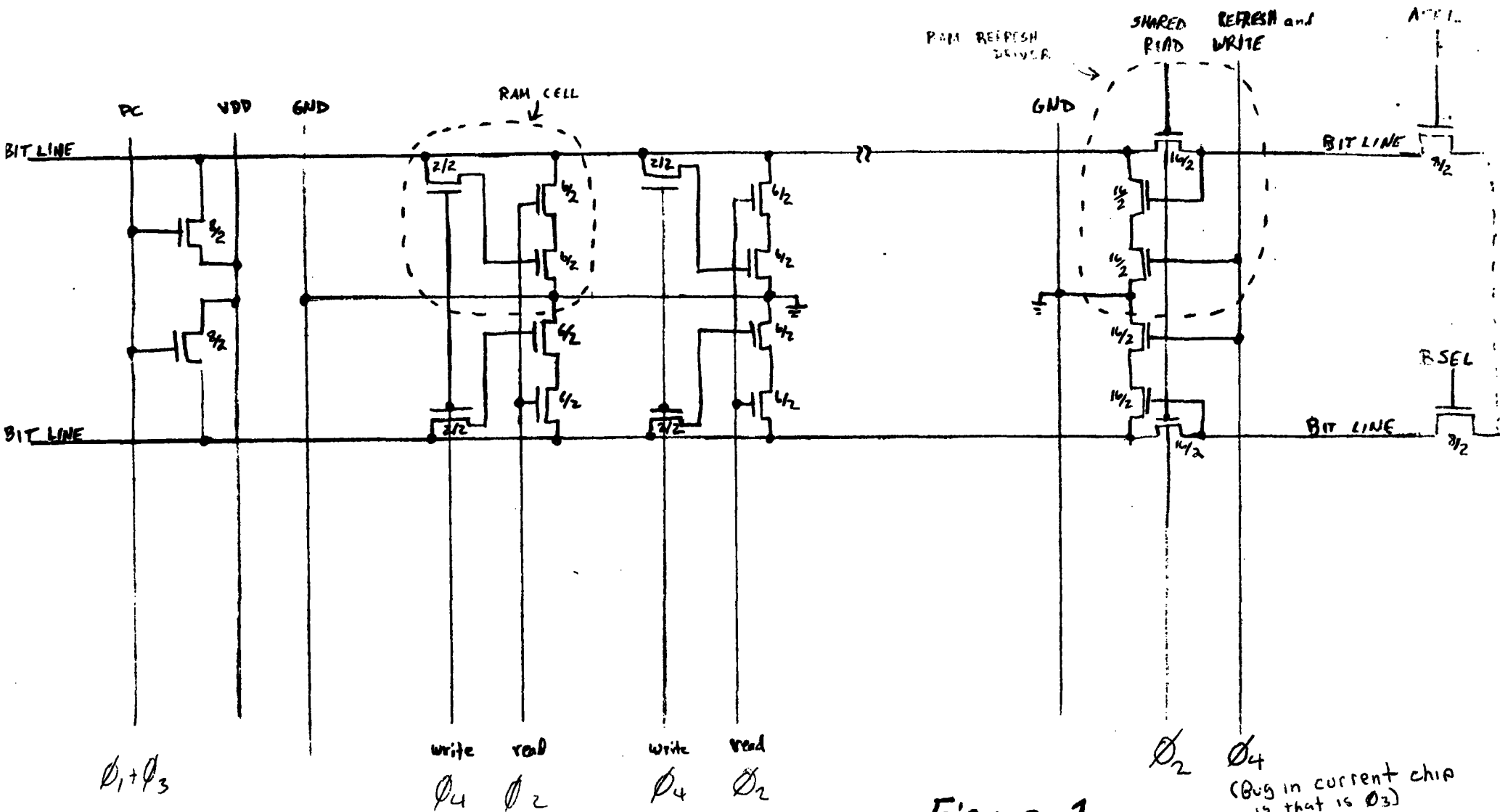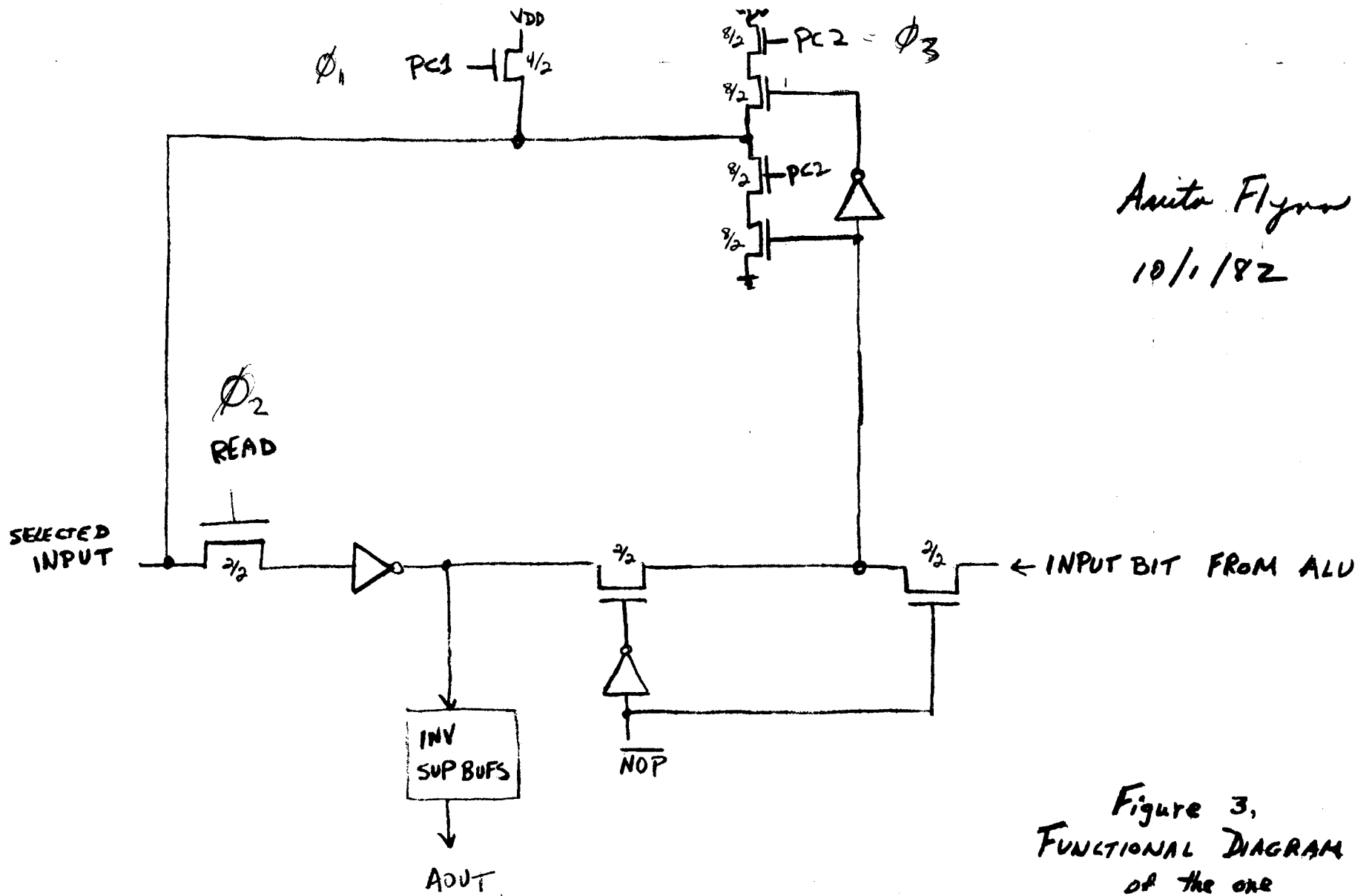Circuit Diagram
of the one
Shared Driver

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Figure 1.
Circuit Diagram
of
Recharge Stage
Ram Cells
Ram Drivers
Decoder

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$\phi_1$

PC1

VDD

4/2

8/2 — PC2 = $\phi_3$

8/2

8/2 — PC2

8/2

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$\phi_2$

READ

2/2

SELECTED INPUT

INV SUP BUFS

2/2

NOP

2/2

← INPUT BIT FROM ALU

AOUT

Figure 3,
FUNCTIONAL DIAGRAM
of the one
Shared Driver

READ   GND   VDD   PC1   PC2   $\overline{NOP}$   GND
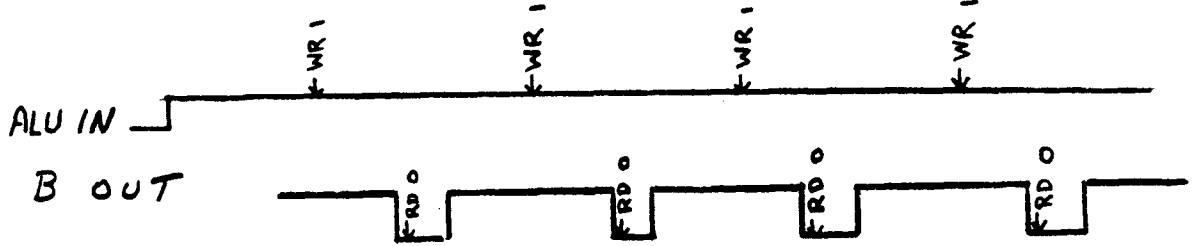
INVERTER

RAM INPUT

< ALU

OUT

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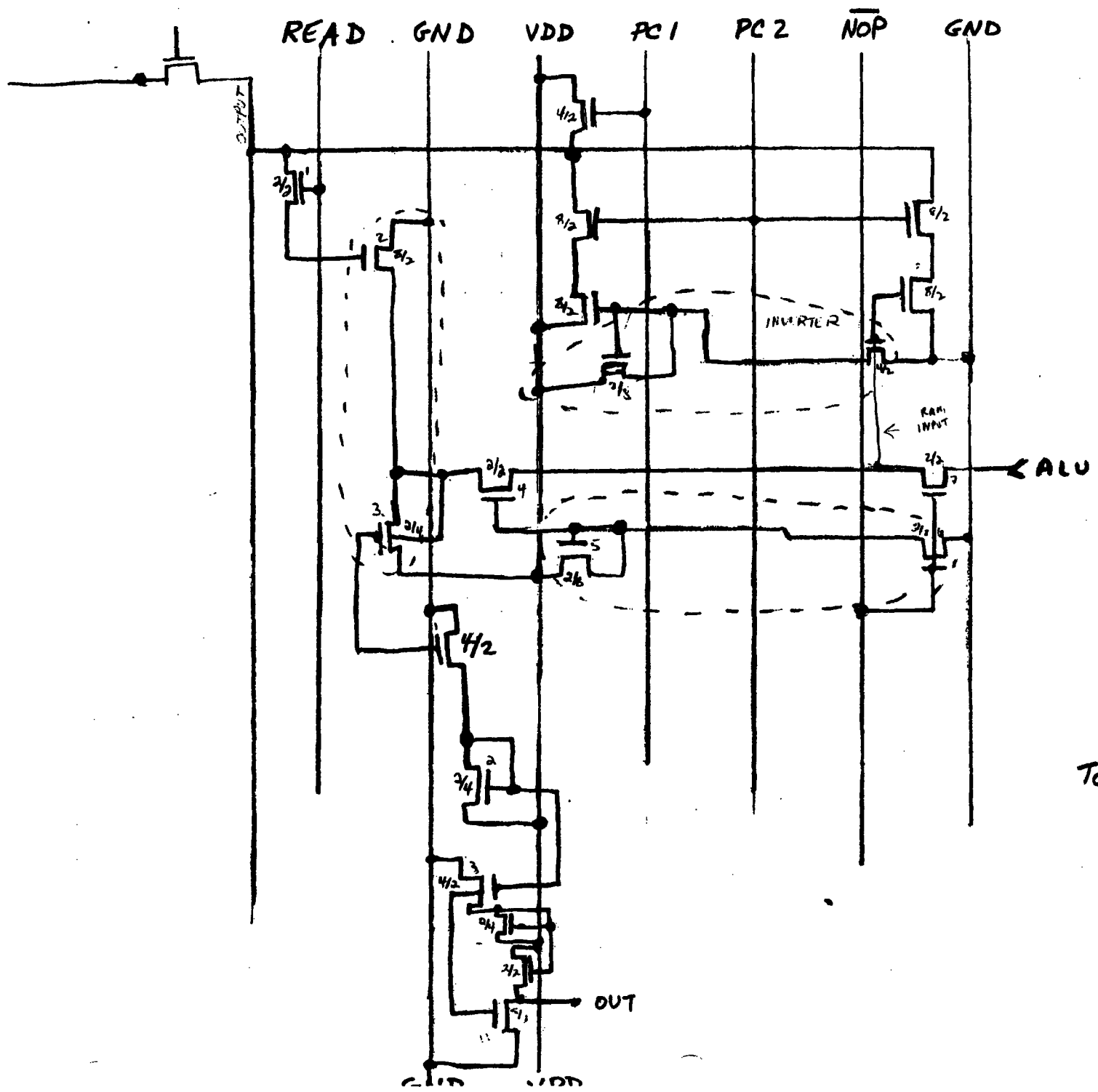
Figure 4.
Topological Layout
on the chip
of the one
Shared Driver

# FIGURE 5. TIMING DIAGRAMS

CASE 1.

NOP̄

Φ2 READ

Φ3

Φ4 WRITE

ALU IN

B OUT

A OUT

CASE 2.

ALU IN

B OUT

CASE 3.

NOP̄

ALU IN

B OUT

(same as above
because NOP̄ low)

CASE 4.

NOP̄

NOP̄

B OUT

A OUT
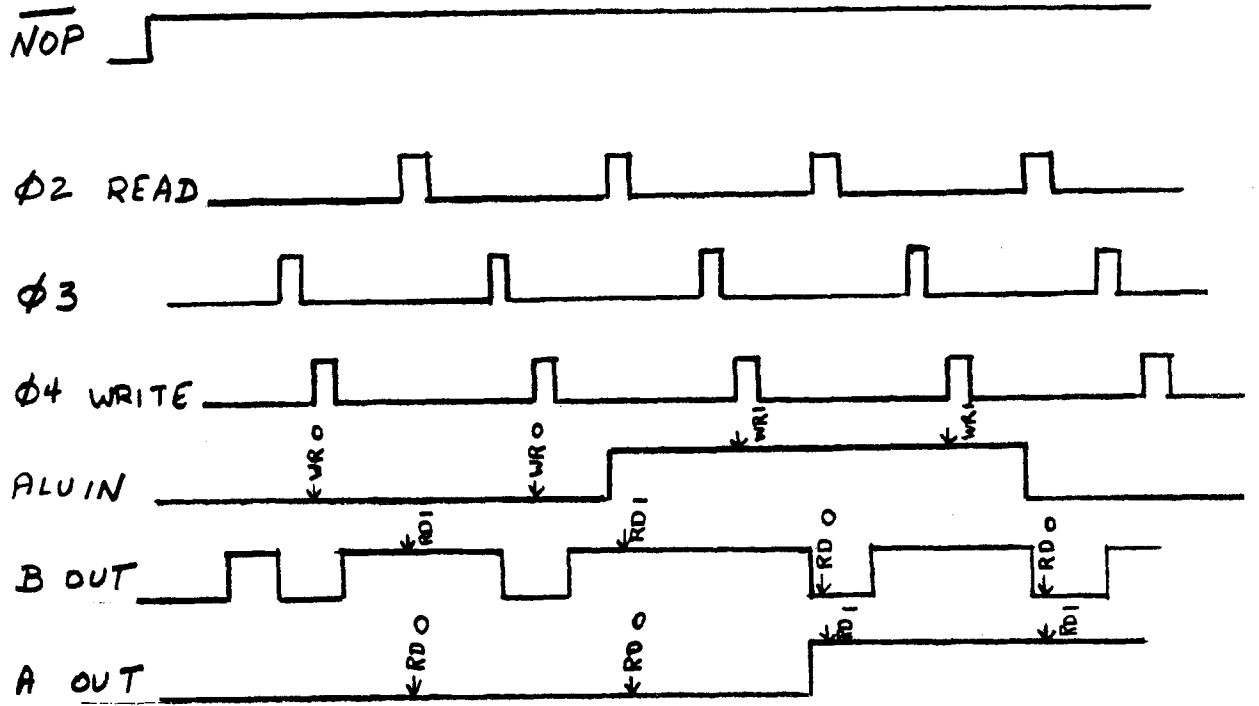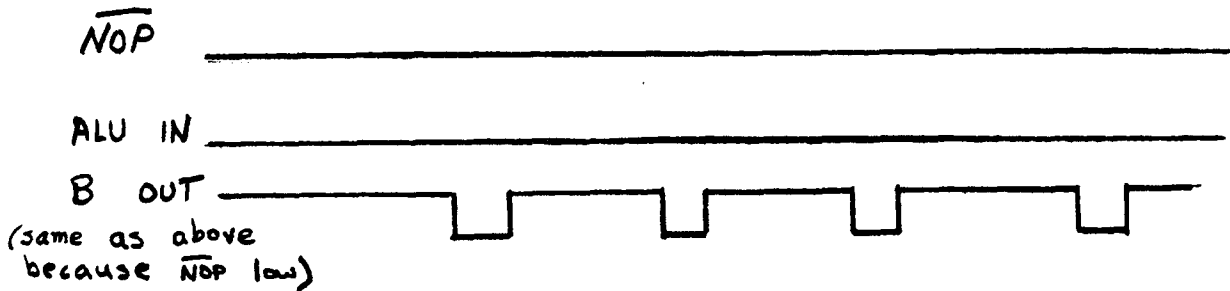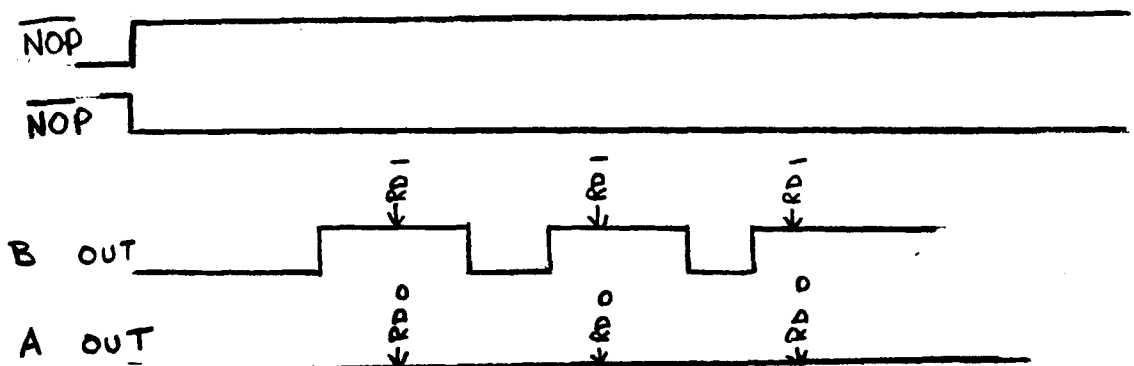
# FIGURE 6. TIMING DIAGRAMS



CASE 5.

φ2 READ

φ3

φ4 WRITE

ALU IN

NOP

A OUT

B OUT

CASE 6.

NOP

ALU IN

A OUT ... DOESN'T CHANGE FROM ABOVE

B OUT ... "                                    "

CASE 7.

NOP

ALU IN

BOUT
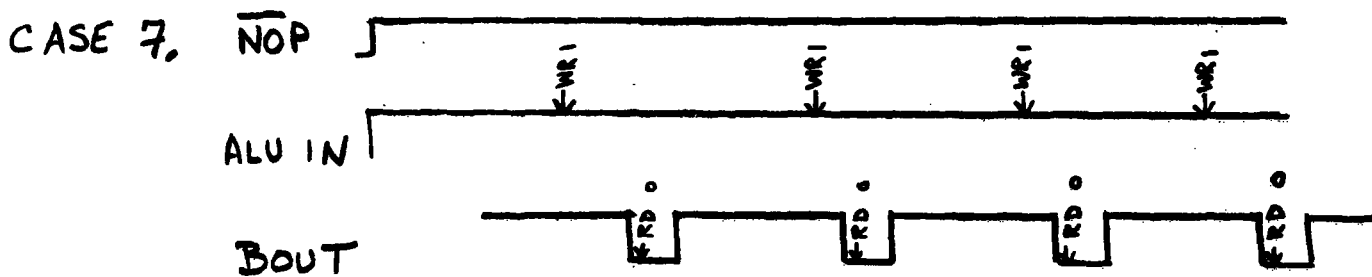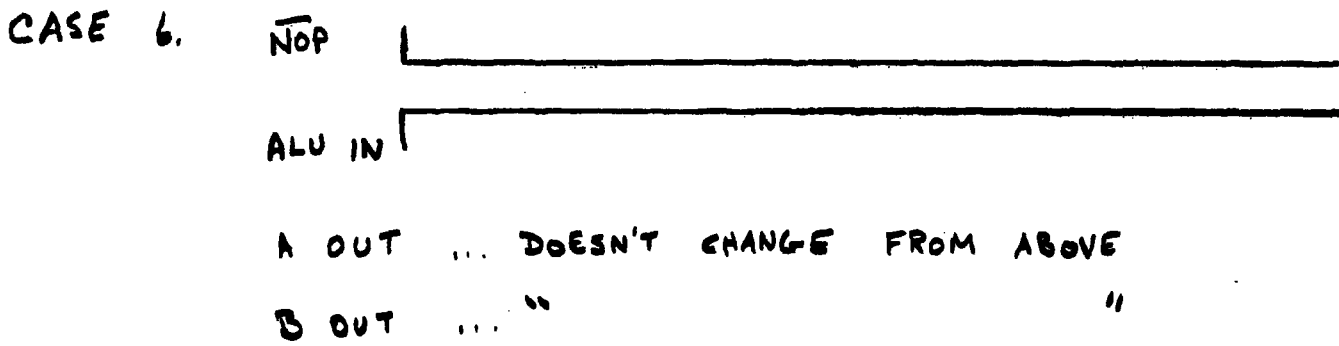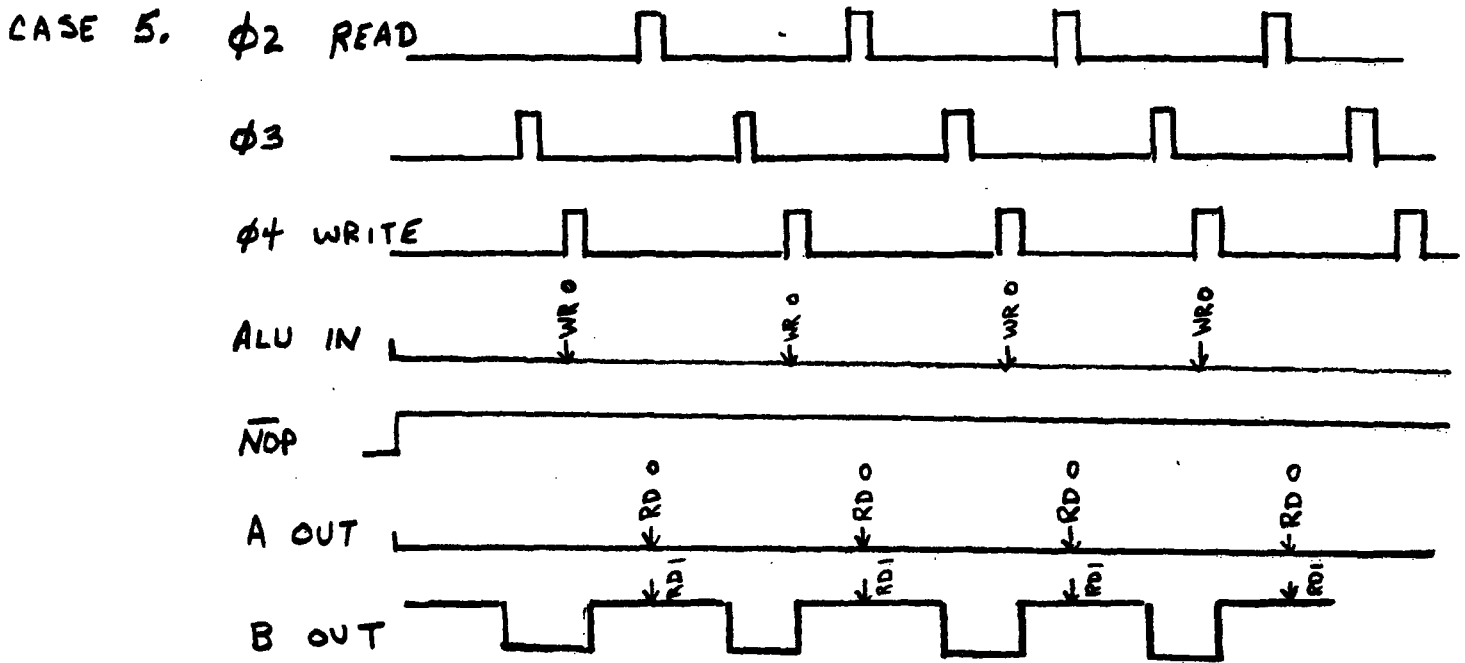
# TIMING DIAGRAMS
## FIGURE 7.



Shared - READ *

PC1 $\phi_1$

Column - READ $\phi_2$

PC2/(REF·WR) $\phi_3$

WRITE $\phi_4$

PC $\phi_1 + \phi_3$
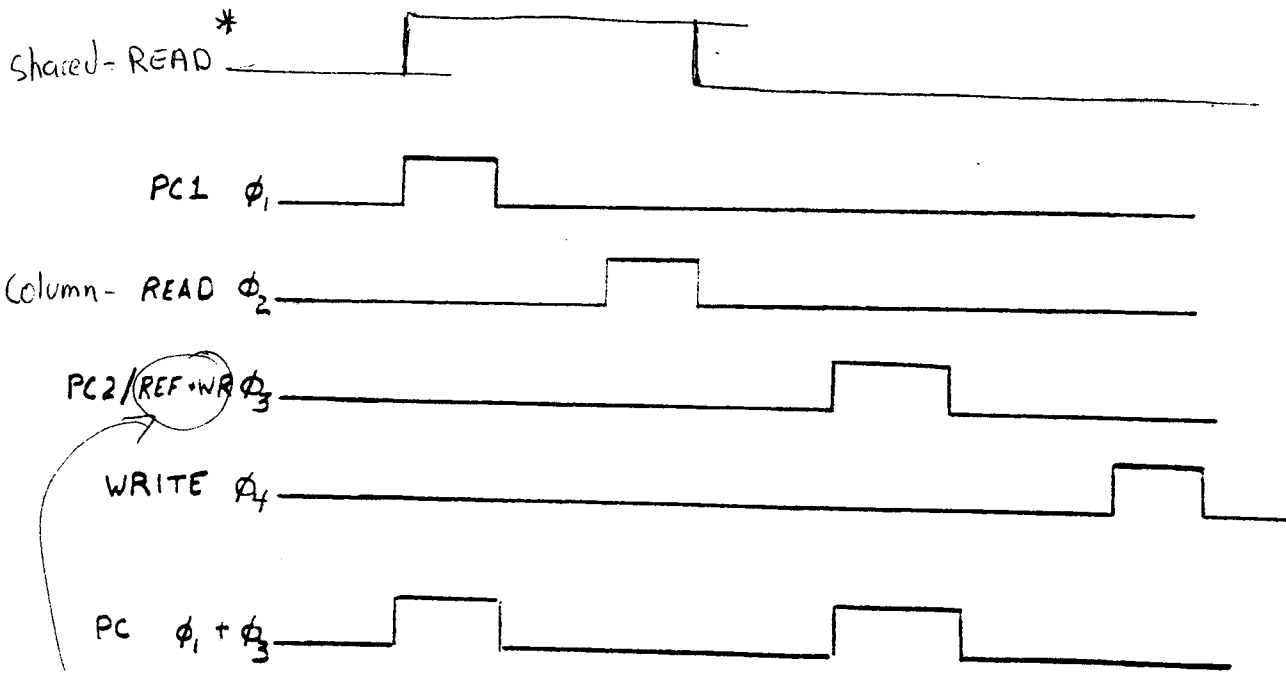
Bug on current
chip. Should really be on $\phi_4$

\* to prevent charge sharing bugs on latching read data
the latches should really be open during precharge.
This is not really very important if the capacitance
ratios are high eneough. — Danny