# Implementation of a Circuit for Communication Using Solitons

by

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Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degrees of

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## Abstract

The Toda lattice is a solvable nonlinear system which supports soliton solutions. Recently, soliton systems have been proposed for a variety of communication and signal processing applications. In this thesis, a hardware implementation of a soliton-based communication circuit is presented. The circuit comprises soliton signal generation and modulation hardware, where multiple solitons are generated and can be amplitude or phase modulated. The Toda lattice circuit is used as a nonlinear multiplexor, where multiple solitons of different wavenumbers are naturally combined by the nonlinear soliton dynamics. Demultiplexing is similarly performed by the soliton dynamics. Simple hardware is then used to demodulate the separated solitons.

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# Acknowledgments

I would like to thank Andrew C. Singer, because without his considerable talents, this thesis would never have been finished in time, nor be quite as good. I must also thank my parents and my brother and sister for all the love and support they gave me during my years at MIT.

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# Chapter 1

# Introduction

Traditional systems for signal processing applications rely heavily on the use of linear time-invariant (LTI) models and a Fourier representation of signals. Recently, a class of nonlinear system models has been shown to possess many of the important properties of LTI systems. Although nonlinear, these systems are analytically solvable through a technique known as "inverse scattering", which can be viewed as a nonlinear analog of the Fourier transform [5]. These systems also admit a class of eigenfunctions, known as solitons, which satisfy a form of superposition [3, 7]. This intriguing class of signals and systems have been proposed for a variety of signal processing and communication applications in which solitons play the traditional role of sinusoidal signals and soliton circuits act as special-purpose signal processors [6].

A diode ladder circuit, presented by Singer in [4], is an accurate model for the Toda lattice, a set of nonlinear equations that support soliton solutions. The diode ladder is shown in Fig. 1-1, with the impedance $Z_n = \alpha/s^2$ realized by the gyrator circuit shown in Fig. 1-2. In [6] a number of compelling communications applications are presented using solitons as carrier waveforms. The nonlinear soliton systems can then be used as tuned multiplexors and demultiplexors for the soliton signals they support. The Toda lattice circuit shown in Fig. 1-1 plays a particularly important role in the development of many of the communication strategies in [5]. This thesis details many of the practical issues involved in the design and implementation of a Toda lattice circuit along with a simple communication example.

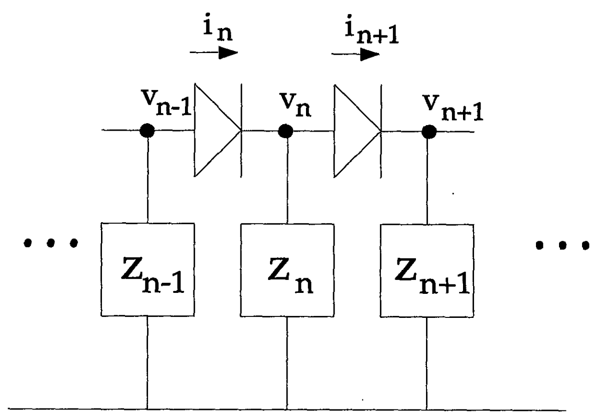


Figure 1-1: Diode ladder network.

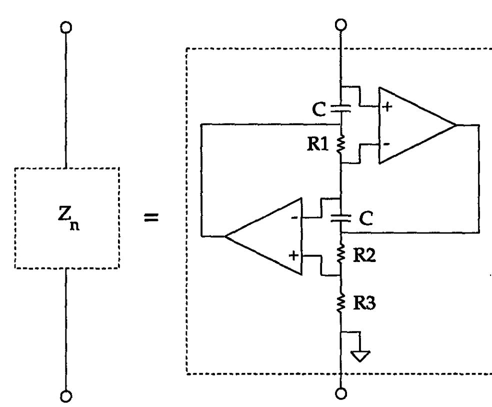


Figure 1-2: Double capacitor circuit design.

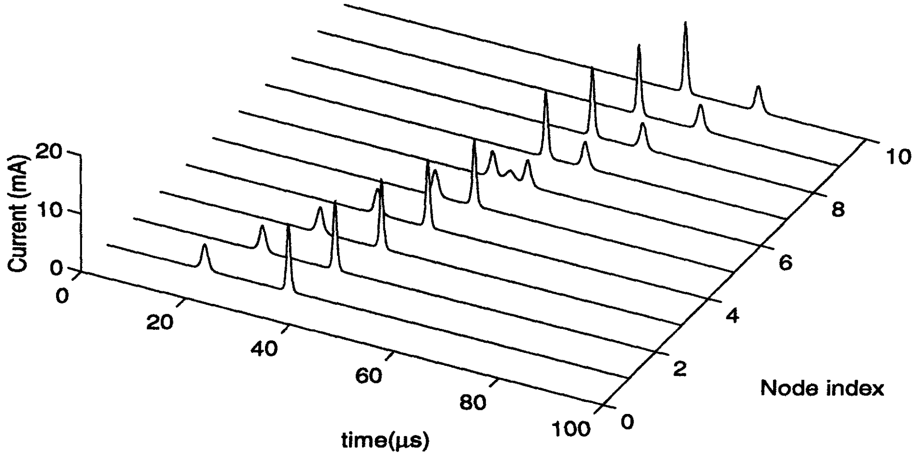


Figure 1-3: HSpice simulation of two solitons in the diode lattice. Each horizontal trace shows the current through one of the diodes.

For communication purposes, two of the most important properties of the Toda lattice solitons are shown in Fig. 1-3. First, these solutions have amplitude-dependent pulse-width and velocity, yielding high-amplitude short-duration solitons which travel faster than those of lower amplitude and longer duration. Second, soliton solutions satisfy a nonlinear form of superposition whereby two solitons pass through one another leaving each virtually unchanged (except for a small phase shift) after their nonlinear interaction [5].

As a function of time, the first trace in the figure shows a small-amplitude long-duration soliton followed by a higher-amplitude, shorter-duration soliton. By the sixth node in the lattice (the sixth trace in the figure), the taller soliton has caught up with the smaller one, and the solitons are coincident. By the tenth node of the lattice, the higher amplitude soliton appears first as a function of time. Hence, this soliton has traveled faster through the lattice. The sixth node of the lattice shows the solitons when they are coincident in time. Rather than a simple linear superposition, the signal displays a highly nonlinear interaction. After the collision, however, each soliton reappears as if the two solitons simply passed through one another. Although this apparent decoupling of solutions is common to linear systems, that a nonlinear

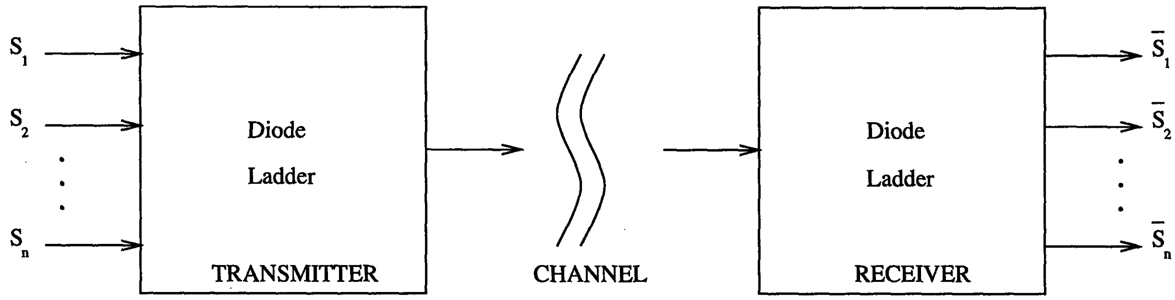


Figure 1-4: Theoretical soliton-based communication system.

system exhibits such a superposition principle is an indication that this a rather remarkable class of systems.

A potential advantage of soliton-based modulation is a form of energy reduction. As multiple Toda lattice solitons interact, the energy of the combined multi-soliton signal is less than when the signals are separate. Fig. 1-3 gives evidence of this behavior, where the amplitude of the signal on the sixth trace is significantly less than the linear superposition of the two soliton amplitudes. Further, although the energy of the transmitted signal is reduced, the ability of a receiver to demodulate the soliton carrier has actually been enhanced [6].

A theoretical soliton-based communication system could function as shown in Fig. 1-4. The transmitter modulates each component soliton signal and then uses the diode ladder to allow the solitons to overlap in time. At this point, the low energy multi-soliton signal is transmitted over a wireless channel. The receiver can then separate the solitons by inserting them into an identical diode ladder circuit. Pulse-position modulation (PPM) can be performed by introducing a small positional shift in the solitons at the transmitter, causing them to appear in different locations at the receiver.

An outline of the thesis is as follows. The circuit designed by Singer in [4] and a description of the Toda lattice equations are discussed in Chapter 2. Based on this design, a preliminary six-stage ladder was constructed on a circuit breadboard. However, it did not perform as simulated. The operational amplifiers on the sixth stage were entering saturation, and the circuit was not robust to component variations: using different operational amplifiers in the gyrator circuit often led to immediate failure. A reliable and fully functional implementation of the diode ladder circuit is presented in Chapter 3. A modulation and demodulation system is also presented, whereby the relative positions of solitons can be modulated at one end of the ladder. The solitons interact, and are demodulated at the other end of the ladder. Design considerations and circuit non-idealities are discussed in Chapter 4. Finally, suggestions for further research and conclusions are given in Chapter 5.

# Chapter 2

# Toda Lattice Circuit Model

The diode ladder circuit developed by Singer in [4] is equivalent to the Toda lattice, a nonlinear system that possesses soliton solutions. The Toda lattice equations describe a chain of masses (each of mass $m$) connected by nonlinear springs which obey a force relationship given by

$$f(r_n) = a\left(e^{-br_n} - 1\right), \tag{2.1}$$

where $a$ and $b$ are arbitrary positive constants, and $r_n = y_{n+1} - y_n$ is the net displacement between the $n$th and $(n+1)$th masses of the ladder. The governing equations of motion for the lattice are given by

$$m\frac{d^2y_n}{dt^2} = a\left(e^{-b(y_n - y_{n-1})} - e^{-b(y_{n+1} - y_n)}\right), \tag{2.2}$$

for masses with rest positions $y_n$. In terms of the forces on the springs, $f_n = f(r_n)$, the expression

$$\frac{d^2}{dt^2}\ln\left(1 + \frac{f_n}{a}\right) = \frac{b}{m}(f_{n-1} - 2f_n + f_{n+1}), \tag{2.3}$$

is equivalent to the equations in (2.2).

To develop a circuit that accurately matches the Toda lattice, the exponential voltage-current relationship of the semiconductor junction diode is exploited [4]. If voltages $v_{n-1}$ and $v_n$ are applied to the terminals of a junction diode, the current through the device is well-modeled by

$$i_n = I_s \left( e^{(v_{n-1}-v_n)/v_t} - 1 \right), \tag{2.4}$$

where $I_s$ is the saturation current and $v_t$ is the thermal voltage of the diode. If the diodes are placed in the ladder configuration shown in Fig. 1-1, then the current through the $n$th shunt impedance, $Z_n$, is given by

$$i_n - i_{n+1} = I_s \left( e^{(v_{n-1}-v_n)/v_t} - e^{(v_n - v_{n+1})/v_t} \right). \tag{2.5}$$

By analogy with (2.2), if the shunt impedance is a "double capacitor" with a voltage-current relation given by

$$\frac{d^2 v_n}{dt^2} = \alpha \hat{i}_n, \tag{2.6}$$

where $\hat{i}_n = i_n - i_{n+1}$ is the current through the $n$th shunt impedance, then the governing equations become

$$\frac{d^2 v_n}{dt^2} = \alpha I_s \left( e^{(v_{n-1}-v_n)/v_t} - e^{(v_n - v_{n+1})/v_t} \right), \tag{2.7}$$

and

$$\frac{d^2}{dt^2} \ln \left( 1 + \frac{i_n}{I_s} \right) = \frac{\alpha}{v_t} (i_{n-1} - 2 i_n + i_{n+1}), \tag{2.8}$$

where $i_1 = i_{\text{in}} - i_2$. These are equivalent to the Toda lattice equations with $a/m = \alpha I_s$ and $b = 1/v_t$. A double capacitor can be realized using ideal operational amplifiers in the gyrator circuit shown in Figure 1-2, which has the required impedance of $Z_n = \alpha/s^2 = R_3/R_1R_2C^2s^2$.

Since any practical implementation must have a finite number of nodes, the lattice must be terminated to avoid reflections. One method of terminating the ladder is to replace the diodes with their equivalent linearized resistance $R_{\text{eq}}$ and then determine the input impedance of the line. This results in

$$Z_{\text{in}} = \frac{R_{\text{eq}}}{2} + \sqrt{\frac{R_{\text{eq}}^2}{4} + \frac{R_{\text{eq}}\alpha}{s^2}}. \tag{2.9}$$

For the component values considered in this thesis and for frequencies below 1 MHz, a load impedance consisting of a 10$\Omega$ resistor and a 0.1$\mu$F capacitor approximate (2.9) well and yield no almost reflections in practice.

When $i_{\text{in}}(t)$ in Fig. 1-1 is of the form

$$\begin{aligned} i_{\text{in}}(t) &= I_s\Omega^2 \text{sech}^2(\gamma t), \\ \gamma &= \Omega\sqrt{I_s\alpha/v_t}, \end{aligned} \tag{2.10}$$

then (2.8) has the solution

$$i_n(t) = I_s\Omega^2 \text{sech}^2(pn - \gamma t), \tag{2.11}$$

where $\Omega = \sinh(p)$. This response corresponds to a single pulse traveling-wave solution, parameterized by the wavenumber, $p$, and is referred to as a soliton solution.

The diode lattice was simulated using HSpice, a circuit simulation package [2], using realistic component models. The diode models used are `d1n4449`'s with $I_s \approx$ 2nA. To prevent saturation of the operational amplifiers in the double capacitor circuits, the resistors are set at $R_1 = R_2 = R_3 = 1\text{k}\Omega$. These values together with capacitors in the gyrators of 10nF permit soliton pulse widths of about 2$\mu$s with amplitudes of about 2mA. The double capacitors use precision `LT1028A` operational amplifiers with a gain bandwidth product of about 50 MHz.

# Chapter 3

# Circuit Implementation

In order to develop a practical modulation and demodulation system, a variety of auxiliary circuitry is required. To begin, the gyrator circuit is inherently unstable, since it corresponds to a linear system with two poles on the imaginary axis. Therefore, its capacitors must be periodically drained by some type of reset circuitry before the voltage across the capacitors becomes high enough to drive the operational amplifiers into saturation. Second, the input to the diode ladder is a current waveform, necessitating a voltage-controlled current source. To induce solitons in the lattice, this current drive waveform should have the correct soliton shape. Hence, a soliton source circuit is needed which must be able to generate multiple solitons with varying sizes and also be sufficiently flexible to permit modulation. Finally, a demodulation system must be developed.

A block diagram of the entire system is shown in Fig. 3-1. Time synchronization in the system is achieved by an external reset signal. To generate solitons, rectangular voltage pulses are generated, combined, shaped, converted to current pulses, and used to drive the diode ladder. A small resistor placed in series with each diode in the ladder allows the current through the diode to be read by observing the voltage across the resistor. A differential amplifier must be used to read this voltage since it is not referenced to ground. At some stage in the ladder, a practical communication system would have a transmitter and receiver for the modulated waveform and the synchronization (reset) signal. In this thesis, however, the two ends of the ladder are

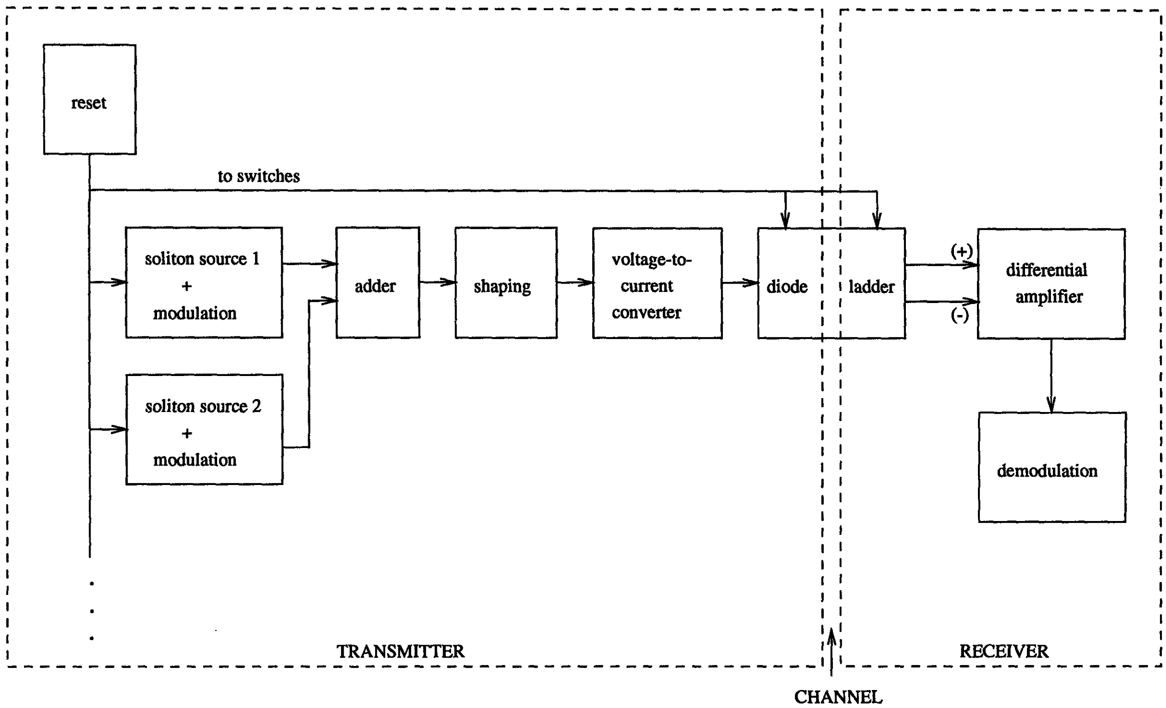


Figure 3-1: Block diagram of entire system.

simply connected by wires.

The reset circuit, shown in Fig. 3-2, uses an LS123 Monostable Multivibrator chip to create an active-high logic-level reset pulse. The reset signal enables DG212 analog switches connected across each capacitor in the gyrator circuit of Fig. 1-2. The switches must be on long enough to fully discharge the capacitors. The time constant for discharge is approximately $RC$, where $R$ is the on-state resistance of the switch. The reset pulse length is controlled by $R_{RESET}$ in Fig. 3-2, with the on-time between reset pulses set by $R_{ON}$.

Assuming constant circuit parameters, solitons are a one-parameter family of solutions, parameterized by the wavenumber $p$. Each soliton generation circuit, shown in Fig. 3-3, has potentiometers which allow an approximate soliton shape to be created. The source circuit employs an LS123 chip, which receives the reset pulse and waits a prescribed time, set by $R_{DELAY}$, before sending out a rectangular voltage pulse, whose width is determined by $R_{WIDTH}$. The pulse height is varied by passing the signal through an inverting amplifier of gain $-R_F/R_{HEIGHT}$, where $R_{HEIGHT}$ is variable. Multiple solitons can be created by duplicating this circuit.

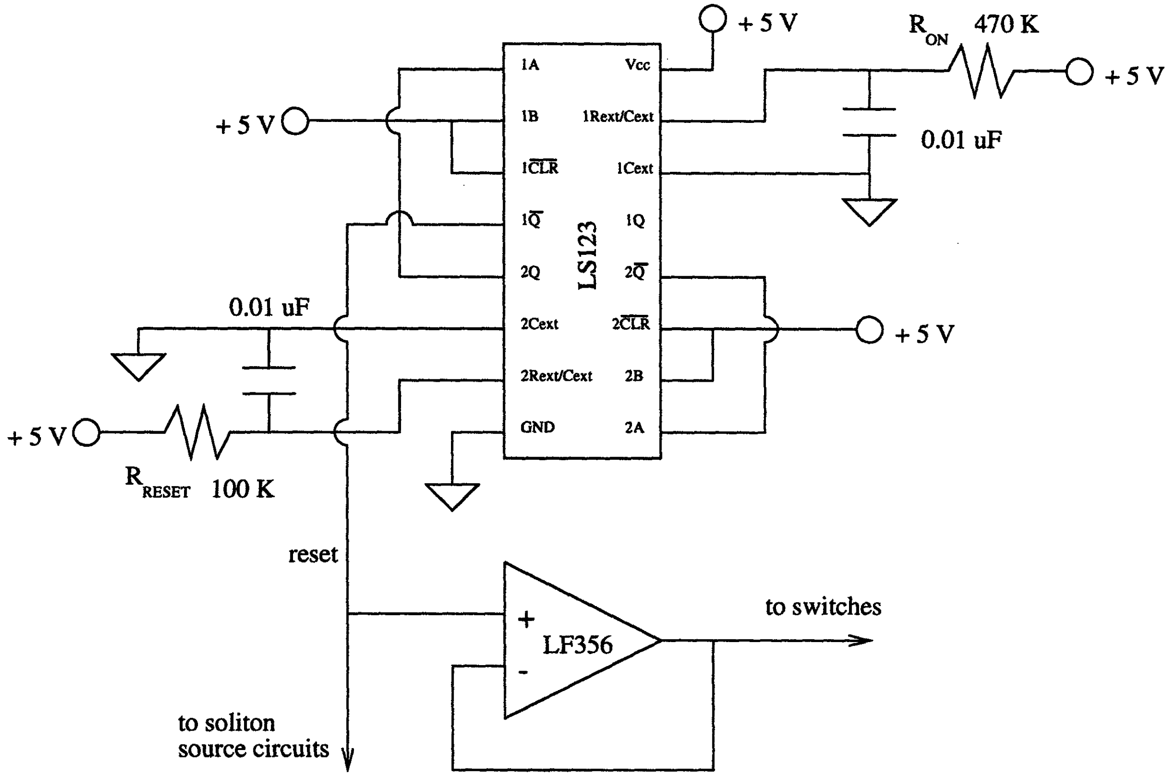


Figure 3-2: Reset circuit.

Solitons are combined with a unity-gain inverting-adder amplifier, as shown in Fig. 3-4. If the combined signals have a DC offset, it is removed by the zeroing input of this amplifier, which is controlled by $R_{ZERO}$. The low-pass filter smoothes out the rectangular pulses to a more soliton-like shape. The signal is then passed through a voltage-to-current converter, taken from [1], and shown in Fig. 3-5. The output of the converter is connected to the input of the diode ladder circuit, whose circuit topology, along with the termination node, is shown in Fig. 3-6. The gyrator circuit that represents the impedance $Z_n$ is shown in Fig. 3-7. A $10\Omega$ resistor is connected in series with each diode in the ladder so that the diode currents can be read as voltages using a differential amplifier, as shown in Fig. 3-8.

A simple binary PPM system can be realized by replacing the resistor $R_{DELAY}$ in Fig. 3-3 with the circuitry shown in Fig. 3-9. For experimentation purposes, debounced single pole double throw (SPDT) switches with logic level outputs, shown in Table 3.1, are used to vary the resistance. For a practical modulation system,

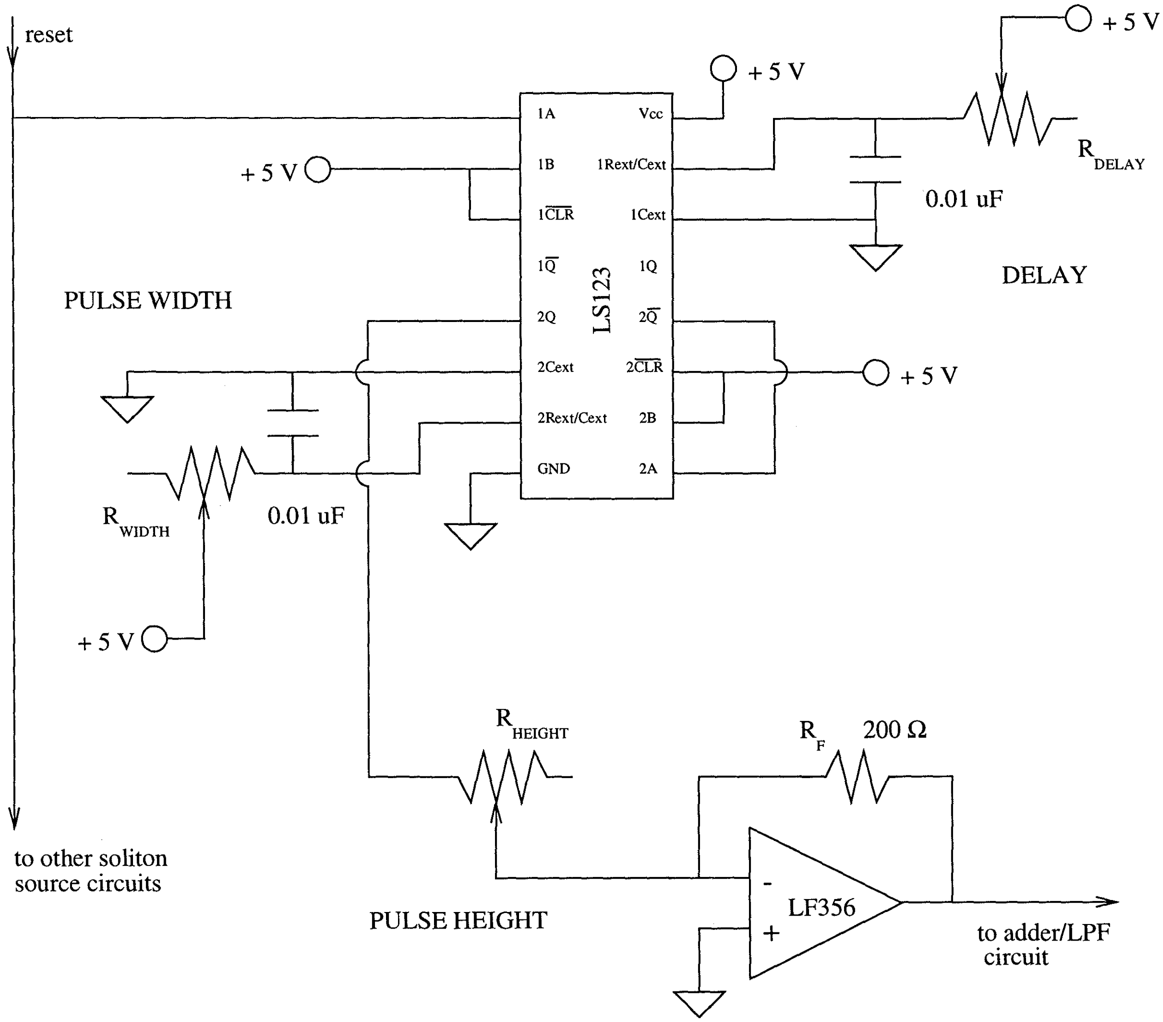


Figure 3-3: Soliton source circuit.

| switch | A | B |
|---|---|---|
| down | H | L |
| up | L | H |

Table 3.1: SPDT switch.

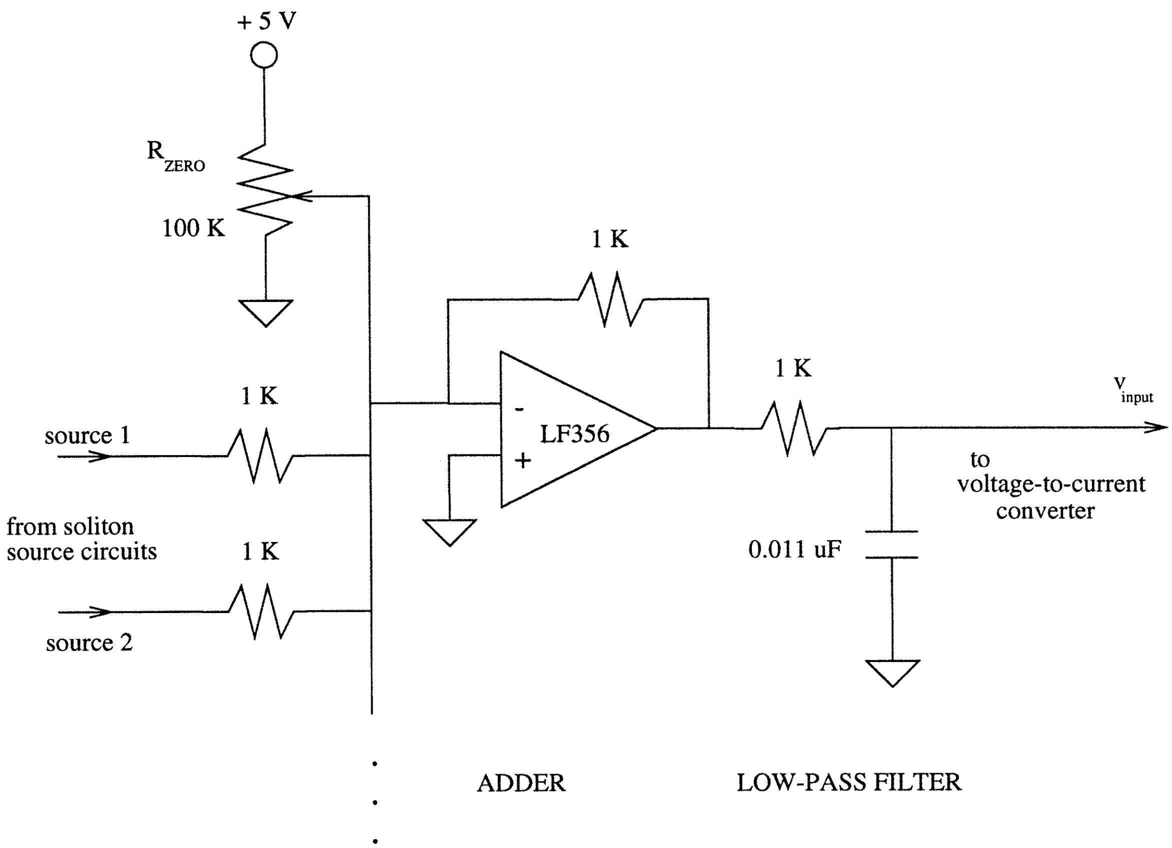


Figure 3-4: Adder - Low-pass-filter circuit.

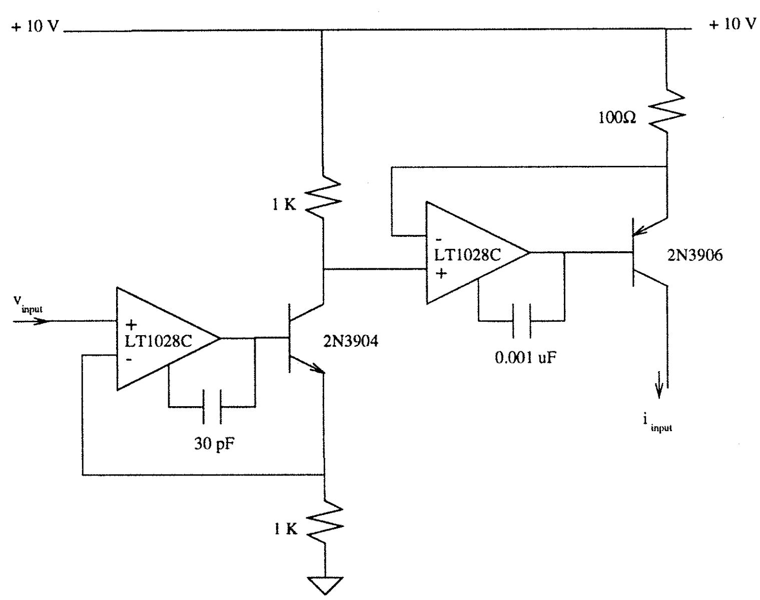


Figure 3-5: Voltage-to-current converter.

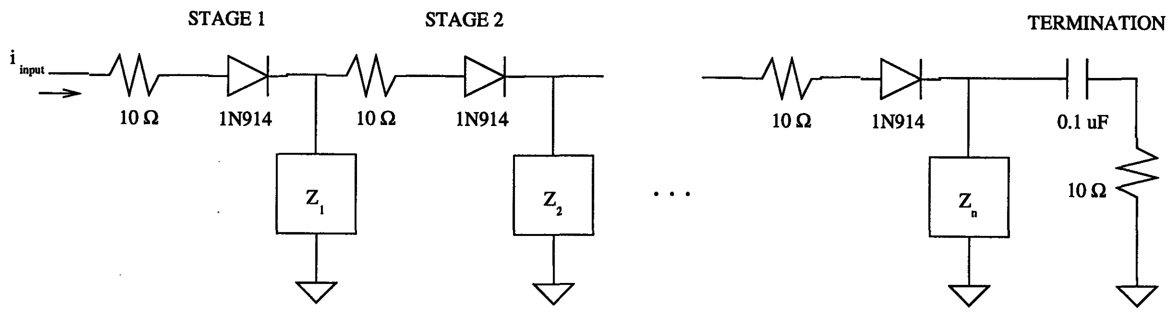


Figure 3-6: Diode ladder network implementation.

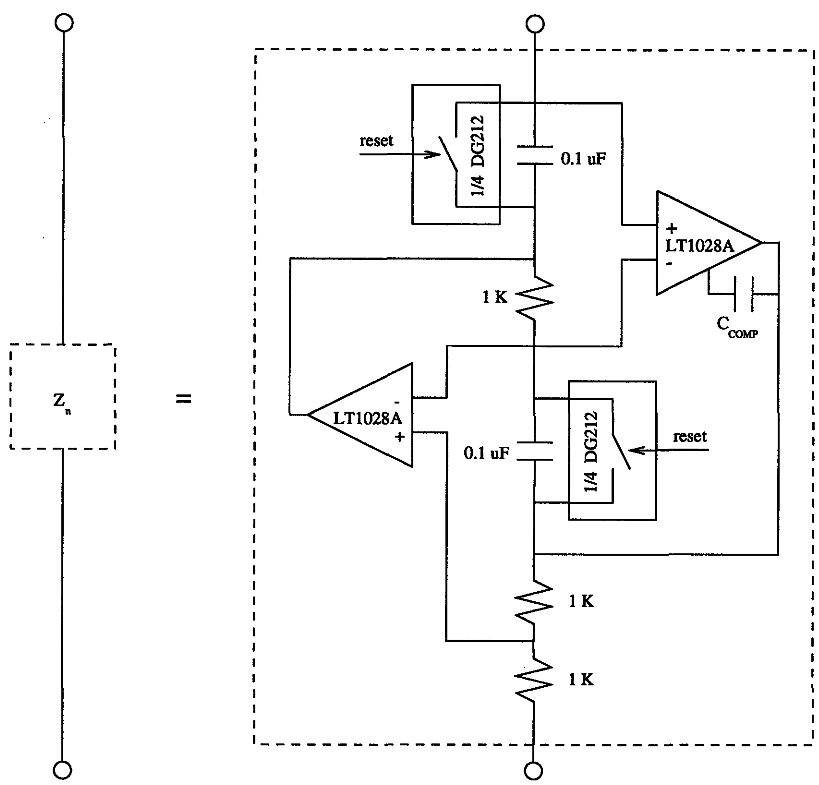


Figure 3-7: Double capacitor circuit.

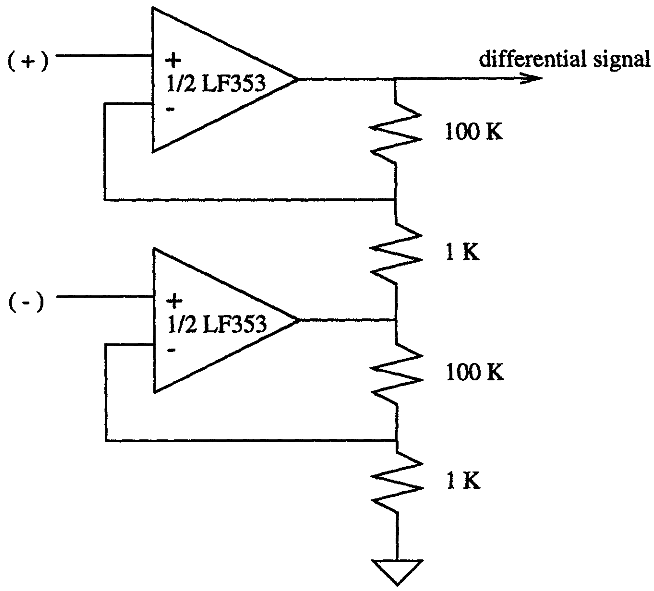


Figure 3-8: Differential amplifier.

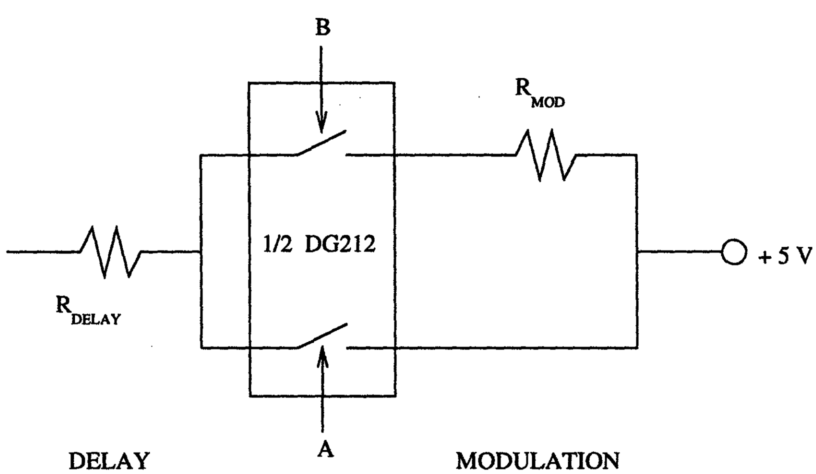


Figure 3-9: Modulation circuitry.

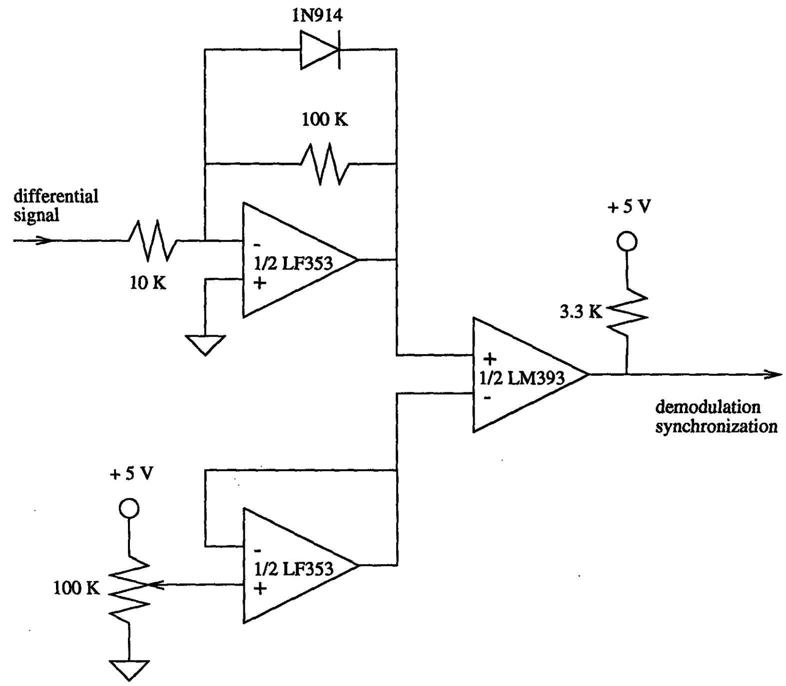


Figure 3-10: Demodulation synchronization circuit.

varistors (voltage controlled resistors) could be used in place of the switches. The length of the delay between reception of the reset signal and generation of a voltage pulse depends directly on the value of the resistance connected to the $1R_{ext}/C_{ext}$ pin in Fig. 3-3. A soliton appears in either its original position, proportional to $R_{DELAY}$, or slightly later in time, proportional to $R_{DELAY} + R_{MOD}$. Hence, a binary PPM system can be realized.

Time synchronization for demodulation is performed using the reset signal, and is facilitated by the negative current 'spike' that appears across the $10\Omega$ resistors at the beginning of the reset pulse. Current flows negatively at no other time, so this spike permits synchronization without signal redistribution. The demodulation synchronization circuit shown in Fig. 3-10 receives the differential signal, which is inverted, amplified, and then compared to a DC voltage through an LM393 comparator. Since the magnitude of the spike is much less than the magnitude of the solitons, a diode clamp is used to inhibit the negative excursion of the inverted and amplified soliton signal. The synchronization signal is fed to the demodulation circuit, shown in Fig. 3-11.

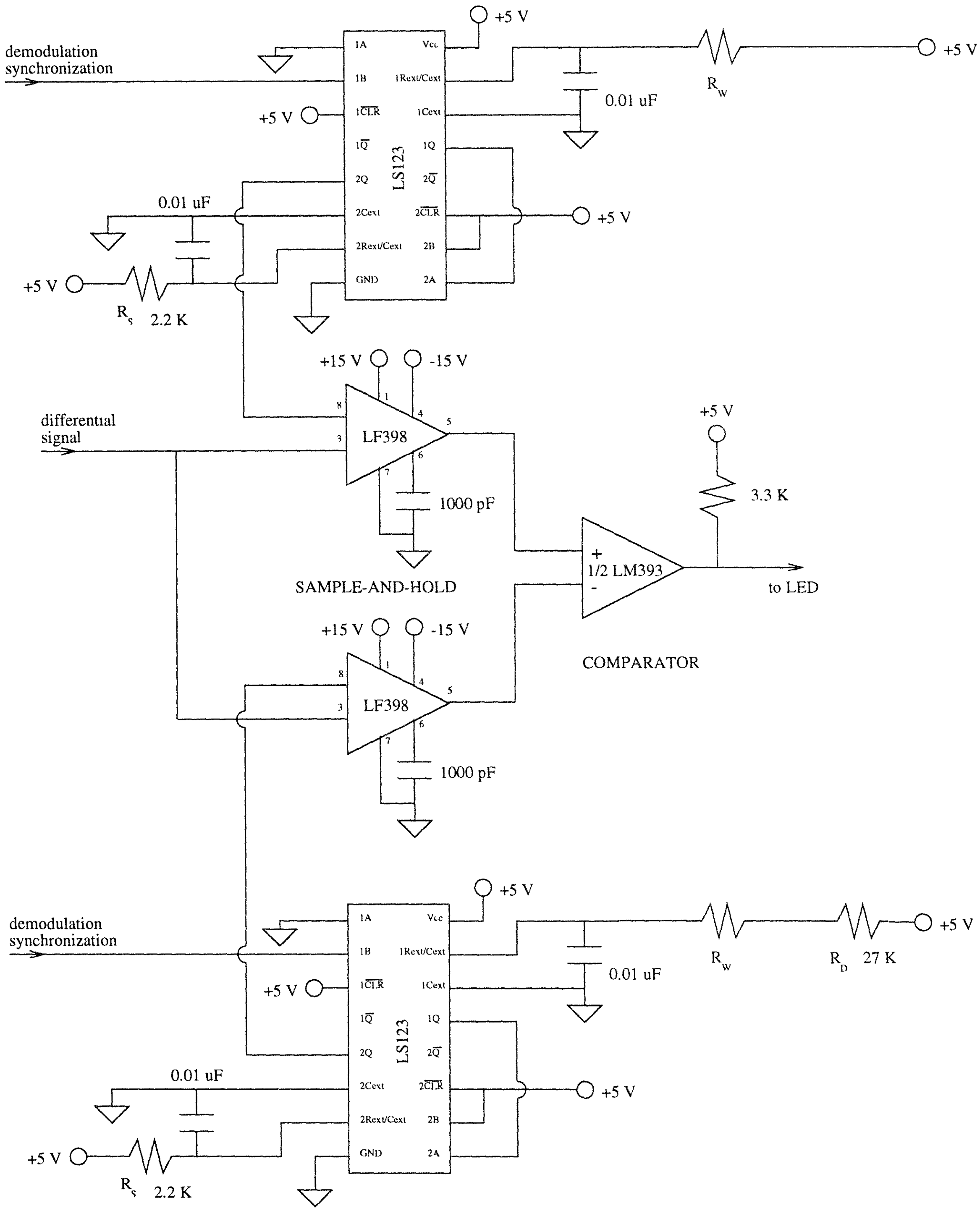


Figure 3-11: Demodulation circuit.

| resistor | soliton 1 | soliton 2 |
|---|---|---|
| $R_{WIDTH}$ | $\sim 8.4\text{k}\Omega$ | $\sim 4.2\text{k}\Omega$ |
| $R_{HEIGHT}$ | $\sim 16.1\text{k}\Omega$ | $\sim 19.1\text{k}\Omega$ |
| $R_{DELAY}$ | $\sim 88\text{k}\Omega$ | $\sim 10\text{k}\Omega$ |
| $R_{MOD}$ | $\sim 3.3\text{k}\Omega$ | $\sim 7.2\text{k}\Omega$ |
| $R_W$ | $\sim 240\text{k}\Omega$ | $\sim 330\text{k}\Omega$ |
| $R_D$ | $\sim 27\text{k}\Omega$ | $\sim 27\text{k}\Omega$ |

Table 3.2: Resistor values.

A binary-valued PPM soliton signal appears in one of two positions. After the synchronization signal is received, demodulation is performed by sampling the differential signal at each of these positions, at the location of the peak amplitude of the soliton. The upper `LF398` in Fig. 3-11 performs a sample-and-hold on the differential signal after a time set by $R_W$, while the lower `LF398` waits a time set by $R_W + R_D$. The sample levels are compared through an `LM393` comparator, whose logic-level output is connected to an LED. Each soliton requires its own demodulation circuit.

A stable nine-stage diode ladder with a two-soliton binary-valued PPM system was constructed. Setting $R_{RESET} = 100\text{k}\Omega$ and $R_{ON} = 470\text{k}\Omega$ in Fig. 3-2 gives a reset pulse of approximately $330\mu$s and an on-time of approximately $1500\mu$s. The resistor parameter values that are used to generate the two solitons are listed in Table 3.2. The nonlinear interaction of the solitons takes place on stage 3 and demodulation is performed from stage 5. Nine stages are included to ensure that the termination node has a negligible effect on the stage where demodulation takes place.

Due to component tolerances and other non-idealities, the diode ladder is not uniform. Unfortunately, soliton velocity is highly dependent on many component parameters. A newly-constructed ladder would have slightly different component parameters, implying that resistor parameter values for the two solitons can only be approximately determined. In the circuit, approximate values are calculated and a small potentiometer is connected in series with each resistor to allow for adjustment.

# Chapter 4

# Design Considerations and Circuit Non-Idealities

The HSpice model for the diode ladder circuit is rather idealistic. Each stage of the ladder is identical to the next, creating a perfectly uniform ladder. The actual circuit implementation, however, is decidedly non-uniform. This chapter discusses some of the non-idealities that are not evident from HSpice simulations of the diode ladder, and also examines the reasons behind the instability of the preliminary six-stage ladder.

The original HSpice design called for 10nF capacitors in the double capacitor circuit, and `d1n4449` diodes with $I_s \approx 2\text{nA}$. The actual circuit, however, uses `1N914` diodes with $I_s \approx 25\text{nA}$. HSpice simulations with $I_s = 25\text{nA}$, $C = 10\text{nF}$ and input rectangular pulses with amplitudes of about 2mA fail to produce soliton solutions. By replacing the capacitors in the gyrator circuit with $C = 0.1\mu\text{F}$ to allow solitons in the 2mA range with $p \approx 6$, HSpice simulations succeed in producing soliton solutions. Despite these changes, the circuit remained unstable: the operational amplifiers on the sixth stage were still entering saturation. Stability was finally achieved by adding a compensation capacitor, $C_{COMP}$, to the double capacitor circuit as shown in Fig. 3-7, which reduces the gain-bandwidth product of the `LT1028A` op-amps. The value of $C_{COMP}$ was determined empirically; the capacitors range in value from 20pF to 40pF. Compensation also makes the ladder robust to non-uniform op-amp device characteristics: $C_{COMP}$ minimizes the effect of these variations, allowing any LT1028A to be used in any stage of the ladder.

HSpice simulations predict that solitons will decay slightly and uniformly in amplitude as they travel down the ladder. The loss comes from the $10\Omega$ resistors, and the non-idealities of the LT1028A operational amplifier model. The decay is uniform because there are no component-to-component variations in the HSpice system model. However, in the actual circuit implementation the decay is more pronounced and is non-uniform. This is probably due to component variations that not only make the diode ladder non-uniform, but also affect the dimensions of solitons that can be supported. Two possible sources, for example, are the variations in $I_s$, the saturation current of the 1N914 diodes, and the capacitors in the double capacitor circuit, whose tolerance is 10%. The amplitude of supported solitons varies directly with $I_s$, while soliton velocity varies with $\sqrt{I_s}$ and with $1/\sqrt{C}$. This may explain why soliton interaction takes place much earlier on the circuit implementation, where interaction occurs on stage 3, than as predicted with HSpice, where interaction generally occurs on stage 5.

Another non-ideality is seen when looking at the node voltages at the top of the double capacitor networks. These node voltages should theoretically be flat when no solitons are passing across them. The circuit, in contrast, exhibits node voltages that rise continuously and irregularly. HSpice simulations also exhibit non-constant node voltages. This is probably due to diode leakage, bias currents, and other non-idealities in the gyrator circuit. Stability is an issue here as well: if the on-time, as controlled by $R_{ON}$ in Fig. 3-2, is too long, rising node voltages can push the operational amplifiers into saturation. Because of this possibility, the on-time is kept as short as possible.

The diode ladder also exhibits an overall warm-up transient, whereby a soliton's position does not remain constant until the transient has passed. The LT1028A data sheets state that the input offset voltage stabilizes after about 5 minutes. The circuit implementation appears to stabilize after about 10 minutes. A drifting input offset voltage implies that the impedance of the double capacitor network is changing, and thus until all LT1028A's have stabilized, a soliton's position at each stage will drift as well.

The precise soliton shape cannot be created by the soliton source circuit, which implies that the diode ladder must 'mold' current inputs of non-soliton shapes into solitons. In both HSpice simulations and the circuit implementation, the input waveform is molded into solitons by the second stage. The explanation of this phenomenon relates to the inverse scattering method of solution whereby a large class of solutions to the Toda lattice comprise a discrete set of soliton components and a continuum of non-soliton components [6, 7]. Essentially, the ladder views the input as a composition of the desired solitons with a non-soliton 'continuum.' The non-soliton components do not propagate at the soliton velocity, and therefore are left behind.

The negative current spike that appears across the $10\Omega$ series resistors at the onset of the reset signal is a result of imperfectly synchronized reset signals. The capacitors in each gyrator circuit thus discharge at slightly different times. This causes a voltage difference across the resistors, which manifests itself as the negative current spike.

Non-uniformities and less than ideal components play a large part in the inability of the diode ladder circuit to match simulated results. There is a cost-performance trade-off: more expensive (but more closely matched) components will allow more predictable and reliable performance. This is important because many of the signal processing applications proposed in [6] rely on a close-to-uniform and stable circuit.

# Chapter 5

# Conclusions

The diode ladder circuit presented by Singer in [4] is a much closer approximation to the Toda lattice equations than any previous circuit, and creates the possibility of several compelling communication scenarios. However, the diode ladder's inherent instability and the non-ideal nature of the ladder's actual breadboard implementation combine to create a set of problems that are not evident from the somewhat idealistic HSpice simulations of the ladder. As such, initial implementations of the circuit on a breadboard were highly unstable. This thesis describes a stable and fully operational breadboard implementation of the diode ladder circuit. A simple PPM system is also presented. Unfortunately, the circuit still does not perform exactly as HSpice simulations predict due to component tolerances and other non-idealities.

Any effort to improve the precision of the components in the diode ladder point in the direction of an integrated circuit implementation of the lattice. As the ladder becomes more uniform and closer to ideal, better performance will be achieved. This will allow more stages to be built to accommodate an increasing number of solitons without losing stability and without too much signal decay. Better diodes with lower saturation current will enable the circuit to operate with higher $p$-valued solitons. These higher-velocity solitons will allow faster modulation and demodulation.

The sample-and-hold demodulation scheme, though clearly a sub-optimal strategy [6], is analogous to a matched filter receiver for a narrow rectangular pulse. The optimal minimum probability of error receiver amounts to processing the received signal with a matched filter for the soliton and then sampling the output at the locations of the two PPM possibilities. Therefore, the sample-and-hold demodulation scheme can be viewed as an approximation to the minimum probability of error receiver in that the LF398 integrates the received soliton signal over two different time periods, and compares the results to determine the most likely location of the soliton.

An unfortunate aspect of the PPM system is the necessity of time-synchronization for demodulation, using the reset signal. Pulse-coded modulation, where a bit would be represented by the appearance or lack of a soliton, has the same problem. Pulse-amplitude modulation (PAM), on the other hand, obviates the need for time-synchronization since a soliton's position has no bearing on demodulation. PAM is also straightforward to implement given that the diode ladder molds non-soliton inputs into solitons: likely, only $R_{HEIGHT}$ in Fig. 3-3 would need to be modulated.

Implementing the Toda lattice circuit model on a breadboard creates a host of interesting problems that are not apparent from the HSpice simulations. Developing better methods of dealing with these non-idealities must be researched before a true communication system can be designed.

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