Characterization of LOCOS and Oxidized Mesa Isolation in Deep-Sub Micrometer SOI NMOS Processes

by

Jeffrey Wade Thomas

Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

May 1995

© Jeffrey Wade Thomas, MCMXCV. All rights reserved.

The author hereby grants MIT permission to reproduce and distribute copies of this thesis document in whole or in part, and to grant others the right to do so.

Author..
Department of Electrical Engineering and Computer Science
May 23, 1995

Certified by..
James E. Chung
Assistant Professor of Electrical Engineering

Certified by..
Craig L. Keast
Director of Microelectronics Laboratory, Lincoln Laboratory

Accepted by..
F.R. Morgenthaler
Chairman, Department Committee on Graduate Students

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

JUL 17 1995

LIBRARIES
Barker Eng

Characterization of LOCOS and Oxidized Mesa Isolation in Deep-Sub Micrometer SOI NMOS Processes

by

Jeffrey Wade Thomas

Submitted to the Department of Electrical Engineering and Computer Science
on May 23, 1995, in partial fulfillment of the
requirements for the degree of

Master of Science in Electrical Engineering and Computer Science

Abstract

Device isolation is a very important component of VLSI manufacturing. In this work, an NMOS process and isolation test structures and devices were designed to characterize LOCOS and Oxidized Mesa isolation for use in SOI technology. For LOCOS, the key variables were the field-implant dose, stress-relief oxide thickness, field-oxidation time/thickness, silicon-film thickness, and field spacing. The four latter variables control the extent of lateral encroachment and stress-related oxidation effects. These parameters along with the field-implant dose, effectively controls the extent of lateral isolation and its effects on devices. The sidewall implant dose and oxidation thickness, which control 2-dimensional charge sharing effects at mesa corners and the existence of parasitic devices, were the variables of interest for Oxidized Mesa isolation. Focusing on thin films, substrates with top layer silicon film thicknesses of 50nm and 90nm were used to fabricate arrays of isolation islands, diode structures, sidegating structures, and transistors of varied dimensions and geometries. LOCOS characterization began with the testing of and performing data analysis on the isolation islands to quantify design constraints on isolation in terms of leakage. Hoand and Colinge suggested that top layer silicon film thicknesses ≥ 150nm necessitated excessive oxidation times to achieve complete isolation[12,14]. Results showed this phenomenon not to exist with top layer silicon film thicknesses of 90nm and below, and presented in design space graphs defining allowable process and structure parameters leading to effective isolation.

Thesis Supervisor: James Chung
Title: Assistant Professor of Electrical Engineering

Thesis Supervisor: Craig Keast
Title: Director of Microelectronics Laboratory (ML), Lincoln Laboratory

Acknowledgments

I would like to express my deepest gratitude to Professor Jim Chung and Dr. Craig Keast for supervising this project, imparting your knowledge of the subject on me, and unknowingly giving me the ever so timely words of encouragement. Thanks to the staff of the Microelectronics Laboratory, Lincoln Laboratory for your patience in enduring the many questions which arose while learning my way around the clean room as well as when doing this thesis work. A special thanks to Dick, Bernie, Doug, Sandy, Kevin, Jim, Sue, Andy, Gwen, Bruce, Debbie, Bob, Jeff, and Johanna of Groups 87 and 23 for your added support. Gratitude also goes out to Jim's research group on campus, Eric, Jeff, Huy, Rajesh, Jung, Jee-Hoon, Jocelyn, Wenjie, and Ben for making my transition back to campus as smooth as possible. You all were a great help.

Special thanks to the Black Graduate Student Association, BGSA, the staff of the Graduate office, and my other friends for being my family away from home and giving me the distractions which forced me to keep the much needed balance. Many thanks to my very close friends, Dee, Don, Nadine, Araba, Rob, Dennis, LaCreis, Matt, Andy, Daniel, Nicole, Cheryl, Sheree, Sylvester, and Amy.

Last, but certainty not least I would like to give a very special thanks to my family and loved ones for the emotional support you displayed since day one back in September, 1993. With the support and love from you that reached Massachusetts from Virginia, my stay was bearable. I dedicate this thesis to you, Betty, William, Deena, LaVerne, Kimberly, and Victor.

This work has been sponsored by MIT Lincoln Laboratory.

Contents

1 Background

1.1 Isolation Characteristics 9
1.2 Bulk CMOS Isolation Technologies 11
1.3 SOI Isolation Technologies 13
1.4 Project Motivation 15
1.5 Organization of Thesis 16

2 Test Structures/Devices Design

2.1 Introduction 19
2.2 Isolation Islands 19
2.3 Sidegating Structures 22
2.4 Comb Diodes 24
2.5 NMOS Transistors 26

3 Fabrication of Test Structures and Devices

3.1 Introduction 32
3.2 Process Parameter Splits 32
3.3 CAFE 35
3.4 Process Flow 36
3.4.1 Wafer Thinning 36

3.4.2 Device Process Flow 37

4 Simulation of LOCOS Field Oxidations

4.1 Introduction 43

4.2 TSUPREM-4 43

4.3 Simulation Procedure 44

4.4 TSUPREM-4 Oxidation Models 47

4.4.1 Oxidation Theory 47

4.4.2 COMPRESS Model 49

4.4.3 VISCOUS Model 56

5 Testing & Results

5.1 Introduction 62

5.2 Testing 62

5.2.1 Focus 62

5.2.2 Setup 62

5.3 Results 63

5.3.1 T_{si} Effects 64

5.3.2 SRO Effects 67

5.3.3 Spacing Effects 70

5.4 TSUPREM-4 Comparisons 72

6 Conclusion

6.1 Introduction 74

6.2 Summary of Results 74

6.3 Future Work 75

References 76

Appendix A 78

Appendix B 90

Appendix C 107

List of Figures

1 Process Description for LOCOS Isolation 17

2 Process Description for Mesa Isolation 17

3 Process Description for Oxidized Mesa Isolation 18

4 Process Description for REM Isolation 18

5 Two Finger Isolation Structure 27

6 Interdigitated Fingers Isolation Structure 28

7 Three Finger Isolation Structure 29

8 Sidegating Structure 30

9 Comb Diode Structure 31

10 34 Minute Dry Oxidation Step 36

11 Die Labeling for each Field Implant 39

12 Process Flow Diagram 40

13 Fabricated Isolation Structures 41

14 Fabricated Sidegating and Comb Diode Structures 42

15 Statements Used to Generate TSUPREM-4 Grid and Grid 46

16 Model TSUPREM-4 Input Stack 47

17 COMPRESS Model Input File 50

18 Graph, Remaining T_{si} vs Oxidation Time 51

19 Structure Cross Section for Wafer 1, 18 min (10%, COMPRESS Model) 52

20 Structure Cross Section for Wafer 2, 21 min (20%, COMPRESS Model) 53

21 Structure Cross Section for Wafer 2, 24 min (30%, COMPRESS Model) 54

22 Structure Cross Section for Wafer 2, 27 min (40%, COMPRESS Model) 55

23 VISCOUS Model Input File 57

24 Structure Cross Section for Wafer 1, 18 min (10%, VISCOUS Model) 58

25 Structure Cross Section for Wafer 2, 21 min (20%, VISCOUS Model) 59

26 Structure Cross Section for Wafer 2, 24 min (30%, VISCOUS Model) 60

27 Structure Cross Section for Wafer 2, 27 min (40%, VISCOUS Model) 61

28 T_{si} and % Oxidation Design Space Graph 66

29 SRO, Implant, and % Oxidation Design Space Graph 69

30 Spacing, Implant, and 20% Oxidation Design Space Graph 71

31 Spacing, Implant, and 10% Oxidation Design Space Graph 71

Table 1 Features of Isolation Structures 20

Table 2 Features of Sidegating Structures 23

Table 3 Features of Comb Diode Structures 25

Table 4 Process Parameters for LOCOS Isolation 34

Table 5 Process Parameters for Oxidized Mesa Isolation 34

Chapter I
Background

1.1 Isolation Characteristics

Isolation is a very important component in integrated-circuit fabrication. The realization of these circuits is achieved by electrically connecting discrete devices. Throughout the development of integrated circuits, there have been a variety of isolation techniques developed to accommodate different process technologies, e.g., N-channel Metal Oxide Semiconductor (NMOS), Complimentary Metal Oxide Semiconductor (CMOS), and bipolar[1]. Each isolation scheme has attributes which enable it to be compatible with certain process technologies; however, there is a continuous effort towards further scaling device dimensions and increasing the number of devices per chip[2]. As a result, very stringent requirements on isolation characteristics are being imposed.

Achieving low-leakage currents is a must as it degrades circuit performance due to effects such as excessive crosstalk and increased charge at storage nodes[2]. Isolation schemes should be simple in that they are transparent to existing device process flows. The number of additional masking steps needed to fabricate the isolation structure should be minimized to reduce the overall process complexity. Minimizing the mask count also enhances the final product yield by reducing the likelihood of defect formation and

manufacturing costs[1,3,4]. Planarity is another characteristic of device isolation which is very important in realizing smaller device features due to the need for good step coverage and fine-line lithography of subsequent layers[5]. As the push to increase the number of devices per chip persists, isolation technologies will have to be scalable. The minimal device separation for increased packing density will have to be achieved. Maintaining a reliable device process flow mandates the need for controlled lateral encroachment, (the reduction of active device area by the intrusion of the field oxide during growth from the isolation structure) and the lateral diffusion of field-implants into active areas. Device parameters are sensitive to geometrical variations which are affected by lateral encroachment, e.g., the Narrow Channel Effect. In the case of obtaining minimum width and pitch for increased packing density and future ULSI needs, the extent of lateral encroachment undoubtedly will have to be suppressed[1,2,3,5]. Finally latch-up, a parasitic bipolar-transistor action in CMOS technology, will have to be eliminated. More prevalent as device dimensions decrease, latch-up results in a low resistance path between power supply and ground[6].

Presented above are isolation characteristics for current VLSI applications and the upcoming ULSI era. As device geometries are further scaled, the requirements placed upon these characteristics will become even more stringent. By no means are the isolation characteristics to taken as separate entities in the realm of VLSI and future ULSI applications. Each characteristic contributes significantly to the successful fabrication and implementation of VLSI devices and circuits, and undoubtedly will make equal contributions in the ULSI era.

1.2 Bulk CMOS Isolation Technologies

CMOS isolation technologies can be categorized into two groups: LOCOS based and non-LOCOS based. Local Oxidation Of Silicon (LOCOS) involves the selective oxidation of the silicon substrate around active device areas to grow a "field oxide" which dielectrically isolates discrete devices. Fabricating the isolation structure starts with the growing of a thermal, stress relief oxide (usually 20-60nm) and the deposition of a Chemical Vapor Deposition (CVD) nitride layer (usually 100-200nm). Next a photolithography step and subsequent nitride etch are used to define active areas. Once this is done, a channel stop implant and a final thermal oxidation (usually 300-1000nm) are performed to laterally isolate the defined active regions. The isolation structure is completed with the removal of the nitride layer[1]. Figure 1 shows the process sequence for conventional LOCOS. The lateral encroachment of the "Bird's beak, " which is inherent in LOCOS based isolation technologies, is proportional to the thickness of the field oxide grown. For this reason there have been a number of LOCOS based isolation schemes developed to reduce the Bird's beak encroachment while preserving the other needed isolation characteristics. The most well-known of the advanced LOCOS isolation technologies are Sealed Interface Local Oxidation (SILO) of silicon, Poly Buffered LOCOS (PBL), and SideWAll Masked Isolation (SWAMI)[1,7,8]. Two isolation schemes which developed from PBL are Framed Poly Buffered LOCOS and Sealed Poly Buffered LOCOS[9,10].

As the category implies, non-LOCOS isolation schemes involve achieving dielectric device separation through means other than selective oxidation of silicon. To date there are two sub categories of non-LOCOS isolation schemes, Selective Epitaxial Growth (SEG) and Trench/Refill[4,11]. SEG starts with a thermally grown oxide (usually 2μm). Next a trilayer resist coat and photolithography step are used to expose the areas where the "selective" growth will take place. After an anisotropic oxide etch to open windows to the substrate, polysilicon is deposited over the oxide while single crystal silicon, to be used for device fabrication, grows in the open windows. The isolation structure is completed with a step to planarize the wafer surface which removes the polysilicon from the top layer of isolation oxide[4]. Basic Trench/Refill begins with a stress relief oxide and a CVD nitride layer (both comparable to those thicknesses used in LOCOS). As in LOCOS, a photolithography step is used to pattern the nitride layer. Afterwhich the exposed nitride, oxide, and subsequently the silicon substrate are etched to form "trenches." A thin thermal oxide is grown and CVD oxide is deposited into the trenches to serve as the isolating dielectric. Completing the process is a Chemical Mechanical Polish (CMP) or Reactive Ion Etch (RIE) step to planarize the substrate surface[11].

All of the above bulk CMOS isolation schemes have been proven effective for use in VLSI applications. Each has its attributes which makes it more attractive than others in specific cases. In general the particular isolation scheme chosen depends on the special concerns it has to address. Using conventional LOCOS as the baseline, complexity becomes an issue as more advanced LOCOS and non-LOCOS schemes attempt to reduce

lateral encroachment and in turn increase packing density, e.g., SEG and Trench have zero Bird's beak, but involve anisotropic etches, polysilicon deposition, and planarization techniques[7,8]. Good scalability is achieved by both non-LOCOS and advanced LOCOS schemes while planarity and latch-up immunity are dominated by non-LOCOS technologies due to the nature of the processes[4,11].

1.3 SOI Isolation Technologies

Silicon-On-Insulator (SOI) isolation differs from bulk isolation due to the buried dielectric, primarily silicon-dioxide (SiO_2). Silicon-dioxide gives SOI technology intrinsic vertical isolation; however, VLSI and future ULSI applications require total isolation. The two most prominent isolation techniques for SOI CMOS technology are conventional LOCOS and Mesa[12].

LOCOS isolation for SOI involves identical steps taken for bulk LOCOS; however, the field oxide grown for SOI is not as thick as that grown for bulk CMOS. The field oxide grown only has to be thick enough to oxidize the top layer silicon film thickness (t_{si}). Once the silicon film is oxidized down to the Buried OXide (BOX), the active device area is totally isolated from all others.

Mesa isolation begins similarly to LOCOS. First a stress relief oxide and a CVD nitride layer are grown and deposited, respectively. A photolithography step and nitride etch define the active areas where the mesas will be formed. After the nitride and oxide are anisotropically etched, the silicon substrate is RIE etched down to the buried oxide to form the mesa structure. The process is completed with the passivation of the mesa sidewalls which is usually done at the gate oxide step[12]. As in LOCOS for SOI, once

the isolation structure is fabricated, each active device area is totally isolated from any other. See figure 2. Oxidized Mesa and Rounded Edge Mesa are advanced versions of mesa isolation. Different from straight mesa, Oxidized Mesa utilizes a sidewall implant and an oxidation done directly after the substrate etch to round the corners of the mesa island. REM uses of the deposition, patterning, and anisotropic etching of polysilicon to form a mock (polysilicon) mesa structure with side spacers atop the substrate. An anisotropic etch transfers the rounded edge pattern to the substrate[12,13]. Figures 3 and 4 show the fabrication steps for Oxidized Mesa and REM, respectively. Both LOCOS and Mesa satisfy the needs for CMOS VLSI applications. Compared to bulk CMOS isolation SOI isolation is physically simpler; however, problems exist with each that raise concerns as to their effectiveness for use in the future ULSI era.

Lateral encroachment is a severe problem with LOCOS. Oxidation kinetics show that an oxide thickness of $2.2{\times}t_{Si}$ is needed to laterally isolate adjacent islands; however, it has been reported that due to stress build up in the silicon film, an oxidation time equal to triple that needed to grow an oxide $2.2{\times}t_{Si}$ thick on bulk is actually needed for isolation when field spacings are 1µm and below[1]. This poses a problem for realizing smaller devices when the film thickness is ≥ 150nm due to severe lateral encroachment of the Bird's beak[1,14,15]. Oxide encroachment also presents a problem with parasitic transistors formed in parallel with the main device. If the width of this parasitic device is comparable to that of the main device, i.e., if lateral encroachment is extensive, the "subthreshold kink" will be manifested in the subthreshold slope of the device. Also a stress-induced, sharp-tipped Si filament located directly under the Bird's beak can be a

source of off-state leakage current. Moreover, if complete isolation is not achieved the filaments of adjacent active areas can touch, electrically connecting the islands[16,17].

Mesa is plagued with gate oxide thinning and sidewall leakage. Due to the sidewall having a different crystalline orientation than the top of the mesa, the oxide thickness there can be 30% thinner than that on top. Gate oxide thinning is also present at the corners of mesa because of compressive-stress-limited diffusion. These two effects cause early gate oxide breakdown[12,14]. Parasitic sidewall devices are also inherent to mesa isolation as the gate of the devices stretches over the mesa sides. Charge sharing between the main and parasitic devices causes lowered threshold voltages at mesa corners. As in the case of LOCOS, this shows up in the subthreshold slopes of the device as leakage current. Oxidized mesa and REM offer advantages over straight Mesa by creating thicker sidewall oxides to prevent parasitics and rounding corners to reduce 2-dimensional charge sharing effects[12,13,14,].

In terms of the isolation characteristics needed for CMOS fabrication, LOCOS and Mesa are suitable for sub micron technologies; however, in making the transition from bulk to SOI, problems arise with device performance and leakage from parasitics. As is the case in bulk isolation, the determining factor as to which scheme is more applicable depends on the specific concerns the isolation scheme has to address for a given process.

1.4 Project Motivation

SOI technology has undergone much development over the last decade due to its potential use in VLSI CMOS applications. SOI offers many advantages compared to bulk technology, e.g., a simpler isolation structure and radiation-resistant circuits. Latch-up is

completely eliminated in SOI due to the absence of wells. The nature of Mesa isolation and the use of LOCOS with thin films guarantees higher packing density with SOI. Also in the case of thinner films, lowered junction capacitances and increased circuit speed will be achieved[1,14,18]. Although SOI substrates have the intrinsic vertical isolation and a simpler isolation process, isolation-related effects are manifested in device performance degradation. Thus the key issue of device isolation still must be addressed before SOI technology can enter into mainstream VLSI CMOS applications. Studying the effects of various process parameters, e.g., field-oxide thickness, field implants, and stress-relief oxide thickness on the different SOI isolation technologies will aid in understanding how each technology can be implemented in VLSI CMOS applications. Moreover, this will serve as the basis for investigating the potential of SOI technology for the upcoming ULSI era, where device geometries will be further scaled.

1.5 Organization of Thesis

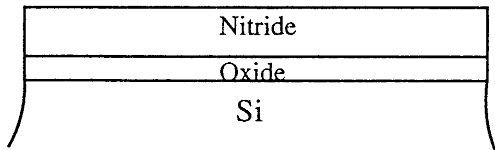
Chapter two describes the design of the test structures used in the experiments and explains their purpose in the project.

Chapter three explains the design of the fabrication process, lists the process parameter splits, and explains how the process flow was generated.

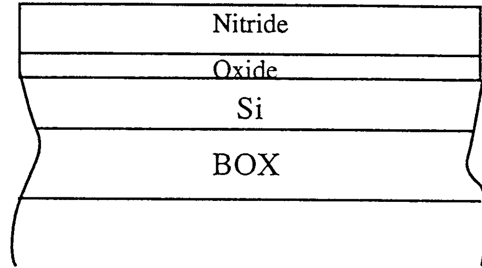
Chapter four explains the simulation of the field-oxidations and the simulation tool used.

Chapter five explains the tests performed on the fabricated structures and devices. Data analysis and results obtained from testing will be given.

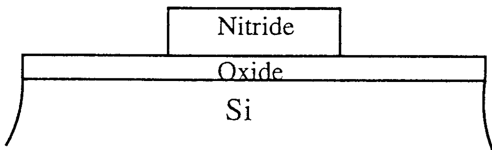
Chapter six concludes the thesis and outlines possible future work.



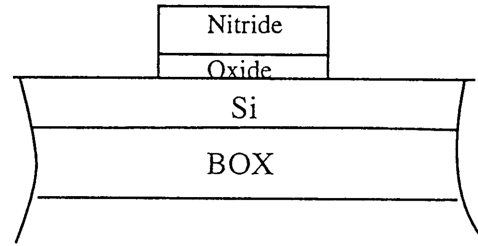
Grow Stress Relief Oxide
Deposit Nitride Layer



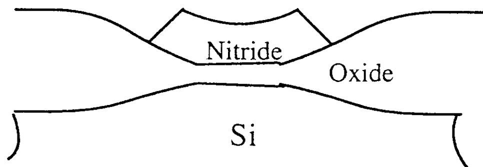
Grow Stress Relief Oxide
Deposit Nitride Layer



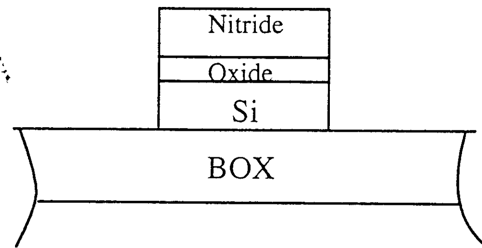
Pattern Nitride Layer
For Oxidation Mask



Pattern Nitride And Oxide Layers



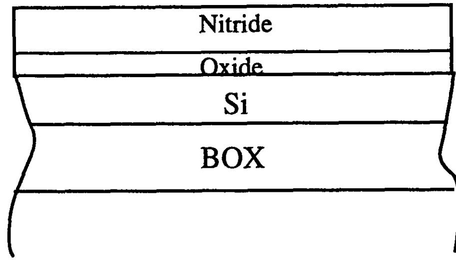
Oxidize To Grow Field Oxide
After Channel Stop Implant



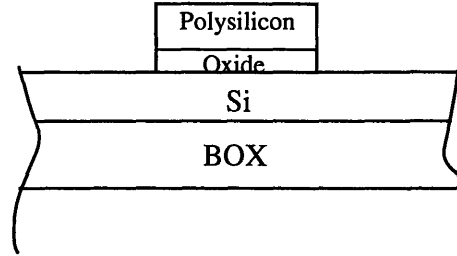
Etch Down To BOX

Figure 1: LOCOS

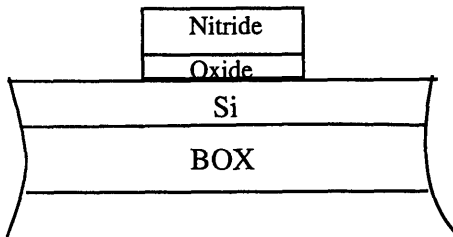
Figure 2: Mesa



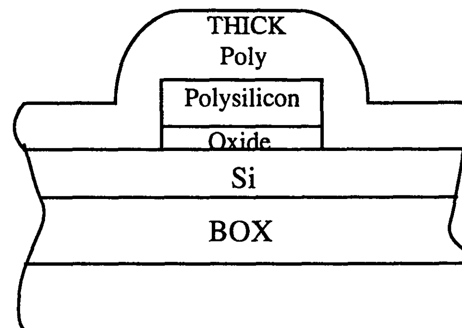
Grow Stress Relief Oxide
Deposit Nitride Layer



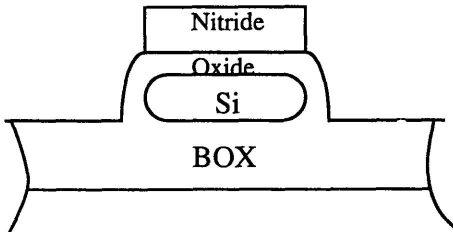
Grow Stress Relief Oxide
Deposit Poly Layer Equal To Si Film Thickness
Pattern Both Layers



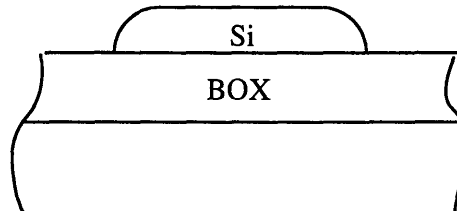
Pattern Nitride And Oxide Layers



Deposit Thick Poly Layer
After Field Implant



Etch Down To BOX And Oxidize



Etch Poly To Transfer Pattern Of Poly Spacers
Remove Stress Relief Oxide

Figure 3: Oxidized Mesa

Figure 4: Rounded Edge Mesa (REM)

Chapter II
Test Structures/Devices Design

2.1 Introduction

This chapter describes the design of the various test structures and devices used for the project. In addition to describing the basic design, a summary of variations in design parameters for each test structure and device are given. Finally, the purpose of each test structure or device in the experiment will be explained.

2.2 Isolation Islands

Figure 5 shows a layout of the basic isolation structure or "island" used to study the effects of process parameters on active area leakage current. It consists of two degenerately doped silicon strips (or fingers) separated by a field region dielectric. Focusing on 1-dimensional leakage, the aspect ratio of the structures was designed to decouple any 2-dimensional effects in leakage current in the structures. The length and width of the active structures were set to 100μm and 2μm, respectively. The features of interest in the structure were the "total active length" of the separated islands (100μm for the basic structure) and the separation or field spacing which, began at 0.4μm and varied up to 5μm. The variations in the structure were such that different total active lengths were obtained. See figure 6. In the case of figure 7, the aspect ratio was decreased to

introduce 2-dimensional effects in the leakage current. Table 1 summarizes the feature variations of the isolation islands.

Structure Parameters	Basic Two Fingers	Three Fingers (2-D)	Medium Sized Interdigitated	Large Sized Interdigitated
Active Width (μm)	2	2	2	2
Total Active Length (μm)	100	20	~20,000	~200,000
Field Spacing (μm)	0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.2, 1.5, 2.0, 3.0, 5.0	0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.2, 1.5, 2.0, 3.0, 5.0	0.5, 0.7, 1.0	0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.2, 1.5, 2.0, 3.0, 5.0

Table 1.

The purpose of the isolation islands were to aid in the characterization of process parameter induced isolation effects. For LOCOS the parameters were the isolation mask, field implant, and field-oxide thickness. The thermal stress relief oxide grown just prior to the deposition of the nitride layer serves as a buffer between the nitride layer and the silicon substrate. Although dependent upon temperature, the intrinsic stress of the as deposited nitride layer is on the order of 10^{10} dynes/cm^2. Upon cooling, without a stress relief oxide this nitride layer would impart a compressive stress on the order of 10^8 dynes/cm^2 in the silicon substrate which would cause severe dislocation damage during a subsequent oxidation[18]. The nitride/oxide layer thickness ratio determines the effectiveness of the buffering oxide layer. Generally, to alleviate the stress and prevent the

formation of dislocations, the minimum oxide thickness used should be $1/3 \times t_{nit}$, the thickness of the nitride layer[1].

The field oxide and field implant determines the physical completion and effectiveness of isolation by separating adjacent active areas and increasing the doping at the active area edge to prevent early inversion. Once the silicon surrounding an active area is oxidized down to the BOX, total isolation is achieved. Haond reported that the oxidation time needed to completely isolate active areas was much greater than bulk estimates. For isolation spacings on the order of 1μm and below, it was found that the time needed for isolation was triple the time needed to grow an equivalent isolating oxide thickness on bulk. If the top layer silicon film is not completely oxidized in the field regions, silicon filaments would exist under the Bird's beak. Under oxidation would result in the electrical connection of adjacent active areas. For this reason, it was proposed that an extensive over oxidation be used to prevent the Si filament, which can be a source of off-state leakage current in addition to intra-island leakage[12,14,15]. In his study of SOI oxidation kinetics, Crowder also reported the presence of Si filaments for sub micron field spacings. Crowder also noticed that over oxidizing silicon films resulted in the upward bending of the film due the expansion of the oxide grown at the back interface. This suggests that over oxidizing during the field isolation step may not be the best solution to the problem of active-area isolation by LOCOS technique. For example, as device dimensions and active area sizes further decrease, over oxidation conceivably may completely erase smaller active areas. Rather, optimization of the amount of field oxide

grown, and the field implant combination, should be used to achieve effective isolation[14].

The isolation structures were used to characterize SOI isolation through studying the effects process variation. Isolation process parameters were the isolation mask (nitride & oxide layers), field implant, and field-oxide thickness. By varying the field spacing and total active length parameters, the isolation structures were used to study process-condition-induced leakage effects, geometrical leakage effects, and packing density. The Mesa version of these test structures were used as controls in this experiment because once the mesa structure is formed, there was no conduction path between adjacent active areas, i.e., no leakage was expected.

2.3 Sidegating Structures

Figure 8 shows a section of the basic test structure used to study sidegating. It consists of active area strips (100µm long and 2µm wide) which are traversed by poly silicon gates. The field region separating the active areas ranged from 0.5µm up to 2µm. The layout of the gate lines and the alternating metal connections to the active areas were constructed to emulate the source and drains of MOSFETs. To effectively study sidegating, active area edges where the gate traverses a silicon step were needed. The actual structure used in the experiment consisted of 100 active areas and 10 gates lines giving a total of 200 edges where the gates crossed silicon steps. The width of the gate was set to 2µm. To give a control in this experiment, one structure consisted of an active area 100µm and 200µm wide. The total area of this structure equaled that of the other

structures; however, the number of silicon steps for the gates to traverse was minimized. Table 2 summarizes the feature variations of the sidegating structures.

Structure Parameters	Basic Structure	Control Structure
Active Area Width (μm)	2	200
Active Area Length (μm)	100	100
Field Spacing (μm)	0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.2, 1.5, 2.0	--

Table 2.

For LOCOS the resulting lateral encroachment from the Bird's beak creates a transition region between the field and active area regions. Coupled to the extent of the Bird's beak and the transition region is the amount of field oxide grown and the field spacing. As suggested above, the field oxidation time needed to completely isolate active areas was much longer than normal for submicron field spacings. This was due to the stress build up in the silicon film as the last remaining section of the film was being oxidized. Because the Bird's beak is proportional to the amount of field oxide grown, narrow field spacings and long oxidations would facilitate more lateral encroachment and thus a long transition between regions. It is desirable to have a short transition because a

long transition promotes sidegating, the formation of parasitics, and device performance degradation.

As mentioned in Chapter one, Mesa isolation inherently has parasitic devices due to the fact that the gate runs over the sidewalls of the structure and the tendency for the gate oxide to be 30% thinner on the sidewalls than that grown on the top. Also charge sharing between the main and sidewall device lowers the threshold voltage at the mesa corners. Sidegating in Mesa isolation results in the presence of sidewall leakage in the sub threshold current of devices[14]. Oxidized Mesa improves the quality of isolation by increasing the gate oxide thickness of the sidewalls and rounding the mesa corners if the oxidation is performed above 965°C, the viscous flow temperature of oxide[14]. Additionally, the sidewall implant increases the doping of the sidewalls thus increasing the threshold voltage of the sidewalls. Done effectively the presence of the sidewall leakage should not be a factor in the subthreshold slope of devices.

These test structures were designed to allow study of the dependence of field spacing, field oxidation, and field implant on sidegating for LOCOS. In the case of Oxidized Mesa the parameters were the sidewall implant and sidewall oxidation thickness.

2.4 Comb Diodes

Figure 9 represents the layout of the comb diode structures used in the experiment to study stress-induced diode leakage. Similar to a n-channel MOSFET from a top view, the structure has two n+ implanted regions separated by a polysilicon gate. The n+ regions are electrically connected to give the effect of a very large diode. Between the two abutted poly gate structures is a p+ region for contact to the substrate. The width of

the poly gate fingers and the active areas are each 2μm. There are a total of 100 gate fingers which gives a total of 200 intersecting points where leakage can occur. The length of the gate fingers and the length of the diode junction was set to 20μm for this device. There was one variation to the design of the device wherein the junction length of one structure was kept the same as above, while the number of intersection points was increased to 4000. Table 3 summarizes the design features of the comb diodes. Note: Due to the fact that this experiment was for NMOS technology, the diode structures designed will be fabricated, but will not be functional, i. e., no p+ implant was used.

Structure Parameters	Diode 1	Diode 2
N+ Region Width (μm)	2	2
Poly Gate/Junction Length (μm)	20	20
Number of Intersections	200	4000

Table 3.

As mentioned before, there is stress between the silicon nitride and the silicon substrate. The use of the stress relief oxide is to alleviate this stress and reduce the likelihood of dislocation defect formation; however, thin oxide layers allow more of the stress inherent in the nitride layer to couple into the substrate promoting the likelihood of substrate crystal damage. Dislocations extending across the n+/p junctions of the diode device would result in easier conduction paths for dopants causing unwanted leakage

through the junction and possibly early junction breakdown [19]. In this experiment, the comb diodes were used to study the process dependent occurrence and effects of stress/damage induced leakage.

2.5 NMOS Transistors

The test structures mentioned in the above sections were designed to investigate discrete SOI isolation effects, namely active-area leakage, sidegating, and diode leakage; however, these effects are also manifested in the performance of devices. For example, in his study of the effects of sidegating on SOI transistors with LOCOS isolation, Chen found that the subthreshold current and subthreshold kink were dependent upon the width of the transistor. As previously mentioned, the kink in the subthreshold current was from a parasitic transistor in parallel with the main device. As the width of the main device is decreased, the subthreshold kink decreases due to the parasitic device characteristic over shadowing that of the main device. Also contrary to the Narrow Width Effect in bulk devices, as the channel width of a n-channel SOI MOSFET was reduced, the threshold voltage was found to decrease due to the overbearing presence of the parasitic device[16]. A host of transistors with W/L ratios varying from 50/50 to 1.5/0.15 were designed to allow investigation of the device performance and degradation under the influence of the above effects.

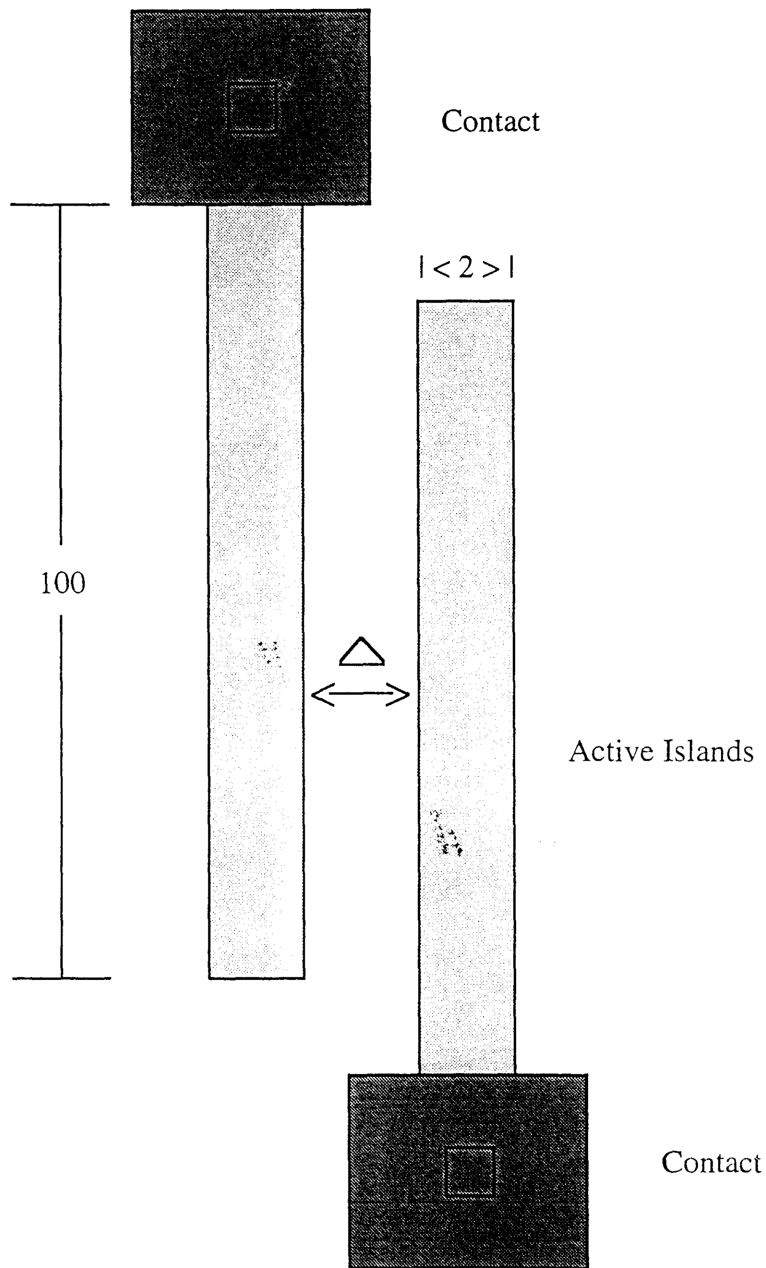


Figure 5: Two Finger Isolation Structure

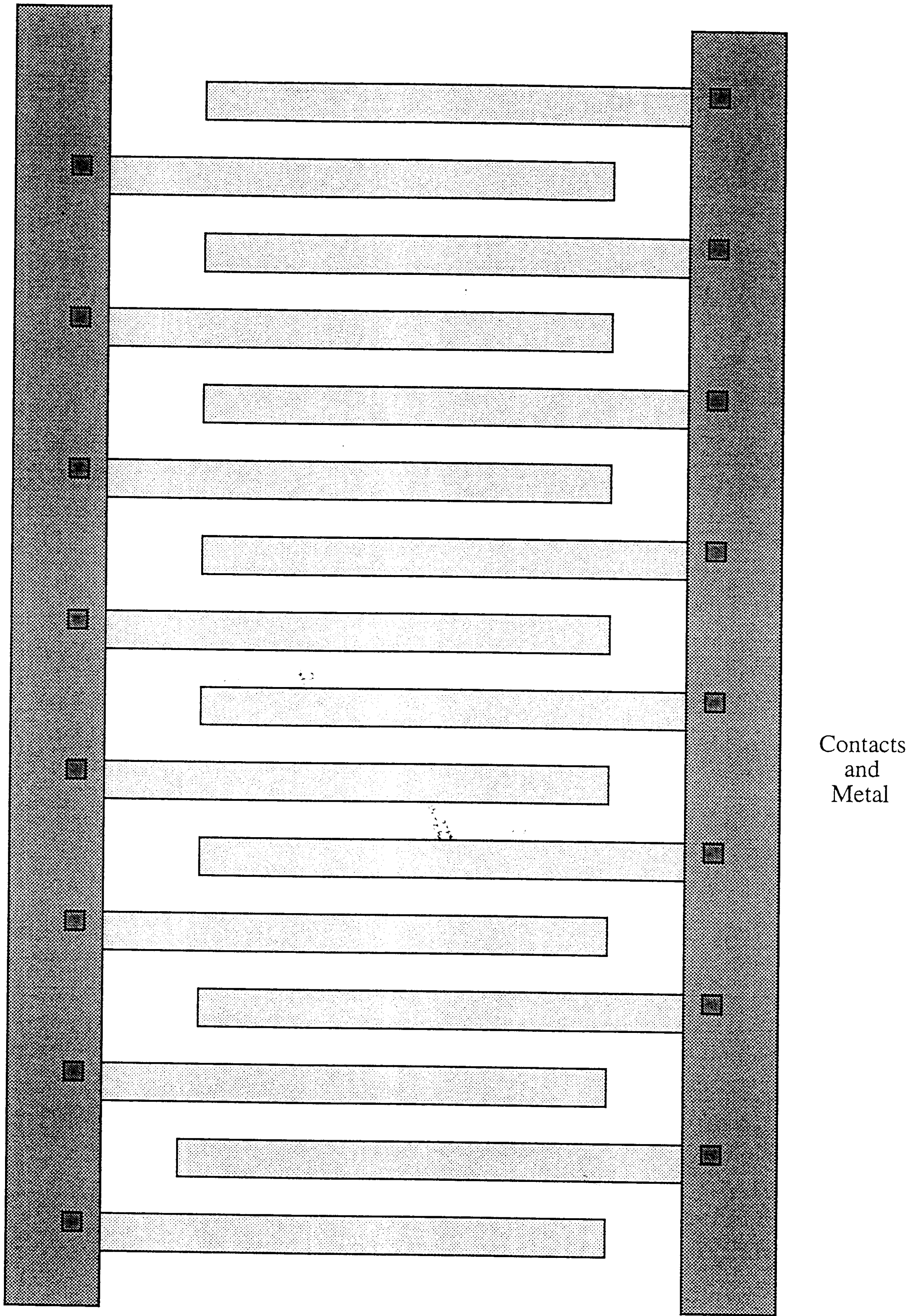


Figure 6: Interdigitated Fingers

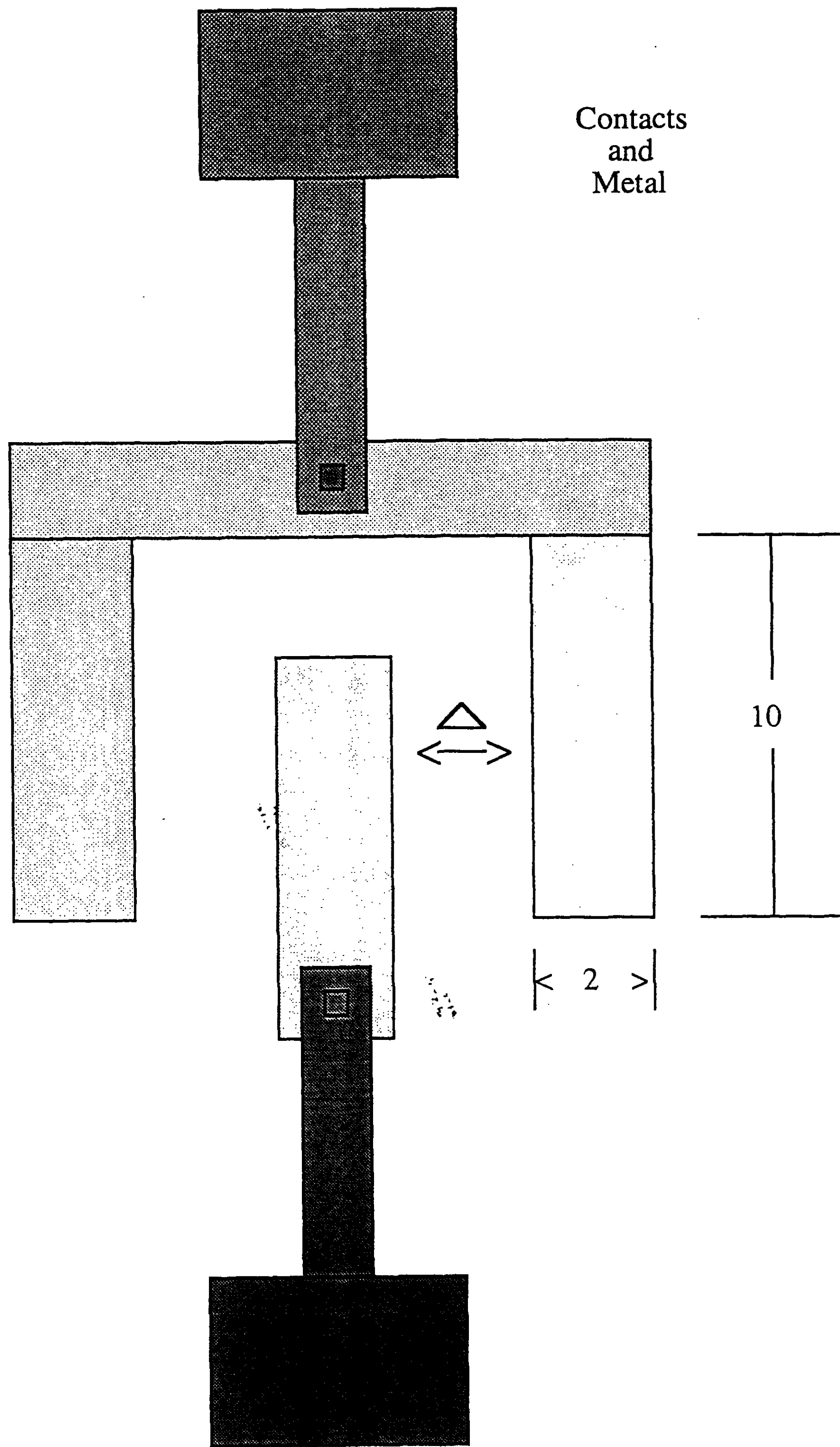


Figure 7: Three Finger Structure with Small Aspect Ratio

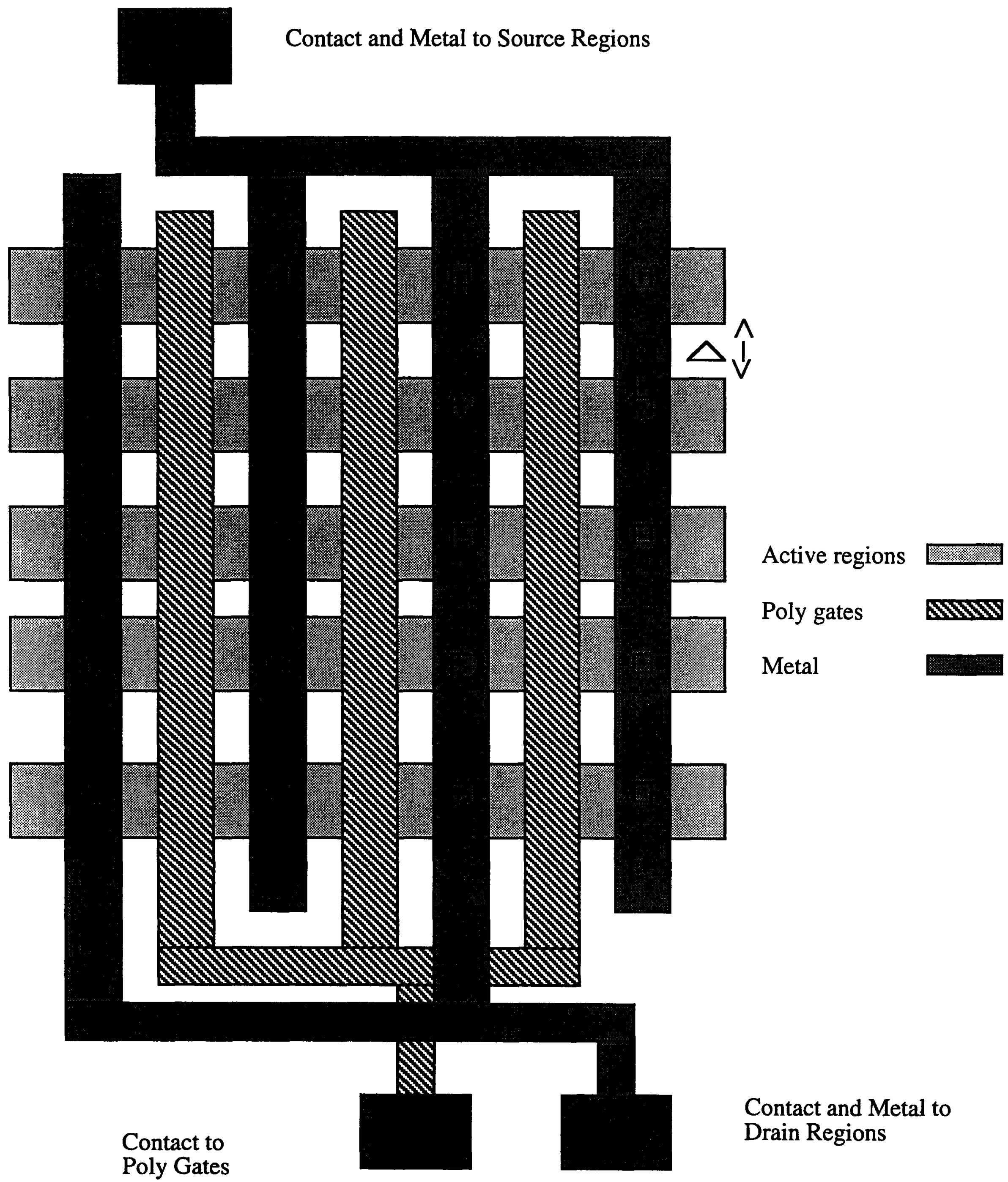


Figure 8: Sidegating Structure

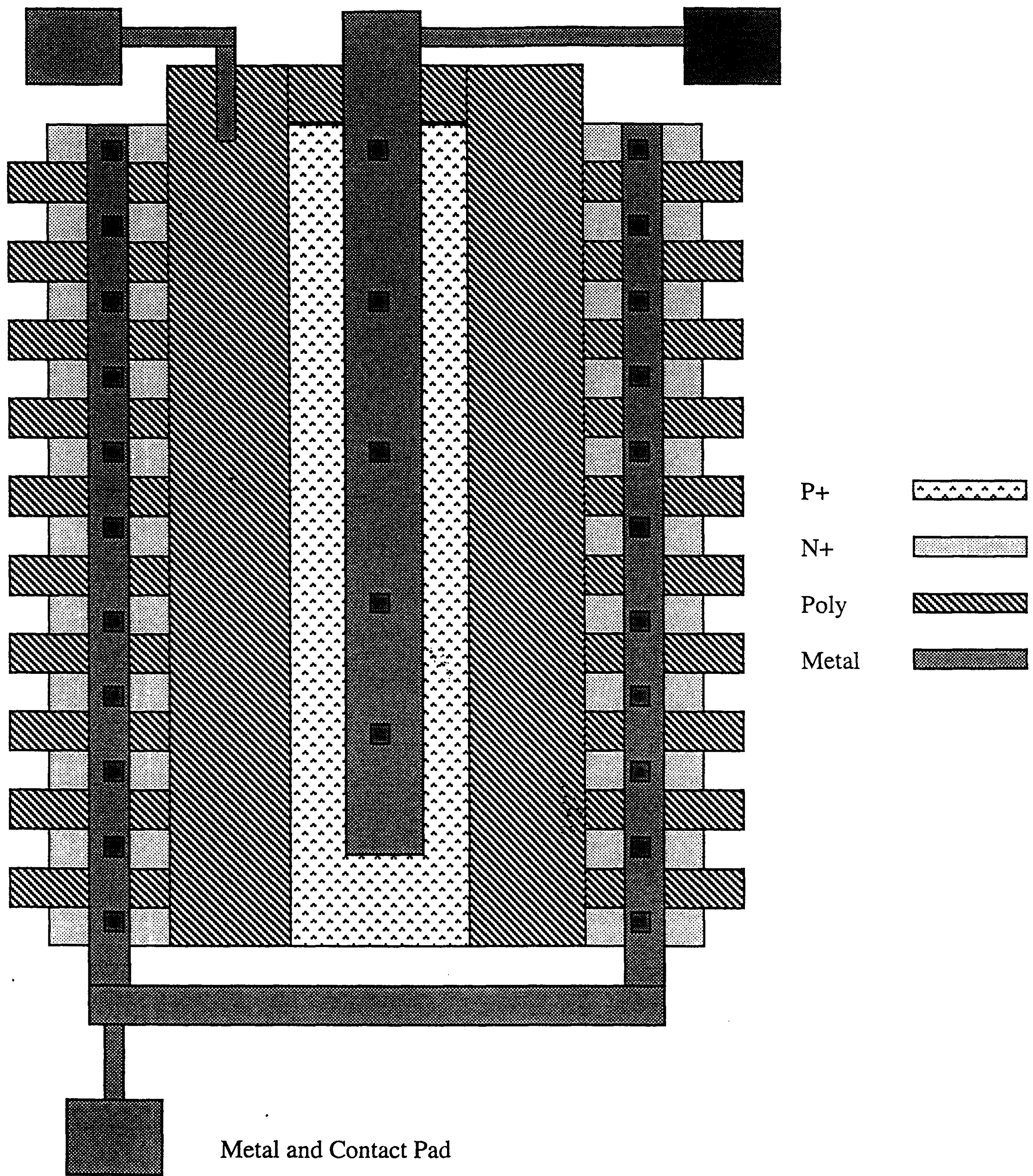


Figure 9: Comb Diode

Chapter III
Fabrication of Test Structures and Devices

3.1 Introduction

This chapter begins by describing the process parameter splits for both LOCOS and Oxidized Mesa isolation schemes. Next the tool used to originate the Process Flow Representation (PFR) will be discussed. Finally, the process flow will be explained. Generation of the process flow and device fabrication were done at the Microelectronics Laboratory (ML) at Lincoln Laboratory.

3.2 Process Parameter Splits

There were a total of sixteen Separation by IMplanted OXygen (SIMOX) wafers used in this experiment. Since LOCOS is the more prevalent isolation scheme and because it has more process variables, the focus of the experiment was skewed in its favor and more wafers were dedicated to its study. Twelve wafers were used for the study of LOCOS while the remaining four were used to study Oxidized Mesa. The goal of the parameter splits was to try to develop test structures and devices that had an overlapping mesh of parameters. While some parameters were common to both isolation schemes, each had its unique set of characterizing parameters.

There were two silicon-film thicknesses, t_{si}, used in the experiment. Due to the fact that the most interesting and promising uses for SOI lies in the use of thin films and

fully depleted devices, the first silicon-film thickness was set at 50nm[20]. The same motivation led to the second, yet more conservative film thickness of 90nm. Six LOCOS wafers had a t_{Si} of 90nm while the remaining six LOCOS and the four mesa wafers had a t_{Si} of 50nm. The stress relief oxides used for the LOCOS wafers were 10nm and 35nm. With the masking nitride layer set to 100nm, the 35nm oxide was used to emulate a normal nitride/oxide ratio used for LOCOS while the 10nm oxide was used to intentionally introduce a stress factor into the experiment. Four of the LOCOS wafers of each film thickness had the 35nm oxide while two had the 10nm oxide. The influence of the stress relief oxide affected the Oxidized Mesa isolation only at the sidewall oxidation step. A 35nm oxide was used with all mesa wafers. There were a total of four different field oxidations used in LOCOS. As mentioned before, the study focused on the effectiveness of combining a "normal" field-oxidation time with field implants to achieve isolation. Starting with the wafers that had the 35nm stress relief oxide (for both film thicknesses), the field-oxidation times per wafer were chosen to give a 10%, 20%, 30,% and 40% over oxidation, with the normal oxidation time taken to be the theoretical time, as determined by TSUPREM-4, needed to oxidize down to the BOX. The four remaining wafers (two with 90nm t_{Si} and 10nm oxide, two with 50nm t_{Si} and 10nm oxide) received either a 20% and 30 % over oxidation. In order to ensure maximum possible control in the oxidations, the oxidation temperature was held constant for all oxidations while the oxidation time was varied. Each wafer received three Field implants. There were a total of 21 die per wafer. Four die to be used as controls received no Field implant, five die received field implant F1, six die received field implant F2, and the remaining six die received field implant F3. F1, F2, and F3 were 1E13, 5E13, and 1E14 BF2 implants for the LOCOS wafers, respectively. These implants, which were the sidewall implant for the Oxidized Mesa wafers, were 1E12, 5E12, and 1E13 BF2 implants respectively. The implant energy for wafer with t_{si}=90nm and t_{si}=50nm were 50Kev and 30Kev, respectively. The angle of the implants was set to 45°, and each wafer was rotated 720° while being implanted to

ensure that all sidewalls of the mesa received the implant. The sidewall oxidation thicknesses for the Oxidized Mesa wafers were set to 100nm and 200nm. These values were chosen to offset the removal of the sidewall oxide by subsequent etching of the stress relief and sacrificial gate oxides and to ensure proper rounding of the mesa corners as well as sidewall passivation. Tables 4 and 5 summarize the process parameter splits of each wafer for LOCOS and Oxidized Mesa, respectively.

Process Parameters/ Wafer #	T_{nit} (nm)	T_{si} (nm)	SRO (nm)	Field Oxidation (% over)	Field Implants
1	100	90	35	10	F1-F3
2	100	90	35	20	F1-F3
3	100	90	35	30	F1-F3
4	100	90	35	40	F1-F3
5	100	50	35	10	F1-F3
6	100	50	35	20	F1-F3
7	100	50	35	30	F1-F3
8	100	50	35	40	F1-F3
9	100	90	10	20	F1-F3
10	100	90	10	30	F1-F3
11	100	50	10	20	F1-F3
12	100	50	10	30	F1-F3

Table 4.

Process Parameters/ Wafer #	T_{nit} (nm)	T_{si} (nm)	SRO (nm)	Field Implants	Sidewall Oxidation (nm)
13	100	50	35	F1-F3	100
14	100	50	35	F1-F3	100
15	100	50	35	F1-F3	200
16	100	50	35	F1-F3	200

Table 5.

3.3 CAFE

The process flow for the experiment was created by the Computer-Aided Fabrication Environment (CAFE) software system developed at MIT. CAFE was designed for use in all aspects of integrated circuit manufacturing, i.e., process design and planning and fabrication[21]. At Lincoln Laboratory CAFE is primarily used to generate the process flow for a wafer lot and as a tracking system for the lot as it is being processed. Process flows are generated by using, Flowtool, a program within the CAFE environment which manages a database of fabrication instructions or opsets. Flowtool operates by allowing the originator of the process flow to select and edit an opset corresponding to a particular fabrication step and write it to a Process Flow Representation (PFR) file. For example, selecting the "diff-ox-exp" opset from the opset database creates a window wherein all the parameters for an oxidation to be carried out by the diffusion bay can be entered. Figure 10 shows the results of selecting the diff-ox-exp opset, editing it, and writing it to a PFR file. This diffusion step was a step in the fabrication sequence of the experiment wherein wafers 1-8 and 13-16 received a dry oxidation at 1000°C for 34 minutes with a 10 minute anneal in N_2 at 1000°C. As shown in the figure, the opset window allows the originator to include any special instructions which maybe needed. Once the PFR file is completed, it can be loaded into the CAFE lot tracking system and wafer processing can begin. Once a fabrication step is carried out, CAFE advances the lot to a next queue for subsequent processing.

```
(diff-ox-exp
        :temp-C 1000
        :dryox-time-min 34
        :wetox-time-min 0
        :anneal-temp-C 1000
        :anneal-time-min 10
        :anneal-gas ":N2"
        :rampdown-gas ":N2"
        :rampdown-temp-C 800
        :expected-thickness-A 350
        :number-of-points 49
        :tag1 " I got the settings from Bruce's logs----please confirm settings."
        :tag2 " Which furnace=? Might have to adjust time by a minute or so."
        :tag3 "These are SOI wafers.....measure monitor for thickness."
        :wafs1 ("1-8" "13-16")
        :wafs2 ("1-8" "13-16")
        :wafs3 :none
```

Figure 10: 34 Minute Dry Oxidation Step

3.4 Process Flow

3.4.1 Wafer Thinning

The first step in the process flow was the thinning of the top layer silicon film. The starting top layer thickness and BOX thickness were 200nm and 380nm, respectively. Each of the SIMOX wafers used in the experiment were mapped using a SOI measuring program on a Prometrix 650FT Film-Thickness probe to determine the uniformity of the top layer film thickness. The average silicon-film thickness for a particular group of wafers was used for the thinning procedure calculations. In addition to the desired final silicon-film thickness, the starting film thickness included the amount of silicon consumed during processing. The fabrication steps that consumed silicon were the stress relief oxide oxidation, sacrificial gate and gate oxidations, and the S/D implant re-oxidation/activation. The actual thinning was done by growing a sufficiently thick oxide and removing it with Buffered hydrofluoric acid (BHF). For example, wafers 1-4 were wafers in the LOCOS splits which were to have a final film thickness of 90nm. The

thickness of the stress relief, sacrificial gate and gate oxides was 35nm, 5nm, and 5nm, respectively. All 16 wafers in the experiment received an activation re-oxidation that resulted in an oxide growth of 7.5nm. Taking the amount of silicon consumed by oxide growth to be 44% of the final oxide thickness, the wafers had to be thinned to approximately 113.6nm[19]. The average silicon-film thickness of this group of wafers was 204.4nm; therefore, a 201.7nm thick oxide was grown and stripped.

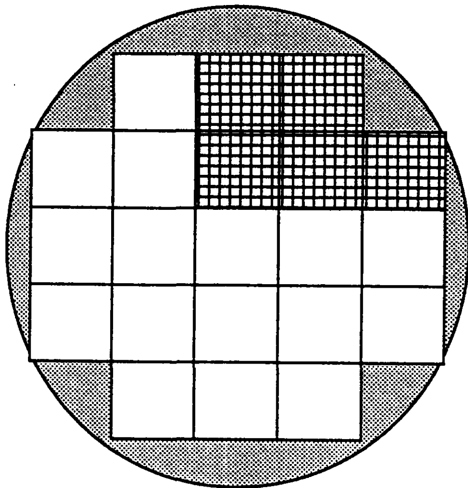
3.4.2 Device Process Flow

After each set of wafers were thinned to their respective starting thickness, the remaining process was that of an NMOS enhancement process for both types of isolation schemes. For the isolation mask (nitride/oxide), the wafers were dry oxidized at 1000°C for either 4 or 34 minutes for grow the 10nm or 35nm stress relief oxide, respectively. This was followed by Low Pressure CVD (LPCVD) deposition of 100nm of silicon nitride. Advanced 248-nm lithography along with APEX-E photoresist was used to ensure the opportunity of studying close island spacings. After patterning the active device regions and plasma etching of the oxidation mask (the oxide was not removed with the LOCOS wafers), the mesa wafers were plasma etched in a LAM Autoetch 490 using $CF_4/He/Cl_2$ etch chemistry to form the mesa structure. Next each LOCOS wafer received the three field implants followed by its respective field oxidation while each mesa wafer received the three sidewall implants and its respective sidewall oxidation. All field oxidations were carried out at 1050°C to coincide with the temperature used by Crowder in is study of SOI oxidation kinetics[15]. Also due to the fact that the field oxide thickness was a parameter and thin films were used, each oxidation run ramped the temperature in nitrogen only. This avoided any oxidation outside of the designated oxidation time. Figure 11 shows the numbering of the die for each implant. The shaded die are those which received the respective implant. The thermal cycle used to grow the

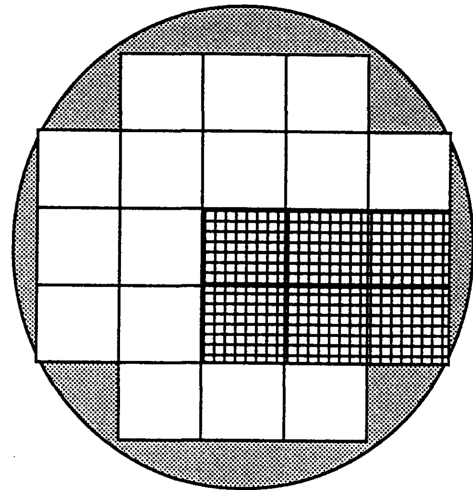
5nm sacrificial gate and gate oxides was an 800°C, 30 minute dry oxidation. The wafers with final a film thickness of 50nm and 90nm received V_T adjust implant of 2.6E12 BF2 dose @ 30Kėv and 3.3E12 BF2 dose @ 50Kev, respectively. The gate material was 250nm of amorphous silicon deposited at 570°C. After gate patterning, the source/drain implant consisted of a 5E15 arsenic dose @ 25Kev. Re-oxidation activation was performed on all wafers at 850°C for 30 minutes. The remaining process was standard procedure for contact definition and metal deposition and patterning. The metal used for this experiment was a 600nm trilayer stack of TiN/AlSi/Ti. The thickness ratio for the trilayer stack is 100nm/450nm/50nm. Figure 12 shows a block diagram of the process. Figures 13 and 14 show pictures of the test structures at the completion of fabrication. Appendix A lists the PFR file generated with Flowtool.

	2	5	6	
1	3	7	8	9
21	4	10	11	12
20	19	13	14	15
	18	17	16	

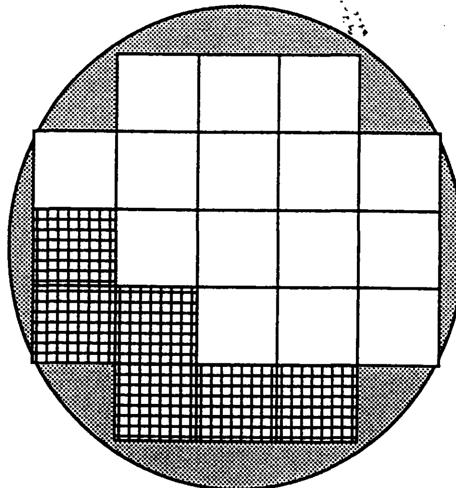
Die Numbering For Field Implants



Field Implant # 1



Field Implant # 2



Field Implant # 3

Figure 11: Die Labeling For Each Field Implant

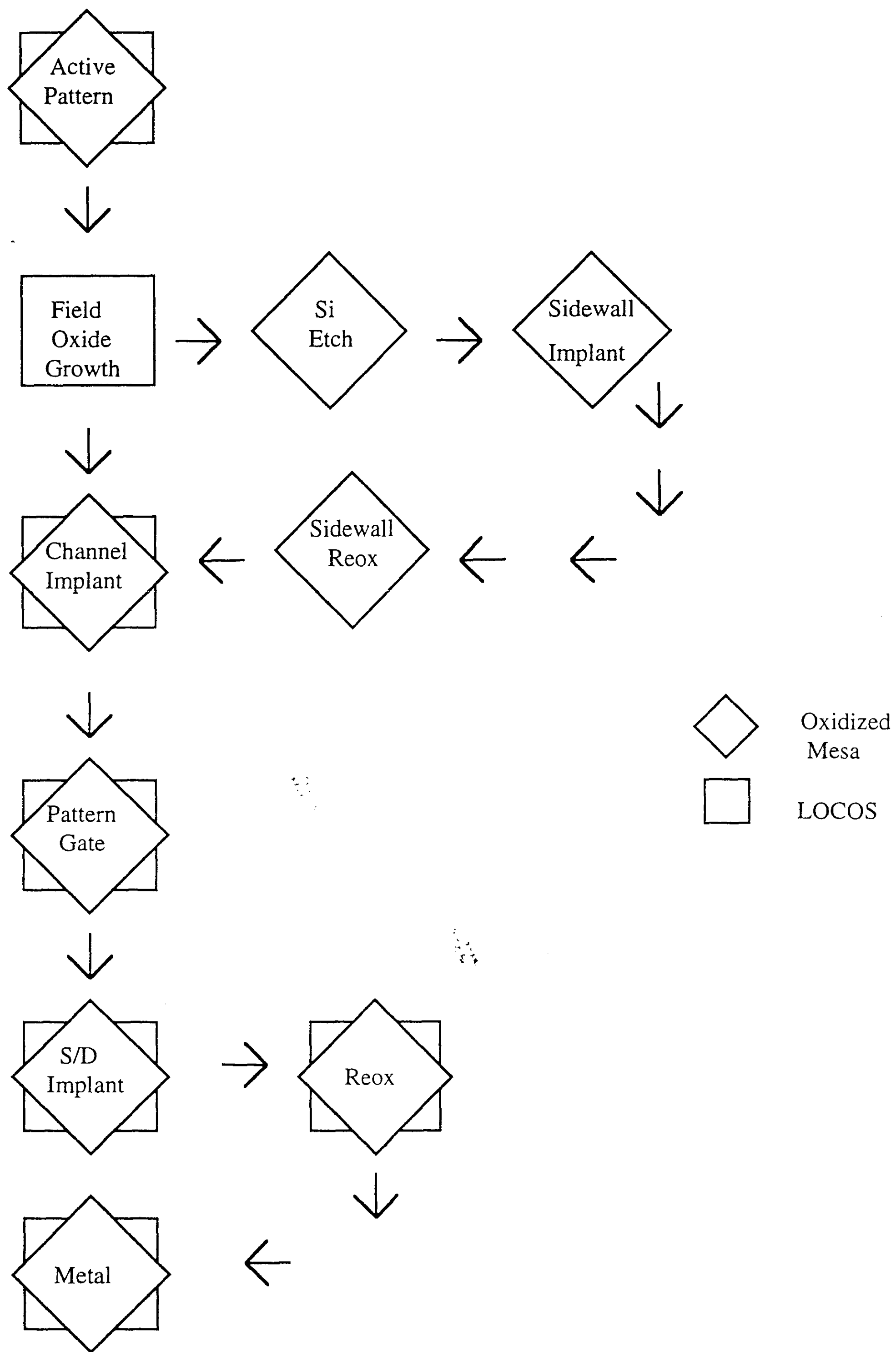
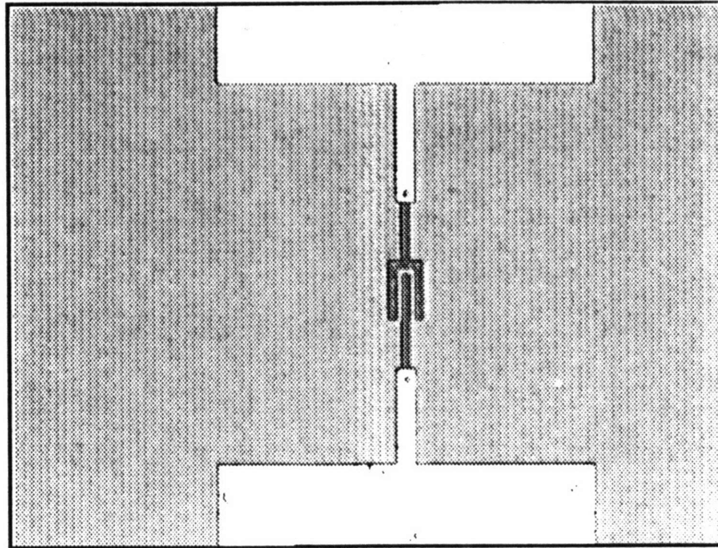
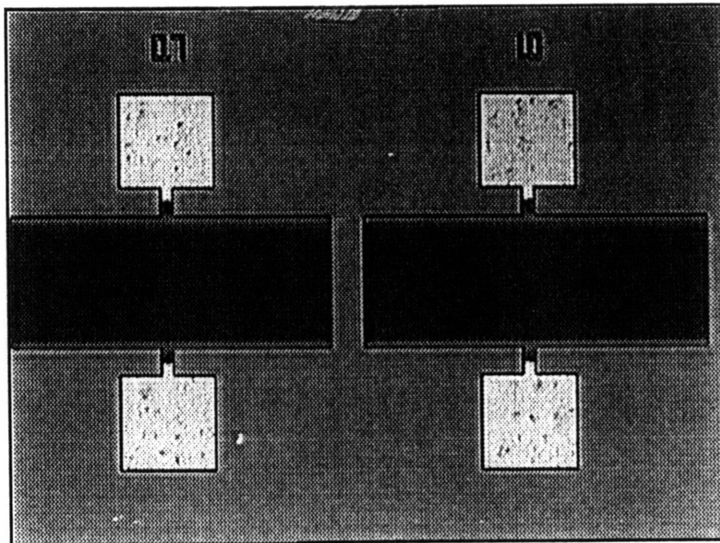


Figure 12: Process Flow Diagram

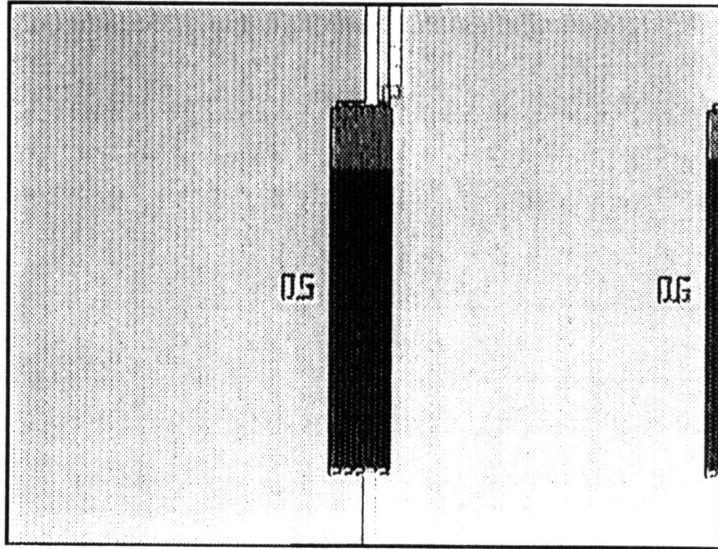


Three Finger Isolation Structure: 5.0μm spacing

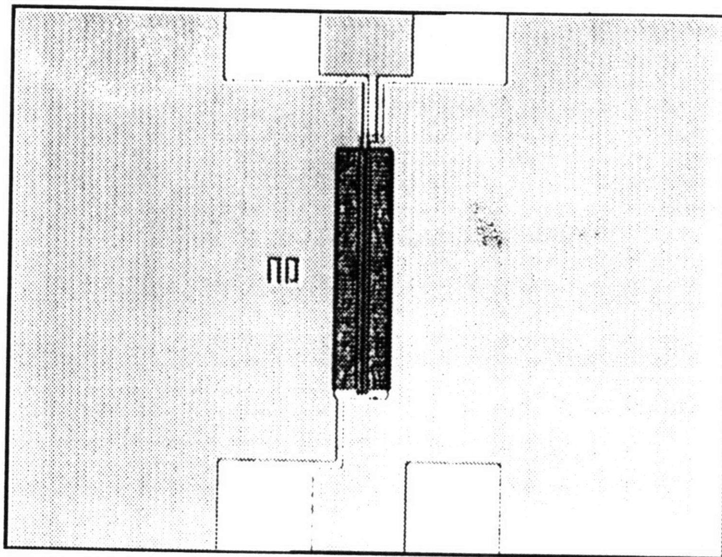


Medium Sized Interdigitated Fingers Isolation Structure: 0.7μm and 1.0μm spacing

Figure 13



Sidegating Structure: 0.5μm Field Spacing Between Active Areas



Small Sized Comb Diode

Figure 14

Chapter IV
Simulation of LOCOS Field Oxidations

4.1 Introduction

This chapter introduces the program used to simulate the LOCOS field oxidations for the experiment and explains the various options and parameters available for use in the simulation process.

4.2 TSUPREM-4

TSUPREM-4 is a computer program for simulating the processing steps used in the fabrication of integrated circuits and discrete devices. It is capable of modeling ion implantation, inert ambient drive-in, epitaxial growth, silicon and polysilicon oxidation, and low-temperature deposition and etching of various materials. The incorporation and redistribution of impurities is simulated in a two-dimensional cross section of the silicon wafer. Provided in the output of the program are the boundaries of the various material layers in the structure, the distribution of impurities in each layer, and the stresses produced by oxidation, thermal cycling, and film deposition[22]. For this experiment, focus was placed on those steps and parameters used to simulate the field oxidations of the LOCOS splits to determine appropriate oxidation times. Cross sections of the structure after oxidation were generated to determine the effectiveness of the oxidation, i.e., whether the silicon film was oxidized completely down to the BOX.

4.3 Simulation Procedure

The procedure for simulating field oxidations consisted of generating the input "stack" or file, which defines the initial silicon substrate and lists the fabrication steps to be simulated, and the actual TSUPREM-4 simulation of the input file. Initializing the substrate is done with TSUPREM-4 device-structure specification statements [22]. For bulk simulation the "mesh" statement along with the "grid.fact" parameter is the simplest method of defining the silicon substrate. This statement produces a rectangular, grided structure representing the wafer cross section. Due the fact that SOI wafers have two silicon regions separated by the BOX, the substrate/structure definition has to be done with the "line" and "region" statements. The line statement (used in both X and Y directions) defines the rectangular structure and sets the grid. The region statements define what material lies within a specified section of the structure[22]. Figure 15 shows the statements used to initialize the structure for the input file used to simulate those wafers with a top-layer silicon-film thickness of 90nm and the grid generated for the structure. The pitch of the grid is set with the "spacing" parameter. The top-layer silicon layer is located between y=0μm and y=0.11μm. The BOX is located between y=0.11μm and y=0.5μm, and the region below y=0.5μm is the handle wafer.

The fabrication processes modeled by TSUPREM-4 are approximated numerically using finite-difference and finite-element solution techniques. The solutions are calculated at the nodes of each triangle created by the grid; therefore, it is advantageous to have a denser grid in the top layer silicon film and at any "important" boundary consisting of two different materials as this gives more accurate simulation results. x=1.0μm is the center point of the nitride window where the field oxide is grown. The final step in defining the simulation structure was the initialization of the substrate background impurity concentration and the crystal orientation.

Figure 15 shows that the wafers used in the experiment had a background concentration of 1E15 Boron and a <100> crystal orientation. The remainder of the input

stack consists of the process steps to be carried out in the simulation program. Once the structure was defined, the isolation mask (stress relief oxide and nitride layers) was specified, and thermal oxidation was done using the "method" an "diffuse" statements. The method statement specifies the oxidation model the program will use, and the latter sets the diffusion parameters (time, temperature, oxidation type). The "deposition" statement along with its parameters, thickness and spaces, deposited the nitride layer of a specified thickness and set the grid for the layer. The nitride layer was etched in the field region with the "etch" statement, which selectively etched the specified material in particular sections of the structure[22]. Next the field oxide was grown by using the method and diffuse statements once more. Figure 16 shows the input stack that defines the structure to have a top layer silicon film thickness of 90nm, grows a 35nm stress relief oxide, deposits and selectively etched a 100nm nitride layer, and performs a 5 minute dry oxide at 1050°C. The resulting structure was used as the initial structures in the input stack that performed the field oxidation simulations for the wafers with various top silicon film and stress relief oxide thicknesses.

```
line x location=0 spacing=0.05 tag=left
line x location=0.5 spacing=0.05
line x location=1.0 spacing=0.01
line x location=1.5 spacing=0.05 tag=right

line y location=0 spacing 0.01
line y location=0.11 spacing=0.01 tag=boxtop
line y location=0.50 spacing=0.05 tag=boxbottom
line y location-1.0 spacing=0.1 tag=bulkbottom

region oxide xlo=left xhi=right ylo=boxtop yhi=boxbottom
region silicon xlo=left xhi=right ylo=boxbottom yhi=bulkbottom
init boron=1e15 <100>
```

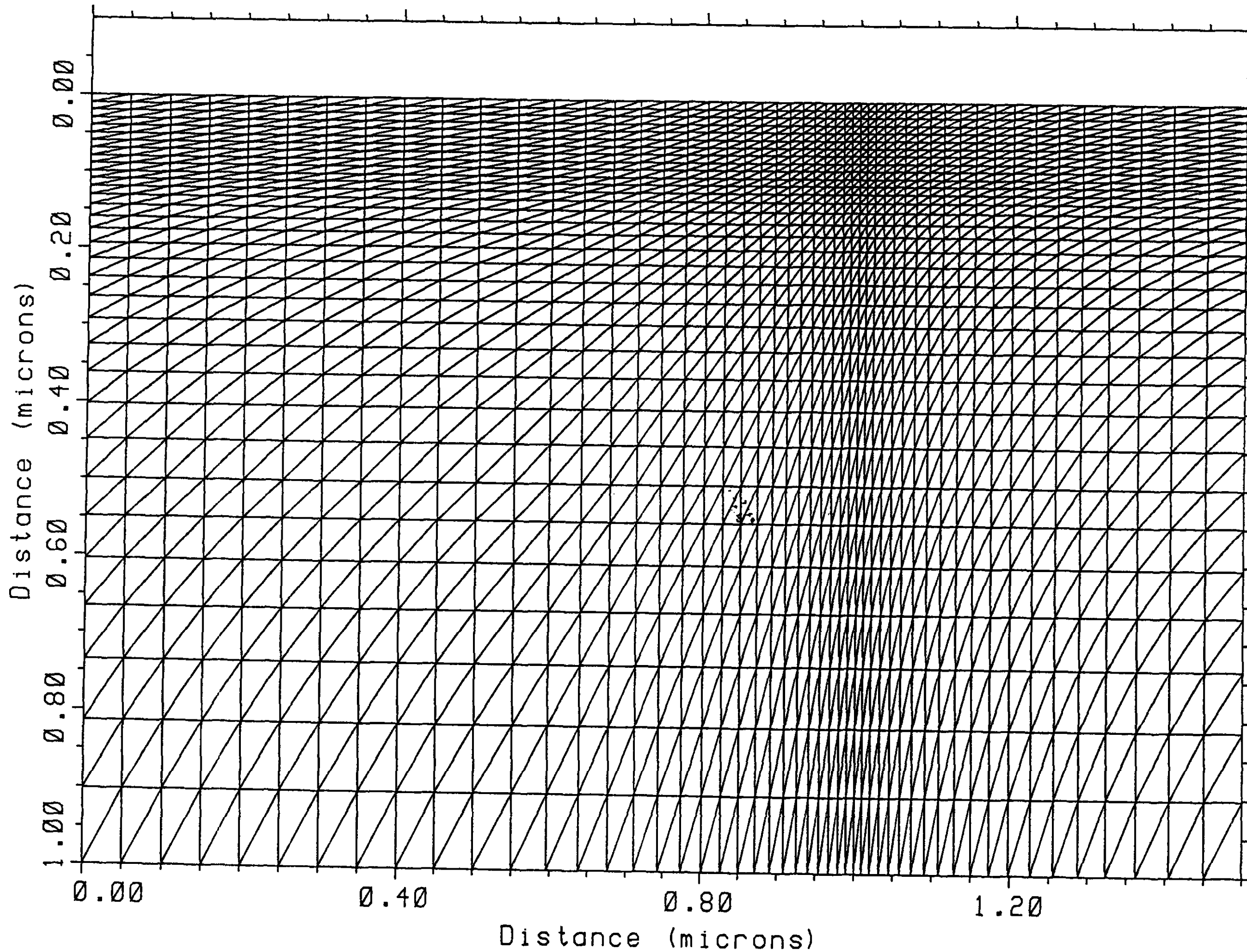


Figure 15: Statements Used To Generate Grid And Grid

```
$ Setup SOI substrate, initialize grid
line x location=0 spacing=0.05 tag=left
line x location=0.5 spacing=0.05
line x location=1.0 spacing=0.01
line x location=1.5 spacing=0.05 tag=right

line y location=0 spacing 0.01
line y location=0.11 spacing=0.01 tag=boxtop
line y location=0.50 spacing=0.05 tag=boxbottom
line y location-1.0 spacing=0.1 tag=bulkbottom

region oxide xlo=left xhi=right ylo=boxtop yhi=boxbottom
region silicon xlo=left xhi=right ylo=boxbottom yhi=bulkbottom
init boron=1e15 <100>

$ Grow Stress relief oxide----350A
method vertical dy. oxide=0 grid.oxi=4 init=0.15
diffuse temp=1000 time=4 dryo2

$ Deposit nitride layer----1000A
deposition nitride thick=.1 spaces=2
etch nitride right p1.x=0.8

$ Use compress model to perform 5min dry oxidation
method compress grd.oxi=4 init=0.15
diffuse temp=1050 time=5 dryo2
structure outfile=simox900-350.5dryc
stop
```

Figure 16: Model TSUPREM-4 Input Stack

4.4 TSUPREM-4 Oxidation Models

4.4.1 Oxidation Theory

Oxidation in TSUPREM-4 is based on the theory of Deal and Grove[22]. The flux of oxidant (either O_2 or H_2O) from the bulk of gas of the oxide/gas interface is given by

$$F=h(C^*-C_O) \qquad (4.4.1)$$

where h is the gas-phase mass-transfer coefficient, C_O is the concentration of oxidant at the oxide surface, $C^*= Hp_g$, H is Henry's Law constant and p_g is the partial pressure in the oxidant in the bulk gas. The flux of oxidant in the oxide is

$$F=D(C_o-C_i)/y \qquad (4.4.2)$$

where d is the diffusivity of the oxidant in the oxide, C_i is the concentration if the oxidant at the oxide-silicon interface, and y is the thickness of the oxide. The rate of the oxidizing interface is

$$F=k_sC_i \qquad (4.4.3)$$

where k_s is the chemical surface-reaction rate constant for the oxidation. Solving the equations gives

$$N(dy/dt)=F= k_sC^*/(1 + k_s/h + k_sy/D) \qquad (4.4.4)$$

where dy/dt is the oxide growth rate and N is the number oxidant molecules per cubic centimeter available for the oxidation. Equations (4.4.1)-(4.4.4) solved one dimensionally, gives

$$y^2+Ay-B(t-\tau)=0 \qquad (4.4.5)$$

where $A\equiv 2D\ (1/k_s + 1/h)$, $B\equiv 2DC^*/N$, and $\tau \equiv (y_o^2 + Ay_o)/B$. y_o is the amount of oxide grown prior to oxidation. A and B are expressed in terms of the linear and parabolic rate constants B/A and B, respectively[22,23].

TSUPREM-4 uses both analytical and numerical oxidation models. The analytical models, ERF1, ERF2, and ERFC models, are designed for very fast and rough simulation of basic structures. These models are limited to structures which are planar and may be covered by an oxide layer. When using these oxidation models, all oxidation masking layers present on the initial structure are ignored. Due to the topography of the wafer surface after nitride patterning, the analytical models are insufficient for simulating

LOCOS field oxide growth. The numerical oxidation models, VERTICAL, COMPRESS, and VISCOUS are designed to accurately simulate any structure, regardless of the surface topography or oxidation masking layers. Using equations (4.4.1)-(4.4.4), these models calculate the oxide growth rate at every point of the oxide/silicon interface[22]. The difference in the numerical models lies in the method in which the oxide flow caused by volume expansion is calculated. The VERTICAL model, the least complex and least accurate of the three, was used to simulate the growth of the stress relief oxide due its speed and the planarity of the structure surface at the time of this processing step. The COMPRESS model, the second simplest, and the VISCOUS model, the most complex and most accurate, was used in the simulation of the field oxidation where the structure topography was not planar due to the presence of the nitride oxidation mask.

4.4.2 COMPRESS Model

The COMPRESS model simulates the viscous oxide flow during oxidation. The movement of the oxide-silicon interface across the structure is two dimensional, and the variation of the crystal orientation is accounted for when the oxidation rate is calculated. The model uses the finite-element solutions approach (with three nodes per triangle) to offer speed in the calculations. Defining a very dense grid when using this model increases the simulation time, as there are more triangles present in the structure; however, more accurate results are obtained. In order for the model to remain numerically well-behaved, a small amount of compressibility is allowed. Due to this, as well as the simple approach to performing calculations, the COMPRESS model cannot be used to calculate accurate values of stress[22].

The COMPRESS model was used to determine the approximate oxidation times needed for the experiment. Once the time it took for the field oxide to just reach the BOX was determined, the percent over oxidation was calculated and simulated to generate the

cross sectional profiles for the structures. Figure 17 shows the input stack used to grow the field oxide using the COMPRESS model. The time listed in the input stack is that needed for the 10% over oxidation for wafer 1. The "initialize" statement with the in.file parameter specifies the structure with a structure file generated with the input stack in figure 16. The method statement was used as before to determine the model to be used in the oxidation. Once the oxidation was performed, the output structure was then saved for future reference and cross section generation.

```
$ Initialize structure with presaved structure
initialize in.file=simox900-350.5dryc

$ Choose oxidation model and perform oxidation
method compress grid.oxi=4 init=0.15
diffuse temp=1050 time=18 weto2

$ Save output structure
structure outfile=simox900-350.18c
```

Figure 17: COMPRESS Model Input File

Figure 18 shows a graph of remaining top layer silicon versus oxidation time for each of the top layer silicon/stress relief oxide thicknesses combinations, i.e., 90nm/35nm, 90nm/10nm, 50nm/35nm, and 50nm/10nm. This graph accurately shows that the COMPRESS model does not account for stress in its calculations. This is evident from the linearity of the plots. The curves would become more parabolic as the oxidation increased due the stress that develops in SOI substrates as the last section of top layer silicon is oxidized. Figures 19 through 22 show the sections for wafers 1-4, respectively. The width of the nitride window is 0.4μm for all structures.

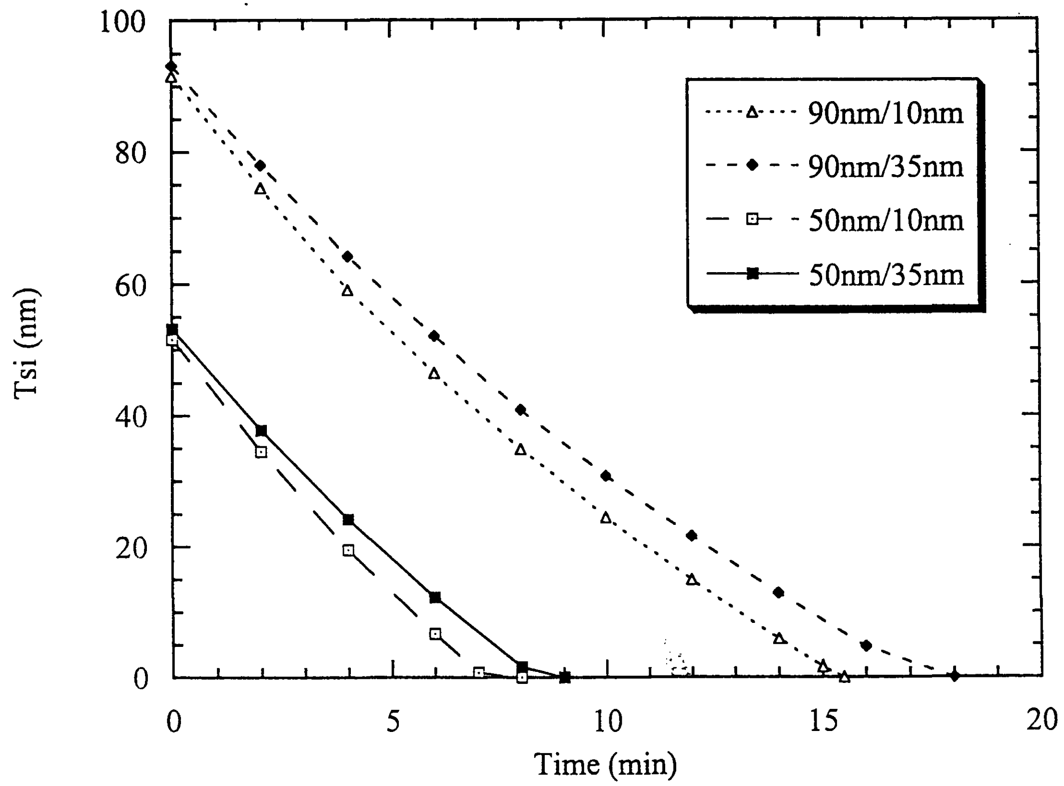


Figure 18: Graph, Remaining Top Layer Si vs Oxidation Time (Compress Model)

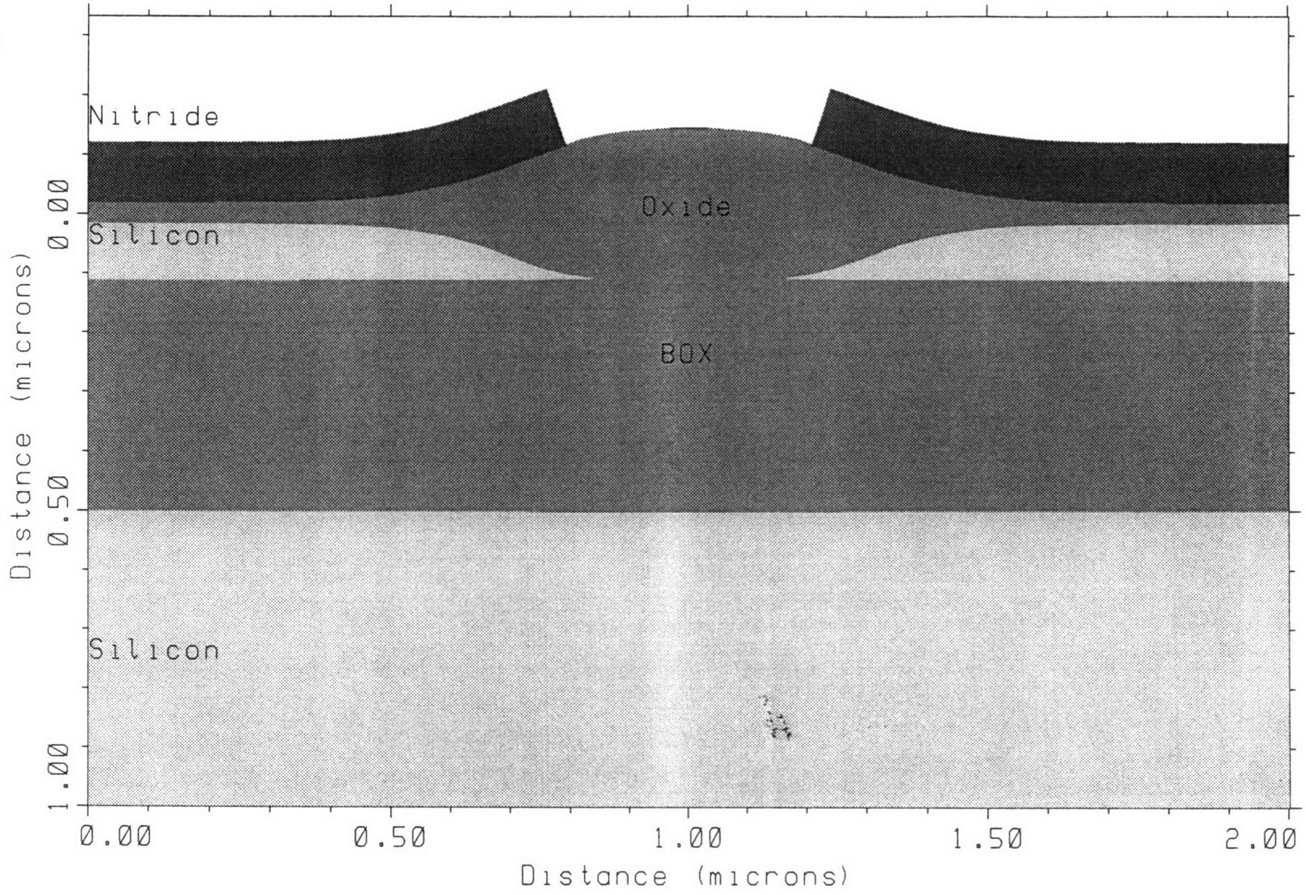


Figure 19: Cross Section For Wafer 1, (10% Over Oxidation, COMPRESS Model)

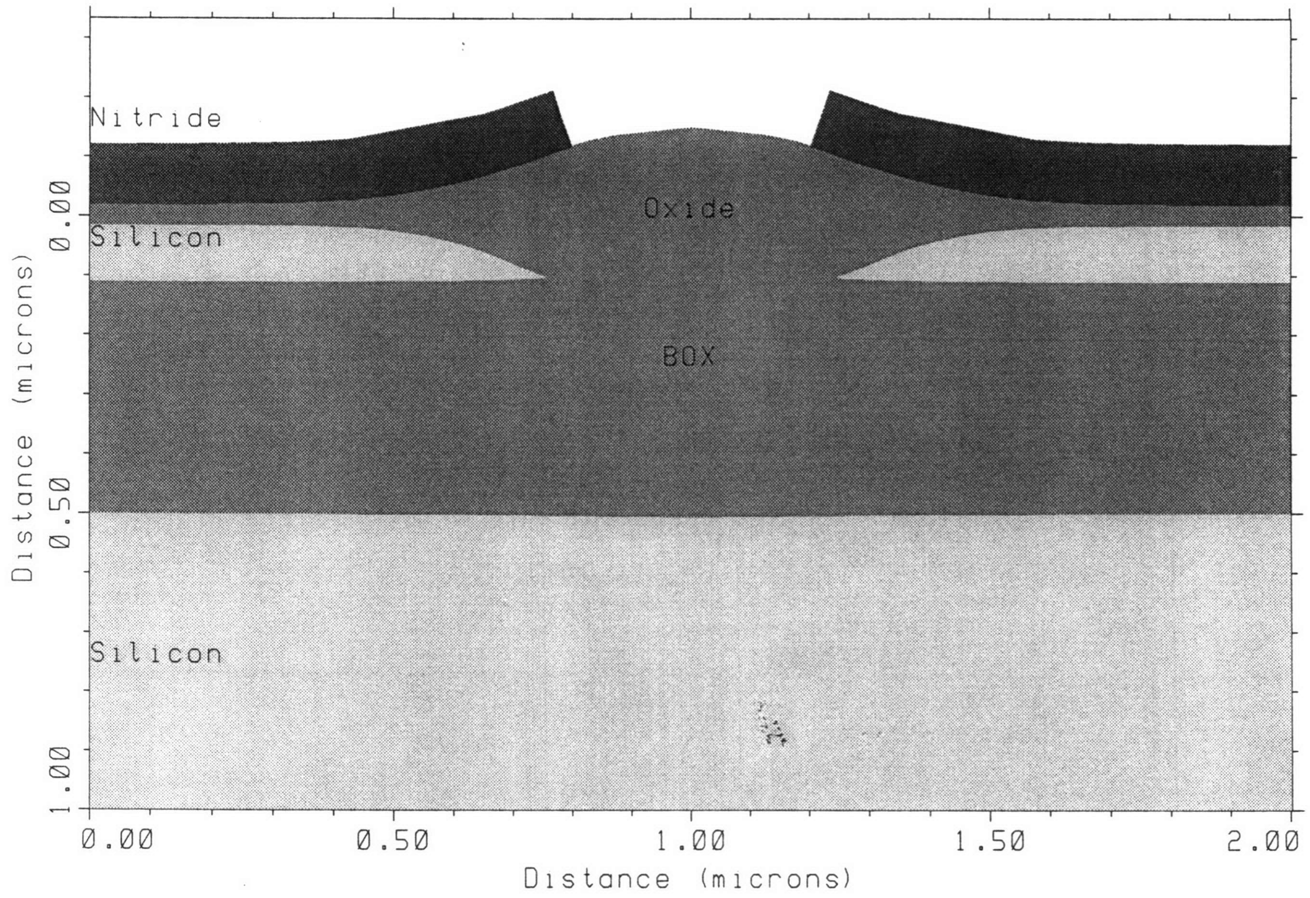


Figure 20: Cross Section For Wafer 2, (20% Over Oxidation, COMPRESS Model)

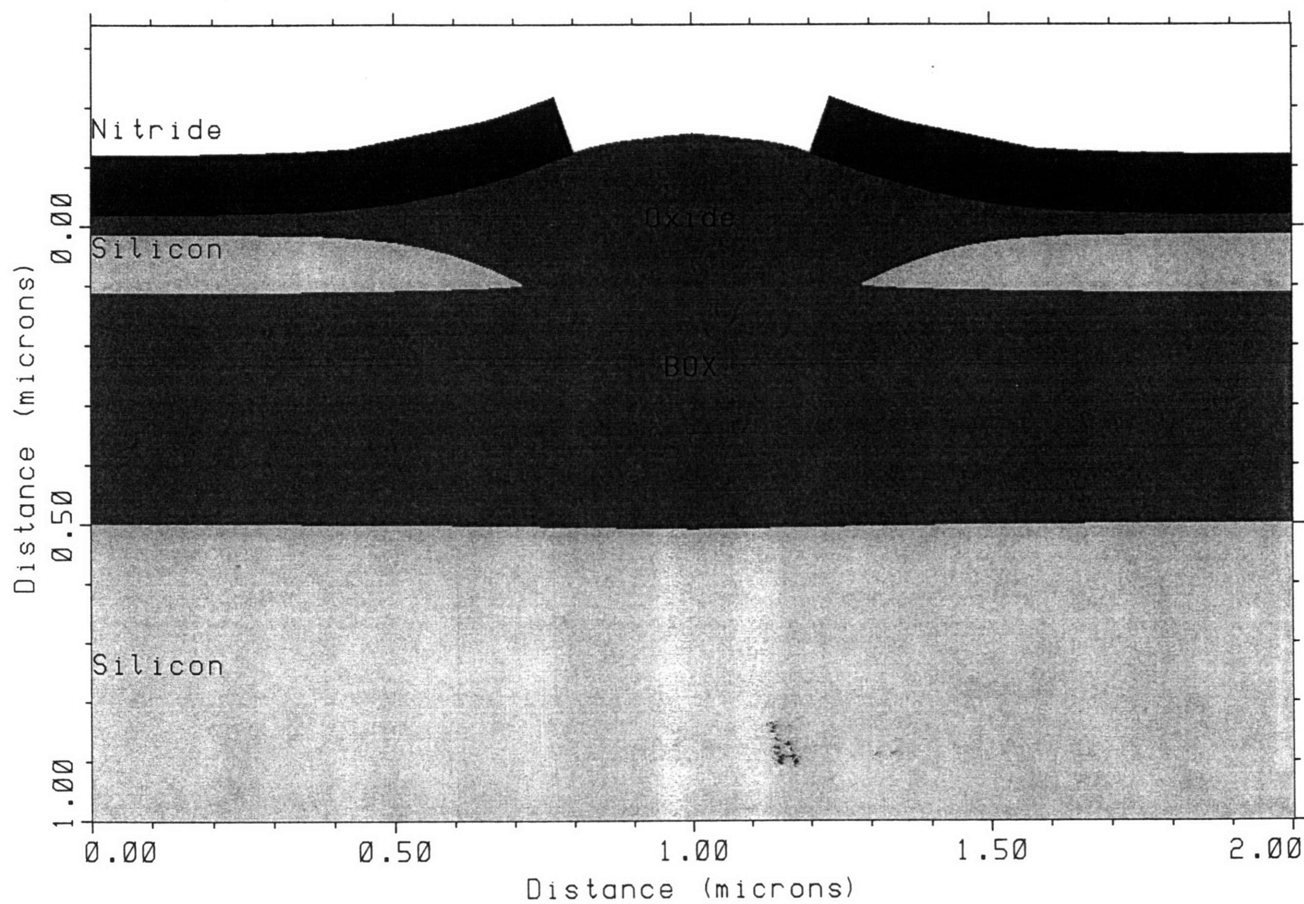


Figure 21: Cross Section For Wafer 3, (30% Over Oxidation, COMPRESS Model)

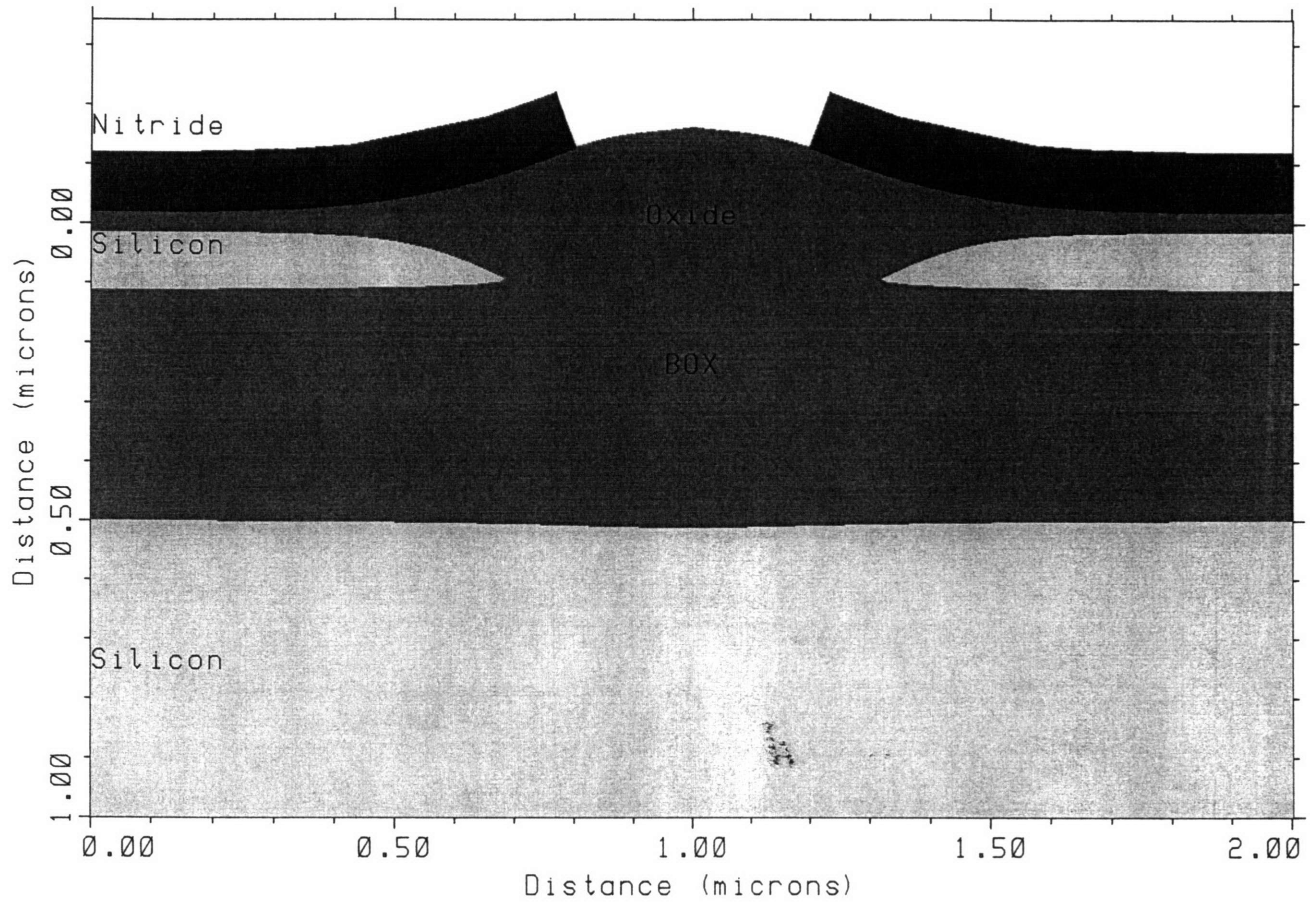


Figure 22: Cross Section For Wafer 4, (40% Over Oxidation, COMPRESS Model)

4.4.3 VISCOUS Model

The VISCOUS model is similar to the COMPRESS model in that it simulates the two dimensional, viscous flow of oxide during oxidation. It uses 7 nodes to perform calculations making it considerably slower than the COMPRESS model; however, it gives more accurate results. Although the VISCOUS model uses the same approach to calculating oxidation rates, a different set of parameters are used to take in account stress effects on oxidation[22].

The parameters used in the VISCOUS oxidation model are visc.o, visc.e, and visc.x for the "material" statement. These parameters are the exponential prefactor for viscosity, the activation energy for viscosity, and the incompressibility factor for a specified material, respectively. Parameters for the "ambient" statement are Vc, Vr, Vt, Vd, and stress.d. Vc is the activation volume for the dependence of oxide viscosity on shear stress. Vr and Vt are the activation volumes for the dependence of the surface reaction rate on normal and tangential stresses, respectively. Vd is the activation volume for the dependence on pressure of the diffusivity of the oxidizing species in the oxide. stress.d determines whether the stress dependence of oxidant diffusivity, surface reaction rate, and oxide viscosity are included when using the VISCOUS model. Default values of these parameters for each material present during oxidation are provided by TSUPREM-4. These values give realistic results without stress dependence; however, the values should be changed to model stress during oxidation.

Figure 23 shows the input file used to obtain more accurate oxidation results. The parameter values in the input file were determined based on findings of Crowder[15]. The overall effect is to make the materials present during oxidation more viscous. Figures 24 through 27 show simulation cross sections for wafers 1-4 using the VISCOUS model. The rigidness of the nitride layer and the presence of the silicon filament shows that stress is more accurately modeled by the VISCOUS model. The remaining simulation cross sections for wafers 5-12 are shown in Appendix B.

```
$ Initialize structure with presaved structure
initialize in.file=simox900-350.5dryc

$ Choose oxidation model and perform oxidation
method viscous grid.oxi=4 init=0.15
ambient Vc=722 Vr=12.5 Vd 65 stress.d weto2
material oxide visc.o=3.13e13 visc.3=-2.74 visc.x-0.499
material nitride visc.o=2.94e14
material silicon visc.o=2.94e16
diffuse temp=1050 time=18 weto2

$ Save output structure
structure outfile=simox900-350.18c
```

Figure 23: VISCOUS Model Input File

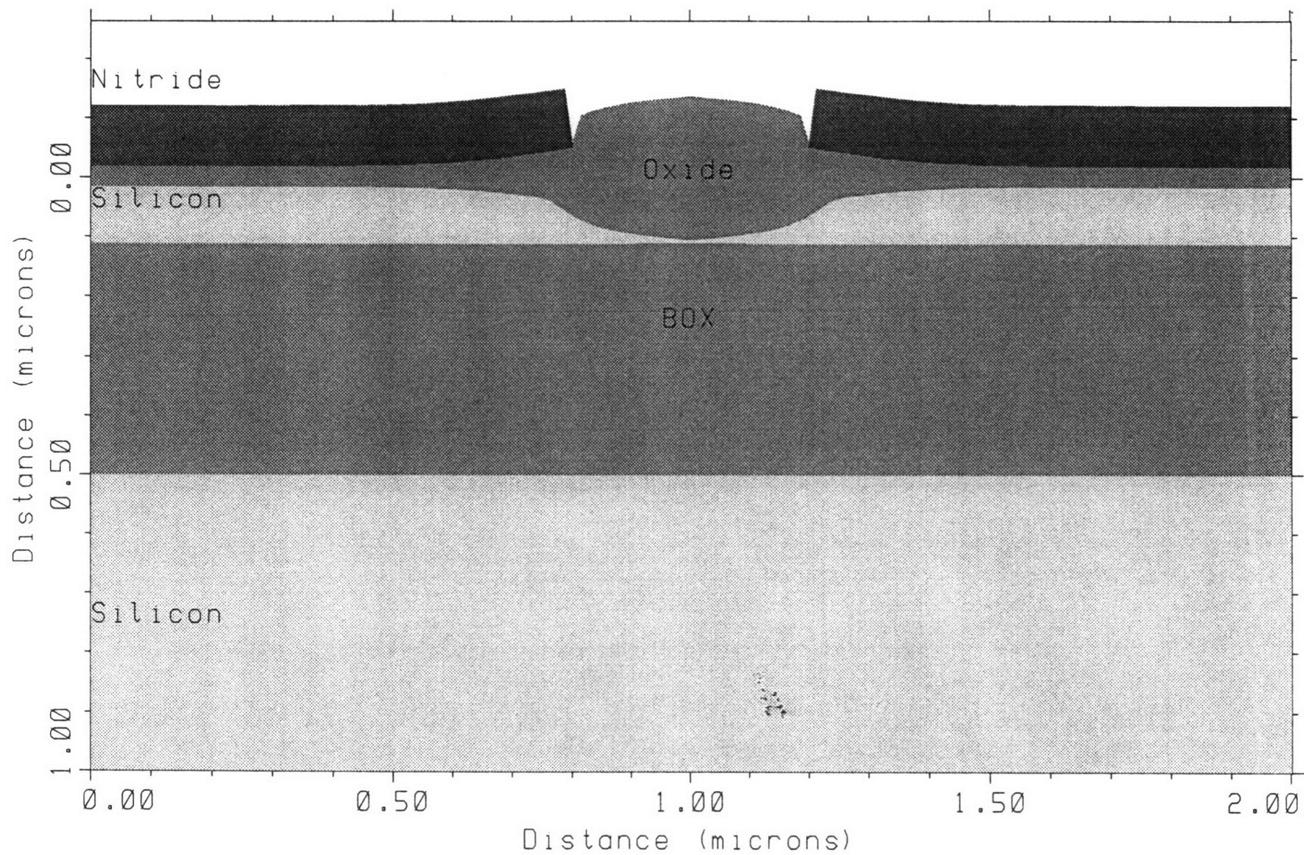


Figure 24: Cross Section For Wafer 1, (10% Over Oxidation, VISCOUS Model)

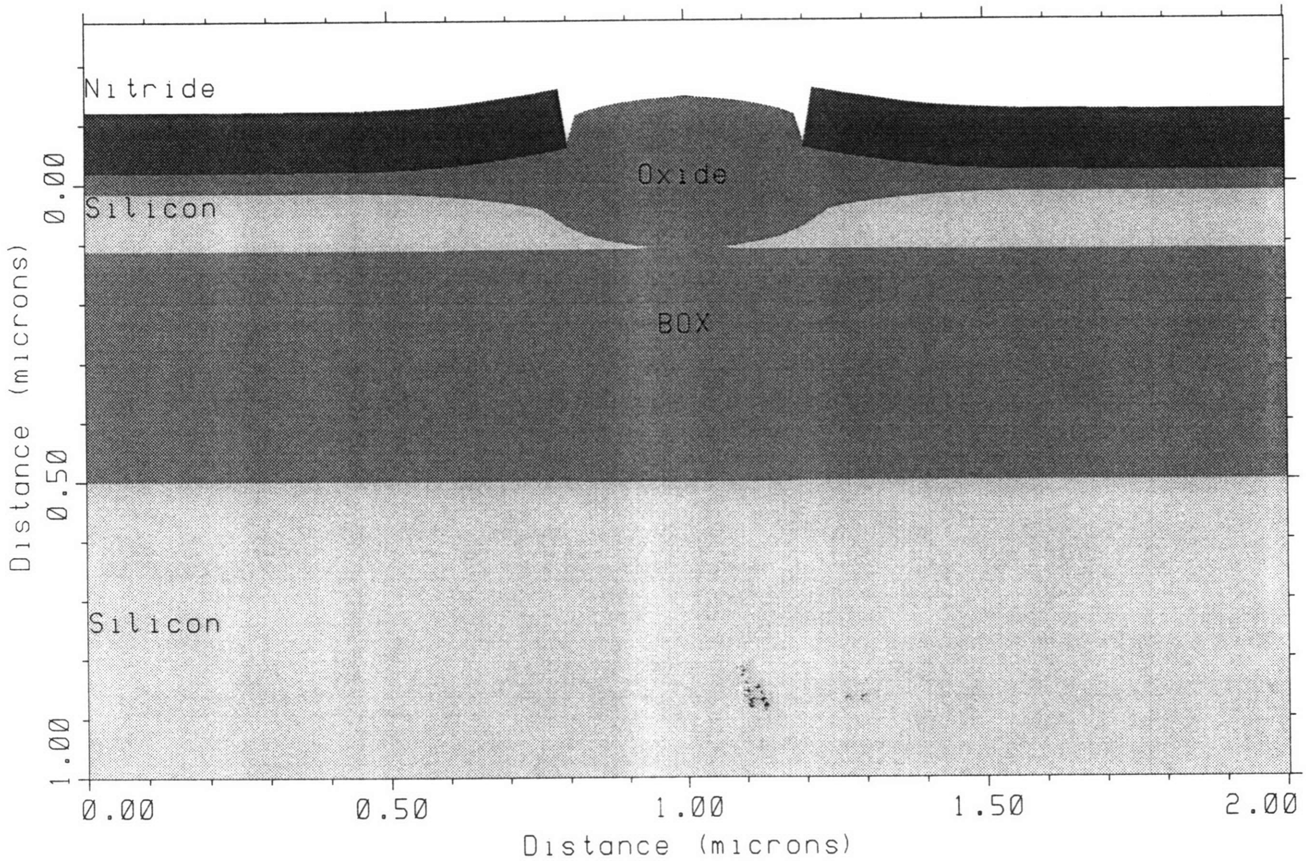


Figure 25: Cross Section For Wafer 2, (20% Over Oxidation, VISCOUS Model)

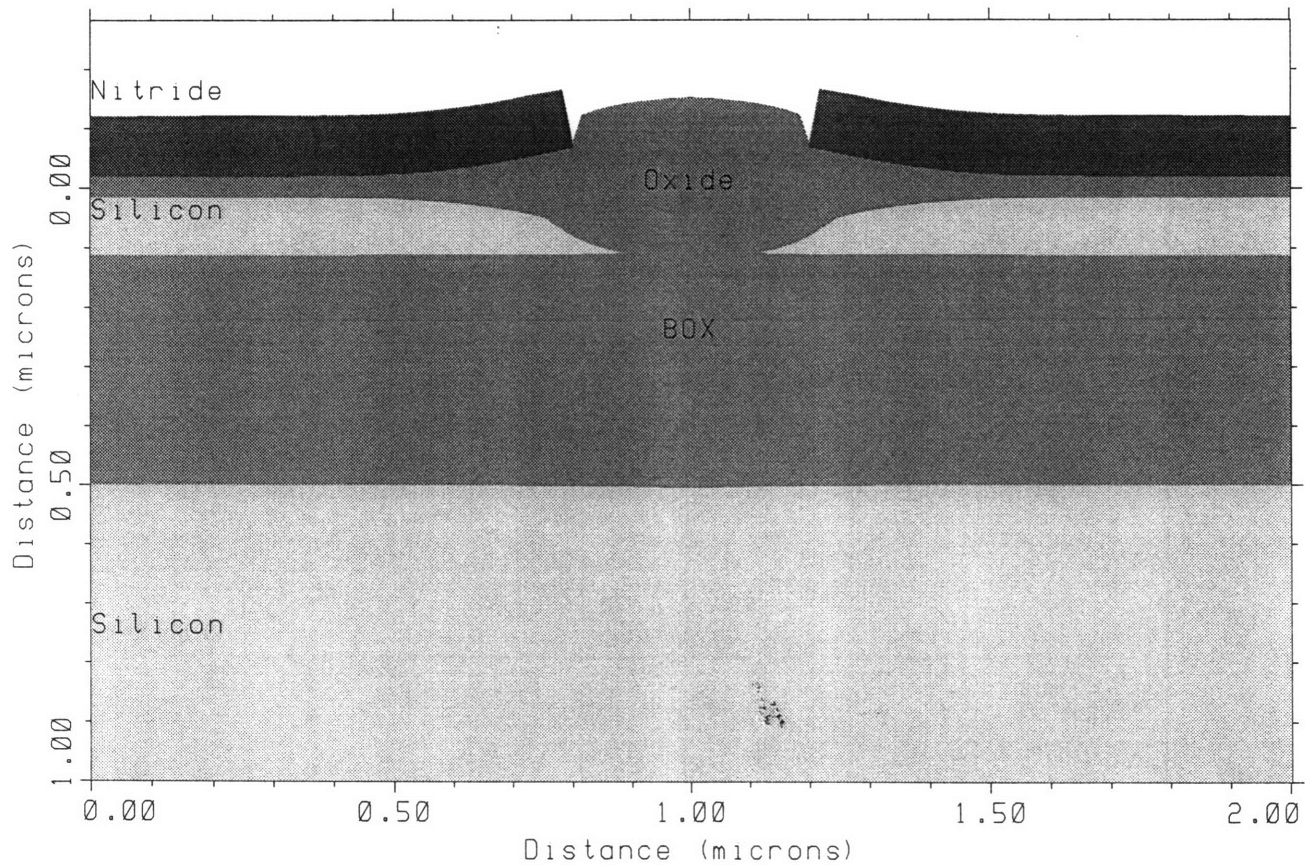


Figure 26: Cross Section For Wafer 3, (30% Over Oxidation, VISCOUS Model)

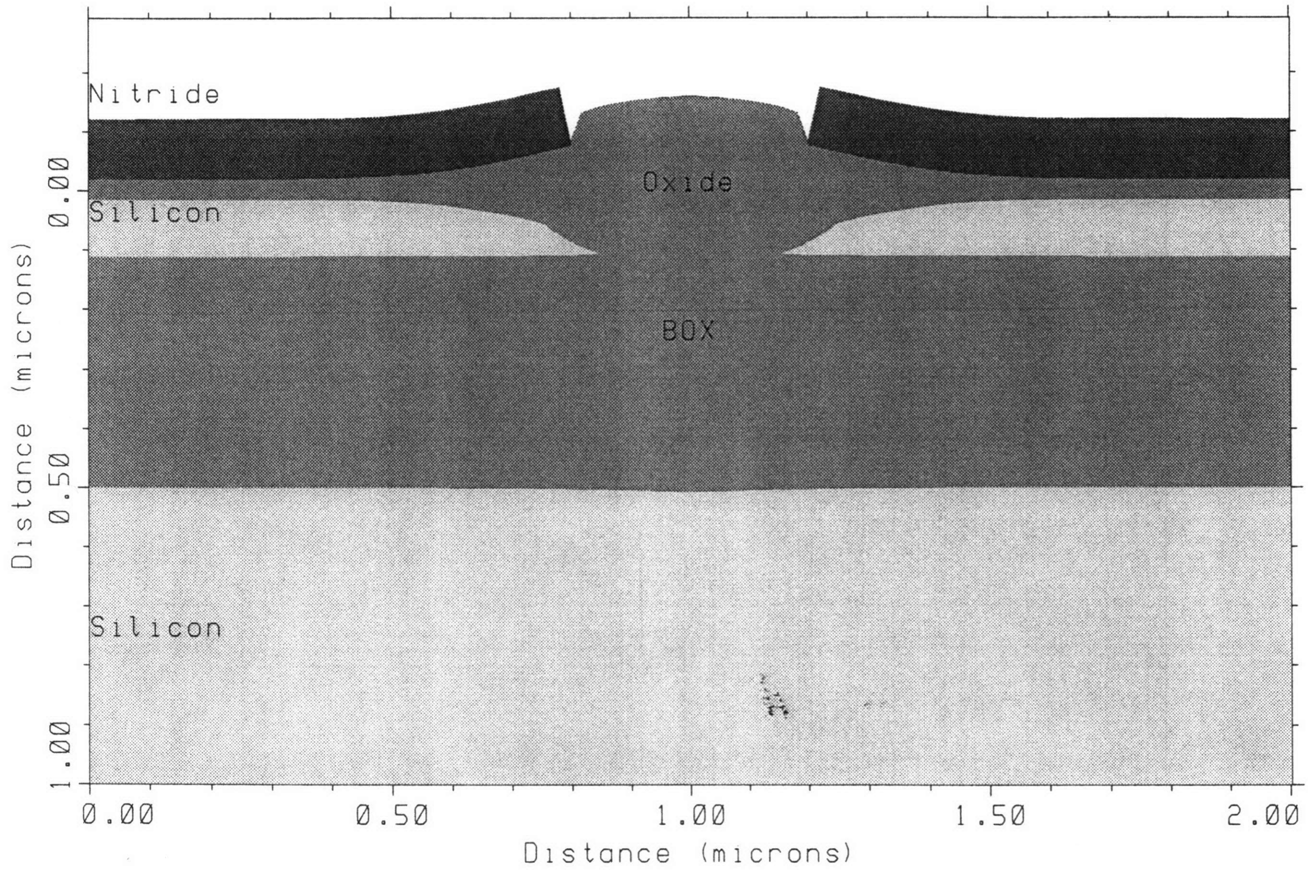


Figure 27: Cross Section For Wafer 4, (40% Over Oxidation, VISCOUS MODEL)

Chapter V
Testing & Results

5.1 Introduction

This chapter begins by describing the purpose of the specified testing, the test procedure, and test setup. Next the results of the testing and data analysis are presented, and TSUPREM-4 simulation results are compared with the electrical data.

5.2 Testing

5.2.1 Focus

The aim of the testing was to gather data from the simplest structure and begin isolation characterization with it. The simplest test structure was the isolation islands which were used to characterize LOCOS isolation. The basic form of the isolation islands, that was used in the testing, was the simple two-finger structure. The varied sizes and dimensions of the structure were designed and fabricated to have an adequate supply of test structures if characterization was not possible with the two finger structures alone.

5.2.2 Setup

A HP 4145B Semiconductor Parameter Analyzer was used to perform the measurements. The isolation islands consisted of three terminals, the two n+ silicon islands and the substrate silicon of the SOI wafers. For notation, one island was labeled

"S" for source, the other was labeled "D" for drain, and the substrate silicon, "B" for bulk or back gate. For preliminary testing, V_s was set to ground and V_d was swept from -20v to 20v, while V_b was stepped from -50v to 50v. Plots of I_{ds} vs V_{bs} at constant V_{ds} showed substantial BOX leakage current. I_{bs} reached a minimum of 10na at V_{bs}=-20v and a maximum of 1ma at V_{bs}=50v; this effect was observed with some of the LOCOS wafers. As a means to confirm actual BOX leakage, the same measurement was performed on isolation structures fabricated using Oxidized Mesa isolation; the effect was not observed. Further inter-wafer investigation of the electrical characteristics of the LOCOS structures led to the conclusion that random pipes existed in the BOX. These pipes explained the random presence of the I_{bs} for those wafers in which the field oxide did not reach down to the BOX. In order to measure the leakage current between the two islands, terminal B was defined as a current source set at a constant current of 0a. In this manner V_b would float to keep I_{bs} constant at 0a. The isolation structures were then each viewed as a two-terminal structure having terminals, S and D. Actual data measurements were performed by keeping terminals B and S as mentioned above and sweeping V_d from -50 to 50v.

5.3 Results

In order to analyze the gathered data, series of plots having I_{ds} as the dependent variable and either V_{ds} or the various process and structure parameters as the independent variables were made. General observations for I_{ds} were that it decreased with an increase in % over oxidation, SRO thickness, field spacing, and field-implant dose. The island field spacing represented in most plots is 0.4µm. This field spacing was chosen due to its maximum leakage potential. For a given set of process parameters, the structure with this

field spacing would leak more than a structure with a greater field spacing. When this structure is isolated, it is assumed that structures with a greater field spacing will be isolated as well. When plotting I_{ds} vs V_{ds}, V_{ds} was swept from 0v to 50v in the plots to show the leakage characteristics beyond the normal chip operating voltages.

To eliminate the confusion of interpreting raw-data plots, graphs of the allowable isolation design space were created from the raw-data plots. In generating the design space, the trends of the data were used to outline the design constraints. In most instances, the leakage-current behavior was "digital" in nature. That is, leakage was either present or not present; however, in some cases, some data points did not follow these major trends. Further analysis of the data suggested that those data points not coinciding with the major trends were random glitches in the measurements, possibly originating from defects in the wafers or due to statistical variation in the actual processing. The raw-data plots used to create the design-space graphs are available in Appendix C for further review.

5.3.1 T_{si} Effects

As mentioned in Chapter III, two different top-layer silicon thicknesses were used in the experiments, 50nm and 90nm. Within each t_{si}/split, there were two SRO thicknesses, 10nm and 35nm. Wafers 1-4 had a t_{si}/SRO combination of 90nm/35nm, wafers 5-8 had 50nm/35nm, and wafers 9-10 and 11-12 had combinations of 90nm/10nm and 50nm/10nm, respectively. Note: The starting t_{si} of the structures was slightly greater than the final nominal value due to the extra silicon consumed during device fabrication.

Defining leakage current as $I_{ds} \geq 50pA$ per 100µm of island edge, the wafers having a t_{si} of 50nm revealed no leakage current for either t_{si} /SRO combination.

As the field spacing between the islands is decreased below 1µm, and the SRO thickness is decreased below $1/3 \times t_{nit}$, with t_{nit}=100nm, the stress created during field oxidation increases. The effect is a decrease in the likelihood of oxidizing down to the BOX and an increase the likelihood of leakage current between the islands. No leakage current was observed for the isolation structure with a 0.4µm field spacing on either wafer 11 or 12. This suggests that a top layer t_{si} of 50nm was too thin to induce the isolation-inhibiting stress. However, leakage current was observed in several of the wafers which had a t_{si} of 90nm.

Figure 28 is the design space graph based solely upon the top-layer silicon thicknesses and % over oxidations used in the experiment. The shaded area represents the t_{si} and % over-oxidation combinations which would result in complete isolation between islands regardless of the other existing process parameters used in the experiment. For example, for a t_{si} of 90nm, an over oxidation of 40% and beyond is sufficient for complete isolation even in the case of having no field implant and a SRO thickness of 10nm. As seen in the graph, there is a large area in which the field oxidation itself is not sufficient for isolation, and optimization of other process parameters becomes necessary.

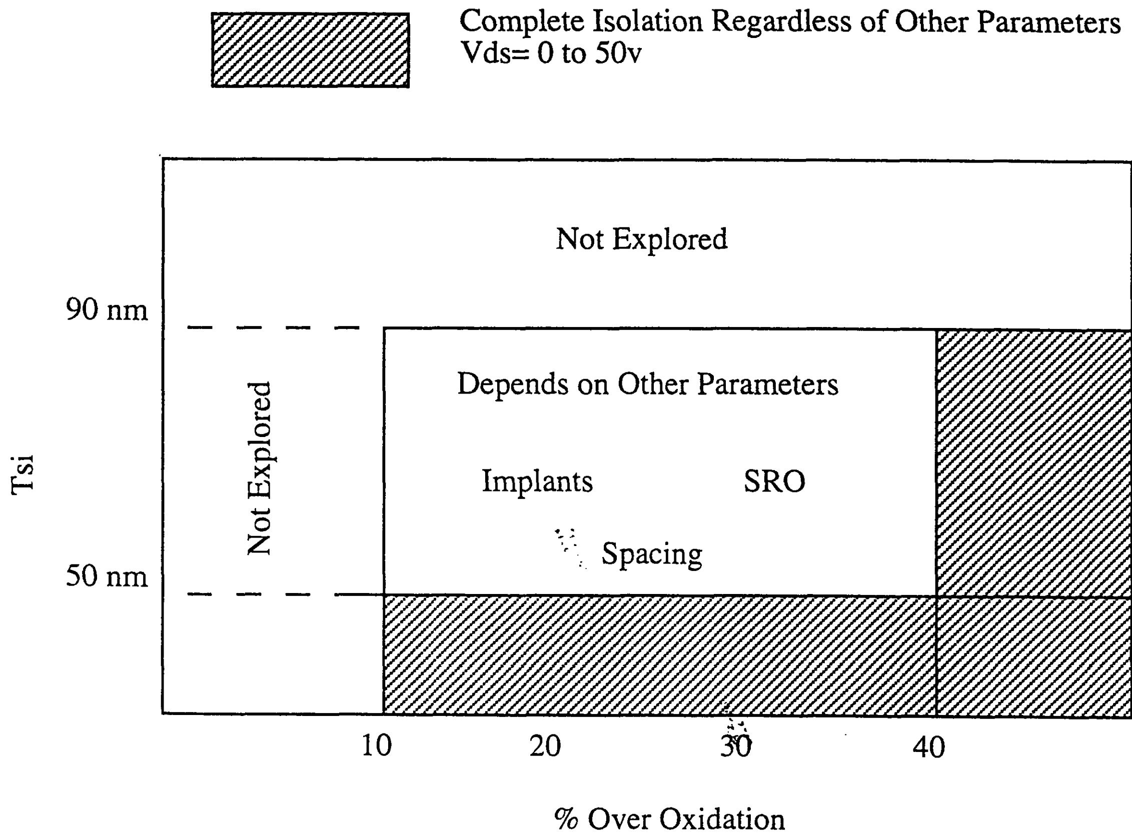


Figure 28: Design Space Graph for Tsi and % Over Oxidation

5.3.2 SRO Effects

The top-layer silicon thickness is the first variable to be examined in determining the constraints of the design space. Within the realm of each t_{si}, the next major variable is the SRO thickness. This is illustrated by the design-space graphs in figure 29. The SRO thickness is on left side of the graphs, while the field implants are on the right side. The region labeled "Gray Zone" is where the digital nature of the leakage ceased. Wafers are represented by the different % over oxidations and SRO combinations. Implants represent different die across an individual wafer.

As mentioned above, differences in the SRO had no effect in the case of t_{si}=50nm; all structures were completely isolated. In the case of t_{si}=90nm, complete isolation is possible by using a 35nm SRO, a 30% over oxidation, and any one of Field implants F1-F3; however, field implant F0 fails for this SRO thickness. The Gray Zone means that for the die which received field implant F0, for a given % over oxidation, the leakage was determined by the field spacing. This region was not designated as an allowable design space due to the impracticality of using LOCOS isolation techniques with no field implant, from a device point of view.

The top left region of the graph is where acceptable isolation cannot be determined by just the particular combination of % over oxidation, SRO thickness, and field implant. For a given field implant, the field spacing determines the isolation effectiveness.

If a 10nm SRO is used, a 37% over oxidation, and any one of field implants F0-F3 should be used for complete isolation. Notice that constraints for the 10nm SRO border at 27% and 37% over oxidation. These constraint lines represent wafers 9 and 10 which

were oxidized along with wafers 2 and 3, respectively. Due to the t_{si} of wafers 9 and 10 before the field oxidation, they received a slightly greater % over oxidation than wafers 2 and 3. The space labeled "Not Explored" is a design region in which there was no data. There were only two wafers dedicated to the 90nm/10nm t_{si}/SRO combination. The region labeled "Dead Zone" is where the stress induced by the presence of the 10nm SRO was not overcome by the % over oxidation. At or below 27% over oxidation, all structures leaked, regardless of the field implant or field spacing.

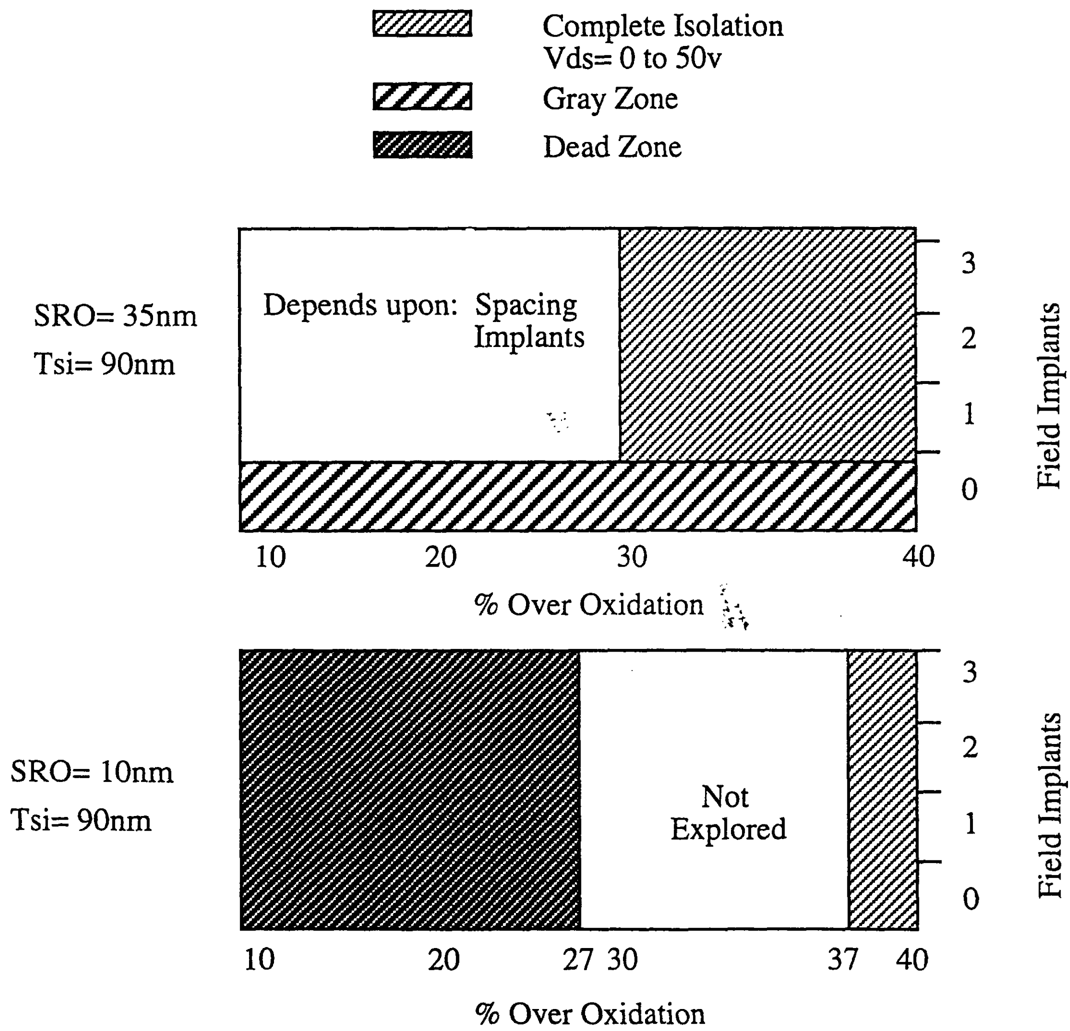


Figure 29: Design Space Graph for SRO, % Over Oxidation, and Field Implants

5.3.3 Spacing Effects

When choosing allowable design parameters to the left of the 30% constraint line for tsi=90nm and SRO=35nm, isolation is determined by the field spacing and V_{ds} for a given field implant. Figure 30 shows the design-space graph for t_{si}=90nm, SRO=35nm, % over oxidation ≥ 20%, V_{ds}=50v, and various field implants and field spacings. As stated above, the normal trend for isolation is that it increases with field spacing and implant. The graph deviates from this trends for field implant F3 when V_{ds}=50v. The darkly shaded region for V_{ds}=50v while the lighter region is valid for V_{ds}≤5v. It is not understood why this anomalous effects happened; however, it was observed that for increased V_{ds}, leakage current was higher for structures with field implant F3 than for field implant F2. See Appendix C for Ids vs Vds plots.

Figure 31 shows the design space graph for t_{si}=90nm, SRO=10nm, % over oxidation ≥ 10%, V_{ds}=5v, and various field implants and field spacings. This graph is created for V_{ds}=5v because structures of all field spacings leaked at V_{ds}=50v. Leakage was dependent upon the operating voltage for this set of parameters. It can be seen that the graph does indeed follow the trends of leakage. There was not any difference in the effects of field implants F1 and F2; however, the minimum allowable field spacing decreased to 0.9μm for field implant F3. This was attributed to increased oxidation rates due to the presence of the field implant dose in the silicon[19].

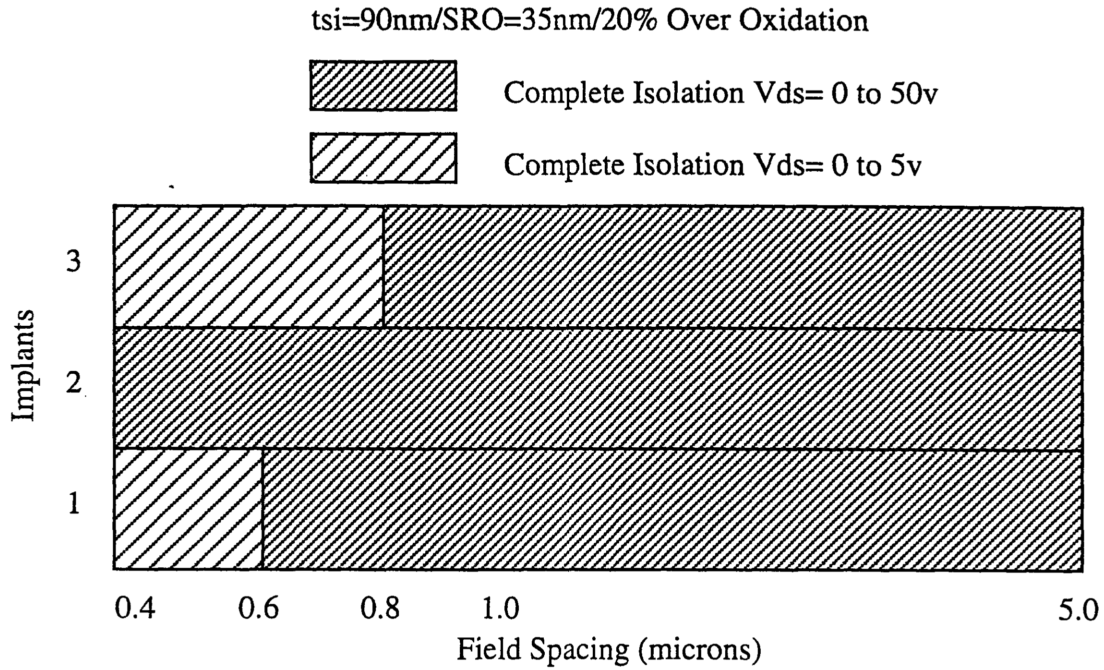


Figure 30: Design Space Graph for Field Implants and Spacings

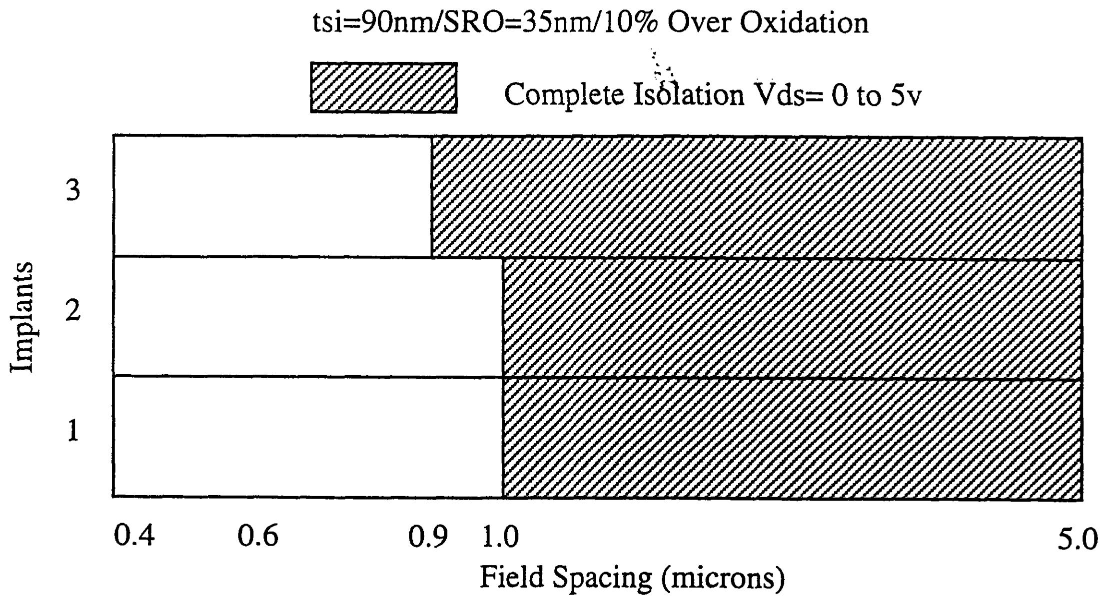


Figure 31: Design Space Graph for Field Implants and Spacings

5.4 TSUPREM-4 Comparisons

Structure cross section generated by the COMPRESS and VISCOUS models were compared to electrical data to determine if the simulations were correct. The models showed that the wafers that exhibited no leakage solely due to the field oxidation did indeed have structure cross sections showing complete isolation; however, there were cases where the electrical measurements conflicted with the TSUPREM-4 structure cross sections.

The COMPRESS model correctly showed isolation for each oxidation split for t_{si}=50nm. The structure cross sections indeed showed the field oxide reaching the BOX. For t_{si}=90nm, the model showed that the all oxidation splits were sufficient for isolation while the electrical data showed that only wafers 4 and 10, which received a 40% and 37% over oxidation, respectively were completely isolated without the aid of field implants.

The VISCOUS model showed the same results for all oxidation splits for t_{si}=50nm except for the 10% over oxidation used in conjunction with the 35nm SRO. The structure cross section for this oxidation reveals a thin silicon filament extending between the silicon islands. See Appendix A. This disagrees with the electrical measurements, i. e., no leakage was present. It is expected that the presence of a field implant would eliminate any leakage through the filament; however, for the model to have been correct, there should have been leakage current in structures which received no field implant. No such leakage was found. In the case of t_{si}=90nm, the VISCOUS model correctly modeled wafer 1, which received a 10% over oxidation. Its cross section reveals a thin filament

between the silicon islands. This suggests that the leakage current would be modulated by the field spacing and field implants, and this was the case as shown by figures 29 and 31. This leakage modulation also was seen with wafer 2, which received a 20% over oxidation; however, this was not illustrated by the VISCOUS model cross section. It showed no filament in the cross section. Last was wafer 9, which received the 27% over oxidation with the 10nm SRO. Recall that this wafer exhibited leakage for all field implants and spacings. This electrical behavior suggests little oxidation towards the BOX and the existence of a thick filament; however, the structure cross section does not reveal such a filament. See Appendix B.

Chapter VI
Conclusion

6.1 Introduction

This chapter gives a summary of the results and offers suggestions for future work.

6.2 Summary of Results

In order to optimize LOCOS and Oxidized Mesa isolation process parameters for SOI technology, characterization of the isolation schemes was necessary. The global contribution of the work in this thesis was the design of the test devices/structures as well as the fabrication procedure needed to realize the test device/structures. Beginning with the characterization of LOCOS isolation, electrical measurements of the isolation islands were taken to quantify design constraints on the isolation structures in terms of leakage between adjacent device active areas. Haond and Colinge suggested that having top-layer silicon film thicknesses ≥ 150nm necessitated excessively long oxidation times to achieve complete isolation[14,20]. This phenomenon was not found to happen with top- layer silicon thicknesses of 90nm and below. Electrical measurements showed that complete dielectric isolation could be achieved with a 40% over oxidation of the field region regardless of other process parameters. If a shorter oxidation time is desired, similar

results could be obtained by working within the design constraints set by the field field-oxidation time, field-implant dose, and field spacing.

6.3 Future Work

There are many avenues to be investigated in terms of future work. In respect to the isolation islands and characterizing the LOCOS isolation, Scanning Electron Microscope (SEM) cross sections would be useful for evaluating the isolation structures' shapes and lateral encroachment as dependent upon field spacing and fabrication parameters. This data could then be mapped to MOSFET electrical measurements and sidegating tests to determine the impact of submicron field spacings and ΔW on MOSFET narrow width effects and device performance degradation. Electrical measurements of the MOSFETs fabricated with Oxidized Mesa isolation would be used to make conclusions about 2-dimensional charge sharing effects, which were reported in devices fabricated with straight Mesa isolation. On a global scale, future work for this project would involve replicating the experiment in CMOS with more process parameter splits. This would allow investigation of the Comb diode structures, a more thorough examination of the isolation schemes, and provide a means to characterize these isolation schemes for p-channel MOS (PMOS) technology.

Bibliography

[1] Wolf, S., *Silicon Processing for the VLSI Era, Vol. 2*, Lattice Press, California, 1990.

[2] Shibata, T., *et al.*, "New Device Isolation Technology for the VLSI Era, " *JST News, Vol.2*, No. 4, p.23, August, 1983.

[3] Oldham, W. G., "Isolation Technology for Scaled MOS VLSI, " *IEDM Digest*, 1982.

[4] Borland, J., *et.al.*, "Advanced Dielectric Isolation Through Selective Epitaxial Growth Techniques, " *Soild State Technology*, p.141, August, 1985.

[5] Hui, J., *et al.*, "Scaling Limitations of Sub micron Local Oxidation Technology, " *Proceedings from the International Electron Devices Meeting*, p.392, 1985.

[6] Muller, R.S. & Kamins, T. I., Device Electronics for Integrated Circuits, Wiley and Sons, New York, 1986.

[7] Guegan, S., *et. al.*, "Isolation Design Comparisons for 0.5μm CMOS Technology Using SILO Process, " *Microelectronic Engineering, Vol 19*, p.13-16, 1992.

[8] Chiu, K.Y., *et. al.*, "Sloped-Wall SWAMI-a Defect-Free Zero Bird's Beak Local Oxidation Process for Scaled VLSI Technology, " *IEEE Trans. on Electronic Devices, Vol. ED-30*, No.11. p.1506, November, 1983.

[9] Meyssen, V. M. H., *et. al.*, "Framed Poly Buffer LOCOS Technology for 0.35μm CMOS, " *Microelectronic Engineering, Vol 19*, p.257-260, 1992.

[10] Wils, N. A. H., *et. al.*, "A New Sealed Poly Buffer LOCOS Isolation Scheme, " *Microelectronic Engineering, Vol 15*, p.643-646, 1991.

[11] Fuse, G., *et. al.*, "A Practical Trench Isolation With A Novel Planarization Process, " *IEDM Digest*, 87.

[12] Colinge, Jean-Pierre, *Silicon-on-Insulator Technology: Material to VLSI*, Klumer, Academic Publishers, Boston, 1991.

[13] Le Ne´el, O., *et. al.*, "Rounded Edge Mesa for Sub micron SOI CMOS Process," *ESSDERC*, September, 1990.

[14] Hoand, M., *et. al.*, "Lateral Isolation in SOI CMOS Technology, " *Solid State Technology*, p.47, July, 1991.

[15] Crowder, S., *et. al.*, unpublished.

[16] Chen, J., *et. al.*, "Effects of the Field-Edge Transistor on SOI MOSFETS, " *VLSITA*, p.219, 1991.

[17] De Wolfe, I. *et al.*, "Investigation of Local Isolation Structures on SIMOX Substrates with Micro-Raman Spectroscopy and Correlation with Xtem, " Proceedings of the Fifth International symposium on Silicon-on-Insulator Technology and Devices, p.307, May, 1992.

[18] Claeys, C., *et. al.*, "Defect Generation/Control Related to Isolation Technology, " Proceedings of the first International Autumn School 1985: Gettering and Defect Engineering in the Semiconductor Technology (GADEST), p.100, October, 1985.

[19] Reif, R. Course Notes, 6.774, 1994.

[20] Colinge, Jean-Pierre, "Thin-film SOI Devices: A Perspective, " *Microelectronic Engineering, Vol 8*, p.127-147, 1988.

[21] Fischer, Greg, Beginner's Guide to Fabrication using CAFE Manual, October, 1993.

[22] TSUPREM-4 Manual, Technology Modeling Associates, December, 1993.

[23] Grove, A. S., *Physics and Technology of Semiconductor Devices*, John Wiley & Sons, New York, 1967.

Appendix A
Process flow for experiment

```
lefine isoltest
  (flow
   (:doc "isolation test")
   (:version
    (:modified :number 1.0 :by "Jeffrey Thomas" :date "Oct. 26, 1994 "
               :what "Beta version"))
    (:body
load
       :material-1 "p-type"
       :wafers-1 "1-16"
       :wafers-2 :none
       :wafers-3 :none
       :wafers-4 :none
       :wafers-5 :none
       :tag "Use the SOI wafers"
       )
label-exp
       :wafs "1-16"
       :tag "Wafers are already labeled on the back"
       )
diff-ox
       :anneal-time-min 10
       :anneal-gas ":N2"
       :rampdown-gas ":N2"
       :rampdown-temp-C 800
       :expected-thickness-A 2017
       :number-of-points 9
       :tag1 "Try to get as close as possible "
       :tag2 "SOI film is around 1100A"
       :wafs1 "1-4"
       :wafs2 :none
       :wafs3 :none
       )
diff-ox
       :anneal-time-min 10
       :anneal-gas ":N2"
       :rampdown-gas ":N2"
       :rampdown-temp-C 800
       :expected-thickness-A 2910
       :number-of-points 9
       :tag1 "Try to get as close as possible "
       :tag2 "SOI film is around 700A"
       :wafs1 "5-8"
       :wafs2 "13-16"
       :wafs3 :none
       )
diff-ox
       :anneal-time-min 10
       :anneal-gas ":N2"
       :rampdown-gas ":N2"
       :rampdown-temp-C 800
       :expected-thickness-A 2256
       :number-of-points 9
       :tag1 "Try to get as close as possible "
       :tag2 "SOI film is around 1000A"
       :wafs1 "9-10"
       :wafs2 :none
       :wafs3 :none
       )
diff-ox
       :anneal-time-min 10
       :anneal-gas ":N2"
       :rampdown-gas ":N2"
       :rampdown-temp-C 800
       :expected-thickness-A 3146
```

```
        :number-of-points 9
        :tag1 "SOI film is around 600A"
        :wafs1 "11-12"
        :wafs2 :none
        :wafs3 :none
        )
wet-etch-bhf-dewet
        :film-thk-A 3140
        :percent-overetch 25
        :wafs "1-16"
        :tag "when  wafers 11&12 dewet, the rest are finished also !"
        )
diff-ox-exp
        :temp-C 1000
        :dryox-time-min 34
        :wetox-time-min 0
        :anneal-temp-C 1000
        :anneal-time-min 10
        :anneal-gas ":N2"
        :rampdown-gas :N2
        :rampdown-temp-C 800
        :expected-thickness-A 350
        :number-of-points 49
        :tag1 "I got the settings from Bruce's logs-----please confirm settings"
        :tag2 "which furnace= ?  might have to adjust time by a minute or so"
        :tag3 "These are SOI wafers.....measure monitor"
        :wafs1 ("1-8" "13-16")
        :wafs2 ("1-8" "13-16")
        :wafs3 :none
        )
diff-ox-exp
        :temp-C 1000
        :dryox-time-min 4
        :wetox-time-min 0
        :anneal-temp-C 1000
        :anneal-time-min 10
        :anneal-gas ":N2"
        :rampdown-gas :N2
        :rampdown-temp-C 800
        :expected-thickness-A 100
        :number-of-points 49
        :tag1 "I got the settings from Bruce's logs-----please confirm settings"
        :tag2 "which furnace= ?  might have to adjust time by a minute or so"
        :tag3 "These are SOI wafers.....measure monitor"
        :wafs1 "9-12"
        :wafs2 "9-12"
        :wafs3 :none
        )
diff-lpcvd-nitride
        :wafs1 "1-16"
        :wafs2 "1-16"
        :wafs3 :none
        :wafs4 :none
        :tag4 "These are SOI wafers.....measure monitor only"
        :thickness-A 1000
        :number-of-points 9
        )
photo-stepper-thin
        :define "Active pattern"
        :reticle "DOTFET1"
        :dswjob "DOTFET_L1"
        :wafs1 "1-16"
        :wafs2 "1-16"
        :wafs3 "1-16"
        :wafs4 "1-16"
```

```
        :tag1 "Jeff T. will do the exposing."
        )
(plasma-etch-nitride
        :thickness-A 1000
        :number-of-points 9
        :wafs1 "1-16"
        :wafs2 "1-16"
        :wafs3 ("1" "9")
        :tag1 "There is a split in the oxide under the nitride.  W1-350A, W9-100A."
        :tag3 "expect 100 and 350A oxide in field region"
        )
(plasma-etch-oxide
        :thickness-A 350
        :etch-stop-film "Si"
        :etch-stop-thk-A 600
        :wafs1 "13-16"
        :wafs2 "13-16"
        :tag2 "These are the mesa wafers"
        :number-of-points 4
        )
(plasma-etch-si-drytek
        :thickness-A 600
        :etch-stop-film "SiO2"
        :etch-stop-thk-A 4000
        :mw-strip? "?"
        :wafs "13-16"
        :tag "These are the MESA wafers"
        )
(photo-gasonics-piranha
        :wafs "1-16"
        )

(photo-scanner-thin
        :device "Field Implant -1, LOCOS/MESA"
        :mask "See Doug"
        :wafs1 "1-16"
        :wafs2 "1-16"
        :wafs3 "1-16"
        :wafs4 "1"
        :wafs5 "1-16"
        :tag2 "Jeff, Doug, or Gwen should expose wafers."
        )
(impl
        :Species "BF2"
        :Energy-KeV 50
        :Dose-ions/cm2 1E13
        :Tilt-deg. 10
        :Orientation-deg. 27
        :pr-present? "yes"
        :pr-fusion-baked? "no"
        :tag "these are the LOCOS wafers"
        :wafs "1-12"
        )
(impl
        :Species "BF2"
        :Energy-KeV 30
        :Dose-ions/cm2 2e12
        :Rotation-deg 720
        :Tilt-deg. 30
        :Orientation-deg. 27
        :pr-present? "yes"
        :pr-fusion-baked? "no"
        :tag "The wafers will be rotated while implanted----MESA.  Notice tilt."
        :wafs "13-16"
        )
```

```
photo-gasonics-piranha
        :wafs "1-16"
        )
photo-scanner-thin
        :device "Field Implant -2,  LOCOS /MESA"
        :mask "See Doug"
        :wafs1 "1-16"
        :wafs2 "1-16"
        :wafs3 "1-16"
        :wafs4 "1"
        :wafs5 "1-16"
        :tag2 "Jeff, Doug, or Gwen should expose wafers."
        )
impl
        :Species "BF2"
        :Energy-KeV 50
        :Dose-ions/cm2 5E13
        :Tilt-deg. 10
        :Orientation-deg. 27
        :pr-present? "yes"
        :pr-fusion-baked? "no"
        :tag "this is second LOCOS implant"
        :wafs "1-12"
        )
impl
        :Species "BF2"
        :Energy-KeV 30
        :Dose-ions/cm2 1e13
        :Rotation-deg 720
        :Tilt-deg. 30
        :Orientation-deg. 27
        :pr-present? "yes"
        :pr-fusion-baked? "no"
        :tag "This is MESA dose -2.  Wafers will be rotated. Notice tilt."
        :wafs "13-16"
        )
photo-gasonics-piranha
        :wafs "1-16"
        )
photo-scanner-thin
        :device "Field Implant -3,  LOCOS /MESA"
        :mask "See Doug"
        :wafs1 "1-16"
        :wafs2 "1-16"
        :wafs3 "1-16"
        :wafs4 "5"
        :wafs5 "1-16"
        :tag1 "Jeff, Doug, Gwen should expose wafers."
        )
impl
        :Species "BF2"
        :Mass-AMU "?"
        :Energy-KeV 50
        :Dose-ions/cm2 1e14
        :Tilt-deg. 10
        :Orientation-deg. 27
        :pr-present? "yes"
        :pr-fusion-baked? "no"
        :tag "LOCOS field implant-3"
        :wafs "1-12"
        )
impl
        :Species "BF2"
        :Mass-AMU "?"
        :Energy-KeV 30
```

```
        :Dose-ions/cm2 5E13
        :Rotation-deg 720
        :Tilt-deg. 30
        :Orientation-deg. 27
        :pr-present? "yes"
        :pr-fusion-baked? "no"
        :tag "MESA-dose-3.  Wafers will be rotated while implanted. Notice tilt."
        :wafs "13-16"
        )
(photo-gasonics-piranha
        :wafs "1-16"
        )
(diff-ox
        :temp-C 1050
        :wetox-time-min 18
        :anneal-temp-C 1000
        :anneal-time-min 10
        :anneal-gas :N2
        :rampdown-gas :N2
        :rampdown-temp-C 800
        :expected-thickness-A 2311
        :number-of-points 9
        :tag2 "RAMP IN NITROGEN ONLY!  this is field oxide 1"
        :tag3 "Measure the monitor wafer only"
        :wafs1 "1"
        :wafs2 "1"
        :wafs3 :none
        )
(diff-ox
        :temp-C 1050
        :wetox-time-min 21
        :anneal-temp-C 1000
        :anneal-time-min 10
        :anneal-gas :N2
        :rampdown-gas :N2
        :rampdown-temp-C 800
        :expected-thickness-A 2566
        :number-of-points 9
        :tag2 "RAMP IN NITROGEN ONLY!!!  this is field oxide 2&9"
        :tag3 "Measure monitor only"
        :wafs1 ("2" "9")
        :wafs2 ("2" "9")
        :wafs3 :none
        )
(diff-ox
        :temp-C 1050
        :wetox-time-min 24
        :anneal-temp-C 1000
        :anneal-time-min 10
        :anneal-gas :N2
        :rampdown-gas :N2
        :rampdown-temp-C 800
        :expected-thickness-A 2800
        :number-of-points 9
        :tag2 "RAMP IN NITROGEN ONLY!! this is field oxide 3"
        :tag3 "Measure monitor only"
        :wafs1 ("3" "10")
        :wafs2 ("3" "10")
        :wafs3 :none
        )
(diff-ox
        :temp-C 1050
        :wetox-time-min 27
        :anneal-temp-C 1000
        :anneal-time-min 10
```

```
        :anneal-gas :N2
        :rampdown-gas :N2
        :rampdown-temp-C 800
        :expected-thickness-A 3030
        :number-of-points 9
        :tag2 " RAMP IN NITORGEN ONLY! this is field oxide 4"
        :tag3 "Measure monitor only"
        :wafs1 "4"
        :wafs2 "4"
        :wafs3 :none
        )
(diff-ox
        :temp-C 1050
        :wetox-time-min 8.5
        :anneal-temp-C 1000
        :anneal-time-min 10
        :anneal-gas :N2
        :rampdown-gas :N2
        :rampdown-temp-C 800
        :expected-thickness-A 1350
        :number-of-points 9
        :tag2 " RAMP IN NITROGEN ONLY! this is field oxide 5"
        :tag3 " Measure monitor only!"
        :wafs1 "5"
        :wafs2 "5"
        :wafs3 :none
        )
(diff-ox
        :temp-C 1050
        :wetox-time-min 9.5
        :anneal-temp-C 1000
        :anneal-time-min 10
        :anneal-gas :N2
        :rampdown-gas :N2
        :rampdown-temp-C 800
        :expected-thickness-A 1468
        :number-of-points 9
        :tag2 "RAMP IN NITROGEN ONLY! this is field oxide 6, 11."
        :tag3 "Measure monitor only"
        :wafs1 ("6" "11")
        :wafs2 ("6" "11")
        :wafs3 :none
        )
(diff-ox
        :temp-C 1050
        :wetox-time-min 10.5
        :anneal-temp-C 1000
        :anneal-time-min 10
        :anneal-gas :N2
        :rampdown-gas :N2
        :rampdown-temp-C 800
        :expected-thickness-A 1580
        :number-of-points 49
        :tag2 "RAMP IN NITROGEN ONLY! this is field ox seven, twelve."
        :tag3 "Measure monitor only"
        :wafs1 ("7" "12")
        :wafs2 ("7" "12")
        :wafs3 :none
        )
(diff-ox
        :temp-C 1050
        :wetox-time-min 12
        :anneal-temp-C 1000
        :anneal-time-min 10
        :anneal-gas :N2
```

```
        :rampdown-gas :N2
        :rampdown-temp-C 800
        :expected-thickness-A 174
        :number-of-points 49
        :tag2 "RAMP IN NITROGEN ONLY! this is field ox eight"
        :tag3  "Measure monitor only"
        :wafs1 "8"
        :wafs2  "8"
        :wafs3 :none
        )
(diff-ox
        :temp-C 1050
        :dryox-time-min "?"
        :anneal-temp-C 1000
        :anneal-time-min 10
        :anneal-gas :N2
        :rampdown-gas :N2
        :rampdown-temp-C 800
        :expected-thickness-A 1000
        :number-of-points 9
        :tag2 "RAMP IN NITROGEN ONLY! MESA Sidewall oxide-1"
        :tag3 "Measure monitor only!"
        :wafs1 "13-14"
        :wafs2 "13-14"
        :wafs3 :none

        )
(diff-ox
        :temp-C 1050
        :dryox-time-min "?"
        :anneal-temp-C 1000
        :anneal-time-min 10
        :anneal-gas :N2
        :rampdown-gas :N2
        :rampdown-temp-C 800
        :expected-thickness-A 2000
        :number-of-points 9
        :tag2 "RAMP IN NIRTROGEN ONLY! MESA Sidewall oxide-2"
        :tag3 "Measure monitor only."
        :wafs1 "15-16"
        :wafs2 "15-16"
        :wafs3 :none
        )
(wet-strip-lpcvd-nitride
        :film-thk-A 1000
        :thk-to-etch-A 1000
        :etch-stop-film "SiO2"
        :etch-stop-thk-A 100/350
        :bhf-etch-time-min 0.5
        :nitride-strip-time-min 60
        :wafs1 "1-16"
        :wafs2 "1-16"
        :tag2 "Etch-stop-thck for wafers 1-8 & 3-16 is 350A,..for wafers 9-12, 100A."
        )
(wet-etch-bhf-timed
        :film-thk-A 100
        :thk-to-etch-A 100
        :percent-overetch 10
        :wafs "9-12"
        :tag "LOCOS"
        )
(wet-etch-bhf-timed
        :film-thk-A 350
        :thk-to-etch-A 350
        :percent-overetch 10
```

```
        :wafs ("1-8" "13-16")
        :tag  "LOCOS/MESA"
        )
(diff-ox
        :temp-C 800
        :dryox-time-min 30
        :anneal-time-min 10
        :anneal-gas :N2
        :rampdown-gas :N2
        :rampdown-temp-C 800
        :expected-thickness-A 50
        :number-of-points 9
        :tag2 "Sacrificial gate"
        :tag3 "measure monitor only"
        :wafs1 "1-16"
        :wafs2 "1-16"
        :wafs3 :none
        )
(impl
        :Species "BF2"
        :Energy-KeV 30
        :Dose-ions/cm2 2.6E12
        :Tilt-deg. 10
        :Orientation-deg. 27
        :pr-present? "yes"
        :pr-fusion-baked? "no"
        :tag "Active area implant for 500A film/MESA"
        :wafs ("5-8" "11-16")
        )
(impl
        :Species "BF2"
        :Energy-KeV 50
        :Dose-ions/cm2 1.5E12
        :Tilt-deg. 10
        :Orientation-deg. 27
        :pr-present? "yes"
        :pr-fusion-baked? "no"
        :tag "Active/channel area implant for 900A film"
        :wafs ("1-4" "9-10")
        )
(wet-etch-bhf-timed
        :film-thk-A 50
        :thk-to-etch-A 50
        :percent-overetch 10
        :wafs "1-16"
        :tag " Do this step as part of the RCA clean before oxidation."
        )
(diff-ox
        :temp-C 800
        :dryox-time-min 30
        :anneal-time-min 10
        :anneal-gas :N2
        :rampdown-gas :N2
        :rampdown-temp-C 800
        :expected-thickness-A 50
        :number-of-points 9
        :tag1 "There is 50A of oxide on wafers.  Dip in 100:1 Hf to strip."
        :tag2 "Gate Oxide"
        :tag3 "measure monitor only"
        :wafs1 "1-16"
        :wafs2 "1-16"
        :wafs3 :none
        )
(diff-lpcvd-a-si
        :wafs1 "1-16"
```

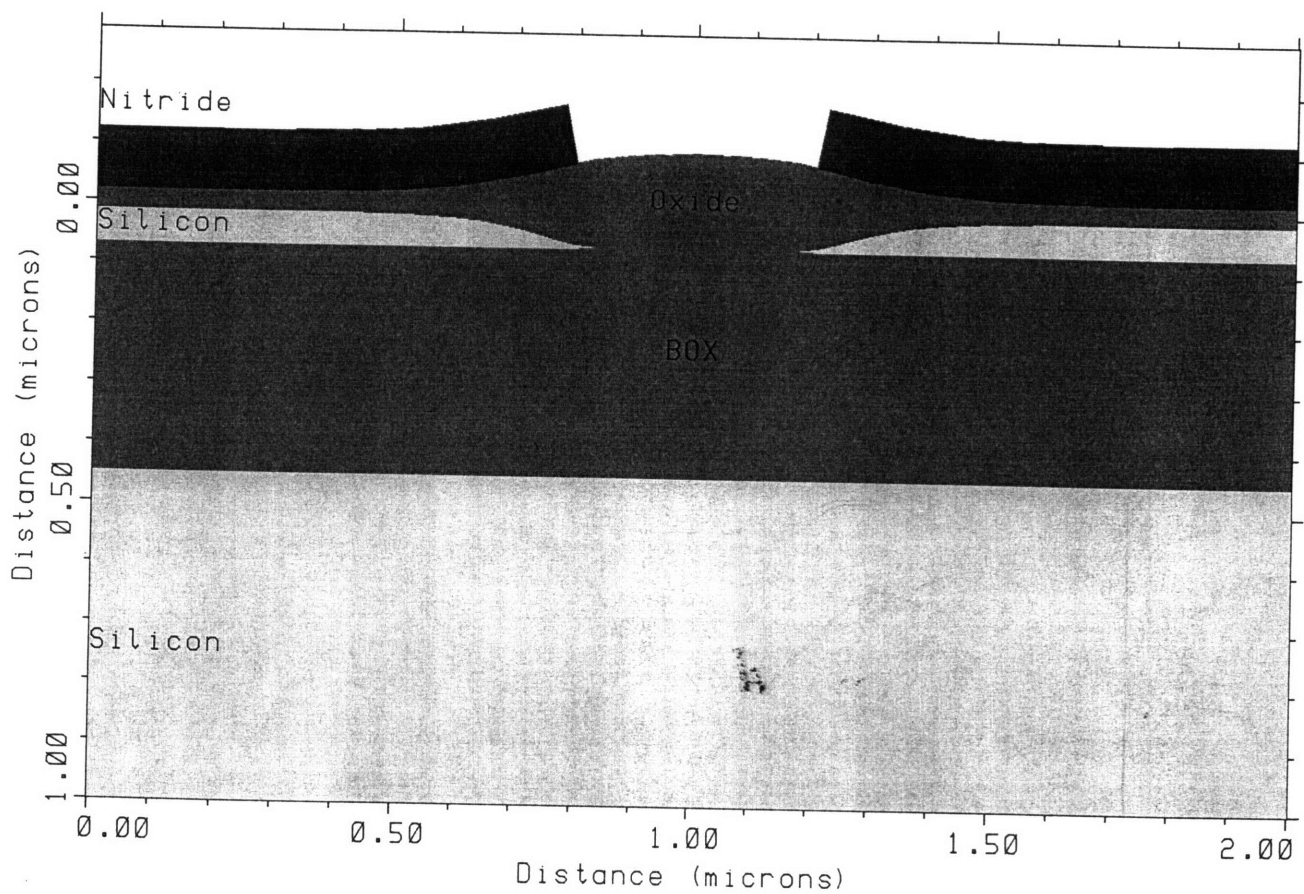
```
        :wafs2 "1-16"
        :wafs3 :none
        :tag2 "Send monitor with wafers."
        :tag3 "Measure monitor only.......SOI wafers."
        :thickness-A 2500
        :number-of-points 9
        )
(photo-stepper-thin
        :define "Poly"
        :reticle "DOTFET4 "
        :dswjob "DOTFET_L4"
        :alignment-tolerance-nm 150
        :wafs1 "1-16"
        :wafs2 "1-16"
        :wafs3 "1-16"
        :wafs4 ("1" "16")
        :tag1 "Jeff will expose on XLS."
        :tag2 "Expose monitor also."
        )
(plasma-etch-n+poly
        :thickness-A 2500
        :etch-stop-film "SiO2"
        :etch-stop-thk-A 50
        :wafs1 "1-16"
        :film-type "oxide"
        :number-of-points 5
        :wafs2 "1-16"
        :wafs3 "1-16"
        :wafs4 "1-16"
        :wafs5 "1-16"
        :tag1 "Wafers have undoped poly "
        :tag3 "Etch Monitor first....Etch to endpoint + 20s overecth"
        )
(impl
        :Species "As"
        :Charge 1
        :Energy-KeV 25
        :Dose-ions/cm2 4E15
        :Tilt-deg. 10
        :Orientation-deg. 27
        :pr-present? "no"
        :pr-fusion-baked? "no"
        :hard-copy? "no"
        :tag "S/D implant"
        :wafs "1-16"
        )
(photo-gasonics-piranha
        :wafs "1-16"
        )
(diff-ox
        :temp-C 850
        :dryox-time-min 30
        :anneal-temp-C 850
        :anneal-time-min 10
        :anneal-gas :N2
        :rampdown-gas :N2
        :rampdown-temp-C 800
        :expected-thickness-A 75
        :tag1 "reox"
        :wafs1 "1-16"
        )
(diff-lpcvd-teos-undoped
        :wafs1 "1-16"
        :wafs2 "1-16"
        :wafs3 :none
```

```
        :thickness-A 5000
        :tag2 "send monitor with wafers"
        :number-of-points 9
        )
photo-coat-back-etch
        :wafs "1-16"
        )
wet-etch-bhf-dewet
        :film-thk-A 5000
        :percent-overetch 25
        :wafs "1-16"
        :tag "5000A Teos on 75A oxide on 2500A poly on  oxide"
        )
photo-gasonics-piranha
        :wafs "1-16"
        )
photo-stepper-thick
        :define "Contacts"
        :reticle "DOTFET7"
        :dswjob "DOTFET_L7"
        :alignment-tolerance-nm 150
        :wafs1 "1-16"
        :wafs2 "1-16"
        :wafs3 "1-16"
        :wafs4 "1-16"
        :tag1 "Jeff will expose on XLS."
        :tag2 "pattern monitor also."
        )
plasma-etch-contacts-vert
        :thickness-A 5000
        :etch-stop-film "Si"
        :wafs1 "1-16"
        :wafs2 :none
        :tag1 " Shoot monitor available to give to Bruce before etch"
        :number-of-points 4
        )
photo-act-piranha
        :wafs "1-16"
        )
metal-sputter-alsi
        :thickness-A 7000
        :ion-sputter-wafers? "yes"
        :wafs1 "1-16"
        :wafs2 "1-16"
        :wafs3 "1-16"
        :tag3 "If possible use Sigma system  with the TiN/AlSi process."
        )
photo-stepper-thin
        :define "metal"
        :reticle "DOTFET8"
        :dswjob "DOFET_L8"
        :alignment-tolerance-nm 150
        :wafs1 "1-16"
        :wafs2 "1-16"
        :wafs3 "1-16"
        :wafs4 "1-16"
        :tag1 "Jeff will expose on XLS."
        )
plasma-etch-alsi
        :thickness-A 7000
        :etch-stop-film "SiO2"
        :etch-stop-thk-A 5000
        :mw-strip? "Yes"
        :wafs1 "1-16"
        :tag1 "Send patterned monitors to Bruce before etch to check out etch."
```

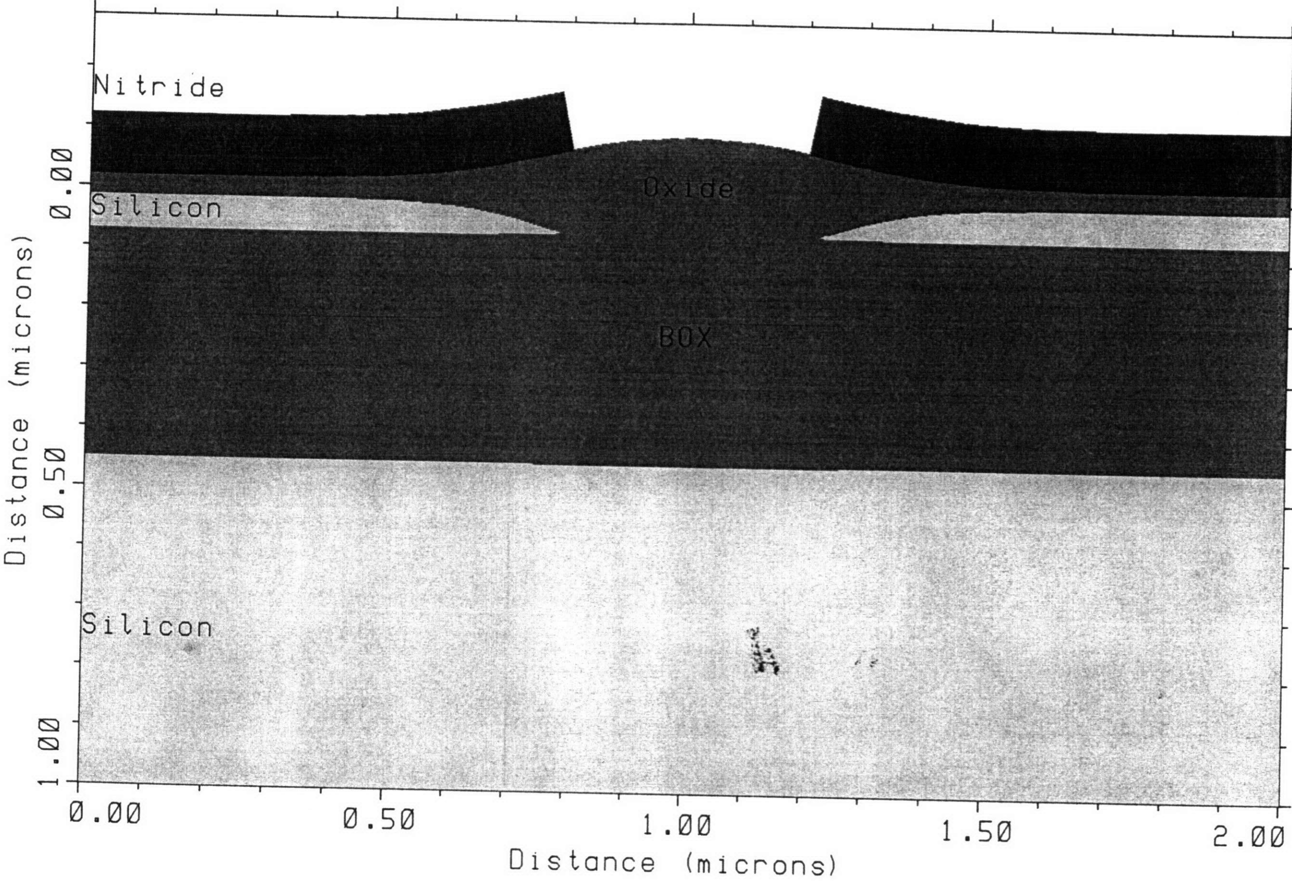
```
        )
photo-gasonics-act
        :wafs "1-16"
        )
diff-sinter
        :temp-C 400
        :anneal-time-min 20
        :anneal-gas :N2
        :tag1 "test before sinter"
        :wafs1 "1-16"
        :wafs2  "1-16"
        )
))
```

Appendix B
TSUPREM-4 cross sections for wafers 5-12

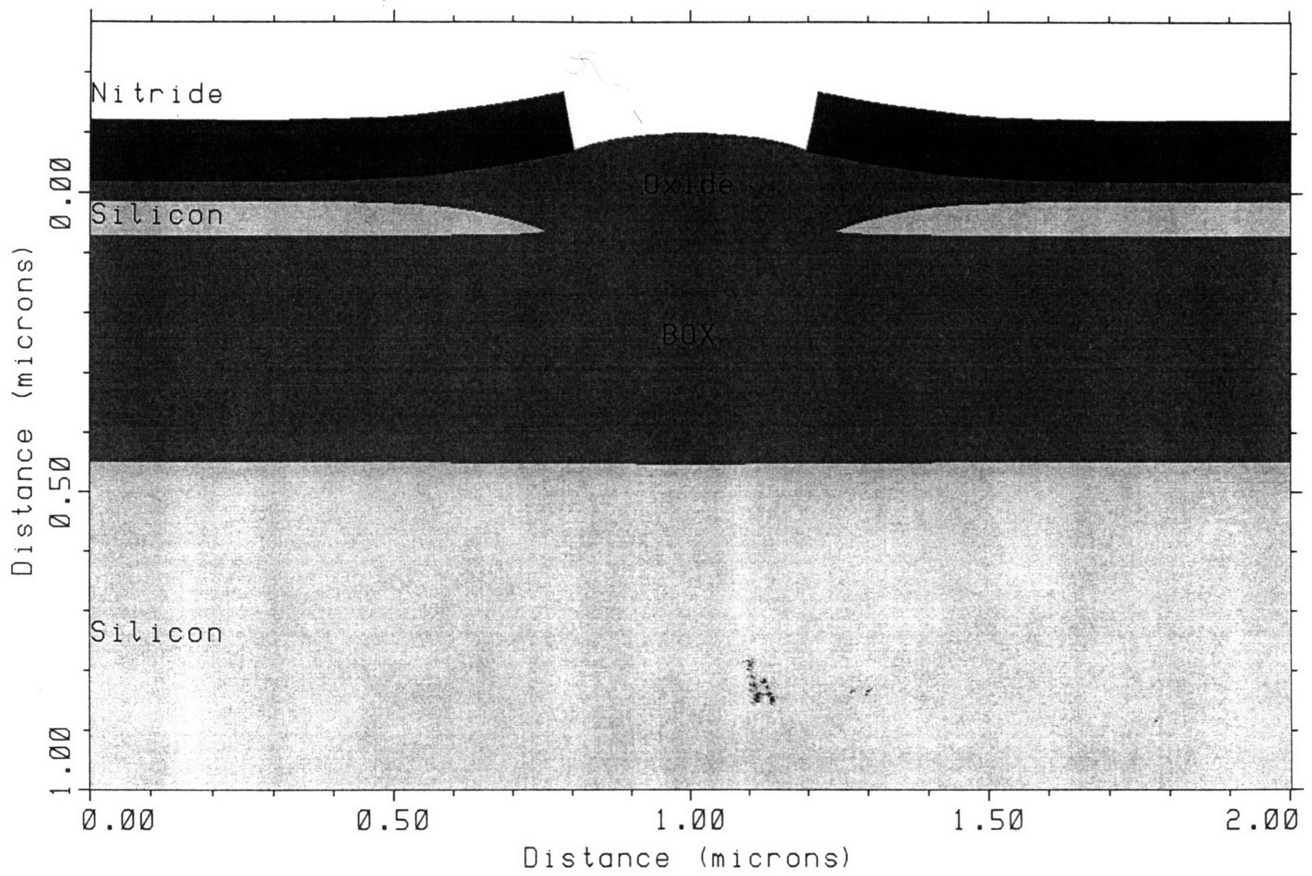
Wafer 5, 10% Over Oxidation, 8.5 min (Compress Model)



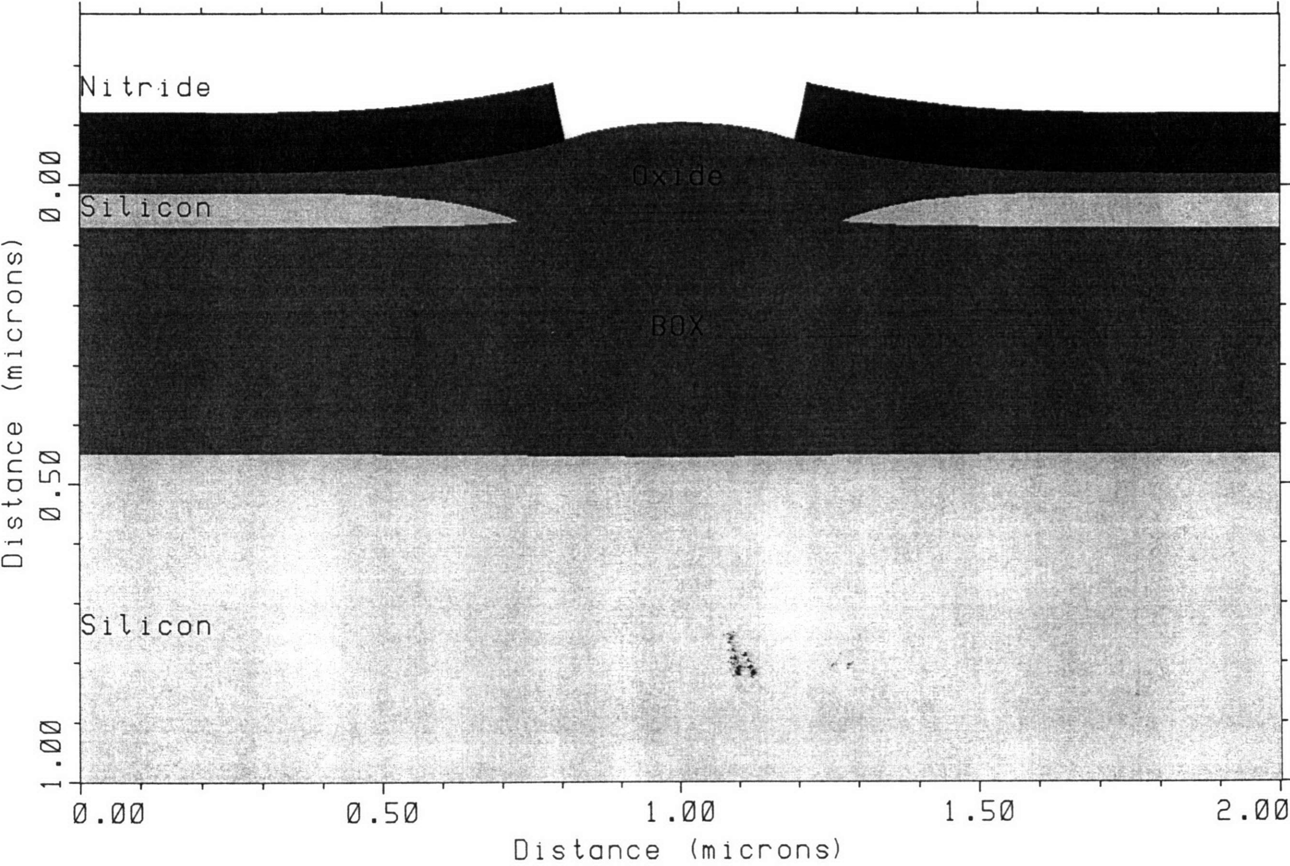
Wafer 6, 20% Over Oxidation, 9.5 min (Compress Model)



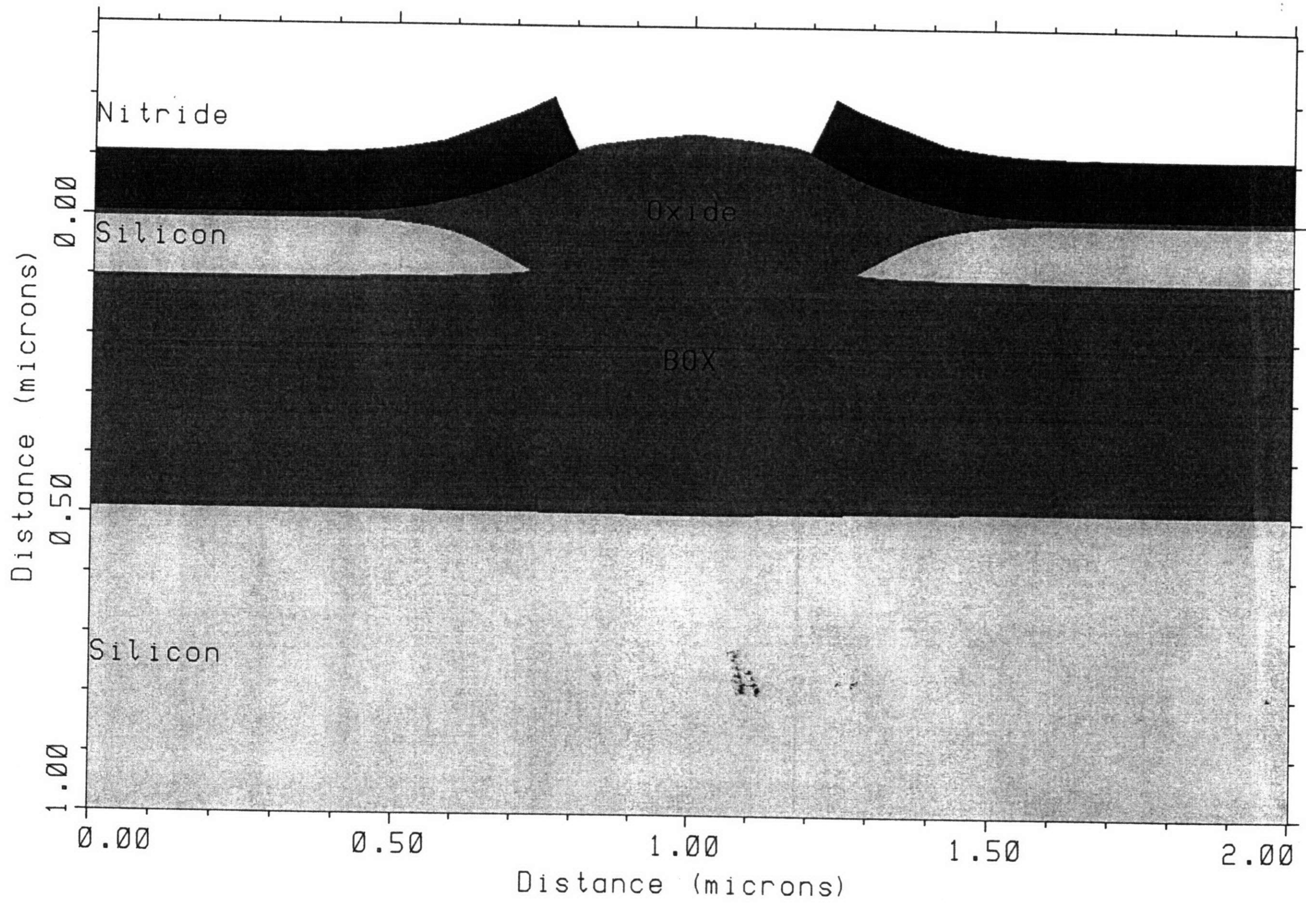
Wafer 7, 30% Over Oxidation, 10.5 min (Compress Model)



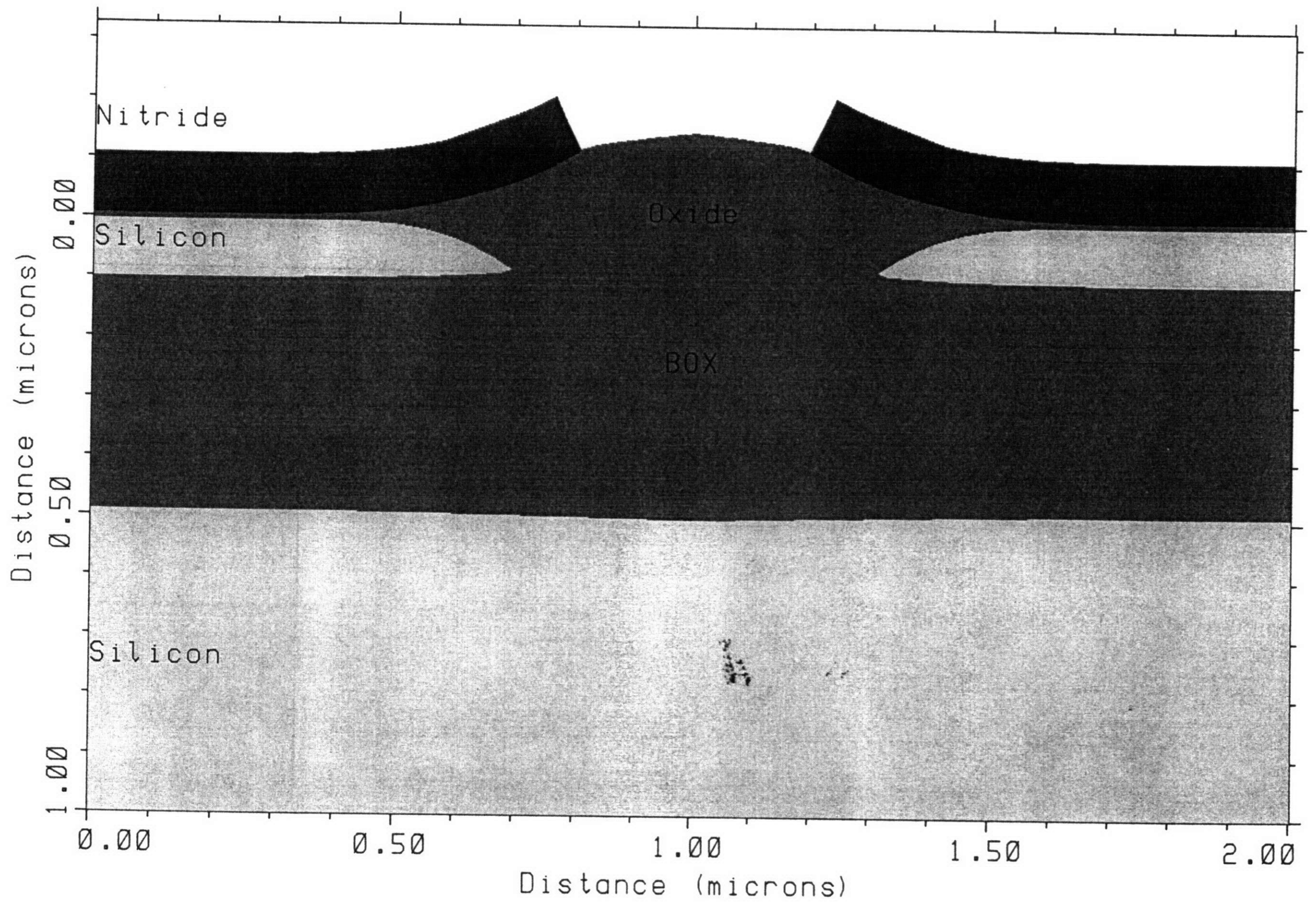
Wafer 8, 40% Over Oxidation, 12 min (Compress Model)



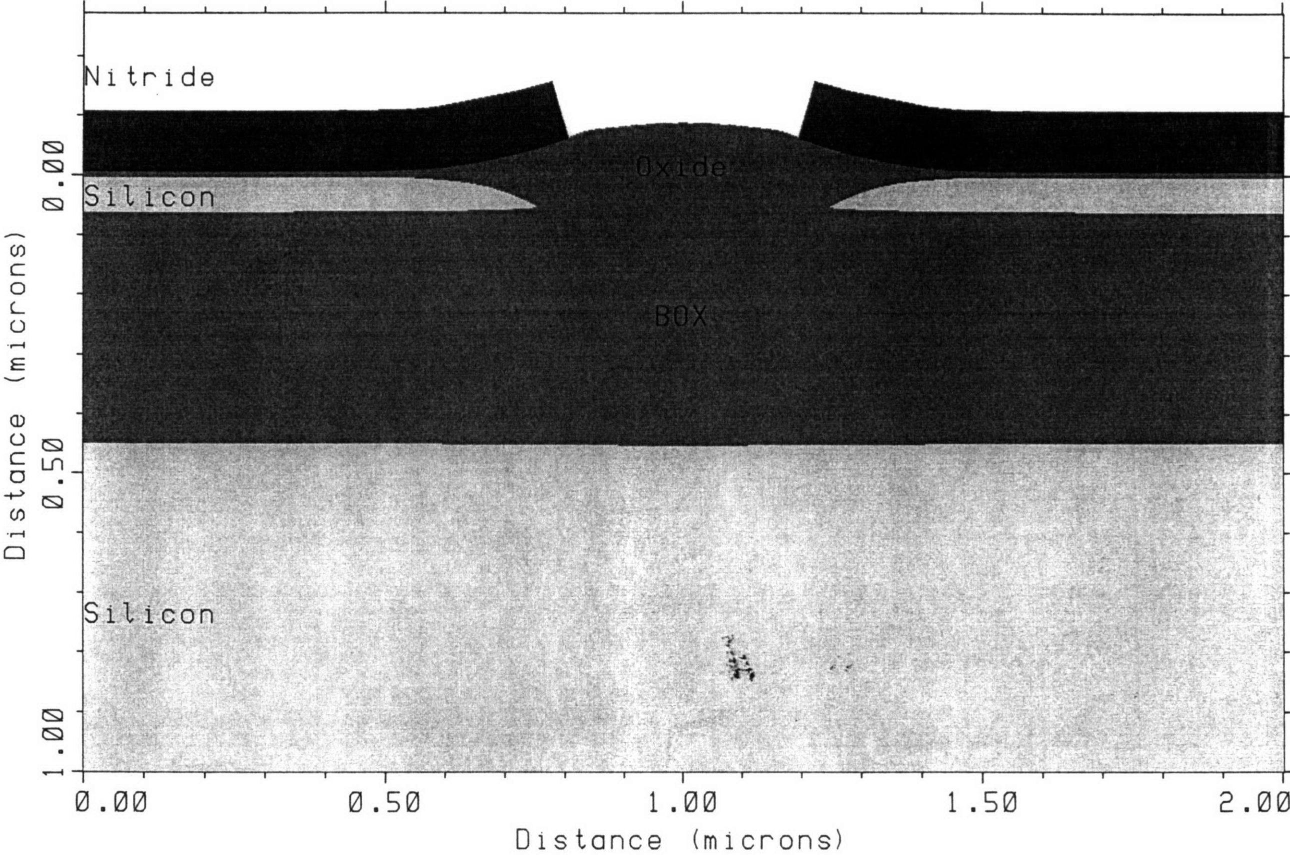
Wafer 9, 27% Over Oxidation, 21 min (Compress Model)



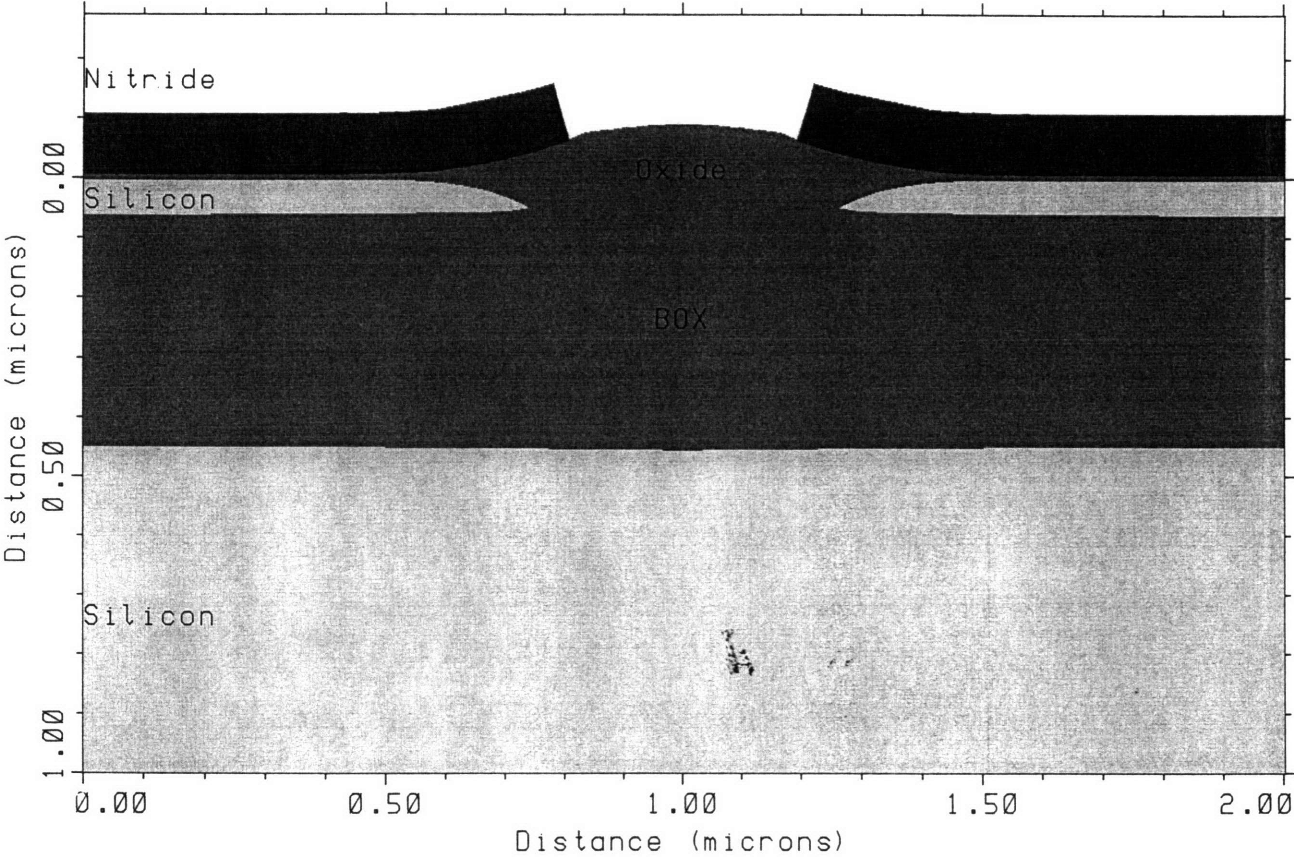
Wafer 10, 37% Over Oxidation, 24 min (Compress Model)



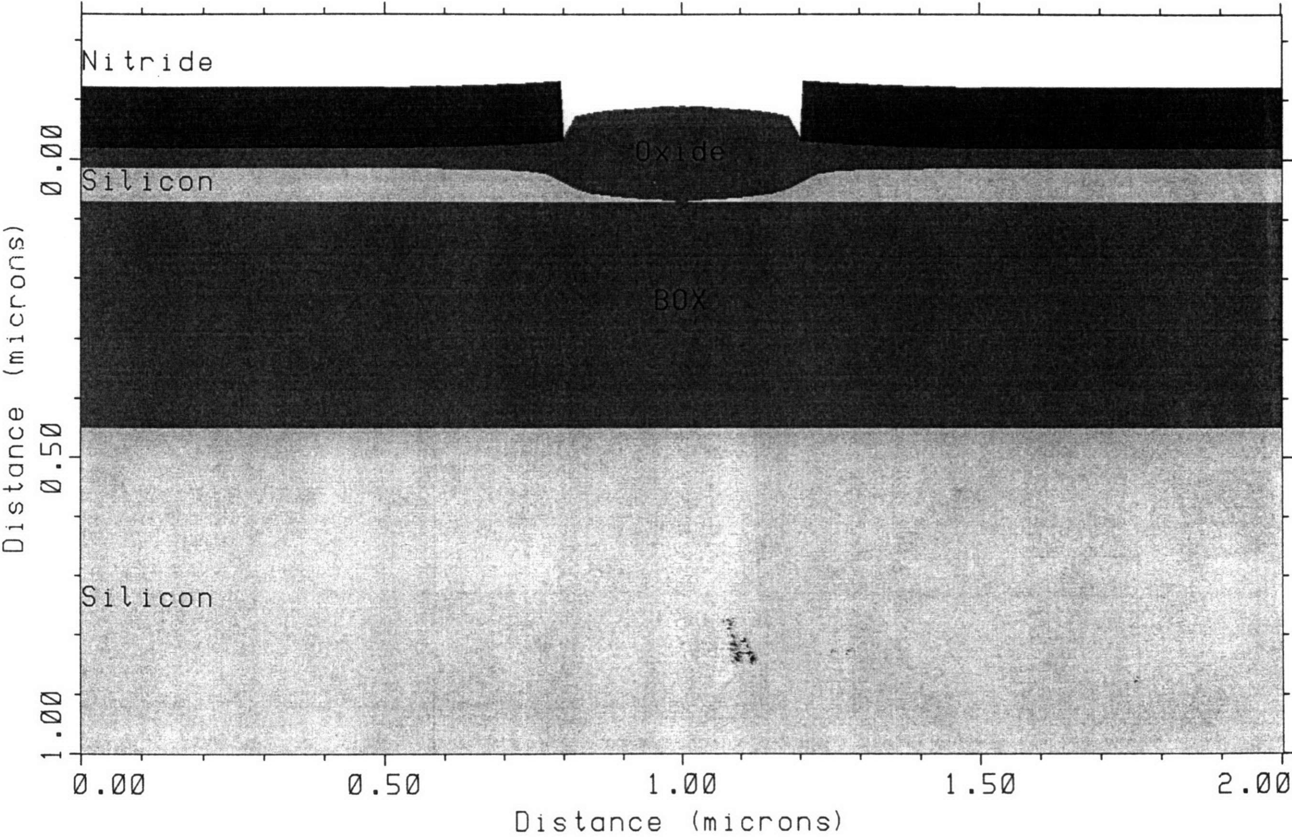
Wafer 11, 27% Over Oxidation, 9.5 min (Compress Model)



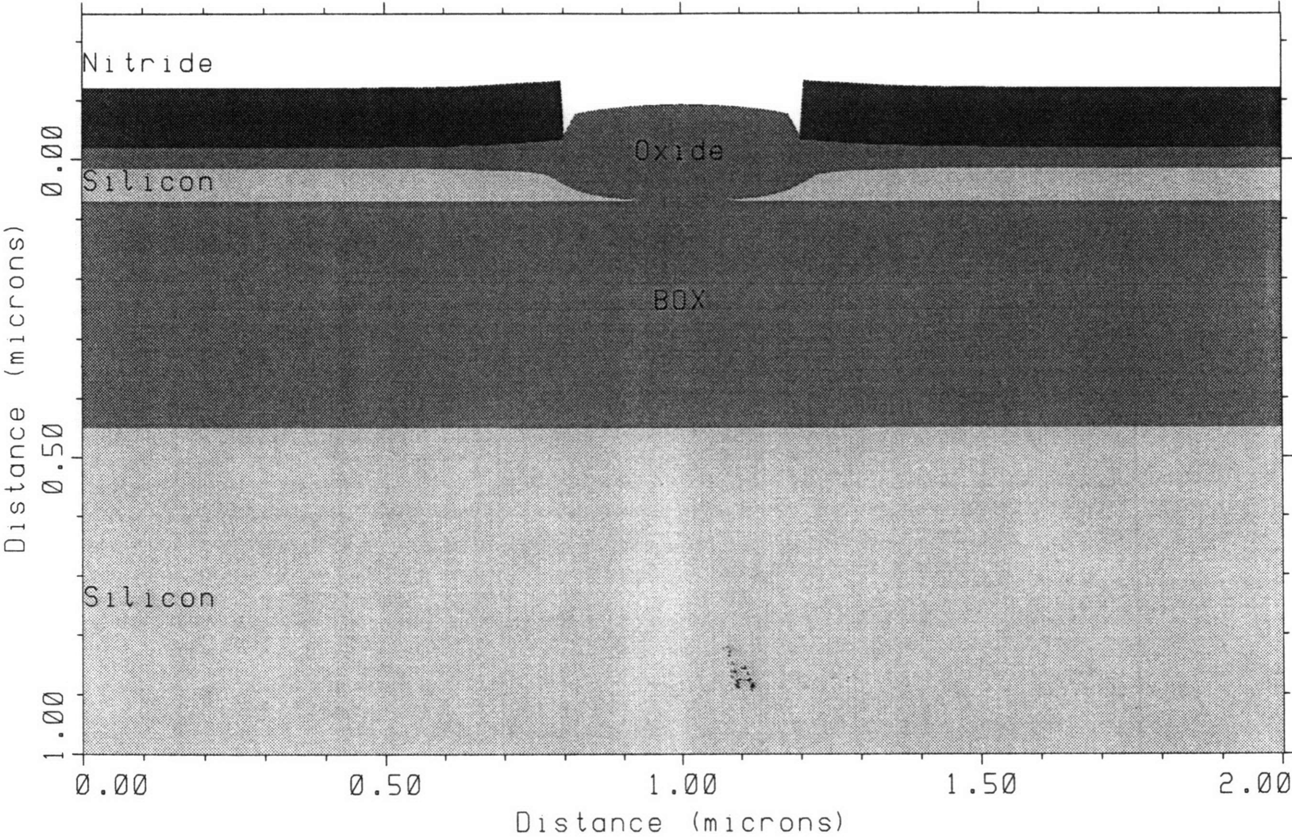
Wafer 12, 37% Over Oxidation, 10.5 min (Compress Model)



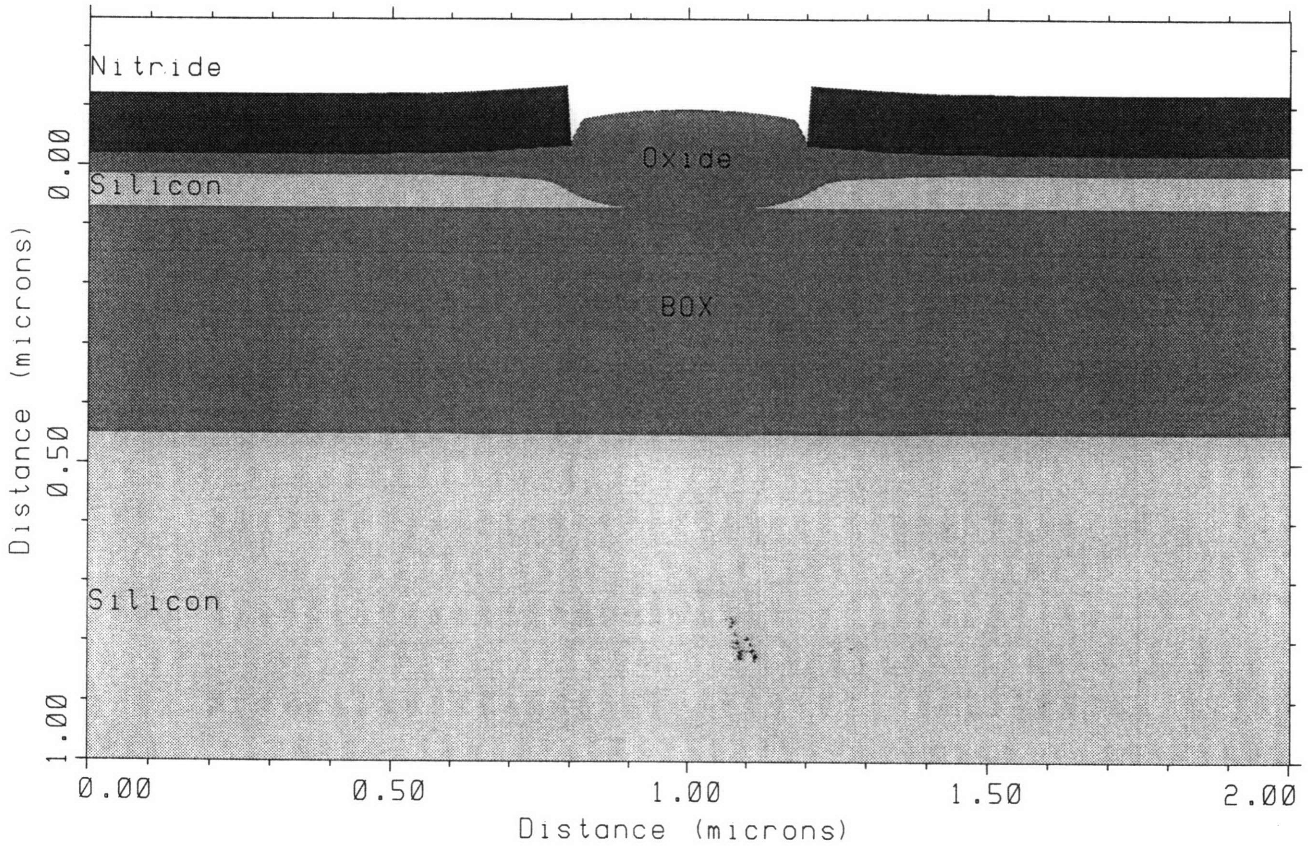
Wafer 5, 10% Over Oxidation, 8.5 min (VISCOUS Model)



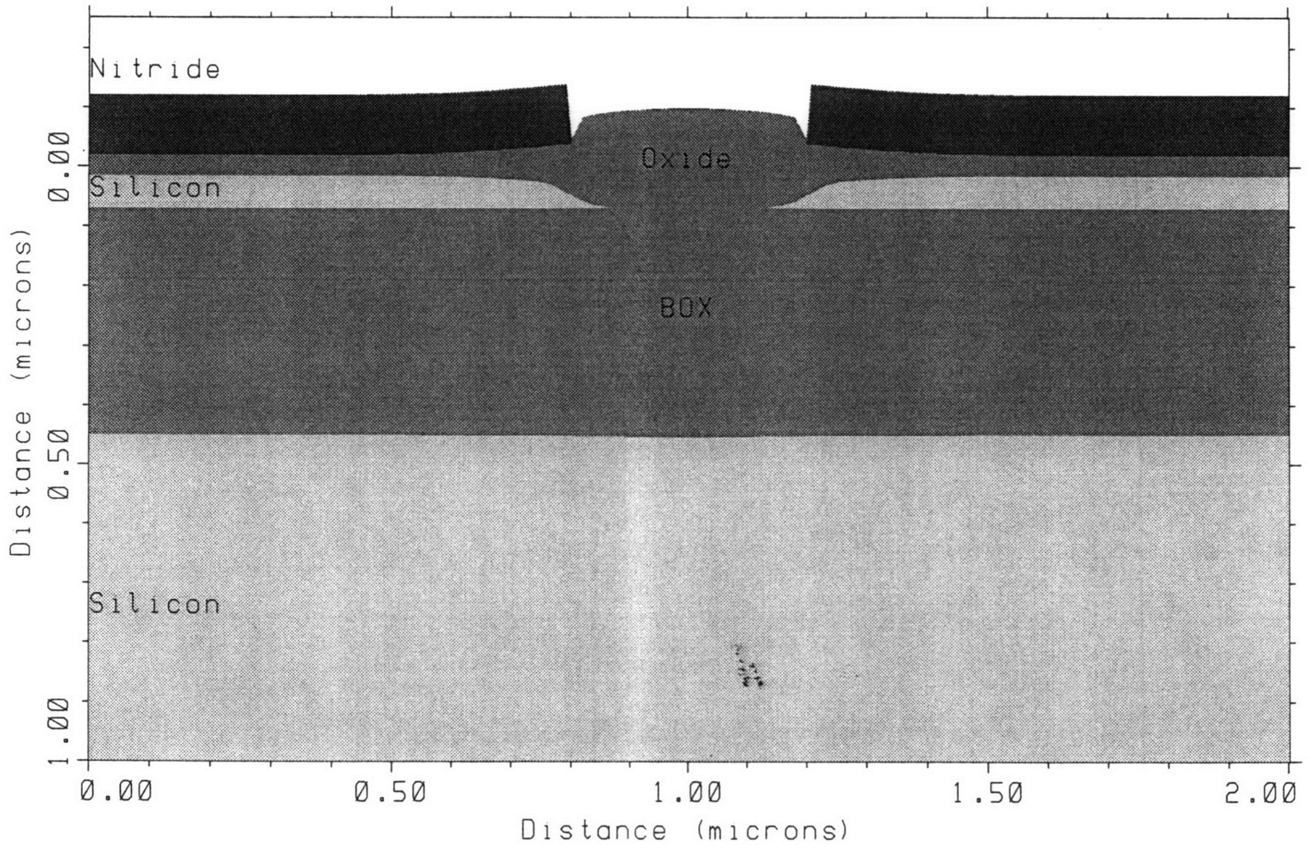
Wafer 6, 20% Over Oxidation, 9.5 min (VISCOUS Model)



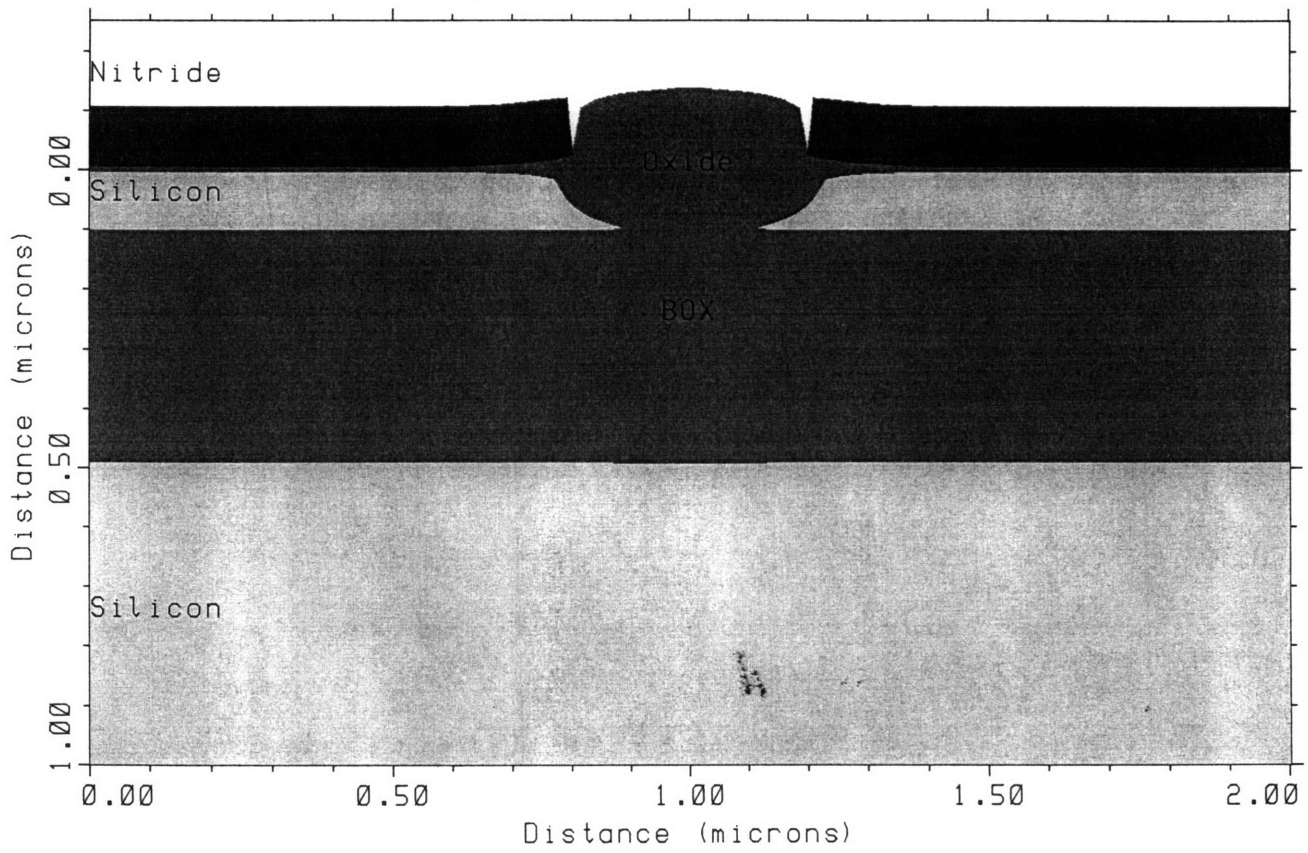
Wafer 7, 30% Over Oxidation, 10.5 min (VISCOUS Model)



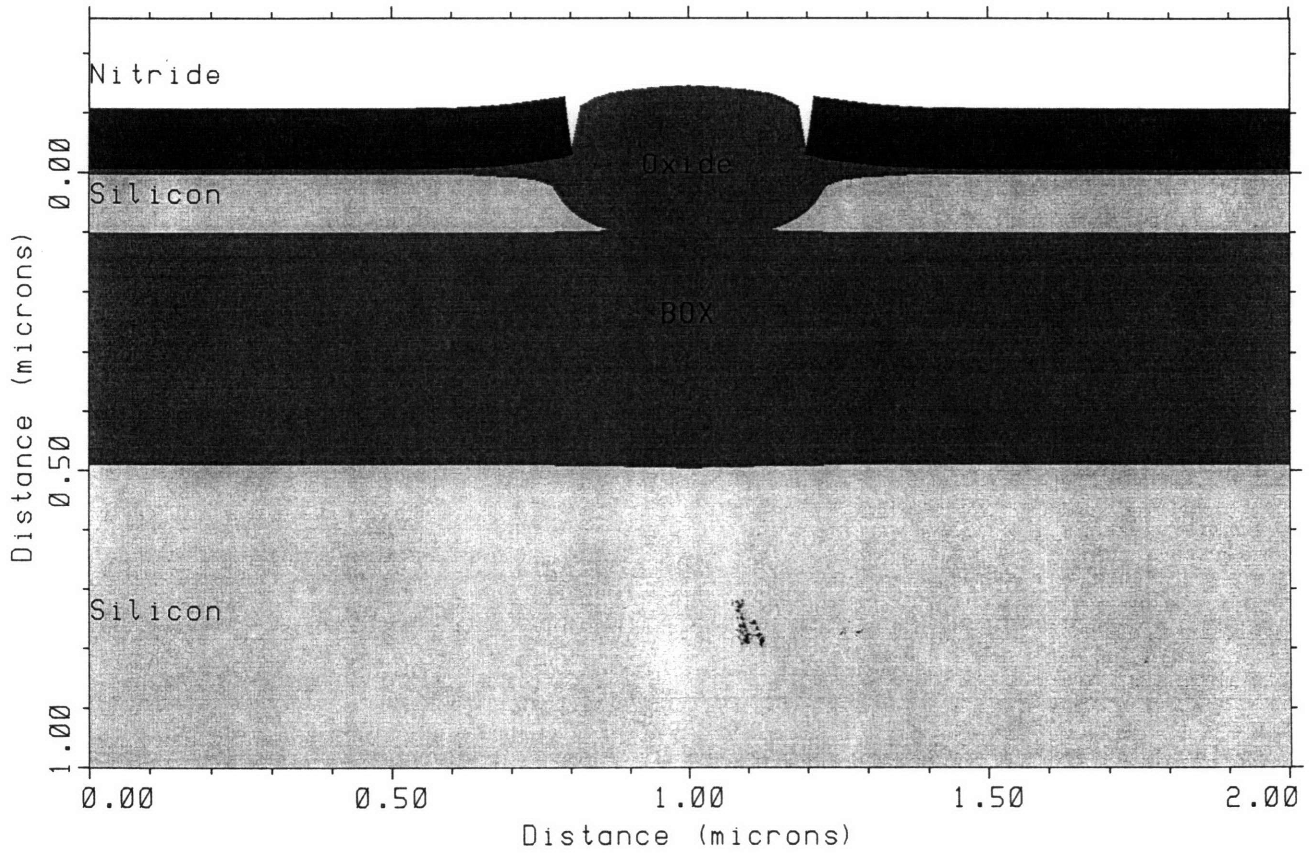
Wafer 8, 40% Over Oxidation, 12 min (VISCOUS Model)



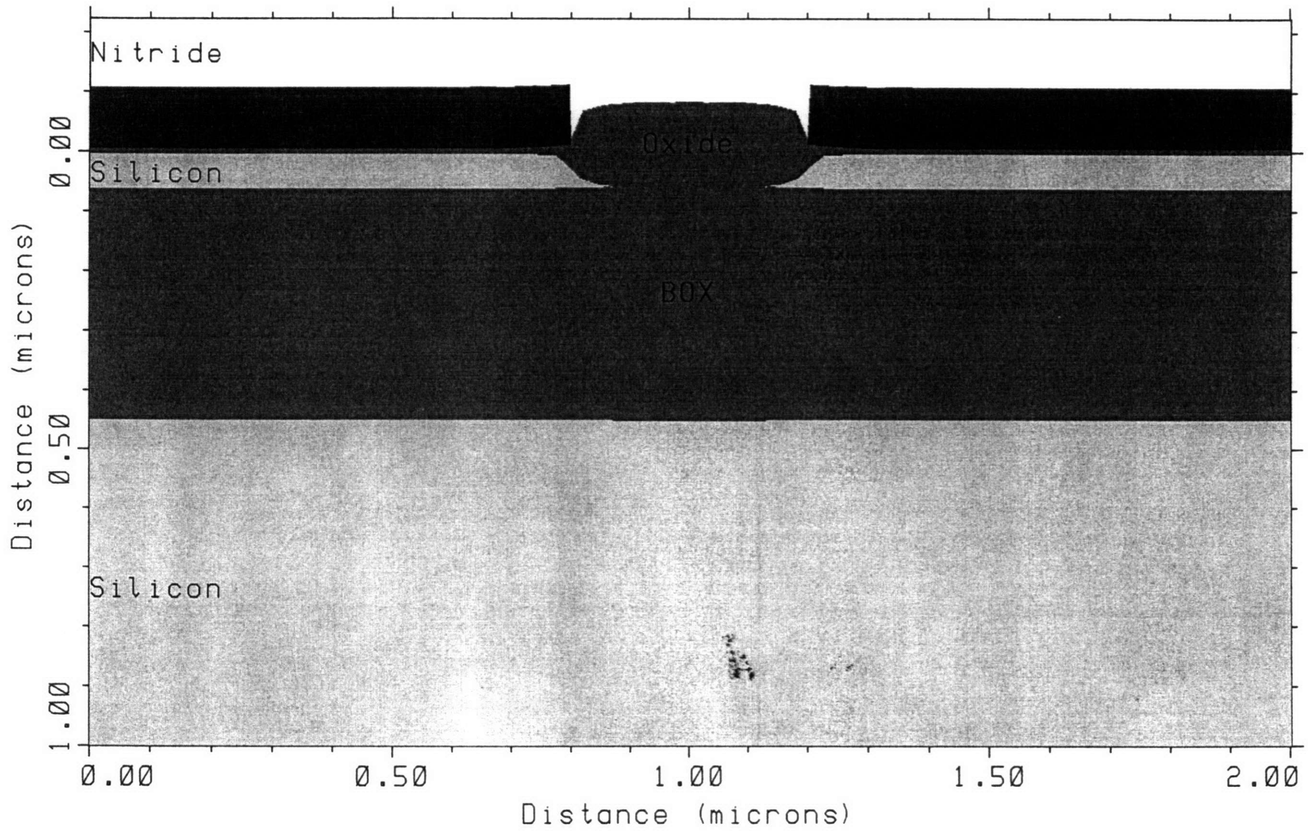
Wafer 9, 27% Over Oxidation, 21 min (VISCOUS Model)



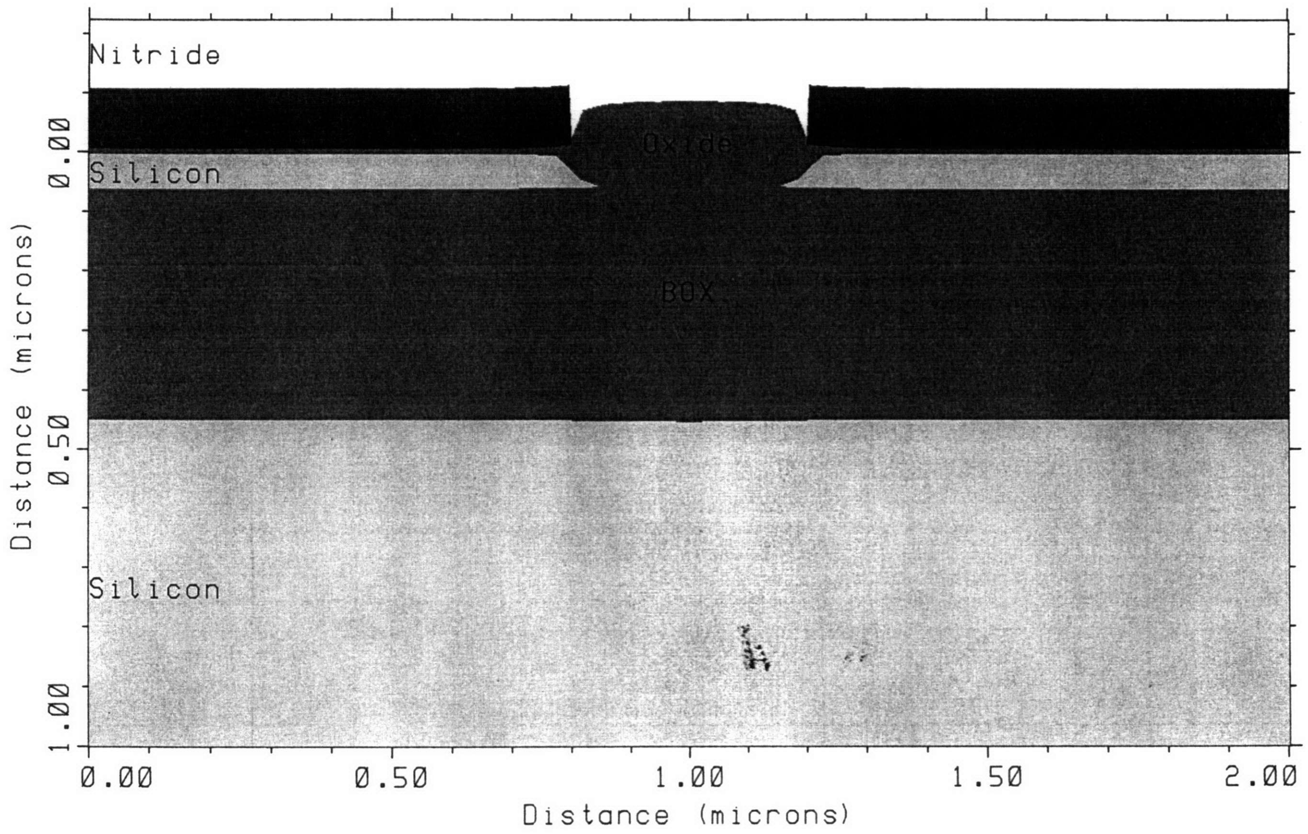
Wafer 10, 37% Over Oxidation, 24 min (VISCOUS Model)



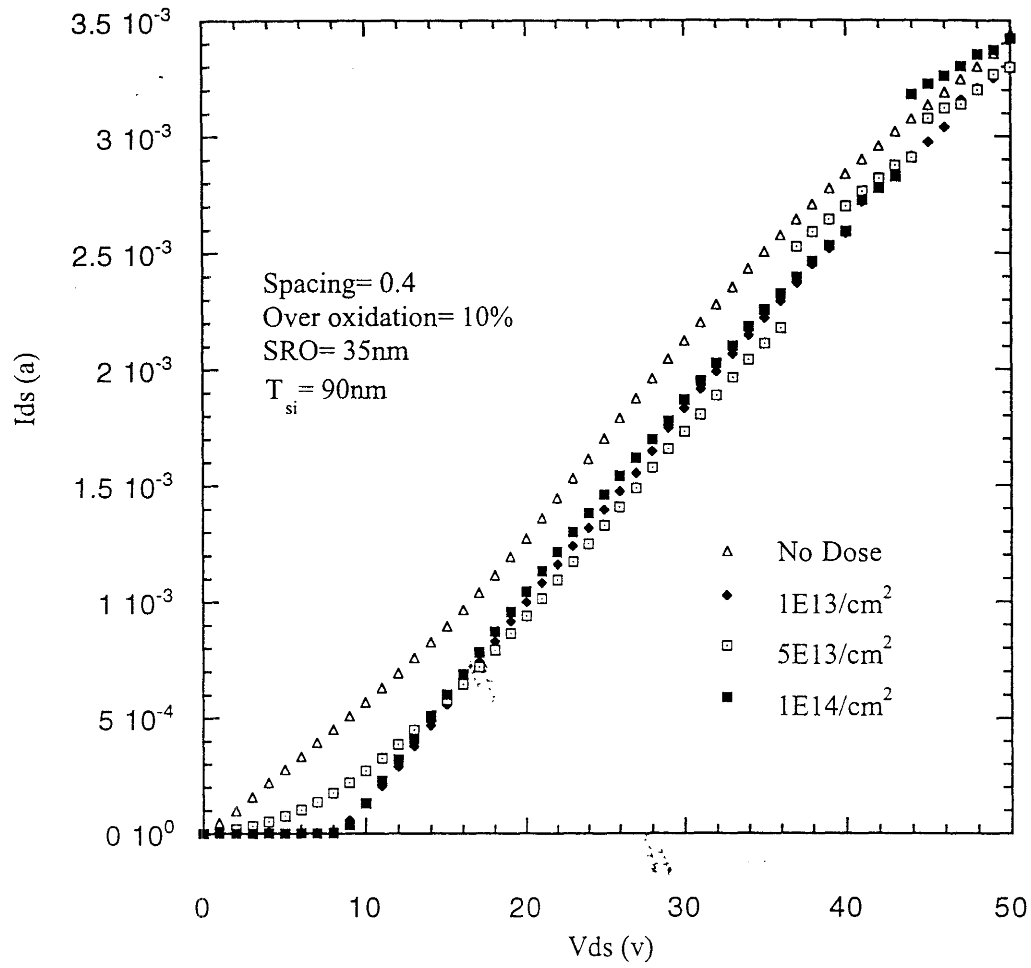
Wafer 11, 27% Over Oxidation, 9.5 min (VISCOUS Model)



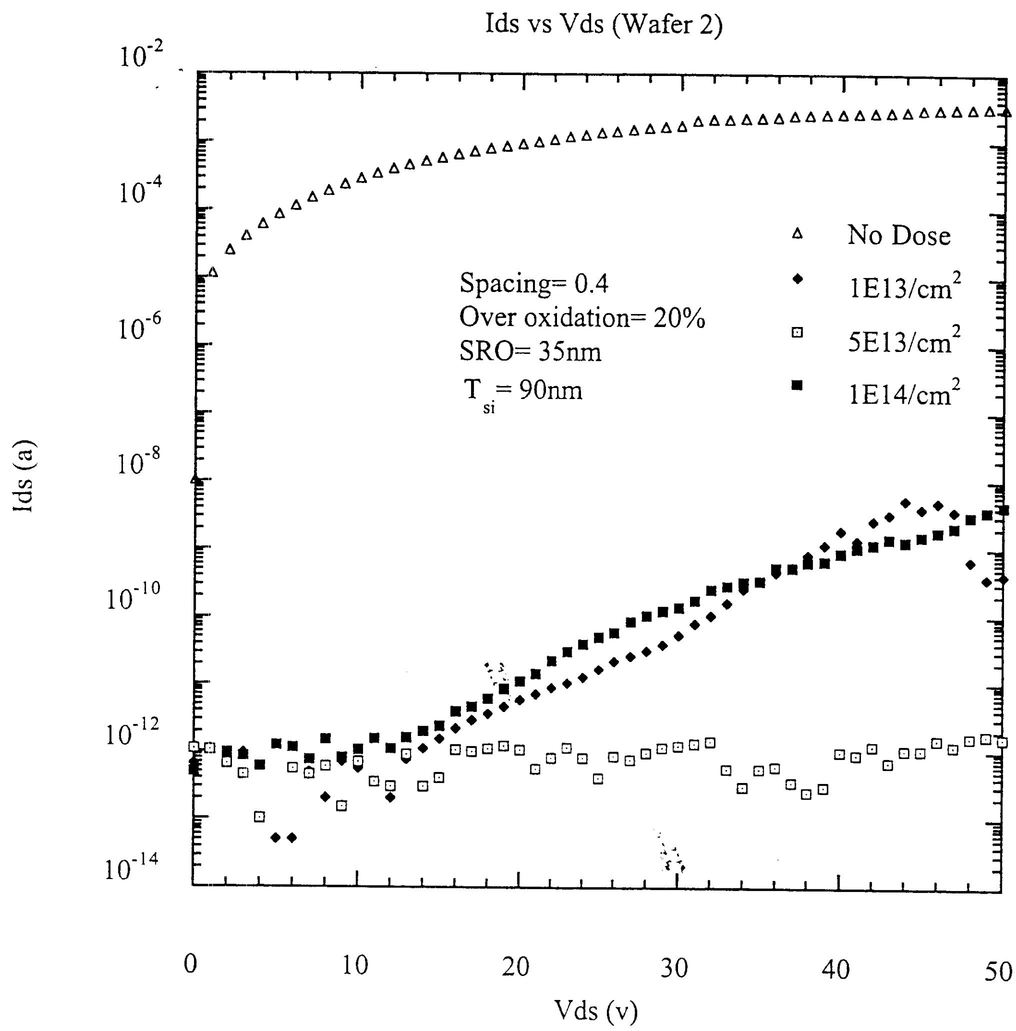
Wafer 12, 37% Over Oxidation, 10.5 min (VISCOUS Model)

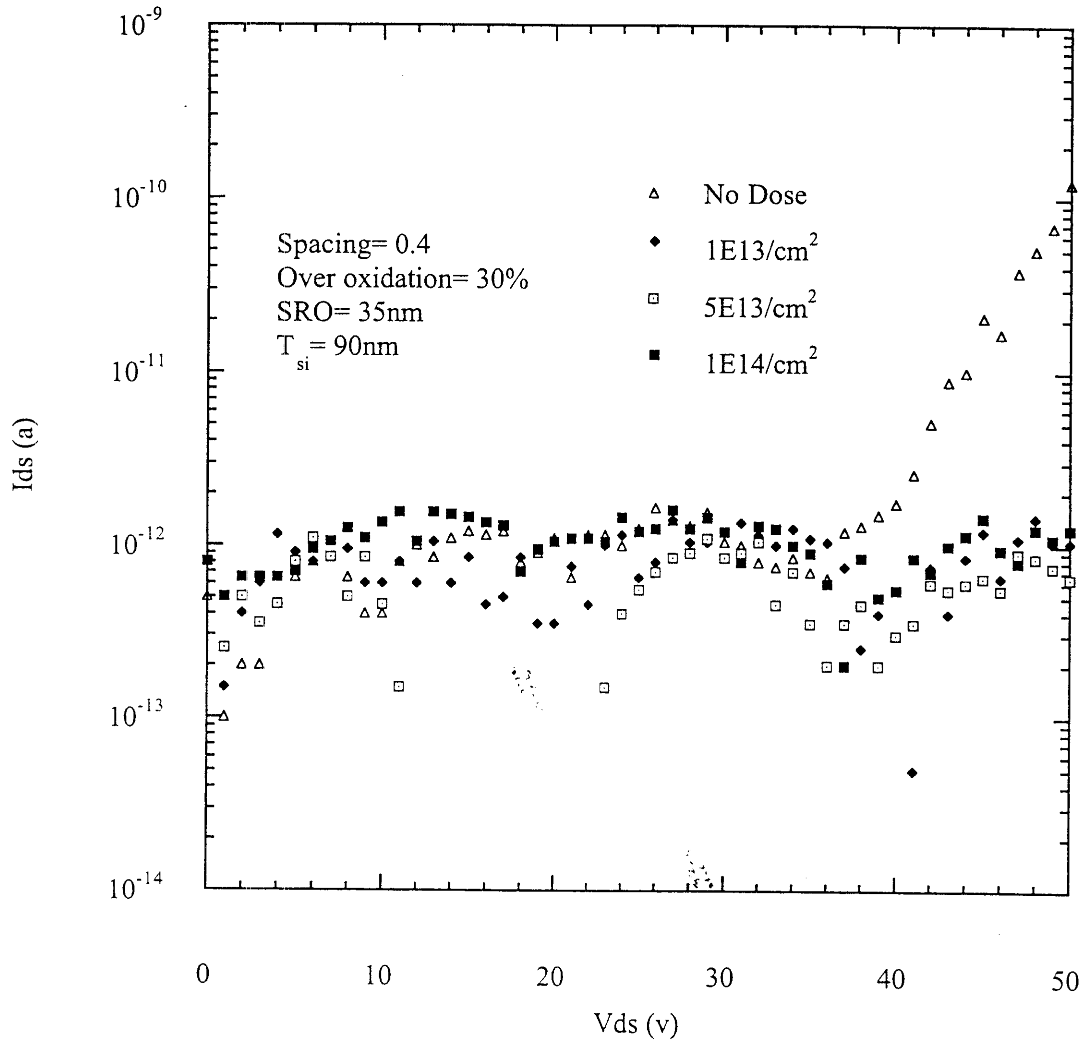


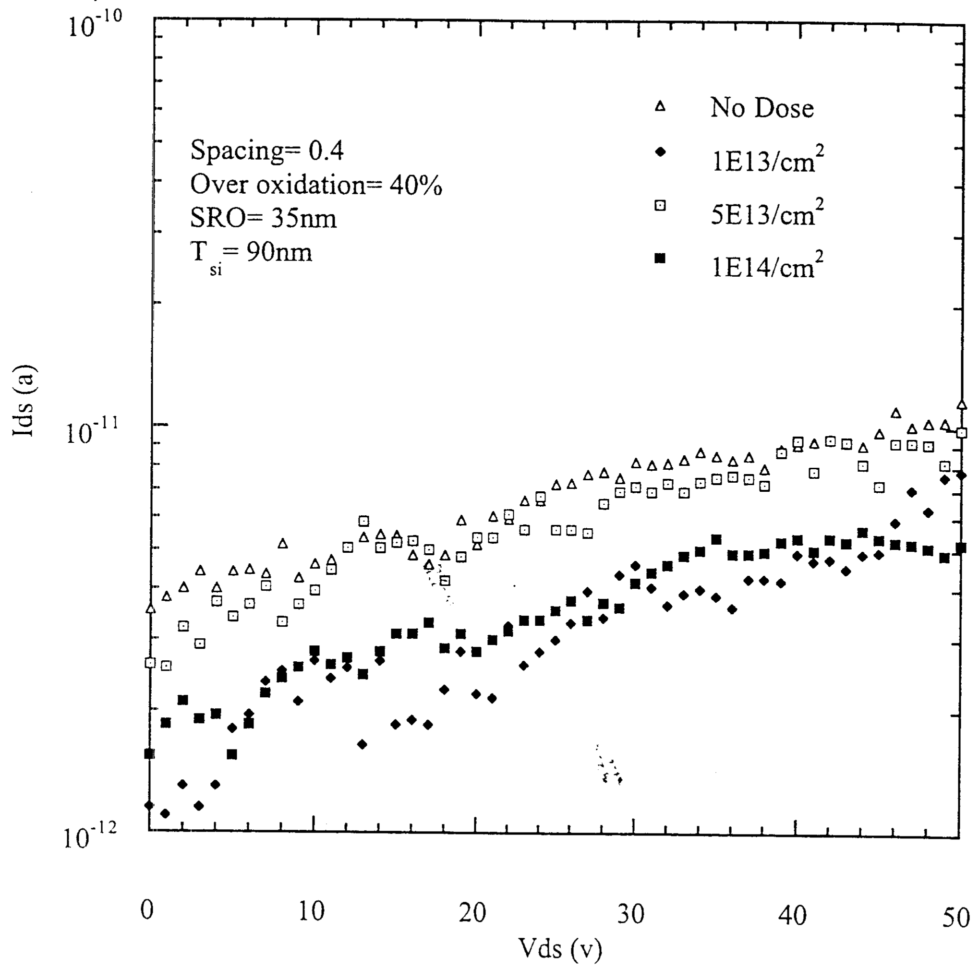
Appendix C
Raw data plots used to define design space

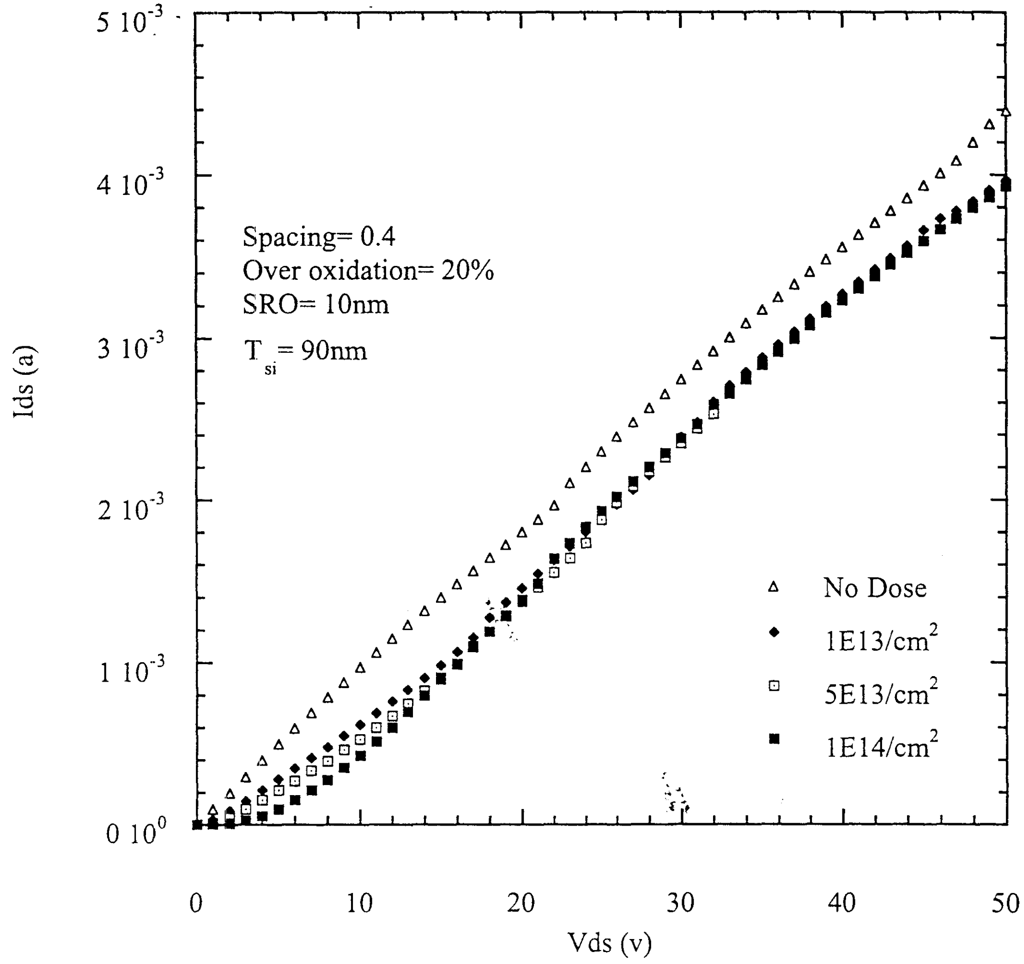


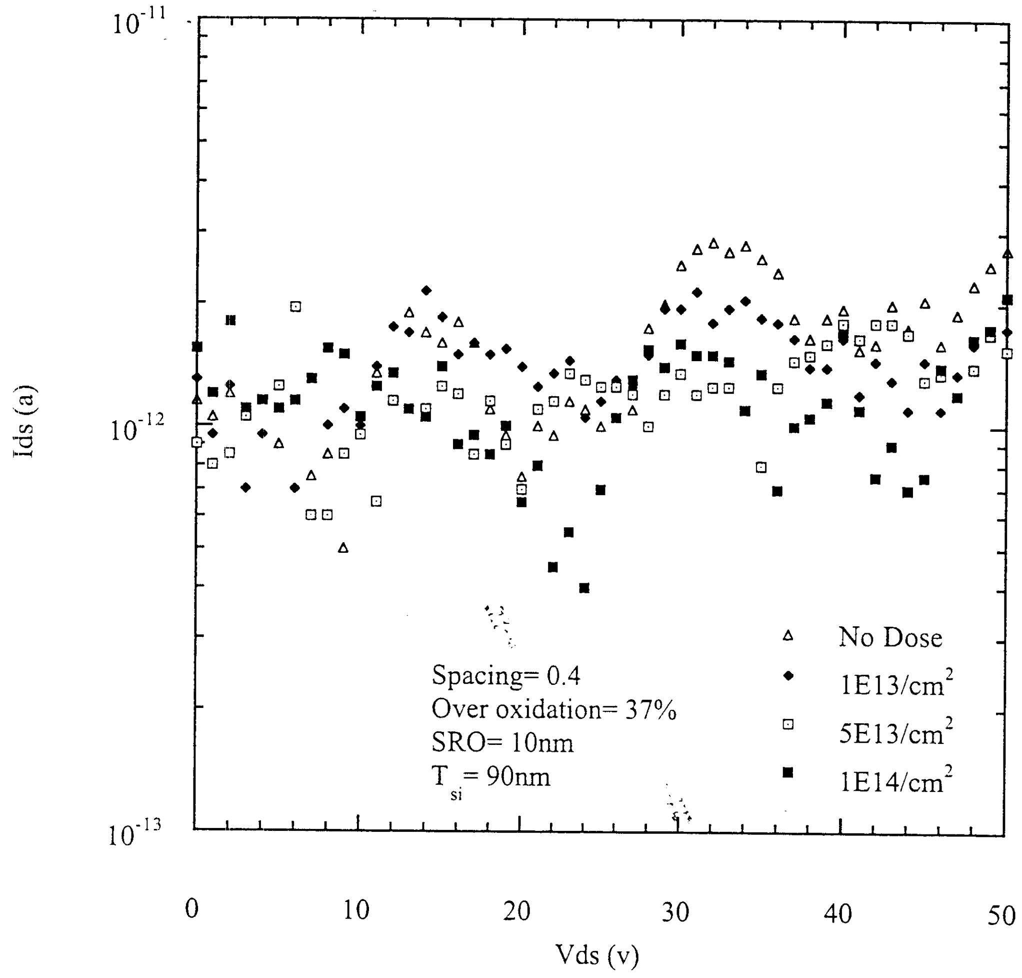
Ids vs Vds (Wafer 1)
3.5 10-3
3 10-3
2.5 10-3
2 10-3
1.5 10-3
1 10-3
5 10-4
0 10^0
Ids (a)
Spacing= 0.4
Over oxidation= 10%
SRO= 35nm
Tsi= 90nm
No Dose
1E13/cm2
5E13/cm2
1E14/cm2
0
10
20
30
40
50
Vds (v)

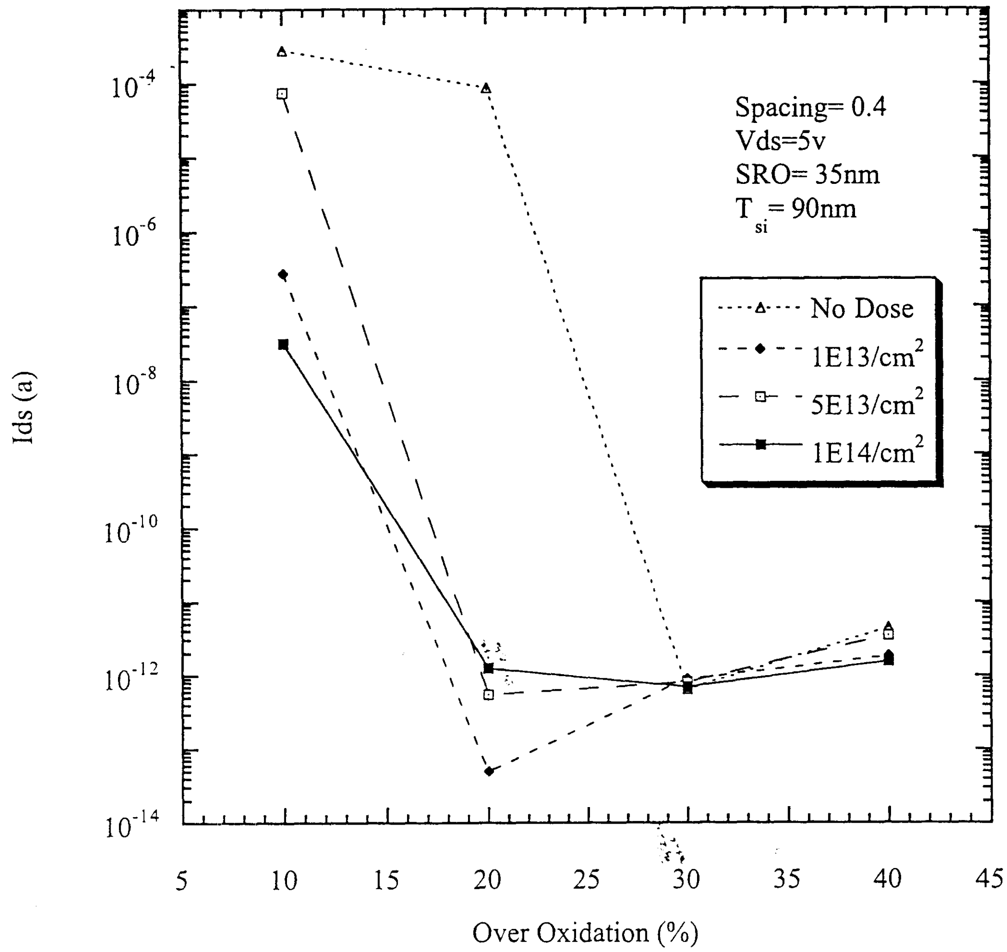

Ids vs Vds (Wafer 2)
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
10^{-14}
Ids (a)
0
10
20
30
40
50
Vds (v)
Spacing= 0.4
Over oxidation= 20%
SRO= 35nm
T_{si}= 90nm
No Dose
$1E13/cm^2$
$5E13/cm^2$
$1E14/cm^2$


Ids vs Vds (Wafer 3)
Spacing= 0.4
Over oxidation= 30%
SRO= 35nm
T si = 90nm
No Dose
1E13/cm2
5E13/cm2
1E14/cm2
Ids (a)
Vds (v)
10-9
10-10
10-11
10-12
10-13
10-14
0
10
20
30
40
50

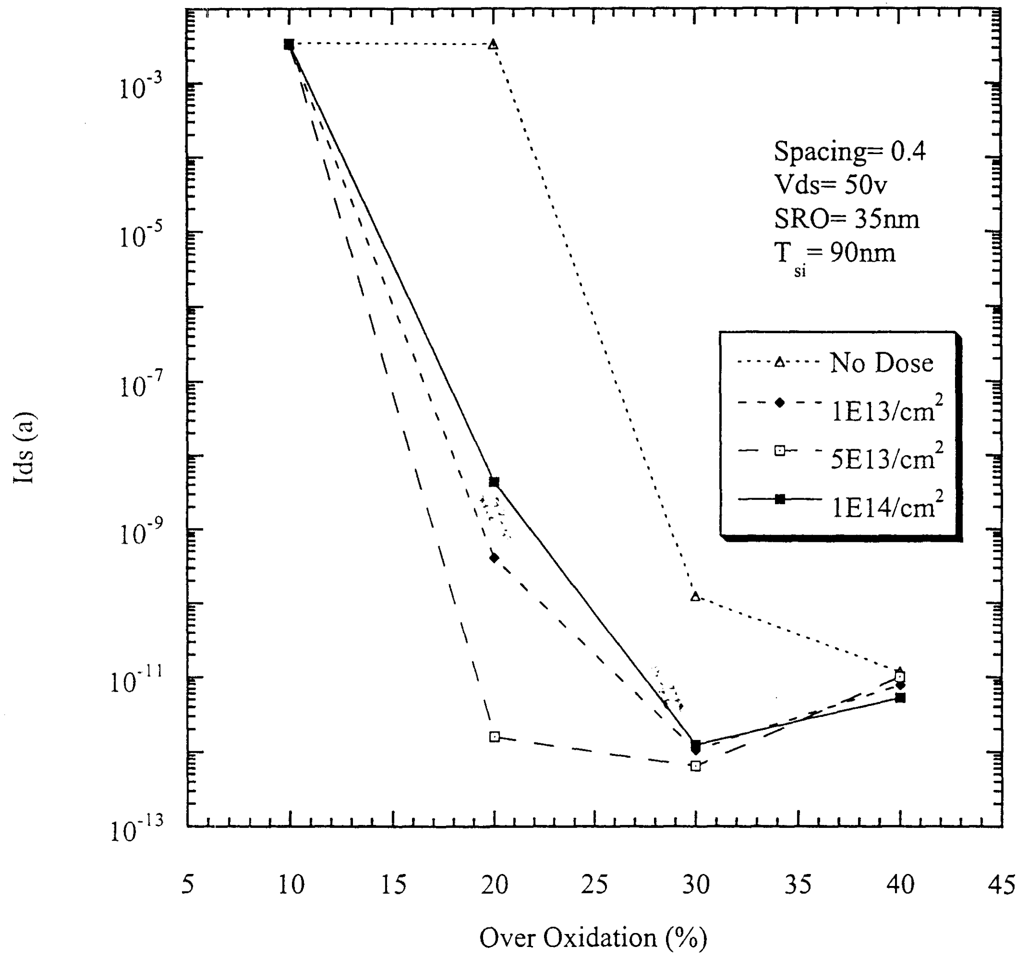

Ids vs Vds (Wafer 4)
No Dose
1E13/cm2
5E13/cm2
1E14/cm2
Spacing= 0.4
Over oxidation= 40%
SRO= 35nm
Tsi = 90nm
Ids (a)
10-10
10-11
10-12
0
10
20
30
40
50
Vds (v)

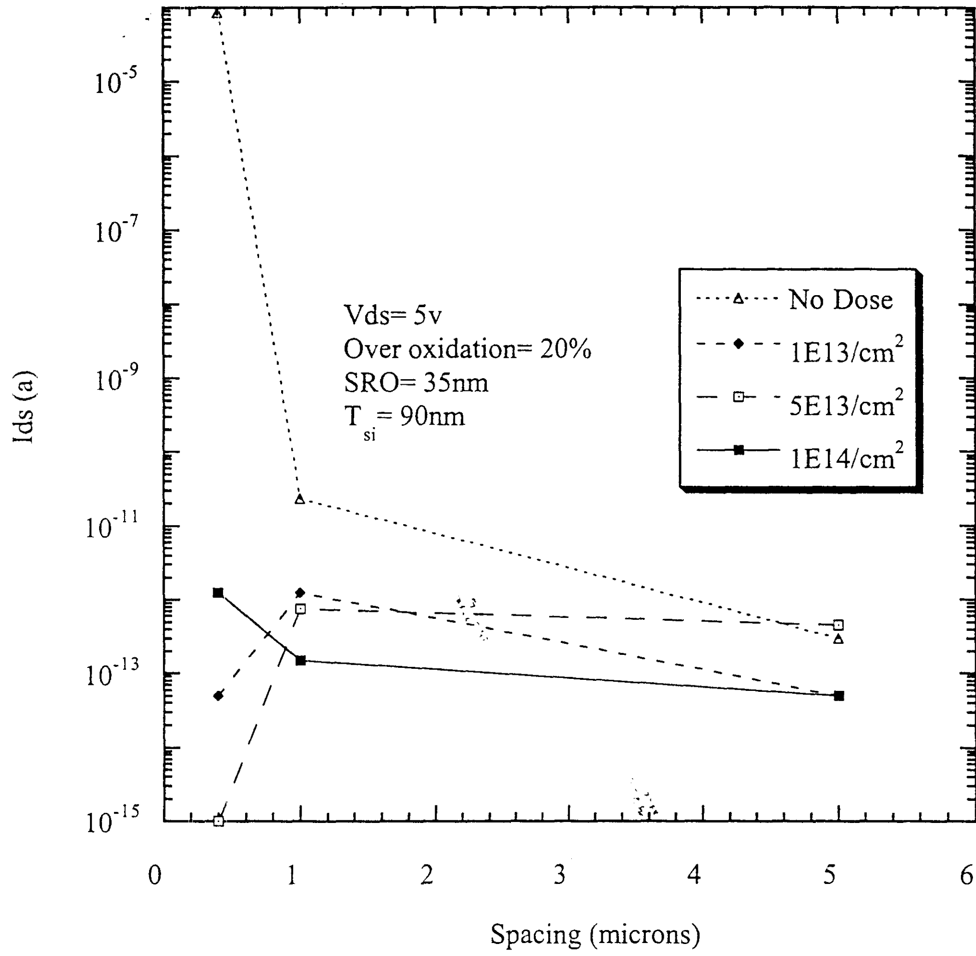

Ids vs Vds (Wafer 9)
5 10^-3
4 10^-3
3 10^-3
2 10^-3
1 10^-3
0 10^0
Ids (a)
Spacing= 0.4
Over oxidation= 20%
SRO= 10nm
T si = 90nm
No Dose
1E13/cm2
5E13/cm2
1E14/cm2
0
10
20
30
40
50
Vds (v)

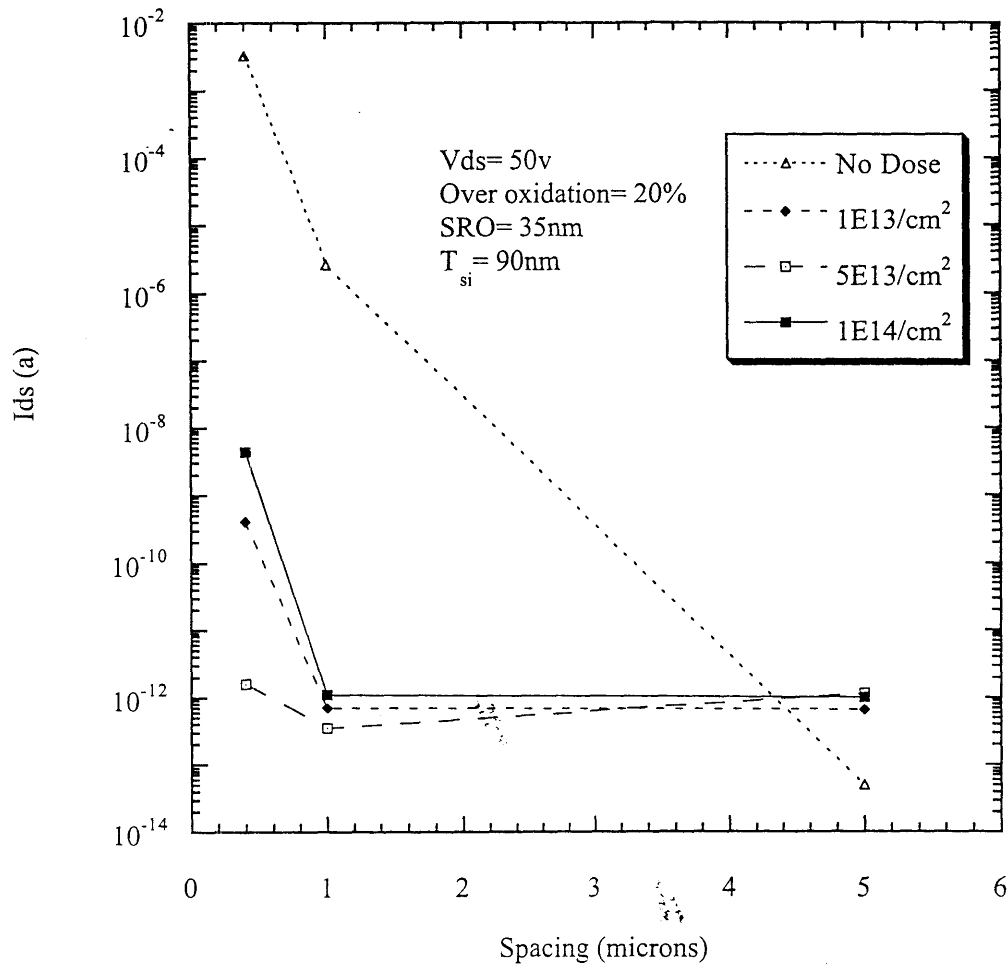

Ids vs Vds (Wafer 10)
10^{-11}
10^{-12}
10^{-13}
Ids (a)
0
10
20
30
40
50
Vds (v)
Spacing= 0.4
Over oxidation= 37%
SRO= 10nm
T_{si}= 90nm
No Dose
1E13/cm^2
5E13/cm^2
1E14/cm^2

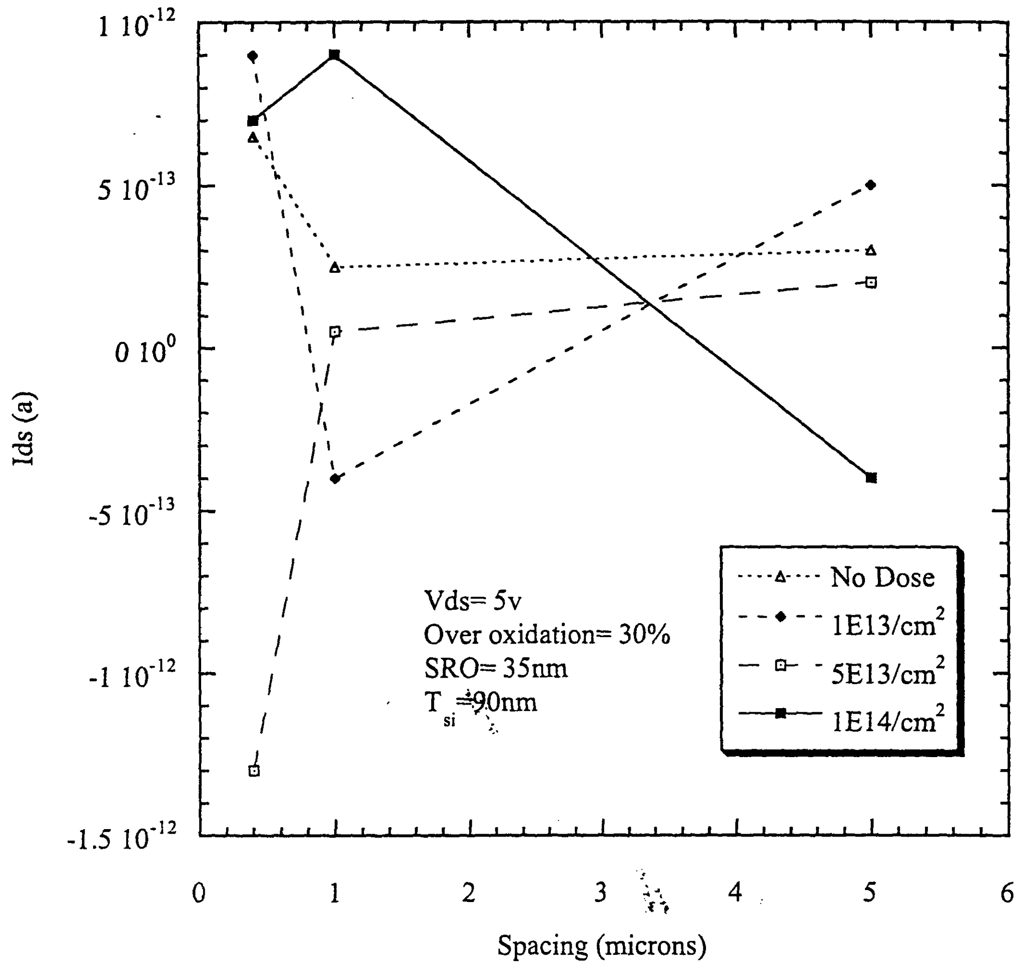


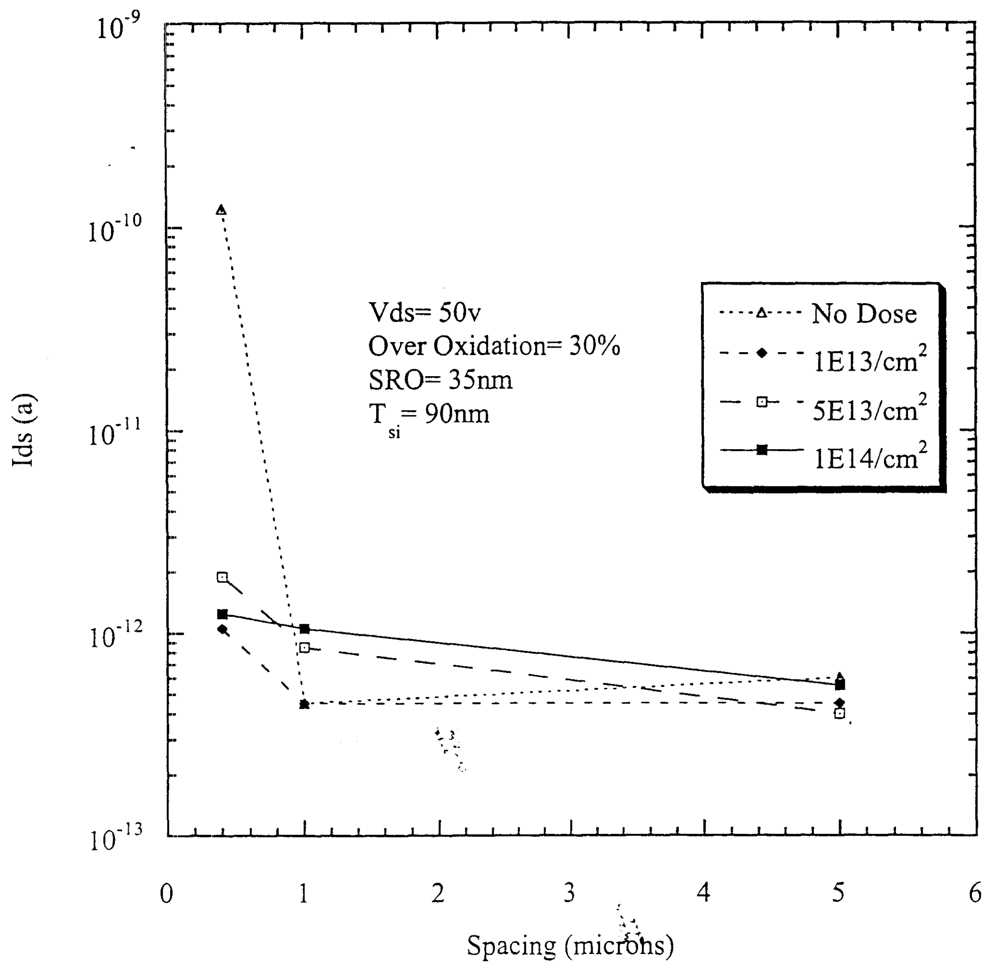
Ids vs % Over Oxidation (Wafers 1-4)
Spacing= 0.4
Vds=5v
SRO= 35nm
T si = 90nm
No Dose
1E13/cm2
5E13/cm2
1E14/cm2
Ids (a)
10-4
10-6
10-8
10-10
10-12
10-14
5
10
15
20
25
30
35
40
45
Over Oxidation (%)

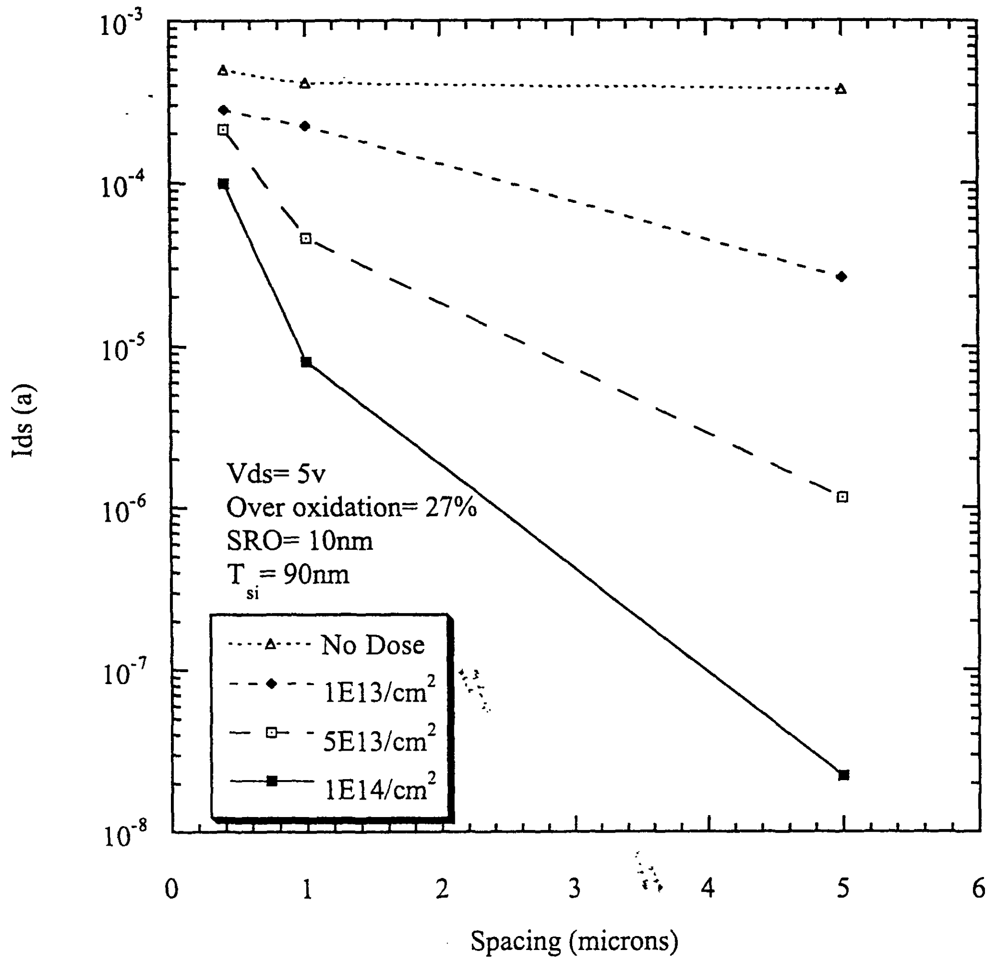

Ids vs % Over Oxidation (Wafers 1-4)
Spacing= 0.4
Vds= 50v
SRO= 35nm
T si = 90nm
No Dose
1E13/cm2
5E13/cm2
1E14/cm2
Ids (a)
10-3
10-5
10-7
10-9
10-11
10-13
5
10
15
20
25
30
35
40
45
Over Oxidation (%)

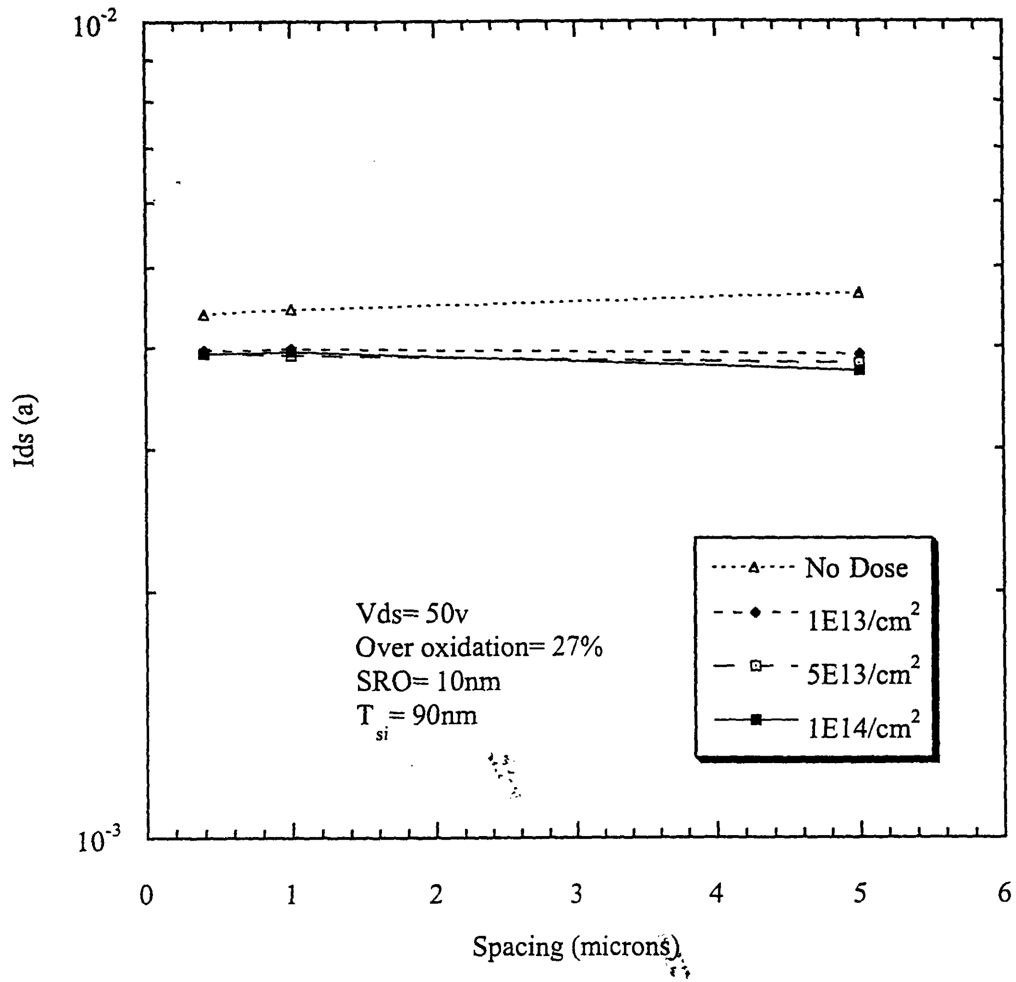

Ids vs Field Spacing (Wafer 2)
Ids (a)
Spacing (microns)
Vds= 5v
Over oxidation= 20%
SRO= 35nm
T si = 90nm
No Dose
1E13/cm2
5E13/cm2
1E14/cm2
10-5
10-7
10-9
10-11
10-13
10-15
0
1
2
3
4
5
6

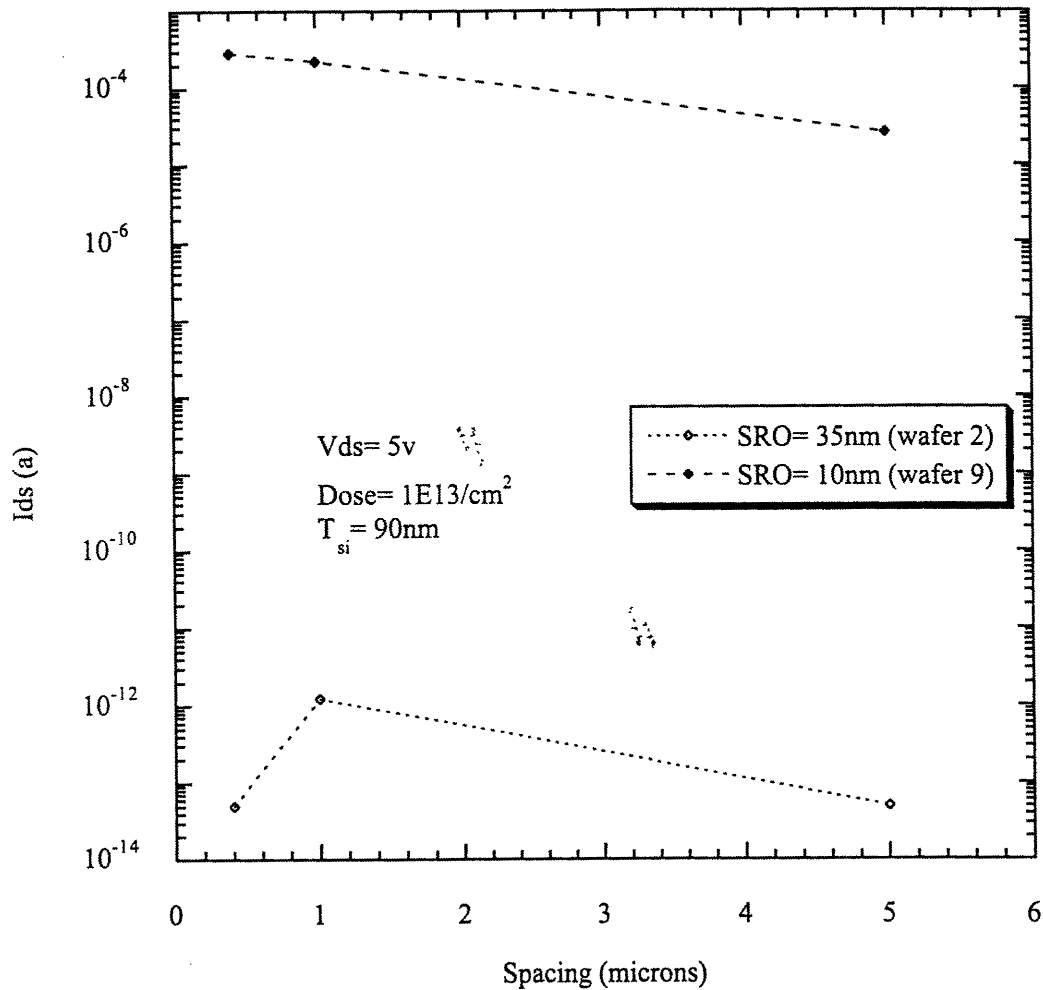

Ids vs Field Spacing (Wafer 2)
Vds= 50v
Over oxidation= 20%
SRO= 35nm
T si = 90nm
No Dose
1E13/cm2
5E13/cm2
1E14/cm2
Ids (a)
10-2
10-4
10-6
10-8
10-10
10-12
10-14
0
1
2
3
4
5
6
Spacing (microns)

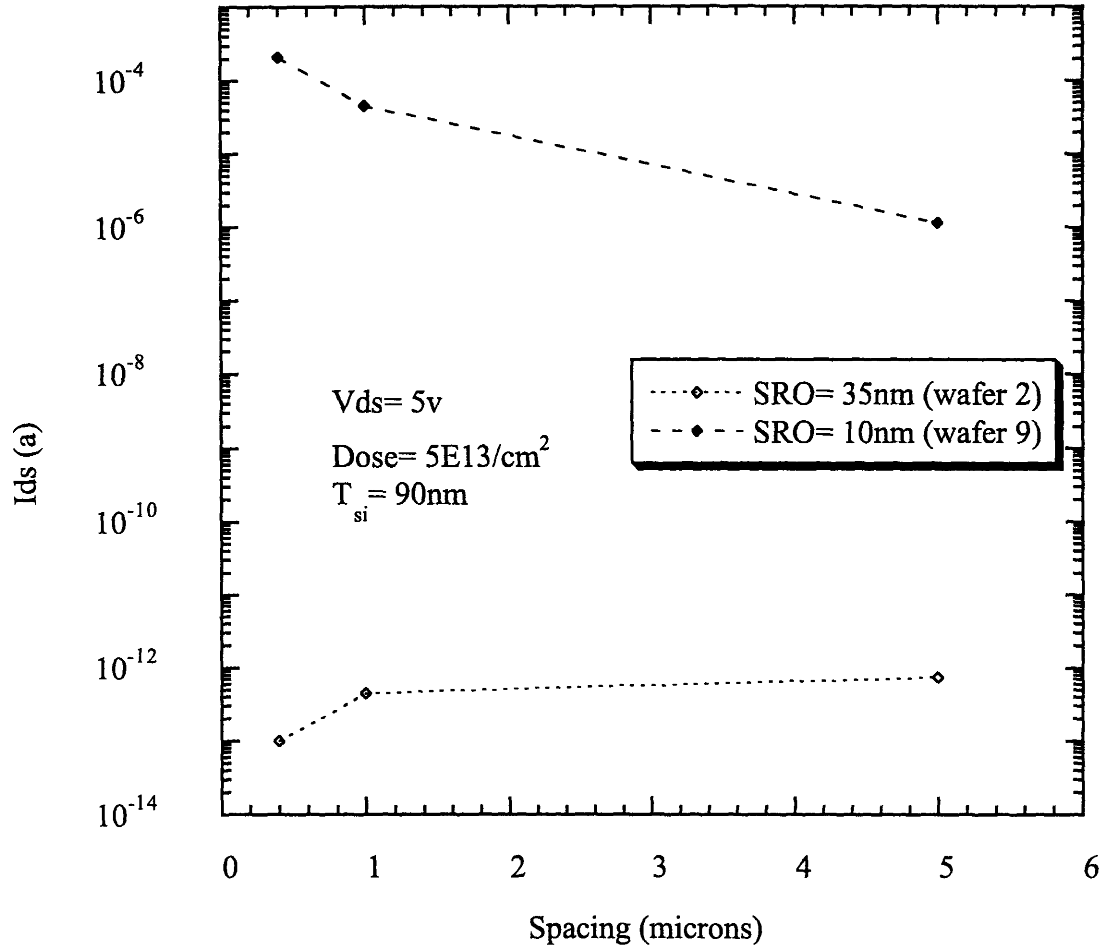

Ids vs Field Spacing (Wafer 3)
1 10-12
5 10-13
0 100
-5 10-13
-1 10-12
-1.5 10-12
Ids (a)
0
1
2
3
4
5
6
Spacing (microns)
Vds= 5v
Over oxidation= 30%
SRO= 35nm
T si =90nm
No Dose
1E13/cm2
5E13/cm2
1E14/cm2


Ids vs Field Spacing (Wafer 3)
Vds= 50v
Over Oxidation= 30%
SRO= 35nm
T si = 90nm
No Dose
1E13/cm2
5E13/cm2
1E14/cm2
Ids (a)
Spacing (microns)
10-9
10-10
10-11
10-12
10-13
0
1
2
3
4
5
6

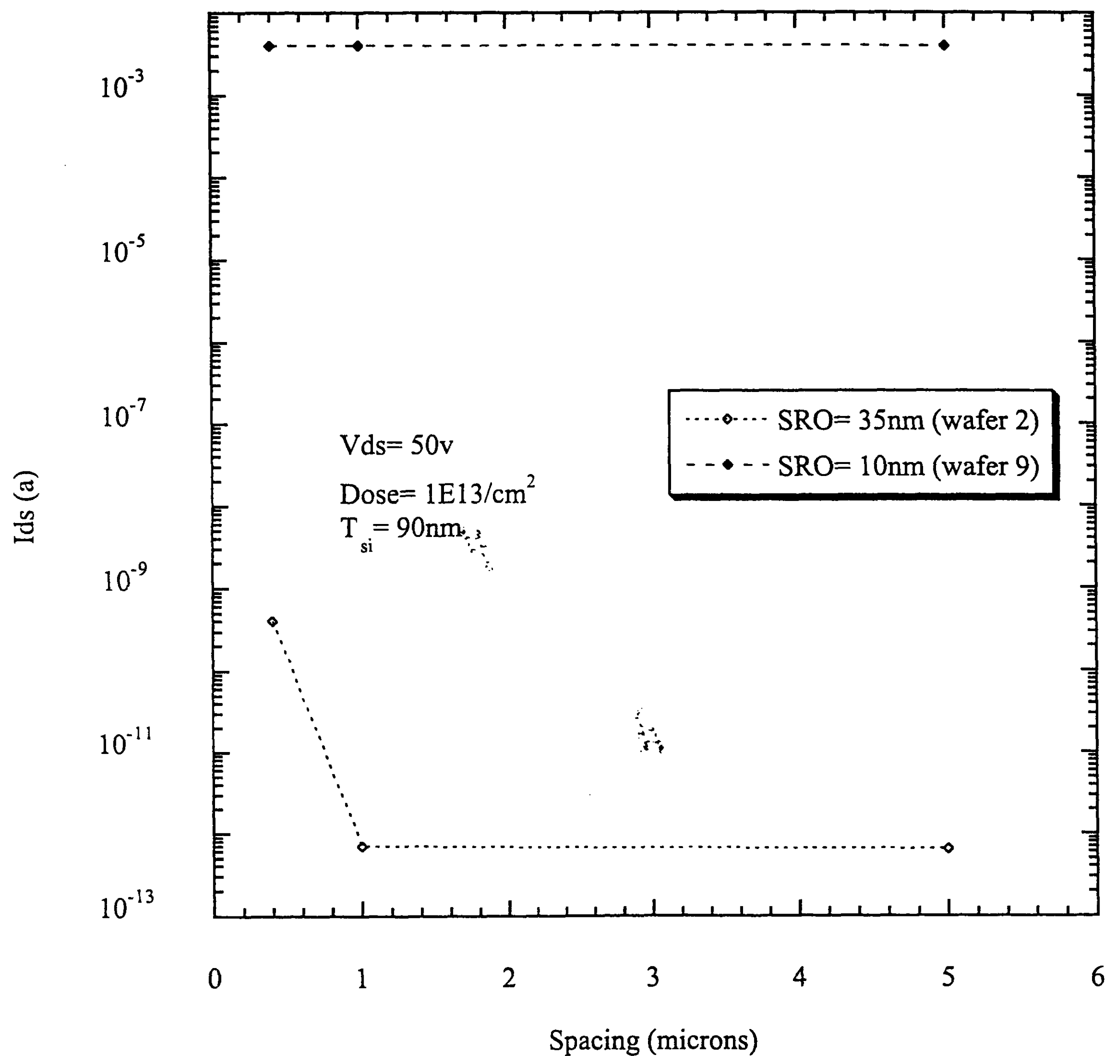

Ids vs Field Spacing (Wafer 9)
Ids (a)
Spacing (microns)
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
0
1
2
3
4
5
6
Vds= 5v
Over oxidation= 27%
SRO= 10nm
T_{si} = 90nm
No Dose
1E13/cm^2
5E13/cm^2
1E14/cm^2

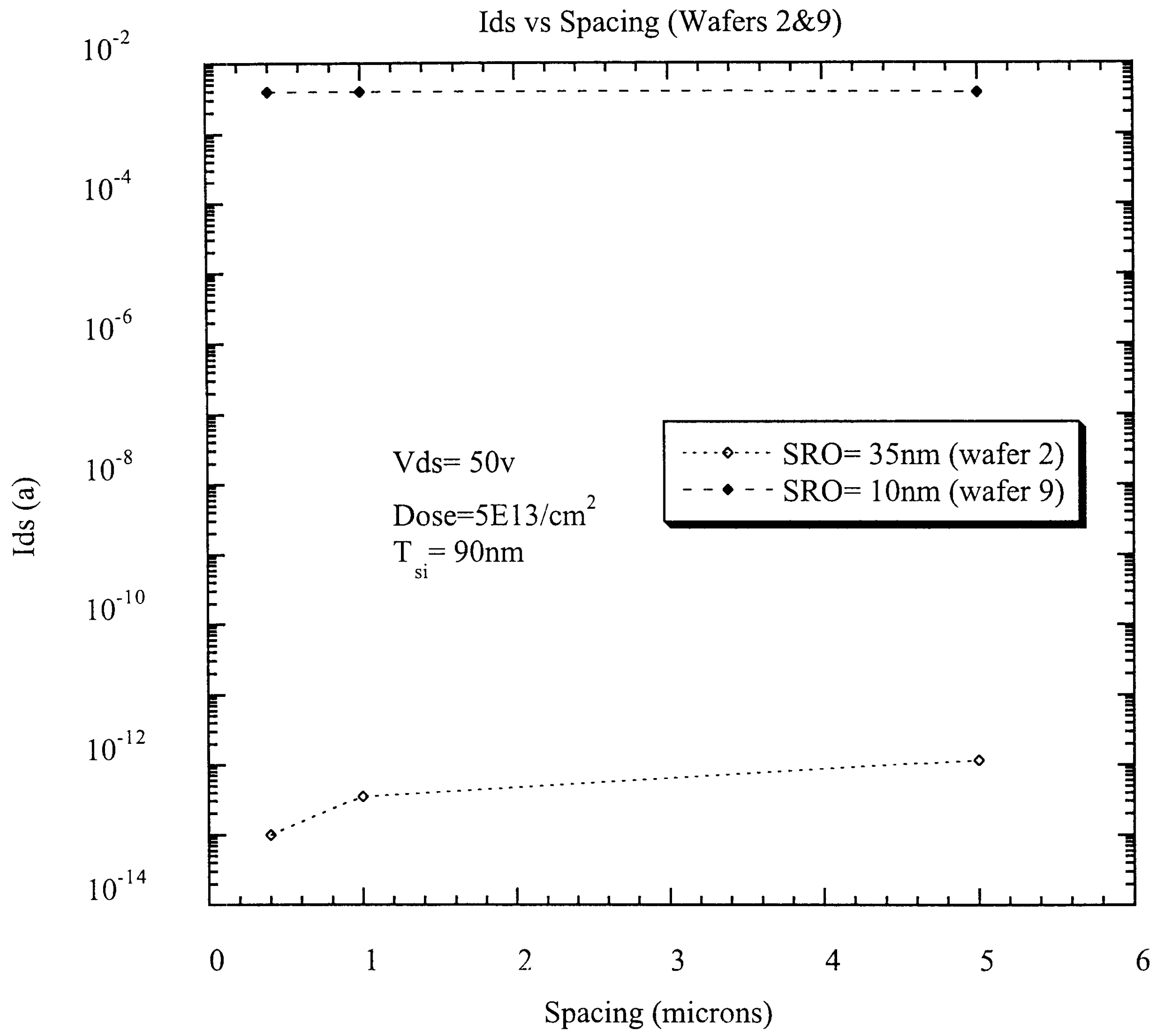

Ids vs Field Spacing (Wafer 9)
10^-2
10^-3
Ids (a)
Vds= 50v
Over oxidation= 27%
SRO= 10nm
T si = 90nm
No Dose
1E13/cm2
5E13/cm2
1E14/cm2
0
1
2
3
4
5
6
Spacing (microns)


Ids vs Spacing (Wafers 2&9)
Ids (a)
10^-4
10^-6
10^-8
10^-10
10^-12
10^-14
Vds= 5v
Dose= 1E13/cm^2
T_si= 90nm
SRO= 35nm (wafer 2)
SRO= 10nm (wafer 9)
0
1
2
3
4
5
6
Spacing (microns)

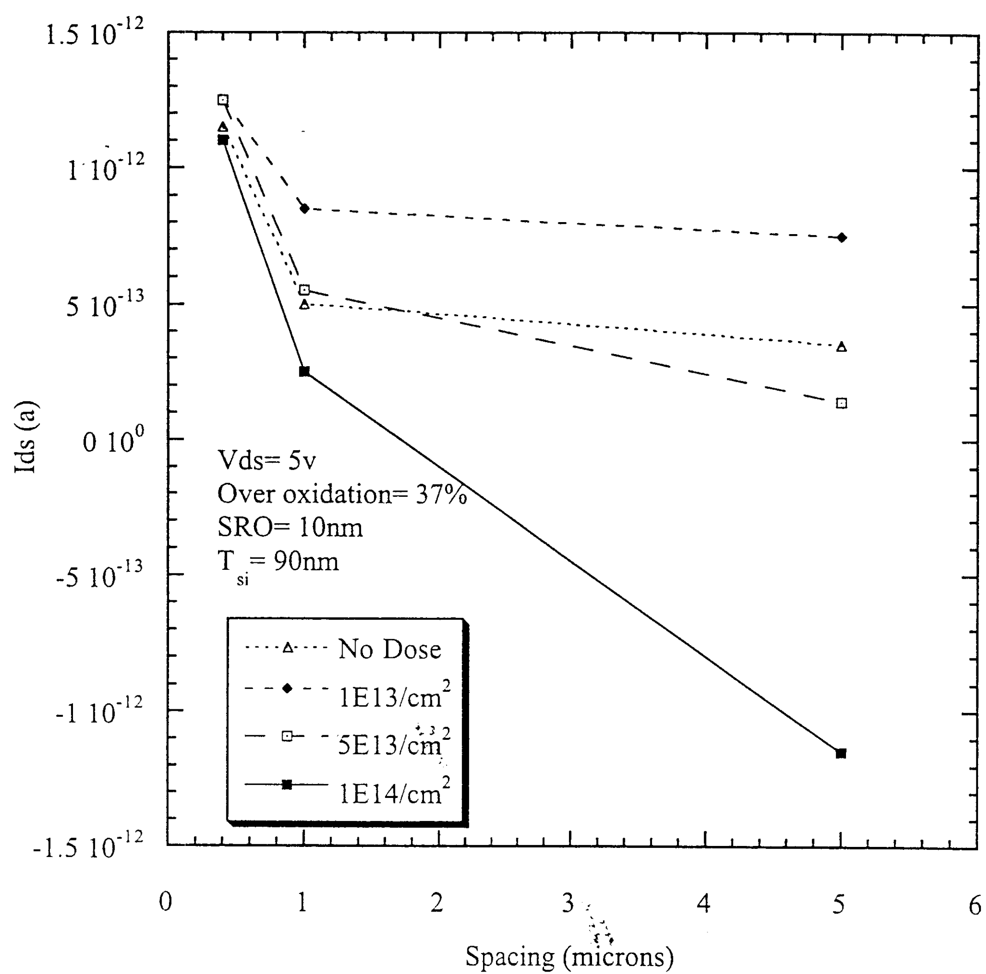


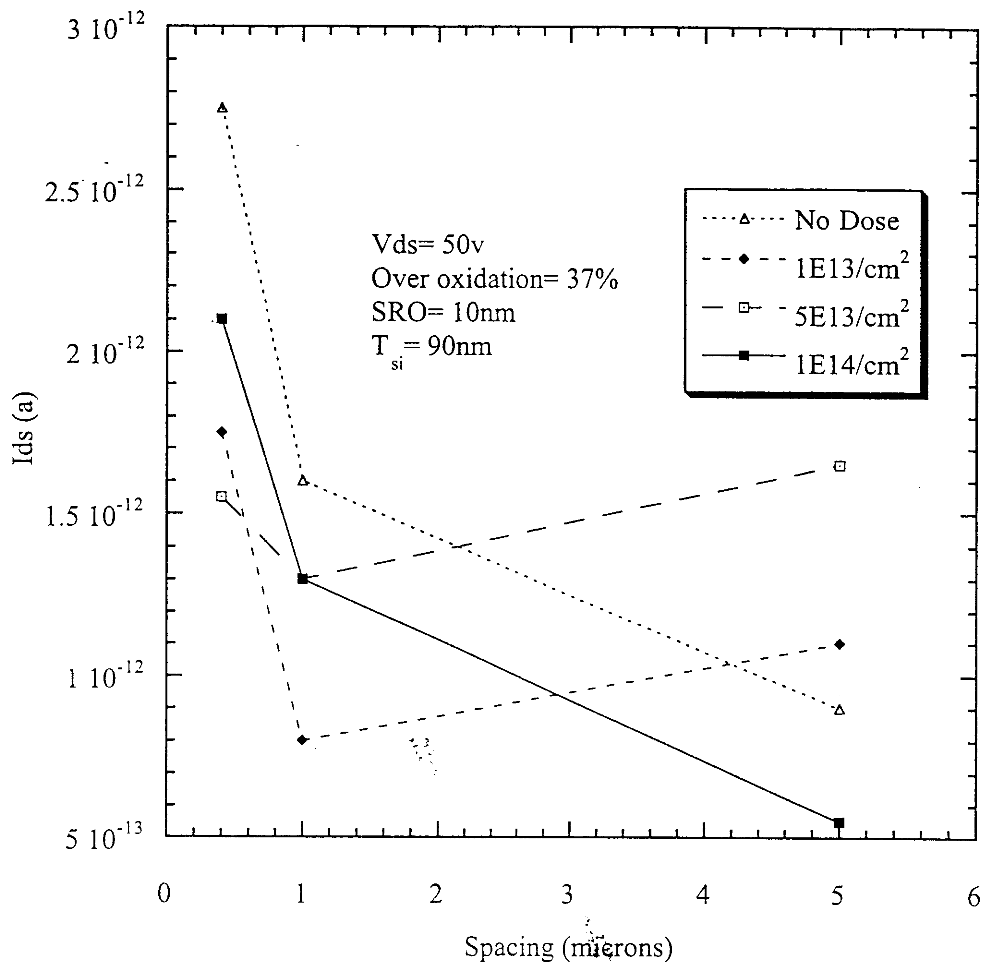
Ids vs Spacing (Wafers 2&9)
Ids (a)
10^-4
10^-6
10^-8
10^-10
10^-12
10^-14
Vds= 5v
Dose= 5E13/cm^2
T_si = 90nm
SRO= 35nm (wafer 2)
SRO= 10nm (wafer 9)
0
1
2
3
4
5
6
Spacing (microns)


Ids vs Spacing (Wafers 2&9)
Ids (a)
10-3
10-5
10-7
10-9
10-11
10-13
0
1
2
3
4
5
6
Spacing (microns)
Vds= 50v
Dose= 1E13/cm2
Tsi = 90nm
SRO= 35nm (wafer 2)
SRO= 10nm (wafer 9)



Ids vs Spacing (Wafers 2&9)
10-2
10-4
10-6
10-8
10-10
10-12
10-14
Ids (a)
Vds= 50v
Dose=5E13/cm2
Tsi= 90nm
SRO= 35nm (wafer 2)
SRO= 10nm (wafer 9)
0
1
2
3
4
5
6
Spacing (microns)


Ids vs Field Spacing (Wafer 10)
1.5 10-12
1 10-12
5 10-13
0 10^0
-5 10-13
-1 10-12
-1.5 10-12
Ids (a)
Vds= 5v
Over oxidation= 37%
SRO= 10nm
Tsi= 90nm
No Dose
1E13/cm2
5E13/cm2
1E14/cm2
0
1
2
3
4
5
6
Spacing (microns)


Ids vs Field Spacing (Wafer 10)
3 10-12
2.5 10-12
2 10-12
1.5 10-12
1 10-12
5 10-13
Ids (a)
Vds= 50v
Over oxidation= 37%
SRO= 10nm
T si = 90nm
No Dose
1E13/cm2
5E13/cm2
1E14/cm2
0
1
2
3
4
5
6
Spacing (microns)