

Inductance Cancellation Techniques with Application to EMI Filters and Components

by

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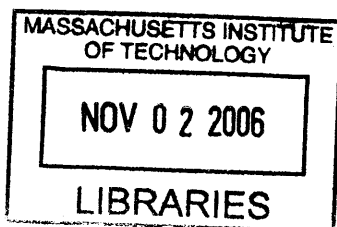
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Abstract

Inherent parasitic effects in passive circuit components, such as the equivalent parallel capacitance of magnetic windings and the equivalent series inductance (ESL) of capacitors, become dominant factors limiting the attenuation of high frequency signals in power filter networks. These limitations have generated recent interest in methods for compensating or mitigating parasitics to increase filter performance, including the use of coupled magnetic windings to cancel the effects of capacitor parasitic inductance. The use of these inductance cancellation windings allows for a reduction in filter volume and cost and/or an increase in its attenuation performance.

This thesis extends the efficacy of inductance cancellation techniques by enhancing the manufacturability and usability of self-contained integrated filter elements, and by more effectively addressing cancellation in common- and differential-mode filter topologies, such as those designed for reducing electromagnetic interference (EMI).

A design methodology and fabrication process is presented for packaging a capacitor and matched inductance cancellation winding together to create a self-contained integrated filter element. Experimental results from the creation of three independent designs clearly illustrate the high level of performance and repeatability that is achievable.

Discrete magnetic windings are used to implement inductance cancellation in filter topologies designed to attenuate both common- and differential-mode signals. The number of capacitors required for even simple designs motivate the use of a single cancellation winding for two capacitors. An analytical model along with extensive experimental results successfully demonstrate. This approach is demonstrated in an adaptation of a commercially-available EMI filter.

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Introduction

THE size and cost of electronic equipment is often dominated by energy processing circuits, as opposed to signal processing circuits. These energy processing circuits, which include passive devices such as inductors and capacitors, represent a large portion of the physical volume of electronic devices. These passive components provide intermediate energy storage to reduce current and voltage ripple and high-frequency noise.

One place where passive components are used heavily is in filters designed to minimize electromagnetic interference (EMI). Minimizing electromagnetic interference is an important consideration in the design of electronic equipment as compliance with standards, such as the Conformité Européene (CE Mark) in the European Union or the Federal Communications Commission (FCC) Part 15 in the United States, must be obtained to allow for product commercialization. The standards set by governing bodies limit the maximum allowable electromagnetic emissions to prevent unintended, and undesirable, interference between electronic devices.

Unlike integrated circuit and semiconductor technology, which has advanced at a rapid pace, the performance of passive components has progressed relatively slowly in comparison. Parasitic effects, such as the parallel capacitance of magnetic windings and the equivalent series inductance (ESL) of capacitors, become dominant factors limiting the attenuation of high frequency signals that can contribute to EMI [1–12]. These limitations have generated recent interest in methods for compensating parasitics to increase filter performance [1, 6–13]. For example, as shown in [1, 6, 7] and summarized in the following section, coupled magnetic windings can be used to cancel the effects of capacitor parasitic inductance. The use of these inductance cancellation windings allows for a reduction in filter volume and cost and/or an increase in its attenuation performance.

1.1 Inductance Cancellation

Consider the second-order low-pass LC filter in Fig. 1.1(a), shown with the first-order capacitor parasitics of equivalent series resistance (ESR) and equivalent series inductance (ESL). At high frequencies the equivalent series inductance of the capacitor causes an increase in the capacitor’s impedance, greatly reducing the filtration performance in the region that it is most desired. The first trace in Fig. 1.2 shows the effect of this increased impedance on the attenuation performance of the simple LC filter like that in Fig 1.1(a). To compensate for the parasitic effects of the capacitor, additional capacitors with higher-frequency resonant modes are normally connected in parallel with the main capacitor, increasing the circuit size and cost.

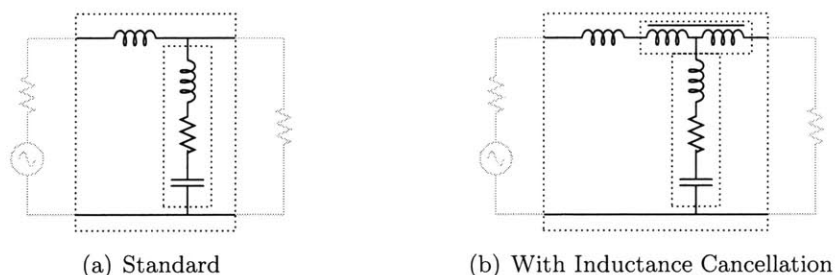


Figure 1.1: Low-pass filter models with first-order capacitor parasitics.

An alternative to adding additional capacitors is to try to reduce the effects of the device parasitics. An example of the performance that can be achieved with reduced parasitic inductance can be seen in the second trace of Fig. 1.2. To achieve this performance, a coupled inductor structure can be inserted into the circuit to induce a voltage that counteracts the voltage due to capacitor equivalent series inductance [1, 6, 7], shown in Fig. 1.1(b). The designed cancellation effect can be achieved using the mutual coupling of magnetic flux between the coupled inductor windings, illustrated in Fig. 1.3.

If the coupled inductors of Fig. 1.3 are treated as windings of a transformer, the circuit model in Fig. 1.4(a) can be used. Analyzing this circuit, one can generate a two-port equivalent ‘T’ model shown in Fig. 1.4(b), where the terminal relationships are given by:

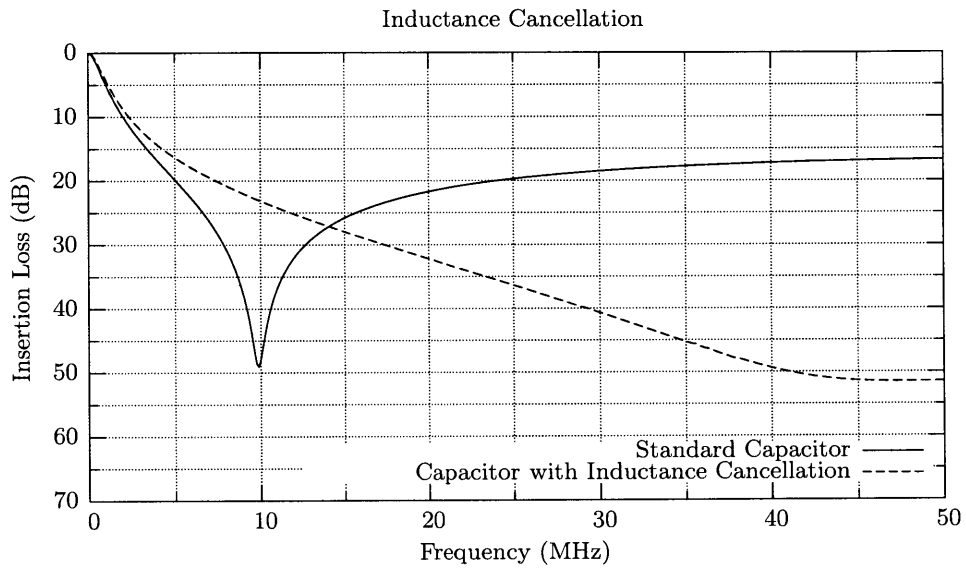


Figure 1.2: Measured results from the low-pass filters in Fig. 1.1 showing the difference in performance between a circuit with a standard capacitor and one with inductance cancellation.

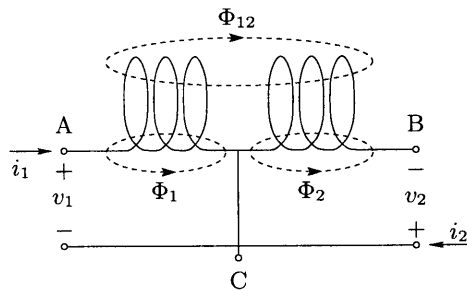


Figure 1.3: Flux linkage in “center-tapped” magnetically coupled windings.

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \quad (1.1)$$

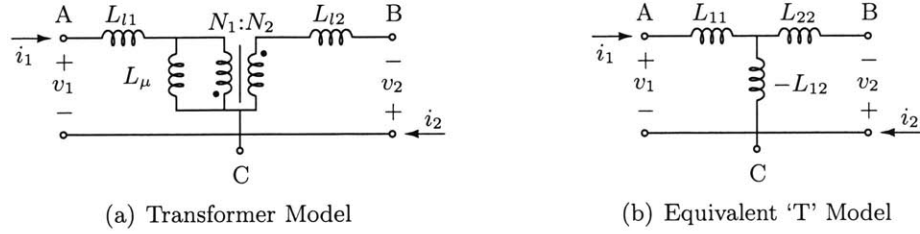


Figure 1.4: Models of center-tapped magnetically coupled windings.

From this model, it can be seen that the induced voltage at the common terminal appears as a negative branch inductance in the equivalent T-model of the coupled magnetic windings [1]. This negative inductance is used to compensate for a device's parasitic inductance, creating a three terminal component with drastically reduced, or in some cases completely eliminated, equivalent shunt path inductance. Fig. 1.5 shows this compensated filter with the coupled magnetic winding represented by its equivalent T model.

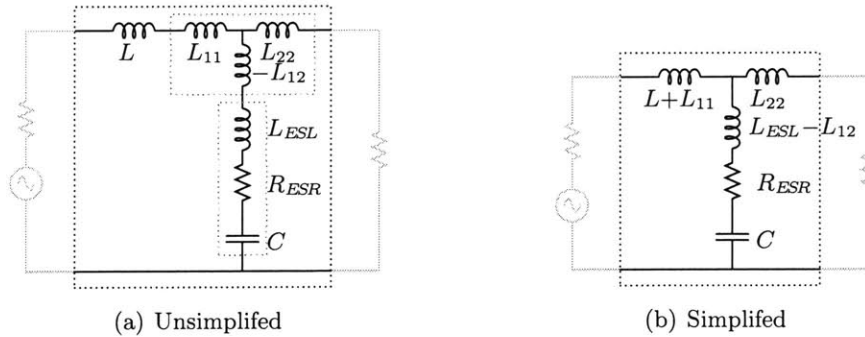


Figure 1.5: LC Low-pass filters with inductance cancellation.

A side effect of the introduction of the magnetic winding is the additional inductance in both branches of the series path of the filter. Conservation of energy dictates that the mutual coupling between the windings can be no greater than the geometric mean of the self-inductances L_{11} and L_{22} . The relationship can be written as

$$L_M \leq k_{12} \sqrt{L_{11} L_{22}} \quad (1.2)$$

where k_{12} is the coupling factor between L_{11} and L_{22} , and bounded by $0 \leq k_{12} \leq 1$. Energy conservation also ensures that the matrix L in (1.1) is positive semidefinite.

This additional series inductance limits the applications where inductance cancellation can be useful [14], however filtering is one application where it is often advantageous. The attenuation of a filter is determined by the ratio of the series-path to the shunt-path impedance, so the additional series inductance, however small, serves to improve the attenuation.

1.2 Thesis Objectives and Organization

The objective of this research is to extend the inductance cancellation approach outlined here, with focus placed on enhancing the manufacturability and usability of integrated filter elements, and on more effectively addressing common- and differential-mode filter topologies, such as those designed for attenuating EMI.

The primary results of the work presented in this thesis can be separated into three main areas: integrated filter element fabrication, balanced inductance cancellation, and multiple capacitor inductance compensation.

Chapter 2 develops a method for the design and fabrication of an integrated filter element, a three-terminal device including a capacitor and an inductance cancellation winding. Chapter 4 extends this design to a four-terminal element by incorporating an additional cancellation winding. The primary development of this chapter involves exploiting the magnetic coupling between the two windings to increase the effective mutual inductance in each.

Chapter 3 uses discrete windings to implement inductance cancellation in filters designed to attenuate EMI. The number of capacitors required for common- and differential-mode filtering motivates the use of a single coil for two capacitors, and the discrete winding approach integrates well into the assembly procedure for many EMI filters.

Finally, Chapter 5 concludes this thesis.

Integrated Filter Element Fabrication

CHAPTER 1 illustrated the basis for inductance cancellation, and this chapter provides an implementation of the technique. Previous work has covered two methods for implementing the magnetic windings: incorporating the windings onto the printed circuit board [6, 14], and embedding the windings within the capacitor to form an integrated filter [1, 14]. This chapter further develops the second method by realizing a low-cost repeatable process for constructing and incorporating a magnetic winding with a capacitor, extending previous work in this area [14]. Together, the winding and capacitor are referred to as integrated filter element.

2.1 Motivation

When implementing inductance cancellation, a trade-off is made on the design of the magnetic windings. Repeatability is a primary concern, as deviation in the value of cancellation can have a significant impact on the realized performance [6]. Printed circuit board windings provide a consistent, repeatable structure which results in a very small variance, but can require a significant board footprint and must be re-designed for each circuit.

To reduce the board space required, as well as free the circuit designer from the burden of implementing and refining winding designs, an effective method to integrate the cancellation winding into the capacitor is sought. Integrating the capacitor and winding together would create a self-contained filter element that could be used in existing circuit designs with little modification, assuming that a repeatable construction method is developed.

2.2 Design Methodology

Developing a process to construct the filter elements depends greatly on the size and shape of the capacitor, as well as the required size of the inductance cancellation winding. This thesis focuses primarily on applications to EMI filters, and for this reason, two capacitors are chosen which share a number of characteristics with the capacitors used in most EMI filters.

Vishay BCcomponents Series MKP338 capacitors in 330nF and 1.0 μ F, part numbers 2222-338-24334 and 2222-338-24105 respectively, are X2 rated film capacitors, indicating they are approved for both line-to-line and line-to-ground connections. These capacitors are formed by rolling a long sheet of metalized polyester film into an oblong cylinder, sputtering metal on each end, attaching external leads, then encapsulating the component inside of a flame retardant rectangular casing. The two capacitors differ primarily in their capacitance ratings and physical package size. The size difference between the two capacitors also indicates that their equivalent series inductance will be different; the 1.0 μ F capacitor is larger and therefore has a larger average inductive loop area.

The goal is to find a method to add a separately formed winding to space near, or within, the capacitor casing. Fig. 2.1 shows side- and end-cut views of the 330nF capacitor (the shiny section in the center of Fig. 2.1(a) is where a section of the cylindrically wound metalized polyester has been removed). In these photos, it can be seen that there is space between the bottom of the metalized film and the bottom of the capacitor case, an ideal location for the inductance cancellation winding. This area of the capacitor provides easy connection to the capacitor leads without any modification to the case. Even though the space is partially filled by potting compound from the factory, adequate space remains below the potting compound to place the winding for prototyping purposes.

The construction process for the integrated filter element considered here is composed of three primary tasks: the creation of the coupled magnetic winding, forming of the electrical connection between the capacitor and winding, and finally the encapsulation of both devices into a single physical package.

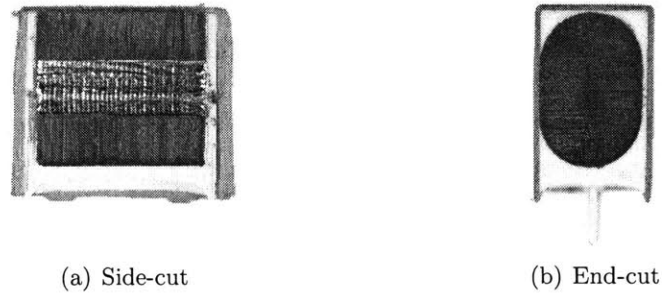


Figure 2.1: Cutaway photos of a Vishay BCcomponents Series MKP338 2222-338-24334 330nF X2 film capacitor.

2.2.1 Coupled Magnetic Winding

A number of constraints are placed on the design and construction of the magnetic winding. The winding must meet resistance and inductance requirements, while having its size limited by the cross-sectional, side, or footprint area of the capacitor. The winding resistance must be low enough to handle the current through the series path of the filter, and not contribute in any substantive form to the losses in a system. As described in Chapter 1, the mutual inductance of the winding is responsible for counteracting the equivalent series inductance of the capacitor, and its value should be very close to the measured equivalent series inductance of the capacitor.

While the maximum outline size may be set for the winding by the capacitor dimensions, it can be designed to have any number of layers and be constructed from any conductor thickness. Additional layers serve to increase the winding inductance, and the variable conductor thickness allows integrated filter elements to be constructed with different series-path current ratings using the same capacitor. To ensure repeatability and linearity, the winding is formed from a conductor such as copper without a core, and properly insulated with a non-conducting material when appropriate.

Winding Design

Guidelines for the design of inductance cancellation windings on printed circuit boards are given in [6, 7], and more thoroughly developed in [14]. However the windings required for

integration can be significantly smaller than those used in the PCB designs, due to the increased thickness of the conductor compared to the thin traces on a PCB.

For the winding designs considered here, an outer footprint is chosen allow adequate clearance of the capacitor terminals and package edges. Both capacitors considered in this chapter have a footprint shape similar to the one shown in Fig 2.2, where the positioning of the winding relative to the capacitor footprint and terminals is illustrated by the dashed outline.

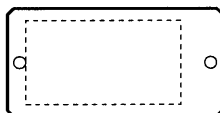


Figure 2.2: Diagram showing the layout relationship of the winding footprint within the capacitor footprint.

Analytical solutions for coupled magnetic coils exist [15,16], however using a CAD package such as FastHenry [17] greatly simplifies the process of calculating the inductance and resistance for arbitrary winding designs. While no rules-of-thumb have been developed to instantiate the design process, over the course of this work it has been found that a two-layer winding design is adequate for a wide range of capacitor package sizes from various manufacturers. Fig. 2.3 shows a typical two-layer winding pattern that can be used as a starting point for design.

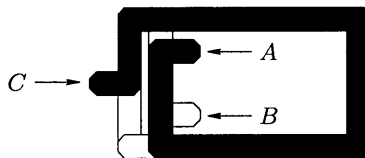


Figure 2.3: Example two-layer Inductance cancellation winding design to be used as a starting point for winding designs. The top layer is represented in solid black, and the bottom layer in white. The two layers are mirror images of each other.

Winding Fabrication

The greatest benefit of a two-layer design comes from its relative simplicity and ease of fabrication. The winding can be inexpensively fabricated from a single layer pattern that

can be constructed from a sheet of conductive material with the appropriate thickness in a number of ways: stamping, chemical etching, mechanical milling, or cut with an abrasive-jet (water-jet). This single layer design can then be folded or joined into its final form. Fig. 2.4 shows a single-layer winding pattern that can be folded into the two layer design illustrated in Fig. 2.3.

Additional leads must be attached to the winding at its endpoints to ensure they extend outside of the final encapsulation. This can be done by soldering, or otherwise joining, short wires perpendicular to the winding. Alternatively, the two external terminal leads can be constructed as part of the original winding pattern, and bent appropriately to extend outward.

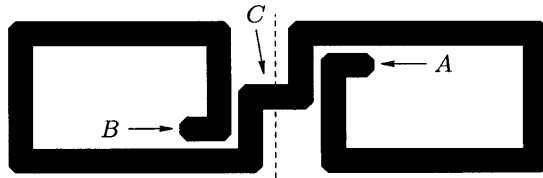


Figure 2.4: Example inductance cancellation winding design shown in a single-layer pattern which can be of folded into the design of Fig. 2.3.

In a controlled manufacturing process, the forming and folding the windings can be automated to provide a consistent repeatable result. However, folding the windings individually by hand for prototyping purposes does not necessarily provide this same consistency. For this reason, an alternative process for constructing prototype windings has been developed.

To assemble one winding by hand, external leads are attached at the end-points (A,B) of the single layer pattern in Fig. 2.4, then the winding is cut at the central fold mark (C). The two layers are electrically insulated, then joined together using solder. This method, while more consistent than hand folding, still produces measurable part-to-part variation.

If a number of windings are to be fabricated, the previous method can be further enhanced to improve the consistency. By cutting a number of single-layer patterns on a metal sheet such that they are held in by a number of cut-tabs (e.g. as done with lead frames), two of these sheets can be overlaid to align any number of windings simultaneously. This ensures that each winding is aligned identically to the others on the sheet, greatly reducing the part-to-part variation. A sheet of windings, as shown in Fig. 2.5(a), produces a total of twenty

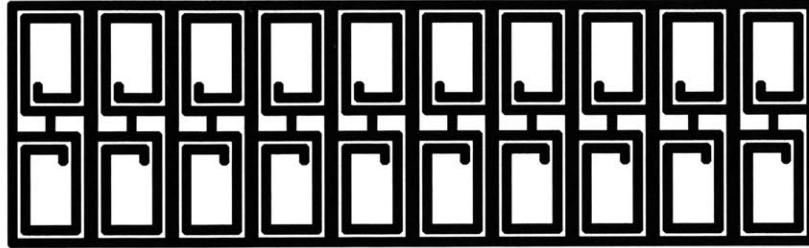
windings. The full process can be separated into three main steps: insulation masking, soldering and alignment, and de-tabbing to separate the windings from the sheet. This process is shown pictorially in Fig. 2.5.

The two sheets are electrically insulated with a thin material, such as Kapton adhesive tape, that can withstand temperatures used for joining. Mask holes are cut in the insulating material where the joints between layers will exist, and then solder paste applied. To join the two sheets together, the top sheet is aligned over the lower one, then placed on a hot plate or in a solder reflow oven. The sheets should be fixed in place to avoid any movement as the solder paste melts and solidifies. After the joining of the two sheets, the windings can then be removed from the sheet by cutting at the tabs. The windings are then ready to be integrated with capacitors.

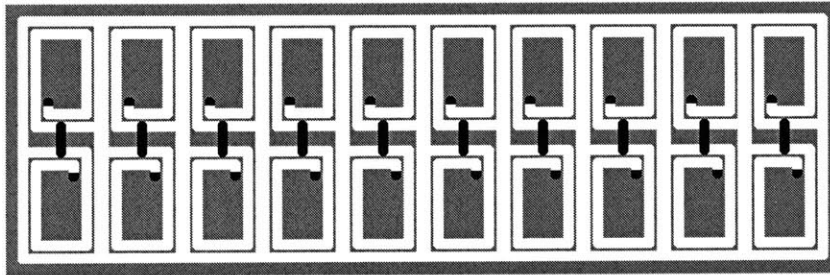
2.2.2 Integration and Encapsulation

The process of integration involves electrically joining the cancellation winding with the capacitor, and exposing the external terminals. One electrode of the capacitor remains as an external lead for the filter element, whereas the other is connected to the magnetic winding; the two endpoints of the winding become external leads of the filter element, forming a three-terminal filter component.

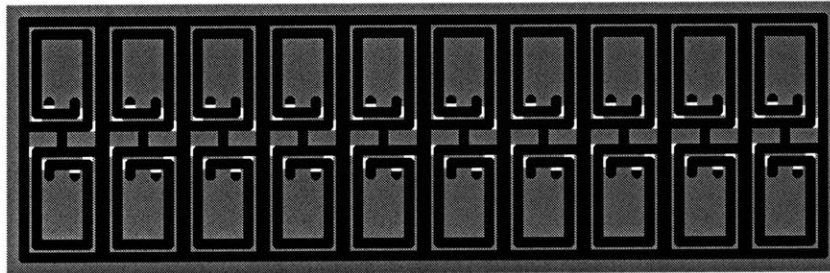
Attaching the winding to the capacitor electrode should be done in a manner that can be precisely repeated, as the attachment location on the capacitor electrode impacts the effective shunt inductance of the filter element, influencing the inductance cancellation performance. If the inductance cancellation winding is to be integrated as part of the initial capacitor fabrication process, the winding can be attached to the capacitor lead a specific distance from the metalized film roll before encapsulation. If the capacitor is already potted, the winding is positioned a fixed distance from the bottom of the capacitor case instead, as the winding cannot be positioned directly against the potting compound at the bottom of the capacitor due to the inconsistent potting height, varying measurably between capacitors. To position the winding relative to the bottom of the case, a small alignment fixture, shown in Fig 2.6, is used to hold the winding allowing it to be repeatably positioned on the capacitor for it to be soldered.



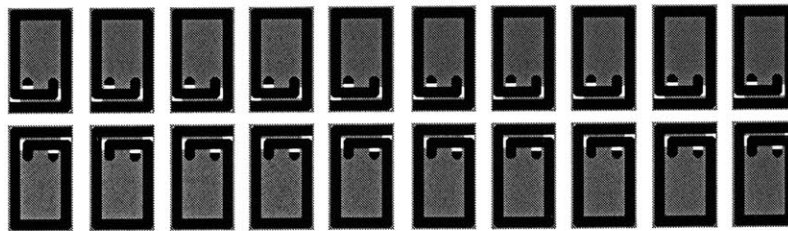
(a) Original Single-Layer Sheet



(b) Electrical Insulation / Solder Mask



(c) Two Sheets Aligned



(d) De-tabbed and Separated

Figure 2.5: Steps to create a batch of windings from two sheets of single layer patters.

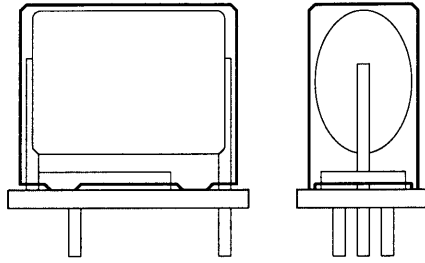


Figure 2.6: Example illustration of fixture used to position the winding flush with the bottom of the capacitor casing for repeatable alignment and joining with the capacitor.

With the capacitor and winding electrically connected, and external leads brought out, the final step is to encapsulate the filter element. The encapsulation provides both mechanical stability as well as electrical isolation, and can be used to tune the final filter element performance by setting the spacing to the external interconnect point. The mechanical and electrical characteristics can be controlled by using different size enclosures, adjusting the positioning of capacitor and winding, or using special potting compounds.

To provide adequate clearance between the winding and the bottom of the filter element in prototype designs, the height of the capacitor may need to be extended. The height is increased by wrapping adhesive tape around the capacitor leaving a small overhang at the bottom of the casing, extending past the cancellation winding. This cavity is then filled with a potting compound, such as 3M Scotch-Weld Epoxy Potting Compound Adhesive (Part DP-270), and left to cure.

When setting the final filter element height using encapsulant, as shown in Fig. 2.7, the residual shunt inductance of the filter can be controlled: increasing the height to add additional inductance or decreasing the height to reduce the inductance. For prototyping work, this allows a fine tuning of the filter element performance at the encapsulation stage without the need to change the winding design or alignment fixture.

2.2.3 Validation and Testing

Two measurement methods are used to validate the proper tuning and operation of the inductance cancellation for the integrated filter element: a multiple two-terminal impedance measurement, and a two-port insertion loss measurement. The impedance measurements

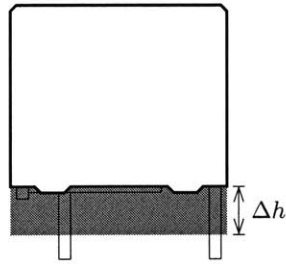


Figure 2.7: Illustration of how the potting process can be used to control the filter element residual shunt inductance by modifying the height of the filter element, using the method shown in Fig. 2.11.

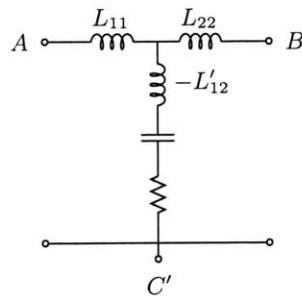


Figure 2.8: Equivalent inductive ‘T’ model of an integrated filter element, additionally showing shunt capacitance and resistance.

are used to calculate the residual shunt inductance of the integrated filter, and insertion loss allows the frequency response of the filter element to be directly measured.

Single-Port Impedance Measurements

Measuring the residual shunt inductance of the filter element provides a single value that can be used to compare devices to verify the fabrication method is providing consistent results. The measured parameters can also be used to determine the parameter values of the filter T-model for use in circuit simulation packages such as Spice.

Three measurements are required to determine the inductance parameters in the T-model of Fig. 2.8: measurements of the inductance between terminals AB , BC , and AC . These three measurements can be written as

$$L_{AB} = L_{11} + L_{22} \quad (2.1)$$

$$L_{BC'} = L_{22} - L'_{12} \quad (2.2)$$

$$L_{AC'} = L_{11} - L'_{12} \quad (2.3)$$

where L'_{12} is the residual shunt inductance, representing the sum of the cancellation winding mutual inductance, the capacitor equivalent series inductance, and any secondary effects due to inductive coupling between the winding and capacitor. The value of L'_{12} , L_{11} , and L_{22} can be found from the three measurements, using

$$L_{11} = \frac{L_{AB} + L_{AC'} - L_{BC'}}{2} \quad (2.4)$$

$$L'_{12} = \frac{L_{AB} - L_{BC'} - L_{AC'}}{2} \quad (2.5)$$

$$L_{22} = \frac{L_{AB} + L_{BC'} - L_{AC'}}{2} \quad (2.6)$$

Ideally, the residual shunt inductance L'_{12} is zero; if the residual is less than zero, there is too much cancellation, if the residual is greater than zero, too little. The measured residual is most useful to evaluate the *relative* variance between filter elements in the fabrication process, and not as a measure of general filter performance.

Two-Port Insertion Loss Measurement

Insertion loss is a measurement of the attenuation of a filter, and is a common method for evaluating the performance of EMI filters [18]. In the most simplistic arrangement, the measurement is made with a sinusoidal input source with a series impedance driving the input port of the filter, while a load impedance is placed across the output port. The ratio between the magnitude of the source voltage and output terminal voltage measured across the load impedance, is the filter insertion loss, and reported in dB. The insertion loss measurements are most easily taken using a network analyzer which provides 50Ω source and

load impedances. Fig. 2.9 illustrates the measurement setup. Measurements in this thesis are made in accordance with those used to evaluate inductance cancellation performance in [1, 14] to allow for direct performance comparison (the filter responses presented in [6] unfortunately are not those of insertion loss, and are not directly comparable, however insertion-loss measurements for these filters appear in [14]). The use of a printed circuit board measurement fixture, as shown in Fig 2.10, ensures the measurement mimics, as closely as possible, realistic filter element usage.

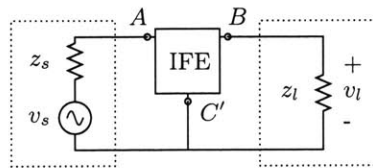


Figure 2.9: Measurement setup for two-port insertion loss measurements. Impedances z_s and z_l are 50Ω .

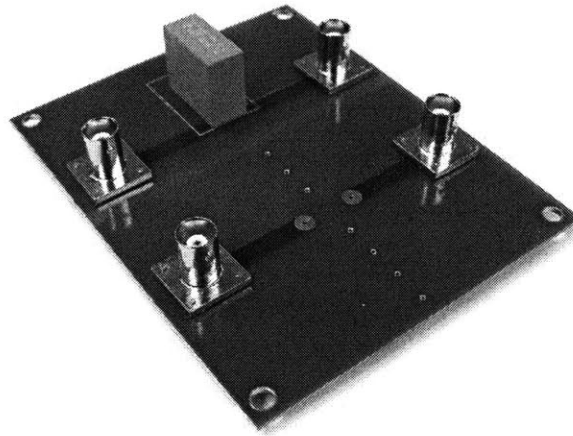


Figure 2.10: Photograph of printed circuit board measurement fixture used in the two-port network measurement shown in Fig 2.9. The mounted capacitor is used as a reference.

With the PCB measurement fixture, and a three terminal filter element, the filter performance can be interactively modified by raising and lowering the element with respect to the circuit board, then observing the change in frequency response. By raising the filter element, the length of terminal C' is increased, increasing the effective shunt inductance of the filter element, shown in Fig 2.11. The change in inductance can be approximated [4] by

$$\Delta L = \mu_0 \frac{A}{w} \quad (2.7)$$

where A and w are illustrated in Fig 2.11. This approximate relationship is valid for $h \ll A$, which may not hold for common sizes of integrated filter elements, however it is still a useful mental tool for approximating the change in inductance.

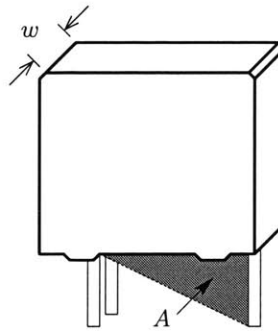


Figure 2.11: Illustration of how to increase effective shunt inductance by lifting the capacitor off the testing fixture to increase loop area.

This method of adjusting the filter element shunt inductance can be used to determine how close the filter element is to having “optimal” inductance cancellation. While intuitively it seems that the optimal output response would occur when the residual shunt inductance is zero, it is often advantageous for a small positive inductance to remain. The proper residual allows the reactive cancellation due to the resonance of the shunt path to be positioned slightly above the highest frequency of interest (instead of being completely eliminated), increasing the insertion loss in this region.

2.3 Implementation

Using the design, fabrication, and measurement methods developed in Section 2.2, two separate integrated filter element designs are presented here. The two selected capacitors are representative of capacitors used in many EMI filters. Vishay BCcomponents Series MKP338 capacitors in 330nF and 1.0 μ F, part numbers 2222-338-24334 and 2222-338-24105 respectively, are X2 rated polyester-film capacitors, indicating they are approved for both line-to-line and line-to-ground configurations. The two capacitors differ primarily in their

capacitance ratings and physical package size, Fig. 2.12 shows a photograph of the two capacitors side by side. The size difference between the two capacitors is indicative of their relative equivalent series inductances; the $1.0\mu\text{F}$ capacitor is larger, has a larger average inductive loop area, and a higher equivalent series inductance. The capacitance ratings of the capacitors are illustrative of their use: the $1.0\mu\text{F}$ capacitor is more likely to be used in filters with a higher current rating than the 330nF capacitor.

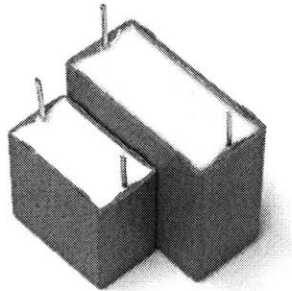


Figure 2.12: Photograph of the Vishay BCcomponents Series MKP338 capacitors in 330nF and $1.0\mu\text{F}$ values. Figs. 2.13 and 2.17 contain the outer dimensions of each respective capacitor.

For both capacitors selected, twenty integrated elements were fabricated to determine the repeatability of the fabrication method. The windings were constructed using the methods described in Section 2.2.1 for fabricating multiple windings simultaneously.

In this section, all simulated inductance values are generated using the FastHenry [17] three-dimensional inductance extraction program. Measured inductance values are taken using an Agilent 4395A Network/Impedance/Spectrum Analyzer at 30MHz , the same frequency as the simulations. The Agilent 4395A is also used for the two-port network measurements of insertion-loss, which provides 50Ω source and load impedances.

2.3.1 Vishay BCcomponents 2222-338-24334 330nF

This capacitor outline and dimensions are shown in Fig 2.13. The measured equivalent series inductance is 9.9nH .

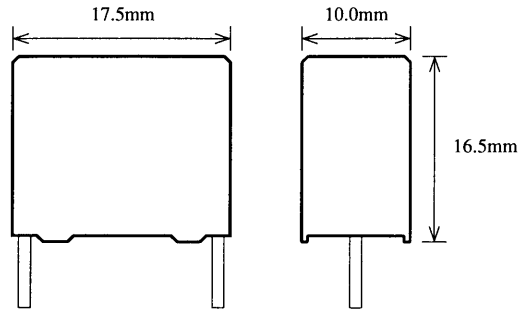


Figure 2.13: Dimensioned illustration of Vishay BCcomponents 2222-338-24334 capacitor.

Winding Design

The filter winding, designed for a maximum series current of 5A, with a loss of no more than 0.01% of the maximum line power at 240V. This corresponds to a series path resistance of less than $4.8\text{m}\Omega$.

The winding inductance is designed to offset the capacitor equivalent series inductance of 9.9nH , and using the basic design of the example coil in Fig. 2.3 as a starting point, the final two-layer coil design is shown in Fig. 2.14. The single layer pattern, fabricated from a 1 mm thick copper sheet using an abrasive-jet cutter, is marked to indicate where the pattern is folded to create the external leads. Fig. 2.15(a) shows a single layer winding as originally cut, and Fig. 2.15(b) shows the winding after the structure has been insulated, folded, and joined into its final two layer form.

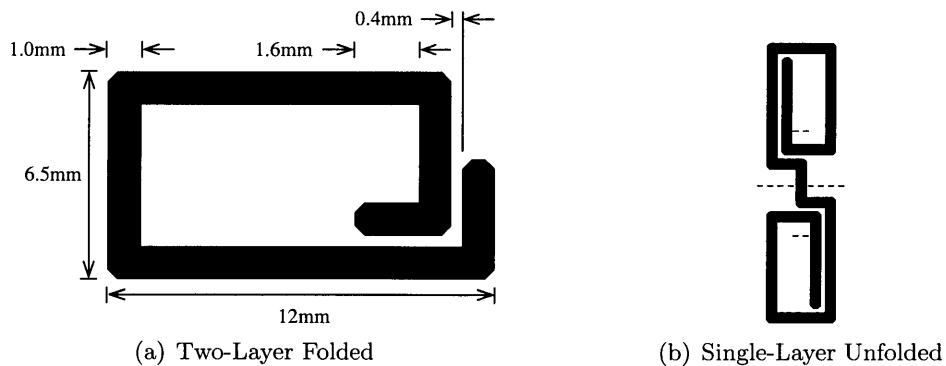


Figure 2.14: Inductance cancellation winding design for use with the Vishay BCcomponents 330n capacitor. Shown in both the two-layer folded and single-layer unfolded designs. The winding is fabricated from 1mm thick copper.

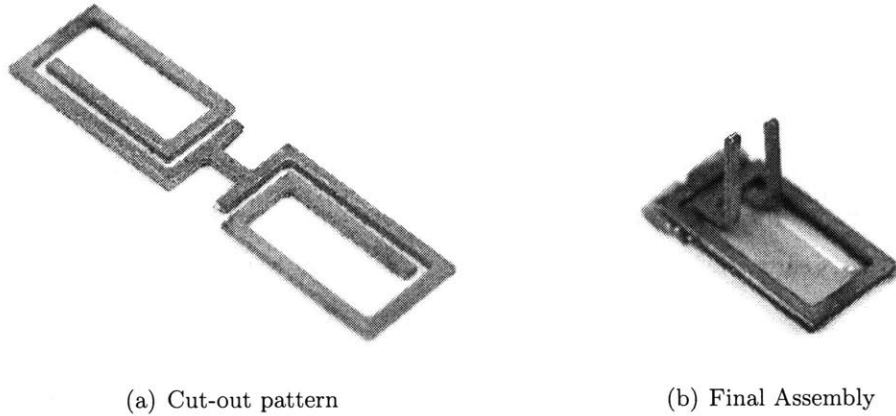


Figure 2.15: Inductance cancellation winding photos of single-layer pattern and final two-layer construction for the 330nF integrated filter element.

Simulation of the winding at 30MHz results in an inductance matrix

$$L = \begin{bmatrix} 14.8 & 11.2 \\ 11.2 & 14.8 \end{bmatrix} \text{ nH}$$

and a total winding resistance of $2.5\text{m}\Omega$ at 60Hz. The measured winding inductances at 30MHz (of one winding selected at random) result in the inductance matrix

$$L = \begin{bmatrix} 26.0 & 8.5 \\ 8.5 & 25.1 \end{bmatrix} \text{ nH}$$

and a measured winding resistance of $3\text{m}\Omega$ at 60Hz.

The measured inductance matrix shows a significant departure from the simulation. This is in part due to the additional interconnect length required to mount the winding on the measurement fixture, which is not reflected in the simulation results. The mutual inductance value is sufficiently close to justify the use of FastHenry for estimation purposes provided the designer takes into account the (consistent) variation between the simulation and real-world measurement setup.

Integration and Encapsulation

The final filter element potting height is determined by the desired residual shunt inductance, which determines the filtering characteristics of the device. This height is determined experimentally using the two-port insertion-loss measurements described in Section 2.2.3. A sacrificial capacitor and magnetic winding were used to determine the optimal potting height, and this same height was used on all elements in the batch. The final fabrication result for the 330nF integrated filter element is shown in 2.16. The three terminal device is 1.75mm taller than the original capacitor casing.

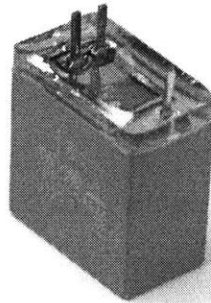


Figure 2.16: Photograph of a completed 330nF integrated filter element with inductance cancellation.

The performance of this integrated filter design is investigated in Section 2.3.3.

2.3.2 Vishay BCcomponents 2222-338-24105 1.0 μ F

This capacitor outline and dimensions are shown in Fig 2.17. The measured equivalent series inductance is 13.3nH.

Winding Design

The filter winding is designed with a maximum series current of 10A, and a loss of no more than 0.01% of the maximum line power at 240V. This corresponds to a series path resistance

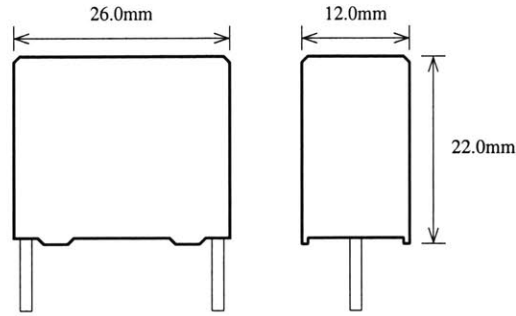


Figure 2.17: Dimensioned illustration of Vishay BCcomponents 2222-338-24105 capacitor.

of less than $2.4\text{m}\Omega$. The winding inductance is designed to offset the capacitor equivalent series inductance of 13.3nH , and using the basic design of the example coil in Fig. 2.3 as a starting point, the final two-layer coil design is shown with dimensions in Fig. 2.18. The single layer pattern, fabricated from a 1mm thick copper sheet using an abrasive-jet cutter, is marked to indicate where the pattern is folded to create the external leads. Fig. 2.19(a) shows the single layer winding as originally cut, and Fig. 2.19(b) shows the winding after the structure has been insulated and joined into its final two layer design.

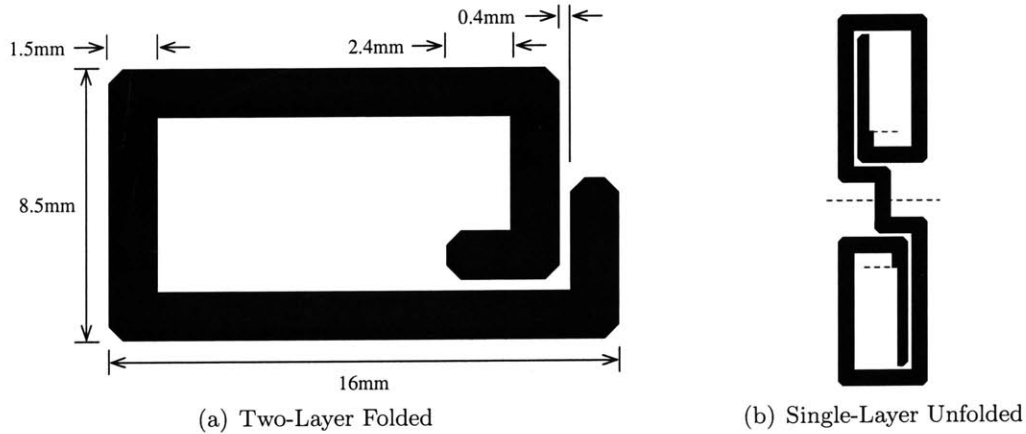


Figure 2.18: Inductance cancellation winding design for use with the Vishay BCcomponents $1.0\mu\text{F}$ capacitor. Shown in both the two-layer folded and single-layer unfolded designs. The winding is fabricated from 1mm thick copper.

The simulated winding inductances at 30MHz result in an inductance matrix

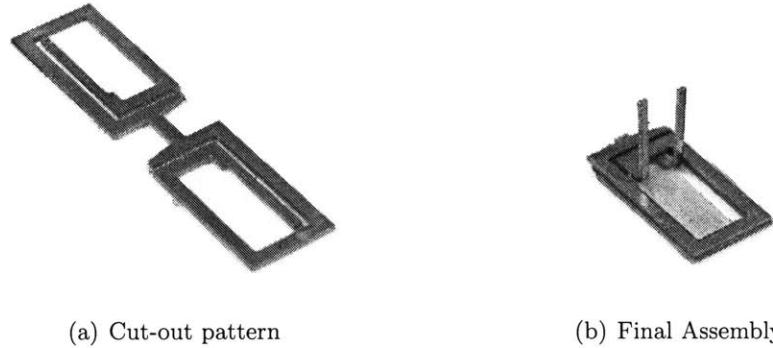


Figure 2.19: Inductance cancellation winding photos of single-layer pattern and final two-layer construction for the $1.0\mu\text{F}$ integrated filter element.

$$L = \begin{bmatrix} 18.6 & 14.8 \\ 14.8 & 18.6 \end{bmatrix} \text{ nH}$$

and a total winding resistance of $2.0\text{m}\Omega$ at 60Hz . The measured winding inductances at 30MHz (of one winding selected at random) result in the inductance matrix

$$L = \begin{bmatrix} 34.0 & 12.7 \\ 12.7 & 32.6 \end{bmatrix} \text{ nH}$$

and a measured winding resistance of $2\text{m}\Omega$ at 60Hz .

Again, the variation between the simulated and measured inductance matrices is significant due to the added interconnect required for the measurement, however, the mutual inductance term (L_{12}) remains reasonably close for the purposes of estimation.

Integration and Encapsulation

The final filter element potting height is determined by the methods described in Section 2.2.3. A sacrificial capacitor and magnetic winding were used to determine the optimal

potting height; this same height was used on all elements in the batch. The final fabrication result for the $1.0\mu\text{F}$ integrated filter element is shown in 2.16. The three terminal device is 1.2mm taller than the original capacitor casing.

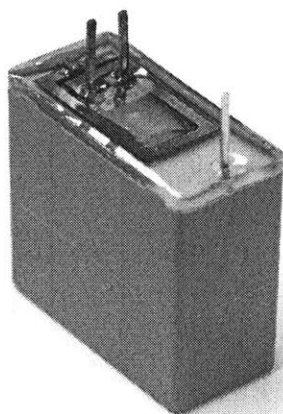


Figure 2.20: Photograph of a completed $1.0\mu\text{F}$ integrated filter element with inductance cancellation..

The performance of this integrated filter design is investigated in Section 2.3.3.

2.3.3 Fabrication Results

To determine the relative precision of the filter element construction, a batch of twenty filter elements was fabricated for each design in Section 2.2. Each element was then characterized using measurements of the residual shunt inductance and insertion-loss.

The residual shunt inductance of each filter was found using the three two-terminal impedance measurements in (2.5), then offset by the geometric mean of all twenty filter elements in the batch to provide a zero centered measurement. Centering the residual inductances around zero is done to eliminate the inductance of the measurement apparatus, and illustrates the error *relative* to the other elements, and not necessarily a specific target residual shunt inductance. Histograms of this data are presented in Figs. 2.21 and 2.22 for the 330nF and $1.0\mu\text{F}$ devices, offset by 1.89nH and 5.09nH respectively. Additionally, it may be useful to consider this data in a normalized form, scaled by the magnitude of

the initial capacitor equivalent inductances to allow a comparison between designs. This results in part-to-part variation measurement of are 8% and 5% for the 330nF and 1.0 μ F filter elements respectively.

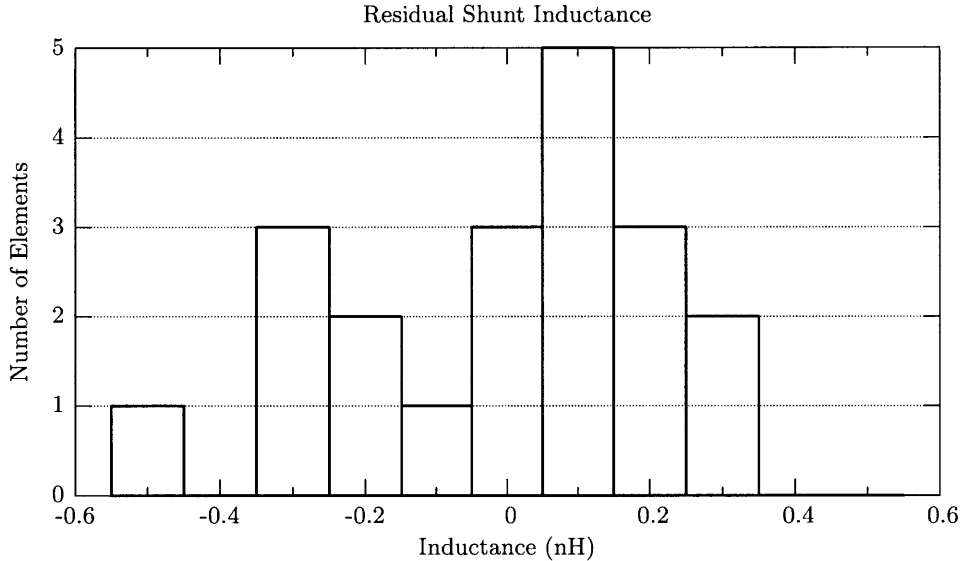


Figure 2.21: Zero centered histogram of measured residual shunt inductance values of twenty 330nF integrated filter elements.

Figs. 2.23 and 2.24 present the insertion-loss measurements of an original unmodified capacitor and the geometric mean response (least squares fit) of the twenty integrated filter elements in the 330nF and 1.0 μ F batches respectively. This illustrates the ‘typical’ insertion loss improvement that can be expected from the integrated elements in place of the standard capacitor. Both integrated filter elements show a significant improvement in performance over a standard capacitor, gaining more insertion-loss at the higher frequencies where the equivalent series inductance would normally dominate. At 30MHz, the upper bound of the conducted EMI specification [3], the 330nF and 1.0 μ F both show an improvement of at least 25dB.

An interesting result in both filter element responses is the unveiling of the resonance located in the low-mid range in the figures. This small resonance results from the distributed nature of the capacitor [19], and is normally insignificant relative to the dominating interconnect inductance.

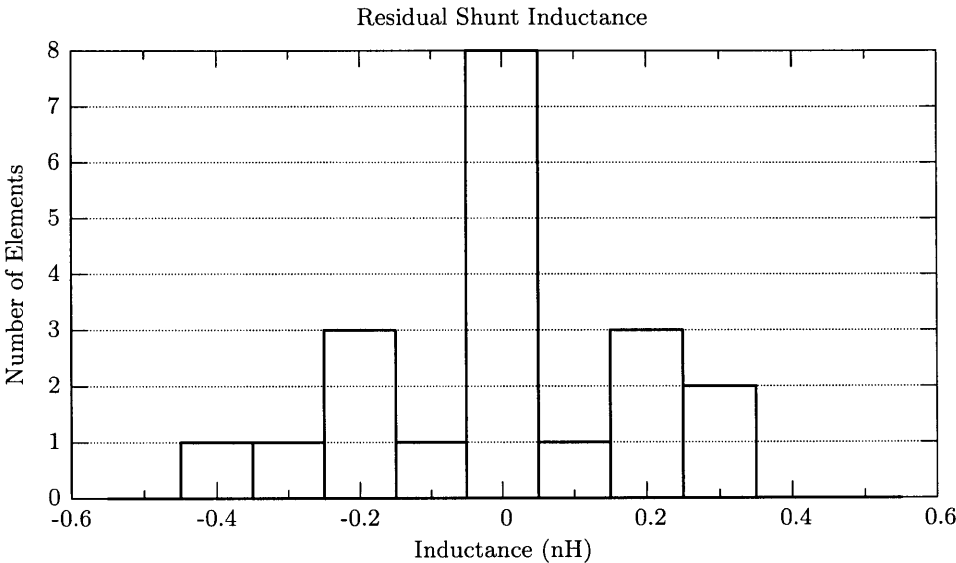


Figure 2.22: Zero centered histogram of measured residual shunt inductance values of twenty 1.0 μF integrated filter elements.

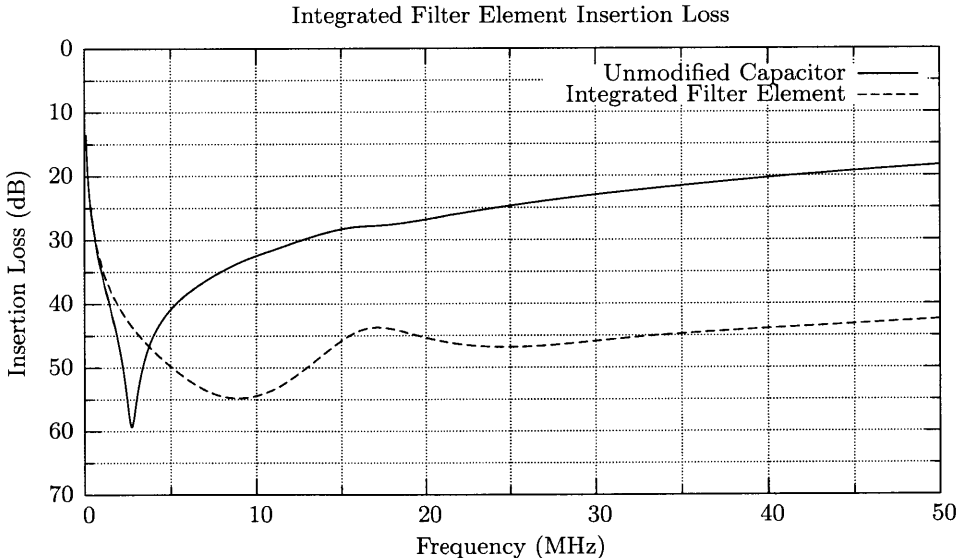


Figure 2.23: Comparison of measured results between the original 330nF capacitor and the (geometric) mean response of the integrated filter elements.

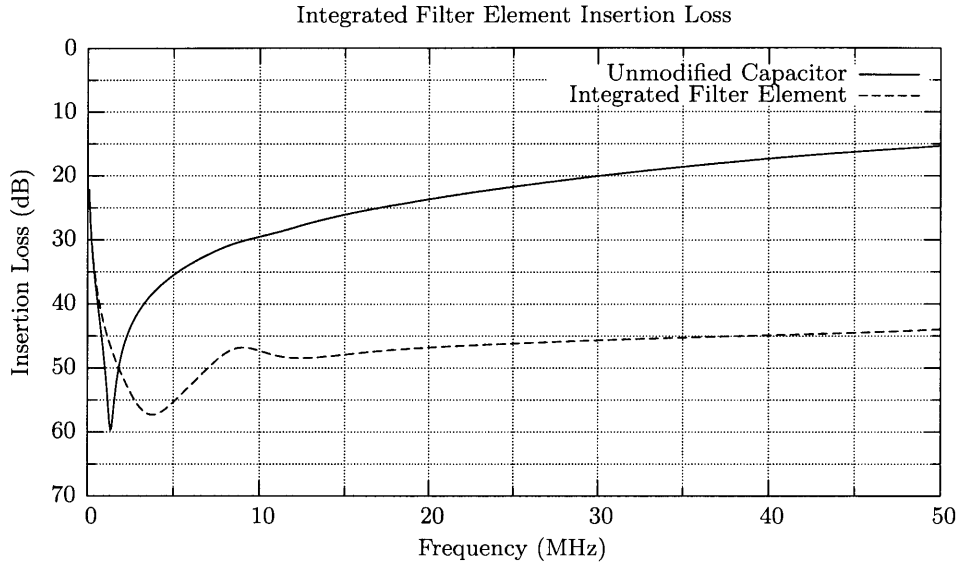


Figure 2.24: Comparison of measured results between the original $1.0\mu\text{F}$ capacitor and the (geometric) mean response of the integrated filter elements.

Figs. 2.25 and 2.26 plot the frequency response for each filter element of the two types, illustrating the part-to-part insertion-loss variations obtained. These figures also include a plot of the difference between the largest and smallest insertion-loss value among filters at each frequency, giving the maximum variation between filter elements of that batch. The maximum variation across the frequency range is 4.1dB for the 330nF device and 3.5dB for the $1.0\mu\text{F}$. Additionally, the insertion-loss measurements of the 330nF integrated filter elements can be compared directly with the results presented in [14] for the 330nF capacitor with inductance cancellation implemented using printed circuit board windings. The variation of insertion loss with the PCB inductance cancellation windings, which are nominally more repeatable than the hand fabrication methods considered here, appear to offer only a slight decrease in the maximum variation.

2.4 Conclusion

This chapter has presented an implementation of inductance cancellation where the coupled magnetic winding is co-packaged with the capacitor to form a self-contained integrated filter

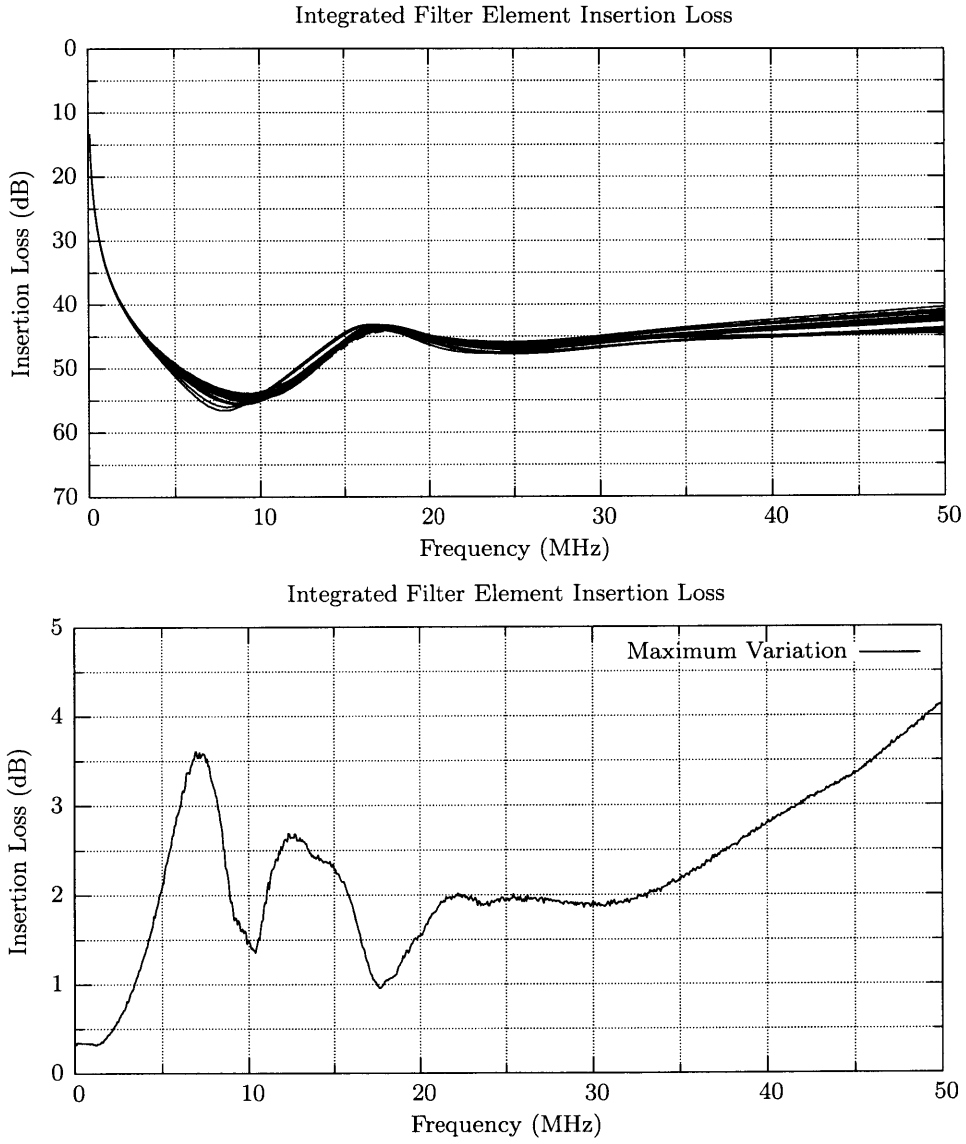


Figure 2.25: Insertion loss measurements of twenty 330nF integrated filter elements.

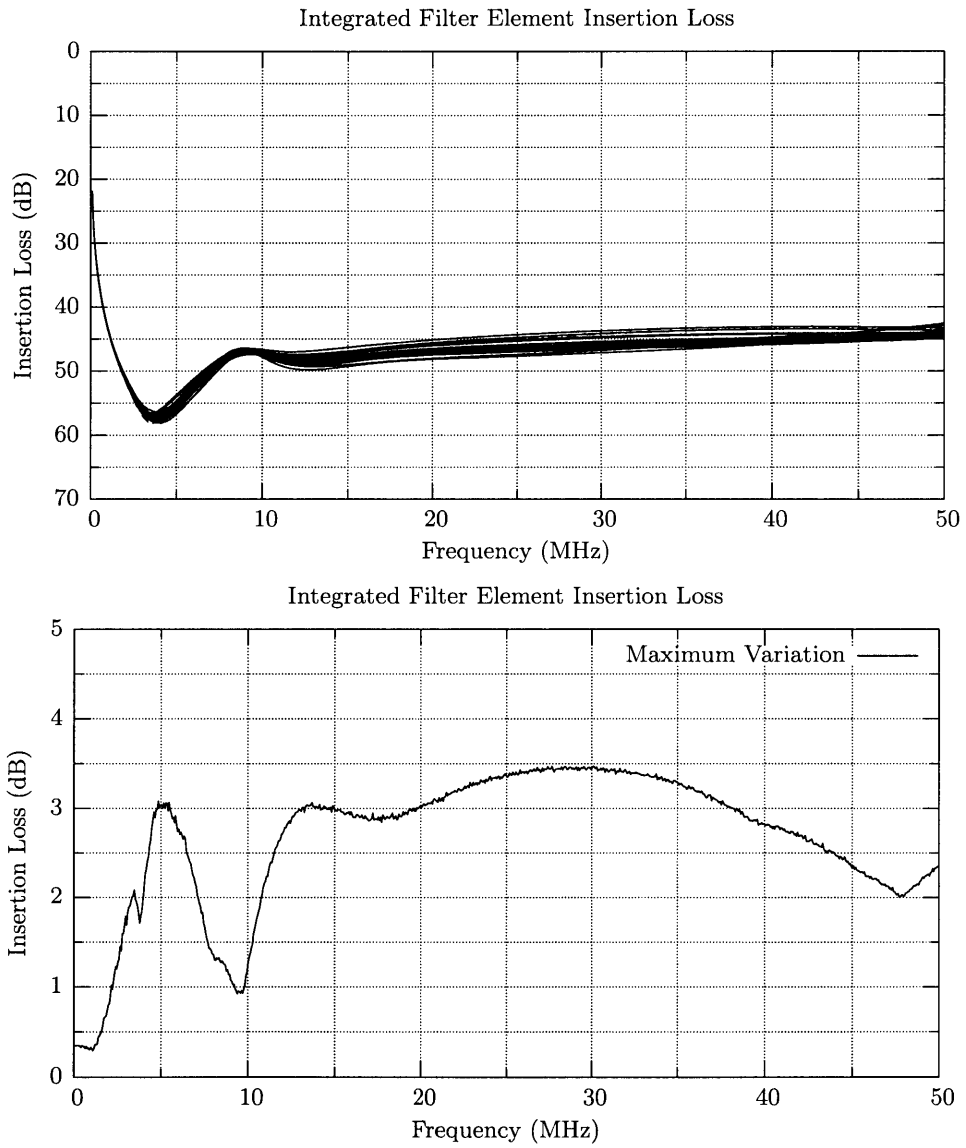


Figure 2.26: Insertion loss measurements of twenty $1.0\mu\text{F}$ integrated filter elements.

element. A design methodology and fabrication procedure suitable for low volume prototyping work (and extendable to high-volume production) is presented. It is implemented using two different capacitors and coil designs. The resulting filter element characteristics and performance measurements validate the feasibility of fabricating devices with repeatable performance results, even using simple hand fabrication and assembly. Additional gains in device repeatability can be expected with a refined process, steadier hand, or mechanized fabrication and assembly. The approach presented here offers a compelling combination of substantial performance improvements, repeatability, and ease of manufacture.

Multiple Element Inductance Compensation

CONVENTIONALLY, inductance cancellation windings have only been used to compensate for the equivalent series inductance of a single capacitor. In a filter designed to attenuate both common- and differential-mode signals with multiple capacitors, this significantly increases the number of windings required. The simple EMI filter in Fig. 3.1 contains three capacitors, and the commercial filter in Fig. 3.14 uses six.

The goal of this chapter is to extend the inductance cancellation presented in Chapter 1 by developing a method that allows for the use of a single magnetic winding to compensate for the effects of equivalent series inductances of two capacitors, instead of just one. For many filter topologies, this provides an opportunity to reduce the number of cancellation windings needed, thereby saving precious space and added cost.

3.1 Motivation

To understand why the use of a single magnetic winding to compensate for the inductive parasitics of two capacitors is of particular value in EMI filtering, consider the structure and operation of an EMI filter. Fig. 3.1 shows the basic structure of an EMI filter designed to attenuate both common-mode and differential-mode signals, along with representative source and load networks for performance evaluation. This circuit can be analyzed by separating its common-mode and differential-mode responses and treating these equivalent circuits as if they were independent [3]. The common- and differential-mode equivalent circuits are shown in Fig. 3.2.

Now, if the circuit of Fig. 3.1 is augmented with inductance cancellation coils for each

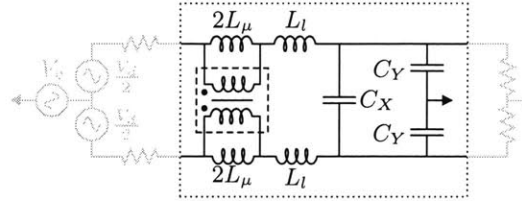


Figure 3.1: Simple EMI filter circuit shown with representative source and load networks for performance evaluation. Some parasitic elements (such as capacitor equivalent series inductance) are not shown explicitly.



Figure 3.2: Models for the simple EMI Filter circuit of Fig. 3.1, decomposed into common- and differential-mode portions.

capacitor, the circuit in Fig. 3.4 is generated. In this new figure, the differential capacitor C_X is fitted with two inductance cancellation coils instead of only one to preserve circuit symmetry. Past work [1] has shown this to be as effective as a single coil, and Fig. 3.3 shows a photograph of this where the inductance cancellation windings are fabricated on a PCB.

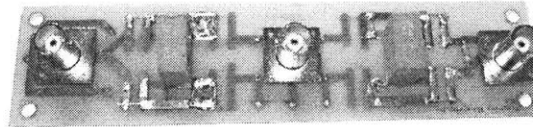


Figure 3.3: Test circuit with balanced inductance cancellation windings implemented in the printed circuit board. Performance of this filter has been previously shown [1].

It is desirable to implement the cancellation windings in a balanced fashion to avoid inserting an unbalanced circuit element within the otherwise well-balanced system. Without balancing the series inductances on both sides of the capacitor, a cross coupling between the differential and common-mode signal sources would result. By avoiding this coupling, the common- and differential-mode circuit equivalents remain straightforward, as illustrated in Figs. 3.5(a) and 3.5(b).

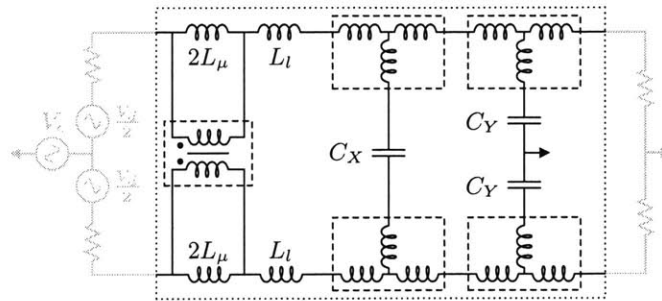


Figure 3.4: Simple EMI Filter circuit from Fig. 3.1 with balanced inductance cancellation of each capacitor.

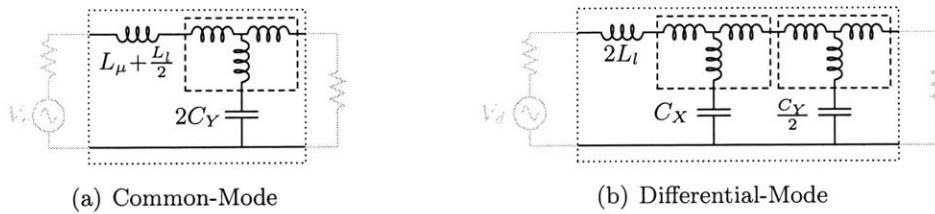


Figure 3.5: Simple EMI Filter circuit with balanced inductance cancellation of each capacitor, decomposed into common- and differential-modes.

As shown in Fig. 3.4, the construction of an EMI filter with full, balanced inductance cancellation would require four magnetically coupled windings when constructed using the previously established method. These windings occupy additional space within the filter, and if placed in close proximity may exhibit secondary effects from magnetic coupling, complicating the design. The effects of coupling on a single capacitor are developed in Chapter 4, and are investigated more thoroughly for two capacitors here in Section 3.3. Given these limitations, it would be a considerable improvement if the number of required windings could be reduced by utilizing a single winding to provide appropriate inductance compensation for two capacitors.

3.2 Implementation

To show experimentally that the use of a single inductance cancellation coil for two capacitors is feasible, a simple test filter was created with a planar winding mounted with EMI filter capacitors inside a shielded enclosure. Fig. 3.6 shows the filter along with the

two Panasonic ECK-ATS472ME6 4700pF Y2 class ceramic capacitors used. This test filter does not directly examine common- and differential-mode testing, however it does provide a straightforward example how a single coil can support the compensation of inductance for two capacitors. A dimensioned line-art drawing of the coil, which was cut using an OMAX abrasive-jet cutter from a single piece of 1mm thick copper, is shown in Fig. 3.7. Based on simulation results from FastHenry [17], the coil itself has a maximum series inductance of 393.0nH, and a maximum equivalent shunt-path inductance of -63.2nH when used for single element inductance cancellation (in the magnetic winding T model). It should be noted that this coil was intentionally designed to be far over-sized for the amount of cancellation required; this was to allow for maximum flexibility in testing.

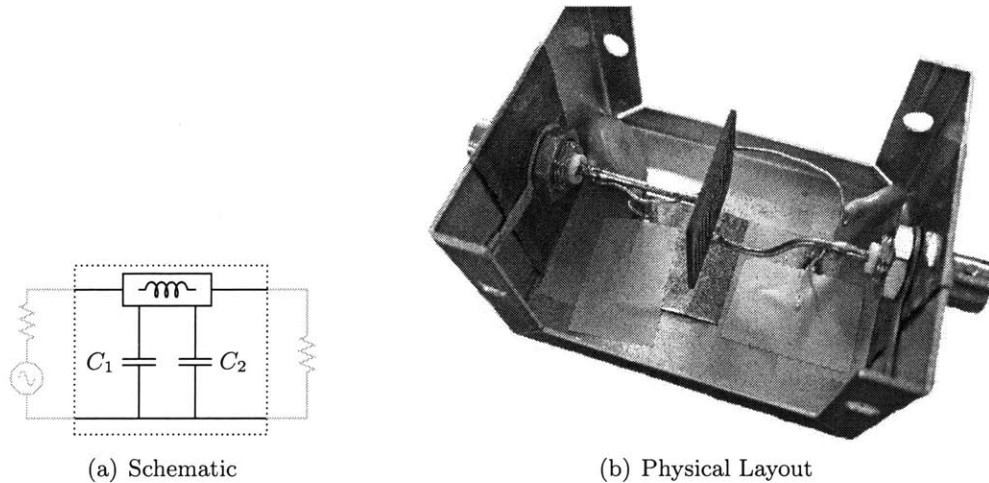


Figure 3.6: Test filter for inductance compensation of two Panasonic ECK-ATS472ME6 4700pF ceramic capacitors using a single magnetic winding.

The procedure outlined here was developed for tuning the filter response of the two capacitors, and is one way a high performance filter response can be determined. Initially, the connection of capacitor C_1 is tuned to optimally cancel its parasitic inductance. This can be done by adjusting the connection point of the capacitor on the winding while observing the filter attenuation (e.g. with a network analyzer), and/or using methods associated with previously described techniques in [6]. Once its optimal position is found, the position of the capacitor is fixed. Following this, the connection of capacitor C_2 is tuned (with capacitor C_1 in place) to find an optimal filter response. This gives one possible combination of capacitor locations on the coupled winding that results in a high performance filter characteristic.

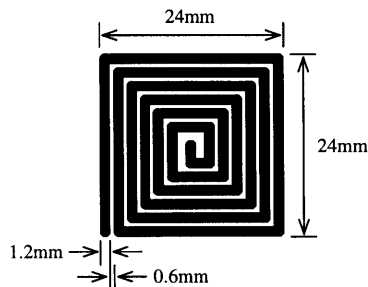


Figure 3.7: Illustration of the planar winding used in the test filters of Section 3.1, fabricated from 1mm thick copper. The total series-path inductance based on simulation is 393.0nH, and the maximum equivalent shunt-path inductance for a single element is -63.2nH (in the magnetic winding T model).

Experimental results for this test system are shown in Fig. 3.8, with data taken from an Agilent 4395A network analyzer which provides 50Ω source and load impedances. Insertion gain measurements were made in accordance with those used to evaluate inductance cancellation performance in [1,6] to allow for direct performance comparison. When tuning the response with only C_1 , two measurements were taken for comparison: one with the capacitor connected directly at the input (source-side) terminal providing no cancellation, and one where the capacitor was connected to the cancellation coil at a location where the output response was optimal. The same approach was taken when tuning the response for the combination of C_1 and C_2 : C_2 was connected either directly at the filter output (load-side) terminal or at a position optimizing the filter response with both capacitors.

The characterization results of the filter attenuation performance clearly show a dramatic improvement (as much as 35dB at high frequency) from the case where no compensation is provided (*Both Not Cancelled*) to the case where inductance compensation is provided for both capacitors (*Both Cancelled*). These results demonstrate that a single coupled magnetic winding can be used to provide inductance compensation for two capacitors, with dramatic performance improvement at high frequencies.

3.3 Coupling of Multiple Windings

When physically placing multiple magnetic windings in close proximity, linked magnetic flux between the windings can affect the predicted performance in various ways [8]. Thus,

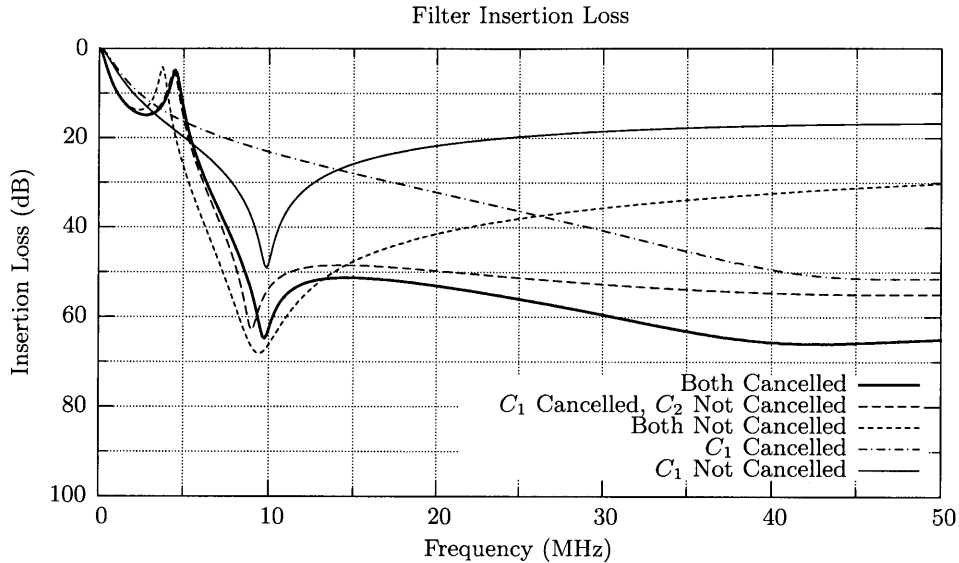


Figure 3.8: Measured results from the test filter in Fig. 3.6 showing the performance of multiple-element inductance compensation.

the implementation of multiple cancellation windings in a single filter may affect the inductance cancellation and filter performance. Here the effects of mutual coupling are explored when two coils are used to provide balanced inductance cancellation for both common- and differential-mode capacitors.

Two additional filters (using the same windings shown in Fig. 3.7) were created to test two coil configurations having different magnetic coupling directions. In addition to a pair of line-to-ground (Y) capacitors (Panasonic ECK-ATS472ME6) for common-mode filtering, these test filters incorporate a Rubycon 250MMCA334KUV class X2 line-to-line capacitor for differential-mode filtering. Fig. 3.9 is a photo of one of the filters, and shows its internal layout. Figs. 3.10 and 3.11 show the filter configurations and illustrate the difference between the two winding orientations.

Windings placed in the *same direction* each throw flux in a way which opposes the flux of its paired winding for common-mode currents, reducing each winding’s effective inductance. In the case of the windings oriented in the *opposite direction*, the flux from each winding is reinforced by the other for common-mode currents, providing a coupling direction like that of a common-mode choke, and increasing each winding’s effective inductance.

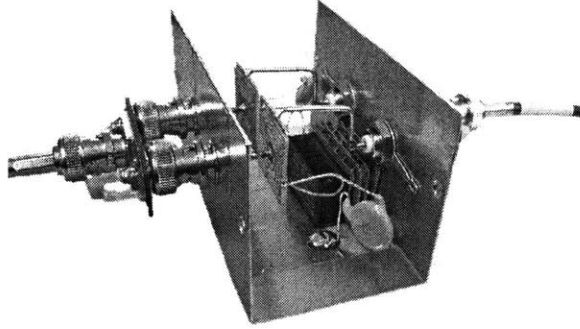


Figure 3.9: Filter for investigation of common- and differential-mode coupling between inductance compensation windings.



Figure 3.10: Two orientations of coupled inductance compensation coils. The coils are of the type shown in Fig. 3.7. C_{Y1} and C_{Y2} are Panasonic ECK-ATS472ME6, C_{X1} is a Rubycon 250MMCA334KUV. The two circuits only differ with respect to mutual coupling among the coils.



Figure 3.11: Flux patterns for common-mode operation of the two magnetic winding configurations of Fig. 3.10. Windings oriented in the *same direction* generate flux in a way which opposes the flux of the paired winding for common-mode currents. Windings oriented in the *opposite direction* generate fluxes which reinforce each other, providing a coupling direction like that of a common-mode choke.

Multiple Element Inductance Compensation

The tuning procedure used here is similar to the one used in the two-capacitor case in Section 3.2. Initially, the connections of capacitors C_{Y1} and C_{Y2} are tuned simultaneously in the common-mode case to compensate for their parasitic inductances (while retaining a balanced configuration). Once the optimal positions are found, the positions of the capacitors are fixed. Following this, the capacitor C_{X1} is tuned in the differential-mode case by moving its connections on both coils symmetrically to find an optimal output response. Tuning is carried out in this order because ideally the addition of the differential-mode capacitor does not affect the common-mode response, while the reverse would not necessarily be true.

The measurement setup for the common- and differential-mode filter insertion-loss performance is taken from [18], with signal generation and measurement performed by the same Agilent 4395A Network Analyzer as in Section 3.2, with Mini-Circuits 180° power splitters (models ZSCJ-2-1 and ZSCJ-2-2) for dividing its output into differential signals, and custom-made common-mode splitters.

In both winding configurations the target frequency for optimization was 30MHz, with measurements shown up to 40MHz. The two orientations possess similar optimized filtration performance, seen in the thicker traces of Fig. 3.12. The thinner traces in show additional measurements from intermediate steps in the tuning process.

The results show that in both winding orientations an equivalent inductance compensation improvement can be achieved for both the common- and differential-modes. This allows the orientation of the windings to be selected based on other factors (e.g. based on magnetic coupling with more dominant circuit parasitics). While the winding orientation does not influence the final optimized response in these filters, how each winding orientation achieves this optimum is slightly different. In Fig. 3.13 the connection locations for the filter capacitors are shown, corresponding to the optimal common- and differential-mode filter response from Fig. 3.12.

Due to the coupling in the common-mode, the connection for the C_{Yn} capacitor was closer to an end terminal on the winding in the *opposite direction* orientation than in the *same direction* orientation. Effectively, in the common-mode, the *opposite direction* orientation has a marginally higher inductance-per-turn than the *same direction* orientation, and thus requires a slightly reduced number of turns to achieve the same performance.

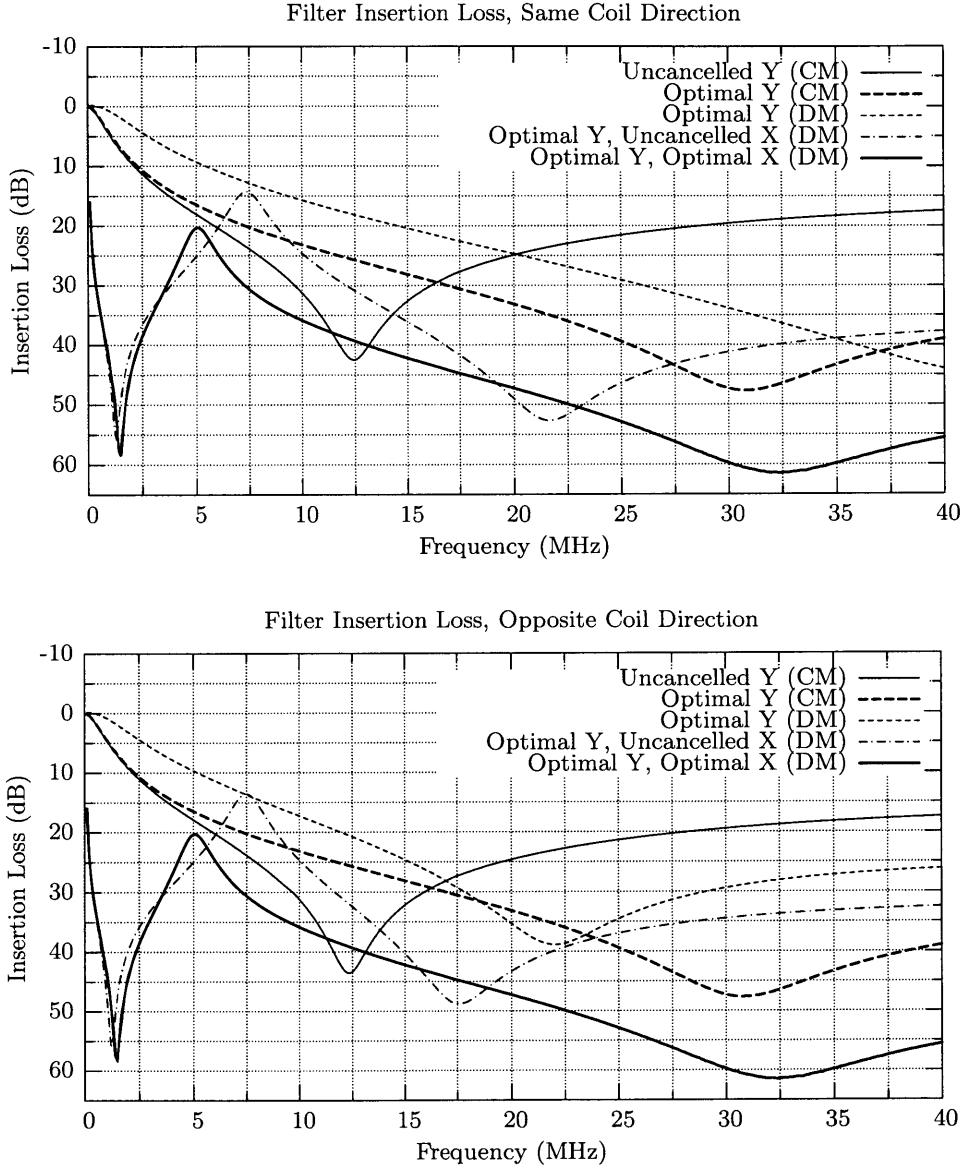


Figure 3.12: Measured results from the coupled inductance compensation winding orientations of Fig 3.10, including both common-mode (CM) and differential-mode (DM) measurements.



Figure 3.13: Connection locations of capacitors corresponding to the results in Fig. 3.12. Only one winding of each pair is shown, the connections made to the other winding are symmetric. X represents the connection location of C_{X1} , Y represents the corresponding C_{Yn} connection location for that winding, I is connected to the input of the filter, and O represents the connection to the filter output.

Even with the the windings in close proximity, the effects of magnetic coupling on the inductance compensation are minimal. In more extreme cases where the coupling is significantly higher, the observed effects may become more pronounced. Even in this case, however, an equivalent performance should be achievable given properly sized windings.

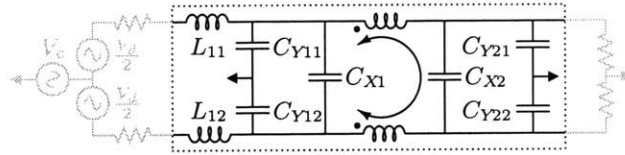
3.4 Application to Commercial EMI Filter

Having shown in the previous sections that a single inductance cancellation winding can be used with two capacitors to improve filtration performance, and that the coupling orientation of multiple windings in a single filter does not adversely affect potential inductance compensation, the use of multiple element inductance compensation in the context of common- and differential-mode EMI filter is examined. A commercially-available filter is used as a starting point.

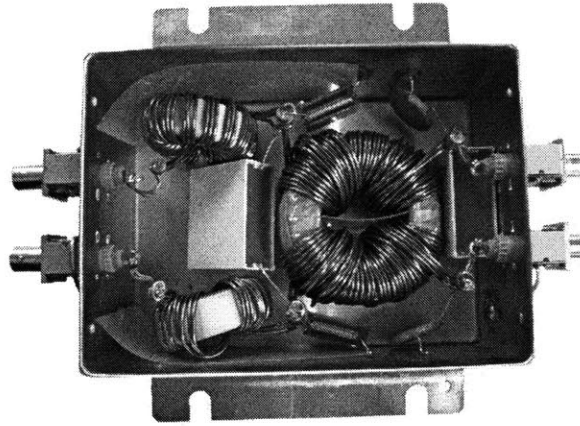
Figs. 3.14(a) and 3.14(b) show the schematic and physical views of the filter, which is rated for up to 250 volts and 25 amps of 50/60Hz alternating current. The large ($15\mu\text{H}$) series inductors L_{11} and L_{12} are particularly bulky, heavy, and expensive components of the commercial filter, and it would be desirable to eliminate them provided that filter performance is preserved. The series inductors were removed to provide working space for installing the inductance cancellation windings, and to provide an opportunity to offset their removal through use of the much smaller cancellation windings. Figs. 3.15(a) and 3.15(b) show the modified schematic and physical layout of the filter with the inductance cancella-

3.4 Application to Commercial EMI Filter

tion windings installed. Additionally, Fig. 3.16 shows the folded design of the inductance cancellation coil used in this filter. As with the previous coil in Fig. 3.7, Fig 3.16 was cut with an abrasive-jet cutter, using 2mm thick copper for enhanced current carrying capacity. The flat winding structure is folded at the center of its longest side to form a square one-piece two-layer winding with Mylar tape used as insulation between the layers. Based on simulation results, the coil is estimated to have a series inductance of 288.3nH, and a maximum equivalent shunt-path inductance of -81.2nH when used for single element inductance cancellation (in the magnetic winding T model). As in the previous test filters, the coil is purposefully over-designed for the required inductance cancellation to allow for additional design flexibility and testing.



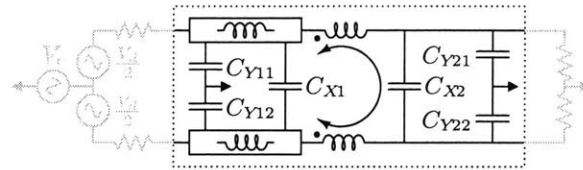
(a) Schematic



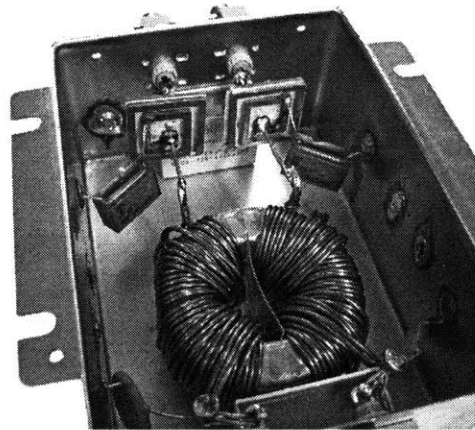
(b) Physical Layout

Figure 3.14: Original Commercial EMI Filter. L_{11} , L_{12} are $15\mu\text{H}$ wound toroidal inductors, C_{Y11} and C_{Y12} are Rifa PME-271 47nF film capacitors, C_{X1} and C_{X2} are Vishay Roederstein F1772-522-2030 $2.2\mu\text{F}$ film capacitors, C_{Y21} and C_{Y22} are 15nF ceramic capacitors, and the common-mode choke has measured leakage inductances of $30.2\mu\text{H}$ and a magnetizing inductance of 4.45mH.

Common- and differential-mode measurements were taken of the unmodified filter, as well as an intermediate step before the inductance cancellation windings were installed. In this intermediate step, the large inductors L_{11} and L_{12} were removed and straight, solid



(a) Schematic



(b) Physical Layout

Figure 3.15: Modified version of the EMI filter in Fig. 3.14 with L_{11} and L_{12} removed, and two inductance compensation windings installed.

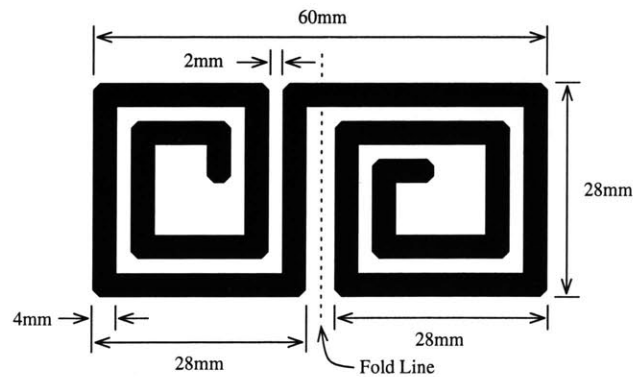


Figure 3.16: Illustration of folded winding used for inductance compensation in the EMI filter of Section 3.4, fabricated from 2mm thick copper. When folded, the total series inductance is 288.3nH, and the maximum equivalent shunt-path inductance for a single element is -81.2nH (in the magnetic winding T model).

14ga wire was installed in their place. This configuration, referred to here as *Without Series Inductor*, was used as a baseline comparison for improvements based on inductance cancellation.

The tuning procedure outlined here is the same as the one used in Section 3.3, and was developed for tuning the filter response due to the common- and differential-mode capacitors. Initially, the connections of common-mode capacitors C_{Y1} and C_{Y2} are tuned simultaneously to compensate (in a symmetric fashion) for their parasitic inductances. Once the optimal positions are found, the capacitors are permanently attached to their respective windings. Following this, the differential-mode capacitor C_{X1} is tuned by moving its connections on both coils symmetrically to find an optimal output response.

This order of tuning makes sense: the common- and differential-mode capacitors do not impact system performance in the same way. In Fig. 3.5(a) it can be seen that the common-mode equivalent circuit is not influenced by the differential-mode capacitance (or the inductance cancellation, other than through the fixed series inductance introduced by the winding); the common-mode filtration operates as if the differential-mode capacitor were an open circuit. However, the differential-mode filtration is dependent on the common-mode capacitance and inductance cancellation. This means that if the inductance compensation for the common-mode capacitance is optimized first, the inductance compensation for the differential-mode capacitor can be tuned subsequently without influencing the common-mode performance.

The results of the completed tuning are shown in Fig. 3.17 along with the stock and baseline filter configurations. It should be noted that tuning of both the common- and differential-modes is based on compromises between high and low frequency performance. This particular “optimal” output response chosen here may not be the highest achievable performance for a particular range of frequencies of interest.

The results of incorporating the inductance cancellation coils reveal a dramatic improvement in the filtration performance for both the common- and differential-mode responses over the baseline (stock filter with L_{11} and L_{12} removed, labeled as *without series inductor*). The common-mode shows improvement across its full range, and the differential-mode shows substantial improvement over its full range except for the small resonance around 2MHz. (This small resonance is caused in part by the capacitor-inductor-capacitor π -section

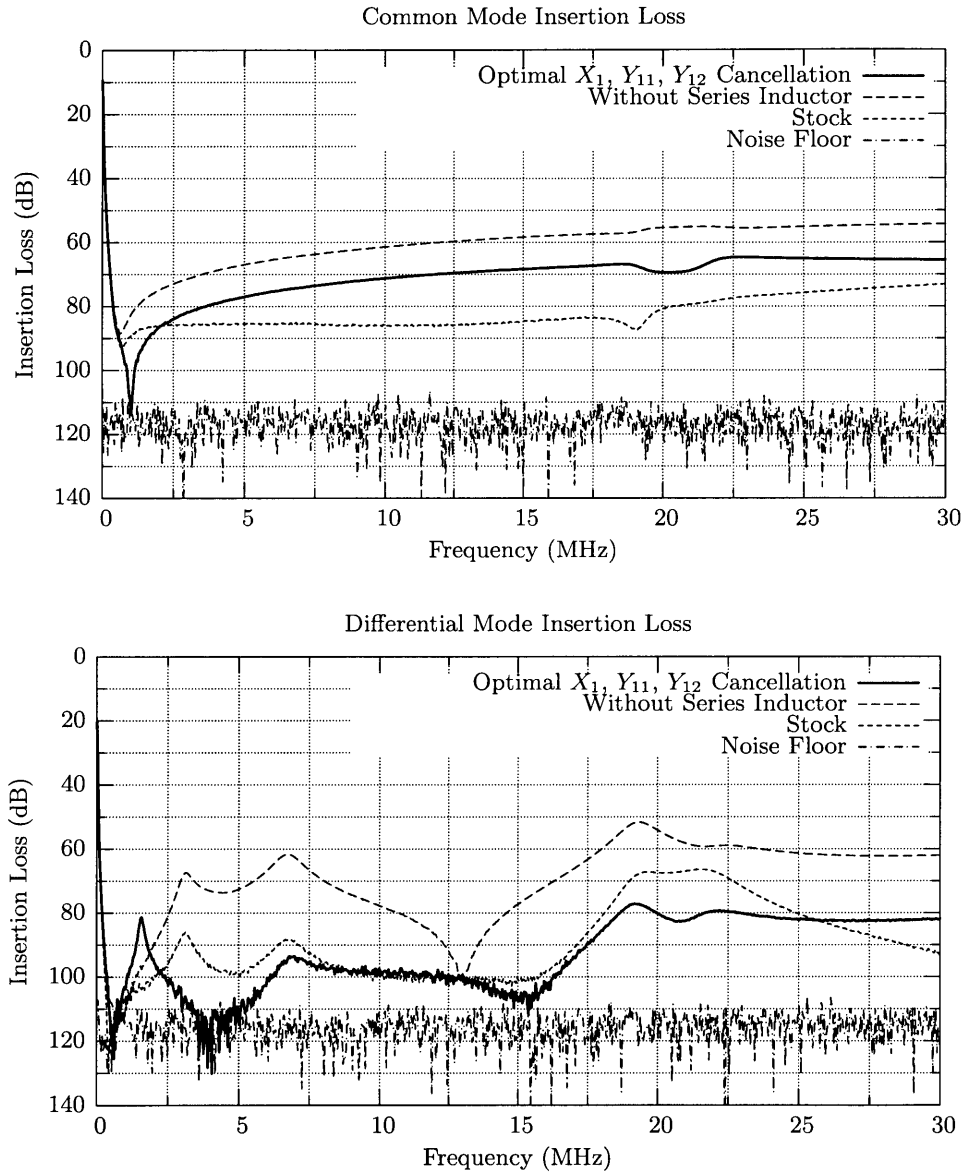


Figure 3.17: Performance comparison of the commercially-available EMI filter in Fig. 3.14 and the modified version in Fig. 3.15, showing performance both without and with inductance compensation.

Table 3.1: Published common- and differential-mode 50Ω circuit insertion loss specifications for the commercially-available EMI filter considered in Section 3.4. All measurements are listed in dB.

	Frequency (MHz)								
	0.01	0.03	0.05	0.1	0.5	1.0	5.0	10.0	30.0
Common-Mode	2	14	22	36	75	75	70	70	48
Differential-Mode	14	14	17	42	75	75	70	70	50

formed with the two capacitors attached to the inductance compensation winding in the differential-mode, and can be reduced by fabricating a winding with lower series inductance than the over-sized one used here.)

The common-mode performance with inductance compensation is somewhat worse than the stock filter by approximately 10dB, while the differential-mode performance is very comparable, even without L_{11} and L_{12} . More importantly, the performance with the inductance cancellation windings exceeded the commercially-published performance specification of the stock filter, shown in Table 3.1, without requiring the large, expensive series inductors of the stock filter.

The results from this commercial EMI filter, as well as those from the test filters in Section 3.1, show clearly that a single magnetically coupled winding can provide effective inductance compensation for two capacitors. Moreover, it is demonstrated that the performance of a commercial filter design can be preserved at lower component weight and cost through use of the proposed approach. It is anticipated that further substantial design improvements could be achieved in a filter expressly designed to take advantage of the inductance compensation method proposed here.

3.5 Analytic Formulations

In this section an analytical basis is sought for the proposed method of compensating for the inductance of two capacitors using a single coupled magnetic winding. It is derived from an extension of the methods used to analyze single-capacitor inductance cancellation techniques. The predictions of this method are then compared to measured results to illustrate its usability.

3.5.1 Extended Cantilever Model

Analysis of inductance cancellation windings with a single capacitor is relatively straightforward since a two-port transformer model of the windings is used, which has only three independent terms. The number of independent terms needed to completely describe coupled magnetics with n terminals is given by $n(n + 1)/2$ [20], which grows as the square of n .

Adding to the complexity is the fact that many models for multiple winding transformers either do not adequately model the complete transformer behavior, or have poor correlation and numeric conditioning to attempted measurements of model parameters from terminal characteristics [21, 22]. One model that is effective, and well conditioned for experimental parameter extraction, is the Extended Cantilever Model [20, 21].

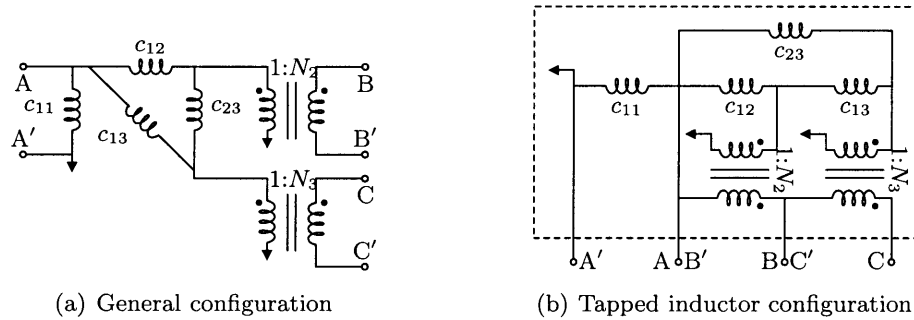


Figure 3.18: Three-port extended cantilever models.

The Extended Cantilever Model of a coupled system yields an equivalent circuit with directly measurable parameters and provides a direct mapping between circuit parameters and the inductance matrix parameters. It is also well conditioned numerically when dealing with small leakage fluxes or high coupling factors. The extended cantilever circuit model for a three-port system is shown in Fig. 3.18(a), with circuit parameters related to impedance matrix parameters as follows:

$$Z = sL \tag{3.1}$$

$$B = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} \\ Z_{21} & Z_{22} & Z_{23} \\ Z_{31} & Z_{32} & Z_{33} \end{bmatrix}^{-1} \quad (3.2)$$

$$N_k = \frac{Z_{1k}}{Z_{11}} \quad (3.3)$$

$$c_{11} = Z_{11} \quad (3.4)$$

$$c_{ij} = -\frac{1}{N_i N_j b_{ij}} \quad (3.5)$$

where b_{ij} is the $(i, j)^{\text{th}}$ element of B .

It should be clarified that the notation used to indicate the impedance matrix Z is representative of only the reactive component of Z due to the equivalent inductance; the extended cantilever model in [20] is formulated only with consideration to inductances. An extension which allows for full Laplace domain circuit elements can be found in [23, 24], however in the idealized case considered here, parasitic resistances and capacitances are assumed to be negligible.

3.5.2 Three-Port Analysis

Fig. 3.18(b) shows the application of the extended cantilever model to a center-tapped winding with two tap points. Fig. 3.19 shows additional circuit connections used for finding the system transfer function. The full transfer function for the system is given in Appendix A, and truncated versions are utilized in this section where appropriate.

By analogy to the case of inductance cancellation for a single capacitor, we desire to find conditions that drive the transfer function from the input source to the output voltage to zero (or close to zero). In finding where the transfer function goes to zero, conditions must be found where both the numerator becomes zero, and the denominator remains finite and non-zero. Starting from the numerator of the full transfer function in (A.1) from Appendix A, setting it equal to zero, refactoring, and dividing by the non-zero value of z_l , a condition is found in which a zero in the numerator can be generated:

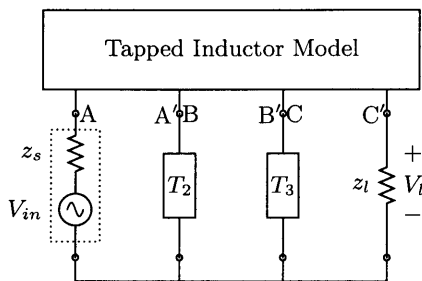


Figure 3.19: Shared-terminal three-port circuit for use with the Extended Cantilever Model tapped-inductor configuration of Fig. 3.18(b). T_2 and T_3 represent the (inductive) high frequency impedances of the capacitors.

$$0 = Z_{13} (Z_{12} + Z_{23} + Z_{13} + Z_{22}) - (T_2 - Z_{12} - Z_{13}) (T_3 - Z_{13} - Z_{23}) \quad (3.6)$$

This result, considered by itself, provides a number of terms that can be adjusted to satisfy the equality. However, in the case of common-mode and differential-mode filtering there are additional constraints that must be considered.

3.5.3 Common- and Differential-Mode Optimization

As described previously in Sections 3.3 and 3.4, in an EMI filter the common- and differential-mode capacitors do not impact system performance in the same way: the common-mode filtration operates as if the differential-mode capacitor were an open circuit, while the differential-mode filtration is dependent on the common-mode capacitance and its inductance cancellation. To find the optimal cancellation for the common-mode capacitor, the transfer function in (A.1) is considered at the limit where $T_3 \rightarrow \infty$ (the differential-mode capacitance is a virtual open circuit for common-mode signals).

$$H(s) = \frac{(T_2 - Z_{13} - Z_{12}) z_l}{\dots} = 0 \quad (3.7)$$

From this result, it is shown that if $T_2 = Z_{12} + Z_{13}$, then full cancellation in the common-mode can be achieved. With the common-mode cancellation constraint met, the result is

then inserted back into the original transfer function in (A.1) to find the constraint placed on the differential-mode compensation:

$$H(s) = \frac{Z_{13} (Z_{12} + Z_{23} + Z_{13} + Z_{22})}{\dots} = 0 \quad (3.8)$$

The numerator of this result contains no terms of T_3 in which to tune in comparison to the terms of the impedance matrix. Additionally, the terms of the impedance matrix in a cylindrically or concentrically wound coil configuration are positive, preventing simple geometries from creating a zero in the transfer function. If differential-mode compensation is to be achieved, this result seems to provide no opportunity for the transfer function to become zero, save for the possibility of making $Z_{13} = 0$. In the case where Z_{13} can be made zero, the transfer function denominator would remain finite and non-zero, representing a possible condition to generate a zero for the transfer function, if the structure can be arranged to provide it.

Another consideration may apply in this case. In past work [6] it was shown that depending on the frequency range of interest, filter performance, even with imperfect cancellation, may be perfectly adequate for practical purposes. With imperfect cancellation, a new term Δ_2 can be defined to be the effective residual shunt-path impedance of the capacitor. More specifically, $\Delta_2 = T_2 - (Z_{12} + Z_{13})$. If this is substituted into the general condition in (3.6), and with the resulting equation rearranged, (3.9) results. This provides a relation where Z_{13} is not explicitly required to be zero for the transfer function to become zero.

$$0 = Z_{13} (T_2 + Z_{22} + Z_{23}) - \Delta_2 (T_3 - Z_{23}) \quad (3.9)$$

Hence, one may gain good performance in both common-mode and differential-mode by realizing substantial (but not perfect) cancellation in common-mode to benefit differential-mode performance.

3.5.4 Simulation and Model Validation

To validate the model and transfer function analysis, the common- and differential-mode filters constructed in Section 3.3 are used as the basis for simulation, excluding the coupling between the two coils. Each of the measurements presented in the section is simulated here using the model developed, to allow comparison to the experimental results.

To simulate both common- and differential-mode responses, the equivalent circuit models for each mode are constructed. These equivalent circuit models, shown in Fig. 3.20, include the inductance compensation windings, as well as the equivalent series resistance and equivalent series inductance of each capacitor. This allows for the direct use of (A.1) from Appendix A, the transfer function of the circuit in Fig. 3.19.

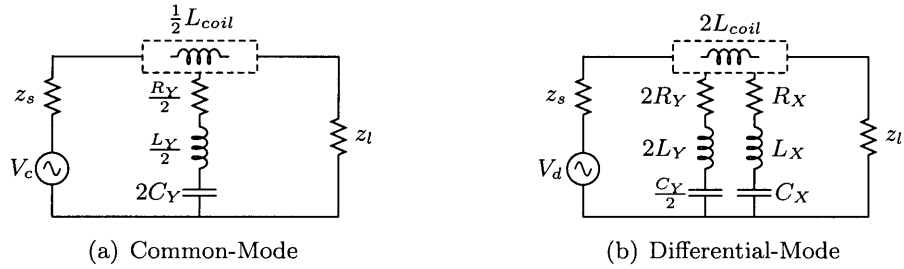


Figure 3.20: Common- and differential-mode equivalent circuits used to simulate the filters in Section 3.3.

For simulation, both the line-to-ground (Y) capacitor (Panasonic ECK-ATS472ME6) and the line-to-line (X) capacitor (Rubycon 250MMCA334KUV) are modeled with first-order equivalent series resistance, equivalent series inductance, and bulk capacitance. The nominal value of capacitance, along with the measured values of inductance and resistance, are used in the model of each capacitor. The parameters are: $R_Y=200\text{m}\Omega$, $L_Y=48.6\text{nH}$, $C_Y=4700\text{pF}$, $R_X=50\text{m}\Omega$, $L_X=49.4\text{nH}$, $C_X=330\text{nF}$. The source and load impedances, z_s and z_l respectively, match those of the network analyzer, 50Ω . The coil used in the test filters, shown in Fig. 3.7, is represented by the inductance matrix L_{coil} , which is obtained using the numerical inductance calculation tool FastHenry:

$$L_{coil} = \begin{bmatrix} 36.52 & 42.62 & 0.236 \\ 42.62 & 224.6 & 8.089 \\ 0.236 & 8.089 & 5.262 \end{bmatrix} \text{ nH}$$

For common-mode, T_3 is set to $1\text{M}\Omega$ to approximate an open circuit, and T_2 is set to the effective impedance of the Y capacitor, $Z_{Y_{CM}} = \frac{1}{2} (R_Y + (j\omega C_Y)^{-1} + j\omega L_Y)$. For the differential-mode simulation, the effective impedance of the Y capacitor is different. With the two capacitors in series, the effective impedance, and thus T_2 , now becomes $Z_{Y_{DM}} = 2 (R_Y + (j\omega C_Y)^{-1} + j\omega L_Y)$. The effective impedance of the X capacitor is $Z_{X_{DM}} = R_X + (j\omega C_X)^{-1} + j\omega L_X$, the value used for T_3 .

The results of the common- and differential-mode simulations are shown in Fig. 3.21. Comparing the simulation results to the experimental data in Fig. 3.12, the differential-mode results do match in an absolute sense. The *Optimal Y (DM)* simulation is roughly between the two measured coupling cases, which is understandable given coupling between the coils is not modeled. However, the addition of the X capacitor in the *Optimal Y, Uncancelled X (DM)* fails to match the same downward-shift in resonance to near 20MHz, which exists in both experimental measurements. The shift of this resonance is representative of an increase in effective inductance in the Y capacitor branch, which may be a result of unmodeled inductive coupling between the X and Y capacitors. The important similarity between the experimental measurements and the simulation is seen comparing *Optimal Y, Uncancelled X (DM)* and the final trace *Optimal Y, Optimal X (DM)*. By appropriately locating the X capacitor on the coil, it is possible to both shift the resonance higher in frequency, and to increase the attainable attenuation.

If consideration is given to modeling the increase in effective inductance in the Y capacitor branch when the X capacitor is present, significantly improved correlations between the experimental measurements and the model simulation result. If $Z_{Y_{DM}}$ is increased by a modest 20% to make $Z_{Y_{DM}} = 2 (R_Y + (j\omega C_Y)^{-1} + j\omega (L_Y + 0.2L_Y))$, and the tuning location of the X capacitor on the coil is slightly moved (by 1.5mm), a refined inductance matrix yields,

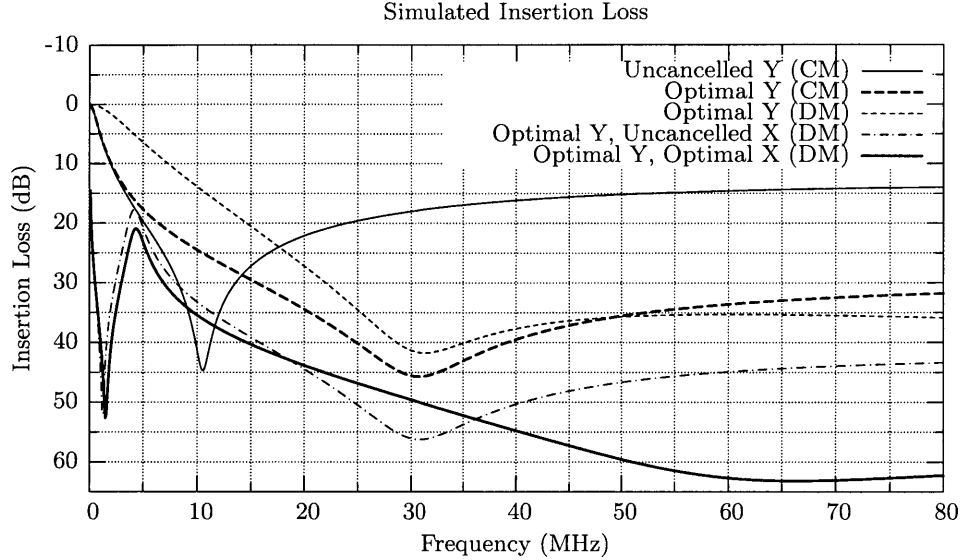


Figure 3.21: Simulated results for the filters in Section 3.3, using the circuits shown in Fig. 3.20. Note the different frequency range than in Fig. 3.12.

$$L_{coil} = \begin{bmatrix} 36.52 & 42.29 & 0.563 \\ 42.29 & 222.4 & 9.091 \\ 0.563 & 9.091 & 5.432 \end{bmatrix} \text{ nH}$$

the plot in Fig 3.22 results. These results correlate significantly better than the case without the added effective inductance, although differences are still notable for *Optimal Y, Uncancelled X (DM)*.

Given the substantial modeling simplifications used in creating these simulations (e.g. neglecting coil-to-coil and other mutual couplings, using simple numerical simulations to obtain coil inductances, etc.) the degree of accuracy of the model is striking, confirming its usefulness for understanding the behavior of such systems.

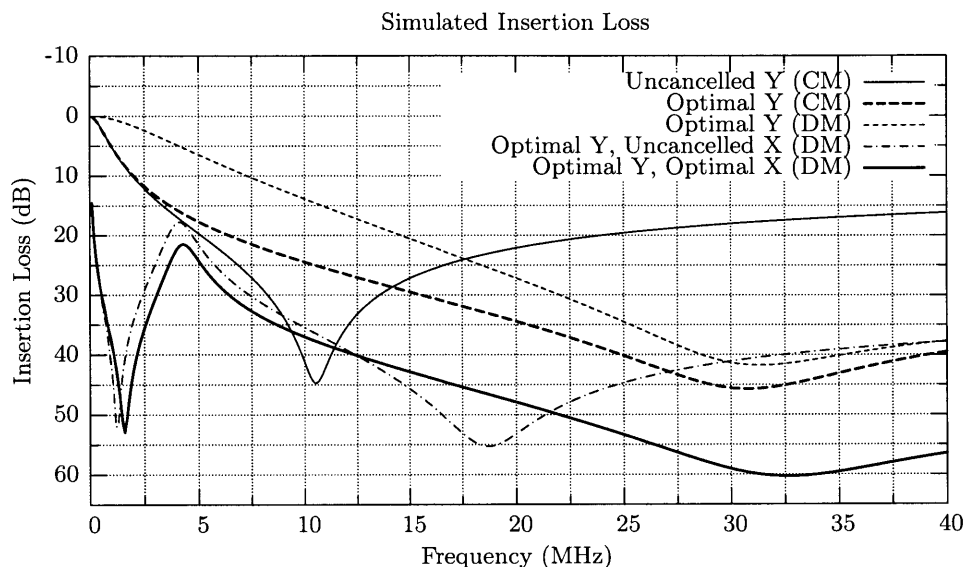


Figure 3.22: Simulated results for the filters in Section 3.3, using the circuits shown in Fig. 3.20 with additional differential-mode Y capacitor inductance.

3.6 Conclusion

The size and performance of discrete EMI filters are often limited by their component parasitics, such as the equivalent series inductance of capacitors. Implementing inductance cancellation traditionally requires at least one winding for each capacitor, increasing the volume and cost of the filter if all capacitor inductances are to be cancelled in a balanced fashion.

This chapter has extended the inductance cancellation presented in Chapter 1 by developing a method that allows for the use of a single magnetic winding to compensate for the effects of equivalent series inductances of two capacitors, instead of just one.

This multiple-element compensation method was applied experimentally to both test filters and to a commercially-available EMI filter with great success. Further, the coupling of closely oriented magnetic windings was also investigated, illustrating their successful use in constrained spaces, and a possible avenue for optimizing winding size. Finally, an analytical basis for the inductance compensation is developed and compared to experimental results.

Balanced Cancellation

THIS chapter presents an alternative implementation of inductance cancellation where two windings, one for each capacitor terminal, are utilized to create a balanced four-terminal filter with minimized shunt inductance. The implementation provides *balanced* impedances in the source and return paths that may be desirable in some applications. Additionally, fabrication techniques from Chapter 2 and results from the coupling of inductance cancellation windings in Section 3.3 are combined to create a novel four-terminal integrated filter element with performance at the same level of an equivalent three-terminal design.

4.1 Motivation

Three terminal filter elements inherently create an imbalance between the source and return paths of the circuit due to presence of the series inductance of the cancellation winding. In many applications this is perfectly acceptable. However, in filters designed to attenuate both common- and differential-mode signals, such as the filters presented in Section 3.1, this can contribute asymmetries which cause cross coupling between the differential and common-mode signal sources. Four-terminal elements can maintain symmetry (or balance) for common- and differential-mode signals. Moreover, use of a balanced four-terminal element provides consistent shunt-path impedance for differential mode signals independent of (balanced) interconnect lead lengths.

Results from a filter using two “balanced” inductance cancellation windings have been presented in [1], illustrating performance similar to that obtainable with a single winding. This chapter extends this work, implementing balanced cancellation for the Vishay BCcomponents 2222-338-24334 330nF capacitor used previously in Section 2.3.1. Furthermore, a

second design is presented where the coupling of flux between the two windings is utilized, yielding an integrated filter element with performance of an equivalent three terminal design, while being amenable to fabrication using the methods established in Chapter 2.

4.2 Flux Coupling

As shown in Section 3.3, the coupling of two windings can have an appreciable effect on the effectiveness of inductance cancellation. The results of this investigation show that for differential-mode signals, orienting the coupled coils such that the fluxes are additive increases the effective inductance of each winding. This result is conceptually intuitive when considering the flux coupling in a single cancellation winding, as shown in Fig. 1.3. Extending this illustration, Fig. 4.1 shows the flux linkages and orientations of two separate windings, when driven with a differential signal.

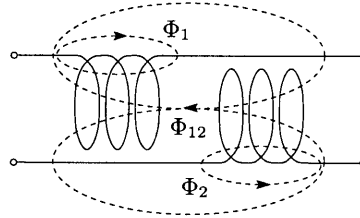


Figure 4.1: Illustration of the flux coupling of two inductance cancellation windings when drive by a differential signal. A capacitor is connected such that each terminal is connected to a separate winding.

4.3 Design and Fabrication

Using the winding structure in Fig. 2.14(a) as a starting point, slight modifications were made to arrive at the design in Fig. 4.2. The goal was to use as close a design as possible to the single two-layer winding design to compare the relative effectiveness of the balanced design. Each of these windings occupies nearly the same footprint area as the parent two-layer design, and utilize nearly the same conductor length.

Simulation results of a single winding gives an inductance matrix of

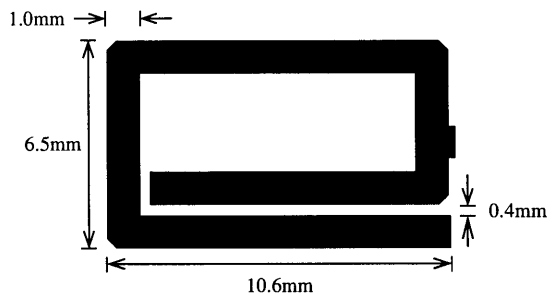


Figure 4.2: Illustration of the winding design used for implementing balanced inductance cancellation for the 330nF capacitor.

$$L = \begin{bmatrix} 12.0 & 2.1 \\ 2.1 & 4.7 \end{bmatrix} \text{ nH}$$

with a total series resistance of $1.3\text{m}\Omega$ at 60Hz. For both the uncoupled and coupled implementations, two windings are insulated and individually joined to separate capacitor terminals, creating a four-terminal filter element. Photographs of prototype filter elements containing this winding design are shown in Fig. 4.3 and 4.4 for the uncoupled and coupled implementations respectively.

To minimize flux coupling in Fig. 4.3, the windings have been joined with the capacitor, extending outward from each terminal. The second design, utilizing the flux linkage between the windings, places both windings in close proximity in the footprint area of the capacitor. Additionally, this design can be fabricated using a slightly modified method from those developed in Chapter 2, allowing for a consistent and reliable integrated filter element to be manufactured.

To adapt the construction methods from Section 2.2 to the coupled balanced filter element, the step illustrated in Fig. 2.5(b), where a solder mask is created, is not performed. The coupled set of windings for the balanced filter element remain entirely insulated from one another, and are not electrically joined. Without joining the two layers together electrically, the alignment of the two winding sheets is maintained using an electrically insulating adhesive, or a two-sided adhesive tape such as Mylar or Kapton. Additionally, when encapsulating the final filter element, small changes in the potting height, as illustrated in

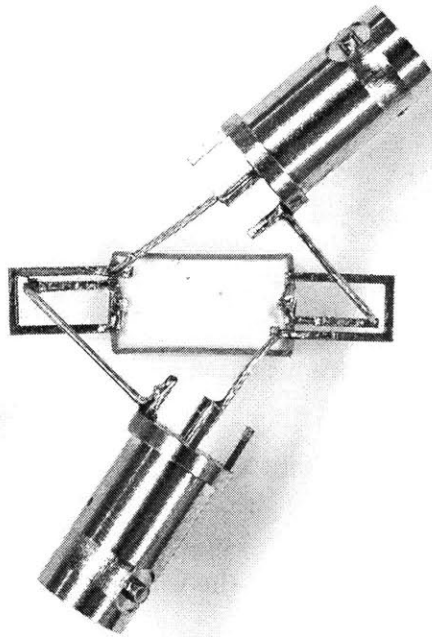
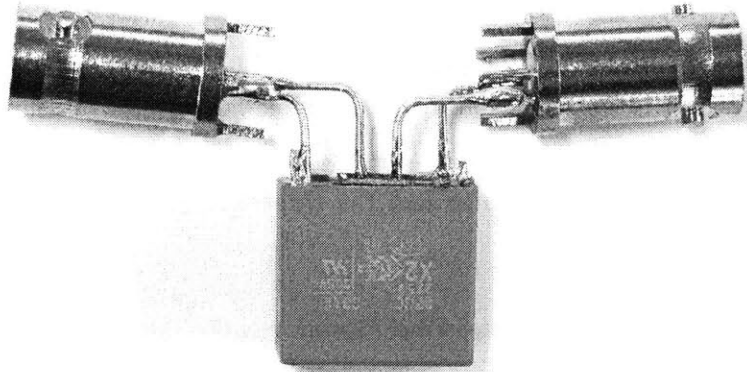
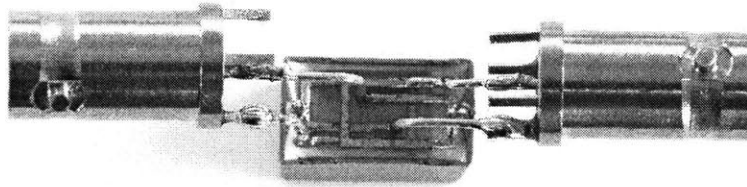


Figure 4.3: Top view photograph of a 330nF four-terminal filter element with *uncoupled* balanced inductance cancellation. The windings can be seen here extending outward from each terminal of the capacitor to minimize any flux coupling between windings.



(a) Side view



(b) Top view

Figure 4.4: Side and top view photos of a 330nF four-terminal integrated filter element with *coupled* balanced inductance cancellation. The two windings are sandwiched together within the footprint of the capacitor to provide meaningful flux coupling.

Fig. 2.7, will not affect the final component performance in an appreciable way as it did with the three-terminal implementation.

4.4 Performance

For the uncoupled configuration, the two windings are expected to provide a total cancellation of 4.1nH, which is less than half of the total capacitor equivalent series inductance of 9.9nH. This is readily seen in Fig. 4.5, where the insertion-loss measurement lies between that of the unmodified capacitor and the three-terminal filter element presented in Section 2.3.1.

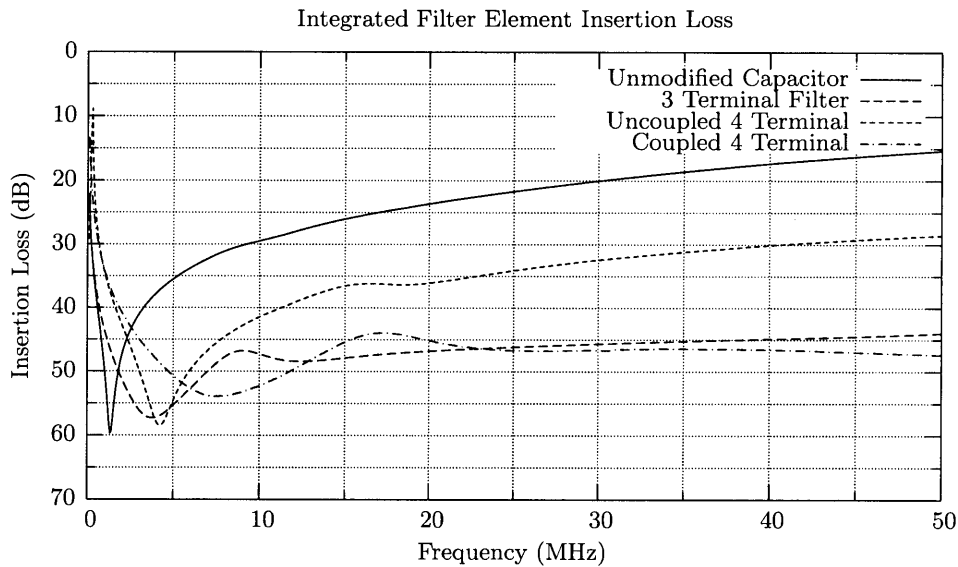


Figure 4.5: Insertion-loss comparison between the uncoupled and coupled four-terminal filter elements, a standard capacitor, and integrated filter element from Chapter 2. All designs use the Vishay BCcomponents 2222-338-24334 330nF X2 capacitor.

The insertion-loss performance of the coupled winding implementation can also be seen in Fig. 4.5, showing a significant improvement over the uncoupled design, and illustrating its ability to achieve performance at or near the same level as the three-terminal single-winding filter element. This allows a four-terminal filter element to be utilized when necessary without a sacrifice in performance.

4.5 Future Work

While this chapter has shown that coupled cancellation coils can be implemented to create a four-terminal filter element, an analytical model has not yet been developed. Implementing the extended cantilever model, as done in Section 3.5 shows promise, however the insertion-loss transfer function results in a relationship with an order of magnitude more terms than in (A.1). Alternative transformer or coupled-inductor models may prove to generate more insightful results.

4.6 Conclusion

This chapter has provided an additional implementation of inductance cancellation utilizing two windings in a balanced configuration. A design utilizing the coupling of flux between the windings has been shown to provide equivalent insertion-loss performance, and automated fabrication potential.

Summary and Conclusions

5.1 Thesis Summary and Contributions

The research presented in this thesis was undertaken to extend the inductance cancellation implementation and design approach from the work in [14]. Focus was placed on enhancing the manufacturability and usability of integrated filter elements, and on more effectively addressing common- and differential-mode filter topologies, such as those designed for attenuating EMI.

The major contributions of the work presented in this thesis can be separated into three main areas: integrated filter element fabrication methods for low- to medium-volume production, multiple capacitor inductance compensation for common- and differential-mode filters, and balanced inductance cancellation with coupled windings.

5.2 Future Work

A number of loose ends remain at the conclusion of this thesis, the majority surrounding the development and understanding of models for the coupling of separate windings. Section 3.3, and even more so Section 4.2, rely on multi-port coupled magnetics having circuit models which offer significantly more complexity than the elegant two-port T-model presented in Chapter 1. The development of a reduced-order physically-based model would make the design of these more complicated inductance cancellation implementations more tractable.

Three-Port Tapped-Inductor Extended Cantilever Model Transfer Function

Equation (A.1) gives the analytic solution of the transfer function from input voltage V_{in} to output voltage V_l for the circuit in Fig. 3.19. The result was found using direct circuit analysis, with the source network consisting of an input voltage source V_{in} with series impedance z_s , and a load network comprised of an impedance z_l . T_2 and T_3 are arbitrary impedances representing the two capacitors.

$$\begin{aligned}
 H(s) = & \frac{(T_2 T_3 - Z_{13} T_3 - Z_{12} T_3 - Z_{23} T_2 \\
 & - Z_{13} T_2 + Z_{12} Z_{23} - Z_{13} Z_{22}) z_l}{T_3 z_l z_s + T_2 z_l z_s + Z_{22} z_l z_s + T_2 T_3 z_s \\
 & + Z_{33} T_3 z_s + 2Z_{23} T_3 z_s + Z_{22} T_3 z_s \\
 & + Z_{33} T_2 z_s + Z_{22} Z_{33} z_s - Z_{23}^2 z_s \\
 & + T_2 T_3 z_l + Z_{11} T_3 z_l + Z_{22} T_2 z_l + 2Z_{12} T_2 z_l \\
 & + Z_{11} T_2 z_l + Z_{11} Z_{22} z_l - Z_{12}^2 z_l \\
 & + Z_{33} T_2 T_3 + 2Z_{23} T_2 T_3 + Z_{22} T_2 T_3 \\
 & + 2Z_{13} T_2 T_3 + 2Z_{12} T_2 T_3 + Z_{11} T_2 T_3 \\
 & + Z_{11} Z_{33} T_3 + 2Z_{11} Z_{23} T_3 + Z_{11} Z_{22} T_3 \\
 & - Z_{13}^2 T_3 - 2Z_{12} Z_{13} T_3 - Z_{12}^2 T_3 + \\
 & Z_{22} Z_{33} T_2 + 2Z_{12} Z_{33} T_2 + Z_{11} Z_{33} T_2 \\
 & - Z_{23}^2 T_2 - 2Z_{13} Z_{23} T_2 - Z_{13}^2 T_2 \\
 & + Z_{11} Z_{22} Z_{33} - Z_{12}^2 Z_{33} - Z_{11} Z_{23}^2 \\
 & + 2Z_{12} Z_{13} Z_{23} - Z_{13}^2 Z_{22}}
 \end{aligned} \tag{A.1}$$

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