Design and Analysis of a 6/4-GHz Receiver Front End

by

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ABSTRACT

This thesis presents the design and analysis of a miniaturized receiver front end for C-band satellite application. The use of monolithic microwave integrated circuit (MMIC) techniques, promises significant savings in mass and volume over current flight hardware. The receiver system is analyzed in terms of its prescribed performance requirements. Particular attention is placed on the downconversion unit, in order to establish component specifications which will enable compliance with the receiver spurious requirements. Based on the established component specifications, a local oscillator is designed. Several possible realizations are investigated, including phase-locked loop and multiplier chain. The multiplier chain approach is selected for advantages of performance, reliability, power consumption, and size. Reference frequency in the local oscillator chain is provided by a low-noise, low-power temperature compensated crystal oscillator. Comb generation is achieved using MMIC silicon amplifiers with bias and drive levels adjusted for best performance. Several filter technologies are considered, including surface acoustic wave, microstrip coupled-line, microstrip interdigital, and dielectric blocks. The driver stage is implemented with an MMIC gain block. Computer simulations are performed and breadboard is constructed to illustrate the local oscillator design concept. The experimental local oscillator is then evaluated against design performance goals as well as simulation results. The successful breadboard prototype is compliant with all performance specifications.

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Chapter 1
Introduction

1.1 Background and Motivation

Satellite communication traffic volume has grown exponentially over the past 25 years. Comparable growth rate is projected to continue until the turn of the century [1]. Such rapid expansion is largely due to the continual growth in global demand for telecommunications services including voice, video, and data [2]. Specific service items include television transmission, public telephony, telegraphy, telex, and mobile services. The number of satellites in orbit increases with traffic growth. The continual increase in the number of earth stations, installed to provide multiple-access communications, also increases significantly the demand in traffic, furthering stimulating the need for more satellites. The ever-increasing capacity of the INTELSAT series of satellites illustrates such a trend. INTELSAT I, launched in 1965, provided 480 half-circuits, whereas INTELSAT VI, launched in 1986, provided 80,000 half-circuits [1].

Increasing need for satellite coverage areas and associated hardware translates directly into increasing demand for satellite receivers. The Early Bird (INTELSAT I) satellite, launched in 1965, employed C-band frequencies for up-link (6 GHz) and down-link (4 GHz) [2]. C-band's usage continued to grow, with each subsequent INTELSAT series of satellites. Today's INTELSAT VI satellite contains approximately 50 transponders operating over C- and Ku-bands [3], in total employing sixteen C-band receivers [1].

As the number of communication satellites in use grows rapidly and the size and packaging density of satellite designs continue to increase, reliability, mass, cost, and efficiency of satellites become increasingly critical and relevant issues. In view of these needs, *miniaturization* of C-band communication components will yield significant improvement to the usefulness of C-band transmission. Miniaturization, through the application of monolithic microwave integrated circuits (MMIC) and other techniques, reduces fabrication cost, increases communications payload life, and decreases payload mass. The latter two factors further reduce the overall costs of satellite communication by extending satellites' useful life and cutting launch costs. MMIC implementation offers higher reliability through batch processing and reduction in parts count due to higher level of integration. Cost saving through MMIC implementation results from reduction in assembly and test times [2]. MMIC insertion has been applied to various transponder subsystems at different frequency bands and has repeatedly been shown to improve performance uniformity, reproducibility, and operational efficiency. Subsystems successfully subjected to MMIC insertion include step attenuators for transponder gain control [4], microwave switching matrices [5], phased-array transmit antennas [6], and solid-state power amplifiers [7].

Most commercial satellite programs at C- and Ku-band use hybrid microwave integrated circuit (MIC) technology for the receivers and other components. Compared to MMIC, MIC techniques have drawbacks in size, mass, cost, and reliability. A current C-band hybrid receiver typically weighs 1.7 kg and has approximate dimensions of 16 x 10 x 8 cm. Miniaturized receivers, realized through MMIC insertion and other techniques, may potentially reduce the size and produce mass savings of greater than 50% per receiver. Miniaturized receivers will also help to improve overall satellite capacity as a function of payload mass [2], by maximizing the given launch weight constraint [1], and enhance satellite system hardware reliability for 18- to 20-year life expectancy [8].

Recent advances in enabling technologies make the miniaturization of C-band receivers a practical goal. The relative maturity of MMIC technology over recent years allows its application to C-band receiver miniaturization. Key MMIC technology advances include improved design techniques employing accurate device and circuit models [9] tailored for fabrication process tolerant designs [10], refined fabrication techniques leading to higher process yields [11], uniform performance characteristics of MMIC components, space qualification of MMICs, and radiation resistance of gallium arsenide (GaAs) field-effect transistors [2]. Space qualification procedures have recently been developed and successfully applied to space-flight Ku-band MMIC amplifiers. The procedures include DC-biased isothermal life tests, manufacturing process control, wafer acceptance tests, lot acceptance tests, and accelerated life tests for reliability assurance [12]. Experimental results indicate that GaAs MMICs are inherently radiation hardened for space applications [13],[14]. There have been several developments of MMIC components for C-band receiver applications. A C-band two-stage MMIC low-noise amplifier (LNA) using metal-semiconductor FET (MESFET) devices has achieved 21-dB gain and 1.7-dB noise figure in the 5.9- to 6.4-GHz up-link band [15]. With high electron mobility transistors (HEMTs), a noise figure of better than 1 dB may be achieved [2]. A MMIC low-noise downconverter has also been developed [16].

Other enabling technologies for miniaturization include surface mount technology (SMT) and availability of new high-performance materials. SMT is attractive for miniaturization due to the availability of hermetic packaging for transistors, resistors, capacitors, and other components. The reduction of process variability associated with small-quantity production through various means has also contributed to SMT's viability. Improved interconnect technology in the area of thermal expansion issues strengthens SMT's usefulness [51]. New high-performance materials such as Kevlar PCB materials, magnesium alloys, and metallized plastics help to achieve miniaturization by enabling significant savings in mass.

Other metal matrix composite materials contribute through their notable thermal advantages [51].

In view of the above discussions, reduction in C-band receiver volume and mass is highly desirable using readily available and mature technologies. Some work has already been accomplished on receiver miniaturization. This thesis addresses the analysis and design issues relevant to the 6/4-GHz receiver front end and associated local oscillator.

1.2 Miniaturized Receiver Front End

This thesis presents the design and analysis of a miniaturized 6/4-GHz receiver front end. Design of the front end is drawn from previous receiver work related to INTELSAT satellites, with several design enhancements to achieve miniaturization.

The receiver is an integral subsystem in a communications transponder. A transponder receives broadband RF signals, channelizes the signals, and interconnects individual channels to transmitters in the IF bands [17]. Figure 1.1 outlines the block diagram of a communications transponder.

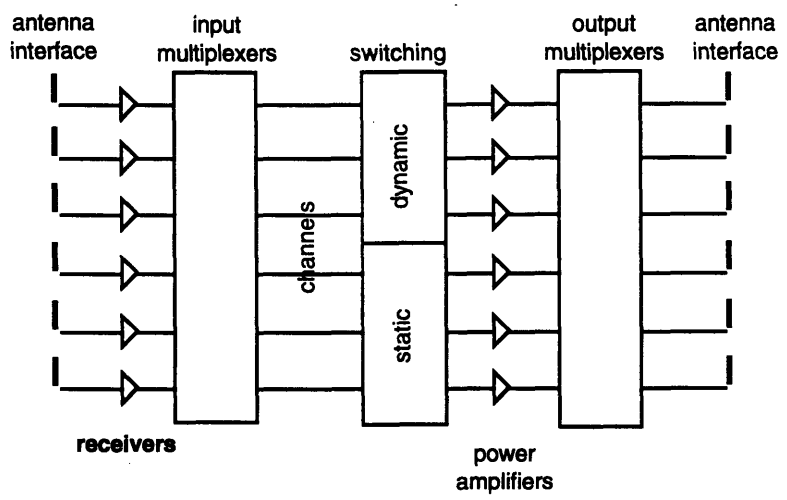


Figure 1.1 Block Diagram of Communications Transponder [17]

The receivers perform downconversion of the up-link RF signals to the down-link frequency. Waveguide filters and multiplexers channelize the frequency band. The individual receive-and-transmit channels are interconnected using switching matrices. The signals are then amplified and re-combined to the desired down-link transmissions.

Each receiver consists of two primary building blocks: receiver front end and gain block. The front end provides low noise amplification and downconversion of the 6-GHz input signal to the 4-GHz band [17]. The gain block amplifies the downconverted signal for IF processing and transmission. Design and implementation of the gain block in C-band receivers are well established. However, much remains to be done in realization of the front end.

In this thesis, the entire receiver system will be analyzed to determine specifications for each of the front end components. Since key receiver performance characteristics are determined by the interactions between the mixer, the local oscillator, and the IF filters, particular emphasis will be placed on the downconversion module. The second part for the completion of the front end is realization of the local oscillator. Requirements of the local oscillator

will be established based on receiver system analysis. Several reference multiplication approaches will be compared [20]. A detailed local oscillator design will be completed based on the approach which best meets the local oscillator specifications. Computer simulations and experimental measurements will be performed to illustrate and confirm the LO design concept. A breadboard prototype will be built as a final design performance confirmation.

1.3 Organization of Thesis

The organization of the thesis is as follows:

- **Chapter 2** presents a generalized receiver system design and analysis. The receiver system is divided into the front end and the gain blocks. The design methodology and analysis results are explained.

- **Chapter 3** focuses on analysis of the front end in terms of the receiver spurious specifications. Mixer performance is characterized to determine key specifications for the local oscillator and the IF filters.

- **Chapter 4** establishes the performance criteria of the local oscillator and presents the physical design of the local oscillator. The design starts with selection of the local oscillator (LO) implementation approach, continues with block diagram design, and completes with implementation of individual components in the block diagram. Simulation of the LO design is presented and discussed in light of measured results.

- **Chapter 5** presents the results of the experimental local oscillator.

- **Chapter 6** presents summary and conclusions and suggests design improvements for future local oscillator development efforts.

Chapter 2
Front End Analysis

2.1 Introduction

As part of a satellite transponder subsystem, the 6/4-GHz receiver provides low-noise amplification of the 6-GHz signals from the satellite antennas and also downconverts them to the 4-GHz band for channel filtering. It consists of two primary building blocks: receiver front end and gain block (Figure 2.1).

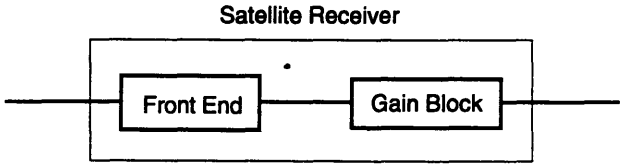


Figure 2.1 Satellite Receiver Blocks

The front end of the receiver provides low noise amplification and downconversion of the 6-GHz input signal to the 4-GHz band. A block diagram is shown in Figure 2.2.

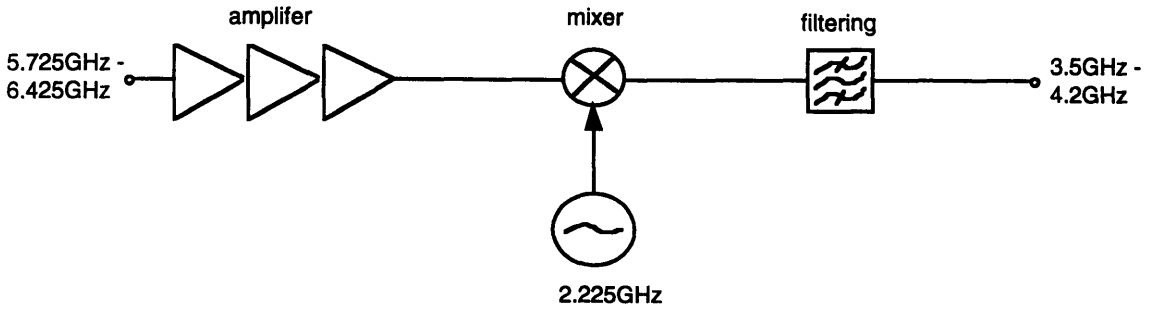


Figure 2.2 Block Diagram of Front End

The input RF signal (5.8-6.425GHz) is initially amplified to the appropriate power level. The mixer then downconverts the RF signal to the IF frequency (3.625-4.2GHz). IF filtering eliminates undesirable spurious signals.

The gain block provides flat, broadband amplification of the IF signal. A block diagram is shown in Figure 2.3.

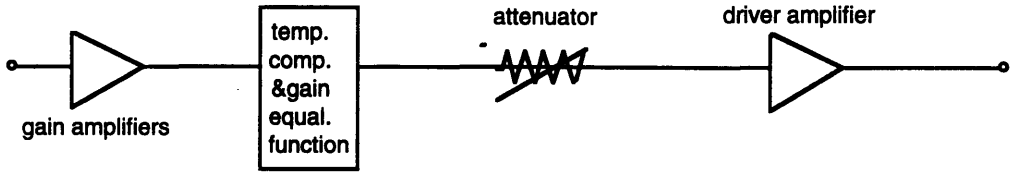


Figure 2.3 Block Diagram of Gain Block

Low level amplification gain devices boost the level of the carrier. The driver amplifier provides the necessary output power. The gain equalizer improves inband flatness and the performance over temperature. The attenuator is used to adjust the overall receiver gain to the desired level.

2.2 System Performance Criteria

Performance of the miniaturized C-band receiver must meet a set of specifications. The specifications are derived from the performance criteria of the popular INTELSAT satellite receivers. A summary of the major performance characteristics of the receiver front end is given in Table 2.1. Brief explanations of the key parameters follow.

Parameter	Requirement	Units
Input frequency	5.8-6.425	GHz nom
Output frequency	3.625-4.2	GHz nom
RF input power	-69 -76	dBm nom
Overdrive capability	20	dB min
RF output power	0	dBm nom
Gain		
Normal	69	dB max
High	76	dB min
Gain flatness		
Per channel	0.2	dB pp max
Full BW (500MHz)	0.5	dB pp max
Gain slope	0.007	dB/MHz max
Gain stability		
Temp (-10/+50°C)	0.7	dB pp max
Over life	0.9	dB pp max
Noise figure	2.7	dB max
Group delay	0.3	ns/ch max
Total phase shift (1 carrier)	1.5	deg max
FM crosstalk (2 carriers)	-175 + 20 log (fm)	dB max
C/I3 (2 carriers)	-26	dBc max
Spurious output		
Inband (3.625-4.2GHz)	-70	dBc max
Conversion products	-60	dBc max
Other (10MHz-18GHz)	-50	dBc max
LO frequency	2.225	GHz nom
LO frequency stability		
Temp (-10/+50°C)	±1	ppm max
Aging (per month)	±0.2	ppm max
Aging (10 years)	±2	ppm max
Short term (100Hz - 12kHz)	25	Hz rms max
Input/output return loss	19	dB min
DC power	7.6	watts max
Weight	1.4	kg max
Size	6 x 4 x 5	inches max

Table 2.1 Receiver Performance Requirements [19]

The receiver is to cover a bandwidth of 575MHz. It receives signals from the satellite antennas at preset power levels and transmits outputs signals to the satellite multiplexers. The receiver must adhere to the drive level specifications to achieve compatibility with the satellite components. Receiver gain also has associated with it a set of specifications in terms of

absolute gain levels, inband flatness, slope, and stability. Noise figure, the ratio of signal-to-noise on the input of a device to signal-to-noise on the output [44], is a key specification. It reflects the amount of noise the receiver system contributes to the carrier signal.

Carrier-to-third order intermodulation product ratio (C/I3) is another key parameter in receiver design. The receiver C/I3, an indicator of the distortions introduced by the system, largely depends on the signal strength of inputs to the amplifiers in the system and the use of attenuators. Amplifiers in the final stage are the most critical. The receiver must be designed such that C/I3 meets the specification under worst-case conditions, where attenuation is at a minimum and input power is at a maximum.

Spurious signal level is also critical to receiver design. Contributions to spurious signals in a receiver are dominated by the front end. In the front end, spurious signals are generated by the mixer modulating the RF with the LO signal to downconvert to IF [21]. The IF filters select the desired IF signals from the spurious spectrum. Overall spurious levels, which must meet the specifications in Table 2.1, are therefore primarily a function of mixer design, LO power, and IF filtering.

2.3 System Analysis

System analysis will be performed in two steps. The analysis performed in this chapter will permit a receiver to be designed which will meet all specifications with the exception of the spurious requirements. Compliance with the spurious requirements will follow detailed analysis of the downconversion unit, to be carried out in Chapter 3.

2.3.1 Initial System Design

Front End

System design of the receiver front end is based on the standard receiver configuration, shown previously in Figure 2.2. Modifications are made to adapt the basic design to one which meets C-band receiver specifications. An extremely low-noise amplifier is used at the front of the block. Pads are placed on both sides of the mixer to compensate for its poor return loss at the expense of additional conversion loss. Selection of the IF signals from the mixer output is performed by a combination of bandpass and bandstop filters. The bandstop filter is required due to the C-band downconversion scheme. The use of 5.8-6.425GHz RF frequencies, along with a 2.225GHz LO, results in a spurious component which lies very close to the IF band, namely the 2LO harmonic at 4.45GHz. A high-Q notch filter is therefore essential. LO drive level is chosen based on test measurements with an existing mixer, to minimize mixer conversion loss and its sensitivity over a range of LO power levels. In conjunction with proper pad placement, the RF chain modules, designed with sufficiently low voltage standing wave ratios (VSWRs), allow direct module connection without use of large isolators [51]. Initial system engineering based on the above principles has produced a set of front end component specifications which will enable the receiver to approximately meet its system requirements. The result is illustrated graphically in Figure 2.4.

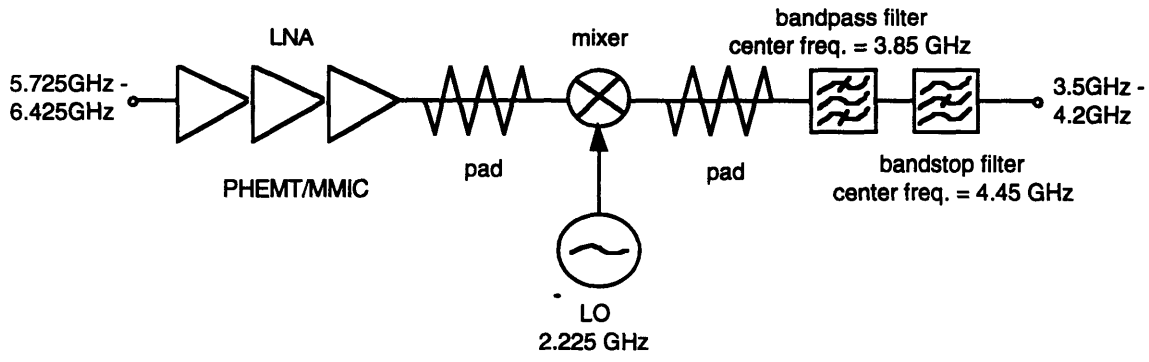


Figure 2.4 Design of Front End

Gain Block

System design of the receiver gain block is based on the standard gain block configuration, shown previously in Figure 2.3. Modifications are made to adapt the gain block to the C-band receiver application. The gain required to meet the desired output drive level is distributed across the entire gain block chain, in order to improve gain isolation. A MMIC digital attenuator implementation is chosen for its miniaturized form and low power consumption [51]. The attenuator commands the receiver gain to compensate for varying input RF levels and output power requirements. It also ensures linearity of receiver operation by backing off the carrier signal strength. The attenuator is strategically positioned toward the end of the chain, to minimize its impact on the noise figure. Temperature compensation may be performed internally in amplifiers with thermistors or externally with a stand-alone device. The external approach is chosen for its ability to compensate for a wider range of gain variation over temperature. Wide variation is expected due to high gain of 110dB over the entire receiver system. An isolator is added to help meet the receiver output return loss specification [17]. Based on the above design guidelines, amplifier, equalizer, and attenuator characteristics are chosen such that the overall gain block will be compatible with the receiver specifications of Table 2.1. Result of the gain block system design is illustrated in Figure 2.5.

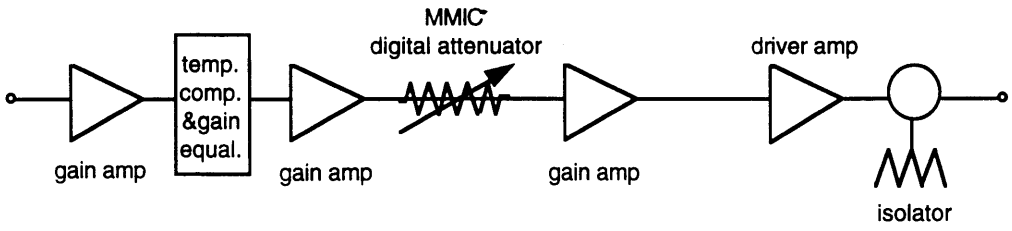


Figure 2.5 Design of Gain Block

2.3.2 Confirmation of Initial System Design

The preliminary system design of the receiver front end and gain block were rigorously examined using computer simulation, to ensure agreement with all receiver specifications. Computer simulation achieved more accurate projection of the relevant performance characteristics by accounting for many second-order effects not considered during preliminary system designs. The simulation tool used is *OmniSys*, a microwave-system simulation program [43].

The preliminary system design was entered into *OmniSys*. A simulation of various receiver performance measures was performed. Sub-system parameters were then modified in order to improve the receiver characteristics to be close to the required specifications. A brief summary of the changes follows.

Values of pads on the RF and IF ports of the mixer were adjusted to further improve return loss, thus helping to meet inband ripple specifications. Amplifier gains were redistributed to improve system noise figure performance. Other amplifier characteristics such as noise figure and compression were modified to more accurately reflect performance of existing devices. An isolator was added at the input to the LNA to improve input impedance matching. The results of the modifications are summarized in Table 2.2 and compared with the preliminary system design as well as the system specifications.

	Specifications	Preliminary Design	*OmniSys* Design
Output power	0dBm	8.8dBm	0.9dBm
Gain			
Normal	69dB max	79dB	71dB
High	76dB min	86dB	78dB
Gain ripple	0.5dB	1dB	0.5dB
Gain slope	0.007dB/MHz max	0.0023dB/MHz	0.0017dB/MHz
Noise figure	2.7dB max	1.2dB	1.4dB
Group delay	2.9ns	1.5ns	2.5ns
C/I3	-26dBc max	-18dBc max	-44.5dBc max
Input return loss	19dB min	15.6dB	17.2dB
Output return loss	19dB min	13.5dB	16.9dB

Table 2.2 Results of Receiver System Design with *OmniSys*

Output power was much closer to the specification. Attenuation throughout the system may be adjusted further to eliminate the additional 0.9dBm in output power. The same methodology may be used to reconcile the projected gain of the system, which was 8dB closer to specification but still 2dB too high. Gain ripple and C/I3 have been improved to be on par with the system specification. Gain slope has also been improved. Noise figure and group delay have been slightly degraded primarily due to the addition of lossy elements in the system. Input and output return losses have been improved as well. The 2dB discrepancy with the specifications may be remedied with the use of isolators.

Key receiver parameters, with the exception of spurious performance, were thus analyzed and improved by modifying the system design. The system performance projections were extremely close to, or exceeded, the required performance specifications. Study of the receiver's spurious performance, which required detailed analysis of the interactions among the mixer, the LO, and the IF filters, was then performed.

Chapter 3
Mixer Spurious Analysis

3.1 Introduction

The downconversion unit, consisting of a mixer, an LO, and IF filters, was analyzed in detail, so that the receiver system may be designed to meet the spurious requirements.

The mixer is the key element in a receiver sub-system. It translates the frequency of the incoming signal to an intermediate frequency (IF) where it is amplified with good selectivity and low noise. The mixer, which consists of a device capable of exhibiting nonlinear performance, is preceded by low-noise GaAs FET amplifier stages for best system noise figure. A double-balanced structure is chosen for its large signal-handling capability, port-to-port isolation, and spurious rejection. The excellent isolation among the three mixer ports, coupled with the high rejection of even-order harmonics, makes the double-balanced topology ideal for suppressed-carrier modulation. IF filtering requirements become more manageable when the amount of RF and LO signals appearing at the IF output are reduced by the carefully balanced wideband transformers [24]. These benefits of the double-balanced topology outweigh the higher LO drive it requires compared to single-ended and single-balanced structures.

Performance characteristics of the mixer determine the specifications of the local oscillator and the IF filters. The RF and LO drive levels, along with the isolation performance of the mixer, determine the levels of spurious output on the mixer IF port. This spurious out-

put in turn dictates the IF filtering requirements. The LO drive level, in addition to influencing spurious output, also modifies the conversion loss and conversion loss sensitivity of the mixer. The impedance match on the LO port of the mixer is critical during the design of the LO, so that the LO signal at the device has the appropriate amplitude. Because of the intimate cross-functional relationship among the mixer, the LO, and the IF filters, thorough analysis of subsystem interdependencies is necessary to ensure a functional downconversion unit.

The double-balanced MMIC mixer has been designed and fabricated. It was characterized to determine the receiver system configuration in terms of power levels, filtering, and matching, as well as to investigate whether the current mixer implementation is an appropriate one. The following mixer performance characteristics were tested:

- Conversion loss,
- Conversion loss sensitivity,
- Signal compression, and
- LO/RF isolation.

3.2 Mixer Performance Criteria

Conversion loss is a measure of the efficiency of the mixer in providing frequency translation between the input RF signal and the output IF signal. Conversion loss sensitivity refers to the variation in conversion loss as a function of the deviation in LO drive level from its nominal value. Signal compression is a measure of the maximum RF input signal for which the mixer will provide linear operation. It is dependent on the LO drive level. Isolation is a measure of the circuit balance within the mixer which determines the amount of leakage among the mixer ports. It is also a function of the LO drive level [24].

In front end analysis, two key system performance characteristics are power levels and spurious rejection. The mixer performance criteria described above are critical in realizing these two front end specifications. Conversion loss, conversion loss sensitivity, and signal compression together dictate the power level and the power level constancy of the receiver front end. Conversion loss must be properly compensated by amplification. Conversion loss insensitivity to LO power level about the nominal point of operation is critical for power level constancy. Signal compression sets an upper limit on the RF input level to the mixer in order for the mixer to operate within its dynamic range. Spurious rejection is a function of the mixer's isolation characteristic, which is also dependent on the LO drive level.

To meet the requirements for the above two key performance characteristics, the LO drive level and the IF filter specifications must be chosen after careful consideration of the aforementioned mixer performance characteristics.

The test measurement setup for characterizing the MMIC double-balanced mixer is shown in Figure 3.1. A sweep oscillator was used for swept-frequency measurement over the 575-MHz RF input band. A directional bridge and detector are used to measure the mixer's conversion loss characteristics. A signal generator with amplifiers was used to produce the necessary LO drive levels. The test measurement setup modeled precisely the environment in which the mixer is intended to be used, e.g. no isolators are used at the RF, LO, and IF ports.

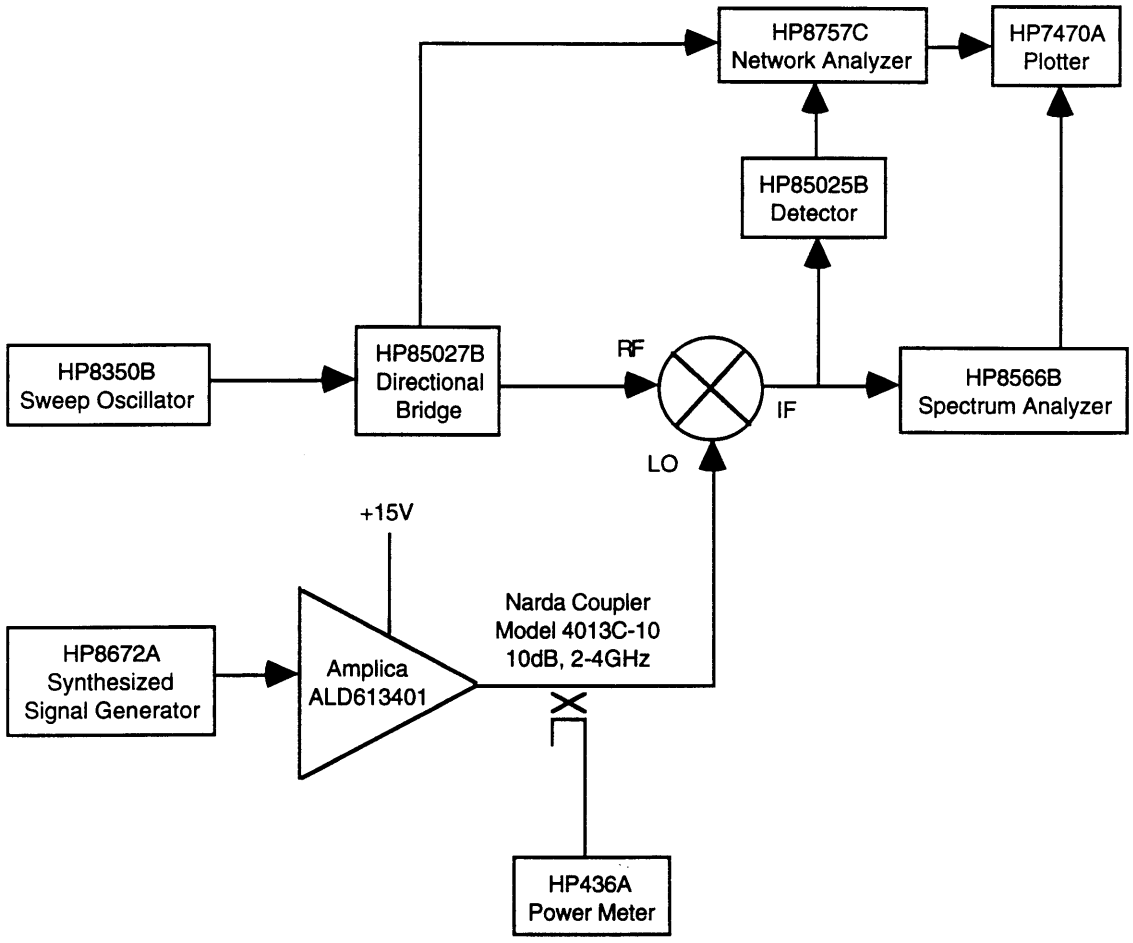


Figure 3.1 Test Measurement Setup for Mixer Characterization

3.3 Local Oscillator Power Analysis

The LO drive level must be selected to achieve best conversion loss insensitivity. Mixer conversion loss was plotted over a range of LO power levels. The results are summarized in Figure 3.2.

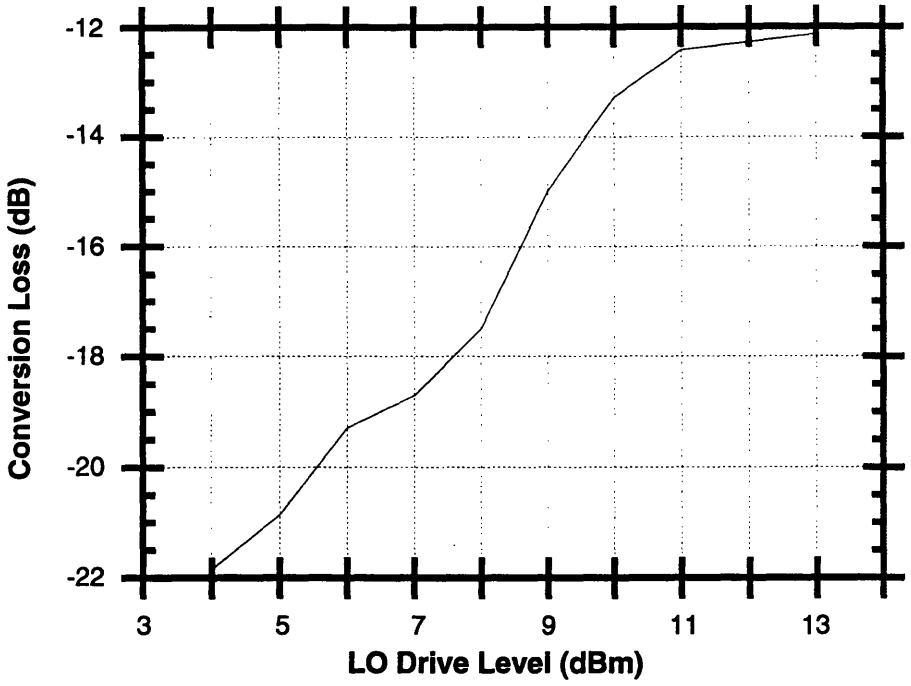


Figure 3.2 Mixer Conversion Loss vs. LO Power

Conversion loss is insensitive at the LO drive level of approximately +13dBm, shown by the flattening of the slope in Figure 3.2. Reasonable LO power variation about this nominal point does not cause significant changes in mixer output level. The LO will therefore be designed to operate with an output level of +13dBm.

3.4 IF Filtering Analysis

IF filtering selects the IF band from the output at the mixer IF port. The spurious signals outside of the band must be attenuated per receiver's spurious specifications. The spuri-

ous output of the mixer is shown in Figure 3.3. This measurement corresponds to the nominal LO drive level of +13dBm.

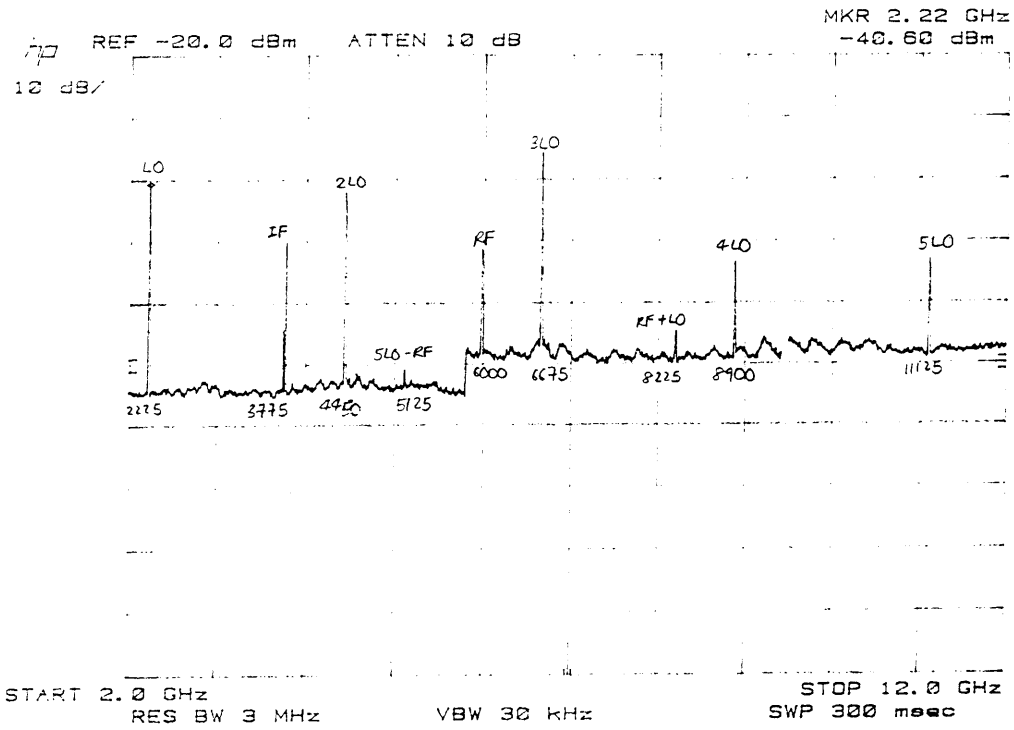


Figure 3.3 Mixer Spurious Output

The IF filtering requirements are determined based on the spurious outputs. Filter rejection is the amount of spurious attenuation which must occur for the spurious to be -60dBc. A *Microsoft Excel* worksheet was constructed to perform the calculations. The filter requirements derived from this analysis are summarized in Figure 3.4.

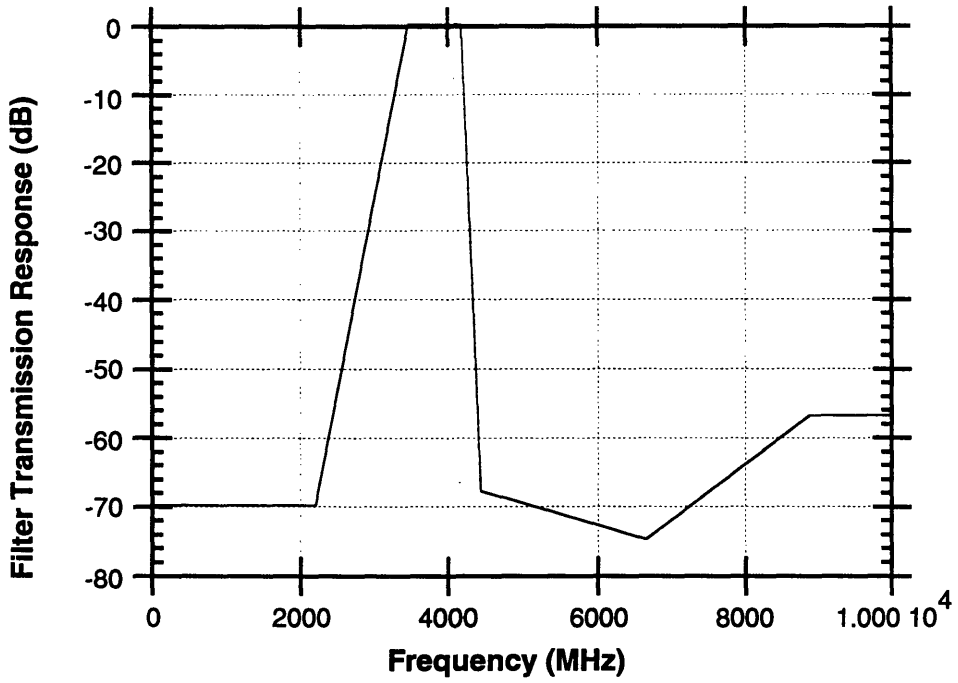


Figure 3.4 IF Filtering Requirements

The IF spurious analysis also determines the maximum bandwidth the receiver is capable of handling without violating spurious requirements. The bandwidth is constrained by the spurious levels inband. Based on the spurious analysis, it was determined that bandwidth up to 575MHz is achievable, ranging from 3.625GHz to 4.2GHz. With any significantly greater bandwidth, the conversion product 4LO-RF will fall inband, violating the receiver's inband spurious specification.

3.5 Alternate Mixer Implementations

Mixer performance presents a weak point in the system design. Poor isolation characteristics of the current mixer implementation makes IF filtering difficult. Its conversion loss characteristics require the use of a high-power local oscillator and high-gain devices throughout the receiver chain, thus increasing the system's power consumption as well as the chance for signal crosstalk.

Poor mixer performance may be explained by several factors. It is an experimental design utilizing a double-balanced topology. Isolation performance is critically dependent on the manufacturing tolerance of the input and output transformers. In addition, the lack of matching networks at the mixer's ports increases the amount of power with which the mixer must be driven in order to achieve acceptable performance. Current biasing is not utilized, in order to conserve power as well as to simplify the design. In the future, a current-biased design may be considered to optimize conversion loss.

An alternative mixer source is being investigated. The mixer under consideration has a triple-balanced topology. Its conversion loss performance and drive level requirements are superior to those of the current mixer implementation. The implications of a better mixer are multiple: the LO power level may be reduced, IF filtering may be much simpler, and a larger receiver bandwidth than 575MHz may be realizable.

Chapter 4
Design of Local Oscillator

4.1 Introduction

The C-band local oscillator provides the 2225MHz signal required by the receiver to translate the 6-GHz RF band to the 4-GHz IF band [18]. This chapter addresses the design issues associated with the local oscillator realization.

4.2 Local Oscillator Performance Criteria

A summary of the major performance specifications of the local oscillator is given in Table 4.1.

Parameter	Requirement	Units
Frequency (f_0)	2.225	GHz nom
Output power	+13	dBm nom
Output power stability	±1	dBm max
Short term stability		
5Hz to 100Hz	0.5	Hz rms max
100Hz to 12kHz	25	Hz rms max
Long term stability		
Temperature (-10/+55°C)	±1	ppm max
Per month	±0.2	ppm max
Over life	±2	ppm max
Phase noise spectral density		
Offset from carrier:		
10Hz	-50	dBc/Hz max
100Hz	-79	dBc/Hz max
1kHz	-98	dBc/Hz max
2kHz	-101	dBc/Hz max
100kHz	-111	dBc/Hz max
1MHz and above	-111	dBc/Hz max
Spurious output		
Within f_0±575MHz	-73	dBc max
Harmonics of f_0	-40	dBc max
Output return loss	16	dB min

Table 4.1 Receiver Performance Requirements [19]

In addition to the specifications listed in Table 4.1, the LO must be designed to realize savings in DC power consumption, size, and mass.

Among the performance parameters listed in Table 4.1, short and long term stability are key design parameters. Short term stability refers to frequency noise and fluctuations within random periods shorter than a few seconds. Long term stability describes slow changes of frequency due to factors such as aging. These two stability measures are illustrated in Figure 4.1.

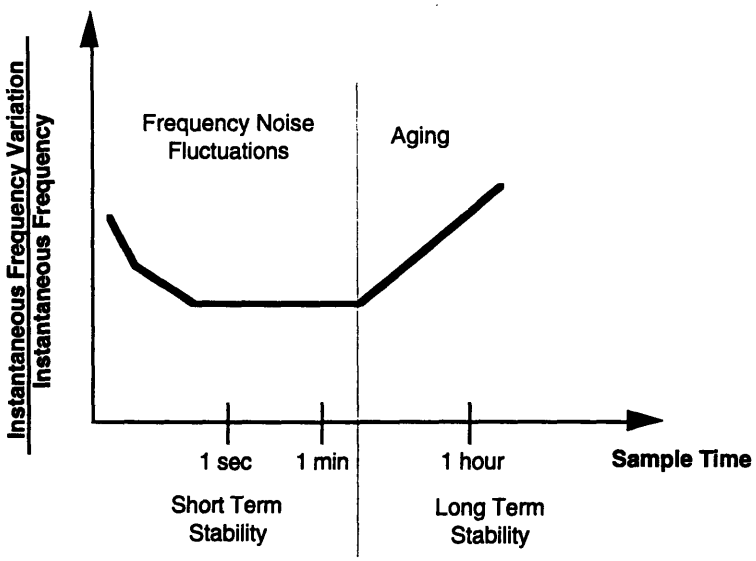


Figure 4.1 Frequency Stability [20]

Phase noise spectral density is another important performance specification. It may be defined as the ratio of the single sideband power of noise (P_{ssb}) in a 1-Hz bandwidth f_m Hz away from the carrier frequency to the total signal power (P_s) (Figure 4.2).

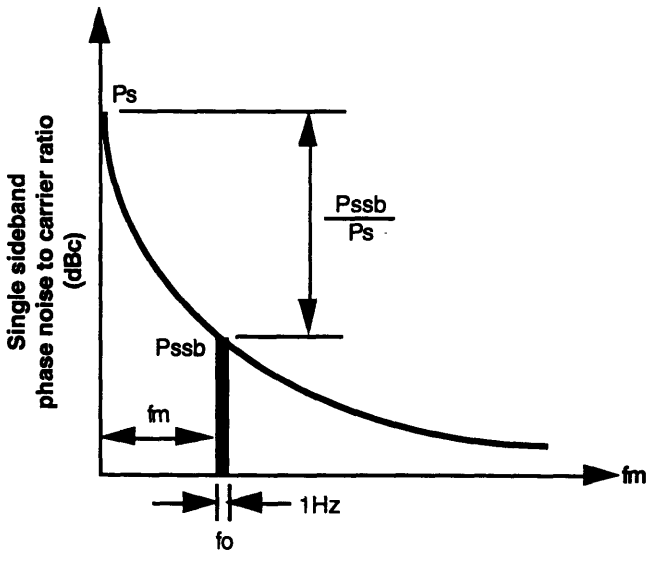


Figure 4.2 Phase Noise Definition [20]

The LO's spurious output specifications are chosen in compliance with the overall receiver spurious requirements. Spurious signals within $f_0 \pm 575$MHz of the LO output will appear at the IF output of the mixer in the inband frequencies (3.625GHz-4.2GHz). Therefore, any spurious in the $f_0 \pm 575$MHz band must be rejected to below -73dBc,* so that the down-conversion unit may meet its inband spurious specification of -70dBc with some margin. LO's harmonic rejection requirement of -40dBc, in conjunction with proper IF filtering, will enable the receiver front end to meet its out-of-band spurious specifications.

The output return loss specification ensures proper impedance match at the LO-mixer interface.

4.3 Design Alternatives

The LO frequency is generated from a reference oscillator with excellent short- and long-term stability. Several approaches exist for using a reference signal to generate a stable RF signal. Different methods yield different phase noise performance [20] and result in trade-offs between DC power consumption, design complexity, reliability, mass, and size. These methods are described in detail in the following sub-sections.

4.3.1 VCO-based Phase-Locked Loop

The phase-locked loop (PLL) approach uses a voltage-controlled oscillator (VCO) to generate the 2225MHz LO signal. The VCO is locked to a low-frequency stable crystal oscillator. Figure 4.3 illustrates the block diagram of a VCO-based single-loop PLL design.

* The receiver's inband spurious specification must be applied to both (f_0, f_0+700MHz) and (f_0-700MHz, f_0) bands, so that RF input ranging anywhere from 5.725GHz to 6.425GHz may have a spurious-free IF output ranging from 3.5GHz to 4.2GHz.

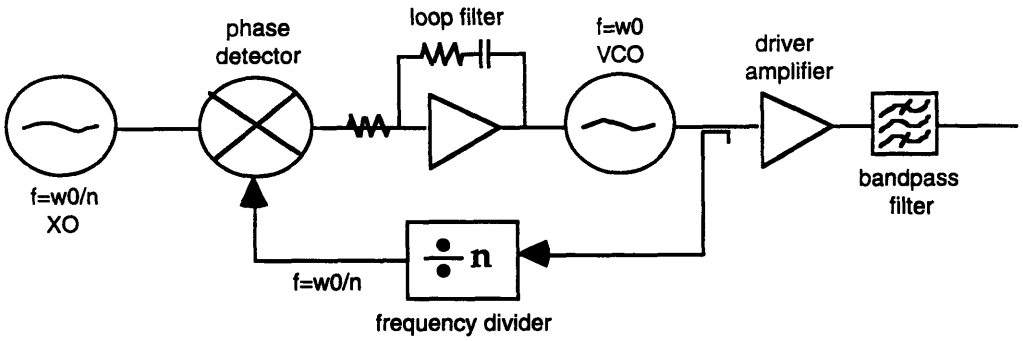


Figure 4.3 VCO-Based Phase-Locked Loop Approach

General Operation

The 2225MHz output signal is generated by the VCO. Output of the VCO corresponds to its nominal oscillation frequency modified by the tuning voltage, as described by the equation

$$\omega_2(t) = \omega_0 + K_0 u_f(t)$$

- ω_2 = angular frequency of the VCO output
- ω_0 = center angular frequency of VCO output
- K_0 = VCO gain in $s^{-1}V^{-1}$
- $u_f(t)$ = output signal of the phase detector loop filter.

The VCO output signal is coupled to a divide-by-n pre-scalar, which translates the frequency of the signal (ω_0) to match that of the reference signal $\left(\frac{\omega_0}{n}\right)$. The phase detector compares the phase of the VCO signal with the phase of the reference signal. Based on the comparison, it generates an output error signal which is approximately proportional (within a limited range) to the amount of phase error,

$$u_d(t) = K_d \theta_e$$

- $u_d(t)$ = output of phase detector
- K_d = gain of phase detector in $s^{-1}V^{-1}$
- θ_e = phase error between VCO output and reference oscillator (XO) signals.

$u_d(t)$ consists of an average DC component and a superimposed AC component. The AC component is undesirable for tuning the VCO frequency. It is rejected by the loop filter.

When the VCO deviates from its center frequency, a non-zero phase error θ_e is generated in the phase detector, which results in a non-zero output signal u_d. After some delay, the loop filter would also produce a finite signal u_f. This signal serves as the VCO tuning voltage and causes the VCO to change its operating frequency in such a way that the phase error finally vanishes. This feedback mechanism synchronizes the VCO output with the crystal oscillator reference signal in frequency as well as in phase [26]. The net result is a LO output signal at the frequency of the VCO but with the stability of the reference crystal.

Loop Filter Design

The loop filter removes the high-frequency components of the tuning signal to the VCO. Loop filtering requirements are typically met by a first-order, low-pass active or passive RC filter [26]. An active design not only enhances the performance of the loop but also allows the inclusion of a sweep generator in the operational amplifier to perform frequency search during start-up [51]. Because the loop filter affects the phase and gain of the PLL, design of the loop filter must take into consideration the best system phase and gain performance. Loop analysis entails examining the phase and gain of PLL components, then employing a Bode plot or similar tools to calculate the phase and gain characteristics of the phase-locked loop's open transfer function. However, control loop analysis does not account

for the many second-order effects in PLL operation. Phase and gain effects are difficult to predict for most devices. Therefore, analytical design of the loop filter is often accompanied by empirical design, where a PLL breadboard is constructed and the optimal loop filter parameters are determined empirically.

Phase Noise Calculation

Phase noise of a VCO-based PLL depends primarily on four factors: divide ratio of the loop and phase noise of the reference oscillator, phase noise of the VCO, and phase noise of the phase detector. Phase noise calculations are shown in Figure 4.4.

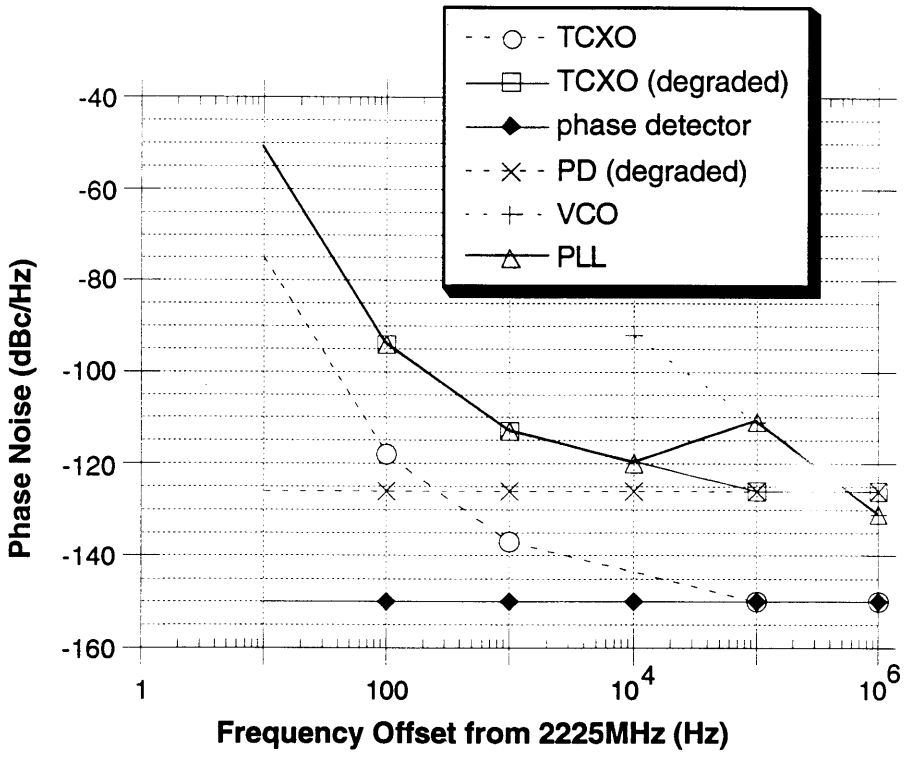


Figure 4.4 VCO-based PLL Phase Noise

Table 4.2 lists the components specifications assumed in the above phase noise calculation. A temperature compensated crystal oscillator (TCXO) is used as the baseline reference signal source. A 139.0625MHz reference frequency is assumed, with a corresponding loop divide ratio of sixteen $\left(=\frac{2225MHz}{139.0625MHz}\right)$.

PLL Component	Phase Noise (dBc/Hz)
TCXO [27]	
@ 10Hz	-75
@ 100Hz	-118
@ 1kHz	-137
@ 100kHz	-150
@ 1MHz	-150
Phase detector noise floor [34]	-150
VCO [35]	
@ 100kHz	-111
@ 1MHz	-131

Table 4.2 VCO-Based PLL Components Phase Noise Specifications

Phase noise degradation by the loop is calculated as follows:

$$20 \times \log \frac{f_0}{f_i} = 20 \times \log(16) = 24.08dB$$

where $\frac{f_0}{f_1}$ is the divide ratio of the loop. Inside the loop bandwidth, the PLL phase noise equals the reference oscillator phase noise degraded by the loop noise, with a noise floor set by the phase noise of the phase detector (which is also degraded by the loop noise). Outside the loop bandwidth, the PLL phase noise equals that of the VCO. The loop bandwidth is selected so that overall PLL phase noise is minimized [20].

Second-Order PLL Design

The PLL approach is useful for generating high frequencies where a large reference pre-scaling ratio would be required. Utilization of higher order PLL topologies will result in a lower overall phase noise compared to that of the multiplier chain approach. Figure 4.5 illustrates a second-order VCO-based PLL design.

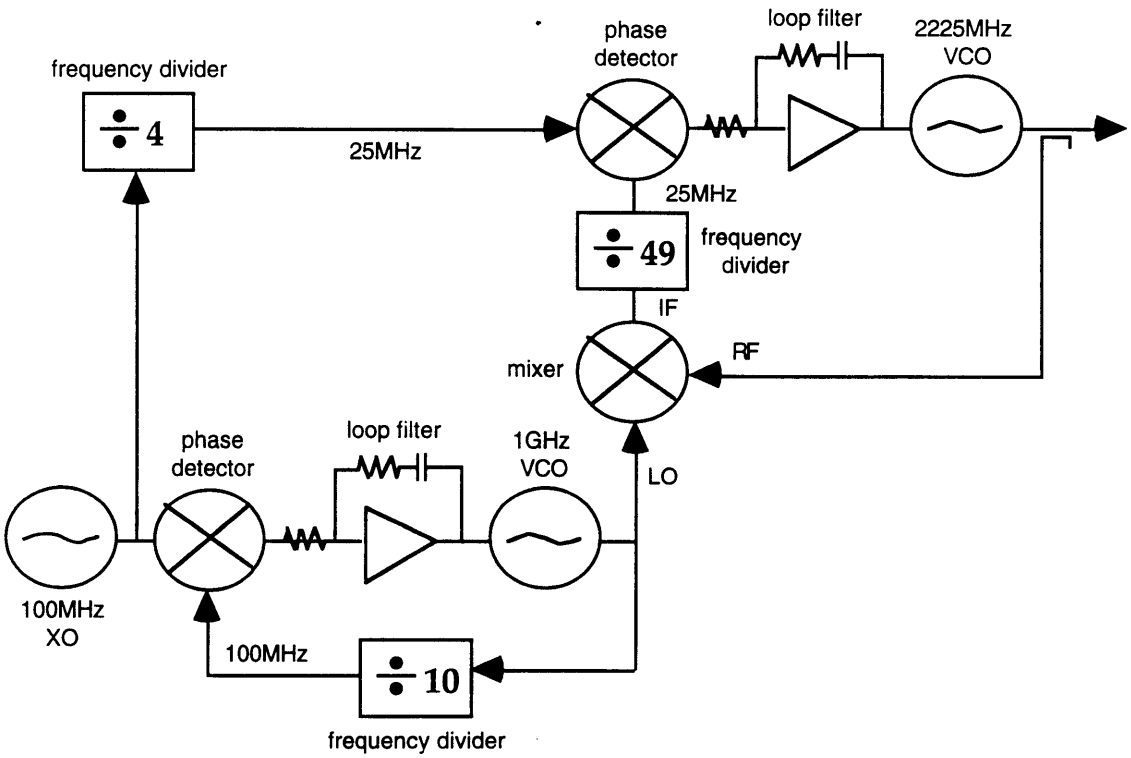


Figure 4.5 VCO-Based Phase-Locked Loop Approach (Second Order)

With the availability of low phase noise, high frequency reference oscillators, a synthesizer designer may reduce the pre-scaling ratio needed and thus attain acceptable phase noise with the single-loop PLL topology. In such cases, the additional complexity of the dual-loop approach does not warrant the phase noise margin it provides. Moreover, multiple-loop designs require additional hardware in terms of VCOs, loop filters, phase detectors, dividers, and mixers, thus significantly increasing overall circuit area, complexity, and cost.

The stringent specifications for the 2225MHz LO implementation push the limits of the VCO-based PLL approach. In order to achieve optimal phase noise, the PLL must be designed with a wide loop bandwidth (20-50kHz). However, wide loop bandwidth compromises loop stability of the PLL. Therefore, the PLL design may not apply well to this frequency synthesis application.

4.3.2 DRO-Based Phase-Locked Loop

The dielectric resonator oscillator (DRO) phase-locked loop uses the high Q of dielectric resonator oscillator to obtain a low phase noise signal at 2225MHz. It is identical in design to the VCO-based PLL except for the substitution of the VCO with the DRO, as shown in Figure 4.6. The result is much better phase noise outside the loop bandwidth. Consequently, the loop bandwidth may be smaller than that of a VCO-based PLL, making for an easier circuit design.

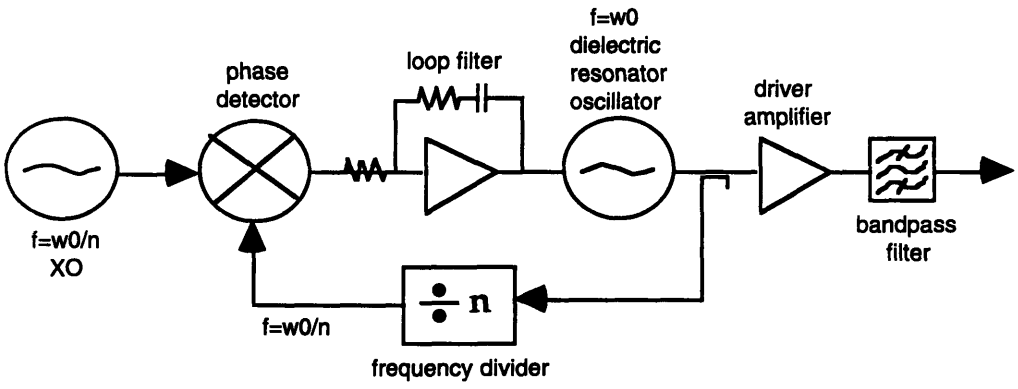


Figure 4.6 DRO-Based Phase-Locked Loop Approach

Phase Noise Calculation

Figure 4.7 illustrates the projected phase noise performance calculation for the DRO-based PLL. This figure shows that DRO-based PLL offers better phase noise performance than VCO-based PLL.

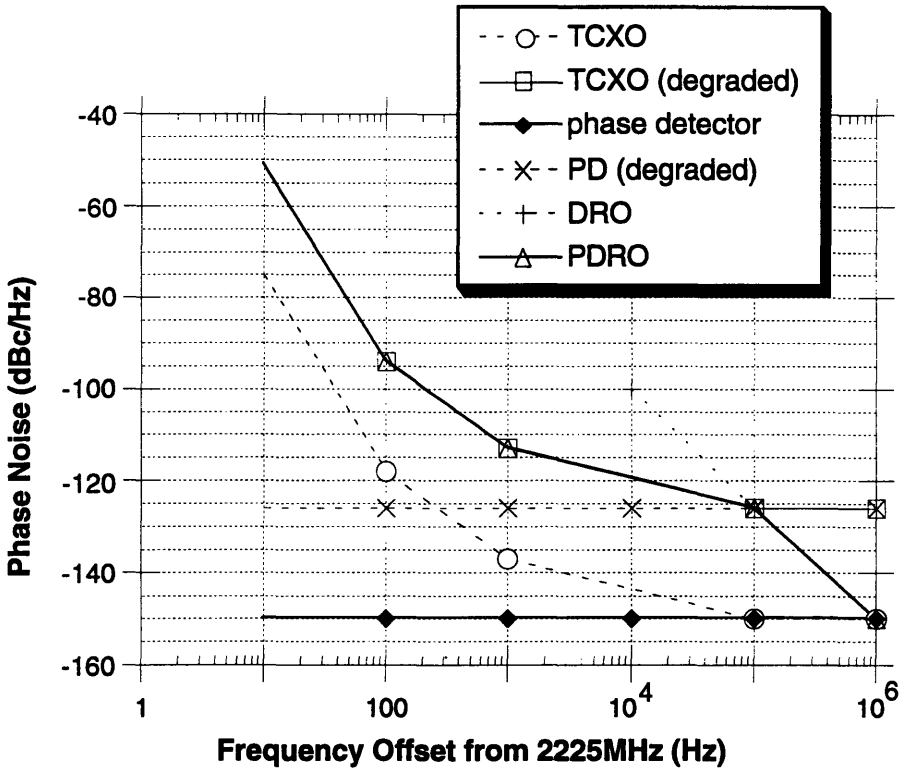


Figure 4.7 DRO-BASED PLL Phase Noise

The methodology for calculating DRO-based PLL phase noise is identical to that for VCO-based PLL phase noise, except the lower DRO noise floor is used in place of the VCO noise floor (for outside of the loop bandwidth). Optimal loop bandwidth remains at 100kHz.

Summary

	VCO	DRO
Phase noise	-97dBc/Hz @ 50kHz -105dBc/Hz @ 100kHz	-100dBc/Hz @ 10kHz -125dBc/Hz @ 100kHz
Bias supply	50mA @ +15VDC	100mA @ +15VDC
Size	0.5" x 0.2" x 0.5"	2.9" x 2.0" x 0.9"
Weight	1.7g	894g

Table 4.3 Comparison between VCO and DRO [36]

Table 4.3 compares the two different implementations of the free-running oscillator. The DRO consumes twice as much power, occupies much larger volume, and has significant more weight as compared to the VCO. In addition, temperature stability of the dielectric material is a major risk factor. The marginal phase noise advantage of the DRO-based PLL approach does not warrant such severe penalties. The DRO-based PLL design was not pursued in favor of other LO implementation approaches.

4.3.3 Multiplier Chain

The multiplier chain generates the 2225MHz output signal by multiplying up the frequency of a low-noise, high-stability crystal oscillator using multiplier stages. A block diagram is shown in Figure 4.8.

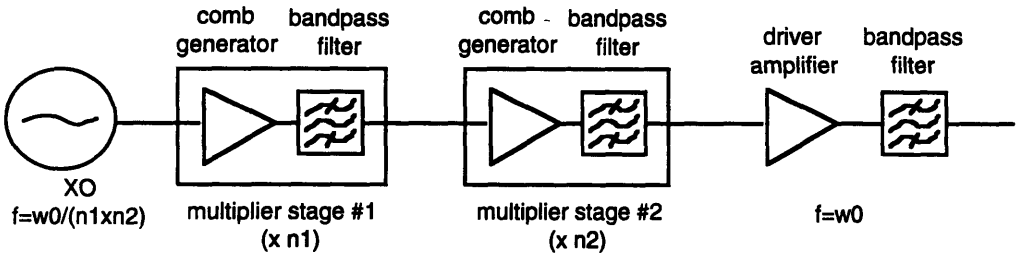


Figure 4.8 Multiplier Chain Approach

General Operation

The multiplier chain employs a series of multiplier stages to generate the desired LO output frequency from the much lower reference oscillator (XO) frequency. Each multiplier stage consists of a comb generator and a bandpass filter. The comb generator generates harmonics of its input signals at its output. The bandpass filter then selects the appropriate harmonic to realize the desired frequency multiple. Comb generation may be implemented with a variety of devices, including step-recovery diodes and amplifiers operated in the non-linear region.

The multiplier chain approach is the least desirable for frequency generation when a large multiplication factor is required. Several multiplier stages would be needed in such cases. Each additional multiplier stage adds to the overall insertion loss and DC power consumption. However, with the recent availability of low-noise, high-frequency crystal oscillators, the number of multiplier stages can be significantly reduced.

Phase Noise Calculation

Phase noise of the multiplier chain is the phase noise of the reference oscillator degraded by the frequency multiplication factor [20]. The phase noise calculations are shown in Figure 4.9. In the multiplier chain, the crystal oscillator presents the only significant contribution to overall phase noise. Unlike the phase-locked approaches, no other noise components in the multiplier chain contribute in a significant way. The amplifiers' low noise figures should be lower than the most stringent phase noise requirement of the LO signal (-150dBc/Hz at >1MHz offset) [20].

TCXO is used as the baseline reference signal source. A 139.0625MHz reference frequency is assumed, with a corresponding multiply ratio of sixteen. The TCXO phase noise specifications are the same as those used for the VCO-based PLL and DRO-based PLL phase

noise calculations (refer to Table 4.2). A phase noise margin of 5dBc/Hz is added to phase noise degradation, to account for secondary phase noise contributions by components other than the TCXO.

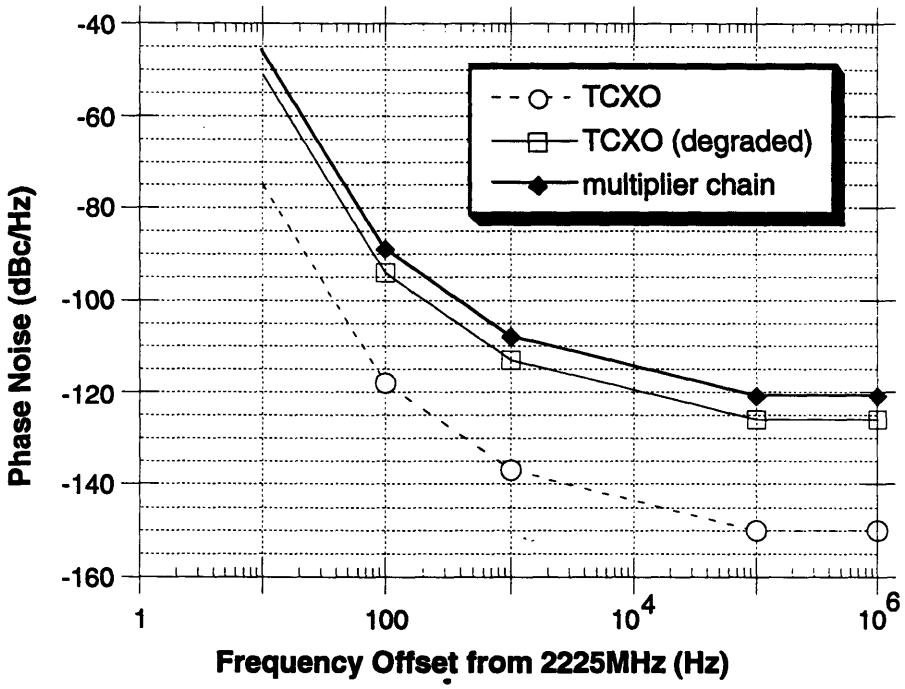


Figure 4.9 Multiplier Chain Phase Noise

The amount of phase noise degradation is as follows:

$$20 \times \log \frac{f_0}{f_i} = 20 \times \log(16) = 24.08dB$$

where $\frac{f_0}{f_1}$ is the total multiply ratio. The amount of phase noise degradation due to the multiplication process may be attenuated by several means. Negative feedback at low frequency may be designed into the amplifiers. Some negative feedback has also been introduced at RF frequency in the past to stabilize the transconductance [20].

4.3.4 Selection of Approach

The topology to be used to implement the C-band receiver LO was chosen based on phase noise characteristics, spurious performance, DC power consumption, size, reliability, and engineering risk. The following considerations were used:

Phase Noise

All three approaches are capable of meeting phase noise specifications of the LO. In general, the multiplier chain approach has the worst phase noise, followed by VCO-based PLL, and DRO-based PLL. PLL designs typically have better phase noise characteristics than the multiplier chain because of the availability of a multiple-loop configuration for high frequency synthesis. In higher-order PLL topologies, multiple phase detectors and adjustment capabilities allow the overall phase noise to be less than that of a simple degradation of the crystal oscillator phase noise by the pre-scaling ratio, as in the case of the multiplier chain. However, in this C-band receiver LO application, availability of a low-noise, high-frequency crystal oscillator [27] and small multiplication factor obviate the need for multiple loops. As illustrated in Figure 4.10, single-loop versions of the VCO-based PLL and DRO-based PLL present only marginal phase noise advantage over the multiplier chain. In addition, the phase noise performance of the multiplier chain approach is less sensitive to power supply noise.

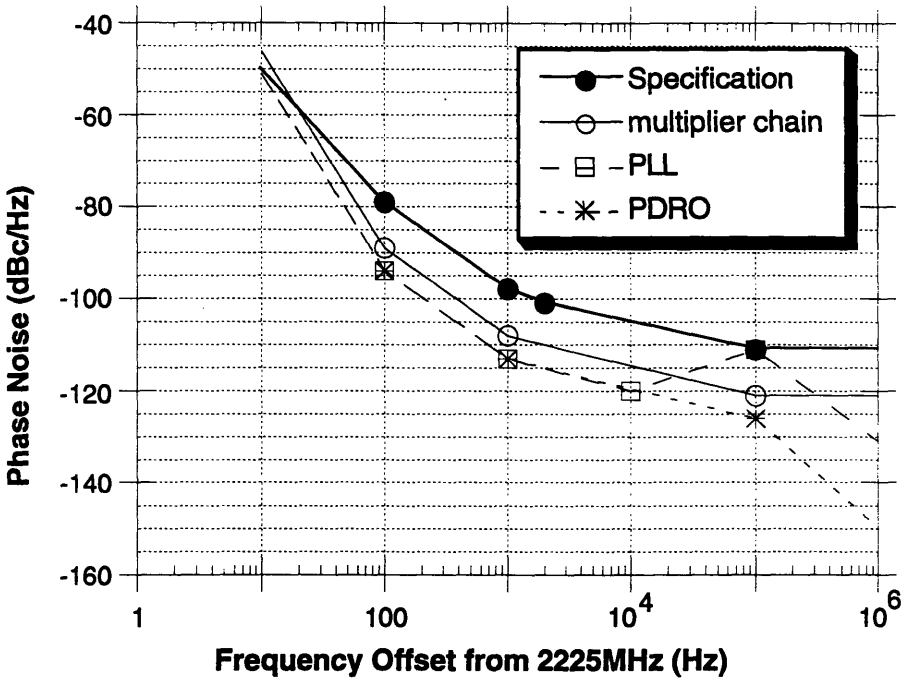


Figure 4.10 Phase Noise Comparisons

Spurious Performance

The PLL designs will have greater difficulty meeting the spurious specifications of the LO compared to the multiplier chain approach. In the PLL, inband spurious due to power supply noise are difficult to remove. In the multiplier chain, out-of-band harmonics are generated but may be removed using filters.

DC Power Consumption

When compared to the PLL approaches, the multiplier chain approach has consumed greater DC power in the past. However, with the availability of low-power comb generators [8] and low-noise, high-frequency reference signal sources [27], the number of multiplier

stages needed is reduced. Therefore, power consumption is significantly improved for the multiplier approach in this C-band application.

Size

The DRO-based PLL approach will yield a significantly larger design than the VCO-based PLL or the multiplier chain approach, due to its use of the relatively bulky dielectric resonator oscillator. The multiplier chain will be equivalent in size to the VCO-based PLL, or perhaps smaller depending on the implementation approaches for the filters in the multiplier stage.

Reliability

The multiplier chain contains less circuitry than either phase-locked implementation, making it an inherently more reliable design. In addition, loop stability and frequency stability must be guaranteed for flight components, also taking into account the effects of temperature and aging. The feedback paths in the PLL designs render them more susceptible to loop stability problems than the multiplier chain. The multiplier chain has better loop stability, since the comb generation devices are unconditionally stable by design under the relevant operating conditions.

The VCO-based PLL and multiplier chain designs exhibit good frequency stability characteristics based on reference oscillator design. The DRO-based PLL design, on the other hand, depends on the resonator materials for long-term stability.

Engineering Risk

In addition, the engineering risk associated with the multiplier chain was considered to be relatively low. Availability of space-qualified low-noise VCOs in the 2-GHz range and

low-noise pre-scalars is an area of concern. The components required by the multiplier chain design are all readily available [27],[28],[29].

Choice of Approach

Table 4.4 summarizes the comparison among the various LO designs based on the issues described above. The multiplier chain design is superior to the other LO implementation approaches on every significant criterion, including power consumption and reliability. Phase noise performance is the only area where all designs are comparable to each other. Therefore, the multiplier chain approach is chosen for implementation of the C-band receiver LO.

	Multiplier Chain	VCO-based PLL (single loop)	VCO-based PLL (dual loop)	Phase-Locked DRO
phase noise	see Figure 4.10			
spurious (bias sensitivity)	low	medium	medium	medium
DC power consumption*	+5V @ 305mA	+5V @ 575mA -5V @ 10mA	+5V @ 760mA -5V @ 20mA	+5V @ 385mA
size	small	small	medium	large
reliability	high	medium	low	low
feedback path	no	yes	yes	yes
simplicity	simple	complex	very complex	complex
engineering risk	low	moderate	high	high

Table 4.4 Comparison of LO Designs

4.4 Multiplier Chain Block Diagram Design

The multiplier chain is based on a reference signal provided by a low phase-noise, high-stability crystal oscillator. The signal is multiplied up in frequency by a series of multi-

* DC power consumption for all four LO designs is calculated assuming the use of an oven controlled crystal oscillator.

plier stages. Each multiplier stage consists of a comb generator and a bandpass filter. The comb generator outputs a harmonic spectrum composed of signals at frequency multiples of its input. The bandpass filter then selects the harmonic at the desired frequency multiple. After the carrier signal is multiplied to the desired RF frequency (2225MHz), a driver amplifier provides the final amplification. A bandpass filter at the output of the driver amplifier rejects any harmonics. The general block diagram for the multiplier chain design is shown in Figure 4.11.

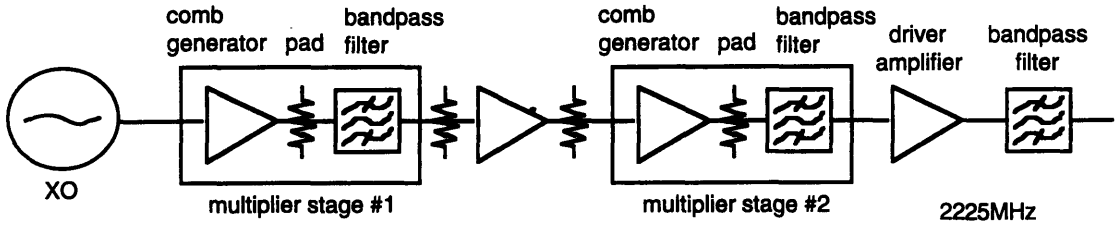


Figure 4.11 Multiplier Chain Block Diagram

4.4.1 Frequency Multiplication

The multiplication scheme uses the availability of high-frequency, low-noise crystal oscillators and custom comb generation to make the filtering requirements less stringent. Once chosen, the multiplication scheme determines the frequency of the crystal oscillator, the number of multiplier stages, and the multiplication factors.

Low phase-noise crystal oscillators are currently available for frequencies up to 155MHz [27]. The highest possible low-noise frequency source is chosen in order to minimize the multiply ratio. However, frequency of the signal source is constrained to finite precision. Table 4.5 shows three multiplication ratios which utilize finite-precision frequency sources to multiply up to 2225MHz. The multiplication ratios considered for further analysis are 16, 20, and 21.

Multiply Ratio	Reference Frequency Required
14	158.9285714...MHz
15	148.3333333...MHz
16	139.0625MHz
17	130.8823529...MHz
18	123.6111111...MHz
19	117.1052632...MHz
20	111.25MHz
21	105.952381MHz
22	101.1363636...MHz

Table 4.5 Selection of Multiply Ratio

Variable comb generations entails choosing multiplication factors where the harmonics are strong relative to their neighboring signals. An example is using a multiply ratio with odd multiplication factors. Odd harmonics in comb generation are generally stronger than their even counterparts, because they multiply off the fundamental signal instead of the weaker second harmonic.

A complementary method for reducing or simplifying the filtering requirements is to implement the higher multiplication factors first in the multiplier chain. Realizing filters with the same absolute sharpness is easier at lower frequencies.

Among the three possible multiplication ratios of 16, 20, and 21, the multiplication ratio of 20 was first considered. It has two possible sets of multiplication factors: 10 x 2 and 5 x 4. Bench measurements of comb generators show that these multiplication factors do not produce strong enough higher harmonics for the multiplier chain. Therefore, this option was eliminated.

The multiplication ratio of 21 was also considered. The multiplication factors will be 7 x 3.* Figure 4.12 shows the block diagram of a multiplier chain based on the 7 x 3 scheme.

* A single-stage x 21 multiplier is not considered due to the potential isolation problem stemming from steep filtering.

This scheme takes advantage of the strong odd harmonics in the comb to make the filtering requirements more lenient than with the 10 x 2 or 5 x 4 scheme.

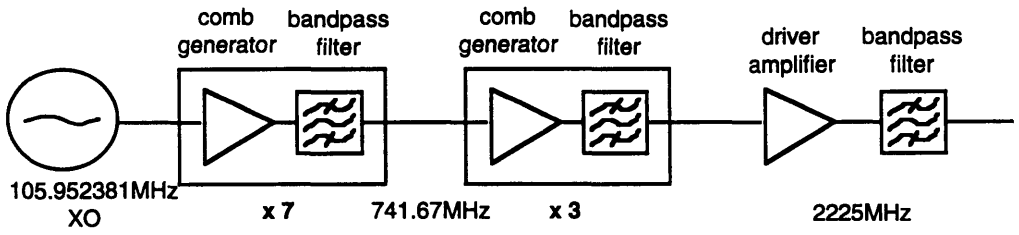


Figure 4.12 Multiplier Chain with 7 x 3 Scheme

Preliminary filter requirements were drafted using measurements of harmonic spectrums generated by the comb generators. The filter requirements depict the amount of rejection necessary on the extraneous harmonics in order for the LO chain to meet its spurious requirements.

Finally, the multiply ratio of 16 was considered. The two possible sets of multiplication factors are 4 x 4 and 8 x 2. Neither set takes advantage of the strength of odd harmonics. The fourth harmonic in the comb generation spectrum was not strong relative to other adjoining harmonics. The second set, on the other hand, has an eighth harmonic that stands at least 10dB above its two neighboring harmonic signals, as demonstrated by preliminary bench measurements. In conjunction with the typically strong second harmonic, this set of multiplication factors presents an attractive multiply scheme. Figure 4.13 shows a block diagram of the multiplier chain employing the 8 x 2 scheme. Based on the bench measurements of comb generators, preliminary filter requirements were drafted. The required filter specifications for the 7 x 3 and the 8 x 2 scheme are shown in Figure 4.14.

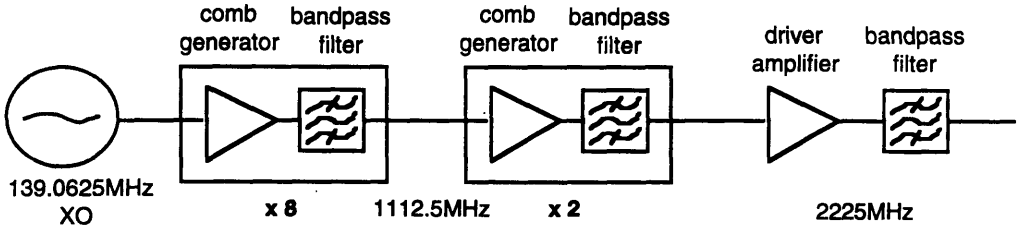


Figure 4.13 Multiplier Chain with 8 x 2 Scheme

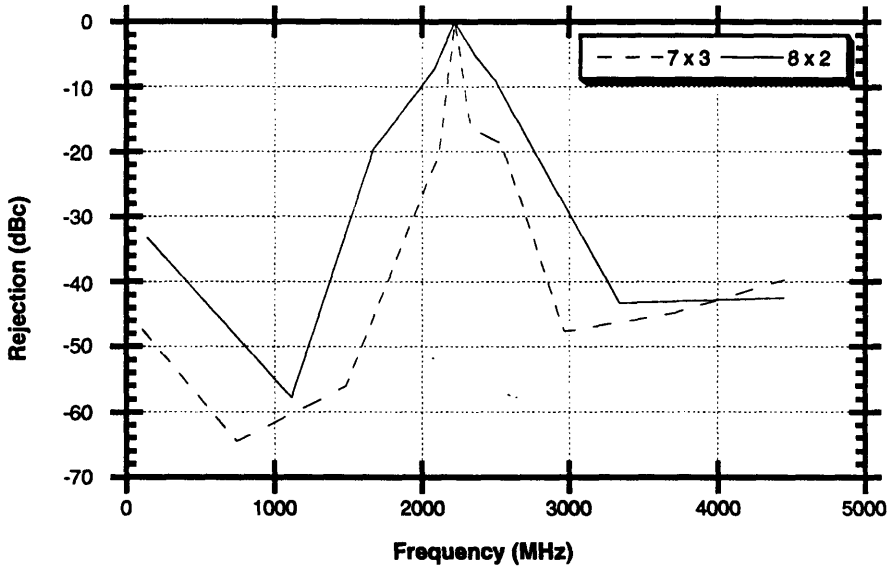


Figure 4.14 Comparison of Filtering Requirements

Figure 4.14 shows that the 8 x 2 scheme presents less stringent filtering requirements than does the 7 x 3 scheme. Moreover, the 7 x 3 scheme will result in greater phase noise degradation due to its larger multiply ratio of 21. Moreover, the crystal oscillator associated with the multiply ratio of 21 will not achieve significantly better phase noise than the crystal oscillator associated with the multiply ratio of 16. Therefore, 8 x 2 was chosen as the multiply scheme for the 2225MHz LO implementation. The reference signal frequency is accordingly fixed at $\frac{2225MHz}{16} = 139.0625MHz$.

4.4.2 Internal Interfacing

The major components in the multiplier chain must be carefully interfaced to avoid problems in mismatch or DC feedthrough.

Attenuators (or pads) are commonly placed between components to reduce mismatch problems. They improve return loss by introducing loss at the interface of two mismatched impedances. In the LO multiplier chain, attenuators are placed strategically at either side of the filters, where the greatest mismatch is likely to occur.

Attenuators are commonly implemented with one of three forms of resistance networks: the *T* section, the π section, and the bridged-*T* section. The three structures are equivalent theoretically but differ in residual and parasitic values in implementation. For low pad values, the π section is the optimal choice. It employs more realistic resistor values. Figure 4.15 illustrates the symmetrical π configuration. Blocking capacitors are placed on either side of the attenuators.

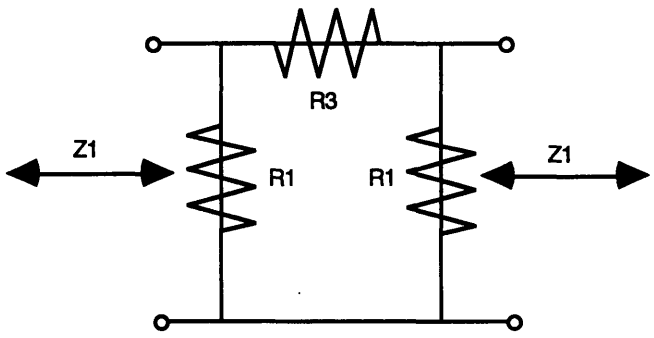


Figure 4.15 Symmetrical π Configuration Attenuator

Parameters of R1 = 17.85Ω, R3 = 3.04Ω will realize 5-dB attenuators in a 50-Ω system.

4.5 Selection of Signal Source

The reference crystal oscillator (XO) must operate at 139.0625MHz and with low phase-noise. The exact phase-noise requirements for the XO are shown in Figure 4.16. They are calculated based on the LO phase noise specifications, taking into account phase noise degradation by multiplication. The multiplier chain approach with a multiply scheme of 8 x 2 is assumed.

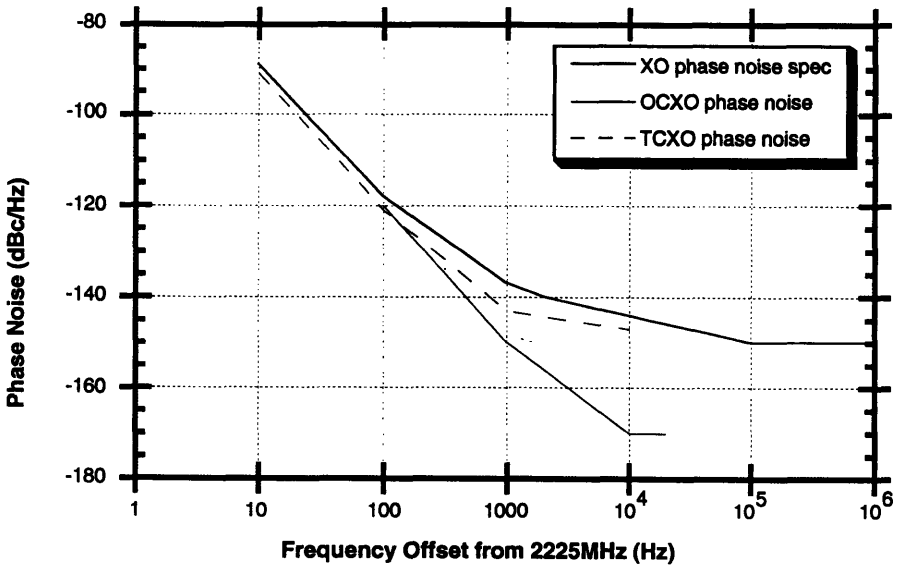


Figure 4.16 Phase Noise Requirements for the Crystal Oscillator

There are four types of crystal oscillators:

- non-compensated crystal oscillator (XO),
- oven controlled crystal oscillator (OCXO),

- voltage controlled crystal oscillator (VCXO),
- temperature compensated crystal oscillator (TCXO).

The four oscillator technologies differ in frequency stability, temperature stability, phase noise, power consumption, and size. The non-compensated XO and VCXO do not meet the LO stability requirements. OCXO is generally the best choice for high-stability and low-phase noise performance, at the expense of greater power consumption. TCXO requires minimal current, although it achieves slightly worse phase noise and stability than OCXO [33]. Table 4.6 compares the specifications of the oven controlled and temperature compensated crystal oscillators. Figure 4.16 compares the phase noise performance of these two technologies against the projected phase noise requirements for the LO reference oscillator.

	OCXO	**TCXO**
Phase noise		
@ 100Hz	-119dBc/Hz	-118dBc/Hz
@ 1kHz	-149dBc/Hz	-137dBc/Hz
@ 10kHz	-166dBc/Hz	-150dBc/Hz
@ 100kHz	< -170dBc/Hz	< -150dBc/Hz
Temp. stability (-10/55°C)	±0.2 ppm	±1 ppm
Size	2" x 3" x 1"	1" x 1.4" x 0.4"
Power supply bias	+12V	+5V
Power consumption	1.32W	0.015W
Space qualification	yes	yes

Table 4.6 Comparison of XO Technologies [27],[33]

It is quite apparent that both oscillator implementations meet the requirements, although the TCXO has slightly worse phase noise performance. Both technologies also meet the LO specification on stability, though once again the TCXO version is more marginal on this requirement. However, the TCXO offers significant size and power consumption advantages

and also works on +5 bias supply. Therefore, the temperature compensated XO is selected as the baseline signal source for the LO implementation.

4.6 Implementation of Comb Generators

4.6.1 Selection of Comb Generation Approach

Comb generators are typically implemented with either step recovery diodes or amplifiers. GaAs multiplier varactors are sometimes utilized, though they are more appropriate for medium power applications as frequency doublers or triplers [39].

Step Recovery Diode

The step recovery diode is analogous to a charge-controlled switch [38]. Positive voltage on the input drives the diode to forward conductance. When in forward bias, the step recovery diode stores charge. In this state, it appears as a low-impedance current source. Once the input signal reverses polarity, the diode becomes reversed-biased and charge is extracted. When all of the stored charge has been depleted, the diode has a higher impedance. It then ceases to conduct current. This switching action generates a train of voltage pulses [39], which convert to a series of impulses in the frequency domain at multiples of the fundamental exciting frequency. The step recovery diodes have a high conversion efficiency to render them part of a practical scheme for multiplying up from a low-frequency oscillator to obtain a higher frequency signal [38].

Amplifier

Amplifiers operated in the non-linear domain may also be used to implement comb generators. The output spectrum of any saturated amplifier will include significant harmonically related components (2f, 3f, etc.) as well as the fundamental signal. In saturation, the

amplifier's output RF waveform is clipped. Fourier expansion of the clipped waveform shows the generation of harmonic components of the fundamental signal. Harmonic output is maximized when the RF input level corresponds to the rated output power of the amplifier. Harmonic output may be further improved by adjusting the bias point (device current) and the phasing of the output filter. For maximal signal strength, the desired multiplied output signals should occur at frequencies within the normal 3-dB passband of the amplifier [37].

Step recovery diodes consume more DC power than do GaAs FET amplifiers. They typically require a RF input drive level of +10dBm or more. Moreover, they are efficient as multipliers with ratios of only two to four [39], due to the amount of harmonic spectrum drop-off per octave in frequency. Because of this constraint, they are not well suited for application to the C-band receiver LO, which requires 8 as one of the multiplication factors. On the other hand, amplifiers may often be tuned to produce a particularly strong harmonic at the desired multiple, even for high-order harmonics. For the above reasons, the amplifiers are more appropriate for this multiplier application.

GaAs FET Amplifier Requirements

The choice of amplifier depends on several factors. MMIC implementations will exhibit relatively more reliable, stable, and reproducible performance [2]. High cutoff frequency and low 1-dB compression point facilitate extended comb generation, for the realization of high multiplication factors [37]. Low noise figure, in order to lower overall phase noise, is critical as well. The Hewlett Packard INA-03 geometry was selected for use as a comb generator.

ISOSAT-based low noise amplifier (INA) is a silicon bipolar MMIC device built with the isolated self aligned transistor process (ISOSAT™). INA-03 offers the following performance parameters [37]:

- High frequency: 2.8GHz f_{3dB}
- Low power: +1dBm P_{1dB}
- High efficiency bias: 12mA.
- Low noise: 2.5dB NF
- High gain: 25dB

4.6.2 Operating Point Selection

Operating point selection consists of choosing the amplifier bias point and drive level. The INA-03 amplifier may be operated at various bias points and drive levels to achieve different performance results. The four primary issues in the selection of operating point are: reliability of operation, sensitivity to bias conditions, harmonic output, and power consumption.

Amplifier Bias Points and Drive Levels

Reliability of operation constrains the range of bias points to a minimum and a maximum. Below the lowest recommended operating threshold, the MMIC is partially turned off, and performance becomes unpredictable. Stability problems can result when the device is operated over a temperature range. The maximum operating threshold is thermally limited. Therefore, it is largely dependent on the thermal conductivity properties of the MMIC packaging [25]. For the INA, bias current should not exceed 16mA. Reliability of operation also constrains the range of RF input drive levels. The INAs may handle RF input powers up to its 1-dB compression point (+1dBm) without reliability concerns. Past its P_{1dB}, junction temperatures may begin to pose reliability problems.

Insensitivity to reasonable operating point variations is another important criteria in choosing the nominal bias point. Harmonic spectrum characteristics should be insensitive to normal deviations in bias conditions and drive levels. The supply from the electronic power conditioner (EPC) is projected to vary by a maximum of ten percent. The ideal bias and drive point will be one about which the harmonic output remains fairly constant over EPC supply

and P_{in} variation, in terms of both the absolute carrier power level and the relative harmonic levels of the spectrum. An inappropriate LO output level will compromise the conversion loss and other performance characteristics of the mixer. Relative harmonic levels sensitive to operating point variation may cause violation of the spurious requirements on the LO output. For example, the harmonic at the desired frequency multiple may lose its margin over its neighbors at a slightly different operating point. It is also good practice to operate the devices as far from the +5V as possible, in order to minimize the effect of variation in the 5-volt supply experienced by the amplifiers.

Bias point should be selected to optimize the harmonic output, in order to facilitate filtering. The LO block diagram design specifies a multiply scheme of 8 x 2. Therefore, the amplifier in the first multiplier stage should be biased such that the eighth harmonic stands out in relation to its neighboring harmonics, whereas the amplifier in the second multiplier stage should be biased such that the second harmonic stands out. The bias point should also be chosen such that the amplifiers demonstrate good return loss at the carrier frequency and, for the linear amplification application, good gain.

Power consumption is another concern in the selection of bias point. Because the +5V supply is fixed, only the current usage may be optimized. Lower current levels mean less power consumed by the dropping resistors.

Selection of Bias Points and Drive Levels

Based on the above four criteria, bench measurements were performed in order to select the optimal operating point. The test setup is shown in Figure 4.17. A 3-dB coupler is used to monitor the input power. The INA-03 is biased at the output with a bias-TEE.

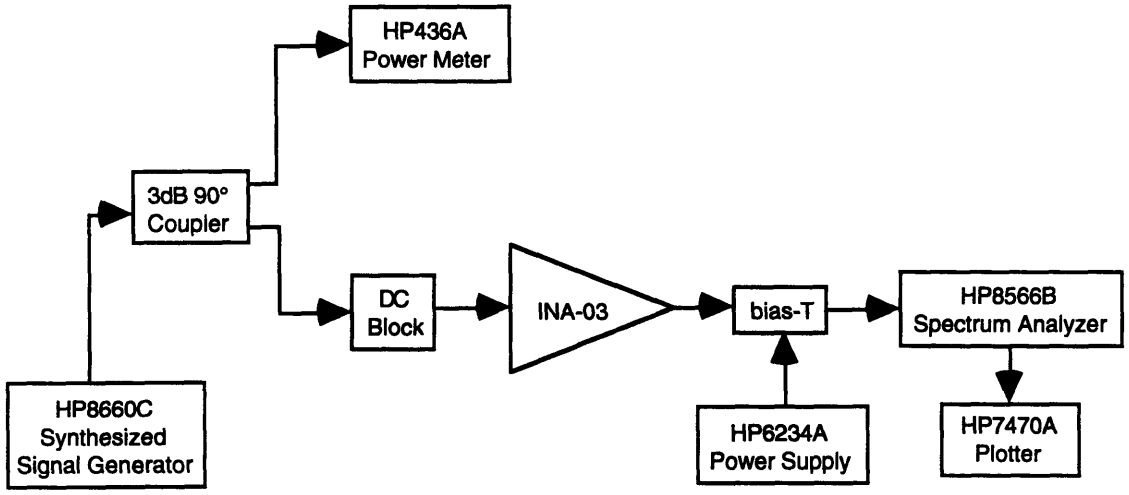


Figure 4.17 Test Setup for Bias Point Selection

The power supply voltage and the signal generator output power were varied and the desired harmonic was measured in the INA's comb output. The parametric study led to the following determinations. The amplifier should be operated at +2.9V with 10mA current. The amplifier should be driven with a RF input of -9.6dBm. The second-stage amplifier should be driven with an input level of -33dBm for linear operation. The second-stage comb-generation amplifier should be operated with -8.0dBm input power. The bias currents and the input drive levels were well below the threshold of reliability concern. The output combs of both stages were consistent for normal variations in supply voltages, currents, and input powers. Comb-line amplifier performance remained constant for up to ten percent variation in supply current. Input power of the first-stage INA may vary by ±4dBm from nominal without affecting comb response. Input power of the second-stage INAs may vary by ±5dBm. These ranges are well above the expected variations in the TCXO's normal operation. Figures 4.18 and 4.19 show the resulting harmonic spectrums of the two comb generation stages as plotted on a spectrum analyzer.*

* A single-stage x 16 multiplier is not considered due to the additional 13dB of amplification it would require as a result of its lack of margin over neighboring harmonics.

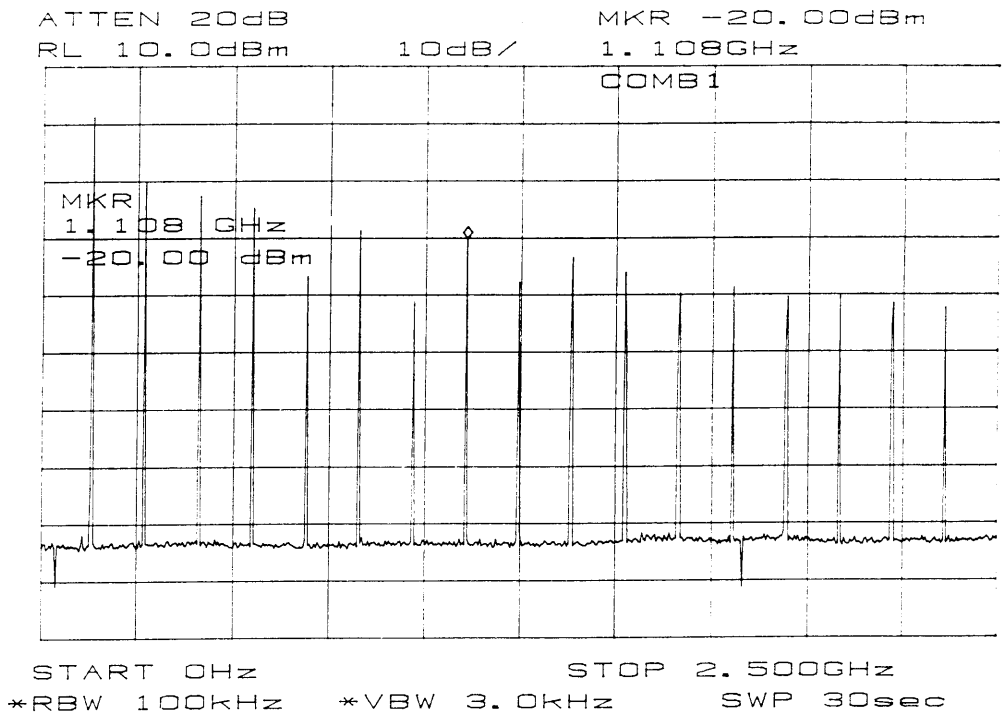


Figure 4.18 Harmonic Output of First-Stage Amplifier (x 8)

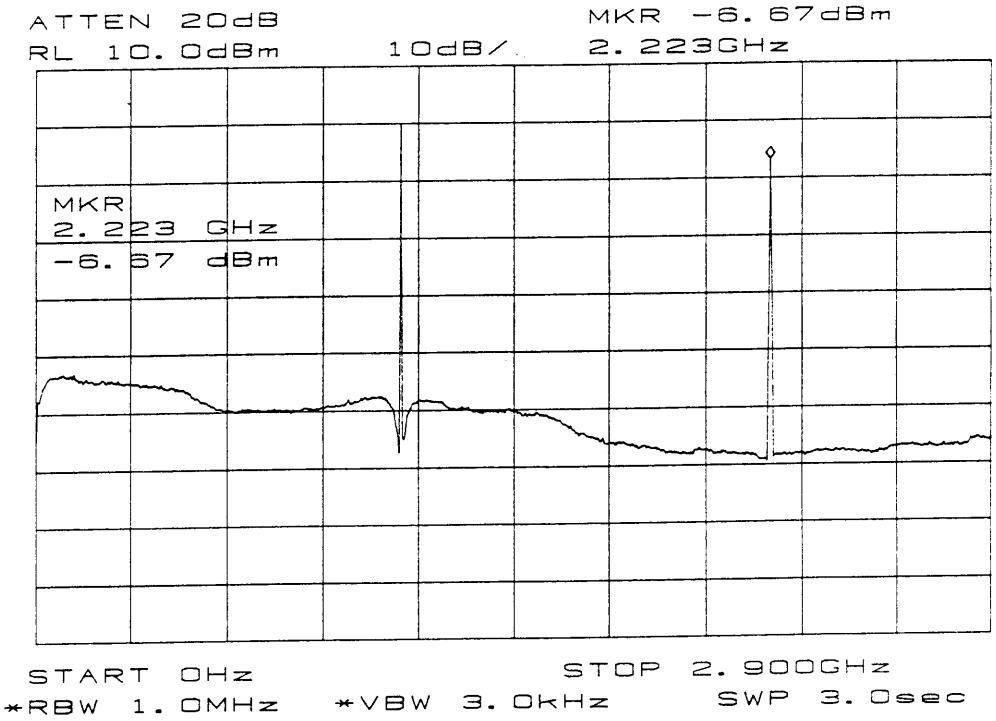


Figure 4.19 Harmonic Output of Second-Stage Amplifiers (x 2)

At the selected bias points, the amplifiers achieve linear gain of 25dB, input return loss of 16dB, and output return loss of 22dB.

Bias Circuitry

Once the appropriate bias point has been selected, circuitry must be provided to ensure that the comb-line amplifier operates at the desired bias point. This bias circuitry must establish the desired bias point across the entire operating temperature range the INA [25].

The biasing scheme chosen was a fixed-voltage bias on collector output of the INA. Temperature compensation and voltage drops were accomplished with addition of a bias stabilization resistor in the collector. The configuration is shown in Figure 4.20.

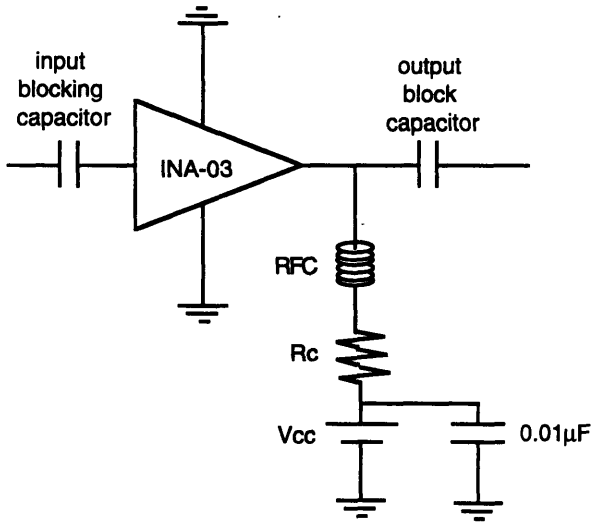


Figure 4.20 Collector Bias Stabilization Biasing Scheme

Voltage is supplied through a radio frequency choke (RFC) to keep the high frequency signal isolated from the DC circuits [25]. The inductor must be free of resonance for frequencies beyond the operating range [52]. A large-valued capacitor connects the DC side of the RFC to ground in order to reject any high-frequency component that gets past the RFC [25]. DC

blocking capacitors provide inter-stage isolation [23]. The capacitor values were selected to provide low impedance paths at the RF frequencies of operation. The bias stabilization resistor (R_C), connected in series with the RFC, performs temperature compensation through a simple feedback process [25]. It also drops the supply voltage to the appropriate bias point. The value of R_C is calculated as follows,

$$R_c = \frac{(V_{CC} - V_d)}{I_d} = \frac{(5V - 2.9V)}{10mA} = 210\Omega$$

where V_d and I_d are the desired bias points, with V_{CC} being the supply voltage. The amplifier schematics are shown in Figures 4.21 and 4.22 with the proposed biasing scheme. Relatively few components are used, and the circuit performance is not very sensitive to the component values, making the design reliable and robust.

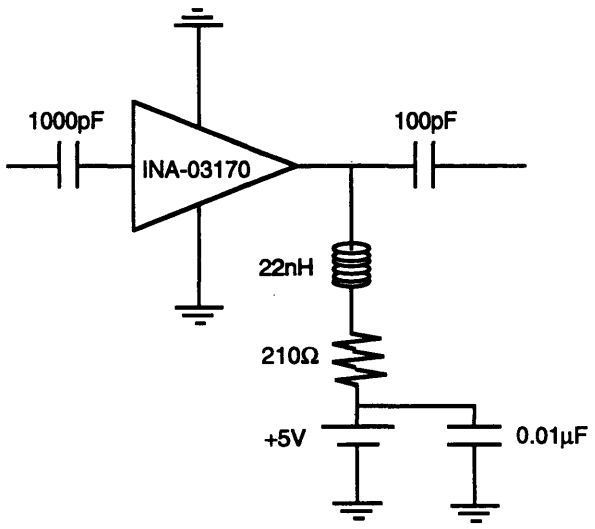


Figure 4.21 Schematic for First Multiplier Stage Amplifier

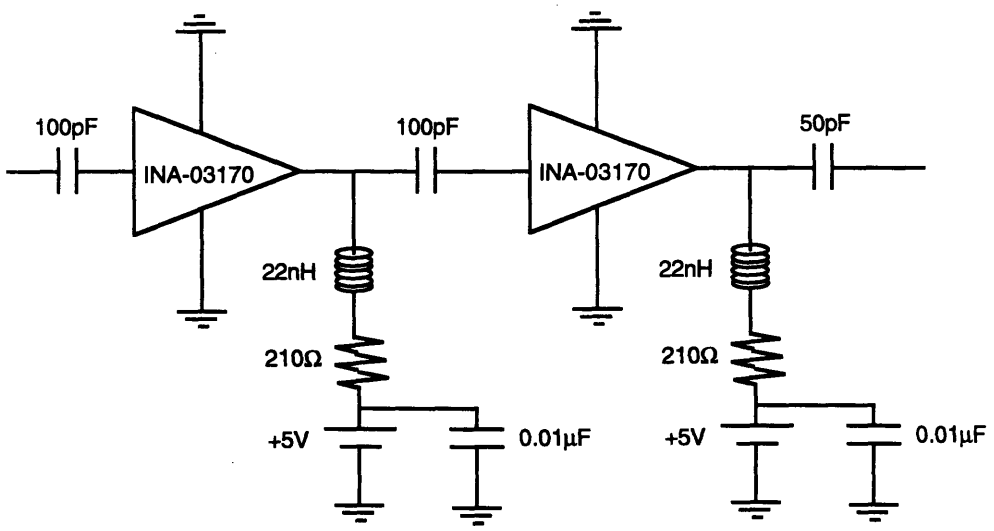


Figure 4.22 Schematic for Second Multiplier Stage Amplifiers

4.6.3 Power Supply Filtering Circuits

The bias points for the amplifiers have been selected so that drifts in supply voltages and currents from their nominal values do not affect comb generation performance. Noise in the supply voltage may also cause non-compliance with LO performance specifications. The noise must therefore be sufficiently attenuated.

Sideband Generation due to Supply Noise

Power supply noise, in the form of a voltage ripple at the switching frequency, causes second order intermodulation during the comb generation process. The noise signal will mix with the fundamental carrier signal to form sidebands spaced about the fundamental signal by the power supply switching frequency [21]. One can therefore expect sidebands at (carrier frequency) ± (switching frequency). With the EPC switching at 100kHz, sidebands will exist at 1112.4MHz and 1112.6MHz for the first stage of the multiplier chain, and at 2224.9MHz and 2225.1MHz for the second stage. Because sidebands are inband spurious, they must meet

the spurious specification of -73dBc for $f_0 \pm 575$MHz. The voltage ripple must be attenuated to a point where the sidebands fall below such requirement.

Test Measurements

Empirical measurements, using the test setup of Figure 4.23, were used to determine the amount of rejection needed on the supply voltage ripple.

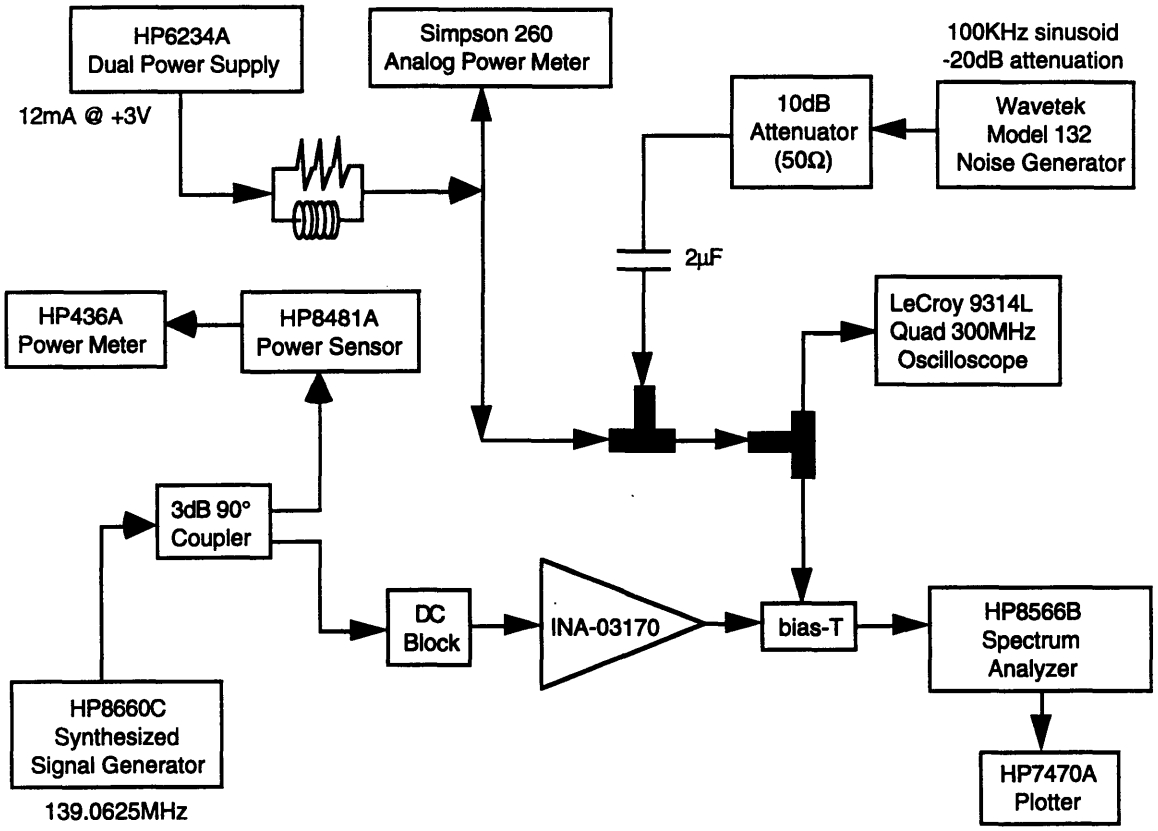


Figure 4.23 Test Setup for Sidebands due to Power Supply Noise

The test setup simulates a noisy EPC by mixing a 100kHz sinusoid into a DC signal using a coupler. A capacitor on the output of the noise generator provided for AC coupling. A parallel resistance-inductance circuit on the DC side was used to increase the impedance of the DC path. The inductor also provided AC isolation between the oscillator and the power supply. The resulting waveform was confirmed on an oscilloscope. The AC noise was ad-

justed to $20mV_{pp}$, in accordance with the noise performance of the EPC. The resulting mixed power supply signal was used to bias the amplifier. The INA was first driven with an input signal at 139.0625MHz, to simulate first stage of the multiplier chain. Table 4.7 records the magnitudes of the sidebands at various supply noise levels.

5	-51.0	-53.0
10	-46.0	-46.1
15	-42.5	-43.0
20	-40.0	-40.5
30	-34.2	-34.4
40	-34.0	-34.4
50	-31.9	-32.7
60	-30.4	-30.8
75	-28.6	-29.0

Table 4.7 Measured Data for Sidebands at 1112.5MHz

Calculation of Attenuation Requirement on Voltage Ripple

The shaded row shows that, with a voltage ripple of 20mV, the sidebands are only 40dB below carrier. An additional 33dB of rejection on the sidebands is desired, to achieve a 73dB spurious-free dynamic range. A goal of -80dBc sideband level is chosen to allow a 7dB margin. To determine the voltage ripple magnitude that corresponds to -80dBc sideband, the measured data is used to graphically correlate the sideband levels (in dBc) with the supply noise levels (in mV). In Figure 4.24, logarithm of the supply noise is plotted against the side-band level (in dBc). Since the plot is approximately linear, the noise level in mV required to achieve -80dBc sidebands is determined by simple linear extension.

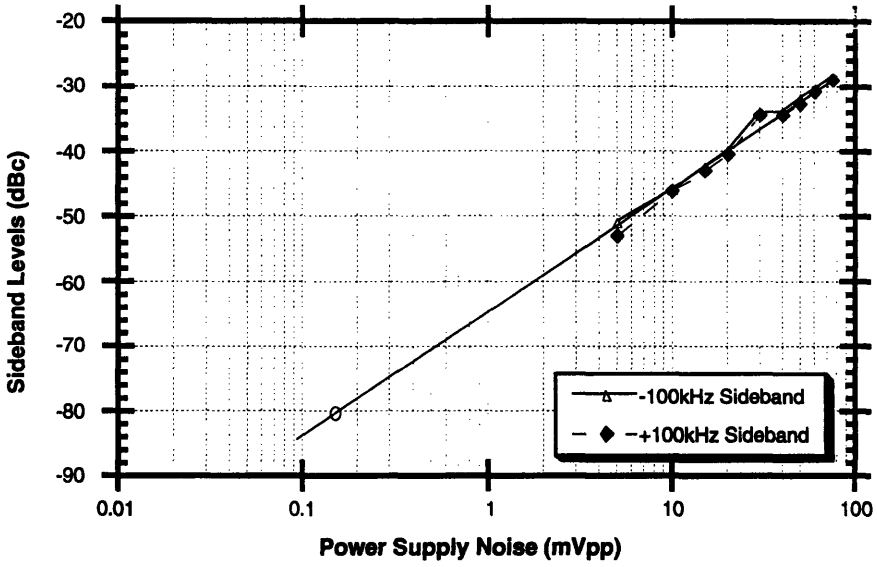


Figure 4.24 Sideband Levels vs. Power Supply Noise

Linear extrapolation shows that a voltage ripple of approximately 0.14mV is required to realize sideband levels of -80dBc. Reducing the supply noise from 20mV to 0.14mV corresponds to -43dB of rejection on the part of the power supply filtering circuitry.

Sidebands about the second stage carrier signal were examined as well. The same test setup as in Figure 4.23 was used, with the amplifier being now driven at 1112.5MHz. The measured data are summarized in Table 4.8.

5	-65.1	-65.9
10	-58.9	-60.8
15	-55.8	-56.8
20	-53.8	-54.8
30	-50.5	-51.5
40	-47.1	-47.8
50	-44.9	-45.6
60	-42.9	-44.0
75	-41.4	-42.6

Table 4.8 Measured Data for Sidebands at 2225MHz

The sidebands about the 2225MHz carrier signal are lower relative to the carrier compared to the sidebands of the first stage (-53.8dBc vs. -40dBc). Therefore, the power supply filtering requirements are constrained by the attenuation requirements of the first stage. Power supply filtering must achieve rejection of at least 43dB at 100kHz.

Implementation of Power Supply Filtering Circuitry

A lowpass filter was used in the power supply circuit to perform the filtering function. It will pass the DC component and reject components at and above 100kHz. Because of the low frequency range, the filter was realized with lumped elements for optimal tradeoff between size and performance. A two-pole structure is needed to achieve 40dB rejection per decade. The cutoff frequency was designed to be slightly lower than 10kHz, so that a minimum rejection of 40dB may occur at one decade away, or at 100kHz. A simple circuit to realize the desired specifications is shown in Figure 4.25. Element parasitics are shown and indicated by a 'p' subscript.

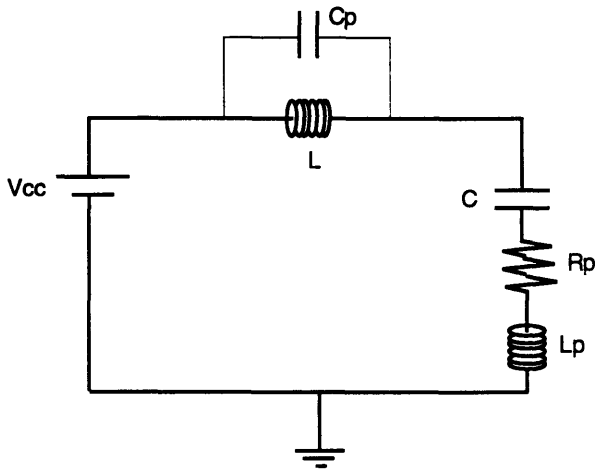


Figure 4.25 Power Supply Filter

L and C values were chosen such that the lowpass filter cuts off at 10kHz, according to the following equation:

$$\sqrt{LC} = \frac{1}{2\pi f} \text{ where } f = 10\text{kHz}.$$

The largest practical value for a capacitor with good characteristics is roughly 1μF. The choice of inductor is more flexible. The effects of resistive drop in the inductor (which may range anywhere from 0.25-2V) must be taken into account. With a 1μF capacitor, the inductor value required to achieve the desired resonant frequency is 250μH.

Figure 4.26 shows the projected filter response. The response differed from strictly lowpass response due to parasitic effects of the lumped elements.

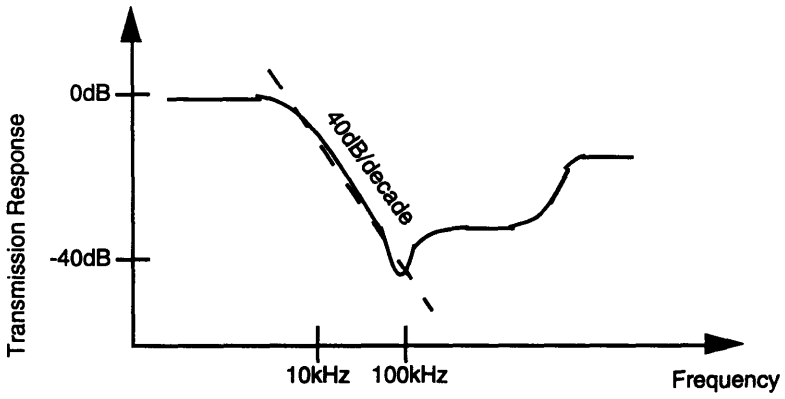


Figure 4.26 Power Supply Filter Response

A notch occurs in the lowpass response due to the resonance of C and L_p, creating a resistive short to ground. The notch may be designed to occur at 100kHz to maximize rejection of the power supply noise. This may be accomplished by choosing a capacitor with the appropriate parasitic inductance value. Additional inductor may be added in series or parallel to achieve the inductance required for resonance at 100kHz. To prevent the notch from shifting with temperature, a capacitor realized with low temperature coefficient dielectrics should be chosen [40]. The filter response rises back up when L and C_p start to resonate, reducing the high frequency rejection characteristics of the inductor. At higher frequencies, the inductive effects of the shunt capacitor also reduce the lowpass effects of the filter.

4.7 Filtering

Bandpass filter, in conjunction with a comb generator, makes up a complete multiplier stage. The comb generator outputs signals at frequency multiples of its input, and the filter selects the desired harmonic. The requirements of the filter depends on the relative harmonic levels of the comb generated and the spurious specifications for the LO system. These specifications are:

- Inside $f_0 \pm 575$MHz -73dBc max
- Outside $f_0 \pm 575$MHz -40dBc max.

The choice of technology with which to implement the filters will be selected based on several criteria. Filter rejection must be sufficient for the LO spurious output to comply with the above specifications. The other major criterion is size. Several filter technologies will be considered, including surface acoustic wave (SAW) [41], microstrip coupled-line, microstrip interdigital, and dieletric block.

4.7.1 Specifying Filter Requirements

Filter rejection requirements were established based on the LO output spurious specifications in Table 4.1 and the optimized comb generator outputs in Figures 4.18 and 4.19.

One approach for determining filter requirements would be to ensure that the spurious in each of the two stages are independently rejected to -73dBc. Thus, the filtering for the second stage may be specified under the assumption that its only input is the carrier signal at 1112.5MHz. The other harmonics at the input to the second stage may be ignored, since they will be at -73dBc or below. This approach greatly simplifies the filter specification process.

The above approach results in filter requirements which are more stringent than needed, leading to unnecessarily difficult filter designs which occupy more space. A more practical approach is to distribute the overall spurious rejection requirements among the two filters such that both filters become equally difficult to design. This scheme uses the filtering provided by the second stage to reduce the rejection requirements of the first-stage filter.

First-Stage Filtering Specification

Largest attenuation must be performed by the first-stage filter, since sharp filter designs are easier to realize at the lower, first-stage frequencies than at the higher, second-stage

frequencies. A rejection figure that may be achieved using most technologies is 60dB. 45dB was assumed in the calculations to leave margin for implementation uncertainties. Figure 4.27 illustrates the preliminary first-stage filter rejection requirements.

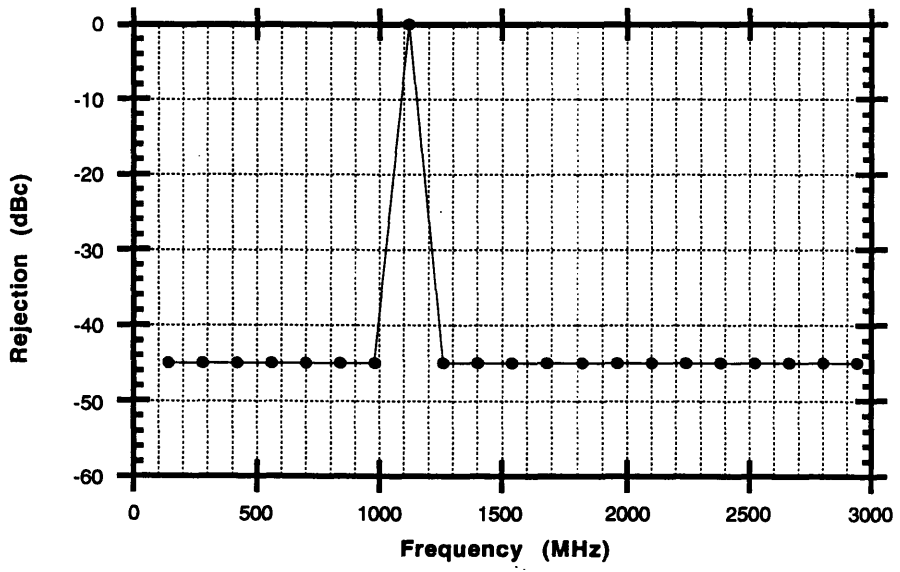


Figure 4.27 First-Stage Filtering Requirements

Second-Stage Filtering Specification

Specification of the second-stage filter is complicated by the fact that input to the second-stage multiplier consists of more than one signal (above -73dBc). The 1112.5MHz carrier signal is accompanied by harmonics which violate the -73dBc spurious requirement. Each of these signals will be the source of its own comb being generated by the second-stage amplifier. Second-stage filter specification must account for spurious contribution from all of the combs combined. Complete analysis of second-stage filter requirements involves the following steps:

1. Determine the levels of those harmonics entering the second-stage comb generator which exceed -73dBc for inband (f_0±575MHz) and -40dBc out-of-band.

2. Calculate the comb generated from each of the above harmonics by the second-stage comb generator.

3. Accumulate the power levels of second-stage harmonics which occur at the same frequencies.

4. Based on above calculation of the spurious levels at the output of the second-stage comb generator, determine the second-stage filter rejection characteristics necessary for the LO output to meet both inband and out-of-band spurious requirements.

Spreadsheets were constructed in *Microsoft Excel* to perform the analysis for the four steps above.

Step One is illustrated in Appendix B.1. Absolute power levels of the comb output of the first-stage INA was measured on the bench (Figure 4.18) through the 21st harmonic. They were then converted to levels relative to the carrier signal, or the eighth harmonic. Based on the first-stage filter rejection of 45dB, the levels relative to the carrier of the harmonics entering the second multiplier stage were calculated.

Step Two is illustrated in Appendix B.2. A comb is characterized out to the 21st multiple for each of the 21 first-stage harmonics. Each comb, generated as a result of the nonlinear mixing in the second-stage comb generator, exhibits gradual attenuation of its higher-order harmonics. The algorithm for calculating attenuation of the harmonics in each comb is based on bench measurements of comb generation at two frequencies, 139.0625MHz and 1112.5MHz (Figures 4.18 and 4.19). The 139.0625MHz attenuation figures are applied to

combs with fundamental frequencies in the range of 139.0625-1112.5MHz. The 1112.5MHz attenuation figures are applied to combs with fundamental frequencies greater than or equal to 1112.5MHz. Uniform attenuation algorithm is not applied to all combs, because harmonic attenuation trends differ with frequency of the fundamental signal. Those combs with higher fundamental frequencies fall off faster in magnitude. The two-tier scheme used here performs a more realistic, yet still worst-case, estimation of attenuation levels of all 21 combs.

Steps Three and Four are illustrated in Appendix B.3. The 21 combs at the output of the 2nd-stage comb generator have many harmonics at common frequencies, since the combs are all harmonically related to 139.0625MHz. Harmonics at the same frequencies add in power (under worst case conditions). The spreadsheet in Appendix B.3 accumulates the power levels of the second-stage harmonics at the same frequencies. Not all such harmonics are accumulated, in the interest of calculation efficiency. Only those harmonics which do not meet the spurious requirement by a margin of more than 12dB (-85dBc for inband and -52dBc for out-of-band) are considered. The 12-dB margin serves the purpose of accounting for those harmonics which only marginally complies with the spurious requirement but will violate it once accumulated with other harmonics at the same frequency. The harmonics chosen to be accumulated are shown in the Appendix B.2 worksheet as shaded cells. After the power levels at each harmonic frequency have been summed, the amount of rejection required of the second-stage filter is calculated at each frequency based on the spurious specifications. Figure 4.28 summarizes the second-stage filtering requirements as calculated in the worksheet in Appendix B.3.

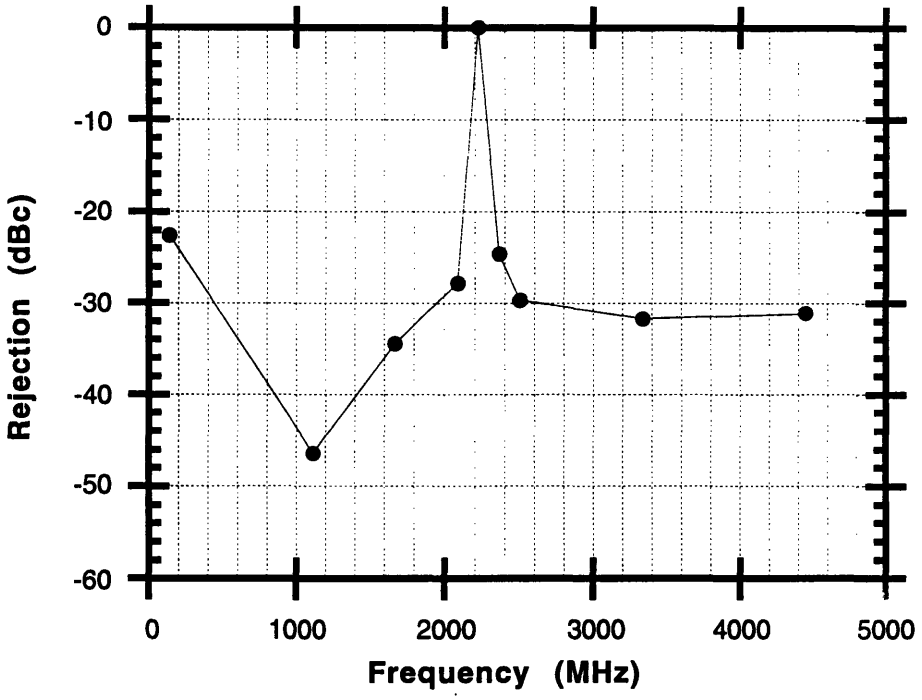


Figure 4.28 Second-Stage Filtering Requirements

Filter Margins

Margins should be added to the above two sets of filter requirements for several reasons.

Response of a saturated amplifier to a comb of harmonics of varying power levels is uncertain. The output signals of the first-stage filter, including the 1112.5MHz carrier, which are entering the second-stage comb generation amplifier may not be amplified uniformly. The 1112.5MHz carrier will saturate the amplifier and harmonics will be derived from it. The carrier will be in the compressed region of the amplifier and thus experience very little gain. Other harmonics will be at power levels below the carrier upon entering the amplifier due to

rejection by the first-stage filter. They may experience greater gain than the carrier. The gain they experience cannot be analyzed by the linear gain concept due of the saturated state of the amplifier. The carrier-spurious isolation will therefore degrade. This degradation is assumed to be nonexistent in the calculations of second-stage filter requirements. The uncertainty may initially be compensated by adding margins to filter rejection specifications.

Relative harmonic levels may vary over temperature and over time. The desired harmonic multiples may not consistently stand out against their neighboring harmonics as desired. Filter margins will also compensate for these phenomena.

Based on the above considerations, 5dB of margin has been added to the first-stage filtering specifications, and 10dB of margin has been added to the second-stage. Figures 4.29 and 4.30 show the final filter rejection specifications for first and second multiplier stages. Experimental results will confirm the adequacy of the margins added. Note that, as initially planned, the two sets of filtering requirements are approximately equivalent in terms of difficulty of realization, bearing the same sharpness relative to the frequency of operation.

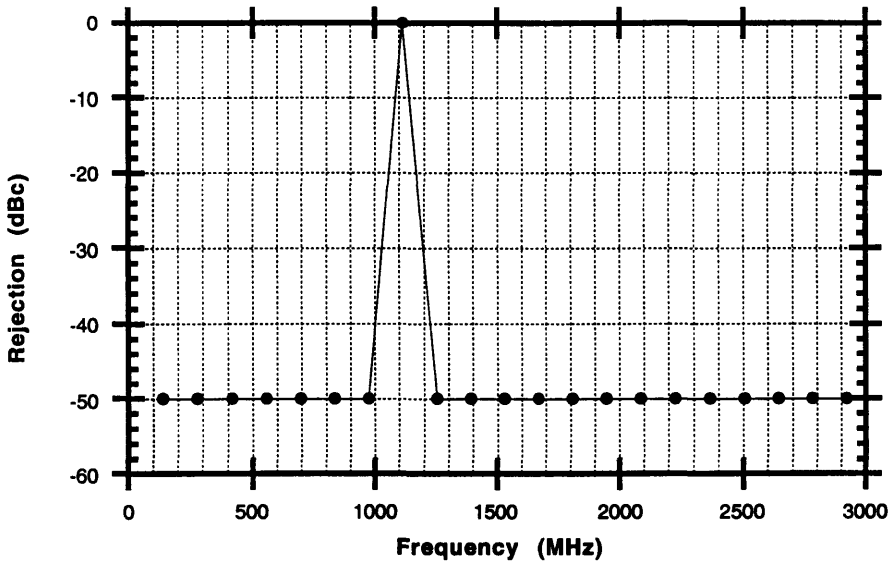


Figure 4.29 Final First-Stage Filtering Requirements

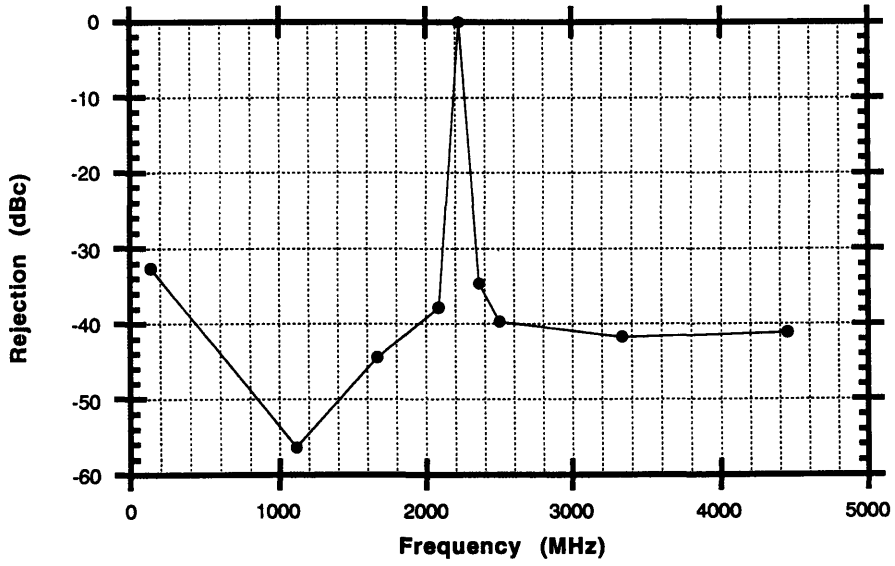


Figure 4.30 Final Second-Stage Filtering Requirements

Filter Bandwidth

The filter passbands must enclose the carrier signals at all times. Therefore, the filter bandwidth must be wide enough to compensate for filter center frequency shift, which may occur due to component variations, temperature changes, and aging. Consequently, the bandwidth requirement is a function of frequency stability of each particular filter technology. For most filter technologies, a bandwidth of approximately 15MHz will be sufficient.

Crystal oscillator frequency drift is not a factor in dictating filter bandwidth. The TCXO's stability of ±2ppm over -10/+55°C and fifteen years translates to a lifetime variation of ±278Hz, well within the bandwidth of most filter designs.

Number of Poles

The minimum number of filter sections necessary may be determined from bandwidth and rejection specifications of Figures 4.29 and 4.30. Equations in [42] are used to calculate the theoretical minimum, as illustrated in Appendix C. Appendix C illustrates the equations used to determine the pole requirements for Chebyshev filters. Both filters require a minimum of three sections. The same conclusion has been reached based on simulations with microwave-system simulator program [43]. The identical pole requirement on both filters illustrates that the filtering requirements have indeed been fairly evenly distributed across the two filters.

With the specification of filter performance completed, various filter implementations were evaluated. Four technologies were assessed in terms of rejection, size, stability, insertion loss, return loss, and engineering risk. Discrete element, printed, and metallized plastic cavity filters were not considered due to size or rejection requirements.

4.7.2 Surface Acoustic Wave (SAW) Filters

SAW devices operate with acoustic rather than electromagnetic waves. Piezoelectric materials are used to convert the incoming electromagnetic signal to an acoustic signal, and vice versa. SAW devices are considered to be rugged and reliable. The semiconductor wafer processing techniques used in the manufacturing of SAW components permit large-volume production of economical and reproducible devices. Compared to other filter technologies, SAW filters often offer advantages in linear phase, low form factor, and rejection. Temperature stability is dependent on the materials selected for SAW device fabrication. Because an acoustic wavelength is much smaller than its electromagnetic counterpart, SAW devices also achieve significant size advantages. However, for the same reason, SAW applications are constrained to low frequencies. Current photolithographic techniques are capable of fabricating electrodes narrow enough for operation up to 2.5GHz. Another drawback is insertion loss. Because the basic SAW transducer is a bidirectional radiator, an inherent 6dB loss is associated with the structure. Other second-order effects raise the insertion loss of typical SAW filters to 15dB-30dB. Triple transit signals intrinsic to SAW devices further aggravate insertion loss. Electrical impedance matching will suppress the effect of triple transit, at the expense of passband ripple and overall filter size. The time spurious responses inherent to SAW filters make them more vulnerable to crosstalk, which will severely compromise rejection [41].

SAW filters' significant size advantage makes them a worthwhile candidate. Their rejection characteristics often match or exceed those of dielectric block filters. However, submicron electrode geometries constrain the usefulness of SAW devices to frequencies that only marginally covers the multiplier chain filters' frequencies of operation. Table 4.9 summarizes available performance for SAW filters for the C-band receiver LO application.

	1112.5-MHz Filter	2225-MHz Filter
Insertion Loss	11dB	13dB
Stopband Rejection	45dBc @ 973MHz 45dBc @ 1251MHz 25dBc @ 2642MHz 25dBc @ 2781MHz 25dBc @ 2920MHz	40dBc @ 1112.5MHz 30dBc @ 2086MHz 30dBc @ 2364MHz 35dBc @ 2503MHz 25dBc @ 2642MHz 25dBc @ 2920MHz 10dBc @ 3337MHz 10dBc @ 4450MHz
Dimensions	0.354Δ x 0.276Δ	0.354Δ x 0.276Δ

Table 4.9 SAW Filter Characteristics

The SAW filters occupy about one-third of the space of the dielectric block filters, and even less compared to the microstrip implementations. However, their significant insertion losses are not compatible with the LO system s power level distribution. With the SAW filters, it will be questionable whether the LO will be able to output the required +13dBm drive level. Most importantly, the SAW filters stopband performance, particularly on the high side, is significantly worse than the minimum filter requirements depicted in Figures 4.29 and 4.30.

The high-frequency range of operation of the LO multiplier filters have clearly compromised the typical advantages of SAW filters. Both insertion loss and stopband performance are unacceptable.

4.7.3 Microstrip Coupled-Line Filters

Microstrip circuits present an attractive alternative in terms of size, weight, economy, and reproducibility. The frequency band most suitable for microstrip application ranges from a few gigahertz up to many tens of gigahertz. The lower bound is determined by practical circuit sizes. The upper bound is constrained by radiation losses, higher-order modes, and fabrication tolerances [45]. The relevant frequencies in the LO multiplier implementations, ap-

proximately 1GHz and 2GHz, lie at the low end of the microstrip usability frequency spectrum. As a result, large physical sizes may be of concern.

An existing design of a three-pole microstrip coupled-line filter was investigated for application to the LO multiplier chain filtering needs. The design is shown in Figure 4.31.

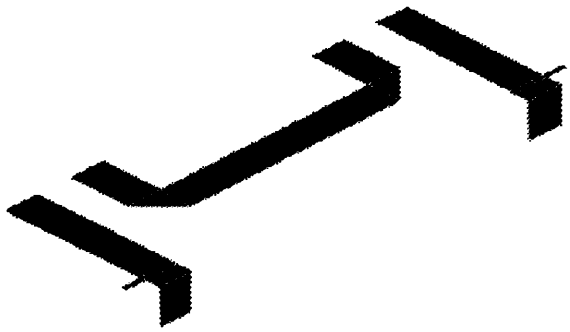


Figure 4.31 Microstrip Coupled-Line Filter

High dielectric constant material is used in order to reduce filter dimensions. The filter employs direct tapping of the resonators for input and output, as described by Dishal [46]. It consists of three resonator structures: two quarter-wavelength resonators which are tapped for input and output and one half-wavelength resonator in the center. The resonator length is the principle factor in determining the filter resonating frequency. Deviations from the resonating frequency will occur due to effects of open ends, interaction between adjacent resonators, and interactions between the resonators and circuit supports. Separation between any two resonators determine the amount of mutual coupling, which establishes the filter shape. The locations of input and output tapping points may be adjusted to realize the desired phase. The initial design was simulated with "*IE3D*" software, an integrated full-wave electromagnetic simulation package [32]. Filter parameters were then tuned in attempt to realize the desired filter specifications.

Initial simulated filter response for the 2-GHz version is shown in Figure 4.32. In comparison with the 2-GHz filter specifications of Figure 4.30, it is clear that rejection requirements are not being met.

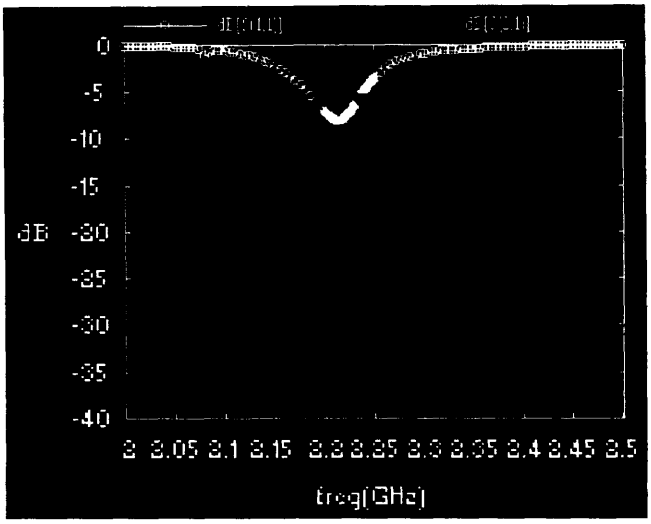


Figure 4.32 Initial 2-GHz Coupled-Line Filter Response

Nearly 20dB of additional rejection is required at the first harmonic offset frequencies (f_0 139.0625MHz).

Improvement of Filter Response

One method of increasing stopband performance is narrowing the filter bandwidth. Bandwidth may be narrowed by reducing inter-resonator coupling, which is accomplished by increasing the spacing between resonators. Simultaneously, the resonators must be lengthened to compensate for the increase in resonant frequency due to drop in capacitances. Simulations show that, even with the original spacings doubled, rejection at the critical points are only improved by 2-3dB. Further increases in spacing are not practical due to circuit size constraints. Another method of improving filter sharpness is increasing its order. However, the addition of resonators results in a much larger circuit size.

Crosstalk

The possibility of crosstalk via inductive coupling was investigated. The input and output tap lines are placed orthogonal to each other, as shown in Figure 4.33. In such configuration, neither capacitive nor inductive input-output coupling will occur. However, simulation does not show improvement in stopband performance. Therefore, a different type of microstrip filter will be necessary in order to achieve the desired rejection performance within the allotted real estate. The interdigital topology is next considered. Its compact, quarter-wavelength structure permits a higher-order filter to be designed without requiring more area.

Figure 4.33 Coupled-Line Filter with Orthogonal Input-Output

4.7.4 Microstrip Interdigital Filters

Microstrip interdigital filter possesses several advantages over the edge-coupled filter described above. The foremost advantage is its extremely compact size. Additionally, it has no spurious second harmonic passband, thus achieving greater rejection on the high side. However, the interdigital approach has several disadvantages. It requires short circuits. The filters tend to be lossier than the edge-coupled versions, with greater sensitivity to element variations. Confirmation of filter design using computer simulation tools is more difficult with the interdigital filters than with the edge-coupled designs [48]. Most microwave CAD

programs, with the exception of those employing electromagnetic methods, do not model accurately the interdigital filter s multiple-coupled structure. They are generally restricted to the analysis of singly coupled transmission line sections. Packages with electromagnetic simulation methods are typically not practical as an iterative design tool due to their long computation times. A tapped-line microstrip filter design, shown in Figure 4.34, is considered here for the LO multiplier filtering application. The short circuits are implemented with via holes. The resonators are quarter-wavelength long.

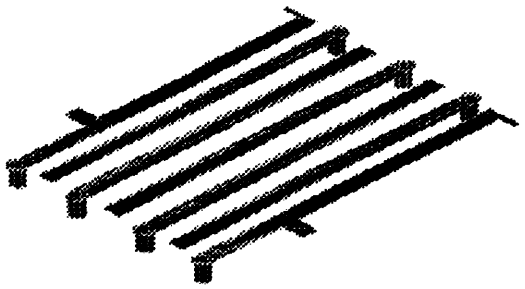


Figure 4.34 Microstrip Interdigital Filter Design

The design method is based on a CAD model proposed in [48] suitable for analysis and optimization of the interdigital filters using a non-electromagnetic simulation program such as *Touchstone*. Even- and odd-mode impedances of the resonators were obtained using equations given in [49], also given in Appendix D. Coupling coefficients were calculated from the impedances. Circuit parameters were then designed to realize the desired coupling coefficients. Because the CAD model of [48] requires the use of equal resonator strip widths for simpler design and analysis of the interdigital filter, the exact coupling coefficients may not be achieved. However, further optimization of the strip spacings will enable fairly accurate realizations.

Simulation of the initial design was performed using a non-electromagnetic simulation program such as *Touchstone*. Grayzel's identity [50] is used to model multiple-coupled transmission line structures as parallel sections of singly coupled lines. The identity, in terms of normalized line capacitances, is illustrated in Figure 4.35 for a five-conductor structure.

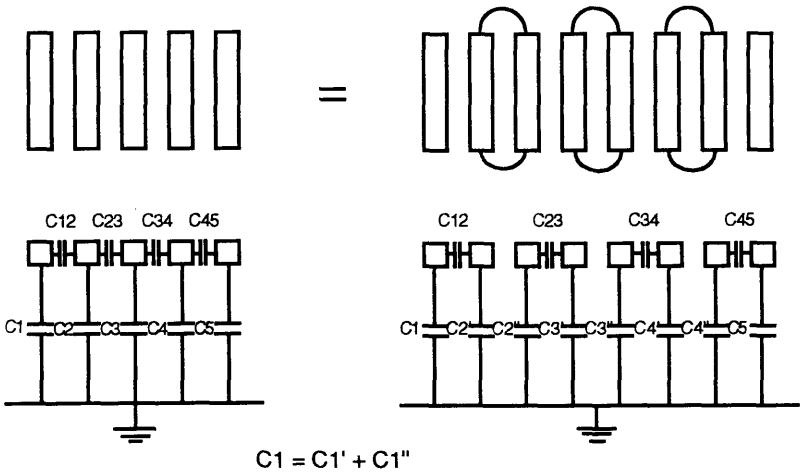


Figure 4.35 Grayzel's Identity for a Five-Conductor Structure [48]

The model based on Grayzel's method was used to simulate a set of even- and odd-mode impedances transformed according to the following equations:

$$Z'_{oe} = \frac{1}{\left(\frac{1}{Z_{oe}} - \frac{1}{2Z_s}\right)}$$

$$Z'_{oo} = \frac{1}{\left(\frac{1}{Z_{oo}} - \frac{1}{2Z_s}\right)}$$

$$Z'_s = 2Z_s$$

where Z_{oe}, Z_{oo}, and Z_s are values of the even-mode impedance, odd-mode impedance, and single-strip impedance for the actual resonators, as calculated using equations in [49]. Figure 4.36 illustrates the use of the transformed impedances in a CAD model.

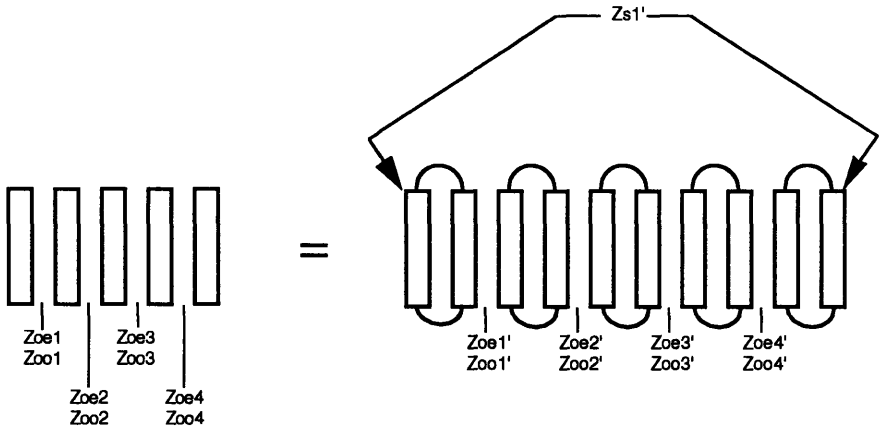


Figure 4.36 Grayzel s Identity for CAD Model [48]

Strip spacings, strip lengths, and tap points were optimized to meet the desired specifications with some margin. Figures 4.37 and 4.38 show the simulation responses for the 1-GHz and 2-GHz filters, respectively.

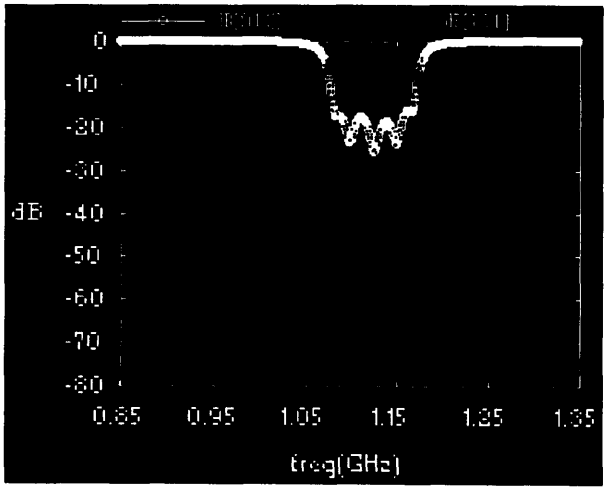


Figure 4.37 1-GHz Interdigital Filter (Simulated)

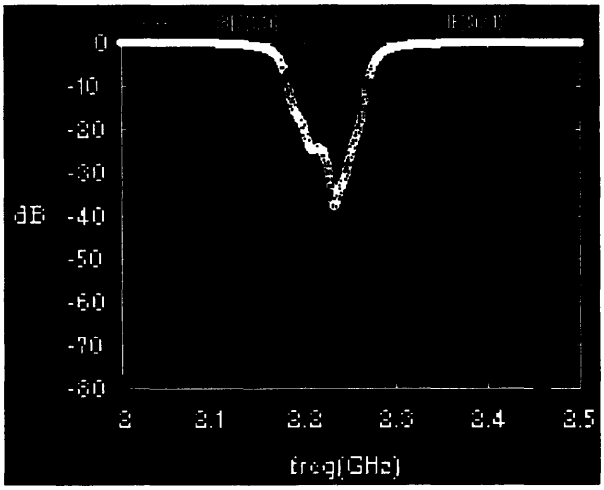


Figure 4.38 2-GHz Interdigital Filter (Simulated)

4.7.5 Dielectric Block Filters

Dielectric block filters offer low loss and high performance in the 300MHz to 6GHz range with 0.1 to 10% 3-dB bandwidths, making them suitable for this receiver LO [29]. The ceramic technology's usable frequencies fill a gap between microstrip and lumped implementations. The 1- to 2-GHz frequencies are often too low to achieve microstrip filters of reasonable physical sizes, but frequently too high for practical lumped-element implementations. An added feature of the dielectric block technology is that the filters do not have second harmonic passbands, thus permitting better rejection performance on the high side. These ceramic filters also offer good temperature stability [29]. Figure 4.39 plots the measured filter response of a 2-GHz dielectric block filter. Table 4.10 compares the measured performance against the filter specifications developed and shown in Figure 4.30.

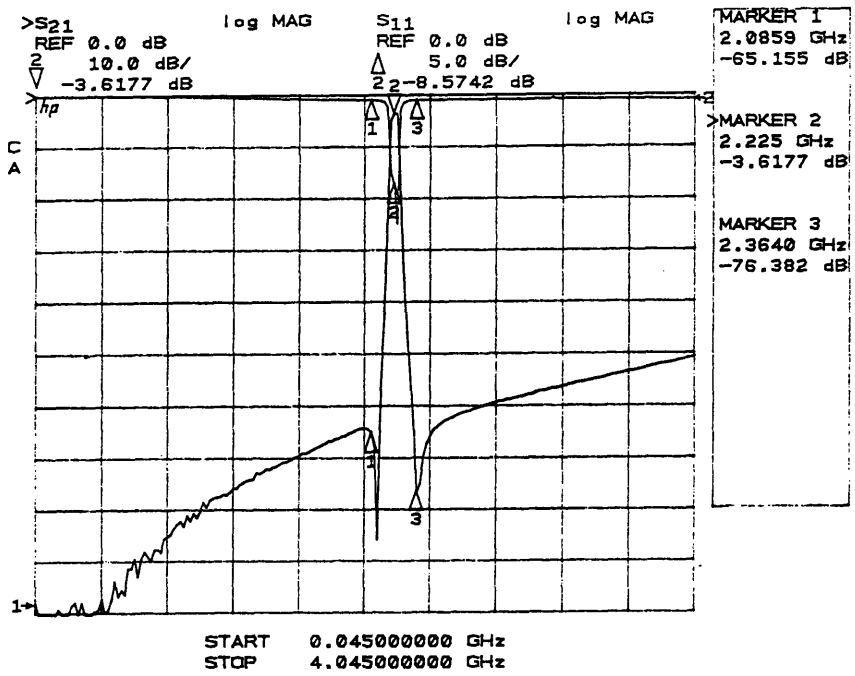


Figure 4.39 2-GHz Dielectric Block Filter Response

	2225-MHz Filter Specifications	2225-MHz 4-Pole Dielectric Block Filter Measured Performance
Insertion Loss	3dB	3.6dB
Bandwidth	15MHz	30MHz
Stopband Rejection	32.6dBc @ 139.10MHz	>96.4dBc @ 139.10MHz
	56.4dBc @ 1112.5MHz	84.4dBc @ 1112.5MHz
	44.4dBc @ 1668.8MHz	65.4dBc @ 1668.8MHz
	37.8dBc @ 2085.9MHz	61.4dBc @ 2085.9MHz
	34.6dBc @ 2364.1MHz	73.0dBc @ 2364.1MHz
	39.7dBc @ 2503.1MHz	58.6dBc @ 2503.1MHz
	41.7dBc @ 3337.5MHz	51.6dBc @ 3337.5MHz
Dimensions		0.64" x 0.275"

Table 4.10 2-GHz Dielectric Block Filter Characteristics

The stopband performance of the dielectric block filter exceeds the proposed requirements by approximately 20dB. The slightly higher insertion loss is easily compensated at a system level. The 30-MHz bandwidth is more than sufficient to cover the rated 6-MHz shift over

temperature, calculated from the filter's temperature stability performance of ±30ppm/°C over -20°C to +70°C. The dielectric block filter is approximately 80% the size of an equivalent microstrip interdigital filter.

4.7.6 Filter Selection

The SAW and microstrip coupled-line filters have been shown to be inadequate for the LO's filtering needs. The SAW filters are too lossy and fail to achieve sharp rejection in broadband. The microstrip coupled-line filters cannot realize the required stopband performance when constrained to a practical physical size. Both of these filter implementations will not be considered for this application. The dielectric block filters provide the best trade-off in size and performance. Therefore, they were selected as the baseline approach. The microstrip interdigital filters, though bigger than their dielectric block counterparts, have all the advantages of MIC circuits, including reproducibility and space qualification. A drawback is the uncertainty in how well the performance of the fabricated circuits will correspond to the predicted results. Nonetheless, benefits of the microstrip implementation warrant the interdigital versions to be considered as plausible solutions to the LO's filtering needs.

4.8 Driver Stage

A driver stage amplifier is needed as the output device of the LO chain to provide the proper output power level. It also provides isolation, acting as a buffer amplifier to prevent mixer power feedback from affecting performance of the LO.

The low-noise Mini-Circuits VNA-25 monolithic amplifier was initially considered for application as the driver amplifier. VNA-25 is a medium power amplifier designed for commercial applications in the frequency range 500-2500MHz. Its bias needs are extremely simple. A RF choke is not required because RF/DC connections within the package are sepa-

rate. Internal capacitors eliminate the need for additional blocking capacitors on input and output [52]. Table 4.11 summarizes the VNA's measured performance. The mounting configuration of the amplifier is shown in Figure 4.40.

Performance at 2225MHz	
Gain	17.7dB
P_{out}	17.0dBm
Input return loss	30.0dB
Output return loss	28.0dB

Table 4.11 VNA-25 Driver Amplifier Performance

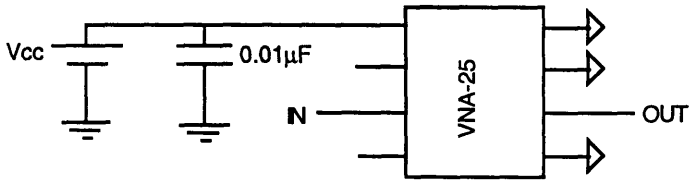


Figure 4.40 VNA-25 Mounting Configuration

With a stability factor (k-factor) much greater than 1.0, the amplifier is unconditionally stable [52]. The low parts count of its bias circuit results in higher reliability. However, the VNA-25 is currently only available in plastic package, rendering it inappropriate for flight applications.

A low-noise MMIC medium power amplifier whose operating range includes 2225MHz has been designed. The amplifier has an estimated 1-dB compression point at +16dBm. The design is projected to be unconditionally stable, operating with 100mA at +3V. Table 4.12 summarizes the amplifier's simulated performance.

Performance at 2225MHz	
Gain	14.3dB
P_{out}	17.0dBm
Input return loss	23dB
Output return loss	15dB

Table 4.12 MMIC Driver Amplifier Performance

This MMIC implementation will be used as the baseline driver amplifier for the multiplier chain LO. Although it has less gain than the VNA-25, the slight difference may be compensated at LO system-level design. Its worse return loss performance is inconsequential due to the projected return loss figures of the filters. Because the amplifier will be driven at a level close to its rated output power at 1-dB compression point, another 2225-MHz filter will be cascaded to its output in order to remove any extraneous harmonics generated.

4.9 Simulation

The LO multiplier chain was modeled and simulated in *Libra*, a microwave device and system analysis program. The purpose was to confirm the local oscillator design and to provide insights into design variations. By enabling relatively quick insight into the expected performance of complex designs, simulation with models reduced the number of hardware iterations needed to complete a functional prototype.

Models generally fit into one of the three major categories: linear, non-linear, and harmonic balance. Simulation using the harmonic balance model was employed for the LO system. Linear models do not account for non-linear performance characteristics such as intermodulation distortion, harmonic generation, or saturation. Full time-domain non-linear models predict more than what was needed for the LO simulation (e.g. transient response) at the expense of much greater complexity and time consumption [22].

Equivalent circuit models were used for INAs, filters, and attenuators. Interdigital filter models were used because of the similarity between the performance of interdigital and dielectric block filters. Amplifier scattering parameters were used in place of circuit models for amplifiers operating in the linear region, in order to reduce computational complexity. All components were assumed to lie on 25-mil alumina substrate. The stages in the multiplier chain were simulated in an incremental fashion.

Accuracy of the multiplier chain simulation was constrained by exactness of the INA circuit model. Power level and spurious rejection characteristics of the local oscillator output depended on consistent generation of a particular harmonic spectrum shape. However, *Libra* was not accurate in its prediction of the harmonic spectrum. INA generated an extended spectrum of harmonics, whereas *Libra* simulation was limited to a much smaller number of harmonics due to memory constraints. The power in the high-order harmonics ignored by *Libra* contributed to inaccuracies in the power levels of the low-order harmonics. Consequently, simulation was not a useful tool in the local oscillator design.

Chapter 5
LO Implementation and Measured Results

5.1 Introduction

A breadboard of the multiplier chain was integrated using components to be used in the final printed circuit board implementation, with the exception of the 1-GHz filter and the driver amplifier.* Although the concept of the multiplier chain is fairly straightforward, several performance issues may not be accurately projected, either in design or by simulation, due to interactions among second-order effects. Such issues include phase noise, power supply noise suppression, comb generation response, etc. For example, impedance mismatch at the outputs of the comb generators introduced by cascading the filters may modify the output comb characteristics. Therefore, the breadboard was used to evaluate the LO design.

5.2 Breadboard

The schematics for the first multiplier stage, second multiplier stage, and driver stage are shown in Figures 5.1, 5.2, and 5.3, respectively. The amplifiers are mounted as shown previously in Figures 4.21, 4.22, and 4.37. The breadboard was integrated such that minimal performance degradation may be attributed to the test setup. For example, SMA and N-type connectors were used to ensure good high-frequency performance. A synthesized frequency

* Substitutes were used for the 1-GHz dielectric block filter and the MMIC driver amplifier due to unavailability of the final parts. The 1-GHz filter was implemented with a 5-pole elliptic function stepped-digit bandpass filter. The driver amplifier was implemented with the plastic-packaged VNA-25.

source was utilized for its frequency stability. A 20-dB attenuator was placed on the source generator to increase the dynamic range of measurement.

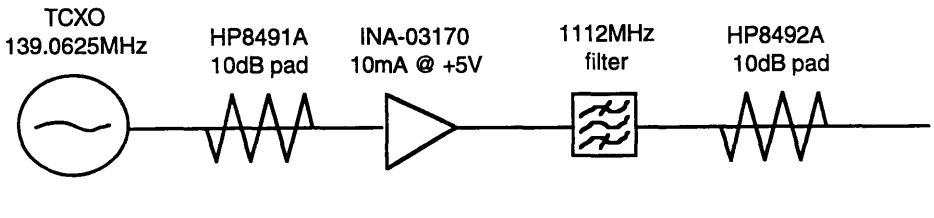


Figure 5.1 Local Oscillator Breadboard Schematic: First Stage

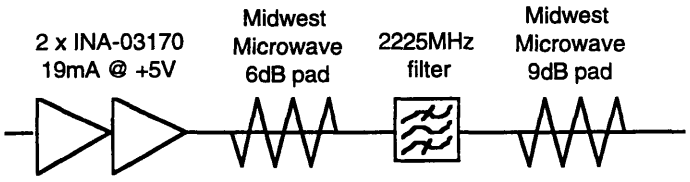


Figure 5.2 Local Oscillator Breadboard Schematic: Second Stage

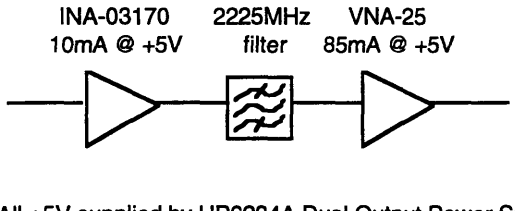


Figure 5.3 Local Oscillator Breadboard Schematic: Driver Stage

5.3 Results

First Multiplier Stage

The first multiplier stage was tested according to the setup of Figure 5.1. As shown in Figure 5.4, spurious output, in particular the seventh harmonic at 973MHz, was significantly higher than the projected -50dBc.

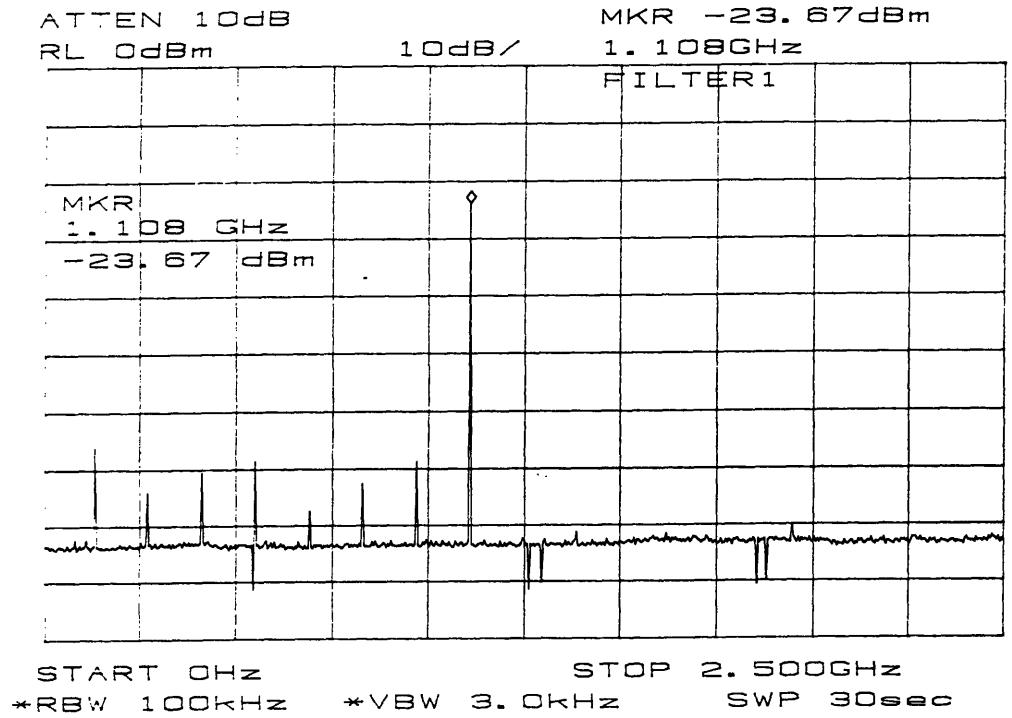


Figure 5.4 Output of First Multiplier Stage

The discrepancy was due to the difference in performance of the substitute stepped-digit bandpass filter and the dielectric block filter. The stepped-digit filter, used as a substitute for breadboarding purposes, has a larger bandwidth than the dielectric block filter it replaces. As can be seen from Figure 5.5, the stepped-digit filter has approximately 24dB of rejection at the seventh harmonic frequency compared to the dielectric block's 50dB. Therefore, the discrepancy is not expected in the final design.

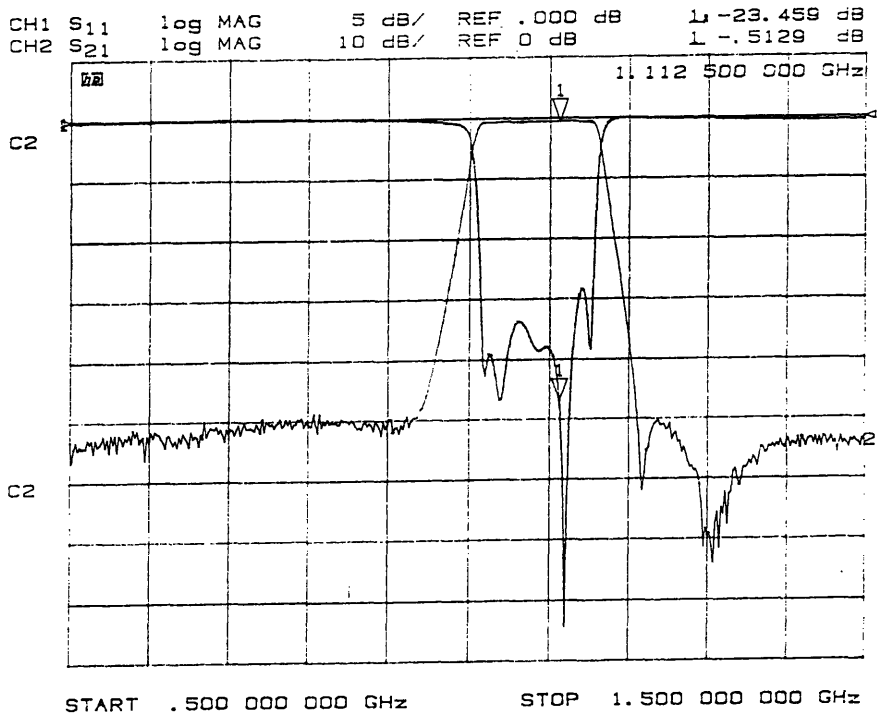


Figure 5.5 Filter Response of the Substitute Stepped-Digit Filter

Second Multiplier Stage

Figure 5.6 shows the output of the second stage gain/comb generation block, with the first multiplier stage cascaded as the input. Harmonics from the 139.0625MHz fundamental were significant. Their levels were approximately 30dB higher than projected. The most problematic were the ±139.0625MHz sidebands about the 2225MHz LO signal. The other spurious signals were more easily filtered.

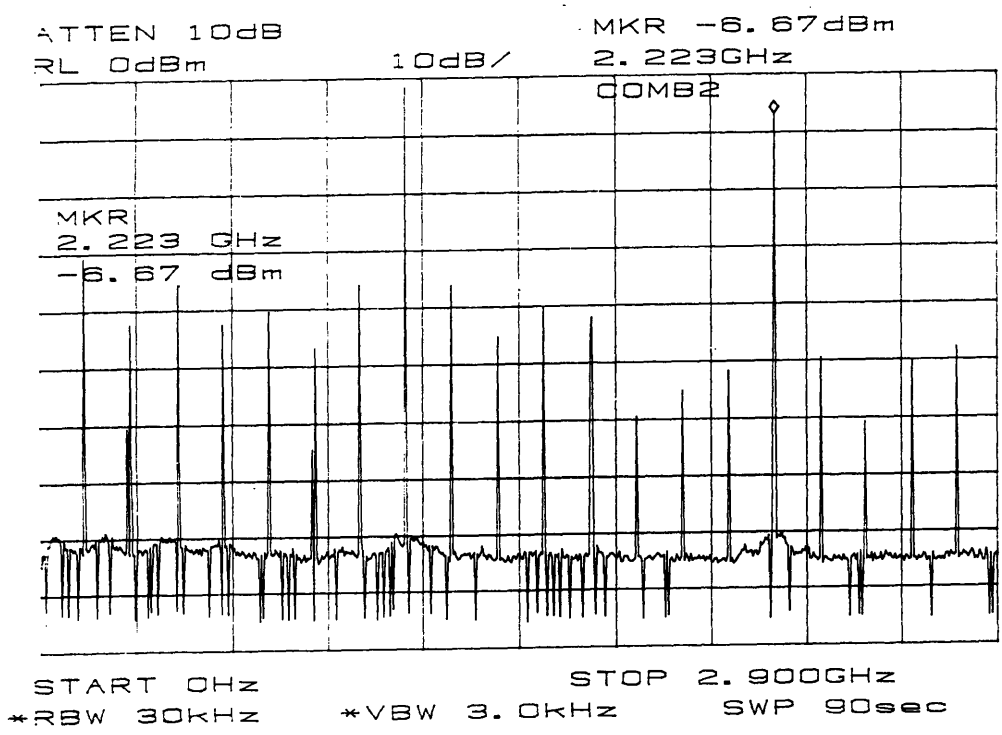


Figure 5.6 Output Spectrum of Second Stage Comb Generator

The cause of the high sidebands was hypothesized to be the high seventh harmonic from the first multiplier stage output, which was not fully attenuated by the 1-GHz stepped-digit filter. The seventh harmonic was significant enough to mix with the eighth harmonic. Such second order intermodulation produced sidebands at 139.0625MHz and 2086MHz [21]. The 139.0625MHz sideband may further excite the comb generator to produce harmonic distortion spectrum with it as the fundamental. It may also re-mix with the other strong signals (such as those at 1112.5MHz and 2225MHz) to generate sidebands at ±139.0625MHz.

Two synthesizers were used to generate signals at the frequencies and power levels of the seventh and eighth harmonics. The signals were coupled together and fed as input to the second stage comb generator (Figure 5.7), to simulate the effect of the comb output from the first multiplier stage.

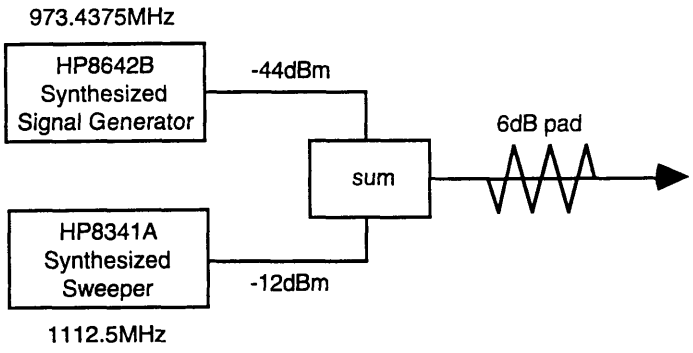


Figure 5.7 Test Setup to Simulate First Stage Output

Figure 5.8 illustrates that the seventh and eighth harmonics together do indeed result in ±139.0625MHz sidebands about the 2225MHz signal, as well as about the other 1112.5MHz harmonics.

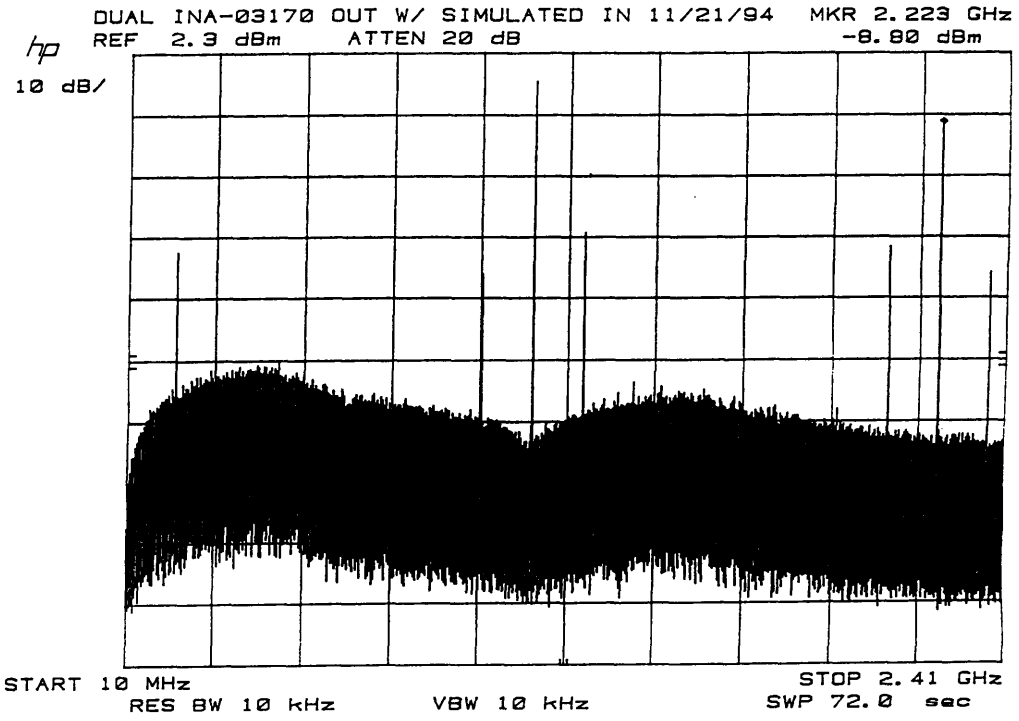


Figure 5.8 Output of Second Stage Comb Generator (with Simulated Input)

The sideband levels dropped in response to decrease in the level of the seventh harmonic. Empirical results showed that, in order for the spurious sidebands to be below -50dBc as originally projected in filtering analysis, the seventh harmonic level needed to be another 33dB lower. Therefore, the final 1-GHz dielectric block filter must realize the stepped-digit filter's rejection at 1112.5MHz + 33dB = 57dB of rejection at the seventh harmonic frequency. This requirement complies with the predicted response of the dielectric block filter, shown in Figure 5.9.

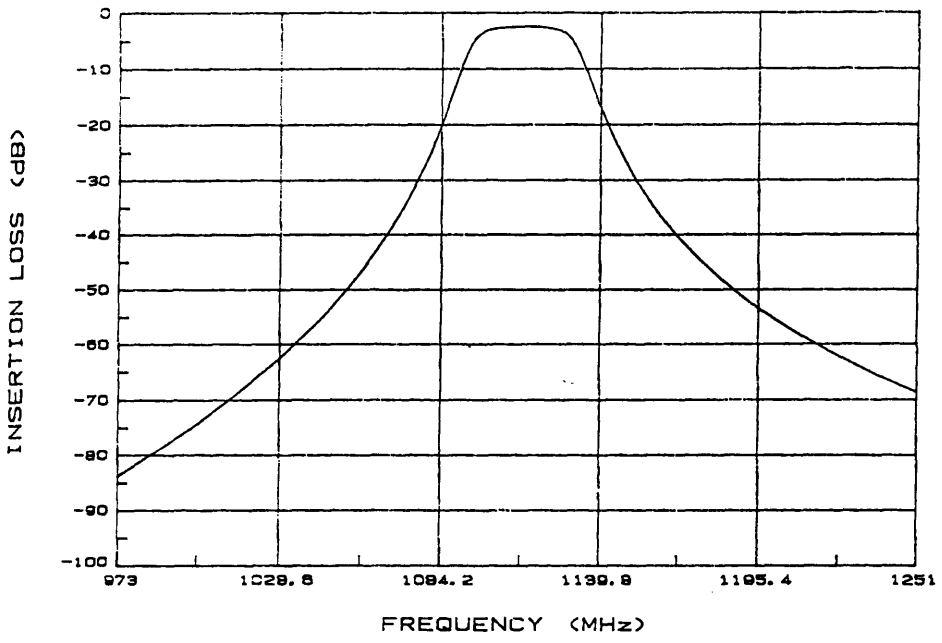
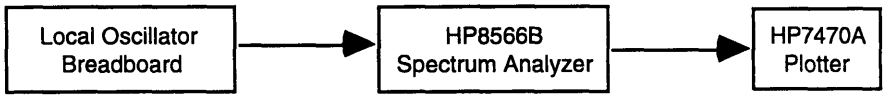


Figure 5.9 Predicted Response of 1-GHz Dielectric Block Filter

Therefore, the higher-than-projected second stage spurious is not expected to be a real effect. With the insertion of the final 1-GHz dielectric block filter, the first stage seventh harmonic would be sufficiently attenuated such that second stage spurious will be rejected to predicted levels.

Final Results

The test measurement setup for characterizing the local oscillator breadboard is shown in Figure 5.10. The local oscillator chain, consisting of components depicted in Figures 5.1, 5.2, and 5.3, followed. RF output was monitored using a spectrum analyzer. Since the driver amplifier was operating linearly, return loss of the multiplier chain may be measured by probing only the driver amplifier. Phase noise measurement techniques are well documented in [20], [53], and [54]. The final output of the LO chain is shown in Figure 5.11.



All +5V supplied by HP6234A Dual Output Power Supply

Figure 5.10 Test Measurement Setup for Local Oscillator Breadboard

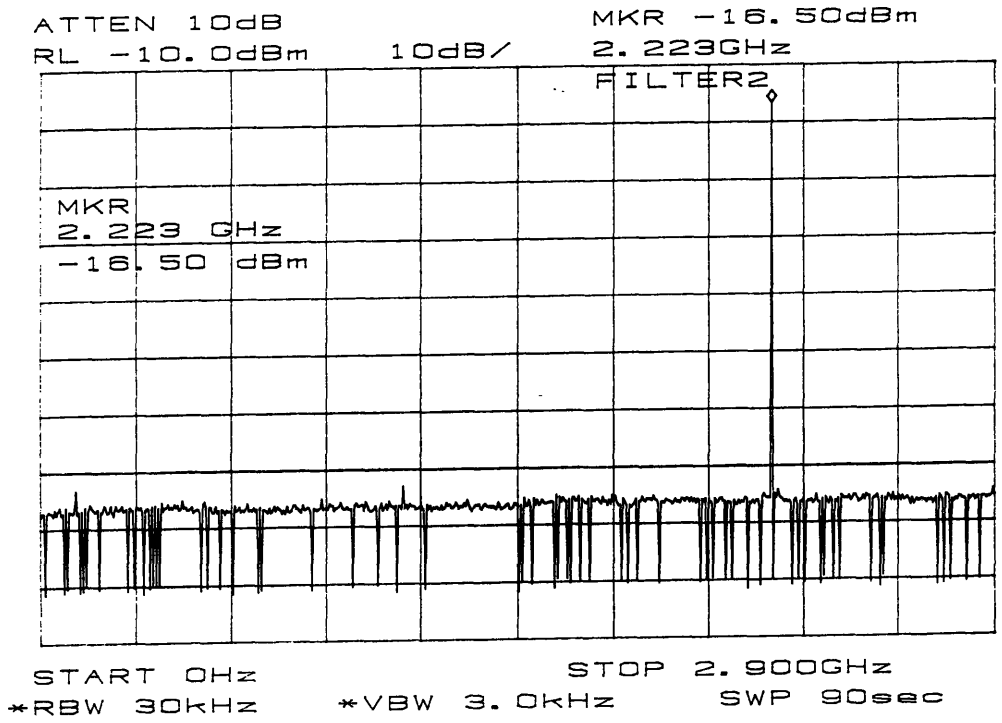


Figure 5.11 Measured LO Output

5.4 Comparison with Initial Specifications

Table 5.1 compares the measured performance of the local oscillator breadboard with the initial specifications.

Parameter	Requirement	Measured Performance
Frequency	2.225GHz	2.225GHz
Output power	+13dBm	+11dBm
Phase noise spectral density		(at +25°C)
Offset from carrier:		
10Hz	-50dBc/Hz	-52dBc/Hz
100Hz	-79dBc/Hz	-81dBc/Hz
1kHz	-98dBc/Hz	-99dBc/Hz
2kHz	-101dBc/Hz	-105dBc/Hz
100kHz	-111dBc/Hz	-114dBc/Hz
1MHz and above	-111dBc/Hz	-123dBc/Hz
Spurious output		
Within f_0±575MHz	-73dBc	< -86dBc
Harmonics of f_0	-40dBc	< -86dBc
Return loss	16dB	17dB

Table 5.1 Comparison of Experimental LO Results with Specifications

The experimental results demonstrated a local oscillator breadboard which meets all major specifications. Spurious performance significantly exceeded the requirement (by more than 13dB). Phase noise performance was on par with the requirements, as was return loss. The 2dB discrepancy in output power may be compensated by adjusting attenuator values throughout the multiplier chain. Power and frequency stability characteristics will be confirmed by extensive environmental testing in the future.

When the breadboard is integrated into a printed circuit board (PCB) form, some performance figures may be expected to deteriorate. In breadboarding, the usage of separately packaged, connectorized components keep power levels and frequencies well isolated. However, in a PCB implementation, the closer proximity of components will likely cause

isolation problems. Spurious from the initial multiplier stage may couple directly to the output of the multiplier chain. Such problems may be avoided through a straight input-output layout, use of metal shielding, and separation of ground planes.

Chapter 6
Conclusions

A 6/4-GHz C-band receiver front end was analyzed, with the purpose of significantly reducing the subsystem size while meeting or exceeding the performance specifications. Specifications for receiver components were developed such that the overall receiver subsystem would comply with its performance specifications. Detailed spurious analysis was performed for the downconversion unit in order to complete the requirement specification for the local oscillator and the IF filters. An experimental local oscillator was subsequently designed and realized. The local oscillator efforts entailed system design, implementation of comb generators, and design and implementation of filters.

The local oscillator design used a low-noise, high-frequency crystal oscillator, the multiplier chain concept, and a tunable amplifier comb output to realize a reliable, high-performing LO sub-system. It used a minimum amount of hardware compared to LO designs for previous C-band receivers. Different components in the multiplier chain utilized a variety of technologies, including lumped elements, MIC and MMIC components, in order to achieve overall development goals of small size and mass.

The experimental realization of the local oscillator showed good agreement with the design goals, in terms of spurious performance, phase noise levels, and output power. It has been demonstrated that multiplier stages are crucial to overall LO design. The initial experimental results showed spurious much more significant than expected in the second multiplier

stage comb output. The problem has been traced to substitution of the 1-GHz dielectric block filter with a stepped-digit filter for breadboarding purposes. It can be corrected with insertion of the final 1-GHz dielectric block filter.

The design technique illustrated for the 2225MHz local oscillator may be extended to single-frequency synthesis of other frequencies by modifying the multiplier stages and the reference signal frequency. The technique for optimizing each multiplier stage for the desired multiplication factor was well outlined. Multiplier filtering requirements have been established through analysis.

Computer modeling tools such as *Touchstone*, *Libra*, and *OmniSys* were utilized extensively throughout all aspects of front end design and analysis and local oscillator design. Methodologies have been established for computer-aided system analysis (*OmniSys*, *Libra*), spurious analysis (*Excel*), filter specification (*Excel*), and filter designs (*Touchstone*, *IE3D*). Future design efforts of similar nature may be based upon the same methodologies.

Phase noise is a key area in which potential improvements appear possible. Because the noise floor of the multiplier chain has been empirically shown to be much lower than the phase noise requirements, the local oscillator phase noise performance will be constrained by the TCXO phase noise characteristics. Due to the lack of an oven controlled frequency compensation system, the TCXO achieves substantial size and power consumption advantages. Narrowband crystal filters may be used at appropriate points in the multiplier chain to compensate for the TCXO's marginal phase noise characteristics [20].

In conclusion, this thesis has introduced and followed through a methodology for the design and analysis of a receiver front end. The experimental results on the local oscillator validate the combination of theoretical, empirical, and computer-aided design techniques employed. The extensive evaluation of implementation choices at various stages of the local

oscillator design and the measured performance have demonstrated validity of the design approach.

Appendix A
IF Filtering Requirement Analysis

Signal	Frequency Range: Start Frequency (MHz)	End Frequency (MHz)	Mixer Spurious Output (dBm)	Rejection Needed by Filters (dB)
LO	2225	2225	-40	-70
IF	3500	4200	-50	0
2LO	4450	4450	-42	-68
5LO-RF	4700	5400	-71	-39
RF	5725	6425	-51	-59
3LO	6675	6675	-35	-75
RF+LO	7950	8650	-64	-46
4LO	8900	8900	-53	-57

Note: The above rejection specs will attenuate all spurious to 60dB below carrier.

Appendix B
LO Filtering Requirement Analysis

B.1 Measured First-Stage Harmonic Spectrum Levels

This appendix summarizes the levels of the spurious inputs to the second-stage comb generator (including the main carrier component at 1112.5MHz).

Harmonic	Frequency (MHz)	First-Stage INA Output Harmonic Levels (dBm)	Levels Relative to Carrier (8th Harmonic) (dBc)	First-Stage Filter Rejection (dB)	Levels Relative to Carrier After Filter (dBc)
1	139.0625	3.1	21.2	-45	-23.8
2	278.1250	-11.0	7.1	-45	-37.9
3	417.1875	-9.2	8.9	-45	-36.1
4	556.2500	-11.7	6.4	-45	-38.6
5	695.3125	-22.0	-3.9	-45	-48.9
6	834.3750	-14.7	3.4	-45	-41.6
7	973.4375	-31.8	-13.7	-45	-58.7
8	1112.5000	-18.1	0.0	0	0.0
9	1251.5625	-27.7	-9.6	-45	-54.6
10	1390.6250	-24.2	-6.1	-45	-51.1
11	1529.6875	-26.8	-8.7	-45	-53.7
12	1668.7500	-26.0	-7.9	-45	-52.9
13	1807.8125	-33.8	-15.7	-45	-60.7
14	1946.8750	-30.0	-11.9	-45	-56.9
15	2085.9375	-28.8	-10.7	-45	-55.7
16	2225.0000	-32.1	-14.0	-45	-59.0
17	2364.0625	-30.9	-12.8	-45	-57.8
18	2503.1250	-34.2	-16.1	-45	-61.1
19	2642.1875	-35.8	-17.7	-45	-62.7
20	2781.2500	-37.0	-18.9	-45	-63.9
21	2920.3125	-38.0	-19.9	-45	-64.9

B.2 Predicted Second-Stage Harmonic Combs

This Appendix summarizes the 21 combs generated by the second-stage comb generator in response to its 21 inputs. (Only the first 21 harmonics from the first multiplier stage are considered here; harmonics higher than 21 are ignored due to their low power levels.) The shaded cells indicate the harmonics in the 21 combs which equal to or exceed -85dBc within f_0±575MHz or -52dBc otherwise (giving 12dB margin above the spurious specifications). They will be accumulated in a later worksheet to determine the total power level of the signals at each harmonic frequency.

First-Stage Output Harmonic #	1st Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)	2nd Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)	3rd Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)
1	139.0625	-23.8	278.1250	-37.9	417.1875	-36.1
2	278.1250	-37.9	556.2500	-52	834.3750	-50.2
3	417.1875	-36.1	834.3750	-50.2	1251.5625	-48.4
4	556.2500	-38.6	1112.5000	-52.7	1668.7500	-50.9
5	695.3125	-48.9	1390.6250	-63	2085.9375	-61.2
6	834.3750	-41.6	1668.7500	-55.7	2503.1250	-53.9
7	973.4375	-58.7	1946.8750	-72.8	2920.3125	-71
8	1112.5000	0	2225.0000	-6.4	3337.5000	-14.7
9	1251.5625	-54.6	2503.1250	-61	3754.6875	-69.3
10	1390.6250	-51.1	2781.2500	-57.5	4171.8750	-65.8
11	1529.6875	-53.7	3059.3750	-60.1	4589.0625	-68.4
12	1668.7500	-52.9	3337.5000	-59.3	5006.2500	-67.6
13	1807.8125	-60.7	3615.6250	-67.1	5423.4375	-75.4
14	1946.8750	-56.9	3893.7500	-63.3	5840.6250	-71.6
15	2085.9375	-55.7	4171.8750	-62.1	6257.8125	-70.4
16	2225.0000	-59	4450.0000	-65.4	6675.0000	-73.7
17	2364.0625	-57.8	4728.1250	-64.2	7092.1875	-72.5
18	2503.1250	-61.1	5006.2500	-67.5	7509.3750	-75.8
19	2642.1875	-62.7	5284.3750	-69.1	7926.5625	-77.4
20	2781.2500	-63.9	5562.5000	-70.3	8343.7500	-78.6
21	2920.3125	-64.9	5840.6250	-71.3	8760.9375	-79.6

First-Stage Output Harmonic #	4th Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)	5th Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)	6th Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)
1	556.2500	-38.6	695.3125	-48.9	834.3750	-41.6
2	1112.5000	-52.7	1390.6250	-63	1668.7500	-55.7
3	1668.7500	-50.9	2085.9375	-61.2	2503.1250	-53.9
4	2225.0000	-53.4	2781.2500	-63.7	3337.5000	-56.4
5	2781.2500	-63.7	3476.5625	-74	4171.8750	-66.7
6	3337.5000	-56.4	4171.8750	-66.7	5006.2500	-59.4
7	3893.7500	-73.5	4867.1875	-83.8	5840.6250	-76.5
8	4450.0000	-15.3	5562.5000	-22.1	6675.0000	-29.3
9	5006.2500	-69.9	6257.8125	-76.7	7509.3750	-83.9
10	5562.5000	-66.4	6953.1250	-73.2	8343.7500	-80.4
11	6118.7500	-69	7648.4375	-75.8	9178.1250	-83
12	6675.0000	-68.2	8343.7500	-75	10012.5000	-82.2
13	7231.2500	-76	9039.0625	-82.8	10846.8750	-90
14	7787.5000	-72.2	9734.3750	-79	11681.2500	-86.2
15	8343.7500	-71	10429.6875	-77.8	12515.6250	-85
16	8900.0000	-74.3	11125.0000	-81.1	13350.0000	-88.3
17	9456.2500	-73.1	11820.3125	-79.9	14184.3750	-87.1
18	10012.5000	-76.4	12515.6250	-83.2	15018.7500	-90.4
19	10568.7500	-78	13210.9375	-84.8	15853.1250	-92
20	11125.0000	-79.2	13906.2500	-86	16687.5000	-93.2
21	11681.2500	-80.2	14601.5625	-87	17521.8750	-94.2

First-Stage Output Harmonic #	7th Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)	8th Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)	9th Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)
1	973.4375	-58.7	1112.5000	-45	1251.5625	-54.6
2	1946.8750	-72.8	2225.0000	-59.1	2503.1250	-68.7
3	2920.3125	-71	3337.5000	-57.3	3754.6875	-66.9
4	3893.7500	-73.5	4450.0000	-59.8	5006.2500	-69.4
5	4867.1875	-83.8	5562.5000	-70.1	6257.8125	-79.7
6	5840.6250	-76.5	6675.0000	-62.8	7509.3750	-72.4
7	6814.0625	-93.6	7787.5000	-79.9	8760.9375	-89.5
8	7787.5000	-42	8900.0000	-41.2	10012.5000	-41.2
9	8760.9375	-96.6	10012.5000	-95.8	11264.0625	-95.8
10	9734.3750	-93.1	11125.0000	-92.3	12515.6250	-92.3
11	10707.8125	-95.7	12237.5000	-94.9	13767.1875	-94.9
12	11681.2500	-94.9	13350.0000	-94.1	15018.7500	-94.1
13	12654.6875	-102.7	14462.5000	-101.9	16270.3125	-101.9
14	13628.1250	-98.9	15575.0000	-98.1	17521.8750	-98.1
15	14601.5625	-97.7	16687.5000	-96.9	18773.4375	-96.9
16	15575.0000	-101	17800.0000	-100.2	20025.0000	-100.2
17	16548.4375	-99.8	18912.5000	-99	21276.5625	-99
18	17521.8750	-103.1	20025.0000	-102.3	22528.1250	-102.3
19	18495.3125	-104.7	21137.5000	-103.9	23779.6875	-103.9
20	19468.7500	-105.9	22250.0000	-105.1	25031.2500	-105.1
21	20442.1875	-106.9	23362.5000	-106.1	26282.8125	-106.1

First-Stage Output Harmonic #	10th Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)	11th Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)	12th Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)
1	1390.6250	-51.1	1529.6875	-53.7	1668.7500	-52.9
2	2781.2500	-65.2	3059.3750	-67.8	3337.5000	-67
3	4171.8750	-63.4	4589.0625	-66	5006.2500	-65.2
4	5562.5000	-65.9	6118.7500	-68.5	6675.0000	-67.7
5	6953.1250	-76.2	7648.4375	-78.8	8343.7500	-78
6	8343.7500	-68.9	9178.1250	-71.5	10012.5000	-70.7
7	9734.3750	-86	10707.8125	-88.6	11681.2500	-87.8
8	11125.0000	-41.2	12237.5000	-41.2	13350.0000	-41.2
9	12515.6250	-95.8	13767.1875	-95.8	15018.7500	-95.8
10	13906.2500	-92.3	15296.8750	-92.3	16687.5000	-92.3
11	15296.8750	-94.9	16826.5625	-94.9	18356.2500	-94.9
12	16687.5000	-94.1	18356.2500	-94.1	20025.0000	-94.1
13	18078.1250	-101.9	19885.9375	-101.9	21693.7500	-101.9
14	19468.7500	-98.1	21415.6250	-98.1	23362.5000	-98.1
15	20859.3750	-96.9	22945.3125	-96.9	25031.2500	-96.9
16	22250.0000	-100.2	24475.0000	-100.2	26700.0000	-100.2
17	23640.6250	-99	26004.6875	-99	28368.7500	-99
18	25031.2500	-102.3	27534.3750	-102.3	30037.5000	-102.3
19	26421.8750	-103.9	29064.0625	-103.9	31706.2500	-103.9
20	27812.5000	-105.1	30593.7500	-105.1	33375.0000	-105.1
21	29203.1250	-106.1	32123.4375	-106.1	35043.7500	-106.1

First-Stage Output Harmonic #	13th Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)	14th Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)	15th Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)
1	1807.8125	-53.9	1946.8750	-56.9	2085.9375	-55.7
2	3615.6250	-68	3893.7500	-71	4171.8750	-69.8
3	5423.4375	-66.2	5840.6250	-69.2	6257.8125	-68
4	7231.2500	-68.7	7787.5000	-71.7	8343.7500	-70.5
5	9039.0625	-79	9734.3750	-82	10429.6875	-80.8
6	10846.8750	-71.7	11681.2500	-74.7	12515.6250	-73.5
7	12654.6875	-88.8	13628.1250	-91.8	14601.5625	-90.6
8	14462.5000	-41.2	15575.0000	-41.2	16687.5000	-41.2
9	16270.3125	-95.8	17521.8750	-95.8	18773.4375	-95.8
10	18078.1250	-92.3	19468.7500	-92.3	20859.3750	-92.3
11	19885.9375	-94.9	21415.6250	-94.9	22945.3125	-94.9
12	21693.7500	-94.1	23362.5000	-94.1	25031.2500	-94.1
13	23501.5625	-101.9	25309.3750	-101.9	27117.1875	-101.9
14	25309.3750	-98.1	27256.2500	-98.1	29203.1250	-98.1
15	27117.1875	-96.9	29203.1250	-96.9	31289.0625	-96.9
16	28925.0000	-100.2	31150.0000	-100.2	33375.0000	-100.2
17	30732.8125	-99	33096.8750	-99	35460.9375	-99
18	32540.6250	-102.3	35043.7500	-102.3	37546.8750	-102.3
19	34348.4375	-103.9	36990.6250	-103.9	39632.8125	-103.9
20	36156.2500	-105.1	38937.5000	-105.1	41718.7500	-105.1
21	37964.0625	-106.1	40884.3750	-106.1	43804.6875	-106.1

First-Stage Output Harmonic #	16th Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)	17th Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)	18th Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)
1	2225.0000	-59	2364.0625	-57.8	2503.1250	-61.1
2	4450.0000	-73.1	4728.1250	-71.9	5006.2500	-75.2
3	6675.0000	-71.3	7092.1875	-70.1	7509.3750	-73.4
4	8900.0000	-73.8	9456.2500	-72.6	10012.5000	-75.9
5	11125.0000	-84.1	11820.3125	-82.9	12515.6250	-86.2
6	13350.0000	-76.8	14184.3750	-75.6	15018.7500	-78.9
7	15575.0000	-93.9	16548.4375	-92.7	17521.8750	-96
8	17800.0000	-41.2	18912.5000	-41.2	20025.0000	-41.2
9	20025.0000	-95.8	21276.5625	-95.8	22528.1250	-91.9
10	22250.0000	-92.3	23640.6250	-92.3	25031.2500	-88.4
11	24475.0000	-94.9	26004.6875	-94.9	27534.3750	-91
12	26700.0000	-94.1	28368.7500	-94.1	30037.5000	-90.2
13	28925.0000	-101.9	30732.8125	-101.9	32540.6250	-98
14	31150.0000	-98.1	33096.8750	-98.1	35043.7500	-94.2
15	33375.0000	-96.9	35460.9375	-96.9	37546.8750	-93
16	35600.0000	-100.2	37825.0000	-100.2	40050.0000	-96.3
17	37825.0000	-99	40189.0625	-99	42553.1250	-95.1
18	40050.0000	-102.3	42553.1250	-102.3	45056.2500	-98.4
19	42275.0000	-103.9	44917.1875	-103.9	47559.3750	-100
20	44500.0000	-105.1	47281.2500	-105.1	50062.5000	-101.2
21	46725.0000	-106.1	49645.3125	-106.1	52565.6250	-102.2

First-Stage Output Harmonic #	19th Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)	20th Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)	21st Harmonic in 2nd-Stage Comb (MHz)	Level Relative to Carrier (dBc)
1	2642.1875	-62.7	2781.2500	-63.9	2920.3125	-64.9
2	5284.3750	-76.8	5562.5000	-78	5840.6250	-79
3	7926.5625	-75	8343.7500	-76.2	8760.9375	-77.2
4	10568.7500	-77.5	11125.0000	-78.7	11681.2500	-79.7
5	13210.9375	-87.8	13906.2500	-89	14601.5625	-90
6	15853.1250	-80.5	16687.5000	-81.7	17521.8750	-82.7
7	18495.3125	-97.6	19468.7500	-98.8	20442.1875	-99.8
8	21137.5000	-41.2	22250.0000	-41.2	23362.5000	-41.2
9	23779.6875	-93.5	25031.2500	-94.7	26282.8125	-95.7
10	26421.8750	-90	27812.5000	-91.2	29203.1250	-92.2
11	29064.0625	-92.6	30593.7500	-93.8	32123.4375	-94.8
12	31706.2500	-91.8	33375.0000	-93	35043.7500	-94
13	34348.4375	-99.6	36156.2500	-100.8	37964.0625	-101.8
14	36990.6250	-95.8	38937.5000	-97	40884.3750	-98
15	39632.8125	-94.6	41718.7500	-95.8	43804.6875	-96.8
16	42275.0000	-97.9	44500.0000	-99.1	46725.0000	-100.1
17	44917.1875	-96.7	47281.2500	-97.9	49645.3125	-98.9
18	47559.3750	-100	50062.5000	-101.2	52565.6250	-102.2
19	50201.5625	-101.6	52843.7500	-102.8	55485.9375	-103.8
20	52843.7500	-102.8	55625.0000	-104	58406.2500	-105
21	55485.9375	-103.8	58406.2500	-105	61326.5625	-106

B.3 Second-Stage Filter Specification

Harmonic Frequency (MHz)	Levels of Harmonics at Specified Frequency (dBc)						Accumulated Harmonic Levels Relative to Carrier @ 2225MHz (dBc)	Rejection Needed by 2nd-Stage Filter (dB)
139.0625	-23.8						-23.800	-22.600
278.1250	-37.9	-37.9					-34.890	-11.510
417.1875	-36.1	-36.1					-33.090	-13.310
556.2500	-38.6	-38.6	-52.0				-35.492	-10.908
695.3125	-48.9	-48.9					-45.890	-0.510
834.3750	-41.6	-41.6	-50.2	-50.2			-38.028	-8.372
1112.5000	0.0	-45.0					0.000	-46.400
1251.5625	-48.4						-48.400	2.000
1390.6250	-51.1	-51.1					-48.090	1.690
1529.6875	-53.7	-53.7					-50.690	-28.710
1668.7500	-52.9	-55.7	-50.9	-50.9	-55.7	-52.9	-44.963	-34.437
1807.8125	-60.7	-53.9					-53.076	-26.324
1946.8750	-56.9	-72.8	-72.8	-56.9			-53.779	-25.621
2085.9375	-55.7	-61.2	-61.2	-55.7			-51.611	-27.789
2225.0000	-59.0	-6.4	-53.4	-59.1	-59.0		-6.400	0.000
2364.0625	-57.8	-57.8					-54.790	-24.610
2503.1250	-61.0	-53.9	-53.9	-68.7	-61.0	-61.1	-49.728	-29.672
2642.1875	-62.7	-62.7					-59.690	-19.710
2781.2500	-57.5	-63.7	-63.7	-65.2	-63.9	-63.9	-54.262	-25.138
2920.3125	-71.0	-71.0	-64.9	-64.9			-60.936	-18.464
3337.5000	-14.7						-14.700	-31.700
4450.0000	-15.3						-15.300	-31.100
5562.5000	-22.1						-22.100	-24.300
6675.0000	-29.3						-29.300	-17.100
7787.5000	-42.0						-42.000	-4.400
8900.0000	-41.2						-41.200	-5.200
10012.5000	-41.2						-41.200	-5.200
11125.0000	-41.2						-41.200	-5.200
12237.5000	-41.2						-41.200	-5.200
13350.0000	-41.2						-41.200	-5.200
14462.5000	-41.2						-41.200	-5.200
15575.0000	-41.2						-41.200	-5.200
16687.5000	-41.2						-41.200	-5.200
17800.0000	-41.2						-41.200	-5.200
18912.5000	-41.2						-41.200	-5.200
20025.0000	-41.2						-41.200	-5.200
21137.5000	-41.2						-41.200	-5.200
22250.0000	-41.2						-41.200	-5.200
23362.5000	-41.2						-41.200	-5.200

Appendix C
Calculation of Minimum Filter Order

Variable	Definition
f_1	lower bound of passband
f_2	upper bound of passband
α_p	passband ripple
f_{s1}	lower rejection point
f_{s2}	upper rejection point
α_s	rejection at f_{s1} and f_{s2}
n	order of lowpass prototype

$$k = \frac{f_2 - f_1}{f_{s2} - f_{s1}}$$

$$k_1 = \left(\frac{10^{\frac{\alpha_p}{10}} - 1}{10^{\frac{\alpha_s}{10}} - 1} \right)^{\frac{1}{2}}$$

$$n \geq \frac{\cosh^{-1}\left(\frac{1}{k_1}\right)}{\cosh^{-1}\left(\frac{1}{k}\right)}$$

Appendix D
Interdigital Filter Design

N = order of lowpass prototype g_i = lowpass prototype element values w = fractional bandwidth of filter R = source and load impedance Z_S = single-strip impedance of resonators f_0 = center frequency of filter	$\theta_1 = \frac{\pi}{2}\left(1 - \frac{\omega}{2}\right)$ $h = \frac{1}{Z_s \tan\theta_1}$
For j = 1 and N-1: $J_{j,j+1} = \frac{h}{\sqrt{g_j g_{j+1}}}$ $Y_{j,j+1} = J_{j,j+1}\sin\theta_1$ $Z_{oe1} = \frac{Z_s}{1 - y_{12}Z_s}$ $Z_{oeN-1} = \frac{Z_s}{1 - y_{N-1,N}Z_s}$ $Z_{oo1} = \frac{Z_s}{1 + y_{12}Z_s}$ $Z_{ooN-1} = \frac{Z_s}{1 + y_{N-1,N}Z_s}$	For j = 2 to N-2: $Z_{oej} = \frac{1}{\frac{2}{Z_s} - \frac{1}{Z_{oej-1}} - y_{j,j+1} - y_{j-1,j}}$ $Z_{ooj} = \frac{1}{2y_{j,j+1} + \frac{1}{Z_{oej}}}$

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