The Physics and Technology of the InAlAs/n^+-InP Heterostructure Field-Effect Transistor

by

David Ross Greenberg

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Abstract

To meet the growing demand for a high-power Heterostructure Field-Effect Transistor (HFET) family based on InP, we have developed and characterized a circuit-capable InAlAs/n$^+$-InP HFET technology employing InP not merely as a *substrate* but also *epitaxially* as the channel and as an etch-stopper in a selectively-recessed gate scheme. This thesis presents an experimental assessment of the benefits and drawbacks of exploiting InP in both roles.

We find that the combination of an InP etch-stopper beneath an n$^+$-InGaAs cap reduces the small-signal parasitic resistances significantly while simultaneously maintaining a tight threshold voltage distribution. We uncover a new mechanism in which the cap conducts *in parallel* with the channel at sufficiently high currents, leading to a rapid reduction in these resistances with increasing current. As a result, we achieve a peak transconductance of 200 mS/mm and a maximum drain current of 430 mA/mm for 0.8 μm gate-length devices.

We also find that the wide-bandgap n$^+$-InP channel eliminates both impact ionization and real-space transfer, leading to very low gate currents and to a drain-source breakdown voltage that *increases* from an off-state value of 10 V as the device is turned on. As a tradeoff, we find that the effective electron velocity approaches the InP saturation velocity of about 1.05×10^7 cm/s for gate lengths below 1.6 μm rather than achieving the material's higher peak velocity. We attribute this to the impact of doping on both the peak velocity and on the conditions necessary for velocity overshoot to take place. Our results indicate that the InAlAs/n$^+$-InP MIDFET is well-suited to applications demanding high drain current, large breakdown voltage, small gate current, low output conductance, and tight threshold voltage uniformity, and for which a moderate frequency response is an acceptable tradeoff.

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Title: Associate Professor of Electrical Engineering

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In many senses, this project began long before my coming to MIT, and I give my love and thanks to my parents and sister for all of their support and encouragement. My friends have been a vital part of my moral support system during these years as well. Though I cannot possibly list everyone here, I extend my appreciation to all of them.

Professionally, I thank first and foremost my advisor and mentor Prof. Jesús A. del Alamo, who not only encouraged and guided me with enthusiastic and insightful advice, but also set an excellent example for how to balance all the many facets of good research. As my thesis committee members, Prof. Charles Sodini and Prof. Clifton Fonstad have also provided excellent advice on presenting my work in its best light.

I also thank Dr. Rajaram Bhat of Bellcore, Redbank, whose high-quality heterostructures were absolutely key to this work. My thanks as well to Peter R. Nuytkens both for his collaboration with me on the resonator appearing in the thesis as well as for his and generous loan of equipment and help for laying out the mask set. Richard Perilli and Tim McClure of the MTCF, as well as James Carter and Mark Mondol of the NNF, were also vital parts of the chain, helping the device processing go smoothly. And thanks to Prof. Sheila Prasad, Prof. Clifton Fonstad, and Dr. Bahman Meskoob for the use of and training on the HP8510B network analyzer which played such a large role in my work.

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Chapter 1:

Introduction

An explosion in the market for high-bandwidth telecommunications applications over the past several years has fueled a growing demand for the development of a family of electronics based on indium phosphide (InP). This demand has been motivated both by the possibility of integrating InP electronics with 1.33 μm and 1.5 μm optical devices as well as by the excellent millimeter-wave performance results reported to date for several types of InP-based Heterostructure Field-Effect Transistors (HFET's). Many of the key applications for an InP-based electronics family, including laser drivers and photodiode receivers for optical communications systems and microwave amplifiers for wireless systems, require devices with not only high frequency response but also the capability of handling large currents and voltages. In addition, receiver applications require very low gate current (I_G) in order to avoid degrading sensitivity through the introduction of excess input noise [1].

Of the several technologies which may be used to realize InP-based HFET's, the majority of research thus far has focused on the InAlAs/InGaAs material system because of the high electron mobility of InGaAs, the low resistance ohmic contacts which can be made to this material, and the excellent electron confinement provided by the InAlAs gate barrier layer. All of these features have contributed to outstanding high-frequency performance. The InAlAs/InGaAs Modulation-Doped FET (MODFET) has, for example, demonstrated values of current-gain cutoff frequency (f_T) of 250 GHz for devices with 0.07 μm gate length (L_g) and with lattice-matched $In_{0.53}Ga_{0.47}As$ channels and over 300 GHz for devices with high InAs mole-fraction pseudomorphic channels [2]. Schemes for integrating InAlAs/InGaAs HFET's with optical detectors without performance degradation have been proposed and successfully tested recently as well, emphasizing the potential of this InP-based optoelec-

tronics technology [3, 4].

Despite their high-frequency merits, however, InAlAs/InGaAs HFET's are quite vulnerable to impact ionization in the narrow-bandgap channel as well as to other hot-electron effects such as real-space transfer [5]. These effects occur even under normal biasing conditions and worsen with increasing InAs mole fraction [6]. In addition to lowering the drain-source breakdown voltage (BV_{DS}) these phenomena degrade voltage gain (a_v) through increased output conductance (g_d) and generate excess I_G from escaping ionized holes [5, 7, 8, 9]. Several studies have explored techniques for reducing these deleterious effects, including engineering the cap layer over the drain-gate gap to lower the peak drain electric field [10] and employing a strained gate-barrier layer to reduce the thermionic field emission of gate electrons into the channel which can produce impact ionization [7]. Others have focused on methods for reducing the consequences of impact ionization, including inserting an additional pseudomorphic layer between gate and channel to block multiplication holes and thus lower excess I_G [11, 12]. The success of these methods and their associated performance tradeoffs are still unclear, however.

Heterostructures incorporating InP itself as *active* layers rather than merely as a *mechanical* substrate offer a very attractive alternative approach for a device technology targeted at high-power and low input-noise telecommunications applications. The advantages promised by InP, summarized in Table 1.1, are two-fold. *Electronically*, the wide bandgap material enjoys an exceptional breakdown field, making it potentially far more resistant to impact ionization compared with InGaAs. In addition, although InP has a smaller electron mobility compared with InGaAs at low electric fields, it shows a higher peak electron velocity over the wide range of moderate to high electric fields (5 to 100 kV/cm) most relevant to modern submicron devices [13]. This behavior is illustrated in Figure 1.1 [15]. Both electronic properties combine to suggest exceptional high-frequency and high-power capabilities. *Chemically*, highly selective etchants also exist for both InGaAs and InAlAs over InP, making InP an

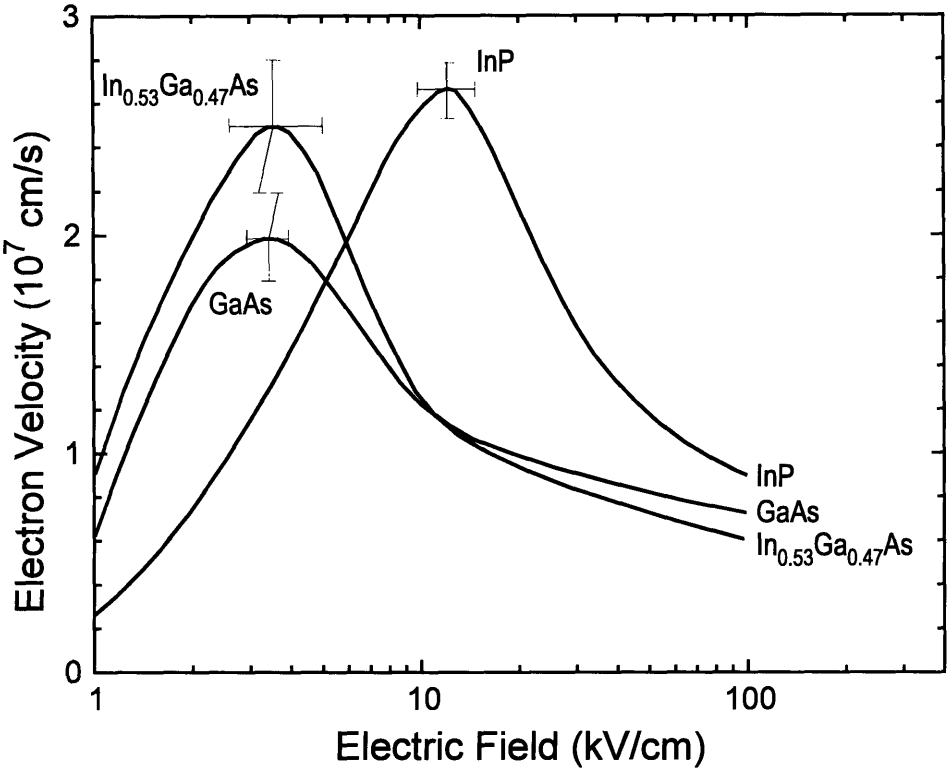

Figure 1.1: Electron velocity vs. electric field curve comparing InP with both GaAs and $In_{0.53}Ga_{0.47}As$ (error bars indicate variation among reported results).

ideal *etch-stop* layer, for example. A robust etch-stop layer is key to combining the use of a recessed-cap technology for low source resistance with the very tight threshold voltage (V_T) distribution needed for volume manufacturing of high-density circuits.

The promised advantages of an InP-channel HFET technology are supported, in fact, by the performance of several other classes of InP-channel FET's reported to date. One well-known device design, the Metal-Semiconductor FET (MESFET) has been unsuccessful on InP thus far [16] due to its low Schottky barrier height ($\Phi_b < 0.5$ eV) [17]. However, the deposited dielectric Metal-Insulator-Semiconductor FET (MISFET) has achieved higher values for power density, power added efficiency, and BV_{DS} compared with any other existing FET, though at the expense of poor reproducibility, large V_T variation, low transconductance (g_m), and significant drain-current (I_D) shift over time [18, 19, 20, 21]. The Junction FET (JFET) has also

Table 1.1: Key InP material parameters (300 K), with GaAs and $In_{0.53}Ga_{0.47}As$ values given for comparison.

Property (300 K)	Material		
	InP	$In_{0.53}Ga_{0.47}As$	GaAs
Bandgap (eV)	1.34	0.75	1.42
Electron effective mass	0.077	0.041	0.067
low-field electron mobility ($cm^2/V{\cdot}s$)	4800	11000	8100
Peak electron velocity (10^7 cm/s)	~2.6	~2.5	~2.0
Electric field at peak velocity (kV/cm)	~12	~3.5	~3.5
Electric field range for velocity > 80% of peak (kV/cm)	~20	~5	~5
Γ-L separation (eV)	0.83	0.75	0.32
Electric field for electron ionization coefficient $\alpha = 10^4$ cm^{-1} (10^5 V/cm)	5	2.3	4
Thermal conductivity (W/cm·K)	0.8	0.05	0.46
Conduction-band discontinuity to common gate-barrier (eV)	$In_{0.52}Al_{0.48}As$: 0.38	$In_{0.52}Al_{0.48}As$: 0.50	$Al_{0.38}Ga_{0.62}As$: 0.30

demonstrated excellent power handling, together with many of the same disadvantages as the MISFET [22, 23]. Despite the fatal drawbacks related to their respective gate-barrier technologies, both the MISFET and JFET clearly demonstrate the potential of using an InP channel.

Most recent InP-channel devices take advantage of the much higher quality heterointerface between channel and gate-barrier possible only in an HFET design. While a highly-mismatched AlGaAs/InP HFET has been fabricated with moderate success [24, 25], the most promising work thus far has focused on the InAlAs/InP HFET in which a lattice-matched or pseudomorphic InAlAs layer acts as the gate bar-

rier [26]. InAlAs/InP MODFET's have achieved values for f_T exceeding 90 GHz at L_g= 0.32 μm, with f_{max} reaching 145 GHz for an L_g= 0.33 μm device [27, 28]. At 30 GHz, similar devices have achieved maximum stable gains of 12 dB, power densities of 1.45 W/mm, and power added efficiencies of 24% [29], while devices with longer gate lengths ($L_g > 1.5$ μm) have shown values for BV_{DS} exceeding 15 V [30]. In addition to the InAlAs/InP MODFET, an InAlAs/n-InP HFET [31] and an InAlAs/InP delta-doped-channel HFET [32] have been reported as well, with similarly interesting results.

The excellent combination of high g_m, I_D, power density, and BV_{DS} achieved in the InAlAs/InP HFET clearly points out the need to study the material system in considerably more detail, well beyond the essentially proof-of-concept studies performed thus far. In particular, no one has yet conducted a comprehensive assessment of the InAlAs/InP HFET so as to allow the device to be compared judiciously against other reported HFET designs on InP. Such a comparison should address three distinct areas, corresponding to each of the three key potential benefits offered by InP as an active device layer.

First, it should explore the chemical selective-etch properties of InP used in combination with InAlAs and InGaAs. Most importantly, this evaluation must consider the efficacy of using InP as an etch-stop layer in combination with a recessed-cap process to reduce source resistance while maintaining a uniform V_T distribution across the wafer. Next, a complete comparison should look at the ability of the wide-bandgap InP-channel to suppress impact ionization as well as other hot electron effects such as real-space transfer. In this area, InP-channel HFET's might be expected to hold an advantage over InGaAs-based devices and show reduced I_G, lower g_d, and improved BV_{DS}. Finally, such a study must consider electron transport in the InP-channel and its impact on the device's frequency response as L_g is scaled down, an area in which InGaAs-based devices have traditionally excelled. Understanding each of these issues is key to allowing device designers to choose the optimal material system for a given

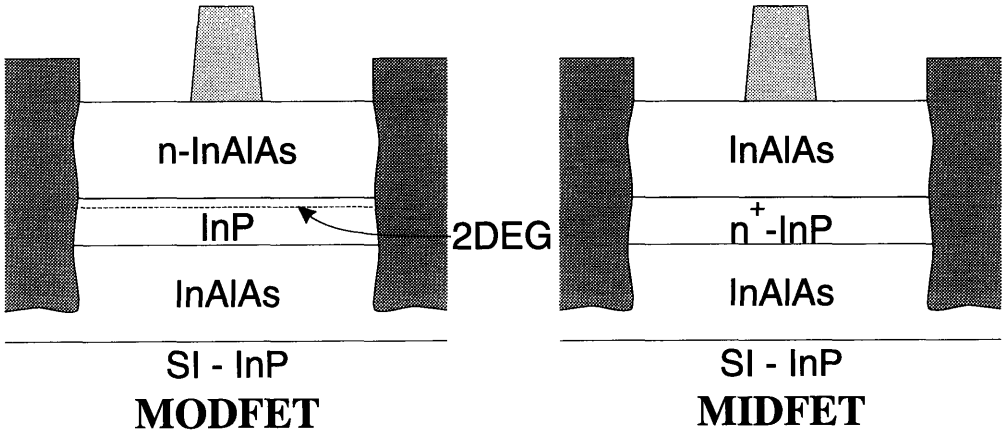

Figure 1.2: A schematic cross-section comparison between the MODFET and the MIDFET in the InAlAs/InP material system (layers are undoped unless otherwise stated).

application.

This thesis presents a comprehensive study of each of these issues and their effect on the performance of submicron InP-channel HFET's, using the InAlAs/n^+-InP Metal-Insulator-Doped-Channel FET (MIDFET) as a vehicle. Studies in a variety of material systems over the past few years have demonstrated that the MIDFET can meet or surpass the more popular MODFET design in many key areas of device performance [33, 34, 35, 36, 37]. Both the MODFET and the MIDFET consist of a thin epitaxial channel layer separated from the gate metal by a lattice-matched or pseudomorphic wider bandgap semiconductor layer. However, as illustrated in Figure 1.2, the two structures differ in the location of the doping which must be introduced to control V_T.

In the MODFET, electrons transfer from donors placed in the gate-barrier layer into an undoped channel. While this configuration leads to a very high channel mobility, the existence of donors in the gate-barrier also leads to a number of deleterious effects which detract from its suitability for high-power, low-input noise applications. These effects include a reduced effective gate-barrier height which increases I_G and reduces BV_{DS} [8], frequency dispersion in figures of merit such as g_m and g_d [38], and

parallel MESFET formation in the gate barrier [39] which brings down g_m, f_T, and f_{max} at relatively low gate-source voltage (V_{GS}) and thus reduces maximum drain current ($I_{D,MAX}$) and the useful V_{GS} swing of the device.

In contrast, the MIDFET heterostructure is grown with an undoped gate-barrier layer and a thin, heavily-doped channel. These features avoid many of the drawbacks that plague the MODFET, leading to reduced I_G, high BV_{DS}, and values of g_m, f_T, and f_{max} that remain high over a very broad V_{GS}. The broad g_m plateau further results in high linearity in I_D vs. V_{GS} and excellent values for both $I_{D,MAX}$ and electron sheet density (n_s). These features are well-suited to a variety of modern telecommunications applications demanding high currents and voltages.

Although the presence of doping in the MIDFET channel does degrade electron mobility, several studies have indicated that ionized impurity scattering has a much smaller effect on the $\sim 1 \times 10^7$ cm/s high-field electron saturation velocity (v_{sat}) [40, 41]. Still more important for the high-frequency performance of submicron devices is the behavior of the peak electron velocity. Studies on bulk material do find that peak velocity degrades with doping, eventually resulting in a velocity-field curve which rises monotonically toward v_{sat} [41]. As device gate lengths begin to drop below $\sim$1 μm, however, evidence of nonstationary transport emerges, with device behavior beginning to reflect electron velocities much higher than predicted solely on basis of bulk material properties. Indeed, MIDFET's in a variety of material systems, including AlGaAs/GaAs [33], AlGaAs/InGaAs [34], and InAlAs/InGaAs [36, 37], have demonstrated high-frequency performance consistent with electron velocities reaching 1.5-2 $\times 10^7$ cm/s, clearly beyond v_{sat}. These results suggest the possibility for similar behavior in n^+-InPchannel HFET's, making it well worthwhile to explore these devices for high-frequency power applications and to examine their transport properties in detail.

The first phase of our study, described in Chapter 2, is the development of an InAlAs/n^+-InP MIDFET technology consisting of heterostructure design, fabrication

process, and mask layout. Our device structure features both an InP channel and an InP etch-stop layer beneath an n^+-$In_{0.53}Ga_{0.47}As$ cap, requiring that we develop appropriate selective and non-selective etch technology for both cap recessing and mesa isolation. This structure is processed in a two-metal level technology with dielectric-assisted lift-off (DALO) patterning capable of producing both high-yield circuits as well as high-performance, submicron discrete devices. Our mask layout includes two separate arrays of devices in various gate lengths and orientations for both low-frequency and microwave probing, supplemented with test structures for characterizing selected process parameters and extracting the values of key device parasitics. The chapter concludes by describing potential improvements to the device technology for future runs, including the development of a novel recessed-ohmic-contact scheme for dramatically reducing the ohmic contact resistance.

Next, we describe the basic device characteristics for our MIDFET technology in Chapter 3. This chapter also develops a small-signal equivalent circuit model and extraction procedure for our devices designed to be accurate enough to foster physical insight while remaining simple enough for rapid automated model parameter extraction over a wide range of biasing conditions.

Our assessment of the InAlAs/InP system is divided between the next two sections, Chapters 4 and 5. Chapter 4 focuses on the use of InP as an etch-stop layer in conjuction with an n^+-InGaAs cap, examining the threshold voltage control which may be achieved as well as exploring the physics of current conduction through the cap structure. Chapter 5 focuses on performance issues related to the InP channel. In particular, we consider the issue of impact ionization and real space transfer and their effect on breakdown voltage, gate current, output conductance, and voltage gain. In addition, we examine electron transport in the device by profiling velocity-dependent small-signal model parameters as a function of both V_{GS} and L_g.

After considering individual devices, we demonstrate the circuit potential of the InAlAs/n^+-InP MIDFET technology in Chapter 6. In this chapter, we describe the

performance of a monolithic, voltage-tunable resonator designed by Peter R. Nuytkens [42] capable of operating at almost 8 GHz using L_g= 1 μm devices.

We offer our conclusions in Chapter 7, including suggestions for further work, followed by two appendices listing our complete process flow as well as the code and brief documentation of BANDSOLV, a one-dimensional heterostructure Poisson solver used to aid in our device design and in the device analysis presented in this work.

Chapter 2:

Device Technology

As a vehicle for studying the InAlAs/n^+-InP MIDFET, we have developed a technology consisting of a heterostructure design, fabrication process, and mask layout. This technology is a judicious tradeoff among several key issues, including achieving high performance, reducing the chance of process failure, minimizing variability in the values of parasitic elements and process parameters, and keeping the process within campus facilities for rapid turnaround time.

A key feature of our process is a selectively-etched recessed-gate, which requires that the heterostructure be designed in advance to include an InP-etch stop layer beneath an n^+-InGaAs cap. Compared with non-self-aligned techniques, recessed-gate technology significantly reduces parasitic source and drain resistance, which are know to degrade figures of merit such as g_m, f_T, and f_{max}, particularly at high I_D [43, 44]. As we shall explore in detail later in this chapter, the selective-etch properties of InGaAs on InP allow us to etch the cap both vertically to a precise depth as well as laterally to a desired gate-cap separation. This results in a tight threshold voltage distribution and excellent breakdown voltage without the need for less exact and more difficult to manufacture methods such as careful timing or iterative I_D-monitoring.

We have also developed a dielectric-assisted liftoff (DALO) process in the course of this thesis. DALO permits optical photolithography to define metal features down to 0.6 μm for good high-frequency performance, while maintaining excellent yield and eliminating the line-width variation and jagged edges that plague alternative techniques such as chlorobenzene soaks.

Our resulting process is a five-mask, two-layer-metal process. The first metal layer is used to form gates, interconnects, and lower capacitor plates, while the second

layer forms additional interconnects, probe/bond pads, and upper capacitor plates. Combined with the use of mesa-resistor technology, this process is capable of yielding circuits of moderate complexity and yet is well-suited to high-frequency, high-power applications and sufficiently reproducible to allow the study of device physics in a well-controlled manner.

After beginning this chapter with a description of our heterostructure design, we present the flow of our fabrication process followed by a discussion of two key areas, etch technology, and DALO patterning, that required particular development. We next provide an overview of our mask set as well as a characterization of the important parasitic resistances inherent to our process using a set of test structure included for this purpose. Our characterization suggests a novel recessed-ohmic-contact scheme for reducing contact resistance to the channel, which we describe and demonstrate as a contribution toward improving future device runs.

2.1 Heterostructure Design

Figure 2.1 shows a typical MIDFET heterostructure used in this work, grown by metallorganic chemical vapor deposition (MOCVD) courtesy of Rajaram Bhat at Bellcore (Red Bank, NJ). From top to bottom, the design consists of a 500 Å n^+-$In_{0.53}Ga_{0.47}As$ cap ($N_D = 1 \times 10^{19}$ cm^{-3}), a 50 Å undoped InP etch-stopper, a 250 Å $In_{0.52}Al_{0.48}As$ gate-barrier, a 100 Å InP channel ($N_D = 5 \times 10^{18}$ cm^{-3}), a 100 Å undoped InP subchannel, and a 1000 Å $In_{0.52}Al_{0.48}As$ electron-confinement / buffer layer, all grown upon a semi-insulating InP substrate. We note that InP epitaxial layers appear twice in this structure: as an etch-stopper beneath the n^+-$In_{0.53}Ga_{0.47}As$ cap, forming the basis for our recessed-gate, and as the channel / subchannel layer. We later explore the consequences of using InP in each of these roles. The undoped subchannel region is included to separate the active region of the device from the potentially poor inverted InP/InAlAs interface.

500 Å	n^+-$In_{0.53}Ga_{0.47}As$	$N_D = 1 \times 10^{19}$ cm^{-3}
50 Å	InP	
250 Å	$In_{0.52}Al_{0.48}As$	
100 Å	n^+-InP	$N_D = 5 \times 10^{18}$ cm^{-3}
100 Å	InP	
1000 Å	$In_{0.52}Al_{0.48}As$	
	S.I. InP Substrate	

Figure 2.1: Heterostructure design for the InAlAs/n^+-InP MIDFET.

Considering the region beneath the gate of a completed MIDFET in which the cap has been etched away, the three most important design criteria for the heterostructure are the gate-barrier and channel thicknesses as well as the channel doping. We designed the gate-barrier to be as thin as possible for high g_m, limited by excessive tunneling and thermionic field emission through the layer and by excessive channel depletion from Fermi-level pinning in the exposed parasitic source and drain regions within the gate-recess well. The channel was also designed to be thin for high device linearity, yet thick enough to allow an acceptable contact resistance (R_c) as well as to prevent noticeable quantization and the consequent reduction in electron confinement. Channel doping was set as high as possible in order to minimize the sheet resistance of the parasitic source and drain regions, consistent with the grower's availability of accurate calibration data and experience in obtaining a high-quality layer. Further notes exploring the impact of tuning each of these heterostructure parameters in a variety of similar device designs may be found in Refs. [7, 35, 36, 37, 43, 46, 55, 61].

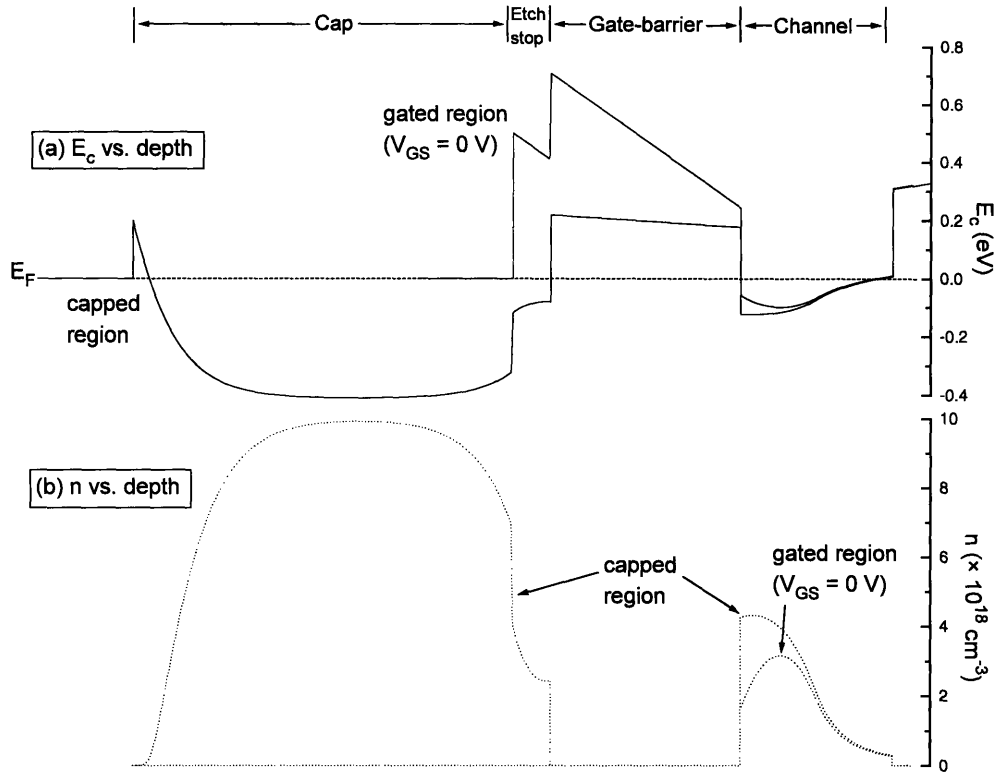

Figure 2.2: BANDSOLV simulated (a) conduction band and (b) electron density vs. depth in the InAlAs/n^+-InP MIDFET for the gated, uncapped (V_{GS}= 0 V) and extrinsic, capped regions.

Three additional design parameters in the extrinsic or capped region of our device are the choice of material, thickness, and doping for the cap layer. We selected $In_{0.53}Ga_{0.47}As$ for this layer, doped as heavily as possible, in order to yield a low sheet resistance (R_{sh}) and to achieve the high Fermi-level with respect to the underlying InP-channel conduction-band edge required for inducing significant charge in the channel. For the same reasons, we made the cap thick as well, constrained to keep the overall heterostructure thickness to around 2000 Å for good metal step coverage and to limit the distance between surface and channel for good ohmic contact penetration.

The dimensions and doping levels of the key layers were tuned with the help of BANDSOLV, a one-dimensional heterostructure Poisson solver written for the thesis and described in Appendix B. Fig. 2.2 shows the resulting simulated conduction band

and electron density profiles for both the gated, uncapped region of the device (at V_{GS}= 0 V) as well as for the extrinsic capped region. We note the effectiveness of the cap in screening the surface Fermi level pinning and in inducing additional charge in the channel. We also note the large electron concentration in the cap itself, key to obtaining a low R_{sh} in this layer.

2.2 Fabrication

Because the benefits provided by the use of an n^+-InGaAs cap layer over an InP etch stop are among the primary interests of this work, we prepare a capless reference sample prior to fabrication by cleaving our full heterostructure into two samples and selectively-etching the cap layer off of one sample. Both samples are then carried through the process.

As illustrated in Figure 2.3, the actual fabrication process begins with a mesa wet-etch sequence, described in detail below, followed by plasma-enhanced chemical vapor deposition (PECVD) of a 3000 Å SiO_2 layer. This layer forms the basis for our dielectric-assisted liftoff (DALO) technique, which we discuss in more detail below. In the DALO process, the SiO_2 layer is wet-etched in buffered oxide etch (BOE) after both the ohmic-contact and gate-level photolithography steps. This leaves a photoresist overhang which facilitates reliable, high-yield liftoff, even on 0.6 μm features.

Next, we pattern, e-beam evaporate, and lift off 50 Å Ni/500 Å Ge/1000 Å Au/300 Å Ni ohmic contacts. We alloy the contacts using a rapid-thermal-annealing (RTA) process, which results in greater contact resistance reproducibility and uniformity as well as smoother morphology compared with furnace anneals. Alloying is a two-step sequence, with the contacts heated first to a stable starting temperature of 250° C for 10 s, and then raised rapidly to 375° C for 10 s.

The heavily-doped cap is fully intact at this stage of processing and thus masks

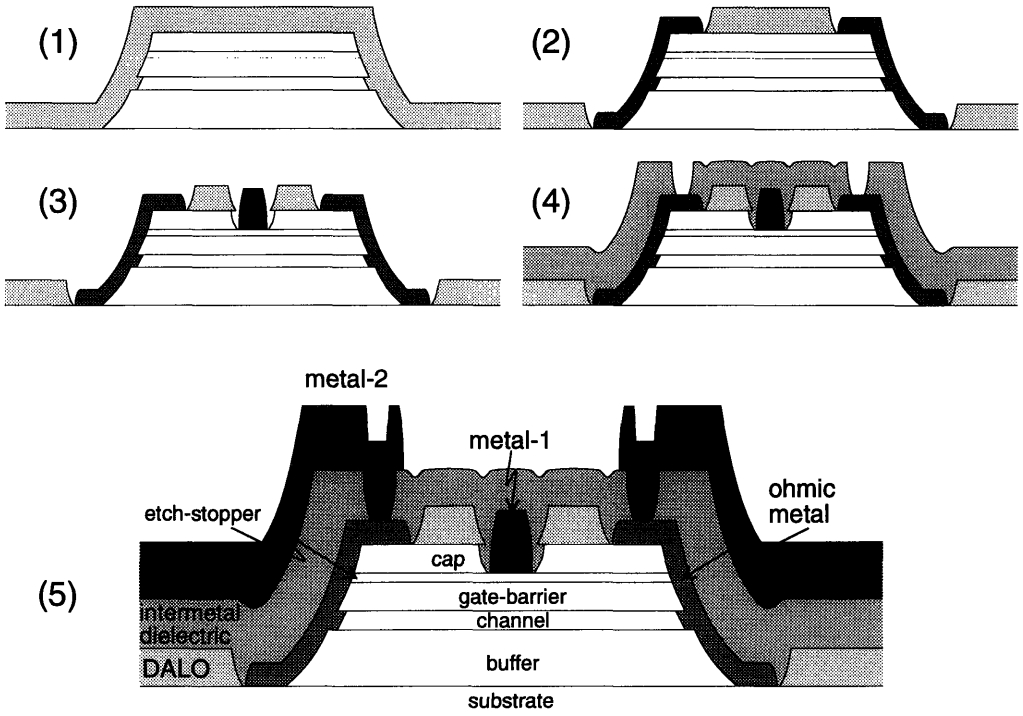

Figure 2.3: Fabrication sequence for the InAlAs/n^+-InP MIDFET. Numbers indicate most recently completed mask step.

our ability to measure R_c to the InP channel for calibrating our anneal recipe. One solution to this issue is to set aside the device samples temporarily while carry a test sample up through the subsequent gate photolithography and cap-recess etch. This test sample may then used to calibrate the anneal before continuing to process the device samples. In order to circumvent such a lengthy process as well as to avoid needlessly consuming heterostructure, we choose instead to optimize our anneals using the uncapped sample which is being processed as a reference. After cleaving off several small pieces, we anneal each piece at a different peak temperature in the range from 355° C to 390° C. We find only random variation in R_c in this range, as shown in Fig. 2.4 and so perform the anneal at the median temperature of 375° C for maximum tolerance.

Following metal-1/gate photolithography and DALO etching, we selectively etch

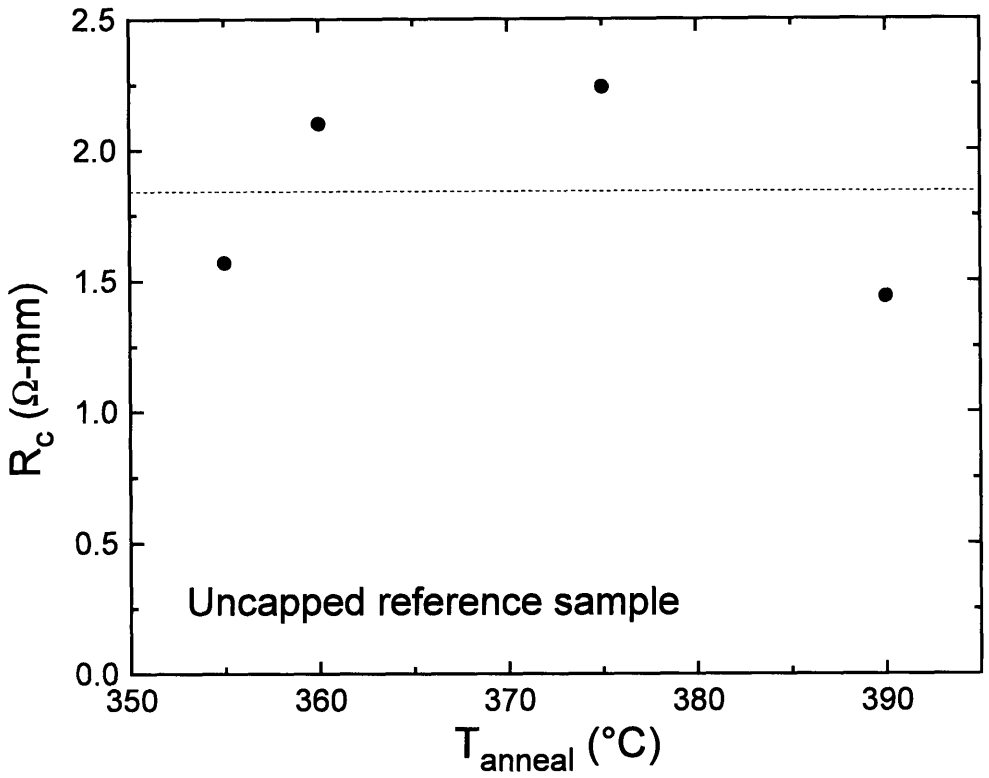

Figure 2.4: Contact resistance vs. anneal temperature on an uncapped calibration sample.

the n^+-InGaAs cap down to the InP etch-stop layer just prior to e-beam evaporation and liftoff of the 250 Å Ti/250 Å Pt/2500 Å Au metal-1/gate layer. Because the vertical etch depth is kept fixed by the etch-stopper, precise timing is unnecessary and we can, in fact, overetch the sample in order to widen the cap recess and form a ~1000 Å gap between cap edge and gate metal. This gap improves breakdown and reduces any cap-gate leakage component of I_G.

After coating the sample with a 5000 Å spin-on glass (cured at 200° C for 30 min.) intermetal-dielectric/passivation layer and patterning/BOE-etching the via-holes, we conclude fabrication by patterning, e-beam evaporating, and lifting off the 250 Å Ti/250 Å Pt/3500 Å Au metal-2 layer. Since the sample cannot be exposed to BOE at this stage, we avoid DALO and instead enhance final liftoff with a robust chlorobenzene soak process capable of defining 8000 Å of metal using 1 μm resist.

Line width variation and edge jaggedness are not an issue here because their scale is small compared with the the relatively large 2 μm minimum feature size of the metal-2 layer.

Our full process flow is itemized in detail in Appendix A.

Realizing this processing technology required particular development in two key areas, etch technology and DALO patterning, which we discuss in more detail in the following sections.

2.3 Etch Technology

We require two distinct types of etchants to fabricate the InAlAs/n^+-InP MIDFET. Essential to our recessed-gate technology is the ability to etch InGaAs selectively while stopping on InP. At the same time, however, we must also be able to etch InP in order to etch through our entire heterostructure for device isolation. From a processing perspective, the simplest thus the most attractive, way to perform this mesa etch is to use a single, non-selective etchant. The very different etch chemistries of the As- and P-based compounds make it difficult to achieve such an etchant, however, as we shall discuss at the end of this section. We therefore adopt an effective second approach in which we alternate two selective etchants: one for etching InGaAs and InAlAs, and another for etching InP. As a further benefit, a selective etchant for InP allows us to reduce gate leakage in our devices by laterally recessing the InP channel layer to isolate it from the gate metal running up the mesa sidewall [45]. In addition to having suitable etch selectivities, appropriate etchants should also have rates on the order of 1000 Å/min. for a balance between reasonable control and good throughput. Furthermore, they should permit masking with soft-baked photoresist to avoid subsequently damaging the substrate with aggressive photoresist stripping methods. The pair of etchants we have selected for our process technology is summarized in Table 2.1.

Table 2.1: Selective etchants for $In_{0.53}Ga_{0.47}As$, $In_{0.52}Al_{0.48}As$, and InP.

Etchant	Conc.	Use	Etch Rate (Å/min.)		
			$In_{0.53}Ga_{0.47}As$	$In_{0.52}Al_{0.48}As$	InP
$H_2SO_4/H_2O_2/H_2O$	1:10:220	Cap recess Mesa etch	2500	3500	< 10
HCl/H_3PO_4	1:19	Mesa etch Sidewall channel recess	< 20	< 8	1000

The first entry in the table is a selective etchant for InGaAs and InAlAs on InP. This H_2SO_4 / H_2O_2 / H_2O solution is commonly used in the AlGaAs/GaAs and InGaAs/InAlAs material systems since it is non-selective among the common As-based III-V compounds [46]. Because it works by oxidizing the sample surface through the H_2O_2 component and subsequently stripping the resulting oxide through the acid, it is also a relatively gentle and uniform etch. At the same time, the etchant is highly selective against InP, with our etch tests showing a selectivity greater than 300:1 for a 1:10:220 solution. This is ideal for our cap recess etch.

Controllable InP etchants are far more difficult to develop or find in the literature. While solutions of bromine / methanol / CH_3COOH, HCl / CH_3COOH / H_2O, and pure HCL all readily etch the material through direct chemical reaction, they all have extremely aggressive rates ranging between 1 μm/min. and 10 μm/min. even when chilled [47, 48]. After testing a variety of etchants, we selected 1:19 HCl/H_3PO_4 as the best choice [49]. This solution has a well-controlled etch rate once thoroughly mixed (the InP rate may be adjusted linearly with HCl concentration up to 10%) as well as a greater than 100:1 selectivity against InGaAs and InAlAs. Its primary drawback is high viscosity, which we accommodate by constantly moving our samples in the solution during etching and by avoiding the use of ultrasound (since the resulting bubbles adhere to the sample surface). While we also explored less viscous etchants based on HCl / H_3PO_4 / CH_3COOH, in concentrations ranging from 1:1:2 to 1:1:6, the

Table 2.2: Non-selective etchants investigated for $In_{0.53}Ga_{0.47}As$, $In_{0.52}Al_{0.48}As$, and InP.

Etchant	Concentration	Etch Rate (Å/min.)		
		$In_{0.53}Ga_{0.47}As$	$In_{0.52}Al_{0.48}As$	InP
$H_2O_2/H_3PO_4/H_2O$	1:1:2	> 2100	N/A	100
$H_2O_2/H_3PO_4/HCl$	7:2:1	> 6400	N/A	800
$H_2O_2/CH_3COOH/HCl$	2:20:1	> 3000	> 3000	> 3000
	1:10:1	> 6000	> 6000	> 6000
	2:90:3	> 2000	> 2000	> 2000
	Recipe			
CH_4/H_2	10 sccm:40 sccm Press. = 40 mTorr Temp. = 60° C Power = 190 W	450	<50	250

InP etch rate was uncontrollably high (0.5-1.5 μm/m) in all cases with the resulting surfaces showing deep, diamond-shaped pits.

An important issue that we uncovered in using selective etchants to alternately etch through successive layers is that the interface between As-based and P-based epitaxial layers can contain a thin region in which the two materials intermix. This interfacial region can be very resistant to both of the selective etchants used for the individual layers. In performing a complete mesa etch, this results in regions of incomplete etching on the wafer, particularly in a thin ring around the sample perimeter. Such a ring reduces the number of working chips yielded from a given sample.

This problem can be eliminated by moving to a non-selective mesa etch technology. As a step toward developing an improved process for future n^+-InP-HFET fabrication, we have therefore explored several potentially suitable etching schemes, both wet and dry, which we summarize in Table 2.2.

Although a reliable wet-etch technology is attractive because it permits a rapid turnaround time and requires little additional equipment, we were not able to identify such a suitable wet etchant. Each of the etchants we tested displayed a combination of undesirable properties, including rapidly-changing etch rate over time, aggressive attacking of the photoresist mask, a large difference in etch rates between materials (leading to a "terracing" effect at the mesa sidewalls), and enhanced etching near the mask boundaries (leading to a "trenching" effect).

Our experiments do, however, recommend reactive-ion etching (RIE) as a promising non-selective approach. In particular, we find that a CH_4/H_2 process achieves a very reproducible etch rate for both InP and InGaAs, is unimpeded by thin interfacial quaternaries between layers, yields extremely vertical sidewalls, and is easily masked using photoresist. The method shows some associated drawbacks as well. Most importantly, we were not able to achieve any InAlAs etching at substrate temperatures of up to 90° C (the maximum temperature achievable in our RIE system), attributed to the fact that the etch by-product trimethyl-aluminum is not volatile at these low temperatures. While some physical sputtering of the InAlAs takes place, it is self-limited to only 50 Å regardless of etch time due to a polymer buildup which occurs on all areas not being actively etched. This polymer also deposits on the photoresist mask, with the resulting strain eventually distorting the pattern. We believe that both of these issues may be resolved to yield an ideal mesa etch technology for InP-channel HFET's by increasing the substrate temperature to over 150° C. This step may significantly enhance the InAlAs etch rate and permit a reduced overall etch duration, preventing excessive polymer buildup on the photoresist.

2.4 Dielectric-Assisted Liftoff (DALO)

Scaling down minimum feature size, particularly gate length, is key to optimizing high-frequency performance in an HFET technology. For our process, we developed a

dielectric-assisted liftoff technique permitting our Karl Süss optical aligner to define features down to 0.6 μm limit without sacrificing high yield for circuit fabrication. This gate length is sufficiently small for studying much of the transport physics most relevent in modern submicron devices.

In a liftoff process using solely positive photoresist, reliability is determined both by the thickness of resist compared to the that of the metal film being patterned as well as by the shape of the resist sidewall. Because the developed resist displays a sloping sidewall, with wider openings at the surface compared with at the substrate, an evaporated metal film tends to be continuous over an entire sample. The film must tear in order to lift off, limiting the metal thickness to about 20% of the resist thickness. Even with this limitation, patterns show jagged edges and small features tend to be pulled off the substrate completely.

One solution to this problem is to soak the sample in chlorobenzene prior to development. This soak hardens the photoresist surface, resulting in a thin lip that breaks the continuity of the subsequently evaporated metal film. We have achieved excellent liftoff using this technique, routinely patterning 4000 Å films with 1 μm resist and successfully testing the technique with films up to 8000 Å.

Because it requires overdevelopment to punch through the hardened photoresist surface, however, chlorobenzene-enhanced liftoff can increase feature size by 0.1 to 0.2 μm. In addition, the formed lip can be somewhat uneven, again leading to jagged edges which can degrade the breakdown voltage by creating local regions of concentrated electric field.

For our process, we have addressed each of these issues by developing a dielectric-assisted liftoff technique. In our DALO process, a sample is coated after the mesa step with a 3000 Å PECVD SiO_2 film, designed to be about the same thickness as the anticipated films to be patterned. After both the ohmic contact and metal-1/gate photolithography steps, the SiO_2 is wet-etched down to the semiconductor in BOE.

This wet etch recesses the SiO_2 film laterally as well, turning the overlying photoresist into a lip which greatly enhances liftoff. The greatest attraction of this technique, in fact, is that it decouples feature patterning from the formation of the lip. Although we employ a standard 1 μm resist thickness to permit sharing of exposure calibration data with our other photolithography steps, DALO easily permits the resist to be thinned down for better feature resolution without sacrificing liftoff yield.

Prior to settling on using a PECVD SiO_2 DALO layer, we explored both spin-on glass as well as PECVD Si_xN_y. Despite its simplicity and rapid turnaround time, we rejected spin-on glass in this context because it suffered from irreproducible changes in etch rate after being subjected to the ohmic contact annealing process and also left small particles of unetched material within feature openings that were smaller than 1 μm. We also rejected Si_xN_y because its high strain limits film thickness. This is particularly important in order to accommodate future versions of our process which might employ Si_xN_y as a passivation layer.

In order to test the resolution of our DALO process, we designed a custom test mask featuring line gratings and dot arrays in a variety of feature and spacing sizes down to 0.5 μm. We find that our DALO process is able to yield metal lines down to the minimum 0.5 μm feature size on full 2 inch wafers. By carefully removing photoresist edge-bead build-up on the sample, we are able to achieve a similar resolution of 0.6 μm on quarter- and eight-wafer samples. Fig. 2.5 shows a scanning-electron micrograph of a completed 0.6 μm gate.

Since DALO requires a BOE etch, we have also tested tolerance to variations in etch time, finding no degradation in liftoff results even after overetching the SiO_2 layer by 150%.

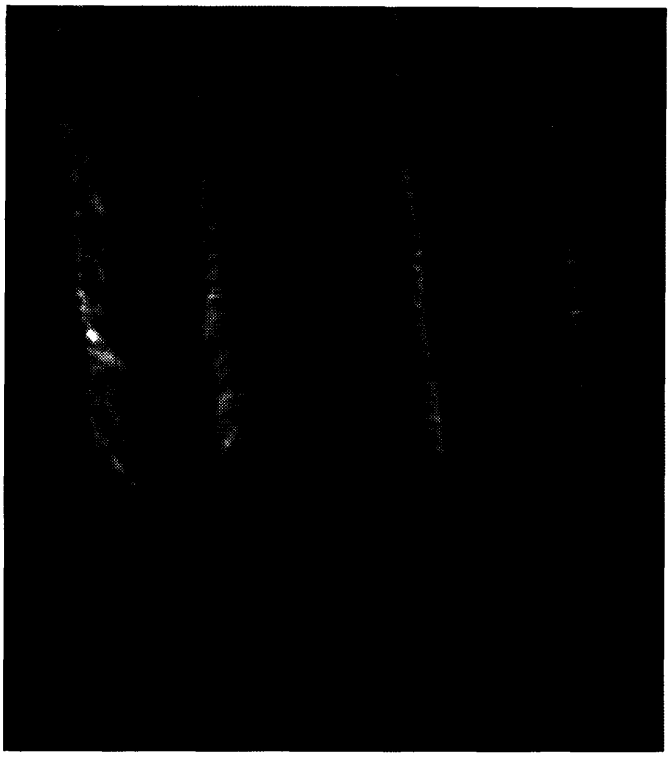

Figure 2.5: SEM micrograph showing a 0.6 μm gate patterned using our DALO process.

2.5 Process Characterization

Figure 2.6 shows a photograph of a completed chip, which measures 3.9 mm $\times$ 4.2 mm. The bottom half of the chip consists of an array of Π-gate microwave devices with 6 gate lengths ranging from 0.6 μm and 2 μm and with current flow oriented 0° with respect to the major wafer flat (some 90° devices are included in the upper-left quadrant). For future use, we also include several devices designed for X-ray or electron-beam written gates down to 0.14 μm. Gate widths and gate-source/gate-drain separations are nominally 200 μm and 2 μm, respectively, with some devices designed for exploring smaller widths or larger gate-drain separations. We also include a test structure with the same layout as the neighboring working devices, but without the active mesa. We use this "open" structure to measure the pad-related parasitic capacitances, a key step in later extracting an accurate small-signal device model.

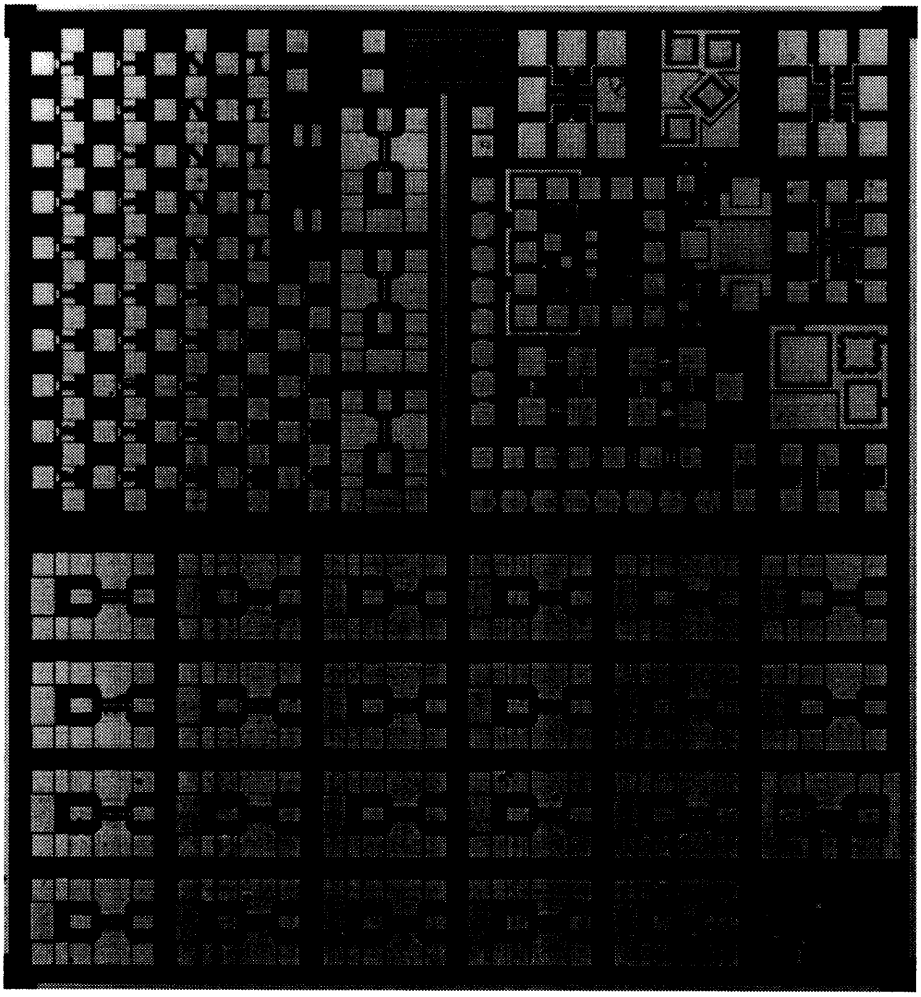

Figure 2.6: Photograph of completed InAlAs/n^+-InP MIDFET chip.

The upper-left chip quadrant contains an array of device designed for standard probe station measurement at low frequencies. Because these devices are small and may be packed densely, we include 10 gate lengths ranging from 0.6 μm to 10 μm, in 0°, 45°, and 90° orientations, with gate-drain separations between 2 μm and 10 μm, and with gate widths ranging from 6 μm to 50 μm.

The upper-right quadrant of the chip includes several diodes for measuring the capacitance-voltage (CV) characteristics of our heterostructure as well as for characterizing gate/channel-sidewall leakage. In order to demonstrate the high-performance circuit potential of our InAlAs/n^+-InP MIDFET technology, our mask also includes

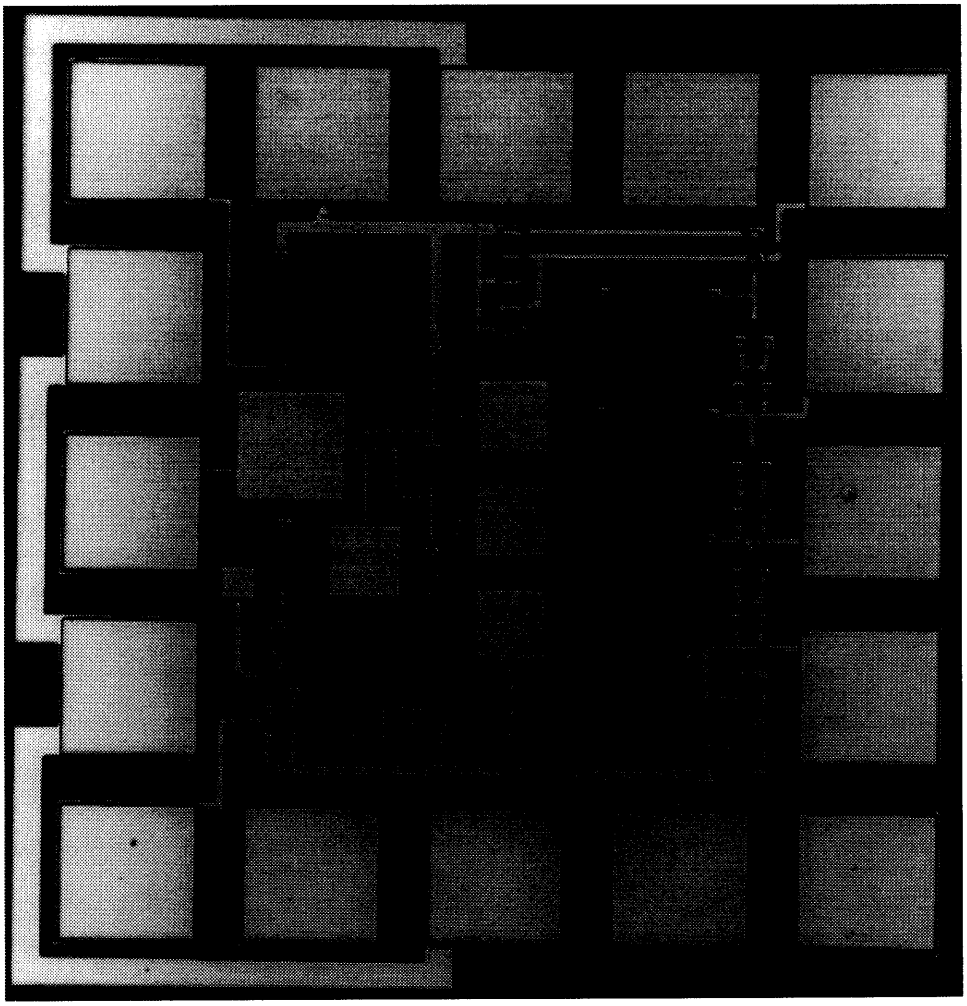

Figure 2.7: Close-up photograph of monolithic, voltage-tunable resonator.

an 8-transistor monolithic, voltage-tunable microwave resonator circuit, designed by Peter R. Nuytkens [42], which takes advantage of our capacitor and mesa-resistor capabilities. A close-up of the resonator circuit is shown in Figure 2.7.

Since parasitic resistance has a large impact on device performance, our chip also includes a set of test structures for characterizing the various parasitic resistances inherent to our technology. As shown schematically in Fig. 2.8, current may pass through up to eight such resistances before reaching the intrinsic device. Each resistance is measured with its own particular test structure, with the results summarized in Table 2.3.

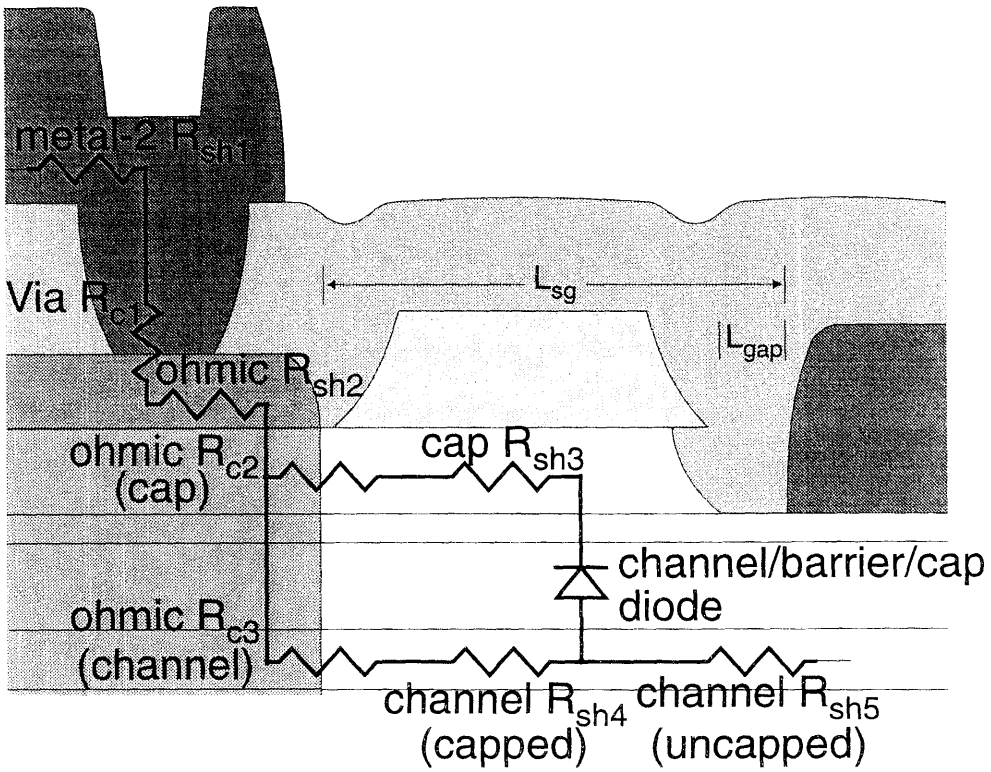

Figure 2.8: Schematic MIDFET cross-section illustrating the components to total parasitic resistance (not shown: metal-2/metal-1 via R_c and metal-1 R_{sh}).

Current enters and exits every device through a metal-2 pad or interconnect. Since we expect metal-2 sheet resistance R_{sh1} to be quite low, we measure the value using a long serpentine strip. Metal-1 which forms both gates and interconnects, is similarly characterized.

Current must next pass from metal-2 to the ohmic-metal through via holes in the spin-on-glass. The associated R_{c1} is measured using a chain of via links between the two layers. In circuit applications, metal-2 and metal-1 connect through vias as well, which are characterized with a similar test structure.

The value R_{sh2} for the annealed ohmic-metal itself is expected to be significantly higher than that of either metal-1 or metal-2 and is thus measured with a shorter strip. The ohmic-metal strip is placed on top of a mesa strip, overlapping the mesa on

Table 2.3: Summary of parasitic resistances.

Parameter	Test Structure	Value	Units
Metal-1 R_{sh}	serpentine strip	60	mΩ/□
Metal-2 R_{sh1}	serpentine strip	45	mΩ/□
Ohmic Metal R_{sh2}	varying width strips	1.25	Ω/□
Metal-2/Metal-1 Via R_c	links	5×10^{-8}	Ω·cm^2
Metal-2/Ohmic Metal Via R_{c1}	links	2×10^{-7}	Ω·cm^2
Cap R_{c2}	TLM	0.15	Ω·mm
Channel R_{c3} (capped)	FGTLM	2.4	Ω·mm
Channel R_{c3} (uncapped)	FGTLM	1.8	Ω·mm
Cap‖channel $R_{sh3}‖R_{sh4}$	TLM	63	Ω/□
Cap‖channel $R_{sh3}‖R_{sh4}$	VDP	50	Ω/□
Channel (capped) R_{sh4}	FGTLM	600	Ω/□
Channel R_{sh5} (uncapped)	TLM	1350	Ω/□
Channel R_{sh5} (uncapped)	VDP	1150	Ω/□
Calculated MIDFET R_s (low I_D)	-	3.8	Ω·mm

both sides just as in an actual device. Strips of two different widths are used to permit the ohmic-on-mesa sheet resistance to be separated out from the ohmic-on-substrate component contributed by this overlap.

In studying the cap layer in detail in Chapter 4, we will find that this layer contributes significantly to carrying current once the total current reaches a sufficiently high value. As a result, the contact resistance R_{c2} to the cap is an important parasitic, as is the value for the cap sheet resistance R_{sh3}. One method for measuring these quantities is the transmission line model (TLM) technique [50]. This method actually measures the parallel combination of the cap and channel. However, the values for the cap R_{c2} and R_{sh3} are expected to be more than 10 times smaller compared with the resistances for the channel and thus dominate the measurement. We can also measure the cap‖channel sheet resistance independently using a Van der Pauw (VDP) test structure, yielding results that agree reasonably well with those from the TLM. The small discrepancy indicates that our mesa are actually slightly narrower than designed due to the lateral etching that occurs when forming them.

Since the cap essentially masks the channel in the TLM structure, we characterize R_{c3} and R_{sh4} for the capped channel layer on actual MIDFET's using the Floating-Gate TLM (FGTLM) technique [51]. The cap in a MIDFET is discontinuous from source to drain due to the recess and thus does not carry current and influence the measurement at low values of I_D.

Because the cap recess is generally wider than the actual gate length in order to improve the breakdown voltage and prevent a leakage path between the gate and the source or drain, current must pass through a short length of uncapped channel (L_{gap}) before reaching the intrinsic channel beneath the gate. We measure R_{sh5} for this gap using a TLM structure fabricated on our reference uncapped sample. Comparing the characterization results for both capped R_{sh4} and uncapped R_{sh5} reveals the effectiveness of the cap in screening Fermi level pinning.

The TLM also permits us to calculate the contact resistance to the channel of the uncapped reference sample. We note that the value of R_{c3} in this case is actually lower than the value for the capped channels of our typical devices, attributed to the ohmic-metal not having to penetrate quite as deep into the sample in order to contact the channel. This behavior suggests that a very attractive way to reduce source and drain resistance in InAlAs/n^+-InP MIDFET's is to *recess* the ohmic contacts. In fact, since the InP channel is itself also an excellent etch-stop layer, the ohmic metal can be evaporated directly onto the channel following a selective-etch process. As a step toward improving our technology for future runs, we have developed and demonstrated such a recessed-ohmic-contact process, which we describe below.

2.6 Recessed Ohmic Contacts

The selective etch-stop properties of the InP channel itself make it natural to try to place the ohmic contact metal directly on top of the channel for improved R_c. At the same time, however, it is essential to ensure that the ohmic metal continues

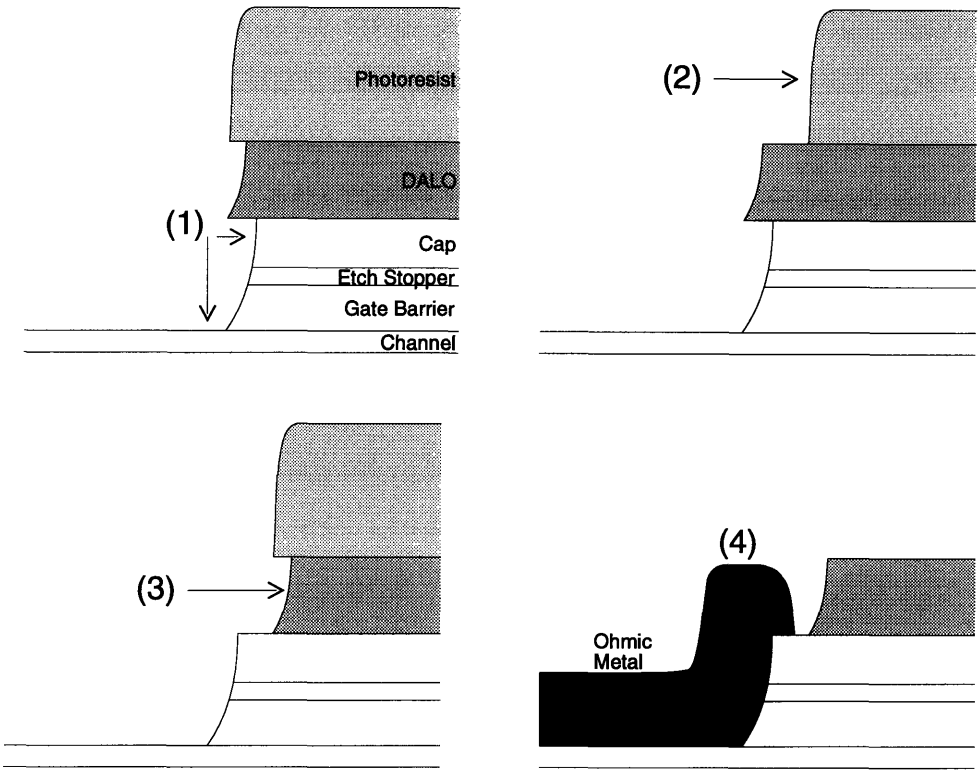

Figure 2.9: Recessed-ohmic-contact process, beginning immediately after initial DALO etch (wet-etch version shown).

to contact the cap, which carries significant current in parallel with the channel at sufficiently high current. To demonstrate the benefits of such a recessed-contact technology, we have developed a four-step process that meets these requirements and which successfully reduces R_c by a factor of two over the standard non-recessed scheme. The process comes in two variations, a wet-etch version, and a hybrid wet-dry-etch version, which differ in only one step. A process flow is illustrated in Fig. 2.9.

Following the standard ohmic photolithography and BOE etch of the DALO SiO_2 layer, the cap, etch-stop, and gate-barrier layers are selectively etched down to the channel. In the wet-etch version of the process, this etch employs the same alternating selective etchant scheme used for the mesa etch. In the hybrid wet-dry version, we use our non-selective RIE recipe to etch down to the InAlAs gate-barrier, where the etch stops naturally. We then switch to a wet etchant to etch the gate-barrier and stop

selectively on the channel. This hybrid approach results in less lateral movement of the cap layer, requiring less photoresist etching in the following step and thus ultimately yielding a wider source-drain spacing for easier gate alignment.

Although the InP-channel is exposed at this point, the cap is hidden beneath the DALO structure and cannot yet be contacted. In the wet-etch version, in fact, the cap has actually etched laterally by a significant amount.

To expose the cap, we next etch the photoresist laterally in an O_2 plasma. Although this etch is isotropic and thus etches vertically as well, the 1.0 μm resist layer is sufficiently thick to withstand some loss of thickness. The lateral resist etching moves the source and drain ohmic contact edges closer together and makes gate alignment more difficult. For this reason, we take care to etch no more than necessary and carefully calibrate the photoresist etch rate prior to the process run to prevent overetching. We have found that the etch latency time for photoresists increases after exposure to the DALO BOE etch, and therefore perform calibration on similarly exposed test samples. In addition, we have also developed a way to characterize the exact lateral etch distance. SEM micrographs of etched samples indicate a nearly 1:1 ratio between the vertical and lateral etch rates in our chamber. Consequently, we can immediately determine the lateral etch distance by determining the change in resist thickness using a profilometer. The simplicity of this method permits frequent monitoring of the device samples while etching in short stages.

After completing the photoresist etch, we perform a second BOE etch to reform the DALO lip. Ohmic contact metal evaporation and liftoff then proceeds as with the standard process.

We have characterized the effectiveness of this new technique using test samples with similar heterostructures to those of our actual MIDFET's. We process these samples using our device mask set up through gate photolithography and the cap recess, stopping prior to the actual gate evaporation. This results in devices with a

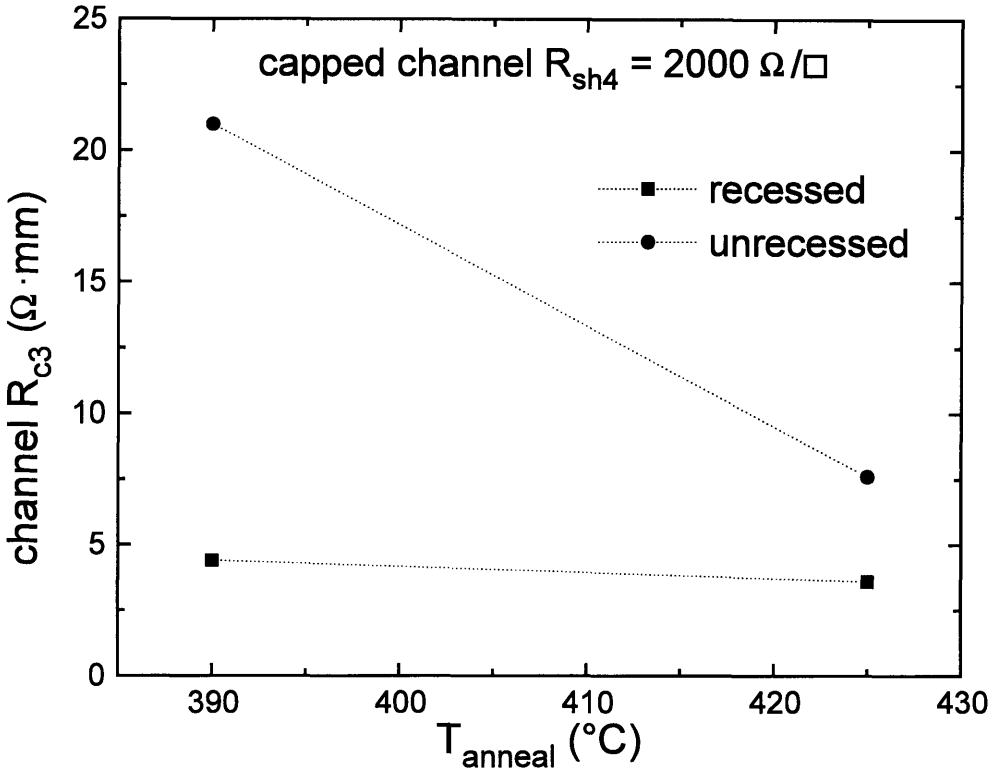

Figure 2.10: Test sample contact resistance vs. anneal temperature for both recessed and non-recessed ohmic contacts.

break in the cap where the gate would normally sit. By measuring an array of such devices with with varying gate length and drain-gate separation, we then characterize R_{sh4} and R_{sh5}, the sheet resistances for both the capped and uncapped channel shown in Fig. 2.8, and ultimately extract channel contact resistance R_{c3}. In addition, we use the TLM test structure to measure cap contact resistance R_{c2}, which verifies that the ohmic metal is making contact to that layer.

Fig. 2.10 summarizes our characterization results, comparing a recessed-contact and a non-recessed-contact reference sample, with pieces annealed at 390° C and 425° C. We note that recessing the ohmic contact cuts R_{c3} in half and reduces the dependence on anneal temperature significantly. The extracted values of R_{c3} are higher than generally observed in our MIDFET's, which we attribute to a greater capped-channel R_{sh4} in this particular sample. Indeed, studies have reported an

approximately quadratic rise in R_c to layers with increasing R_{sh} [52].

2.7 Summary

We have developed a heterostructure design, process, and mask layout for fabricating high-performance InAlAs/n^+-InP MIDFET's. Our device design features both an InP channel and an InP etch-stopper beneath an n^+-InGaAs cap, requiring that we devote some attention to developing an appropriate etch technology. This design is then processed in a two-level-metal technology with DALO patterning capable of producing circuits such as a monolithic, voltage-tunable resonator. As a contribution to future processing runs, we have also developed a recessed-ohmic-contact step that promised to reduct R_c to the buried InP channel in half. The completed chip contains arrays of microwave and low-frequency devices for study, as well as a variety of test structures with which we characterize the process.

Chapter 3:

General Results and Small-Signal Modeling

Assessing the InAlAs/n$^+$-InP MIDFET and identifying the benefits or tradeoffs stemming from using InP epitaxial layers divides naturally into three core chapters. This chapter presents a general performance overview. We focus on typical figures of merit, including g_m, maximum I_D ($I_{D,MAX}$), BV_{DS}, f_T, and f_{max}, that are measured most directly and which are key to evaluating suitability for a wide variety of high-power, high-frequency applications. As a tool for later gathering more fundamental physical insight into our devices, particularly regarding channel electron transport, we also develop a small-signal equivalent circuit model as well as a technique for de-embedding the intrinsic model parameters from among the parasitic elements. This overview and model set the stage for the following two chapters in which we will separate out and explore in detail the advantages of using InP in each of two distinct contexts: as the etch-stop layer for a recessed-cap process, and as the active channel layer itself.

3.1 Device Characteristics

Fig. 3.1 shows g_m, I_D, and I_G vs. V_{GS} for a typical 0.8 μm $\times$ 200 μm InAlAs/n$^+$-InP MIDFET at V_{DS}=5 V, with g_m presented at both low-frequency (DC) and 2 GHz. This millimeter-wave data is acquired using the s-parameter measurement setup described in the next section and represents the total, uncorrected device, with only the parasitic capacitances from the large probe pads subtracted out. At the given V_{DS}, the device operates in the saturation mode (I_D relatively insensitive to V_{DS}), over the full V_{GS} swing. We find that g_m rises approximately linearly with V_{GS} as V_{GS} increases beyond the threshold voltage (V_T= -1.7 V), reaching a peak value

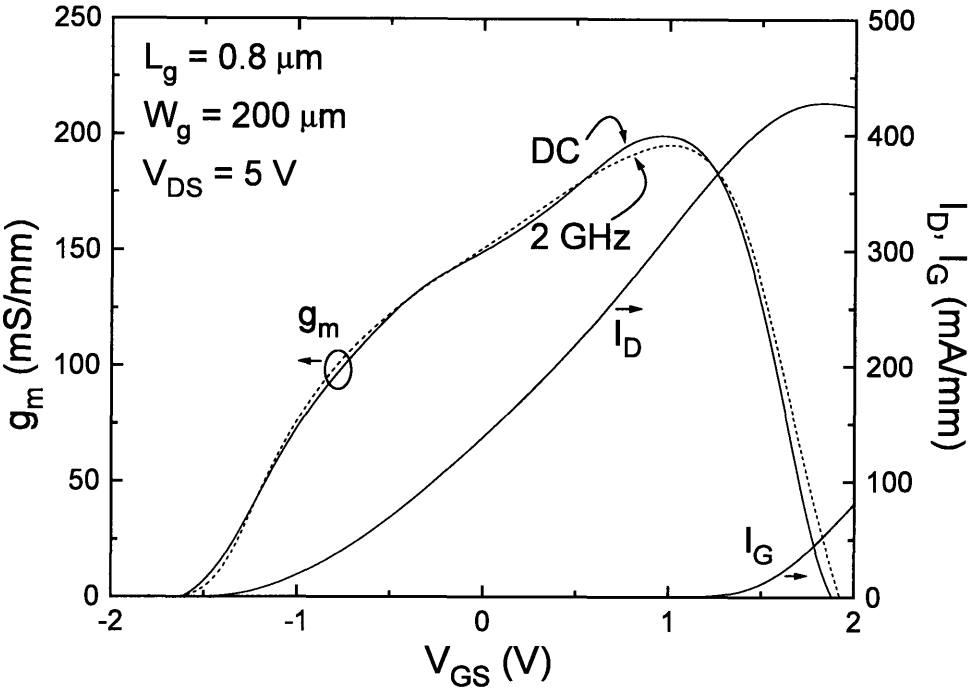

Figure 3.1: g_m (DC and 2 GHz), I_D, and I_G vs. V_{GS} at V_{DS}=5 V for a 0.8 μm × 200 μm device.

of about 200 mS/mm before declining. We also observe a kink or flattening of the slope in g_m vs. V_{GS} at about V_{GS}= −0.75 V. Our undoped-gate-barrier, thin-channel design contributes to a relatively broad V_{GS} swing over which g_m is large, leading to a typical $I_{D,MAX}$ of over 430 mA/mm. These values for both g_m and I_D are the highest reported for any InP-channel HFET design of comparable gate length. An additional benefit of the undoped gate-barrier layer is a low bulk trap density in this layer, contributing to the less than 5% frequency dispersion in g_m over the broad frequency range from DC to 2 GHz. We note that g_m is ultimately limited at high V_{GS} by the onset of significant I_G, which begins to become comparable in magnitude to I_D in our devices at about V_{GS}= 1.25 V.

Although the slope of g_m vs. V_{GS} begins to flatten somewhat at $V_{GS}\simeq$ −0.75 V, we find that it still continues to rise significantly over the remainder of the useful

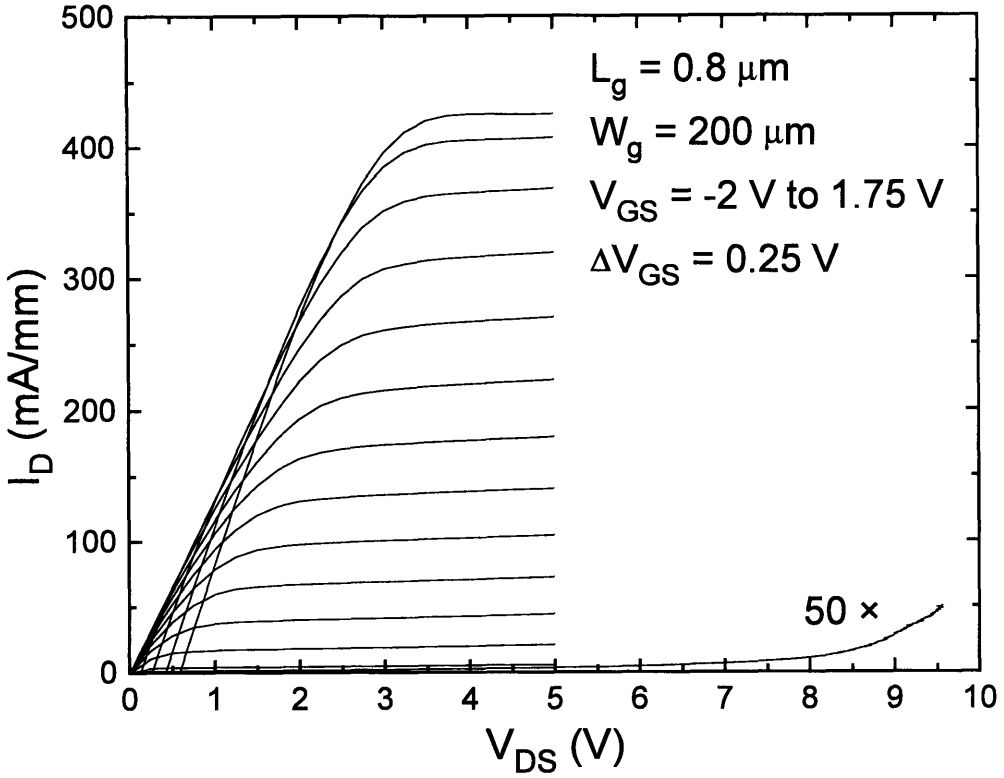

Figure 3.2: I_D vs. V_{DS} with varying V_{GS} for a 0.8 μm × 200 μm device. Trace at pinchoff is magnified 50 × to show off-state BV_{DS}.

V_{GS} swing. This behavior is in contrast to that of several other reported MIDFET's which achieve a broad plateau in g_m at sufficiently short gate lengths due to the onset of velocity-saturation in the channel. We later show that this plateau is actually present in our devices in the intrinsic transconductance (g_{m0}), but masked by a rapid decline in small-signal source-resistance (r_s) as the cap layer begins to carry significant current in parallel with the channel. This nonlinearity in r_s will make it necessary to later correct for the effects of r_s before drawing any physical insight from the behavior of g_m.

In Fig. 3.2, we show the output characteristics for the same device. For V_{GS} at threshold, we observe very sharp pinchoff behavior, with the I-V trace indistinguishable from the x-axis at full-scale. Magnifying the V_{GS}= -1.7 V trace by a factor of 50 reveals the breakdown behavior, with an off-state drain-source breakdown (BV_{DS}),

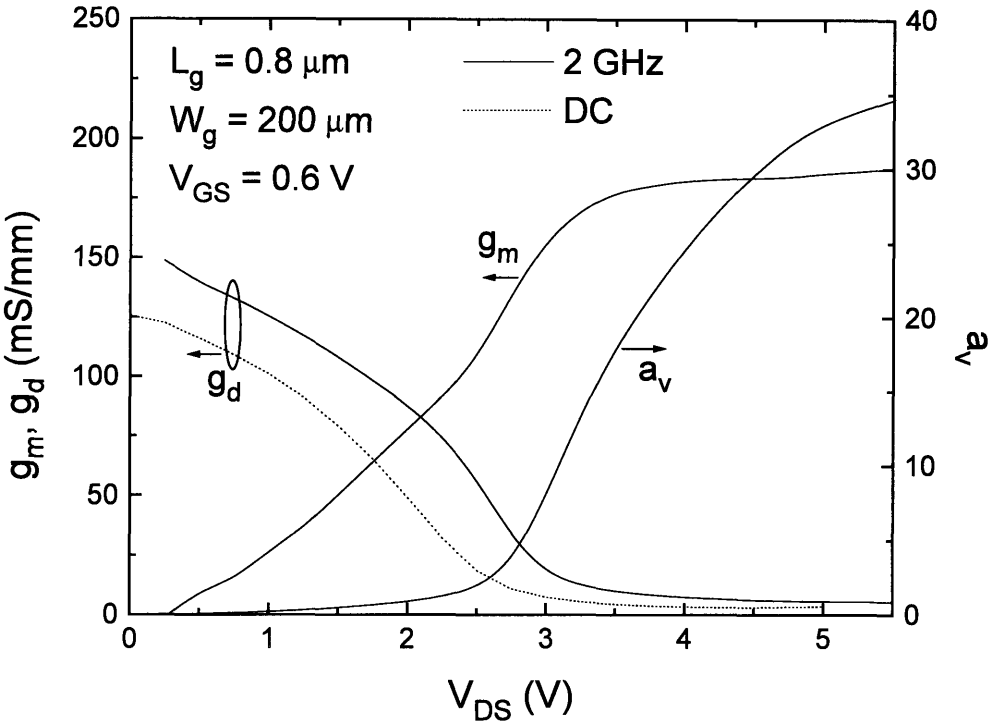

Figure 3.3: g_m and a_v vs. V_{DS} at 2 GHz and g_d vs. V_{DS} at both DC and 2 GHz for V_{GS}= 0.6 V (point of peak g_m).

defined at I_D= 1 mA/mm, of BV_{DS}= 9.6 V. This value is significantly higher than for InGaAs-channel HFET's of comparable L_g. Along with BV_{DS}, a key figure of merit limiting power density in a device is the maximum knee voltage, denoting the transition from linear to saturation mode with increasing V_{DS} at fixed V_{GS}. We observe a maximum knee voltage of about $V_{DS} \simeq$ 3.5 V, higher than for typical InGaAs-channel HFET's due to our comparatively larger source and drain resistance.

Beyond the knee, I_D vs. V_{DS} is quite flat in the device's saturation mode, indicating very low g_d. To explore this behavior further, we plot g_m and voltage gain $a_v = \frac{g_m}{g_d}$ vs. V_{DS} at 2 GHz and g_d vs. V_{DS} at both DC and 2 GHz, all at a fixed V_{GS} of 0.6 V (corresponding to peak g_m) in Fig. 3.3. As the device moves into the saturation mode with increasing V_{DS}, g_d drops rapidly to less than 3.5 mS/mm at DC and to under 5.5 mS/mm even at high-frequency. Combined with the relatively constant value of

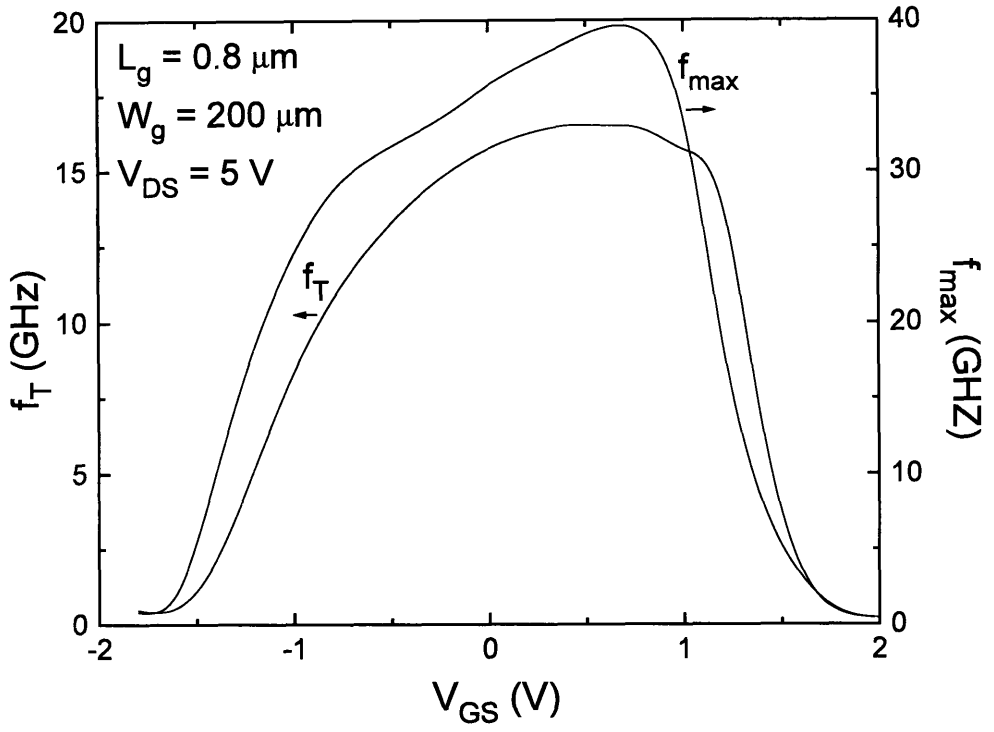

Figure 3.4: f_T and f_{max} vs. V_{GS} at V_{DS}= 5 V.

g_m, this results in a rising voltage gain which exceeds 30 for V_{DS}> 4.5 V.

The high-frequency performance of the L_g= 0.8 μm InAlAs/n$^+$-InP MIDFET is illustrated in Fig. 3.4, which shows both f_T and f_{max} vs. V_{GS} at V_{DS}= 5 V for the same device. As with g_m, f_T rises linearly as V_{GS} is initially increased from threshold. At higher V_{GS}, however, f_T flattens into a broad plateau, peaking at 16.5 GHz and maintaining 90% of this peak value over a V_{GS} swing of 1.5 V. We later attribute this plateau, not directly visible in g_m due to the effects of nonlinear r_s, to a transition from mobility-limited to velocity-saturation-limited transport in the channel. The behavior of f_{max} is closer to that of g_m, showing an r_s-related kink at about V_{GS}= -0.75 V and peaking at a value of 40 GHz.

Fig. 3.5 shows the dependence of f_T and f_{max} on V_{DS}, biased near the peak values

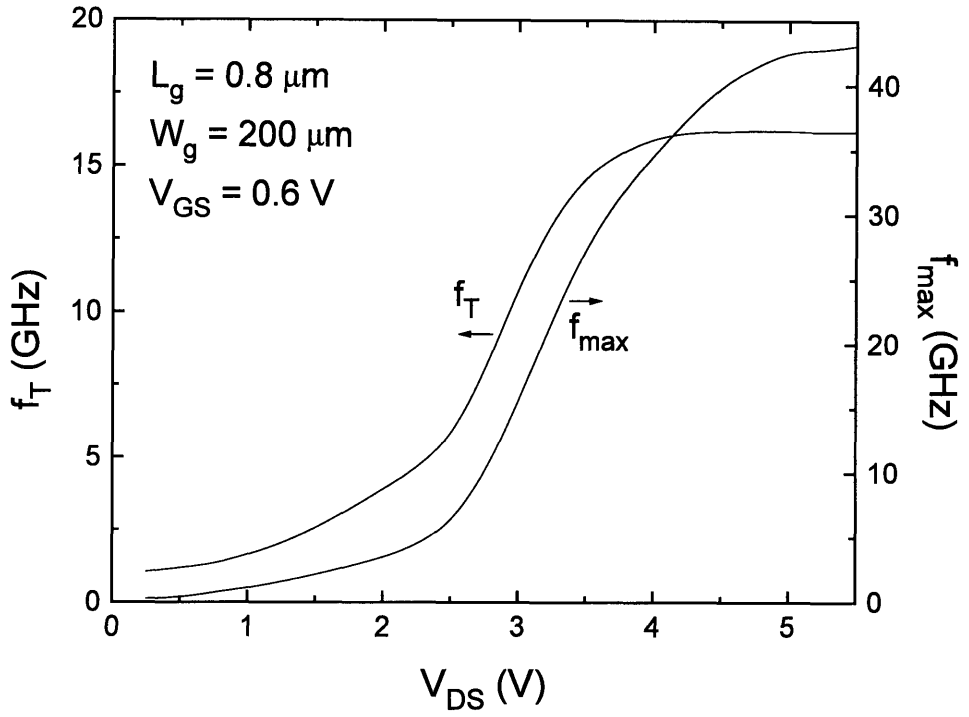

Figure 3.5: f_T and f_{max} vs. V_{DS} at V_{GS}= 0.6 V (approximate point of peak g_m, f_T, and f_{max}).

at V_{GS}= 0.6 V. We find that f_T remains relatively insensitive to V_{DS} over a wide V_{DS} range once the device enters the saturation regime. In contrast, we note that f_{max} continues to rise as V_{DS} is increased. This behavior correlates closely with that of a_v and is thus attributed primarily to the declining g_d noted in Fig. 3.3.

Our findings show that the InAlAs/n$^+$-InP enjoys an attractive combination of high $I_{D,MAX}$, BV_{DS}, g_m, and a_v together with both low g_d and with values of f_T and f_{max} that maintain their peak over a broad V_{GS} swing. These features make the device well-suited to a variety of high-power telecommunications applications and thus an ideal vehicle for assessing the performance of InP-channel HFET's in general compared with other device designs on InP. At the same time, we also note that V_{DS} must exceed a relatively large knee voltage of about 3.5 V, attributed to high source and drain resistance at low I_D, in order to bias the device in its saturation mode.

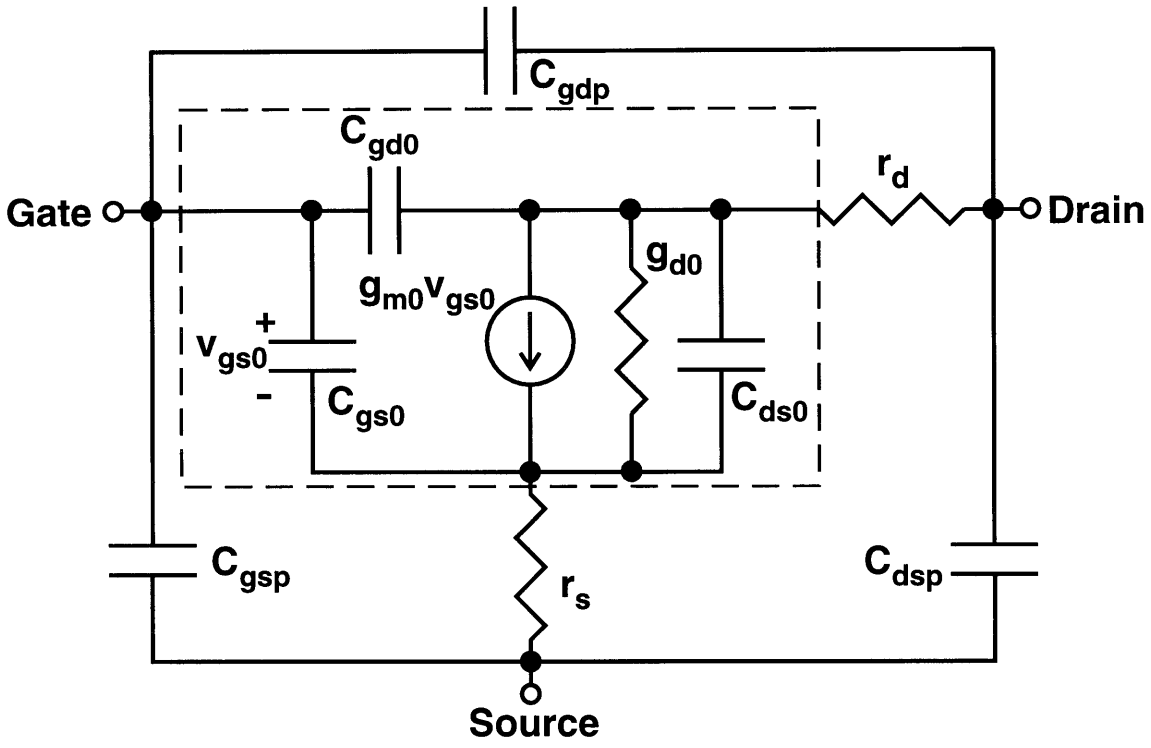

Figure 3.6: Small-signal equivalent circuit model using to model the InAlAs/n^+-InP MIDFET in this work. Dashed line encloses the model for the intrinsic device.

In the following section, we develop a method for modeling the small-signal behavior of the intrinsic device, de-embedding it from the influence of the surrounding parasitic elements, which forms the basis for accurately exploring the physics of the InP channel in the remainder of this work.

3.2 Small-Signal Model Parameter Extraction

We may reveal significant physical insight into the InAlAs/n^+-InP MIDFET, particularly regarding electron transport in the InP channel, by extracting a small-signal model for the device and profiling the behavior of the model parameter values as we vary both L_g and bias. Since this method requires that we solve for all the model parameter values at each of a large number of bias points, a suitable model must be computationally simple without sacrificing accuracy. Our approach in this work is

based on the the FET small-signal equivalent circuit shown in Fig. 3.6, which models the device up through and including the probe pads. We selected this model and the extraction procedure described below in the course of a separate project exploring the impact of the the extrinsic source and drain region on the high-current performance of AlGaAs/n$^+$-InGaAs MIDFET's [35].

The portion of the circuit enclosed by the dashed line models the intrinsic device beneath the gate metal, with the corresponding y-parameter representation given by [53]

$$y_{11} = j\omega \left(C_{gs0} + C_{gd0}\right) \tag{3.1}$$

$$y_{12} = -j\omega C_{gd0} \tag{3.2}$$

$$y_{21} = g_{m0} - j\omega C_{gd0} \tag{3.3}$$

$$y_{22} = g_{d0} + j\omega \left(C_{ds0} + C_{gd0}\right) \tag{3.4}$$

In order to simplify the extraction process, our model eliminates resistance element r_i included in more complex models, since we do not draw any conclusions regarding device physics or performance from this parameter. We also do not include conductances such g_{gs} or g_{gd} in parallel with C_{gs0} or C_{gd0} to account for gate leakage, since correcting for such a large effect is inherently unreliable and the device is largely useless in this region. Thus, we treat this model and all extracted circuit element values as valid only up through the onset of gate leakage.

The two elements in this model most important for understanding transport are the intrinsic transconductance g_{m0} and the gate-source capacitance C_{gs0}. For example, in the HFET's velocity-saturation regime of operation, one can define the effective electron velocity v_e^{eff} in the channel from these parameters through

$$v_e^{eff} \equiv \frac{L_g}{\tau_t} = \frac{g_{m0} L_g}{C_{gs0}} \tag{3.5}$$

where τ_t is the electron transit time from source to drain [14]. The values of g_{m0} and C_{gs0} may themselves be easily extracted from the intrinsic y-parameters, according

to

$$g_{m0} = \Re e\left[y_{21}\right] \tag{3.6}$$

$$C_{gs0} = \frac{\Im m\left[y_{11} + y_{12}\right]}{\omega} \tag{3.7}$$

We note that using this procedure is more accurate than methods which estimate v_e^{eff} through f_T, since f_T is degraded through C_{gd0}, g_{d0}, r_s, and r_d, yielding a value somewhat lower than the true channel velocity [44]. The remaining circuit element values may be similarly extracted according to

$$g_{d0} = \Re e\left[y_{22}\right] \tag{3.8}$$

$$C_{gd0} = -\frac{\Im m\left[y_{12}\right]}{\omega} \tag{3.9}$$

$$C_{ds0} = \frac{\Im m\left[y_{12} + y_{22}\right]}{\omega} \tag{3.10}$$

Although C_{gd0} seems as though it may be extracted through $\Im m\left[y_{21}\right]$ as well, according to Eq. 3.3, comparing our model with a more complex model that incorporates additional elements such as r_i [54] reveals that these elements appear as added terms in $\Im m\left[y_{21}\right]$ that are also linear in ω. The same comparison shows, however, that $\Im m\left[y_{12}\right]$ continues to determine C_{gd0} accurately even in the presence of the minor elements that our model neglects.

We obtain the de-embedded y-parameter model for the intrinsic device through a three stage process. First, we measure the s-parameters over the full range of bias conditions, using an HP4145B to step between bias points and an HP8510 network analyzer to measure the s-parameters from 0.5 to 40 GHz, all under computer control through custom software. Next, we convert the s-parameters to y-parameters and subtract out the impact of the probe pads, modeled by parasitic capacitances C_{gsp}, C_{gdp}, and C_{dsp}. Minor pad inductances are not included in our model, since they may be ignored in the measured frequency range. The third stage corrects for the parasitic source and drain resistances, which are subtracted out after converting to the z-parameter domain. Converting back to y-parameters yields the desired intrinsic model.

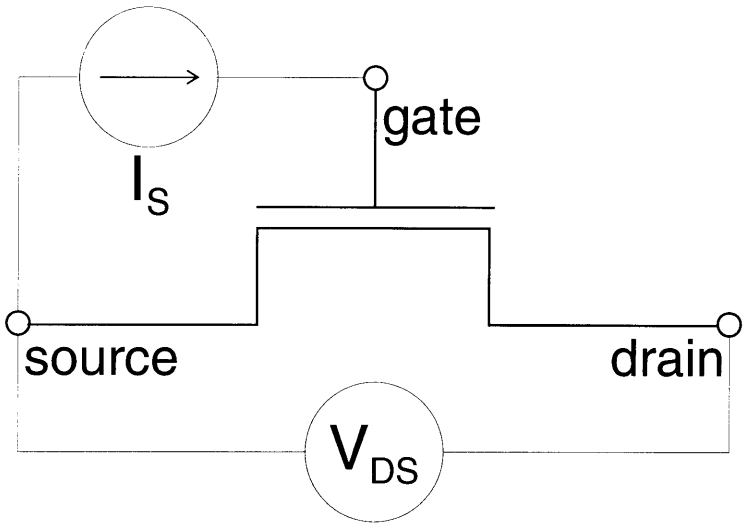

Figure 3.7: Current injection method for measuring parasitic resistance as a function of current, illustrated for r_s.

We extract the parasitic pad capacitance needed in this correction process using a dedicated test structure located near the devices of interest. This test structure has an almost identical layout to that of a working HFET, but lacks the mesa containing the active heterostructure layers. Typical values for C_{gsp}, C_{gdp}, and C_{dsp} are 35 fF, 18 fF, and 29 fF respectively. The value for C_{gsp} is only small correction compared with the intrinsic C_{gs0}, which typically remains between 400 fF and 650 fF for a 0.8 μm $\times$ 200 μm device over most of the useful bias range. In contrast, C_{gdp} and C_{dsp} are of the same order of magnitude as C_{gd0} and C_{ds0}, which average about 5 fF and 25 fF, respectively.

Determining r_s and r_d is somewhat more involved because these values may vary from device to device and are, as we discuss in detail in the next chapter, dependent on I_S and I_D, respectively. While Dambrine *et al.* have illustrated a technique by which these resistances may be extracted directly from the y-parameters with the device biased at V_{DS}= 0 V [54], the method has a drawback in that it extracts r_s and r_d at only at one bias point with no current flowing.

We therefore use a current-injection technique to directly profile r_s vs. I_S and r_d vs. I_D on each device, as illustrated in Fig. 3.7. Although this is a low-frequency technique, the small frequency dispersion shown in Fig. 3.1 indicates that r_s and r_d are rather independent of frequency in our devices. For r_s, we measure V_{DS} as current I_S is injected from gate to source with the drain floating. This measured V_{DS} consists of two potential drops: the one of interest resulting from the parasitic source resistance, and the drop across a portion of the channel near the source through which I_S passes before exiting out the gate. Except at very small currents, however, I_S crowds quite close to the source end of the gate metal and falls off exponentially toward the drain. As we discuss in detail in the next chapter, the channel-resistance component drops rapidly as I_S increases beyond a few mA/mm, with the desired parasitic-source ohmic drop consequently dominating over almost the entire V_{DS} vs. I_S sweep. Finally, the derivative dV_{DS}/dI_S yields r_s. We extract r_d in the same manner.

Because the small-signal model presented here plays a core role in our study of channel transport in this device, we must ensure the quality of our extraction process before proceeding further. Fig. 3.8 illustrates the frequency-dependence of the real and imaginary components of all four de-embedded intrinsic y-parameters for the 0.8 μm $\times$ 200 μm device described above at a typical bias of V_{DS}= 5 V and V_{GS}= 0 V. We note the behavior of $\Im m\,[y_{11}]$, $\Re e\,[y_{21}]$, $\Re e\,[y_{22}]$, and $\Im m\,[y_{22}]$, which yield model parameters C_{gs0}, g_{m0}, g_{d0}, and C_{ds0}, all agree to within 10% with the behavior expected from Eqs. 3.1, 3.2, and 3.4 up to 15 GHz. Beyond 15 GHz, we notice the increasing influence of r_i and other smaller parasitic elements not included in the model [54]. While we do not rely on it for any key physical conclusions in this work, we note that $\Im m\,[y_{12}]$, from which we extract C_{gd0}, is more readily impacted by unaccounted parasitics due to its small magnitude. As a result, it is slightly noisier than the other components and deviates from Eq. 3.2 by 10% at about 8 GHz. We leave a conservative margin and perform all of our parameter extractions at 2 GHz. Finally, we mention that most of the remaining error resulting from the simplification of our model is contained in terms $\Re e\,[y_{11}]$, $\Re e\,[y_{12}]$, and $\Im m\,[y_{21}]$, terms which are

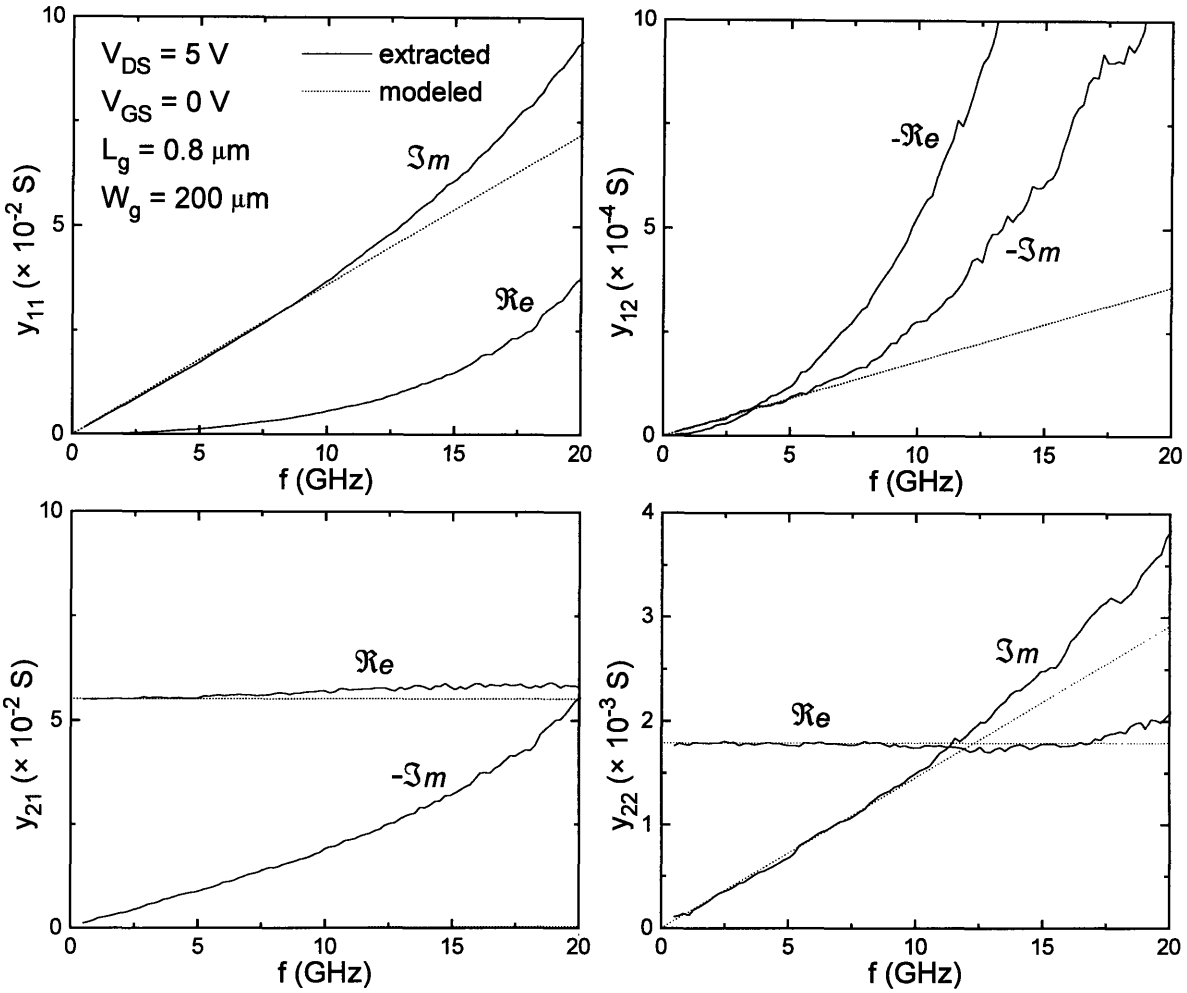

Figure 3.8: Frequency dependence of the extracted and modeled (Eqs. 3.1-3.4) intrinsic y-parameters for a 0.8 μm × 200 μm device at a typical bias of V_{DS}=5 V and V_{GS}=0 V.

fortunately redundant and not used in extracting any of the five model parameter values. These error terms arise primarily from ignoring element r_i. In particular, $\Re e\,[y_{11}]$ and $\Re e\,[y_{12}]$ are not zero as predicted by our model but instead show error terms which are quadratic in ω. We also find that $\Im m\,[y_{21}]$ contains an additional term, linear in ω, that makes it significantly larger than modeled by Eq. 3.3 and not equal to $\Im m\,[y_{12}]$. We avoid drawing any conclusions from these terms in the thesis.

3.3 Summary

We have presented a performance overview of the InAlAs/n^+-InP MIDFET, finding that the device enjoys an attractive combination of high $I_{D,MAX}$, BV_{DS}, g_m, and a_v together with both low g_d and with values of f_T and f_{max} that maintain their peak over a broad V_{GS} swing. At the same time, we find that V_{DS} must exceed a relatively large knee voltage in order to bias the device in its saturation mode, attributed to high source and drain resistances at low I_D. As a whole, these features are well-suited to a variety of high-power telecommunications applications and thus make the device ideal as a vehicle for exploring further the individual contributions of the design's two InP layers in the following chapters. As a key tool for this assessment, we have also developed a small-signal equivalent circuit model for the device, and an extraction procedure for de-embedding the intrinsic model elements from among the parasitics. Our model is both sufficiently accurate to foster physical understanding as well as simple enough for automated parameter extraction over a wide range of biasing conditions and gate lengths.

Chapter 4:

The InP Etch-Stop Layer

The InAlAs/n^+-InP MIDFET employs InP epitaxial layers in two distinct roles. In this chapter, we consider the consequences of the attractive chemical properties of InP, exploring the benefits of using an InP etch-stop layer beneath an n^+-InGaAs recessed cap.

Since reducing parasitic source and drain resistance is crucial for high-power applications, the first section of the chapter explores the role of our cap structure in reducing r_s and r_d. The benefits of a cap layer are conventionally thought to arise primarily from screening Fermi-level pinning and thus reducing channel sheet resistance in the extrinsic source-gate and drain-gate regions as well as from improving ohmic contact resistance. In addition to verifying these mechanisms, which we find to have greatest benefit at low I_D, we also uncover a new phenomenon in which the cap provides a parallel conduction path at larger I_D, bringing down r_s and r_d significantly further.

In the second section of this chapter, we demonstrate that placing the cap structure on top of an InP etch-stopper is highly effective in yielding the benefits of a recessed-cap technology while maintaining a very tight threshold distribution, key for incorporating the devices into manufacturable circuits.

4.1 Cap Performance and Model

In an HFET fabricated using a non-self-aligned technology, the gate metal is simply aligned within a source-drain separation designed sufficiently wide to tolerate photolithographic alignment error. Current must pass through the resulting extrin-

sic source-gate and drain-gate regions in order to access the intrinsic, gated device, adding significant components to the parasitic source and drain resistances (previously illustrated in Fig. 2.8) which are well-known to degrade figures of merit such as g_m, f_{max}, and, at high I_D, f_T as well. The exposed semiconductor surface is subject to Fermi-level pinning in the extrinsic regions which, in the absence of a recessed-cap technology, leads to two major consequences for the behavior of the parasitic source and drain resistances.

Pinning in the extrinsic source-gate and drain-gate regions leads to the formation of depletion regions in the channel layer beneath, reducing the available electron sheet charge density (n_s) there and increasing R_{sh}. The resulting increase in parasitic resistance becomes even worse as the gate-barrier layer is scaled down in an attempt to improve g_m, placing an upper limit on the maximum attainable value of g_m [55].

Since Fermi-level pinning also sets the height of the Schottky-barrier in the intrinsic, gated region of the device, n_s beneath the gate at V_{GS}= 0 V is equal to n_s in the extrinsic source and drain regions. As a result, in a sufficiently short-channel device operating in velocity-saturation, current continuity forces the extrinsic source and drain to enter velocity-saturation as well at a relatively low gate-bias, leading to a dramatic rise in small-signal r_s and r_d and a consequent rapid decline in g_m, f_T, and f_{max} [43].

In the conventional wisdom, a recessed-cap technology is aimed at reducing both of these performance-degrading effects without the need for self-aligning fabrication schemes such as ion implantation which add complexity, degrade BV_{DS}, g_d, C_{gd}, and a_v, and expose the sample to potentially damaging temperatures. As previously illustrated by Fig. 2.2, the surface depletion due to Fermi-level pinning in the extrinsic, capped regions is accommodated by the topmost 200 to 250 Å of the n^+-InGaAs cap rather than by the channel as in the uncapped region. In addition, the Fermi-level (E_F) is set almost 0.4 eV above the n^+-InGaAs conduction band (E_C) in the cap by the presence of large N_D, inducing still more charge in the channel beneath. Indeed,

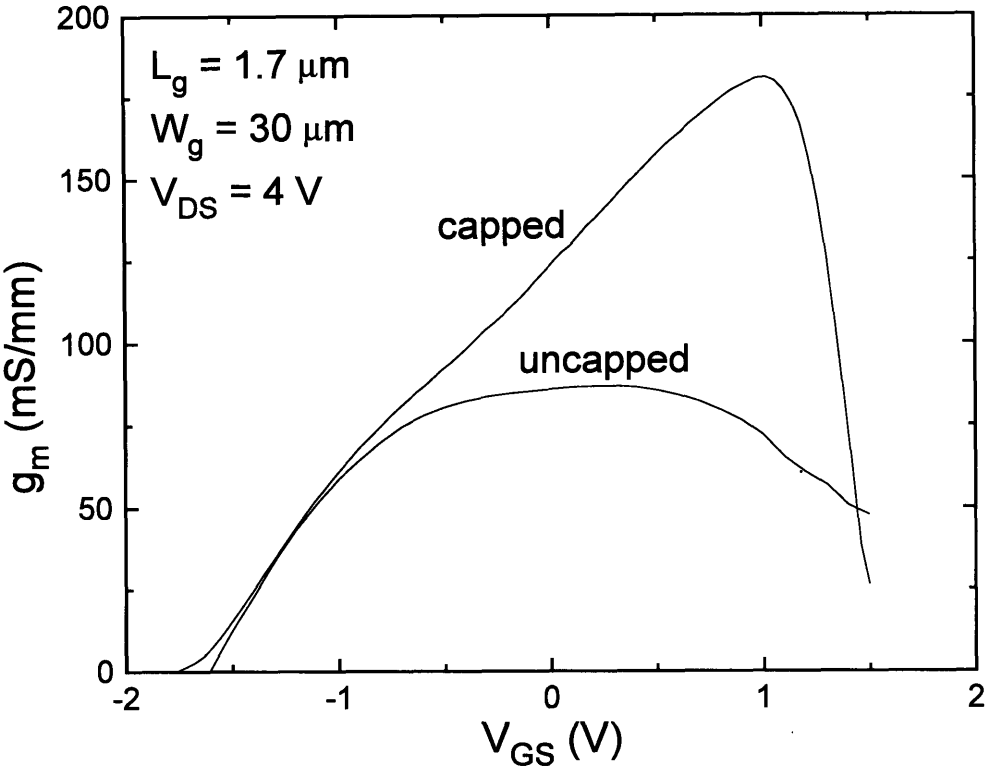

Figure 4.1: g_m vs. V_{GS} at V_{DS}= 4 V for a capped and an uncapped reference 1.7 μm × 30 μm device.

the gate-barrier and topmost region of the channel show an almost flatband condition.

We observe this benefit from the cap experimentally by comparing the channel sheet resistance at low I_D for the extrinsic regions of our capped device with that of a reference device made from the same heterostructure in which the cap has been intentionally etched away during fabrication. As previously listed in Table 2.3, we find that the cap reduces the sheet resistance of the underlying channel from between 1150 and 1350 $\Omega/\square$ down to 600 $\Omega/\square$, a two-fold reduction resulting primarily from the expected increase in n_s and possibly from a consequent improvement in channel electron mobility (μ_e) as well [56].

The benefit of the cap to the device characteristics is illustrated in Fig. 4.1, which shows g_m vs. V_{GS} at V_{DS}= 4 V for both a capped and an uncapped reference 1.7 μm

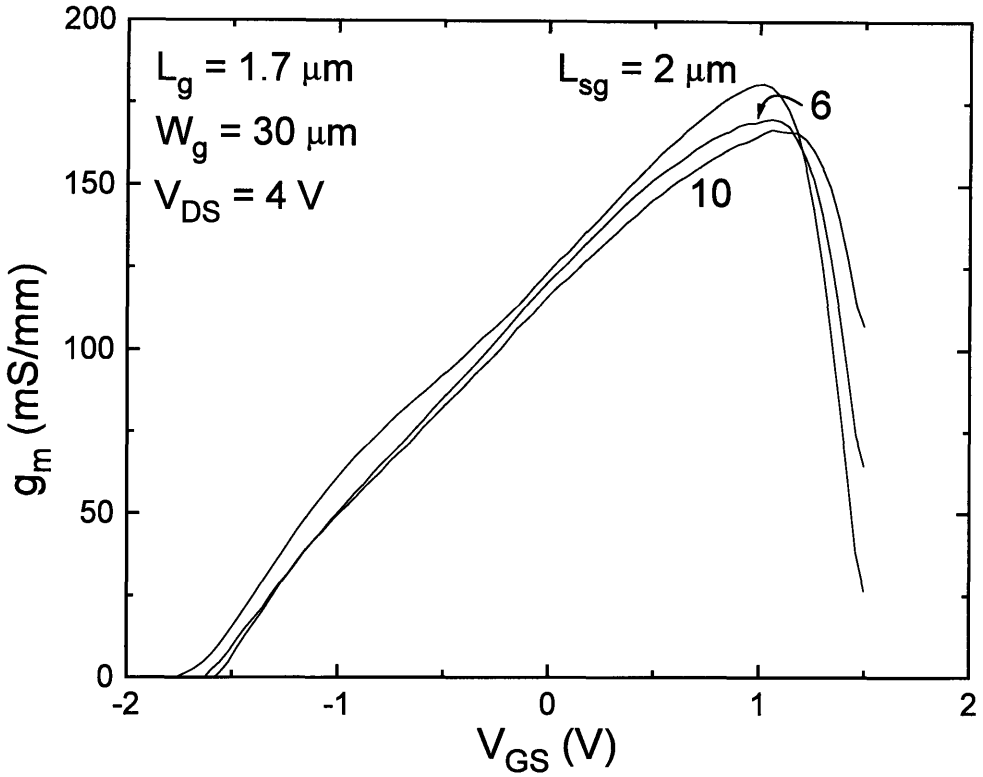

Figure 4.2: g_m vs. V_{GS} at V_{DS}= 4 V for capped 1.7 μm × 30 μm devices with various L_{sg}.

× 30 μm MIDFET. We note that while both devices behave similarly for V_{GS} near V_T, where g_m is low and source resistance has relatively little impact, the capped device peaks at much higher gate bias with a peak value twice that of the uncapped device. This results in over 60% more maximum I_D for the capped device. Furthermore, while g_m for the capped device does not begin to degrade until the onset of significant gate leakage beyond V_{GS}= 1 V, the uncapped device shows a gradual decline in g_m beginning at about V_{GS}= 0.25 V, most likely due to the onset of velocity-saturation in the relatively low-n_s extrinsic device [43].

The benefits of the cap as reported in the literature are generally taken to be limited to those described thus far. However, we have also discovered that the cap may reduce r_s and r_d considerably further through an *additional* mechanism beyond that of a simple increase in extrinsic n_s. Fig. 4.2 shows g_m vs. V_{GS} at V_{DS}=4 V for

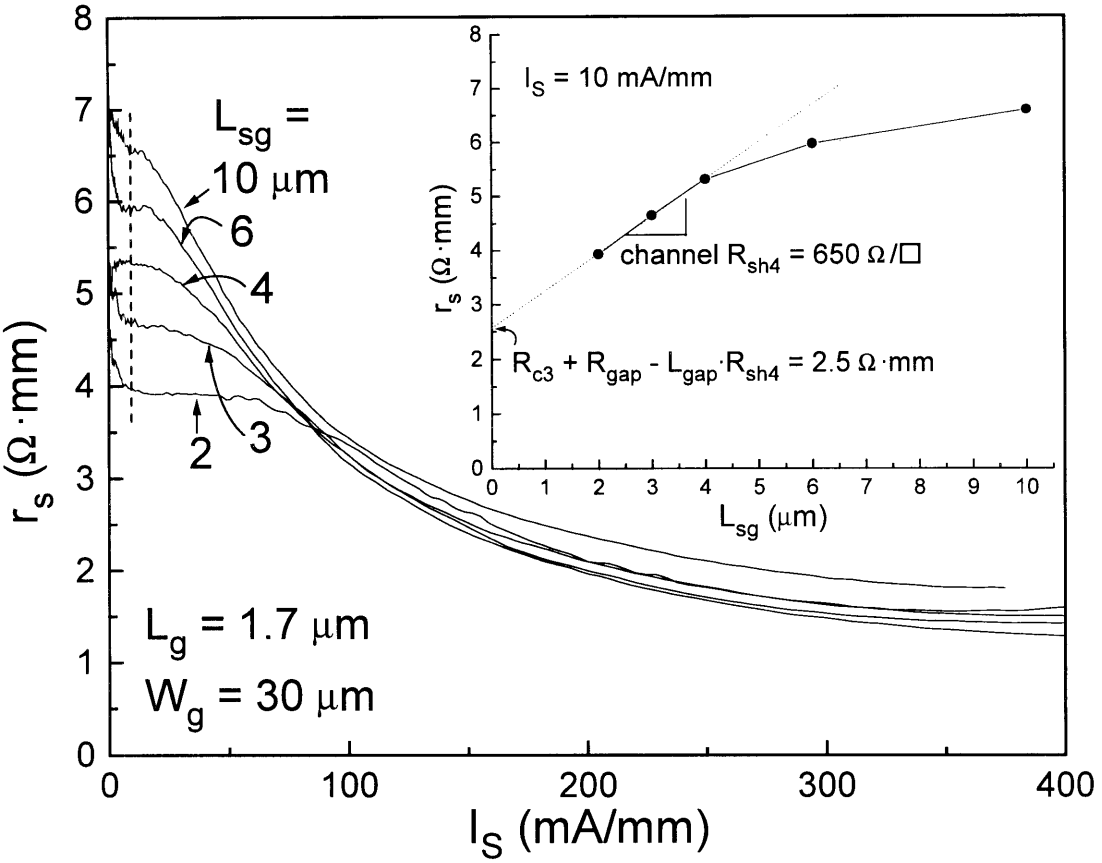

Figure 4.3: r_s vs. I_S for various extrinsic source-gate gap lengths, measured using the current-injection method (see Chapter 3). Inset shows r_s vs. L_{sg} at I_S=10 mA/mm.

three different 1.7 μm × 30 μm devices, each with a different source-gate separation (L_{sg}) between 2 μm and 10 μm. Based on a measured channel R_{sh4} of 600 Ω/□ for the capped extrinsic source, we would expect the parasitic source resistance to increase by almost 5 Ω·mm as L_{sg} is increased from 2 μm to 10 μm, bringing the peak g_m down considerably. Instead, we find only about a 10% reduction in peak g_m between the smallest and largest source-gate separations. If we assume that the intrinsic g_m (g_{m0}) is identical for all three devices at the point of peak observed g_m, the measured differences in peak g_m between any two of the devices may be related to the difference between in r_s through

$$r_s^{(2)} - r_s^{(1)} = \frac{g_m^{(1)} - g_m^{(2)}}{g_m^{(1)} g_m^{(2)}} \tag{4.1}$$

Applying this equation to Fig. 4.2 yields an estimate of 0.34 Ω·mm for the r_s difference between the L_{sg}=2 μm and 6 μm devices, with a 0.5 Ω·mm difference between the L_{sg}= 2 μm and 10 μm devices. Although the accuracy of this estimate is limited by the small statistical variation in peak g_m generally found between even nominally identical devices, the observed r_s variation is still an order of magnitude less than expected based on the capped channel sheet resistance value alone. This behavior suggests that the extrinsic source and drain resistances are highly non-linear, with r_s and r_d dropping considerably at high I_D.

To explore this phenomenon more directly, we employ the current injection technique (see Fig. 3.7) to profile r_s vs. I_S for extrinsic source region in Fig. 4.3, with L_{sg} values of 2, 3, 4, 6, and 10 μm. We may take I_S to be nearly identical to the more commonly referenced I_D for the purposes of this discussion, since I_G is almost negligible over the majority of the useful bias range. We first consider the scan for the L_{sg}= 2 μm device. As I_S is increased above 0, r_s initially drops rapidly up through $I_S \simeq 8$ mA/mm before stabilizing to a constant value of about 4 Ω·mm. This initial drop is due to an unwanted channel-resistance component that is unavoidably measured by the current injection technique and which quickly becomes negligible beyond $I_S \simeq 8$ mA/mm. Thus, the current-injection technique measures an accurate value for r_s over the majority of the scanned I_S range. As I_S is increase further, we find that r_s continues to remain constant at 4 Ω·mm over the low-current range up to $I_S \simeq 80$ mA/mm, the behavior associated with a typical, linear source resistance.

Beyond $I_S \simeq 80$ mA/mm, however, r_s begins a continuous decline, dropping to only $\sim$1.5 Ω·mm by time I_S reaches 400 mA/mm. This drop in r_s is the source of the kink in g_m vs. V_{GS} observed in Fig. 3.1 and permits excellent peak values for figures of merit such as g_m and f_{max} despite a relative high source resistance at low current.

Comparing r_s vs. I_S for varying values of L_{sg} reveals distinct low- and high-current scaling trends. At low currents, where r_s is constant with I_S, we find that r_s increases significantly as L_{sg} is scaled up. We also note that while the L_{sg}=2 μm devices shows a

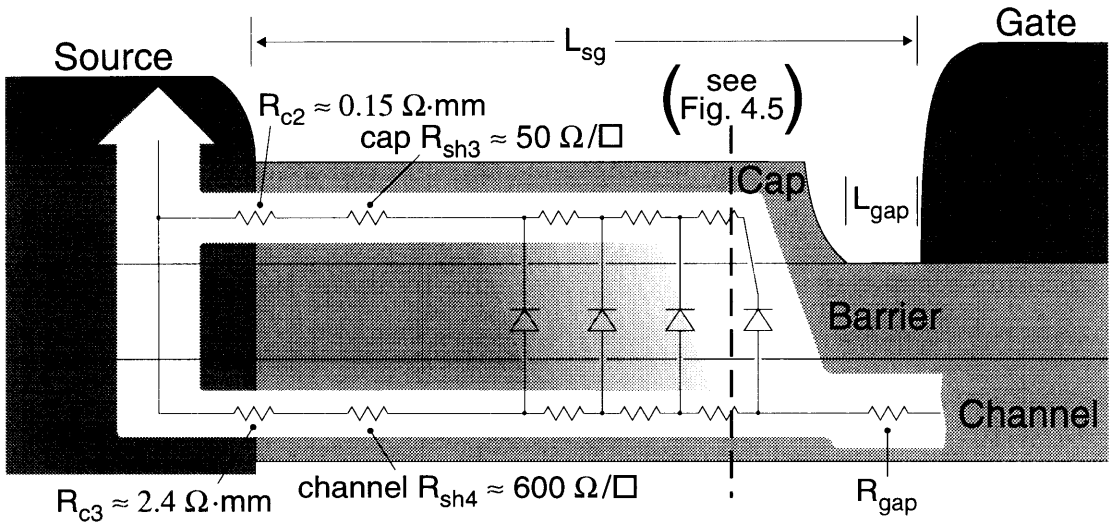

Figure 4.4: Schematic cross-section of the extrinsic source region of an InAlAs/n^+-InP MIDFET, illustrating current transfer into the n^+-InGaAs cap.

relatively large I_S window over which r_s remains constant before declining, this width of this window decreases with increasing L_{sg}, virtually disappearing for L_{sg}>6 μm. As I_S increases, however, and r_s begins to decline, the L_{sg} dependence observed at low currents disappears completely. Indeed, we find that all the curves merge once I_S exceeds 100 mA/mm. This behavior is responsible for the remarkable lack of L_{sg}-dependence in the values of peak g_m for our devices observed in Fig. 4.2.

To account for all features in the behavior of the extrinsic regions of our recessed-cap devices, we propose the model illustrated for the source region in Fig. 4.4. A similar model applies to the extrinsic drain, but with current traveling in the opposite direction. In this model, the cap/barrier/channel layer structure forms an semiconductor-insulator-semiconductor (SIS) diode, with the capped extrinsic source region thus modeled as a distributed diode-resistor network. Because of the presence of this diode and the discontinuity of the cap at the gate recess, almost all current is initially carried by the R_{sh4}=600 $\Omega/\square$ channel layer at small values of I_S and we observe a constant r_s that scales up with increasing L_{sg}.

We explore this scaling behavior in the inset to Fig. 4.3, which plots r_s measured at I_S=10 mA/mm vs. L_{sg}. For the smallest three L_{sg} values, in which the r_s vs. I_S scans show the most distinct flat regions at low I_S, we find that r_s scales up linearly with L_{sg} in a manner consistent with a simple, linear parasitic source resistance with a key component determined by the channel sheet resistance and the dimensions of the source-gate separation. This linear scaling begins to fail for devices with L_{sg}>6 μm in which r_s begins to decline almost as soon as current begins to flow. From the slope of r_s vs. L_{sg} for the L_{sg} values that scale well, we extract a value of 650 $\Omega/\square$ for the capped-channel sheet resistance R_{sh4}, in good agreement with the value of 600 $\Omega/\square$ extracted by FGTLM in Chapter 2. In addition, linear extrapolation to the r_s-axis yields a value of 2.5 Ω·mm corresponding to the residual components of the low-current source resistance not directly related to the capped extrinsic channel. These include three significant terms: channel contact resistance R_{c3}, uncapped gap resistance R_{gap}, and a term $[-L_{gap} \cdot R_{sh4}]$ correcting for the fact that the cap does not extend the full source-gate separation. We ignore both R_{c1} and R_{sh2} (see Fig. 2.8) since they are negligibly small. We can bound L_{gap} to be within 0.1 μm based on the known lateral etch rate and total etch time used in our cap recess, yielding an upper limit for this correction term of $\sim$0.06 Ω·mm. Based on this bound, the extrapolated resistance from the plot, and the value for capped-channel contact resistance listed in Table 2.3, we extract the gap resistance R_{gap} of $\sim$ 0.16 Ω·mm. This value agrees well with the value 0.13 Ω·mm obtained by direct calculation of the product $R_{sh5} \cdot L_{gap}$ (see Table 2.3).

As I_S increases further, current passing through the channel begins to generate a relatively large potential drop in this layer with respect to the source contact. Since little current flows through the R_{sh3}=50 $\Omega/\square$ cap as of yet, the cap remains essentially at the potential of the source. As a result, at sufficiently high I_S the potential across the cap/barrier/channel diode in the region nearest the gate grows large enough for the diode structure to turn on and for significant current to cross over into the cap. The largest current transfer occurs nearest the gate where the potential across the diode

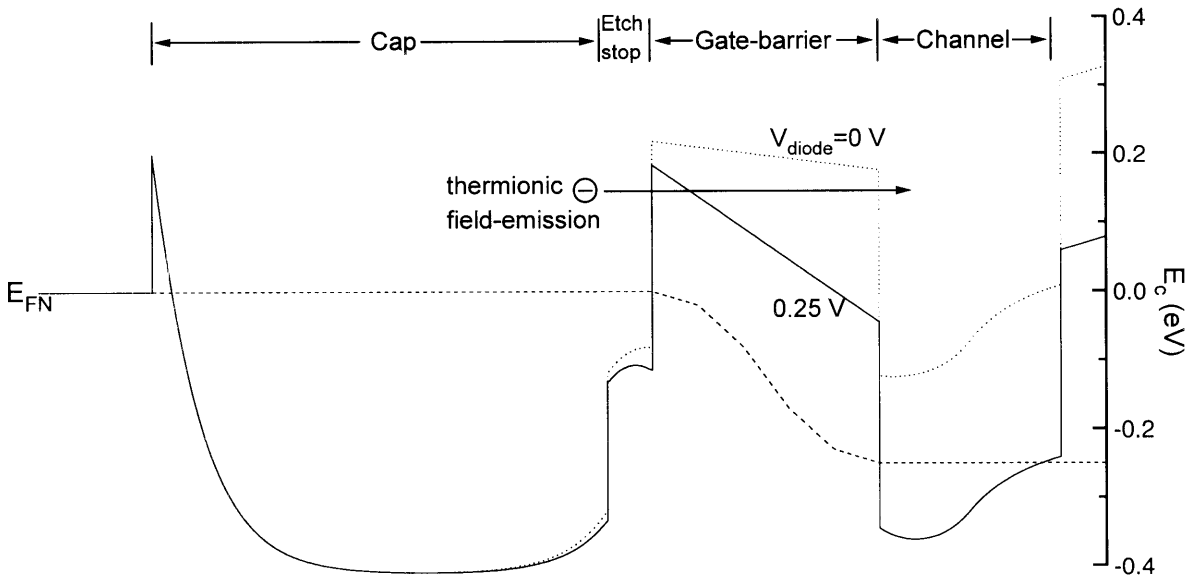

Figure 4.5: Conduction band profile for the cross-section indicated in Fig. 4.4, shown both at equilibrium (I_S=0) as well as at channel-cap potential V_{diode} =0.25 V (I_S≃80 mA/mm for L_{sg}=2 μm), the current at which the diode structure turns on.

structure is greatest, with an exponential falloff toward the source. Since the overall source-gate resistance of the cap, including R_{c2}, is only about 0.25 Ω·mm compared with 3.5 Ω·mm for the underlying channel, r_s declines rapidly with increasing I_S. At the same time, r_s becomes very insensitive to L_{sg} as observed, since all of the current is crowded at the edge of the cap near the gate. To explore the behavior of r_s at high I_S more completely, we can divide it into components. Referring to Fig. 4.4, we obtain

$$r_s \simeq R_{gap} + [R_{c2} + R_{sh3} \cdot (L_{sg} - L_{gap}) + R_{diode}] \,||\, [R_{c3} + R_{sh4} \cdot (L_{sg} - L_{gap})] \quad (4.2)$$

Here, R_{diode} is the effective lumped resistance across the cap/barrier/channel diode, the only term not previously extracted. Substituting values for the known resistance components into this equation yields a value for R_{diode} of ~1.9 Ω·mm. Although we have no independent way to calculate or verify this value, we note that it is at least a non-negative value of reasonable magnitude.

We expect to first observe the onset of cap conduction when the channel-cap potential at the gate end of the extrinsic source (V_{diode}) reaches a particular turn-on voltage, independent of L_{sg}. Since this voltage is attained at lower I_S for the higher-resistance, longer-L_{sg} devices, we expect the decline in r_s for longer L_{sg} devices to begin at lower values of I_S. This is indeed the behavior previously observed in Fig. 4.3. Using the fact that r_s begins to decline at $I_S \simeq 80$ mA/mm for $L_{sg}=2$ μm, together with the values for channel R_{c3} and R_{sh4} previously extracted in Chapter 2, we estimate that the diode turns on at $V_{diode} \simeq 0.25$ V.

Fig. 4.5 shows a BANDSOLV-simulated conduction band diagram for the diode structure, both at equilibrium ($I_S=0$) and at V_{diode} =0.25 V ($I_S \simeq 80$ mA/mm for $L_{sg}=2$ μm), taken at the cross-section indicated by the dashed line in Fig. 4.4. Since we observe little change in the $\sim$ 0.2 eV thermionic barrier height between cap and gate-barrier as the diode moves from equilibrium to turn-on, cap-channel conduction is most likely due primarily to a thermionic field-emission mechanism, as illustrated in the figure.

Although reducing small-signal resistances r_s and r_d is key to improving figures of merit such as g_m, minimizing large-signal resistances R_S and R_D is also important for lowering both the knee voltage in I_D vs. V_{DS} as well as the on-resistance of a device used in the linear regime. To explore this issue further, we consider the data from our current injection technique once again and plot both the source ohmic drop $I_S \cdot R_S$ as well as large-signal R_S vs. I_S for L_{sg}= 2 μm in Fig. 4.6. In contrast with r_s, which drops to 1.5 Ω·mm for I_D= 400 mA/mm, we find that R_S declines to only 2.5 Ω·mm, generating an ohmic drop of about 1.0 V. This ohmic drop, combined with a similar value from the extrinsic drain, accounts for 2.0 V out of the 3.5 V knee voltage observed in I_D vs. V_{DS} (see Fig. 3.2) and is a significant drawback of our current device design.

We find that our cap technology is effective at reducing parasitic source and drain resistance through two distinct mechanisms. By screening surface Fermi-level pin-

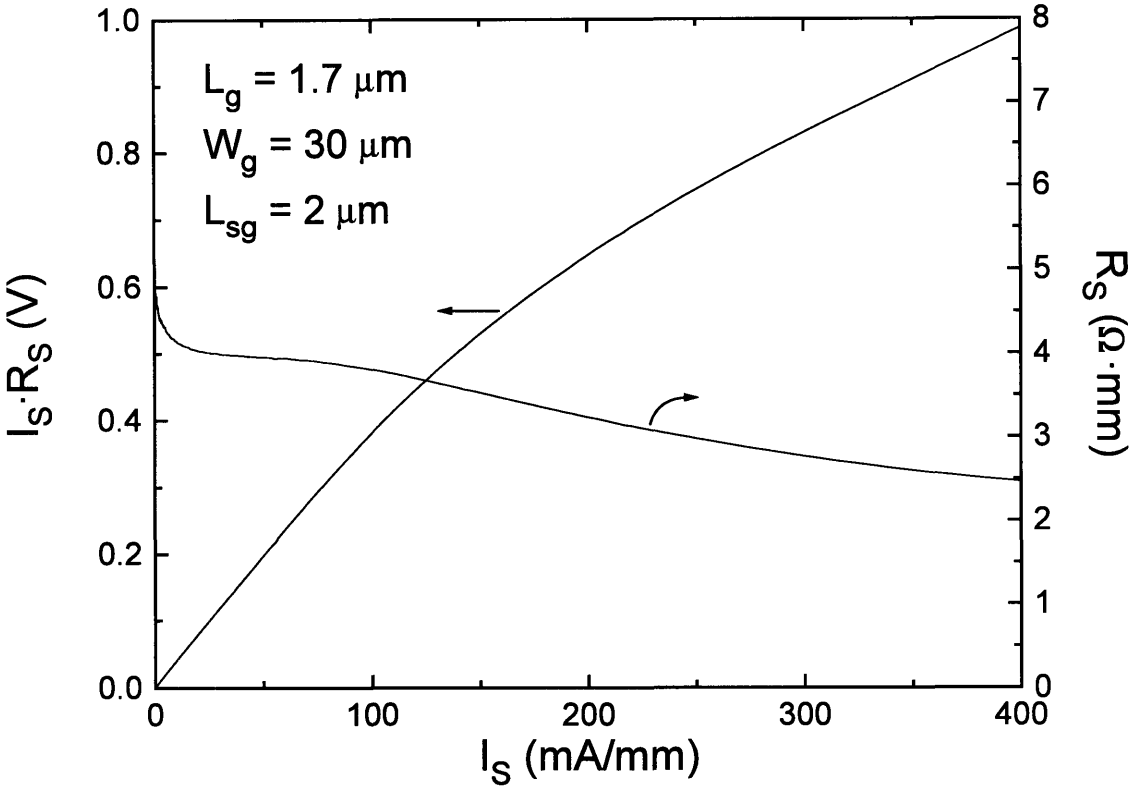

Figure 4.6: $I_S \cdot R_S$ and R_S vs. I_S for L_{sg}= 2 μm, measured using the current-injection method (see Chapter 3).

ning, the cap reduces the underlying channel sheet resistance by a factor of two, most important at low current. This is the mechanism by which a cap structure is conventionally believed to operate. In addition, we have also observed a dramatic reduction in r_s and r_d at moderate-to-high currents via a previously unreported parallel conduction mechanism. This phenomenon opens the possibility for achieving high-performance in a process with large source-drain separation for relaxed lithographic tolerance in a manufacturing environment. Implementing such a technology however, requires that the cap be broken through a recess etch prior to gate deposition, a step which can lead to threshold voltage variation. We consider this issue in the following section.

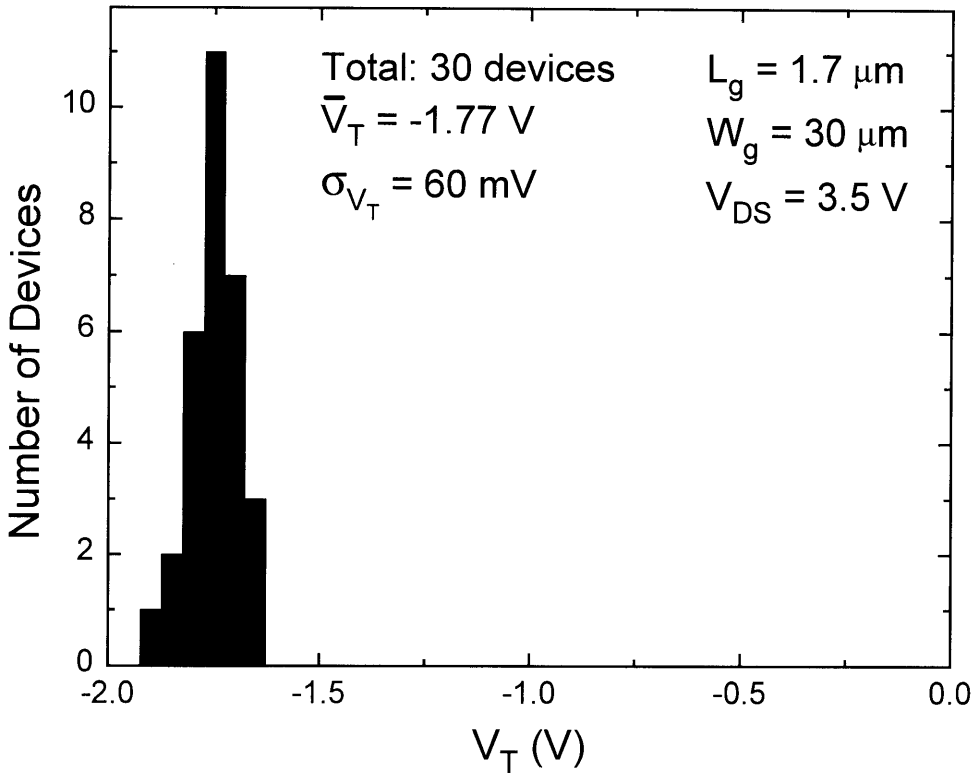

Figure 4.7: V_T distribution for 30 1.7 μm × 30 μm devices.

4.2 Threshold Voltage Distribution

A tight threshold voltage distribution is essential for manufacturing circuits, particularly between pairs of adjacent devices which must be well-matched in order to create high-performance differential-mode circuits. A typical recess-etch process, employing precise etch-timing or iterative I_D-monitoring during the etch, is incompatible with these requirements. The etch depth is difficult to control with sufficient precision using such techniques, causing some of the gate-barrier to be etched as well. This leads to variation in the gate-barrier thickness over the wafer, with a corresponding variation in V_T.

However, the availability of highly-selective etchants for InGaAs over InP, as discussed early in the thesis, makes InP an ideal etch-stop layer to use in a recessed-cap technology. The cap-recess etch stops precisely on the InP etch-stopper, leaving a

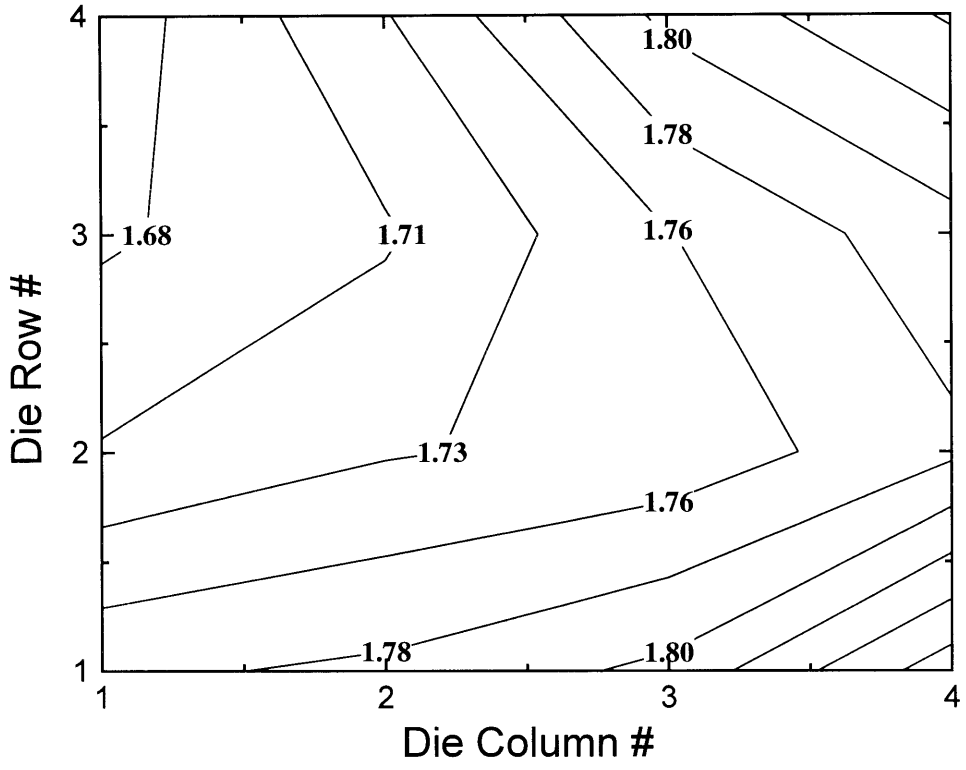

Figure 4.8: Contour map of V_T over sample surface, illustrating growth-related gradient.

well-defined gate-to-channel distance and thus a uniform threshold voltage distribution.

Fig. 4.7 shows a V_T distribution histogram for 30 1.7 μm by 30 μm MIDFET extracted at V_{DS}=3.5 V. The sampled devices are evenly distributed over a typical 16-die sample with an area of approximately 17 mm $\times$ 16 mm. Despite the use of a recessed-cap technology, our sample shows a very tight V_T distribution, with a standard deviation of 60 mV across the sample. Most of this variation actually arises, in fact, from a gentle doping gradient across the sample probably introduced during growth, since we observe a matching gradient in samples fabricated from adjacent wafer pieces. This gradient is illustrated in Fig. 4.8, which shows a contour plot of V_T over the sample surface. The standard deviation between adjacent devices, a figure of merit important for characterizing the matching of differential pairs, is only 13 mV.

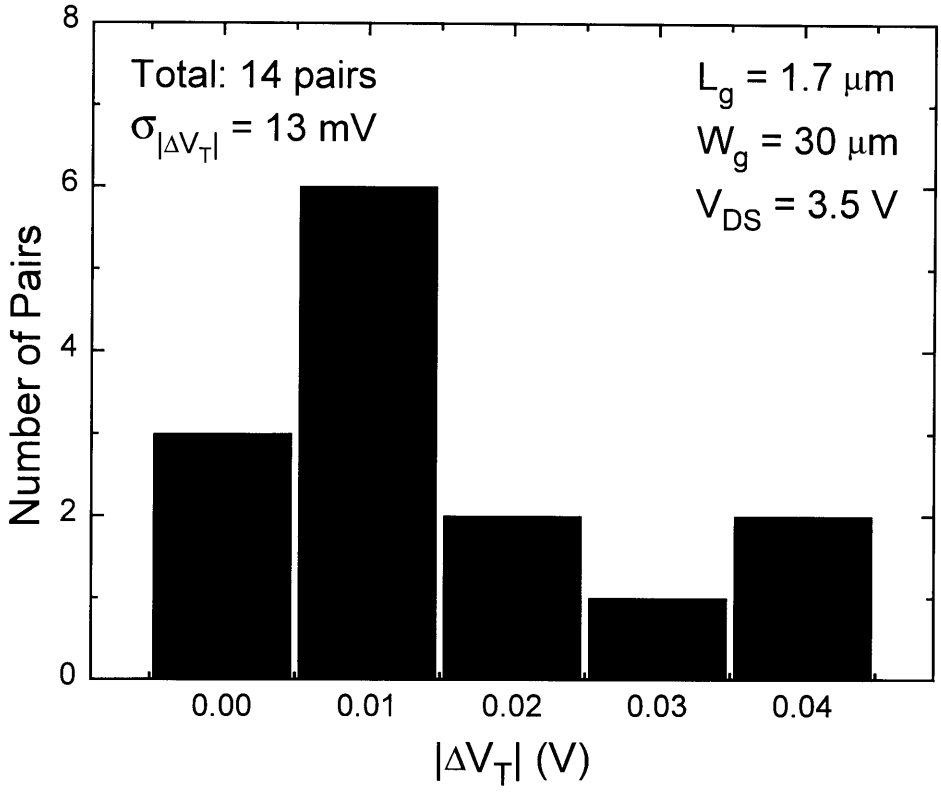

Figure 4.9: $|\Delta V_T|$ distribution for 14 adjacent pairs of 1.7 μm × 30 μm devices.

We illustrate this in Fig. 4.9, a histogram of the distribution of the absolute ΔV_T difference between 14 adjacent device pairs taken from the same sample population.

4.3 Summary

By incorporating a thin InP epitaxial layer as an etch-stopper beneath an n^+-InGaAs cap, we have developed a process that achieves the parasitic source and drain resistance reduction of a recessed-cap technology without sacrificing tight threshold voltage distribution. While a cap is generally believed to reduce channel sheet resistance solely through screening surface Fermi-level pinning, we find an additional mechanism in which the cap provides a parallel conduction path to the channel and carries a majority of the current at high I_D. This previously unreported behavior

leads to a rapid reduction in r_s and r_d with increasing I_D, regardless of gate-source or gate-drain separation, leading to high values for figures of merit such as g_m despite relatively high parasitic resistances at low currents. At the same time, we observe a tight V_T distribution with a standard deviation of 60 mV across the wafer and only 13 mV between adjacent devices. These properties open the possibility for achieving excellent device performance in a manufacturable process with relaxed photolithographic tolerances.

Chapter 5:

The InP Channel

A central distinction of the InAlAs/n^+-InP MIDFET compared with other HFET designs on InP is the use of n^+-InP as the active channel material, exploiting the promising electronic properties of the material. In this chapter, we explore both the benefits as well as the drawbacks involved in using an n^+-InP channel. The first section of the chapter considers the issue of hot electron effects such as impact ionization and real-space transfer. With its wide bandgap, the n^+-InP channel promises to be significantly more immune to these effects compared with InGaAs. We examine electron transport in the next section, employing our small-signal model parameter extraction procedure to profile channel velocity vs. field for devices of various gate lengths.

Our findings reveal that the wide bandgap of InP contributes unequivocally to preventing any discernible impact ionization and thus to reducing I_G, enhancing the on- and off-state BV_{DS}, lowering g_d, and improving a_v compared with typical InGaAs-channel HFET's. We also find that electrons in the InP channel remain cold even at high V_{GS} and V_{DS}, eliminating detectable real-space transfer. On the other hand, we observe an effective electron channel velocity equal only to the material's saturation velocity, and not to its much higher peak velocity. We attribute this reduced effective velocity to the impact of doping on both the steady-state peak velocity of the channel and on the conditions necessary for achieving significant velocity overshoot. These combined properties suggest that the InAlAs/n^+-InP MIDFET is well-suited to a variety of power applications demanding small I_G, high BV_{DS}, low g_d, and large a_v, and for which a moderate frequency response is sufficient.

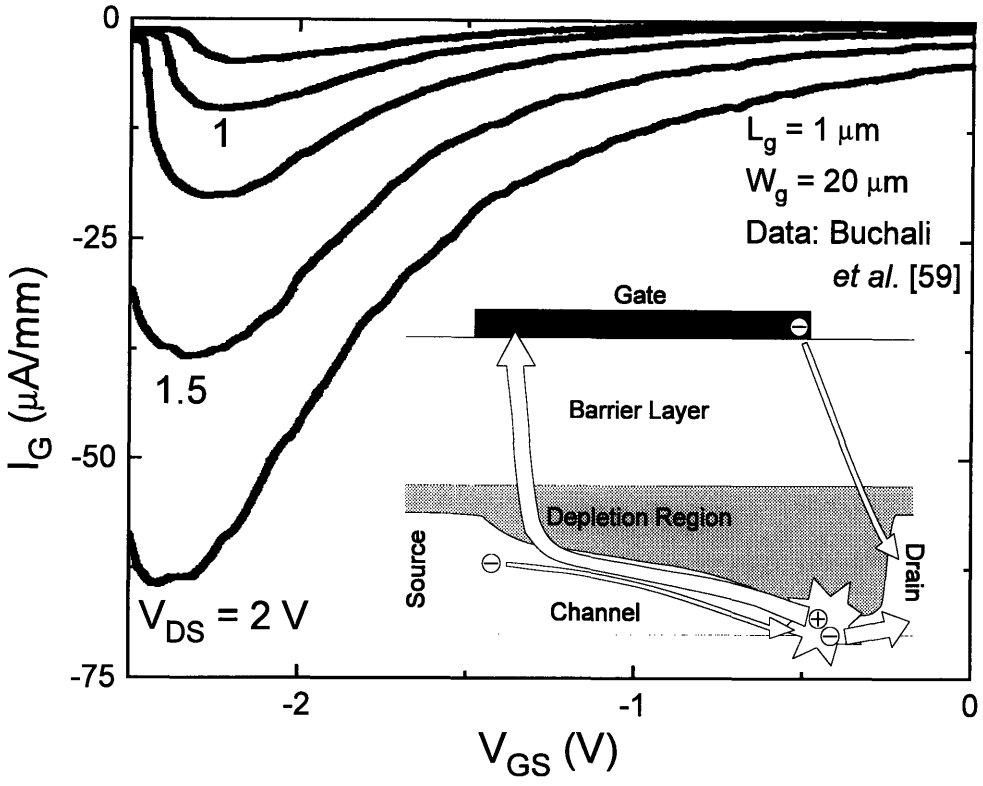

Figure 5.1: I_G vs. V_{GS} for various V_{DS} for a typical InAlAs/InGaAs HEMT from Buchali *et al.* [59]. Inset shows schematic diagram of impact ionization mechanism giving rise to characteristic I_G hump.

5.1 Impact Ionization, Real-Space Transfer, and Breakdown

The large drain-source voltages supported by HFET's used in high-power applications generate extremely high electric fields across the relatively narrow drain regions of the devices. As a result, these HFET's are particularly vulnerable to a number of hot electron effects, including both impact ionization and real-space transfer.

The phenomenon of impact ionization is illustrated in Fig. 5.1, which shows both I_G vs. V_{GS} at several V_{DS} values for a typical InAlAs/InGaAs HEMT from Buchali *et al.* [59] together with an inset diagramming the physical mechanism at work. As they pass from the source end of the channel into the high-field drain region, channel

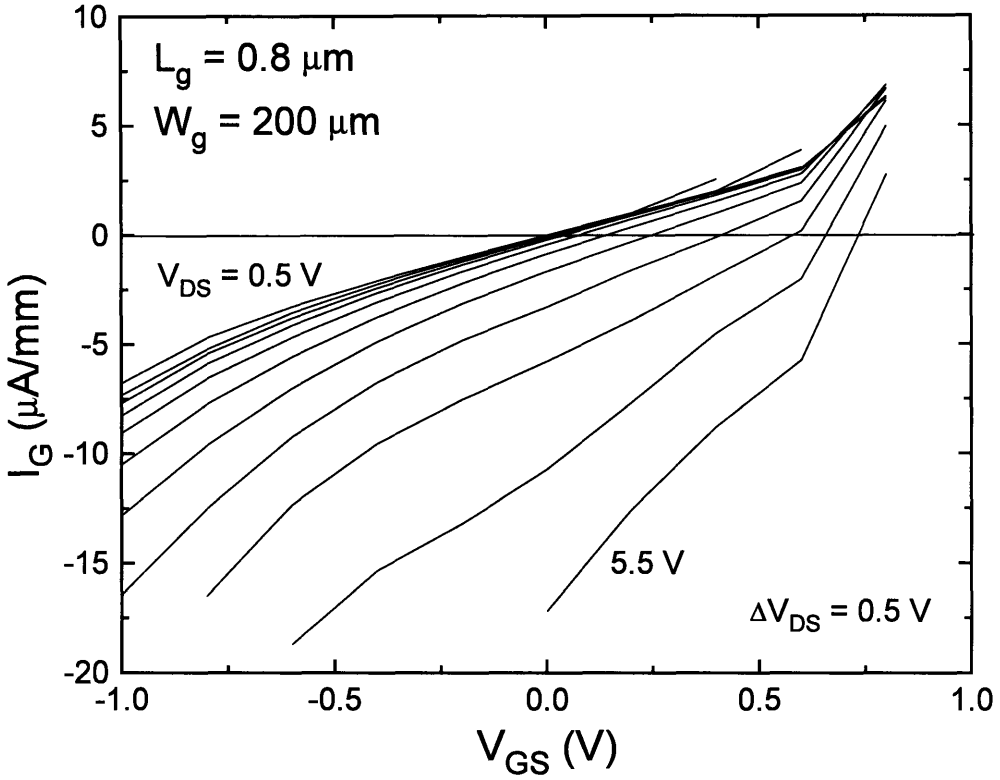

Figure 5.2: I_G vs. V_{GS} for various V_{DS} for a typical 0.8 μm by 200 μm InAlAs/n$^+$-InP MIDFET.

electrons may gain sufficient energy to generate an electron-hole pair in an impact ionization process. A significant quantity of excess electrons and holes may be created in this way as the generated carriers are themselves accelerated by the high drain field and produce additional impact ionization events. The ionized holes travel back through the channel toward the source, with most easily escaping over the gate barrier and creating the large negative-going "hump" in I_G vs. V_{GS} shown in the figure [11, 12, 57, 58, 59, 60]. The excess, randomly-generated gate current in this signature hump contributes to unwanted input noise and reduced sensitivity in device employed in optoelectronic receiver applications. An excess current of ionized electrons also exits the drain. Since this current is a strong function of electric field and thus of V_{DS}, impact ionization leads further to degraded on- and off-state BV_{DS}, high g_d, and reduced a_v.

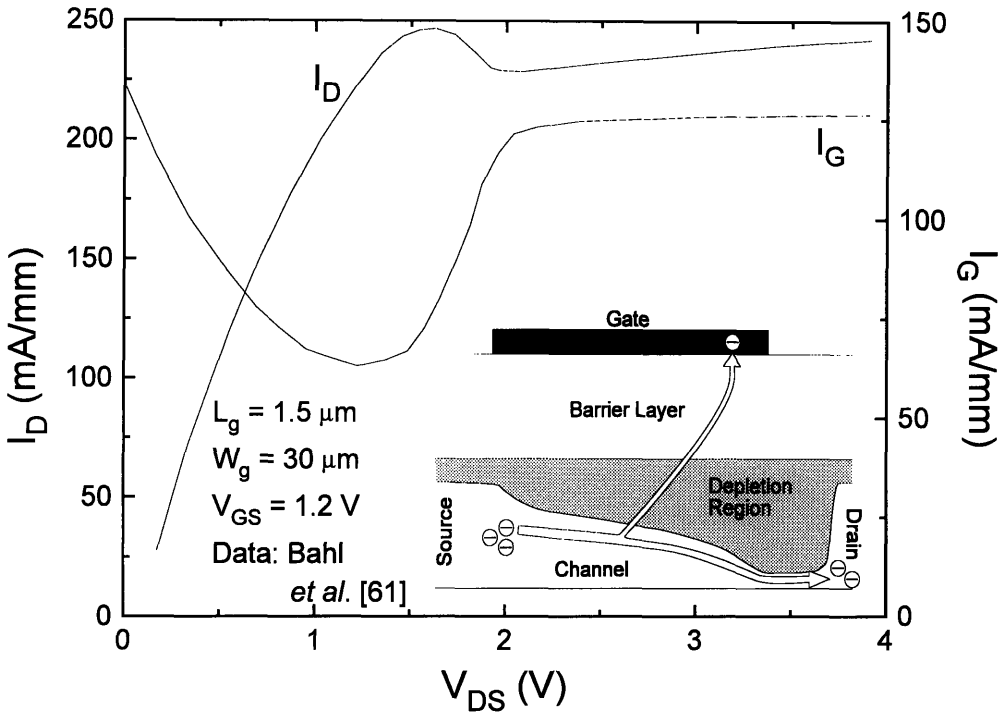

Figure 5.3: I_D and I_G vs. V_{DS} for a typical gate bias for an InAlAs/n$^+$-InGaAs MIDFET from Bahl *et al.* [61]. Inset shows schematic diagram of real-space transfer mechanism giving rise to characteristic I_D dip and I_G rise.

By requiring a greater energy to initiate an ionization event due to its wider bandbap, we expect the InP channel to reduce impact ionization in the InAlAs/n$^+$-InP MIDFET significantly compared with InGaAs-channel devices, leading to lower I_G, improved BV_{DS}, reduced g_d, and increased a_v. To look for the gate current hump in our devices, we plot I_G vs. V_{GS} for several values of V_{DS} for a typical 0.8 μm $\times$ 200 μm device in Fig. 5.2. Significantly, the curves are completely free of the characteristic impact ionization hump at all measured V_{DS} values despite the type II band alignment of the InAlAs/InP system (i.e. negative channel-to-barrier ΔE_v), strongly indicating that the devices are completely free of this deleterious effect.

In addition to initiating ionization events, hot channel electrons passing under the gate may experience real-space transfer or scattering over the conduction band

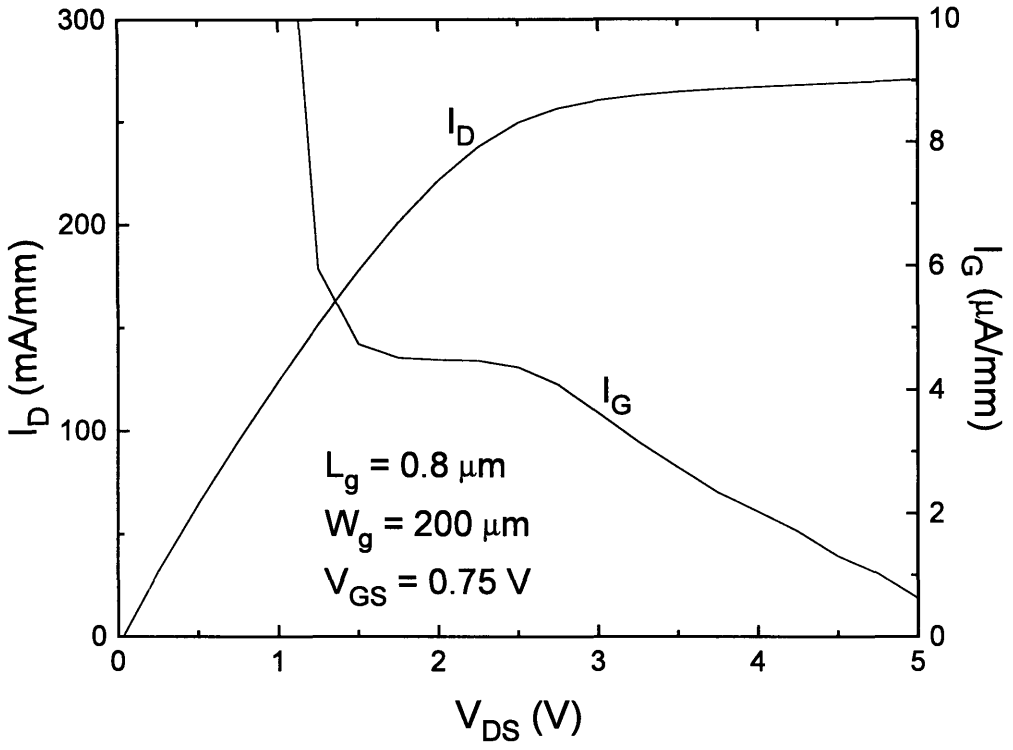

Figure 5.4: I_D and I_G vs. V_{DS} at V_{GS}=0.75 V for a typical 0.8 μm by 200 μm InAlAs/n$^+$-InP MIDFET.

discontinuity of the gate-barrier and exit through the gate rather than into the drain. We show the signature of this effect in Fig. 5.3, which shows both I_D and I_G vs. V_{DS} at a typical gate bias for a reported pseudomorphic InAlAs/n$^+$-InGaAs MIDFET from Bahl *et al.* [61] together with an inset illustrating the phenomenon. Despite the enriched, 52% AlAs mole fraction used in the InAlAs gate barrier of this device, we note a distinctive dip in I_D and rise in I_G with increasing V_{DS} as the device enters saturation mode. Hot electrons may also scatter over the buffer conduction band discontinuity, allowing current to pass through the buffer and consequently leading to an excessive V_{DS}-dependence for I_D. The combined result is a degradation of key device figures of merit.

We explore the issue of real-space transfer in our devices in Fig. 5.4, which shows I_D and I_G vs. V_{DS} at V_{GS}=0.75 V (close to the top of the useful gate swing), for

a typical 0.8 μm $\times$ 200 μm MIDFET. In contrast to the InGaAs-channel device of Fig. 5.3, the InP-channel HFET shows a monotonic rise in I_D with V_{DS}, flattening off with no dip or negative-differential-resistance region to indicate real-space transfer as the device enters its saturation mode. The behavior of I_G similarly shows no real-space transfer rise, confirming that the phenomenon is indeed negligible in our devices. This result suggest that electrons in the n^+-InP channel remain cold even at high V_{DS} and V_{GS}.

The absence of both impact ionization and real-space transfer in our devices contributes a number of key benefits to the InAlAs/n^+-InP MIDFET compared with InGaAs channel devices. One benefit is a significantly lower I_G. We find that $|I_G|$ remains less than 17 μA/mm over the V_{GS} range of useful g_m between -1 V and 1 V, at a typical V_{DS} of 4 V. This value is up to 60 times lower than for reported lattice-matched InGaAs HEMT's operated at a lower V_{DS} of 2 V (including devices with channel edge isolation) [11, 12, 59]. In fact, it could be reduced still further through the use of a strained (AlAs-rich) gate barrier.

A second benefit, which is further enhanced by the excellent electron confinement of the thin MIDFET channel, is very low g_d and good a_v, as previously presented in Chapter 3, despite only modest values for g_m. At 2 GHz and V_{DS}=5 V, for example, g_d remains below 5 mS/mm over a V_{GS} swing of 2 V. We find that g_d rises with V_{GS} at a rate similar to g_m, leading to a broad a_v vs. V_{GS} plateau exceeding a value of 30.

A particularly important benefit to the InAlAs/n^+-InP MIDFET stemming primarily from the absence of impact ionization is its excellent breakdown voltage behavior. Since this deleterious effect is initiated in an FET by high-energy electrons moving through the drain end of the channel, the phenomenon becomes more pronounced with increasing I_D. Consequently, BV_{DS} in a device suffering from the effect degrades from its off-state value as the device is turned on, as is reported in the literature for typical InAlAs/InGaAs HFET's [6]. Our devices behave quite differently, however, as illustrated in Fig. 5.5 which shows I_D vs. V_{DS} for a 0.8 μm $\times$ 200 μm

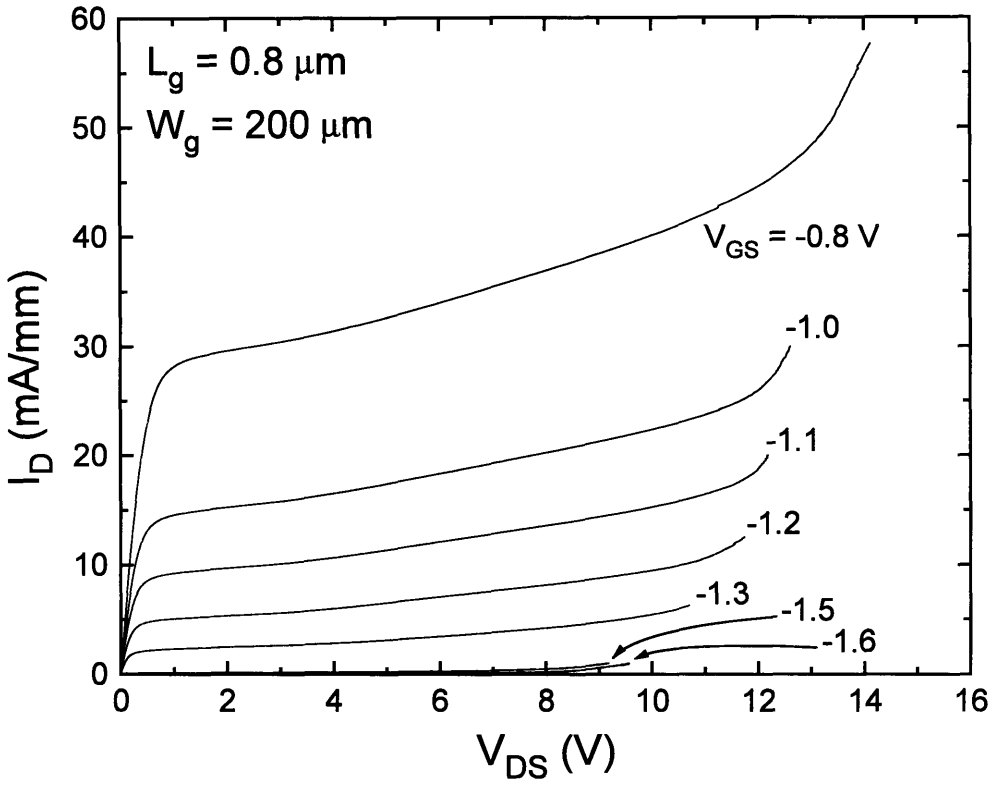

Figure 5.5: I_D vs. V_{DS} for a 0.8 μm × 200 μm MIDFET showing I_D-dependence of BV_{DS} for V_{GS} near and above threshold.

device with V_{GS} varied from just below to moderately above threshold. Rather than degrading with increasing I_D, we find that BV_{DS} in our devices actually *increases* as the device is turned on, confirming that breakdown is not limited by impact ionization in the channel.

To explore the breakdown mechanism further, we plot V_{DS}, V_{DG}, and I_G vs. V_{GS} for the same device in Fig. 5.6, using the Drain-Current Injection technique of Bahl and del Alamo described in [63] with I_D=1 mA/mm. We measure an excellent off-state BV_{DS} and BV_{DG} values of 10 V and 12 V, respectively. We also note that breakdown in our device occurs at constant V_{DG} regardless of V_{GS}, with all injected drain current emerging from the gate. This behavior, which is observed for all values of L_g in the examined range, confirms that breakdown occurs through a *gate-drain* mechanism, such as the thermionic field-emission of electrons from the gate metal,

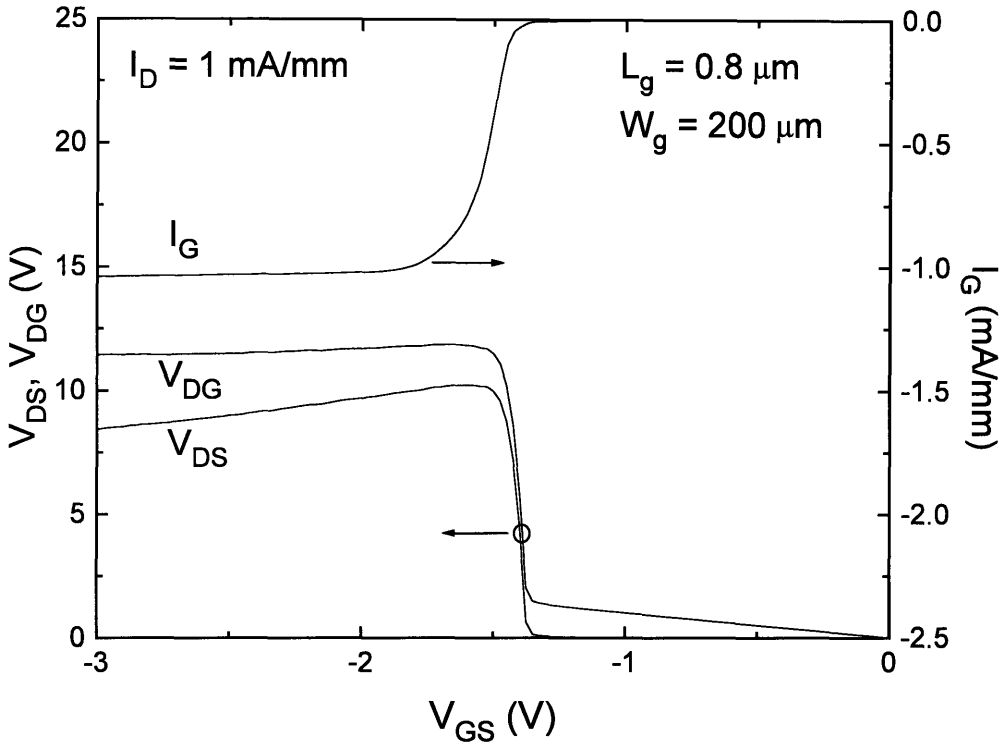

Figure 5.6: V_{DS}, V_{DG}, and I_G vs. V_{GS} at I_D=1 mA/mm for a 0.8 μm × 200 μm MIDFET.

through the gate-barrier, and into the n^+-$In_{0.53}Ga_{0.47}As$ cap.

In summary, our results indicate that the n^+-InP-channel HFET is free from hot electron effects such as impact ionization and real-space transfer, an advantage over InGaAs-channel designs for applications emphasizing small I_G, low g_d, and high BV_{DS}. Indeed, our findings point to considerable room to improve these figures of merit still further, through well-known methods such as the use of a pseudomorphic, AlAs-rich gate barrier layer [37] as well as the use of a double-recessed cap structure [64]. At the same time, however, the fact that electrons in the n^+-InP channel remain cold even at high V_{GS} and V_{DS} suggests a possible tradeoff in the maximum electron velocity that may be achieved in the channel, an issue which we explore in the next section.

5.2 Electron Transport

Except in extremely short-gate devices in which parasitics can become dominant, the electron transit time (τ_t) from source to drain in the channel of an HFET is the key quantity determining the high-frequency performance of the device. For devices of given L_g, this transit time is in turn determined by the velocity of channel electrons. We have found in the previous section that an InP channel can contribute significant benefits to a power HFET compared with the use of InGaAs, such as immunity to impact ionization. We now consider the consequences to the electron velocity and high-frequency performance that result as well.

The relative merits regarding transport between InGaAs and InP are not necessarily clear *a priori*, since each material shows particular advantages in a different electric field range. As we noted in Fig. 1.1 for undoped material, the low-field electron mobility (μ_e) is greater for InGaAs compared with InP, giving InGaAs a potential advantage for devices in which the effective electric field remains below ~5 kV/cm. As the electric field increases, however, the electron velocity in InP attains a greater peak value, over 2.6×10^7 cm/s, and, even after this peak begins to fall, maintains greater electron velocities over a wide range of electric fields out to 100 kV/cm. In shorter gate length devices with higher channel electric fields, this mid- to high-field behavior may allow InP to rival or surpass the high-frequency performance of InGaAs. Complicating the predication of results is the issue of doping, which is known in many bulk materials not only to degrade mobility, but to bring down peak velocity as well, leading to a monotonic rise in electron velocity toward a high-field saturation value that is relatively unaffected by the doping. Doped-channel InGaAs devices have, nevertheless, demonstrated high-frequency performance beyond expectation from bulk material properties, however, presumably due to non-stationary transport effects. The situation regarding doped InP-channel devices has not yet been reported.

In this section, we focus on understanding transport in the n^+-InP-channel. Since both gate-source bias and gate length impact transport directly by determining the electric field profile in the channel, our approach is to define an effective electron velocity (v_e^{eff}) for the channel and profile this quantity with both V_{GS} and L_g, mapping out the transitions between the various transport regimes [35].

One method for studying v_e^{eff} often employed in the literature is to consider the behavior of the product $f_t \cdot L_g$. However, while this product is closely related to v_e^{eff} in the absence of parasitics and for devices in which C_{gd} is negligible compared with C_{gs}, such conditions rarely hold in real devices.

In order to be as accurate as possible in this work, we instead employ our small-signal equivalent circuit extraction procedure presented in Chapter 3. Using this procedure, we extract the model elements g_{m0} and C_{gs0}, free of parasitic influence, and combine these parameters through Eq. 3.5 to obtain v_e^{eff}. Before proceeding further, we mention at this point that care must be taken in interpreting v_e^{eff} as defined in this manner. Strictly speaking, Eq. 3.5 is derived under the assumption of velocity saturation throughout the entire intrinsic device, where electron velocity is relatively insensitive to field at high electric fields. Since we are primarily interested in observing the transition to the velocity-saturation transport regimes and pinpointing the electron velocity in this performance-limiting case, however, the expression is well-suited to our purpose.

We begin by examining the individual behaviors of g_{m0} and C_{gs0}, both as a means of gauging the reliability of our extraction procedure and because g_{m0} is interesting in its own right as an upper limit for g_m as parasitic resistance is reduced. We recall from Chapter 3 that the parasitic capacitance values needed for the extraction procedure are measured using a dedicated test structure located close by to the device under test. Because the procedure is considerably more sensitive to error in r_s and r_d, however, we profile these quantities vs. current on the very same devices being studied. The procedure is occasionally destructive to the device, and so is performed last following

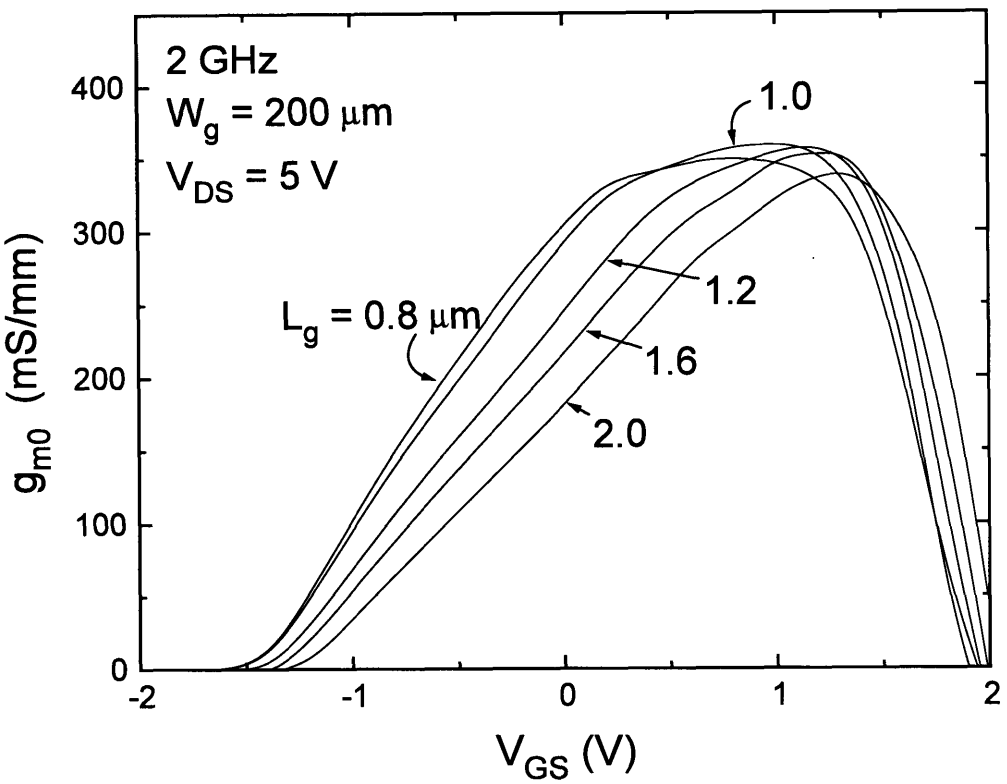

Figure 5.7: Extracted g_{m0} vs. V_{GS} at V_{DS}= 5 V for various values of L_g.

all other measurements.

Fig. 5.7 shows extracted g_{m0} vs. V_{GS} at V_{DS}=5 V for values of L_g between 0.8 μm and 2 μm. For the L_g=2 μm device, we observe a linear rise in g_{m0} with V_{GS} over the entire V_{GS} range from threshold until the onset of significant gate leakage at about 1.25 V. This behavior is consistent with a device in which transport is mobility-limited and sensitive to electric field up to at least V_{GS}=1.25 V [35]. As L_g is scaled down, however, we note two trends. First, the slope of the g_{m0} vs. V_{GS} rise increases, again consistent with the mobility-limited transport. Second, we notice that for for devices with $L_g \leq$ 1.6 μm, g_{m0} begins to become insensitive to V_{GS} at high V_{GS} and flattens into a plateau. The plateau value of g_{m0}, about 350 mS/mm, becomes insensitive to L_g as well. This behavior, which is not visible in g_m vs. V_{GS} due to the influence of non-linear r_s (see Fig. 3.1), indicates the onset of velocity saturation in the channel

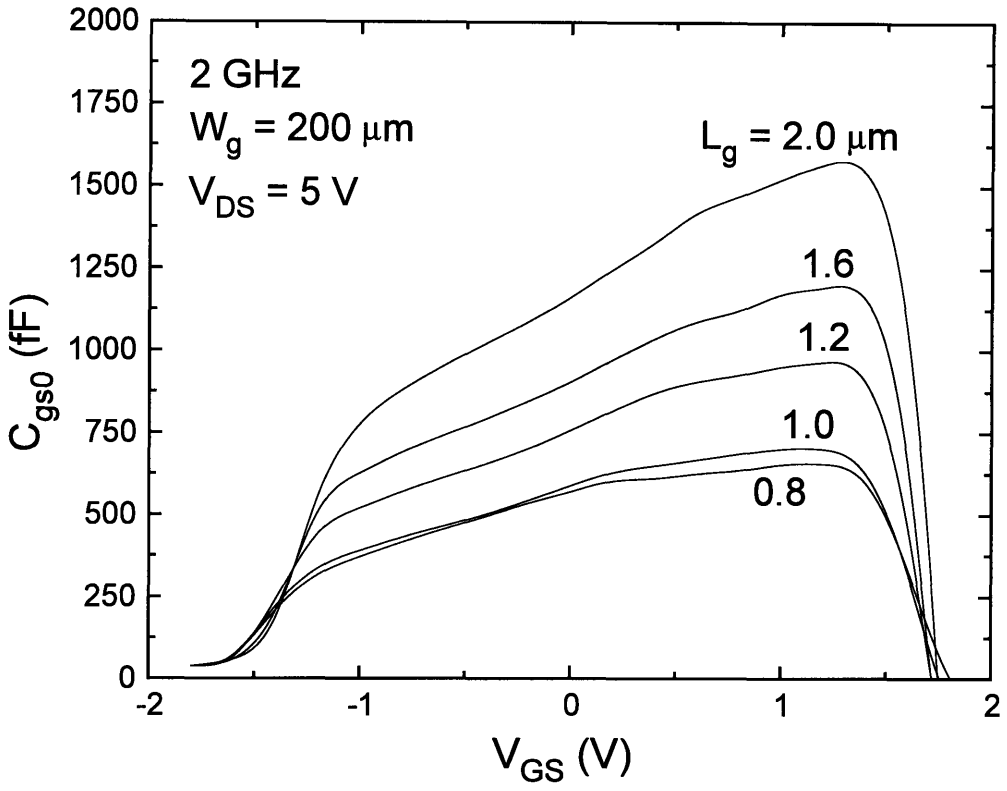

Figure 5.8: Extracted C_{gs0} vs. V_{GS} at V_{DS}= 5 V for various values of L_g.

[35].

At sufficiently high V_{GS} (about 1.25 V in our devices), g_{m0} falls off rapidly. This fall-off is due to the breakdown of our equivalent circuit model with a rapid rise in gate conductance as the gate/barrier/channel diode turns on, which we do not take into account. Since the device is largely useless beyond this point, we make no effort to model its behavior beyond this gate bias.

We look next at the behavior of C_{gs0} vs. V_{GS}, shown in Fig. 5.8. As a general feature, we note that C_{gs0} indeed scales up with L_g, and thus with the area of the gate, as expected. We can gain a more rigorous understanding of the V_{GS} behavior of C_{gs0}, however, by comparing our measured results with those of a model.

In all of our devices, L_g is significantly larger than the gate-channel separa-

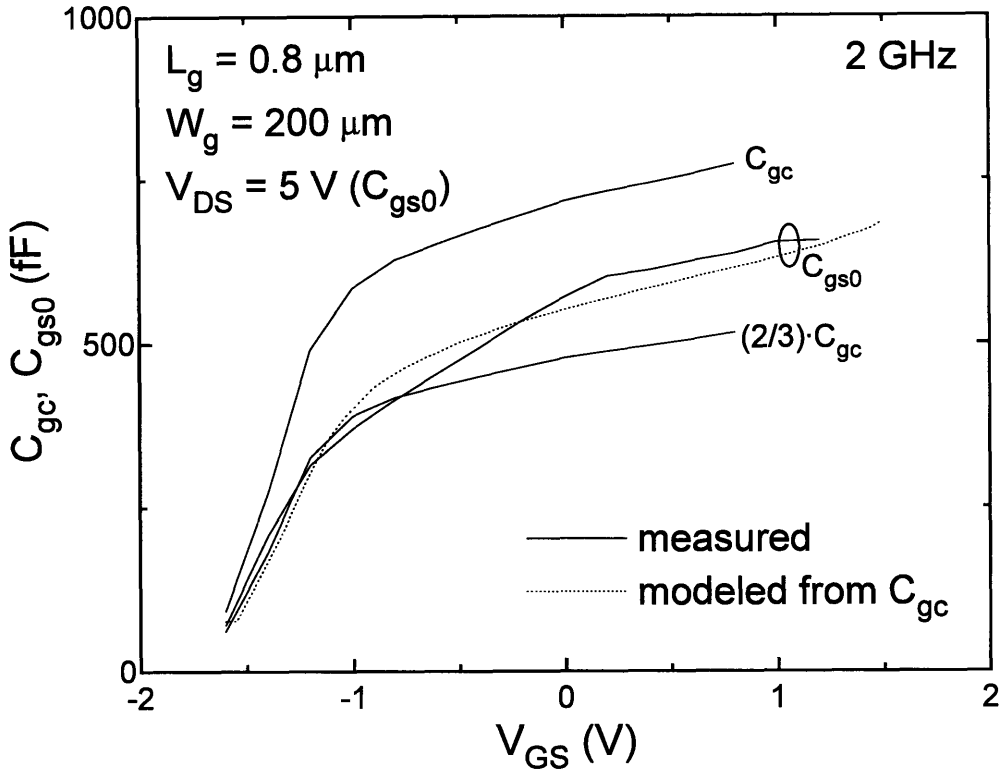

Figure 5.9: C_{gc} (full-scale and $\times\frac{2}{3}$) as well as measured and modeled C_{gs0} vs. V_{GS} for a 0.8 μm $\times$ 200 μm MIDFET.

tion. Consequently, we can model C_{gs0} for our full three-terminal HFET biased in saturation-mode by invoking the gradual channel approximation. This approximation requires that we have either models or actual data describing both the one-dimensional gate-channel charge control for our heterostructure as well the electron velocity-field characteristics of channel.

We first explore the one-dimensional charge control of our device, considering the two-terminal gate-channel or diode capacitance (C_{gc}) which is measured as the sum of extracted C_{gs0} and C_{gd0} for a device biased at V_{DS}= 0 V. Fig. 5.9 shows C_{gc} vs. V_{GS} at 2 GHz for a 0.8 μm $\times$ 200 μm device. We note that C_{gc} initially rises rapidly with V_{GS} as V_{GS} increases beyond threshold and a conducting channel is established, and subsequently flattens out into a more gentle slope. This behavior is very similar to that of the Metal-Oxide-Semiconductor (MOS) capacitor, but with

a more pronounced slope due to the non-negligible thickness of our device channel compared with the gate-channel separation.

Next, we must select a model for channel electron transport in order to complete our three-terminal HFET capacitance model. Trying $v_e = \mu_e \mathcal{E}$ for all $\mathcal{E}$ leads to a prediction for C_{gs0} vs. V_{GS} that is within 10% of $\frac{2}{3}C_{gc}$ regardless of the value of μ_e employed. A comparison with our measured C_{gs0} reveals that this prediction is too small, however, and has a slope with respect to V_{GS} which is too gentle as well. The failure of this simple prediction supports our earlier preliminary conclusions based on the behavior of g_{m0} and f_T vs. V_{GS} that a mobility-limited transport model does not fully explain the behavior of our smallest gate-length devices.

We achieve a more accurate modeling of C_{gs0} by instead employing a simple two-segment piecewise-linear model for electron transport in which v_e is given by $\mu_e \mathcal{E}$ at low fields and saturates to v_{sat} when this velocity is reached. Fig. 5.9 shows the resulting modeled C_{gs0} vs. V_{GS}, compared with the measured values, for a 0.8 μm $\times$ 200 μm device, using μ_e=1100 cm^2/V·s and v_{sat}= 1 $\times$ 10^7 cm/s. Both of these tranport parameters follow from discussion presented later in this chapter. Considering the figure, we note excellent agreement between our model and the measured data. Indeed, this agreement reveals that the larger slope with respect to V_{GS} of C_{gs0} compared with $\frac{2}{3}C_{gc}$ is due to charge being modulated in the drain-bottleneck region of the device. Such behavior indicates that the drain end of the channel is not pinched-off, but rather widens with increasing V_{GS} as expected for a device entering into velocity-saturation-limited transport.

Having extracted both g_{m0} and C_{gs0} and established confidence in their proper behavior, we estimate v_e^{eff} in the n$^+$-InP channel using Eq. 3.5. In order to gain as fundamental a view of channel transport as possible, we examine v_e^{eff} vs. $\mathcal{E}^{eff}$, where $\mathcal{E}^{eff}$ is an effective channel electric field, defined through

$$\mathcal{E}^{eff} = \frac{V_{GS0} - V_T}{L_g} \tag{5.1}$$

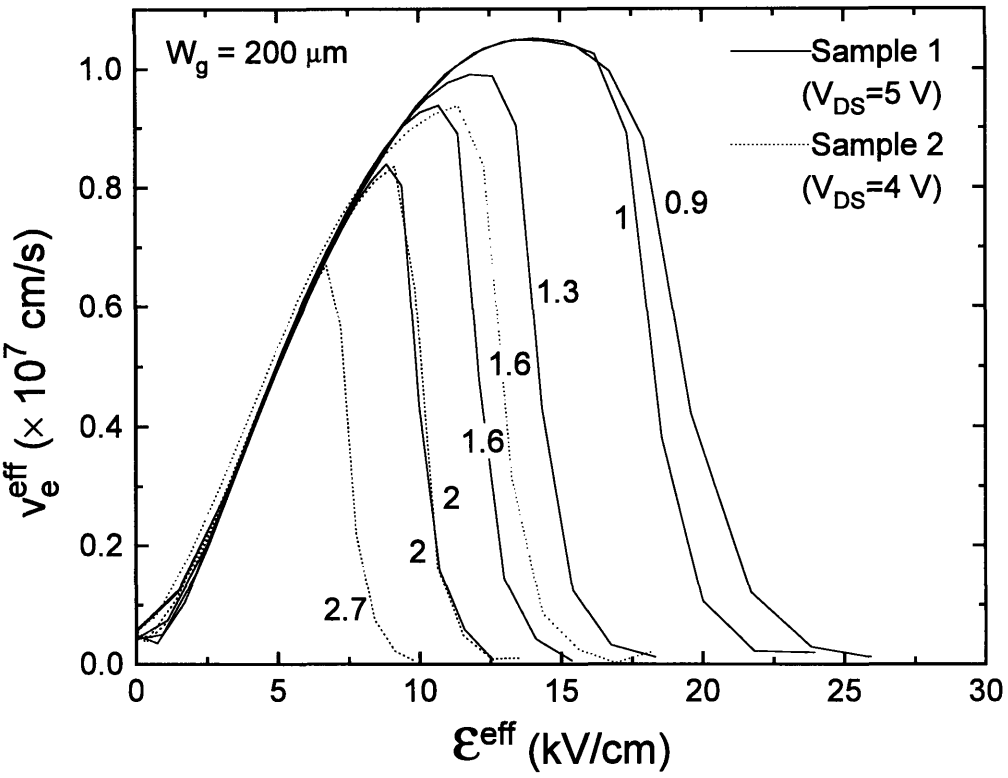

Figure 5.10: v_e^{eff} vs. V_{GS} for various values of L_g and at V_{DS}= 5 V for Sample 1 and V_{DS}= 4 V for Sample 2. Indicated gate lengths are values after correction according to procedure described in text.

and where V_{GS0} is the intrinsic gate-source voltage obtained by subtracting the parasitic source resistance potential drop from V_{GS}. In calculating $\mathcal{E}^{eff}$, we use the values for V_T measured independently in Chapter 4.

Since L_g appears in both Eq. 3.5 and Eq. 5.1, we are careful to ensure that we use accurate values for this quantity, which can differ from the L_g drawn on the mask due to variations in photolithography. To account for this variation, we employ an correction method based on two principles. First, since all devices are fabricated on the same heterostructure, we expect the slope of v_e^{eff} vs. $\mathcal{E}^{eff}$, proportional to channel mobility, to be the same for all devices in the mobility-limited regime. In particular, this should be the case for V_{GS} just above threshold. Second, our experience with photolithography shows that L_g variation generally effects only the smallest L_g values,

with gates longer than about 1.5 μm tending to reproduce quite accurately. Thus, we take our longest, L_g=2 μm device to be of the proper length and correct all shorter gates relative to this so as to achieve the same low-field v_e^{eff} vs. $\mathcal{E}^{eff}$ slope. We obtain the largest correction with the nominally L_g=0.8 μm device, which becomes 0.9 μm. In the remainder of this chapter, we indicate only these corrected values for L_g.

Fig. 5.10 shows the result, plotting v_e^{eff} vs. $\mathcal{E}^{eff}$ for devices with various L_g. For completeness, we supplement the plot with devices from a second sample made from a piece of the same heterostructure, but using an earlier-generation mask containing longer gate lengths. Remarkably, although our correction procedure simply aligns v_e^{eff} vs. $\mathcal{E}^{eff}$ at low-fields, we find that both the L_g=0.9 μm and 1.0 μm devices track each other precisely *even at high fields as the curves plateau.* Thus, by adjust L_g to fit the curves at one point, they proceed to match everywhere as well. We also note that devices of comparable adjusted gate length from the two separate samples display v_e^{eff} vs. $\mathcal{E}^{eff}$ profiles that fall virtually on top of one another as well, with the same peak v_e^{eff} values. These two behaviors combine to support the validity of the correction procedure.

Considering Fig. 5.10, we note that v_e^{eff} does indeed rise linearly with $\mathcal{E}^{eff}$ at low fields, indicating mobility-limited transport with μ_e= 1100 cm^2/V·s. In the shortest-gate devices, however, we clearly observe v_e^{eff} to flatten into a plateau at high fields, with a plateau value of 1.05×10^7 cm/s. The presence of this plateau indicates the onset of velocity saturation. As L_g increases, devices continue to follow the same curve, but achieve increasingly lower peak fields and therefore lower peak electron velocities before the onset of gate leakage.

To examine this scaling behavior further, we plot in Fig. 5.11 the maximum v_e^{eff} attained over V_{GS} at each L_g. We find that v_e^{eff} scales up as approximately $\frac{1}{L_g}$ with decreasing L_g for L_g>1.6 μm, as expected for devices that remain mobility-limited at all bias. For L_g below 1.6 μm, v_e^{eff} saturates to about 1.05×10^7 cm/s.

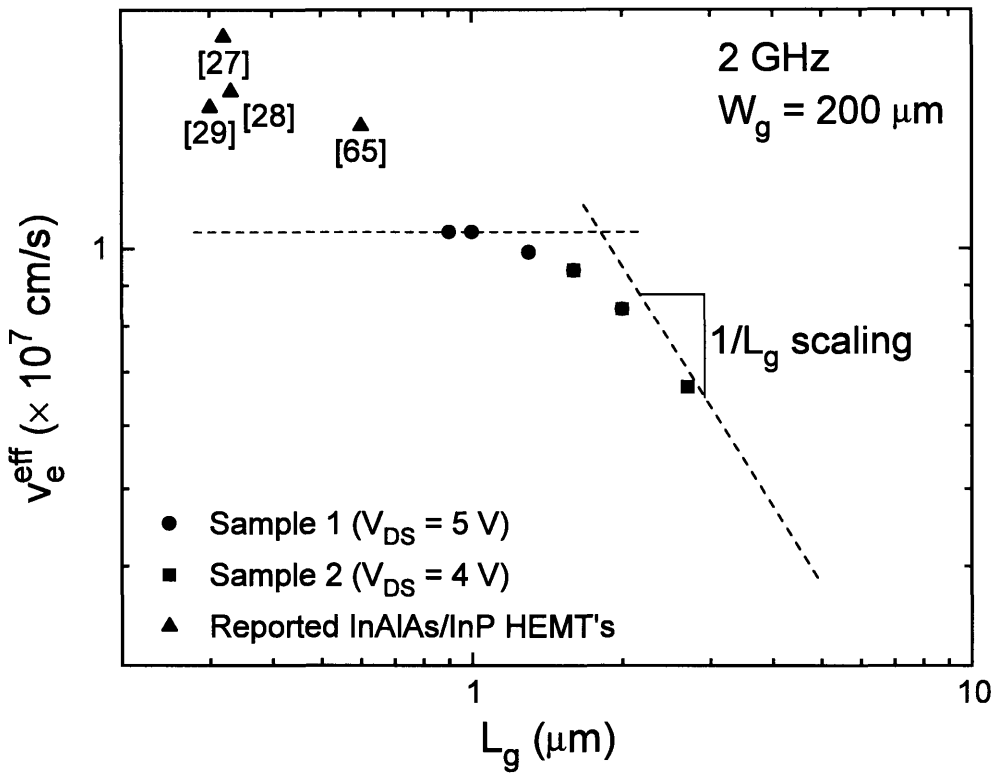

Figure 5.11: Maximum v_e^{eff} vs. L_g, at V_{DS}= 5 V for Sample 1 and V_{DS}= 4 V for Sample 2. Values for several InAlAs/InP HEMT's estimated from reported $f_T \cdot L_g$ values are included for comparison [27-29,65].

Although the electron velocity in undoped InP peaks at up to 2.6 × 10^7 cm/s [13], we do not observe any influence of this peak in our devices. Instead, our maximum extracted velocity agrees well with the saturation velocity expected for InP at high electric fields [13]. This behavior is in contrast with estimated electron velocities achieved in reported InAlAs/InP HEMT devices [29, 27, 28, 65], which reach significantly beyond v_{sat}. Since we cannot perform the careful v_e^{eff} extraction used in this study on these reported devices, we take the reported $f_T \cdot L_g$ product as a lower-bound v_e^{eff} estimate and superimpose several such values on the v_e^{eff} vs. L_g data for our doped-channel devices in Fig. 5.11. We note that undoped InP-channel devices achieve values for v_e^{eff} of at least 1.6 × 10^7 cm/s, much closer to the expected peak velocity for InP.

Our comparison implies that the inability to observe values of v_e^{eff} beyond v_{sat} in our devices is due to the presence of doping. The impact of doping on the observed value for v_e^{eff} in an HFET may best illustrated through the example of GaAs, which is the best characterized of the III-V semiconductors over a wide doping range. In addition to degrading the low-field mobility, doping is found to modify the steady-state velocity-field characteristics of GaAs in two additional ways [41]. First, the electric field at which electrons attain their peak velocity ($\mathcal{E}_{peak}$) increases. Since the existence of this peak arises from electrons attaining sufficient energy to transfer from the material central Γ valley into the low-mobility satellite L-valleys, this increase in $\mathcal{E}_{peak}$ is simply due to the more heavily scattered electrons having increased difficulty in extracting the necessary energy from the applied field. Further, since increased scattering helps to randomize momentum, raising the doping level lowers the average electron velocity corresponding to any given average electron energy. Thus, the peak electron velocity comes down as well.

At sufficiently high doping levels, the steady-state velocity-field curve peak can actually *disappear*, leading to a curve that simply rises monotonically from zero toward v_{sat} with increasing field. Since this behavior, which we observe in the InAlAs/n^+-InP MIDFET, seems to eliminate the possibility of observing values for v_e^{eff} in excess of v_{sat} in the MIDFET design, it might seem initially unrealistic to pursue such a device design for high-frequency applications. Yet, both n^+-InGaAs- and n^+-GaAs-channel devices of comparable or longer gate lengths to those presented here are, in fact, observed to display values for v_e^{eff} significantly beyond v_{sat}, and thus, presumably, beyond the peak velocity of the doping-degraded steady-state velocity-field curve [33, 34, 36, 37]. This picture strongly suggests that a proper correlation of channel material and doping level with observed v_e^{eff} hinges on understanding not only steady-state transport but also non-stationary or transient transport in the channel as well, which Monte Carlo simulations have shown to be important in III-V devices with heavily-doped channels at submicron gate lengths [33].

Although achieving non-stationary values for channel v_e^{eff} beyond v_{sat}, known as velocity-overshoot, is distinct from observing a peak velocity above v_{sat} in steady-state, the two phenomena are, in fact, related. Velocity overshoot can only occur in a single-valley material if the momentum and energy relaxation times for the material are significantly different, as is the case for Si. In the III-V materials in which polar-optical and ionized-impurity scattering mechanisms dominate, however, both relaxation times are similar and single-valley overshoot cannot occur [66]. Instead, overshoot in these materials is due solely to Γ-valley electrons temporarily achieving energies above the L-valley minima prior to relaxing into these valleys. Thus, a necessary condition for observing overshoot in a III-V device is achieving values for $\mathcal{E}^{eff}$ corresponding to a significant steady-state L-valley population, or, equivalently, to achieving $\mathcal{E}^{eff} > \mathcal{E}_{peak}$ [66].

Evaluating this minimum criterion for observing overshoot in devices of a given gate length but with differing doping levels or channel materials therefore reduces to estimating $\mathcal{E}_{peak}$ and comparing this value with the maximum $\mathcal{E}^{eff}$ achieved in the device channel. We can extract an estimation of $\mathcal{E}_{peak}$ which is simple yet represents all the salient first-order physics by considering the first and second moments of the Boltzmann transport equation. Assuming (1) steady-state transport, (2) a uniform material, and (3) a low-field mobility which is approximately constant for $\mathcal{E}$ up through $\mathcal{E}_{peak}$, we may combine these moments to yield the expression [41]

$$\mathcal{E} = \sqrt{\frac{\Delta w}{\langle \tau_w \rangle \, q \mu_e}} \tag{5.2}$$

which estimates the value of $\mathcal{E}$-field at which electrons reach a given excess average electron energy Δw above the equilibrium value. Here, q is the electronic charge, μ_e is the channel mobility, and $\langle \tau_w \rangle$ is the energy relaxation time, assumed approximately constant for a given material over the doping range of interest.

Significant electron transfer to the L-valleys begins when the average electron energy reaches the L-valley minimum, or, more explicitly, when Δw equals the Γ-L

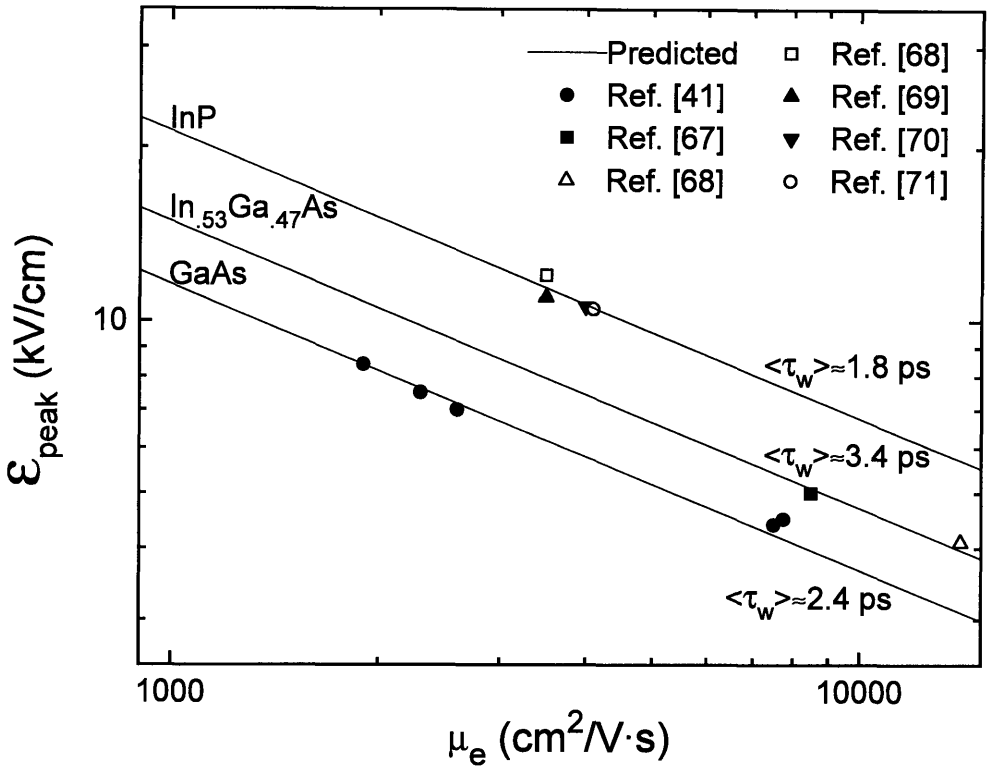

Figure 5.12: Predicted and reported values for $\mathcal{E}_{peak}$ vs. μ_e for InP, $In_{0.53}Ga_{0.47}As$, and GaAs [41,67-71].

valley energy separation $\Delta E_{\Gamma-L}$ (neglecting the much smaller equilibrium average electron energy). Under this condition, Eq. 5.2 becomes

$$\mathcal{E}_{peak} = \sqrt{\frac{\Delta E_{\Gamma-L}}{\langle \tau_w \rangle \, q\mu_e}} \tag{5.3}$$

The power of this simple expression lies in its ability to estimate $\mathcal{E}_{peak}$ for a given material as μ_e varies with doping once $\langle \tau_w \rangle$ is known.

Fig. 5.12 plots reported $\mathcal{E}_{peak}$ vs. μ_e values for InP, $In_{0.53}Ga_{0.47}As$ and GaAs from the literature, including both measured data and full-band Monte Carlo simulation results. In addition, we show the behavior predicted by Eq. 5.3, with $\langle \tau_w \rangle$ determined for each material by a least-squares fit to the literature values. Because of the abundance of available GaAs data [41], we can use this material to help gauge the

validity of our estimation method. We note that Eq. 5.3 yields quite a good match with data from the literature, validating our basic assumption that $\langle \tau_w \rangle$ is rather independent of doping. Although fewer data points exist for $In_{0.53}Ga_{0.47}As$ [67, 68] and InP [68, 69, 70, 71], we find a reasonable fit with these materials as well. Combined, these results suggest that Fig. 5.12 may be used to obtain a useful estimate of $\mathcal{E}_{peak}$ for the particular value of μ_e in our device channels. From the figure, we extract a value for $\mathcal{E}_{peak}$ of about 20 kV/cm corresponding to our channel μ_e of 1150 $cm^2/V{\cdot}s$. Recalling Fig. 5.10, we note that $\mathcal{E}^{eff}$ never exceeds this value for $\mathcal{E}_{peak}$ in our devices, explaining why we observe $v_e^{eff} \leq v_{sat}$, without any indication of non-stationary transport.

We may pursue this issue most clearly by first introducing two quantities: electron velocity ration γ_v and electric field ratio γ_E. The quantity γ_v is simply the maximum extracted value for v_e^{eff} for a given device divided by the steady-state velocity at the corresponding electric field. Thus, a value of 1.0 corresponds to transport predicted purely by the channel's steady-state transport properties, while a value in excess of 1.0 indicates non-stationary transport. Similarly, γ_E is defined as this same corresponding electric field divided by the estimated peak field $\mathcal{E}_{peak}$ for the channel material. Here, a value greater than 1.0 indicates $\mathcal{E}^{eff} > \mathcal{E}_{peak}$ in the device.

Having defined these quantities, we plot γ_v vs. γ_E in Fig. 5.13 for the InAlAs/n^+-InP MIDFET, at each of the gate lengths explored above. In addition, we supplement this plot with values from the literature for n^+-GaAs-channel devices [33, 72]. We choose to estimate $\mathcal{E}^{eff}$ for these reported devices using Eq. 5.1 just as with our own devices, limiting our choices to only those devices for which f_T vs. V_{GS} curves and values for the source resistances have been published. We note that none our devices achieve a value for γ_E greater than 1.0. As a result, we do not observe values for γ_v beyond 1.0. The GaAs data point with γ_E below 1.0 similarly shows no indication of velocity-overshoot. As γ_E exceeds 1.0 for the GaAs devices, however, velocity overshoot in excess of 25% beyond v_{sat} becomes apparent. These results, in addition

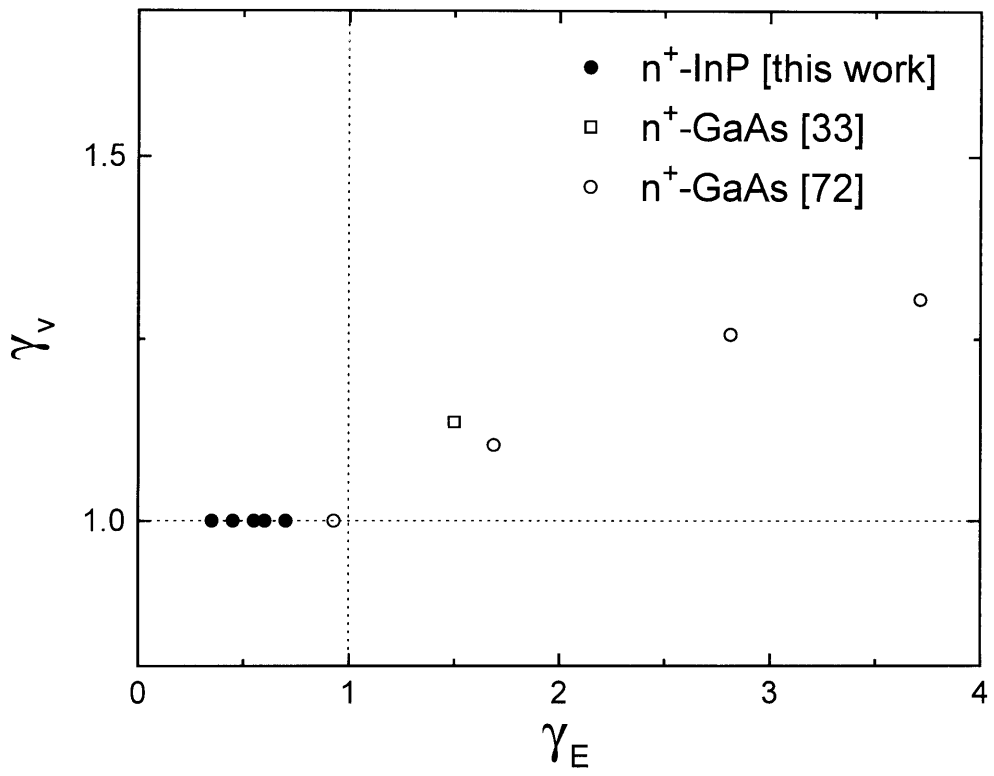

Figure 5.13: γ_v vs. γ_E (as defined in text) for the InAlAs/n$^+$-InP MIDFET studied in this work as well as for reported n$^+$-GaAs-channel devices [33,72].

to offering an explanation for the relatively low values of v_e^{eff} observed in our devices, also indicate the strong possibility for improving the frequency response of our device design in future processing runs by scaling down L_g to raise the achievable channel field beyond $\mathcal{E}_{peak}$.

Thus, we have employed our small-signal parameter extraction method to profile the figures of merit g_{m0} and C_{gs0} over both V_{GS} and L_g, combining the two to yield a profile of v_e^{eff} vs. $\mathcal{E}^{eff}$ in the n$^+$-InP channel. We find a clear transition from devices governed solely by mobility-limited transport at longer L_g to those which experience the onset of velocity-saturation at high V_{GS} and short L_g. Following the scaling of v_e^{eff} with L_g clearly shows that this saturation velocity reaches the InP high-field velocity of about 1×10^7 cm/s in devices with L_g<1.6 μm rather than achieving the material's higher peak velocity. We attribute this low v_e^{eff} to the degrading impact

of doping on both the steady-state peak velocity and on the conditions necessary for observing velocity overshoot.

5.3 Summary

We have carried out an experimental study exploring impact ionization, real-space transfer, and electron transport in the n^+-InP channel. In contrast with narrow-bandgap InGaAs-channel devices, the InAlAs/n^+-InP MIDFET displays no signature of impact ionization or real-space transfer in the gate or drain currents, leading to a gate current which remains below 17 μA/mm under typical bias conditions for 0.8 μm $\times$ 200 μm devices, 60 times lower than for typical reported InAlAs/InGaAs HEMT's. Furthermore, the lack of impact ionization also results in a drain-source breakdown voltage that *increases* as the device is turned on, displaying an off-state value of 10 V. Profiling electron velocity vs. electric field in the channel, we find that this velocity reaches the InP saturation velocity of about 1.05×10^7 cm/s in devices with L_g<1.6 μm rather than achieving the material's higher peak velocity. We attribute this low v_e^{eff} to the degrading impact of channel doping on both the steady-state peak velocity and on the conditions necessary for observing velocity overshoot in the device. Our combined findings indicate that electrons in the n^+-InP channel remain cold even at high V_{GS} and and V_{DS}, leading to small I_G, low g_d, and high BV_{DS}, traded-off against moderate frequency response.

Chapter 6:

Circuit Potential

In the preceding chapters, we have considered the performance of the discrete InAlAs/ n^+-InP MIDFET, finding the device to be well-suited to applications demanding small I_G, large BV_{DS}, low g_d, and high a_v. While many key applications can indeed be addressed through the use of one or two discrete devices, the versatility of an electronics family is vastly improved through the capability to realize circuits. Indeed, regardless of whether or not every such circuit in a given application demands devices capable of high-power performance, there are a number of cost, speed, and reliability advantages to being able to implement a complete telecommunications system on a single chip. An example is an optical receiver, designed to convert an optical pulse from a fiber into an electrical signal and then to synchronize to the incoming bitstream and recover the data. In this case, the HFET driving the photodiode should both enjoy low I_G for high sensitivity and as well as support the relatively large voltage required to bias the photodiode. The remainder of the system, which can include a transimpedence amplifier and phase-locked loop, for example, may not place equally high power demands upon the devices but may benefit nevertheless from being monolithic with the photodiode front end.

In developing our device technology, we have therefore placed considerable emphasis on features which enhance circuit capability, which we demonstrate in this chapter. In the first section, we briefly review the elements of our technology most relevant to circuit fabrication. In the following section, we demonstrate the circuit potential of our device technology using a monolithic, voltage tunable circuit as a vehicle.

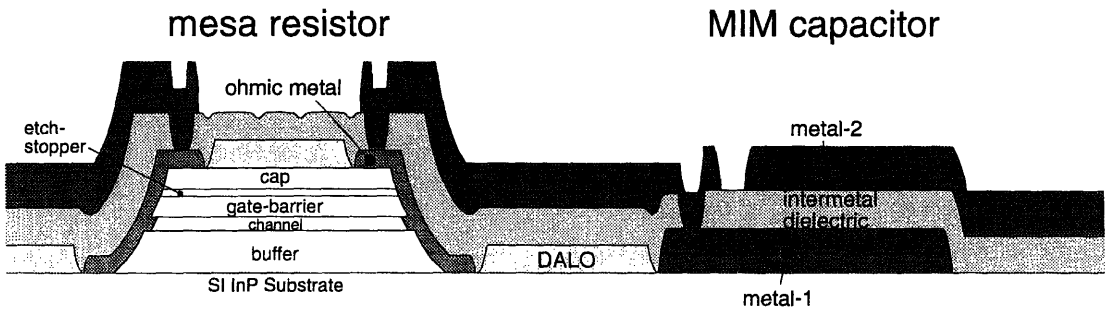

Figure 6.1: Schematic cross-section illustrating the implementation of mesa resistor and MIM capacitor circuit elements in our fabrication technology.

6.1 Circuit Technology Overview

A successful circuit technology addresses at least two distinct issues. First, a technology must be able to realize a sufficiently complete variety of active and passive circuit elements, including HFET's, diodes, resistors, capacitors, and interconnects. In our technology, the design and fabrication of the HFET itself have been previously summarized in detail in Chapter 2. Since the HFET gate already forms a diode with respect to the channel, a diode is easily implemented from an HFET simply by interconnecting the source and drain. Our implementation of the remaining passive devices is illustrated in Fig. 6.1, which shows a mesa resistor connected in series with a metal-insulator-metal (MIM) capacitor.

Mesa resistors are formed in a nearly identical fashion to HFET's, but without the cap-recess or gate metallization steps. Thus, the 50 $\Omega/\square$ cap layer serves as the path for current flow. To achieve a given designed resistance value, the mesa is etched in a long and narrow strip, which is either straight or serpentine depending on how large a resistance is required. The specific shape of the mesa strip can influence the overall shift in mesa dimension resulting from lateral etching during mesa formation. As a result, we include both types of resistors as test structures on our mask set in order to accurately characterize the process for subsequent modeling of circuit performance.

Although it is not necessary for demonstrating discrete devices, our two-level

metal technology permits us to implement both interconnect crossovers as well as MIM capacitors. Accurate knowledge of the areal capacitance between the two metal layers is key to correctly including interconnect crossover capacitance as a parasitic element in circuit model as well as to properly achieving target design values for capacitors used in our circuits. To measure this capacitance, our mask includes a 50 μm $\times$ 50 μm capacitor test structure, which indicates an areal capacitance of 7×10^{-9} F/cm^2. This value corresponds to a crossover capacitance of less than 0.3 fF for typical 2 μm wide interconnects, neglecting fringing capacitance. The capacitor test structure also permits us to test for parasitic conduction through the intermetal dielectric, revealing a greater than 12 GΩ resistance between typical crossovers.

A second issue that is key to a functional circuit technology is yield. For a circuit to work, every device in the circuit, including interconnects, must not only work but also match to within a given specification and exceed a minimum specified level of performance. While we have not addressed this issue exhaustively, we have contributed to improving yield in two ways. First, we have developed a dielectric-assisted lift-off (DALO) process for metal patterning, summarized in Chapter 2, which permits us to achieve fine optically-defined features for our device gates while maintaining excellent liftoff yield over the entire sample, free of breaks in the metal or short-circuits between long runs of closely-spaced interconnects. Second and most unique to our process, however, is our use of an InP etch-stopper beneath an InGaAs cap, characterized in Chapter 4. By ensuring a precise cap etch depth without the need for less accurate methods such as careful timing or iterative drain-current monitoring, our selective-etch technology achieves an extremely uniform threshold voltage over the sample and an even tighter matching between adjacent devices.

To demonstrate the circuit potential of our technology, we have included on our mask set a monolithic, voltage-tunable resonator circuit designed by Peter R. Nuytkens. While a more detailed account of the circuit operation may be found in [42], we present an overview below sufficient for illustrating the successful function of

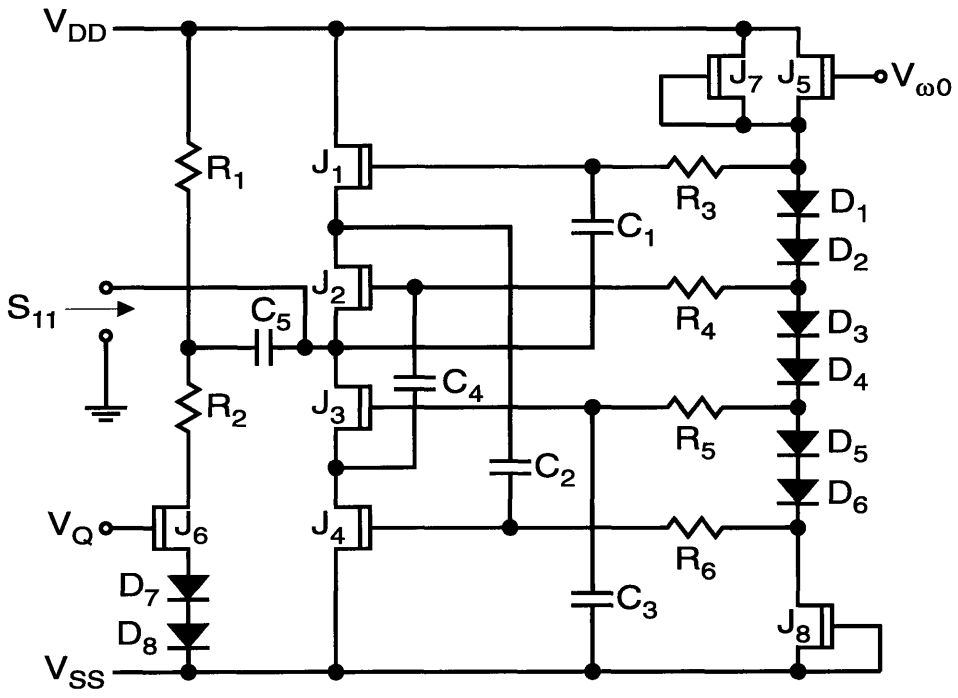

Figure 6.2: Circuit diagram for the monolithic, voltage-tunable resonator.

the circuit.

6.2 A Monolithic, Voltage-Tunable Resonator

As a test vehicle for our circuit capabilities, we have built and demonstrated a voltage-tunable resonator circuit, a key component for implementing highly selective bandpass filters for RF applications. While this particular circuit does not draw on all of the high-current and high-voltage advantages offered by our InAlAs/n^+-InP MIDFET technology, it is an example of the type of circuit that might be integrated with more demanding power circuits for cost and performance benefits to the overall system. As shown in the photograph in Fig. 2.7, the complete circuit is fabricated in a 600 μm $\times$ 600 μm area using 8 transistors, 8 diodes, 6 resistors, and 5 capacitors. While previously reported resonator designs have required a bulky external inductance element in order to achieve high Q values, this design aims to eliminate the need for a physical

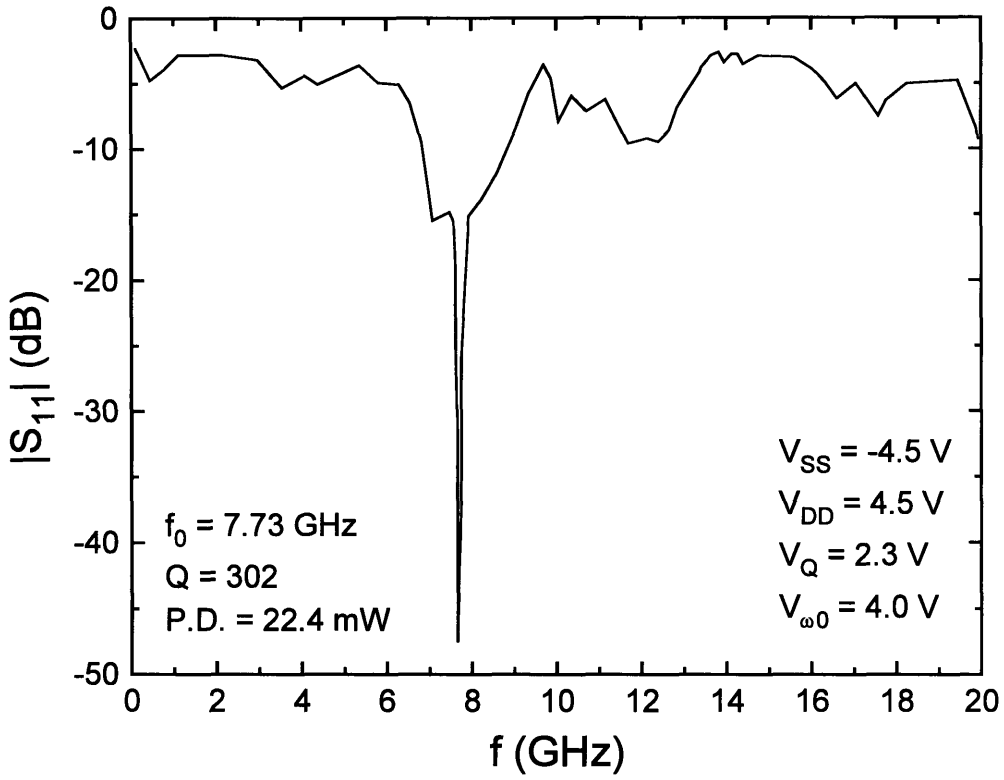

Figure 6.3: Broadband $|S_{11}|$ vs. f for the resonator.

inductance element so as to be fully monolithic for a large savings in complexity and size.

Fig. 6.2 shows the circuit diagram for the resonator. Central to the circuit are HFET's J_1-J_4, which are connected through coupling capacitors in a ring configuration. Through a first-order small-signal modeling in which each HFET is replaced by a simplified three-element equivalent circuit consisting of g_{m0}, C_{gs0}, and C_{gd0}, this ring reduces to a parallel combination of a capacitance, an inductance, and a *negative* resistance. HFET J_6 then acts as a positive parallel shunt resistance which may be tuned through voltage V_Q to completely cancel the negative resistance of the ring, yielding a circuit with a single, extremely hi-Q resonance. Alternately, V_Q may be adjusted to yield a net resistance of 50 Ω, for matching to a transmission line, or to yield higher values of Q as well for intentionally tuning the width of the resonance

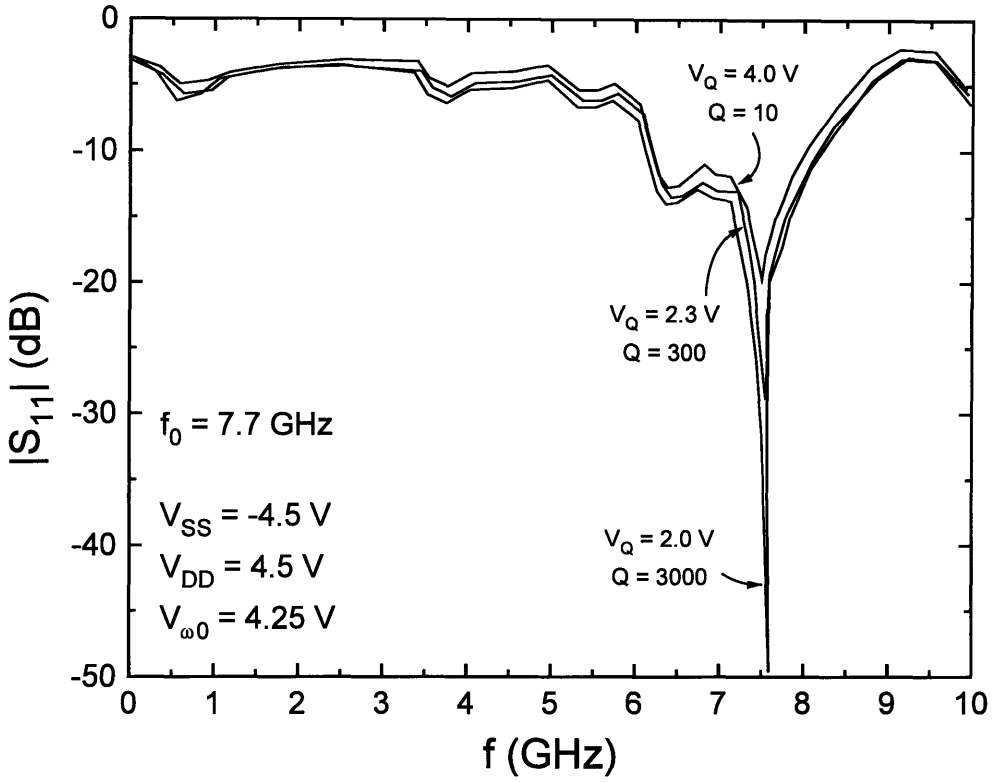

Figure 6.4: $|S_{11}|$ vs. f for the resonator for varying V_Q, showing tuning of Q-factor.

peak. The natural frequency f_0 of the resonator is also voltage tunable, by adjusting $V_{\omega 0}$ applied to HFET J_5. This shifts the gate bias on J_1-J_4, changing the value of g_{m0} for the devices and thus the effective inductance of the LCR equivalent circuit.

The successful operation of the resonator circuit is illustrated in Fig. 6.3, which shows $|S_{11}|$ vs. f over a broad frequency range for a resonator measured as a load to a 50 Ω transmission line. We observe a sharp resonance at 7.73 GHz, with a minimum of -47 dB, compared with an out-of-resonance passband ripple of less than 8 dB. We note that, despite the relative low f_T values for the InAlAs/n$^+$-InP HFET compared with InGaAs channel devices, we are able to achieve circuit function at quite large fractions of peak f_T and thus to operate in the 4-12 GHz range highly desirable for many key telecommunicatons applications. The circuit operates from supply voltages of $\pm$4.5 V, with a power dissipation of 22.4 mW.

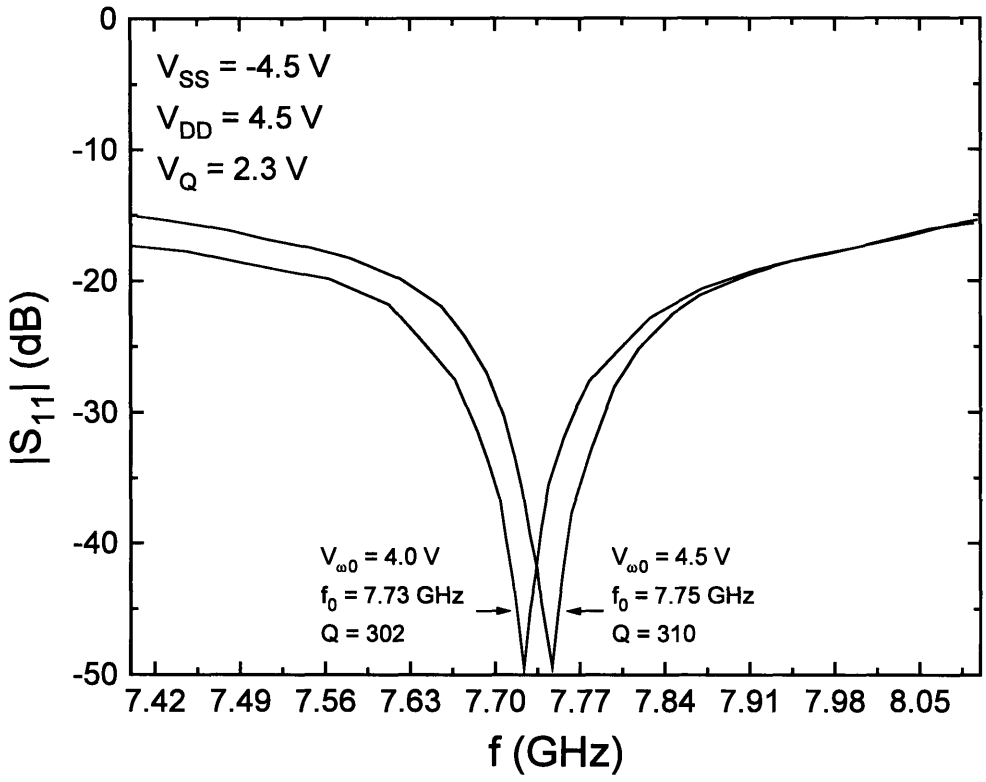

Figure 6.5: $|S_{11}|$ vs. f for the resonator for varying $V_{\omega 0}$, showing tuning of natural frequency f_0.

Two of the most noteworthy features of the resonator circuit are the ability to voltage-tune both Q and f_0. We illustrate the tuning of the Q-factor in Fig. 6.4, which shows $|S_{11}|$ vs. f for varying values of V_Q and with Q ranging from 10 to 3000. Indeed, careful tuning of V_Q yields values for Q in excess of 15000, measured through the width of the resonance 3 dB above the resonance minimum. This value for Q is more than 100 times greater than previously achieved in a monolithic design. We note that the center frequency of the resonance is independent of the tuning of Q-factor and remains fixed. Fig. 6.5 shows $|S_{11}|$ vs. f for varying $V_{\omega 0}$, illustrating the tuning of the resonance frequency over a 20 MHz window without affecting the value of the Q-factor.

6.3 Summary

In addition to yielding high-performance discrete devices, our InAlAs/n^+-InP technology employs DALO metal patterning and the use of a unique InP etch-stop layer to permit the yield and uniformity needed to manufacture circuits. As a vehicle for testing the circuit potential of our technology, we have fabricated and successfully demonstrated a monolithic, voltage-tunable resonator circuit. The circuit achieves a very high Q and operates at a natural frequency of 8 GHz.

Chapter 7:

Conclusions and Suggestions for Future Work

7.1 Conclusions

To address the growing demand for a high-power HFET family based on InP, we have developed and characterized an InAlAs/n^+-InP MIDFET technology employing InP both as the active channel layer and as an etch-stopper in a novel selectively-recessed gate scheme. This work has presented a comprehensive assessment of the technology, focusing on the benefits and drawbacks of exploiting InP epitaxial layers in each of these two roles and aimed at permitting a judicious comparison with other competing HFET designs on InP. The following list summarizes our key conclusions:

- Using an InP etch-stopper beneath an n^+-InGaAs cap in a selectively-recessed gate technology is highly effective at reducing r_s and r_d while simultaneously achieving a tight V_T distribution with a standard deviation of 60 mV across the wafer and only 13 mV between adjacent devices. These properties open the possibility for achieving excellent device performance in a manufacturable, circuit-capable process with relaxed photolithographic tolerances.

- In addition to reducing R_{sh} in the extrinsic source and drain by screening of surface Fermi-level pinning, the cap layer also operates through a previously unreported mechanism by which the low-resistance cap conducts *in parallel* with the channel for sufficiently high current (about 20% of $I_{D,MAX}$ for the nominal L_{sg} of 2 μm). This behavior leads to a rapid reduction in r_s and r_d with increasing I_D, even with gate-source or gate-drain separations of up to 10 μm, leading to high figures of merit such as a peak g_m of 200 mS/mm

and a maximum drain current of 430 mA/mm despite relatively high parasitic resistance at low current.

- The wide-bandgap InP channel is immune to impact ionization, in contrast with the behavior of narrow-bandgap InGaAs channels. A key consequence is an excellent off-state BV_{DS} of 10 V which actually *increases* as the device is turned on.

- The high effective-mass InP-channel also eliminates detectable evidence of real-space transfer in either I_D or I_G, indicating that electrons in this channel material remain cold even at high V_{GS} and V_{DS}. The combined absence of both impact ionization and real-space transfer contribute further to a low I_G which is 60 times less than for reported InAlAs/InGaAs HEMT's as well as to both small g_d and high a_v.

- Profiling v_e^{eff} vs. $\mathcal{E}^{eff}$ reveals that channel electrons achieve only the InP high-field saturation velocity of about 1.05×10^7 cm/s rather than the material's much higher peak velocity. We attribute this behavior to the degrading impact of channel doping on both the steady-state peak velocity and on the conditions necessary for observing velocity overshoot in the device. Balancing this finding against the advantages listed above, we conclude that the InAlAs/n^+-InP MIDFET is well-suited to high-power, low-input-noise applications demanding low I_G, large BV_{DS}, small g_d, and high a_v, and for which a moderate frequency response is an acceptable tradeoff.

- The chemical etch selectivity of the InP channel can be exploited as well in a recessed-ohmic contact scheme capable of reducing contact resistance to the channel by a factor of 2.

- A monolithic, voltage tunable resonator circuit implemented in our InAlAs/n^+-InP MIDFET technology achieves high values for Q tunable to over 15,000, and operates at a natural frequency of 8 GHz tunable over a 20 MHz range, demonstrating the circuit suitability of our device.

7.2 Suggestions for Future Work

While we find that the use of an n^+-InP channel layer offers a number of advantages in HFET design for power applications, this work has shown these benefits come with the tradeoff of a lower velocity compared with the full potential of the material. Our first suggestions address improving v_e^{eff} in future InP-channel devices while preserving most of the remaining benefits.

Our work reveals that heavily-doped channel devices must rely on non-stationary transport effects to achieve values for v_e^{eff} beyond v_{sat}, which in turn requires values for the channel electric field in excess of $\mathcal{E}_{peak}$. High-mobility channel materials such as $In_{0.53}Ga_{0.47}As$ retain sufficient mobility at high doping levels to keep $\mathcal{E}_{peak}$ below achievable fields at our current gate lengths, leading to observable overshoot. Because the mobility of InP is quite low even for undoped material, however, the addition of doping simply drives mobility down too severely, making it difficult to exceed the overshoot criterion.

This issue suggests that one way to proceed is to focus on a HEMT approach, but with doping introduced not only in the gate-barrier layer but in the layer beneath the channel as well, introducing additional channel charge. The use of such a so-called inverted modulation-doping scheme may permit some doping to be removed from the gate-barrier, potentially improving the gate swing and breakdown voltage. A thin delta-doped layer appropriately located in the channel itself has been shown not to harm mobility substantially in InGaAs-channel devices, and might be incorporated into an InP-channel device as well for further increases in channel charge.

A recent composite channel approach, in which a thin layer of undoped InGaAs is introduced just above the n^+-InP channel, has demonstrated excellent preliminary results [73, 74]. The observed high f_T, I_D, and BV_{DS} are possibly due to channel electrons accelerating to a high velocity in the high-mobility InGaAs before launching into the wide-bandgap InP near the drain, where the electric field is greatest. These

early findings suggest introducing such a layer into our design and studying the physics of the device more comprehensively.

Exploring the InAlAs/n^+-InP MIDFET in the deep submicron regime, using a more advanced electron-beam or X-ray lithography technique, is a third approach which might increase the maximum effective electric field in the n^+-InP channel sufficiently to reveal the onset of significant non-stationary effects.

Our work has also revealed tremendous advantages of a cap structure in which the cap carries current in parallel with the channel, and has explored the mechanism by which electrons transfer from cap to channel over the gate barrier. A future device design promises to benefit greatly by further optimizing the cap design given this insight. One way to do this is to introduce either a thin, n^+-InAlAs layer or a graded n^+-InAlAs to n^+-InGaAs layer between the existing n^+-InGaAs cap and the gate-barrier. Such a layer would serve to eliminate the conduction band discontinuity between cap and barrier, allowing electrons to transfer to the channel much more easily. At the same time, adding this layer would effectively uncouple the barrier to cap current transfer from that of the gate diode, adding a degree of freedom to optimizing the gate-barrier without the danger of simultaneously degrading the cap action.

Our device fabrication experience has also shown the difficulty of using wet etch technology to etch through both As- and P-containing layers. Our preliminary work suggests tremendous benefits in reliability and yield moving to dry-etching technology or ion-milling both for the mesa step and for most of the recessed-ohmic-contact procedure. This technology should be pursued further.

Experimentally, exploring the temperature dependendence of both breakdown as well as the cap mechanism would offer additional insight into the underlying physics. A detailed charge control study of the drain region, which could be performed using the small-signal equivalent model already presented here, would also provide inter-

esting insight into the effects of various cap-recess widths, surface treatments, and passivation techniques on both g_d and BV_{DS}.

Finally, a crucial issue in evaluating a device technology for many key applications is noise performance, suggesting that a comprehensive study of noise in InP-channel HFET's compared with competing designs might prove very fruitful.

Appendix A:

Process Flow

InAlAs/n^+-InP MIDFET Process Sequence

1. Equipment/Materials Preparation and Misc. Notes:

   (a) Perform cleaning procedures on all tools and "glassware".

   Minimum "glassware":

   - 7 glass 600 ml beakers - 2 acid, 2 solvent, 2 deionized H_2O, and 1 photoresist developer.
   - 1 poly 600 ml beaker for BOE.
   - 1 glass or Nalgene (poly preferred) 100 ml graduated cyclinder.
   - enough petri dishes and covers to hold samples.

   (b) Obtain metallurgical grade GaAs to use as cap during ohmic contact annealing.

   (c) Make sure the following chemicals are in stock:

   - solvents: TCA, acetone, and methanol.
   - acids/bases: H_2SO_4, H_2O_2, HCl, H_3PO_4, BOE, Semico clean.
   - photolithography: Shipley 1400-27 resist, Shipley Microposit primer (HMDS), Shipley MF-319 developer, chlorobenzene (available in Chemistry stock room).
   - dielectric coating: Allied-Signal Accuglass 311 spin-on glass.

   (d) For best results, prepare the following "etchant #1" concentrate in advance:

   H_2SO_4:H_2O_2:H_2O 1:10:10

Note: allow concentrate to cool down before using. Solution lasts for about 3 weeks.

(e) Always read at least one procedure ahead of your present place in the process and schedule the required equipment in advance to avoid unnecessary delays.

2. Mesa Isolation:

(a) Ultra clean:

i. TCA boil, 2 min., twice.

ii. acetone, ultrasound, 2 min., twice.

iii. methanol, 1 min.

iv. deionized H_2O rinse, 1 min.

v. Semico clean, ultrasound, 1 min.

vi. deionized H_2O rinse, 1 min., and N_2 blow dry. Store carefully if not processing immediately.

(b) Cap Removal (for reference samples only):

i. prepare H_2SO_4:H_2O_2:H_2O 1:10:220 etchant.

ii. etch in ultrasound, min. of 14 sec. per 500 Å cap thickness.

iii. deionized H_2O rinse, 1 min., N_2 blow dry. Store carefully if not processing immediately.

(c) Photolithography:

i. If stored: deionized H_2O rinse, 1 min., and N_2 blow dry.

ii. coat primer (Shipley Microposit primer (HMDS)), let sit 10 sec., spin dry at 5500 rpm, 30 sec.

iii. spin resist, Shipley 1400-27, 5500 rpm, 30 sec. (nominal thickness: 1.1 μm).

iv. heat in soft bake oven, 95° C, 30 min.

v. cool down 5 min.

vi. spray mask with acetone/methanol and N_2 blow dry to clean.

vii. test expose dummy samples, mask MESA (Estimate: 35 sec.).

viii. develop in MF-319, 1 min.

ix. deionized H_2O rinse, 1 min., twice, and N_2 blow dry.

x. microscope inspection.

xi. expose, develop, and inspect device samples.

xii. spray mask with acetone/methanol and N_2 blow dry.

(d) Mesa Etch:

i. descum in Day asher, 100 W, 45 sec., to etch ~250Å of resist.

ii. deionized H_2O rinse, 1 min.

iii. Semico clean, ultrasound, 1 min.

iv. deionized H_2O rinse, 1 min.

v. microscope check: look for resist adhesion problems.

vi. prepare etchants (mix very well, using glass rod):

- etchant #1 - 1 part concentrate to 10 parts H_2O, *or, if concentrate not available*, H_2SO_4:H_2O_2:H_2O 1:10:220.

  Note: if preparing fresh etchant, make sure etchant cools down to room temperature prior to use.

- etchant #2 - H_3PO_4:HCl 19:1

vii. Calibrate etch rates on dummy samples:

- InGaAs - etchant #1, nom. etch rate: 2500Å/min.
- InAlAs - etchant #1, nom. etch rate: 3500Å/min.
- InP - etchant #2, nom. etch rate: 1000Å/min.

viii. mesa etch sequence (perform first on expendable piece if possible): etch in ultrasound at 25° C in heterostructure-dependent sequence, according to the following guidelines (15% overetch included):

- InGaAs (cap) - etchant #1, 14 sec. per 500Å.
- InP (etch-stopper & channel) - etchant #2, 35 sec. per 1000Å.

- InAlAs (gate-barrier & buffer) - etchant #1, 10 sec. per 500Å.

ix. Rinse in deionized H_2O in ultrasound for 1 min., twice, after *each* etchant and N_2 blow-dry at end of sequence.

x. microscope inspection.

xi. If first run was on a dummy sample, repeat for real samples once inspection is satisfactory.

(e) Mesa-Sidewall Channel Isolation:

i. etch in etchant #2 with constant sample movement, nominally 1 min.

ii. deionized H_2O rinse, 1 min., N_2 blow dry, twice.

(f) Remove PR:

i. acetone, ultrasound, 2 min.

ii. rinse briefly in methanol before acetone dries.

iii. deionized H_2O rinse, 1 min., N_2 blow dry.

iv. microscope inspection.

v. measure mesa heights on each sample.

3. Dielectric Deposition for DALO:

i. clean Si dummies in BOE or dilute HF until hydrophobic, followed by deionized H_2O rinse, 1 min., and N_2 blow dry.

ii. clean real samples in Semico clean, ultrasound, 1 min., followed by deionized H_2O rinse, 1 min., and N_2 blow dry.

iii. load PECVD chamber with Si dummies only.

iv. deposit 3000 Å of SiO_2 using prepared recipe on floppy disk.

v. inspect dummies under microscope for particles or pinholes.

vi. cleave dummy samples into small pieces (approx. 1 cm^2).

vii. paint 2-4 black wax stripes on each dummy piece and allow to dry 2 min.

viii. etch SiO_2 on Si dummy in BOE with ultrasound, followed by 1 min. deionized H_2O rinse and N_2 blow dry. Determine clearing time, T_{oxide}, and then etch at 2-3 evenly spaced intervals in between.

ix. rinse dummy pieces in TCA/acetone/methanol to remove black wax stripes and N_2 blow dry.

x. Dektak SiO_2 stripes to determine exact film thickness t_{oxide} and etch rate r_{oxide}. Measure refractive index on ellipsometer. Adjust recipe if parameters are incorrect.

xi. load PECVD chamber with real samples and one Si dummy.

xii. deposit SiO_2 on real samples as before.

4. Ohmic Contact Formation:

(a) Photolithography:

i. deionized H_2O rinse, 1 min., and N_2 blow dry.

ii. coat primer (Shipley Microposit primer (HMDS)), let sit 10 sec., spin dry at 5500 rpm, 30 sec.

iii. spin resist, Shipley 1400-27, 5500 rpm, 30 sec. (nominal thickness: 1.1 μm).

iv. while sample still on spin chuck, remove edge-bead with acetone and swab.

v. heat in soft bake oven, 95° C, 30 min.

vi. cool down 5 min.

vii. test expose dummy samples, mask SRCDRN (Estimate: 35 sec.).

viii. develop in MF-319, 1 min.

ix. deionized H_2O rinse, 1 min., twice, and N_2 blow dry.

x. microscope inspection.

xi. expose, develop, and inspect device samples.

xii. spray mask with acetone/methanol and N_2 blow dry

(b) DALO Etch:

i. descum in Day asher, 100 W, 45 sec., to etch ~250Å of resist.

ii. etch SiO_2 in BOE with ultrasound for $1.1*T_{nitride}$ sec.
As a double check, etch silicon dummy simultaneously and verify that surface becomes hydrophobic.

iii. deionized H_2O rinse, 2 min., twice, and N_2 blow dry.

iv. microscope inspection.

(c) Optional - Ohmic Contact Recess (for selected test samples):

i. prepare etchants (mix very well, using glass rod):

- etchant #1 - 1 part concentrate to 10 parts H_2O, *or*, *if concentrate not available*, H_2SO_4:H_2O_2:H_2O 1:10:220.
Note: if preparing fresh etchant, make sure etchant cools down to room temperature prior to use.
- etchant #2 - H_3PO_4:HCl 19:1

ii. Calibrate etch rates on dummy samples:

- InGaAs - etchant #1, nom. etch rate: 2500Å/min.
- InAlAs - etchant #1, nom. etch rate: 3500Å/min.
- InP - etchant #2, nom. etch rate: 1000Å/min.

iii. recess-etch down to InP channel (perform first on expendable piece if possible):
etch in ultrasound at 25° C in heterostructure-dependent sequence, according to the following guidelines (15% overetch included):

- InGaAs (cap) - etchant #1, 14 sec. per 500Å.
- InP (etch-stopper) - etchant #2, 35 sec. per 1000Å.
- InAlAs (gate-barrier) - etchant #1, 10 sec. per 500Å.

iv. Rinse in deionized H_2O in ultrasound for 1 min., twice, after *each* etchant and N_2 blow-dry at end of sequence.

v. microscope inspection.

vi. If first run was on a dummy sample, repeat for real samples once inspection is satisfactory.

vii. etch back photoresist on Si dummy in Day asher, 100 W, 2 min.

viii. measure vertical resist loss using Dektak: Target value = 2000Å.

ix. repeat etch if target not met, and note total etch time, T_{resist}.

x. etch real samples for time T_{resist}.

xi. microscope inspection.

xii. etch in BOE with ultrasound for $1.1*T_{nitride}$ sec. to recreate nitride undercut.

xiii. deionized H_2O rinse, 2 min., twice, and N_2 blow dry.

xiv. microscope inspection.

(d) Metallization:

i. evaporate contacts: 50Å Ni / 500Å Ge / 1000Å Au / 300Å Ni (include glass cover slip monitor).

(e) Lift-off:

i. place samples on glass slides covered by absorbent clean-room wipes.

ii. dribble acetone on edge of sample until surface is covered.

iii. keep surface wet with acetone until 1 min. after metal film begins to crack.

iv. squirt acetone vigorous at surface until metal film has completely cleared.

v. with sample still wet, transfer to beaker of acetone, ultrasound, 1 min., twice.

vi. methanol rinse before acetone dries.

vii. deionized H_2O rinse, 1 min., and N_2 blow dry .

viii. microscope inspection. Make sure glass slide is clean.

(f) Alloying:

i. TCA boil real samples, calibration samples, and GaAs cap, 2 min.

ii. Load RTA: place sample face-up on thermocouple wafer, and cover with GaAs cap oriented face-down.

iii. Run RTA alloying program. Nominal sequence: ramp to 250° C, hold 10 sec., ramp to 375° C, hold 10 sec., cool.

Adjust program using calibration samples if necessary before proceeding with real samples.

Note: Since heterostructures possess a conducting cap, calibration samples cannot be measured until gate cap recess takes place (before gate metal is deposited). May perform calibration on uncapped reference sample instead.

5. Gate Formation:

(a) Photolithography:

i. rinse deionized H_2O H_2O, 1 min., and N_2 blow dry.

ii. coat primer (Shipley Microposit primer (HMDS)), let sit 10 sec., spin dry at 5500 rpm, 30 sec.

iii. spin resist, Shipley 1400-27, 5500 rpm, 30 sec. (nominal thickness: 1.1 μm).

iv. while sample still on spin chuck, remove edge-bead with acetone and swab.

v. heat in soft bake oven, 95° C, 30 min.

vi. cool down 5 min.

vii. test expose dummy samples, mask GMET (Estimate: 35 sec., vacuum contact).

viii. develop in MF-319, 1 min.

ix. deionized H_2O rinse, 1 min., twice, and N_2 blow dry.

x. microscope inspection.

xi. expose, develop, and inspect device samples.

xii. spray mask with acetone/methanol and N_2 blow dry.

(b) DALO Etch:

i. descum in Day asher, 100 W, 45 sec., to etch ~250Å of resist.

ii. etch SiO_2 in BOE with ultrasound for $1.1*T_{nitride}$ sec.
As a double check, etch silicon dummy simultaneously and verify that surface becomes hydrophobic.

iii. deionized H_2O rinse, 2 min., twice, and N_2 blow dry.

iv. microscope inspection.

(c) Cap Recess (except on uncapped reference samples):

i. prepare H_2SO_4:H_2O_2:H_2O 1:10:220 etchant.

ii. etch in ultrasound, 14 sec. per 500 Å cap thickness, plus an additional 24 sec. for proper lateral etch distance.

iii. deionized H_2O rinse, 1 min., N_2 blow dry.
Note: RTA calibration samples may be annealed now.

(d) Metallization:

i. evaporate gate: 250Å Ti / 250Å Pt / 2500Å Au.

(e) Lift-off:

i. place samples on glass slides covered by absorbent clean-room wipes.

ii. dribble acetone on edge of sample until surface is covered.

iii. keep surface wet with acetone until 1 min. after metal film begins to crack.

iv. squirt acetone vigorous at surface until metal film has completely cleared.

v. with sample still wet, transfer to beaker of acetone, ultrasound, 1 min., twice.

vi. methanol rinse before acetone dries.

vii. deionized H_2O rinse, 1 min., and N_2 blow dry .

viii. microscope inspection. Make sure glass slide is clean.

6. Interlevel Dielectric Deposition and Via Etching:

(a) Double Spin-On Glass (SOG) Coating:

i. TCA boil samples, 2 min., followed by acetone/methanol rinse.

ii. deionized H_2O rinse, 1 min., and N_2 blow dry .

iii. coat primer (Shipley Microposit primer (HMDS)), let sit 10 sec., spin dry at 5500 rpm, 30 sec.

iv. spin Accuglass 311, 4000 rpm, 20 sec. (nominal thickness: 2670Å)
Notes:

- do not blow-clean wafer while on spin chuck (kicks up SOG powder).
- coat *entire* sample as quickly as possible (use 2/3 full medicine dropper for 2 sec. wafer and engage spinner at full RPM immediately upon dispensing).
- rinse spin bowl with methanol periodically to flush SOG dust.
- clean bown with methanol when finished.

v. cure sequence: 100° C, 10 min. (softbake oven), 200° C, 10 min. (prebake oven).

vi. repeat spin process up through cure step.

vii. second cure sequence: 100° C, 10 min. (softbake oven), 200° C, 30 min. (prebake oven).

(b) Via Photolithography:

i. deionized H_2O rinse, 1 min., and N_2 blow dry if stored.

ii. coat primer (Shipley Microposit primer (HMDS)), let sit 10 sec., spin dry at 5500 rpm, 30 sec.

iii. spin resist, Shipley 1400-27, 5500 rpm, 30 sec. (nominal thickness: 1.1 μm).

iv. heat in soft bake oven, 95° C, 30 min.

v. cool down 5 min.

vi. spray mask with acetone/methanol and N_2 blow dry to clean.

vii. test expose dummy samples, mask VIA1 (Estimate: 35 sec.).

viii. develop in MF-319, 1 min.

ix. deionized H_2O rinse, 1 min., twice, and N_2 blow dry.

x. microscope inspection.

xi. expose, develop, and inspect device samples.

xii. spray mask with acetone/methanol and N_2 blow dry.

(c) Via etching:

i. descum in Day asher, 100 W, 45 sec., to etch ~250Å of resist.

ii. etch dielectric in 1:9 BOE:DI with ultrasound for 3 min.

iii. deionized H_2O rinse, 2 min., twice, and N_2 blow dry.

iv. check under microscope for clearing and repeat etch in 10% increments until clear.

7. Interconnect or Pad:

(a) Photolithography:

i. deionized H_2O rinse, 1 min., and N_2 blow dry.

ii. coat primer (Shipley Microposit primer (HMDS)), let sit 10 sec., spin dry at 5500 rpm, 30 sec.

iii. spin resist, Shipley 1400-27, 5500 rpm, 30 sec. (nominal thickness: 1.1 μm).

iv. while sample still on spin chuck, remove edge-bead with acetone and swab.

v. heat in soft bake oven, 95° C, 30 min.

vi. cool down 5 min.

vii. test expose dummy samples, mask MET1 (Estimate: 35 sec.).

viii. develop in MF-319, 1 min.

ix. deionized H_2O rinse, 1 min., twice, and N_2 blow dry.

x. microscope inspection.

xi. chlorobenzene check: expose additional dummy samples.

xii. soak in chlorobenzene, nominally 90 sec.

Note: record "latency" time before image begins to develop out and adjust soak time to attain 20 sec.

xiii. bake 95° C, 5 min.

xiv. develop in MF-319, 2 min.; double rinse H_2O, 1 min.; N_2 blow dry.

xv. microscope inspection.

xvi. expose and develop real samples.

xvii. spray mask with acetone/methanol and N_2 blow dry.

(b) Clean and metal evaporation:

i. descum in Day asher, 100 W, 45 sec., to etch ~250Å of resist.

ii. rinse H_2O, 1 min., and N_2 blow dry.

iii. evaporate pads: 250Å Ti / 250Å Pt / 3500Å Au.

(c) Lift-off:

i. place samples on glass slides covered by absorbent clean-room wipes.

ii. dribble acetone on edge of sample until surface is covered.

iii. keep surface wet with acetone until 1 min. after metal film begins to crack.

iv. squirt acetone vigorous at surface until metal film has completely cleared.

v. with sample still wet, transfer to beaker of acetone, ultrasound, 1 min., twice.

vi. methanol rinse before acetone dries.

vii. deionized H_2O rinse, 1 min., and N_2 blow dry .

viii. microscope inspection. Make sure glass slide is clean.

Appendix B:

BANDSOLV User Guide

B.1 Introduction

BANDSOLV is a semiconductor device simulator in one-dimension employing full Fermi-Dirac statistics and optimized for simulating a variety of heterostructures commonly used in HFET technology. File-oriented and written in C, it may be ported easily to a variety of platforms, including MS-DOS and UNIX. Some of BANDSOLV's key features include:

- Ability to simulate arbitrary heterostructure designs, drawing materials from a user-definable file.
- Choice of either zero-electric-field or Fermi-level pinning as the substrate interface boundary condition.
- Specification of alloy layers by interpolating two previously defined materials.
- Two distinct output files, one optimized for displaying band diagrams and carrier/charge volume-densities vs. depth, and the other for exploring sheet-densities vs. bias for each layer.
- Automatic bias sweeping.
- Nonuniform gridpoint spacing.

BANDSOLV does not include band non-parabolicity or permit full quantum-mechanical (Schrödinger's equation) solutions. Nevertheless, we find room temperature results to agree remarkably well (with a few percent) with the output of more advanced programs for the most common simulations of threshold voltage and

charge control used in HFET design and analysis. A more limiting restriction is that BANDSOLV does not calculate current flow, and thus cannot properly calculate quasi-Fermi-level bending for a structure under bias. Instead, the program assumes that the quasi-Fermi-level splits at the Schottky-metal/heterostructure interface and is flat everywhere in the heterostructure. This is appropriate only for structures in which the surfacemost layer nominally contains no charge and acts as the primary bottleneck to current flow, an assumption tailored to HFET physics. Equilibrium (zero bias) simulations are not restricted in this way, of course.

This manual describes the operating procedures for using BANDSOLV, including defining a master material file, designing heterostructure input files for simulation, running the program, and interpreting the output.

B.2 Program Setup

BANDSOLV consists of the actual executable file, **bs.exe** in MS-DOS or **bs** in UNIX, together with the materials definition file **material.dat** and any number of user heterostructure input files. Before running the program, the executable should be placed into either the current working directory or a directory in the user's path. The **material.dat** file and user input files must sit in the current working directory.

B.3 Materials Definition

For flexibility, BANDSOLV keeps all material parameters in a separate file, **material.dat**, which may be edited or extended at any time.

A sample file is listed below:

```
# Materials data file for PC-Bandsolv;
# InP family (lattice matched);
inp:    me=0.075, mh=0.60, eg=1.34, es=12.4, dec=0.0;
inalas: me=0.086, mh=0.59, eg=1.46, es=12.4, dec=0.3;
ingaas: me=0.041, mh=0.48, eg=0.75, es=13.9, dec= -0.2;
```

Much of the syntax of this sample file applies not only to **material.dat** but to the user input files as well. All files are organized into "logical lines," terminated by a semicolon. Carriage returns and other white space are ignored. This behavior allows a single logical line to span more than one physical line if it improves readability. Any line beginning with a "#" symbol is treated as a comment and is ignored up through the terminating semicolon. Comments may be inserted at will to document a file and make it easier to edit in the future. All other lines contain information for BANDSOLV and consist of a list of keywords or variables which are separated by the user's choice of either a colon or comma (both may be mixed on the same line to enhance readability).

In **material.dat**, each material is defined by one line. We use the first non-comment line in the sample listing (beginning with "inp") to illustrate this procedure. The first keyword on each line defines the material name, "inp' in this case. The next four variables, "me," "mh," "eg," and "es" set values for the electron density-of-states effective mass, the hole density-of-states effective mass, the bandgap (in eV), and the dielectric constant for the material. These terms may appear in any order following the material name, and each will be set to zero automatically if no specific value is given. Finally, the variable "dec," which may also appear anywhere on the line, sets the relative position of the conduction band with respect to all other materials in the same *family.* A family is defined as a group of materials that may be used together in the same heterostructure. In our example, "inp," "inalas," and "ingaas" form such a

family. Another family might be "gaas" and "algaas."

There are two additional points to note. First, although a user's input file, described below, may specify a layer as an alloy between two defined materials, the material parameters for the alloy are calculated using linear interpolation of the five material parameters defined above. Therefore, any alloy composition which must be modeled more precisely should be given its own name, such as "in60ga40as" and defined explicitly in **material.dat**. Second, a material should appear only once in the **material.dat** file. Lines with the same material name appearing later in the file will supercede and overwrite the material parameter values defined earlier.

B.4 Heterostructure Definition

A heterostructures to be simulated is defined in its own input file, which may be given any filename lacking an extension. For our example, we will consider the input file **midfet**, representing a simplified InP-channel MIDFET:

```
# InP-channel MIDFET;
# general parameters;
temp=300,
schottky=0.7,substrate=0.7,
startbias= -1,endbias= -0.5,stepbias=0.1,
depth=350;

# layer structure (surface to substrate);
inalas: thick=250,grid=125,nd=1e14,no-e,no-h;
inp:    thick=100,grid=50,nd=5e18;
inalas: thick=1000,grid=250,nd=1e14;
```

User input files share some basic syntax with **material.dat**: logical lines end with a semicolon, comment lines begin with "#," and keywords or variables within a logical line are delimited by either a colon or comma.

Unlike **material.dat**, however, the user input file is split into two sections. The first section is a single logical line that defines general simulation parameters and variables related to biasing and boundary conditions. The second section, consisting of all subsequent lines, defines the heterostructure layers.

Stepping through our sample file, the general parameters are defined as follows. Variable "temp" sets the simulation temperature in K. Although low temperatures may be set, BANDSOLV is increasingly less accurate as temperature drops due to the lack of a Schrödinger solver. Also, the simulation temperature impacts only the energy distribution of carriers. BANDSOLV does not include a provision to account for the effects of temperature on material parameters such as bandgap.

Heterostructures are assumed capped by a metal "gate." The variable "schottky" defines the Schottky-barrier between this metal and the top heterostructure layer, in eV. Since all III-V surfaces are pinned, a free surface may also be simulated by setting "schottky" to the Fermi-level pinning position, referenced to the top layer conduction band. Such a structure may be simulated only in equilibrium.

Similarly, if present, the variable "substrate" sets a Fermi-level pinning position for the bottommost (nearest to substrate) heterostructure layer. This is key to properly modeling layers grown on semi-insulating substrates. If "substrate" is absent, a zero-electric-field boundary condition is assumed.

The following three variables allow BANDSOLV to automatically simulate a series of biases applied to the gate with respect to the substrate. The initial and final biases are set using "startbias" and "endbias," while "stepbias" defines the increment. The variable "stepbias" must be set to a non-zero value or the simulation may enter an

endless loop.

Although BANDSOLV always solves for the entire heterostructure internally, a user may care to view information for only a limited region near the surface. The depth of this region is defined with "depth," In our structure, for example, only the top 350 Å are interesting, and sit on top of a thick 1000 Å buffer.

Following the general parameters line, the input file contains the actual heterostructure layer definitions, from surface to substrate. The first keyword is the material name, "inalas," for example. To specify an interpolated alloy, a second material name may follow, followed by the variable "interp" set to the alloy fraction between the first and second materials. After the material specification, the variable "thick" sets the layer thickness, while "grid" sets the number of intervals into which to divide the simulation grid for that layer. Donor and acceptor concentration may be defined with either "nd" and/or "na," respectively.

Finally, each layer definition line may contain two additional keywords, "no-e" and "no-h." Including these keywords turns off the calculation of electron concentration or hole concentration in the layer. Since BANDSOLV cannot calculate quasi-Fermi-level bending in a device under bias, simulated charge in the top layer may be non-physical in certain cases. For example, consider a MISFET-type structure using an undoped, wide-bandgap gate-barrier layer at the surface and simulated at large negative bias. Starting from the substrate, the Fermi-level in such a structure remains flat throughout most of the structure and then bends almost exclusively within the gate-barrier layer to meet the Fermi-level in the gate. Thus, in an actual MISFET, the Fermi-level in the gate-barrier layer never approaches the conduction or valence bands and no significant charge exists in the layer. In a BANDSOLV simulation, however, the Fermi-level is held flat throughout the structure, instantly splitting at the gate/heterostructure interface. This may erroneously lead to the Fermi-level intersecting the gate-barrier layer valence band, causing a false build-up of holes. Adding "no-h" prevents this by manually turning off hole calculation.

B.5 Heterostructure Simulation

Once **material.dat** and a user input file has been defined, BANDSOLV is ready to run. Typing:

```
bs inputfile
```

starts BANDSOLV, where **inputfile** is the user input file (**midfet** in our previous example). The program notifies the user as it finishes simulating each bias point, and ultimately generates two output files, described in the next section.

B.6 Output File Formats

Upon completion, BANDSOLV reports all results in two separate output files. These files share the same base name as the input file, but end with ".dat" and ".ns" extensions: **midfet.dat** and **midfet.ns** in our example. The first file, **midfet.dat**, contains energy band and carrier/charge volume-density information as a function of depth into heterostructure, for each bias point. The second file, **midfet.ns**, contains integrated carrier/charge sheet-densities for each heterostructure layer as a function of bias point, useful for charge-control analysis.

The first several lines of **midfet.dat** appear as follows:

```
 DIST       EC       EV              N              P            RHO
 -125  1.00000  1.00000 0.000000e+000 0.000000e+000 0.000000e+000
    0  1.00000  1.00000 0.000000e+000 0.000000e+000 0.000000e+000
    0  1.70000  0.24000 0.000000e+000 0.000000e+000 1.000000e+014
    2  1.68975  0.22975 0.000000e+000 0.000000e+000 1.000000e+014
    4  1.67950  0.21950 0.000000e+000 0.000000e+000 1.000000e+014
```

The first line consists of column headings. The six columns contain, in turn: depth below the surface in Å, conduction band and valence band energies in eV with respect to the Fermi-level, electron and hole concentrations in cm^{-3}, and net concentration [$N_D - N_A + p - n$], also in cm^{-3}. Subsequent lines contain the simulation output, down to a depth specified by "depth" in the user input file. Note the special line at a depth of -125 Å. This line does not actually represent the heterostructure and is included so that graphical plotting packages correctly draw a small horizontal line representing the gate-metal Fermi-level when the data is graphed. In a file representing more than one bias point, blocks of data for the other biases follow in turn, with each block separated by a blank line.

We reproduce the first six columns of **midfet.ns** below:

VGS	N1	P1	RHO1	EF1	EB1
-1.000	0.000e+000	0.000e+000	2.480e+008	-5.124e+005	-5.123e+005
-0.900	0.000e+000	0.000e+000	2.480e+008	-4.819e+005	-4.819e+005
-0.800	0.000e+000	0.000e+000	2.480e+008	-4.508e+005	-4.508e+005
-0.700	0.000e+000	0.000e+000	2.480e+008	-4.192e+005	-4.191e+005
-0.600	0.000e+000	0.000e+000	2.480e+008	-3.870e+005	-3.870e+005
-0.500	0.000e+000	0.000e+000	2.480e+008	-3.543e+005	-3.543e+005

Again, the first line contains column headings. The first column lists all simulated bias values in Volts. The next three columns contain the values from the similarly labeled **midfet.dat** columns, but presented as sheet-densities integrated over layer 1 (the top layer). The next two columns indicate the electric field in V/cm at the top and bottom interfaces of the layer. Five columns per each additional layer follow.

With the information just presented, the user is ready to simulate any heterostructure. Good luck and thanks for trying BANDSOLV.

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