Electrochemical and Photoelectrochemical Micromachining of Silicon in HF Electrolytes

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Abstract

Over the last two decades there has been great interest and increasing activity in micromachining of small, three-dimensional, microelectromechanical silicon structures. Applications include pressure sensors, accelerometers, gyroscopes, micro-valve, channel and pump systems for drug delivery, and actuated micro-mirror arrays to name a just few. Device fabrication and performance has been, in part, limited by the ability to micromachine the desired device geometries, and more specifically, to achieve micron or sub-micron sized, stress free, and high aspect ratio structures with precisely controlled dimensions. This thesis investigates the micromachining capabilities afforded by electrochemical and photoelectrochemical etching of silicon in HF electrolytes.

The etching characteristics of bulk p-Si and n-Si were systematically studied as a function of key variables including bias, HF concentration, illumination intensity and wavelength, and doping density. The silicon etch rate was found to increase nearly linearly with the flux of holes to the silicon-electrolyte interface. By appropriate choice of applied bias and HF concentration, the room temperature p-Si etch rate was controlled over three orders of magnitude up to 100μm/min. The n-Si etch rate, which is negligible in the absence of illumination due to the lack of holes, was found to increase linearly with above band-gap illumination intensity.

The feasibility of etching vertical high aspect ratio structures into n-Si by illuminating through a patterned metal mask was demonstrated by micromachining columns and walls with 5:1 aspect ratios and 1μm line widths. Further optimization, however, was hampered by mask layer etching or delamination from the substrate.

Etching of silicon samples, containing both p- and n-regions, was studied to develop p-n junction etch-stops which would permit allowing selective etching of either the p- or n-regions. The p-n junctions internal to these samples were found to drastically influence the anodic hole currents to the silicon-electrolyte interface. Reverse biased p-n junctions block anodic currents preventing p-Si etching, and forward biased p-n junctions

inject holes into n-Si resulting in dissolution in the absence of illumination. Photo-biases and photo-currents generated at illuminated p-n junctions were found both to drive p-Si anodic with respect to n-Si and to supply anodic currents to p-Si regions, promoting their dissolution. The effects of p-n junctions on etching currents were mathematically modeled for the case of abrupt p-n junctions, and verified by measuring the current-voltage characteristics of epi-layer samples. Virtually all of the potential applied between the sample and electrolyte was found to fall across a reverse biased junction which, depending on the sample doping profile and bias, could be either the Schottky-like barrier at the silicon-electrolyte interface or a p-n junction.

These various phenomena were employed to develop 3 novel and distinctly different p-n junction etch-stops techniques. The p-on-n etch-stop entails selective etching of an n-Si substrate to form free standing p-Si structures, by illuminating the sample and applying a p-n junction reverse bias. The p-well etch-stop entails selective etching of p-Si regions in an n-substrate, by illuminating the sample to drive p-regions anodic with respect to n-Si. The p-n-p etch-stop entails selective etching of a p-Si substrate to form free standing p-on-n multi-layer structures. Each etch-stop was successfully demonstrated by micromachining cantilever beams with high quality etch-stop surfaces. Ultra-high etch-stop selectivities up to $\approx 10^8$ were achieved, and sub-micron 0.6 and 0.8μm thin cantilever beams were fabricated. Furthermore, these etch-stops are compatible with moderate and light doping densities, which allowed fabrication of stress-free cantilever beams exhibiting virtually no curl over their 650μm length.

We conclude that electrochemical and photoelectrochemical micromachining of silicon in HF electrolytes is a highly versatile technique with many desirable capabilities, and should prove to be a useful and enabling micromachining technology.

Thesis Advisor: Harry L. Tuller
Title: Professor of Ceramics and Electronic Materials

Chapter 1

Introduction

1.1 Motivation

1.1.1 Micromachining and Microelectromechanical Systems

Over the last fifteen to twenty years there has been much interest and increasing activity in micromachining of materials to form small three dimensional structures [1]. Applications for such structures range from simple porous membranes or diffraction gratings to highly intricate sensors that are integrated with optics and electronics. In fact it is the ability to integrate the small three dimensional mechanical structures with input/output electronics to create microelectromechanical systems (MEMS) that has made micromachining such an enabling technology. Sensors for measuring pressure, acceleration, strain, acoustic signals, chemical concentrations, etc. have been made smaller, more sensitive, more rugged and reliable, and significantly cheaper by micromachining than with macro-fabrication technologies. As a consequence, these sensors are now finding many new applications, in automobiles, health care, manufacturing control systems, aviation, and consumer electronics. Other applications for MEMS devices include manipulation of matter at microscopic scales, using micro-valves, pumps, and channel systems for drug delivery, biological manipulation at the cellular level, and micro-actuators for micro-robotics and fine positioning.

As the MEMS community works to develop devices with advanced capabilities and higher performance-price ratios, there is a driving force to achieve ever more complex structure geometries, to more precisely control device dimensions, and to develop more cost-effective processing techniques. Since the limiting factor is typically the capabilities of present micromachining techniques, there is a continuing need to develop more versatile, powerful, and enabling micromachining technologies.

1.1.2 *Bulk Silicon Micromachining*

Silicon continues to be the most used and technologically important micromachining material for several reasons. First, silicon has very desirable mechanical and thermal materials properties [2]. Second, silicon's success in the microelectronics industry has served to develop many technologies which are directly applicable to MEMS fabrication. Photolithography, diffusion, implantation, oxidation and thin film deposition processes have been developed to within submicron tolerances, and the related processing equipment as well as high purity single crystal silicon with optimized mechanical properties are all readily available at reasonable costs. Third, these technologies allow batch processing making MEMS devices more affordable. And finally, silicon permits the fabrication of both micromechanical structures and electronics on one substrate to achieve truly integrated microelectromechanical systems, allowing of new possibilities for 'smart' devices.

Of the various silicon micromachining technologies [1], the most mature is bulk silicon micromachining which involves the controlled dissolution of sections of a Si substrate to reveal the desired device. Since conventional VLSI etching techniques are inadequate for either forming underetched structures or precisely controlling vertical dimensions, etch-stops must be used to define the structure geometry. The most commercially successful and widely used etch-stops are the heavily boron doped (p^+) etch-stop [3 ,4] and the n-Si electrochemical passivation etch-stop [5 -8], both of which use EDP (ethylenediamine pyrocatechol) or KOH type anisotropic etchants [9].

These techniques, however, do have limitations. The very high (near-solubility limit) boron doping levels of the p^+ etch-stop yield highly stressed structures which tend to buckle or curl [10 ,11]. Furthermore the degenerate nature of the etch-stop precludes formation of electronics in the structure itself. The anisotropic KOH or EDP etchants dissolve (111) crystal planes very slowly which may limit the device geometry or overall size. Reasonable etch rates require elevated temperatures, which must be equally maintained over an entire wafer to ensure etch uniformity. The etch-stop selectivities, defined as the ratio of the silicon to etch-stop etch rates, limit the ability to precisely control device dimensions. With KOH, selectivities are only $\leq 10^2$ and 10^2 to 10^3 for the p^+ and anodic passivation etch-stops respectively [4,9], depending on the etchant concentration, dopant concentration, and temperature. And finally, these etch-stops depend on chemical etching of silicon which provides very little micromachining versatility beyond the specific etch-stop process itself.

1.1.3 *Electrochemical Micromachining*

Given the limitations of existing micromachining technologies, it was decided to investigate electrochemical and photoelectrochemical micromachining of silicon as an alternative bulk silicon micromachining technique. Our interest in this topic first arose

from numerous interesting observations in the literature on electrochemical and photoelectrochemical etching of III-V semiconductors. For example, p-type versus n-type dopant selectivity was demonstrated by electrochemically etching GaAs [12] and GaP [13]. Illumination selectivity was demonstrated by photoelectrochemical etching using 1) optical masks to form localized recesses [14], 2) pattern projection to form topographical micro-lenses [15], 3) focused laser beams to form vias or tunnels [15,16], and 4) interference patterns from two noncolinear intersecting laser beams to form diffraction gratings [17]. In addition, bandgap selective etching was demonstrated by preferentially photochemically etching the lower bandgap GaAs of a GaAs/AlGaAs heterostructure [18].

The enhanced capabilities and versatility afforded by electrochemical and photoelectrochemical etching of semiconductors arises from the anodic nature of the dissolution process. Dissolution requires the presence of both a sufficient anodic potential and holes at the semiconductor-electrolyte interface. Numerous etching and sample parameters affect these two requirements, including the applied bias(es), doping type and density, electrolyte composition, the presence of buried p-n junctions, and photo-generated biases and currents.

The aim of this work is to better understand how these parameters should be controlled to achieve selective etching, etch-stops, and more generally, three dimensional structures in silicon.

1.2 Methodology and Scope

While electrochemical and photoelectrochemical dissolution of silicon has been studied by numerous groups (see chapter 2), very little has been done to apply this etching technique to bulk silicon micromachining which is the focus of the present work. In chapter two we review the current understanding of electrochemical etching of bulk silicon in fluoride electrolytes, followed by a review of previous electrochemical micromachining studies for both silicon and other semiconductors.

In chapter three we first present the theoretical aspects behind electrochemical etching of p- and n-type semiconductors and silicon in particular. We then develop a model for calculating anodic currents and potential distributions across the silicon-electrolyte interface of samples containing both p- and n-regions. This model is applied to calculate the current-voltage characteristics of a variety of sample doping profiles, including p-layers on n-substrates, n-layers on p-substrates, n-p multilayers on p-substrates, and illuminated p-layers on n-substrates.

In chapter four the experimental methods and sample preparation are described. In chapter five we first present our systematic studies of bulk p- and n-Si etching characteristics as a function of the key variables including, electrolyte composition,

illumination intensity, and doping density, with the goal of either confirming or extending the present understanding in the literature. These characteristics are used to identify means for achieving p-n junction etch-stops and for etching of high aspect ratio structures. p-n junction etch-stops are studied and demonstrated using epi-layer samples and by machining of micro-cantilever beams. The feasibility of etching vertical high aspect ratio structures using illumination through patterned metal masks on n-Si samples is demonstrated.

In chapter six these experimental results are compared to the models developed in chapter three, and an understanding of the various etch-stop mechanisms is developed. Parameter 'windows' are established within which p-n junction etch-stops and etching of high aspect ratio structures can be achieved, and guidelines are set for optimizing the various processes. The abilities and limitations of the p-n junction etch-stops are explained and contrasted to alternative techniques. And finally, in chapter eight we propose some aspects if silicon electrochemical micromachining in HF warranting further study.

Chapter 2

Literature Review

The literature pertinent to electrochemical and photoelectrochemical micromachining of silicon is reviewed in this chapter. First, the silicon electrochemical etching characteristics and dissolution mechanisms are summarized, followed by a review of electrochemical and photoelectrochemical selective etching techniques reported for both silicon and other semiconductors. A discussion of the more general theoretical aspects of semiconductor electrochemistry and the semiconductor-electrolyte-interface [19 -28] is deferred to chapter 3.

2.1 Anodic Dissolution of Bulk Silicon in Fluoride Electrolytes

Electrochemical etching of semiconductors proceeds when they are anodically biased. In general, holes are driven to the semiconductor-electrolyte-interface which destabilizes surface atoms and allows for their dissolution by attack of electrolyte species. When silicon is anodically biased in aqueous electrolytes, a relatively inert passivating oxide layer forms on the surface which dramatically impedes further dissolution. Reasonable electrochemical silicon etch rates therefore require fluoride electrolytes which effectively attack Si-O bonds and dissolve the oxide. Anodic dissolution of bulk n- or p-silicon in fluoride electrolytes has been well reported in the literature [29 -75]. The observed etching characteristics and effects of important parameters are now summarized, followed by a detailed review of the dissolution mechanisms in section 2.1.2.

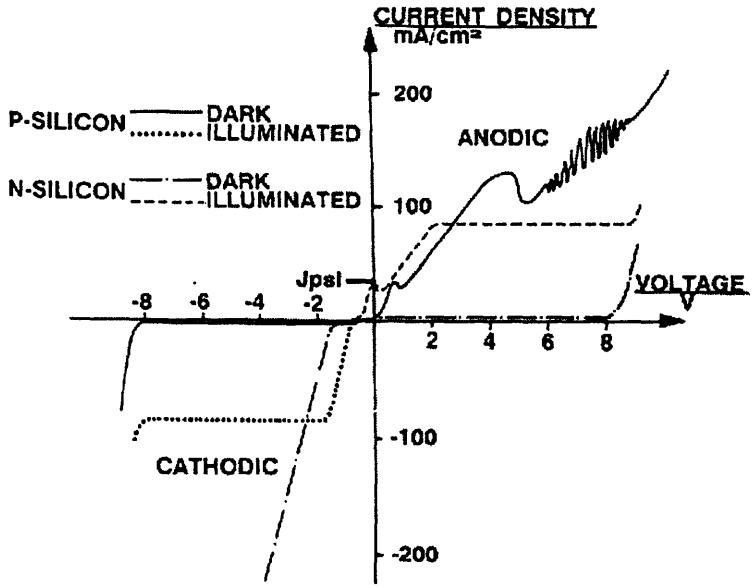

Figure 2.1. Typical current-voltage characteristics (versus Platinum reference electrode) of n- and p-type silicon in 2.5 weight percent HF electrolyte, using 100 mV/s sweep rate. Reproduced from reference [49].

2.1.1 Etching Characteristics and the Effects of Important Parameters

2.1.1.1 Effect of Bias, Illumination, and Doping type

The details of the electrochemical current-voltage (I-V) characteristics of p- and n-type silicon reported in the literature tend to vary from paper to paper, due to the wide range of parameters that influence the cell current. The general aspects of the I-V characteristics tend to be similar, however, and a typical representation is shown in figure 2.1 for silicon in 2.5 weight percent HF electrolyte [49].

The I-V characteristics are measured by passing current between a silicon electrode and platinum counter electrode which are both immersed in the electrolyte. The anodic current density and thereby the silicon dissolution rate are related to the potential drop across the silicon-electrolyte interface. Unfortunately the potential applied between the silicon and platinum electrodes also drops across the electrolyte and the platinum-electrolyte-interface. The silicon-electrolyte-interface potential drop is therefore measured relative to an 'ideally' polarizable reference electrode near the silicon surface, which allows one to accurately monitor changes in the fraction of the cell voltage that falls across the silicon-electrolyte interface. It is this fraction that is referred to by the terms "cell potential (or bias)" and "potential (or bias) applied to the silicon electrode" in this thesis. The reader is warned that a variety of reference electrodes have been used to

study electrochemical dissolution of silicon in the literature, including the standard calomel electrode (SCE), the normal hydrogen electrode (NHE), a platinum wire dipped in the HF electrolyte, and in a few cases no reference electrode at all. All measurements in this thesis were made with respect to the standard calomel electrode (SCE).

p-type silicon

As seen in figure 2.1, no cell current flows at p-Si electrodes when biased at potentials less than ≈0V (Pt) (with respect to a platinum wire dipped in the electrolyte). At sufficiently high cathodic potentials electrical breakdown occurs in the silicon space-charge layer at the interface producing high cathodic currents. Cathodic currents are also obtained when p-Si is irradiated with above band-gap illumination and biased less than -1V (Pt). Cathodic currents at silicon electrodes do not result in dissolution, however, but rather H_2 evolution and hydrogenation of the silicon surface [76]. At biases anodic of ≈0 V (Pt) the holes in p-Si are driven to the silicon-electrolyte interface causing dissolution. Two current peaks are observed in the anodic I-V characteristics, and will be referred to as J_{crit} (labeled as J_{PSL} in figure 2.1) and J_{max}.

At current densities below J_{crit} silicon only partially dissolves forming a porous layer which grows into the surface [30,32,33,37,38,39,42,43,45,62,77]. Zhang *et. al.* [51] report that a uniform porous layer forms only at low current densities for which exponential current-voltage characteristics are observed. The fraction of the surface covered by porous silicon then progressivly decreases as the current density approaches J_{crit}. Some researchers have reported that the porous layer is a highly hydrogenated amorphous silicon film [30,33,50]. Others studies based on x-ray and electron diffraction report the porous silicon layer to be monocrystalline with the same orientation as the substrate [36,37,42,43]. Unagami [39] reports that both amorphous and monocrystalline layers coexist, with a very thin amorphous silicon layer forming first followed by growth of monocrystalline porous silicon underneath.

The porous silicon microstructure is found to depend on many dissolution parameters. Pore radii can range from approximately 10 to 120Å [43,45], and the overall porosity can vary from 26 to 81% [43,45,77]. In general, porosity and pore size tend to increase with 1) decreasing doping density, 2) increasing current density, and 3) decreasing HF concentration [38,45,77]. The porous silicon formation rate can vary from ≈0.5 to 10 μm/min and increases with increasing current density and HF concentration [38,39,77].

When the current density is raised above J_{crit} the porous silicon layer spontaneously separates from the surface and floats away [30,74]. At this point the rate of Si-O bond formation begins to outpace the rate of Si-O bond dissolution by the HF electrolyte and an oxide layer is formed. The chemical dissolution of this oxide by the electrolyte becomes the etch rate-limiting process [46,55,]. Etching at current densities above J_{crit} is generally reported to yield electropolished surfaces, however this is not entirely correct. There is in fact poor agreement in the literature as to which etching potentials or current densities produce electropolishing. Electropolishing conditions are

reported to occur: 1) at both current plateaus, followed by localized corrosion at higher potentials [64,69], 2) at potentials positive of the first current peak [51,55], 3) at current densities above which spontaneous current oscillations occur [61], and 4) at current densities somewhat above J_{crit} [31,67,70], below which rough but progressively smoother etch surfaces are observed with increasing current density.

Smooth electropolished surfaces form because the applied potential falls mostly across the oxide layer which drives the migration of ionic species. The electric field strength becomes concentrated at raised sections of the silicon/oxide interface and is lower at depressed sections. Raised sections therefore oxidize faster, depressed sections oxidize slower, and the silicon/oxide interface is smoothed over time.

Anodic oxide thicknesses are approximately 20Å to 100Å [68,69] and increase with applied potential [41,46,69]. Anodic oxide etch rates are about two orders of magnitude faster than thermal oxide etch rates, depending on the oxide composition and anodizing potential [46,68]. The oxide near the silicon/oxide interface is 10 to 20% sub-stoichiometric in oxygen and varies with applied potential and electrolyte fluoride concentration [41,46,78]. Chazalviel [69] and Gerischer *et. al.* [46] report the existence of two distinct oxide compositions. A porous and fragile wet oxide/hydroxide is found near the oxide-electrolyte interface. It contains primarily negativly charged especies and has a low refractive index approaching that of water ($\eta \approx 1.33$) [68]. A dry sub-stoichiometric oxide is found between the silicon substrate and wet oxide. This oxide has a refractive index approaching that of thermal oxides ($\eta \approx 1.46$) [68], and contains mostly positivly charged species.

n-type silicon

n-type silicon, in contrast to p-Si, has an abundance of electrons instead of holes. The cathodic hydrogen formation reaction therefore proceeds readily without illumination, but virtually no anodic dissolution is found to occur. Heavily doped n^+-Si has different anodic etching characteristics than n-Si and actually does dissolve in the dark. This is further explained in section 2.1.1.2. When n-Si is illuminated and anodically biased, photo-generated minority holes are swept to the interface and dissolution occurs. The anodic current increases with anodic bias until a plateau is reached where the current is limited by the hole photo-generation rate [55,67,70]. The anodic current then remains constant with further increasing bias until electrical breakdown is achieved. Under sufficiently high illumination intensities, the anodic I-V characteristics are nearly identical to those for p-Si except for a $\approx$0.5 V shift in the cathodic direction [55,61]. This shift results from the difference in Fermi energies between the n and p silicon, causing a $\approx$0.5 V difference in the flat band potentials of the n- and p-silicon-electrolyte interfaces. Consequently, a more anodic potential is necessary to drive holes to the silicon-electrolyte interface in p-Si than in n-Si.

Porous silicon also forms on n-Si when etched at current densities below J_{crit}. The current density can be controlled in 3 ways: 1) n-Si can be illuminated at a high intensity using a sufficiently low anodic bias to keep $J < J_{crit}$, 2) n-Si can be illuminated with a low

intensity giving an illumination-intensity-limited current density below J_{crit}, and 3) n-Si can be etched without illumination using a potentiostat in galvanostatic mode with the current setting below J_{crit}, resulting in limited breakdown. Porous films formed by method 3, however, tend to be non-uniform due to varying breakdown field strengths over the silicon surface, and swirl patterns [42] or defect delineation [34,44] are typically observed.

Two distinctly different porous layer morphologies form on n-Si: a nanoporous layer like that which forms on p-Si having pore diameters of ≈50Å, and a macroporous silicon layer having pore diameters of ≈0.1 to 15μm [36,37,56,66,73,74]. (Macropore formation is also observed in n-GaAs [79], and is probably a common phenomena for n-type semiconductors). Macropores result as a consequence of the reverse biased n-Si-electrolyte interface which concentrates the hole current at pore tips. Pore initiation proceeds spontaneously on smooth silicon surfaces yielding $\approx 10^{10}/cm^2$ tiny etch pits after only a few seconds of anodization [36,56,66]. Many of these pits merge to form approximately $10^6/cm^2$ to $10^8/cm^2$ stable pores which then continue to grow into the substrate [36,56,66].

In the absence of illumination, pores grow by either electrical breakdown or interfacial tunneling which is enhanced at sharply curved pore tips [34,36,57,66,73]. These pores tend to be highly branched, tend to propagate along [100] directions in both (100) and (111) substrates, and tend to have diameters less than 1μm [56,66,73]. The inter-pore spacing (or wall thickness) is generally a little less than twice the silicon space charge width at the silicon-electrolyte interface. Pore diameters and wall thickness decrease (and pore density increases) with increasing doping density and HF concentration [66].

Macropore growth on illuminated n-type silicon proceeds by the enhanced collection of photo-generated holes at pore tips. Lehmann *et. al.* [56,73] have demonstrated that arrays of macropores hundreds of microns deep with uniform diameters can be grown when using backside wafer illumination. The authors calculated the resulting hole concentration profile which revealed that all of the photo-generated holes are consumed by the pore tips resulting in depleted and therefore inert pore walls. No macropores form when the wafer front-side is illuminated with filtered light ($\lambda < 0.8\mu m$) because most photons are absorbed near the surface and not at pore tips [56]. When front-side illumination with infrared or white-light is used holes are generated both deep in the bulk and near the surface, and macropores are observed to grow both vertically (into the substrate) and laterally (increasing in diameter) [56,74]. Macropore diameters tend to increase with increasing light intensity, increasing HF concentration, and decreasing doping density [56,74]. Primary pores and pore branches grow in (100) directions independent of wafer orientation [56].

A nanoporous silicon layer covers both the macropore walls and the top silicon surface between macropores [73,74]. The nanoporous layer thicknesses reach steady-state values of ≈2 to 6μm and ≈0.1 to 1μm for the top surface and macropore sidewalls respectively when n-Si is etched with $30mW/cm^2$ front-side white-light illumination.

Thicknesses increased with increasing doping density, and decreasing illumination intensity [74].

No significant difference has been reported for anodic oxide formation between sufficiently illuminated n-Si and illuminated or non-illuminated p-Si.

2.1.1.2 Effect of Doping Density

p-type silicon etching characteristics are nearly independent of doping density, except for a small cathodic shift in the I-V curves with increasing acceptor doping density N_A. I-V characteristics of heavily doped p^+-Si (N_A=1x10^{19}cm^{-3}) were reported to be ≈100mV cathodic of those for moderately doped p-Si (N_A=1x10^{15}cm^{-3}) [51,57]. Gaspard *et. al.* [80] report the magnitude of the cathodic shift to be proportional to $(N_A)^{1/2}$.

The electrochemical etching of heavily doped n^+ silicon, on the other hand, differs significantly from that of lightly or moderately doped n-Si. Current-voltage characteristics of n^+ silicon etched in the dark are similar to those for p-Si or illuminated n-Si [34,51,57]. A porous silicon layer is formed at low potentials where exponential I-V characteristics are observed. At slightly higher potentials the current goes through a local maximum (first current peak), followed by an electropolishing regime. Theunissen [36] measured n-Si dark etching currents as a function of donor doping density N_D in a 5% HF electrolyte and at 10V (SCE) bias. Current densities were found to increase with N_D from ≈0.01mA/cm^2 for N_D≈10^{14}cm^{-3} to ≈10mA/cm^2 for N_D≈2x10^{16}cm^{-3} to ≈500mA/cm^2 for N_D≈4x10^{18}cm^{-3}. Samples etched for 30 minutes at these conditions showed three different etching behaviors: 1) n-Si with N_D>2x10^{18}cm^{-3} dissolved rapidly leaving an electropolished surface, 2) n-Si with 2x10^{16}<N_D<2x10^{18}cm^{-3} formed a brownish-black pitted surface with pit density increasing with N_D, and 3) no etching was observed for N_D<2x10^{16}cm^{-3}.

The dark current-voltage characteristics of moderately doped n-Si (10^{16}<N_D<10^{18} cm^{-3}) show an initial current density plateau of approximately 0.01mA/cm^2 at low potentials, followed by increasing current densities at higher potentials [34,36]. Current density increases faster and begins increasing at lower potentials with increasing N_D. Current densities also increase faster and begin sooner on rough rather than chemically polished surfaces. Furthermore, dark currents of moderately doped n-Si increase with time when etched at constant potentials.

These dark n-Si etching results can be understood by the pore-tip electrical breakdown mechanism discussed earlier. Breakdown should occur at lower potentials for higher N_D because breakdown voltages are to a first approximation inversely proportional to doping density [81]. Electric field strengths become magnified at surface defects producing higher current densities on rough surfaces. Current densities further increase as small etch-pits and pores form with etching time. At doping densities above 10^{17} to 10^{18}cm^{-3}, tunneling of electrons from interface states to the conduction band becomes the

dominant charge transfer mechanism [36,81] and rapid dissolution and electropolishing becomes possible at sufficiently high potentials.

2.1.1.3 Effect of Crystal Orientation

Electrochemical etching of silicon in fluoride electrolytes is virtually isotropic. Under electropolishing conditions when oxide dissolution is rate-limiting, (111) and (100) surfaces are found have identical etch rates [64]. At lower potentials near the first current peak, both J_{crit} and the current density at potentials just after the peak are found to be slightly higher for (100) than for (111) [34,64,73] and (110) [73] surfaces. This difference however is small as compared that observed for EDP or KOH anisotropic etchants. Lehmann [73] reports that $J_{crit}(111)/J_{crit}(100)$ and $J_{crit}(110)/J_{crit}(100)$ ratios are nearly identical and range from nearly 1 for dilute 1% HF electrolytes to a minimum of 0.8 for 5% HF electrolytes. Lehmann explains preferential macropore propagation along [100] directions by the slightly higher (100) etch rate. No difference in the onset of etching potential is observed for (100), (110) and (111) surfaces.

2.1.1.4 Effect of Electrolyte pH and Fluoride Concentration

Silicon electrochemical etching currents increase with fluoride concentration (C_F) for all anodic etching potentials, illumination intensities, and silicon doping types and densities [44,46,51,55,66,67]. High C_F favors porous silicon formation since J_{crit} increases with C_F, and conversely low C_F electrolytes favor electropolishing.

The dependence of current on C_F has been reported to be first order, second order, and values in between. This discrepancy exists because electrolyte compositions vary from study to study, having some combination of HF, NH_4F, HCl, NH_4Cl, and NH_4OH components. Authors typically compare current density to the stoichiometric (total) concentration of fluoride in the electrolyte, without taking into account low HF dissociation and significant association of HF_2^- and other species.

The currents at both current peaks (J_{crit} and J_{max}) were measured as a function of pH for a low C_F electrolytes (< 1 weight % HF) [46,64]. The currents were found to be highest at pH ≈ 2.5, dropping of sharply at higher pH and more gradually at lower pH. In addition the maximum at pH ≈ 2.5 was virtually independent of C_F. Chazalviel *et. al.* [64] calculated the concentrations of various fluoride species in these electrolytes, namely F^-, HF_2^-, and HF_{undiss}, and plotted them as a function of pH. The HF_2^- ion concentration turned out to have a pH dependence nearly identical to that of etching current, implying HF_2^- species are dominant in the dissolution process. This is consistent with studies on thermal SiO_2 dissolution in HF where the HF_2^- and to a lesser extent HF_{undiss} species were determined to be responsible for oxide dissolution [82 ,83 ,84].

Silicon I-V characteristics in high C_F electrolytes (≥10 weight % HF) are noticeably perturbed [51,61], due to rapid hydrogen gas evolution which irreproducibly interferes with processes at the silicon-electrolyte interface.

Etching currents were observed to decrease with the presence of cations such as Ca^{2+}, Ba^{2+}, Al^{3+}, and K^+ due to low fluoride solubilities. Presence of anions such as Cl^- or SO_4^{2-} has no effect [64].

Addition of 1 to 2 drops of Triton X 100 non-ionic wetting agent per 100 mL of electrolyte was found to produce smoother etched surfaces[67,70], presumably by reducing the silicon-electrolyte interfacial energy and thereby reducing the sticking of hydrogen bubbles to the surface. Similar results were reported for electrolytes prepared by diluting 48% (conc.) HF with 1:1 mixtures of DI H_2O and absolute ethanol [40].

2.1.1.5 Effect of Electrolyte Agitation

Memming and Schwandt [33] and Etman *et. al.* [65] studied the effect of silicon electrode rotation rates on anodic dissolution in low C_F electrolytes (<1 weight % HF). The effect of rotation rate was found to become more significant with higher fluoride concentrations. Reproducibility of silicon current-voltage characteristics in HF were found to be excellent for rotated electrodes but poor for immobile ones , and the hysterisis between forward and reverse sweeps became less pronounced with increasing rotation rates [65]. Current densities increased with rotation rate, however the Levich relation ($J \alpha [\text{rotation rate}]^{1/2}$) was not obeyed for either the current peaks or current valleys after the peaks, indicating mass transfer is not the only rate limiting process. Based on mixed-kinetics analysis of their data, Etman *et. al.* [65] suggest diffusion limitation is caused by SiF_6^{2-} diffusion away from the surface over the entire potential range. Turner [30] however reported that the addition of fluosilicic acid (H_2SiF_6) to the electrolyte does not affect the minimum current density necessary for electropolishing, which would imply that SiF_6^{2-} diffusion is not rate limiting.

2.1.2 Electrochemical Silicon Dissolution Mechanisms

2.1.2.1 Dissolution at low current densities ($J<J_{crit}$): Amorphous silicon and mono-crystalline nanoporous silicon formation.

As discussed in section 2.1.1.1, amorphous or monocrystalline porous layers form on silicon surfaces when etched at low current densities in HF electrolytes. A reaction mechanism must exist which removes silicon atoms from the surface by replacing their back-bonds with fluoride or oxide ligands. It also must proceed preferentially at specific surface sites so that silicon only partially dissolves and forms a porous silicon layer.

Furthermore, it must explain hydrogen gas evolution at the silicon surface which is observed during porous silicon formation [29,30,32,33,71].

The dissolution reactions

Turner [30] was the first to propose a reaction mechanism to explain these observations, in which silicon is first oxidized into a divalent SiF_2 intermediate species and then chemically attacked by water, forming silicon oxide and hydrogen as discribed by the reactions:

$$Si + 2HF \rightarrow SiF_2 + 2H^+ + 2e^- \quad (2.1)$$
$$SiF_2 + 2H_2O \rightarrow SiO_2 + 2HF + H_2 \quad (2.2)$$

Memming *et. al.* [33] proposed a disproportion reaction sequence (2.3-2.7) to explain the deposition of amorphous silicon films:

$$Si + 2HF + \lambda h^+ \rightarrow SiF_2 + 2H^+ + (2-\lambda)e^- \quad (\lambda \approx 2) \quad (2.3)$$
$$SiF_2 \rightarrow Si_{(amorphous)} + SiF_4 \quad (\text{fast}) \quad (2.4)$$
$$Si_{(amorphous)} + 2H_2O \rightarrow SiO_2 + 2H_2 \quad (\text{slow}) \quad (2.5)$$
$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \quad (\text{fast}) \quad (2.6)$$

and

$$SiF_4 + 2HF \rightarrow H_2SiF_6 \quad (\text{fast}) \quad (2.7)$$

Amorphous films form by reaction 2.4 and would tend to remain on the silicon surface provided that reaction 2.5 was sufficiently slow. Only ≈40% of the SiF_2 intermediates were thought to participate in reaction 2.4, with the rest decomposing by either reaction 2.8 or 2.9:

$$SiF_2 + 2HF \rightarrow SiF_4 + H_2 \quad (\text{followed by 2.7}) \quad (2.8)$$
$$SiF_2 + 2H_2O \rightarrow SiO_2 + 2HF + H_2 \quad (\text{followed by 2.6}) \quad (2.9)$$

Reaction 2.8 proceeds chemically because the electronegative fluoride ligands form highly polarized Si-F bonds that destabilize the silicon back-bonds, allowing attack by HF [75,85]. An alternate disproportionation reaction mechanism was postulated by Peter *et. al.* [50] involving $HSiF_3$ species which were detected by Fourier-transform infrared measurements:

$$Si + h^+ + HF + 2F^- \rightarrow SiHF_3 \quad (2.10)$$
$$2SiHF_3 \rightarrow Si + H_2SiF_6 \quad (2.11)$$

competing with:

$$SiHF_3 + 3HF \rightarrow H_2SiF_6 + H_2 \quad (2.12)$$

A recurring problem with these proposed reaction schemes is that the authors overlook the initial hydrogen passivation of the silicon dangling bonds [68,75,85]. Very recently Gerischer *et. al.* [91] proposed a reaction sequence (reactions 2.13-2.19) that includes initial hydrogen passivation of the surface. The notation Si_2-$SiH_{2(surface)}$ refers to a surface Si atom with two Si-Si back-bonds and two hydrogen passivated dangling bonds. First one of the hydrogen passivated bonds is oxidized to form HF and a uncompensated electron. This electron is then passivated by fluorine in a second oxidation reaction. The highly polar Si-F bond destabilizes the Si-Si back-bonds allowing their splitting by HF molecules. This results in formation of an aqueous $HSiF_3$ molecule and restoration of the initially hydrogen passivated silicon surface. Hydrogen gas evolves later during a chemical reaction of $HSiF_3$ with water, ultimately forming the stable SiF_6^{2-} species. A schematic of the reaction sequence is shown in figure 2.2.

$$Si_2\text{-}SiH_{2(surface)} + F^- + h^+ \rightarrow Si_2\text{-}SiH^{\bullet}_{(surface)} + HF \quad (2.13)$$

$$Si_2\text{-}SiH^{\bullet}_{(surface)} + F^- + \lambda h^+ \rightarrow Si_2\text{-}SiHF_{(surface)} + (1-\lambda)e^- \quad (2.14)$$

$$Si_2\text{-}SiHF_{(surface)} + HF \rightarrow Si\text{-}SiHF_{2(surface)} + SiH_{(newly\ passivated\ dangling\ bond)} \quad (2.15)$$

$$Si\text{-}SiHF_{2(surface)} + HF \rightarrow HSiF_{3(aq)} + SiH_{(newly\ passivated\ dangling\ bond)} \quad (2.16)$$

$$HSiF_3 + H_2O \rightarrow HOSiF_3 + H_2 \quad (2.17)$$

$$HOSiF_3 + HF \rightarrow SiF_4 + H_2O \quad (2.18)$$

$$SiF_4 + 2F^- \rightarrow SiF_6^{2-} \quad (2.19)$$

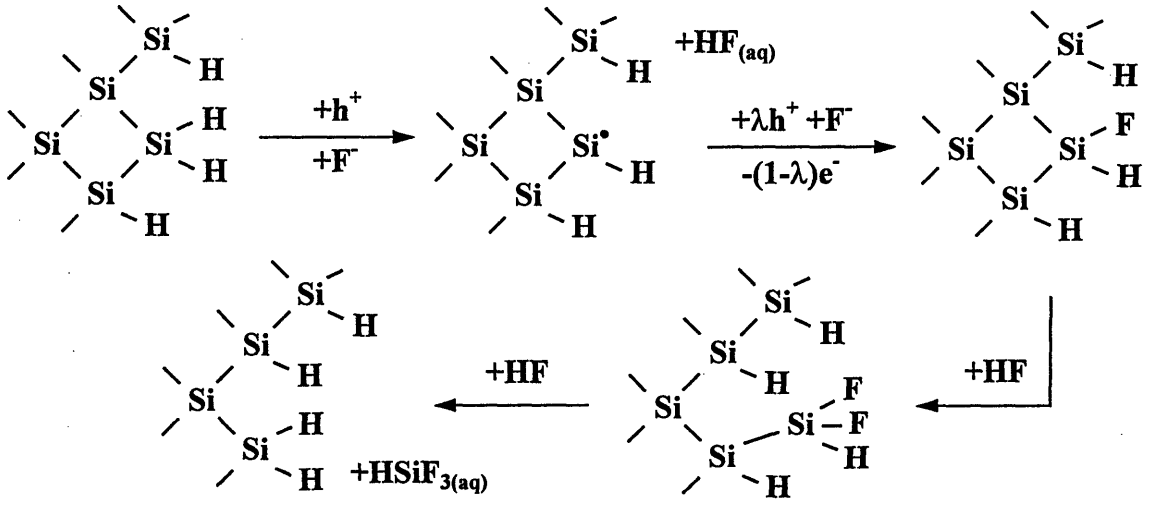

Figure 2.2. Schematic diagram of the reaction sequence 2.13-2.16 showing the electrochemical and chemical processes involved in removing a silicon atom from the surface. Redrawn from reference [91].

Matsumura *et. al.* [41] were the first to notice a photo-current doubling and quadrupling effect for n-Si etching. Photo-current doubling or quadrupling indicates that one or three electrons respectively are injected from partially oxidized silicon surface atoms into the conduction band for each photo-generated hole that is injected to silicon surface atoms from the valence band. They proposed the following overall reaction mechanism, where λ varies from 1 to 3 for photo-current doubling to quadrupling:

$$Si + 6HF + \lambda h^+ \rightarrow H_2SiF_6 + 4H^+ + (4-\lambda)e^- \quad (2.20)$$

The rate constants for electron injection into the conduction band from the various oxidized silicon states Si(0) to Si(III) are much slower than for hole injection from the valence band [47,71]. Photo-current doubling or quadrupling is therefore only observed at very low light intensities ($\leq 10\mu W/cm^2$ for Q=4 and $\leq 1mW/cm^2$ for Q=2) when holes are scarce [41,54,71].

Lewerenz *et. al.* [47] proposed the following more detailed reaction sequence for etching when photo-current quadrupling is observed. The $SiHF_3$ intermediate species and both fluorinated and hydrogenated silicon surface species participate:

$$Si + F^- + h^+ \rightarrow SiF_{(surface)} \quad (2.21)$$
$$SiF_{(surface)} + F^- \rightarrow SiF_{2(surface)} + e^- \quad (2.22)$$
$$SiF_{2(surface)} + HF \rightarrow SiHF_3 + e^- \quad (2.23)$$
$$SiHF_3 \rightarrow SiF_{3(surface)} + H^+ + e^- \quad (2.24)$$
$$SiF_{3(surface)} + F^- \rightarrow SiF_4^- \quad (2.25)$$
$$SiF_4^- + HF \rightarrow SiHF_5^- + e^- \quad (2.26)$$
$$SiHF_5^- + F^- \rightarrow SiHF_6^{2-} + H^+ + e^- \quad (2.27)$$

Reactions 2.20 and 2.21-2.29 indicate a tetravalent dissolution mechanism. This is inconsistent with the consensus in the literature that porous silicon forms by a divalent process as is represented by reactions 2.1 through 2.19 [33,39,51,55,56,71]. Blackwood *et. al.* [71] used a ring-disk electrode to measure hydrogen evolution as a function of quantum efficiency Q. A hydrogen evolution efficiency η_H of 100% is defined for the generation of one H_2 molecule per silicon atom dissolved. η_H was found to increase from 0 to 100% as the Q decreased from 4 to 2, and therefore the tetravalent dissolution only occurs at the very low current densities where photo-current quadrupling is observed. The competition between electron injection and hydrogen evolution can be illustrated by the following reaction sequence [71]:

$$Si(0) + h^+ \rightarrow Si(I) \quad (2.28)$$
$$Si(I) \rightarrow Si(II) + e^- \quad (2.29)$$
$$Si(II) \rightarrow Si(IV) + 2e^- \quad (2.30)$$

competing with:

$$Si(II) + 2H^+ \rightarrow Si(IV) + H_2 \quad (2.31)$$

Reaction 2.32 shows a more general version of the overall porous silicon formation reaction (ignoring disproportionation), where m=1 and n=0 for Q=4, m=1 and n=1 for Q=2, and m=2 and n=2 for Q=1:

$$Si + mh^+ + 6HF \rightarrow H_2SiF_6 + (4\text{-}m\text{-}n)e^- + (4\text{-}n)H^+ + 1/2nH_2 \qquad (2.32)$$

Rate-limiting dissolution processes and the evolution of porous silicon

The preceding reactions help explain the dissolution valence and reaction products observed during silicon etching, but not the observed current density nor the resulting surface morphology.

Mass transport of reactants or products through the porous layer is not rate-limiting, at least for layers up to 10 μm thick [39,51,57,80]. Some process near the silicon-electrolyte interface must therefore limit the rate. The current is found to vary exponentially with increasing potential near the onset of etching, having a slope of approximately 60 mV/decade [33,51,55,57,80]. There is disagreement in the literature as to the identity of the corresponding rate-limiting process. Some report that charge transfer across the Helmholtz double layer (Tafle kinetics) is rate-limiting [33,55,57], while others report that current flow across the silicon space-charge layer at the electrolyte interface (Schottky barrier thermionic emission) is rate limiting [42,43,80]. Others have reported that either process may limit the rate [51], or that thermionic emission is observed at lower potentials and Tafel behavior at higher potentials [63]. Both of these pocesses can result in exponential I-V characteristics with a 60 mV/decade slope as is demonstrated in chapter 3.

Gaspard *et. al.* [80] have calculated the current-voltage characteristics of p-Si electrodes, by 1) assuming that the rate-limiting process is thermionic emission across the Shottky barrier and 2) taking into account the fraction of applied potential which falls across the Helmholtz layer. Their results are consistent with the observation that the current-voltage characteristics of p-Si electrodes shift cathodically with $(N_A)^{1/2}$. Further evidence supporting a thermionic emission rather than a Tafel rate-limiting process comes from the Pourbaix diagram. Silicon oxidation is thermodynamically possible in aqueous electrolytes above -1.1 V (SCE) [86 ,76], significantly below the the zero current potential of ≈-0.4 V (SCE) and the etching onset potential ($J \geq 10$ mA/cm^2) of ≈0V (SCE). It appears that the first oxidation step in the dissolution reaction sequence proceeds exceedingly slowly by electron injection into the valence band, and etching is therefore rate-limited by thermionic emission of holes across the Schottky barrier to the silicon-electrolyte interface.

The nature of the microscopically spatially varying reaction mechanism which leads to nanopore formation is still in question. While interesting, it is of marginal importance for silicon micromachining because the faster etch rates and smoother surfaces of the electropolishing regime are preferred, and is therefore only briefly discussed. Unagami [39] proposed that silicic acid forms a hindrance layer on pore walls which protects them from further attack. Beale *et. al.* [43] proposed that pore walls are

depleted due to the silicon-electrolyte interface depletion layer, which restricts anodic current to within the pores and limits dissolution to only pore tips. Anodic current is supplied by a thermionic emission process and pore tips therefore grow wherever the barrier height is lowest, which can be influenced by impurities, random fluctuation in dopant concentrations, or the microscopically random nature of the chemical reactions with surface species. Foll [61] suggested that pore walls are stabilized by a quantum isolation effect which increases the band-gap to ≈1.5 eV resulting in hole depletion. More esoteric diffusion-limited aggregation and finite diffusion length models were also proposed which are left for the reader to pursue [74,87 ,88].

2.1.2.2 Electropolishing and Anodic Oxide Dissolution

There is a consensus in the literature that the dissolution of an anodic oxide layer limits the overall silicon electrochemical etch rate in the electropolishing regime. Studies (see section 2.1.1.5) have shown that mass transport at the oxide/electrolyte interface contributes to but is not the only rate-limiting process. Breaking of bridging Si-O bonds in Si-O-Si groupings has been reported the rate-limiting step in SiO_2 glass dissolution [83].

Silicon dissolution during electropolishing is vaguely described as a tetravalent process in which 4 holes are needed to remove each silicon atom. It reality is somewhat less than tetravalent as determined by dissolution valence (ξ) studies. ξ was measured to be 3.5 [34], 3.8 [55], 3.5 → 3.7 [67], 3.5 → 3.6 [71], and ≈4 [73].

Memming [33] proposed the first reaction sequence (2.33-2.34) in which silicon dangling bonds are passivated by and back-bonds replaced by hydroxide ligands. A slight modification was presented by Zhang *et. al.* [51] which also includes the overall oxide dissolution reaction (2.35-2.37).

$$Si + 4H_2O + 4h^+ \rightarrow Si(OH)_4 + 4H^+ \quad (2.33)$$

$$Si(OH)_4 \rightarrow SiO_2 + 2H_2O \quad (2.34)$$

$$Si + 4OH^-_{ads} + \lambda h^+ \rightarrow Si(OH)_4 + (4-\lambda)e^- \quad (2.35)$$

$$Si(OH)_4 \rightarrow SiO_2 + 2H_2O \quad (2.36)$$

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \quad (2.37)$$

Lewerenz [68] proposed a mechanism explaining how the silicon surface atom back-bonds are replaced, as shown in reactions 2.38-2.40. First holes oxidize water molecules resulting in Si-OH passivation of the silicon surface, then two neighboring Si-OH bonds split off a water resulting in a Si-O-Si bridging oxygen bond. This is thought to polarize the Si-Si back-bonds leading to oxygen insertion by a site-exchange mechanism. This reaction sequence is divalent, however, and must be limited to the onset of electropolishing.

$$Si + H_2O + h^+ \rightarrow SiOH + H^+ \quad (2.38)$$
$$2SiOH \rightarrow Si_2O + H_2O \quad (2.39)$$
$$2Si_2O \rightarrow SiO_2 + 3Si \quad (2.40)$$

One serious problem not addressed by these reaction schemes is the isolation of the silicon surface and electrolyte by the anodic oxide. Consequently reacting species must first be transported through the oxide, which includes the transport of oxygen species towards silicon and positive charges away from silicon.

The anodic oxide composition varies from the electrolyte to the bulk silicon interfaces. It primarily contains negatively charged species near the electrolyte [68,89], and positively charged species near the silicon interface [69]. Furthermore the oxide is substoichiometric in oxygen near the silicon interface [41,46,90] which is consistent with measured dissolution valences of less than 4. The substoichiometry most likely consists of oxygen vacancies which can be represented as Si-Si bonds penetrating into the oxide [41,69].

Chazalviel [69] proposed a transport mechanism consistent with the observations listed above. Holes are injected from the silicon substrate into the oxide which dissociates some of the Si-Si bonds into positively charged three-fold coordinated O_3Si^+ species: (Subscripts used here refer to the number of bonds rather than stoichiometric composition).

$$O_3SiSiO_3 + h^+ \rightarrow O_3Si^+ + O_3Si^\bullet \quad (2.41)$$
$$O_3Si^\bullet + h^+ \rightarrow O_3Si^+ \quad (2.42)$$

The charge can then move to a neighboring site by the translation of an Si-O bond as shown in reaction 2.43 and figure 2.3, resulting in a net motion of positive charge towards the electrolyte and oxygen species towards the silicon substrate:

$$O_3Si^+ + O_4Si \rightarrow O_4Si + O_3Si^+ \quad (2.43)$$

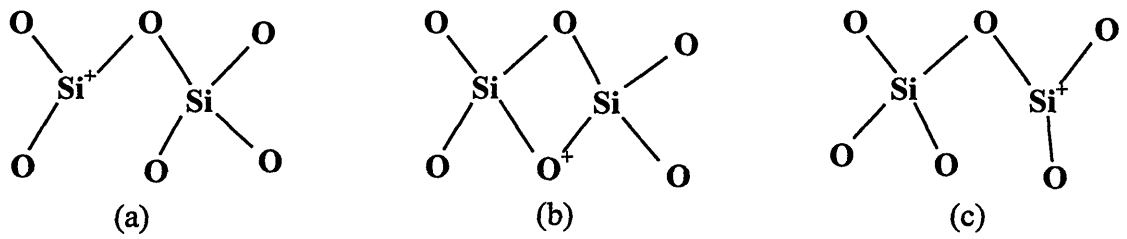

Figure 2.3. Schematic of a reaction mechanism for the transport of species through the anodic oxide: positive charges move away from the silicon/oxide interface while oxygen species move towards silicon by local redistributions.

Chazalviel also proposed a variety of other reactions which may occur within the anodic oxide as the positive charges moving towards the electrolyte annihilate negative species near the oxide/electrolyte interface:

$$O_3Si^+ + OH^- \leftrightarrow O_3SiOH \quad (2.44)$$

$$O_3SiOH \leftrightarrow O_3SiO^- + H^+ \quad (2.45)$$

$$O_3SiO^- + O_3Si^+ \leftrightarrow O_3SiOSiO_3 \quad (2.46)$$

$$O_3SiOSiO_3 + OH^- \leftrightarrow O_3SiO^- + O_3SiOH \quad (2.47)$$

$$O_3Si^+ + O_3SiOH \leftrightarrow O_3Si(OH)^+SiO_3 \quad (2.48)$$

A puzzling feature of the silicon current-voltage characteristics (see figure 2.1) is the increase in current (and dissolution rate) at potentials after the first current peak. One would instead expect the current, which is rate-limited by chemical dissolution of the oxide layer, to be independent of potential. I propose the following explanation based on Chazalviel's ion/oxygen transport mechanism and reactions 2.51-2.55. First it is clear that not all of the oxygen atoms form bridging Si-O-Si bonds (represented by $O_3SiOSiO_3$ species), but rather a highly defective oxide is formed. Second, it is known that chemical attack of the bridging oxygen bonds is the rate-limiting oxide dissolution step, and H^+ adsorption on the bridging oxygen (i.e. $O_3Si(OH)^+SiO_3$) weakens the Si-O bond catalyzing its attack [83]. At higher potentials the oxide become more nonstoichiometric near the silicon/oxide interface [41,46], providing greater numbers of Si-Si bonds that can be dissociated into O_3Si^+ species by hole injection. The rate of Si-Si bond dissociation should also increase with potential as the injection field becomes stronger and more holes become accumulated at the silicon/oxide interface. Since most of the applied potential falls across the anodic oxide [57], the transport rate of the O_3Si^+ and OH^- ions increases with rising potential forming greater numbers of weakened Si-O bonds in the form of O_3SiOH or $O_3Si(OH)^+SiO_3$ species. These effects therefore all contribute to increasing the formation rate and concentration of broken or weakened Si-O-Si bonds in the oxide, enhancing its chemical dissolution rate.

2.1.2.3 The Transition from Porous Silicon to Electropolishing

We have seen that at low potentials corresponding to porous silicon formation the silicon surface is attacked by fluoride ligands forming $SiF_{2(surface)}$ species followed by chemical attack of the Si-Si back-bonds. At higher electropolishing potentials on the other hand, the silicon surface is oxidized by oxygen species transported across the oxide. A transition between the two mechanisms must occur at intermediate potentials in the vicinity of the first current peak.

It appears this transition is not abrupt but rather proceeds over a wide potential range. Zhang *et. al.* [51] reported that a uniform porous silicon layer only forms at potentials where exponential current-voltage characteristics are observed. At higher

potentials the surface then becomes visibly rougher on a larger scale and the fraction of surface covered by porous silicon decreases to zero as the first current peak is approached. Furthermore, the etched surface is not electropolished at potentials just above the first current peak but rather progressively becomes smoother over approximately 2 volts (for 5Ωcm p-Si, 5% HF) until electropolished surfaces are obtained [31,67,70]. Dissolution valence (ξ) measurements at potentials near the first current peak also indicate a more gradual transition between mechanisms. ξ is found to increase from $\approx$2 at low porous silicon formation potentials to 2.7-2.8 [39,73], and in general to increase with potential before the first current peak [43,67]. After the peak the dissolution valence continues increasing with potential over $\approx$2 V until reaching a more stable value [55,71,73]. These results indicate a progressive increase in the fraction of surface atoms removed by a tetravalent rather than divalent mechanism with increasing potential.

Numerous authors have proposed that surface silicon atoms can be passivated by either fluoride or hydroxide ligands [44,46,51,75,91], corresponding to reactions 2.49-2.51:

$$Si + 2HF + 2h^+ \rightarrow SiF_{2(surface)} + 2H^+ \quad (2.49)$$

$$Si + 2H_2O + 2h^+ \rightarrow Si(OH)_{2(surface)} + 2H^+ \quad (2.50)$$

$$Si + H_2O + HF + 2h^+ \rightarrow SiF(OH)_{(surface)} + 2H^+ \quad (2.51)$$

Propst and Kohl [75] propose that a fluoride is more electronegative than the hydroxide and therefore destabilizes the silicon back-bonds to a lesser extent. Thus while the back-bonds of a $SiF_{2(surface)}$ species can be chemically attacked by HF forming SiF_4, the attack of $Si(OH)_{2(surface)}$ species back-bonds may be kinetically slow or even deactivated. Dissolution of the $Si(OH)_{2(surface)}$ species would therefore be a slower process requiring either an exchange of hydroxide ligands by fluoride ligands [44], or an electrochemically assisted oxidation of the back-bonds leading to tetravalent dissolution. It is reasonable to expect that the relative rates of the hydroxide passivation, fluoride passivation, and ligand exchange reactions vary with applied potential. The first current peak could then occur when the hydroxide passivation rate significantly outpaced the ligand exchange reaction or fluoride passivation rate, in effect isolating silicon atoms from fluoride ligands. Oxide formation could then proceed by reaction 2.52, and the dissolution rate would become limited by HF attack on the Si-O-Si bonds.

$$2SiOH \rightarrow Si_2O + H_2O \quad (2.52)$$

2.2 Electrochemical Micromachining

The electrochemical dissolution characteristics of silicon described above are conceptually similar to that of other semiconductors, given an appropriate electrolyte to oxidize surface atoms and effectively remove the reaction products. As a result, the various electrochemical micromachining techniques developed for one semiconductor are generally applicable to others. The following electrochemical micromachining review is therefore developed with respect to selectivity rather than semiconductor type.

2.2.1 Selectivity for Dopant Type and Density

2.2.1.1 selective etching of p versus n

Selective etching of p versus n-type semiconductors was first reported in the early 1970's. Nuese *et. al.* [12] electrochemically dissolved a p-GaAs substrate leaving behind a 2 to 10 μm thick n-layer, and Meek *et. al.* [13] dissolved a p-GaP layer from a n-GaP substrate. In both cases NaOH electrolytes were used and the anodic potential was applied directly to the p-type semiconductor. It was found that p-regions near the contact tend to etch faster, resulting in electrical isolation and incomplete etching of the p-regions further away from the contact. This was prevented either by 1) placing the counter electrode at the wafer edge furthest from the contact thereby etching the contact region slowest [12], or 2) slowly immersing the wafer into the electrolyte to ensure that the p-regions furthest from the contact dissolve first [13]. In both cases etch-stop surfaces were rough, which was attributed by Nuese *et. al.* [12] to be due to slight etching of the n-type material.

p versus n selectivity has also been demonstrated in silicon [92 -96]. In each case n-Si structures (cantilever beams or bridges) were formed on a p-Si substrate, using masked ion implantation of protons [92,94] or phosphorous [93,95]. (The nature of the implanted ion in ref. [96] was not disclosed). The n-Si structure thicknesses and widths ranged from 0.2 to 2 μm and 10 to 40 μm respectively, depending on implantation/anneal conditions and mask geometries used. Anodic biases were uniformly applied to the p-substrates using backside wafer ohmic contacts and the front surface was exposed to an HF electrolyte. The p-Si was preferentially etched at low biases corresponding to porous silicon formation [92,93,94,96]. The p-Si substrate between and immediately below the n-Si structures was converted to porous silicon and then either dissolved with dilute KOH or NaOH at room temperature [94,96], or oxidized to form SiO_2 for silicon-on-insulator electrical isolation of the structures [92,93]. In three of the studies an LPCVD Si_3N_4 layer covered the n-Si structures during the etching process. This layer was deposited to either 1) protect the structures during the subsequent oxidation of porous silicon into SiO_2 [93], 2) prevent depletion layer punch-through during anodization [94], or 3) to serve as a

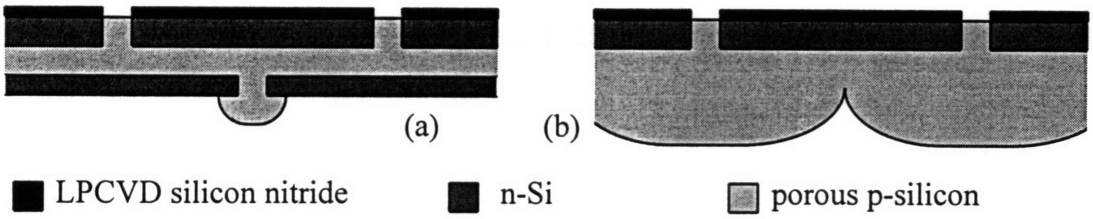

Figure 2.4. Schematic cross-section of the porous silicon formation profile attained during preferential p-Si etching with (a) and without (b) a buried n-layer etch-stop.

mask during sample IC fabrication [92]. Rather than first forming porous silicon, Branjeberg *et. al.* [95] were able to etch their structures using a 1.5V bias (applied between the p-substrate and platinum counter-electrode) and reported achieving electropolished surfaces.

Benjamin *et. al.* [94,93] further improved their process by burying a patterned n-layer etch-stop in the p-substrate below the n-Si structures. This limited porous silicon formation to the p-Si between the two n-Si regions, allowing control of the gap between the n-Si structures and substrate. A comparison of the etch profiles obtained with and without the buried n-layer is shown in figure 2.4.

The p versus n selective etching results described above contradict reports in the literature, which state that the anodic p-substrate bias will forward bias the p-n junction causing hole injection into and subsequent dissolution of the n-structures [13,97 ,98]. Both the hole injection and n-Si dissolution were confirmed by the author and are presented in the chapter 5. This apparent contradiction is explained in the discussion section.

A different p versus n selective etching technique has been reported by Yoshida *et. al.* [99]. This technique involves illuminating a sample containing p- and n-Si regions, which generates a p-n junction photobias that anodically biases p-Si with respect to n-Si. The p-Si was found to anodically dissolve while the complementary cathodic H_2 generation reaction proceeded simultaneously on n-Si regions. Such an electroless process eliminates the need for sample electrodes and external voltage sources significantly simplifying processing. The disadvantages however are 1) limited structure geometries and 2) low p-Si etching potentials which result in porous silicon formation and slow rates. The porous silicon formation rate was found to saturate at ≈0.2 to 0.3 μm/min when the ratio of p-n junction to p-silicon/electrolyte interface areas (A_{pn}/A_{se}) exceeded 50, and otherwise decreased linearly to zero with decreasing A_{pn}/A_{se}. Micro-bridges 1 μm thick by 30 μm wide were formed by etching in 10% HF for 180 minutes using 30mW/cm^2 illumination from a 1kW Xenon lamp. The p-Si surrounding the

micro-bridges was anodically oxidized into porous silicon, then oxidized in wet O_2 at 1000°C to form SiO_2, and finally removed with a chemical HF etch.

2.2.1.2 selective etching of n versus p

Very little has been reported on n versus p selectivity in the literature. n-type GaAs [100 ,101] and SiC [102 ,103] layers on p-type substrates were photoelectrochemically etched using focused (above-band-gap photon energy) laser beams. In each case the anodic bias was applied directly to the n-layer, except in ref. [101] where the process appears to be electroless with both anodic and cathodic reactions occurring on the wafer, however this was not explicitly stated by the authors. The illuminated areas of the n-layer dissolved down to the p-substrate where etching stopped.

n versus p etch selectivities were reported to be 15000 and $\approx 10^6$ for GaAs and SiC respectively. SEM micrographs of the etched regions, however, show rough side walls and non-uniform etch-stop surfaces. Some etch-stop surface roughness on SiC was due to ≈500Å patches of remnant n-SiC which became electrically isolated before etching was complete. The extent to which p-substrate dissolution or p-n interface roughness (as a result of sample processing) contributed to etch-stop surface roughness is unclear.

The anodic potential (except for ref. [101]) was kept below the etching onset potential for the p-type semiconductor and above that of the illuminated n-type semiconductor. Only n-layer etching was therefore expected. Based on experimental results obtained in this thesis, it is clear that both the location of the anodic contact and the use of localized illumination contributed to successful n versus p selectivity. By applying an anodic bias to the n-layer the p-n junction becomes reverse biased. This electrically isolates the p-substrate from anodic currents, thereby preventing its electrochemical dissolution once it is exposed to the electrolyte. Furthermore, once the illuminated n-layer area etches down to the p-substrate there is no longer any illuminated p-n junction area. This eliminates photo-current and biases effects which result in preferential dissolution of p-type regions.

The n versus p etch-stop observed in ref. [101] is explained by a semiconductor-electrolyte interface band bending mechanism, which determines whether photo-generated holes are swept to or away from the interface. The energy bands at an n-GaAs-electrolyte interface are bent upwards sweeping holes to the interface, while the bands at a p-GaAs-electrolyte interface are bent downward sweeping them away. A test sample was fabricated consisted of a semi-insulating substrate onto which 0.1 μm p-GaAs and 1.0 μm n-GaAs layers were deposited in that order. The sample was etched with 0.5 W/cm^2 light from a He-Ne laser, resulting in only n-layer dissolution and a measured n-p etch-stop selectivity of >1000.

2.2.1.3 *selective etching of n^+ versus n*

The n^+/n etch-stop was the first electrochemical dopant selective etch-stop demonstrated on silicon [104 ,105]. It has been used to form thin n-Si wafers [104,106], cantilever beams [107], diaphragms for pressure sensors [108 ,109 ,110], membranes for nuclear particle channeling studies [111], and also for fabrication of isolated integrated circuits [105,106,112]. The n^+/n etch-stop is based on the fact that moderately doped n-Si ($N_D \leq 2x10^{16}cm^{-3}$) does not anodically etch in the dark while heavily doped n^+-Si ($N_D \geq 2x10^{18}\ m^{-3}$) does. (The reader is referred back to section 2.1.1.2). Micromachining with the n^+/n etch-stop typically involves growing (and perhaps patterning) an epitaxial n-layer on an n^+-substrate, exposing all or part of the n^+-substrate to an HF electrolyte, and anodically biasing either the n or n^+ regions causing n^+ dissolution. Membranes have been etched as thin as 0.7 μm [111], and can be as thick as is limited by practical epi-layer growth. A particular advantage of the n^+/n etch-stop over the electrochemical passivation etch-stop (which use EDP or KOH anisotropic etchants) is the ability to form circular membranes due to the isotropic nature of anodic etching in HF.

It is however difficult to form high quality, mirror-smooth etch-stop surfaces. Often residual films, small pits, deep pores, and delineated defects such as stacking faults are found on the surface [104,105,106]. Although large applied potentials are required to electrically breakdown and etch lightly doped n-Si in the dark, etching proceeds at much lower potentials if pore tips are present to concentrate the field strength. Unfortunately pores often form during n^+ etching and subsequently end up at the n^+-n interface. This can significantly limit the n^+ etch rate because only a few tenths of a volt may exist between the onsets of n^+ etching and n-Si pore propagation [94]. An additional problem is the difficulty in growing high quality epi-layers (free of dislocations and stacking faults) on heavily doped substrates.

2.2.1.4 *selective etching of p^+ versus p*

It is also possible to make use of the cathodic shift of p-Si current-voltage curves with $(N_A)^{1/2}$ [80], to preferentially etch p^+-Si versus p^--Si [96]. Unfortunately the magnitude of this cathodic shift is only ≈0.1V for p-Si having doping densities of $1.5x10^{15}cm^{-3}$ and $3x10^{19}cm^{-3}$ [96]. Etching is therefore limited to porous silicon formation and very low etch rates. There are no known reports in the literature demonstrating successful micromachining with the p^+/p etch-stop. The cathodic shift phenomena has however been used to profile the acceptor impurity concentration in p-type substrates. Heavier doped p-Si has higher etching currents at a given potential. Current density can therefore be measured as a function of etch depth and then converted to an acceptor doping density-depth profile [113].

2.2.1.5 *The inversion layer etch-stop*

The inversion-layer etch-stop is related to selective etching of p versus n, except that an applied bias (rather than donor doping) is used to create an inversion layer in the p-substrate which is depleted of holes. The inversion bias can be applied to either a Schottky barrier or MOS structure. This etch-stop was briefly discussed by Lee [98] and Branebjerg *et. al.* [95], and has also been applied to the electrochemical passivation etch-stop [114 ,115].

2.2.2 *Selectivity for Illumination Intensity*

Illumination selective etching is achieved by spatially controlling light intensity over an n-type semiconductor surface. Illuminated areas are photoelectrochemical etched at rates proportional to the incident light intensity, allowing the formation of complex topological features. Most illumination selective studies were performed on III-V semiconductors, and include the use of 1) optical masks to form localized recesses and high aspect ratio structures [14,116], 2) pattern projection to form topographical micro-lenses [15], 3) focused laser beams to form vias or tunnels [15,16,117], and 4) an interference pattern of two noncolinear intersecting laser beams to form diffraction gratings [17].

Ostermayer *et. al.* [118] developed a theoretical model to predict the depth and spatial resolution of diffraction grating formed in III-V semiconductors as a function of illumination intensity and wavelength, drift and diffusion of photo-generated holes, and the semiconductor dissolution reaction rate. The theory was verified with experimental measurements, and predicted that higher resolutions (or aspect ratios) are achieved with faster surface reaction rates. Fast rates rapidly consume holes at the semiconductor surface preventing their lateral diffusion away from the illuminated areas.

Very little has been reported on illumination selective etching of silicon. Tenerz *et. al.* [119] used a He-Ne laser beam to etch a hole through an n-Si wafer, and Eddowes [120] used a patterned optical mask of undisclosed composition in an attempt to etch high aspect ratio structures. Eddowes found that two distinctly different results were obtained, depending on whether the dissolution kinetics are limited by the oxidation reaction rate or by the dissolution of oxidized species from the surface. The second case corresponds to etching in the electropolishing regime where an anodic oxide covers the surface. The etch-rate is limited by oxide dissolution and photo-generated holes therefore have ample time to diffuse laterally before they are consumed at the surface, resulting in isotropic etching. Eddowes reported that samples etched under these conditions showed smooth electropolished surfaces and underetching below the mask edge with an undercut length approximately equal to the etch depth. Eddowes also etched samples under illumination intensity-limited conditions so that the formation of oxidized species became rate limiting. A very rough porous silicon surface was obtained after etching to a 50 μm

depth, having ≈20 μm deep macropores. The sidewalls at the mask edges were reported as rough but 'minimally' undercut. Eddowes' results are consistant with the above theory of Ostermayer *et. al.*.

Illumination selective etching was also demonstrated on a n-type beta-SiC sample masked with patterned 1000Å Cr and 3000Å Au layers [121]. The Cr etched slowly and is therefore not an ideal mask material. The SiC was etched in a 2.5% HF electrolyte using ≈0.85 V (SCE) and ≈0.5 W/cm^2 UV illumination from a 200 W Hg arc lamp. Etch rates under these conditions were ≈530Å/min, and etched surfaces had ≈0.2 to 0.3 μm roughness features thought to be caused by defect delineation.

2.2.3 Selectivity for Minority Carrier Lifetime

The minority carrier lifetime etch-stop is conceptually similar to illumination selective etching. Both use illumination to etch n-Si, but rather than spatially modulating light intensity to control etching, the minority carrier lifetime etch-stop uses ion implanted damage to spatially vary the recombination rates of the photo-generated holes. This technique has been demonstrated on Si and GaAs wafers [122 ,123 ,124 ,125], however there are as yet no reports in the literature of its application to MEMS fabrication.

The minority carrier lifetime etch-stop technique is not suitable for etching of high aspect ratio structures because the vertical etch-stop dimensions are limited by low (≤1μm) ion-implantation depths. It does however permit underetching of very thin free standing structures or membranes. Lee *et. al.* [123] used 120 keV phosphorous implantation to fabricate films having a thickness of ≈155 nm, which agreed well with the expected 150nm projected range. Good etch-stops require sufficiently high concentrations of ion-implantation induced recombination centers, to ensure that photo-generated holes are annihilated before being swept to the electrolyte interface. Implantation doses ≈10^{13}/cm^2 into n-Si wafers were sufficient for B, Ne and P ions but not for protons which are too light to create sufficient damage.

2.2.4 Selectivity for Band-Gap

Etching studies of III-V semiconductor heterostructures have demonstrated that the lower band-gap semiconductor can be preferentially dissolved. GaAs/AlGaAs heterostructures consisting of alternating n-type AlGaAs and GaAs layers were etched in an electroless process (no externally applied bias) using focused laser beams [18]. Photo-generated holes were confined in the GaAs layers due to the 0.4 eV valence band discontinuity, resulting in lateral GaAs etching and undercutting of the AlGaAs layers by ≈10 μm. Khare *et. al.* [101] illuminated similar heterostructures with 800nm photons and found that while at these wavelengths, holes were only generated in the lower band-gap

GaAs layers, thin ≈0.2 μm AlGaAs layers would also etch. Some of the holes generated in the underlying GaAs layer crossed the GaAs/AlGaAs valence band barrier by tunneling or thermionic emission and were then be swept to the semiconductor-electrolyte by the interfacial band bending. If thicker AlGaAs layers were used, however, these holes recombined before reaching the surface and etching stopped at the AlGaAs surface.

Nuese *et. al.* [12] used an n-$GaAs_{1-x}P_x$/p-GaAs heterostructure to improve the surface quality of their p versus n etch-stop. The etch-stop surfaces obtained from p-n GaAs homostructure samples were rough due to slight etching of the n-type material, but mirror smooth for the heterostructure samples. They proposed that n-layer etching resulted from either minority hole diffusion from within the n-type material to the semiconductor-electrolyte interface or by thermal electron-hole generation within the interfacial space-charge layer. Smoother surfaces would therefore be obtained with the higher band-gap n-GaAsP layer which has lower minority hole concentrations and diffusion lengths. It is much more probable, however, that holes were injected into the n-layer by the forward biased p-n junction, which would not happen across the valence band discontinuity barrier at the GaAs/GaAsP interface.

While silicon, germanium and silicon carbide have all been electrochemically etched, there have been no reports in the literature of bandgap selective etching for the Si-Ge-C system.

Chapter 3

Theory

The electrochemical etch-rate of silicon is closely related to the anodic current density across the silicon-electrolyte interface, as demonstrated by our results in chapter five. In chapter two we have shown that the current density is limited by either the applied potential across the silicon-electrolyte interface or by the availability of holes at the interface. Thus in order to predict whether specific p- or n-regions of a p-n structure will etch, it is necessary to determine both the magnitude of the hole current in those regions and their potentials with respect to the electrolyte.

In this chapter we develop the theoretical aspects concerning the distribution of currents and potentials within structures containing p-n junctions. First the current-voltage equations characteristic of the p-n junctions and silicon-electrolyte interfaces are presented. These equations are then combined to model the current-voltage characteristics of the overall structures. Ultimately the etch rates of the various p- or n-regions regions can be calculated, and p-n junction etch-stop performance can be evaluated as a function of sample doping profiles and etching parameters.

3.1 The Semiconductor-Electrolyte Interface

A semiconductor-electrolyte interface some characteristics of both metal-semiconductor and metal-electrolyte interfaces. When two materials are contacted the Fermi levels of both equalize by a redistribution of mobile charges, resulting in excess charge and a potential drop at the interface. (While there is in fact no Fermi energy of an electrolyte because Fermi statistics do not apply to redox couples in solution, this term has been used for convenience in the literature and actually means the Fermi energy of the solid that is in equilibrium with the electrolyte). At metal-metal interfaces the excess charge develops over only a few angstroms because of the metals' high electron concentrations. At metal-semiconductor interfaces, all of the potential drop falls across the semiconductor space charge layer which extends into the semiconductor from the interface due to their relatively low free carrier concentrations [81]. Similarly, at metal-electrolyte interfaces all of the potential drops across the electrolyte in the Helmholtz

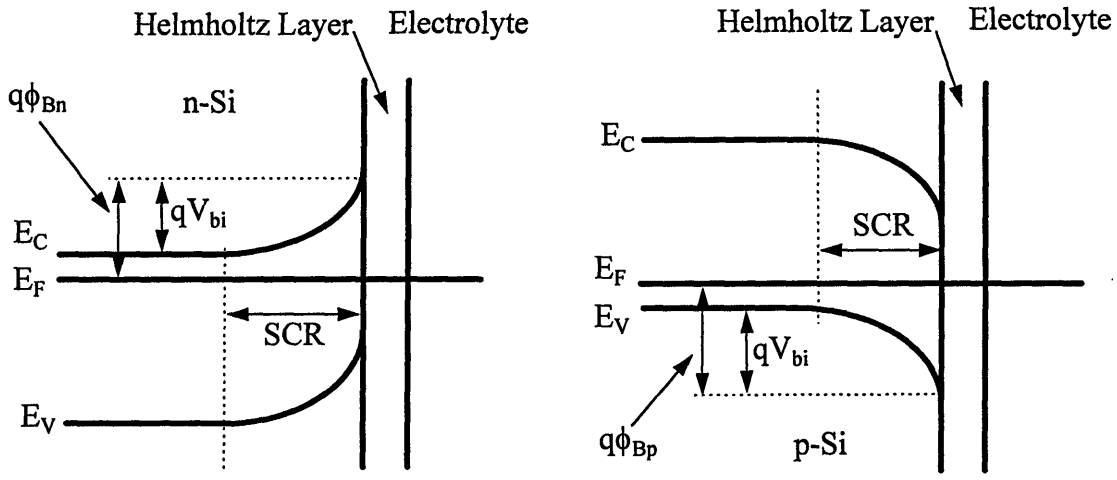

Figure 3.1. Energy band diagrams of n- and p-type semiconductor-electrolyte interfaces showing the semiconductor space charge region (SCR) and electrolyte Helmholtz layer.

layer, which is composed of specifically and nonspecifically adsorbed ions at the interface [126].

At semiconductor-electrolyte interfaces, the potential drop is distributed between the semiconductor space-charge and electrolyte Helmholtz layers, with the relative magnitudes depending on the semiconductor doping density, electrolyte concentration, presence of interface states, and the semiconductor and electrolyte dielectric constants [26]. The energy band diagrams of n- and p-type semiconductor-electrolyte interfaces are drawn in figure 3.1 showing the Helmholtz layer, semiconductor space charge region (SCR), Schottky barrier heights ϕ_{Bn} and ϕ_{Bp}, and the built-in junction potentials V_{bi}.

The sum of the n and p-Si barrier hights equal to the energy band gap:

$$q(\phi_{Bn}+\phi_{Bp})=E_g \tag{3.1}$$

and the built-in junction potential and barrier height are related through E_C-E_F and E_F-E_V for n and p-type semiconductors respectively, as is shown in equation 3.2:

$$\begin{aligned}\phi_{Bn} &= V_{bi(n)} + \frac{kT}{q}\ln\left(\frac{N_C}{N_D}\right)\\ \phi_{Bp} &= V_{bi(p)} + \frac{kT}{q}\ln\left(\frac{N_V}{N_A}\right)\end{aligned} \tag{3.2}$$

Two other factors not included in figure 3.1 can affect the potential distribution at semiconductor-electrolyte interfaces. These include the presence of semiconductor interface states and an electrolyte Gouy layer. Interface states, while important in many semiconductor-electrolyte systems, have a negligible effect on the silicon-HF system because the surface states are passivated by hydrogen atoms. The Gouy layer is a diffuse extension of the Helmholtz layer composed of ions electrostatically attracted to the interface charge, and is only significant in very dilute electrolytes. From this point forward only silicon electrodes in non-dilute HF electrolytes will be considered in the discussion and the influence of Gouy layers and surface states is therefore ignored.

As discussed in chapter 2, the semiconductor-electrolyte interface potential is measured with respect to a reference electrode. The potential distribution diagram of a biased p-silicon-electrolyte interface is drawn in figure 3.2, showing the relative potentials of the electrolyte, reference electrode, and bulk silicon. The difference between the reference electrode potential (V_{REF}) and the electrolyte 'Fermi level' ($V_{electrolyte}$) is a constant labeled as C, and is equal to the sum of the other potentials:

$$C = V_a + \Psi_s + V_H \tag{3.3}$$

V_a is the silicon potential that is measured with respect to the reference electrode during experimentation, V_H is the potential drop across the Helmholtz layer, and Ψ_s is the potential difference between the silicon bulk and the silicon surface. Ψ_s is given by equation 3.4, where V_{bi} is the built in junction potential and V_{SCR} is the fraction of the overall potential drop across the silicon-electrolyte interface that falls across the SCR.

$$\Psi_s = V_{bi} - V_{SCR} \tag{3.4}$$

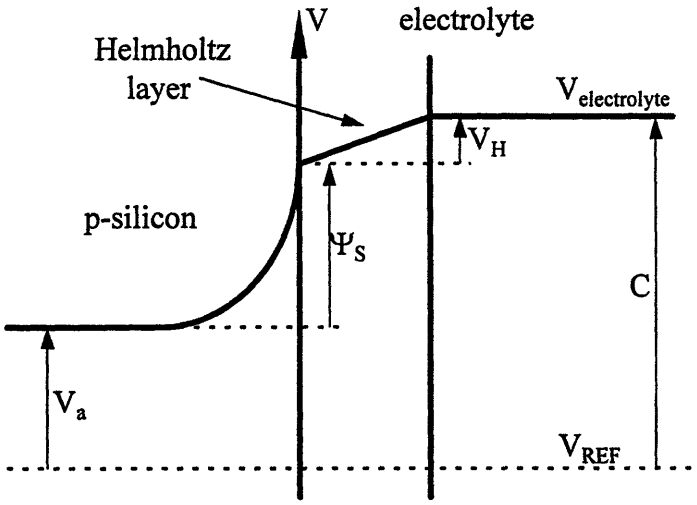

Figure 3.2 Potential distribution diagram of a silicon-electrolyte interface, showing the relationship between the reference electrode, electrolyte, and bulk-silicon potentials.

From figure 3.2 it is clear that the potential drop across the silicon-electrolyte interface, which we will refer to as V_{sei}, is equal to $C\text{-}V_a$ as shown in equation 3.5.

$$V_{sei} = C - V_a = \Psi_s + V_H \tag{3.5}$$

Equation 3.3 assumes that the resistances of the silicon substrate, the silicon ohmic contact, and the electrolyte are negligible. When appreciable current flows across the silicon-electrolyte interface these assumptions are not valid and need to be corrected for. The standard electrochemical procedure is to keep the reference electrode as close as possible to the working electrode without blocking its access to the electrolyte. Some separation is therefore necessary in which a potential drop can be generated. This effect is enhanced by the experimental apparatus used in this thesis which requires a silicon to reference electrode separation of ≈15mm. If the electrolyte, silicon, and ohmic contact resistances (R_{el}, R_{si}, R_C) are known, the measured potential (V_a) can be corrected by subtracting the resistive potential drop $i(R_{el}+R_{si}+R_C)$ from it:

$$V_{eff} = V_a - i(R_{el}+R_{si}+R_C) \tag{3.6}$$

3.1.1 I-V Characteristics of Bulk p-Si-Electrolyte Interfaces

Modeling of anodic etching currents at high potentials corresponding to electropolishing conditions is a difficult problem because of the many variables affecting the oxide dissolution rate. Such currents and etch-rates are therefore best obtained from experimental data which is presented in chapter 5. The modeling of p-n junction etch-stops fortunately only requires equations for low currents near the onset of etching where the problem is more tractable. These equations are now developed.

p-Si current-voltage characteristics were calculated by Gaspard *et. al.* [80] under the assumption that the rate limiting process is thermionic emission across the SCR. By taking into account the fraction of applied potential that falls across the Helmholtz layer their calculations predict a cathodic shift in p-Si current-voltage characteristics with $(N_A)^{1/2}$, consistent with experimental results. The thermionic emission current-voltage characteristics of a Schottky barrier are given by:

$$J = \left[A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right)\right]\left[\exp\left(\frac{qV_{SCR}}{kT}\right) - 1\right] \tag{3.7}$$

where A^* is a constant, ϕ_B is the Schottky barrier height, and V_{SCR} the externally applied potential across the barrier [81]. The -1 term within the second brackets is ignored for a silicon-electrolyte interface because the irreversible anodic reaction blocks the reverse

cathodic current. While other cathodic reactions such as hydrogen evolution may occur these will ignored. Thus by using equations 3.2-3.4, equation 3.7 can be rewritten as:

$$J = A^{*}T^{2}\frac{N_A}{N_V}\exp\left(-\frac{q\Psi_S}{kT}\right) \tag{3.8}$$

Equation 3.3 can be rewritten as:

$$\Psi_s = C - V_a - V_H \tag{3.9}$$

and substituted into equation 3.8 to give:

$$\begin{aligned} J &= K\exp\left(\frac{q(V_H + V_a)}{kT}\right) \\ K &= A^{*}T^{2}\frac{N_A}{N_V}\exp\left(-\frac{qC}{kT}\right) \end{aligned} \tag{3.10}$$

By using the electrical displacement conservation equation (eqn.3.11) at the silicon-electrolyte interface, the Helmholtz potential drop can be evaluated by equation 3.12:

$$\varepsilon_S E_S = \varepsilon_H E_H \tag{3.11}$$

$$V_H = E_H\delta = (\varepsilon_S/\varepsilon_H)E_S\delta = \varepsilon_S E_S/C_H \tag{3.12}$$

where E_H, E_S, ε_H, ε_S are the electric fields and dielectric permitivities in the Helmholtz layer and semiconductor surface, and δ and C_H are the Helmholtz layer thickness and capacitance respectively. The semiconductor electric field is given by [81]:

$$E_S = \sqrt{\frac{2qN_A}{\varepsilon_S}\left(\Psi_S - \frac{kT}{q}\right)} \tag{3.13}$$

Equation 3.12 can be evaluated by substituting for E_S with equation 3.13 and using equation 3.8 to calculate Ψ_s, giving:

$$V_H = \frac{1}{C_H}\sqrt{2\varepsilon_S N_A kT[-\ln(J) + \ln(A^{*}T^{2}) + \ln(N_A/N_V) - 1]} \approx K'\sqrt{N_A} \tag{3.14}$$

Calculated V_H values based on equation 3.15 [80] for lightly and heavily doped p-Si at current densities of 1 and 100 mA/cm^2 are summarized in table 3.1. The effect of the logarithmic terms on V_H are small in comparison to the effect of changes in N_A, and V_H therefore increases to a good approximation with $N_A^{1/2}$. The current-voltage characteristics for p-Si can therefore be calculated using equations 3.10 and 3.14, and should shift cathodically with $N_A^{1/2}$ as the V_a+V_H term in equation 3.10 increases with $N_A^{1/2}$.

	$J = 1$ mA/cm^2	$J = 100$ mA/cm^2
$N_A = 10^{15}$ cm^{-3}	$V_H = 1.26$ mV	$V_H = 1.09$ mV
$N_A = 10^{19}$ cm^{-3}	$V_H = 153$ mV	$V_H = 140$ mV

Table 3.1. Helmholtz potential drop at p-Si electrolyte interfaces as a function of acceptor doping density and current density.

3.1.2 I-V Characteristics of Bulk n-Si-Electrolyte Interfaces

Photo-induced hole currents at illuminated n-Si-electrolyte interfaces depend on the collection efficiency of photo-excited holes at the interface. Uosaki and Kita [26] have presented the following approach for calculation the photo-current at reverse biased silicon-electrolyte interfaces. Assuming all holes generated in the SCR contribute to the photo-current (i.e. without recombining in the SCR or at the interface) then the current from this region is:

$$J_{drift} = \int_0^{W_{SCR}} g(x)dx = -qI_o[\exp(\alpha W_{SCR}) - 1] \tag{3.15}$$

where g(x) is the minority hole generation rate depending on the photon absorption coefficient α, the depth from the surface x, and number of incident photons I_o:

$$g(x) = I_o \alpha \exp(-\alpha x) \tag{3.16}$$

and W_{SCR} is the SCR depletion width given by:

$$W_{SCR} = \sqrt{\frac{2\varepsilon_s}{qN_D}\left(\Psi_s - \frac{kT}{q}\right)} \tag{3.17}$$

For an n-Si electrolyte junction equation 3.3 can be written as:

$$C = V_a - \Psi_s + V_H \tag{3.18}$$

where the Ψ_s is negative due to the convention that forward biases are positive. The n-Si flat-band potential, which was measured to be -0.5V (SCE) [48,59] and -0.57V (SCE) [63], corresponds to the potential at which $\Psi_s = 0$ assuming that $\partial V_H/\partial V_a=0$. Therefore Ψ_s can be solved in terms of V_a for substitution into equation 3.17:

$$\Psi_s = V_a - C + V_H \approx V_a + 0.52 \tag{3.19}$$

where 0.52 represents the average of the flat-band potentials.

The photo current contribution from outside the SCR can be solved using the hole continuity equation (3.20) and boundary conditions of $p = p_o$ at $x = \infty$ and $p = 0$ at $x = W_{SCR}$.

$$\frac{\partial p(x)}{\partial t} = D\left[\frac{\partial^2 p(x)}{\partial^2 x}\right] + g(x) - \frac{p(x)}{\tau} \tag{3.20}$$

$$J_{diff'n} = qI_o \frac{\alpha L_D}{1+\alpha L_D} \exp(-\alpha W_{SCR}) + qp_o \frac{D}{L_D} \tag{3.21}$$

L_D and D are the hole diffusion length and diffusion coefficient respectively. The total photo-current is obtained by adding J_{drift} and $J_{diff'n}$' after omitting the last term in equation 3.21 which is not significant for large band-gap semiconductors. 0.494 represents 0.52 - kT/q.

$$J_{ph} = qI_o\left[1 - \frac{\exp\left[-\alpha\sqrt{\frac{2\varepsilon_s}{qN_D}\left(V_a + 0.494\right)}\right]}{1+\alpha L_D}\right] \tag{3.22}$$

Equations 3.15, 3.21, and 3.22 are compared to measured current-voltage characteristics of illuminated n-Si in figure 3.3. Values of $N_D = 7\text{x}10^{15}$ cm^{-3}, $L_D = 5\text{x}10^{-3}$ cm [81], and $qI_o = 0.0772$ A/cm^2 (from 87 mW/cm^2) were used in the calculations corresponding to the experimental parameters. The measured current-voltage characteristics used white light illumination, but in order to use equation 3.22 in a

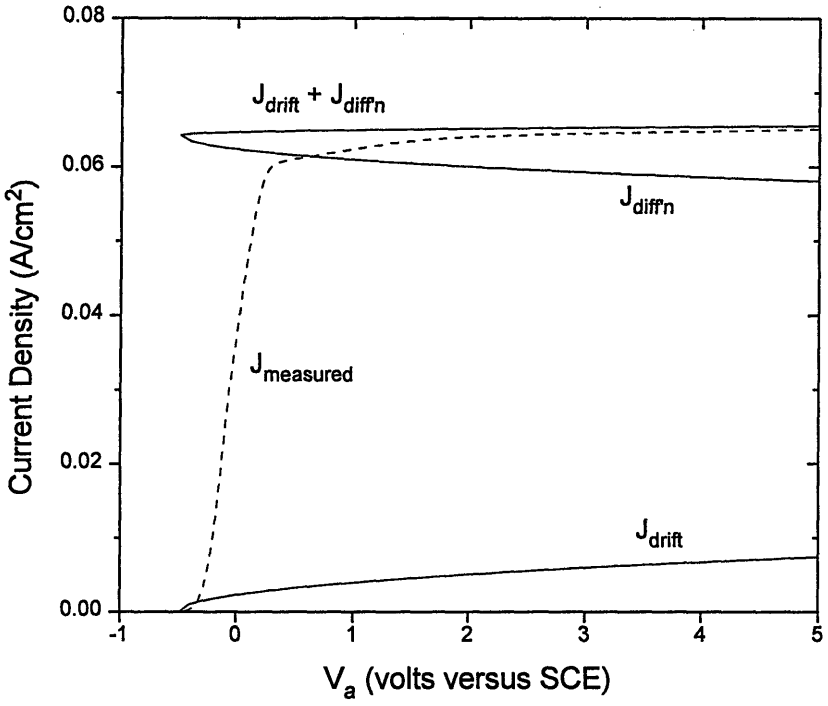

Figure 3.3. A comparison of the photo-current at a n-Si electrode as calculated using equations 3.15, 3.21, and 3.22 to the measured n-Si current-voltage characteristics. $J_{measured}$ was obtained using 5% HF, 5 Ωcm n-Si, 200 mV/s sweep rate, and 87 mW/cm^2 white light illumination. The experimental procedure is described in chapter 4.

convenient form an effective value of $\alpha = 1000cm^{-1}$ is used which corresponds to an estimated average photon wavelength of $\lambda = 0.8\mu m$ as estimated from the relative spectral response curve in figure A2.3. The calculated and measured curves agree well for $V_a > 1V$, however they clearly do not apply for $V_a < 0.2V$ and become undefined for $V_a < -0.494V$.

Wilson [22] refined this model by taking into account the hole surface recombination rate and charge transfer rate at the silicon-electrolyte interface, which are given by:

$$J_{rec} = S_{rec}p_s = S_{rec}p_w\exp\left(\frac{q\Psi_s}{kT}\right) \tag{3.23}$$

$$J_{CT} = S_{CT}p_s = S_{CT}p_w\exp\left(\frac{q\Psi_s}{kT}\right) \tag{3.24}$$

where p_s and p_w are the hole concentrations at the silicon-electrolyte surface and depletion region edge (x = W) respectively, and S_{rec} and S_{CT} are recombination and charge transfer parameters given by:

$$S_{rec} = \int_{E_v}^{E_c} \upsilon \sigma_R N_R(E) dE \left\{ \begin{array}{l} 1 + \exp\left(\frac{q\Psi_S}{kT}\right)\exp\left(\frac{E - E_F}{kT}\right) + \\ R\exp\left(\frac{q\Psi_S}{kT}\right)\left[1 + \exp\left(-\frac{q\Psi_S}{kT}\right)\exp\left(\frac{E - E_F}{kT}\right)\right] \end{array} \right\} \tag{3.25}$$

$$S_{CT} = \int_{E_v}^{E_c} \upsilon \sigma_{CT} N_{CT}(E) dE \tag{3.26}$$

$N_R(E)$ and $N_{CT}(E)$ are area densities of recombination and charge transfer centers, υ is the hole thermal velocity, and σ is the interaction cross-section. The continuity equation is then solved with the boundary condition p = 0 at x = W replaced by

$$J = -D\left[\frac{\partial p(x)}{\partial x}\right] = Sp(x) \qquad \text{at } x = W \tag{3.27}$$

where S is a boundary condition parameter to be determined. Thus $J_{diff'n}$ equals

$$J_{diff'n} = qI_o\left(\frac{L}{L + D/S}\right)\left(\frac{\alpha L_D}{1 + \alpha L_D}\right)\exp(-\alpha W_{SCR}) \tag{3.28}$$

The two unknowns, S and p_w, can be solved for by equating:

$$Sp_w = J_{diff'n} = J_{rec} + J_{CT} \tag{3.29}$$

giving

$$S = \frac{(S_R + S_{CT})\exp\left(\frac{q\Psi_S}{kT}\right) - \frac{(D/L_D)[1 - \exp(-\alpha W)]}{\exp(-\alpha W)[\alpha L_D/(\alpha L_D + 1)]}}{1 + \frac{[1 - \exp(-\alpha W)]}{\exp(-\alpha W)[\alpha L_D/(\alpha L_D + 1)]}} \tag{3.30}$$

The expected cell current can then be calculated with the equation

$$J_{ph} = qI_o \frac{S_{CT}}{S_{rec} + S_{CT}} \left[1 - \frac{\exp[-\alpha W]}{1+\alpha L_D} + \exp[-\alpha W] \left(\frac{L_D}{L_D + D/S} \right) \left(\frac{\alpha L_D}{\alpha L_D + 1} \right) \right] \quad (3.31)$$

Wilson calculated n-Si current-voltage characteristics based on equation 3.31 and obtained curves having the same shape as the measured curve in figure 3.2. The onset voltage was found to shift cathodically by 0.06V for each order of magnitude increase in $(S_{rec} + S_{CT})$ [22].

3.2 I-V Characteristics of p-n Junctions

The ideal p-n junction current-voltage characteristics are given by the Shockley equation 3.32, where V_{pn} is the applied voltage drop across the junction, p_{no} and n_{po} are the minority electron and hole concentrations, D_n and D_p are the electron and hole diffusivities, and L_n and L_p are the electron and hole diffusion lengths.

$$J_{pn} = J_S \left[\exp\left(\frac{qV_{pn}}{kT} \right) - 1 \right] \quad (3.32)$$

$$\text{where} \quad J_S = \frac{qD_p p_{no}}{L_p} + \frac{qD_n n_{po}}{L_n}$$

The current-voltage characteristics of silicon p-n junctions however deviate from ideal behavior. Generation and recombination currents in the depletion zone, surface leakage currents, tunneling and reverse bias breakdown can significantly contribute to the current at various potentials. The reverse bias current of silicon p-n junctions is dominated by the generation current given by equation 3.33 where τ_e is the effective lifetime and W is the depletion width:

$$J_R = \frac{qn_i W}{\tau_e}$$

$$\text{where} \quad \tau_e = \frac{\sigma_p \sigma_n \upsilon_{th} N_t}{\sigma_p \exp\left(\frac{E_t - E_i}{kT} \right) + \sigma_n \exp\left(\frac{E_i - E_t}{kT} \right)} \quad (3.33)$$

σ is the capture cross section, υ_{th} is the thermal velocity, N_t and E_t are the recombination center density and energy, and E_i is the intrinsic Fermi level.

At low forward biases a recombination current dominates over the Shockley diffusion current giving

$$J_F = qn_i W \frac{\sigma \upsilon_{th} N_t}{2} \exp\left(\frac{qV_{pn}}{2kT}\right) \tag{3.34}$$

where $\sigma\upsilon_{th}N_t/2 \approx 1/\tau_e$ [81]. Therefore assuming that generation-recombination currents dominate over Shockley diffusion currents, the p-n junction current-voltage characteristics can be written as:

$$J_{pn} = J_F - J_R = \frac{qn_i W}{\tau_e}\left[\exp\left(\frac{qV_{pn}}{2kT}\right) - 1\right] \tag{3.35}$$

W is the p-n junction depletion width given by equations 3.36 to 3.38 for the overall and single-sided depletion zone widths respectively. $V_{bi(pn)}$ is the junction built-in potential given by equation 3.39.

$$W_{pn} = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)(V_{bi(pn)} - V_{pn} - 2kT/q)} \tag{3.36}$$

$$W_p = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_D}{N_A(N_A + N_D)}\right)(V_{bi(pn)} - V_{pn} - 2kT/q)} \tag{3.37}$$

$$W_n = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_A}{N_D(N_A + N_D)}\right)(V_{bi(pn)} - V_{pn} - 2kT/q)} \tag{3.38}$$

$$\text{where} \quad V_{bi(pn)} = \frac{kT}{q}\ln\left(\frac{N_D N_A}{n_i^2}\right) \tag{3.39}$$

Surface leakage currents can significantly contribute to the p-n junction current-voltage characteristics if the junctions extend to poorly passivated surfaces with large surface state densities. This proved to be the case for some of the test samples used in this thesis which were diced with a diamond saw, resulting in a cut through the p-n junctions. The leakage current was especially noticeable at reverse biases giving approximately three orders of magnitude higher currents than expected, and were found to decrease after if the samples were dipped in HF, presumably by etching some of the surface damage and hydrogen passivating the surface bonds.

When illuminated, the p-n junction current-voltage characteristics are:

$$J_{pnIL} = J_S\left[\exp\left(\frac{qV_{pnIL}}{kT}\right) - 1\right] - J_L \tag{3.40}$$

where J_L is the short circuit photo-current. The photo-bias generated by an illuminated p-n junction is obtained by solving equation 3.40 for V_{pnIL}, giving:

$$V_{pnIL} = \frac{kT}{q}\ln\left(\frac{J_{pnIL} + J_L + J_S}{J_S}\right) \tag{3.41}$$

3.3 The Effect of Buried p-n Junctions on Silicon-Electrolyte Interface I-V Characteristics: The Distribution of Applied Potentials

In section 3.1 we related the potential drop across the silicon-electrolyte interface (V_{sei}) to the measured potential (V_a) as given in equation 3.5, and showed how V_{sei} is distributed between the Helmholtz layer and SCR. When samples containing both p- and n-regions are anodically etched, some of the potential drop (V_{sei}) will also fall across p-n junctions that are in the current path. In such cases equation 3.5 is modified as follows:

$$V_{sei} = C - V_a = \Sigma_i \Psi_{pn(i)} + \Psi_s + V_H \tag{3.42}$$

where $\Sigma_i \Psi_{pn(i)}$ is the summation of potential drops across one or more p-n junctions with the convention that forward biases are positive.

This equation is now solved for three specific sample doping profiles to determine the potential distributions between the various junctions, which allows calculation of the anodic current to the silicon-electrolyte interface.

3.3.1 p-Layer on n-Substrate

The energy band and potential distribution diagrams for a p-layer on n-substrate sample is shown in figure 3.4. When such a sample is anodically biased the p-n junction becomes reverse biased while the Schottky barrier at the silicon-electrolyte interface is

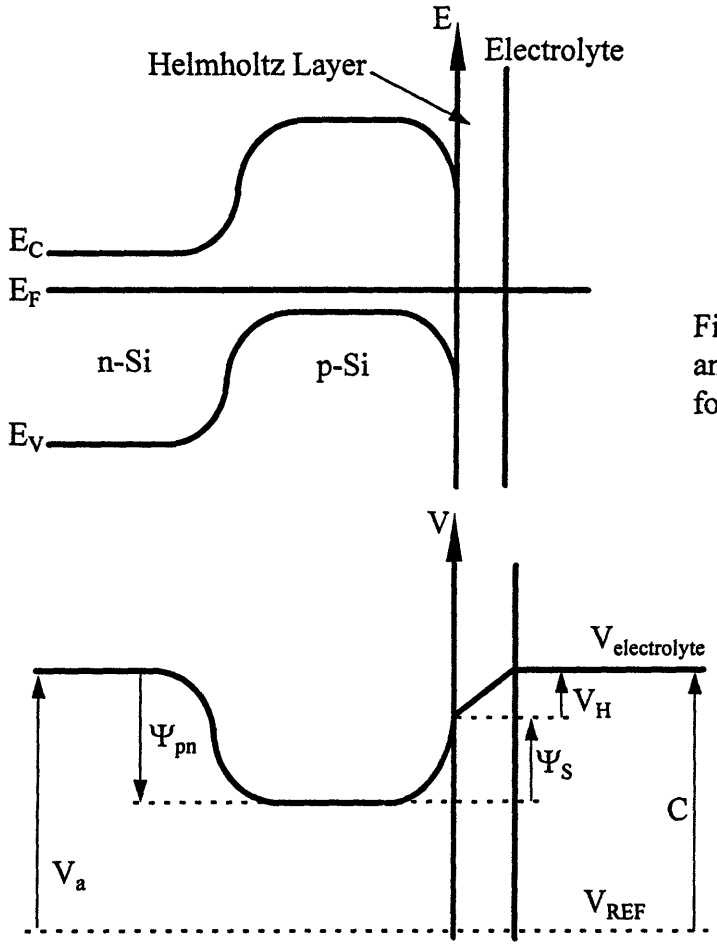

Figure 3.4. Energy band diagram and potential distribution diagrams for a p-layer on n-substrate sample.

forward biased. Etching of the p-layer will be impeded by the reverse biased p-n junction which blocks the flow of anodic current.

Equation 3.42 can be rewritten for the p-layer on n-substrate case by substituting $-V_{bi(pn)}+V_{pn}$ for $-\Psi_{pn}$, where the negative sign arises from the convention of positive forward biases. Thus

$$V_{sei} = C - V_a = -\Psi_{pn} + \Psi_s + V_H \tag{3.43}$$

and therefore:

$$V_{SCR} - V_{pn} = V_a - C - V_{bi(pn)} + V_{bi(scr)} + V_H \tag{3.44}$$

Assuming that hole recombination at the silicon-electrolyte interface is negligible and that the p-n junction and silicon-electrolyte interface areas are equal, the p-n junction, SCR, and external cell current densities must be equal in magnitude:

$$J_{cell} = - J_{pn} = J_{SCR} \tag{3.45}$$

The SCR and p-n junction current-voltage characteristics (equations 3.8 and 3.35 respectively) can be rewritten as equations 3.46 and 3.47, and then equated giving equation 3.48:

$$J_{SCR} = A^{*}T^{2}\frac{N_A}{N_V}\exp\left(-\frac{qV_{bi(SCR)}}{kT}\right)\exp\left(\frac{qV_{SCR}}{kT}\right) = \vartheta\exp\left(\frac{qV_{SCR}}{kT}\right) \tag{3.46}$$

$$J_{pn} = \frac{qn_i W_{pn}}{\tau_e}\left[\exp\left(\frac{qV_{pn}}{kT}\right)-1\right]$$

$$= \sqrt{\frac{2\varepsilon_s qn_i^2}{\tau_e^2}\left(\frac{N_A+N_D}{N_A N_D}\right)(V_{bi(pn)} - V_{pn} - 2kT/q)}\left[\exp\left(\frac{qV_{pn}}{kT}\right)-1\right] \tag{3.47}$$

$$= \frac{\beta}{\tau_e}\sqrt{(V_{bi(pn)} - V_{pn} - 2kT/q)}\left[\exp\left(\frac{qV_{pn}}{kT}\right)-1\right]$$

$$V_{SCR} = \frac{kT}{q}\ln\left[\frac{\beta}{\vartheta\tau_e}\sqrt{(V_{bi(pn)} - V_{pn} - 2kT/q)}\left[\exp\left(\frac{qV_{pn}}{kT}\right)-1\right]\right] \tag{3.48}$$

The constants ϑ and β are equal to $3.44\text{x}10^{-10}$ and $1.56\text{x}10^{-13}$ respectively, using $N_A=5\text{x}10^{15}\text{cm}^{-3}$, $N_D=7\text{x}10^{15}\text{cm}^{-3}$, and $A^{*}=30\text{A/cm}^2\text{K}^2$ [81]. Equation 3.48 can be substituted into equation 3.44 giving

$$\frac{kT}{q}\ln\left[\frac{\beta}{\vartheta\tau_e}\sqrt{(V_{bi(pn)} - V_{pn} - 2kT/q)}\left[\exp\left(\frac{qV_{pn}}{kT}\right)-1\right]\right] - V_{pn} = V_a - C + V_H - V_{bi(pn)} + V_{bi(SCR)} \tag{3.49}$$

which can now be used to solve for V_{pn} as a function of V_a. $V_{pn}=f(V_a)$ can then be substituted into equation 3.47 to calculate the expected cell current of as a function of the sample's bias with respect to the standard calomel electrode. In order to do so we first must evaluate the constants on the right hand side of equation 3.48.

$V_{bi(pn)}= 0.669\text{V}$ as calculated using equation 3.39 and N_A, N_D $=5\text{x}10^{15}\text{cm}^{-3}$ and $7\text{x}10^{15}\text{cm}^{-3}$ respectively, which are the doping densities of the epitaxial-layer test samples

used in this thesis. The flat-band potential for p-Si in an HF electrolyte has been measured as 0.3 to 0.4 (SCE) [33,57,69], and corresponds to the condition of $V_{SCR}=V_{bi(SCR)}$. Thus assuming that V_H is independent of V_a, we can evaluate C-V_H by substituting $V_a=V_{fb}\approx 0.35V$ and $V_{SCR}=V_{bi(SCR)}$ into equation 3.9 giving

$$C - V_H = V_{fb} \approx 0.35 \tag{3.50}$$

At equilibrium, $V_{pn} = 0$ and $V_{SCR} = 0$ so that equation 3.42 can be rewritten as:

$$V_a = V_{bi(pn)} - V_{bi(scr)} + C - V_H \quad \text{(at equilibrium)} \tag{3.51}$$

$V_{bi(scr)}$ can be calculated from the p-Si zero current potential (V_{zcp}) equal to -0.4 (SCE) [63,76, and the author's data in chapter 5], which corresponds to $V_{SCR}\approx 0$ assuming that only negligible cathodic currents are present. Thus we can evaluate $V_{bi(SCR)}$ by substituting $V_a=V_{zcp}=-0.4V$ and $V_{SCR}=0$ into equation 3.9 giving

$$V_{bi(scr)} = -V_{zcp} + C - V_H = 0.4 + 0.35 = 0.75 \tag{3.52}$$

Figures 3.5 (a) and (b) shows the potential that drops across the p-n junction and Schottky barrier space charge regions respectively. Except for ≈0.1V virtually all of the overall potential drop falls across the reverse biased p-n junction at anodic sample biases, and virtually all of the potential drops across the reverse biased Schottky barrier at cathodic biases. Figure 3.6 shows the calculated cell current as a function of V_a, showing the characteristic $(V)^{1/2}$ dependence of a reverse biased p-n junction for which minority carrier generation in the depletion zone dominates over the ideal p-n junction diffusion current.

3.3.2 n-Layer on p-Substrate

The energy band diagram for an n-layer on p-substrate sample is shown in figure 3.7. When such a sample is anodically biased the p-n junction becomes forward biased and the Schottky barrier is reverse biased. As a result holes can be injected by the forward biased p-n junction into the n-layer providing a high non-equilibrium minority hole concentration in the absence of illumination. These holes can then diffuse to the SCR where they are swept to the interface, resulting in n-layer etching.

The hole injection rate is determined by the p-n junction forward bias, which is the fraction of the potential drop across the silicon-electrolyte interface (V_{sei}) that falls across the p-n junction. The p-n junction forward bias must satisfy both the hole and electron current equations which, assuming ideal p-n junction behavior, are given by:

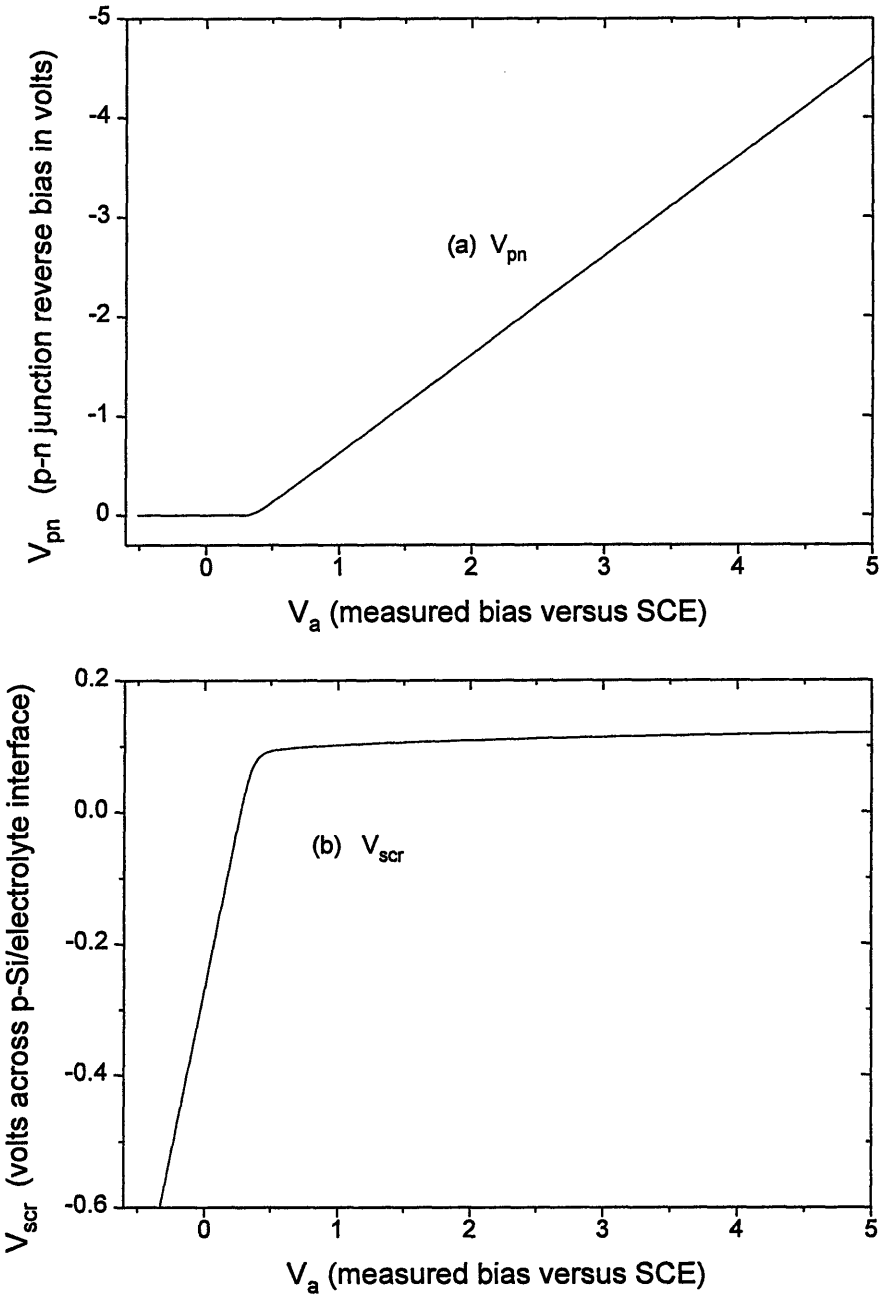

Figure 3.5. Plots of the calculated distribution of applied potential between the p-n junction (V_{pn}) and the silicon-electrolyte interface (V_{scr}) versus cell potential (V_a) for a p-layer on n-substrate sample.

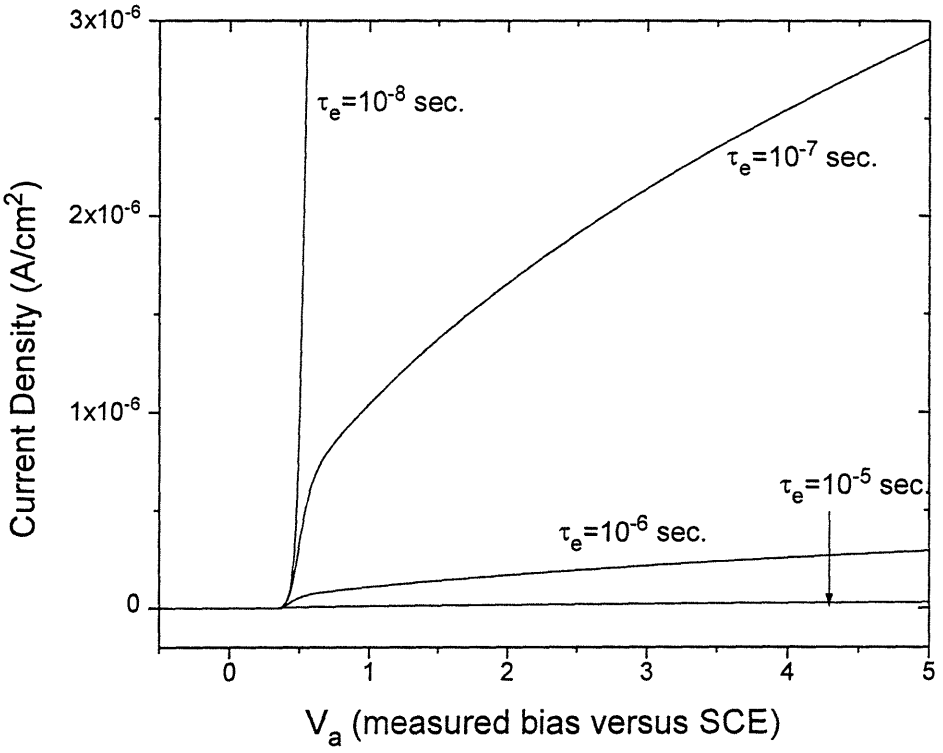

Figure 3.6. Graph of the calculated anodic current through a p-layer on n-substrate sample as a function of V_a applied to the substrate at various values of the effective minority carrier lifetime τ_e .

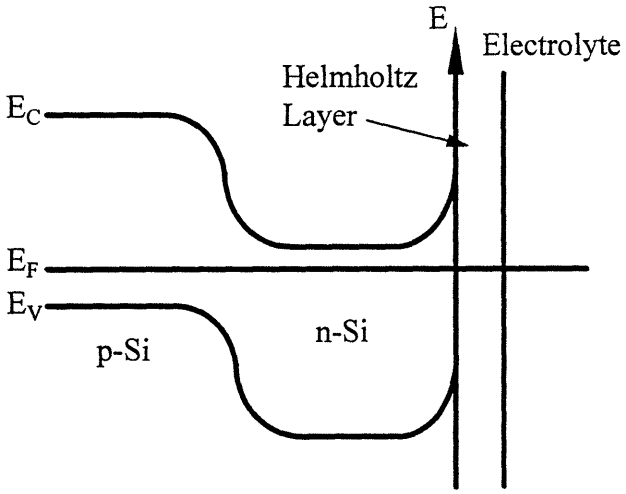

Figure 3.7. Energy band diagram for a n-layer on p-substrate sample.

$$J_{h^+} = \frac{qD_p n_{po}}{L_p}\left[\exp\left(\frac{qV_{pn}}{kT}\right) - 1\right] \tag{3.53}$$

$$J_{e^-} = \frac{qD_n p_{no}}{L_n}\left[\exp\left(\frac{qV_{pn}}{kT}\right) - 1\right] \tag{3.54}$$

Equation 3.54 reveals that for any given p-n junction forward bias there must be a corresponding electron current from the n-layer to the p-substrate. This electron current must be supported by an electron source, either by generation within the n-layer or by electron injection from the electrolyte.

While the anodically biased silicon-HF electrolyte interface is a good sink for holes via the dissolution reaction, it is a poor source of electrons. The dissolution reaction is irreversible, and even if some other cathodic proceeds simultaneously which liberates electrons it quickly becomes negligible with increasing anodic potential. Thus the silicon-electrolyte interface effectively behaves as a hole-pass, electron-block filter which limits the p-n junction forward bias and consequently limits the hole injection rate according to equation 3.53.

Several n-layer sources for electrons can be identified, however each provides only small electron currents: 1) electrons can be thermally generated, 2) they can be generated by field enhanced breakdown at pore tips, 3) they can be injected into the n-Si conduction band by photo-current doubling and quadrupling as explained in section 2.1.2.1, and 4) Searson and Zhang [57] propose that surface valence electrons can tunnel into the n-Si conduction band which they attribute as the source of the $\approx 10^{-5}$A/cm^2 anodic current observed at non-illuminated bulk n-Si electrodes.

We will present data in chapter five which is consistent with the premise of a p-n junction forward bias limited by electron generation. Furthermore the data indicates that the primary electron sources are injection from the silicon-electrolyte interface and field enhanced generation at pore tips.

3.3.3 The p-n-p Multilayer

The distribution of potential through a p-n-p multilayer sample is similar to that of a p-layer on n-substrate sample, in that most of the potential across the silicon-electrolyte interface drops across a reverse biased p-n junction. In the p-n-p sample, however, part of the potential also drops across the extra p-n junction which is forward biased. The energy band and potential distribution diagrams of the p-n-p multi-layer sample is shown in figure 3.8.

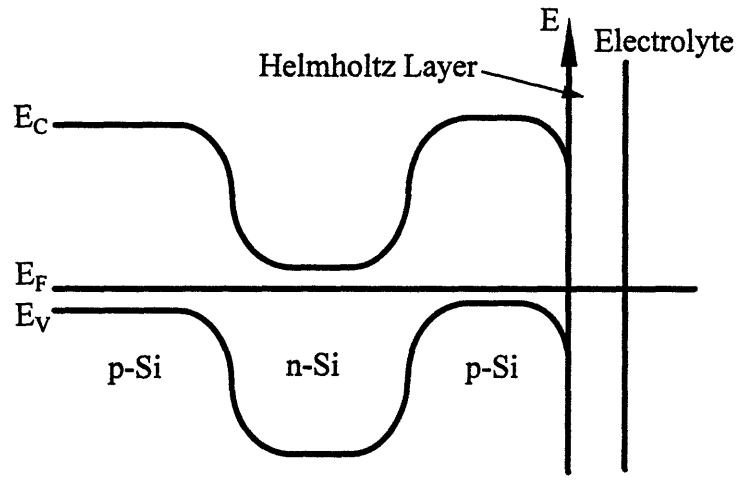

Figure 3.8. Energy band diagram for a p-n-p multi-layer sample.

The potential distribution equation for the p-n-p sample can be written as:

$$V_{sei} = C - V_a = -\Psi_{pn(r)} + \Psi_{pn(f)} + \Psi_s + V_H \tag{3.55}$$

and therefore: $$V_{SCR} + V_{pn(f)} - V_{pn(r)} = V_a - C - V_{bi(pnr)} + V_{bi(pnf)} + V_{bi(scr)} + V_H \tag{3.56}$$

Again assuming that that hole recombination is negligible, and that the p-n junction and silicon-electrolyte interface interfaces are equal the current densities can be equated as

$$J_{cell} = J_{SCR} = -J_{pn(r)} = J_{pn(f)} \tag{3.57}$$

The equation $J_{SCR} = -J_{pn(r)}$ was solved in section 3.3.1 giving:

$$V_{SCR} = \frac{kT}{q}\ln\left[\frac{\beta}{\vartheta\tau_e}\sqrt{(V_{bi(pn)} - V_{pn} - 2kT/q)}\left[\exp\left(\frac{qV_{pn}}{kT}\right) - 1\right]\right] \tag{3.58}$$

The equation $-J_{pn(r)} = J_{pn(f)}$ can be solved using equation 3.35 giving

$$V_{pn(f)} = \frac{2kT}{q}\ln\left[-\sqrt{\frac{V_{bi(pn)} - V_{pn(r)} - 2kT/q}{V_{bi(pn)} - V_{pn(f)} - 2kT/q}}\left[\exp\left(\frac{qV_{pn(f)}}{2kT}\right) - 1\right] + 1\right] \tag{3.59}$$

Equations 3.58 and 3.59 can be substituted into equation 3.56 giving

$$\frac{kT}{q}\ln\left[\frac{\beta}{\vartheta\tau_e}\sqrt{(V_{bi(pn)}-V_{pn}-2kT/q)}\left[\exp\left(\frac{qV_{pn}}{kT}\right)-1\right]\right]$$
$$+\frac{2kT}{q}\ln\left[-\sqrt{\frac{V_{bi(pn)}-V_{pn(r)}-2kT/q}{V_{bi(pn)}-V_{pn(f)}-2kT/q}}\left[\exp\left(\frac{qV_{pn(f)}}{2kT}\right)-1\right]+1\right]-V_{pn} \qquad (3.60)$$
$$= V_a - C + V_H - V_{bi(pn)} + V_{bi(pn)} + V_{bi(SCR)}$$

where the constants on the right hand side of the equation can be evaluated in a similar manner as for the p-layer on n-substrate sample giving +0.4V. This equation is considerably more difficult to solve because $V_{pn(f)}$ could not be completely isolated in equation 3.57 and thus appears in equation 3.60. $V_{pn(f)}$ was determined by solving equation 3.59 using iteration by re-calculating $V_{pn(f)}$ using the previous result until convergence.

Figures 3.9 and 3.10 show the potential drops across the two p-n junctions and the silicon-electrolyte interface, as well as the resulting cell current as a function of cell potential (V_a) for various values of the effective minority carrier lifetime τ_e. Again we see that most of the applied potential falls across the reverse biased p-n junction under anodic bias, and across the Schottky barrier under cathodic bias. Furthermore, decreasing minority carrier lifetime which results in increased generation current in the reverse biased p-n junction results in a higher potential drop across the Schottky barrier consistent with the increase in cell current.

3.3.4 Illuminated p-Layer on p-Substrate

When illuminated, the reverse biased p-n junction current voltage characteristics are dominated by the photo-current J_L as given by equation 3.40 and plotted in figure 3.11. In addition, illumination induces a photo-bias which drives the p-layer anodic with respect to the n-substrate, resulting in a shift in the p-Si etching onset potential cathodically with respect to the potential V_a applied to the n-substrate.

Equation 3.42 can be rewritten for the illuminated p-layer on n-substrate case giving

$$V_{SCR} - V_{pnIL} = V_a - C + V_H - V_{bi(pn)} + V_{bi(scr)} \qquad (3.61)$$

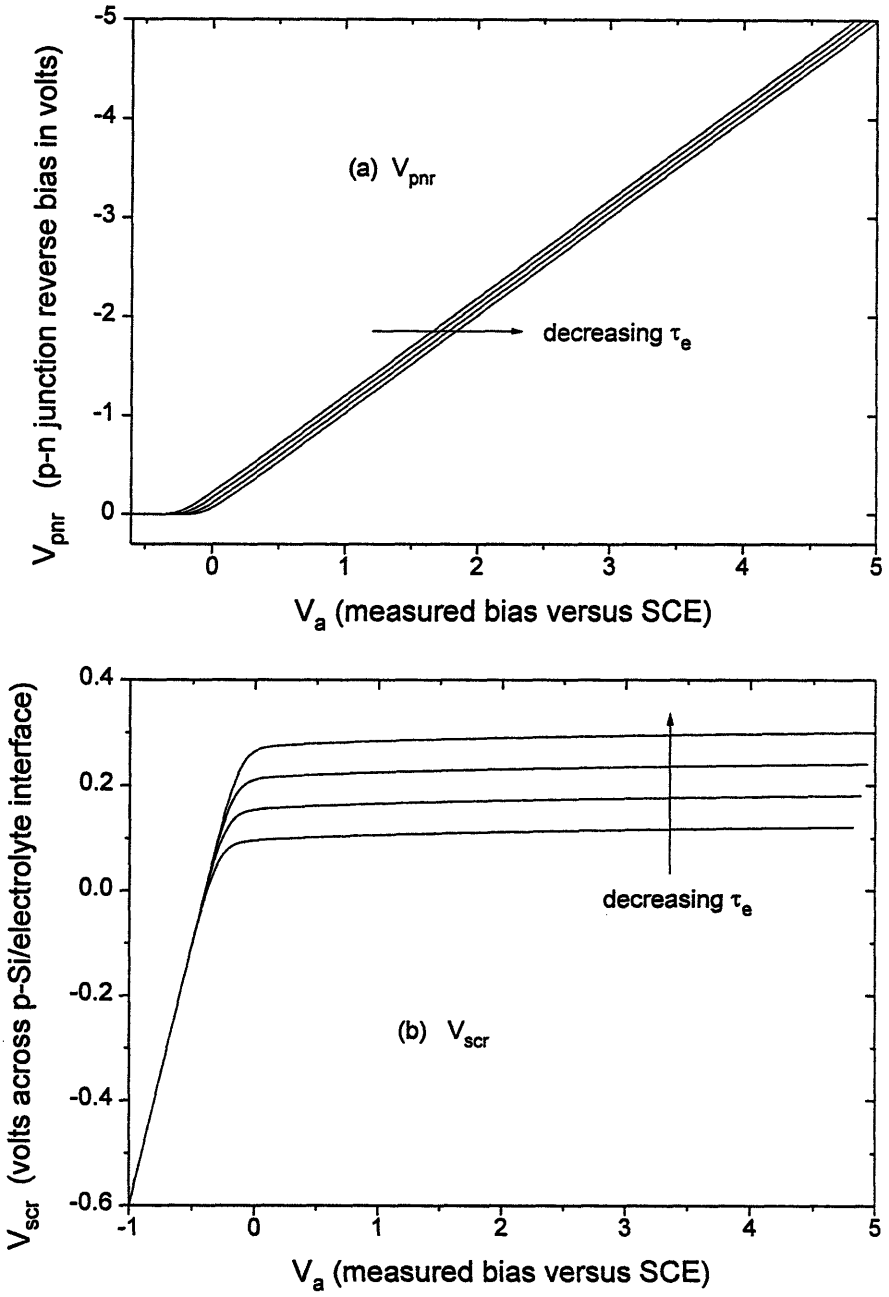

Figure 3.9. Plots of the calculated distribution of applied potential between the reverse biased p-n junction ($V_{pn(r)}$) and the silicon-electrolyte interface (V_{scr}) versus cell potential (V_a) for a p-n-p multilayer sample at various values of the effective minority carrier lifetime τ_e.

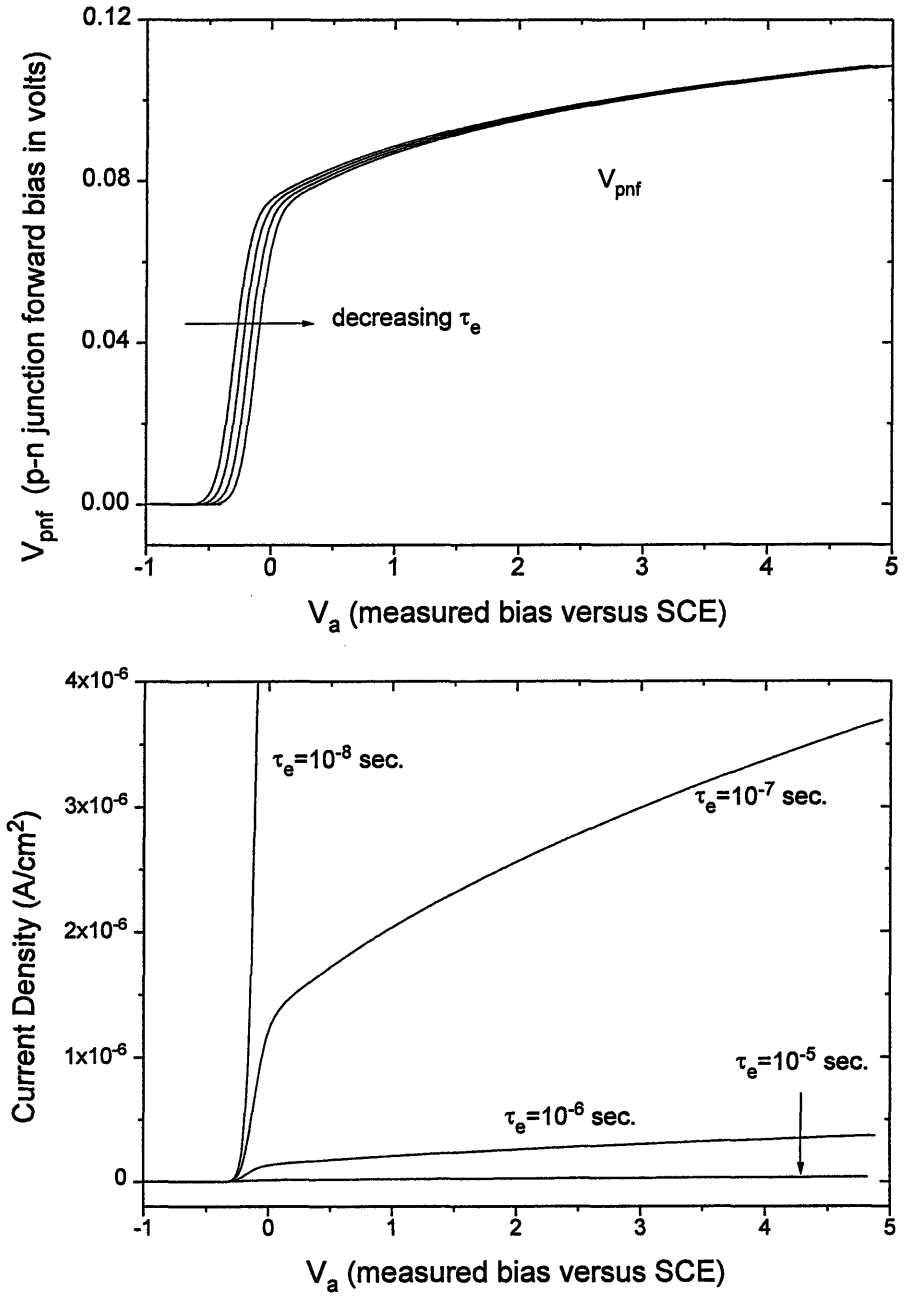

Figure 3.10. Plots of the calculated distribution of applied potential between the forward biased p-n junction ($V_{pn(f)}$) and the calculated anodic current through a p-n-p multilayer sample as a function of V_a, at various values of the effective minority carrier lifetime τ_e.

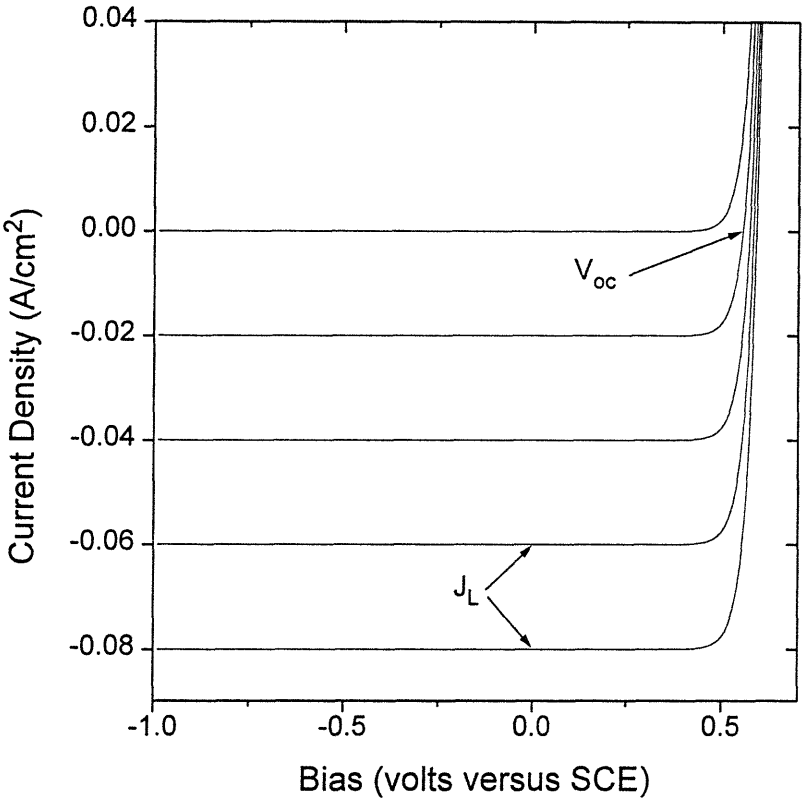

Figure 3.11. Illuminated p-n junction current-voltage characteristics calculated using equation 3.40, where $J_{S = 1x10^{-11}}$ A/cm^2 and J_L = 0.02, 0.04, 0.06, and 0.08 A/cm^2.

Assuming that the hole recombination is negligible and that the p-n junction and silicon-electrolyte interface interfaces are equal, the current densities can be equated as

$$J_{cell} = J_{SCR} = - J_{pn(IL)} \tag{3.62}$$

$J_{SCR} = - J_{pn(IL)}$ can be solved for V_{SCR} using equations 3.46 and 3.40 (assuming ideal p-n junction current-voltage characteristics), giving

$$V_{SCR} = \frac{kT}{q} \ln\left[-\frac{J_S}{\vartheta} \exp\left(\frac{qV_{pnIL}}{kT} \right) + \frac{J_S}{\vartheta} + \frac{J_L}{\vartheta} \right] \tag{3.63}$$

After substituting equation 3.63 into equation 3.61 we obtain

$$\frac{kT}{q}\ln\left[-\frac{J_S}{\vartheta}\exp\left(\frac{qV_{pnIL}}{kT}\right)+\frac{J_S}{\vartheta}+\frac{J_L}{\vartheta}\right]-V_{pnIL}=V_a-C-V_H-V_{bi(pn)}+V_{bi(SCR)} \qquad (3.64)$$

which can again be used to solve for V_{pnIL} as a function of V_a, and then for the cell current.

Figures 3.12 (a) and (b) show the potential drops across the illuminated p-n junction and Schottky barrier space charge regions respectively. Again most of the potential falls across the reverse biased p-n junction, however a greater potential drop is observed across the Schottky barrier than for non-illuminated p-on-n samples consistent with the higher anodic current passing through the silicon-electrolyte interface. Figure 3.13 (a) shows that for any given V_a, the photo-bias increases with illumination intensity driving the p-layer more anodic and thereby increasing V_{SCR}.

Figure 3.13 shows the calculated cell current for the illuminated p-layer on n-substrate sample. When compared to the current-voltage characteristics of non-illuminated samples (figure 3.6 -note the difference in y-axis scale) we see the expected cathodic shift of $\approx$0.5V in the p-Si etching onset potential due to the photo-biasing effect. The current then increases to illumination intensity limited plateaus similar to the etching characteristics of n-Si.

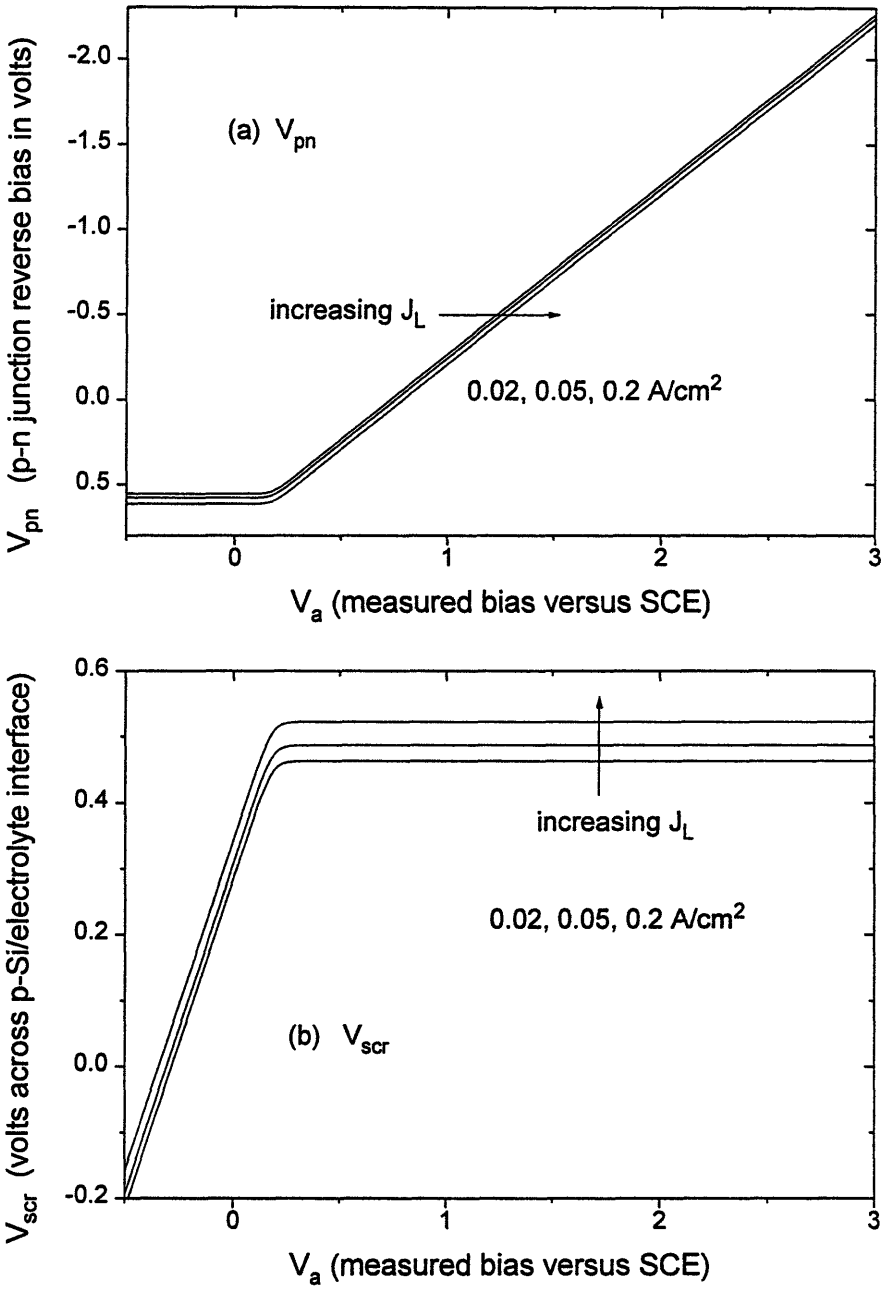

Figure 3.12. Plots of the calculated distribution of applied potential between the p-n junction (V_{pnIL}) and the silicon-electrolyte interface (V_{scr}) versus the cell potential (V_a) for three different illumination intensities.

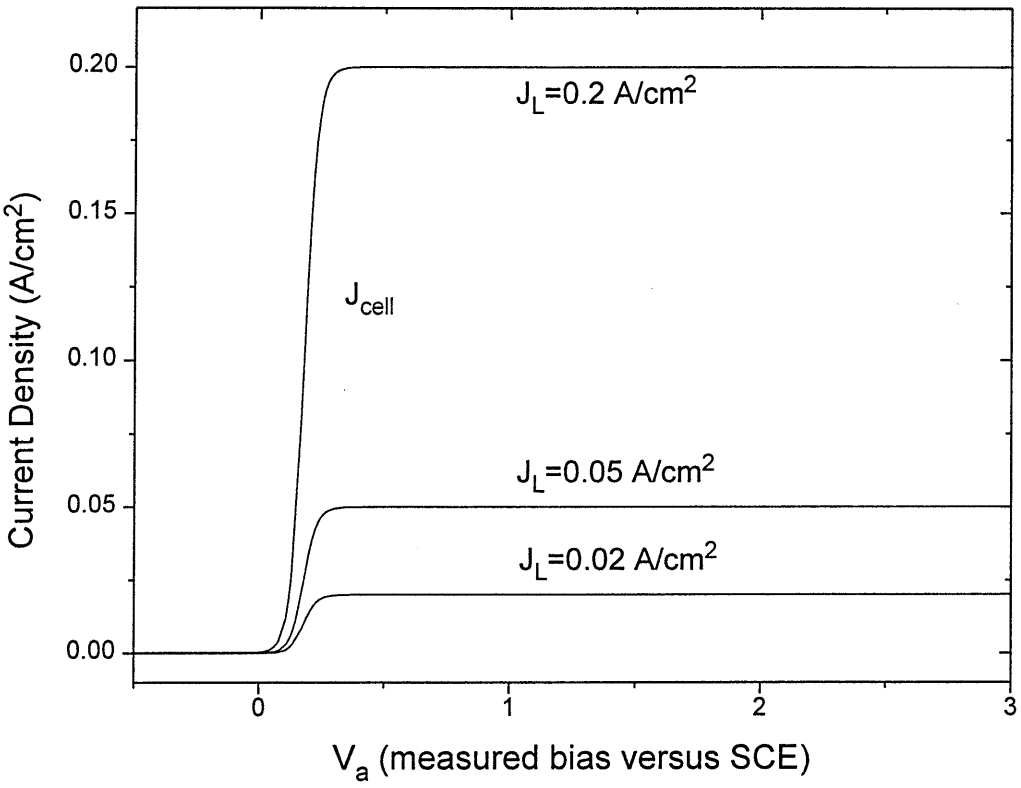

Figure 3.13. Graph of the calculated anodic current through an illuminated p-layer on n-substrate sample as a function of bias applied to the n-substrate for three different illumination intensities.

Chapter 4

Experimental

This chapter discusses the experimental procedures used for investigating anodic silicon micromachining in HF electrolytes. Sample preparation, the electrochemical etching apparatus, etching procedures, and data acquisition equipment and techniques are included.

4.1 Sample Preparation

Anodic etching experiments were made on four distinct groups of samples: a) bulk n- and p-type silicon, b) epi-layer samples with one or more uniform and continuous epitaxial n- or p-Si layers, c) cantilever beam test samples formed by dopant implantation or diffusion through oxide masks, and d) n-Si samples with patterned metal mask layers for etching of high aspect ratio structures.

Once fabricated, the samples were diced using a MicroAutomation 1006 diamond saw to form 0.5 by 1.0 cm rectangles (except for some bulk-Si samples which were instead scribed and cleaved to approximately the same size) for mounting into the cell sample holder.

4.1.1 Epi-Layer Samples

Epi-layer samples with five different doping profiles on (100) wafers were obtained from two sources[1,2]. Layer thickness', doping densities, and substrate doping densities were verified using spreading resistance analysis[3] and are summarized in table 4.1.

---

1 Lawrence Semiconductor Laboratories Inc., Tempe, Arizona

2 M/A-Com Semiconductor

3 Solecon Laboratories, Inc., San Jose, CA

NAME	SOURCE	SUBSTRATE		LAYER 1			LAYER 2		
		type	cm^{-3}	type	cm^{-3}	μm	type	cm^{-3}	μm
epi(p/n)	L.S.	n	$2x10^{15}$	p	$5x10^{15}$	2.25			
epi(n/p/n)	L.S.	n	$2x10^{15}$	p	$5x10^{15}$	2.25	n	$7x10^{15}$	0.75
epi(n/p)	L.S.	p	$2x10^{15}$	n	$7x10^{15}$	2.25			
epi(p/n/p)	L.S.	p	$2x10^{15}$	n	$7x10^{15}$	2.25	p	$5x10^{15}$	0.75
epi(n/p^+)	M/A-COM	p^+	$6x10^{19}$	n	$1x10^{15}$	9.5			

Table 4.1. Doping profiles of epi-layer samples. The notation n/p/n refers to an n-layer on a p-layer on an n-substrate.

NAME	SUBSTRATE		PROCESSING CONDITIONS				
	type	cm^{-3}	implanted atom	implant dose cm^{-2}	energy keV	anneal time min.	anneal temp. °C
cb^{imp}(n/p)	p	$2x10^{15}$	P	$1x10^{13}$	250	45	1100
cb^{imp}(p/n/p)	p	$2x10^{15}$	P	$1x10^{13}$	250	45	1000
			B	$3x10^{12}$	50	45	1000

Table 4.2. Implantation and anneal processing conditions for implanted cantilever beam samples. The notation n/p refers to an n-Si cantilever beam on a p-Si substrate.

NAME	SUBSTRATE		PROCESSING CONDITIONS			
	type	cm^{-3}	diffused atom	diffusion time	diffusion temp. °C	p-n junction depth μm
cb^{diff}(p/n)	n	$2.4x10^{15}$	B	2.5 hr.	1050	2.8
cb^{diff}(n/p1)	p	$2x10^{15}$	P	90 min.	1100	1.7
cb^{diff}(n/p2)	p	$2x10^{15}$	P	?	?	4.9
cb^{diff}(p-well)	n	$3x10^{15}$	B	14 hr.	1150	2.65
			P	90 min.	1100	1.1

Table 4.3. Diffusion process conditions for indiffused cantilever beam samples. The notation n/p refers to an n-Si cantilever beam on a p-Si substrate.

4.1.2 *Cantilever Beam Test Samples*

Cantilever beam test samples having a variety of doping profiles were prepared by first growing and patterning an oxide mask (Fig. 4.1a) onto either n- or p-type $\approx 10^{15}$ cm^{-3} (100) Si substrates, followed by indiffusion or implantation of boron or phosphorous. Both n-Si cantilever beams on p-Si substrates (Fig. 4.1b) and p-Si cantilever beams on n-Si substrates (Fig. 4.1c) were formed. 'Multi-layer p/n/p' cantilever beam test samples consisting or n-type cantilever beams capped with a thin p-Si layer (Fig. 4.1e) were prepared by first implanting phosphorous and then boron into masked p-Si substrates. 'p-well' cantilever beam test samples were prepared by first forming an oxide mask with a ≈1x1mm opening and indiffusing boron to form a p-Si well in an n-Si substrate, followed by indiffusing phosphorous through the mask shown in figure 4.1a to form n-Si cantilever beams positioned over the well. (Fig. 4.1f).

Beam widths were 180μm for the 'solid' beams and 50μm for the arms of the 'hollow' beams. Beam lengths were approximately 650μm but varied somewhat between sample types.

Formation of oxide masks and indiffusions were performed at Draper Laboratories[4]. Implantations and subsequent anneals were performed at MIT, using an AI Accelerators Inc. implanter and an Omega 1 three zone control furnace with 4 inch diameter quartz tube with a 3L/min O_2 gas flow. Processing conditions are summarized in Tables 4.2 and 4.3 for implanted and indiffused cantilever beam samples respectively. The resulting dopant profiles are shown in figure 4.2.

4.1.3 *n-Si samples with patterned metal mask layers*

Etching of high aspect ratio structures was attempted by spatially blocking incident illumination using patterned metal masks on n-Si substrates. The samples were fabricated at Draper Laboratories by sputter depositing metal layers and patterning using a mask consisting of a variety of geometrical features including comb-drives, rectangles, and fine lines, with feature sizes ranging from 2μm to over 50μm. Three types of masked samples were made using $\approx 2x10^{15} cm^{-3}$ phosphorous doped (100) n-Si wafers and the following metal layers: 1) 0.1μm TiW, 2) 0.04 μm Ti (for adhesion) and 0.07 μm Pt, and 3) 0.04μm Cr (for adhesion) and 0.07μm Au.

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4 Charles Stark Draper Laboratories, Cambridge, MA

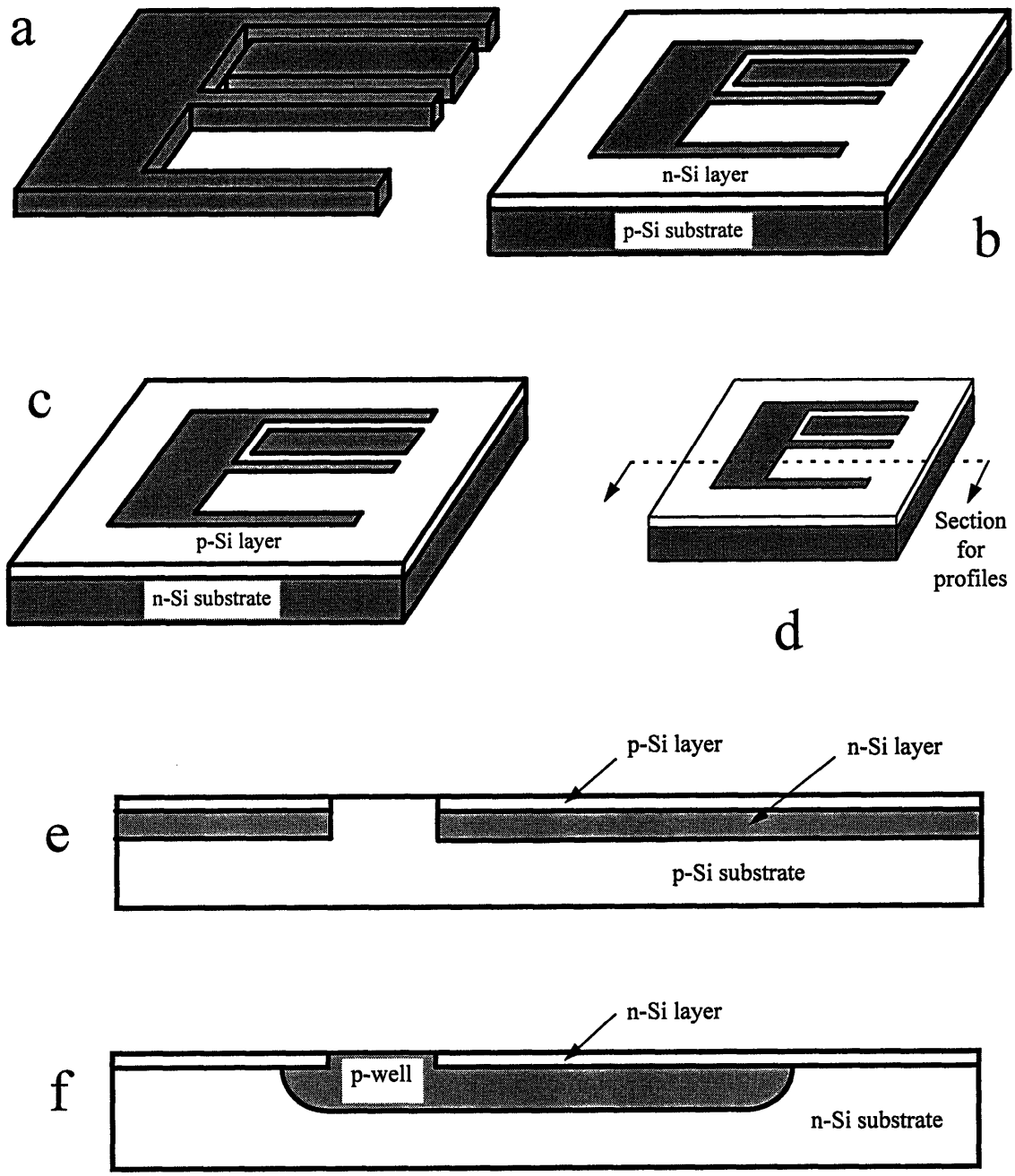

Figure 4.1. Schematic diagrams of a) the oxide mask geometry used for implantation or indiffusion of cantilever beam samples, b) n-Si cantilever beam on p-Si substrate samples, c) p-Si cantilever beam on n-Si substrate samples, and cross-sections of e) p/n/p and f) p-well cantilever beam samples.

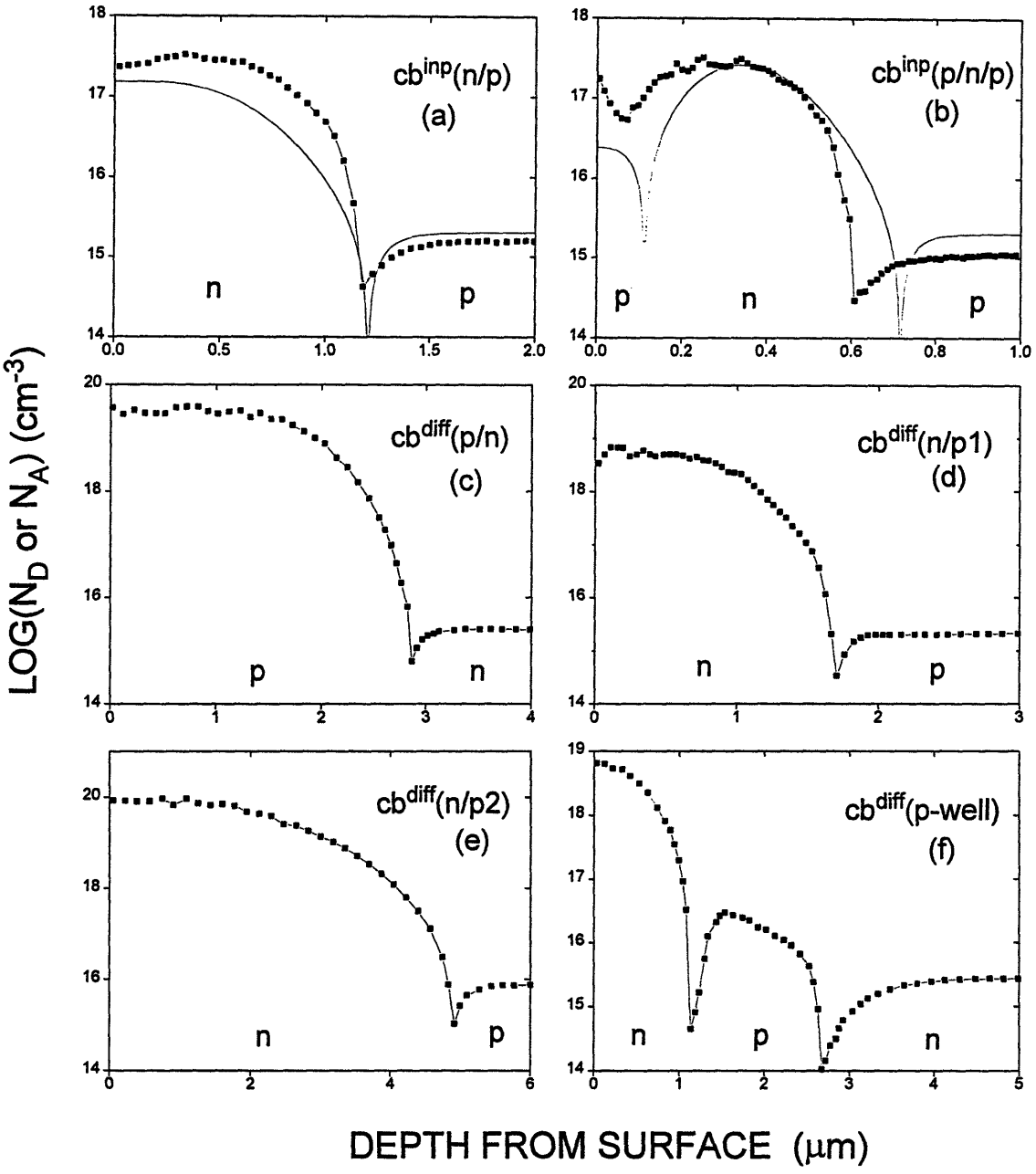

Figure 4.2. Doping profiles of implanting or indiffused cantilever beam samples as a function of depth from the surface. Points represent spreading resistance analysis data measured by Solecon Laboratories, San Jose, CA. Solid curves shown for implanted samples represent calculated dopant distributions based on the implantation energy and dose, and anneal time and temperature. Calculation details are presented in appendix A1.

4.1.4 Sample Cleaning and Ohmic contacts

Prior to etching, samples were sequentially cleaned for at least 20 seconds in TCA to dissolve organic contaminants, acetone to dissolve TCA, and methanol to dissolve acetone, then dipped in 5% HF to strip the native oxide, and rinsed in DI water. All solvents were electronics grade and at room temperature. This cleaning process was considered sufficient because the silicon surface is continuously renewed during dissolution.

Ohmic contacts to the backsides of indiffused cantilever beam samples and n-Si samples with patterned metal masks were made at Draper Laboratories. Heavily doped surface layers were first applied to the wafer backsides prior to other processing steps using a spin-on diffusion of phosphorous or boron glass for n-Si or p-Si substrates respectively. 0.1μm titanium-tungsten alloy and 0.2μm gold layers were sputtered onto the wafer backsides after wafer processing was completed.

Ohmic contacts to the other samples were made by applying liquid gallium directly onto the silicon surface after cleaning the surface and removing the native oxide. Good ohmic contacts to the backsides of n-Si substrates were achieved only after scratching the gallium-silicon interface with a scriber.

In some instances it was necessary to apply an ohmic contact to the sample front surface to either independently bias specific n-or p-type regions, compensate for photo-generated biases, or measure how the applied cell bias is distributed between buried p-n junctions and the silicon-electrolyte interface. Ohmic contacts to front-side surface layers were formed by applying gallium onto the cleaned and HF dipped surface and attaching a platinum lead with epoxy for mechanical support and electrical isolation.

4.2 Etching Apparatus

A schematic of the apparatus used for silicon anodic etching is shown in figure 4.3. The apparatus consists of an electrochemical cell which serves to contain the HF electrolyte and define the silicon-electrolyte interface, illumination and electrolyte circulation systems, and a computer controlled potentiostat to apply the etching bias.

4.2.1 The Electrochemical Cell

A schematic of the electrochemical cell is shown in figure 4.4. The cell was based on a design developed by Dan Gealy[5], and was constructed entirely from Teflon

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5 Dan Gealy, Ph.D. thesis, Massachusetts Institute of Technology, June 1989.

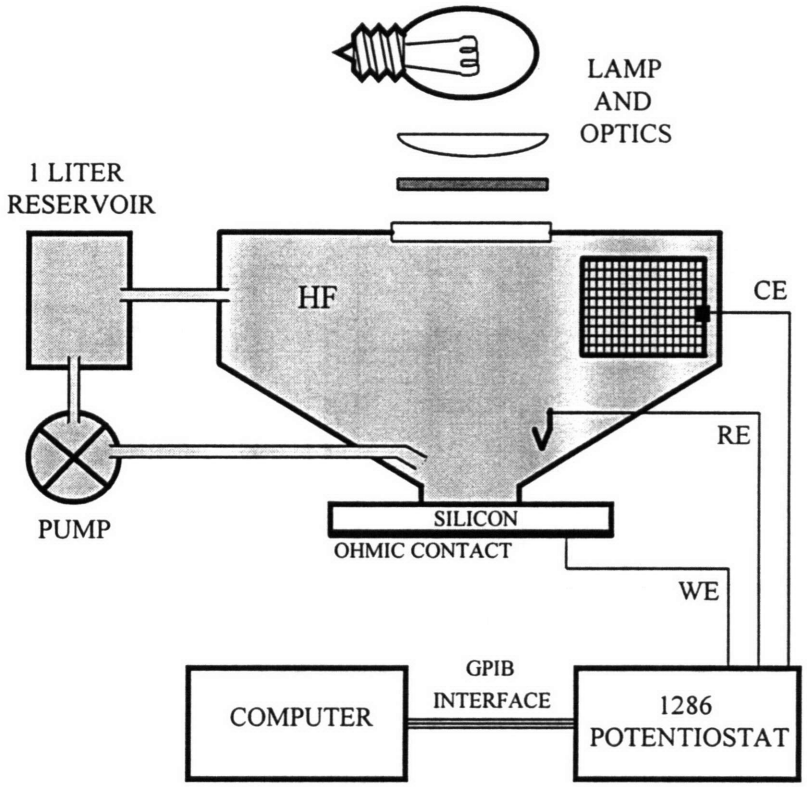

Figure 4.3. Schematic diagram of the experimental apparatus used to anodically etch silicon in HF electrolytes.

and polyethylene due to the corrosive nature of aqueous HF. 1/2 or 3/8 inch thick Teflon sheet was machined to form the cell bottom, cell sides, teflon seal holder, window holder, etc., and then assembled using a CHEMGRIP[6] Teflon etching and bonding kit. Teflon pieces were first masked with tape to expose only the bonding surfaces and then immersed into the etching agent to strip fluorine atoms from the surface using an active form of sodium in solution, making the surface receptive to adhesive bonding. The etching agent (composed of sodium, naphthalene, diethylene glycol and dimethyl ether) quickly becomes inactive by reacting with moisture in the atmosphere or water adsorbed on the Teflon surface. It was therefore necessary to drive off adsorbed water by heating the Teflon pieces to above 100°C and etch in a dry box.

The CHEMGRIP bonding epoxy, like all other adhesives tested, is unstable in aqueous HF. In order to obtain a stable bond and prevent contamination of the electrolyte, the Teflon pieces were machined to within 2mil tolerance and bonded under

6 Norton Co., Performance Plastics, Wayne, NJ

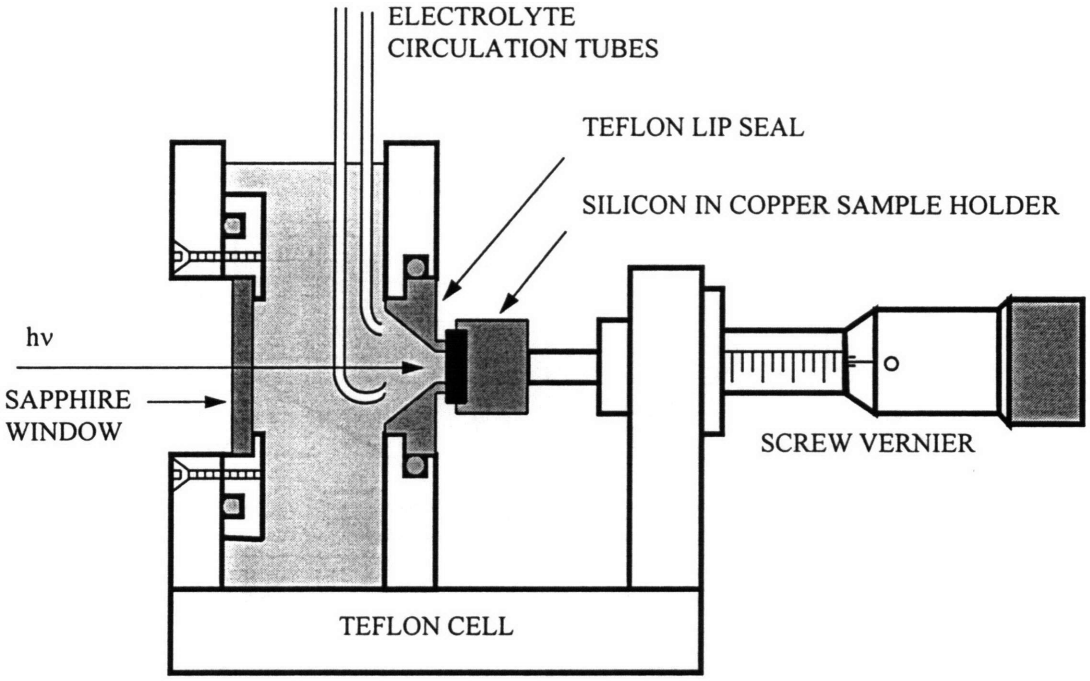

Figure 4.4. Schematic diagram of the electrochemical cell.

pressure to drive all excess epoxy from the joint space. As a result, the HF electrolyte was repelled from the epoxy in the ≈2mil bond space by the hydrophobic Teflon surfaces. It was later found that Dow Corning #730 Fluorosilicone is significantly more (although not totally) resistive to HF, and may be a more suitable adhesive.

The silicon-electrolyte interface area is defined by a circular Teflon lip against which samples are pressed using a micrometer screw vernier mounted to the cell, which allows for convenient exchange of samples. The silicon-electrolyte interface seal is machined onto a removable Teflon insert to allow periodic replacement of the easily damaged soft Teflon lip. Silicon samples are attached to the vernier plunger using a machined copper holder with a rectangular recess in which samples are placed. Viscous Dow Corning high vacuum silicone grease is dabbed at the four corners of the samples to hold them in place.

The counter electrode consists of a 3x5cm 10mil platinum mesh and is held in place by melting the mesh edge into a thermo-plastic polyethylene frame. A polymer-body Calomel reference electrode (Fisher Scientific Cat # 13-620-258) is immersed directly in the electrolyte with the tip approximately 15mm from the silicon-electrolyte interface. No attempt was made to seal the cell from the environment.

4.2.2 *The Illumination System*

The cell design incorporates a 25mm diameter sapphire window to allow sample illumination through an optically flat surface, rather than through a liquid-air interface which is an easily perturbed by cell vibrations, electrolyte flow, or bubbles.

White light illumination is provided by a 1kW Oriel Quartz Tungsten Halogen lamp with an F/0.7 Aspherab borosilicate crown condenser and an Oriel 41960 secondary focusing lens. Control of illumination wavelength is achieved by installing colored-glass filters into a black Delrin holder mounted between the secondary lens and sapphire window. An IR filter consisting of a quartz container and 1.9cm of DI water is placed between the condenser and secondary lens to both reduce electrolyte heating and protect the colored-glass filters.

Desired illumination intensities are reproducibly obtained by controlling lamp current using a Sorensen DCR300-9B DC power supply. The current was controlled to within 0.5% by measuring the voltage drop across a 0.2036±0.001Ω shunt resistor, consisting of five 1Ω, 10W resistors connected in parallel. The shunt resistance was calculated from the slope of a current-voltage sweep generated by the 1286 after compensating for lead resistance, and is stable to within 0.5% with respect to ohmic heating upon passing 8.0 amps DC current.

Reported illumination intensities (mW/cm^2) were calculated by integrating the illumination spectral irradience from 310nm (borosilicate glass absorption cut-off) to 1107nm (silicon band-gap), without correcting for the differences in reflection of the silicon-electrolyte interface and photodiode. Spectral irradience was measured with an Oriel 7183 silicon photodiode and KRATOS GM252 monochrometer after calibration with an Oriel 63350 calibrated lamp.

Calibration details and the relative spectral irradiences of the intensities of white and filtered light used in this thesis are presented in Appendix A2.

4.2.3 *The Electrolyte Flow System*

Electrolyte circulation serves to a) minimize mass transfer kinetic limitations of the dissolution reaction, b) remove bubbles evolved at the silicon-electrolyte interface, and c) minimize electrolyte composition variations over the duration of etching experiments by using a 1 liter electrolyte reservoir. The electrolyte is circulated using a Cole-Parmer Masterflex LX type pump, and flows from the 1 liter reservoir, through the pump, into the cell through two 1/8 inch inner-diameter tubes directed at the sample surface, and back to the reservoir. The pulsed flow generated by the pump is smoothed using a flow integrator (consisting of a rigid polyethylene container which encloses a $\approx 30cm^3$ air pocket over the electrolyte) installed between the pump and cell.

Experiments were typically performed using a 600mL/min flow rate. Some cantilever beam samples with very thin and hence fragile beams were etched using a

400mL/min flow rate to avoid breakage. The silicon dissolution current-voltage characteristics were found to be nearly identical when using 400 or 600mL/min flow rates, indicating that mass transfer kinetics at these rates are not limiting. Unfortunately, the flow rate over the whole surface is not constant, and some regions such as those near the seal edge experience lower flow than others. This is thought to cause some etch rate nonuniformity such as curvature seen on deep electropolished etch-pits. At lower flow rates, the dissolution current was observed to decrease and sometimes become irreproducible from sweep to sweep. This irreversibility is due to inefficient removal of bubbles formed at the silicon-electrolyte interface during dissolution, resulting in a variation in the effective interface area. Bubble trapping, as shown in figure 4.5, is exasperated by the recessed shape of the silicon-electrolyte interface seal, vertical silicon-electrolyte interface, and the hydrophobic nature of silicon and Teflon surfaces.

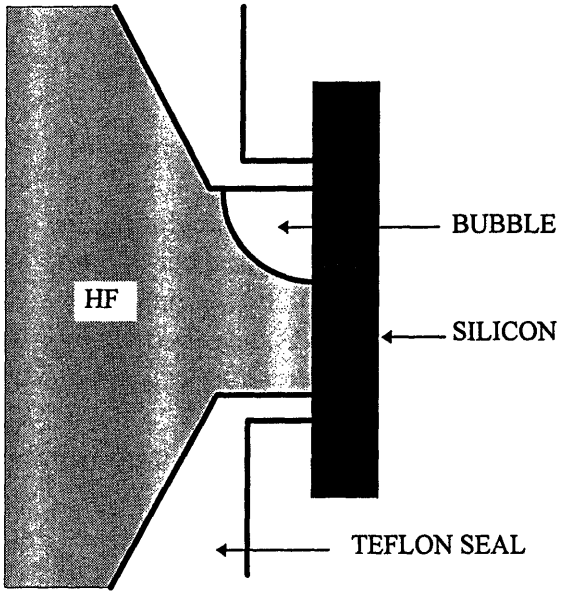

Figure 4.5. Schematic diagram of the vertical silicon-electrolyte interface and Teflon lip seal showing a trapped bubble which, unless removed, results in cell current irreproducibility and uneven etched surfaces.

4.2.4 HF Electrolyte

Aqueous HF electrolyte solutions having 1, 2.5, 5, 10, 15, and 20 weight percent HF concentrations were prepared by diluting 48% aqueous HF[7] with deionized water. No additional purification was attempted to remove the impurities present in the 48% HF solution, which are listed in Table 4.4. The electrolyte temperature was 20 ± 3°C for all experiments. The cell was not sealed and so electrolytes were exposed to the atmosphere.

7 Mallincrodt AR®

Electrolyte concentrations are reported in weight percent HF, consistent with similar studies in the literature. Calculations to determine the stoichiometric molality, pH, and molalities of F^-, H^+, and HF_2^- ions and undissociated HF in solution for the various weight percent concentrations used in this thesis are presented in appendix A3. The results are summarized in Table 4.5.

IMPURITY	CONC	IMPURITY	CONC
Assay HF	48.0-51.0%	Heavy metals (i.e. Pb)	< 0.5ppm
Arsenic	< 0.05 ppm	Iron	< 1ppm
Copper	< 1ppm	Phosphate (PO4)	< 1ppm
Chloride	< 5ppm	Residue after ignition	< 5ppm
Fluosilic Acid H_2SiF_6	< 0.01ppm	Sulfate and Sulfite (as SO_4)	< 5ppm

Table 4.4. Impurity concentrations present in 48% HF solutions.

Weight percent HF	C	pH	$[F^-]$	$[H^+]$	$[HF_2^-]$	[HF]
1	0.5051	1.5141	0.01391	0.03061	0.01671	0.4577
2.5	1.2821	1.1580	0.01718	0.06951	0.05233	1.1602
5	2.6316	0.8553	0.01931	0.13954	0.12023	2.3718
10	5.5556	0.5250	0.02122	0.29851	0.27729	4.9798
15	8.8235	0.3160	0.02228	0.48303	0.46075	7.8797
20	12.500	0.1574	0.02303	0.69594	0.67291	11.1312

Table 4.5. Stoichiometric molality (mol/kg H_2O), molalities of ionic species and undissociated HF in solution, and pH of the various weight percent HF electrolyte compositions at 25°C.

4.3 Etching Experiments and Data Acquisition

4.3.1 Etching Procedure and Data Acquisition

A typical etching procedure involved filling the reservoir with electrolyte, mounting a sample against the Teflon seal, filling the cell with electrolyte by raising the reservoir, starting the electrolyte circulation pump, connecting the Solatron 1286 potentiostat leads to the sample, platinum counter electrode and Calomel reference electrode (as shown in see figure 4.3), entering the experimental parameters into a

computer program which controls the experiment, and if necessary, setting the lamp current.

Experiments were controlled using software[8] running on a 486 66MHz personal computer. The programs would first prompt for experimental parameters, including 1) the silicon-electrolyte interface area, 2) etching parameters such as applied bias and etch time, and 3) data acquisition parameters such as the potentiostat current sense measuring resistor magnitude and on-screen plotting axes. The program would then 1) send appropriate commands to the potentiostat via a GPIB interface to start the experiment, 2) collect current, applied bias and etching time data from the potentiostat, 3) plot the data on the screen in real-time to permit monitoring, 4) integrate the current over time to calculate the coulombs passed through the cell, 5) shut down the potentiostat to electrically isolate the sample at the end of the experiment, and 6) save the data on disk in a format appropriate for exporting into graphing software.

4.3.2 Current-Voltage and Current-Time Experiments

The 1286 potentiostat was controlled to either collect current versus voltage (I-V) or current versus time I(t) data.

I-V characteristics were measured by running the 1286 in potentiostatic mode and sweeping the applied bias, usually from the more cathodic to more anodic bias and then back. Sweep rates were typically 20mV/sec for short sweeps (over approximately 1 or 2 volt range) and up to 100mV/sec when sweeping from ≈0 to ≈10 volts. I-V sweeps were measured while systematically varying other important parameters influencing silicon etch rates, including HF concentration, illumination intensity and wavelength, silicon doping density and crystallographic orientation, dopant type and doping profiles, and externally applied p-n junction potentials (see next section).

I(t) data were also measured with the 1286 in potentiostatic mode by fixing applied potential and measuring current over time. Experiments were run until the user input time had elapsed or until a specific number of coulombs were passed through the cell. I(t) data were systematically collected as a function of applied bias, HF concentration, and illumination intensity for the various bulk silicon and epi-layer samples. Etch rates were then determined by dividing the etch pit depths (measured using DEK TAK[9] profilometry) by the etching time.

The silicon dissolution valence, defined as number of elementary charges passed for each silicon atom removed, was calculated as shown in equation 4.1 using the etch depth and the number of coulombs passed during etching.

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8 Written by Dan Gealy and customized by the author.

9 Sloan DEK TAK 8000

$$DV = \frac{(\text{coulombs passed} / 1.9x10^{-19})(28.085)}{(\text{etch pit depth})(\text{area})(2.33)(6.02x10^{23})} \quad \text{holes/atom} \qquad (4.1)$$

where 28.085 g/mol is the molecular weight of silicon, *area* is the silicon-electrolyte interface area, and 2.33 g/cm^3 is the density of silicon.

4.3.3 Experiments Using Two 1286 Potentiostats

In some experiments, 2 potentiostats were simultaneously controlled by the computer programs to apply the cell bias with the first potentiostat (1286#1), and either 1) independently bias specific n-or p-type regions, 2) compensate for photo-generated biases, or 3) measure how the applied cell bias is distributed between p-n junctions and silicon-electrolyte interface with the second potentiostat (1286#2). 1286#2 was powered through an isolation transformer to isolate it from ground and connected between the back-side and front-side ohmic contacts as shown in figure 4.6, with the RE1 + CE and RE2 + WE leads shorted together.

When compensating for photo-generated biases or independently biasing n-Si and p-Si regions, 1286#2 was operated in potentiostatic mode to bias the buried p-n junction and thus behave as an ideal current source or sink. While it was possible to use a battery in place of 1286#2, this presented difficulties in accurately setting the junction bias and monitoring the junction current.

When measuring the distribution of the 1286#1 bias between the silicon-electrolyte interface and buried p-n junction, , 1286#2 was operated in standby mode. This allowed the potential between RE1 and RE2 to float, and 1286#2 thus behaved as a

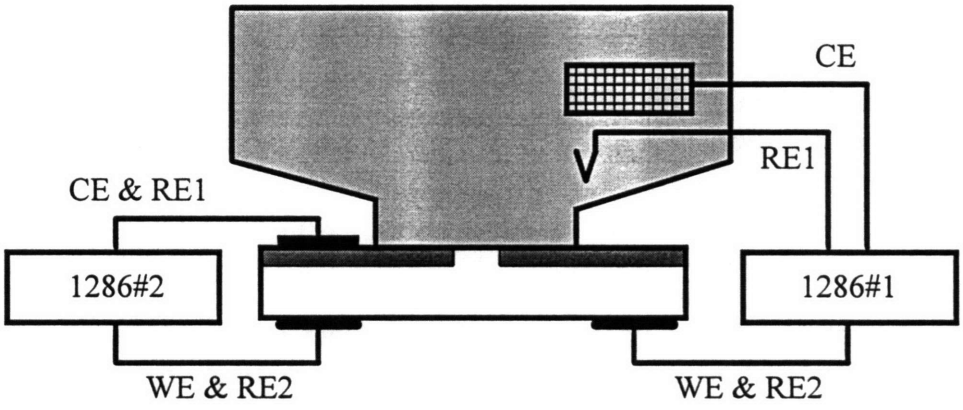


Figure 4.6. Schematic diagram showing the connection of two 1286 potentiostats to a cantilever beam sample.

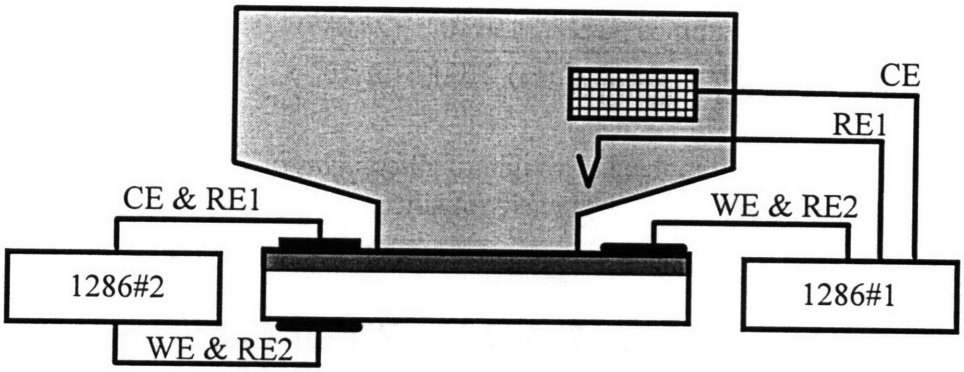


Figure 4.7. Schematic diagram showing the connection of two 1286 potentiostats to a n-epi on p-Si substrate sample for demonstrating its p-n-p transistor characteristics in HF electrolyte.

volt-meter for determining the junction potential drop.

In addition, two potentiostats were simultaneously operated in the configuration shown in figure 4.7 to demonstrate the p-n-p transistor characteristics of a n-epi on p-Si substrate sample immersed in HF electrolyte. The potentiostats were connected in common base mode with 1286#2 across the emitter-base (p-n) junction and 1286#1 across the collector-base (silicon-electrolyte interface) junction. 1286#1 was swept in potentiostatic mode from reverse to forward p-n junction bias, and 1286#2 was set to 0.5V (SCE), a potential above the n-Si anodic dissolution onset bias to demonstrate the correlation between n-Si etching current and p-n junction current.

4.3.4 Post-Etch Sample Cleaning

After etching, all samples were removed from the cell, rinsed with either methanol or deionized water, and carefully cleaned with Solon cotton tipped applicators dipped in acetone to remove the dabs of high vacuum silicone grease at the corners. Electropolished samples were then rinsed in methanol to remove any residual acetone and allowed to dry in air. Samples etched under porous silicon conditions were instead rinsed in DI water and immersed in 25 weight percent KOH at room temperature to dissolve the porous silicon. Typically rapid bubble evolution was observed for approximately 5 seconds although in a few instances bubbles formed slowly and persisted for over a minute. Once bubble evolution ceased the samples were removed, rinsed in DI water, dipped in 5% HF for 15 seconds, rinsed in DI water again, and left to dry in air. Occasionally the evolved bubbles remained adhered to the surface shielding the porous silicon from the KOH solution. If so the bubbles were dislodged by rinsing in DI water and then re-immersed in the KOH solution.

Chapter 5

Results

In this chapter we present experimental data of etching studies on the various samples outlined in chapter 4 and show SEM micrographs of the resulting structures. During the course of this thesis many experiments were performed on bulk n- and p-Si to systematically determine the effects of key etching parameters such as applied bias, HF concentration, illumination intensity, illumination wavelength, doping density, and crystallographic orientation, on the resulting etch rate, dissolution valence, and etched-surface smoothness. These results are first summarized with an emphasis on those parameters important for understanding the p-n junction etch-stop and high aspect ratio etching results. A more complete presentation and discussion of the bulk silicon etching studies is deferred to the appendix.

In section 5.2 the etching studies of cantilever beam test samples are presented, demonstrating the ability to achieve high quality p-n junction etch-stops with three novel techniques. This is followed by a study of the etching characteristics of epi-layer samples which confirms the theoretical aspects developed in chapter three. And finally, the more preliminary results on etching of high-aspect ratio structures using optical masking is presented in section 5.4.

5.1 Etching Characteristics of Bulk Silicon

5.1.1 Effect of Etching parameters on Bulk Silicon Current-Voltage Characteristics

HF concentration

The current-voltage characteristics of 5Ωcm p-Si are shown in figure 5.1 for a range of HF concentrations. These characteristics were measured using electrolyte circulation (see section 4.2.3) so that mass transport kinetics are not rate limiting. The current-voltage characteristics of 5Ωcm n-Si are presented in figure 5.2 showing similar

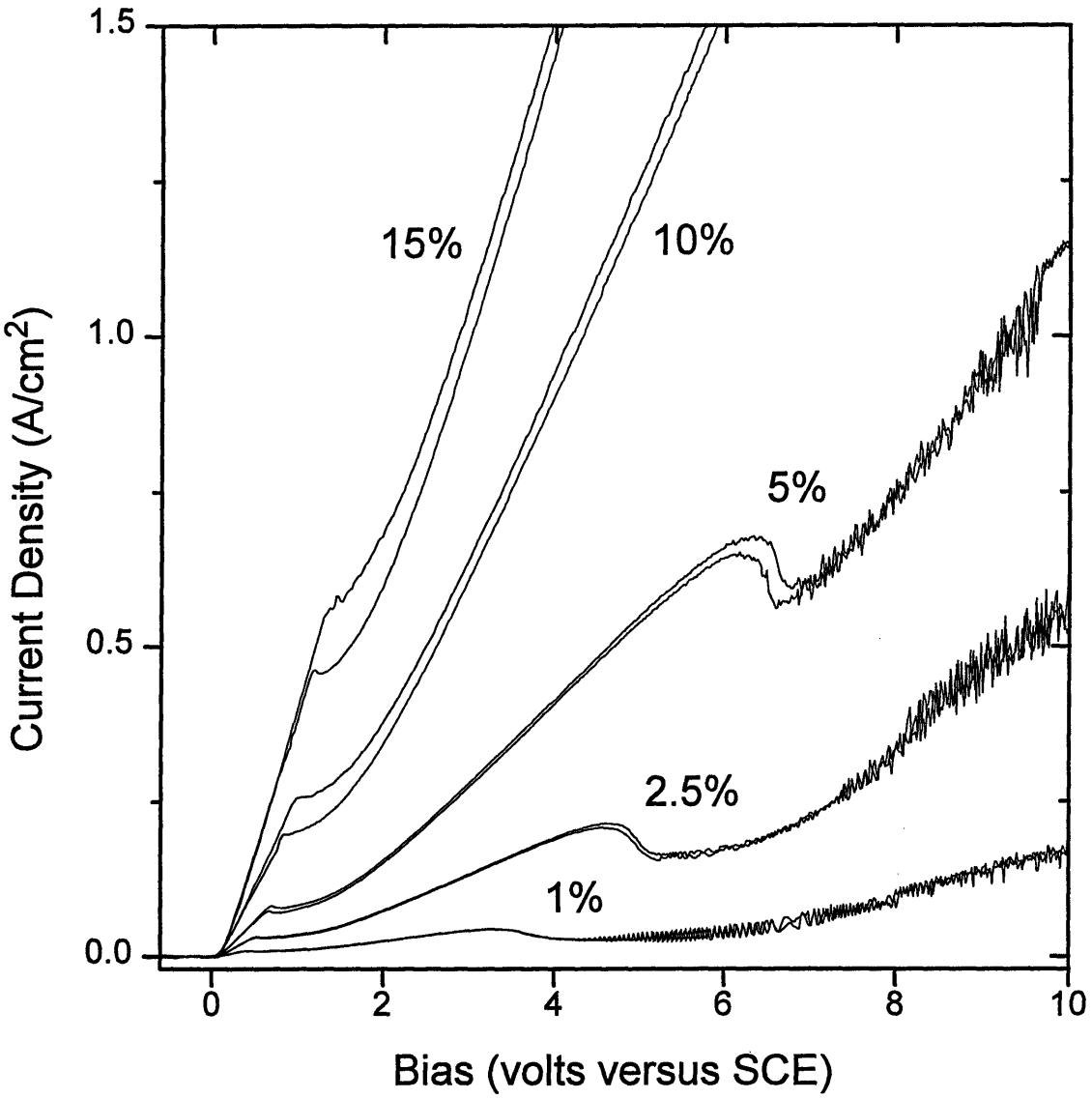


Figure 5.1. Current-voltage characteristics of 5Ωcm p-Si as a function of electrolyte HF concentration, measured using 100mV/s sweep rate, 600mL/min electrolyte flow rate, and no illumination.

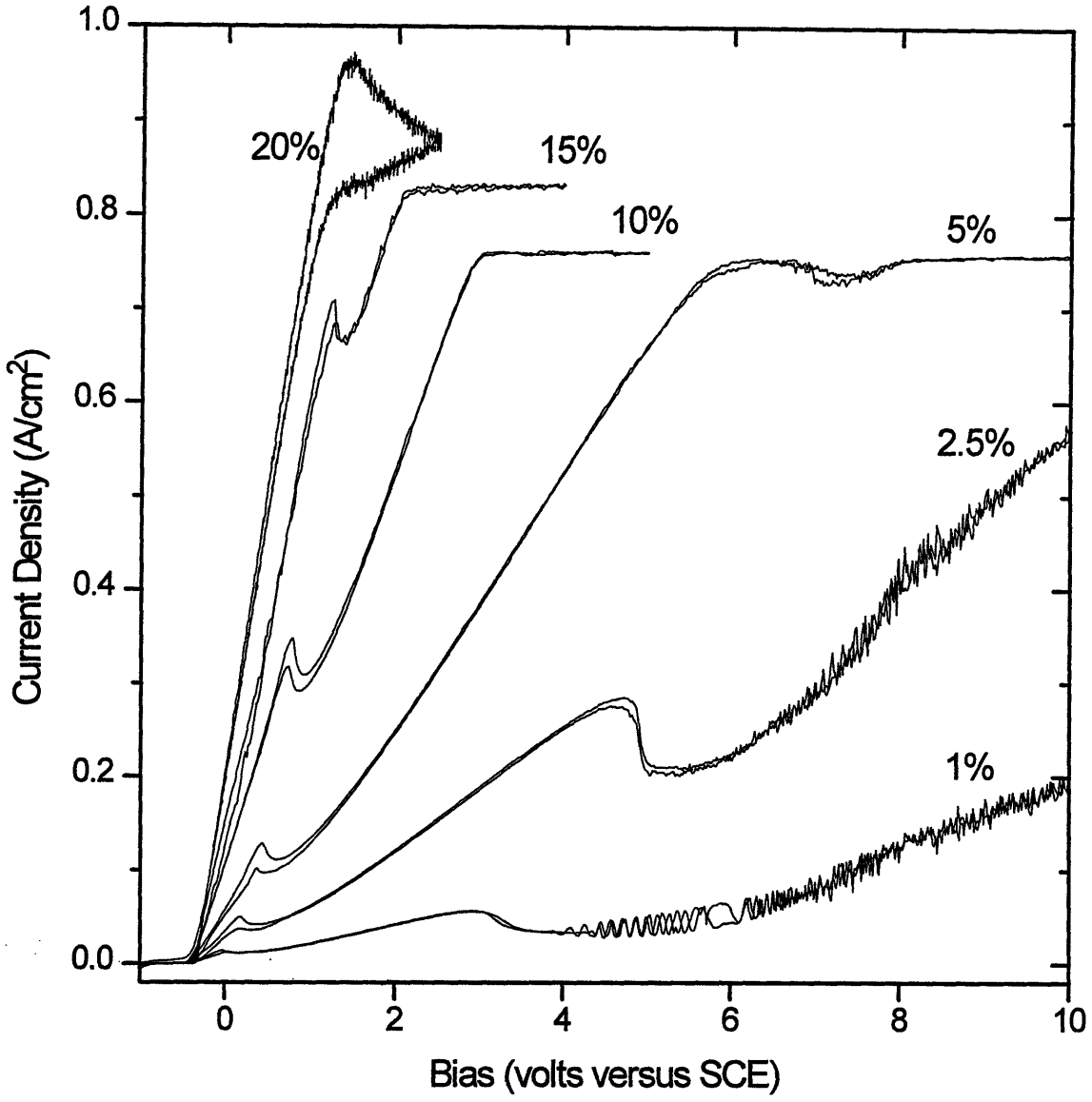


Figure 5.2. Current-voltage characteristics of 5Ωcm n-Si as a function of electrolyte HF concentration, measured using 1.42 W/cm^2 white light illumination, 100 mV/s sweep rate, and 600 mL/min electrolyte flow rate.

behavior until the etch rate becomes limited by the photo-generation rate.

The curves exhibit two current peaks consistent with other reports in the literature, however the current densities and biases corresponding to the second current peaks are higher than for studies where electrolyte agitation was not employed. A linear (ohmic) region in the I-V characteristics is evident at biases below each peak, which was found to result primarily from the IR resistive drop in the ≈1.5cm of electrolyte between the silicon surface and the reference electrode. The I-V characteristics, after compensation for the electrolyte resistive drop ($V_{eff} = V_a - IR_{el}$), show virtually no linear regions (see appendix 4). The current-voltage characteristics below the first current peak are nearly independent of HF concentration, indicating that mass transfer or concentration of fluoride species in the electrolyte do not significantly limit the dissolution rate below the first current peak. After compensating for the electrolyte IR drop we also find that the bias corresponding to the second current peak is virtually independent of HF concentration, occurring at ≈2V and ≈3V (SCE) for n-Si and p-Si respectively. This suggests that the second current peak arises from a bias-dependent change in anodic oxide composition which impedes the attack of Si-O-Si bonds as discussed in section 2.1.2.2.

The first and second peak current densities were plotted as a function of $[HF_2^-]$, $[F^-]$, and $[HF_{undissociated}]$ using log-log plots. The slopes of these plots for both peaks were found to be linear with $[HF_2^-]$ and $[HF_{undissociated}]$ but not with $[F^-]$, indicating that the first two species but not F^- participate in the dissolution reaction. The slopes 'n' and 'm' corresponding to the equation $J\alpha[HF_2^-]^n[HF_{undissociated}]^m$ are summarized in table 5.1

	first peak		second peak	
	n	m	n	m
p-Si forward sweep	1.16	1.38	1.37	1.64
p-Si reverse sweep	1.21	1.40	1.38	1.66
n-Si forward sweep	1.18	1.38	1.38	1.66
n-Si reverse sweep	1.21	1.40	1.38	1.65

Table 5.1. Reaction orders 'n' and 'm' of the reaction $J\alpha[HF_2^-]^n[HF_{undissociated}]^m$ for the first and second current peaks of p- and n-Si.

Illumination intensity

The current-voltage characteristics of p-Si were found to be virtually independent of illumination intensity, except for a 0.025V shift in the anodic direction for illuminated versus unilluminated p-Si.

n-Si current-voltage characteristics, on the other hand, show very low currents when unilluminated and a large dependence on illumination intensity. Figure 5.3 shows repeated current-voltage sweeps from -1 to ≈12V SCE at 100mV/s on the same

repeated current-voltage sweeps from -1 to ≈12V SCE at 100mV/s on the same unilluminated 5Ωcm n-Si sample in 5% HF electrolyte. The dark current increases with each sweep as micro-pores and pits develop on the surface which facilitate localized breakdown. The first sweep was measured on the initially polished surface as provided by the wafer supply house, and exhibits an anodic current of approximately 10^{-5} A/cm^2 which increases by less than a factor of 2 over the 12 volt sweep. This current density is orders of magnitude higher than that expected for thermal generation in the depletion zone and must therefore result from some electron injection process into the conduction band. It is surprising, however, that this process occurs virtually independently of applied potential. Nevertheless it is evident from figures 5.1 and 5.3 that unilluminated n-Si etching currents are at least 4 orders of magnitude lower than those of p-Si except at high potentials.

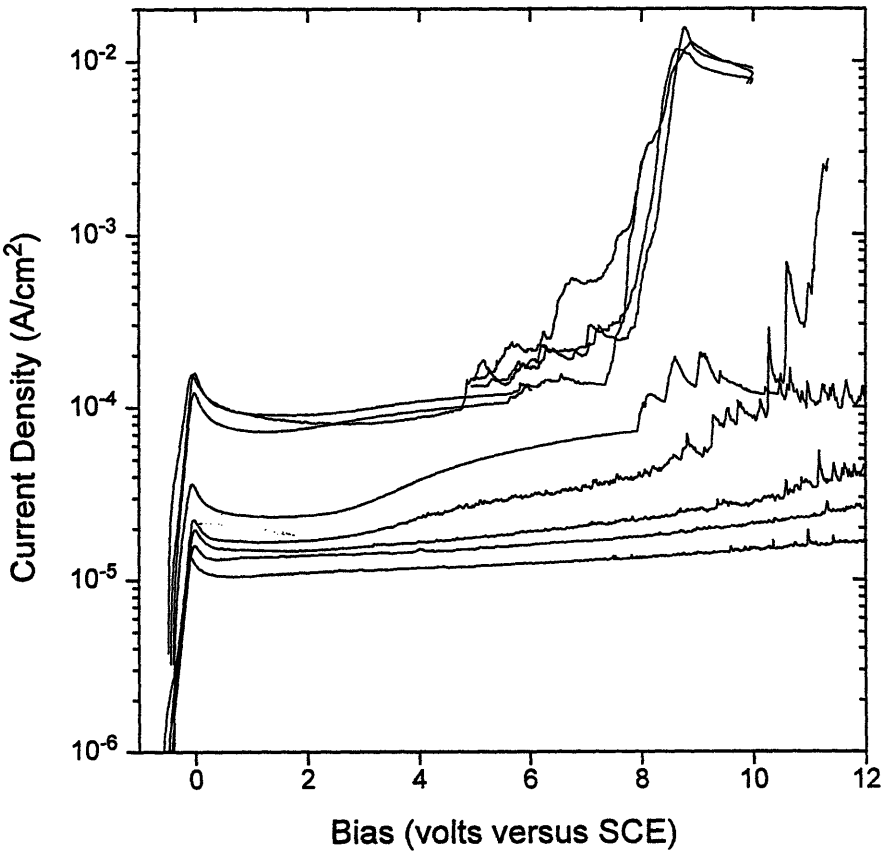


Figure 5.3. Repeated current-voltage sweeps (100mV/s) on the same non-illuminated 5Ωcm n-Si sample in 5% HF showing increasing dark current with subsequent sweeps as the surface roughens and micro-pores develop.

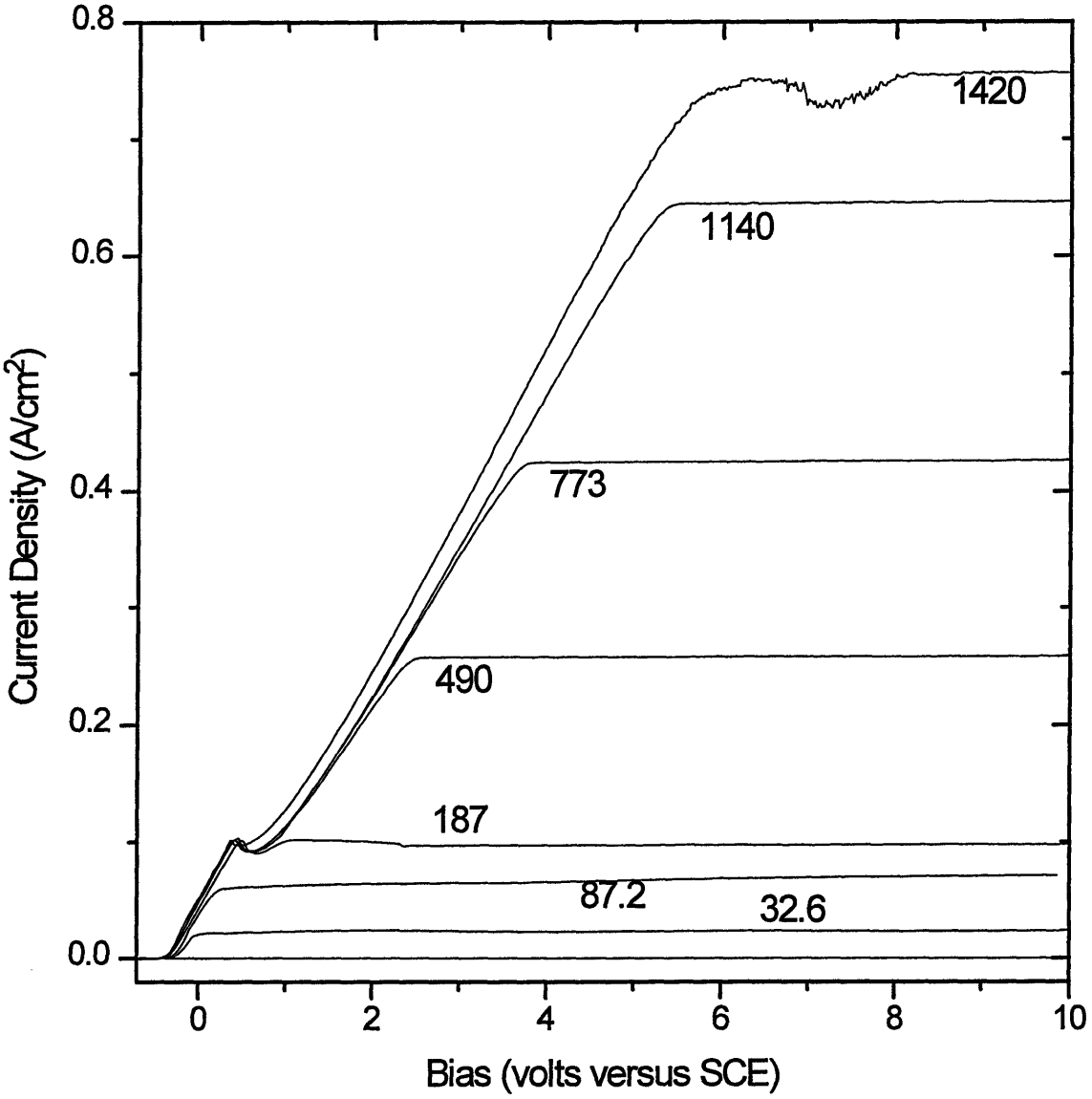


Figure 5.4. Current-voltage characteristics of 5Ωcm n-Si as a function of illumination intensity in mW/cm^2 as shown in the graph. Measured using 5% HF, 600mL/min electrolyte flow rate, and 200mV/s sweep rate (except for the 1420mW/cm^2 curve which was measured with 100mV/s sweep rate).

Figure 5.4 shows n-Si current-voltage characteristics as a function of illumination intensity. revealing a p-Si like behavior followed by a current plateau when the current becomes limited by the hole photo-generation rate. The plateau current density is plotted as a function of illumination intensity in figure 5.5 showing a linear dependence. Some deviation is evident at lower current densities corresponding to porous silicon formation, presumably because the roughened surface collects incident photons more efficiently by reducing reflection and promoting photon absorption near the surface.

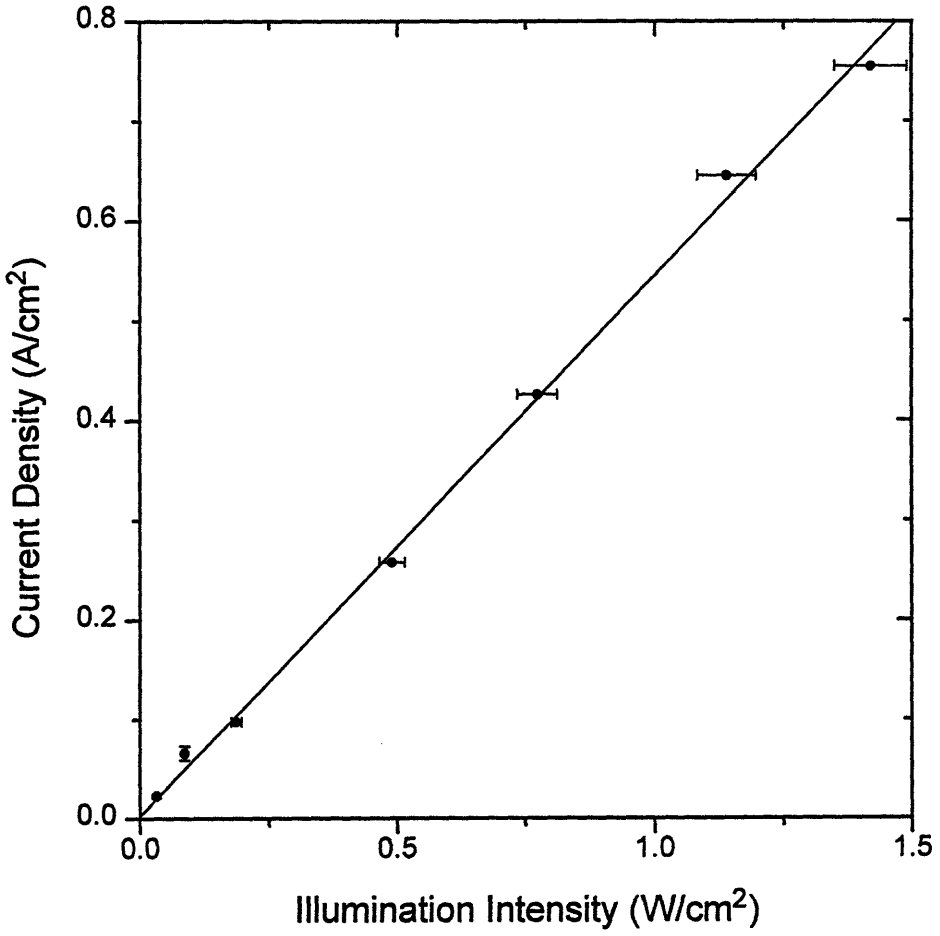


Figure 5.5. Illumination-intensity-limited current density of 5Ωcm n-Si (from figure 5.12) as a function of illumination intensity.

Doping Density and Crystallographic Orientation

Both p- and n-Si I-V characteristics were found to shift cathodically with increasing doping density. p-Si I-V characteristics shifted proportionately with $(N_A)^{1/2}$ in agreement to the results of Gaspard *et. al.* [80], with a shift of ≈0.13V from $N_A=7x10^{14}cm^{-3}$ to $N_A=1x10^{19}cm^{-3}$. For n-Si the cathodic shift was measured to correlate better with the shift in Fermi energy than with $(N_D)^{1/2}$. A cathodic shift of 0.08V was measured between the current-voltage characteristics of $N_D=1x10^{14}cm^{-3}$ and $N_D=4x10^{15}cm^{-3}$ n-Si.

No significant difference was observed in the current-voltage characteristics of (111), (110), or (100) p-Si. For n-Si, however, the first peak current density for (111) wafers was only about 75% of that for (100) wafers, comparable to the results of Lehmann [73].

5.1.2 The Silicon Electrochemical Etch Rate

For micromachining, etch rate rather than etching current is the parameter of importance. We therefore measured the p- and n-Si etch rates as a function of applied bias and current density using various HF concentrations and illumination intensities by a series of timed etch experiments and subsequent DEK TAK measurements of the etch depth. The etch rate as a function of applied bias in 1%, 5%, and 15% HF electrolytes is plotted in figures 5.6 and 5.7 for 5Ωcm p-Si and 5Ωcm n-Si respectively. Notice the close resemblance of these graphs to the current-voltage characteristics in figures 5.1 and 5.5. The dependence of etch rate on anodic current is presented in figures 5.8 and 5.9. Two particularly impressive results are evident for electrochemical silicon etching in HF. First, the etch rate can be controlled over orders of magnitude by appropriately choosing the bias and HF concentration, which can even be extended beyond those used in figures 5.8 and 5.9. Electrolyte HF concentrations are readily availlable to 48% and can be easily diluted to hundredths of a percent or less. The Solartron 1286 potentiostat limited our experiments to 12.8V (SCE), however we expect greater anodic biases will continue to yield higher current densities. Second, silicon can be etched at rates in excess of 100μm/min as compared to the maximum of ≈0.8μm/min for KOH type etchants at 80°C.

The arrows in figures 5.8 and 5.9 indicate the first peak current density and the dashed lines show calculated etch-rates assuming dissolution valences of 2 and 4 for the upper and lower lines respectively. The dissolution valence for all three electrolyte HF concentrations is 4 in the electropolishing regime and increases from 2 to 4 as the current density approaches the first current peak. The dissolution valence is a useful micromachining parameter since it permits the calculation of the volume of silicon removed from the charge that is passed through the external cell circuit. More dissolution valence results are presented in appendix 4.

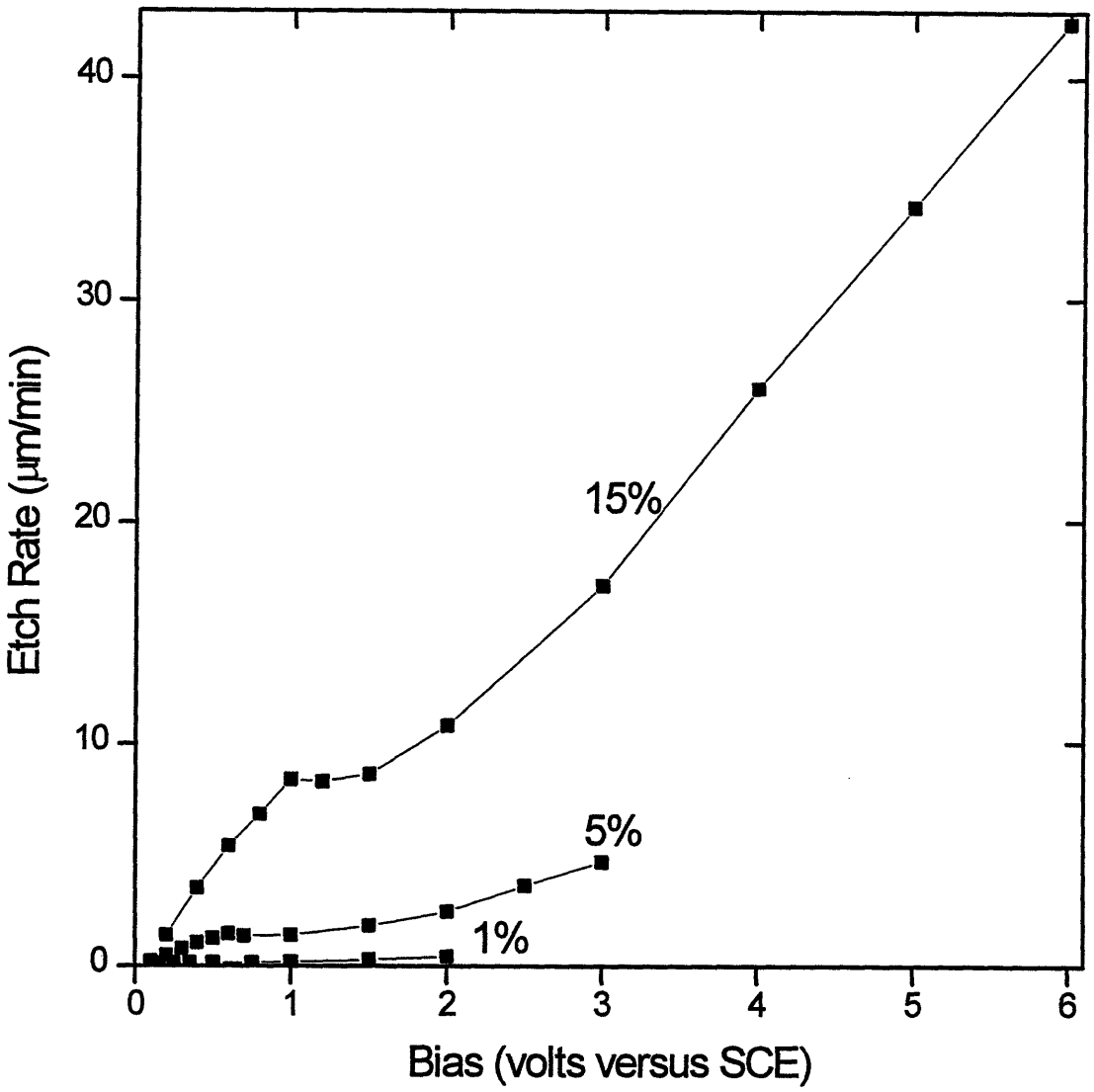


Figure 5.6. 5Ωcm p-Si etch rate as a function of bias for 1, 5, and 15% HF electrolytes.

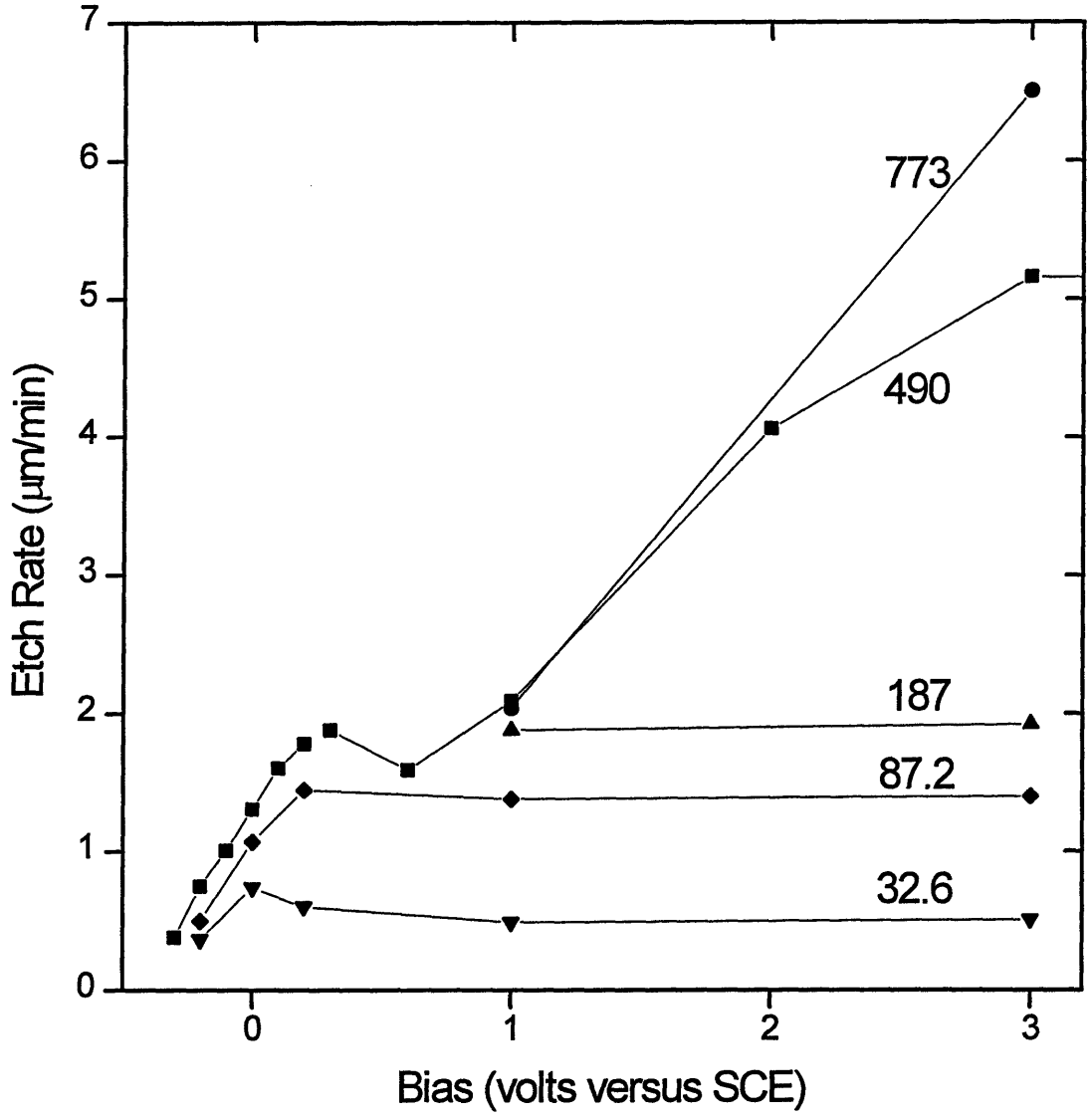


Figure 5.7. The etch rate 5Ωcm n-Si in 5% HF as a function of cell bias for various white light illumination intensities (mW/cm^2) as indicated.

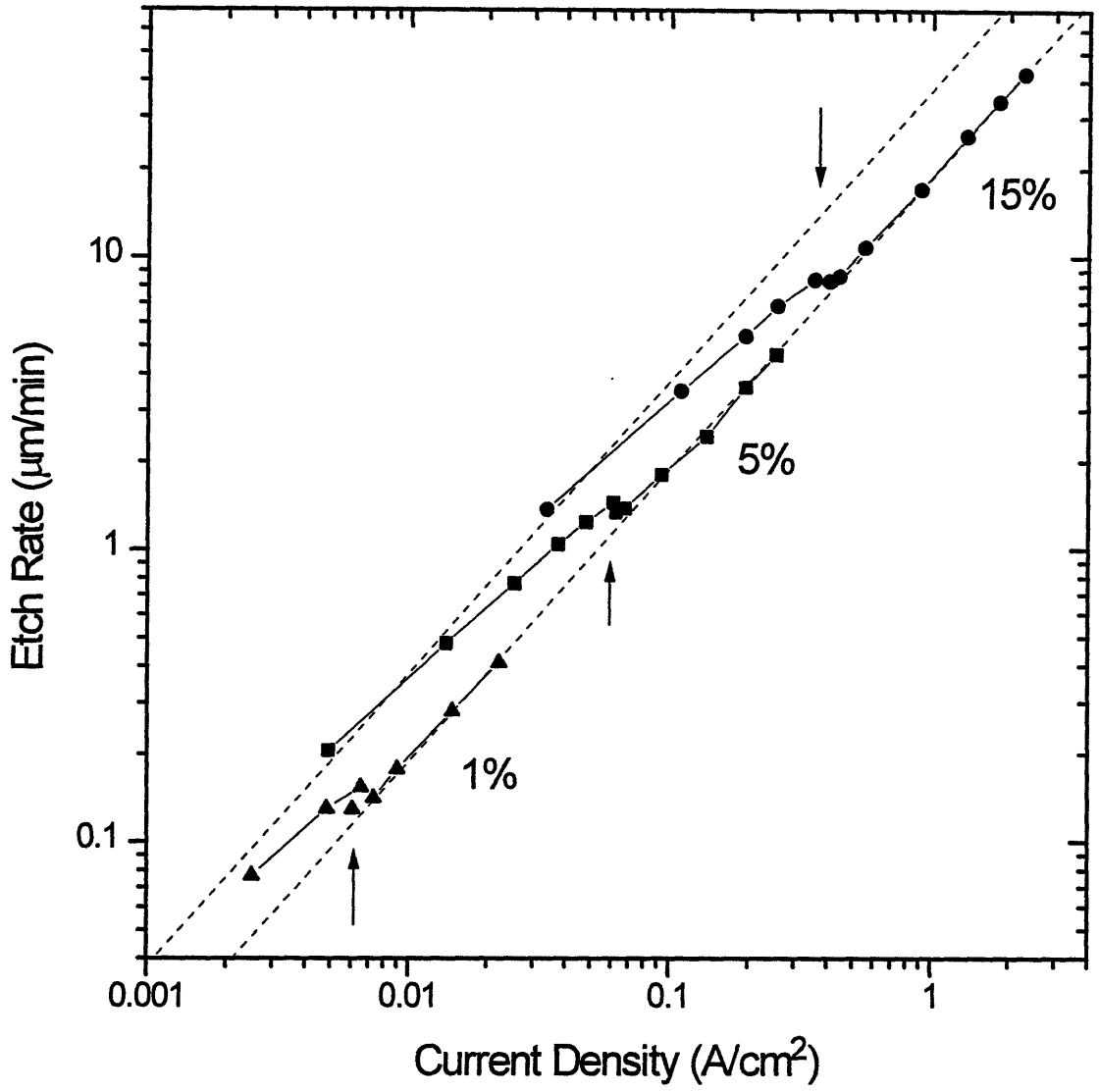


Figure 5.8. Etch rates of 5Ωcm p-Si as a function of current density in 1, 5, and 15% HF. Dashed lines indicate the expected etch-rate as a function current density for dissolution valences of 2 and 4, and arrows indicate J_{crit}.

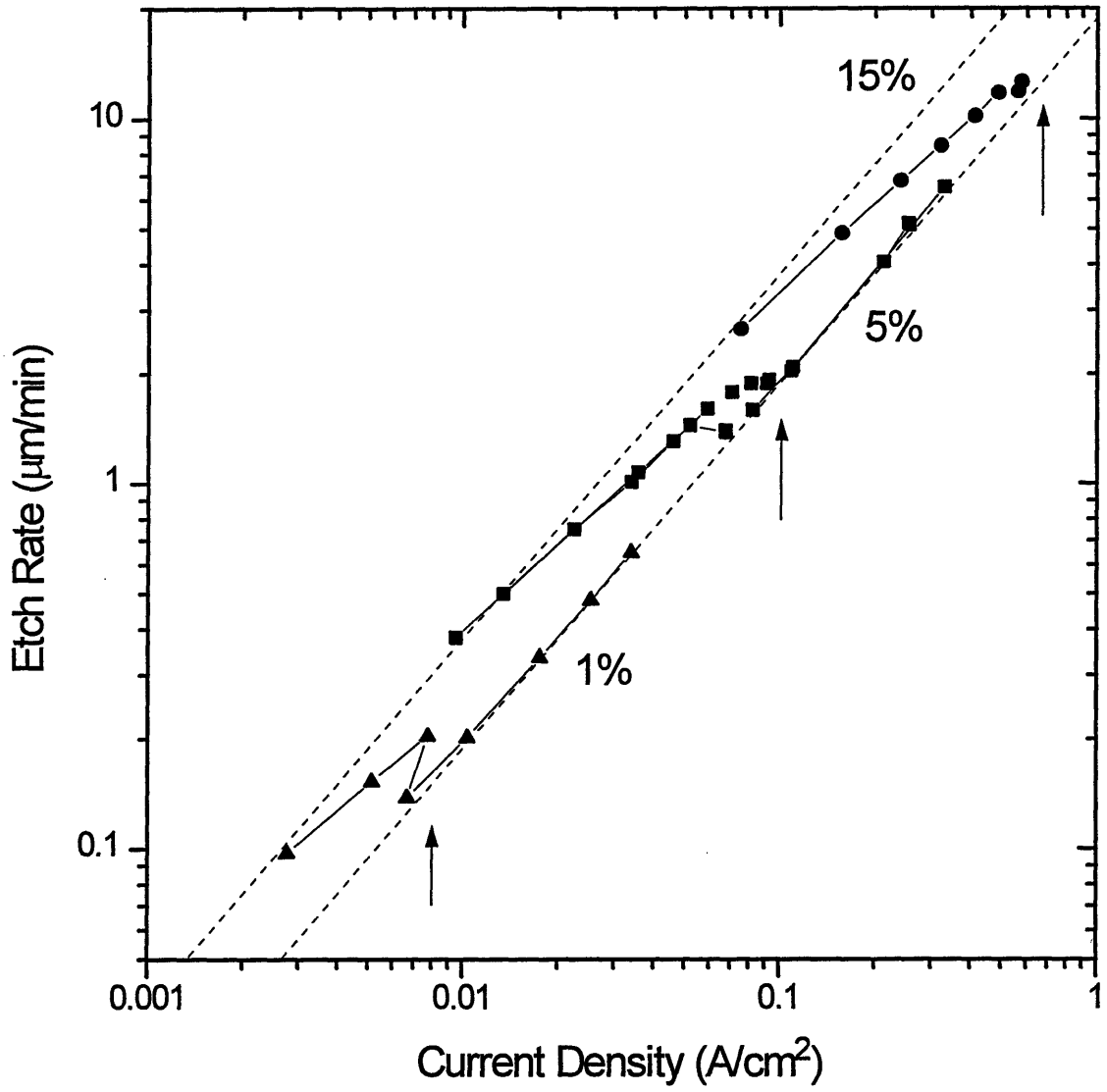


Figure 5.9. Etch rates of 5Ωcm n-Si as a function of current density in 1% HF and 187mW/cm^2 white light illumination, 15% HF and 1140mW/cm^2 white light illumination, and 5% HF and 773, 490, 187, and 87.2 mW/cm^2 white light illumination. Dashed lines indicate the expected etch-rate as a function current density for dissolution valences of 2 and 4, and the arrows indicate J_{crit}.

5.1.3 Morphology of Etched Surfaces

p- and n-Si samples were systematically etched at various biases and HF concentrations to determine the resulting surface smoothness. Figure 5.10 shows the profilometry traces of surfaces etched in 5% HF at potentials and current densities as indicated in figure 5.11. At current densities above porous silicon formation progressively smoother surfaces were obtained with increasing current density. Feature sizes decreased from 0.5μm at 0.6V (SCE) (just below the first current peak), to 0.1μm at 0.75V (SCE), to 0.01μm (which was the resolution of the Sloan DEK TAK III) for biases greater than or equal to 3.0V (SCE). No differences in surface morphology was found on surfaces etched below, at, or above the second current peak. A similar study of illuminated n-Si revealed surface roughnesses with feature sizes an order of magnitude larger than for p-Si near the first current peak. These surfaces however quickly became smoother with increasing current density until a <0.01μm feature size was observed at 3V (SCE) just as for p-Si.

Profilometry traces of porous silicon surfaces were not measured because porous silicon is removed from micromachined surface, typically by a 5 second dip in 25 weight percent KOH at 25°C. Consequently the porous silicon/bulk silicon interface morphology and its evolution during porous silicon removal is of greater importance . The surface morphology after the KOH dip was found to vary dramatically depending on doping type and the etching conditions. Very rough surfaces with feature sizes of tens of microns were obtained both before and after the KOH dip when etched at current densities approximately 2/3 of that of the first peak. Zhang *et. al.* [51] reported that both electropolishing and porous silicon formation proceeds simultaneously on the surface at these potentials which may explain the dramatic roughening. Much smoother surfaces with sub-micron feature sizes were obtained for p-Si samples etched at lower porous silicon formation potentials. Presumably the interface between the nano-porous layer and bulk silicon is uniform resulting in smooth surfaces after porous silicon removal. When n-Si is electrochemically etched in the porous silicon regime both macro-pores and nano-porous films are formed as explained in section 2.1.1.1. After the KOH dip, the surface consists of overlapping inverted tetrahedron pits bounded by (111) planes as shown in figure 5.12. Apparently even at room temperature the 25 weight percent KOH solution rapidly etches non (111) silicon planes, resulting in lateral etching of the macropores until only (111) planes are exposed. The lower magnification micrograph shows terraces which can form when electrolyte agitation is insufficient to remove hydrogen bubbles evolved at the surface. These bubbles isolate the surface from electrolyte and thereby locally prevent etching until they are dislodged.

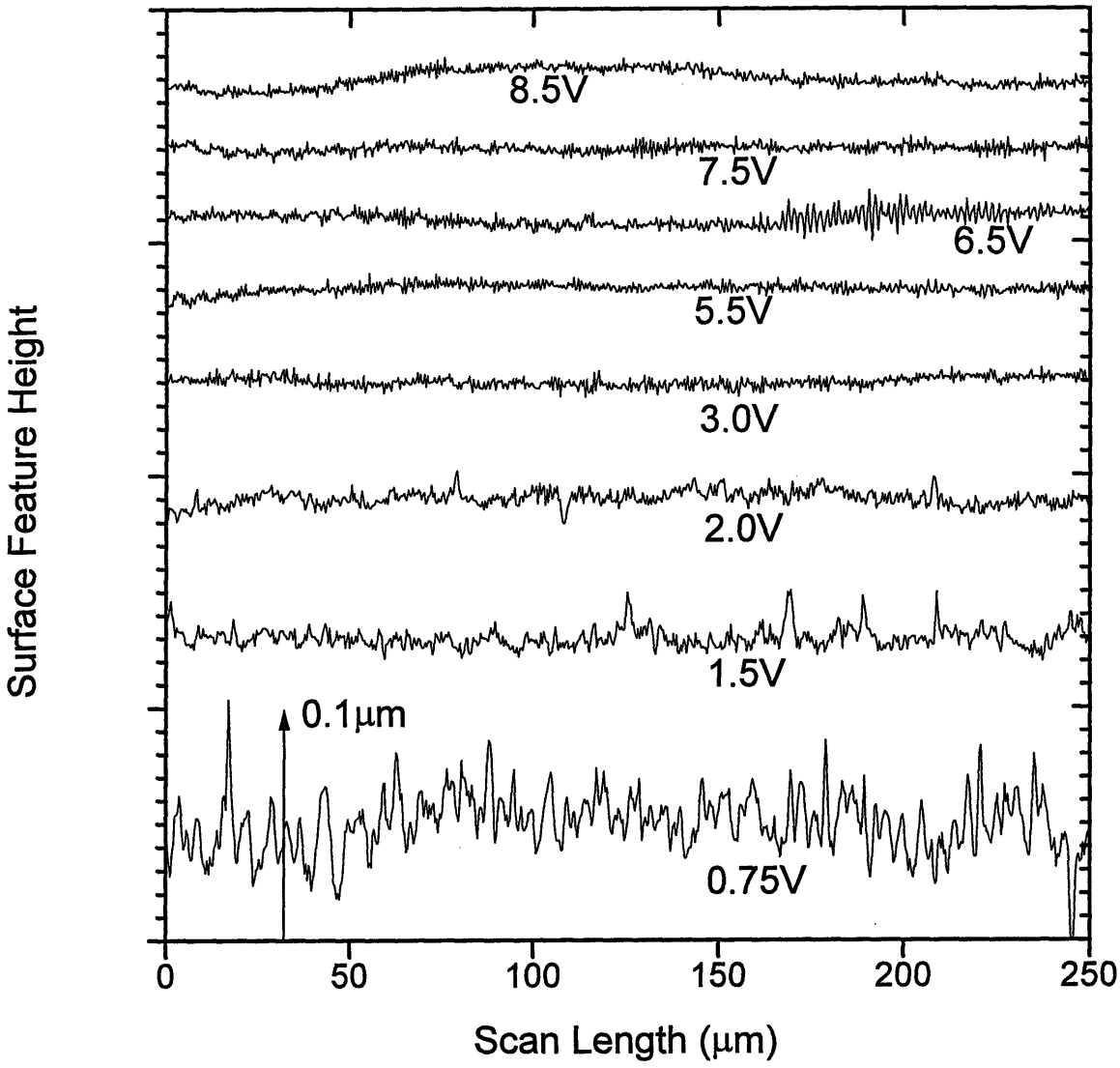


Figure 5.10. DEK TAK III surface profiles of 5Ωcm p-Si samples etched at the potentials indicated.

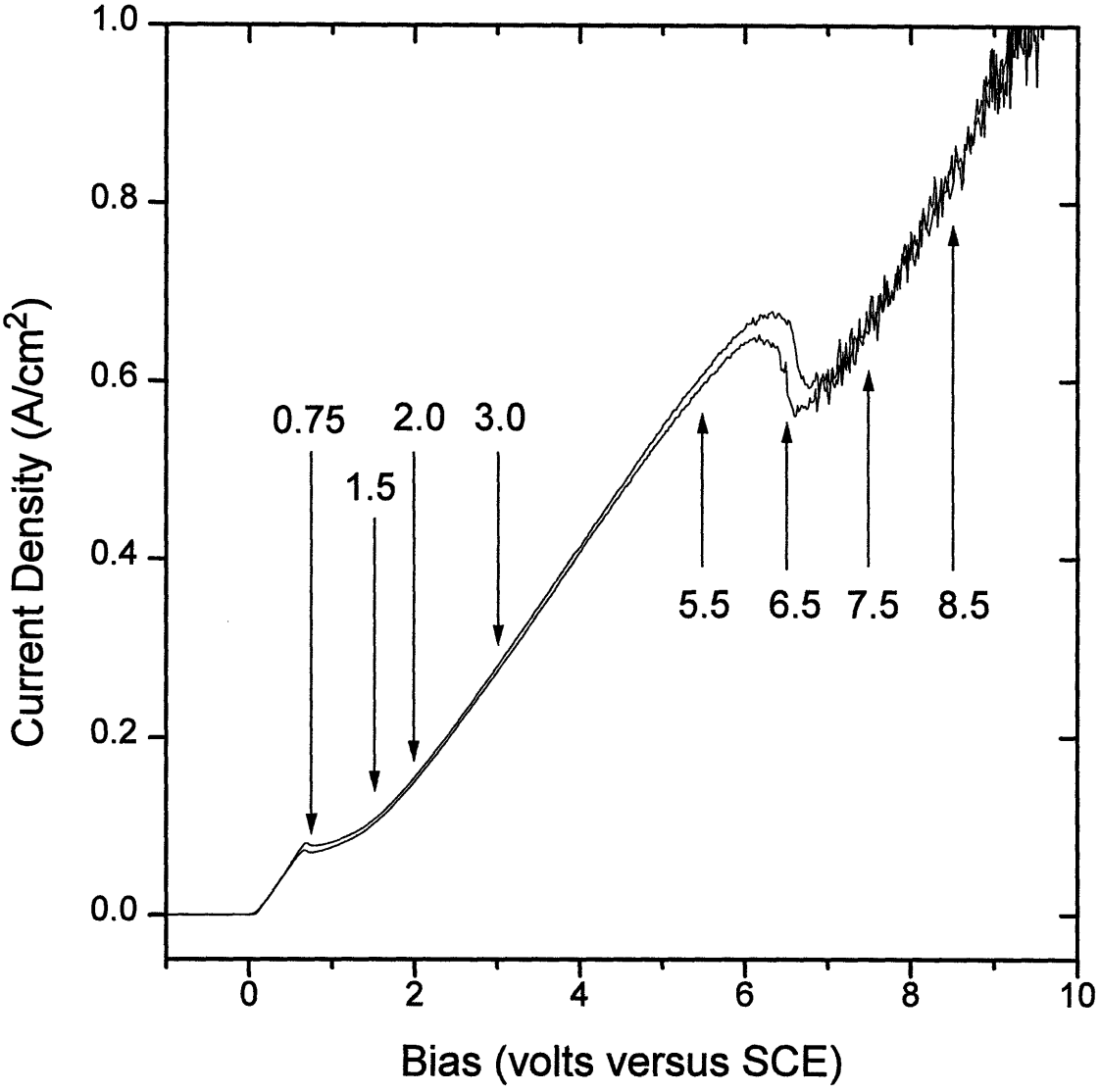


Figure 5.11. Current-voltage characteristics of 5Ωcm p-Si showing the potentials at which samples where etched before measuring the resulting surface smoothness.

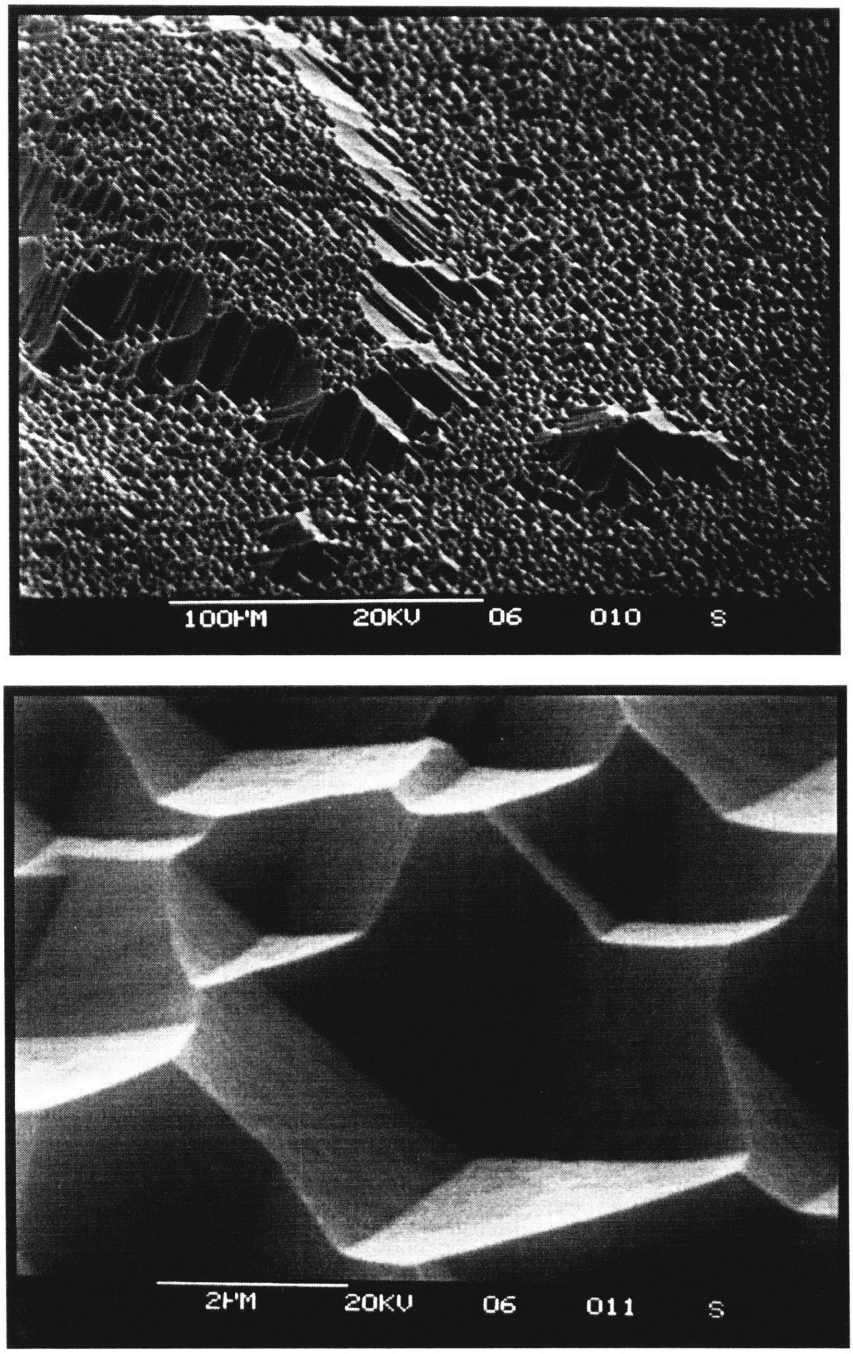


Figure 5.12. SEM micrographs of 5Ωcm n-Si surfaces etched in 5% HF using 0.1V (SCE) and 187mW/cm^2 white light illumination after the porous silicon layer was removed by a 10 second dip in 25 weight percent KOH at 25°C.

5.1.4 *Selective Etching Possibilities Arising from Differences in p-Si and n-Si Etching Characteristics*

Bulk silicon micromachining is possible when specific regions of a silicon sample exhibit vastly different etch rates allowing selective removal of the fast etching regions. When the current-voltage characteristics of p-Si and both illuminated and unilluminated n-Si are compared as shown in figure 5.13, three apparent selective etching possibilities are immediately evident. First, n-Si can be selectively etched in the potential 'window' between -0.5V and 0.0V (SCE). Second, p-Si can be selectively etched versus unilluminated n-Si at potentials greater than 0.0V (SCE). And finally, illuminated n-Si can be selectively etched versus unilluminated n-Si at potentials greater than -0.5V (SCE).

Unfortunately these selective etching possibilities are not trivial to implement due to a variety of complications. In the case of illuminated n-Si versus p-Si, the illuminated p-n junctions generate photo-biases which drive p-Si anodic with respect to n-Si. In the case of p-Si versus unilluminated n-Si, holes can be injected by the forward biased p-n junction into the n-Si causing its dissolution. Difficulties are also encountered when etching high aspect ratio structures using optical masking which are discussed in section 5.4.

In the next section we present experimental evidence for these p versus n selective etching complications, and show how they were overcome to achieve three distinctly different p-n junction etch-stops.

5.2 Etching of Cantilever Beam Test Structures

Cantilever beam test structures were fabricated as described in section 4.12 to demonstrate the feasibility of the p-n junction etch-stop techniques. In each case the silicon around and below the cantilever beams (see figure 4.1) having the opposite doping type was selectively etched. Both the cantilever beams and the surrounding silicon were exposed to the electrolyte as shown in figure 4.6. Typically the silicon surrounding the cantilever beams accounted for only ≈7% of the total 0.075cm^2 silicon-electrolyte interface area. The area of silicon being etched exposed to the electrolyte increases with time as cantilever beam underetching proceeds, and therefore the current-voltage characteristics of cantilever beam structures are reported as currents rather than current densities.

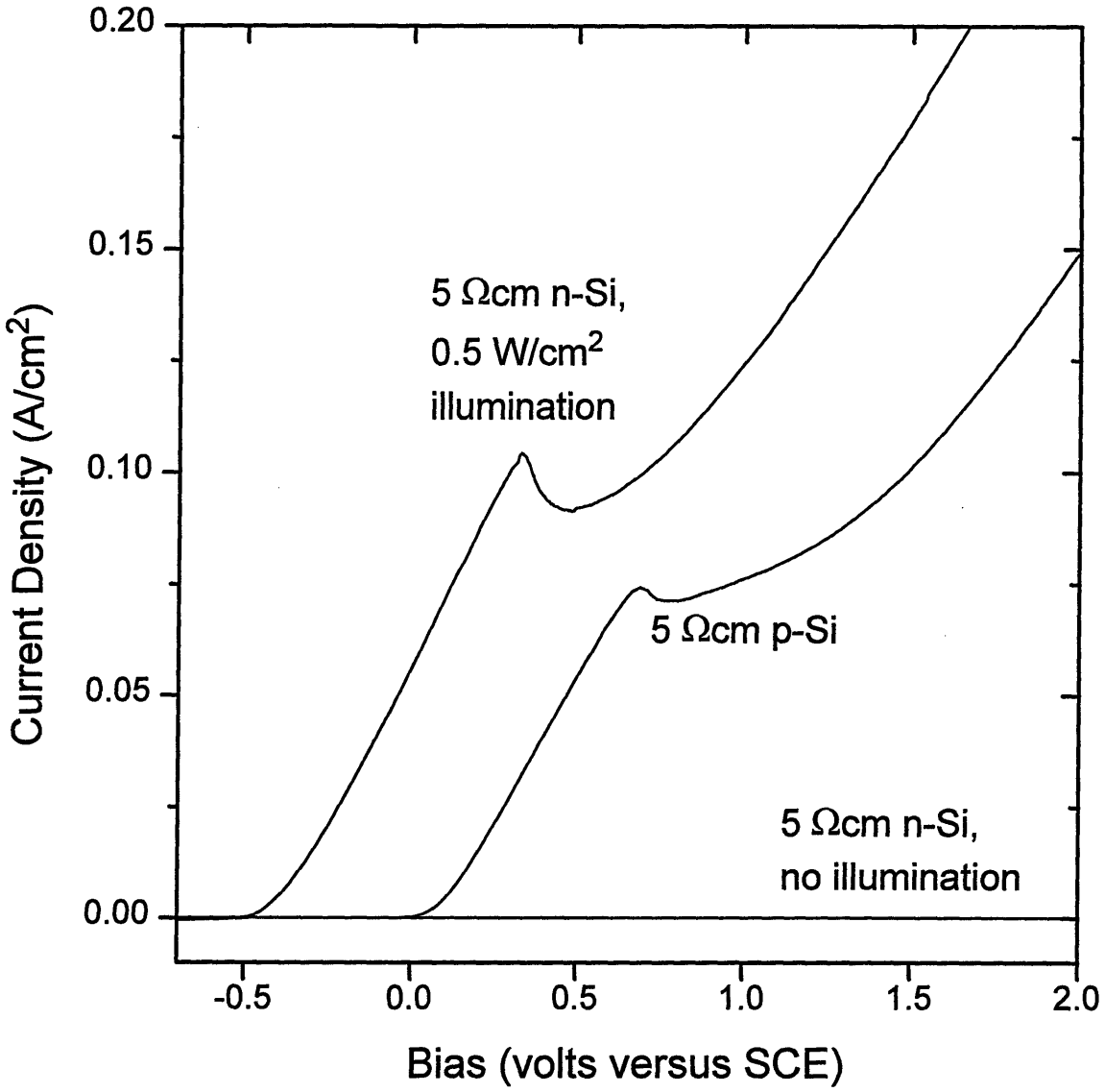


Figure 5.13. Comparison of the current-voltage characteristics of 5Ωcm p-Si to illuminated and non-illuminated 5Ωcm n-Si.

5.2.1 *The p-on-n Etch-Stop*

Figure 5.14 shows a comparison of the current-voltage characteristics of illuminated p-on-n cantilever beam test samples to those of bulk p-Si and n-Si. The cell potential (plotted on the x-axis) is applied to the n-Si substrate. The illuminated p-n junction biases the p-layer anodic with respect to the n-substrate, and consequently the etching onset shifts cathodically to ≈-0.7V (SCE). This current corresponds to p-layer etching as verified using DEK TAK profilometry. A second rise in cell current is observed at ≈-0.4V (SCE) corresponding to etching of the small illuminated n-Si area. Micromachining of p-Si structures by selective etching of the illuminated n-substrate is therefore not possible because the photo-bias shift is greater than the window for selective etching of n-Si versus p-Si.

In order to compensate for the photo-bias we first shorted the p-layer to the n-substrate by applying liquid gallium across the p-n junction. Curve (a) of figure 5.15 shows the I-V characteristics of the shorted p-on-n cantilever beam test structure without illumination. The p-layer readily etches since the reverse biased p-n junction which normally blocks anodic currents is shorted by the gallium. Note that the p-layer etching onset potential is shifted cathodically as compared to previously shown 5Ωcm p-Si current-voltage characteristics because of its higher $N_A=4x10^{19}$ cm^{-3} doping density. Curves b, c, and d (solid curves) show the p-on-n cantilever beam test structure I-V characteristics when illuminated with 25, 80 and 160nW/cm^2 white light respectively. The etching current of these curves is a summation of both the illuminated n-Si and p-Si currents. When the p-Si current (curve a) is subtracted from curves b, c, and d the characteristic n-Si illumination intensity limited current-voltage characteristics become clearly visible. While n-Si versus p-Si selective etching is now possible between ≈-0.4 and -0.25V (SCE) the maximum n-Si etch rate is very low because of the narrow bias window and underetching of 50μm wide cantilever beams was achieved only after 3 hours. Furthermore etching is limited to the porous silicon regime which requires subsequent porous silicon removal and yields rough n-Si etched surfaces.

These limitations were overcome by reverse biasing rather than shorting the p-n junction, thereby allowing independent biasing of the n- and p-regions. Such independent biasing is possible because the p-n junction is reverse biased which sustains the potential difference. Figure 5.16 shows the I-V characteristics of the p-on-n cantilever beam test structure as a function of p-n junction bias. These curves were measured without illumination and the current therefore represents only p-layer etching. Figure 5.16 clearly shows the 1:1 correlation between p-n junction reverse bias and the suppression of p-Si etching to more anodic biases. When illuminated, the p-n junction reverse bias can now be used to widen the potential window for selective etching as shown in curves c and d of figure 5.17. It therefore becomes possible to etch n-Si in the electropolishing regime using sufficiently high n-Si and p-n junction biases and illumination intensities.

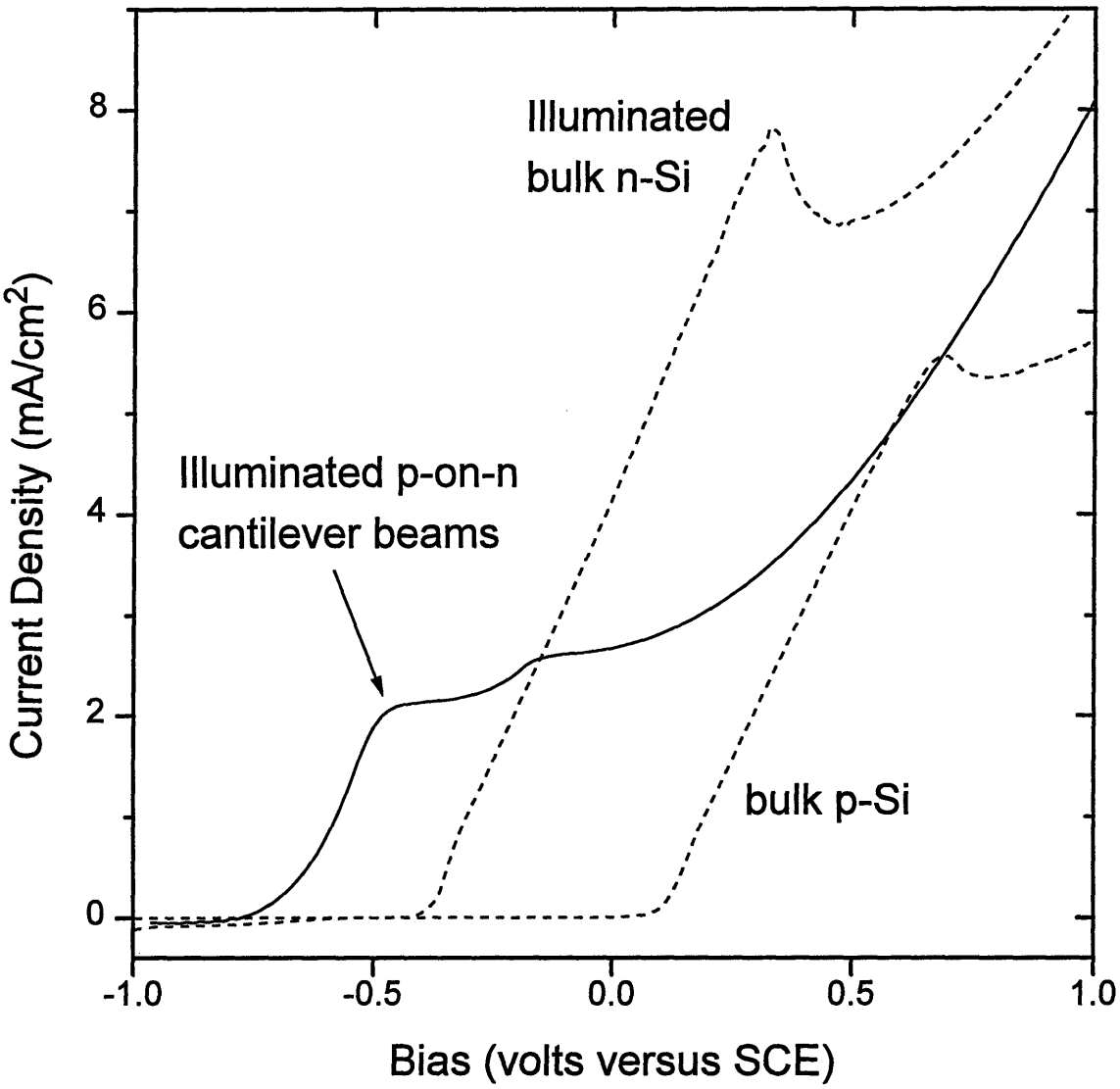


Figure 5.14. Comparison of the current-voltage characteristics of illuminated p-on-n cantilever beam samples to those of bulk 5Ωcm p-Si and illuminated 5Ωcm n-Si.

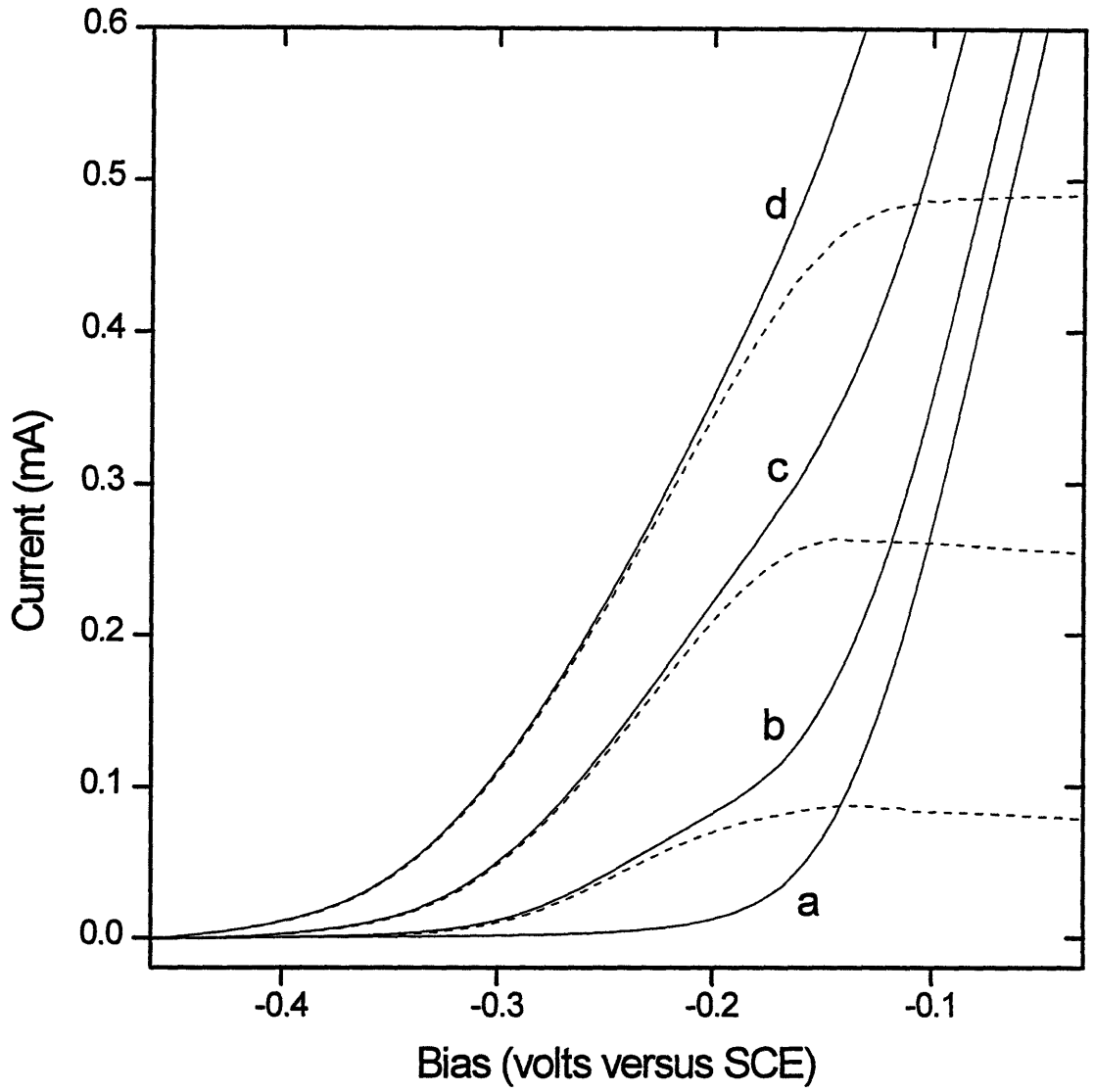


Figure 5.15. Current-voltage characteristics at different white light illumination intensities of p-on-n cantilever beam samples with the p-layer is shorted to the back-side ohmic contact: a) dark, b) 25mW/cm^2, c) 80mW/cm^2, and d) 160mW/cm^2. The total current (solid curves) include the etching currents of both the p-layer and the illuminated n-region which defines the beams. The dashed curves were calculated by subtracting curve a from curves b, c, and d, and therefore show only the n-Si etching current.

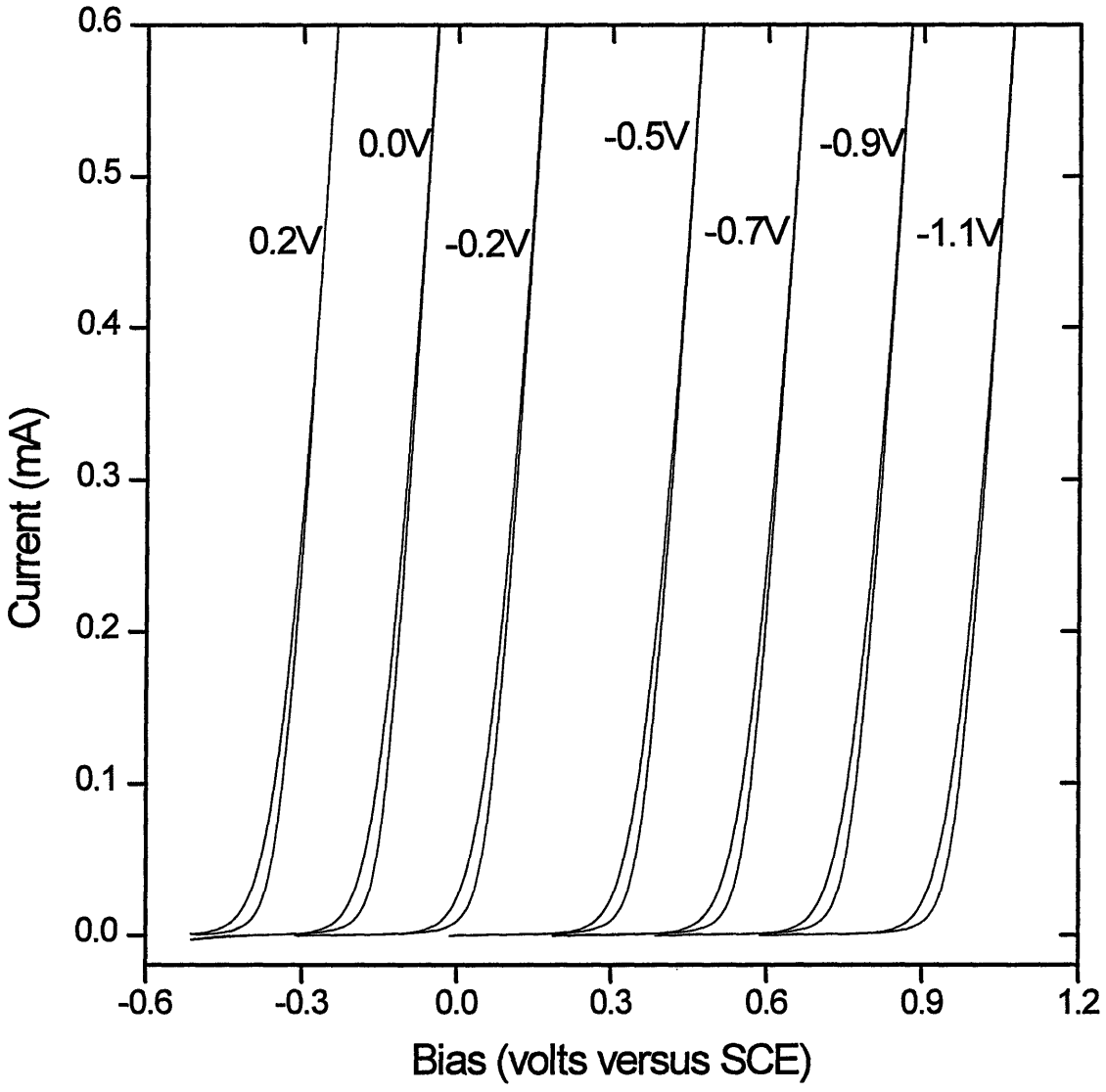


Figure 5.16. Current-voltage characteristics of p-on-n cantilever beam samples as a function of varying p-n junction reverse bias. Measured using no illumination, 5% HF, and 20mV/s sweep rate.

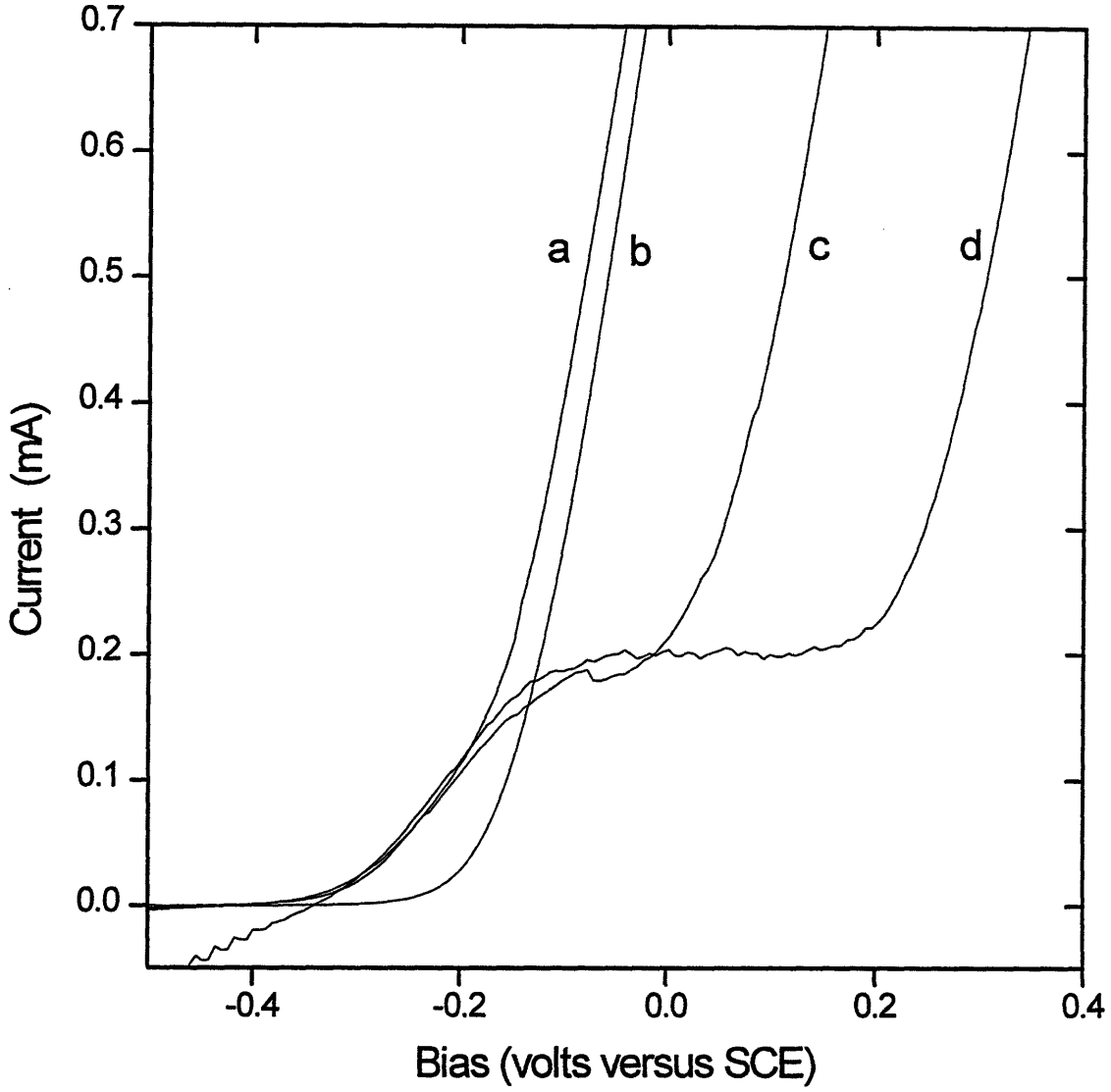


Figure 5.17. Current-voltage characteristics of p-on-n cantilever beam samples as a function of varying p-n junction reverse bias: b) no illumination and 0.0V reverse bias, a, c, and d) 80mW/cm^2 and 0.0V, 0.2V, and 0.4V reverse bias respectively.

Figure 5.18 shows a typical current versus time curve for etching of a p-on-n cantilever beam test structure. The current increases with time as the cantilever beams are underetched and the n-Si area exposed to the electrolyte increases.

SEM micrographs of successfully etched cantilever beams are shown in figures 5.19 and 5.20 for 4 different etching conditions. Beam dimensions are 3.3μm thick by 180μm wide by 650μm long. All were etched at potentials above the first current peak to achieve reasonable etch rates, and all except for 5.20(a) were etched at electropolishing conditions (≥ 3V (SCE) and sufficient illumination intensities so as not to be rate limiting). Notice that the electropolished samples are smooth and curved while the 5.20(a) sample surface is angular. Several factors affect the shape of the etch-pit bottom which are discussed in chapter 6. Figures 5.21 (a) and (b) show SEM micrographs of the n-Si etched surface morphology below the cantilever beams for the samples in figures 5.20(a) and 5.19(b) respectively. As expected from the etched surface morphology results on bulk silicon, the surface etched at 1.0V (SCE) exhibits more roughness than the one etched at 3V (SCE). Some residual roughness is still present on the surface etched at 3V (SCE) because of partial absorption of the incident illumination by the 3.3μm thick beam, which reduces the photo-generated current density below that of electropolishing conditions.

Figure 5.22. shows an enlargement of a corner of the cantilever beam in figure 5.19 (a). The high quality etch-stop is revealed by the preservation of the indiffusion profile formed during fabrication of the test structures. The n-Si was etched at a rate of ≈2μm/min, which when compared to the ≈Å /hour chemical etch rate of silicon in HF reveals an extremely high etch-stop selectivity of $\approx 10^8$.

5.2.2 The p-well Etch-Stop

The idea behind the p-well etch-stop is to make use of the photo-bias effect shown in figure 5.14, which provides a bias window between -0.7 to -0.5V (SCE) for selective etching of p-Si in contact with an illuminated p-n junction versus n-Si. The p-well cantilever beam test structure geometry, shown in figures 4.1(f) and 4.2(f), consists of a square p-well diffused into an n-substrate into which n-Si cantilever beams are diffused.

Figure 5.23 shows the current-voltage characteristics of the p-well structure (solid lines) at illumination intensities of 33, 87, 190, and 490mW/cm^2. The x-axis indicates the bias applied to the n-substrate, and the p-Si potential is therefore a summation of the x-axis potential plus the photobias. With increasing illumination intensity the I-V characteristics show both a shift in the cathodic direction and a more rapidly increasing cell current, which can be explained by the increases in photo-bias and hole generation rate with illumination intensity. The dashed lines show the etch rate of only the illuminated n-Si layer, which was measured by mounting the test sample in the cell such that the silicon-electrolyte interface Teflon seal was not over the p-well region. The illuminated n-Si etch rate is also found to increase with illumination intensity and

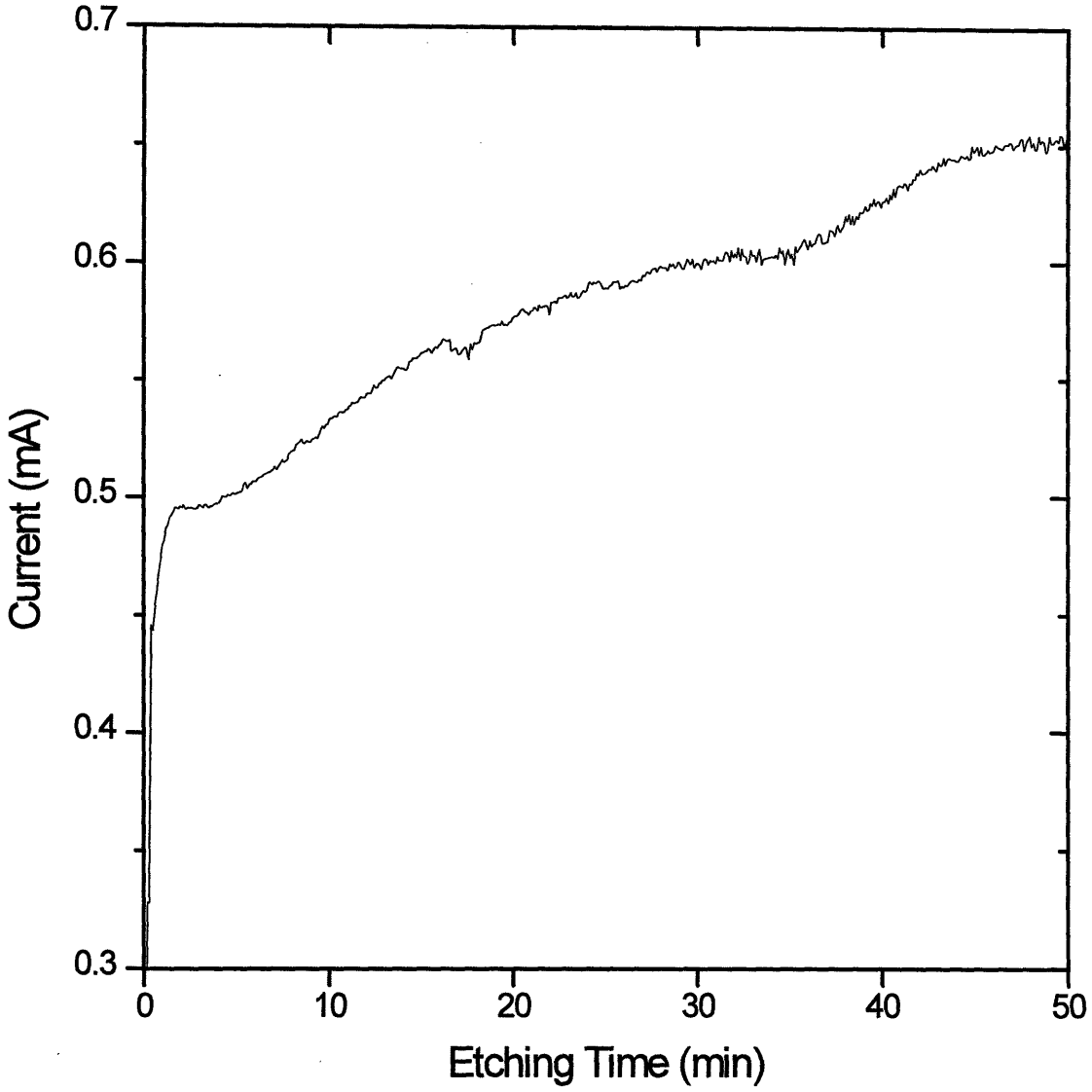
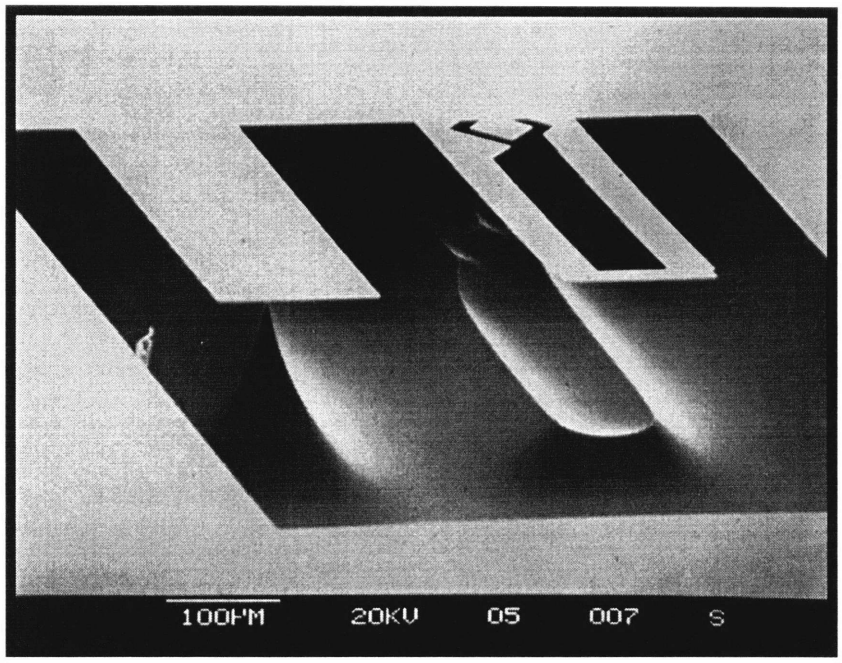
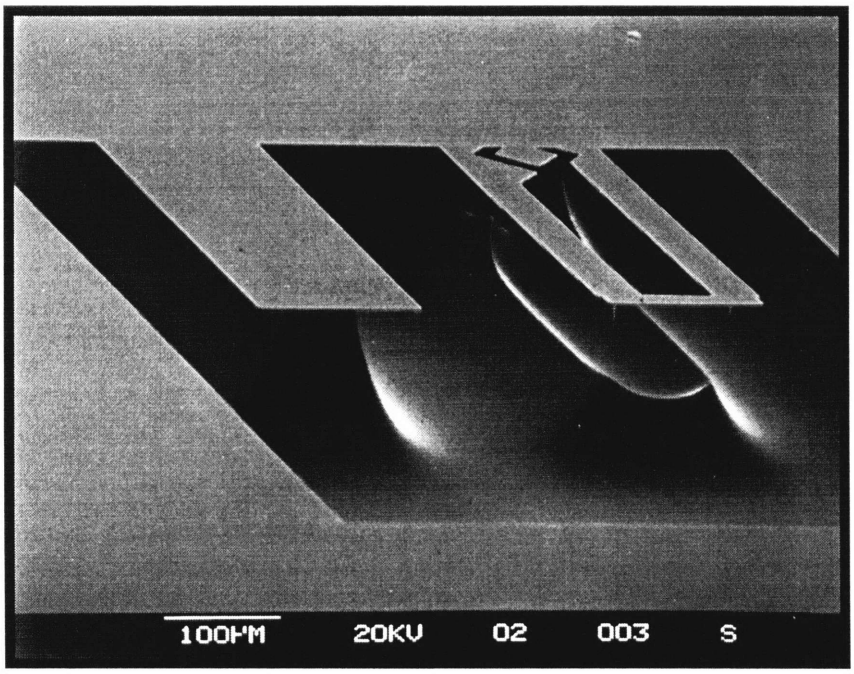


Figure 5.18. Typical measured current as a function of etching time for p-on-n cantilever beam samples. Etched using 0.2V (SCE), 0.7V p-n junction reverse bias, 5% HF, 600mL/min flow rate, and ≈200mW/cm^2 white light illumination.

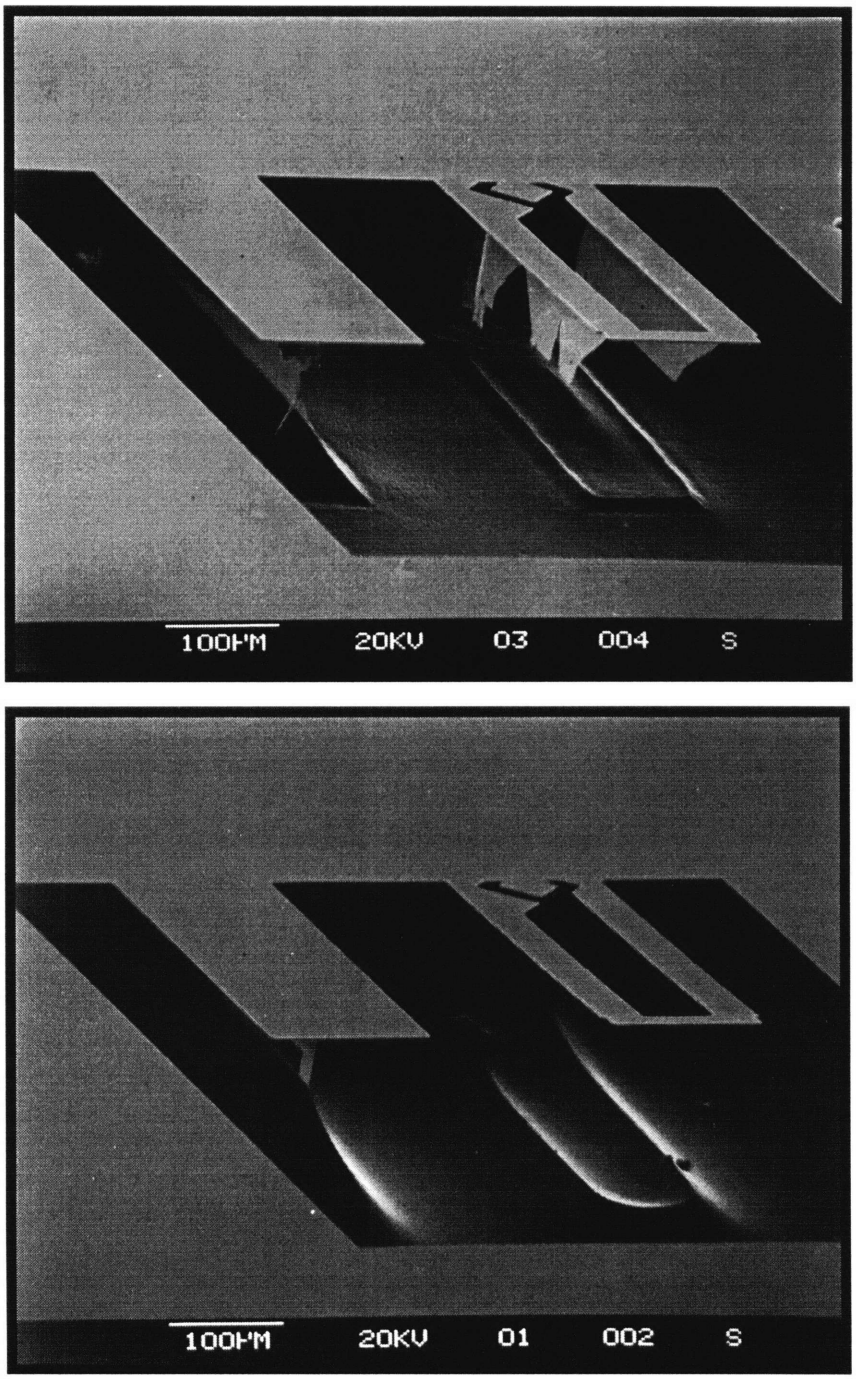


(A)



(B)

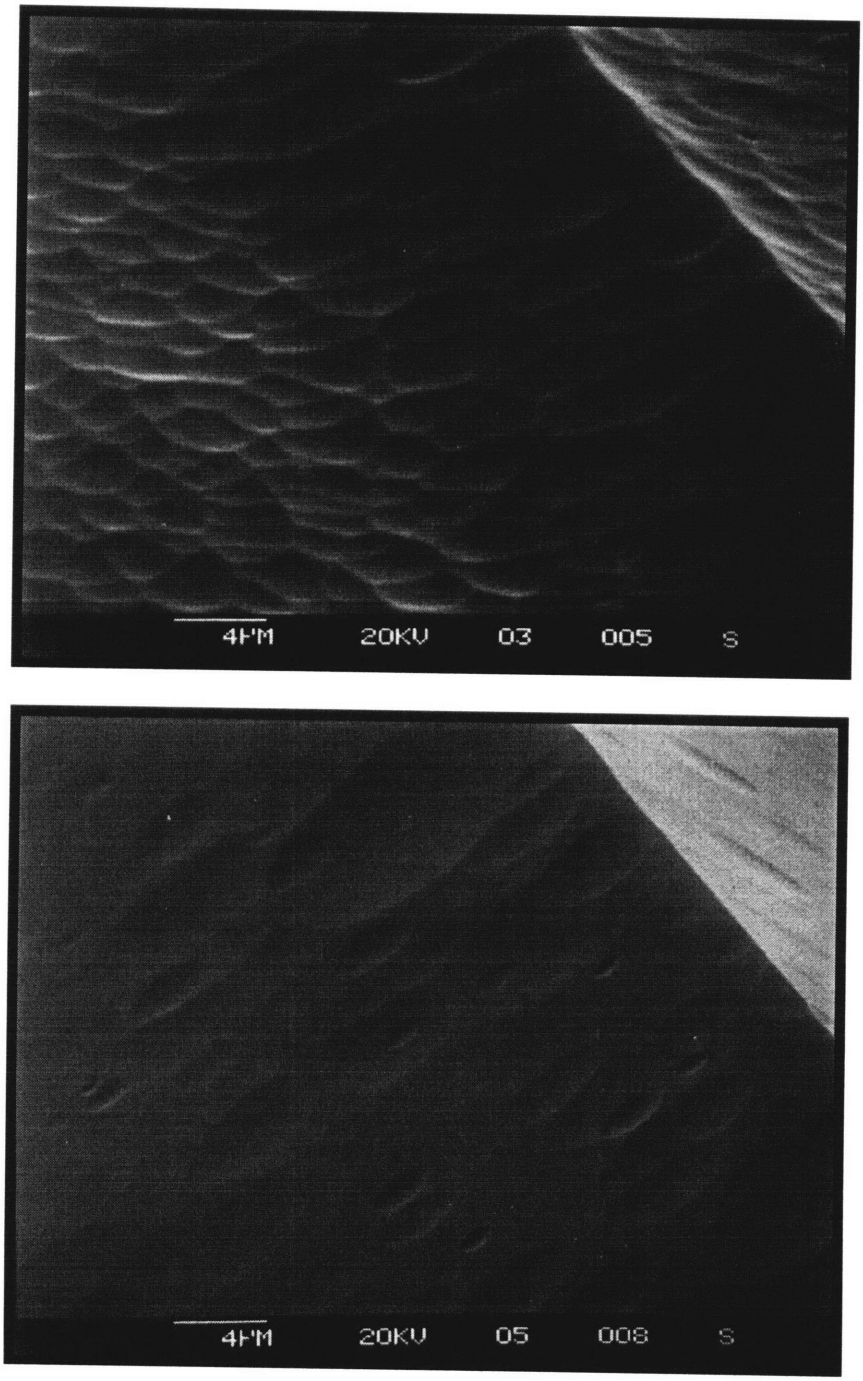
Figure 5.19. SEM micrographs of p-on-n cantilever beams etched using: (A) 3.0 V (SCE), -3.5 V p-n junction bias, 5% HF, 0.77 W/cm^2 white light illumination, 45 minutes etch time, (B) 5.0 V (SCE), -5.5 V p-n junction bias, 5% HF, 1.14 W/cm^2 white light illumination, and 20 minutes etch time. Beam dimensions are 3.3 x 180 x 650 μm.



(A)

(B)

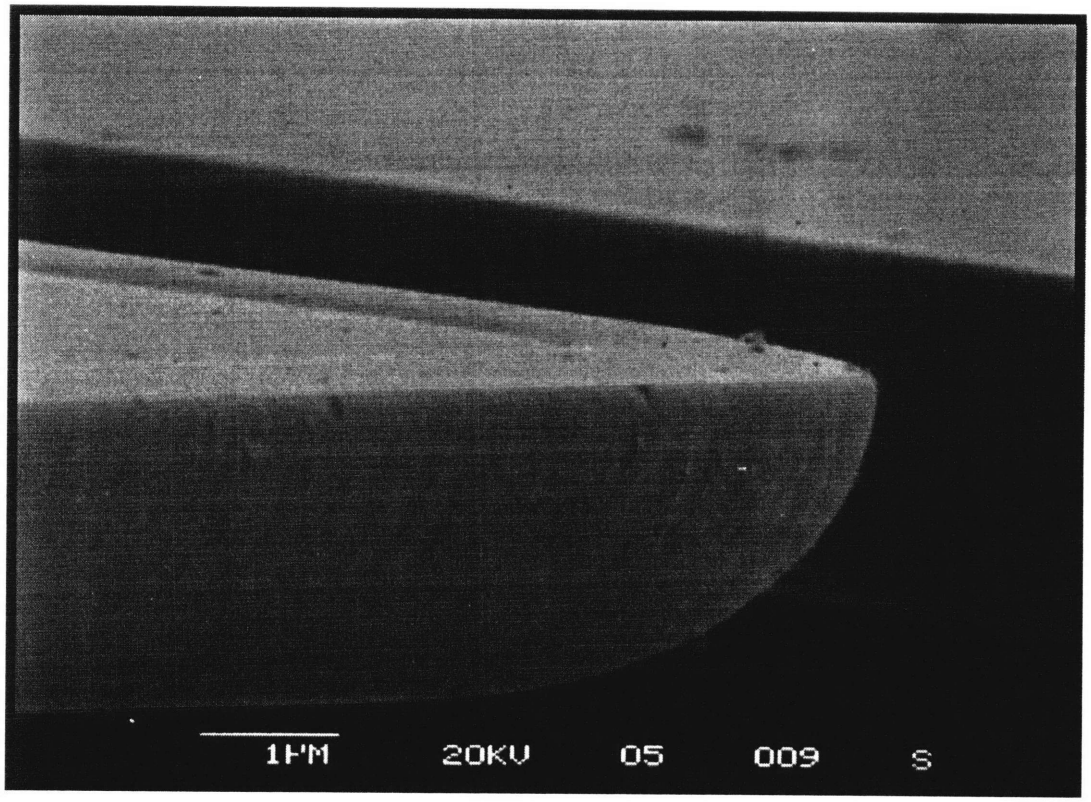
Figure 5.20. SEM micrographs of p-on-n cantilever beams etched using: (A) 1.0 V (SCE), -1.5 V p-n junction bias, 5% HF, 0.49 W/cm^2 white light illumination, 90 minutes etch time, (B) 3.0 V (SCE), -3.5 V p-n junction bias, 5% HF, 0.9 W/cm^2 red (λ>0.7µm) light illumination, and 20 minutes etch time. Beam dimensions are 3.3 x 180 x 650 µm.



(A)

(B)

Figure 5.21. SEM micrographs of n-Si surfaces etched in 5% HF using (A) 1.0V (SCE) and 490mW/cm^2 white light illumination, and (B) 3.0V (SCE) and 770mW/cm^2 white light illumination.



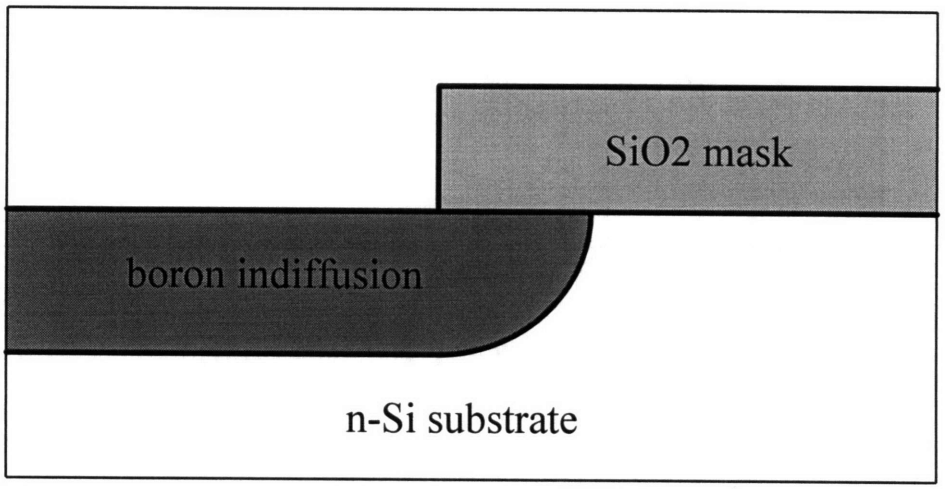


Figure 5.22. SEM micrograph showing an enlargement of a corner of the p-on-n cantilever beams in figure 5.20 (A). The high quality p-n junction etch-stop is clearly revealed by the preservation of the cantilever beam in-diffusion profile formed during processing of the test structure. Etch-stop selectivity is approximately 10^8.

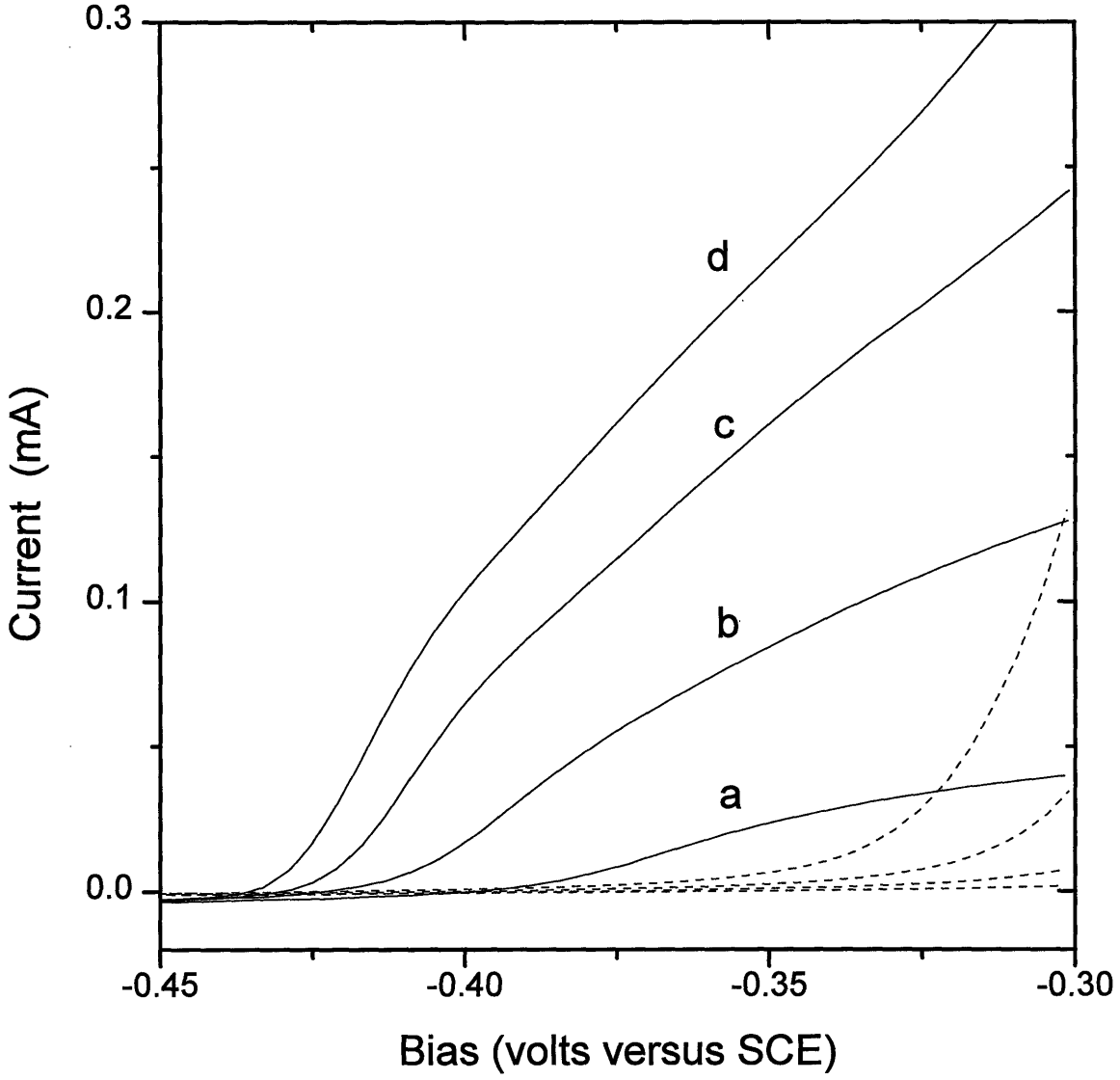


Figure 5.23. Current-voltage characteristics as a function of white light illumination intensity of p-well cantilever beam samples etched in 5% HF using 400mL/min flow rate and 20mV/s sweep rate. a) 32.6mW/cm^2, b) 87mW/cm^2, c) 187mW/cm^2, and d) 490mW/cm^2. The dashed curves were measured away from the p-well and therefore show only the etching current of the top n-Si layer.

becomes substantial at ≈-0.375V (SCE).

Figure 5.24 shows the effect of HF concentration on the p-well sample's I-V characteristics (solid lines) and on the n-layer (dashed lines). Only the p-Si current-voltage characteristics shift cathodically and exhibit more rapidly increasing currents at higher HF concentrations. And finally, the effect of illumination wavelength on the I-V characteristics are presented in figure 5.25, showing that higher energy photons having shallow absorption depths are less efficient for photo-biasing the p-well and generating an anodic current.

Typical current versus etch time measurements for the p-well cantilever beam test structures are plotted in figure 5.26, showing a rapidly decreasing current in the first few minutes as the p-Si surrounding the cantilever beams is removed, followed by a lower current as the p-Si below the beams etches laterally inward. The SEM micrographs in figure 5.27 show successful underetching of the p-well cantilever beams. The lower micrograph shows the cross section of the broken beam (top micrograph) demonstrating the ability to fabricate sub-micron thick structures. The cantilever beams are 1.5mm long and only 0.6μm thick which made it nearly impossible to avoid breakage during handling. Clearly etching did not stop at the n-substrate/p-well junction as expected but rather penetrated into the substrate leaving a rough surface after subsequent porous silicon removal. A high quality etch-stop was obtained, however, at the cantilever beam/p-well junction. Figure 5.28 shows an SEM micrograph of the bottom surface of the broken cantilever beam from figure 5.27 which has been flipped over onto a polished silicon surface. The beam edge shows the high etch-stop quality which has again preserved the fabrication features. The underside is relatively smooth with ≈0.03μm surface feature sizes except at the beam center where the feature size increases to 0.2μm.

The p-Si surrounding the cantilever beams was easily removed, however it was much more difficult to completely underetch the beams. Underetching was not achieved for potentials below -0.4V (SCE), for illumination intensities lower than 0.5W/cm^2, or for HF concentrations below 15%. Figure 5.29 shows a cleaved p-well cantilever beam test structure where only partial underetching was achieved. The etching conditions were identical to those for the sample in figure 5.27 except that 5% rather than 15% HF was used and the potential was slightly more anodic at -0.39 rather than -0.4V (SCE). Unfortunately the choice of etching conditions was also constrained by etching of the n-Si cantilever beams at potentials greater than -0.39V (SCE) for illumination intensities of 0.57W/cm^2, and at even lower potentials for higher intensities.

5.2.3 The p-n-p Etch-Stop

The p-n-p etch-stop was developed as a means for overcoming the problem of hole injection from a p-substrate to an n-Si etch-stop layer which occurs when attempting to selectively etch p-Si versus n-Si. Figure 5.30 shows sequential current voltage sweeps for a continuous n-layer on p-substrate sample which has a doping profile as shown in

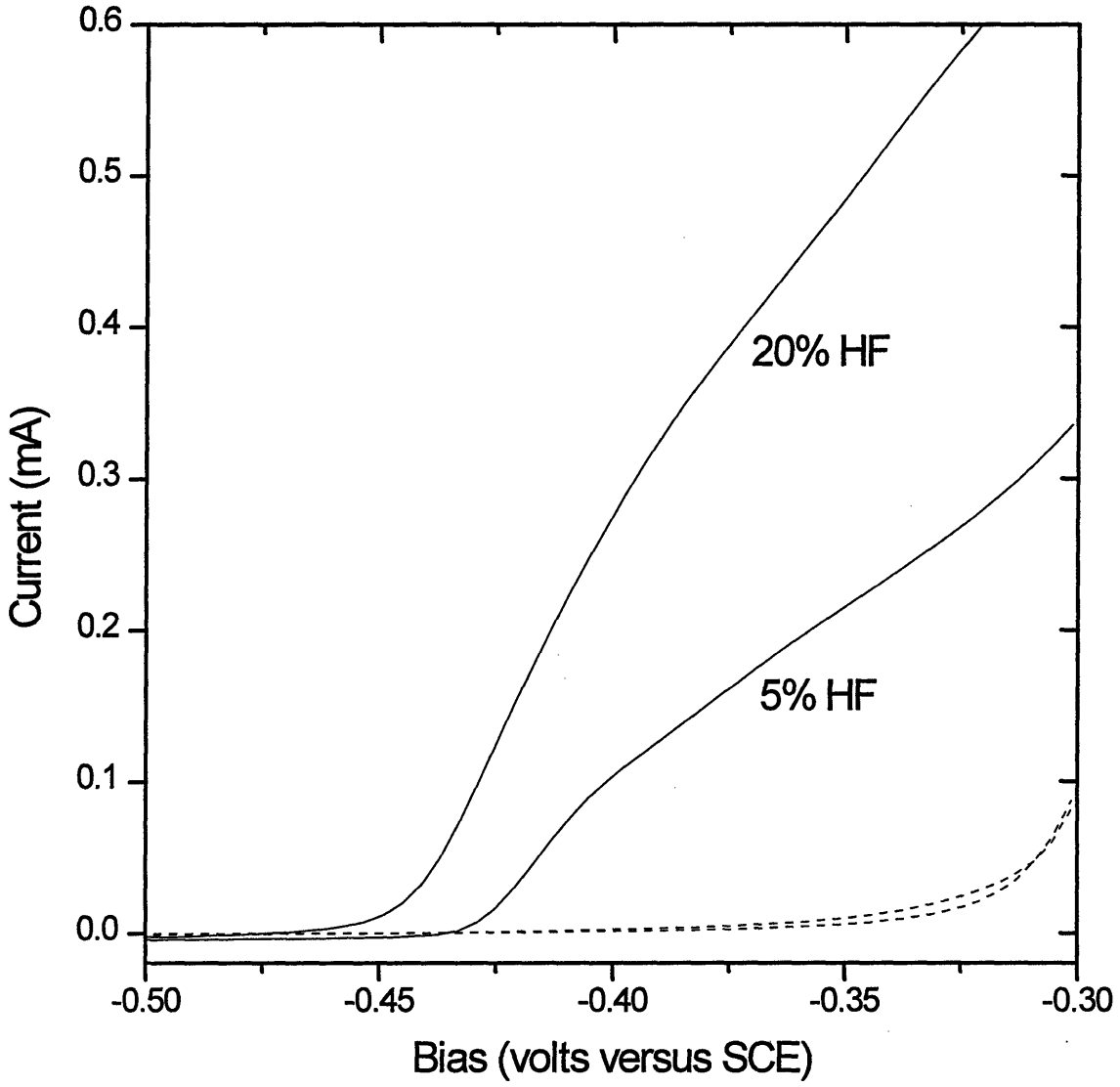


Figure 5.24. Current-voltage characteristics as a function electrolyte HF concentration for etching of p-well cantilever beam samples using 400mL/min flow rate, 20mV/s sweep rate, and 490mW/cm^2 white light illumination intensity (solid curves) and no illumination (dashed curves).

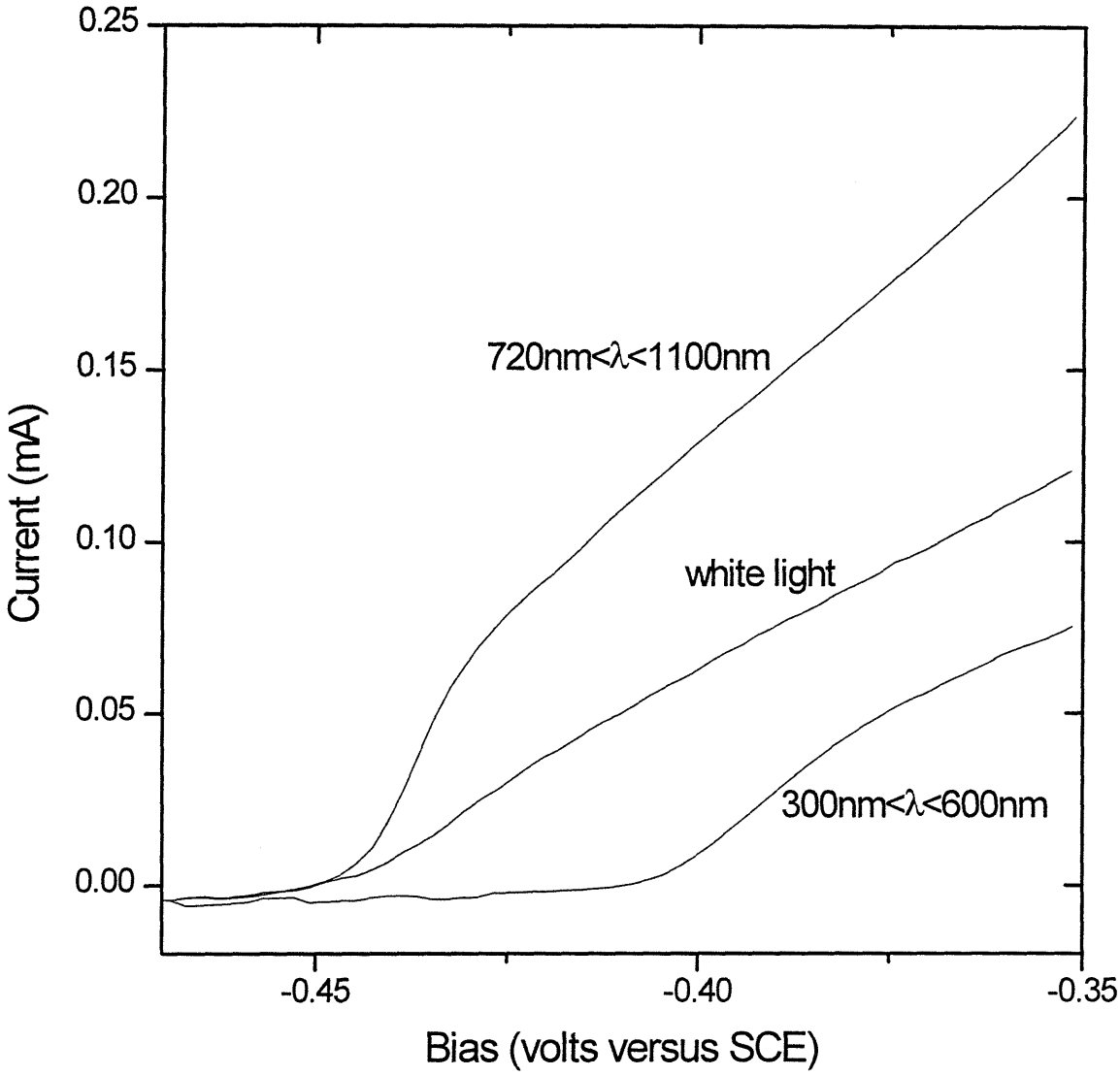


Figure 5.25. Current-voltage characteristics as a function illumination wavelength for etching of p-well cantilever beam samples using 400mL/min flow rate, 20mV/s sweep rate, 5% HF and 87mW/cm^2 illumination intensity at the wavelengths indicated.

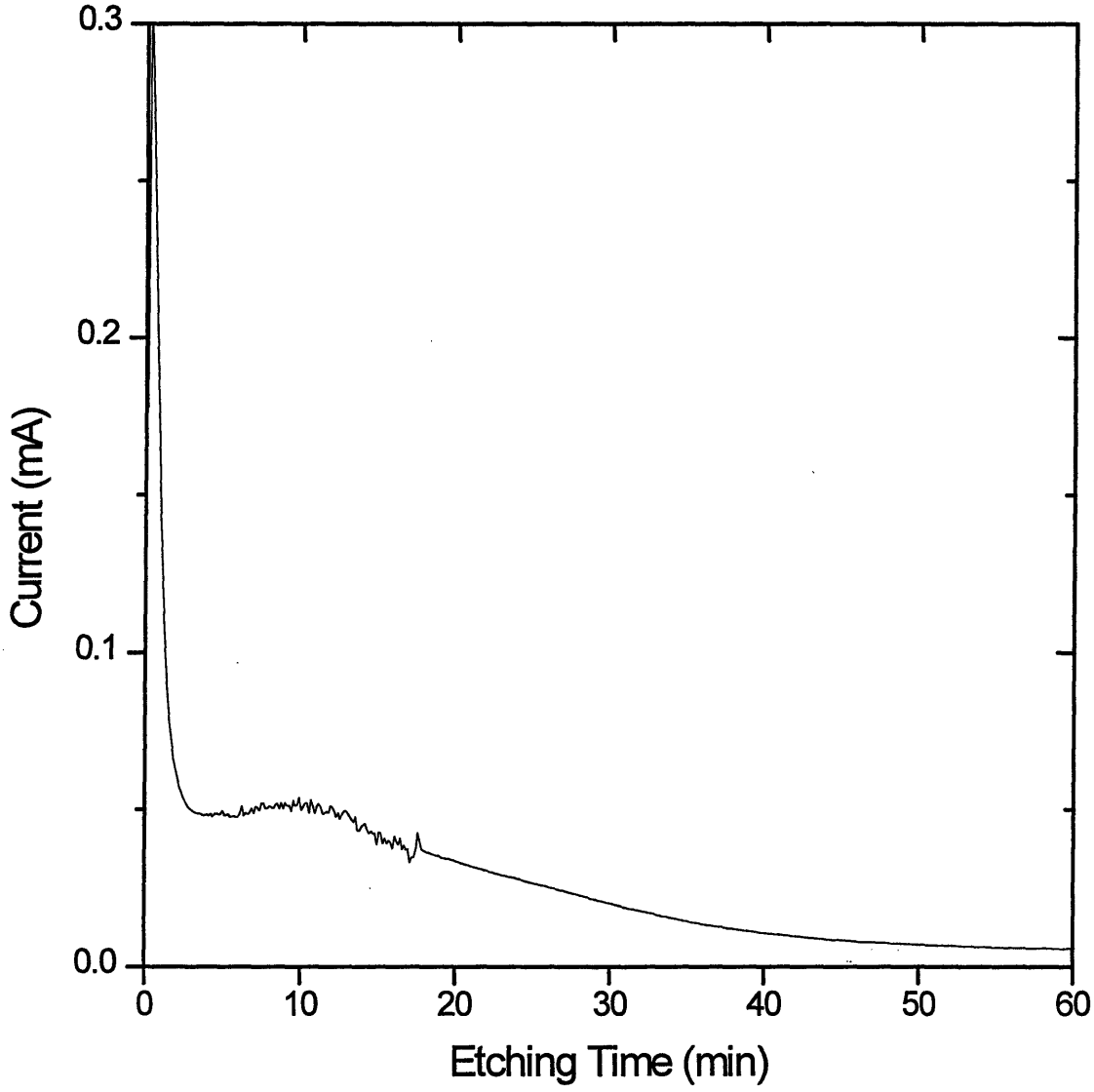


Figure 5.26. Typical measured current as a function of etching time for p-well cantilever beam samples. Etched using -0.4V (SCE), 15% HF, 400mL/min flow rate, and 570mW/cm^2 filtered illumination (λ>600nm).

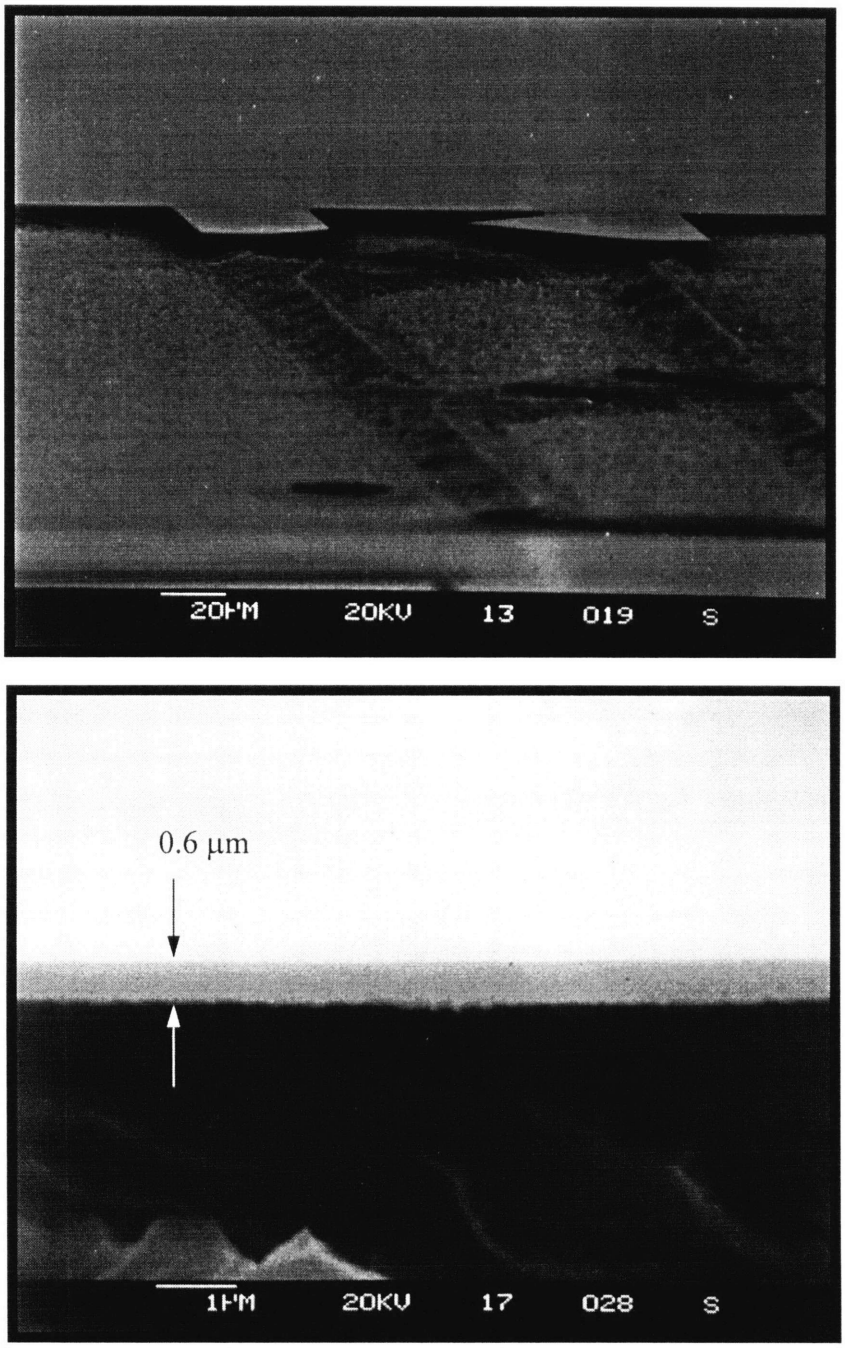


Figure 5.27. SEM micrographs of cleaved p-well cantilever beams etched using -0.4 V (SCE) cell bias, 15% HF, 0.57 W/cm^2 red light illumination, and 60 minutes etching time. The lower micrograph shows an enlargement of the cleaved surface of the broken cantilever beam in the top micrograph, revealing a sub-micron thick p-well etch-stop.

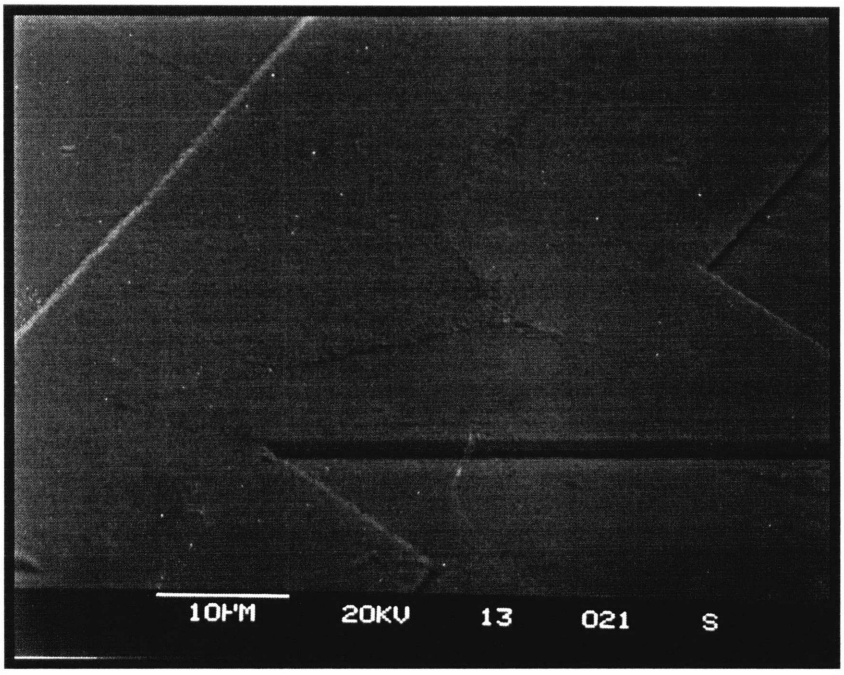


Figure 5.28. SEM micrograph of the underside of the cleaved cantilever beam from figure 5.27. The surface is roughest at the center of the beam with a feature size of ≈0.2μm.

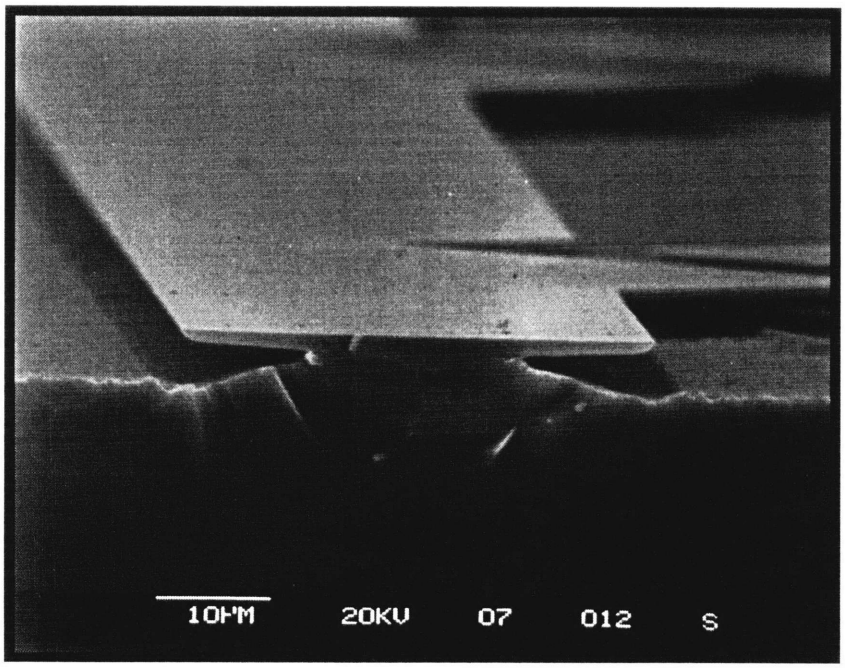


Figure 5.29. SEM micrograph of a cleaved p-well cantilever beams sample after etching using -0.39 V (SCE) cell bias, 5% HF, 0.57 W/cm^2 red light illumination, and 60 minutes etching time.

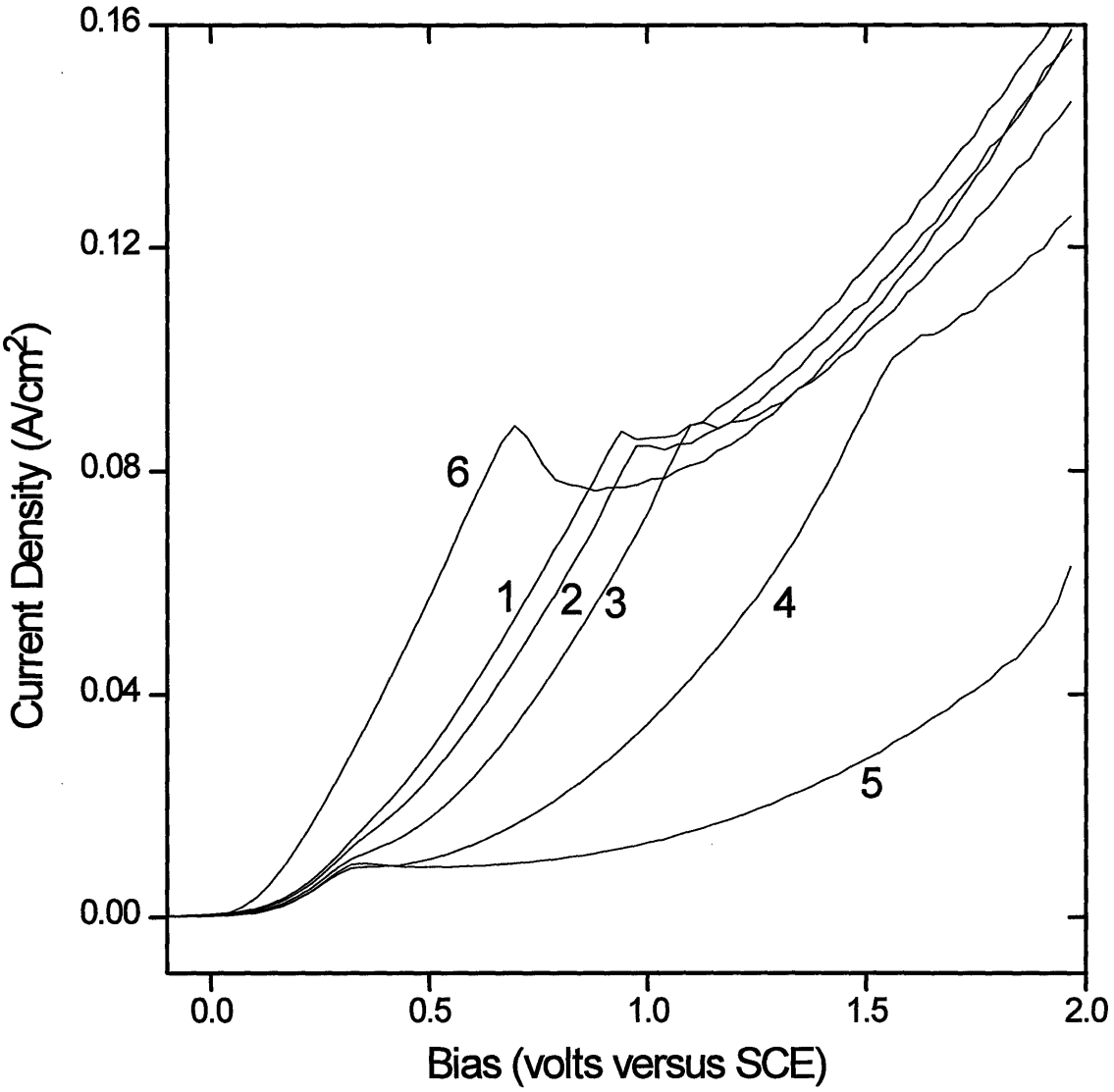


Figure 5.30. Sequential current-voltage sweeps (measured at 100mV/s) on the same n-on-p cantilever beam sample (n/p1). By the sixth sweep the n-layer is completely removed and bulk p-Si current-voltage characteristics are obtained.

figure 4.2(d). The current decreases with each subsequent sweep as the n-layer etches toward the metallurgical junction and N_D decreases. Even then the etch rate remains significant, however, and the characteristic p-Si current-voltage characteristics are observed by the sixth sweep indicating complete n-Si removal.

The p-n-p etch-stop involves placing a capping p-layer over the n-Si layer which introduces a reverse biased junction in the current path. This junction serves to prevent etching of the outer p-layer which in turn prevents etching of the underlying n-layer. Figure 5.31 shows a comparison of the current-voltage characteristics of bulk p-Si and a continuous p-n-p multilayer (with a doping profile given in figure 4.2b), revealing a p-n-p multilayer current density 3 orders of magnitude lower than that of p-Si. Figure 5.32 shows repeated current voltage sweeps from -0.2 to 1.5V (SCE) at 50mV/s on the same p-n-p multilayer sample. At ≈0.75V (SCE) the current of the first 3 sweeps increases after which each subsequent sweep exhibits a larger current even at lower potentials. If however the same experiment is performed with sweeps only to 0.75V (SCE) or below, each subsequent sweep follows the I-V characteristics of the first sweep without any current increase at low potentials. Figure 5.33 shows an SEM micrograph of the sample surface after the repeated sweeps shown in figure 5.32. Tetrahedral pits can be seen on the surface resulting from preferential etching of either stacking faults introduced during ion implantation or dislocations at low angle grain boundaries. Furthermore, a series of concentric rings surrounds some of the pits. These rings were only observed on samples where the repeated sweeps exceeded 0.75V (SCE) , at which point the multilayer begins to etch laterally away from the defect site. Each subsequent sweep therefore has a higher current because of the increased p-Si area exposed to the electrolyte. The decoration of stacking faults and dislocations was determined to begin at ≈0.2V (SCE) corresponding to the increase in current observed in figure 5.31.

Figure 5.34 shows SEM micrographs of the p-n-p multilayer after etching in 5% HF at 0.5V (SCE) for 45 and 10 minutes for the top and bottom micrographs respectively. The lighter areas surrounding each defect site indicate underetching of the p-n-p multilayer. No lateral multilayer etching has occurred even after etching for 45 minutes at 0.5V (SCE). An interesting 4-point pattern is obtained after short etching times which is thought to result from preferential etching of the 4 corners of the stacking faults.

A typical graph of the etching current of p-n-p cantilever beam samples as a function of time is shown in figure 5.35. The rise in current results from the increasing p-substrate/electrolyte interfacial area as both the cantilever beams and the multilayer surrounding the defects become underetched. Figures 5.36 and 5.37 show SEM micrographs of underetched p-n-p multilayer cantilever beams. In both cases the etching time was insufficient to completely underetch the wide beams as seen by the darker region in the middle. The lower micrograph in figure 5.37 shows a cross section of the broken beam edge of the top micrograph. The ability to fabricate sub-micron thick structures having high quality etch-stops is again demonstrated.

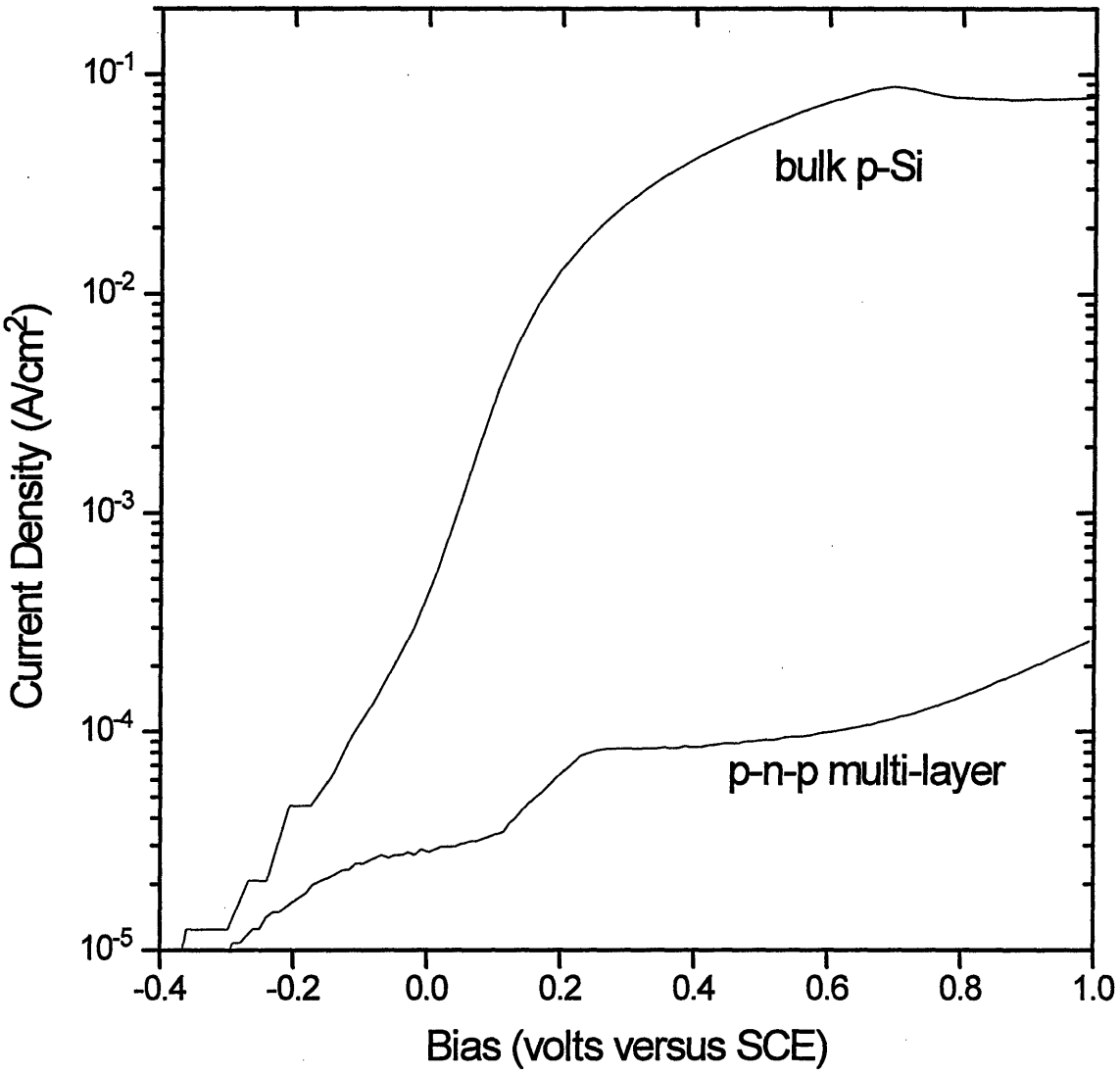


Figure 5.31. Comparison of the current-voltage characteristics of bulk p-Si to those for the p-n-p multilayer of a p-n-p sample.

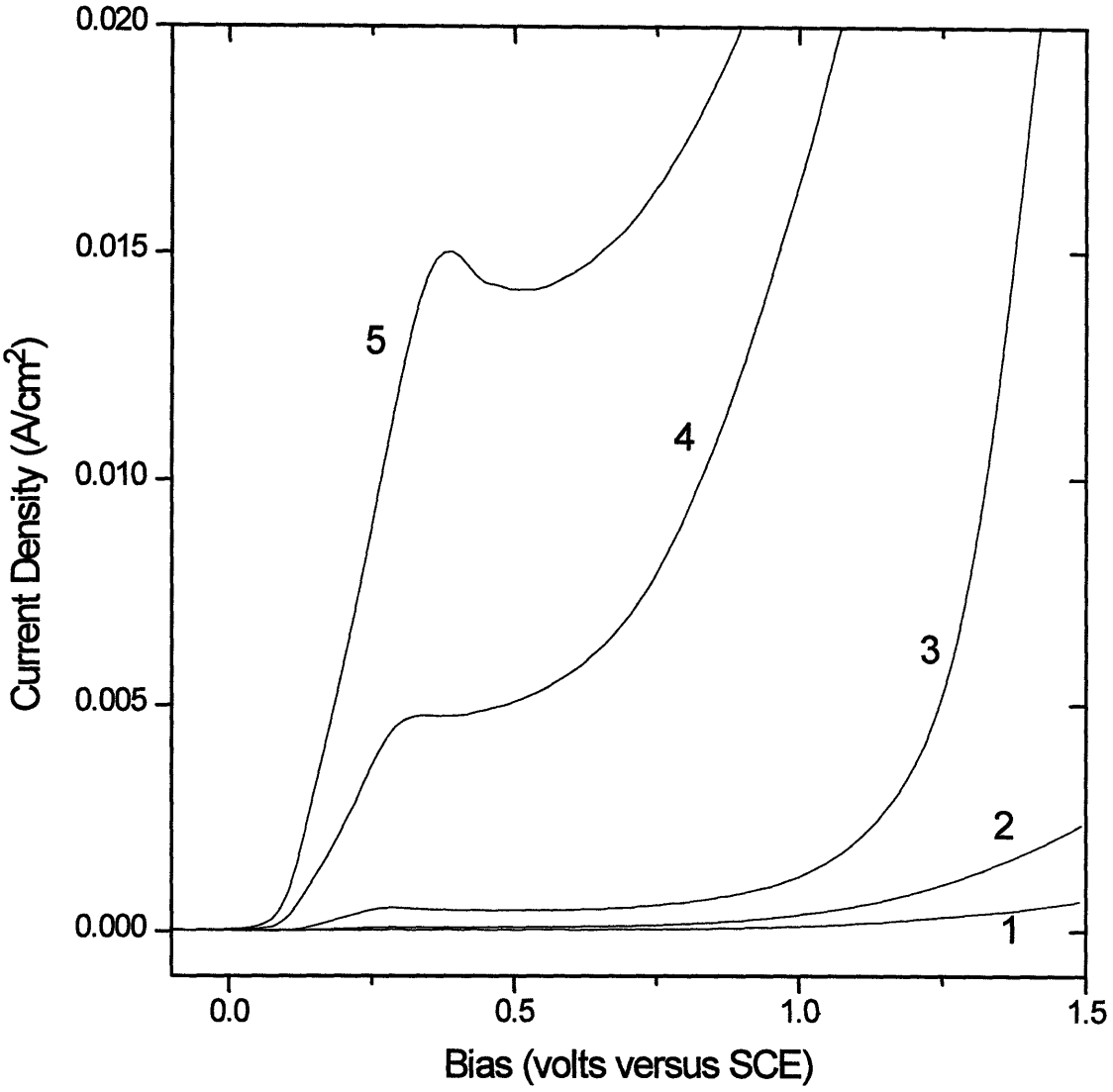


Figure 5.32. Sequential current-voltage sweeps (measured at 50mV/s) on the same p-n-p cantilever beam sample. Above ≈0.7V (SCE) the multi-layer etches laterally away from defects presumed to be stacking faults exposing new p-Si which etches during the subsequent sweep.

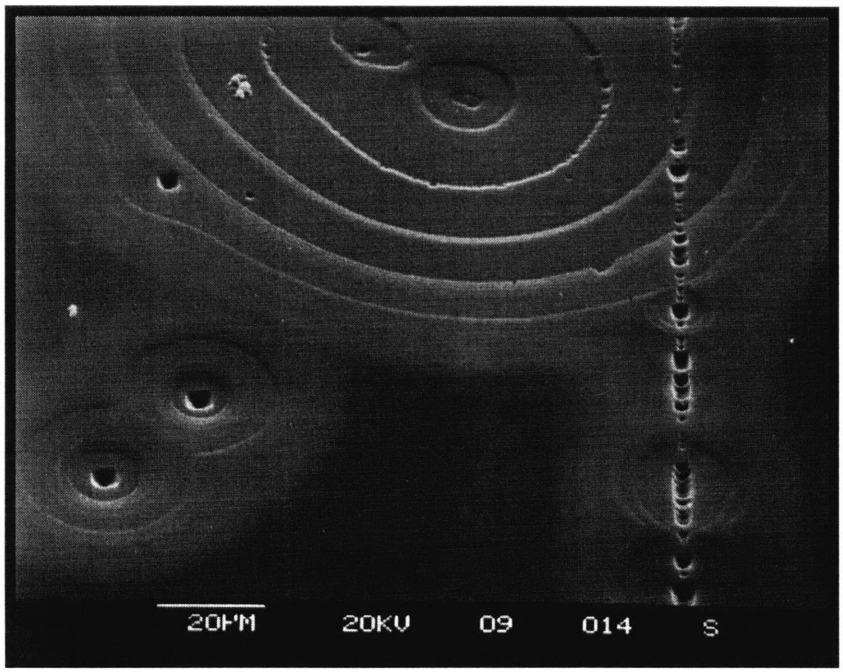


Figure 5.33. SEM micrograph showing lateral p-n-p multi-layer etching at crystallographic defects during sequential potential sweeps from -0.5 to 1.5V (SCE) at 50mV/s in 5% HF.

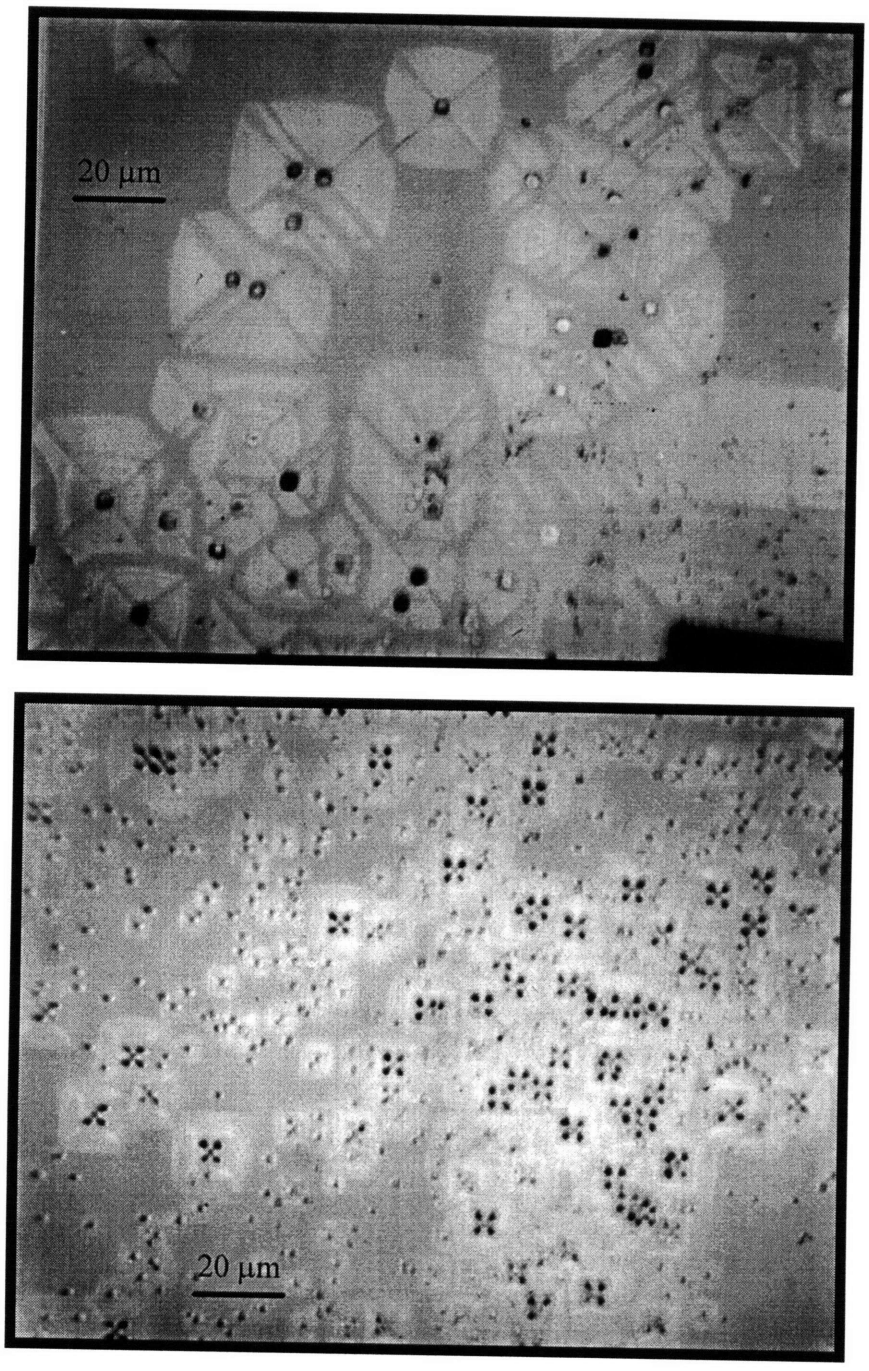


Figure 5.34. SEM micrographs of the p-n-p multi-layer surface after etching at 0.5V (SCE) in 5% HF for (A) 45 minutes and (B) 10 minutes.

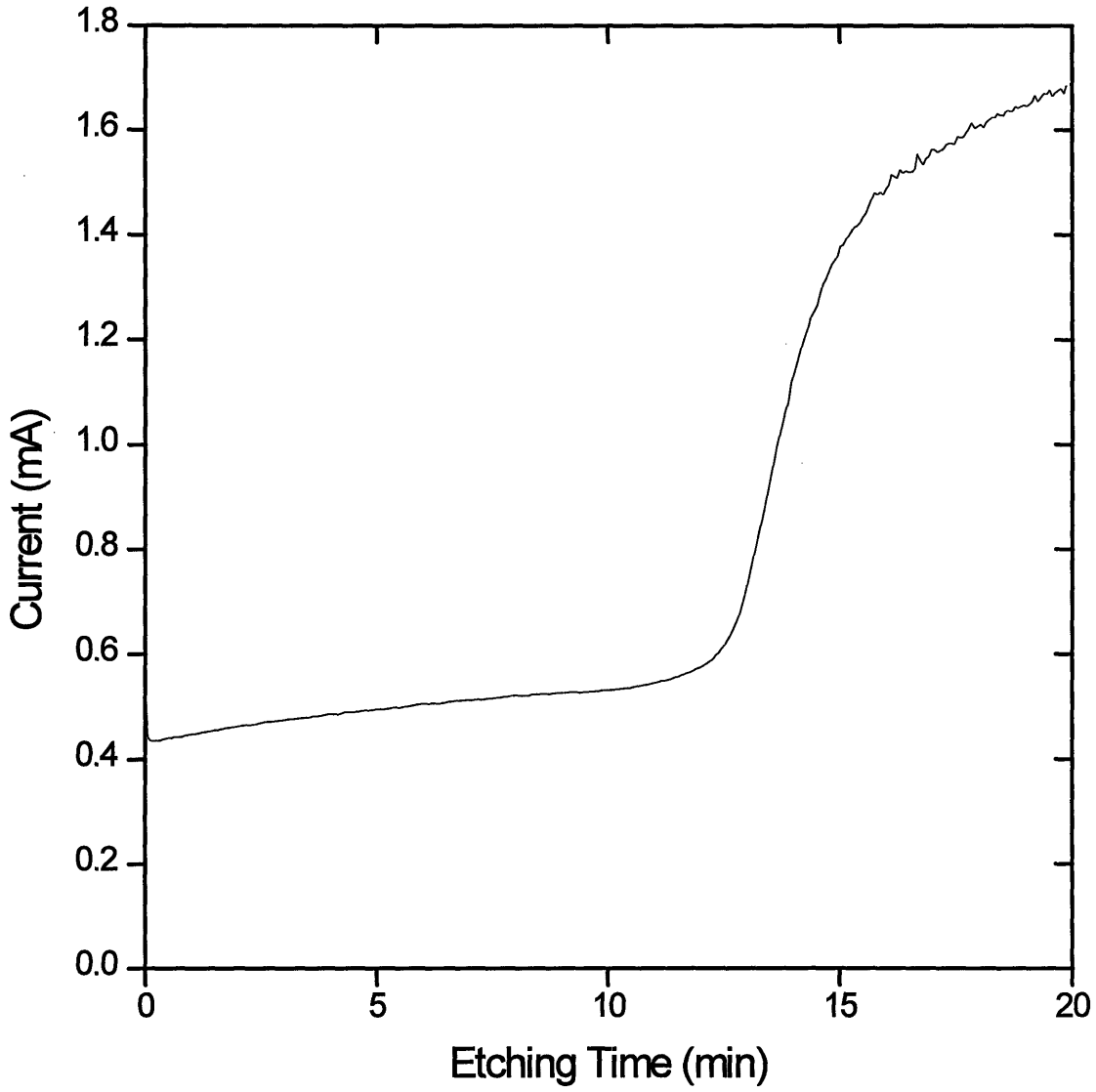


Figure 5.35. Typical measured current as a function of time for etching of p-n-p cantilever beam samples. Etched using 0.3V (SCE), 5% HF, and 400mL/min flow rate.

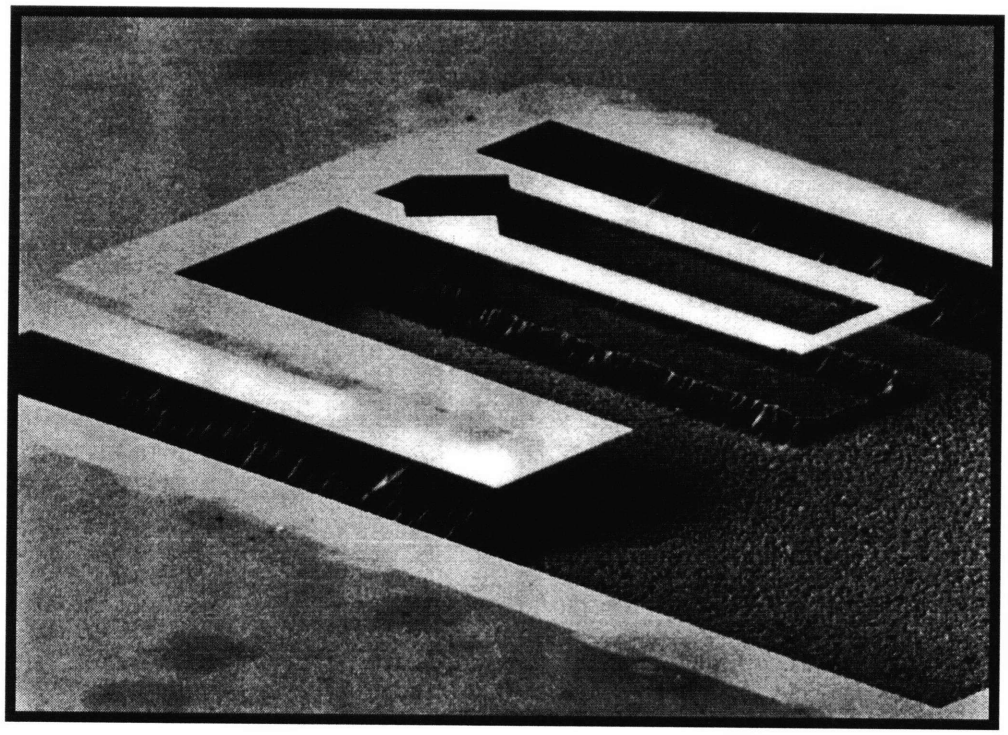


Figure 5.36. SEM micrograph of p-n-p cantilever beams etched using 0.3 V (SCE) cell bias, 5% HF, no illumination, and 60 minutes etching time. Porous silicon, which forms on etched surfaces at these etching parameters, was removed by a 5 second dip in 25 weight percent KOH at room temperature. Beam dimensions are 0.8 x 180 x 700 μm, and the etch pit depth between the cantilever beams is approximately 90 μm.

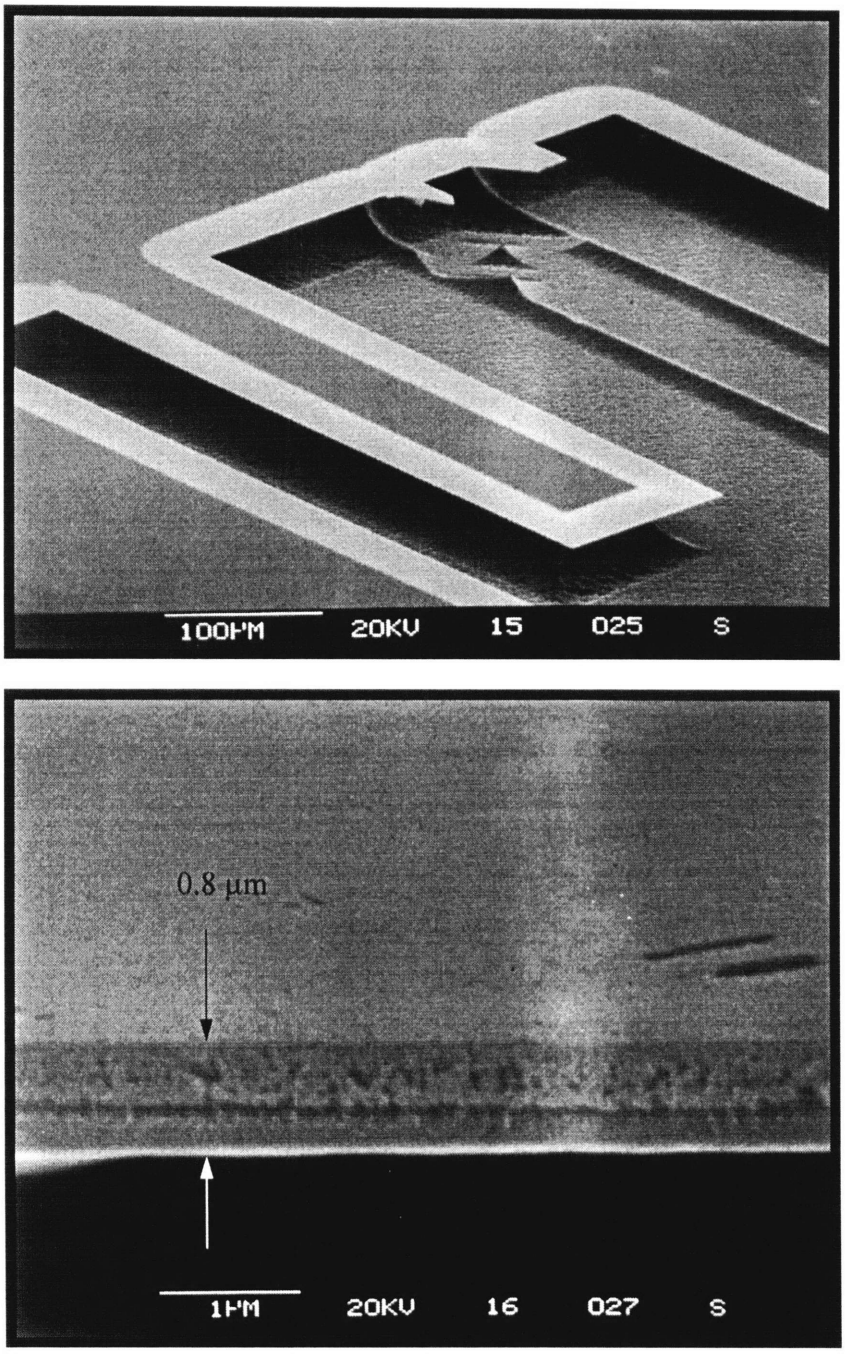


Figure 5.37. SEM micrographs of p-n-p cantilever beams etched using 0.2 V (SCE) cell bias, 15% HF, no illumination, and 20 minutes etching time. The lower micrograph shows an enlargement of the cleaved surface of the broken cantilever beam in the top micrograph, revealing a sub-micron thick p-n-p etch-stop.

5.3 Etching Characteristics of Epi-Layer Samples

In order to investigate the potential and anodic current distributions across etch-stop layers with well defined p-n junction characteristics we prepared five different epi-layer samples with doping profiles of n-on-p, n-on-p^+, p-on-n, p-n-p, and n-p-n as explained in section 4.1.1.

5.3.1 p-Layer on n-Substrate

Figure 5.38 shows the current-voltage characteristics of two p-on-n epi-layer samples. Contrary to our expectations the samples exhibit current densities of 3 or 4 orders of magnitude higher than that across a reverse biased p-n junction. This was determined to result from surface leakage currents at the sample edge where the wafer is diced through the p-n junction. Curve (a) shows how dipping the sample in HF immediately before measuring the current-voltage characteristics reduces the leakage current, presumably by etching some of the heavily damaged surface and hydrogen passivating the surface states. Further evidence for the p-n junction surface leakage current was observed on the surfaces of etched samples which exhibit enhanced p-layer etching at the Teflon seal edge, as shown in figure 5.39. The leakage current injects holes into the p-layer which, being majority carriers, are able to drift or diffuse to the silicon surface exposed to electrolyte.

The p-n junction current-voltage characteristics were measured by applying gallium ohmic contacts to both sides of the epi-layer sample, and are shown by the solid curve in figure 5.40. The dashed lines are p-n junction current-voltage characteristics calculated using equation 5.1 for three values of τ as shown.

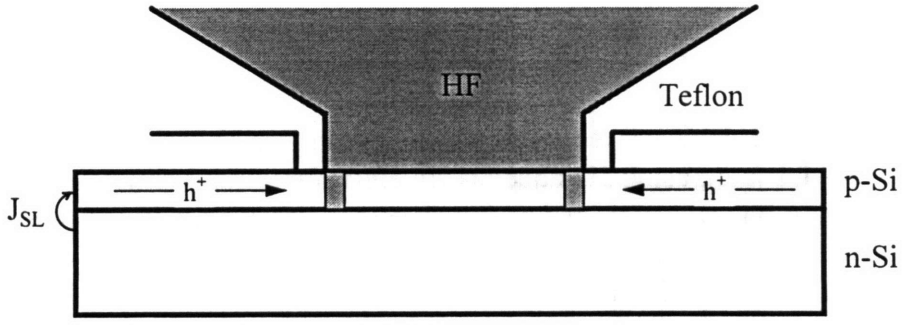


Figure 5.39. Schematic diagram showing enhanced p-layer etching of p-on-n epi-layer samples at the Teflon seal edge.

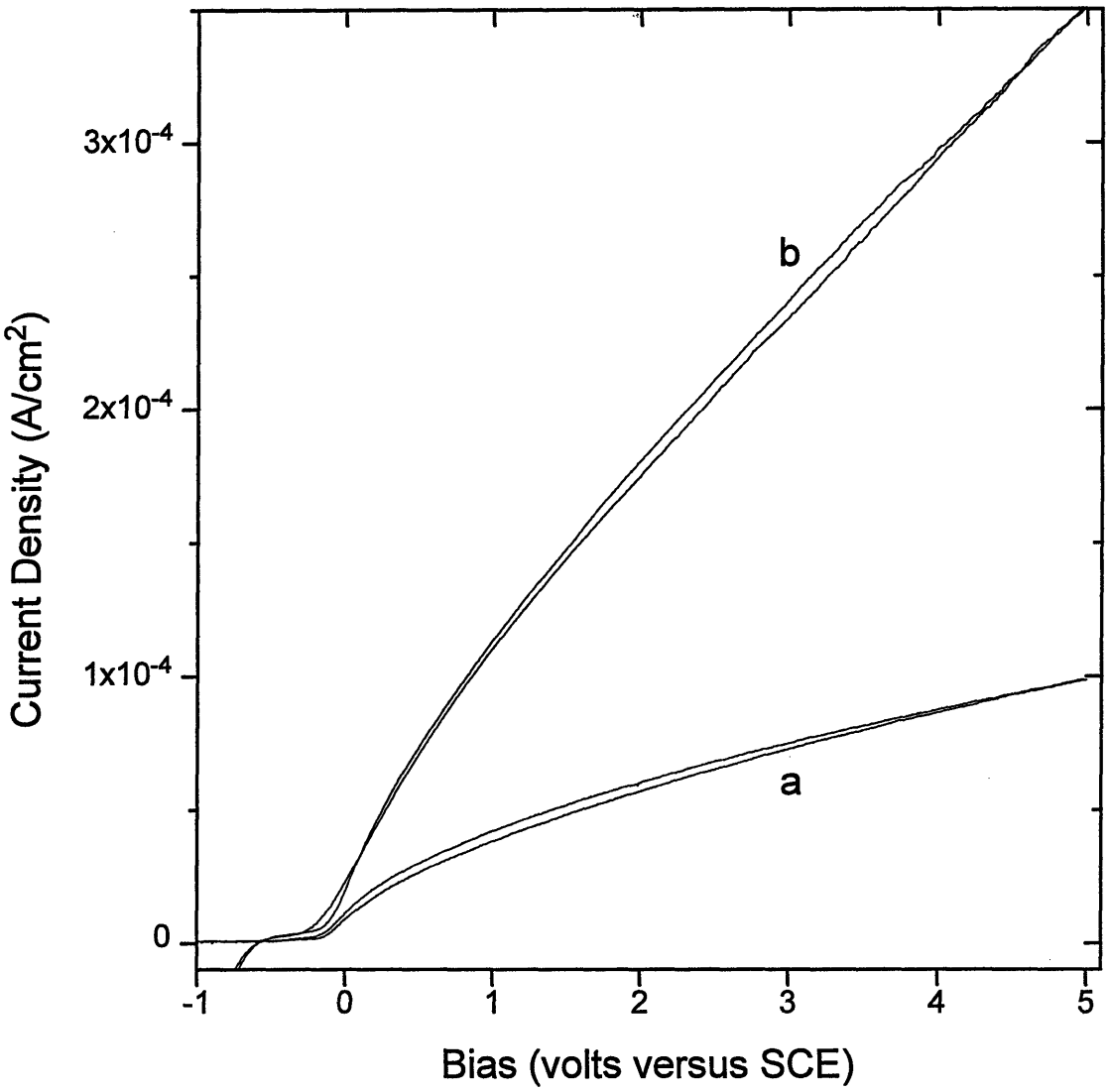


Figure 5.38. Current-voltage sweeps for p-on-n epi samples (2.25μm 5E15 cm^{-3} p-layer on 5Ωcm n-Si substrate), using 5% aqueous HF electrolyte, 20mV/s sweep rate, 600mL/min electrolyte flow rate, and no illumination. Sample (a) shows particularly low p-n junction leakage current, while sample (b) has high leakage which was typical for samples not immersed in HF immediately before etching.

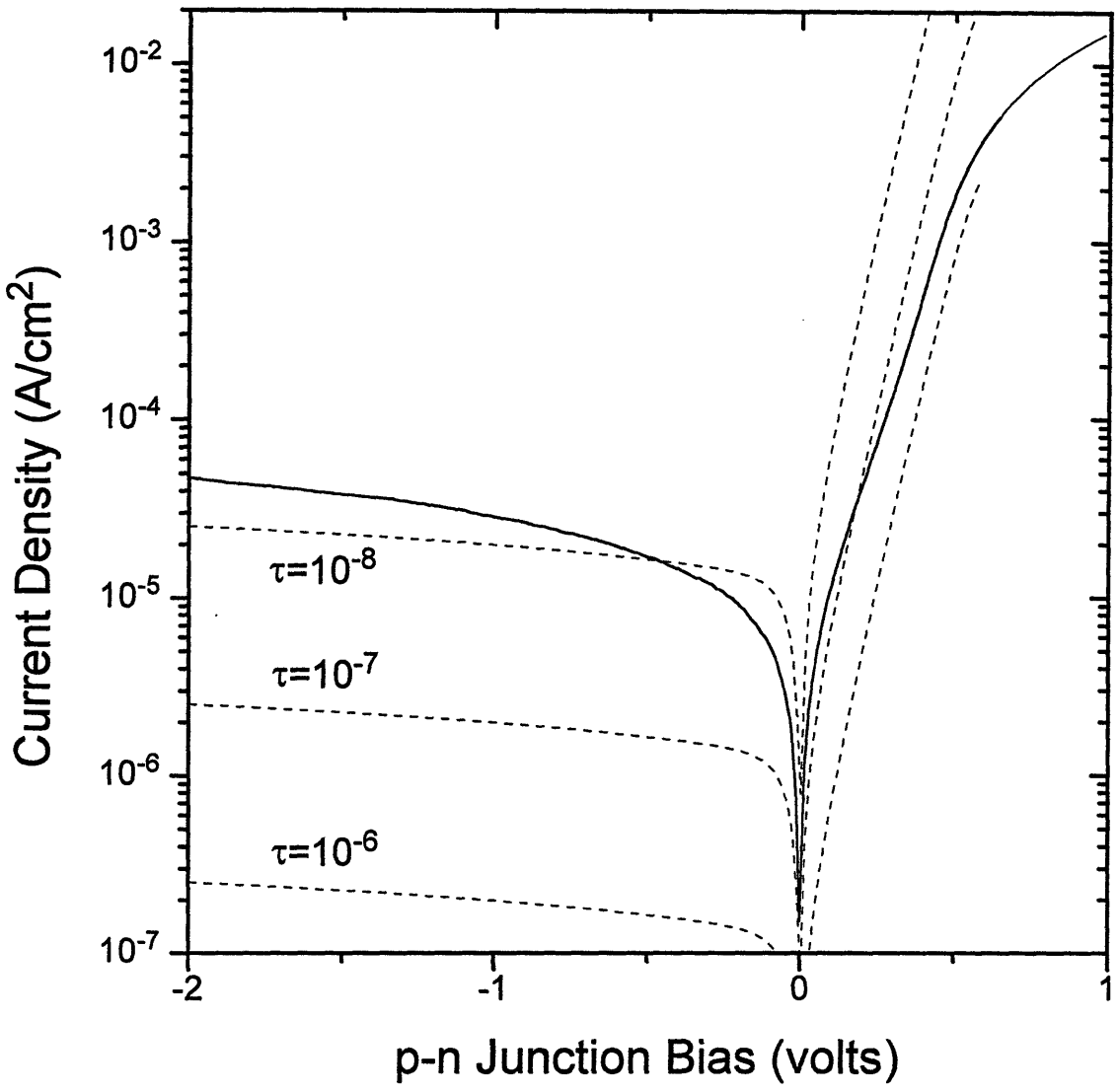


Figure 5.40. Measured current-voltage characteristics (solid line) of the p-n junctions ($N_D = 7x10^{15}cm^{-3}$, $N_A = 5x10^{15}cm^{-3}$) in epi-layer samples. The dashed lines show calculated p-n junction current-voltage characteristics corresponding to equation 5.1 assuming n=2 and τ_e=10^{-6}, 10^{-7}, and 10^{-8} seconds.

$$J = \frac{qn_i W}{\tau}\left[\exp\left(\frac{qV}{2kT}\right) - 1\right] \qquad (5.1)$$

Equation 5.1 assumes generation/recombination currents are dominant over the ideal p-n junction diffusion current as explained in section 3.2. Clearly non-ideal current-voltage characteristics are observed for these p-n junctions with apparently low minority carrier lifetimes of $\approx 10^{-8}$, indicating a high leakage current.

In order to determine the p-layer etch rate the samples were etched at constant biases ranging from 0 to 5V (SCE) in 5% HF for 20 minutes. The etch depth was then measured (away from the more rapidly etched region near the Teflon seal edge) using DEK TAK profilometry. The calculated etch rates as a function of potential are shown by the up-triangles in figure 5.41. The dashed lines represent the bulk p-Si and illuminated n-Si etch rates in 5% HF. The p-layer clearly etches at least three orders of magnitude slower than bulk p-Si as a result of the revere biased p-n junction. We suspect most of this etch rate results from the surface leakage current, and should therefore be significantly lower than 10^{-3} μm/min if the p-n junction did not extend to the diced edge.

5.3.2 n-Layer on p-Substrate

The current-voltage characteristics of the n-on-p (a) and n-on-p^+ (b) epi-layer samples is shown in figure 5.42, for 1, 5, and 15% HF electrolytes. The reader is directed to four important features. First, after the initial current increase at 0V (SCE) a current density plateau is observed over several volts which is virtually independent of increasing potential. Second, after the plateau the current again increases rapidly in a non-reproducible fashion, both with respect to the rate of increase and the bias at which it begins. Third, the plateau current density increases with HF concentration, and finally, the current-voltage characteristics of both the n-on-p and n-on-p^+ samples are nearly identical.

Since silicon has a minority diffusion length much greater than the n-layer thickness, most of the holes injected across the forward biased p-n junction should reach the silicon-electrolyte interface. Therefore, at the cell biases corresponding to the low current density plateaus, the p-n junction forward bias must be small and virtually independent of cell bias. Most of the potential drop must therefore fall across the reverse biased Schottky barrier at the electrolyte interface. This reasoning was verified by measuring the common-base transistor characteristics of the p-n-electrolyte system, where the p-substrate is treated as the emitter, the n-layer the base and the electrolyte the collector. The transistor-like characteristics were measured using 2 potentiostats as shown in figure 4.7, with the first used to supply 0.5V (SCE) to the n-layer (collector-base voltage) and the second to sweep the p-n junction (emitter-base) voltage from -1.5 to 1.0V. Figure 5.43 shows that virtually no n-Si etching (collector-base current) occurs

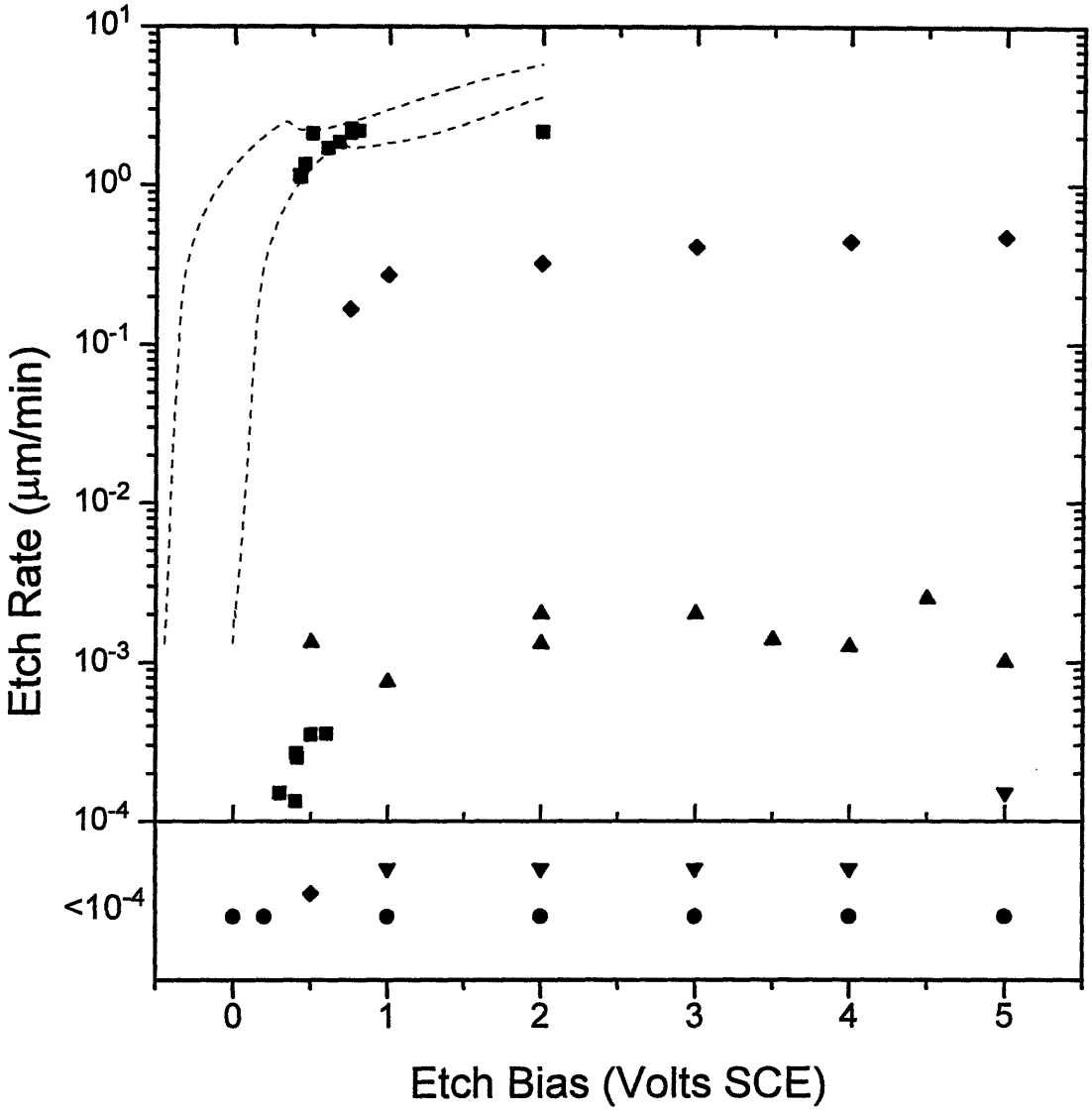


Figure 5.41. Plot of etch rates versus etching bias for epi-layer samples as determined by DEK TAK profilometry. Dashed lines show bulk n- and p-Si etch rates.
( ) n-on-p (◊) n-on-p^+ (Δ) p-on-n (O) p-n-p (∇) n-p-n

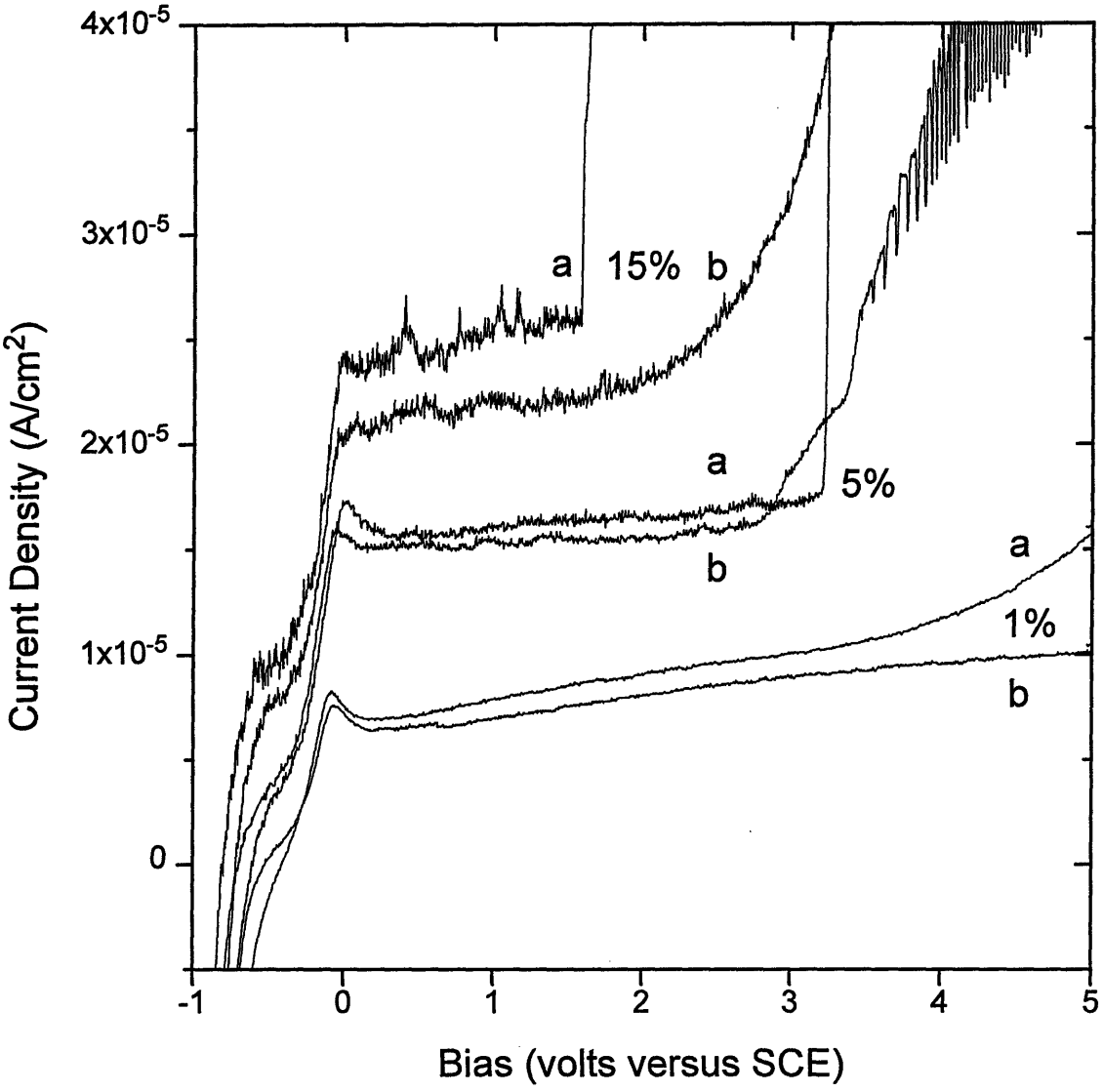


Figure 5.42. Current-voltage sweeps for n-on-p epi samples as measured in 1, 5, and 15% aqueous HF electrolyte, using 20mV/s sweep rate, 600mL/min electrolyte flow rate, and no illumination. a) 2.25μm 7x1015 cm^{-3} n-Si epi-layer on 5Ωcm p-Si substrate, b) 9.2μm 1x1015 cm^{-3} n-Si epi layer on 0.001Ωcm p^{+}-substrate.

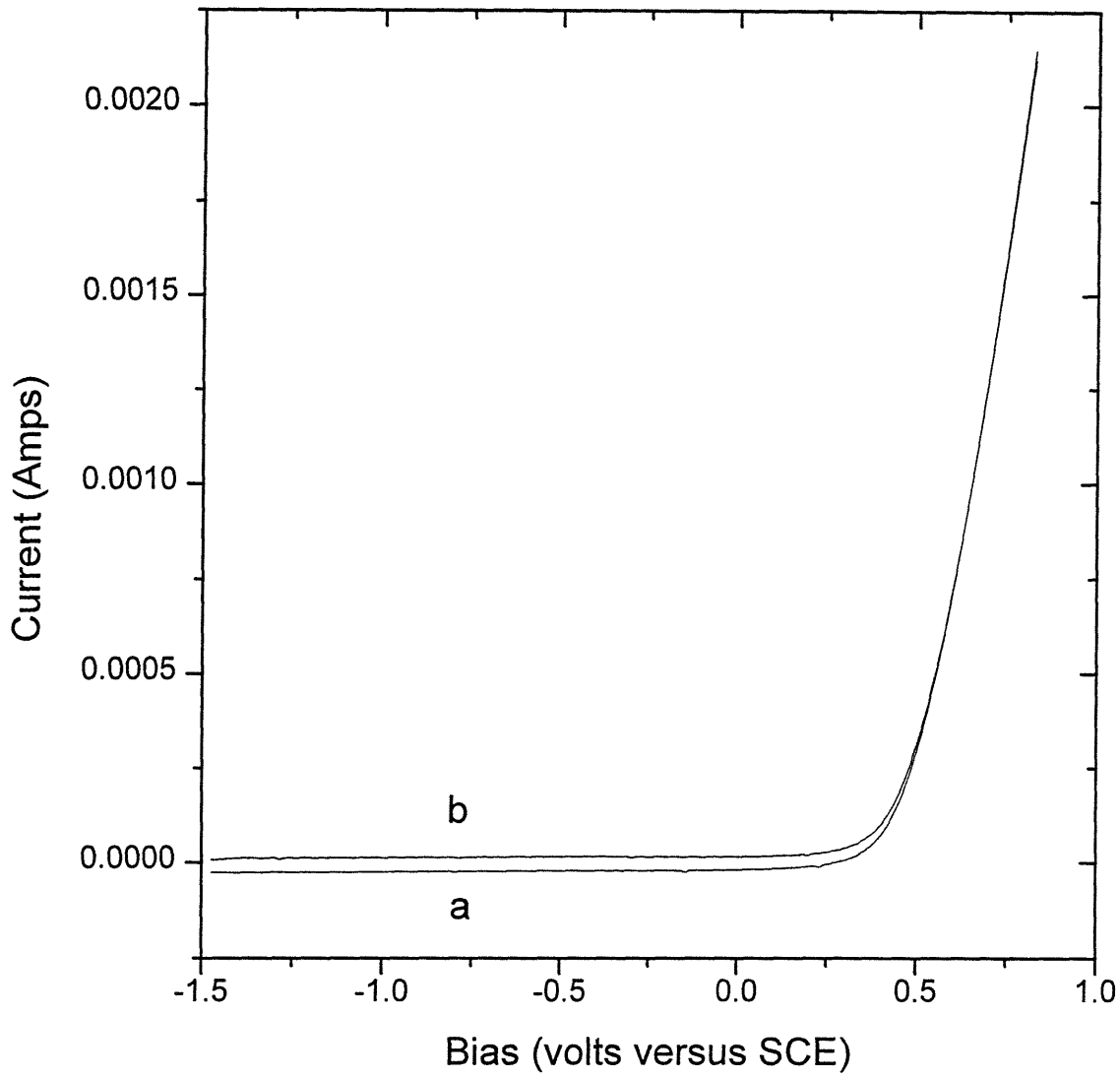


Figure 5.43. A comparison of the (a) p-n junction current to (b) the cell current of a n-on-p epi-layer sample measured in common base mode as the p-n junction bias is swept from -1.5 to 1.0 volts and 0.5V (SCE) is applied to the n-layer.

until holes are injected into the n-layer across the forward biased p-n junction, at which point the n-layer etching current and the and p-n junction current become equal.

The p-n junction forward bias was directly measured as a function of cell bias using a second potentiostat across the p-n junction as shown in figure 4.6 while the cell bias was swept from -1 to 3.6V (SCE). The p-n junction bias is plotted in figure 5.44 curve (c) showing a bias of ≈40mV at cell potentials corresponding to the current density plateau. Curve (b) shows the p-n junction current as calculated using the measured bias and the p-n junction current-voltage characteristics shown previously in figure 5.40. Figure 5.45 shows an enlargement of these characteristics near 0V, with the dashed line representing a best-fit curve to equation 5.2 which has the form of equation 5.1. The best fit parameters J_o and n are $8.068 \times 10^{-6} A/cm^2$ and 3.564 respectively.

$$J = J_o \sqrt{.674 - V} \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] \tag{5.2}$$

Again we see the cell and p-n junction currents have the same dependence on cell bias except for a multiplication factor of 0.74, which is presumably due to the difference in p-n junction and silicon-electrolyte interface areas.

Figure 5.46 shows a more detailed view of the irreproducible current increase after the current density plateau. Curves a, b, and c are again the cell current, the p-n junction current, and the p-n junction voltage. First, notice that the cell current becomes much larger than the p-n junction current. Since hole injection across the p-n junction is the only significant source of holes in the unilluminated n-layer, the excess cell current must result from etching of the p-substrate. Since the cell current density is orders of magnitude lower than that of bulk p-Si, only a small fraction of the silicon-electrolyte interface is exposed to p-Si, indicating that the n-layer has etched down to the p-substrate only at localized points. This is consistent with the highly pitted appearance of these samples after etching. Second, notice that the p-n junction forward bias increases just as p-Si etching begins. Figure 5.48 shows a schematic of the sample cross section where p-Si etching occurs. Assuming little of the applied potential drops in the short-circuiting pore, the applied potential at the exposed p-region must therefore drop across the p-Si electrolyte interface. The distribution of the overall potential drop between the p-n junction and silicon-electrolyte interface therefore becomes perturbed in the vicinity of the p-n-electrolyte triple junction resulting in an increased p-n junction forward bias and subsequently a greater injection current.

The p-n junction leakage current at the diced sample edges was not found to noticeably contribute to n-layer etching. No enhanced etching was observed at the Teflon seal edge, presumably because the distance between the sample edge and the Teflon seal is greater than the minority hole diffusion length.

Figure 5.47 shows the cell current , p-n junction bias and calculated p-n junction current for the n-on-p^+ epi-layer sample. The current-voltage characteristics and potential

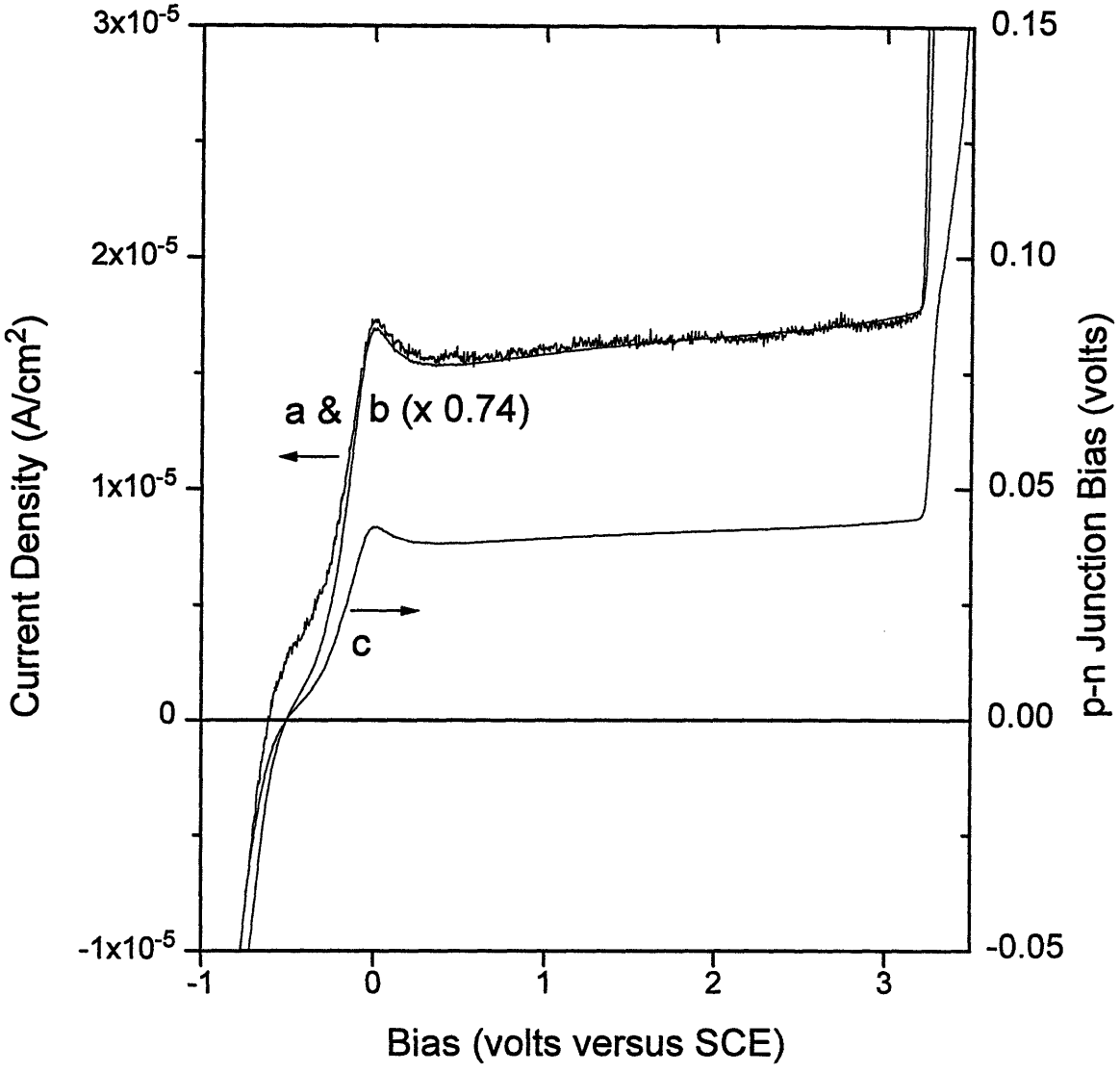


Figure 5.44. Simultaneous measurements of the (a) electrochemical cell current across an n-on-p epi-layer sample and (c) the bias across the p-n junction. Curve (b) is the current across the p-n junction as calculated using curve (c) and the measured p-n junction current-voltage characteristics shown in figure 5.53 and 5.54.

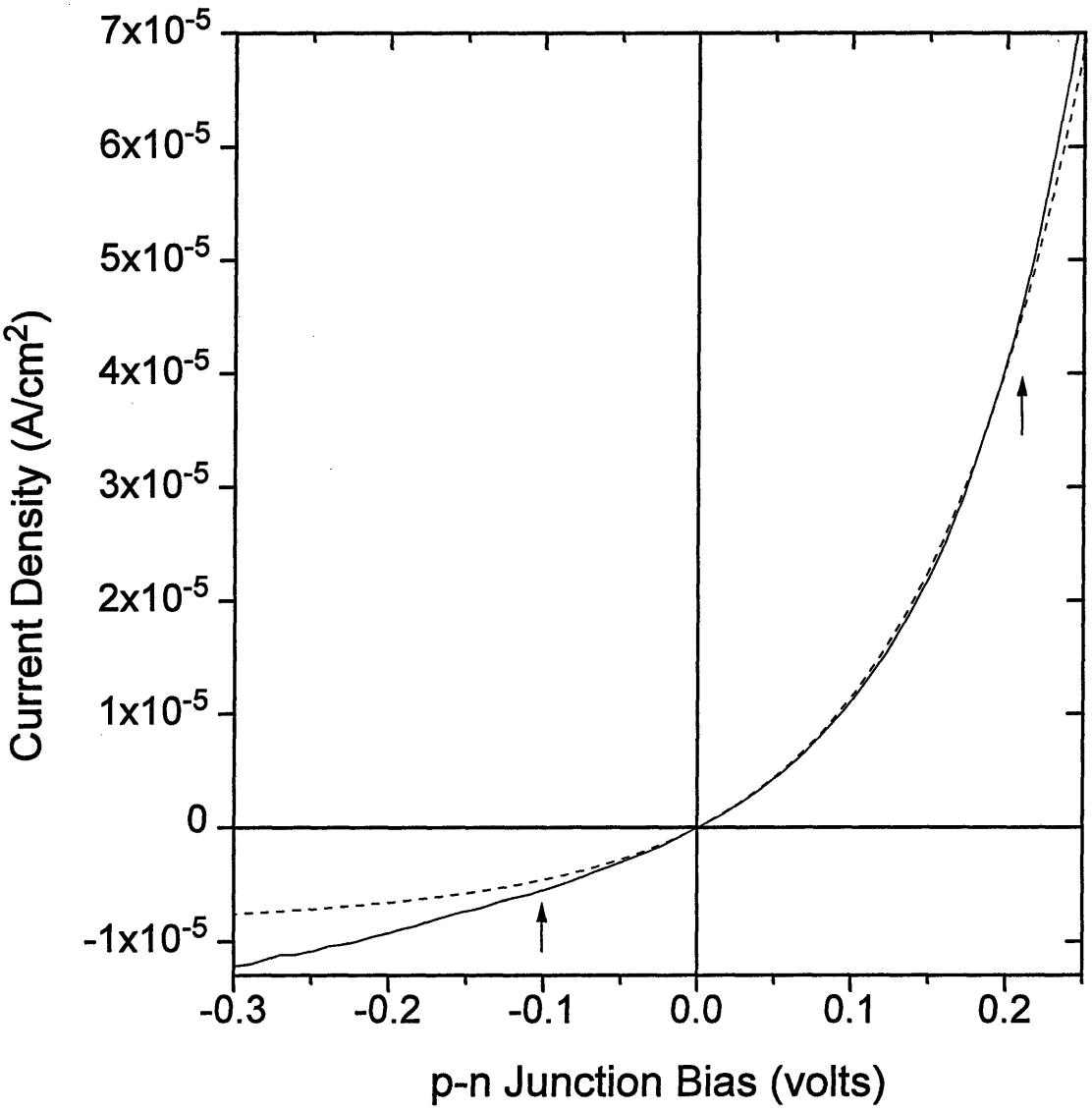


Figure 5.45. Measured current-voltage characteristics (solid line) of the p-n junctions ($N_D = 7x10^{15}cm^{-3}$, $N_A = 5x10^{15}cm^{-3}$) in the epi-layer samples. The dashed line shows the calculated best fit curve corresponding to equation 5.2, and the arrows indicate the data range used for curve fitting.

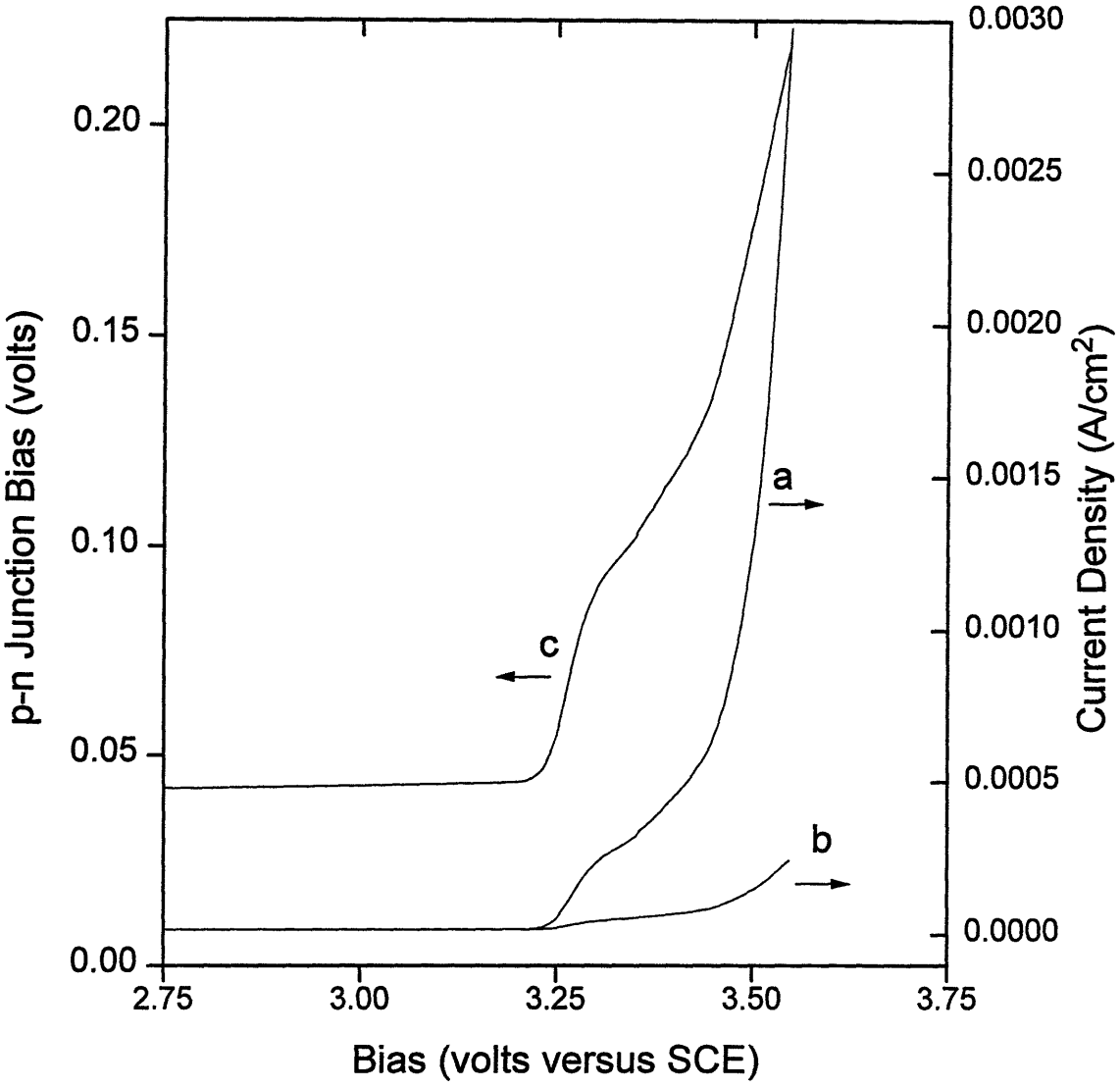


Figure 5.46. An enlargement of figure 5.42 in the vicinity of 3.25V (SCE) showing the relationship between the electrochemical cell current across an n-on-p epi-layer sample (a), the bias across the p-n junction (c), and the calculated current across the p-n junction (b) during n-on-p etch-stop failure.

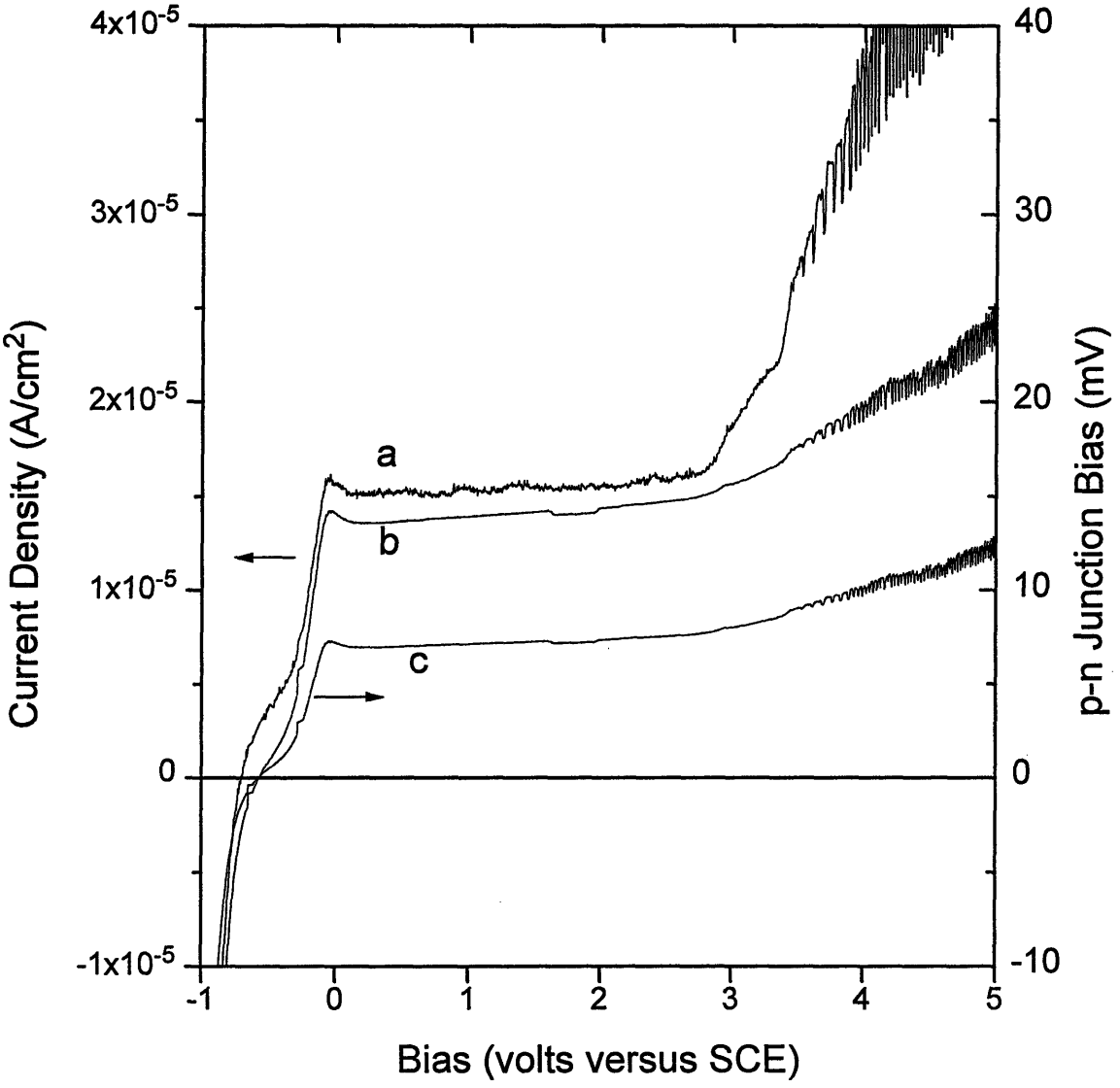


Figure 5.47. Simultaneous measurements of the electrochemical cell current across an n-on-p^+ epi-layer sample (a) and the bias across the p-n junction (c). Curve (b) is the current across the p-n junction as calculated using curve (c) and the measured p-n junction current-voltage characteristics.

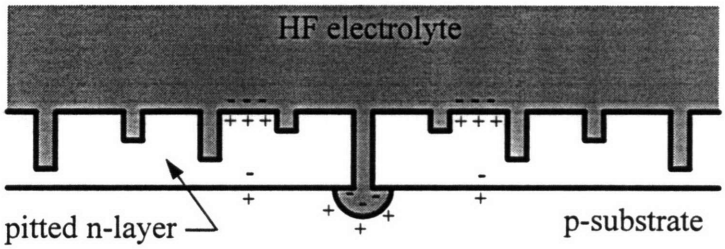


Figure 5.48. Schematic diagram of a cross section of the n-Si epi-layer on p-substrate sample showing localized p-Si etching and the potential drops at the interfaces.

distributions are very similar to those of the p-on-n sample, except for potentials above the current plateau where the current is found to increase less rapidly.

The etch rate of the n-Si epi-layer on p-substrate samples were again measured using DEK TAK profilometry. Figures 5.49 and 5.50 show the etching currents as a function of time for these experiments, revealing two distinctly different characteristics. At low etching potentials the current densities were $\approx 2 \times 10^{-5}$ A/cm^2 for several minutes, after which the n-layer degraded resulting in a approximately linear current density increase with time. The degraded surfaces were pitted which is consistent with the localized p-Si etching as discussed earlier. The time before degradation decreases with increasing bias. Samples etched at higher biases immediately exhibited high current densities characteristic of bulk n-Si etching when hole supply is not rate limiting. In this case the n-layer etched away after approximately one minute at which point the current density changed to that characteristic for bulk p-Si etching. Clearly at higher potentials an adequate p-n junction forward bias must exist to supply approximately 0.1A/cm^2 anodic current to the n-layer. In section 3.3.2 we explain that the rate of electron generation in the n-layer limits the electron current across the p-n junction, which in turn limits the p-n junction forward bias according to equation 3.54, which in turn limits the hole injection rate according to equation 3.53. We attribute the high currents and rapid electron generation of the samples etched at high biased to field enhanced breakdown at pore tips which form at the silicon-electrolyte interface. Figure 5.49 reveals a high charging current at very short times which, probably due to an accompanying voltage spike, initiates breakdown at the pore tips which is then sustained at low voltages. Other explanations do not seem consistent with the data in figures 5.42, 5.44, and 5.46 which show that when voltage is gradually increased, the very high current densities of figure 5.50 are not obtained even up to 3.55V (SCE).

Figure 5.51 shows the same etch rate experiments for the n-on-p$^+$ samples. The rapid n-layer etching at short times is not observed even at a bias of 5V (SCE). Instead we see the low $\approx 2 \times 10^{-5}$ A/cm^2 initial current density followed by n-layer degradation as for the n-on-p samples etched at low potentials. Figure 5.41 shows the measured etch

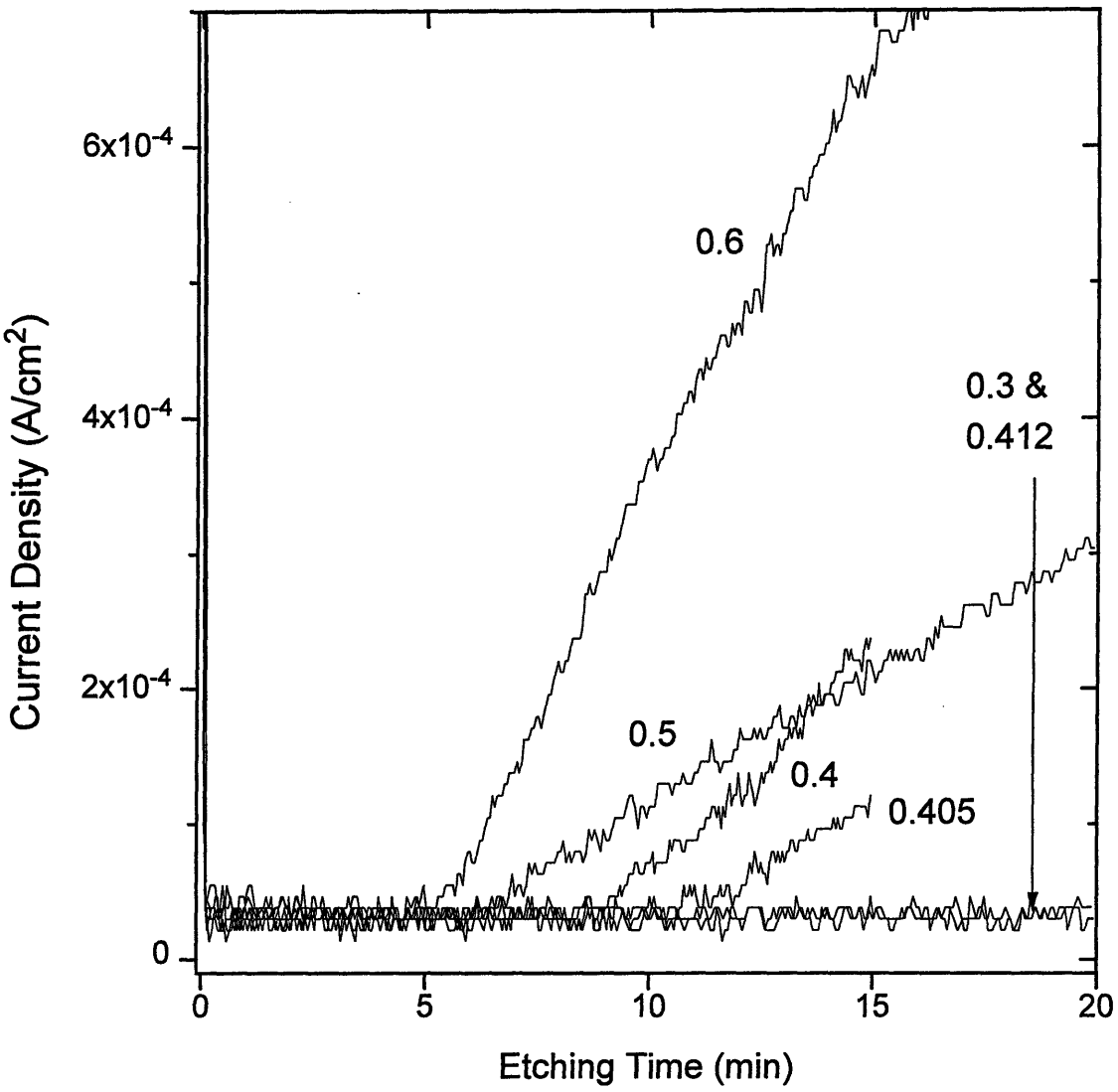


Figure 5.49. Current density as a function of etch time for epi n-on-p samples etched at various biases (SCE), using 5% HF, 600 mL/min electrolyte flow rate, and no illumination.

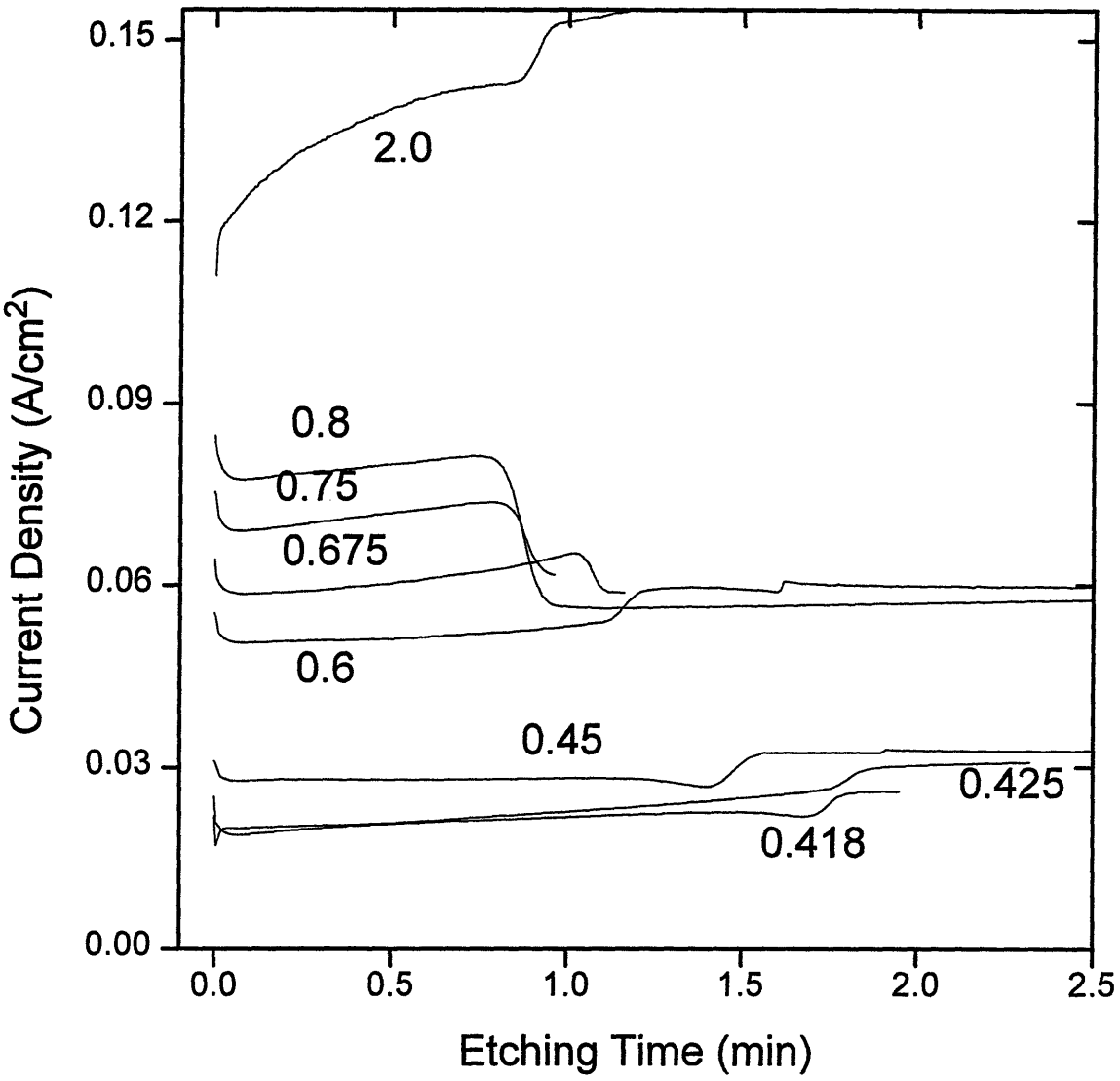


Figure 5.50. Current density as a function of etch time for epi n-on-p samples etched at various biases (SCE), using 5% HF, 600 mL/min electrolyte flow rate, and no illumination.

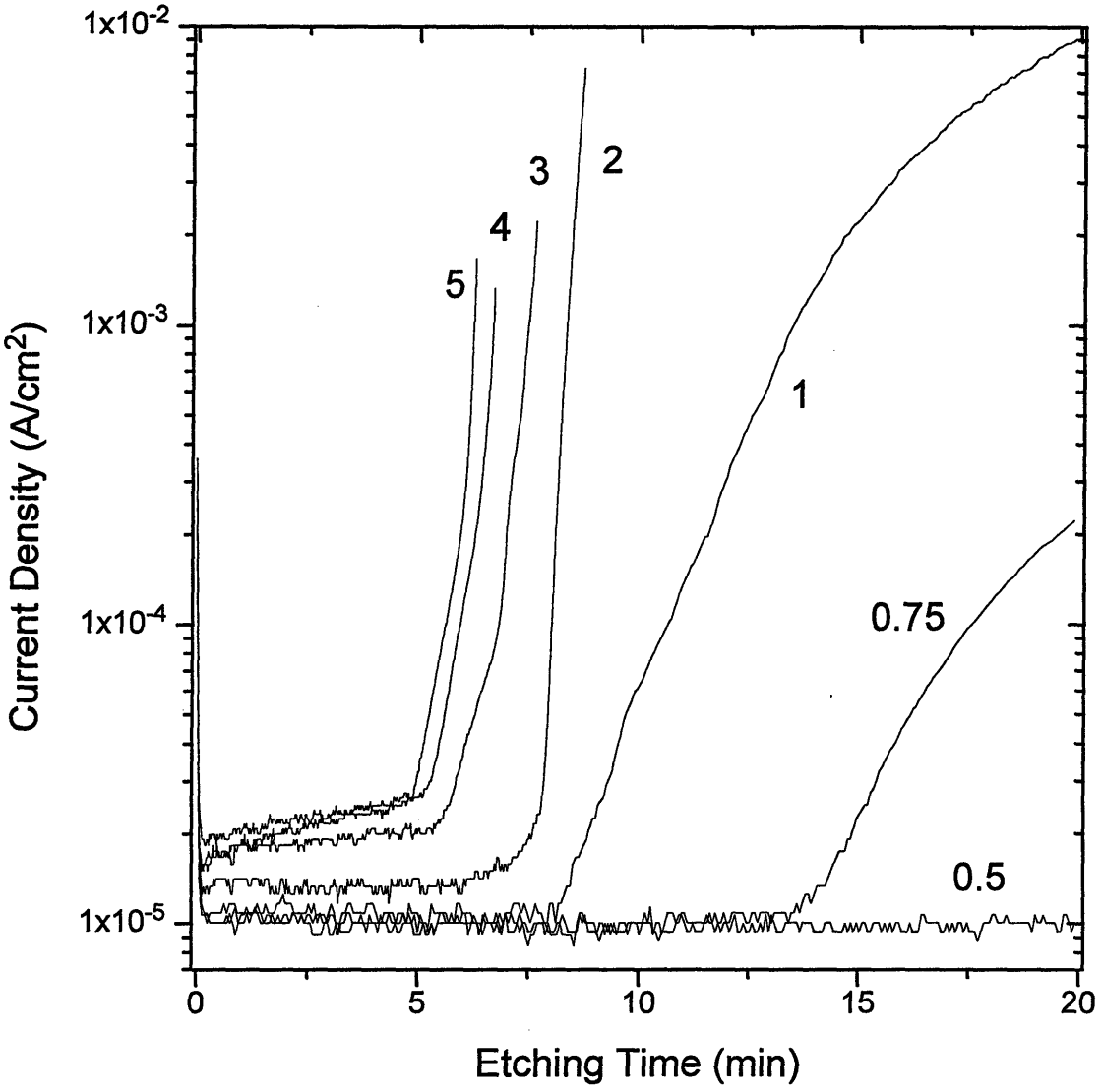


Figure 5.51. Current density as a function of etch time for 9.2μm 1x1015 cm^{-3} n-Si epi layer on 0.001Ωcm p^{+}-substrate samples etched at various biases, using 5% HF, 600 mL/min electrolyte flow rate, and no illumination.

rates of the n-on-p (square symbols) and n-on-p^+ (diamond symbols) samples. It is important to note that the effective etch rate is even more rapid than shown due to pore penetration into the n-layer which was not detected by the 12.5μm diameter DEK TAK stylus.

5.3.3 p-n-p Multilayer

The current-voltage characteristics of p-n-p epi-layer samples are shown in figure 5.52. p-n junction surface leakage again significantly contributes to the anodic current resulting in enhanced p-layer etching at the Teflon seal edge. Curve (a) shows the current-voltage characteristics of a sample immediately after it was dipped in HF to passivate the surface states, while curve (b) shows the characteristics of a sample not dipped in HF. Curve (a) shows two current density plateaus of $7x10^{-6}$ and $2.7x10^{-5}$ A/cm^2 which are separated by a rapid current increase at ≈3V (SCE). Most of the overall potential drop again falls across a reverse biased p-n junction as observed for the p-layer on n-substrate epi-layer samples as is evident by the similar square root current-voltage dependence at low potentials.

The potential drop across the two p-n junctions was measured as a function of cell potential using a potentiostat connected between the p-layer and the p-substrate in a similar fashion as was done for the n-on-p samples. The sum of the p-n junction potentials is plotted in figure 5.53 (b) showing an increase over potentials corresponding to the first current density plateau but not the second. Curve (c) is the fraction of the overall potential drop between the p-substrate and electrolyte that falls across the p-layer/electrolyte interface Schottky barrier. Assuming that 1) the built-in potentials of the two p-n junctions ($V_{bi(r)}$ and $V_{bi(f)}$) are equal and opposite, 2) the built-in potential of the p-Si electrolyte Schottky barrier ($V_{bi(SCR)}$) equals 0.75V (equation 3.56), and 3) C-V_H =0.35V (equation 3.54), the fraction of the overall potential drop which falls across the Schottky barrier (V_{SCR}) can be written as: (see section 3.3.3)

$$V_{SCR} = V_a + 0.4 + (V_{pn(r)} - V_{pn(f)}) \tag{5.3}$$

where V_a is the cell potential, and ($V_{pn(r)}$ - $V_{pn(f)}$) is the sum of the potential drops across the p-n junctions given by curve (b). V_{SCR} is plotted as a function of cell potential in figure 5.53 (c). Thus we see that except for ≈0.4V all of the potential drop falls across the reverse biased p-n junction during the first current plateau, after which all further increases in potential drop fall across the silicon-electrolyte interface. In other words, the p-n-p multilayer initially behaves like a p-on-n sample until the second plateau, where it reverts to the behavior of a n-on-p sample. We believe that the rise between the two plateaus is a consequence of depletion layer punch-through of the thin 0.75μm p-layer. Assuming V_{SCR}=0.4V as determined from figure 5.53 (c), the depletion layer width at the

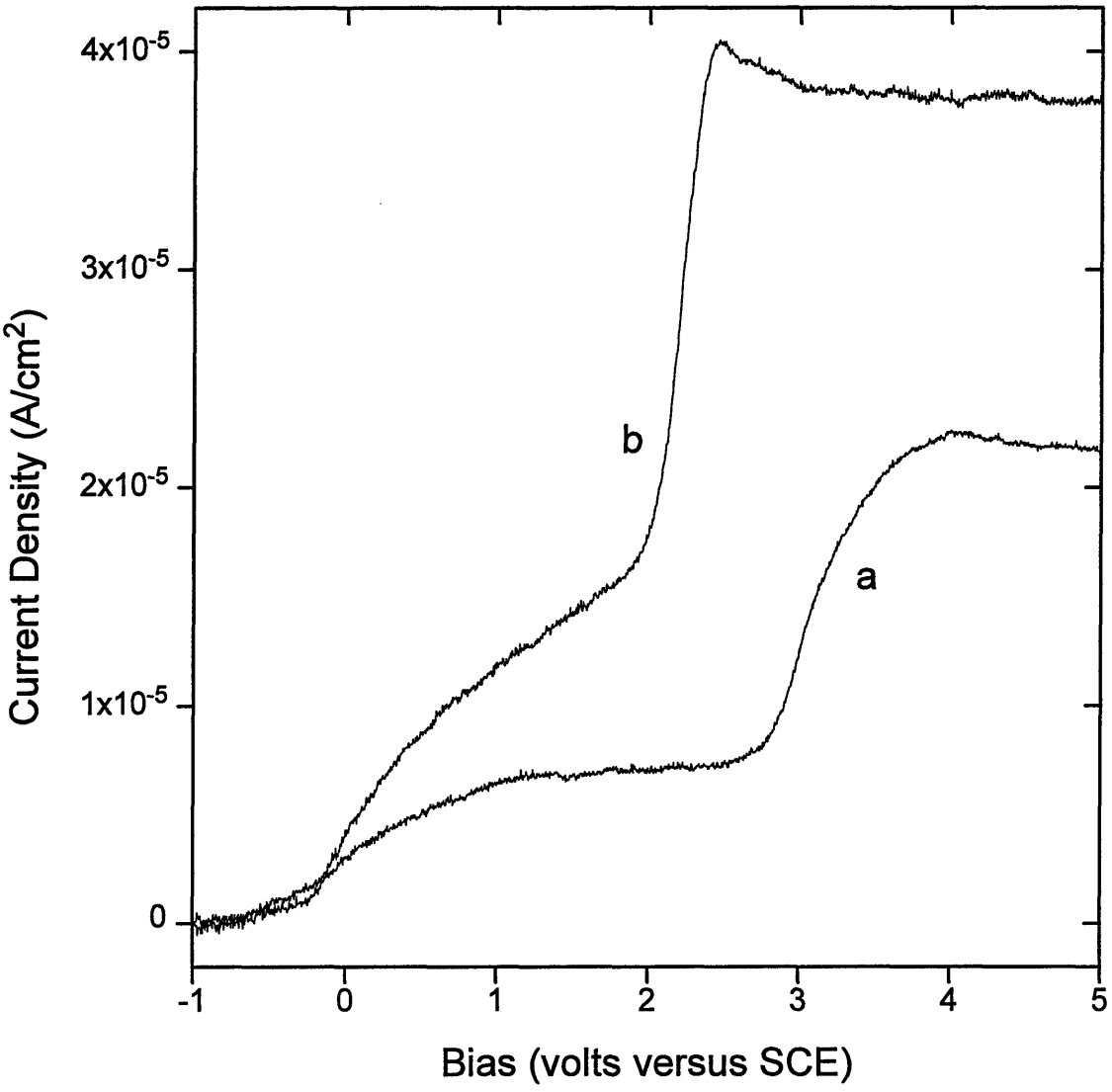


Figure 5.52. Current-voltage sweeps of p-n-p epi multilayer samples in 5% HF electrolyte, using 20mV/s sweep rate, 600mL/min electrolyte flow rate, and no illumination.

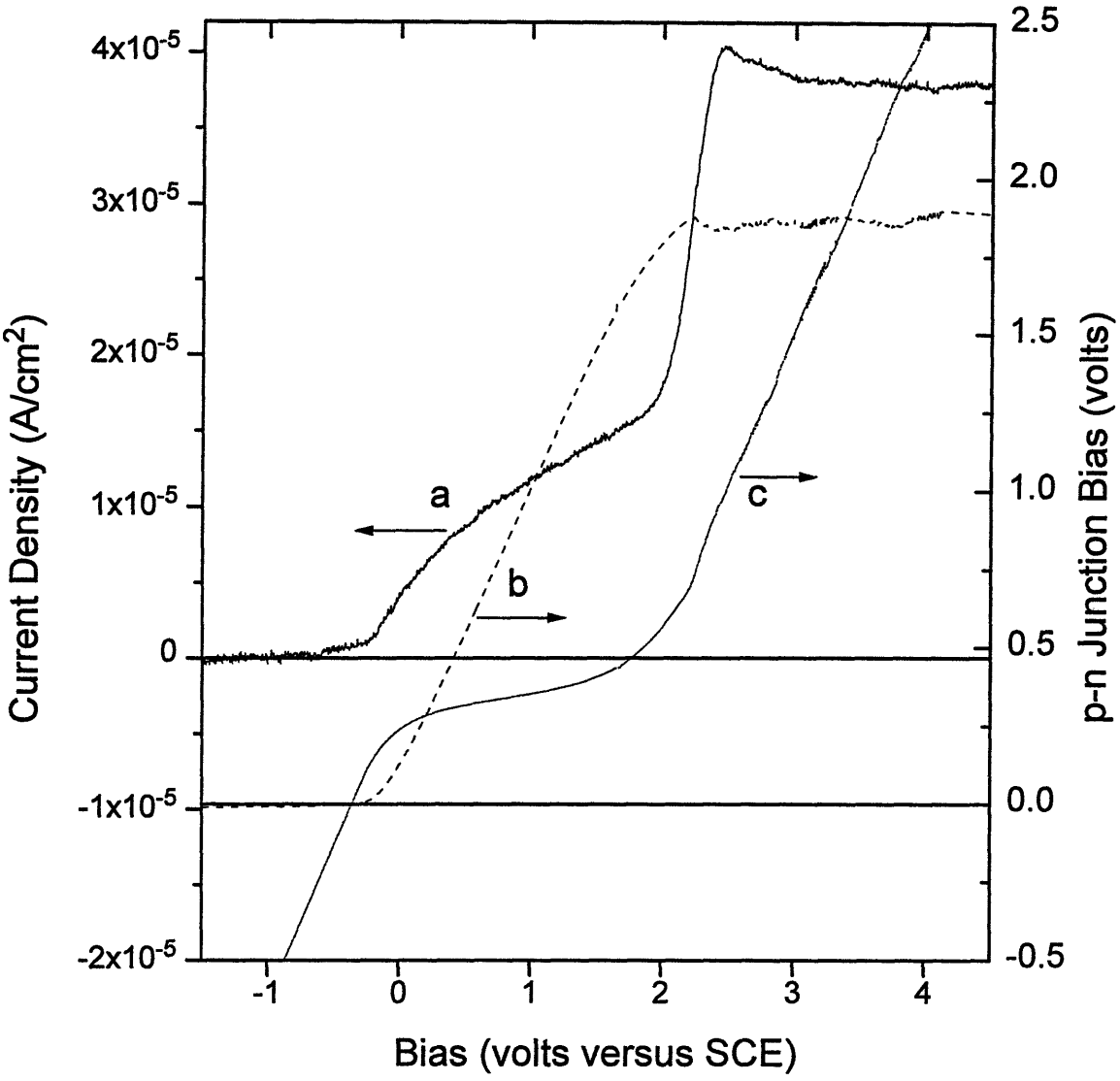


Figure 5.53. Simultaneous measurements of the electrochemical cell current across (a) a p-n-p multi-layer sample, and (b) the bias across between the top p-layer and p-substrate. Curve (c) is the cell bias (x-axis) minus the bias represented by curve 2.

p-layer electrolyte interface can be calculated using equation 3.17 giving 0.29μm. And assuming $V_{pn(r)}$=1.9V as determined from curve (b), the depletion layer width in the p-side on the reverse biased p-n junction can be calculated using equation 3.37 giving 0.62μm. Added together the these equal 0.914μm which is slightly higher than the 0.75μm p-layer thickness.

The p-n-p multilayer etch rates were measured for biases from 0 to 5V (SCE) and are plotted in figure 5.41. Except for the enhanced etching at the Teflon seal lip resulting from surface leakage currents the p-n-p multilayer samples exhibited no measurable etch rate (greater than the 10^{-4} μm/min resolution of the experiment) over the entire potential range.

5.3.4 n-p-n Multilayer

The current-voltage characteristics of the n-p-n multilayer samples, shown in figure 5.54, are similar to those of the n-on-p epi-layer samples indicating that most of the overall potential drop still falls across the n-layer/electrolyte interface rather than across the extra reverse biased p-n junction. This initially seems surprising since the n-substrate/p-layer junction should not provide sufficient holes to account for the anodic current, however the surface leakage current injects holes into the sandwiched p-layer effectively shorting the reverse biased p-n junction.

5.3.4 The Effect of Illumination

All epi-layer samples etch when illuminated as shown in figure 5.55 due to photo-bias and current generation at the illuminated p-n junctions. Notice that the p-on-n and n-p-n illuminated current-voltage characteristics are similar, as are those for the n-on-p and p-n-p samples. Clearly illumination shorts the current blocking effect of reverse biased junctions as is evident by the high p-on-n and p-n-p current-voltage characteristics. The measured p-on-n current-voltage characteristics (curve a) and calculated p-on-n current-voltage characteristics (chapter 3) which we discuss in chapter 6. Apparently the presence of a second epi-layer (i.e. n-p-n rather than p-on-n) has little effect on the etching onset potential for either p- and n-substrate samples. A ≈1V shift in the etching onset potential is evident, however, between n- and p-substrates. The n-p-n sample exhibits higher current densities than the p-on-n sample to ≈0.8V (SCE), at which point the thin n-layer has dissolved.

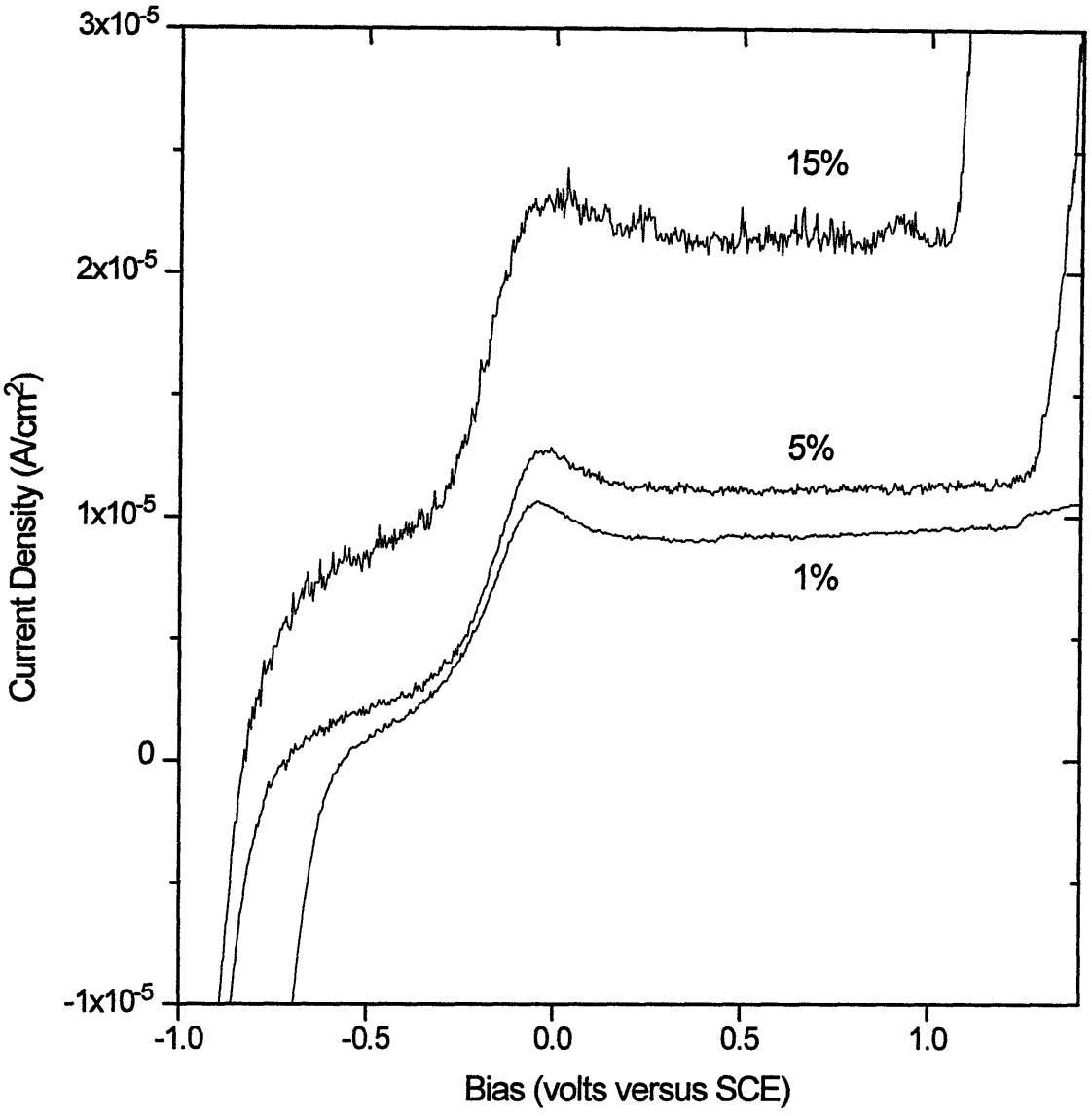


Figure 5.54. Current-voltage sweeps of n-p-n epi multilayer samples in 1, 5, and 15% aqueous HF electrolytes, using 20mV/s sweep rate, 600mL/min electrolyte flow rate, and no illumination.

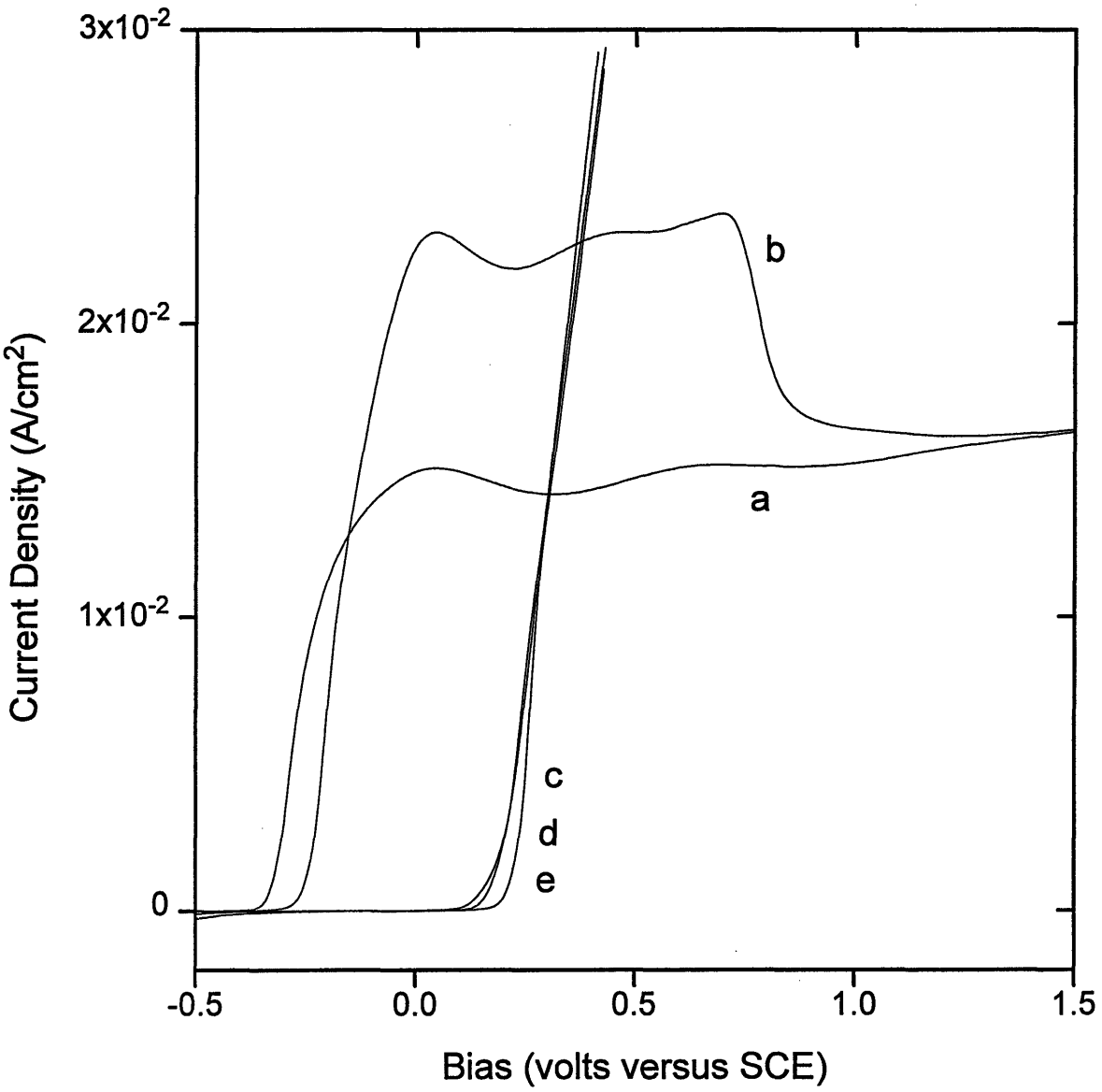


Figure 5.55. Current-voltage characteristics of the epi samples illuminated with 32.6 mW/cm^2 white light. Measured using 5% HF, 20mV/s, and 600mL/min flow rate. a) p-on-n, b) n-p-n, c) n-on-p, d) n-on-p$^+$, e) p-n-p

5.4 Etching of High Aspect Ratio Structures Using Optical masking

n-Si wafers with patterned metal masks were prepared for high aspect ratio etching studies in which illuminated n-Si is selectively etched versus unilluminated n-Si. The mask pattern included a range of line widths down to 1μm, and three mask compositions were used including TiW, Pt on Ti, and Au on Cr layers as explained in section 4.1.3.

Figure 5.56 shows the dark and illuminated current-voltage characteristics of the masked samples. The characteristic n-Si illumination intensity limited regimes are clearly visible in the illuminated curves. Unfortunately the current-voltage characteristics of the metal-silicon-HF electrolyte interface is too complex to easily resolve the etching signatures of the metal layers.

The Ti layer of the Pt-Ti mask was found to etch for all potentials corresponding to n-Si etching, resulting in delamination of the Pt layer before any high aspect ratio structures could be formed.

The TiW mask layer proved to be electrochemically inert in 5% HF up to ≈0.1V (SCE). Unfortunately the TiW layer buckled and delaminated from the n-substrate at the mask edges and at pinholes as shown in figure 5.58. Delamination precluded the ability to form high aspect ratio structures with narrow line widths as shown in the lower micrograph. Furthermore, delamination and buckling increased with both HF concentration and etching potential, precluding the ability to even form ≈20μm wide structures at reasonable etch rates. Figure 5.59 shows the top surfaces of high aspect ratio pillars after TiW mask removal using H_2O_2 at 25°C. The extent of delamination is clearly visible by the step at the top of the pillar resulting from underetching below the delaminated mask. To minimize delamination, samples were etched at low potentials with the unfortunate trade-off of low etch rates. 100 minutes were required to etch the high aspect ratio structures shown in figure 5.58. Etching with filtered red or white light produced poor results with significantly more mask underetching than with filtered blue light which was used for the samples shown in the micrographs. These results are discussed in chapter 6.

While the Au-Cr mask adhered well to the n-Si, it was not as inert as the TiW mask due to dissolution of the Cr layer. The Au-Cr mask proved to be only inert in dilute 1% HF electrolyte and at low biases just above the n-Si etching onset potential, again resulting in low etch rates. The superior adhesion, however, allowed etching of narrow line width structures as shown in figure 5.60. The rough sidewalls and bottom surface were caused during porous silicon removal with 25% KOH, which was found to rapidly etch non (111) crystal planes even at 25°C. It is therefore not a suitable etchant for removing porous silicon from high aspect ratio structures.

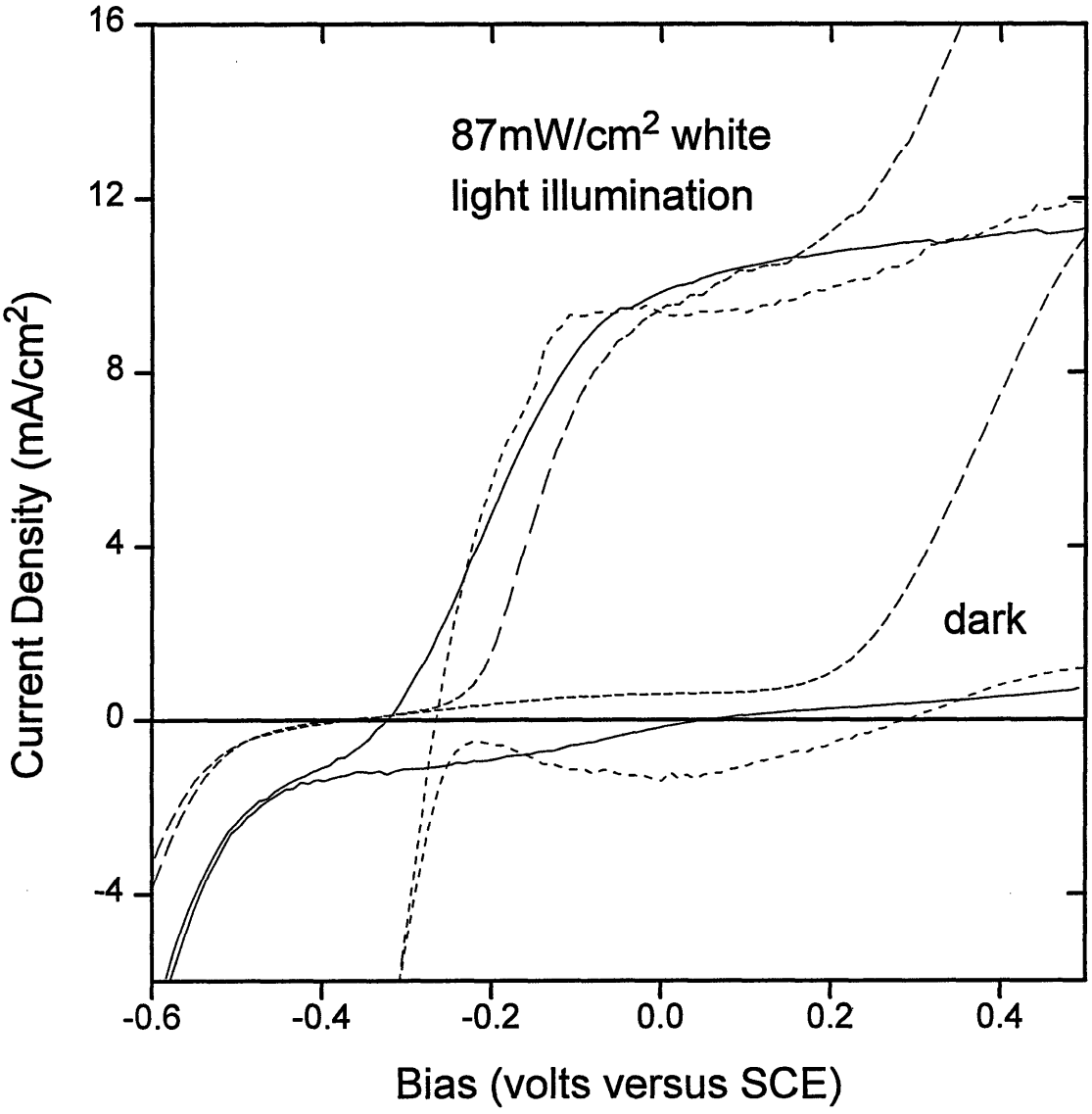


Figure 5.56. Current-voltage characteristics of dark and illuminated n-Si samples with optical masks for etching of high aspect ratio structures. Solid: Au-Cr mask, Dashed: TiW alloy mask, Dotted: Pt-Ti mask.

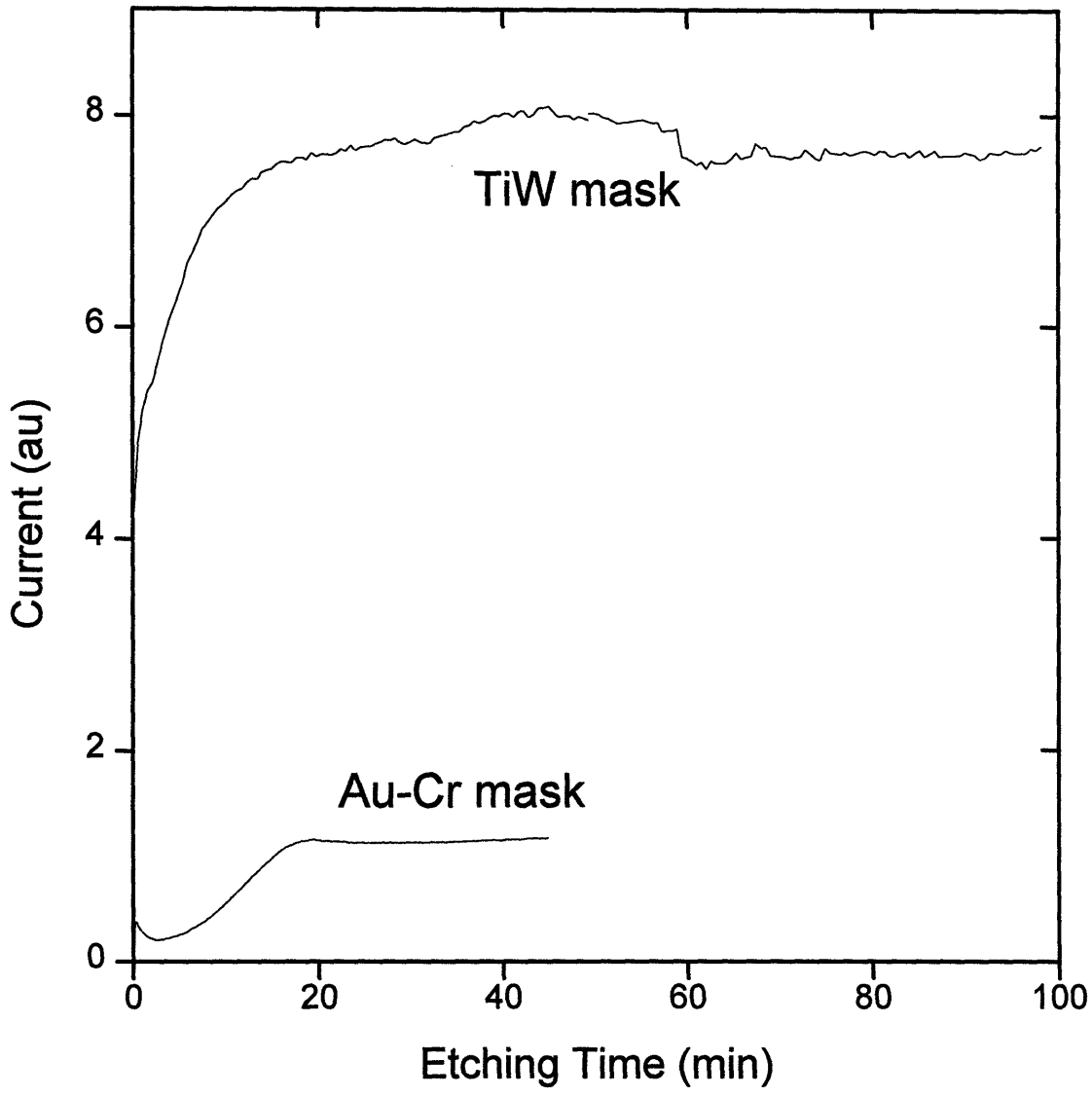


Figure 5.57. Etching current versus time of illuminated n-Si samples masked with patterned Au-Cr, TiW, and Pt-Ti layers used for etching of high aspect ratio structures.

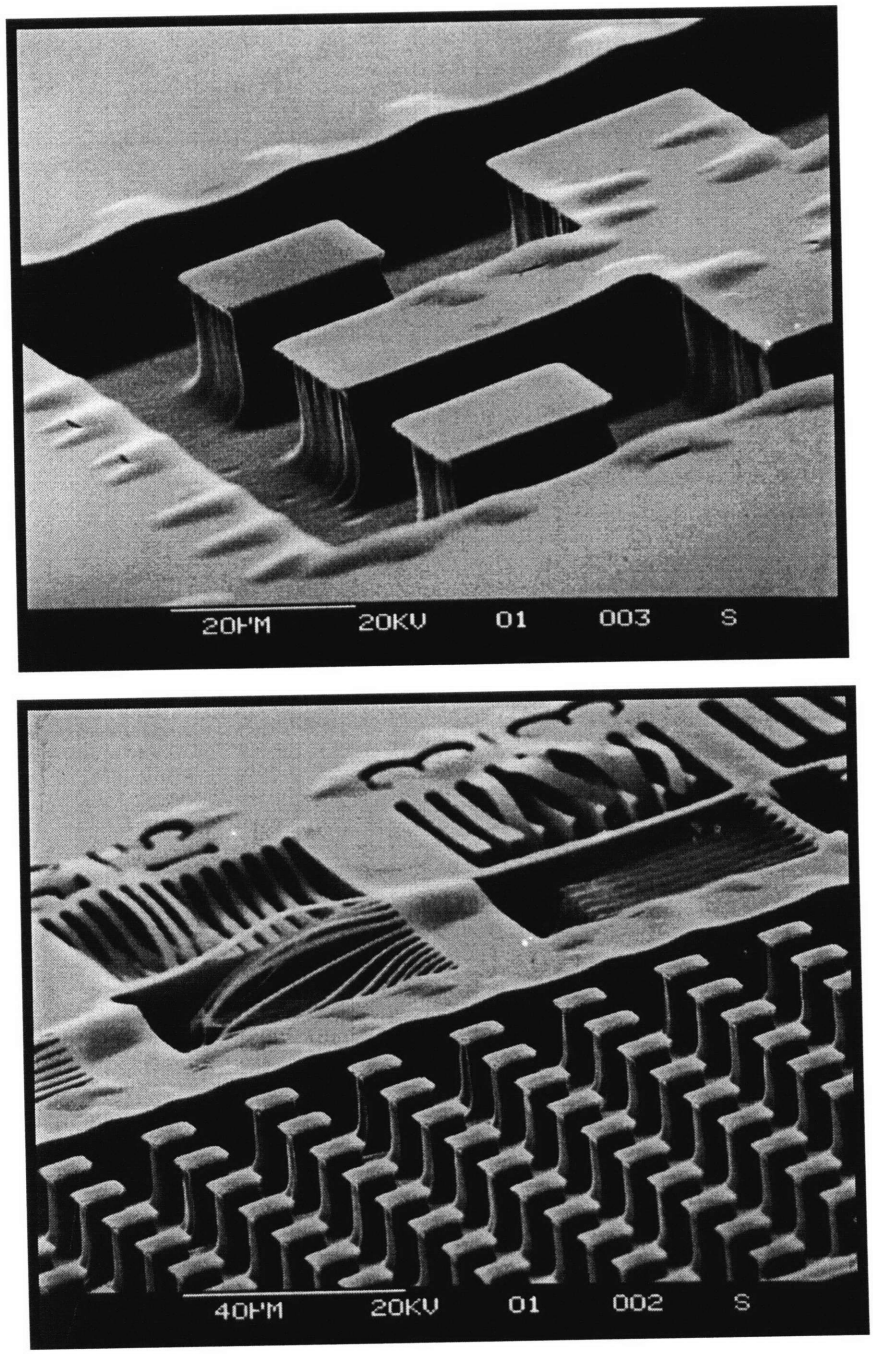


Figure 5.58. SEM micrographs of n-Si high aspect ratio structures etched using a TiW patterned mask, -0.15V (SCE), 5% HF, 32.7mW/cm^2 blue filtered illumination (λ<0.6µm) for 100 minutes. TiW delamination from the silicon substrate is evident which precludes etching of narrow structures less than ≈10µm wide.

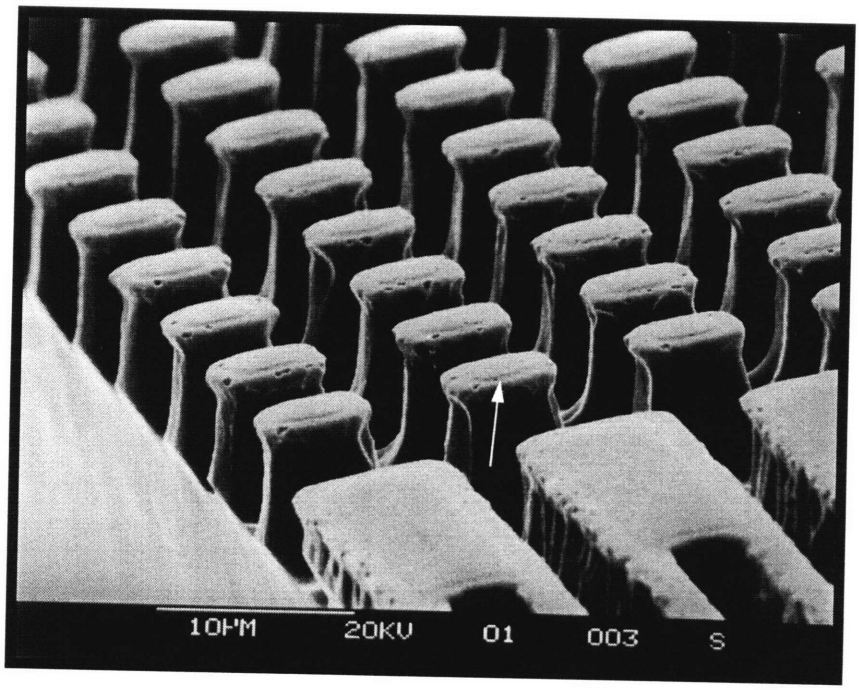


Figure 5.59. SEM micrograph of n-Si high aspect ratio structures etched using a TiW patterned mask, -0.15V (SCE), 5% HF, 32.7mW/cm^2 blue filtered illumination (λ<0.6μm) for 60 minutes. The TiW mask was removed after etching with a 20 minute H_2O_2 etch at 25°C, showing the underetching where delamination occurred (arrow).

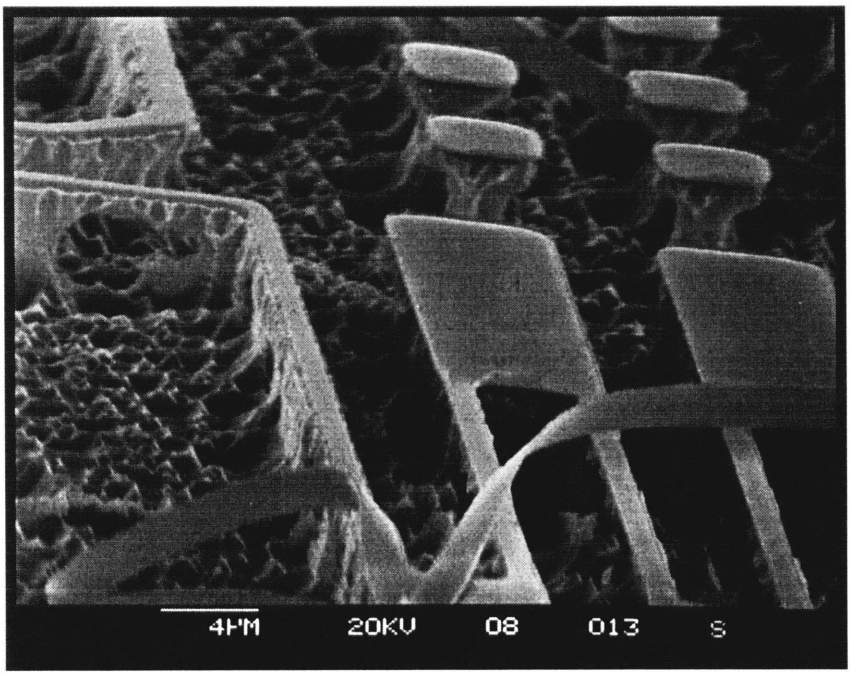


Figure 5.60. SEM micrograph of n-Si high aspect ratio structures etched using a Au-Cr patterned mask, -0.15V (SCE), 1% HF, and 32.7mW/cm^2 blue filtered illumination (λ<0.6μm) for 45 minutes. Narrow strips of the Au-Cr mask have delaminated and are curled near the surface. Etching of ≈1μm wide high aspect ratio structures is demonstrated however the sidewalls are very rough and undercut due to porous silicon removal using 25 weight percent KOH at 25°C.

Chapter 6

Discussion

Electrochemical and photoelectrochemical micromachining of silicon has been investigated to develop a new and hopefully enabling micromachining technology. In chapter two we reviewed the few electrochemical micromachining studies previously reported in the literature. In general, these studies include 1) selective etching of n-layers on p-substrates accomplished by illumination and direct anodic biasing of the n-layer (section 2.2.1.2), and 2) selective etching of p-substrates at porous silicon formation potentials to form underetched n-Si structures which were ion implanted into the substrate and, in most cases, capped with a LPCVD silicon nitride layer.

In chapter five we first presented a systematic study of bulk silicon etching characteristics which confirmed and complemented previous reports in the literature. Next we demonstrated three novel p-n junction etch-stops afforded by electrochemical and photoelectrochemical micromachining of silicon in HF electrolytes, and presented experimental results showing which biases and illumination intensities are necessary to achieve successful results.

This was followed by a study of the etching characteristics of epi layer samples having various sequences of n- and p-layers, revealing four key observations. First, virtually all of the potential applied between the sample substrate and electrolyte falls either across the Schottky barrier at the silicon-electrolyte interface when it is reverse biased, or across a reverse biased p-n junctions in the current path. Second, reverse biased p-n junctions effectively block anodic currents preventing etching of the following p- or n-regions. Third, surface leakage currents were found to short-circuit these blocking junctions degrading etch-stop performance. Forth, the initial current density across epitaxial n-layers on p-substrates were found to be very low ($\approx 10^{-5} A/cm^2$) because little of the overall potential drop falls across the forward biased the p-n junction, preventing rapid hole injection into the n-layer. The n-layer etches non-uniformly producing a highly pitted macroporous surface. These macropores rapidly etch through the n-layer into the p-substrate, at which point the p-n junction forward bias increases resulting in rapid n-layer etching.

In chapter three we developed the theoretical aspects governing how the overall potential applied across the sample substrate and electrolyte is distributed between the silicon-electrolyte interface and the p-n junctions in the current path. These potential

drops were correlated to the sample potential as measured with respect to the cell reference electrode, which also allowed calculation of the expected cell current.

And finally, we also demonstrated the feasibility of etching high aspect ratio structures and described the difficulties caused by delamination and dissolution of the patterned metal mask layers.

In this chapter we compare the experimental results of chapter five to the models in chapter three and further develop our understanding of the etch-stop mechanisms. We use the results of the bulk etching characteristics to establish parameter 'windows' within which p-n junction and etching of high aspect ratio structures can be achieved, set guidelines for optimizing the various processes, and discuss their capabilities and limitations. Finally we compare electrochemical and photoelectrochemical silicon micromachining in HF electrolytes with other bulk silicon micromachining techniques.

6.1 Selective Etching and Etch Stop Mechanisms

Electrochemical etching of silicon requires injection of holes to the surface, which either break the back-bonds of surface silicon atoms allowing their attack by electrolyte HF species (at porous silicon formation potentials), or to oxidize surface atoms to a valence state of +4 which then react with oxygen species from the electrolyte to form an oxide layer (at electropolishing potentials). Etching of bulk p-Si is therefore easily achieved by applying an anodic bias to drive the naturally abundant holes to the surface. n-Si, on the other hand, exhibits etch rates orders of magnitude lower than p-Si at the same anodic bias because holes are scarce. Rapid n-Si etch rates are achieved when high non-equilibrium minority hole concentrations are generated by above band-gap illumination. Models in good agreement with the observed bulk p- and illuminated n-Si current-voltage characteristics have been presented in the literature (see sections 3.1.1 and 3.1.2).

The electrochemical etching characteristics of structures having both n- and p-regions are not as easily understood because of the influence of internal p-n junctions on the potential distributions and anodic currents within the sample. In fact, there have been conflicting reports in the literature as to the mechanisms of the few p-n junction etch-stops studied, and no self-consistent model has been reported which can explain both the literature results and those in this thesis.

Our results have shown that p-n junctions affect the potential distributions and anodic currents within p-n structures in several important ways. Forward biased p-n junctions can inject holes into n-layers, providing an alternate source other than above band-gap illumination for introducing non-equilibrium holes in n-Si. Reverse biased p-n junctions block anodic currents thereby effectively reducing the etch rates of subsequent p- or n-regions. Illuminated p-n junctions generate photo-biases which anodically bias p-regions with respect to n-regions. Illuminated p-n junctions also generate photo-

currents which supply anodic currents across reverse biased p-n junctions effectively short circuiting their current blocking characteristics. And finally, p-n junction leakage currents either within the bulk or at the semiconductor surface degrade the p-n junction etch-stop performance by permitting significantly higher currents across reverse biased p-n junctions.

By understanding these effects we can now explain both the etching characteristics of the epi-layer structures and the various phenomena observed while micromachining cantilever beam structures with the three novel p-n junction etch-stop techniques. Table 6.1 summarizes the doping profiles and etching procedures required for implementing these etch-stop techniques. Each requires an anodic bias applied to an electrical contact on the wafer backside. In addition, the p-on-n and p-well etch-stops are photo-initiated processes requiring illumination, and the p-on-n etch-stop further requires a second electrical contact to the p-regions which are to remain unetched.

	substrate dopant type	etched silicon dopant type	etch-stop dopant type	electrical contact to wafer backside	electrical contact to etch-stop layer	illumination
p-on-n	n	n	p	yes	yes	yes
p-well	n	p	n	yes**	no	yes
p-n-p	p	p	p on n	yes	no	no
HARS*	n	n	metal***	yes	no***	yes

* high aspect ratio structures, ** see section 6.3, *** patterned mask on the n-Si surface, see section 6.2.

Table 6.1. Table of the etching requirements and doping profiles for implementation of the p-n junction etch-stops and etching of high aspect ratio structures.

6.1.1 p-on-n

Contrary to bulk p-Si, anodically biased p-on-n samples were found to exhibit low p-Si etch rates when not illuminated. This observation is consistent with the model presented in chapter three, that the p-Si etch rates are limited by the reverse biased p-n junction current which blocks the arrival of holes to the p-Si/electrolyte interface. For silicon junctions, the anodic current should therefore be equal to the generation current in the p-n junction depletion zone (equation 3.33) which dominates over the ideal p-n junction diffusion current. This generation current is proportional to the depletion zone width giving a square root dependence on the p-n junction bias (equation 3.36), and inversely proportional to the effective minority carrier lifetime τ_e which approximately equals 10^{-5} seconds for high quality p-n junctions.

Since most of the applied potential falls across the p-n junction, the cell bias can be taken as an approximate measure of the p-n junction bias. The current-voltage characteristics of p-epi layer on n-substrate samples shown in figure 5.39 exhibit this square root dependence. However, the corresponding value for τ_e is approximately 10^{-8} seconds, three orders of magnitude lower than expected. As explained in chapter five, we attribute this low effective minority carrier lifetime and the correspondingly higher p-Si etch rate to surface leakage currents originating at the sample edges where sample dicing cuts through the p-n junction. Dicing produces a highly defective layer extending several microns from the surface in which the p-n junction generation current is dramatically enhanced. These currents were reduced by dipping the samples in 5% HF which presumably etched some of the damaged silicon and passivated the surface states with hydrogen. In retrospect, greater effort should have been made to remove this damaged layer by either etching the sample in 20:1 HNO_3:HF or by growing a thermal passivating oxide. Nevertheless , our results show that p-structures on n-substrates etch at least three orders of magnitude slower than bulk p-Si, which should increase to more than six orders of magnitude if surface leakage currents are eliminated.

The other discrepancy between the measured and calculated current-voltage characteristics for p-layer on n-substrate samples is a ≈0.6V shift in their etching onset potentials. Etching onset was measured at ≈-0.2V (SCE), similar to that of bulk p-Si (note: here we define the etching onset potential as that corresponding to a current density of 10^{-5}A/cm^2). This is inconsistent with figure 3.4 which shows that V_a of a p-on-n sample should be shifted anodically by V_{bi}=0.67V as compared to bulk p-Si due to the presence of the p-n junction potential drop. As expected this shift is evident in the calculated current-voltage characteristics shown in figure 3.6. While the measured results would agree well with the calculated results if V_{bi} was omitted from equation 3.44, we find no valid justification for doing so.

The current blocking character of p-n junctions can be circumvented by either shorting or directly biasing the p-n junction as shown in figure 5.16, permitting etching of the p-structures at bulk p-Si etch rates while n-regions, which are not illuminated, do not etch. Apparently shorting or directly biasing the p-n junction could be used to selectively etch p-Si versus n-Si, for example by etching the p-well structure. There are two difficulties with this approach, however. First, an ohmic contact must be made to each p-region in the presence of the HF electrolyte, and second, any portions of the p-regions that become isolated from the ohmic contact cease etching. This is a particularly difficult problem for etching of p-well type structures since the p-Si directly below the cantilever beams are the last to etch.

6.1.2 p-n-p

The current-voltage characteristics of p-n-p epi-layer samples were found to be nearly identical to those of the p-on-n samples at biases up to ≈2V (SCE). This is consistent with the potential drop across the various junctions calculated in chapter three

which show that virtually none of the overall potential falls across the extra forward biased p-n junction. At approximately 2V (SCE), however, the current density nearly triples as shown in figure 5.52. At this bias depletion zone punch-through occurs across the top p-layer as the reverse biased p-n junction and silicon-electrolyte interface Schottky barrier depletion zones overlap. The p-n-p multi-layer etching characteristics now become more similar to those of n-on-p samples and etch-stop performance is degraded.

6.1.3 Illuminated p-on-n

The other method of supplying anodic currents to p-structures on n-substrates is to generate a p-n junction photo-current using illumination, which is the basis of the p-well etch-stop. Selective etching of the p-well requires the presence of a potential window in which p-Si etches while n-Si does not. The cell bias applied to the illuminated n-substrate must therefore be below the n-Si onset etching potential. The illuminated p-n junction must also supply a photo-bias in excess of ≈0.5V to compensate for the shift in bulk p-Si versus n-Si current-voltage characteristics (figure 5.13), thereby providing the window shown in figure 5.14. Since the photo-bias is limited to ≈0.6V as shown in figure 3.11, there exists only a small potential window for p-well etching. As a result, the ≈0.1V shifts in p-Si and n-Si current-voltage characteristics as a function of doping density (figures A4.21 and A4.23) must be considered when choosing cell bias. The window is maximized for low N_D and high N_A, and minimized for high N_D and low N_A. Based on the ≈0.5V shift that was measured between the current-voltage characteristics of $N_D=8x10^{14}cm^{-3}$ n-Si and $N_A=2x10^{15}cm^{-3}$ p-Si and a maximum photo-bias of ≈0.6V, we see that in the worst case scenario the bias window can completely disappear.

As a result we can now understand our difficulty in underetching the p-well cantilever beam structures which have a doping profile as shown in figure 4.2(f). The cantilever beams are heavily doped n-Si with $N_D>10^{18}cm^{-3}$, and the p-well doping density is $\approx 4x10^{17}cm^{-3}$ near the surface but only $\approx 10^{16}cm^{-3}$ between the beams and the substrate. While figure 5.24 shows that the p-well begins etching at potentials ≥-0.45V (SCE) we found that underetching was only achieved for potentials ≥-0.4V (SCE). Furthermore we see that increasing HF concentration and illumination intensity increases the potential window (figures 5.23 and 5.24), consistent with our observations that underetching could not be achieved for electrolytes with less than 15% HF or for illumination intensities less than $0.5W/cm^2$ red (λ>720nm) illumination. Wavelength primarily influences the effective p-n junction illumination intensity due to the photon absorption depth dependence on wavelength. High energy photons tend to be absorbed near the silicon surface before reaching the p-n junction.

The current-voltage characteristics of illuminated p-on-n epi-layer samples were modeled in section 3.3.4 and graphed in figure 3.13. Figure 3.13 shows that the etching onset shifts cathodically with increasing p-n junction photo-generated current J_L,

consistent with the experimental results of the p-well structure shown in figure 5.23. In addition, figure 3.13 reveals a illumination intensity limited plateau similar to that observed for bulk n-Si. This is consistent with the measured current-voltage characteristics of illuminated p-on-n epi-layer samples shown in figure 5.55(a), except for a slight low frequency oscillation probably caused by porous silicon formation on the surface which effects photon scattering and absorption efficiency. We again find a ≈0.6Vshift between the calculated and measured etching onset potential as was observed for non-illuminated p-on-n samples. This again implies that perhaps the term v_{bi}=.669V should be omitted from equations 3.44 and 3.61 for the non-illuminated and illuminated cases respectively.

The current-voltage characteristics of illuminated p-well samples differ from the calculated current-voltage characteristics for three reasons. First, silicon-electrolyte interface Schottky behavior as given by equation 3.46 is only valid at low current densities. As the current density approaches the first current peak, the reaction kinetics become increasingly limited by dissolution of the oxidized reaction products until a uniform anodic oxide layer forms at the peak current density. Second, the theoretical calculations assume a constant p-n junction photo-bias J_L, which in fact varies with potential as the p-n junction depletion zone width changes. And third, the theory assumed that the p-n junction and silicon-electrolyte interface areas are equal which is not true for the p-well structure. More accurately,

$$i_{cell} = i_{SCR} = - i_{pn(IL)} \tag{6.1}$$

$$\text{and therefore} \qquad J_{cell} = J_{SCR} = - J_{pn(IL)}[A_{pn}/A_{SCR}] \tag{6.2}$$

Using equation 6.2 and following the approach of section 3.3.4, equations 3.63 and 3.64 can be written as

$$V_{SCR} = \frac{kT}{q} \ln\left[-\frac{J_S}{\vartheta}\frac{A_{pn}}{A_{SCR}} \exp\left(\frac{qV_{pnIL}}{kT}\right) + \frac{J_S}{\vartheta}\frac{A_{pn}}{A_{SCR}} + \frac{J_L}{\vartheta}\frac{A_{pn}}{A_{SCR}} \right] \tag{6.3}$$

$$\frac{kT}{q} \ln\left[-\frac{J_S}{\vartheta}\frac{A_{pn}}{A_{SCR}} \exp\left(\frac{qV_{pnIL}}{kT}\right) + \frac{J_S}{\vartheta}\frac{A_{pn}}{A_{SCR}} + \frac{J_L}{\vartheta}\frac{A_{pn}}{A_{SCR}} \right] - V_{pnIL} = V_a - C - V_H - V_{bi(pn)} + V_{bi(SCR)} \tag{6.4}$$

and again solved for V_{pnIL}, V_{SCR}, and J_{cell} as a function of V_a. These are graphed in figures 6.1 and 6.2 for J_L=0.5A/cm^2 and A_{pn}/A_{SCR} ratios of 4, 2, 1, 0.5, and 0.25. Figure 6.2 shows that the onset etching potential is not affected by varying the p-n junction to silicon-electrolyte interface area ratio. The cell current increases linearly with the

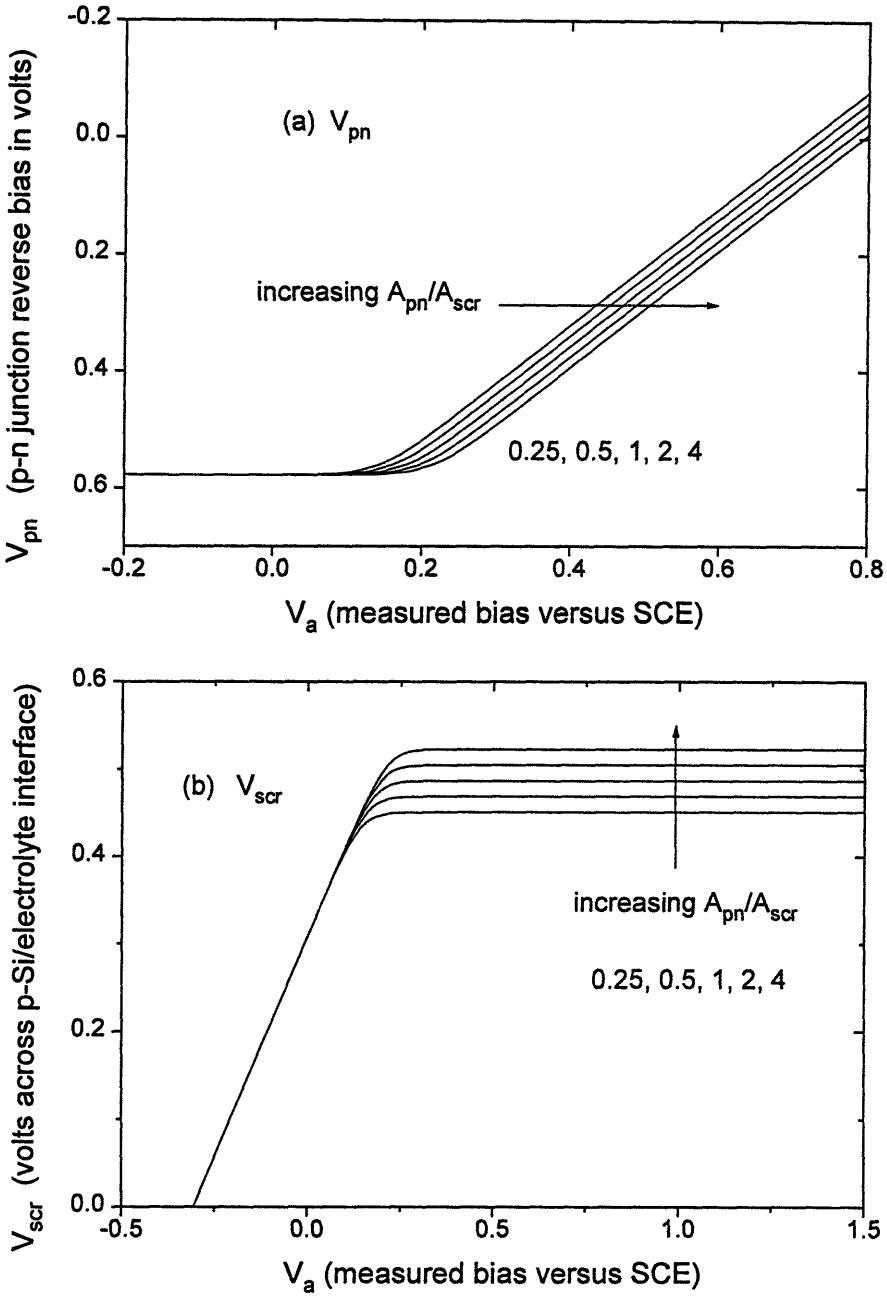


Figure 6.1. Plots of the calculated distribution of applied potential between the p-n junction (V_{pnIL}) and the silicon-electrolyte interface (V_{scr}) versus the cell potential (V_a) for five different ratios of the p-n junction and silicon-electrolyte interface areas.

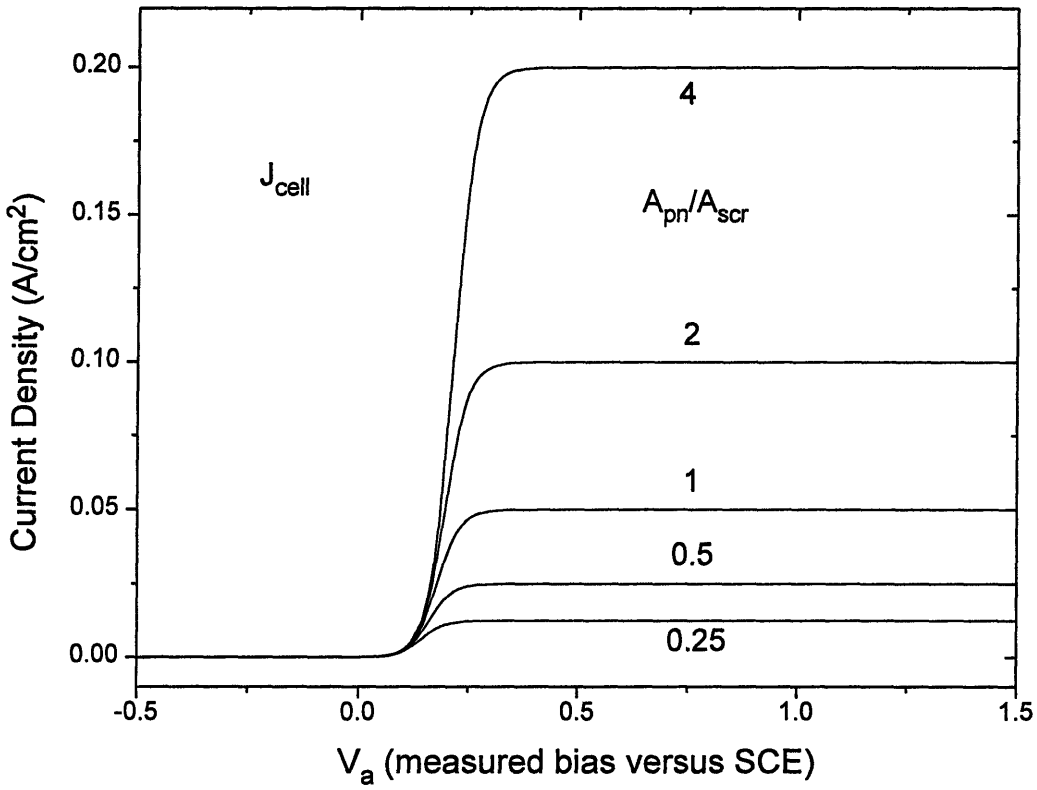


Figure 6.2. Graph of the calculated anodic current through an illuminated p-layer on n-substrate sample as a function of bias applied to the n-substrate for five different ratios of the p-n junction and silicon-electrolyte interface areas.

A_{pn}/S_{SCR} ratio as predicted by equation 6.2. Figure 6.1 shows that with an increasing A_{pn}/A_{SCR} ratio, increasingly more of the overall potential drops across the Schottky barrier and less across the p-n junction.

While the p-well structure provided a potential window just wide enough to selectively etch the p-well with respect to the cantilever beams, we were unable to use a sufficiently low bias to prevent etching of the n-substrate. This was a surprising result because figure A4.23 shows that etching of the lightly doped substrate should require higher potentials than that of the more heavily doped cantilever beams. We propose that the substrate etching results from field enhancement at the pore tips. The p-well is etched at porous silicon formation potentials, and therefore pores grow down to the p-well/n-substrate etch-stop providing small radius pits which locally concentrate the field. This mechanism was previously suggested by Benjamin [94] to explain similar difficulties in the n^+-Si versus n-Si etch-stop (section 2.2.1.3).

6.1.4 n-on-p

The failure mechanism for the poor performance of the n-on-p etch-stop results from an inherent instability in maintaining virtually all of the potential drop across the reverse biased Schottky barrier. Our experimental measurements of n-on-p epi-layer samples revealed that initially only ≈0.04V drops across the forward biased p-n junction resulting in a hole current of only $\approx 1.5 \times 10^{-5} A/cm^2$ to the silicon-electrolyte interface. In section 3.3.2 we explained that the rate of electron generation in the n-layer limits the electron current across the forward biased p-n junction, which in turn limits the p-n junction forward bias according to equation .3.54, which therefore limits the hole injection rate according to equation 5.53. We then proposed four possible source for electron generation in the n-layer, one of which includes tunneling of surface valence electrons into the n-Si conduction band as was suggested by Searson and Zhang to explain the $\approx 10^{-5} A/cm^2$ anodic current observed at non-illuminated bulk n-Si electrodes. Except for a rapid current density increase at ≈3V (SCE) which is discussed shortly, the current-voltage characteristics of n-on-p epi-layer samples in 5%HF as shown in figure 5.42 are strikingly similar to those of non-illuminated bulk n-Si shown in figure 5.3. This strongly suggests that the non-illuminated bulk n-Si anodic current is in fact due to electron injection into the conduction band, and is the dominant source of electrons in the n-layer which limits the p-n junction forward bias and hole injection.

The low $\approx 1.5 \times 10^{-5} A/cm^2$ anodic current to the silicon-electrolyte interface results in porous silicon formation. Holes are therefore preferentially collected at pore tips which results in macroporous silicon formation much like that reported by Lehmann *et. al.* [56,73] on bulk n-Si when using back-side wafer illumination. (See section 2.1.1.1) The $\approx 1.5 \times 10^{-5} A/cm^2$ anodic current across the p-n junction is therefore collected by a very small fraction of the silicon-electrolyte interface area, and the pores propagate through the n-layer extremely quickly as compared to the rate which would be obtained by a uniform etch front. Figure 5.46 shows the changes in the cell and p-n junction currents and p-n junction forward bias once the macropores reach the substrate, revealing a rapid increase in the p-n junction forward bias. We attribute this increase to a perturbation in the distribution of applied potential between the p-n junction and the Schottky barrier at the silicon-electrolyte interface which occurs in the vicinity of the p-n-electrolyte triple junction. As a result the hole injection rate into the n-layer becomes dramatically increased and the n-layer is quickly dissolved.

Based on this understanding we propose possible solutions: 1) the p-n-p etch-stop which we have developed and demonstrated, 2) deposition of a layer of material inert in the HF electrolyte (i.e., parylene, polyimide, or LPCVD silicon nitride) to the top of the n-Si which will prevent pore initiation and propagation down to the p-substrate, thereby eliminating the inherent instability, 3) applying a second electrode to the n-layer to impose a reverse bias across the p-n junction which will eliminate hole injection, and 4) introducing minority hole recombination centers into the n-layer by ion implantation for example, which will recombine the injected holes before they reach the silicon-electrolyte

interface. Interestingly, the recombination in solution 4 will consume many of the electrons generated in the n-layer that are required to satisfy the forward biased p-n junction electron current equation (3.54). This in turn will further reduce the hole injection rate. We therefore believe this reduced-minority-carrier-lifetime n-on-p etch-stop will provide good n-Si versus p-Si selectivity and warrants further study.

6.1.5 An Enhanced Understanding of the Existing Literature

Our new understanding of the etch-stop mechanisms can be used to explain the successes and failures of electrochemical micromachining processes previously reported in the literature. Selective etching of p-substrates below n-structures was achieved for one of two reasons. Most of the n-structures were capped with a LPCVD Si_3N_4 layer as shown in figure 6.3 [92,93,94]. This serves to prevent macropore growth through the n-layer into the p-substrate thereby preventing the n-on-p etch-stop instability as explained above. And second, all of n-regions were fabricated by ion implantation [92-96] which reduced the minority carrier lifetimes, thereby preventing hole arrival to the silicon-electrolyte interface and reducing the hole injection rate as also discussed above.

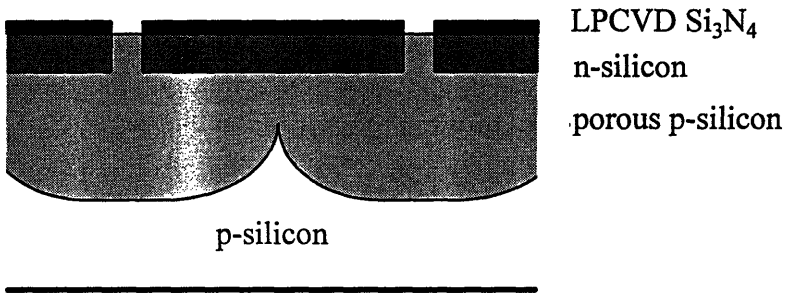


Figure 6.3. Schematic diagram of LPCVD Si_3N_4 capped n-on-p samples used in the literature to selectively etch p-Si, forming n-Si structures.

Benjamin's improved process [93,94], which incorporates a buried n-layer to limit vertical etching, is shown in figure 2.4. The buried n-layer is in fact a variation of the p-n-p multilayer consisting of a very thick top p-layer. Benjamin reports that the buried n-layer is inert because n-Si does not etch in the dark, however it is in fact the p-n-p multi-layer aspect of the buried layer which is inert and limits the vertical etching. This could be verified by comparing the gap between the top n-layer and buried etch-stop of an etched sample to the doping profile.

Selective etching of an n-type layer on a p-type substrate has been reported for GaAs [101] and SiC [102,103]. In each case the anodic bias was applied directly to the n-layer and the sample was illuminated with a focused laser beam as shown in figure 6.4.

The p-substrate is not exposed to the electrolyte until the etch-front reaches the p-n junction, at which point there is no longer an illuminated p-n junction to provide photo-bias effects. The newly exposed p-substrate does not etch due to the reverse biased p-n junction which blocks anodic current resulting in a p-n junction etch-stop. Nevertheless this approach can not achieve under-etched structures and is of limited interest.

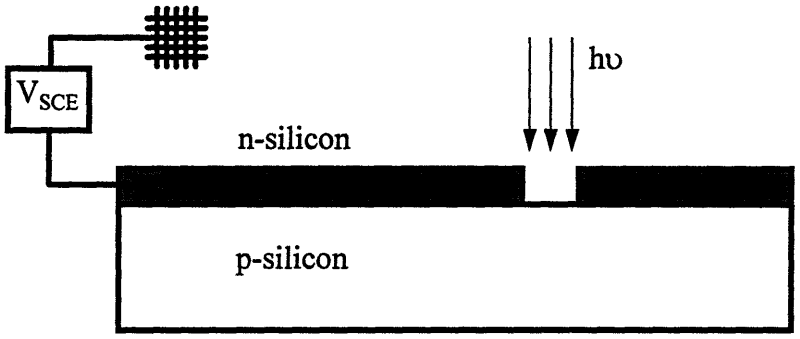


Figure 6.4. Schematic diagram showing the selective etching of n-layers on p-substrates reported in the literature.

6.2 Windows of Operation and Optimal Values of Etching Parameters

Electrochemical etching of silicon requires a hole current to the silicon-electrolyte interface. Applied bias is most important parameter governing silicon etch rates. All three p-n junction etch-stops developed in this thesis require a specific range or 'window' of biases to achieve good results. Illumination also provides a means of generating anodic currents, but it is distinctly different from applied bias in that there is not a specific illumination intensity 'window' required to achieve the p-n junction etch-stops. The other parameters play a less significant role. Changes in illumination intensity, photon wavelength, doping density, and electrolyte HF concentration and ionic strength tend to shift the etch-stop bias windows, and electrolyte HF composition and circulation effect the rate of the dissolution reaction which becomes rate limiting at sufficiently high anodic currents.

The ultra-high selectivity of the p-on-n etch-stop is achieved by simultaneously imposing a p-Si bias below that of the p-Si etching onset etching potential while biasing n-Si above its etching onset potential. The n-substrate must therefore be biased anodic of ≈-0.5V (SCE), however significantly higher biases of at least 3V (SCE) are desirable to

achieve electropolished surfaces and rapid etch rates. The illumination intensity should be greater than 0.5W/cm^2 to achieve electropolishing in 5% HF electrolytes. When not directly biased, the p-Si potential is equal to that applied to the n-Si substrate (V_a) plus the photo-bias (V_{pn}) generated by the illuminated p-n junction. Since p-Si has a onset etching potential approximately 0.5V anodic of that for n-Si, it is necessary to apply a p-n junction reverse bias (V_R) equal to $-V_a-V_{ph}+V_{pn}$ in order to prevent p-Si etching. In practice we typically apply a p-n junction reverse bias potential of $V_R=-V_a-0.5V$ which provides an n versus p selectivity of $\approx 10^8$.

Several factors were found to affect the shape and surface morphology of the n-Si etch-pit surfaces. The silicon directly below the cantilever beams does not begin etching until exposed to the electrolyte, so that higher peaks are formed under wider beams. The p-Si beams also absorb a fraction of the incident illumination which, if the applied bias and illumination intensity correspond to illumination intensity limited regime, will result in slower etching below the beams. A greater fraction of the incident illumination will be abbsorbed with increasing photon energy. Etching under electropolishing conditions produces curved surfaces because the photo-generated holes have ample time to diffuse laterally, while etching in the porous silicon regime produces angular surfaces provided that illumination intensity is not rate limiting. Angular surfaces form because of the isotropic nature of electrochemical silicon etching in HF, which tends to preserve the 45° slopes which form below the cantilever beams as the n-Si surface etches both laterally inward under the beam and down into the substrate.

The p-n-p etch-stop does not protect the etch-stop layer by imposing a cathodic bias, but rather employs a reverse biased p-n junction to limit the anodic current to the silicon-electrolyte interface. The p-substrate is biased above its etching onset potential and therefore, given a source of holes, the p-layer would also readily etch. Clearly the selectivity of the p-n-p must be less thant that of the p-on-n etch-stop, and is limited either by the current across the reverse biased p-n junction or by some alternate dissolution mechanism similar to that observed at anodically biased non-illuminated n-Si electrodes. We were unable to etch the p-n-p cantilever beam test structures above ≈0.6V (SCE) due to the presence of defects presumed to be stacking faults which etched laterally consuming the multi-layer. These defects locally etched above ≈0.2V (SCE) to form small 5μm square holes in the multi-layer which were stable over time. These holes exposed the p-substrate to the electrolyte which eventually resulted in multi-layer underetching giving a free-standing membrane with 5μm pores. Our results on p-n-p epi-layer samples show that in the absence of such defects, the multi-layer is stable until the p-n junction depletion zone punches-through the capping p-layer, which occurred at ≈2V (SCE) for a 0.75μm thick layer.

Electrolyte HF concentration has several important effects on etch rate and etched surface smoothness. Assuming no electrolyte IR drop, the etch rate at porous silicon formation potentials is virtually independent of HF concentration. At higher potentials, increasing HF concentrations etch the dissolution products more rapidly resulting in an increase in the first current peak biases and current densities. Thus there is a trade off

between faster rates and smoother surfaces when using the p-n-p etch-stop which has a limited bias window of operation.

The electrolyte IR drop between the silicon surface and reference electrode can be substantial even when the electrodes are separated by only one centimeter, especially in dilute 1 or 5% HF electrolytes. The measured applied bias V_a is no longer a true measure of the potential drop across the silicon-electrolyte interface and must be corrected using $V_{corr}=V_a-IR$. This can be particularly troubling when using the p-well etch-stop which has a narrow window of operation. If the reference electrode is moved closer or further from the silicon surface the change in the IR potential drop may shift the potential across the silicon-electrolyte interface outside of the bias window.

6.3 The Capabilities and Limitations as Compared to other Silicon Bulk Micromachining Techniques

Electrochemical and photoelectrochemical micromachining of silicon in HF electrolytes offers unique and desirable capabilities as compared to traditional chemical bulk micromachining.

The two most preferred and commercially successful micromachining etch-stops used today both employ EDP and KOH type (LiOH, NaOH, CsOH) basic solutions. The p^+ etch-stop involves fabricating heavily boron doped structures ($N_A>2x10^{19}cm^{-3}$) which etch 10^2 to 10^3 slower than lightly or moderately doped silicon in KOH, depending on the doping density and etchant temperature and concentration. The electrochemical passivation etch-stop involves applying an anodic bias to the n-regions of a p-n structure to form an anodic oxide. Silicon anodic oxides only etch appreciably in HF electrolytes and therefore the n-Si etch rate is reduced by $\approx 10^2$ to that of the anodic oxide etch rate in KOH. The p-regions continue to etch because the reverse biased p-n junction protects them from the anodic passivation current. This etch-stop requires very low p-n junction leakage currents and typically good reproducibility and yield requires independent biasing of both the n- and p-regions to ensure that the p-Si regions do not also passivate. The etch-stop selectivities are up to one order of magnitude higher for EDP than KOH, but still orders of magnitude lower than those achieved for the electrochemical etch-stops presented in this thesis.

The chemical silicon etch rate in HF is only angstroms per hour. The electrochemical etch-stops therefore provide ultra-high selectivities of up to 10^8 when either the p- or n-regions are anodically etched at rates of micrometers per minute while the other doping type is held below it etching onset potential. Furthermore electrochemical etching requires the arrival of holes to the silicon-electrolyte interface. These anodic currents are drastically reduced by reverse biased internal p-n junctions in the current path, again providing ultra-high p-n junction etch-stop selectivities. High

selectivities are desirable because otherwise the etch rate of the etch-stop material is not negligible over the duration of the micromachining process resulting in a change of the structure dimensions with etching time. This is particularly a problem when micromachining capacitive sensors having signals proportional to $1/d^2$ or mechanical devices having deflections proportional to d^3. Furthermore high selectivities become increasingly important when micromachining sub-micron sized structures for which the relative error $\Delta d/d$ rapidly increases.

Probably the greatest advantage of electrochemical micromachining is its versatility. KOH and EDP etchants chemically dissolve silicon which provides few opportunities for limiting the etch rate to provide etch-stops. Electrochemical etching on the other hand requires hole arrival to the silicon-electrolyte interface which can be controlled in a variety of ways including bias, illumination, the presence of internal p-n junctions, and the presence of minority hole recombination centers. We have shown that bulk silicon electrochemical etch rates can be controlled over orders of magnitude by appropriately choosing the bias, HF concentration, and in some cases illumination intensity. Furthermore, etch rates up to 100μm/min can be achieved at room temperature. In contrast, KOH or EDP etch rates are limited to ≈0.8μm/min and requires heating to 80°C or above. We have shown how the various capabilities for controlling electrochemical etch rates can be used to achieve three novel p-n junction etch-stops, have proposed a fourth etch-stop possibility in section 6.1.4, and have demonstrated the feasibility of etching vertical high aspect ratio structures. Furthermore two of these etch-stops are photo-initiated which provides added versatility by, for example, etching only specific p-wells on a wafer by passing the incident illumination through a mask.

Three other important capabilities are worth mentioning. The electrochemical etch-stops allow fabrication of sub-micron sized structures which we have demonstrated by forming 0.6 and 0.8μm thin cantilever beams. The etch-stops are compatible with light or moderate doping densities which permits fabrication of stress and curl free structures thereby preserving the original dimensions. And third, the external electrochemical cell current provides a convenient means for in-situ monitoring of the etching reaction which, in some cases, can also be used to detect defective wafers and monitor quality control.

Perhaps the greatest advantage of the p^+ etch-stop is its simplicity of implementation. Wafers merely need to be placed in heated KOH or EDP for a predetermined period of time. Unfortunately the resulting p^+ structures are heavily boron doped resulting in high internal stresses, buckling, and curling. Furthermore the degenerate nature of these structures precludes forming electronics such as piezoresistors in the structures themselves. As a result there has recently been much activity in the MEMS community to commercially apply the electrochemical passivation etch-stop, which has a similar complexity of implementation to the etch-stops developed in this thesis. The electrochemical etch-stops require application of anodic bias to the wafer through an ohmic contact isolated from the electrolyte. Furthermore the p-well and p-on-n etch-stops require illumination and the p-on-n etch-stop also requires a second sample

electrode to the p-regions. Since wafer illumination is already used in photolithography and since the challenges for etching while applying wafer biases are currently being solved, commercial application of electrochemical and photoelectrochemical silicon micromachining should not prove too difficult.

And finally, the other significant limitation of electrochemical micromachining is the hazardous and highly corrosive nature of HF electrolytes. Special care is necessary to avoid skin contact and exposure to fumes. HF attacks most metalization layers, silicon dioxide, and PECVD silicon nitride which are used to fabricate both electrical contacts to micromachined structures and microelectronics for smart MEMS. It is therefore necessary to either perform the micromachining process before depositing these materials or to protect them from the electrolyte using LPCVD silicon nitride or parylene coatings. EDP and KOH type etchants are also not ideal. EDP solutions are carcinogenic, and while KOH type solutions introduce alkali metal impurities which have debilitating effects on silicon electronics.

Chapter 7

Conclusions

Electrochemical and photoelectrochemical micromachining of silicon using HF electrolytes was studied to realize new methods for fabricating sensors, actuators, and microelectromechanical systems. Our results demonstrate this technique is a highly versatile micromachining technology having numerous desirable and enabling capabilities.

Three novel and distinctly different p-n junction etch-stops which we refer to as p-on-n, p-well, and p-n-p were developed and successfully demonstrated by micromachining cantilever beams structures. All three etch-stops are compatible with light or moderate doping densities which yielded stress-free and curl-free structures. Etch-stop selectivities as high as 10^8 were achieved permitting superior dimensional control of micromachined devices. Furthermore, we demonstrated the capability of fabricating sub-micron sized structures by micromachining 0.6 and 0.8μm thin cantilever beams. By appropriately choosing the etch-stop and etching parameters we can now selectively etch n-Si, p-Si, or simultaneously etch both n- and p-Si at a user-controlled relative rate. And finally, the photo-initiated p-on-n and p-well etch-stops can be combined with optical masking to micromachine only selected regions of a wafer.

The feasibility of etching high aspect ratio structures in n-Si using illumination through patterned metal masks was demonstrated by fabricating pillars and 1μm wide walls with 5:1 aspect ratios and vertical walls. The process was limited by mask layer dissolution and delamination from the silicon substrate, and otherwise is expected to permit etching of structures with significantly higher aspect ratios.

The etch-stop mechanisms were modeled to establish the distribution of anodic potentials and currents within the various p- and n-regions and verified with experimental studies on epitaxial layer samples. Virtually all of the potential applied between the sample substrate and electrolyte was found to drop across either the Schottky barrier at the silicon-electrolyte interface or any reverse biased p-n junctions in the current path, effectively shielding the following p- or n-regions from anodic currents. Hole generation either from illumination, surface leakage currents, or recombination/generation centers were found to short-circuit these blocking junctions degrading etch-stop performance.

With our new understanding of the etch-stop mechanisms we were able to explain the successes an failures of previous electrochemical micromachining studies in the literature.

And finally, we have established then parameter windows within which successful p-n junction etch-stops and etching of high aspect ratio structures can be achieved, and outlined guidelines for optimizing these processes.

Based on these results, we conclude that electrochemical and photoelectrochemical micromachining of silicon in HF electrolytes is a powerful and highly versatile technique which, as the MEMS community strives to fabricate ever more complex structures with precisely controlled dimensions, should prove to be a useful and enabling technology.

Chapter 8

Future Work

Electrochemical and photoelectrochemical micromachining of silicon in HF electrolytes is a new and virtually unexplored field with numerous directions warranting further study.

We have demonstrated the feasibility of etching vertical high aspect ratio structures using patterned metal masks, however mask etching and/or delamination from the substrate limited the aspect ratios and structure line widths which we could achieve. The delamination problem could be solved by annealing the metalized sample, forming an intermediate silicide layer. Alternatively electrochemical dissolution of the metal layer could be eliminated by first depositing a LPCVD silicon nitride or parylene layer, which would isolate the metal from the anodic bias. One could also bias the metal layer cathodically further preventing its dissolution. Once suitable masks are developed, the optimal values of applied bias, electrolyte HF concentration, illumination intensity and wavelength which minimize underetching, minimize surface roughness, and yield vertical walls can be investigated more rigorously.

We measured and modeled the currents across p-on-n and p-n-p epi-layer samples, and found that the etching current exhibited a square-root dependence on applied bias. It would be interesting to reproduce these results with germanium, for which the ideal p-n junction diffusion current dominates over the depletion zone generation current. The epi-layer current-voltage characteristics for germanium samples should therefore exhibit a saturation current rather than square-root dependence, which would further verify aspects of the model.

Sub-micron 0.6 and 0.8μm thin p-n junction etch-stop capability and high p-n selectivities were demonstrated. It would be very useful to investigate the limits of these processes, for example, the minimum possible structure dimensions which can be fabricated, or the maximum p-n selectivities afforded by the p-well and p-n-p etch-stops. The current-voltage characteristics of epi-layer samples having low surface leakage currents should measured to determine if p-Si when adequately shielded from holes also exhibits the 'dark' $\approx 10^{-5} A/cm^2$ etching current density as observed for non-illuminated n-Si electrodes.

A systematic study of silicon etching as a function of electrolyte composition was beyond the scope of this thesis. Possible improvements would be to add wetting agents

to remove hydrogen bubbles from the surface giving improved surface uniformity, or to add HCl and NH_4F which would reduce the electrolyte IR drop by increasing the ionic strength. Furthermore it would be interesting to investigate electrochemical silicon micromachining in anhydrous HF-acetonitrile, which does not form porous silicon layers and should give smooth etched surfaces.

A reduced-minority-carrier-lifetime etch-stop was proposed in section 6.1.4 which, like the p-n-p etch-stop, would function without the need for illumination or a second sample electrode.

The electrochemical nature of this micromachining process can be applied to other semiconductors which typically can not be micromachined with traditional silicon processes. Of particular interest is SiC for high temperature applications.

The ultimate goal, however, is to fabricate MEMS devices. We have demonstrated that electrochemical silicon micromachining in HF can be successfully and reproducibly used to fabricate cantilever beams with high dimensional control. It is now necessary to develop the next level of sophistication, for example to form structures containing piezoresistors or buried electrodes for extracting capacitive signals and allowing actuation.

Appendix

A1 Calculation of Implanted and Annealed Doping Profiles

This section presents the calculations used to determine implantation and anneal conditions for achieving desired doping profiles. A computer program was written to calculate dopant distributions as a function of implantation range (R_p), straggle (ΔR_p), and dose (S), diffusion coefficient (D), and anneal temperature (T) and time (t).

R_p and ΔR_p for boron and phosphorous implantation into silicon as a function of beam energy were determined using the program TRIM[1], with silicon atom displacement and lattice binding energies set to 17eV and 2eV respectively.

Diffusivities were calculated using D=0.76exp(3.46/kT) for boron and D=3.85exp(3.66/kT) for phosphorous. Diffusivities were assumed independent of the presence of other dopants. Anneals were performed under flowing O_2 to prevent phosphorous evaporation from the surface.

Dopant distributions as a function of depth from the surface (x) were calculated using equation A1.1, which assumes the boundary condition A1.2.

$$C = \frac{S}{2\sqrt{2\pi\Delta R_p^2 + 4Dt}} \left\{ \exp\frac{-(x-R_p)^2}{2\Delta R_p^2 + 4Dt}\left[1 + erf\left(\frac{\frac{R_p\sqrt{4Dt}}{\sqrt{2}\Delta R_p} + \frac{x\sqrt{2}\Delta R_p}{\sqrt{4Dt}}}{\sqrt{2\Delta R_p^2 + 4Dt}}\right)\right] + \exp\frac{-(x+R_p)^2}{2\Delta R_p^2 + 4Dt}\left[1 + erf\left(\frac{\frac{R_p\sqrt{4Dt}}{\sqrt{2}\Delta R_p} - \frac{x\sqrt{2}\Delta R_p}{\sqrt{4Dt}}}{\sqrt{2\Delta R_p^2 + 4Dt}}\right)\right] \right\} \text{ cm}^{-3} \quad \text{(A1.1)}$$

$$\left.\frac{\partial C}{\partial x}\right|_{(x=0)} = 0 \quad \text{(A1.2)}$$

1 TRIM ©1990, by the authors J. F. Ziegler and J. P. Biersack, "The Stopping and Range of Ions in Solids", Permagon Press, NY, 1985

A2 Illumination Intensity Measurements

Illumination intensity was determined by measuring the photocurrent generated by an Oriel #7183 silicon photodiode, and converting the photocurrent to intensity using the photodiode spectral response and spectral irradiance of the light reaching the diode. This section details the experimental procedure and calculations used in the measurements.

The photodiode was installed against the circular Teflon-lip seal of the PEC cell where Si etching samples are otherwise mounted. The photo-voltage generated across a load resistor was measured and converted to current-density using ohms law and the illuminated photodiode area:

$$I_{ph} = \frac{V_{ph}}{R_L} x \frac{1}{Area} \qquad A/cm^2 \qquad (A2.1)$$

The load resistance (R_L)was determined to within 0.005% from the slope of a current-voltage sweep generated by a Solatron 1286 potentiostat. The calculations used to convert I_{ph} to light intensity follow.

A2.1 Intensity Measurements of Monochromatic Light

Monochromatic light intensity (W/cm^2) was calculated by dividing the photodiode current-density (A/cm^2) by the photodiode responsivity (A/W) at monochromatic wavelength. Figure A2.1 shows the silicon photodiode spectral responsivity PSR(λ), where data points are Oriel's responsivity measurements and the curve represents a 10th order polynomial best fit. A computer program was written to calculate the monochromatic light intensity using the 10^{th} order polynomial, and user input wavelength, photodiode type, illuminated area, load resistance, and measured photo-voltage. In addition, the program checks for photodiode linearity by ensuring that photodiode current-density is below $0.02/R_L$ A/cm^2. High illumination intensities required the use of small load resistance's and/or neutral density filters.

The calculated illumination intensity does not account for differences in electrode versus photodiode surface reflectivity, nor for electrolyte absorptivity

A2.2 Intensity Measurements of White or Colored-Glass Filtered Light

Illumination intensity calculations for non-monochromatic light is more complex due to the spectral dependence of both the incident light at the detector and the photodiode responsivity. Furthermore, the lamp spectral irradience is a function of filament temperature, which varies with lamp current.

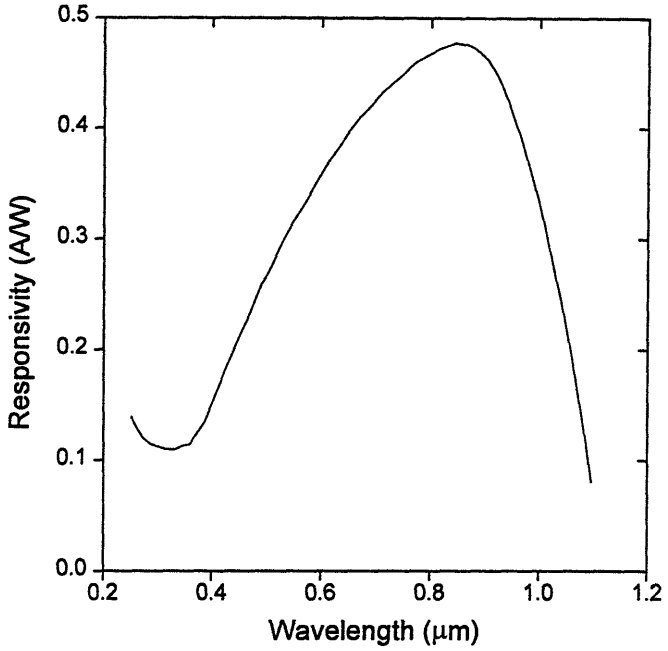


Figure A2.1. Spectral responsivity of the Oriel #7183 silicon photodetector.

Before converting photodiode current-density to illumination intensity it is necessary to first calculate the effective photodetector responsivity EPR (A/W) by weighting the photodetector spectral responsivity PSR(λ) (figure A2.1) by the relative spectral intensity RSI(λ) reaching the detector:

$$EPR = \frac{\int_{\lambda_{min}}^{\lambda_{max}} PSR(\lambda)RSI(\lambda)\partial\lambda}{\int_{\lambda_{min}}^{\lambda_{max}} RSI(\lambda)\partial\lambda} \qquad \text{A / W} \qquad \text{(A2.2)}$$

RSI(λ) is a product of the of the lamp spectral irradience LSI(λ), colored glass filter transmittence FT(λ), borosilicate crown glass transmittence GT(λ), and electrolyte and water filter transmittence WT(λ). GT(λ) and FT(λ) are obtained by first digitizing and then curve fitting to Oriel's measured transmittences.

The transmittence of HF electrolyte is assumed to equal that of DI water, and is calculated from the absorption coefficient α(λ) (see figure A2.2) [128] by:

$$WT(\lambda) = \frac{I}{I_o} = \exp[-\alpha(\lambda)x] \qquad \text{(A2.3)}$$

where x is the optical path length.

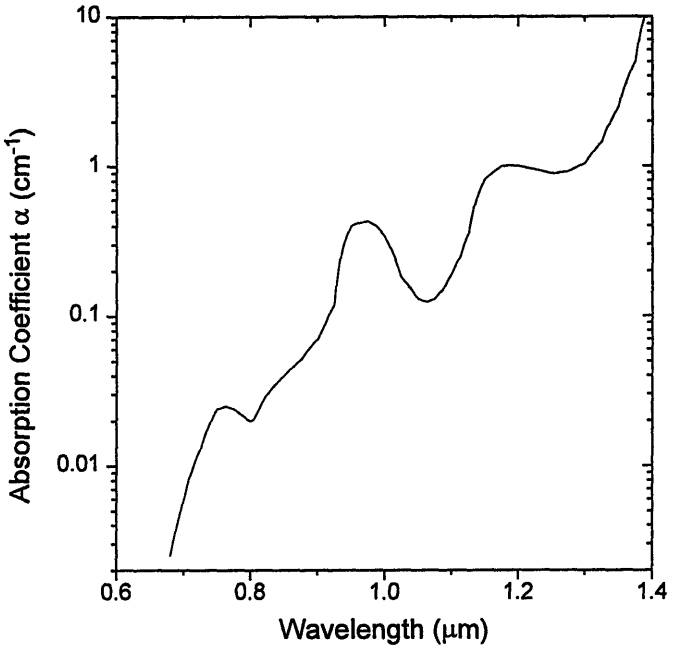


Figure A2.2. Absorption coefficient of DI water at 25°C.

Using λ_{min} =310nm (borosilicate crown glass optical cut-off) and λ_{max} =1107nm (silicon band edge wavelength), equation A2.2 becomes:

$$EPR = \frac{\int_{310}^{1107} PSR(\lambda)LSI(\lambda)FT(\lambda)GT(\lambda)WT(\lambda)\partial\lambda}{\int_{310}^{1107} LSI(\lambda)FT(\lambda)GT(\lambda)WT(\lambda)\partial\lambda} \quad A/W \qquad (A2.4)$$

Once the lamp spectral irradience LSI(λ) is determined, equation A2.4 can be evaluated, and the light intensity is calculated by dividing the measured photodiode current density by EPR, the effective photodiode responsivity. All calculations were again done by a computer program, which prompts for the illuminated area, load resistance, photovoltage, lamp current (for LSI(λ) calculations), water filter/electrolyte optical path length, and type of colored glass filter.

A2.2.1 Calculation of Lamp Spectral Irradience LSI(λ)

Lamp spectral irradience was determined by passing the lamp's illumination through a calibrated Kratos GM252 grating monochrometer (with 1180 mm^{-1} grating), and onto an Oriel #7183 Si photodiode to determine the generated photocurrent over a wavelength range from 250 to 950nm. Photovoltage was measured across a 981.39Ω load resistor using Keithley 181 nanovoltmeter and converted to I_{ph} using Ohm's law. Monochrometer slit width and height were set to 1mm and 6.5mm respectively, yielding

a 3.3nm linear dispersion. The active photodiode surface was held at 1.7cm from the exit slit and 50.0 cm from the center of the lamp filament. The photodetector was shielded from stray light by installation in a custom machined black Delrin holder, and covering the small gap between the holder and the monochrometer exit slit housing with electrical tape. A mask immediately before the entrance slit and a black anti-reflective material 1.0m behind the lamp served to eliminate secondary reflections from laboratory surfaces.

Data acquisition was controlled by computer program to 1) collect photovoltage measurements from the Keithley 181 through a GPIB interface, 2) use a National Instruments LAB-PC D/A board to both control the monochrometer stepper motor and measure the analogue wavelength signal, and 3) calculate LSI(λ) using equation A2.5:

$$LSI(\lambda) = \frac{I_{ph}(\lambda)}{PSR(\lambda) \times 3.3 \times Area \times MTRANS(\lambda)} \qquad \frac{W}{cm^2 nm} \qquad \text{(A2.5)}$$

$I_{ph}(\lambda)$ is the photocurrent, PSR(λ) is the photodiode spectral responsivity, 3.3 is a correction factor for the 3.3nm linear dispersion of the 1mm monochrometer slit width, *Area* is the photodiode illuminated are, and MTRANS(λ) is the monochrometer transmissivity (see below).

The lamp spectral irradience was measured as a function of DC current from a Sorensen DCR 300-9B power supply. LSI(λ) data was curve fit to equation A2.6 [129], where the curve fit parameters a ($\mu m^4/m^2$) and T (degrees Kelvin) are used in the computer program to generate LSI(λ) data.

$$LSI(\lambda) = \frac{a}{\lambda^5 \left\{ \exp\left(\frac{14387}{\lambda T}\right) - 1 \right\}} \qquad \frac{W}{cm^2 nm} \qquad \text{(A2.6)}$$

A2.2.2 Monochrometer Transmissivity MTRANS(λ)

The Kratos GM252 monochrometer transmissivity was measured using a calibrated 1kW QTH Oriel lamp and Oriel #7183 Si photodiode, with a lamp-monochrometer-photodiode configuration identical to that used in LSI(λ) measurements. MTRANS(λ) was calculated using equation A2.7, where CLBLMP(λ) is the spectral irradience of the calibrated lamp (at a distance of 50.0cm when powered by 7.90 amps DC), and other parameters are as defined in equation A2.5.

$$MTRANS(\lambda) = \frac{I_{ph}(\lambda)}{PSR(\lambda) \times 3.3 \times Area \times CLBLMP(\lambda)} \qquad \text{(A2.7)}$$

7.90 amps DC lamp current was supplied by the Sorensen DCR300-9B power supply, and controlled to within 0.05% by measuring voltage drop across a 0.2012±.0001Ω shunt resistor using the 1286 potentiostat in half-standby mode (ΔRE). The shunt resistor consisted of 5 1Ω, 10W resistors connected in parallel, and its resistance was calculated from the slope of a current-voltage sweep generated by the 1286 after compensating for lead resistance. The shunt resistor was immersed in DI water to reduce ohmic heating, and under these conditions no increase in resistance was observed (greater than 0.5% or .0001Ω) upon passing 7.90 amps DC current.

A2.3 Spectra Irradience of Illumination Intensities Used in the Thesis

Calculated intensities for both white and filtered illumination used in this thesis are reported in mW/cm^2. The spectral irradience (intensity as a function of photon wavelength) incident on the silicon-electrolyte interface depends on lamp current and presence of any colored-glass filter in the light path. Figures A2.3, and A2.4 show the relative spectral irradience RSI(λ) for the various calculated illumination intensities of white and filtered light, as determined by equation A2.8.

$$RSI(\lambda) = LSI(\lambda)FT(\lambda)GT(\lambda)WT(\lambda) \qquad \text{(A2.7)}$$

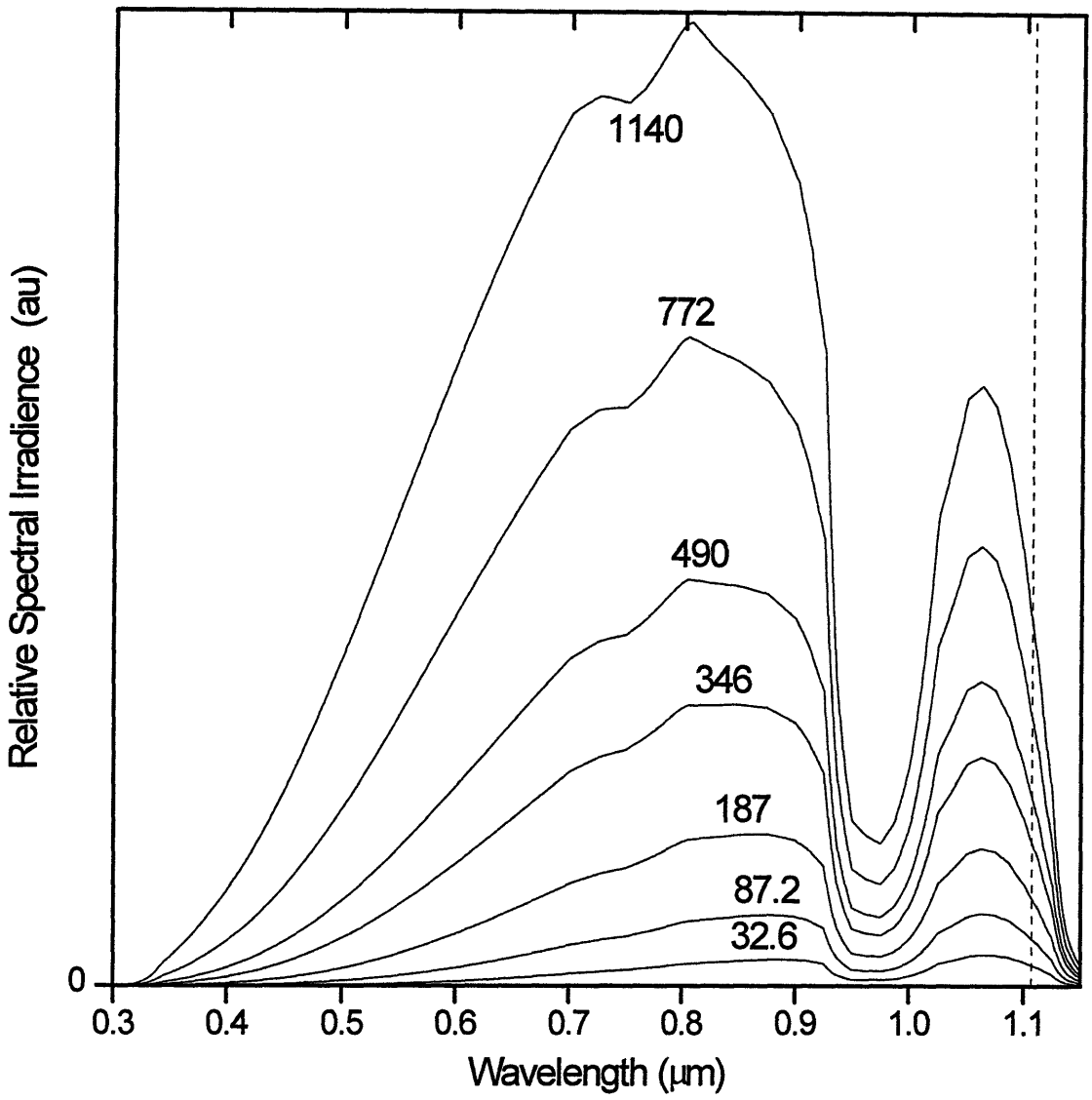


Figure A2.3. Relative spectral irradience of the various white light illumination intensities (as indicated in mW/cm^2) used in the thesis. The dashed line shows the wavelength (1.107μm) corresponding to the silicon band-gap energy.

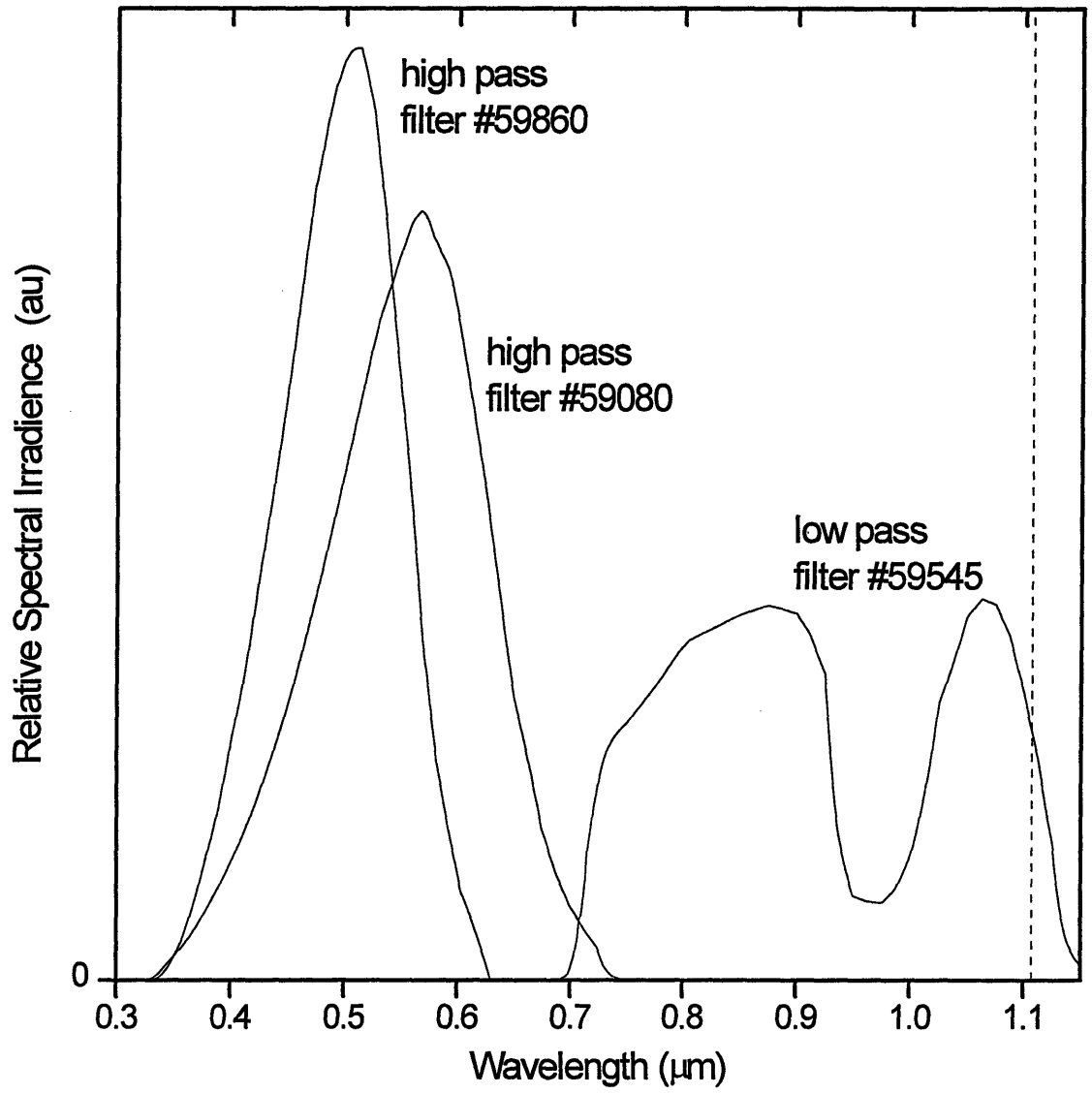


Figure A2.4. Relative spectral irradience of the white light illumination passed through Oriel #59860, 59080, and 59545 colored glass filters. The dashed line shows the wavelength (1.107μm) corresponding to the silicon band-gap energy.

A3 Calculations of HF Electrolyte Molalities

This thesis reports electrolyte HF concentration in weight percent HF, consistent with similar studies in the literature. This section shows the calculations used to obtain molalities of F^-, H^+, HF_2^-, and undissociated HF in the aqueous HF electrolytes used.

Weight percent HF is be converted to molality by the relation:

$$C = \frac{x}{0.02(100-x)} \quad \frac{mol}{kg} \tag{A3.1}$$

where C is the stoichiometric molality in mol solute per kg solvent, x is the weight percent of HF, and 0.02 is the molecular weight of HF in kg/mol.

Hydrofluoric acid is a weak acid with an dissociation constant of $K=6.84 \times 10^{-4}$ mol/kg at 25°C [130] for the reaction:

$$HF \leftrightarrow H^+ + F^- \tag{A3.2}$$

In addition, hydrofluoric acid has a strong tendency to associate:

$$HF_2^- \leftrightarrow HF + F^- \tag{A3.3}$$

with an association constant of k=0.381 mol/kg at 25°C [130].

The molalities of dissociated and undissociated electrolyte species are related to the stoichiometric molality C by:

$$m_{H^+} + m_{HF_2^-} + m_{HF} = C \tag{A3.4}$$

and

$$m_{F^-} + 2m_{HF_2^-} + m_{HF} = C \tag{A3.5}$$

For ease of calculations, the ratios y and z are defined as:

$$y = m_{F^-}/C \tag{A3.6}$$

$$z = m_{HF_2^-}/C \tag{A3.7}$$

Therefore it follows from equations A3.4 and A3.5 that:

$$m_{HF} = C(1-y-2z) \tag{A3.8}$$

and $$m_{H^+} = C(y+z) \tag{A3.9}$$

The equilibrium constants may thus be expressed as:

$$K = \frac{a_{H^+}a_{F^-}}{a_{HF}} = \frac{m_{H^+}m_{F^-}\gamma_{H^+}\gamma_{F^-}}{m_{HF}\gamma_{HF}} = \frac{Cy(y+z)\gamma_{\pm}}{(1-y-2z)} \tag{A3.10}$$

and $$k = \frac{a_{HF}a_{F^-}}{a_{HF_2^-}} = \frac{m_{HF}m_{F^-}\gamma_{HF}\gamma_{F^-}}{m_{HF_2^-}\gamma_{HF_2^-}} = \frac{Cy(1-y-2z)}{z} \tag{A3.11}$$

where a and γ are the activities and activity coefficients respectively, $\gamma_{\pm}$ is the mean activity coefficient equal to $(\gamma_{H^+}\gamma_{F^-})^{1/2}$, and γ_{HF} in equation A3.10 and $(\gamma_{HF}\gamma_{F^-})/\gamma_{HF2^-}$ in equation A3.11 are taken equal to 1. $\gamma_{\pm}$ is evaluated by the extended Debye-Hückel law [131]:

$$-\log\gamma_{\pm} = Az_+z_- \frac{\sqrt{I}}{1+Ba\sqrt{I}} \tag{A3.12}$$

where A and B equal 0.5115 and 0.328 respectively for aqueous solutions at 25°C, z_+ and z_- are the ionic charges which equal one for binary electrolytes, 'a' is an adjustable parameter which roughly corresponds to the size of the hydrated ions (in angstrom units) and is taken as 6Å for HF (9Å for H^+, 3Å for F^-), and I is the ionic strength given as:

$$I = (m_{H^+} + m_{F^-} + m_{HF_2^-})/2 = C(y+z) \tag{A3.13}$$

Equation A3.11 is solved for z to obtain:

$$z = \frac{C(y-y^2)}{2Cy+k} \tag{A3.14}$$

and equations A3.12, A3.13, and A3.14 are combined to obtain:

$$\gamma_{\pm} = 10^{\left[-0.5115 \frac{\sqrt{Cy + \frac{C(y - y^2)}{2Cy + k}}}{1 + 1.968\sqrt{Cy + \frac{C(y - y^2)}{2Cy + k}}} \right]} \qquad \text{(A3.15)}$$

Equations A3.10 and A3.11 are combined to obtain:

$$\frac{K(1-y-2z)}{C\gamma_{\pm}^2} = y^2 + \frac{Cy^2(1-y-2z)}{k} \qquad \text{(A3.16)}$$

which, after substitution of equation A3.14 for z and rewriting, results in:

$$0 = \frac{Cy^2\gamma_{\pm}^2}{K\left[1 - y - \frac{2C(y - y^2)}{2Cy + k}\right]} + \frac{C^2y^2\gamma_{\pm}^2}{Kk} - 1 \qquad \text{(A3.17)}$$

Equations A3.15 and A3.17 are then solved by iteration, by guessing a value for y to solve for $\gamma_{\pm}$, and using the result in equation A3.17 to obtain a better value for y, etc.. After solving for y, values for I, $\gamma_{\pm}$, and the molalities of F^-, H^+, HF_2^-, and undissociated HF are calculated using the appropriate equations above.

Calculated values are presented in table 4.4.

A4 Bulk Silicon Etching Characteristics

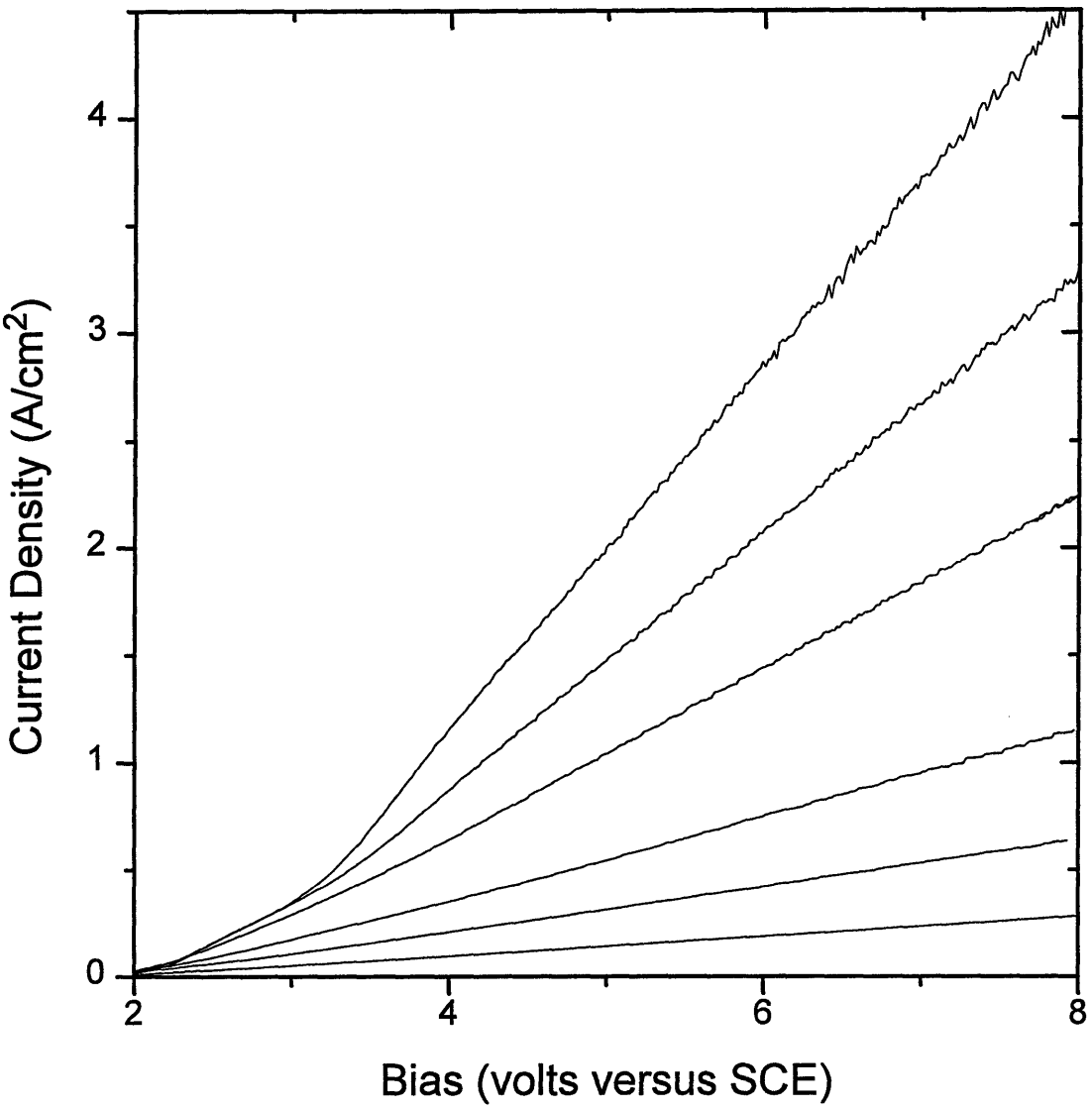


Figure A4.1. Current-voltage sweeps of the PEC cell as a function of electrolyte HF concentrations using a platinum foil working electrode and the 0.075 cm^2 teflon sample seal. Electrolyte cell resistances are: 285.4Ω, 122.3Ω, 66.14Ω, 33.34Ω, 22.24Ω, and 15.65Ω for the 1%, 2.5%, 5%, 10%, 15%, and 20% HF concentrations respectively.

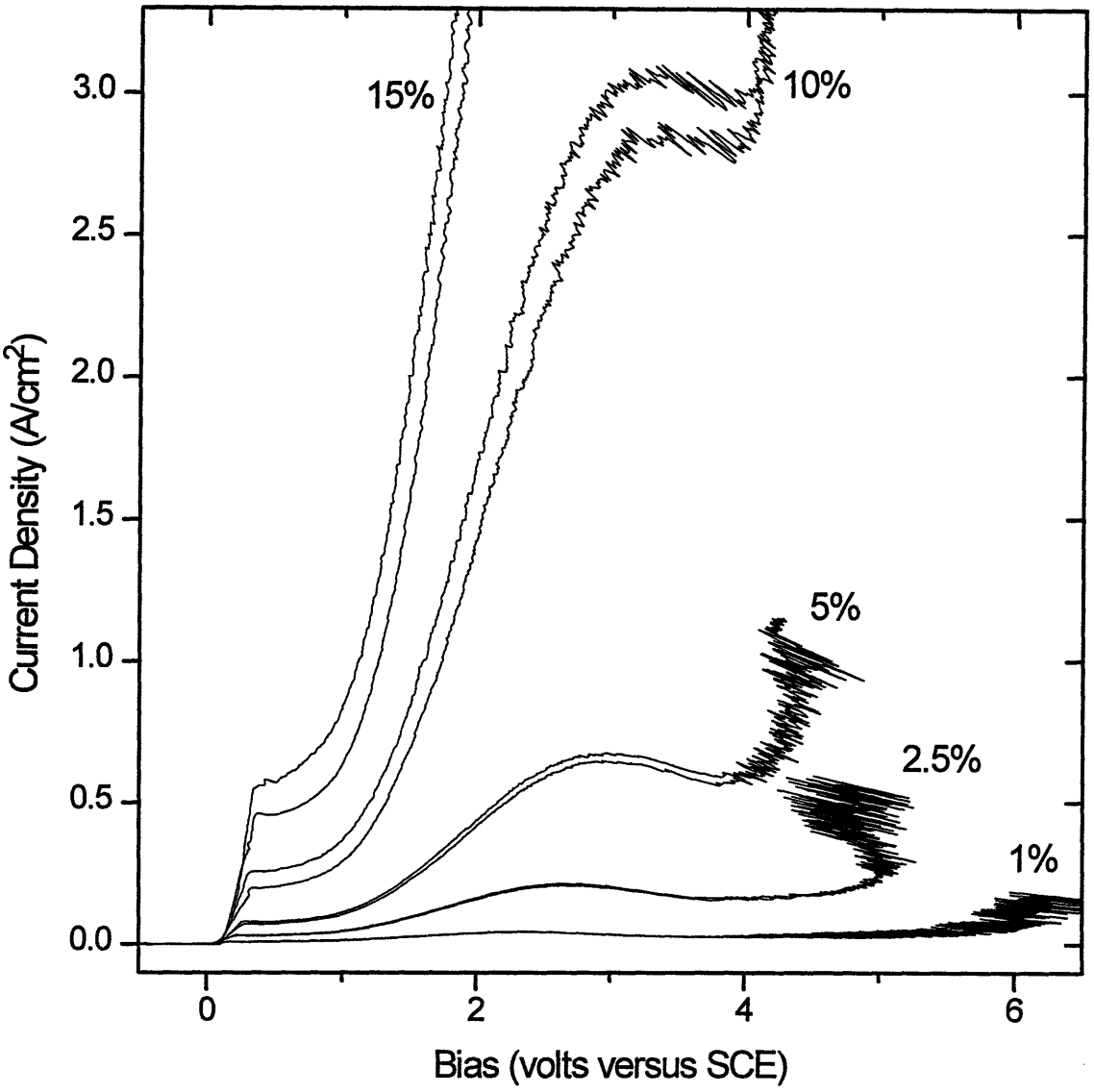


Figure A4.2. Current Voltage characteristics of 5Ωcm p-Si as shown in figure 5.1 but after compensating for the electrolyte IR voltage drop.

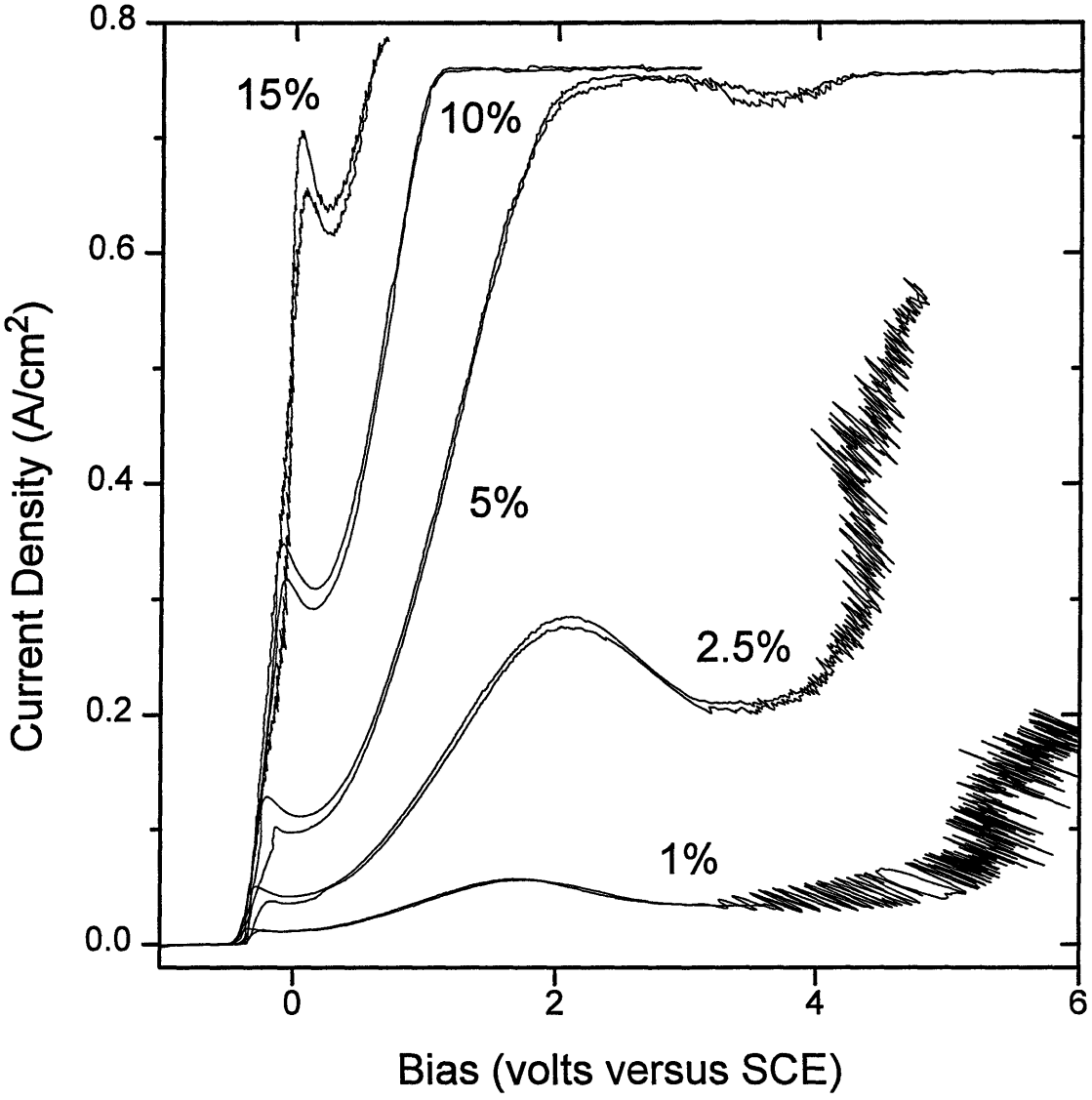


Figure A4.3. Current-Voltage characteristics of 5Ωcm n-Si as shown in figure 5.2 but after compensating for the electrolyte IR voltage drop.

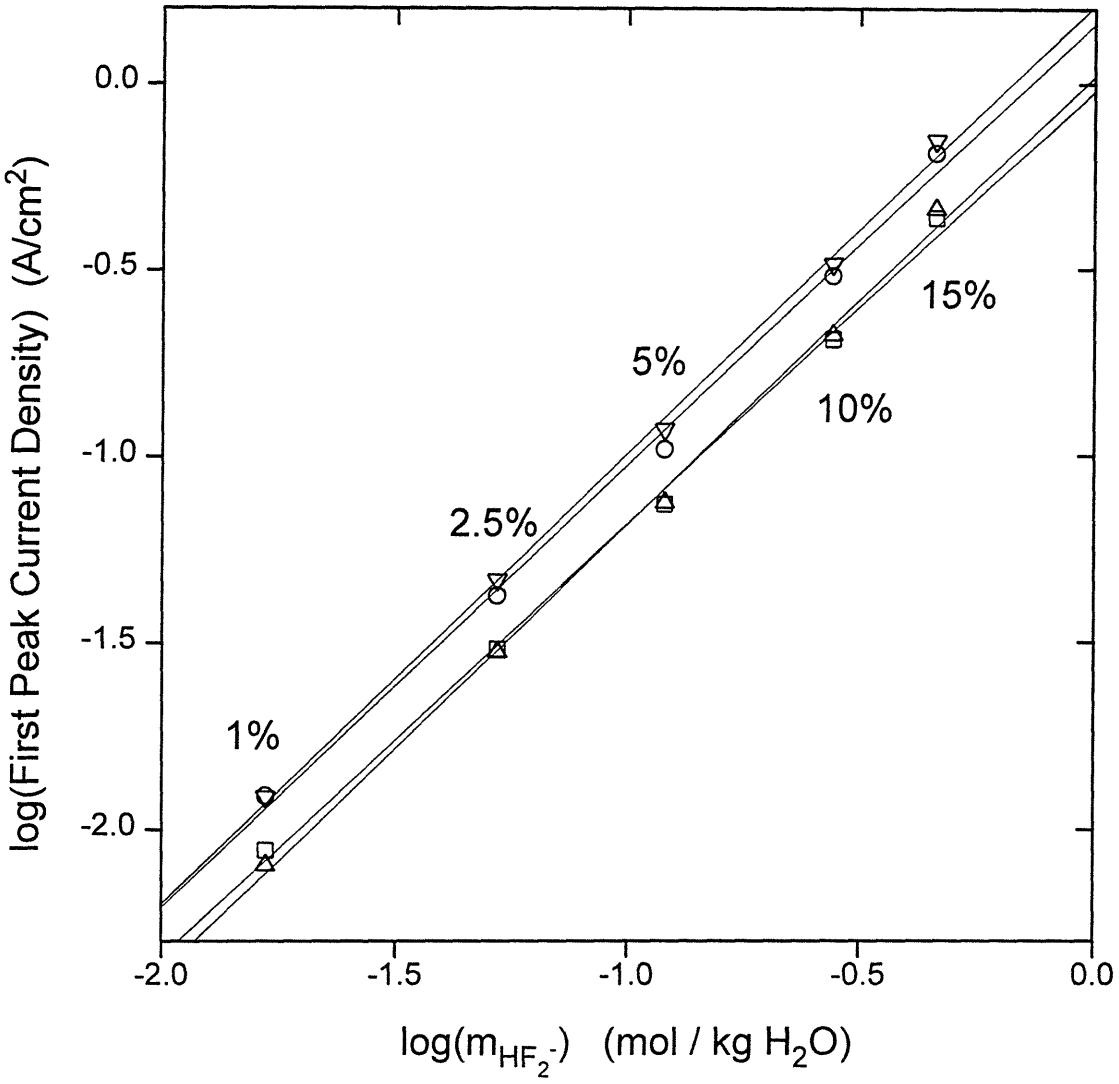


Figure A4.4. Log-Log plot of first-peak current densities of 5Ωcm n- and p-Si as a function of electrolyte HF_2^- molality. Lines show best fit slopes for n in $I \propto [HF_2^-]^n$.

( ) 5Ωcm p-Si, forward sweep, n=1.16
(Δ) 5Ωcm p-Si, reverse sweep, n=1.21
(O) 5Ωcm n-Si, forward sweep, n=1.18
(∇) 5Ωcm n-Si, reverse sweep, n=1.21

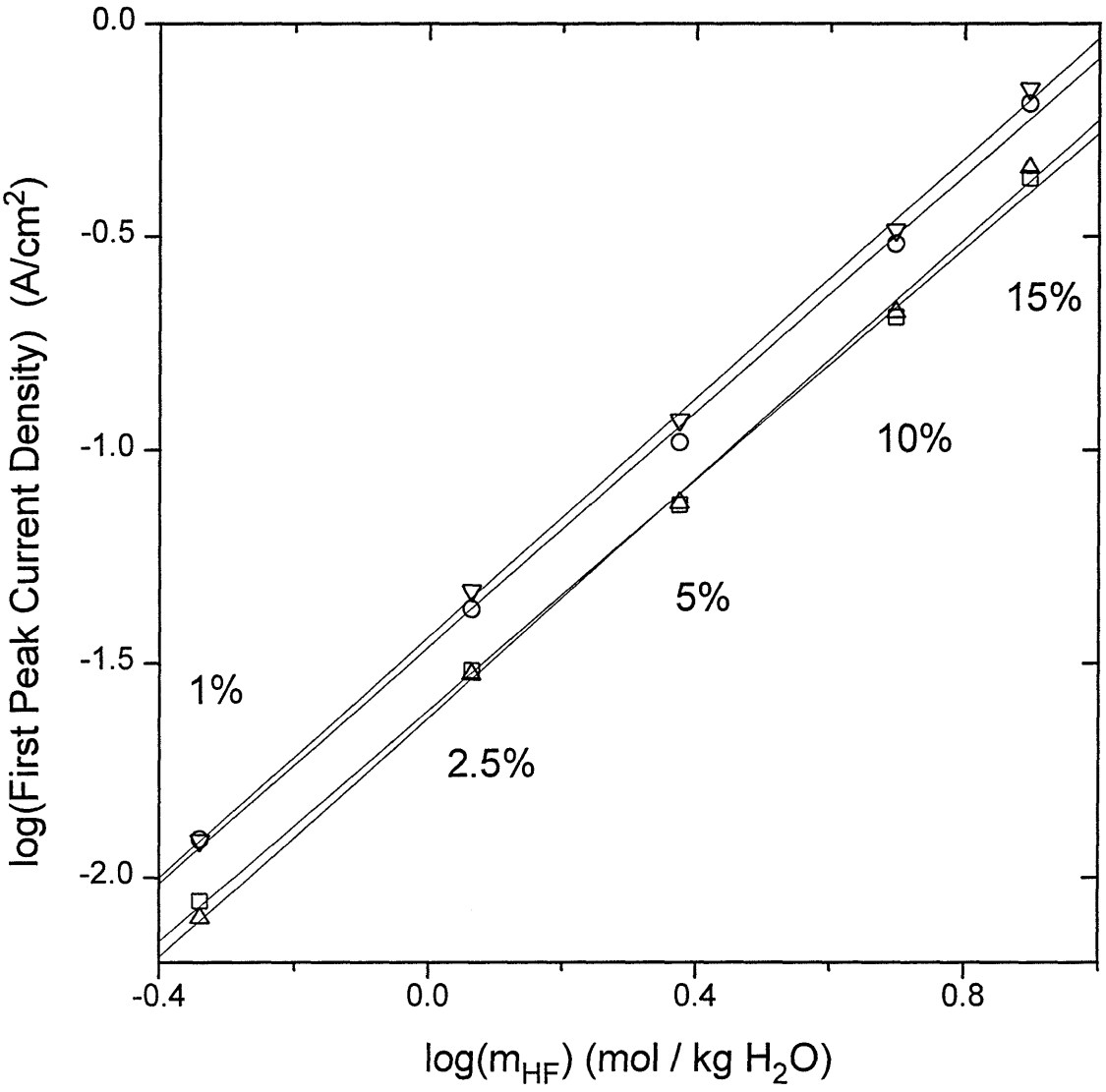


Figure A4.5. Log-Log plot of first-peak current densities of 5Ωcm n- and p-Si as a function of electrolyte $HF_{undissociated}$ molality. Lines show best fit slopes for n in $I \propto [HF_{undissociated}]^n$.

( ) 5Ωcm p-Si, forward sweep, n=1.35
(Δ) 5Ωcm p-Si, reverse sweep, n=1.40
(O) 5Ωcm n-Si, forward sweep, n=1.38
(∇) 5Ωcm n-Si, reverse sweep, n=1.40

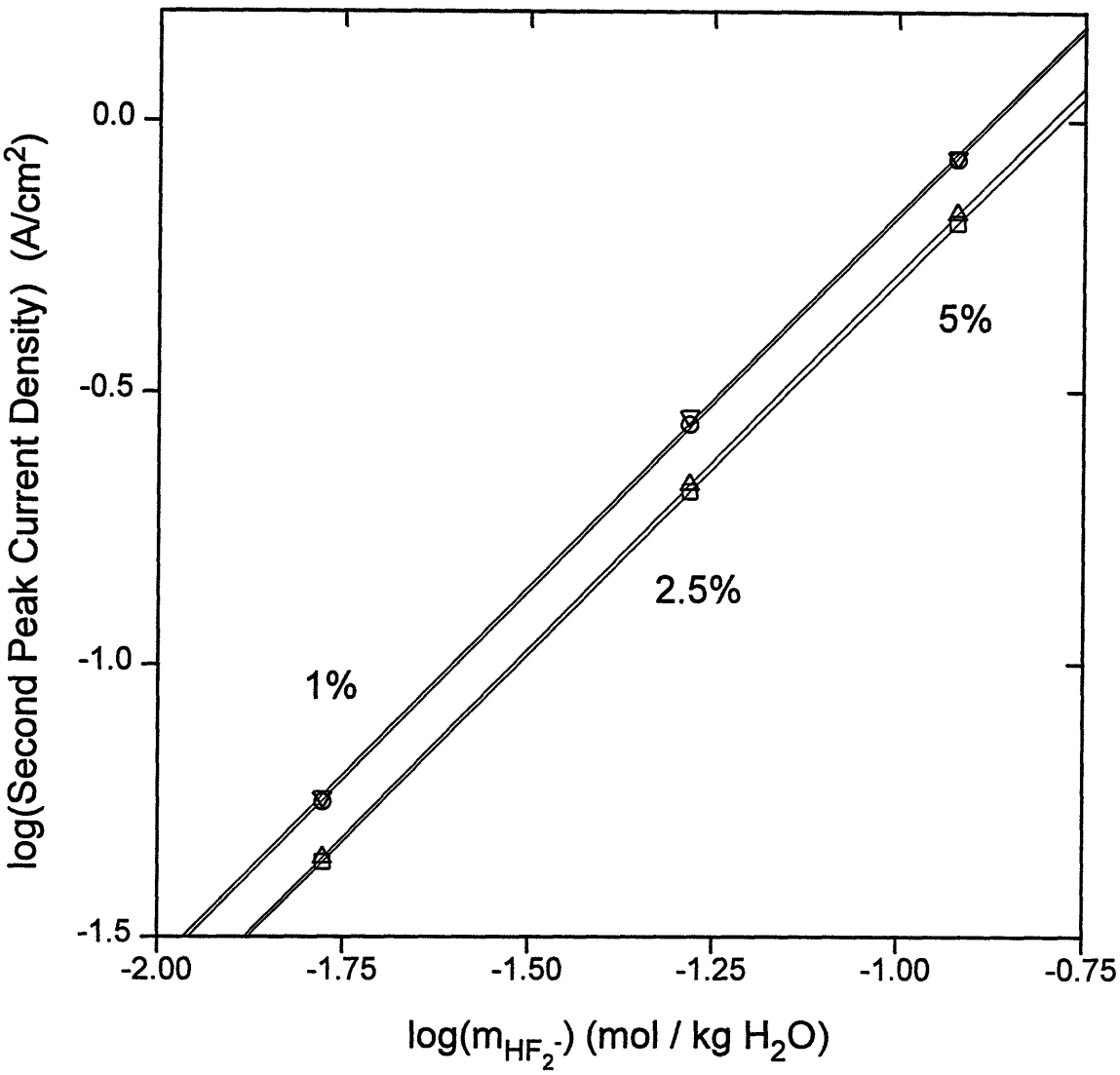


Figure A4.6. Log-Log plot of second-peak current densities of 5Ωcm n- and p-Si as a function of electrolyte HF_2^- molality. Lines show best fit slopes for n in $I \propto [HF_2^-]^n$.

( ) 5Ωcm p-Si, forward sweep, n=1.37 (Δ) 5Ωcm p-Si, reverse sweep, n=1.38

(O) 5Ωcm n-Si, forward sweep, n=1.38 (∇) 5Ωcm n-Si, reverse sweep, n=1.38

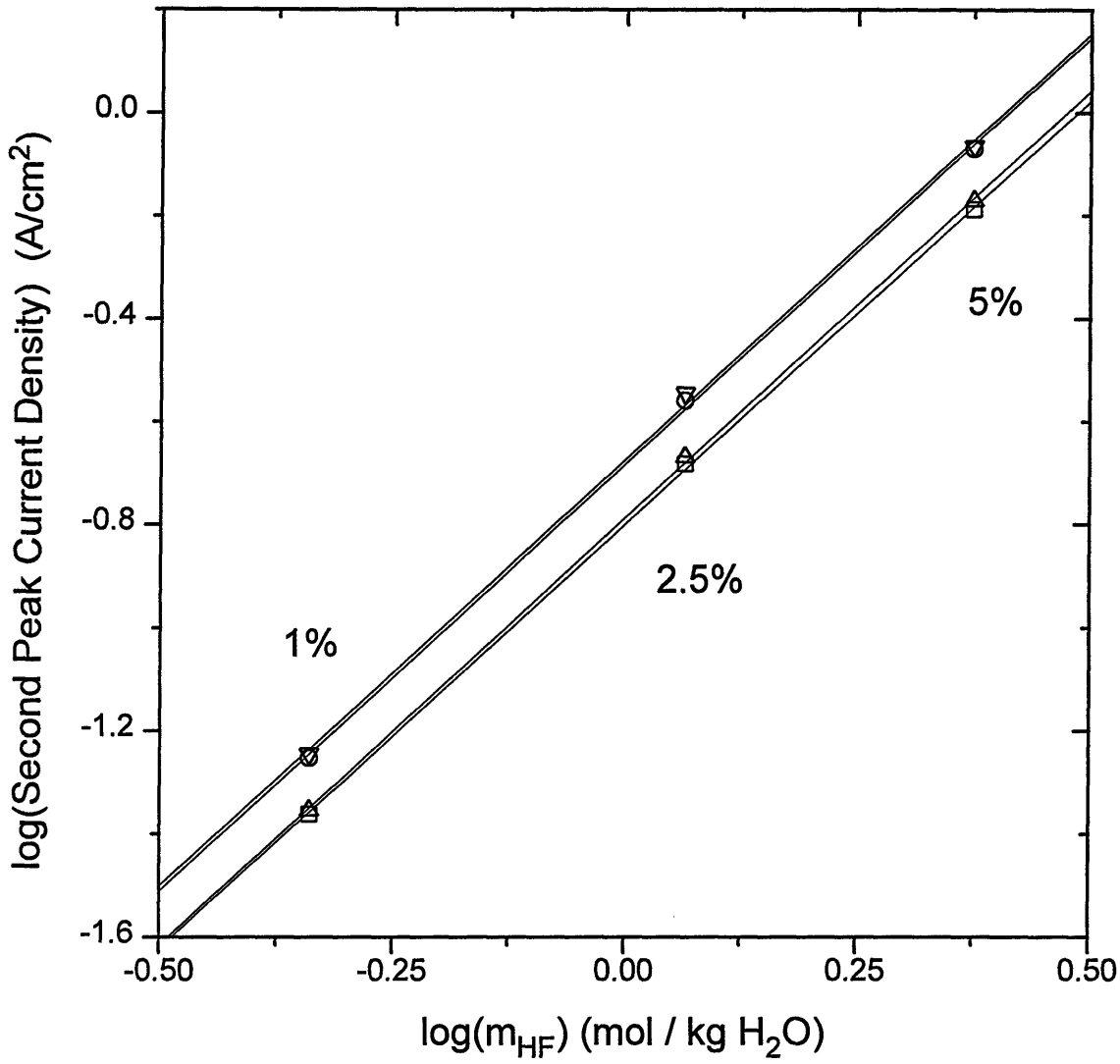


Figure A4.7. Log-Log plot of second-peak current densities of 5Ωcm n- and p-Si as a function of electrolyte $HF_{undissociated}$ molality. Lines show best fit slopes for n in $I\alpha[HF_{undissociated}]^n$.

( ) 5Ωcm p-Si, forward sweep, n=1.64
(Δ) 5Ωcm p-Si, reverse sweep, n=1.66
(O) 5Ωcm n-Si, forward sweep, n=1.66
(∇) 5Ωcm n-Si, reverse sweep, n=1.65

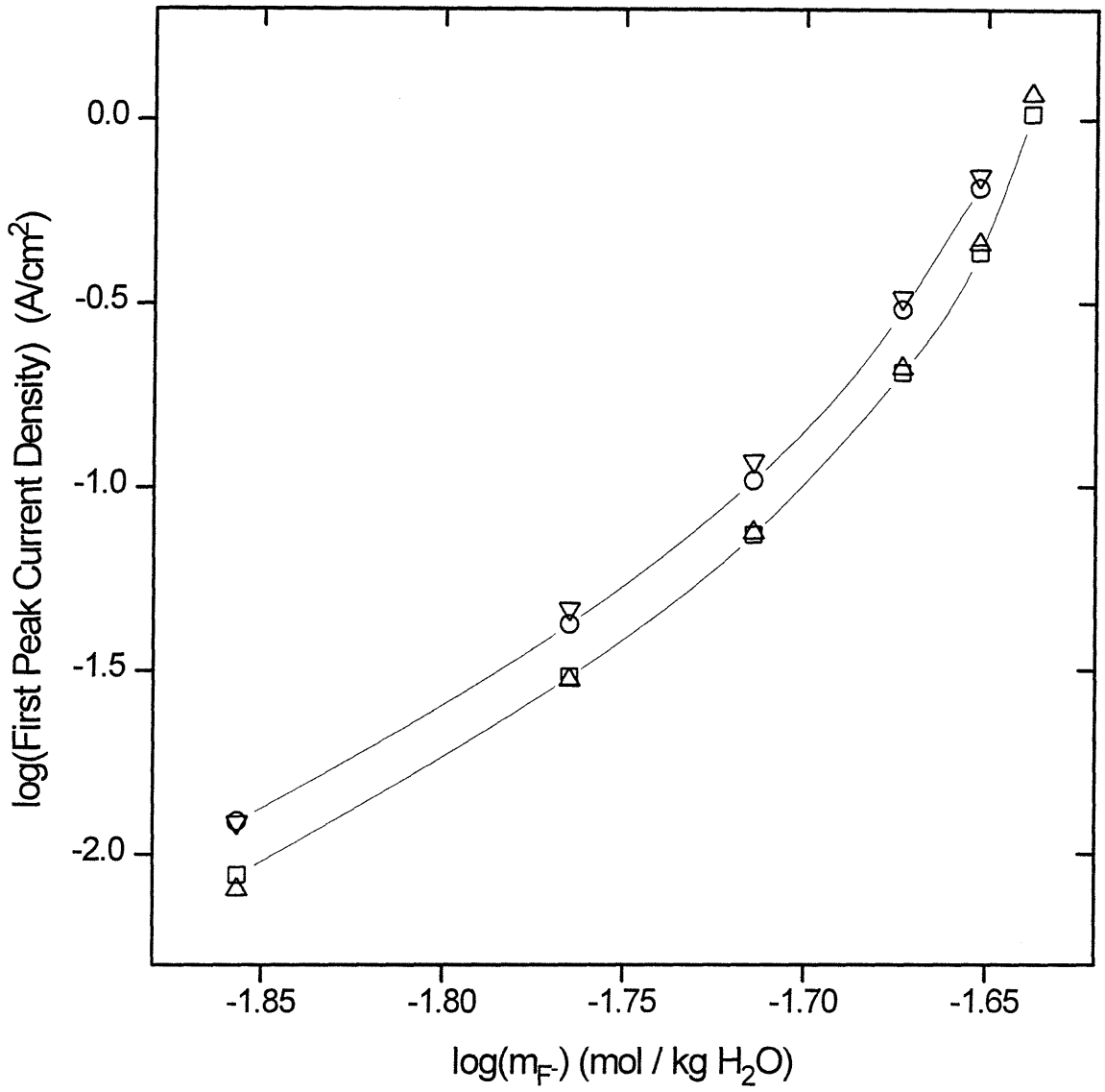


Figure A4.8. Log-Log plot of first-peak current densities of 5Ωcm n- and p-Si as a function of electrolyte F^- molality.

( ) 5Ωcm p-Si, forward sweep
(Δ) 5Ωcm p-Si, reverse sweep
(O) 5Ωcm n-Si, forward sweep
(∇) 5Ωcm n-Si, reverse sweep

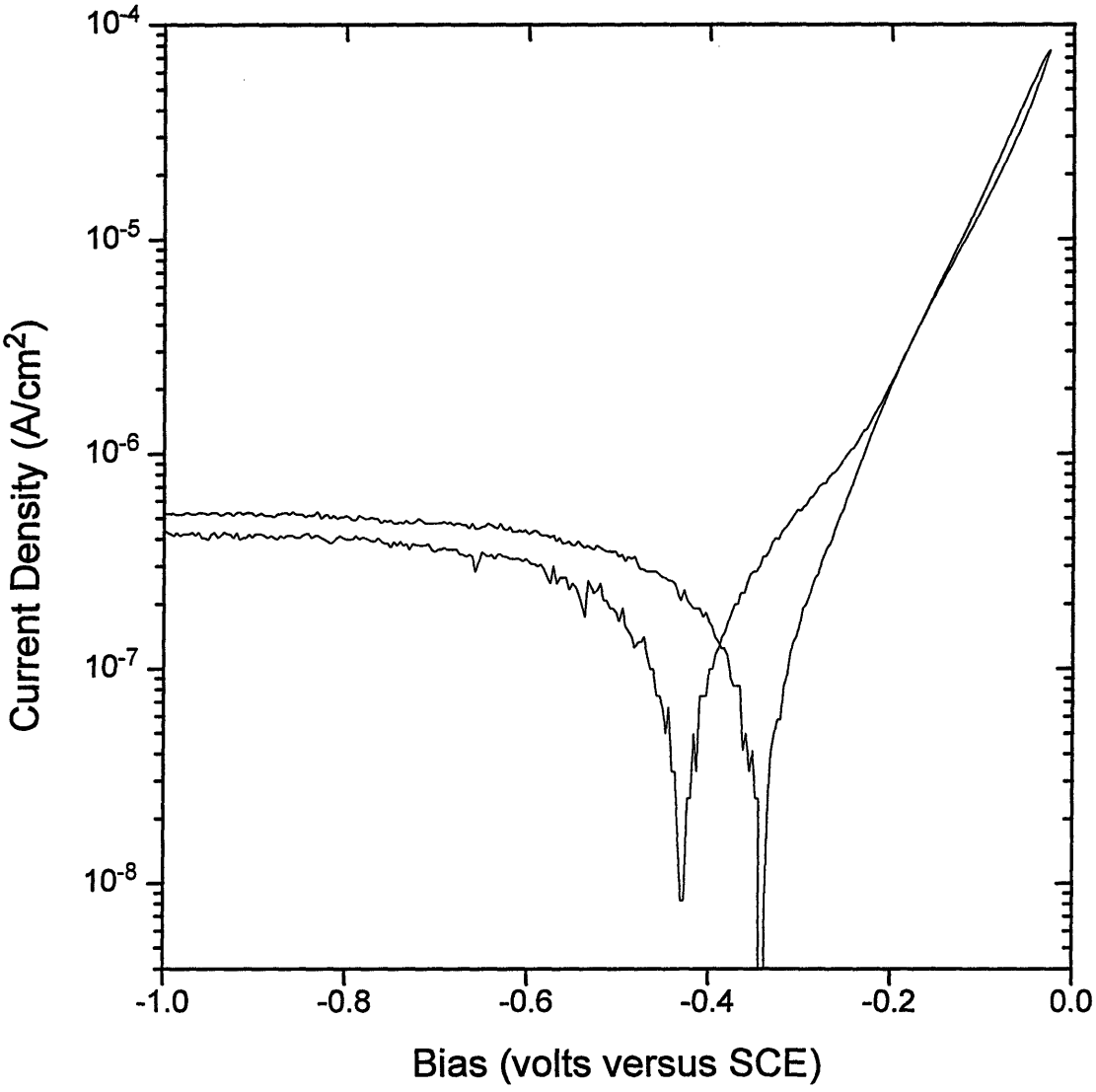


Figure A4.9. Current-voltage characteristics of 5Ωcm n-Si showing the zero current potential of ≈ -0.4 V (SCE). Measured using 5% HF, no electrolyte flow rate, and 10mV/s sweep rate.

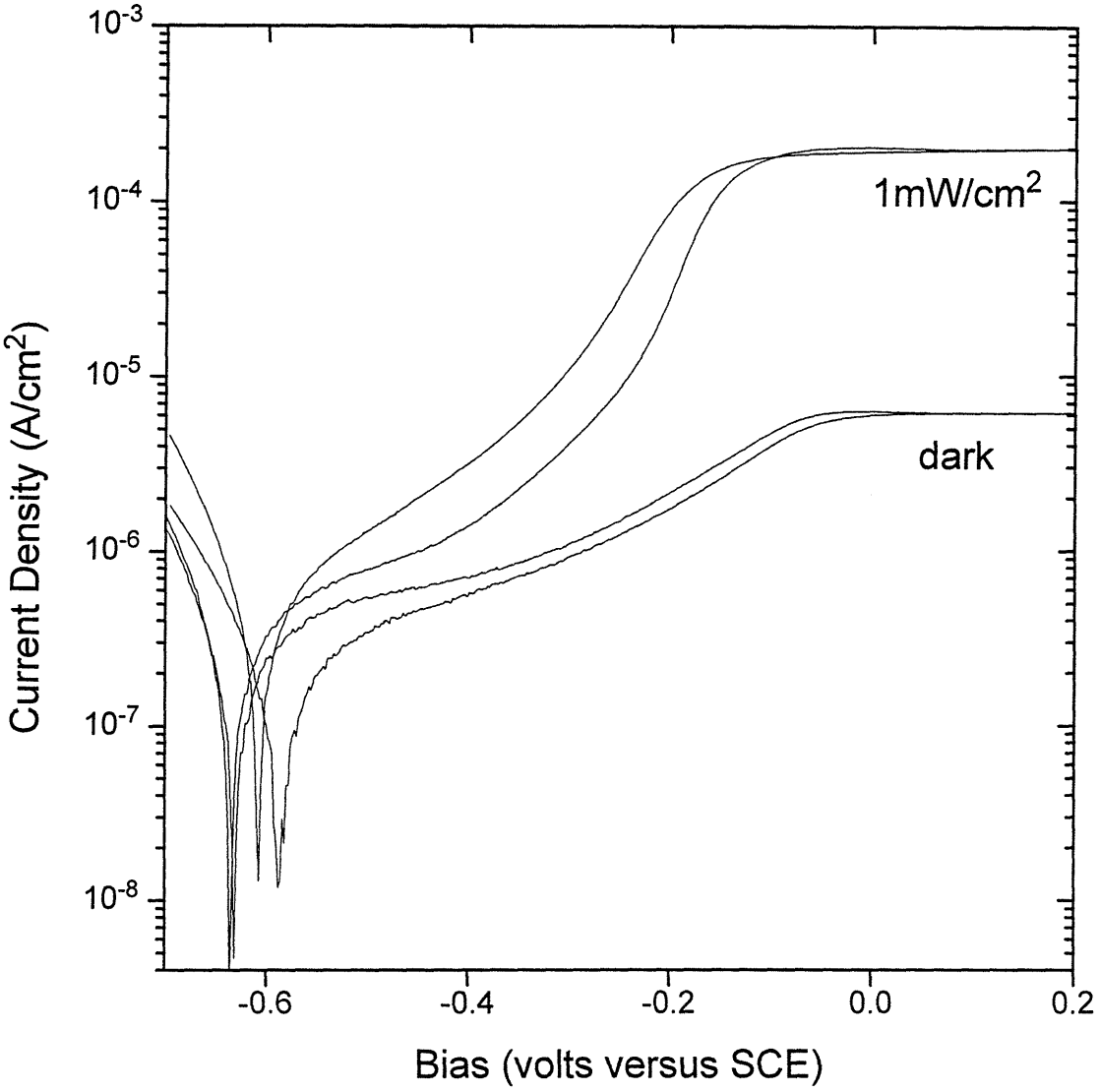


Figure A4.10. Current-voltage characteristics for weakly illuminated and unilluminated 5Ωcm n-Si showing the zero current potential of ≈ -0.6 V (SCE). Measured using 5% HF, no electrolyte flow rate, and 10mV/s sweep rate.

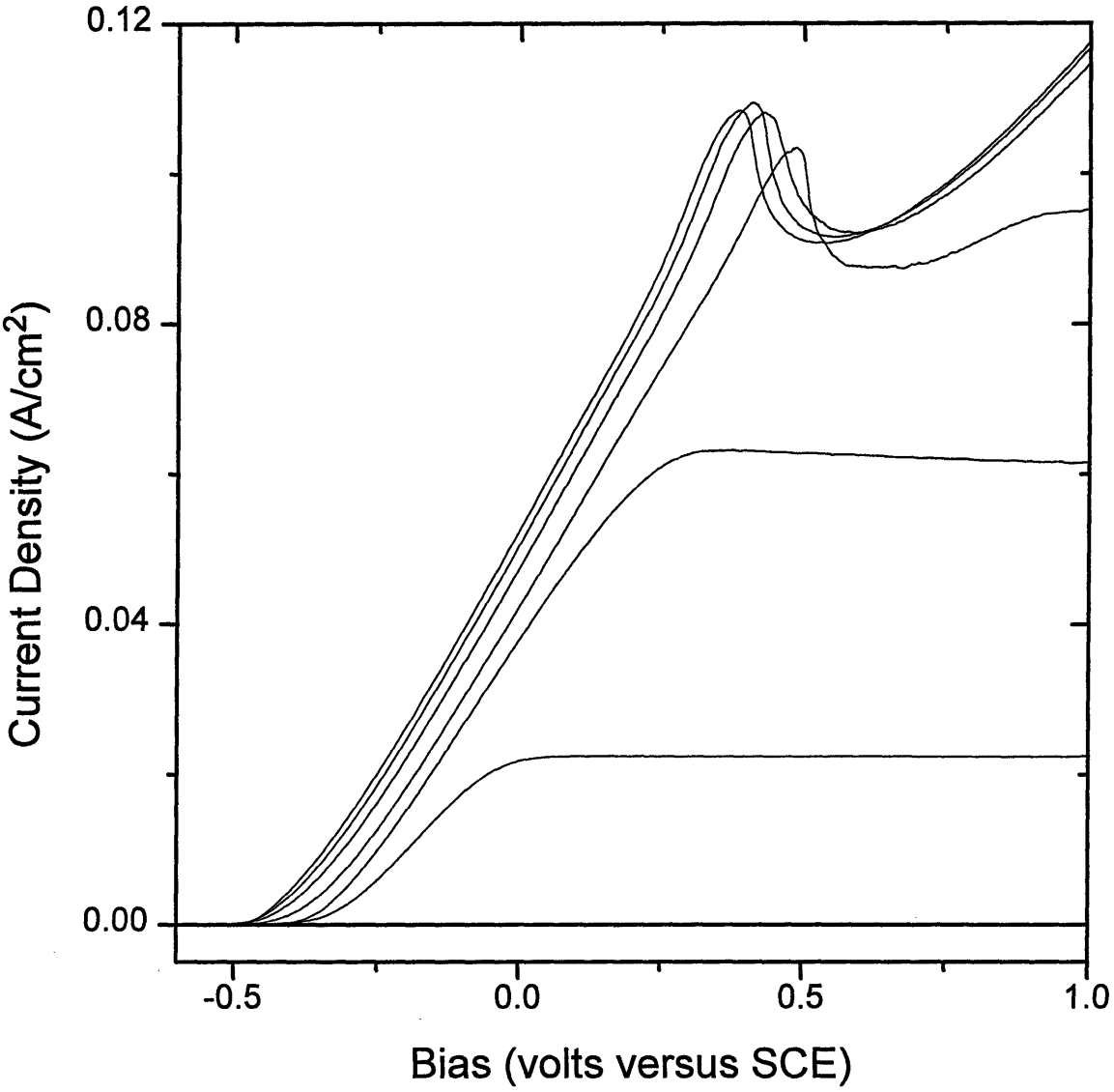


Figure A4.11. Current-voltage characteristics of 5Ωcm n-Si as a function of illumination intensity, measured using 5% HF, 600mL/min electrolyte flow rate, and 20mV/s sweep rate. Illumination intensities are 32.6, 87.1, 187, 490, 773, 1140, and 1420 mW/cm^2.

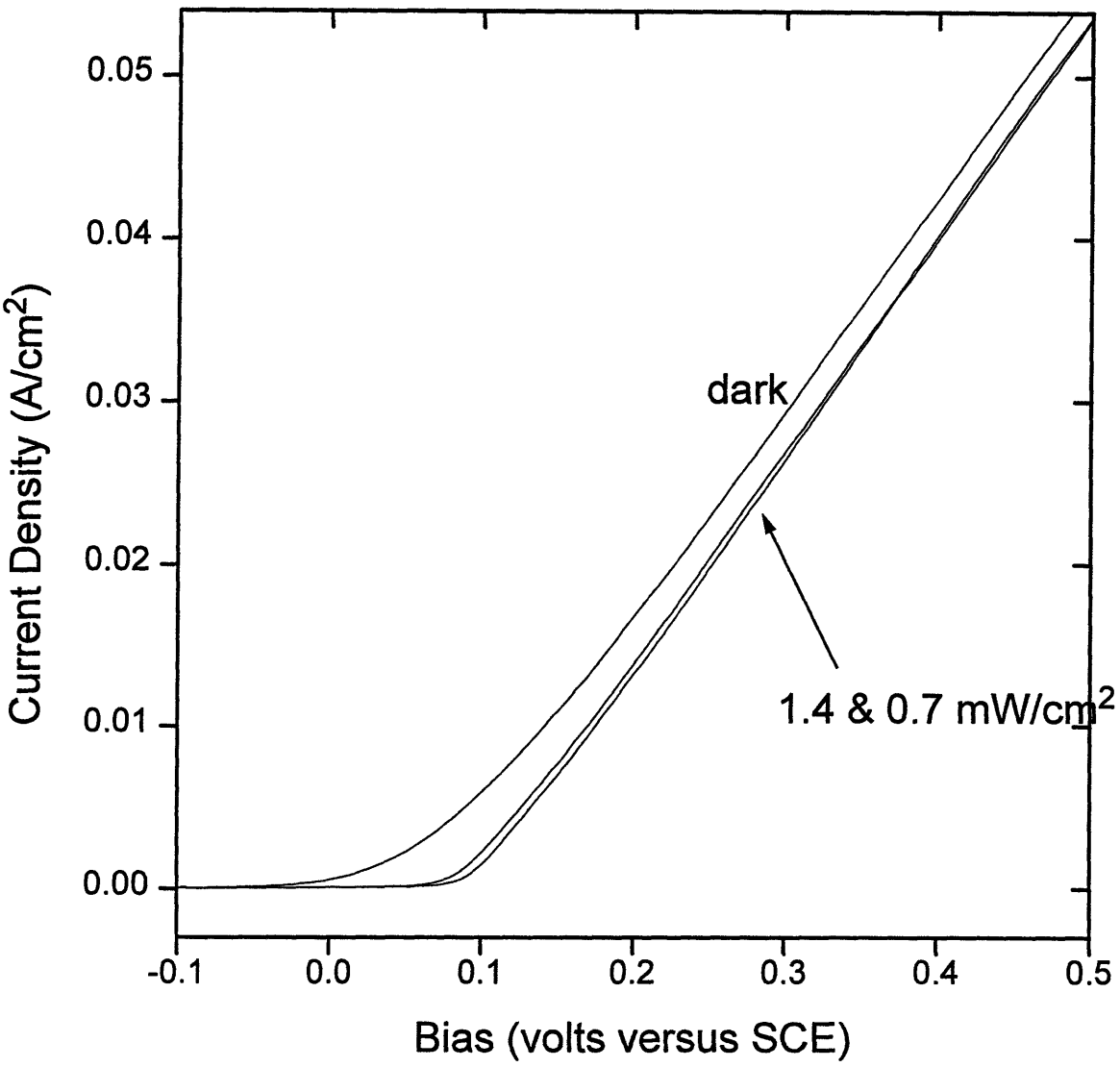


Figure A4.12. Current-voltage characteristics of 5Ωcm p-Si as a function of illumination intensity, measured using 5% HF, 600mL/min electrolyte flow rate, and 20mV/s sweep rate.

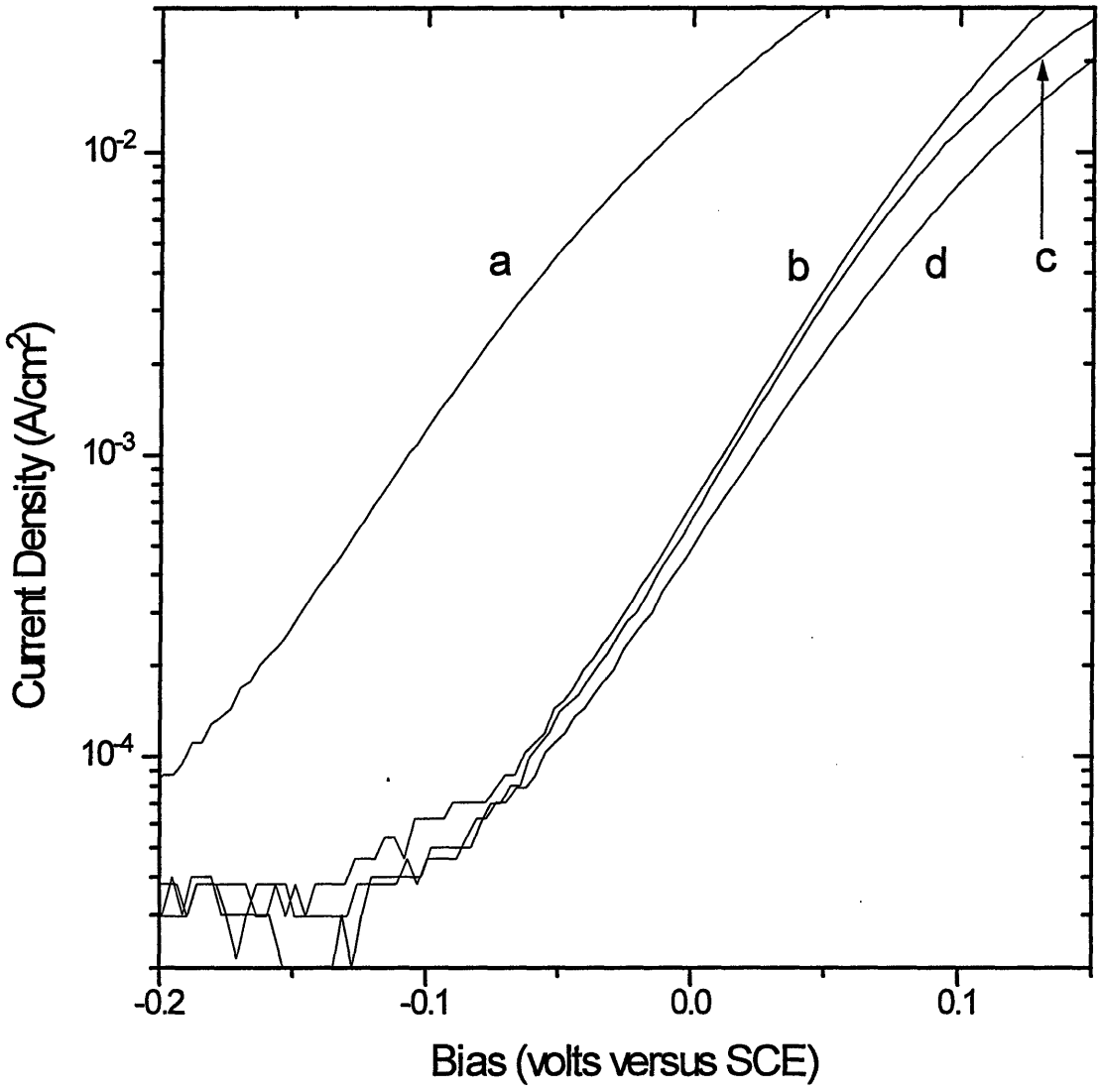


Figure A4.13. Current-voltage characteristics of boron doped (100) p-Si as a function of doping density after compensating for electrolyte IR voltage drop. Measured using 5% HF, 600mL/min electrolyte flow rate, and 20mV/s sweep rate.
a) .007 Ωcm, b) 1.04 Ωcm, c) 5.06 Ωcm. d) 19.3 Ωcm.

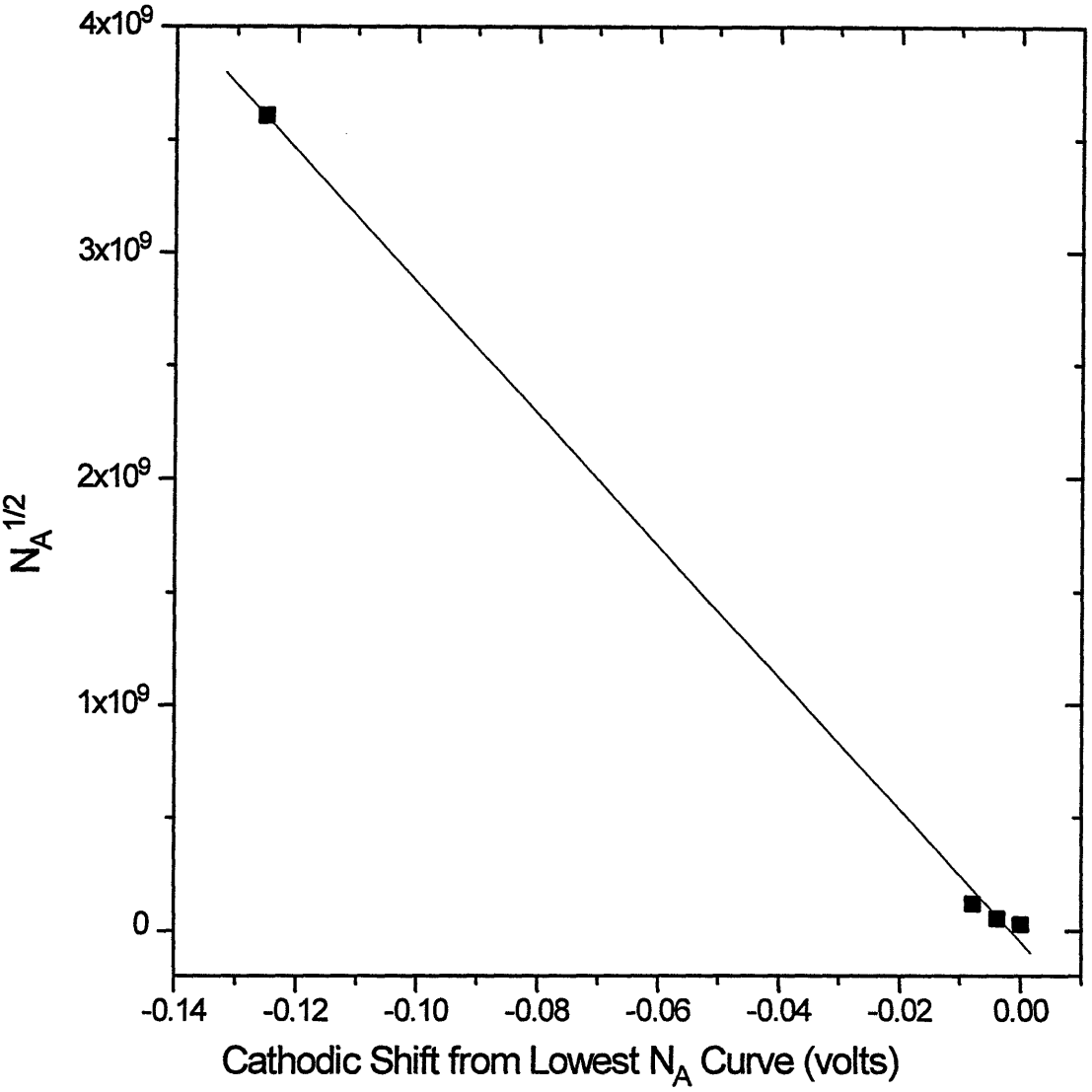


Figure A4.14. A plot of $(N_A)^{1/2}$ for the p-Si samples shown in figure A4.13 as a function of the shift in current-voltage characteristics from those of the right-most curve.

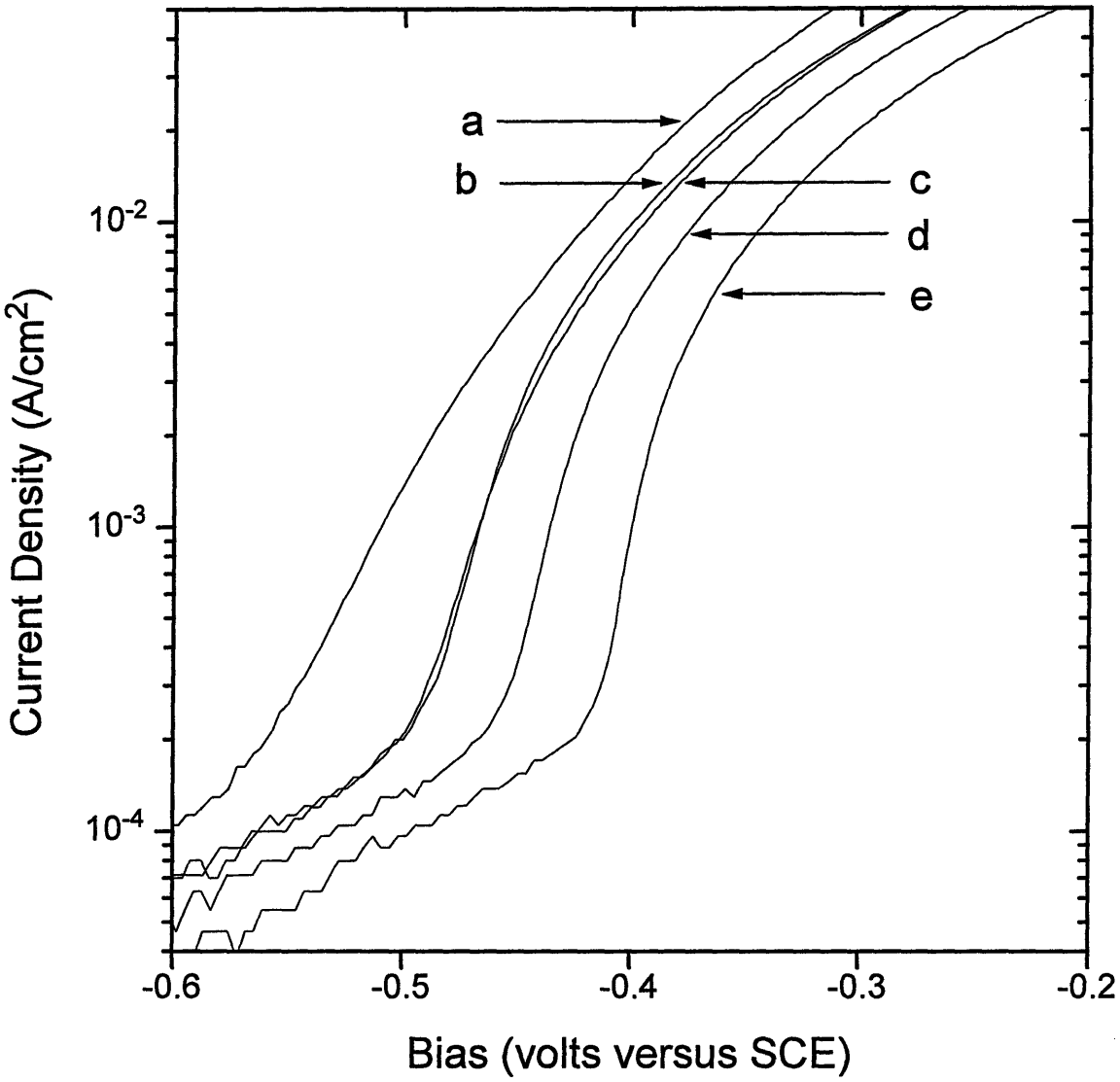


Figure A4.15. Current-voltage characteristics of phosphorous doped (100) n-Si as a function of doping density after compensating for electrolyte IR voltage drop. Measured using 1420mW/cm^2 white light illumination, 5% HF, 600mL/min electrolyte flow rate, and 20mV/s sweep rate. a) .067 Ωcm b) 1.04 Ωcm c) 5.14 Ωcm, d) 10.4 Ωcm e) 20.6 Ωcm f) 35.1 Ωcm.

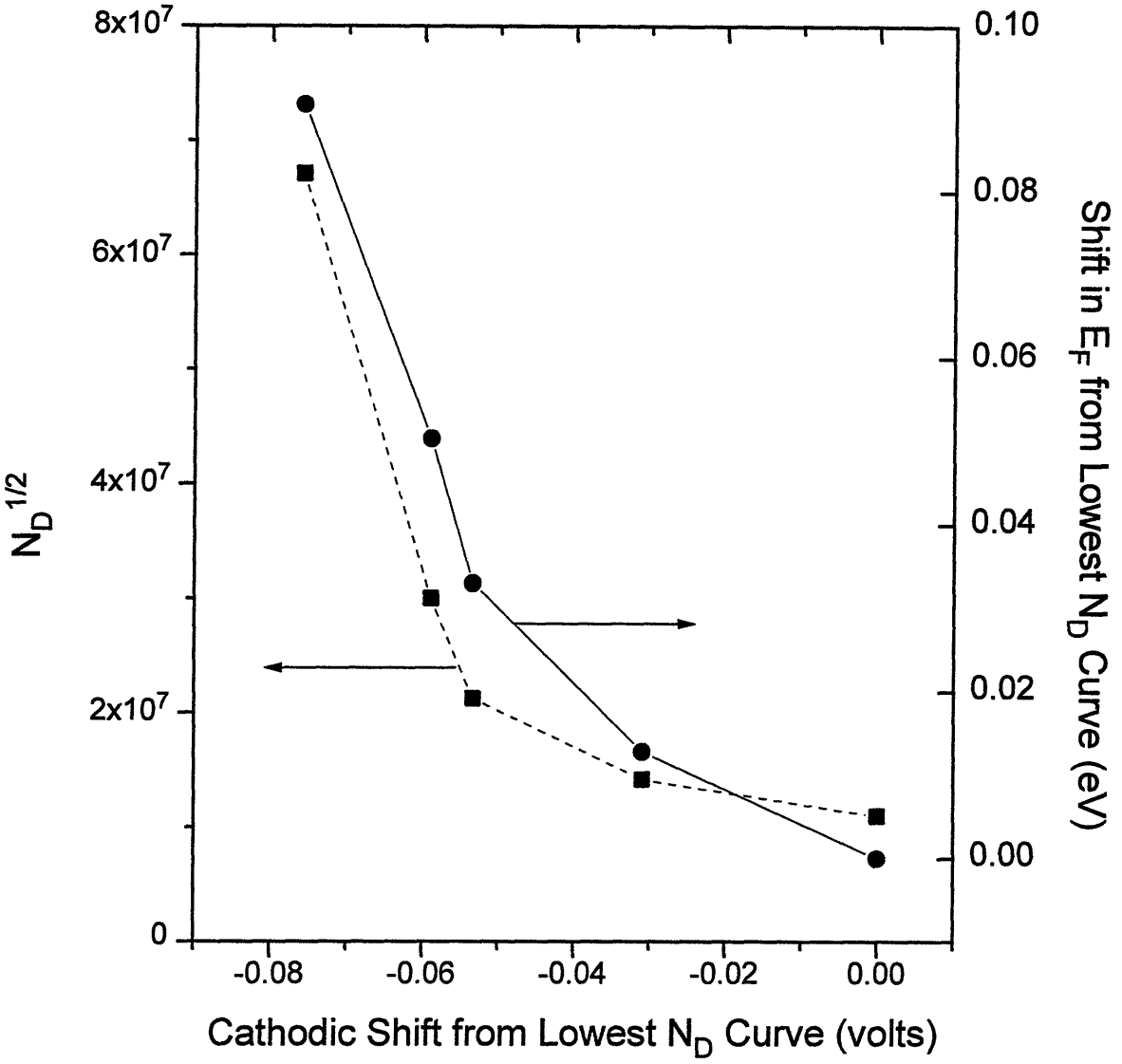


Figure A4.16. A plot of $(N_D)^{1/2}$ of the n-Si samples shown in figure A4.15 as a function of 1) the shift in the current-voltage characteristics from the right-most curve (left-side y-axis), and 2) the shift in the Fermi energy from the right-most curve calculated by $\Delta E_F = kT[\ln(N_{D1}/n_i)-\ln(N_{D2}/n_i)]$ (right-side y-axis).

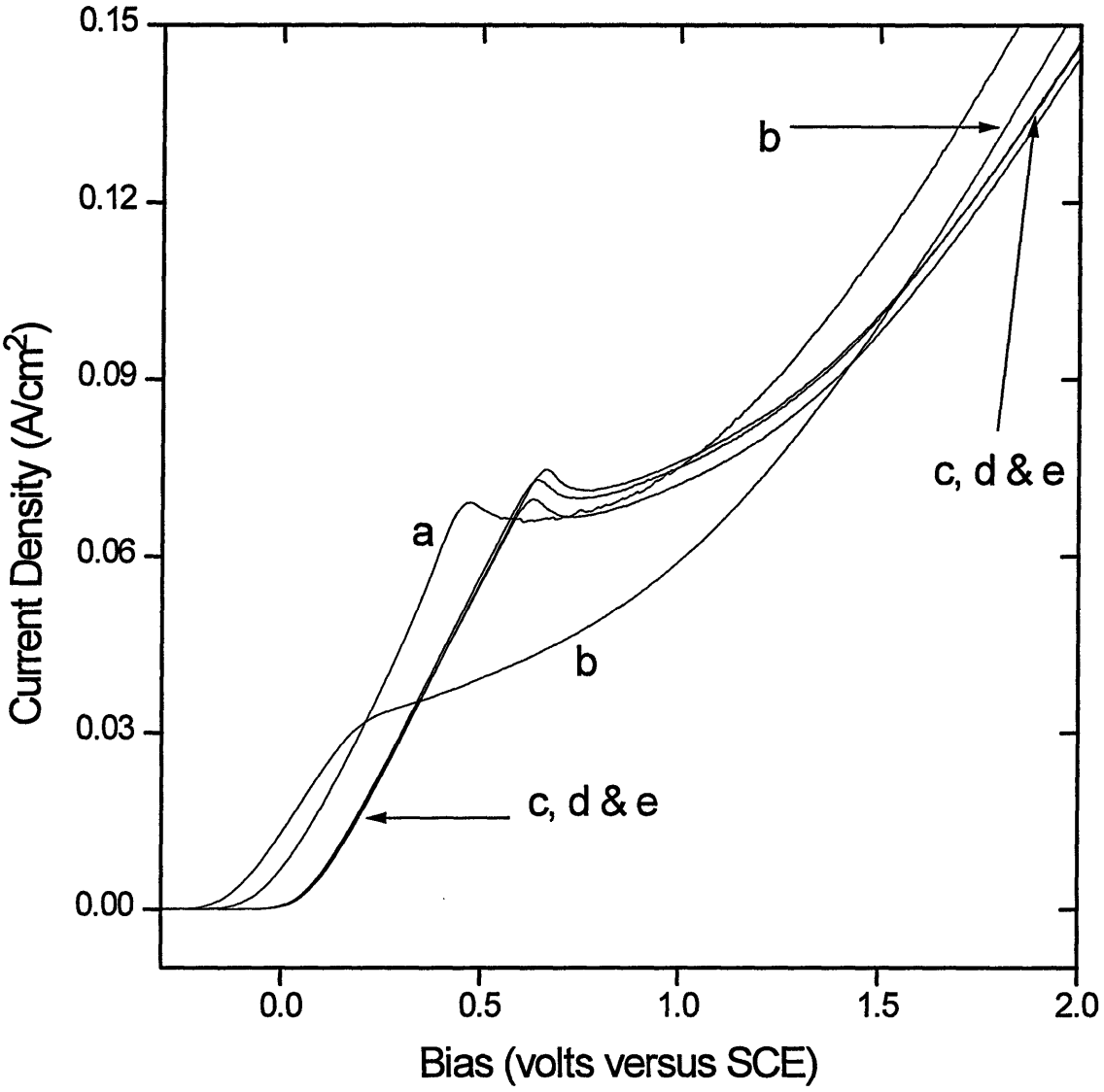


Figure A4.17. Current-voltage characteristics of boron doped p-Si showing the effect of crystallographic orientation, measured using 5% HF, 600mL/min electrolyte flow rate, and 20mV/s sweep rate. a) 0.007Ωcm (100), b) 0.002Ωcm (111), c) 5.06Ωcm (100), d) 0.7Ωcm (110), e) 7.0Ωcm (111).

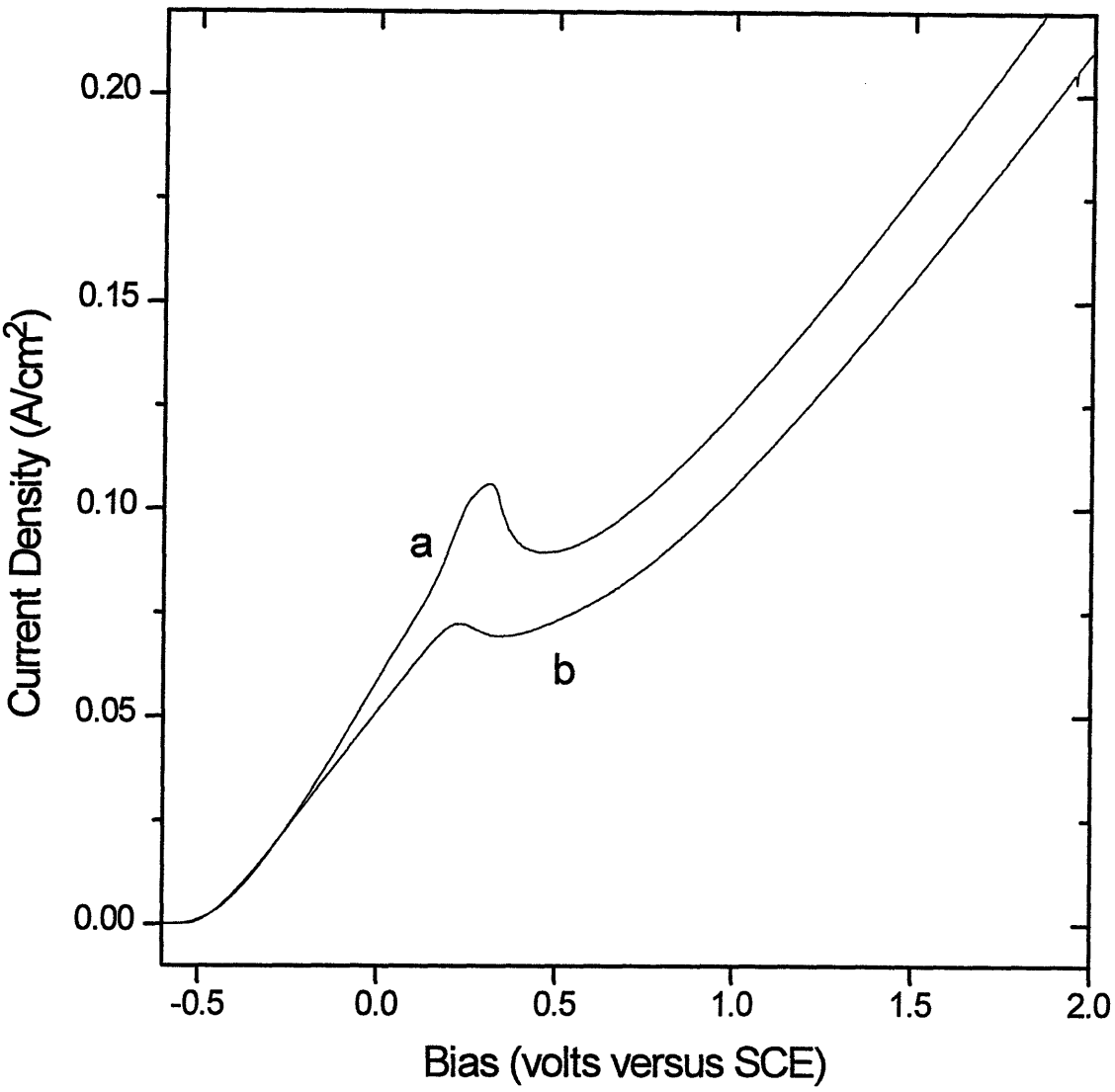


Figure A4.18. Current-voltage characteristics of phosphorous doped n-Si showing the effect of crystallographic orientation, measured using 1420mW/cm^2 white light illumination, 5% HF, 600mL/min electrolyte flow rate, and 20mV/s sweep rate. a) 1.04Ωcm (100), b) 3Ωcm (111).

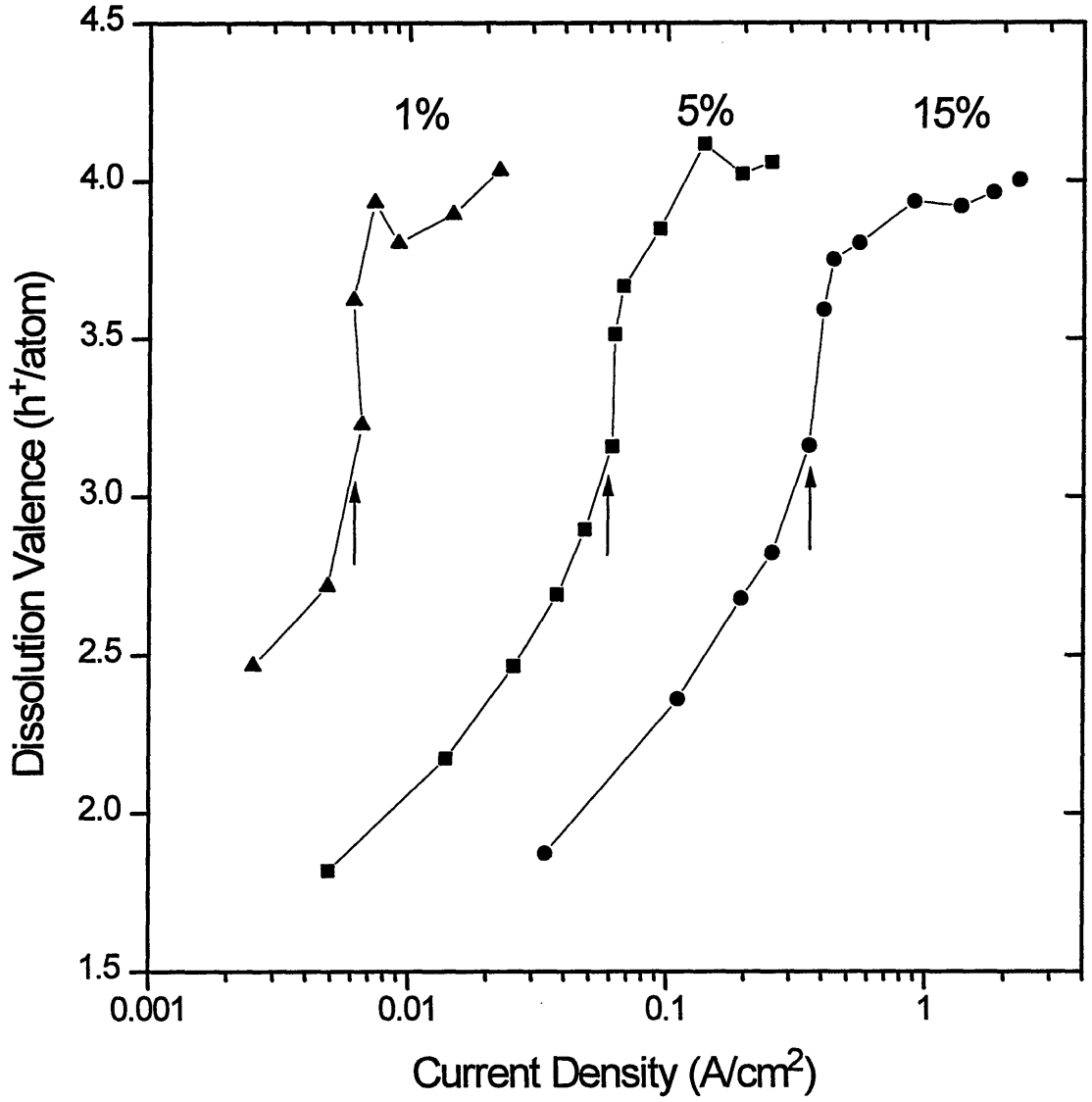


Figure A4.19. Dissolution valence for etching of 5Ωcm p-Si as a function of current density, in 1, 5, and 15% HF. Arrows indicate J_{crit}.

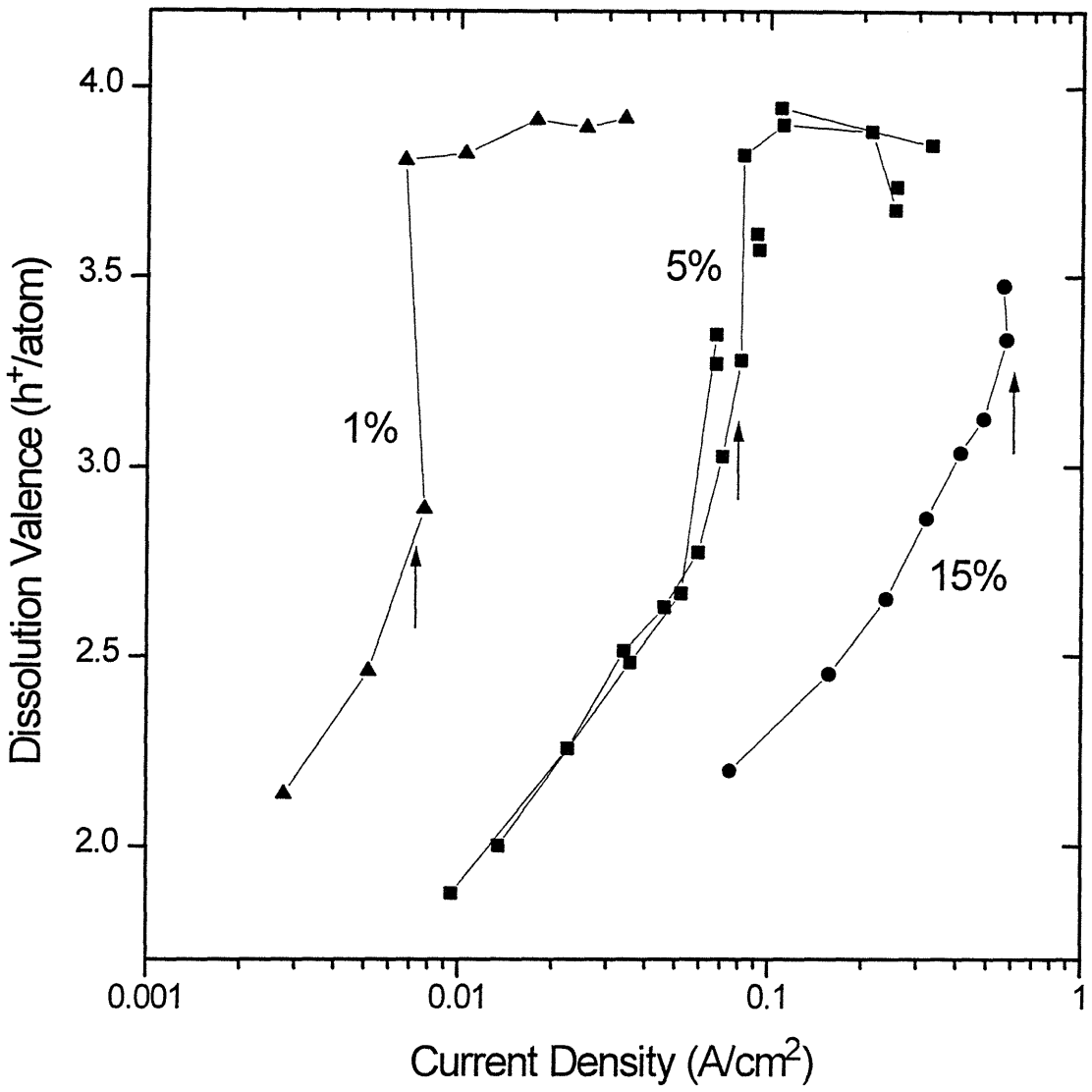


Figure A4.20. Dissolution valence for etching of 5Ωcm n-Si as a function of current density, in 1% HF and 187mW/cm^2 white light illumination, 15% HF and 1140mW/cm^2 white light illumination, and 5% HF and 773, 490, 187, and 87.2 mW/cm^2 white light illumination. Arrows indicate J_{crit}.

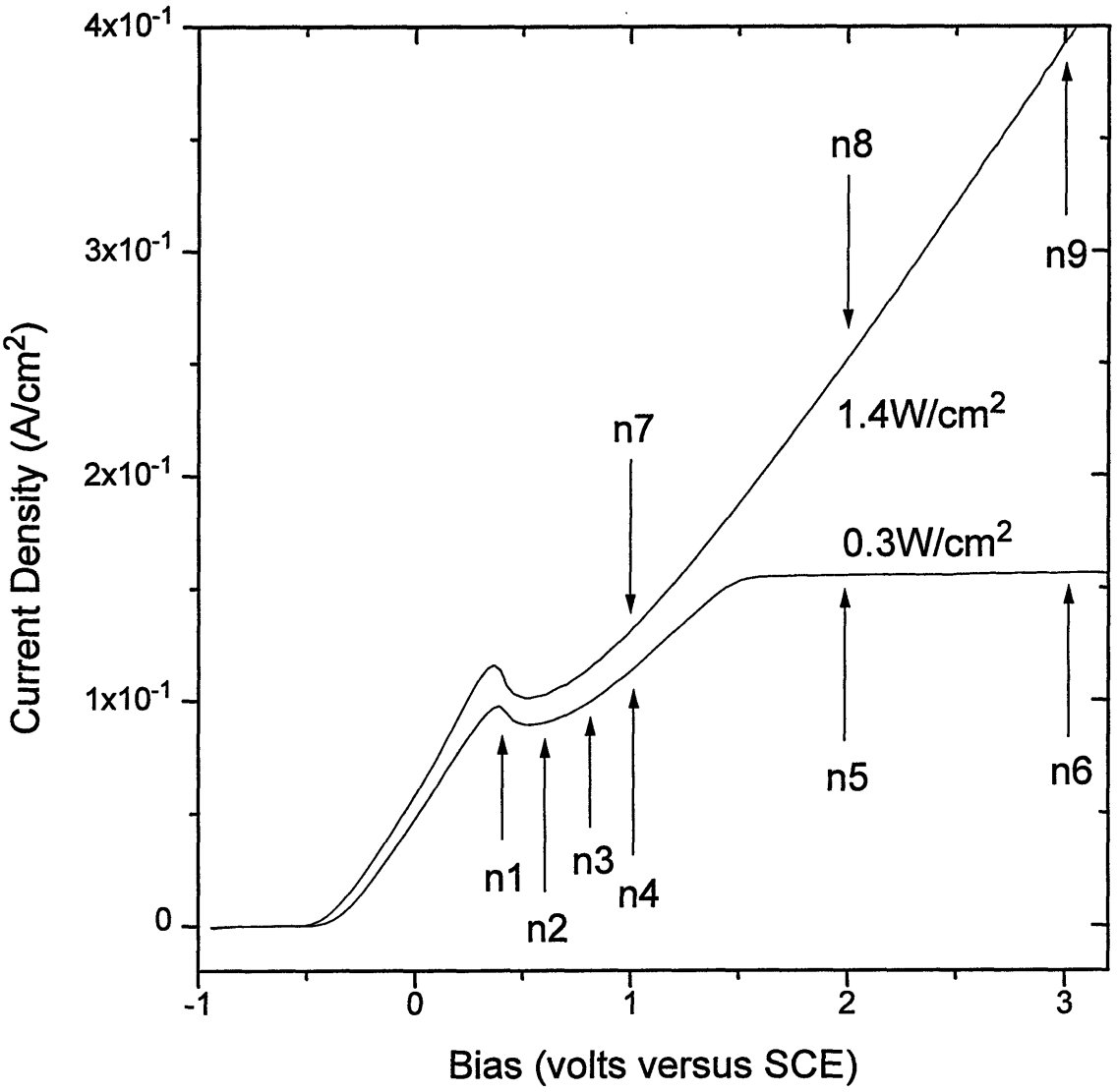


Figure A4.21. Current-voltage characteristics of 5Ωcm n-Si illuminated with white light as indicated showing the potentials at which samples where etched before measuring the resulting surface smoothness.

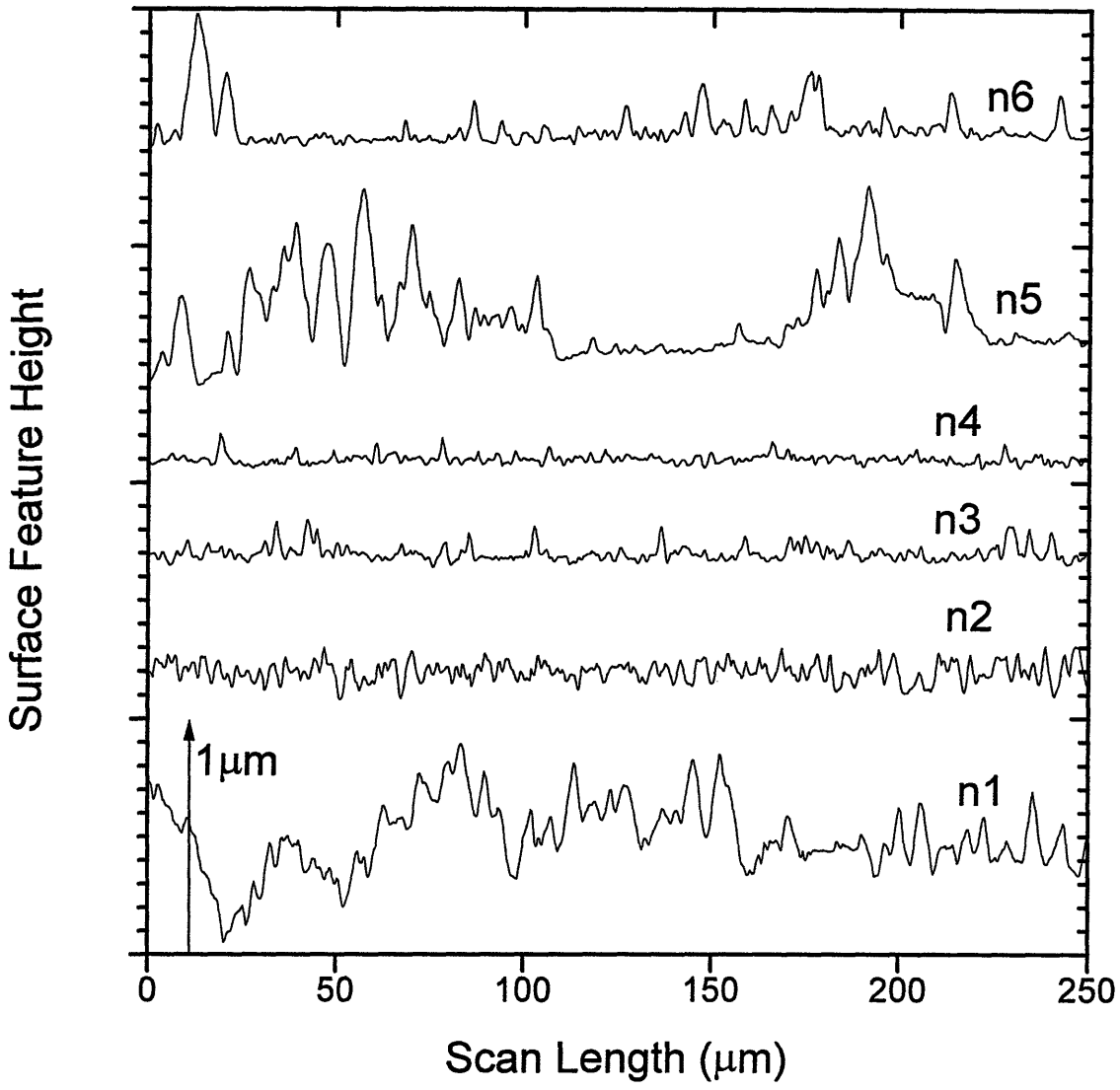


Figure A4.22. DEK TAK III surface profiles of 5Ωcm n-Si samples etched at the potentials indicated in figure A4.21.

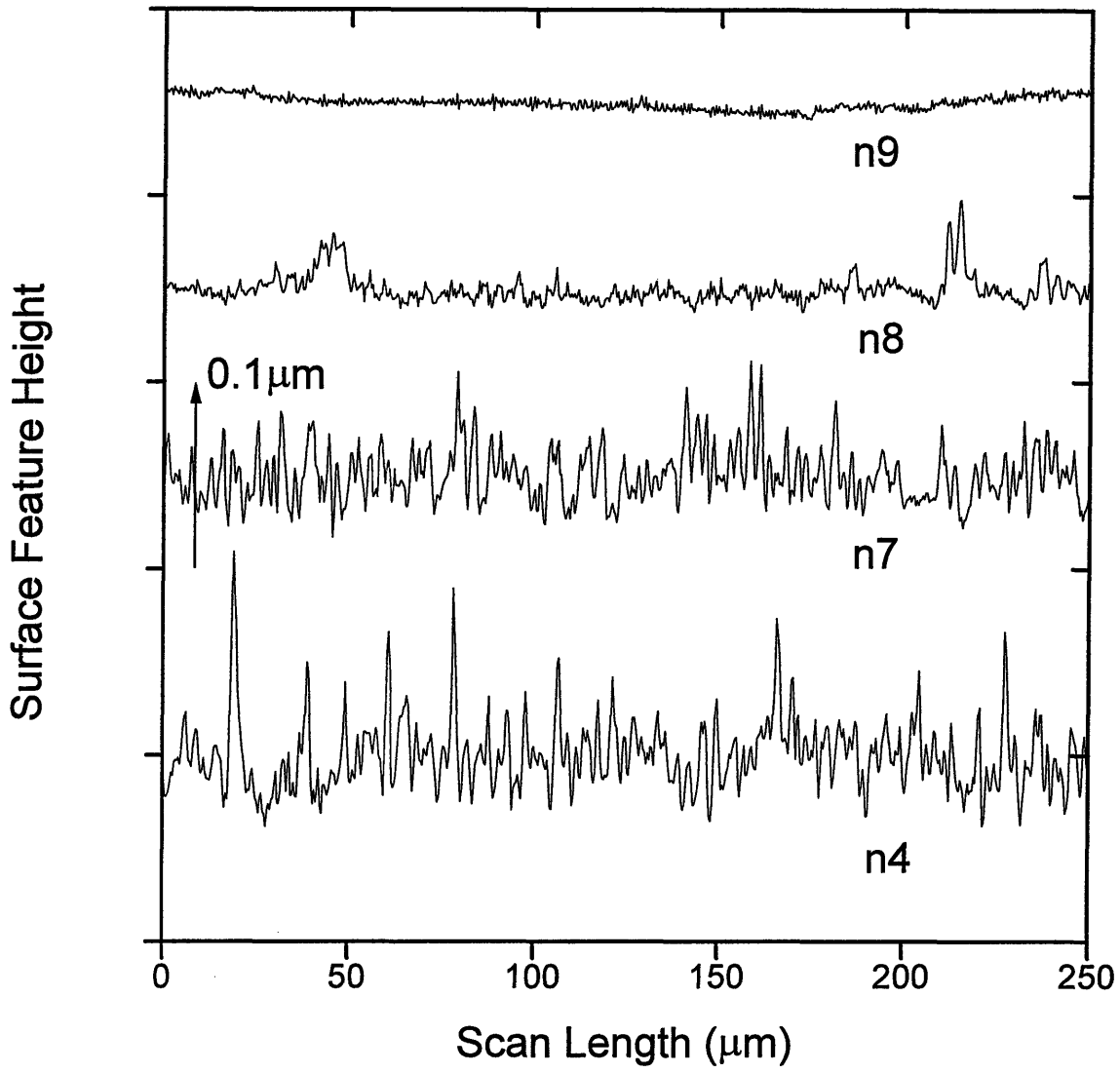


Figure A4.23. DEK TAK III surface profiles of 5Ωcm n-Si samples etched at the potentials indicated in figure A4.21.

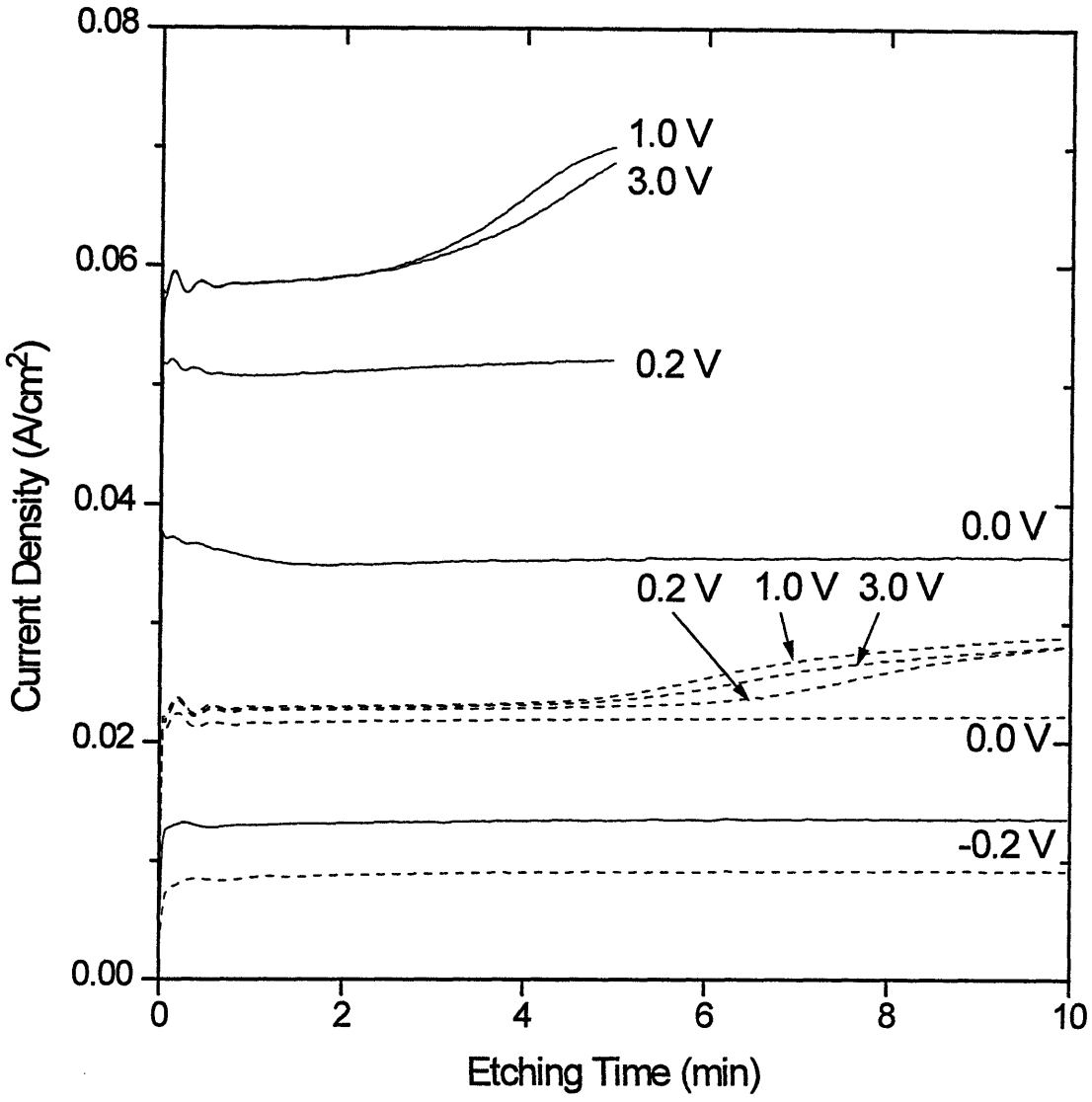


Figure A4.24. Current density versus etching time for 5Ωcm n-Si etched at the indicated biases (SCE) in 5% HF and at 87.2 mW/cm² white light illumination (solid curves) and 32.6 mW/cm² white light illumination (dashed curves).

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