Intellectual Property Strategy:
Analysis of the Flash Memory Industry

by

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ABSTRACT

This thesis studies the intellectual property strategy of companies in the flash memory industry, with special emphasis on technology and the development of nitride-based flash, a new and emerging type of memory technology. First, general perspectives and frameworks for licensing of patents and know-how are explored. Then, the participants in the flash memory industry are mapped to a product value chain, which is in turn mapped to an intellectual property value chain. We use a patent database analysis software IPVision in order to examine the patent portfolios of some of the memory chip companies. Analysis of the patent positions allows us to draw conclusions about the direction of technology development.

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1. Introduction

Intellectual property is an essential component of business strategy for technology companies in the flash memory industry. Due to the explosive growth of portable consumer electronics applications and an ever-increasing market demand for larger amounts of memory in smaller chips, there has been constant pressure to innovate the product technology. However, development costs are high and the market is characterized by serious competition and eroding profit margins. In this severe environment, a company's ability to effectively build and protect its intellectual property is critical.

Generally speaking, the term Intellectual Property (IP) encompasses all of the tangible forms of ideas and know-how that can be legally protected. In the flash memory space, patents are the most common form of intellectual property. Patents can be used in many ways, as protection against competitors, as a source of income through licensing, and as leverage in cross licensing agreements.

This thesis work will explore intellectual property strategy as it relates to the flash memory business. The end goal is to understand the industry, technology, players and trends in order to evaluate the progress of a new type of memory storage method called "nitride" or "trap storage".

Although flash memory has a history of over twenty years, the current portables market started its dramatic expansion less than ten years ago. Therefore, the market is a dichotomy of old and young characteristics. As we might expect to see in mature technologies, the flash market has strongly established players, complex licensing relationships and patent networks. Yet at the same time, the market demand for more flash and emerging portable applications create pressure for new technology solutions. New proposals to solve the limitations of the current technology are constantly being evaluated. Nitride-based storage is a popular emerging alternative, and we are

interested to understand the progress of the different types of proposals, in order to predict whether or not they can overtake the mainstream floating gate technology.

This thesis work is divided into three main parts.

First, we will look at a broad range of perspectives related to intellectual property licensing strategies. We will see how the role of licensing has changed as a result of time and legislation. In many cases, it has gone from being an auxiliary strategy to becoming a primary focus of both universities and companies.

In the second part, Chapters 3 and 4, we will examine actual applications of intellectual property strategies in the flash memory market. Chapter 3 gives a broad overview of the flash memory market. Licensing relationships in the mainstream industry are covered in Chapter 4, as well as examples of litigation between flash companies.

In the third part of this work, which starts in Chapter 5, we will employ a software system called IP-Vision^{SM} to analyze patent portfolios and patent activities of companies in the flash memory industry. Since flash memory intellectual property strategy places a high priority on patents, there is a high correlation between patenting activities and market trends. Thus it is possible to form useful conclusions about the dynamics of the industry as well as identify emerging technologies. We will explore the advantages of being the first to market in terms of establishing key patents in both fundamental technology and standardized interfaces, and the opportunities for new players.

2. Literature Review of Intellectual Property Strategy

2.1. About the Patent System

2.1.1. Patents, Copyrights and Trademarks

Patents, copyrights, and trademarks are forms of Intellectual assets that can be obtained and bartered under guidelines defined by the government legal system. The government's role is to provide incentive for technology progress and invention, by encouraging public disclosure while at the same time protecting the rights of the creator. This motivation forms the basis for regulation of all three of these rights. Of the three, patents correlate most closely with technology innovations. Copyright is regulated by the U.S. Copyright Office, and patents and trademarks are processed by the United States Patent and Trademark Office (USPTO), which is a federal agency in the Department of Commerce.

First, let's discuss the basic definitions of these different types of rights. A trademark is described by the USPTO as, "a word or symbol or design that identifies and distinguishes the source of the goods of one party from those of others".[1] Trademarks are useful for branding strategies. A copyright is a type of ownership of the means of expression of literary or artistic works and computer programs.[2] Copyright is granted immediately upon creation of the work in a tangible form.[3] No official action is required, but companies sometimes find it useful to register their works at the Copyright Office in order to publicize their legal ownership. It is also required that a copyright be registered before any legal action can be undertaken against a copyright infringer. Both copyright and trademark rights can be obtained with minimal legal costs.

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[1] United States Patent and Trademark Office, "Trademark, copyright or patent", obtained Jan 10, 2006, <http://www.uspto.gov/web/offices/tac/doc/basic/trade_defin.htm>.

[2] Qtd. in Bentley, p.29.

[3] U,S, Copyright Office, "What is a Copyright?", Obtained January 10, 2006) <http://www.copyright.gov/circs/circ1.html>.

Compared to copyrights and trademarks, patents are more difficult and expensive to obtain. A patent describes an invention and makes specific claims of originality. In exchange for public disclosure of the invention, the owner of the patent has the legal right to prevent any one else from "making, using, selling, or importing an object or device that incorporates any feature covered by the specified claims."[4] This monopoly extends over twenty years from the date that the patent application is filed.[5]

Although copyrights and trademarks can also be important to a technology company's intellectual strategy, the focus of this thesis will be on patents and patent-related strategy. The criteria and process for obtaining patents is more complex and expensive. Also, the association between technology innovation and patents is more direct.

2.1.2. Patent Criteria

In order to become a patent, an idea must first meet specific criteria in terms of field and novelty. Once an application has been accepted for processing, it is then examined by experts in the relevant field. The examiner confirms the soundness of the arguments in the application and searches for other prior art to refute the claimed originality. Prosecution is the process in which the examiner corresponds with the inventor or the inventor's counsel to discuss the claims. Often as a result of prosecution, broad claims will have been reworded or removed altogether. After a patent is granted, the owner of the idea is given sole ownership rights; no one else is allowed to use the idea without the inventor's permission for twenty years from the application date. In this way, motivation in the form of a competitive advantage is provided to inventors.

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[4] Jaffe, p.26.

In the United States, not every new idea can be patented. The government restricts granting of patents for immoral reasons if they might be considered contrary to public policy. Recent biological or biotechnical discoveries fall into these controversial categories.[6] The criteria for suitable subject matter can be summarized as - one or more of the following:

i) A process, such as a new approach to brewing beer or to depositing circuits on silicon,
ii) an article of manufacture, such as a kit to identify an infectious disease or a machine, such as new machine tool or automobile carburetor,
iii) a composition of matter, such as novel type of concrete or a new molecule,
iv) new and useful improvements to the above,
v) any distinct and new variety of plant that is asexually reproduced,
vi) any new, original, and ornamental design for an article of manufacture.[7]

The patent application must also pass three other tests:

i) Utility: Does the invention really do anything, and if so, does it solve the problem it sets out to address?
ii) Novelty: is the claimed invention really original?
iii) Non-obviousness: even if new, would the claimed invention have been obvious to one of ordinary skill in the art at the time of the invention?[8]

Each country has it own laws, and criteria and legal proceedings can vary among the different countries. For example, the United States is one of the few countries to award patents on a *first-to-invent* basis, whereas most of the others have chosen to go with the *first-to-file* method. In the *first-to-invent* philosophy, "intellectual property is predicated on natural rights"[9], and the individual who can provide sufficient proof that he/she was the first to invent the ideal, regardless of file date, will ultimately prevail. But the *first-to-file* system is considered easier to implement and maintain, because the patent is awarded to the first person who filed the application. Conflict

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[5] US Patent and Trademark Office, "What is a Trademark or Servicemark?", obtained Nov 3, 2005, <http://www.uspto.gov/web/offices/pac/doc/general/index.html#ptsc>.

[6] Bently, p.385.

[7] Jaffe, p.27.

[8] Jaffe, p.27-28.

occurs when two different people file for the same idea, under the two different types of systems. In this global economy, products are often manufactured and sold in more than one country. Thus, patent conflicts can become very complicated. There have been recent efforts by the World Trade Organization (WTO) to unify the patent laws, but it is a big political challenge.

Patents can provide effective legal barriers to entry against competitors who wish to enter the product market. This competitive advantage forms a critical component to product strategy. For successful products, enforcement and ownership disputes tend to be high stakes events. It has been estimated that 12-19 out of every 1000 patents may become the subject of litigation sometime in its lifetime.[10] The cost of a patent lawsuit cost can start at between one to three million dollars or higher.[11] Thus, it is not enough just to have an inventor who can write significant patents. Other means of protection are needed in order to maintain the competitive advantage provided by patents. There are several supporting industries that analyze intellectual property, and provide expertise in law and litigation.

2.1.3. A Typical Legal Patent Dispute

It should be noted that a patent provides an exclusionary right rather than an enabling right. The US PTO defines a patent as "the right to exclude others from `making, using, offering for sale, or selling' the invention in the United States or `importing' the invention into the United States."[12] If the patent rights are infringed, the patentee must enforce his/her patent without the help of the US PTO. Furthermore, independent invention, by which the patent is violated without knowledge of

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[9] Bently, p.367.

[10] Scotchmer, p.203.

[11] Schotchmer, p 200.

[12] U.S. Patent and Trademark Office, "General information concerning patents", last modified Jan 2005, Obtained Nov 4, 2005,, <http://www.uspto.gov/web/offices/pac/doc/general/index.html#ptsc>.

the infringing party, is not a defense to infringement.[13]

A typical dispute over patent infringement is described below:

> If someone else undertakes activities that are covered by the claims of the patent, they are said to infringe the patent. When the patentee learns that someone is infringing its patent, it will typically write him/her a letter. This letter is likely to demand that the alleged infringing activity stop. Depending on the patentee's business strategy, the letter may offer to license the patent, in return for a royalty or other consideration. The recipient of such a letter has essentially 3 choices. They can agree to take a license and pay royalty (if that option is offered); they can stop doing whatever is alleged to have created the infringement; or they can simply continue as before and wait for the patentee's next move. In many cases, the parties will enter into negotiations to try to resolve the dispute. Such negotiations may lead to a kind of license agreement, either with or without royalty payment. However, if negotiations are unsuccessful, the patentee can try to stop the alleged infringement by initiating litigation in federal court to enforce the patent. If the patentee can prove that someone is infringing the patent, they are entitled to an injunction (an order from the court) ordering the infringing activity to cease. They are also entitled to receive damages, money paid in compensation for the infringement that occurred.
>
> The defendant in an infringement suit will typically counter-sue, claiming that the patent itself is invalid. There are a variety of grounds for claiming invalidity, the most straightforward of which is, in effect, that the examiner made a mistake and that the invention is not novel, or is obvious. Thus, to prevail in this litigation, the patentee needs the court to decide that the patent is valid and being infringed. The alleged infringer can prevail via either finding of non-infringement or a finding that the patent is not valid.[14]

Although there are many other variations of patent conflicts, by this example, we can see that the holder of a patent wields a significant amount of power. Even if the final verdict should eventually be determined to be "non-infringing", the patentee has the advantage of incumbency. The challenger needs be willing to spend a great deal of time and money to reach that decision. Thus, when undertaking product development, an individual should consider the patents that he/she holds and the possibilities of infringing upon others patents.

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[13] Scotchmer with Maurer, Stephen M, (Chapter 3) "A Primer for Nonlawyers on Intellectual Property", p82.

[14] Jaffe, p.31.

2.2. The Basis of Intellectual Property Strategy

In addition to patents and other government granted rights such as copyrights and trademarks, there are other components to intellectual property. John Cronin from ipCapital Group defines IP in very general terms as protected innovation, described in Figure 1 by the concentric circles.

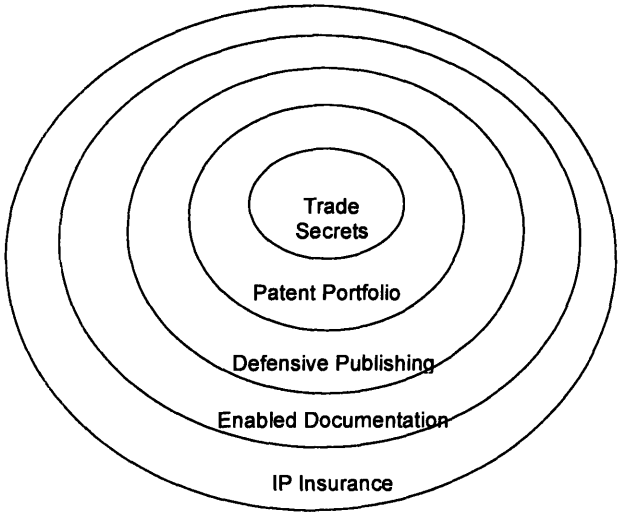

Figure 1: J. Cronin's IP Circles[15]

Good IP strategy strikes a balance between public and private information. As we learned in the previous section, patents are public disclosures which also provide authorizations to legal monopoly of claimed new idea provided the disclosure is complete enough to "enable" others to practice the invention. In order to keep some competitive advantage, it may not be wise to publicize the whole recipe needed to make a product. In this case, maintaining the idea as a trade secret is the preferred strategy. A trade secret is undisclosed confidential information which may be vital to a product, for example, Coke's secret formula. Defensive publishing is a way to claim rights to non-exclusive use of an idea. If a concept is publicly disclosed and not included in a

patent application within a year after publication, the concept becomes public domain and anyone is allowed to use the idea. This strategy can be useful to reduce patenting fees on ideas that do not provide competitive advantage in themselves. Enabled documentation covers any other documents that were not converted into trade secrets or patents. Finally, IP insurance is a method of risk management to hedge against the possibility patent or trade secret lawsuits.

2.3. Perspectives about Licensing of Intellectual Property

Thus far, we have focused on patents as a protective means against competitors for individuals making their own products based on the invention. In addition, patents can be sold, licensed, and cross-licensed. Licensing, especially, is another common patent-related activity. If a patent is analogous to a parcel of land, then licensing is much like renting. With the owner's permission, others can access the patent (or land) in exchange for some consideration. If the fee is fixed, the exchange is called a *licensing fee*; if the return is some percentage based on the total goods sold, it is considered a *royalty*. Generally speaking, royalties are a few percentage points of the total cost of goods sold. There is more risk tied to royalty arrangements, but the upside is usually higher than a fixed license fee. If the patent licensing right is exchanged for the right to use another individual's patent, this is an example of *cross-licensing*. When competitors have similar technologies with overlapping components, they may agree to license their related patent portfolios to each other.

There are many opinions about the purpose of intellectual property licensing. The range of perspectives is broad, from a form of globalization strategy, to as a complement or alternative to research and development, to firm focus. Moreover, the schools of thought have evolved over time, and with the rise and fall of different technology industries.

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[15] Qtd. in Davis and Harrison, p.24.

2.3.1. Mini-Monopolies and Anti-trust

For companies seeking to consolidate competitive advantage, licensing of patents and copyrights provide a legal means to build competitive advantage through "mini-monopolies"[16]. When a company makes a product, patents can provide barriers to entry to control competition with its own products. However, there are certain behavioral guidelines that must be followed. First and foremost, licensing activity is subject to government limitations of anti-trust. Use of the patents in conjunction with other companies is especially subject to scrutiny. Therefore, even if it may be in the best interest for a single company to hold exclusive rights to a patent in order to maintain its market dominance, that company may be forced to share its rights, in compliance with government policies of anti-trust.

In "*Antitrust policy for the licensing of intellectual property: An international comparison*", Richard Gilbert from the University of California at Berkeley describes the U.S. Department of Justice and the Federal Trade Commission and EU Commission's policies. Licensing agreements should not violate the Sherman Act (or the European counterpart to the Sherman Act) which states "every contract, combination in the form of trust or otherwise, or conspiracy in restraint of trade or commerce among the several states, or with foreign nations, is hereby declared to be illegal."[17]

The author explains that nine non-competitive licensing activities were defined by the United States in the 1970's. Subject to court interpretation, and rules of reason, they are as follows:

1. Royalties not reasonably related to sales of the patented products;
2. Restraints on licensee's commerce outside the scope of the patent (tie-outs);
3. Requiring the licensee to purchase unpatented materials from the licensor (tie-ins);
4. Mandatory package licensing;

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[16] Gilbert, RJ. p. 208.

[17] Qtd in Gilbert, RJ.

5. Requiring the licensee to assign to the patentee patents which may be issued to the licensee after the licensing arrangement is executed (exclusive grantbacks);
6. Licensee veto power over grants of further licenses;
7. Restraints on sales of unpatented products made with a patented process;
8. Post-sale restraints on resale; and
9. Setting minimum prices on resale of the patent products.[18]

Europe has a similar overall philosophy of anti-trust, with small differences in implementation details. For example, in Europe, block exemptions for trade restriction are law, they are not subject to interpretation.

Thus, it is important to understand that the legal restrictions involved with technology licensing. The monopolist competitive advantage may not be extended beyond the bounds of the patent itself. In the electronics industry, there have been instances in which companies are forced to license their patents to their competitors in order to provide the marketplace with at least two sources for the same product. Intel and AMD are a prime example of this relationship. In 1991, in compliance with the Sherman Anti-trust Act, Intel was forced by the government to license its x386 microprocessor core to AMD, royalty-free[19].

2.3.2. Innovations in Universities

Companies that make and sell their own products generally aim to limit their licensing the related patents, in order to control competition with their own products. In contrast, universities seek to license as much as possible, because their primary directives should be towards the education of its students and knowledge creation, rather than commercialization. By licensing, universities can maintain their focus on research and innovation, and the research products may still be accessible to start up companies and existing businesses.

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[18] Gilbert, RJ., p. 209.

[19] Singer, Michael, "Intel and AMD: A long history in court", ZDNet News, June 28, 2005, Obtained Jan 10, 2006 <http://news.zdnet.com/2100-9584_22-5767146.html>.

The MIT Technology Licensing Office (TLO) is a successful example of a university licensing center. According to its mission statement, there are four main benefits to technology licensing. Technology licensing provides (i) tangible evidence of progress to tax payers, (ii) monetary incentive to faculty and students, (iii) an additional source of income to the university, and (iv) job opportunities to new graduates. [20] As a result of its technology program, MIT collects $30-40M per year in royalty payments. About 20-28% of the royalty income goes directly to the inventors, the other 80% covers the program costs and distribution to the university. In 2005, 20 start up companies were formed based on the patents licensed by the MIT TLO. The additional publicity generated by these entrepreneurial commercialization efforts enhances the reputation and relevancy of the university as a technology innovation center.

Many universities have similar licensing programs. Rebecca Henderson, Adam B. Jaffe and Manuel Trajtenberg, studied the overall trend of universities in their paper, "Universities as a source of commercial technology: a detailed analysis of university patenting, 1965-1988". Their data found that the annual number of patents being filed by universities increased 15x between 1965 to 1988. In contrast, the total U.S. patenting rate increased about 50%. During this period, the number of universities patenting their research also increased from 50 in 1965 to over 150 in 1988. Since it is difficult to actually match patents to their resulting revenues, the authors use a Citation Intensity Index in order to value the "effectiveness" of a patent. The premise is that a patent which is cited or referenced by other patents will have a greater probability of being useful than a patent that is never cited. The research concluded that the effectiveness of university patents over general patents increased in 1965 to 1980, but after that, there was a steady decrease. The decrease

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[20] MIT Technology Licensing Office, "Mission Statement", Obtained Jan 10, 2006, <http://web.mit.edu/tlo/www/mission.html>.

seemed to be triggered by the Bayh Dohl Act in 1980. This legislation gave universities the right to own the patents that result from federally funded research. With this more direct motivation, universities increased the number of patents applications, perhaps without maintaining the quality. In the last 5 years covered by the study, the effectiveness of university patents was found to be very similar to that of patents filed by industry.

The effectiveness of university patents, as measured by licensing income is studied by the Association of University Technology Managers (AUTM)'s 2003 survey. Figure 2 shows the accumulated gross income over time. According to this bar graph, in 2003, the 195 universities that were surveyed accumulated over $1B income from running royalties alone. A portion of this income is redirected back to the basic research operations. In this way, universities have another source of income in addition to their usual tuition and grants.

Figure US-27: Gross Income Received by Income Type, All Respondents, 2003

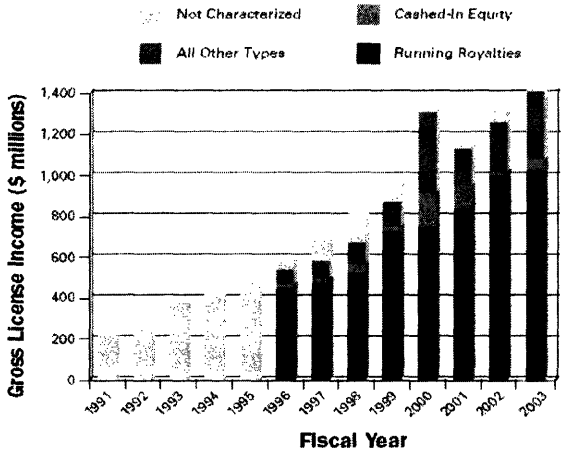

Figure 2: Income from Licensing Activities from 195 US Universities[21]

[21] Ed. by Ashley J. Stevens, D. Phil, and Frances Toneguzzo, "AUTM Licensing Survey, FY 2003", AUTM, Obtained Jan 10, 2005, <http://www.autm.net/events/File/Surveys/03_Abridged_Survey.pdf>.

2.3.3. Measuring Effectiveness of Patents by Surveys

In the previous section, the effectiveness of patents in universities was measured based on citation intensity and income from licensing. Another way to study the contribution of patents to the company's bottom line is described in "*Appropriating the Returns from Industrial Research and Development*", by Richard Levin et. al. Here, the effectiveness of patents is studied in relation to other alternatives. In a systematic attempt to determine the return on investment for intellectual property, R&D executives from over one hundred industries were surveyed. The topics were divided into 4 parts, (i) the effectiveness of other alternatives besides patents to protect competitive advantage, (ii) the cost and time to imitate innovations of rivals, (iii) links between an industry's technology and other sources of technological contribution, and (iv) the pace and character or the technological advance.[22]

Although there were variations due to the nature of the different industries, certain common trends were observed. Patents were generally rated less effective than other advantages such as early lead time and the learning curve. Patents for products were considered more effective than process patents. Secrecy was a more effective strategy for process patents; which leads some firms to often avoid patenting of process innovations altogether. Also, patents were less effective as a licensing/revenue generating strategy, and tended to be used more as defensive measures.

These trends were also examined within the context of their specific industries, as shown in Table 1.

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[22] Levin,p. 790.

Table 2. Effectiveness of Process and Product Patents in Industries with Ten or More Survey Responses

	Process patents		*Product patents*	
Industry	*Mean*	*Standard error*	*Mean*	*Standard error*
Pulp, paper, and paperboard	2.6	0.3	3.3	0.4
Cosmetics	2.9	0.3	4.1	0.4
Inorganic chemicals	4.6	0.4	5.2	0.3
Organic chemicals	4.1	0.3	6.1	0.2
Drugs	4.9	0.3	6.5	0.1
Plastic materials	4.6	0.3	5.4	0.3
Plastic products	3.2	0.3	4.9	0.3
Petroleum refining	4.9	0.4	4.3	0.4
Steel mill products	3.5	0.7	5.1	0.6
Pumps and pumping equipment	3.2	0.4	4.4	0.5
Motors, generators, and controls	2.7	0.3	3.5	0.5
Computers	3.3	0.4	3.4	0.4
Communications equipment	3.1	0.3	3.6	0.3
Semiconductors	3.2	0.4	4.5	0.4
Motor vehicle parts	3.7	0.4	4.5	0.4
Aircraft and parts	3.1	0.5	3.8	0.4
Measuring devices	3.6	0.3	3.9	0.3
Medical instruments	3.2	0.4	4.7	0.4
Full sample	3.5	0.06	4.3	0.07

Source: Authors' calculations. Mean score on a scale of 1 to 7.

Table 1: Survey Responses about the effectiveness of patents in different industries[23]

Based on the responses, patents in the drug industry resulted in good returns and competitive protection. Industries related to chemistry and having heavy R&D costs also had stronger preferences for patents. Interestingly, in most of the other industries, patent protection was not considered the best means for appropriation. The authors also offered some comments about this finding. "Although our respondents were asked to describe the typical experience of firms in their industries, they may well have overlooked aspects of appropriability that are particularly relevant for new firms". Also, we would like to suggest the possibility that the nature of competition in

these industries may have changed since this study was conducted in 1987.

2.3.4. Licensing

In Levin's work, as well as much of the other literature written prior to the 1990's, licensing is considered a by-product of research, rather than a goal of research. Edward Roberts suggests in "Licensing: An effective alternative" (1980), that a passive-active dichotomy[24] exists in a commercial corporation. The patent attorney is too far downstream from the sources of innovation to effectively build a licensing strategy, and the scientists and actual inventors may not have sufficient understanding of business to direct their research activities for maximum profit. Several companies were studied and it was found that 99.5% of all patents issued generate less than $1M in revenue. Furthermore, within the subset of licensed patents, the average revenue is closer to $5,000/year. In this context, making product and protecting the product by patents should be considered more effective than licensing.

Since 1990 however, there has been a surge in licensing activity, and changes in the companies' approaches to patent creation and licensing. In 1997, direct royalties and licensing fees collected was reported to be $30.3B. It was estimated that the actual sales associated with the licensing transactions was close to $673B. In comparison, the United States's total exports for that year were $678B.[25] Potential royalty income is certainly a significant motivation to license. In the following sections, we will discuss other possible reasons to license, and frameworks for decision making.

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[23] Levin, p. 801.

[24] Roberts, "Licensing: an effective alternative" p.230.

[25] Contractor, p.42.

2.3.5. Licensing as a Component of Globalization Strategy

In choosing to license, one motivation may be to augment a globalization strategy. In "*Perspectives for International IP Managers*", Farok J. Contractor discusses the complementary roles of licensing, investment, and trade, in global operations.[26] He introduces two ways to think of intellectual property licensing.

1) *Licensing as a foreign market entry alternative to direct exports or foreign direct investment.* In addition to a direct export, customers in a foreign country can buy American products that were produced by an affiliate company within that country. Sometimes this approach makes more sense especially if the foreign country has more expertise to produce and distribute in that country.

In the United States, royalties and licensing fees payments grew at a rate of 12.6% annually during 1986-1996. At the same time, US foreign direct investment or exports grew at 8%. In contrast, the US economy grew at 4%. From these numbers, we can appreciate the value of licensing to a foreign company.

2) *Auxiliary channel for income extraction and tax minimization.* Royalty payments made by licensees can be expensed, as long as the royalties are reasonable. Licensing and royalty payments are also considered more attractive accounting alternatives to dividend payments. It is interesting to note that most of the international licenses are intra-firm, and are part of a global tax planning strategy.

2.3.6. As a Function of Product, Industry, Resources

Another way to think about licensing, is as a function of product , industry and resources. In 1996, Massaki Kotobe, Arvind Sahay and Preet S. Aulakh wrote a paper titled "*Emerging Role of*

Technology Licensing in the Development of Global Product Strategy: Conceptual Framework and Research Propositions". The authors presented a framework in which intellectual property licensing may take on more pro-active corporate role, depending on factors of product market, industry level and resource-based factors.

Product – Consumers tend to choose the products that they perceive to have the stronger market presence. They prefer the brands or platforms that have long term prospects and are more likely to deliver complementary products and/or services in the future. This behavior is considered a positive *network externality*. Network externalities are the gains in utility that can be ascribed to the increase in the number of other consumers using the same product or other goods in conjunction with the product.[27] In addition to the consumer momentum effect, end products that are built from many components will also have high network externalities, because there are many interfaces and opportunities for integration.

According to this theory, companies that make products with high network externalities will have incentive to license producers of associated products in order to improve the market share of that type of product. Compatibility also provides an incentive for technology licensing. The authors have found that there is more licensing where there are higher requirements for compatibility.

Industry level – The relevant variables are (i) industry structure, and (ii) technology intensity. In industry structure, the competitiveness of the industry is related to the amount of licensing that occurs. In the extremes of high and low competition, there is little IP licensing. In perfect competition, all companies will have the same technology and there is no advantage to technology

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[26] Contractor, p. 41-50.

[27] Katz and Shapiro, 1985.

licensing. In a monopoly, a single firm will not want to share its competitive advantage. Thus, licensing relationships are more likely to be found in the intermediate levels of industry concentration.

Technology intensity is related to three types of relationships. The first one is in industries that add significant value at an early stage in the value chain. A large amount of R&D may be needed. The second characteristic is a high level of flow of information and applications across to other industries. The third is that the rate of change is high. Examples of industries with high technology intensity are: software, semiconductor, computer, biotechnology, etc. The authors believe that the greater the technology intensity, the more technology licensing that occurs to firms in other industries outside of the original industry.

Resource based factors – Other environment factors such as cross-border legal enforcement of intellectual property laws, and international norms can affect licensing. Licensing is not necessary if infringement with impunity is possible. Complementary assets during the manufacturing and commercialization process may also affect licensing decisions. A cited example is the instance in which Sun Microsystems licensed its microprocessor designs to Philips and others, because they had a greater capacity to integrate the chip into an end product and make and sell the end product in large numbers.[28] Thus, the authors generalized that the lower the complementary assets that exist in a firm, the greater the incidence of technology licensing.

2.3.7. Licensing Pre-empts Imitation

Another method of determining when to license may be based on the threat of imitation. Charles bHill wrote a paper, in 1992, called "*Strategies for exploiting technological innovations: when and*

when not to license". This paper provides a framework for determining when licensing is a good strategy. Figure 3 shows the determinants for competitive advantage. The factors to consider are competitive intensity, barriers to imitation, and profitability. When competitive intensity is high, and competitors are capable and the profit of the product is substantial, speed of imitation should be fast. If profitability is high, competitor capability is also high and competitive intensity is low, then transaction cost will be high.

The Determinants of Transaction Costs and the Speed of Imitation

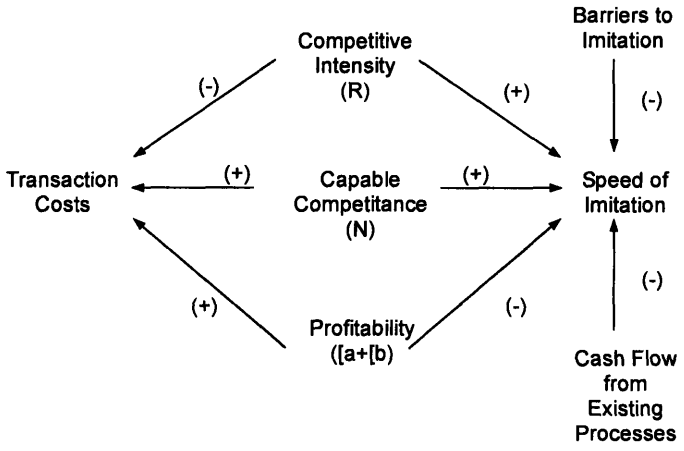

Figure 3: C. Hill's Determinants for Competitive Advantage[29]

When an innovation is successful, it attracts the attention of many imitators who eventually find a way to invent around the patent, thus the original innovator's can only expect a temporary advantage. In such a case the innovator may be better off licensing his technology so that he can

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[28] Khazam and Mowery, p.89-102.

[29] Hill, p. 345.

at least shares in the profits of his competitors. Figure 4 gives a framework for deciding to license or not to license.

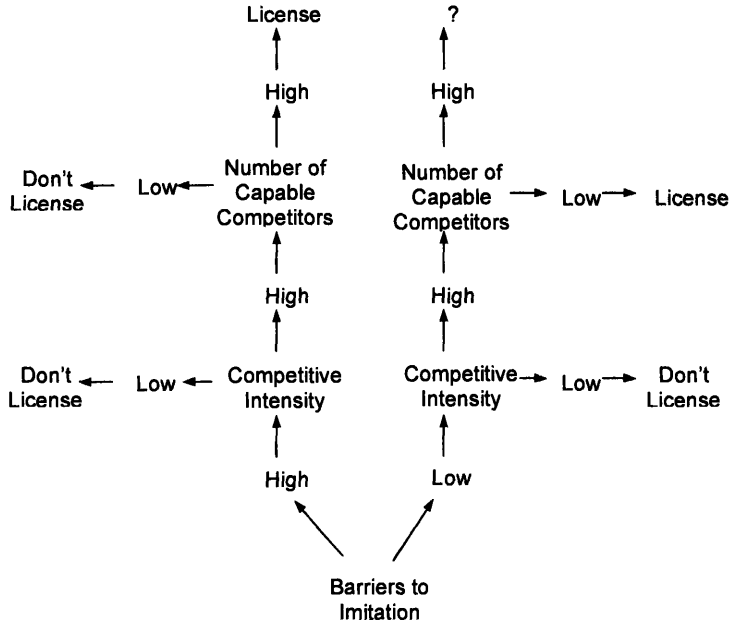

Figure 4: C. Hill's Decision Framework[30]

The trade-offs between maximizing profit and losing competitive advantage are shown, especially with respect to the complementary assets. The firm's own complementary assets and the competitor's assets should be evaluated.

> If the first mover advantages look substantial, and if barriers to imitation are high, it may pay not to license unless rivals also have the capability and incentive to develop their own, possibly better, technology. If rivals do have the capability and incentive, it may pay the innovator to forego any possible first mover advantages in order to establish its technology as the dominant design in the industry. By doing so, it will at least collect royalty

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[30] Hill, p. 435.

payments.[31]

The author also examines the transaction costs of licensing due to contracting and expected loss. He points out three potential issues: (i) uncertainty of the invention's true value and subsequent price undervaluation, (ii) monitoring costs, and (iii) danger of second order diffusion, in which the competitor develops a better, superceding innovation.

2.3.8. Licensing vs. In-house R&D

Choosing to take a license may also an alternative to in-house research and development. Joshua S. Gans wrote "*Incumbency and R&D Incentives: Licensing the Gale of Creative Destruction*," in 2000. The paper focuses on how an incumbent firm balances in-house R&D with licensing technology from external firms. Many technology advances are very resource heavy and require large financial investments. In such cases, collaboration or licensing may be an effective alternative. However, the bargaining process and economic environment should also be factored into the decision making. The author suggests that, in order to maintain a strong bargaining position, large firms should not depend solely on outside firms for technology.

Another role for technology licensing is given in Kenneth Cort's paper, "*Focused firms and the incentive to innovate*". First, the author cites several sources that believe horizontal firms are more innovative than vertical firms.

> A number of papers have looked at the firm's choice of scope as a strategic commitment device, among them Vickers (1984), Shephard (1987), Bonnano and Vickers (1988), Rey and Stiglitz (1995), and Corts and Neher (1998). These papers emphasize the ability of the firm to credibly alter product market behavior by limiting the firm's scope.[32]

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[31] Hill, p. 433.

[32] Corts, p.342.

He recommends that in order to maintain a firm's focus, it is a good idea to license out technology ideas for the ancillary products. In this way, the company can focus its resources on the development of its core products, and still profit from the ideas that may be valuable, but not necessarily related to the core business.

2.3.9. Licensing Arrangement Fees

Having discussed motivations for licensing, we will now shift the discussion to the licensing agreement itself. Regarding the nature of the licensing agreement and remuneration, K Shapiro of "*Patent Licensing under Strategic Delegation*", believes that:

> In concentrated industries, royalty licensing is preferable to fixed-fee licensing. A proof was worked out based on a duopoly situation in which the licensor is willing to sell two licenses to two separate companies. However, if there are several licensees, then a fixed licensing scheme may be more common. Thus, depending on the strategic incentives of the firm, the licensing payment scheme can be chosen between royalty and fixed fee. Especially separation of ownership from control and managerial incentives that may be indexed only to profits. [33]

Exclusivity also changes the price of licensing. Where exclusive licensing does not conflict with the Sherman Act, exclusive licensing can command a premium over non-exclusive contracts.

Furthermore, licensing arrangement fees may also depend on the nature of the industry. For example, in the technology standards committee for JEDEC, any technology that is developed within the community must be made available to all members for a reasonable non-discriminatory fee.

2.3.10. How Licensing Affects Other Firms

It is interesting to understand how one company's licensing activities can influence others in the

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[33] Shapiro, p. 241.

same industry. Downstream firms are generally worse off for the licensing due to the complementary assets. This is especially true when a logical series of patents are owned by different companies in competition with each other. Also for a patent to be useful, a company needs to be prepared to take legal action against infringing parties. Competitors will also file alternative means patents as a counter-action. In recent years, it has become a general practice for companies to build stacks or networks of patents.

Some people have questioned whether the patent system is actually slowing down commercialization of new technologies. Carl Shapiro wrote "*Navigating the patent thicket: cross-licenses, patent pools, and standard setting*". In his paper, he defined a *patent thicket* as "a dense web of intellectual property rights that a company must hack its way through in order to actually commercialize new technology."

Adam Jaffe and Josh Lerner, authors of Innovation and it Discontents, also believe that the current patent system endangers innovation and progress. The patent thicket around products complicates introduction of new technology. The incentive for filing patents has turned into defensive strategy, if a company chooses not to file patents, then they may be forced into the position of paying royalties instead of cross-licensing. "Companies are like countries in an arm's race: since the terms of the cross-licensing agreement are driven by the size and quality of each company's patent portfolio, every company wants to have the best portfolio, in order to be in the strongest position in cross-licensing negotiations"[34]

2.4. Value Hierarchy Framework

As E. Roberts pointed out in 2.3.4, intellectual property strategy is too important to leave to the

patent attorneys who do not have an expert understanding of either the market or the technology. Companies that deal with intellectual property should understand how to maximize the value creation and value extraction processes. The Value Hierarchy Framework was introduced by Julie L. Davis and Suzanne S. Harrison in Edison in the Boardroom (How Leading Companies Realize Value from their Intellectual Assets). This five tiered framework is depicted in Figure 5. Each level is built based on the previous levels, and each represents a different expectation that the company has about the contribution that its intellectual property/intellectual assets (IP/IA) function should be making towards the corporate goals. At each stage, five "Best Practices" are given.

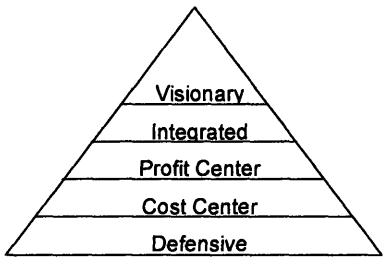

Figure 5: The Value Hierarchy[35]

Level 1: Defense

In the first level of defense, the simplest goal is to "stake a claim". Products should be protected by patents and patents serve as a legal shield to protect the company from litigation. Competitors can be either prevented from using that asset, or forced to make a less desirable design-around. At this level, patents are also considered valuable legal assets, to improve leverage during cross-licensing negotiations. Companies mostly rely on the IP attorneys to process and prioritize the patents. A summary of the company's goals and best practices at this level is given in Table 2.

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[34] Jaffe and Trajtenberg, p.60

[35] Davis and Harrison, p.12.

Level One: Defense	
Companies are trying to accomplish	**Best practices**
1. Generate significant number of patents for their IP portfolio. 2. Ensure that their core business is adequately protected 3. Initiate basic processes to facilitate patent generation and maintenance 4. Initiate basic processes for enforcing patents 5. Ensure that their technical people have freedom to innovate	1. Take stock of what you own. 2. Obtain intellectual property while ensuring design freedom 3. Maintain your patents. (don't let good ones lapse) 4. Respect the IP rights of others. 5. Be willing to enforce, or don't bother to patent at all.

Table 2: Value Hierarchy, Level One Summary

Level 2: Cost Center

The second level, Cost Center, is a defensive mode, much like Level 1. The difference is that Level 2 companies also consider how to reduce costs of filing and maintain IP portfolios. Software packages and electronic IP inventory systems can help to link the value of patents to the costs. The goals and best practices at the second level are given in Table 3.

Level Two: Cost Control	
Companies are trying to accomplish	**Best practices**
1. Reduce costs associated with their IP portfolios 2. Refine and focus the IP that is allowed into their portfolios	1. Relate patent portfolio to business use 2. Establish an IP committee with cross-functional members 3. Establish a process and criteria for screening patents 4. Set detailed guidelines for patent filing and renewal 5. Regularly and systematically review the portfolio to prune patents not worth maintaining

Table 3: Value Hierarchy, Level Two Summary[36]

[36] Davis and Harrison, p.44,46.

It is important to understand the contents of the patent portfolio in order to understand how to "prune" effectively. As corporate strategy changes, or technology direction changes, certain patents may become less valuable, and therefore can be abandoned to save the maintenance fees. It is also recommended to staff a patent committee with cross-functional members in order to implement a patent screening process. At this defensive and cost-conscious level, only patents that have current or future value should be filed and/or maintained.

Level 3: Profit Center

At Level 3, IP is considered to be a business asset, as well as a legal asset. Best practices at this level are summarized in Table 4. Here companies look at the patents in their portfolios and strategize how to extract the value.

Level Three: Profit Center	
Companies are trying to accomplish	**Best practices**
1. Extract value directly from their IP as quickly and inexpensively as possible 2. Focus on noncore, nonstrategic IP that has tactical (as opposed to strategic) value	1. Obtain management buy-in 2. Start a proactive licensing organization 3. Consider IP donations and royalty audits 4. Organize to extract value 5. Develop advanced screening criteria

Table 4: Value Hierarchy, Level Three Summary[37]

Level 4: Integrated

In Level 4, companies look beyond defense, costs and profits. They use IP to position themselves broadly in the marketplace and also for tactical maneuvers. IP is considered an integrated business

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[37] Davis and Harrison, p.67, 69.

asset that can be used for negotiation, company strategy positioning, even as a way to affect the stock price. IP, especially in these circumstances, is not just limited to patents, but also includes know-how.

At this level, IP strategy is aligned with corporate strategy. After the corporate goals and direction is understood, then companies should consider what new intellectual property should be created. The IP strategy should be managed across multiple functions, such as "Research and development, finance and taxes (charitable contributions to achieve tax savings), human resources (compensation system), marketing (understand future trends and competitors plans), information technology (database for competitors products and technologies)".[38] In order to communicate effectively across the different organizations, the IP knowledge must be codified in some centralized way. This IP knowledge should not be limited to patents, but should include any relevant information such as key persons, and computer programs. This understanding is especially important during acquisitions, in order to make sure that all pieces are included. Assessment of competitor's activities is also recommended at this level. The summary of goals and best practices for Level Four are given in Table 5.

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[38] Davis and Harrison, p.108-110.

Level Four: Integrated	
Companies are trying to accomplish	**Best practices**
1. Extracting strategic value from their IP 2. Integrating IP awareness and operations throughout all functions of the company 3. Becoming more sophisticated and innovative in managing and extracting value from the firm's IP	1. Align IP strategy with corporate strategy 2. Manage IP and intellectual assets across multiple functions 3. Conduct competitive assessment 4. Codify IP knowledge and share it with all business units 5. Focus on strategic value extraction

Table 5: Value Hierarchy, Level Four Summary[39]

Level 5: Visionary

The Visionary state is the ultimate Holy Grail in which companies look outside themselves and at the future. According to Davis and Harrison, "companies at this level use their [Intellectual Assets] to stake a claim to the future, defining and protecting both their current products and markets as well as those to come."[40]

Level Five: Visionary	
Companies are trying to accomplish	**Best practices**
1. Staking a claim on the future 2. Encouraging disruptive technologies 3. Embedding intellectual assets and IA management into the company culture	1. Identifying gaps to create trends in one's own industry - setting "new rules of the game" 2. Patenting strategically – creating patents that position the company in the path of industry evolution 3. IAM performance measurement and reporting

Table 6: Value Hierarchy, Level Five Summary[41]

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[39] Davis and Harrison, p.96-97.

[40] Davis and Harrison, p.123.

Here, the company takes a leadership role by identifying customer need and other trends in the industry. As George Pake, founder of Xerox PARC once said, "the best way to predict the future is to invent it."[42] A performance measurement and reporting system should be implemented, in order to link the IP activities to cash flow. Figure 6 shows the activities of IP strategy at the visionary level. Here, we can see that all of the functions have been integrated together, based on a closed loop of four major decision making points, i) Patent Criteria and Decision Making Process, ii) Valuation of the Opportunity, iii) Value Extraction, and iv) Assess Need for New Innovation. Thus, business strategy, product mix, strategic positioning, and competitive assessment are all taken into consideration for patent portfolio management and generation.

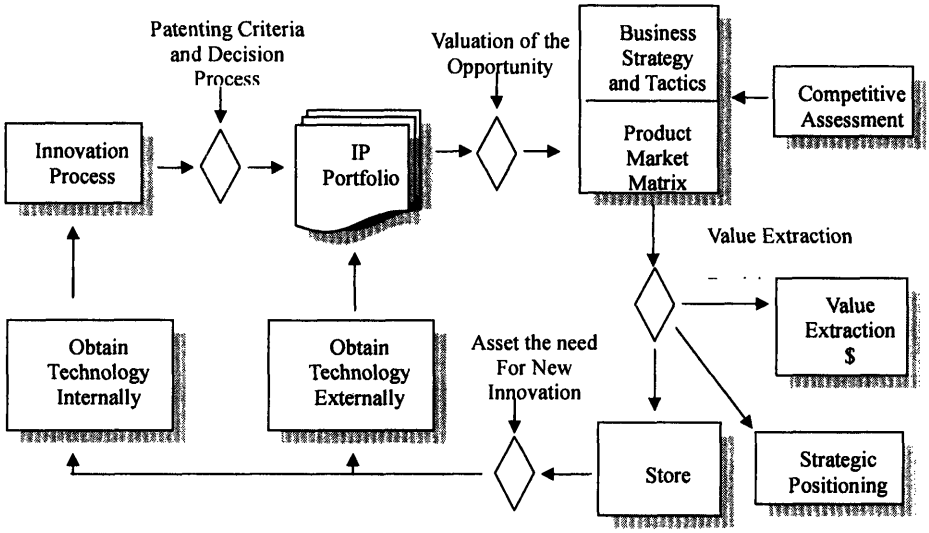

Figure 6: IP Management System (Visionary Focus)[43]

2.5. Valuation of Intangibles

In the Value Hierarchy, business strategy and IP strategy should become, Zen-like, "at one with

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[41] Davis and Harrison, p.123,126.

[42] Qtd. in Davis and Harrison, p.126.

each other". However, currently there is no standardized method for business and financial reporting of IP and associated intangibles, therefore the tendency is for these assets to be undervalued or viewed with uncertainty. Thus companies that report to shareholders may choose to focus on tangible strategies, rather than the intangible. Baruch Lev attempts to prescribe a solution to this issue in his book, *Intangibles: management, measurement, and reporting*. In his book, Lev defines intangibles as assets that can provide future benefit to the company, but do not take a physical or financial form.[44] By separating out the R&D stages and development of intellectual property, and reporting in a periodic manner, it can be possible to systematically value such intangibles. Only then can IP strategy be truly reflected in business strategy.

2.6. Conclusion

Thus intellectual property is defined as legally protected know-how, which includes, but is not limited to patents, trademarks, copyrights, trade secrets, defensive publishing, enabled documents, and insurance. The criteria and complexity of the patent application process has been explored, and several perspectives about patent licensing and its role in business strategy have also been discussed. Like other important assets of a company, IP must be managed to create shareholder value. The Value Chain Hierarchy is a framework with which companies may manage intellectual property strategy in discrete stages.

Having set the stage for thinking about appropriate strategies based on industry concentration, speed of development, etc, we would now like to apply these ideas specifically to the flash memory industry.

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[43] Davis and Harrison, p.125.

[44] Lev, p. 6.

3. Flash memory industry

3.1. Introduction

We will start by explaining the characteristics of the flash memory and its underlying technology. We will then look at the products value chain and the participating companies, with special focus on the memory manufacturers and new technology trends.

3.2. Background

3.2.1. History of Science

Flash memory is a type of non-volatile storage, in which data is maintained even after power is discontinued. The first floating gate flash memory was invented in the 1980's, and was originally used for niche applications to store small amounts of BIOS code. In the first half of the 2000's, it overtook DRAM to become a mainstream technology driver. Today, flash memory is a one of the fastest growing markets in the history of semiconductor memories. According to Jeff Neal at Optionetics, the high density flash market is expected to increase at a rate of 18% a year for the next five years.[45]

Yet for many years, flash was not considered a particularly exciting technology. In the early days of personal computers, boot-up BIOS code was stored in flash memory because of its capability to maintain data without power. Although this property of *non-volatility* could also be found in other types of memory like hard disk and floppy disk, flash memory was preferred because the form factor was smaller and mechanically moving parts were not required.

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[45] Neal, Jeff, "Outside the box: The flash memory surge", October 5, 2005 (obtained Jan 10, 2006) <biz.yahoo.com/opt/051005/7e25ed9f3fef2187d4aa8fb6280dc784.htm>

Other types of semiconductor memories, like SRAM and DRAM are *volatile*. They require power to maintain data. Digital data, in the form of "1"'s and "0"'s, is stored as electrical charge on a capacitor. If power is lost, then the electrical charge is dissipated and data is lost. The basic flash memory cell operates on a different principle from SRAM and DRAM cells. Figure 7 gives illustration of a DRAM cell and a flash memory cell. In the conventional flash cell, there is an extra charge storage region or *floating gate*, which is completely surrounded by insulating material. Once electrons are stored in the floating gate, they can not escape easily, because of the surrounding insulator.

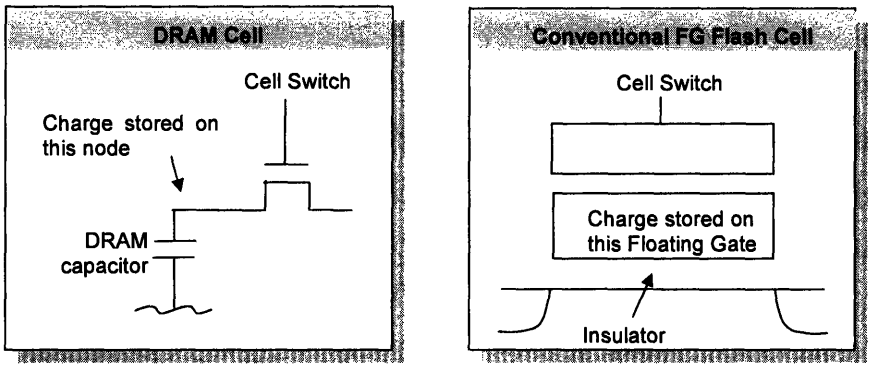

Figure 7: DRAM and Flash Memory Cells (conceptual)

However, the procedure of forcing electrons through the insulator, and into and out of the storage region requires excessive energies. High voltages are required and the program execution time is orders of magnitude slower than for SRAM and DRAM. Also, the high energy fields contribute to insulator wear-out over many programming cycles. Table 7 shows a comparison between the characteristics of SRAM, DRAM and Flash, as well as hard disk.

	SRAM	DRAM	Flash	Hard disk
Type	Volatile	Volatile	Non-volatile	Non-volatile
Read speed	1ns	10ns	100ns – 1000ns	
Program speed	1ns	10ns	10,000,000ns – 1,000,000,000ns	
Operation voltages	1V	1V	10V – 20V	
Endurance/Cycling	10e15 ?	10e15?	10e5	
Cost per Bit	10x	1x	4x → 0.5x	0.01x

Table 7: Comparison between DRAM, SRAM, Hard disk and Flash

Initially in the early days, because the speed of flash was slower than SRAM and DRAM, and its cost/bit was high compared to hard disks, its primary application was in computer BIOS. BIOS chips required only a few hundred kilobytes and speed was not of concern. In this niche application, there was no pressure to improve the technology, and thus the pace of innovation was relatively slow.

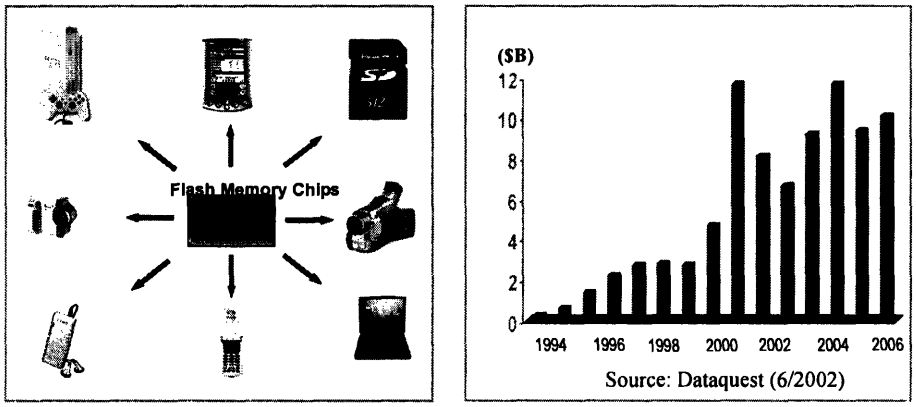

Figure 8: Rapid Flash Market Expansion

However, the 1990's brought in a new age of portable consumer and data networking applications. Suddenly data storage needed to be, not only non-volatile, but small and low power as well. Before this time, hard disk was the primary type of memory used for non-volatile storage of program code and data. But hard disk was not a practical technology choice for small portable

devices like PDA's, cell phones, MP3 players, digital cameras and camcorders. Although the cost of flash was very high compared to that of hard disk, it met the other requirements of non-volatility, small size and low power. Therefore, out of all the other available memory types, flash memory was the most logical fit.

Memory manufacturing is a very capital intensive business. Increased demand for higher volumes is the primary driver for technology scaling. By improving the ability to draw smaller geometries, chip size decreases, and more chips can fit onto a single wafer, which in turn directly reduces the chip cost. The fixed costs for equipment investments and process development are significant. Over $2-3B is required to build a single advanced fabrication center. In order to break-even in the long term, steady, high volumes are needed. Fortunately, the rate of market growth has allowed companies to enjoy profitability, even with the high equipment and R&D costs. At the moment, flash memory has avoided the cyclical tendency of DRAM. However, in the past three years, the margins have steadily fallen from an average of 40% to 20%.

During this market expansion, the pace of technology improvement has accelerated. The leading companies in the industry have invested billions of dollars in manufacturing in order to meet the demand. The rapidity of advancement has also made it difficult for followers to keep up, thus the increasing the gap between the industry leaders and the followers.

3.2.2. Flash Market - Product Value Chain

The flash memory market consists of more than 80 companies[46] which provide different components or services along the product value chain. At the base of the chain are the flash

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[46] Webfeet Research, " Flash and Alternative Nonvolatile Memories Technologies and Companies", Obtained Jan 1, 2006, <http://www.dri.co.jp/auto/report/wf/wfmt65005.htm>.

memory technology manufacturers, which supply the memory chips. NAND and NOR are the two most popular standardized chips that are incorporated in many types of products. Figure 9 describes some examples of products within the flash memory value chain. The three types of products shown are Memory Cards, Cell phones, and iPods™.

Flash memory cards such as SanDisk's CompactFlash™ are widely used in digital cameras to store pictures. To make a memory card, two,four, or eight NAND flash memory chips are usually packaged together with a controller chip. Controller chips can be made using conventional CMOS processing, thus controller chips can be cheaply manufactured by companies other than the original flash memory manufacturer. Tokyo Electron is an example of a NOR flash distributor that has moved up the value chain to include designing and selling of controller chips. The company contracts the actual manufacturing to low-cost and efficient foundries in Taiwan. Assembly of the flash cards is also usually done in companies outside of the United States and Japan because of the cost savings. As with most types of assembly, technology know-how is not very sophisticated and cost is the most important criteria,therefore the location of assembly plants are chosen to be in areas with a plentiful supply of low-cost labor.

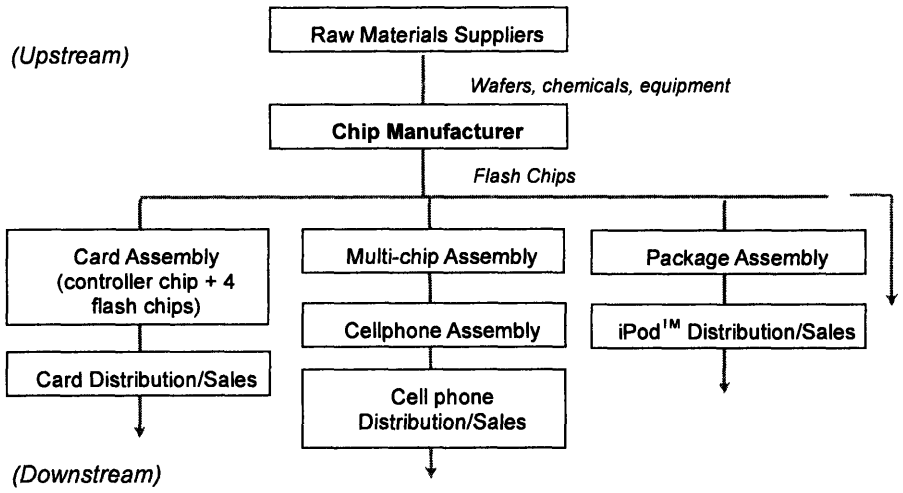

Figure 9: Flash Products Value Chain

Cell phones use NOR flash for code and data storage. Large amounts of memory are required in order to store the software to receive and transmit data signals, and address books and games, as well as other features and functions. A NOR flash chip is packaged together with SRAM in a multi-chip module. (Next generation 3G cell phones also include an additional NAND flash chip in the module.) This module is then purchased by cell phone manufacturers. It is estimated that the NOR flash memory contributes to 50-60% of the cost of a cell phone.

Another recent high-volume product that uses flash is the digital music player. Apple's Ipod Shuffle™ has gained recent popularity, but many similar types of digital media players are also offered by other major consumer electronics companies. NAND flash chips are purchased and then assembled with the other components to make the product.

3.2.3. Memory Chip Manufacturing Market

As we can see from the preceding description, memory chip manufacturers form the base of all of the products related to flash in the product value chain of Figure 9. The top ten manufacturers of flash memory chips for 2002 and 2004 are given in Table 8 below. In 2002, the top ten companies represented 70% of the total flash market. In 2004, the top ten companies represented almost 95% of the total market. In this period there were two major consolidations, AMD and Fujitsu merged their flash divisions into one company, called Spansion, and Hitachi and Mitsubishi's semiconductor companies spun off to form Renesas.

Rank In 2004	Company Name	Revenue In 2004	Revenue In 2004	Rank in 2002	Market share in 2002
1	Samsung	$3,994m	25.1%	2	12%
2	AMD/Spansion	$2,411m	15.2%	4 and 5	7%
3	Toshiba	$2,334m	14.7%	3	9%
4	Intel	$2,285m	14.4%	1	21%
5	STMicroelectronics	$1,217m	7.7%	6	6%
6	Sharp Electronics	$885m	5.6%	7	4%
7	Renesas Technology	$865m	5.4%	9	3%
8	Silicon Storage Tech	$447m	2.8%	10	3%
9	Macronics International	$334m	2.1%		
10	Hynix	$221m	1.4%		
	Others	$902m	5.7%		
	Total Revenue	$15,895m	100%		

Table 8: Top 10 Flash Companies in 2002 and 2004[47]

The flash memory market is segmented into three main types, NAND, NOR and Embedded. The characteristics of these markets are given in Table 9. NAND competes on cost and has the largest memory sizes, 1Gbit or more. The data storage flash cards in digital cameras use NAND flash. NOR type flash was developed for code storage, and its read access time is about 50ns. Chip area per bit is greater than in NAND in order to achieve fast read speed, and the memory size is also

[47] Compiled from <http://www.electronicsweekly.com/articles/article.asp?liArticleID=38701> and <www.iSupply.com>.

limited to about 0.5Gb. Cell phones use NOR flash for code and data storage. The last category, embedded, covers a wide range of applications. Embedded flash refers to the technology in which flash and logic are integrated onto a single chip. It is more application specific - for example, integration of flash for direct code storage execution with a micro-controller chip. Embedded flash is currently limited by the high cost of adding flash process steps to normal logic. Generally, the cost of an embedded part (flash + logic on a single chip) is greater than total cost of packaging two chips together (flash chip + logic chip + packaging cost). Cost sensitive products choose the separate chip package solution, but higher margin products which differentiate themselves based on performance, drive development of eEmbedded flash. It is expected that the applications for Embedded flash will continue to grow in the future.

Characteristics	NAND	NOR	Embedded
Application	Mass Data Storage	Code Storage	Code and Data
Cost ($/MBit)	0.03	0.08	0.35
Size	512Mb – 8Gb	< 512Mb	<32Mb
Competes based on	COST	PERFORMANCE (&cost)	FUNCTIONALITY (&cost)
Specification	Standard	Standard Some interface customization	Customized

Table 9: Flash Market Segment Characteristics

NOR and NAND standards were originally introduced by different companies. Intel developed the original technology and standard for NOR flash and has maintained an industry leadership position for two decades. NAND technology was developed and standardized by Toshiba. Toshiba licensed its NAND technology to Samsung in order to satisfy its customers' requirement of having an available second source supply. However, in 2004, Samsung took leadership over the original developers of both NAND and NOR flash in the same year. More recently, an American company, Micron has entered the NAND market, and combined forces with Intel for

further development of NAND. The licensees of Intel's NOR and Toshiba's NAND flash technologies are shown in Table 10below.

Intel (NOR) licensees	Toshiba (NAND) licensees
Sharp Fujitsu and AMD Infineon Winbond Toshiba Samsung	Samsung (1992 to present) Hynix (1996 to 2002) [48]

Table 10: Intel and Toshiba's licensees

Samsung is the only company that manufactures large volumes of both NAND and NOR flash memories as well as cell phones and other flash products. Its products cover the flash memory market in both the horizontal and vertical directions. It has been the only licensee of Toshiba's NAND technology since 1992.[49] Part of the reason that Samsung enjoys such a significant presence is that Korean labor and other infrastructure costs are lower than Japan and the United States. The company also aggressively pursues economies of scale with large manufacturing volumes.

3.2.4. IP Value Chain for Flash Chips

In order to understand the ways in which the technologies of each company compete with and complement each other, it is important to understand that the subject matter of intellectual property can also be mapped to a type of IP value chain. If the highest degree of competition occurs between companies occupying the same stage of the product value chain, then we would expect the

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[48] EE Times, "Toshiba files ITC suit against Hynix", Oct 4, 2005, Obtained Nov 4, 2005, <http://eetimes.com/news/semi/showArticle.jhtml?articleID=171202788>

[49] Toshiba Press Release, "Toshiba and Samsung Electronics to Cooperate on SSFDC Development and Standardization" Jun 5, 1996, Obtained Jan 10, 2006, <http://www.toshiba.co.jp/about/press/1996_06/pr0501.htm>.

technologies would also behave similarly. For example, an innovation in a new packaging technology should not pose much of a threat to chip manufacturers.

The components of a typical flash product, SONY MemoryStick™, are illustrated in Figure 10. This product is used as data storage media for consumer electronics products such as digital cameras, camcorders, laptops and MP3 players. The 1GByte flash card is made up of 8 NAND flash chips, 4 on each side, and one controller chip. The bus interface and protocol to transfer commands and data between the chips is standardized.

The 1Gbit flash NAND chip is also a standard component. This chip consists of memory cells arranged in a two dimensional array. A single memory cell can be accessed by a unique set of X and Y addresses, which are controlled by decoding circuits surrounding the memory array. There are three basic accessing operations, read, program and erase. The erase operation is performed before any other operation, it resets the states of all the memory cells in the selected block., so that all the cell states are "1". In the program operation, write circuits determine the appropriate voltages to apply so that the selected memory cells will switch to "0". During read operation, sensing circuits "sense" the signals of selected memory cells. The actual design of these circuits is dependent on the type of memory cell, but generally speaking, there is a large degree of freedom in how these circuits can be described. This is not the case for the memory cell; its structure and operation are constrained by a host of complex variables, such as the physics of electron and hole behavior under different voltage conditions, manufacturing limitations, number of device terminals, etc. To make a simplistic analogy to the software world, memory cells are to basic language constructs, as circuits are to programming code. In electronics, functions are implemented with circuits, and in software they are implemented by code. In both cases, there is a high degree of freedom in the implementation of functions, whereas the language constructs and memory cells are more fundamental and less flexible.

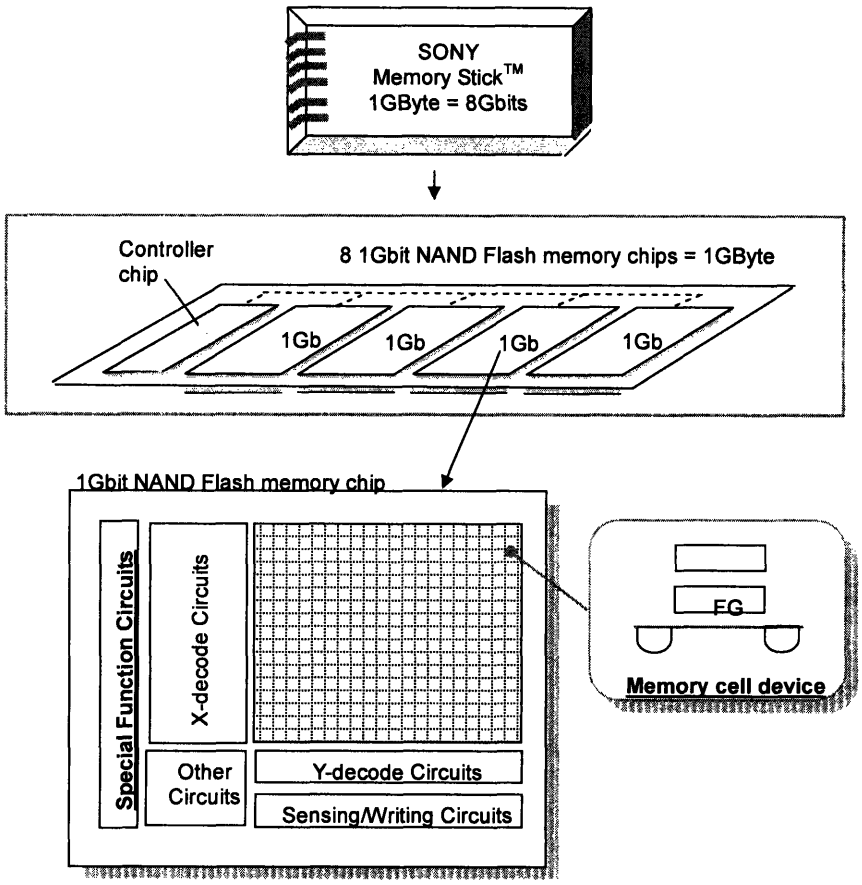

Figure 10: SONY MemoryStick™ Components

The flash value chain for a typical flash product can be mapped to the IP value chain as shown in Figure 11. In this figure, the IP that is included to make a flash memory chip is enclosed by the dotted grey line. The categories of IP are divided into two stages, Memory (Chip) Technology and Product Specific Technology. The flash memory chip specific technology is all of the IP related to making the flash memory chip, in a semiconductor manufacturing plant. The product specific technology refers to the layers of technology on top of the flash memory chip, needed to make a product.

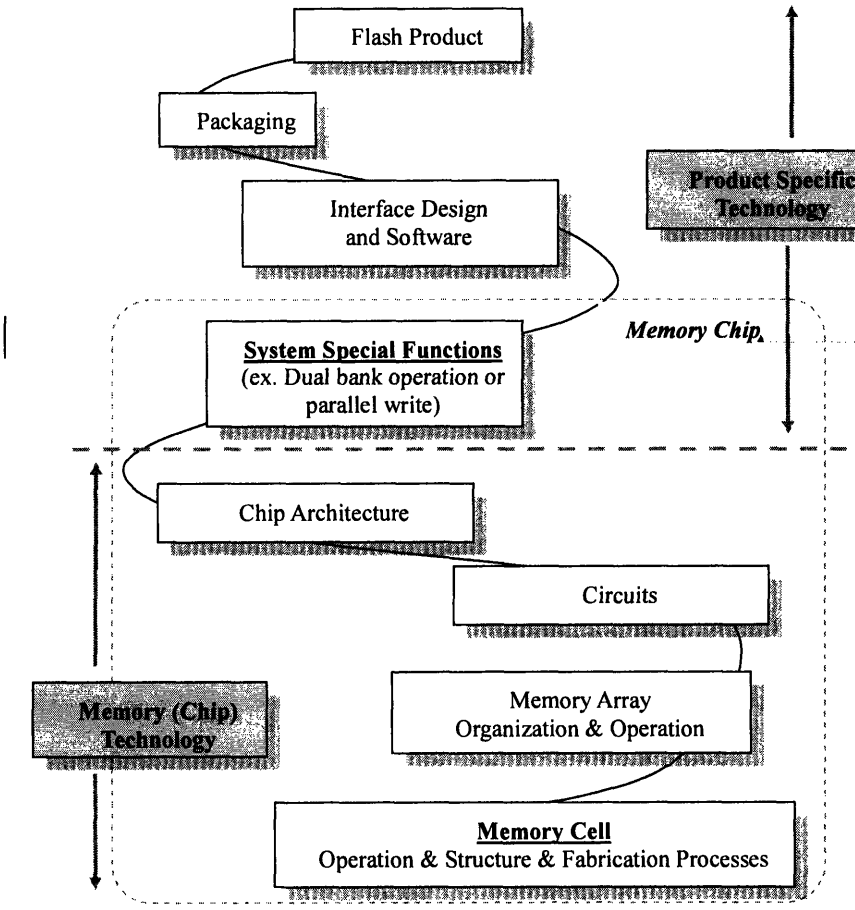

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Figure 11: Flash Intellectual Property Value Chain

It is generally understood that certain categories of IP are more critical than others for patent positioning. In Figure 11 we propose that the underlined categories are the most fundamental and difficult to design-around.

In the Memory Chip technology area, there is a tendency for the "critical-ness" of a patent to increase with movement down towards the root of the flash IP value chain. For example, at the

most primary level, memory cell structure and operation is fundamental. Flexibility of implementation increases going along the chain. Patents that cover the memory cell and operation are stronger than circuit patents, because circuits are highly flexible and are characteristically easy to design-around.

At the product specific technology level, interface and other behavioral patents can also provide strong protection. If a special function has been patented, and this function is required by all compatible chips, then that patent is strong. Although the function may be implemented by several circuit variations, since it the behavioral function itself that has been constrained, the associated patent has the power to prevent others from being able to make a compatible product. An example of such a behavioral feature is Intel's *read-while-write,* which is a function in a standard NOR product. This feature allows a user to read from one block at the same time that a different block is being programmed or erased.

Due to standardization, interface related patents may be strong in the same manner as the special function behavioral patents. Interfaces between components need to be standardized, in order to minimize design cost and time. SONY MemoryStick™ standard is an example of interface/behavior related IP. All memory stick compatible providers are required to join the SONY MemoryStick ™ consortium and to license the associated patents and know-how. Thus, SONY's patents at the product level have significant power.

The terms NOR flash and NAND flash refer to types of chip technologies. A more detailed description of these technologies and markets will follow.

3.2.5. NOR Flash Market

Intel is the original manufacturer of NOR type flash memory chips, and still maintains leadership in

this market. NOR flash provides high performance capability to store program code. But because the size of the software programs is always increasing, there is a corresponding demand for higher density Flash at lower cost. Intel's position within the NOR flash market will be examined using Porter's Five Forces model, as illustrated in Figure 12.

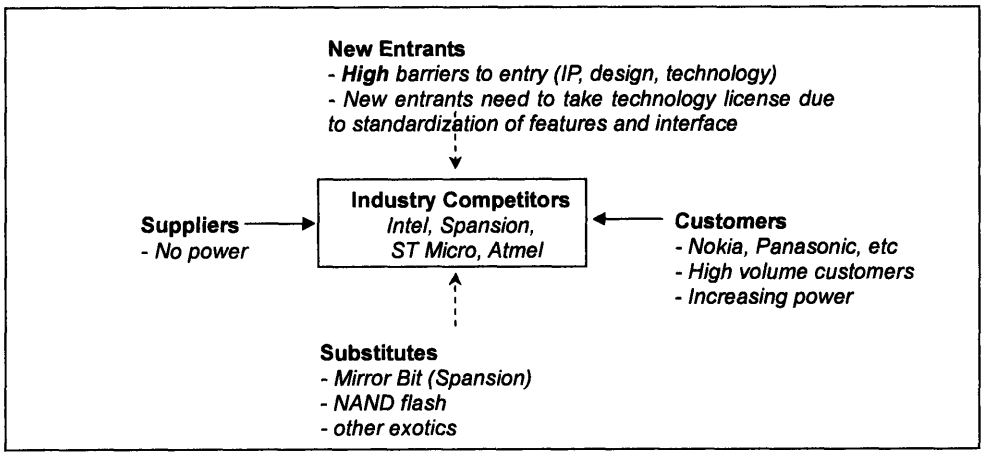

Figure 12: Porter's 5 Forces applied to Intel's NOR product

New entrants: Flash memory, in general, has high barriers to entry, because the memory process technology is very difficult and expensive. It can easily take five years to qualify a new process technology to meet difficult reliability and retention standards.

Over the years, Intel has built many design features into its NOR products, including a software interface and compiler. Its consistent dominant position has made it the *de-facto* standard. Making an Intel-compatible chip is complicated and requires several iterations to ensure that every feature behaves exactly as it should. Some of the design features like *read-while-write* are protected by strategic function or architecture patents that are almost impossible to bypass. As a result all of the companies who compete with Intel must have cross-licensing agreements. A limited degree of cross-licensing is permitted because Intel recognizes that customers will require a

second source, and because it has run afoul of the Sherman Act in the past.

Industry competition: Intel has maintained its dominant position in the NOR market segment. It is difficult even for competitors with legitimate cross-licensing rights to keep up with Intel's speed of development and sales volumes. Intel channels a great deal of its R&D funds towards continuous flash memory development and controls the standard for NOR type flash. With every successive generation, its chips are becoming smaller, lower power and faster. With the exception of Spansion (the merger between AMD and Fujitsu), competitors usually provide lower-end, lower-density NOR products that are one or two generations behind.

Customer power: Customers wield some power, because they tend to have large orders and specific performance requirements. The NOR type flash is used for code storage in cell phones, set top boxes, and digital cameras. In the past few years, the buyers have passed on their pricing pressures to Intel. In 2000, Intel's margins were 40%, they dropped to 30% in 2001, and 2002, were 20%.

As mentioned previously, customers require a second source in order to ensure low prices and availability of supply. For this reason, Intel was forced to share IP in a partnership with Sharp, and later provided a royalty-free cross-license to AMD. Thus customer power prevents Intel from completely monopolizing the NOR flash market.

Supplier power: Intel manufactures flash memory chips. Its suppliers are chemical and equipment companies. Usually these companies do not have significant power over Intel. Because Intel is a large and leading edge customer, the equipment companies frequently work closely with Intel to provide complementary services or to develop the tools to meet Intel's special needs.

Substitutes: NOR Flash is unlikely to be replaced by another non-flash technology in the near future. There are several alternatives being developed based on exotic new materials, such as FeRAM and MRAM, as well as ouvonic and R-material. But these are still far from mature. (NAND was invented as a low-cost alternative to NOR) Another type of substitute is the pairing of high speed SRAM with low cost Flash, like NAND. Some of the earliest PDA's used this approach, but it was not cost effective for larger memory sizes. Recently, Samsung has announced a new project initiative called ONE-FLASH, which combines NOR and NAND into one chip.

Thus the NOR market is very difficult to penetrate due to the high capital costs, strong existing bonds with customers, and IP protection at the product and interface level. However, in terms of market growth, demand for NOR has slowed down in recent years. NAND sales overtook NOR sales as of 2004. As cell phones incorporate more applications like pictures and MP3 players, their data memory requirements are increasing in addition to their existing need for code memory. Furthermore, if the ONE-NAND is realized, Intel's sales to cell phone companies will be severely affected.

3.2.6. NAND Flash Market

NAND flash was invented in Toshiba, as a low-cost standard product. Its purpose is to provide high density mass storage at the lowest possible cost. The interface was standardized by Toshiba, who was market leader until 2002, when it was overtaken by Samsung. Figure 13 shows Toshiba's strategic position, described using Porter's 5 forces framework.

New entrants: NAND's manufacturingprocess technology is considered slightly more demanding than NOR, because high density requires aggressive scaling techniques. The process defect

density must be tighter since memory sizes are larger too. On the otherhand, the circuit design is more simple and functionality is not as restricted by patents as in NOR circuits. Furthermore, the performance criteria for NAND is much more relaxed than for NOR. Overall, the technology and patent barriers to enter the NAND market are easier than for NOR.

Industry competition: Because cost is the primary basis for competition, the manufacturer that can operate at the lowest cost wins in this market. Toshiba originally introduced the concept of NAND flash and dominated the market until 2001. However in 2004, its lead was overtaken by Samsung. Located in Korea with lower labor costs and favorable currency exchange rates, Samsung's overall cost structure was lower than that of Toshiba. The irony of this situation is that Toshiba originally licensed the NAND technology to Samsung in order to satisfy the customer's second source requirements. The other competitors such as Mitsubishi and Renesas use alternative internally developed technology memory array structures that are not as cost effective as Toshiba and Samsung. In fact in the final month of this thesis research, December 2005, Renesas cancelled its NAND-flash compatible program.

Customer power: Compared to the NOR industry, customers have more power in the NAND market. They are not locked into any single supplier. Since NAND is standardized, they can shop for the lowest cost product. This arrangement is extremely difficult for the manufacturers, because the manufacturers require high volumes in order to spread out the fixed costs.

A further example of customer power in the NAND market is the recently announced joint venture between Micron and Intel for NAND flash development. Apple Computer is said to be a big influencer in the decision to form the joint venture. It is pre-paying $500 million to this joint

venture, in order to guarantee supply of memory for its Ipods until the year 2010. [50]

Supplier power: Supplier power is low, just like in the NOR market.

Substitutes: There are not many substitutes for low-cost mass storage NAND flash. Alternative approaches are NOR flash and small form factor hard drives. But the NOR flash is not cost effective. Hard drives consist of mechanically moving parts which require more current and are more fragile, both characteristics that are not good for low power, portable applications.

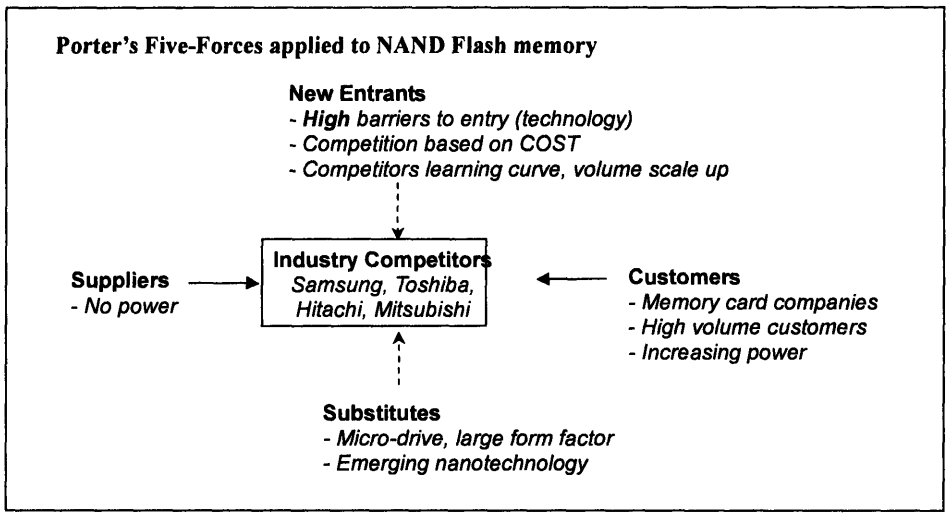

Figure 13: Porters 5 Forces applied to Toshiba's NAND product

Thus, although the NAND market may be easier to penetrate from a design and patent point of view compared to the NOR market, it is more competitive, with lower margins.

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[50] Kawamoto, Dawn, "Apple lines up for Intel-Micron flash" CNET News, Nov 28, 2005, Obtained Jan 10, 2006 <http://asia.cnet.com/reviews/hardware/desktops/0,39001729,39293838,00.htm>.

3.2.7. Embedded Flash Market

Both NAND and NOR are highly competitive standardized markets. In contrast, the Embedded Flash market has more types of products, albeit each product has a smaller volume of sales. The main challenge with Embedded Flash is the extra complexity and process cost. Furthermore, since the volume of sales for each Embedded Flash products is much smaller than for the NAND and NOR, technology development costs can not be recouped as easily. Therefore, Embedded flash companies follows a Foundry model, rather than manufacturing themselves.

Foundry model Silicon Storage Technology (SST) is currently the leading Embedded Flash company. It has licensing agreements with several foundries. The foundry model was developed due to the high cost of building manufacturing facilities, and is essentially a manufacturing center for many customers. The customer designs a chip and the foundry manufactures it. The most conventional technology is CMOS logic and using registers and SRAM for on-chip memory, but there is increasing interest in flash memory integration. If non-volatile memory can be embedded onto the chip, access times can be reduced and chip performance increases. SST provides an Embedded Flash solution. However, the incremental cost of SST's Embedded Flash technology over a conventional CMOS process is very high, almost 30%, so the cost of logic portion of the chip is also penalized. Thus, SST's Embedded Flash provides performance and functional enhancement, but is not a low-cost solution.

3.2.8. New Memory Cell Technology

The conventional floating gate memory cell device has dominated Flash for over thirty years. However, there are several new up-and-coming challengers. This author has especial interest in

an alternative storage media called "trapped storage", in which electrons are stored in an insulator rather than the conductive polysilicon gate of floating gate memories. The most common trapping media is nitride, but several other variations are being explored.

3.2.9. Nitride Storage Memory Devices

Conventional flash memory products are based on the floating gate device, in which electrons are stored on an insulated floating polysilicon gate. However, as technology scales to smaller and smaller dimensions, the floating polysilicon gate has limitations, due to oxide defects, high electric field and high aspect ratios. Many alternative memory cells have been proposed, with varying degrees of acceptance.

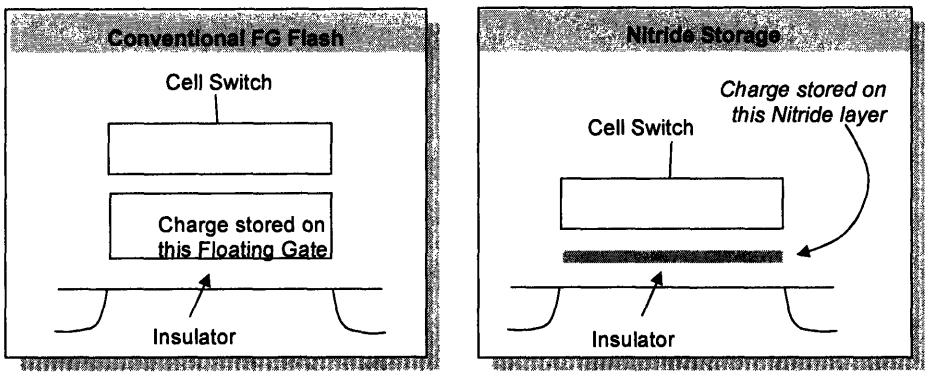

Figure 14: Nitride Storage vs. Conventional FG Storage

Nitride trap storage is an established alternative storage medium to floating gate. In this type of memory device, electrons are stored into a nitride layer instead of floating gate. SeeFigure 14. There are some advantages in the material properties of nitride that improve scaling and reliability. Renesas, formerly Hitachi and Mitsubishi, has been using a nitride device, called SONOS, for its embedded smart cards. Smart card is considered a niche product, compared to NOR and NAND volumes, but this market is also growing rapidly, especially in Europe. Recently there has been a

renewed interest in using nitride, in a slightly different way, in order to make next-generation NOR and NAND products.

Saifun Semiconductor is one of the leaders of the renewed nitride storage movement. It was generously funded by the Israeli government and formed a partnership with Tower Semiconductor Manufacturing, also in Israel. By creatively applying the principles of "reverse read" and "drain induced barrier lowering" effect, two bits may be stored within one single cell, effectively doubling the cell density. The technology process is simple, and the value proposition is attractive. Saifun has licensed its memory cell technology to several companies, like Matsushita, Macronics, Spansion, and SMIC. The most successful of these licensees to date is Spansion, which has a series of products called Mirror Bit, that directly compete with Intel's NOR, based on this nitride storage principle.

Halo LSI is another company that started working with nitride memory around the same time as Saifun. The technology is called ***Twin MONOS***. Although the nitride material properties are similar to Saifun's, the device structure and properties are different, as shown in Figure 15. As a result, the device can operate at faster and at lower power, and has better scalability in the future.

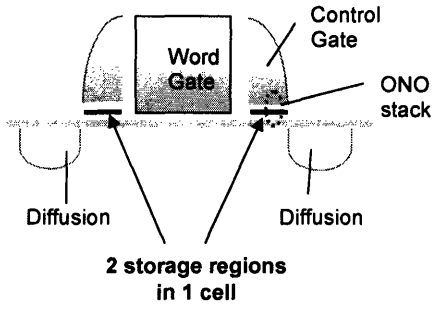

Figure 15: Halo LSI's Twin MONOS Cell

It is one of the primary goals of this thesis to understand the current status of nitride flash and its future potential to impact the conventional NOR and NAND markets.

3.2.10. Other flash memory device alternatives

Besides nitride, several other types of memory cell devices are also under development:

FeRAM: In Ferroelectric memory (FeRAM), data is stored as a fixed polarization within a special dielectric material. The endurance is high, about 10e12, however read is destructive, which reduces the range of possible applications.

FeRAM's support camp includes Hynix, Texas Instruments, and OKI, Celias Semiconductor, Kentron Technologies, Ramtron, and Rohm. Symetrix Corp has a Non-destructive Read-out (NDRO) FeRAM technology called "Trinion". In 2003, Symetrix licensed its technology Oki Electric.[51]

MRAM: MRAM has theoretical read and write speeds of 2-3nsec, which makes it a prime candidate to replace SRAM and and other applications that can use non-volatility with high performance. The difficulty with this technology is the manufacturability. Even a 0.1A variation of oxide thickness can lead to magnetic tunneling junction resistance changes of several percentage points.[52]

MRAM's support camp includes Cypress Semiconductor, IBM, Infineon Technologies, Motorola,

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[51] OKI Electric News Release, "Trinion cell provides Key to NDRO-FeRAM Accord", obtained Nov 5, 2005, <http://www.electronicstalk.com/news/oki/oki124.html>.

[52] Clendenin, Mike, EE Times, "MRAM and FeRAM are at the finish lineObtained Nov 5, 2005, <http://www.eet.com/story/OEG20030326S0047>.

3-D Memory (Matrix Semiconductor): Matrix semiconductor uses a diode-based approach to non-volatile memory. By stacking layers of memories, the effective area of a single bit can be very small. Current applications are restricted to One-Time-Programmable (OTP) products like Nintendo's game cube software cards or the voice chips in stuff animals. In November 2005, Matrix was acquired by SanDisk.

Ovonyx Phase-Change: Phase-change media is another method of non-volatile memory storage. Although different companies focus on different material compositions, the common characteristic of phase-change memory is that the material's crystal structure can be manipulated to change the device's resistance by one to two orders of magnitude. This change can be brought on by either high current or heat. Ovonyx is a company currently pursuing commercialization of its array-addressed memory systems through joint development programs with a number of licensees including BAE Systems, Intel, ST Microelectronics, Nanochip and Elpida Memory.

3.3. Summary

The flash memory industry has rapidly evolved in the past twenty years, due to the recent explosive demand for portable consumer electronics. In this section, we explained the basic characteristics of flash memory, the main products and the companies that make the products. We also described some of the major alternative technologies that are currently under development. Nitride-based flash is one of the primary candidates to replace the main-stream floating gate flash in the future. This introduction sets the stage for subsequent discussions about intellectual property licensing within the Flash industry, as well as further exploration with regard to the potential of nitride-based

flash.

4. Licensing in the Flash Memory Industry

4.1. Licensing Strategies of Chip Manufacturers

There is a great deal of licensing and litigation activity in the flash memory industry. In this section, we will see how the general strategies described in Chapter 2 can be applied to the flash memory industry.

Licensing as a Function of Products, Industry and Resources

Kotobe, Sahay and Aulakh's theory of "Licensing as a Function of Products, Industry and Resources" described in Section 2.3.6, appears to be consistent with our understanding of the flash industry. We find that the memory chip products have high positive network externalities due to the standardization of the NAND and NOR products. Since the introduction of NOR and NAND chips, more than ten years ago, there has been no new standard component. Intel and Toshiba also have several licensees of their technology. Furthermore, we see some evidence of "brand" buying in that the chips that are specified with lower cycling ability are not received favorably, even though the application requirement may not need such high reliability. This behavior fits the authors' theory that there is more licensing where there are higher requirements for compatibility.

The second component, industry level, includes both factors of (i) industry structure and (ii) technology intensity. Since the memory chip manufacturers enjoy margins greater than 20%, we conclude that the industry structure is "intermediate" and thus there is a fair degree of licensing. In other areas of the value chain further downstream where competition is more intense, the relationships between companies are much less amicable and more litigious. Regarding technology intensity, semiconductor manufacturing falls into the category of high intensity, because

R&D and other early stage costs are high.

Finally, the resource factors: whenever complementary assets are low, more technology licensing would be expected. We can explain the lower complementary assets in the following way – flash memory technologists are narrow specialists. It is difficult for them to cross over to other areas. Therefore, products can not be changed often or easily, and licensing of technology may seem more suitable than building up the expert resources in-house.

Thus, the theory of "Licensing as a Function of Products, Industry and Resources," explains licensing behavior in the flash memory industry very well.

Licensing Pre-empts Invention

We also find that some elements of Hill's framework which was described in Section 2.3.7, "Licensing Pre-empts Invention", also bear out in the flash memory industry. Hill said that when an innovation is successful and attracts the attention of many imitators, the imitators will eventually find a way to invent around a patent. Therefore, it may be better for the innovator to license the technology in order to at least share the profits of his competitors.

Referring back to Figure 4, we can see how the Decision Framework works in conjunction with other factors during the building of the NOR and NAND standards. It was previously discussed that both Toshiba and Intel licensed their technologies to third parties in order to satisfy their customer's requirements for second sourcing. At that time, the profit margins were high and the capable competitors were enticed to license rather than building competing standards, thus Toshiba and Intel could effectively spread their standard and consolidate their position as standards setters. Intel went even further to entrench its position by continuously adding features to its NOR product over the years. More recently, at this time when the market has become more competitive with

lower profit margins, Intel is able to block new entrants, because designing around all of the accumulated features has become too difficult.

Unfortunately, the Decision Framework does not give a clear prescription to license or not license with regard to the current situation of NAND. The original NAND patent will expire in 2007. Some DRAM makers like Hynix and Micron have been refitting their capabilities to design and make NAND chips. In this case, we would follow the right fork of the Decision Framework: the barriers to imitation have been lowered by the expiration of the patent → competition intensity is high → and competitor capability is high → ?. Thus, Toshiba's current position appears to be untenable. "

Licensing vs. In-house R&D

In Section 2.3.8, "Licensing vs. In-house R&D", Gan's discusses how companies should focus their resources on developing core products and license out its ancillary ideas. For this theme, we will focus on the Embedded Flash foundry and Design House model.

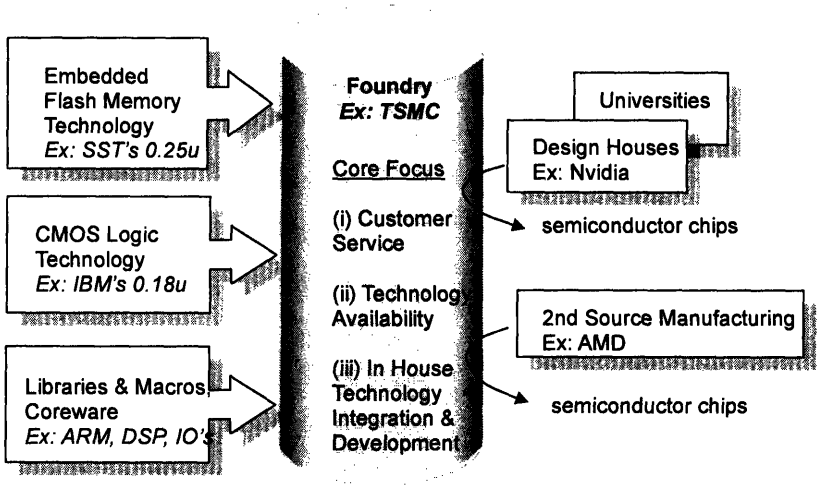

Figure 16: Foundry Licensing Model

Figure 16 shows an example of a semiconductor foundry's operation. Taiwan Semiconductor Manufacturing Corporation (TSMC) is one of the largest foundries in the world. It provides manufacturing services to design houses and universities that do not have their own manufacturing capability, or to other manufacturers that need a second source supplier. TSMC can not be an expert in every kind of technology, but it needs to supply the best low-cost total solution to its customers. Therefore, TSMC relies on licensing in order to complete its technology lineup. Embedded flash memory companies such as SST work with TSMC to install their technology and build libraries of macros so thatcustomers can incorporate the flash blocks into their logic designs. In this type of arrangement, TSMC typically pays SST a royalty of 1-2% of the wafer cost.

The Patent Thicket: How licensing affects other firms

The patent thicket that was described by Shapiro and Jaffe, among others, is clearly a problem in the flash memory industry. We can see the evidence of this in the numerous cross-licensing agreements and lawsuits and counter-lawsuits. The next section will explain more details about the interactions between the companies and IP licensing.

4.2. Flash Memory Licensing Activities

4.2.1. Licensing Agreements

A summary of some of the major licensing and cross-licensing relationships between the flash memory companies is given in Table 11.

Party 1	Party 2	Litigation involved?	Date	Description
Intel	AMD	Note 1	1976	Cross-licensing for Flash since 1976 Renewed for May 2001, for 10 more years[53]
Intel	Sharp	No	1992	NOR
Motorola	AMD	no	July 1998	Embedded flash memory
Micron	Mostel	Yes	Mar 2000	DRAM
SanDisk	TDK	no	July 2000	Flash memory integrated circuits and card products(from SanDisk) Flash card products (from TDK)
SanDisk	Hitachi	no	Oct 2000	Binary and multi-level flash
Sharp	Winbond	No	Nov 2001	Advanced Contactless Tech (Sharp proprietary)
SanDisk	Lead Data	no	July 2002	Flash memory card patents, including Compact Flash but not Secure Digital or Memory Stick (SanDisk) Memory and memory card patents (from Lead Data)
AMD/Fujitsu	Saifun	yes	July 2002	
Samsung	SanDisk	yes	Aug 2002	Flash memory and card patents for next 7 years
EMC	Hitachi	yes	Mar 2003	Hard disk software
SanDisk	Silicon Systems	no	June 2004	Solid state disk drives
M-Systems	SanDisk	no	Sept 2004	USB flash drives
Toshiba	Microsoft	no	April 2005	Computer and consumer electronics technologies, details confidential
SanDisk	SONY	No	Sept 2005	Memory micron format
SanDisk	Sharp	?	?	ETOX and MLC Sharp pays Sandisk royalty fees
Intel	Micron	no		NOR boot block, NAND flash
Samsung	SONY	no	Dec 2004	24,000 patents (confidential)
Intel	SST	no		Interface
SanDisk	Samsung, Toshiba, Sharp, Renesas			

Table 11: Cross-licensing agreements for flash products

In this Table, we can see all the licensing activities between the major NAND and NOR manufacturing partners during the early stages of standards building. The chip standard became

[53] AMD Press Release, "Intel and Advanced Micro Devices Renew Patent Cross-License Agreement", May 4, 2001, Obtained, January 10, 2006 <http://www.pcstats.com/releaseview.cfm?releaseID=572>.

de-facto around the year 2000. After that, we see more licensing activity at the product IP levels. Consistent with this observation, we also see more litigation after the year 2000. We speculate that this could be due to the increasing maturity of the market and competition.

4.2.2. Litigation

The threat of litigation provides a strong disincentive to infringe. However, the so-called *patent thicket* is very complex and rife with overlaps, so that maintaining a policy to completely avoid infringement is nearly impossible. This is complicated by the ambiguous nature of patent claims, especially when words can be interpreted differently from jury to jury, and oftentimes judgments can be overturned upon appeal. Some examples of litigation will be described below. It is our belief that the licensing and litigation follows in general accordance to C. Hill's *Decision Framework*, with additional consideration to two other factors, i) market maturity and ii) position of the company along the IP value chain. In the discussion of the IP value chain, we determined that patents derive strength by being fundamental and difficult to design around due to either i) physical constraints or ii) standard constraints. In the first case, physical constraints usually occur at the highest level of the IP value chain, around the Memory Cell technology level. In order to establish standard constraints, it is first necessary for companies to gain some measure of universal acceptance; joint development through consortiums and/or licensing the standard are common methods. When the market is more mature, characterized by falling profit margins, we see that the product patent holders become more active against other product distributers. In the examples of litigation that follow, we see that product patent holders litigate against others, with no license given at the conclusion. However, during the early stages of market development for Product companies, or for companies that exist solely to disseminate basic Memory Cell Technology, licensing or cross-licensing are more common results of litigation.

Lexar Media vs. Memorex (2001-2005)

In 2001, Lexar Media claimed that Memorex infringed on its flash patents listed in Table 12.[54] Memorex (Memtek Products Inc.) sold CompactFlash cards without obtaining a license from Lexar. In the settlement, Memorex agreed to make a one-time payment for past sales and refrain from selling CompactFlash products in the future. This litigation did not result in a future license/cross-license.

Patent Number	Application Date	Title	US Secondary Classes
5,479,638	Mar 26, 1993	Flash memory mass storage architecture incorporation wear leveling technique	706/900, 711/108, 711/156, 711/165, 711/202
5,818,781	Nov 13, 1996	Automatic voltage detection in multiple voltage applications	365/189.09. 365/227
5,907,856	Mar 31, 1997	Moving sectors within a block of information in a flash memory mass storage architecture	711/156, 711/165, 711/203, 711/206
5,930,815	Oct 7, 1997	Moving sequential sectors within a block of information in a flash memory mass storage architecture	711/156, 711/165, 711/206
6,145,051	Mar 3, 1999	Moving sectors within a block of information in a flash memory mass storage architecture	711/156, 711/165, 711/203, 711/206

Table 12: Lexar Media's's Patents in Lexar Media v.s. Memorex

Lexar Media vs. Toshiba (2002 to 2005)

In 2002, Lexar Media filed three separate lawsuits against Toshiba. The first involved an accusation of stealing trade secrets. Because Toshiba had a seat on Lexar's board of directors, it was in a privileged position to learn confidential information about Lexar's fast write speed product, and then chose to partner with Lexar's competitor, SanDisk. The lawsuit was prosecuted in the United States in front of a jury. The verdict went against Toshiba, "breach of fiduciary duty and theft of trade secrets" and a fine of $380 million was imposed for compensatory damages and $84

million for punitive damages.[55] The other two lawsuits, one about unfair competition practices and the other about patent infringement of 10-14 patents are still pending. Toshiba has counter-sued in the patent infringement case.

Lexar vs. Fuji Photo Film (2002 to present) and Ritek (2002-2003)

At the same time that Lexar filed against Toshiba in 2002, it also filed separately against Fujifilm, alleging that Fuji's photo media products infringe on Lexar's patents, listed in Table 13[56]. Fujifilm turned around and involved Ritek, which was its CompactFlash card provider. Ritek agreed to settle with a one time payment to Lexar, but charges against Fujifilm were maintained until after the lawsuit with Toshiba was settled. In 2005, Fujifilm counter-sued Lexar Media for infringement of Lexar products of Fujifilm's US patents 5,303,198; 5,386,539; and 5,390,148.

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[54] Jurrien, Ilse, "Lexar and Memorex settled patent infringement", Let's Go Digital Magazine, August 15, 2005, Obtained Nov 5, 2005, <http://www.letsgodigital.org/en/news/articles/story_4070.html>.

[55] Lexar Media's press release, "California Jury Orders Toshiba to Pay an Additional $84 Million in Punitive Damages to Lexar Media, Inc:; Total damages of $465 Million, the Largest IP Verdict in California History", March 24, 2005, Obtained Nov 5, 2005, <http://www.lexar.com/newsroom/press/press_03_24_05b.html>.

[56] Lexar's press release, "Lexar Media Settles Patent Dispute with Ritek Corporation, Supplier to Fuji Photo Film, U.S.A.", Oct 3, 2003 Obtained Nov 5, 2005, <http://www.lexar.com/newsroom/press/press_10_03_03.html>.

Patent Number	Application Date	Title	US Secondary Classes
5479638	Mar 3, 1993	Flash memory mass storage architecture incorporation wear leveling technique	705/900, 711/108, 711/156, 711/165, 711/202
6145051	Mar 3, 1999	Moving sectors within block of information in a flash memory mass storage architecture	711/156, 711/165, 711/203, 711/206
6397314	Nov 2, 2000	Increasing the memory performance of flash memory devices by writing sectors simultaneously to multiple flash memory device	365/189.04. 365/230.03, 711/5, 711/103, 711/202h
6202138	Jan 20, 2000	Increasing the memory performance of flash memory devices by writing sectors simultaneously to multiple flash	365/189.04, 365/230.03, 711/5, 711/103, 711/202
6262918	Jun 30, 2000	Space management for managing high capacity nonvolatile memory	365/185.29, 365/218, 365/230.03
6040997	Mar 25, 1998	Flash memory leveling architecture having no external latch	365/189.05

Table 13: Lexar's patents in Lexar vs. Fujifilm

Toshiba vs. Hynix (2004– present)

Toshiba and Hynix had a cross-licensing agreement between 1996 to 2002. However, in renewal negotiations, they were not able to come to agreement on the licensing terms. In 2004, Toshiba filed a suit against Hynix for infringement of its DRAM and NAND flash patents.[57] It is currently pursuing an additional suit to stop the import of Hynix products into Japan and the United States.

Sandisk vs. ST Microelectronics (2005– present)

SanDisk sued ST Microelectronics regarding the claimed infringement of Patent 5,991,517 (see Table 14) by ST Microelectronics' NAND and NOR products. This patent covers a basic algorithm to program a flash memory cell. In this first action, ST Microelectronics won the suit and was legally declared to be innocent of infringement. However, on appeal, the court

[57] Global Sources, "Toshiba files lawsuit against Hynix", Oct 5, 2005, Obtained Nov 5, 2005, <http://www.globalsources.com/gsol/I/Multifunction-USB/a/9000000067489.htm>.

overturned the ruling and reinstated the lawsuit.

.Patent Number	Application Date	Title	US Secondary Classes
5,991,517	Dec 20, 1996	Flash EEPROM System With Cell by Cell programming Verification	714/8

Table 14: SanDisk's patents in SanDisk vs. ST Microelectronics

Saifun vs. AMD/Fujitsu (2002)

In 2002, Saifun sued AMD and Fujitsu for violating its patents of Memory Cell Level Technology. Although there were allegations of breached confidentiality in addition to patent infringement, the end result was that Saifun licensed its technology to AMD/ Fujitsu (now Spansion).

4.3. Conclusion

Thus, we can see many activities of licensing and cross-licensing among flash memory companies. Some speculations were raised as to whether the behavior could be explained by looking at the company's position on the IP value chain and the market maturity. We will return to this topic in the following section.

5. Patent Analysis

5.1. Flash Memory Patents

Patents are an important building block to the intellectual property strategy of a technology company. In order to extract future value from research and development activities, companies need to have a means to map and evaluate their own patents. Looking at patents also allows us to understand the positions of industry players to an extent beyond that which is available by general public disclosures and news. In this section, we will look at flash memory patents of flash memory chip providers. The purpose is to i) understand the general positions and ii) identify trends, especially with respect to the nitride flash movement.

5.2. Using IPVision[SM] on the US PTO database

First, we would like to collect all the patents related to flash. There are over five million patents in the United States, and every year, the United States Patent and Trademark Office (US PTO processes over three hundred thousand patent applications and grants about eighty thousand.[58] Identifying the patents relevant to flash memory and managing the large volume of data requires a specific software solution.

IPVision[SM] is a software system that has been developed by Main Street Partners in order to analyze patent portfolio and positions. Figure 17 shows how IPVision is linked with the USPTO Online Database through a web-interface. The USPTO online database maintains two types of data: (i) patents from 1976 to the present, and (ii) published applications from 2001 to the present. Using the IPVision software interface, the user can quickly access USPTO patent summary information about the dates, inventors, claims, and class categories. Lists resulting from searches, can be compared or combined or subtracted, and several kinds of analysis can also be conducted.

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[58] Office of Electronic Information Products, Patent Technology Monitoring Division, "U.S. Patent Statistics Chart Calendar Years 1963-2004", U.S. Patent and Trademark Office, Obtained Nov. 4, 2005, <http://www.uspto.gov/web/offices/ac/ido/oeip/taf/us_stat.htm>.

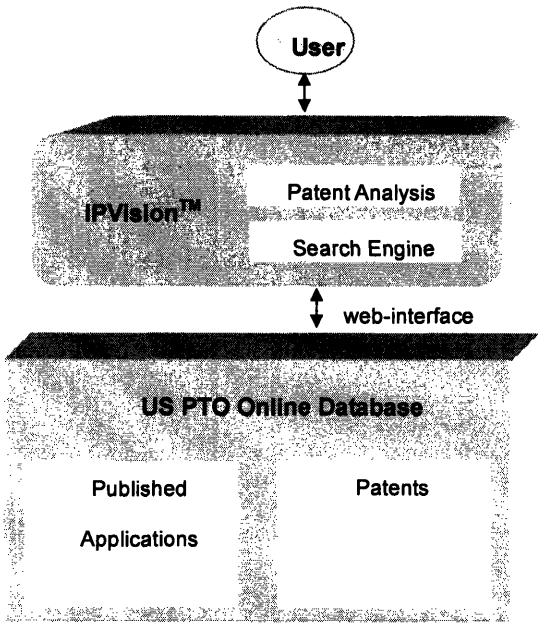

Figure 17: IP-Vision system for patent analysis

Figure 18 shows the top portion of an IPVision patent data record. (The full text of this particular patent data record can be found in Appendix B1.) In this example, the patent number is 6934190, the title is "Ramp source hot hole programming method for trap based nonvolatile memories", and the assignee company is AMD, which is located in Santa Clara, California. The application was first filed in June of 2004, and was granted as an issued patent in August of 2005.

Patent Number:	6934190
Title:	Ramp source hot-hole programming for trap based non-volatile memory devices
Abstract:	Methods of operating dual bit memory devices including programming with a range of values are provided. The present invention employs a range of ramp source program pulses to iteratively perform a program operation that employs hot hole injection. The range is related to channel lengths of individual dual bit memory cells within the memory device. To program a bit of a particular dual bit memory cell, a negative gate program voltage is applied to its gate, a positive drain voltage is applied to its acting drain, and its substrate is connected to ground. Additionally, a ramp source voltage of the range of ramp source program pulses is concurrently applied to an acting source of the dual bit memory cell. A verification operation is then performed and the programming is repeated with a decremented ramp source voltage on verification failure.
Issue Date:	20050823
Agent:	Eschweiler & Associates, LLC
Application Date:	20040609
Application Serial Number:	863933
Application Series Code:	
Assignee Addresses:	Sunnyvale, CA
Assignees:	Advanced Micro Devices, Inc.
Assistant Examiner:	
Claims:	1. A method of programming a bit of a dual bit memory device comprising: applying a negative gate program voltage to a gate of the memory device; applying a drain program voltage to an acting drain of the memory device; and iteratively applying a range of ramp source voltages to an acting source of the memory device. 2. The method of claim 1, wherein applying the range of ramp source voltages comprises: selecting an initial value as a ramp source voltage; applying the ramp source voltage to the acting source

Figure 18: Partial Patent Data Record Example

By accessing the patent database, patents can be mapped along various dimensions. For example, products can be divided to technical categories, and the associated patents can be graphed according to the assignee or the inventor or the date or with reference to other patents.

Patent analysis by this methodology can provide insight about many things, such as i) who are the main patent holders, ii) relationships between technologies of companies, iii) correlation between high patent activity and product development, iv) identification of emerging technologies, and v) identification of confidential technology development activity.

5.3. Flash memory patents as an aggregate

5.3.1. Identifying all flash-related patents

Gathering all of the patents related to flash memory is not a straightforward procedure, because there is no specific category reserved for "Flash Memory" in the US PTO system. The number of "memory" patents in the US PTO database is close to forty-thousand. When the Patent Office formed the classification system, it combined all of the memory types together, and sub-divided based on function and characteristics. Therefore many classes contain SRAM and DRAM patents as well as flash patents. In order to extract the flash related patents from the US PTO database, we used a combination of key word identification, class-pair filtering and assignee and inventor searches. This search procedure is shown by the block diagram in Figure 19. The first step is the keyword search. Many patents can be found by searching for key words that are uniquely related to flash in the patent title, abstract, specification or claims. However, patent law does not require an inventor to describe his or her invention using specific words, which makes searching by keywords a hit or miss proposition. Despite this limitation, keyword searching is a good starting point. In the second step, we perform a class-pair analysis on the patents that were found in the keyword search. By identifying the class-pairs that are unique to flash memory, we can find more patents. Finally, in the final step, we can track assignees or authors on an individual basis to find patents that could not be found by either of the previous key word or class-pair search procedures.

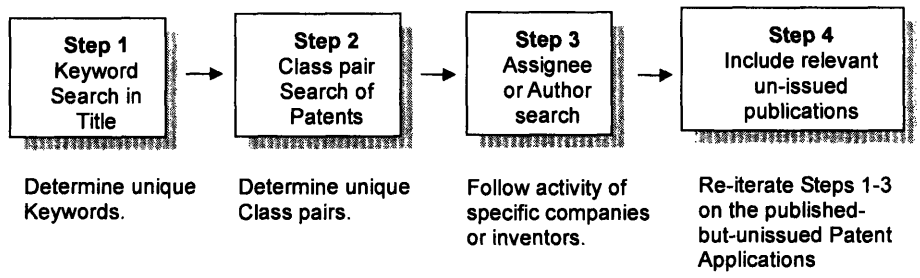

Figure 19: Searching Procedure to Find All Flash Patents

Step 1) Key words in title or abstract

Table 15 gives a list of the key words that were input as search parameters into the USPTO patent search website via the IPVision system. The list was expanded incrementally as we gained experience with the database and identified new flash related word phrases. More details about the actual procedure are given in Appendix B1. The number of patents that resulted from this search was 11823 patents.

	Key Words in Patent Title
K1	((stack or split) and gate)
K2	(((program and verify) or (erase and verify)) or (electrically and erasable) or (programmable and memory))
K3	(monos or mnos or sonos or (twin and flash) or nrom or (trap and memory) or (nor and memory) or (nand and memory))
K4	((smart and card) or eeprom or eprom or etox or nvram or non-volatile or nonvolatile or (volatile and non) or (flash and memory))
K5	(chalcogenide or mram or m-ram or (magnetic and memory) or feram or fe-ram or (ferroelectric and memory))

Table 15: List of sample key words

Based on random checking of about 500 patents, the probability that non-flash patents are included in this group is less than 1%. Furthermore, about 24 extraneous patents were deleted manually from this key-word based list.

Step 2) Class pair matching

In the next step, we conducted a patent class-pair analysis. When a patent application is filed with the US Patent and Trademark Office, its claims are reviewed and the application is assigned to one of approximately 450 Main Classes and 150,000 Sub-Classes in the United States Patent

Classification System. This Patent Classification System has many uses, but its primary administrative purpose is to assist USPTO Patent Examiners in their review of patent applications, so that a pharmaceutical patent will be reviewed by an expert in that field instead of by an Examiner trained in mechanical engineering. The Patent Classification System is not perfect, but it does tend to aggregate related patents by technical area and thus provides another insight into the patent universe.

In our class pair analysis we took the patents obtained with the Key Words list in Table 15 and sorted them by the class-pairs assigned to them by the US PTO. This resulted in a list of over 1200 different class-pairs. For each class pair, we reviewed the patents assigned to that class-pair and as appropriate, we read the class-pair definition from the Manual of Patent Classification to determine if that class pair is unique for flash memory. We found that often times a class pair can include other types of memory technologies or circuits. If more than 95% of the patents in that class pair were flash patents, then we considered that class pair to be UNIQUE to flash (Class A). If more than 85% of the patents were flash patents, then that class pair was categorized as MOST (Class B). Many class pairs contain less than 10% flash patents (Class C).

After going through each of the twelve hundred classes, we found about sixty-two classes that could be classified as either UNIQUE or MOST. Combining the UNIQUE and MOST lists with the KEYWORDS list, we identified a total of 16824 patents. An image of the relationships between the collected patents is given in Figure 20.

Table 16 shows the partial results of our categorization. More details about the search procedure and the class pair categorization are given in Appendix B2.

Figure 20 gives a break down of the patent search results. The dotted line represents the total

number of flash patents that exist in the US PTO. The gray shaded area depicts the number of patents that have been collected. Ideally the number of patents collected will be equivalent to the total number of flash patents. The weakness of this collection procedure is that some patents will be collected that do not relate to flash memory, and others will be missing. However, the number of patents collected should be sufficient for trend analysis, and we would prefer to have extra un-related patents rather than leave out a potentially important flash-related patent.

Class A Unique to Flash (>95%)	**Class B** Mostly Flash (>85%)	**Class C** Low Flash (<10%)
257/314 257/315... 257/317 257/319 257/320-324 256/326	257/316 257/318 257/325 257/411	235/487 235/492 257/298 257/350 257/410 257/506 257/679
		327/96 327/111 327/390 327/536 348/247 358/471 361/749
365/145 365/185.01-185.03 365/185.5-185.11 365/185.14-185.16 365/185.18-185.19 365/185.25...	365/185.09 365/185.12 365/185.17 365/185.2...	365/182 365/184 365/185.04 365/185.05...

Table 16: Class-pairs Categorization (partial list)

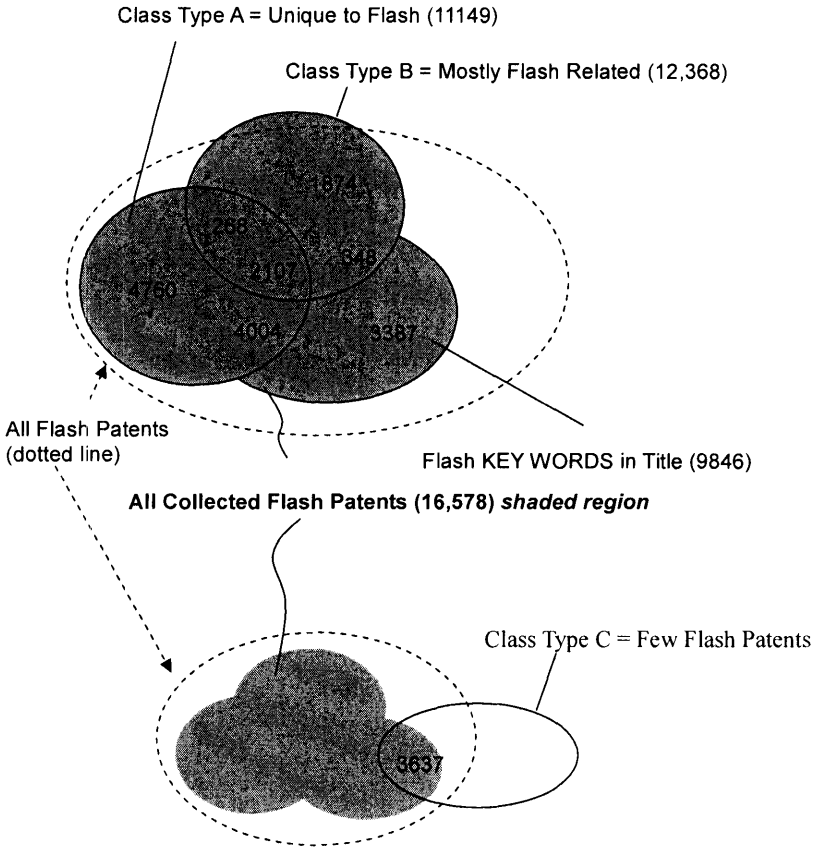

Figure 20: Results of Search for All Flash Patents

Step 3) Inventor or Assignee Focus

We can further refine the search for flash-related patents based on a specific assignee or inventor. For example, we are aware that some companies such as SanDisk, Saifun, Halo LSI and Matrix are only involved in flash memory. Therefore, we can gather all the patents associated with these companies without further scrutiny.

When we did so, we found that several new patents. The percentage of patents that were already

found by the previous key word or class-pair searches is shown below in Table 17.

Company	Percentage of patents already found/Patents found by Assignee Search only
Matrix Semiconductor	27%
SanDisk	80%
Saifun	80%
Halo LSI	80%

Table 17: Assignee Search Results

This step also provides a measure of how complete this search method is. According to this spot-check, we can estimate that the number of patents collected is less than 80% of the total number of possible flash memory-related patents.

Also, certain specialists spend a lifetime in a field, inventing new types of memory devices or methods. The new inventions might not show up in a normal flash key word search or assignee analysis. However, if the inventor name is constant, we may be able to find them.

Step 4) Un-issued Patent Applications

In addition to the issued patents, the USPTO also maintains a database of recent patent applications. Patent applications are publicly available eighteen months after the application is filed. In order to find the flash-related patent applications, we performed Steps 1-3 on the database of Patent Applications. By this method, we found another 5286 relevant patent applications.

It should be noted that since these are un-issued patent applications, there is a possibility that these applications will not make it past the prosecution process. However, for our purposes to study activities in the flash memory industry, it is useful to include these un-issued patent applications.

Summary

In summary, we collected a total number of 24285 patents and applications.

All told, we found a total 19103 patents resulting from Steps 1-3, and 5286 patent applications in Step 4.

KeyWord Search	11,823
Class-pair	14,851
Flash specific companies	531
Un-issued Applications	5,286

5.3.2. General Trends

We choose to work with patents based on the date on which they were filed, rather then when they were issued, because the filing date is closer to the invention date. Furthermore, patents usually can take from one to four years to from application to issue, depending on the complexity of the patent prosecution process. By working with patents based on the filing date we can ignore this variability.

The number of flash patents that were filed each year is graphed in Figure 21. As we might have expected, the increase in the number of issued patents corresponds closely with the revenue of flash memory. Technology development and market development as well as defensive legal mechanisms are all factors that contribute to the increasing number of patents filed per year.

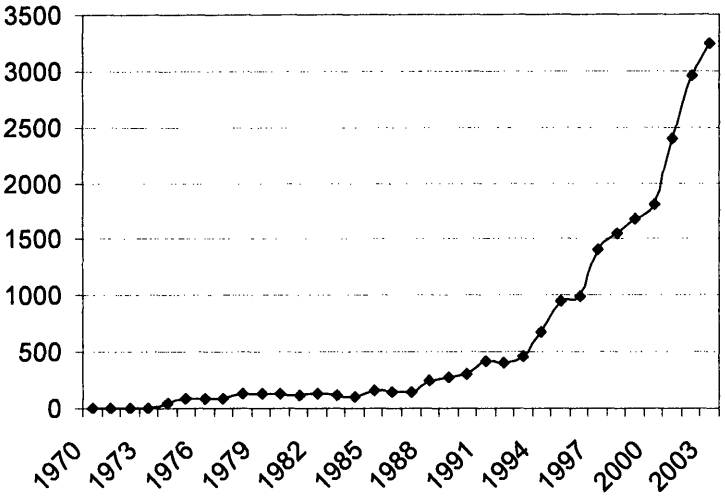

Figure 21: Flash Patents vs. Years

Assignee Analysis

Figure 22 shows the top ten companies holding the largest flash patent portfolios. Not surprisingly, these names roughly correspond with the largest flash producers in the industry.

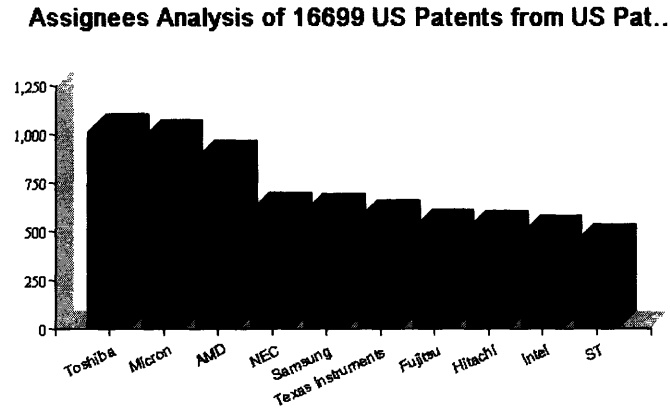

Figure 22: Top 10 Flash Patent Holders

	Assignees	Total US Patents ▷ statistics
1.	Toshiba • Toshiba Corporation (1) • Toshiba (1013) • Toshiba Micro-Electronics Corporation (1)	1014
2.	Micron • Micron Technology (1) • Micron Technology, Inc. (1) • Micron Telecommunications, Inc. (1) • Micron Communications, Inc. (1) • Micron Technologies, Inc (1) • Micron (913) • Micron Quantum Devices, Inc.... more	986
3.	AMD • Advance Micro Devices, Inc. (3) • AMD (872) • Advanced Micro Devices, In. (1) • Advanced Mirco Devices (1) • Advaned Micro Devices, Inc. (1) • Advanced Micro Devices, Ltd. (1) • Adanced Micro Devices, Inc.... more	880
4.	NEC • NEC Electronics Corporation (57) • NEC Research Institute, Inc. (6) • NEC Electroincs Corporation (1) • NEC (546) • NEC Electronics Inc. (2)	610
5.	Samsung • Samsung SDI Co., Ltd. (1) • Samsung (567) • Samusung Electronics Co., Ltd. (1) • Samsung Electronics Co., LTE (1) • Samsung Electro-Mechanics Co., LTD (1) • Samsung Eletronics Co., Ltd. (2) • Samsung... more	600
6.	Texas Instruments • Texas Instrumens Incorporated (1) • Texas Instruments Deutschland GmbH (1) • Texas Instrument Incorporated (5) • Texas Instruments, Incorporated (7) • Texas Instruments, Inc. (13) • Texas Instruments... more	573
7.	Fujitsu • Fujitsu (506) • Fujitsu Ltd. (10) • Fujitsu Fanuc Limited (3) • Fujitisu Limited (1) • Fujitsu VLSI Limited (14)	520
8.	Hitachi • Hitachi Tohbu Semi-conductor, Ltd. (1) • Hitachi ULSI Engineering Co., Ltd. (4) • Hitachi Keiyo Engineering Co., Ltd. (6) • Hitachi Microcomputer System Ltd. (1) • Hitachi ULSI Engineering Corporation... more	515
9.	Intel • Intle Corporation (1) • Intel Corpration (1) • Intel (488)	490
10.	ST • STMicroelectronics Ltd. (2) • STMicroelectronics, S.A. (21) • STMicroelectronics, Inc. (39) • STMicrolelectronics, Inc. (1) • STMicroeletronics S.R.L. (3) • STMicroelectronics (367) • STMicroelectronics... more	446

Figure 23: Assignee Name Groupings

Inconsistency of the assignee's names can add to the complexity of analysis. In Figure 23, we can see how the names for the top ten flash patent holders were grouped. A single assignee may be represented with multiple names and spellings, as well as mis-spellings. For example, there are more than seven different variations and mis-spellings for AMD; "Advanced Micro Devices", "Advance Micro Devices", "AMD", "Advanced Mirco Devices", "Advaned Micro Devices, Inc.", "Advanced Micro Devices, Ltd.", "Adanced Micro Devices, Inc." We used a feature in IP-Vision that allows aliasing of names in order to group patents into one main assignee group:

```
AMD (|Advance Micro Devices*|Adanced Micro Devices*|Advanced Micro
Devices*|Advanced Mirco Devices|Advaned Micro Devices*|AMD|);
```

A complete description and total list of the aliased names is provided in Appendix B4.

.

Another reason that the number of filed patents is increasing with every year is that the number of companies entering into the market is also increasing. In Figure 24, the bold line represents the total number of companies filing flash patents per year. The dotted line shows the number of companies that have filed two or less flash-related patents per year.

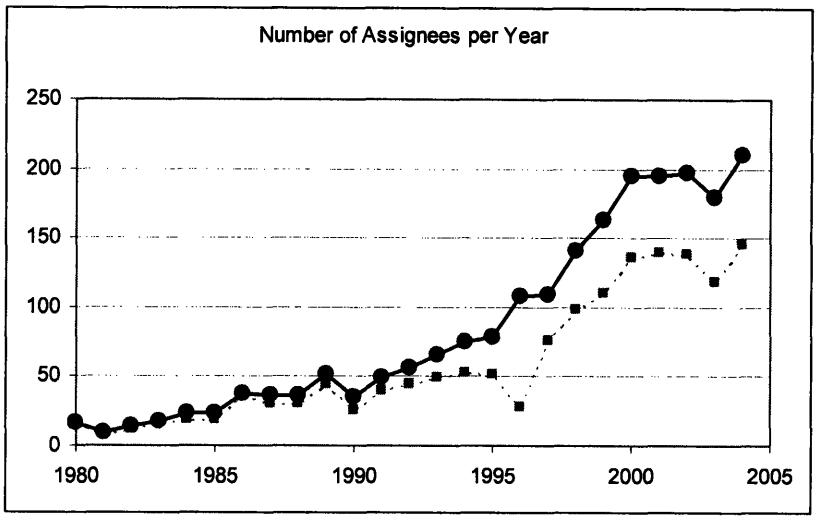

Figure 24: Number of Companies Filing Flash Patents Per Year

We can see that before 1990, patent activity in the flash memory area was sporadic for all the companies. Later, between 1990-1995, we start to see an increase in the number of patents being filed and the emergence of serious flash players. After 1995, the number of companies filing two or more patents (equivalent to the subtraction of the dotted line from the blue line) appears to settle to a steady number of roughly 50. However, the number of companies filing two or less patents increases significantly between 1996 to 2005. We propose that as the flash market grew, it may have attracted many new entrants and stimulated alternative solutions and inventions.

5.4. Mapping Class-Pairs to the Flash IP Value Chain

Within the class-pairs list, four main classes were identified: 257, 365, 438, and 711. The sub-definitions for the secondary class-pairs and their categorizations are given in Table 18.

Class Number	Description	Memory Technology	Product Technology
257/314-326	Active solid state devices (e.g. transistors, solid-state diodes)	Cell/Device	
257/411	Active solid state devices (e.g. transistors, solid-state diodes) – compsite or layered gate insulator (e.g., mixture such as silicon oxynitride)	Cell/Device	
365/145	Static information storage and retrieval – ferroelectric	Circuits	
365/185.01	Static information storage and retrieval – floating gate	Circuits	
365/185.02-185.033	Static information storage and retrieval – [various]	Circuits	
438/201	Semiconductor device manufacturing: process – including insulated gate field effect transistor having gate surrounded by dielectric (i.e., floating gate)	Process	
438/216	Semiconductor device manufacturing: process – gate insulator structure constructed of diverse dielectrics (e.g., mnos, etc.) or of nonsilicon compound	Process	
438/257	Semiconductor device manufacturing process – having additional gate electrode surrounded by dielectric (i.e., floating gate)	Process	
438/263	Semiconductor device manufacturing: process – tunneling insulator	Process	
438/266	Semiconductor device manufacuturing process – having additional nonmemory control electrode or channel o=portion (e.g., for accessing field effect transistor structure, etc.)	Process	
438/287	Semiconductor device manufacturing: process - gate	Process	
709/224	Electrical computers and digital processing systems: multiple computer or process coordinating		System
711/103	Electrical computers and digital processing systems: memory – programmable read only memory (prom, eeprom, etc.)		System
714/8	Error detection/correction and fault detection/recovery		System
717/168	Data processing: software development, installation and management		System

Table 18: Class Pairs vs. IP Value Chain Position

When comparing between two different patent portfolios, it is important to understand where each portfolio rests along the flash memory IP value chain. Otherwise, the true network

externalities can not be comprehended. Thus, it is helpful to map the class-pair category to its corresponding position along the Flash IP value chain. In

Figure 25, we show the IP value chain once more, with the class-pairs mapped to their corresponding positions along the chain. Note that class 257 and 438 deal with memory structure and process recipes and techniques. Class 365 is related more to the implementation of circuits or organizations around the memory cells. Class 711 deals with the system level implementations. We believe that there are many other classes that can be included into the product technology

category, however they are widely scattered, and are therefore more difficult to find.

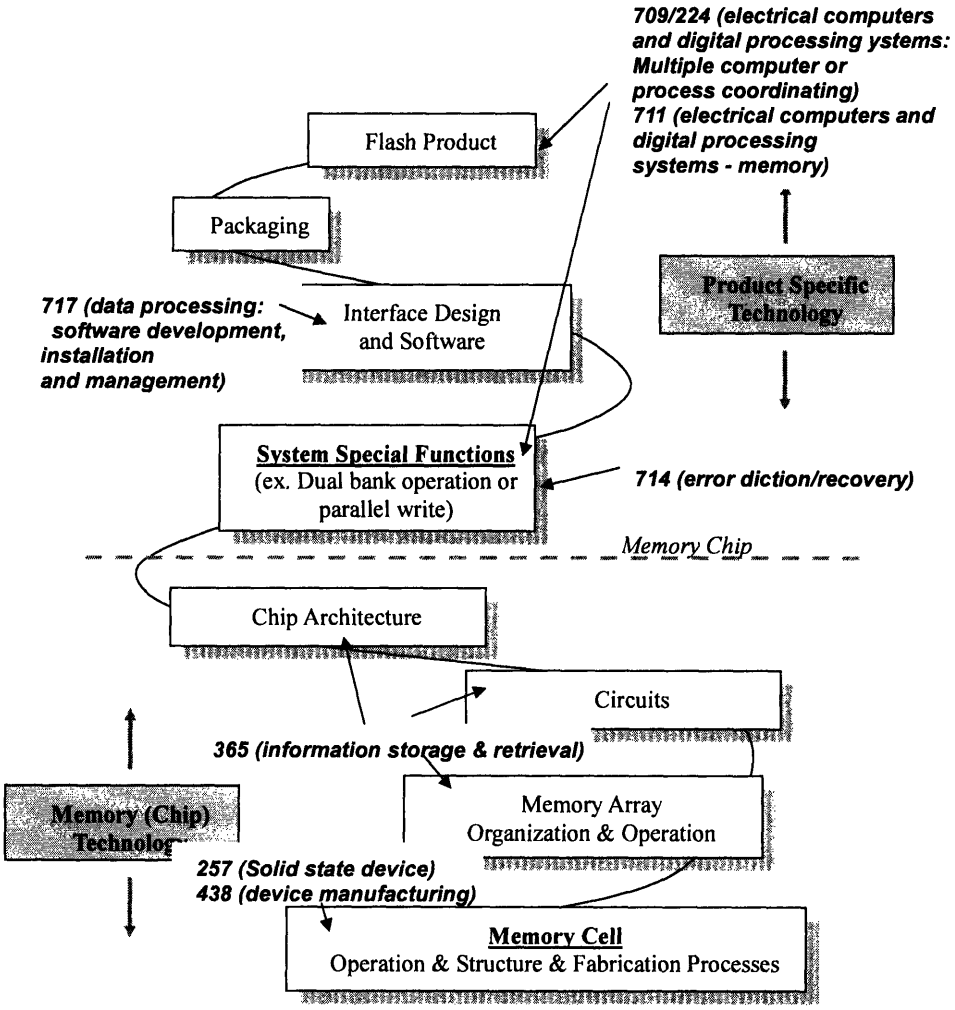

Figure 25: IP Value chain with corresponding Class-pairs

As we can see in Figure 25, some patent classes, such as 365, cover more than one stage along the IP value chain. For our next discussion, we would like to group the different classes into 4 main

categories:

(i) Device: This represents innovation at the most fundamental levels. Memory cell structure and operations and arrangements are the most basic building blocks.

(ii) Process: Manufacturing recipes. Although this is still considered low-level technology development, there are additional degrees of freedom in this category, compared to Device. There are multiple ways to make a single memory structure.

(iii) Circuits: This category encompasses the memory array architectures and circuits that may be used to make a memory chip. There may be some overlap with system-level patents in the Product category.

(iv) Product: This category includes many classes, from system-level arrangements and usage, to special functions like wear-leveling or parallel chip operation, etc.

Based on the four categories of patents, we sampled the patents of twelve flash companies in order to compare the composition of their portfolios. The results are given in Table 19. The first column gives the total patents that were included in the calculation. The second column, "Number of Product Classes", shows the number of class-pairs that fall into the category of product technology, according to the definition given in Figure 25. In the case of Intel, the number 10 means that there are at least 10 different primary US classes that were grouped together. The following 4 columns show the ratio of that category over the total number of patents. For Intel, 34% of its patents can be classified as "Product"-related, 7% are Device innovations, 12% are Process innovations, and the remaining 47% of its patents fall into the Circuits area.

Companies	Total Patents For this data	Number of Product classes	Products Many Classes	Device 257	Process 438	Circuits 365,327,360
Intel	560	10	34%	7%	12%	47%
Toshiba	1159	6	4%	21%	10%	66%
Samsung	645	4	4%	23%	27%	46%
Sandisk	219	4	16%	6%	8%	70%
Lexar	53	3	70%	0%	0%	30%
Renesas/Hitachi	258	2	5%	16%	10%	69%
Saifun	45	1	4%	18%	13%	64%
Halo	60	0	0%	22%	32%	47%
Macronix	327	3	3%	15%	40%	42%
Infineon	264	2	2%	20%	30%	48%
SST	98	2	6%	27%	14%	53%
Micron	1103	8	7%	21%	27%	44%

Table 19: Patent mix ratios between Device, Process, Circuit and Products Technology

Continuing to refer to Table 19, we can draw several inferences about the companies involved, based on their patent mix. Most of the companies have patents in each of the four categories, with the extreme exception of Lexar, which has no Device or Process patents, and Halo, which has no Product patents. Therefore we may infer that Lexar's core business is related to product technology that is relatively high up on the IP value chain, and Halo's business focus is on technology at the chip manufacturing and memory device level.

5.5. Analysis of Major Companies

Because Intel and Toshiba are the original inventors of NOR and NAND technologies, we would like to start by studying the patent portfolios of these two companies. Furthermore, in the past three years, both the leadership that both companies has enjoyed is under threat by increasing competition. There are also indications that the NOR market is saturating, and that NAND faces technology scaling challenges. It would be very interesting to understand what future strategies are being considered by these leading companies.

5.5.1. Intel

Patent Characteristics

We found over 500 flash patents assigned to Intel. The graph in Figure 26 shows the steady increase of patents being filed between 1974 and 2004. It should be noted that the observed decrease between 2002 and 2004 is most likely due to insufficient data, since patent applications are not publicly available until eighteen months after they have been filed.

In 1998, we see a sharp dip in the number of patents being filed. This could be due to the economic downturn experienced during that year.

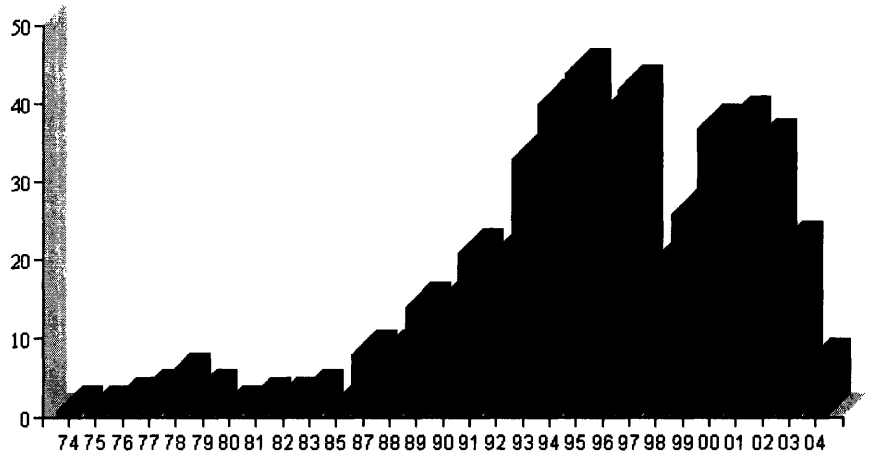

Figure 26: Intel's patent applications vs. time

The ratio of flash patents to total patents in Intel's portfolio is only 5%, as shown in Figure 27 Interestingly, revenue from flash also represents about 5% of Intel's total income.

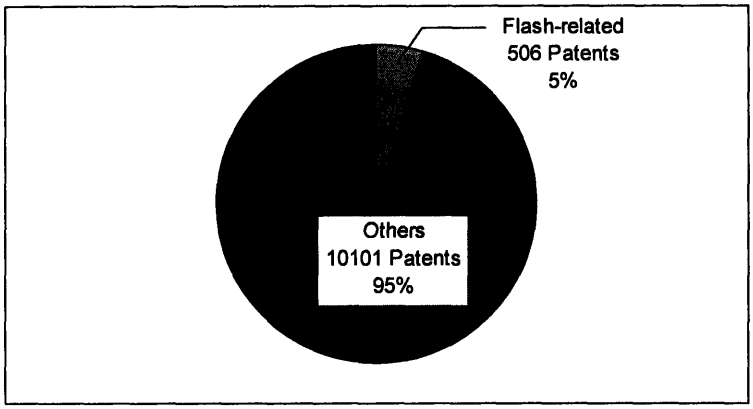

Figure 27: Intel's flash-related patents vs. total number of patents

Inventor Analysis

Performing inventor analysis resulted in over 500 inventor names. Table 20 shows the top performing flash inventors at Intel and the years in which their patents were filed.

Inventors	Total US Patents	Role	Beginning year	End Year
Atwood, Gregory E.	27	Circuit Designer	1989	1997
Hasbun, Robert N.	26	Circuit Designer	1992	2000
Fazio, Albert	25	Circuit Designer	1989	2002
Fandrich, Mickey L.	23	Circuit Designer	1991	1997
Tedrow, Kerry D.	21	Circuit Designer	1991	2002
Rozman, Rodney R.	20	Circuit/System Designer	1989	1996
Robinson, Kurt B.	19	Circuit Designer	1991	1999

Table 20: Most prolific flash inventors at Intel

We speculate that some of these inventors who have not written an invention in the past five years have either (i) since left the company, or (ii) been promoted so that they are no longer involved in direct engineering. Also, interestingly, the most prolific patent writers are all circuit designers. This confirms our understanding that Intel's core technology is related more to circuit innovations, rather than at the memory cell level.

Insight into the Future

We attempt to anticipate Intel's future strategy by looking at the titles of some of the most recently filed patents, listed in Table 21.

Patent Number	Application Date	Inventors	Title
6522568	7/24/2001	Nair, Rajendran	Ferroelectric memory and method for reading the same
6529398	9/27/2001	Nair, Rajendran;Chow, David G.	Ferroelectric memory and method for reading the same
6617209	2/22/2002	Chau, Robert;Arghavani, Reza;Doczy, Mark	Method for making a semiconductor device having a high-k gate dielectric
6646903	12/3/2001	Chow, David GenLong	Ferroelectric memory input/output apparatus
6646904	12/21/2001	Chow, David GenLong	Ferroelectric memory and method of reading the same
6836816	3/28/2001	Kendall, Terry L.	Flash memory low-latency cache
6853571	8/20/2002	Doller, Edward M.	Stacked non-volatile memory device and method of making the same
6876567	12/21/2001	Chow, David GenLong	Ferroelectric memory device and method of reading a ferroelectric memory
6941423	12/22/2003	Coulson, Richard L.	Non-volatile mass storage cache coherency apparatus
6951764	7/20/2004	Andideh, Ebrahim	Ferroelectric memory device with a conductive polymer layer and a method of formation

Table 21: Ten Most Recent Patents by Intel

There are two interesting trends to note, and both of them relate to high-speed embedded flash. We see two patents that connect flash to cache applications. The other trend is a steady number of ferroelectric patents. FeRAM is an alternative solution to floating gate memory for embedded applications. It could be a goal within Intel to use FeRAM for the next generation of microprocessor chips.

Discussion

Intel's rise to NOR flash leadership was primarily due to first mover advantage in which it could establish the standard and then control the licensing the technology associated with the circuit

functions and interfaces. The company was one of the first to offer low density, high random access memories, timed to meet the emerging cell phone market boom. However, the memory cell that the products were based on is over thirty years old. While there have been significant efforts to scale the technology further, the overall mentality of the company seems to have been "if it ain't broke, don't fix it."

This philosophy is reflected in the patent ratio mix. Going back to Table 19, we can see that 34% of its patents are Product, 47% are circuits, and only 7% are Device and 12% are Process-related. Thus, the patent ratio correlates with the theory that Intel's success comes largely from implementation and productization of a conventional base memory cell technology. Thus, it was not too surprising when we scanned through Intel's patents and applications and could not find any other new device structures for nitride or anything else.

Considering the nature of Intel's technology competency, as well as the slow down in the NOR market, it may be advisable for Intel to enter the other faster growing markets. It would seem to be in Intel's strategic interest to leverage its position to find a partner with basic memory cell technology that could also take advantage of Intel's significant portfolio of Circuit and Product patents. In this regard, as recently as December 2005, there was a joint venture announcement between Intel and Micron, to start next generation NAND development.

5.5.2. Toshiba

Patent Characteristics

In Toshiba, 1169 out of its total 23171 patents are related to flash. The ratio of flash patents to total patents of 5% is very similar to that of Intel. However, we should pause to note that Toshiba is a Japanese company and there is a possibility that not all of its patents are being filed in the United States.

Inventor Analysis

The results of an analysis of the top ten most prolific inventors are given in Table 22. As we saw with Intel, we see that most of these inventors are circuit designers.

Inventors	Total US Patents	Role	Beginning year	End Year
Tanaka, Tomoharu	137	Device Engineer	Mar 1990	June 2004
Atsumi, Shigeru	85	Device Engineer	May 1984	July 2004
Nakamura, Hiroshi	85	Circuit Designer	Sep 1992	Jan 2005
Shirota, Riichiro	83	Device/Process	Nov 1988	Nov 2004
Iwata, Yoshihisa	71	Flash until 2001 Magnetic Memory Dev.	Nov 1998	Sep 2004
Iwahashi, Hiroshi	69	Circuit Designer	Dec 1985	Apr 2003
Aritome, Seiichi	68	Circuit Designer	Feb 1990	Mar 2004
Tanzawa, Toru	67	Circuit Designer	Jun 1994	Jul 2004
Imamiya, Kenichi	52	Circuit Designer	Sep 1993	Jan 2005
Takeuichi, Ken	52	Circuit Designer	Jun 1995	Aug 2004

Table 22: Ten Most Prolific Flash Memory Inventors in Toshiba (over all time)

All of the inventors in the Table 22 have had a very long history at Toshiba, and must have contributed a great deal to the company's success. But from this information, it is not clear if the listed individuals are still active in Toshiba's most recent projects. In order to identify the most current active inventors, we narrowed the field of patents to the past three years, between Jan 01, 2003 to present. The resulting number of patents and applications is 369. The top ten list of inventors for this more recent group of patents applications is given in Table 23.

Name	Number of Patents	Listed in the Overall Top 10?
Kishi, Tatsuya	18	
Tanaka, Tomoharu	18	Yes
Amano, Minoru	17	
Hosano, Koji	17	
Imamiya, Kenichi	17	Yes
Iwata, Yoshihisa	17	Yes
Ueda, Tomomasa	16	
Nakamura, Hiroshi	15	
Saito, Yoshiaki	14	

Table 23: Ten Most Prolific Flash Inventors in Toshiba (Jan 1, 2003 to Present)

As we can see, only three individuals are common to both lists, Yoshihisa Iwata, Kenichi Imamiya and Tomoharu Tanaka.

Insight into the Future

According to the ten most recent patent application titles in Table 24, like Intel, most of Toshiba's flash patents seem to be aimed at improvements to its core product. Magnetic memory development also appears to be on-going.

Publication Number	Application Date	Inventors	Title
usApplication: 20050185347	4/21/2005	Inomata, Koichiro (Yokohama-shi, JP);Nakajima, Kentaro (Yokohama-shi, JP);Saito, Yoshiaki (Yokohama-shi, JP);Sagoi, Masayuki (Yokohama-shi, JP);Kishi, Tatsuya (Yokohama-shi, JP)	Magnetoresistive element and magnetic memory device
usApplication: 20050185468	4/28/2005	Hosono, Koji (Yokohama-shi, JP);Imamiya, Kenichi (Tokyo, JP);Nakamura, Hiroshi (Fujisawa-shi, JP);Nakabayashi, Mikito (Chigasaki-shi, JP);Kawai, Koichi (Yokohama-shi, JP)	Non-volatile semiconductor memory device
usApplication: 20050216723	5/19/2005	Imamiya, Kenichi (Tokyo, JP)	Non-volatile semiconductor memory device
usApplication: 20050219909	5/27/2005	Futatsuyama, Takuya (Yokohama-shi, JP);Imamiya, Kenichi (Tokyo, JP);Hosono, Koji (Yokohama-shi, JP);Shibata, Noboru (Kawasaki-shi, JP)	Non-volatile semiconductor memory device, method for sub-block erase and electric device with the same
usApplication: 20050224898	6/3/2005	Momose, Hisayo (Tokyo, JP);Iwai, Hiroshi (Kawasaki-shi, JP);Saito, Masanobu (Chiba-shi, JP);Ohguro,	MOSFET with a thin gate insulating film

		Tatsuya (Yokohama-shi, JP);Ono, Mizuki (Yokohama-shi, JP);Yoshitomi, Takashi (Kamakura-shi, JP);Nakamura, Shinichi (Yokohama-shi, JP)	
usApplication: 20050232015	6/17/2005	Mori, Seiichi (Tokyo-To, JP)	Non-volatile semiconductor memory and manufacturing method thereof
usApplication: 20050237829	4/13/2005	Nakamura, Hiroshi (Fujisawa-shi, JP);Tanaka, Tomoharu (Yokohama-shi, JP)	Non-volatile semiconductor memory device
usApplication: 20050243620	6/24/2005	Imamiya, Kenichi (Tokyo, JP);Kawai, Koichi (Yokohama-shi, JP)	Non-volatile semiconductor memory device
usApplication: 20050254289	7/1/2005	Nakajima, Kentaro (Tokyo, JP);Amano, Minoru (Kawasaki-shi, JP);Ueda, Tomomasa (Yokohama-shi, JP);Takahashi, Shigeki (Yokohama-shi, JP)	Magnetic memory device and method of manufacturing the same
usApplication: 20050254298	7/19/2005	Umezawa, Akira (Tokyo, JP)	Channel erase type nonvolatile semiconductor memory device and electronic card and electronic apparatus using the device

Table 24: Toshiba's Ten Most Recent Patent Applications/Publications

Related to nitride, we were able to find one nitride patent based on a keyword title search of "ONO". The patent number is 6118699, titled, "Semiconductor memory device, using MONOS type nonvolatile memory cell." The application date is Sept 12, 2000. We checked to see if any other patents within Toshiba referenced this patent and found several. The landscape map in Figure 28 shows that there are five more patents that are derived from this patent. Note that we would not have been able to identify these patents by the normal 1-2-3-4 step process given in Section 5.3, as they did not have any of the keywords in their titles..

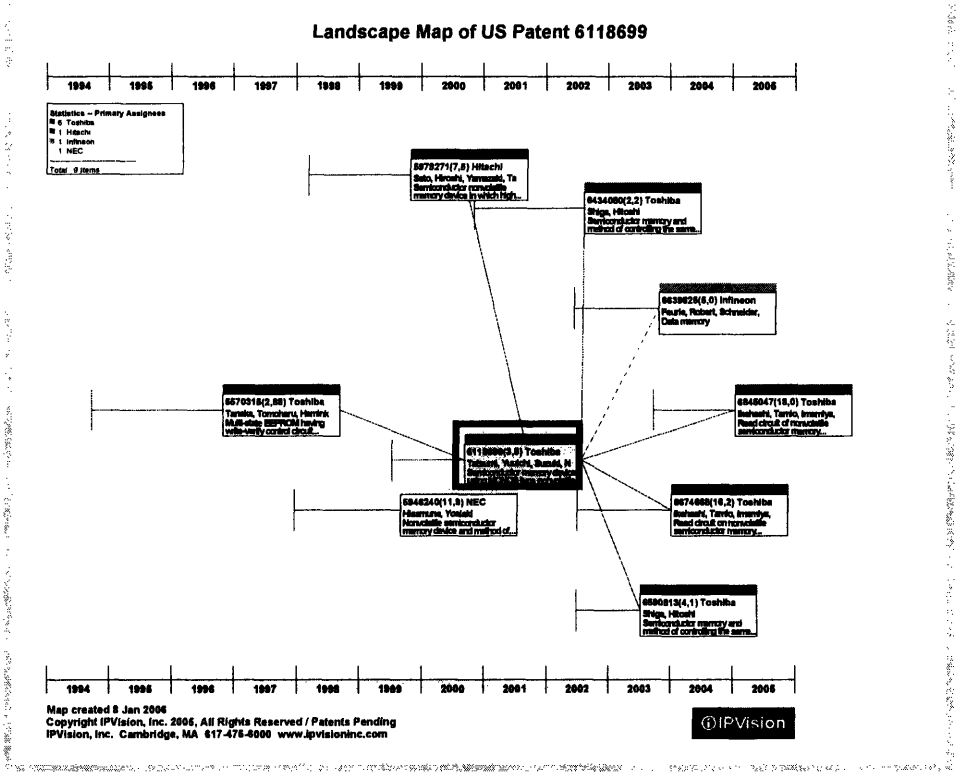

Figure 28: Landscape map for Toshiba's MONOS patent 6118699

5.5.3. SanDisk

SanDisk is a successful licensing and product company. Early in its company history, it made a bet on the then emerging NAND technology, and partnered with Toshiba. The two companies agreed to co-develop NAND chip designs and Toshiba guaranteed a supply of chips to SanDisk in order for SanDisk to sell them under its own brand name. SanDisk developed its own application specific cards, it invented the PC flash memory card in 1993 and the CompactFlash card in 1994. These cards are widely used in laptops and digital cameras. It has also partnered with the SD consortium as well as SD's rival, Sony MemoryStick.

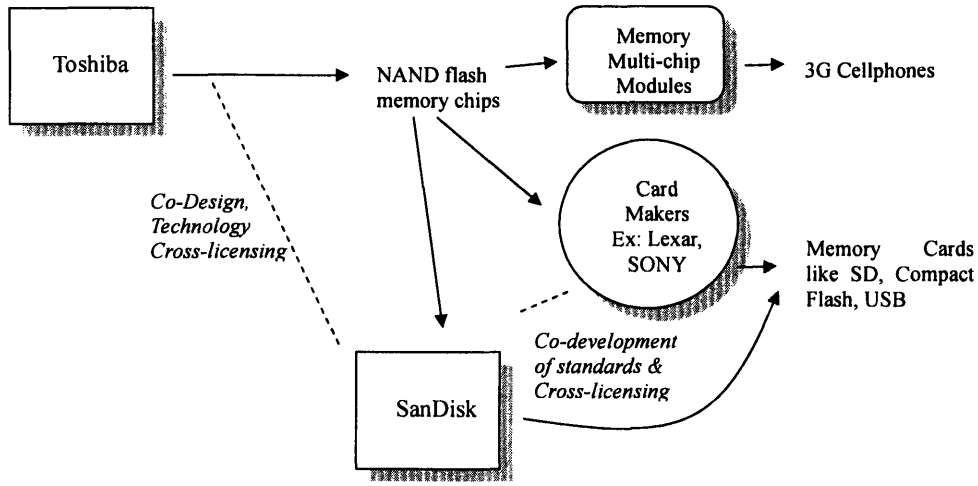

Figure 29: SanDisk's relationships

From Figure 29 above, it can be seen that SanDisk, as an early adopter of the memory card standards, enjoys a rather unique position as both a licensor and competitor to the other memory card companies. The company innovates to establish new standards for emerging applications. This year, SanDisk introduced both a new memory stick with SONY, and a new encryption USB device for PC's. Its 263 patents cover a wide range of categories. Figure 30 gives a bar graph of SanDisk's patents according their primary class category, and Table 25 below explains the class definitions. As we can see from the class numbers, SanDisk's patents spread across the entire IP value chain, because at one point or another it was engaged in activities at all the stages, from memory cell development, to circuit design and product design. Figure 31 shows a patent citation interconnection map of SanDisk's patents. Each square in the map represents a single patent, and the interconnections between the squares shows the citation relationships. Patent clusters can suggest the areas in which the company is focusing its development efforts. We expect to see a

correlation between the patents that are the most interconnected, and the relevance of that patent to the project or company.

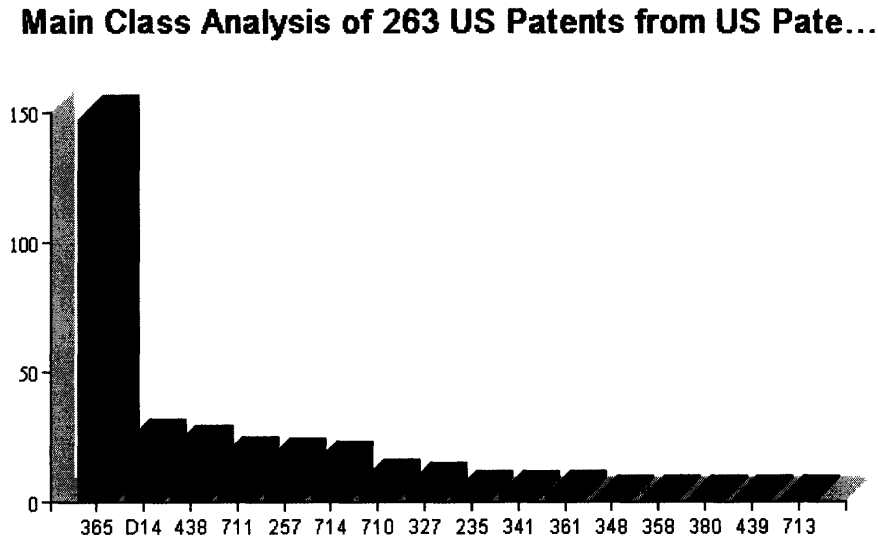

Figure 30: SanDisks's Patent Portfolio Primary Class Analysis

Main Class Analysis of 263 US Patents from US Patent Data		
Class No:	Title	No of Patents
365	Static information storage and retrieval	148
D14	Recording, communication, or information retrieval equipment	23
438	Semiconductor device manufacturing: process	20
711	Electrical computers and digital processing systems: memory	16
257	Active solid-state devices (e.g.,transistors, solid-state diodes)	15
714	Error detection/correction and fault detection/recovery	14
710	Electrical computers and digital data processing systems: input/output	7
327	Miscellaneous active electrical nonlinear devices, circuits, and systems	6
235	Registers	3
341	Coded data generation or conversion	3
361	Electricity: electrical systems and devices	3
348	Television	1
358	Facsimile and static presentation processing	1
380	Cryptography	1
439	Electrical connectors	1
713	Electrical computers and digital processing systems: support	1

Table 25: Class Definitions of SanDisk's Patents

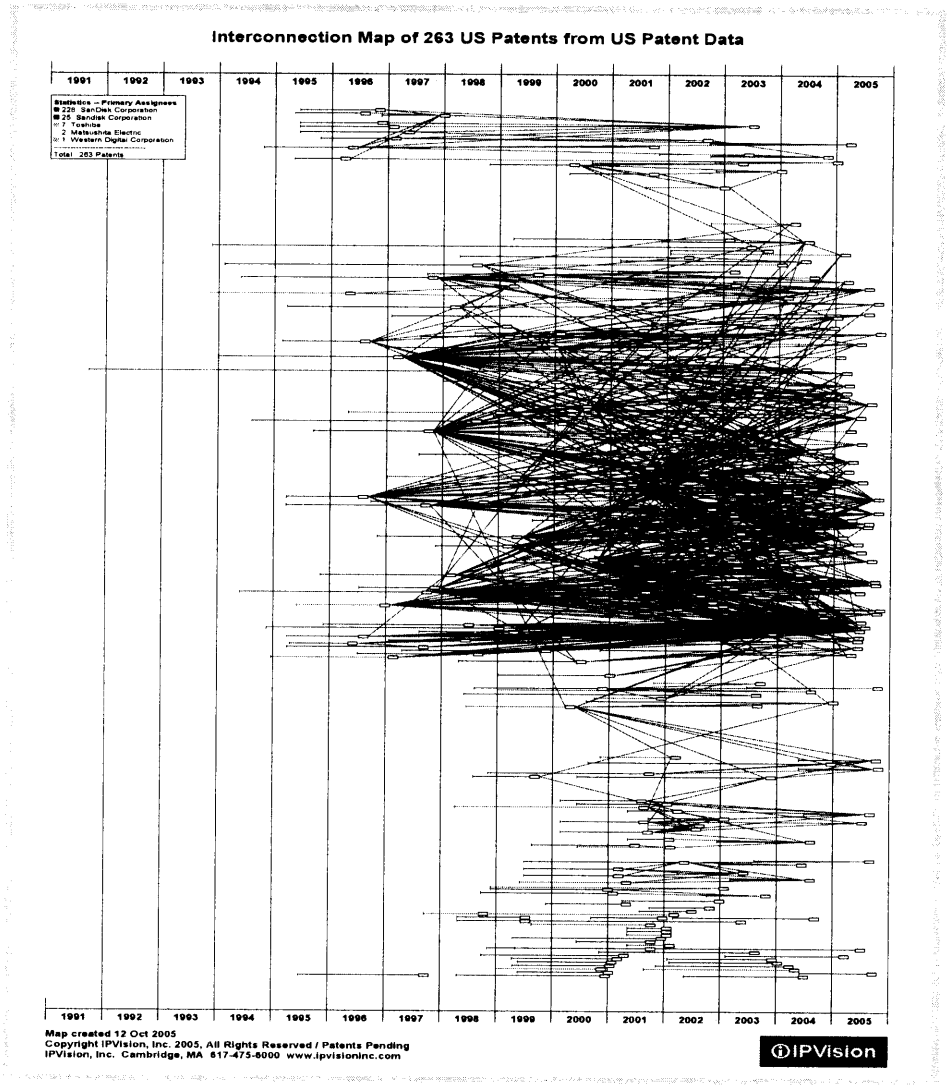

Figure 31: Interconnection map of SanDisk's patents

Moreover, if a patent is referenced by many other companies in the industry, we might expect that this patent has an industry-wide significance. In the case of SanDisk, we found a moderate correlation between its patents that were the subject to litigation, and the number of times that those

patents were referenced by other patents. We sorted SanDisk's patents according to the number of forward references, and listed the top 10% in **Table 26**. When we compared the five patents (in **Table 27**) which were named in infringement lawsuits against that list, we found four of the five patents matches.[59] Interestingly, the only unmatching patent, 5991517, was the subject of a lawsuit by SanDisk against ST Microelectronics, in which ST Microelectronics first won a judgment of non-infringement, but the lawsuit was reinstated upon appeal. The final outcome is still pending.

Patent Number	Title	Number of FC (Referenced By)
5172338	Multi-state EEprom read and write circuits and techniques	429
5602987	Flash EEprom system	149
5663901	Computer memory cards using flash EEPROM integrated circuit chips and memory-controller systems	146
5535328	Non-volatile memory system card with flash erasable sectors of EEprom cells including a mechanism for substituting defective cells	105
6103573	Processing techniques for making a dual floating gate EEPROM cell array	85
5887145	Removable mother/daughter peripheral card	79
5508971	Programmable power generation circuit for flash EEPROM memory systems	69
5583812	Flash EEPROM system cell array with more than two storage states per memory cell	67
6222762	Multi-state memory	64
5495442	Method and circuit for simultaneously programming and verifying the programming of selected EEPROM cells	59
5661053	Method of making dense flash EEPROM cell array and peripheral supporting circuits formed in deposited field oxide with the use of spacers	54
5671229	Flash eeprom system with defect handling	54
5532962	Soft errors handling in EEPROM devices	52
6151248	Dual floating gate EEPROM cell array with steering gates shared by adjacent cells	52
5563825	Programmable power generation circuit for flash eeprom memory systems	50
5592420	Programmable power generation circuit for flash EEPROM memory systems	50
5719808	Flash EEPROM system	50

Table 26: Top 10% of SanDisk's most cited patents

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[59] Staff writer, "SanDisk Appeals ITC Ruling, Heads to Court – Again", Electronic News, December 6, 2005, Obtained January 10, 2005,<http://www.reed-electronics.com/electronicnews/article/CA6289428>.

Patent Number	Application Date	Primary US Class	Title	Number of FC (Referenced By)
5172338	4/11/1990	365/185.03	Multi-state EEprom read and write circuits and techniques	429
5602987	12/29/1993	714/8	Flash EEprom system	149
5583812	2/16/1995	365/185.33	Flash EEPROM system cell array with more than two storage states per memory cell	67
5719808	3/21/1995	365/185.33	Flash EEPROM system	50
5991517	12/20/1996	714/3	Flash EEprom system with cell by cell programming verification	17

Table 27: SanDisk's patents that were named in infringement litigation

5.6. Key patents from lawsuits

Based on the previous analysis of Saifun's patents, we would like to make a generalization about patents and litigation in the flash memory industry. There seems to be a correlation between the number of times that a patent is cited and 1) the likelihood that this patent will be the subject of an offensive lawsuit, and 2) the likelihood of a favorable judgment.

To check this theory, we looked at a few of the other lawsuits, narrowing the criteria to patents that were named in offensive lawsuits, rather than defensive. This is because offensive lawsuits are based on the confidence that companies have in their patents. Patents named in defense are not expected to be as strong – if the defensive patents are strong, then a more likely outcome would be a cross-licensing agreement in the early stages of negotiation. Unfortunately, the number of patents that fit this profile is too few to confirm this theory statistically within the scope of this work. However, we did find a general correlation.

Lexar vs. Memorex, Toshiba

In 2002, Lexar sued Toshiba and Memorex based on ten patents. Five of the patent numbers were released into press publications, they are 5479638, 5,818,781, 5907,856, 5,907,856,

5,930,815, and 6,145,051.[60] [61] The positions of these patents with respect to the number of patent citations is given in

Patent Number	Application Date	Primary US Class	Title	Number of FC (Referenced By)	Lawsuit ?
5596526	8/15/1995	365/185.17	Non-volatile memory system of multi-level transistor cells and methods using same	37	
5835935	9/13/1995	711/103	Method of and architecture for controlling system data with automatic wear leveling in a semiconductor non-volatile mass storage memory	37	
5845313	7/31/1995	711/103	Direct logical block addressing flash memory mass storage architecture	36	
5907856	3/31/1997	711/103	Moving sectors within a block of information in a flash memory mass storage architecture	29	Yes
6125435	11/24/1997	711/201	Alignment of cluster address to block addresses within a semiconductor non-volatile mass storage memory	28	
5838614	5/19/1997	365/185.11	Identification and verification of a sector within a block of mass storage flash memory	25	
5818781	11/13/1996	365/226	Automatic voltage detection in multiple voltage applications	22	Yes
6081878	2/25/1998	711/168	Increasing the memory performance of flash memory devices by writing sectors simultaneously to multiple flash memory devices	22	
5928370	2/5/1997	714/48	Method and apparatus for verifying erasure of memory blocks within a non-volatile memory structure	19	
6034897	4/1/1999	365/185.33	Space management for managing high capacity nonvolatile memory	19	
6115785	5/13/1999	711/103	Direct logical block addressing flash memory mass storage architecture	18	

[60] Jurrien, Ilse, "Lexar and Memorex settled patent infringement", *Let's go Digital: Your online magazine for digital imaging*, August 15, 2005, Obtained January 11, 2006,<http://www.letsgodigital.org/en/news/articles/story_4070.html>.

[61] Abramson, Ronna, "SanDisk fans hold fast" TheStreet.com, December 15, 2005, Obtained January 11, 2006, <http://www.thestreet.com/pf/tech/semis/10257544.html>.

5930815	10/7/1997	711/103	Moving sequential sectors within a block of information in a flash memory mass storage architecture	17	Yes
6151247	3/7/2000	365/185.11	Method and apparatus for decreasing block write operation times performed on nonvolatile memory	17	
6202138	1/20/2000	711/168	Increasing the memory performance of flash memory devices by writing sectors simultaneously to multiple flash memory devices	17	
6040997	3/25/1998	365/185.33	Flash memory leveling architecture having no external latch	16	
6145051	3/8/1999	711/103	Moving sectors within a block of information in a flash memory mass storage architecture	15	Yes
5953737	7/7/1998	711/103	Method and apparatus for performing erase operations transparent to a solid state storage system	14	
6076137	12/11/1997	711/103	Method and apparatus for storing location identification information within non-volatile memory devices	14	
6128695	9/18/1998	711/103	Identification and verification of a sector within a block of mass storage flash memory	14	
6141249	9/3/1999	365/185.11	Organization of blocks within a nonvolatile memory unit to effectively decrease sector write operation time	14	
6182162	3/2/1998	710/11	Externally coupled compact flash memory card that configures itself one of a plurality of appropriate operating protocol modes of a host computer	14	

Table 28. As we can see, four of the five patents are found in the top 25% of the list. The other patent 5,479,638, which was named in the lawsuit was found to be assigned to Cirrus Logic (which was the former name of Lexar). The number of forward citations on this patent, named "Flash memory mass storage architecture incorporation wear leveling technique", and having the application date of Mar 26, 1993, was 73.

In this case, Memorex decided to settle and accept a license from Lexar. The case against Toshiba

is still ongoing. Thus, although the final decision was not determined by a court, these patents seem relatively strong, and their characteristic of high citation rate seems to corroborate our theory.

Patent Number	Application Date	Primary US Class	Title	Number of FC (Referenced By)	Lawsuit ?
5596526	8/15/1995	365/185.17	Non-volatile memory system of multi-level transistor cells and methods using same	37	
5835935	9/13/1995	711/103	Method of and architecture for controlling system data with automatic wear leveling in a semiconductor non-volatile mass storage memory	37	
5845313	7/31/1995	711/103	Direct logical block addressing flash memory mass storage architecture	36	
5907856	3/31/1997	711/103	Moving sectors within a block of information in a flash memory mass storage architecture	29	Yes
6125435	11/24/1997	711/201	Alignment of cluster address to block addresses within a semiconductor non-volatile mass storage memory	28	
5838614	5/19/1997	365/185.11	Identification and verification of a sector within a block of mass storage flash memory	25	
5818781	11/13/1996	365/226	Automatic voltage detection in multiple voltage applications	22	Yes
6081878	2/25/1998	711/168	Increasing the memory performance of flash memory devices by writing sectors simultaneously to multiple flash memory devices	22	
5928370	2/5/1997	714/48	Method and apparatus for verifying erasure of memory blocks within a non-volatile memory structure	19	
6034897	4/1/1999	365/185.33	Space management for managing high capacity nonvolatile memory	19	
6115785	5/13/1999	711/103	Direct logical block addressing flash memory mass storage architecture	18	
5930815	10/7/1997	711/103	Moving sequential sectors within a block of information in a flash memory mass storage architecture	17	Yes

6151247	3/7/2000	365/185.11	Method and apparatus for decreasing block write operation times performed on nonvolatile memory	17	
6202138	1/20/2000	711/168	Increasing the memory performance of flash memory devices by writing sectors simultaneously to multiple flash memory devices	17	
6040997	3/25/1998	365/185.33	Flash memory leveling architecture having no external latch	16	
6145051	3/8/1999	711/103	Moving sectors within a block of information in a flash memory mass storage architecture	15	Yes
5953737	7/7/1998	711/103	Method and apparatus for performing erase operations transparent to a solid state storage system	14	
6076137	12/11/1997	711/103	Method and apparatus for storing location identification information within non-volatile memory devices	14	
6128695	9/18/1998	711/103	Identification and verification of a sector within a block of mass storage flash memory	14	
6141249	9/3/1999	365/185.11	Organization of blocks within a nonvolatile memory unit to effectively decrease sector write operation time	14	
6182162	3/2/1998	710/11	Externally coupled compact flash memory card that configures itself one of a plurality of appropriate operating protocol modes of a host computer	14	

Table 28: Lexar top 26 most cited patents

ATMEL vs. SST

In 2003, ATMEL won a patent infringement lawsuit against SST, based on patent numbers 4,511,811 and 4,673,829.[62] These patents were bought from SEEQ Technologies, which is the name of a company no longer in existence. When we look at the position of these patents with respect to SEEQ's total portfolio of 30 patents, these patents are found at position 16 and 17, which

is in the lower half of the citation index. At first glance, this would seem to disprove our theory that offensive patents have high citation counts. However, if we compare these two patents to the patents within ATMEL's own patent portfolio, based on relative citation numbers, these patents would fall into the top 20%.

Saifun vs. AMD/Fujitsu

Saifun's 2001 lawsuit against AMD and Fujitsu is a combination of patent infringement and

5.7. Nitride Activity

Our specific interest within the flash industry is nitride-based flash, which is currently under development and in the early stages of production in some places. For the past five years, the attention that nitride-based technology has been receiving from conferences and publications has been steadily increasing. As with any new technology, the community response is highly polarized, it is regarded with considerable skeptism by some and supported with fanatical zeal by others. The patenting activities of four flash companies that developing nitride-based flash products are graphed below in Figure 32. The seven main companies are Saifun, AMD/Fujitsu/Spansion, Hitachi/Renesas, Macronix, Infineon, Tower, and Halo LSI.

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[62] SST News Release "SST Comments on Court Decision in Lawsuit with ATMEL", Sept 18, 2003, Obtained January 11, 2006, <http://www.sst.com/news/?id=211>.

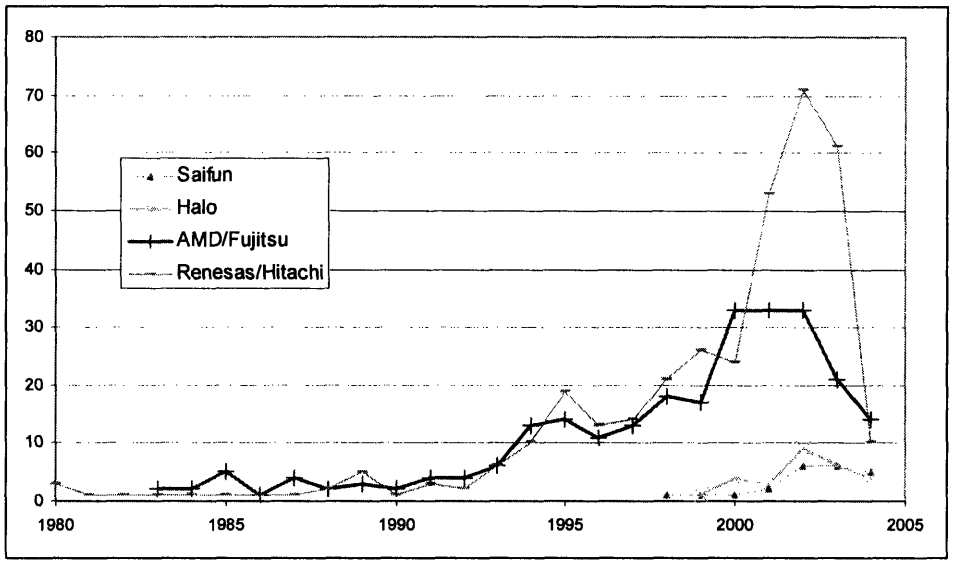

Figure 32: (Nitride) Companies patenting activities

Saifun

Saifun's technology is called NROM. Saifun's 61 patents are divided into 8 main US classes as shown in Figure 33 and Table 29 below

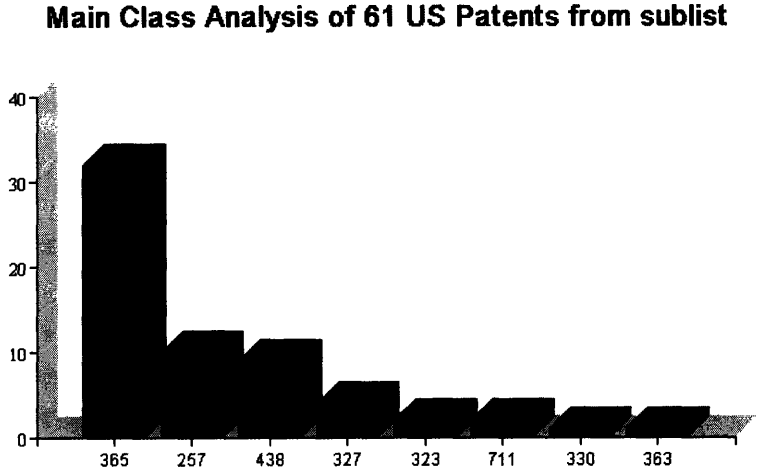

Figure 33: Main class analysis of Saifun's patents

8	Main Class Analysis of 61 US Patents from sublist	
Class No.	Title	No. Patents
365	Static information storage and retrieval	32
257	Active solid-state devices (e.g.,transistors, solid-state diodes)	10
438	Semiconductor device manufacturing: process	9
327	Miscellaneous active electrical nonlinear devices, circuits, and systems	4
323	Electricity: power supply or regulation systems	2
711	Electrical computers and digital processing systems: memory	2
330	Amplifiers	1
363	Electric power conversion systems	1

Table 29: Class definition of Saifun's patents

If we map out the patents along the time scale and show the interconnections between their references, (Figure 34) we can see that all of the patents are built around a key set of patents which were granted between 1999 and 2001. The connections between the patents are very tight. This seems to suggest that improvements and enhancements of the core technology are a consistent party of the patent strategy. The primary focus of this company has been to license and co-develop its nitride-based technology with many licensees.

Patent citation indexing is shown in Table 30.

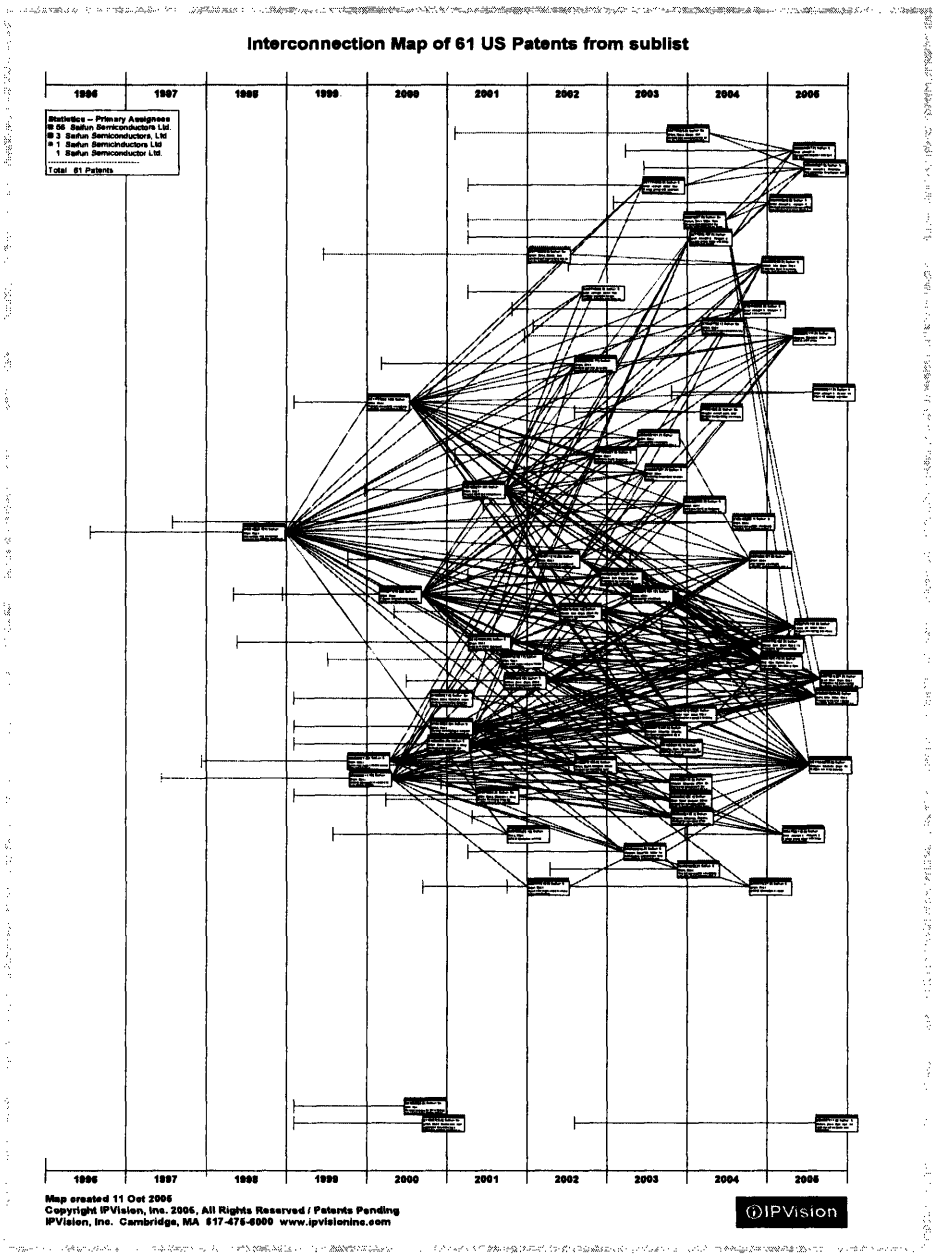

Figure 34:Interconnection map of Saifun's patents

Patent Number	Application Date	Primary US Class	Title	Number of FC (Referenced By)
5768192	7/23/1996	365/185.24	Non-volatile semiconductor memory cell utilizing asymmetrical charge trapping	194
5963465	12/12/1997	365/63	Symmetric segmented memory array architecture	41
5966603	6/11/1997	438/258	NROM fabrication method with a periphery portion	83
6011725	2/4/1999	365/185.33	Two bit non-volatile electrically erasable and programmable semiconductor memory cell utilizing asymmetrical charge trapping	165
6030871	5/5/1998	438/276	Process for producing two bit ROM cell utilizing angled implant	68
6128226	2/4/1999	365/185.21	Method and apparatus for operating with a close to ground signal	33
6134156	2/4/1999	365/189.07	Method for initiating a retrieval procedure in virtual ground arrays	41
6201282	12/23/1999	257/390	Two bit ROM cell and process for producing same	39
6215148	5/20/1998	257/316	NROM cell with improved programming, erasing and cycling	29
6285574	7/6/1999	365/63	Symmetric segmented memory array architecture	18
6297096	7/30/1999	438/261	NROM fabrication method	16
6348711	10/6/1999	257/316	NROM cell with self-aligned programming and erasure areas	24
6396741	5/4/2000	365/185.22	Programming of nonvolatile memory cells	17
6490204	4/5/2001	365/185.28	Programming and erasing methods for a reference cell of an NROM array	16
6552387	12/14/1998	257/324	Non-volatile electrically erasable and programmable semiconductor memory cell utilizing asymmetrical charge trapping	21

Table 30: Saifun's most cited patents

Halo LSI

Halo LSI's memory is also nitride-based but the structure and operation is different from Saifun's basic memory structure. Since the starting point on the value chain is the same, the categories and characteristics of the patent portfolio look very similar.

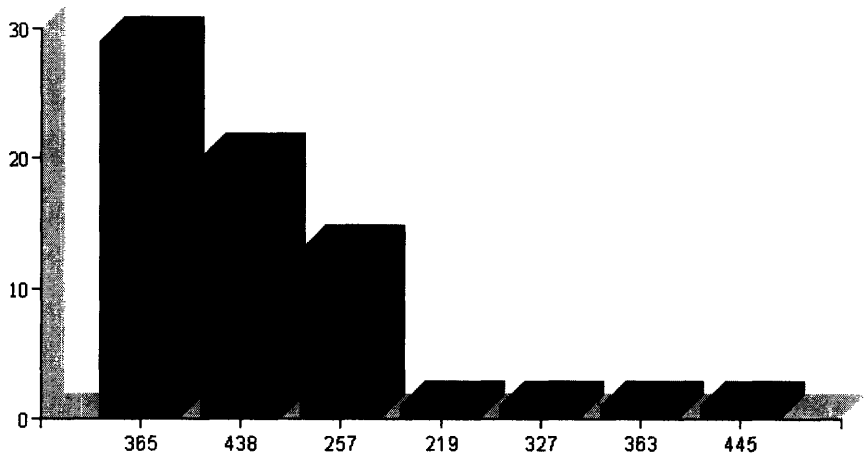

Figure 35: Main class analysis of Halo's patents

7	Main Class Analysis of 66 US Patents from sublist	
Class No.	Title	No. of Patents
365	Static information storage and retrieval	29
438	Semiconductor device manufacturing: process	20
257	Active solid-state devices (e.g.,transistors, solid-state diodes)	13
219	Electric heating	1
327	Miscellaneous active electrical nonlinear devices, circuits, and systems	1
363	Electric power conversion systems	1
445	Electric lamp or space discharge component or device manufacturing	1

Table 31: Class definitions of Halo's patents

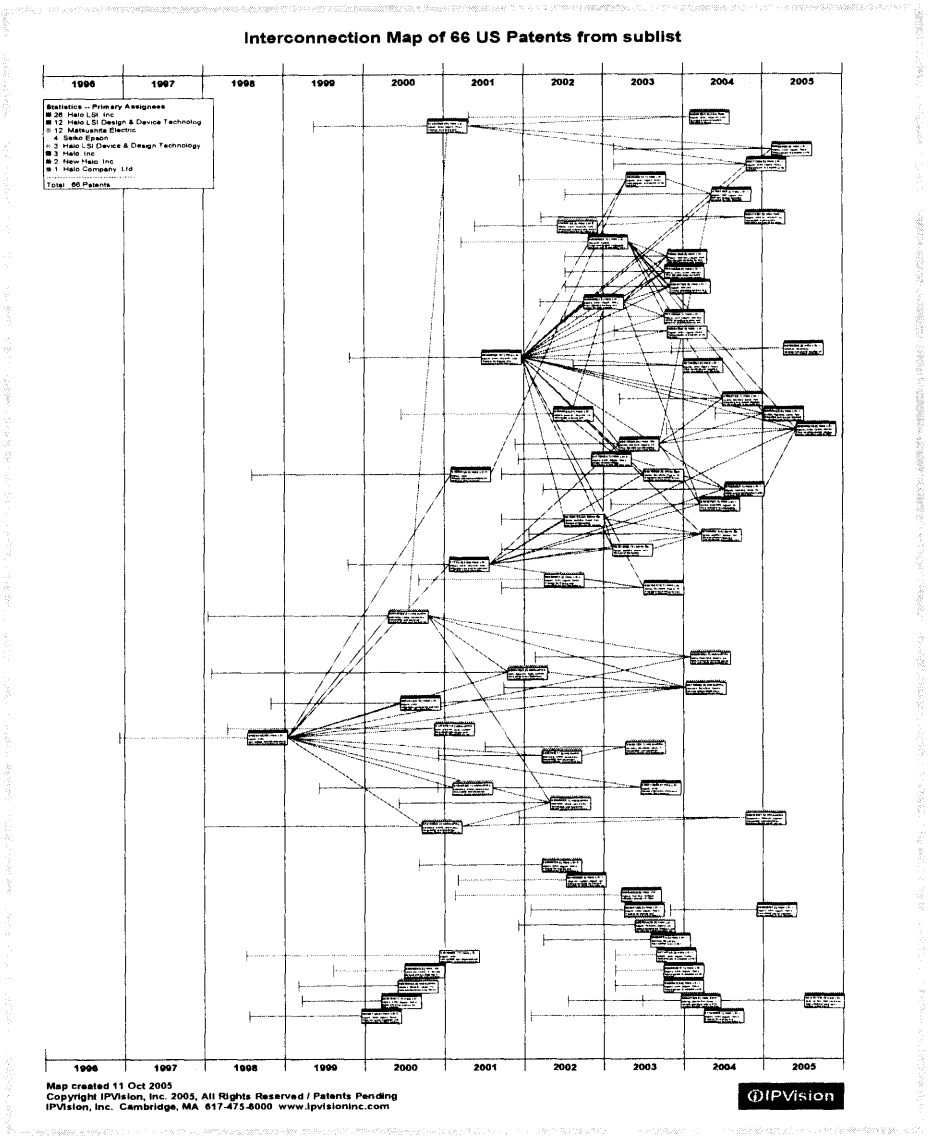

Figure 36: Interconnection map of Halo's patents

Patent Number	Application Date	Primary US Class	Title	Number of FC (Referenced By)
6248633	10/25/1999	438/267	Process for making and programming and operating a dual-bit multi-level ballistic MONOS memory	106
5780341	12/6/1996	438/259	Low voltage EEPROM/NVRAM transistors and making method	86
6177318	10/18/1999	438/267	Integration method for sidewall split gate monos transistor	72
6133098	5/17/1999	438/267	Process for making and programming and operating a dual-bit multi-level ballistic flash memory	44
6388293	6/16/2000	257/365	Nonvolatile memory cell, operating method of the same and nonvolatile memory array	26
6413821	9/18/2001	438/257	Method of fabricating semiconductor device including nonvolatile memory and peripheral circuit	26
6531350	11/21/2001	438/197	Twin MONOS cell fabrication method and array organization	25
6051860	1/16/1998	257/316	Nonvolatile semiconductor memory device and method for fabricating the same and semiconductor integrated circuit	22
6157058	7/8/1998	257/315	Low voltage EEPROM/NVRAM transistors and making method	19
6518124	9/18/2001	438/257	Method of fabricating semiconductor device	19
6074914	10/30/1998	438/257	Integration method for sidewall split gate flash transistor	17
6469935	3/19/2001	365/185.18	Array architecture nonvolatile memory and its operation methods	13
6399441	5/21/2001	438/257	Nonvolatile memory cell, method of programming the same and nonvolatile memory array	10

Table 32: Halo's most cited patents

5.8. Examining Published Applications to Detect New Trends

Further useful information can be obtained from the public patent applications. By examining the types of patents that are currently in the processing pipeline, we can get the latest picture of the company's research and development strategies. Patent applications become available to the

public eighteen months from the filing date. Appendix B5 shows the 5286 flash patent applications that were published, but not yet granted between the dates of March 15, 2001 and December 20, 2005. A subset of the top filers is given in Table 33. From this table, it looks like the companies with the highest levels of recent activity are Micron, Toshiba, Samsung, Renesas, Hynix and Fujitsu.

Assignees Analysis of ALL_APPS_NO_PATENTS_5286 Patent Items from subtracted lists	
Assignees	**Total Patent Items**
unspecified	2864
Micron<LI>Micron (263)</LI><LI>Micron Technology, Inc (5)</LI>	268
Toshiba<LI>Toshiba (171)</LI><LI>KABUSHIKI KAISHA TOSHIBA. (1)</LI>	172
Samsung<LI>Samsung Electronic Co. Ltd. (1)</LI><LI>Samsung (152)</LI><LI>SAMSUNG ELECTRO-MECHANICS CO., LTD. (1)</LI><LI>SAMSUNG ELECTRONICS CO. LTD. (6)</LI><LI>Samsung Electronics Co., Inc. (7)</LI>	167
RENESAS TECHNOLOGY CORP.	128
Hynix<LI>Hynix Semiconductor Inc. (115)</LI>	115
ST<LI>STMicroelectronics, Inc. (16)</LI><LI>STMicroelectronics SA (8)</LI><LI>STMicroelectronics (68)</LI><LI>STMICROELCTRONICS S.r.l (1)</LI><LI>STMicroelectronics Pvt. Ltd. (1)</LI><LI>STMicroelectronics S.r.l (1)</LI>	95
Fujitsu<LI>Fujitsu (88)</LI>	88

Table 33: Subset of Recently Published Patent Applications

The extent of Micron's patenting activity is especially interesting considering its recent alliance with Intel and their plans to build a NAND-flash plant in the United States. The original NAND flash patents will expire in 2007, which means that anyone can freely use the original device patent, leaving the market open to new unlicensed competitors. Therefore, we would be curious to see what areas they are patenting in, could they be improving the NAND? Or could they be exploring other technologies? After reviewing the list of Micron's applications, we found that twenty of the two hundred sixty eight applications, about 10% have the word "NROM" in their title. Ten percent would seem to be a significant number. Therefore, we may speculate that Micron has a

nitride-based memory program within their company. This information would be difficult to find in any other public way.

In reviewing Samsung's patent applications, we also find that there have been several recent patents in the nitride-based memory area. (Appendix C1)

Until a patent has actually been granted, it is not required for the assignee to be publicly known. Some companies take advantage of this in order to avoid attention to their secret or submarine projects. In Table 33, 2864 patents, or more than two thirds of the published applications are unspecified. However, it is possible in many cases to trace the author and agent to the company, by taking a few extra steps. An example of this procedure is described in Appendix B6. By this method, we find that Macronix has also been filing many NROM-related patents.

5.9. Conclusion

Thus, by using IP-Vision[SM] to scrutinize patent portfolios in more detail, we have been able to go beyond the general theories of Chapter 2. We characterized the patent portfolios of companies according to the categories in the IP value chain, and found correlation between their positions and licensing and litigation activities.

6. Direction of Nitride Flash

It is still too early to tell if nitride flash will ultimately replace the conventional floating gate type of flash. However, there are several positive indicators.

Combined together, Saifun and Halo have a significant number of licensees, which is a sign that the industry is open. Considering the fact that the conventional memory device is more than 20 years

old, this acceptance is actually very meaningful. When we look at the patent portfolios of the original market leaders, Toshiba and Intel, the rate of new innovation seems to be low. In contrast, most of the other companies such as Micron, Samsung, Spansion, Renesas, Infineon, and Macronix have been aggressively pursuing nitride patents. One benefit of all of this activity has been an increase in the number of citations for both Saifun and Halo's basic device patents. According to our theory about citation level and patent strength, a higher forward citation number corresponds to higher probability of success during an infringement lawsuit.

There is one concern regarding the balance within Halo and Saifun's patent portfolio. When we mapped the patents of both of these companies on the IP value chain, we found that they are heavily weighted on the side of Memory Technology. However, all of the major players in today's flash market have strong Product patents. It is possible, but not likely that the nitride-based product obsoletes all of the preceding floating gate Product patents. Therefore, it remains a question as to whether or not a licensing partnership would be advisable with the major Product presences like Lexar or SanDisk. However, it may be that the current licensing partnerships already provide indirect relationship channels to those companies.

Although Intel and Toshiba have repeatedly resisted innovations outside of its own device structure, this situation may change in the future. In December 2005, Samsung announced its roadmap for NAND, in which a shift from floating gate memory to nitride-based memory is planned for the year 2008. Samsung has the largest manufacturing capability in the world, and has already been engaged in nitride research and development for several years. It will be interesting to see Intel and Toshiba's responses. Intel had already announced a partnership with Micron to gain entry into the NAND market. That Micron is also developing nitride is an additional benefit for Intel.

7. Conclusion

Thus, we conclude on our exploration of intellectual property and patent licensing strategy in the flash memory industry. Patents play a key role in shaping this market, and we discussed the common factors that influence the effectiveness of patents in different industries. We also applied other general frameworks such as the Licensing Decision Framework, and Porter's Five Forces in order to deepen our understanding of NOR and NAND. We introduced the IP value chain, which mapped patents according to their function in order to gain more insight into the relationships between patent portfolios and core competencies. IP-Vision provided an invaluable means to extract the patents, manage the patent lists, conduct data analysis, and present the results in the most effective graphical form. We also introduced a proposal regarding the existence of a correlation between patents that are named in offensive lawsuits, and the strength of these patents based on citation indexing. Our key motivation for this work was to find patterns in licensing activity related to the flash memory industry. In our analysis, we focused on nitride storage and uncovered new insights and trends in this new field. We look forward to seeing how the future plays out, to confirm or refute our predictions.

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Appendix B1

Patent Data Record for Patent Number 6934190

Patent Number:	6934190
Title:	Ramp source hot-hole programming for trap based non-volatile memory devices
Abstract:	Methods of operating dual bit memory devices including programming with a range of values are provided. The present invention employs a range of ramp source program pulses to iteratively perform a program operation that employs hot hole injection. The range is related to channel lengths of individual dual bit memory cells within the memory device. To program a bit of a particular dual bit memory cell, a negative gate program voltage is applied to its gate, a positive drain voltage is applied to its acting drain, and its substrate is connected to ground. Additionally, a ramp source voltage of the range of ramp source program pulses is concurrently applied to an acting source of the dual bit memory cell. A verification operation is then performed and the programming is repeated with a decremented ramp source voltage on verification failure.
Issue Date:	20050823
Agent:	Eschweiler & Associates, LLC
Application Date:	20040609
Application Serial Number:	863933
Application Series Code:	
Assignee Addresses:	Sunnyvale, CA
Assignees:	Advanced Micro Devices, Inc.
Assistant Examiner:	
Claims:	1. A method of programming a bit of a dual bit memory device comprising: applying a negative gate program voltage to a gate of the memory device; applying a drain program voltage to an acting drain of the memory device; and iteratively applying a range of ramp source voltages to an acting source of the memory device. 2. The method of claim 1, wherein applying the range of ramp source voltages comprises: selecting an initial value as a ramp source voltage; applying the ramp source voltage to the acting source of the memory device; verifying the program operation; and on failure of verification, reducing the ramp source voltage by a step value and re-applying the ramp source voltage to the acting source, re-applying the gate program voltage to the gate, and re-applying the drain program voltage to the acting drain. 3. The method of claim 1, further comprising selecting a wordline to provide the negative gate program voltage, selecting a first bitline to provide the drain program voltage to the acting drain, and selecting a second bitline to provide the range of ramp source voltages to the acting source. 4. The method of claim 1, further comprising selecting a first active region of the memory device as the acting source and a second active region as the acting drain associated with a first bit of the memory device. 5. The method of claim 1, further comprising selecting a second active region of the memory device as the acting source and a first active region as the acting drain associated with a second bit of the memory device. 6. The method of claim 1, further comprising selecting the range of ramp source voltages according to expected channel lengths. 7. The method of claim 1, wherein the applied negative gate program voltage is about -;9 volts. 8. The method of claim 1, wherein the applied drain program voltage is about 6 volts. 9. The

method of claim 1, wherein the range of ramp source voltages is about -;0.7 volts to 1.5 volts. 10. The method of claim 2, wherein the step size is about 0.1 volts. 11. A method of operating an array of dual bit memory cells comprising: selecting a dual bit memory cell of the array and selecting a bit of the dual bit memory cell; selecting a first active region of the dual bit memory cell as an acting source for the selected bit and selecting a second active region of the dual bit memory cell as an acting drain; and programming the selected bit of the dual bit memory cell by iteratively applying a range of ramp source program voltages and employing hot hole injection. 12. The method of claim 11, wherein programming the selected bit of the dual bit memory cell comprises iteratively applying a ramp source voltage of the range of ramp source program voltages to the acting source, applying a positive drain voltage to the acting drain, and applying a negative gate program voltage to a gate of the dual bit memory device. 13. The method of claim 11, wherein the ramp source voltage is obtained by decrementing a previous ramp source voltage by a step value. 14. The method of claim 12, further comprising verifying the programming of the selected bit after applying the ramp source voltage. 15. The method of claim 14, wherein verifying the programming comprises measuring a threshold voltage for a side of the selected dual bit memory device that corresponds to the selected bit and comparing the measured threshold voltage with a range of acceptable program threshold voltages. 16. The method of claim 11, further comprising reading the selected bit of the dual bit memory cell by applying a read voltage bias across the acting source and the acting drain regions, applying a read gate voltage to a gate of the dual bit memory cell, and measuring source-drain current to determine content of the selected bit. 17. The method of claim 11, further comprising performing a block erase on the array of dual bit memory cells by applying a positive erase voltage to gates and connecting active regions and substrate to ground. 18. A method of configuring programming operation for a number of dual bit memory cells comprising: determining channel lengths for the number of dual bit memory cells; creating a population distribution associating the channel lengths with the number of dual bit memory cells; and determining an acceptable range of ramp source pulses for programming of the number of dual bit memory cells. 19. The method of claim 18, further comprising identifying a suitable step size at least partly according to the population distribution. 20. The method of claim 18, wherein determining channel lengths comprises identifying allowable channel lengths for the number of dual bit memory cells. 21. The method of claim 18, wherein determining channel lengths comprises measuring dimensions of one or more of the number of dual bit memory cells. 22. The method of claim 18, wherein determining the acceptable range of ramp source pulses comprises identifying a first ramp program voltage corresponding to a largest channel length and identifying a second ramp program voltage corresponding to a smallest channel length. 23. The method of claim 18, wherein the channel lengths include actual and expected channel lengths. 24. The method of claim 19, wherein identifying the suitable step size is further comprises analyzing desired speed of operation. 25. A method of programming a bit of a dual bit memory device comprising: applying a negative gate program voltage to a gate of the memory device; applying a drain to source voltage across an acting drain and an acting source of the memory device concurrent to applying the negative gate program voltage; verifying the programming of the bit; and on failure of verification, incrementing the drain to source voltage by a step value, re-applying the negative gate program voltage, re-applying the incremented drain to source voltage, and re-verifying the programming of the bit until a successful verification. 26. The method of claim 25, wherein incrementing the drain to source voltage comprises decrementing an applied ramp source program voltage to the acting drain.

Examiner: Le; Vu A.

Field Of Search: 365/18519,185.22,185.03,185.24

Foreign Refs:

Government Interests:	
International Classes:	G11C 016/04
Inventor Residence:	Sunnyvale, CA, Sunnyvale, CA, Fremont, CA, San Jose, CA, San Jose, CA
Inventors:	Liu, Zengtao, Liu, Zhizheng, He, Yi, Haddad, Sameer, Randolph, Mark
Notice:	
Other Refs:	
PCT 102E Date:	
PCT 371 Date:	
PCT Filing Date:	
PCT Number:	
PCT Pub Date:	
PCT Pub Number:	
Parent Case Text:	
Primary US Class:	365/185.19
Priority Data:	
Secondary US Classes:	365/185.22
Expired Date:	
Number of BC (US References):	6
Number of FC (Referenced By):	0
Parent Application Date:	
Parent Application Number:	
Parent Patent Number:	
Referenced By:	
Referenced By Assignees:	
Reinstallation Date:	
Relation To Parent:	
Root Application Date:	
Root Application Number:	
Root Patent Number:	
US Reference Assignees:	National Semiconductor Corporation, ¥, Saifun Semiconductors Ltd.¥, Tower Semiconductors Ltd.¥, , Advanced Micro Devices, Inc., Taiwan Semiconductor Manufacturing Company, SanDisk Corporation, Advanced Micro Devices, Inc.
US References:	5284784, 6396741, 6438031, 6645813, 6664587, 6788583

US References
(patents, apps.):

Assigned:

Current Assignees: Advanced Micro Devices, Inc.

Date Assigned:

Appendix B2

Key Words Search Procedure for flash patents

IPVision has a limit to the search field, therefore the list of words needs to be sub-divided. The resulting lists can be combined together afterwards.

1. ((stack or split) and gate)

2. (((program and verify) or (erase and verify)) or (electrically and erasable) or (programmable and memory))

3. (monos or mnos or sonos or (twin and flash) or nrom or (trap and memory) or (nor and memory) or (nand and memory))

4. ((smart and card) or eeprom or eprom or etox or nvram or non-volatile or nonvolatile or (volatile and non) or (flash and memory))

5. (chalcogenide or mram or m-ram or (magnetic and memory) or feram or fe-ram or (ferroelectric and memory))

Subtract
1. (developer or liquid)

Flash Only Companies – Testingthe robustness of the search procedure

Certain companies only sell flash products. Therefore, we can do another search based on the assignee name. Without the specific assignee name search, we find that only a fraction of the patents were found.

Matrix Semiconductor	27%
Sandisk	80%
Saifun	80%
Halo	80%

By the results of this spot test, we estimate that our search method includes only about 80% of the all the flash patents that exist in the US PTO database.

Appendix B3

1. First we did a class-pair analysis on the SanDisk patents. The reason for specifically choosing SanDisk is that this company has patents with the following properties, (i) a sizable group of patents, (ii) flash specific, so that we don't need to worry about filtering out non-flash patents, and (iii) the patent categories cover the entire range of the IP value chain. After extracting the list of class-pairs from SanDisk's' patents, for each class-pair, we then searched the US PTO database for all patents that use the same class-pair. After we manually checked the list of patents (by quickly eyeballing the titles), we then classified the class-pair, as "Unique to flash memory", or "Mostly flash" or "Not flash". The requirements for the different bins are listed below.

Uniquely flash	95% of the patents are flash patents
Mostly flash	>80% of the patents are related to flash
Half flash	~50% of the patents are related to flash
Not flash	<20% of the patents are related to flash

2. We only include "Uniquely flash" and "Mostly flash" to our total class-pair list. However, we expect that many of the "half flash" and "not flash" patents were picked up by the key word search.

3. We repeated procedures 1 and 2, this time using the patent list resulting from the key word search.

The list of classes is given below. The number of patents column gives the number of patents in the US PTO patent database that call that particular class-pair.

	Class Pair	Description	Number of Patents
V1	257/314	Active solid-state devices (e.g.,transistors, solid-state diodes) - variable threshold (e.g., floating gate memory device)	785
V2	257/315	Active solid-state devices (e.g.,transistors, solid-state diodes) - with floating gate electrode	1361

V3	257/316	Active solid-state devices (e.g.,transistors, solid-state diodes) - with additional contacted control electrode	1425
V4	257/317	Active solid-state devices (e.g.,transistors, solid-state diodes) - with irregularities on electrode to facilitate charging or discharging of floating electrode	393
V5	257/318	Active solid-state devices (e.g.,transistors, solid-state diodes) - additional control electrode is doped region in semiconductor substrate	246
V6	257/319	Active solid-state devices (e.g.,transistors, solid-state diodes) - plural additional contacted control electrodes	271
V7	257/320	Active solid-state devices (e.g.,transistors, solid-state diodes) - separate control electrodes for charging and for discharging floating electrode	245
V8	257/321	Active solid-state devices (e.g.,transistors, solid-state diodes) - with thin insulator region for charging or discharging floating electrode by quantum mechanical tunneling	780
V9	257/322	Active solid-state devices (e.g.,transistors, solid-state diodes) - with charging or discharging by control voltage applied to source or drain region (e.g., by avalanche breakdown of drain junction)	197
V10	257/323	Active solid-state devices (e.g.,transistors, solid-state diodes) - with means to facilitate light erasure	63
V11	257/324	Active solid-state devices (e.g.,transistors, solid-state diodes) - multiple insulator layers (e.g., mnos structure)	520
V12	257/325	Active solid-state devices (e.g.,transistors, solid-state diodes) - non-homogeneous composition insulator layer (e.g., graded composition layer or layer with inclusions)	139
V13	257/326	Active solid-state devices (e.g.,transistors, solid-state diodes) - with additional, non-memory control electrode or channel portion (e.g., accessing field effect transistor structure)	221
V14	257/411	Active solid-state devices (e.g.,transistors, solid-state diodes) - composite or layered gate insulator (e.g., mixture such as silicon oxynitride)	477
V15	365/145	Static information storage and retrieval - ferroelectric	1058
V16	365/185.01	Static information storage and retrieval - floating gate	432
V17	365/185.02	Static information storage and retrieval - disturbance control	246
V18	365/185.03	Static information storage and retrieval - multiple values (e.g., analog)	750
V19	365/185.04	Static information storage and retrieval - data security	228
V20	365/185.05	Static information storage and retrieval - particular connection	425
V21	365/185.06	Static information storage and retrieval - segregated columns	199
V22	365/185.07	Static information storage and retrieval - cross-coupled cel	126
V23	365/185.08	Static information storage and retrieval - with volatile signal storage device	319
V24	365/185.09	Static information storage and retrieval - error correction (e.g., redundancy, endurance)	571
V25	365/185.1	Static information storage and retrieval - extended floating gate	264
V26	365/185.11	Static information storage and retrieval - bank or block	934

		architecture	
V27	365/185.12	Static information storage and retrieval - parallel row lines (e.g., page mode)	420
V28	365/185.13	Static information storage and retrieval - global word or bit lines	301
V29	365/185.14	Static information storage and retrieval - program gate	343
V30	365/185.15	Static information storage and retrieval - weak inversion injection	72
V31	365/185.16	Static information storage and retrieval - virtual ground	261
V32	365/185.17	Static information storage and retrieval - logic connection (e.g., nand string)	550
V33	365/185.18	Static information storage and retrieval - particular biasing	1391
V34	365/185.19	Static information storage and retrieval - multiple pulses (e.g., ramp)	381
V35	365/185.2	Static information storage and retrieval - reference signal (e.g., dummy cell)	571
V36	365/185.21	Static information storage and retrieval - sensing circuitry (e.g., current mirror)	853
V37	365/185.22	Static information storage and retrieval - verify signal	868
V38	365/185.23	Static information storage and retrieval - drive circuitry (e.g., word line driver)	716
V39	365/185.24	Static information storage and retrieval - threshold setting (e.g., conditioning)	585
V40	365/185.25	Static information storage and retrieval - line charging (e.g., precharge, discharge, refresh)	432
V41	365/185.26		506
V42	365/185.27	Static information storage and retrieval - substrate bias	370
V43	365/185.28	Static information storage and retrieval - tunnel programming	650
V44	365/185.29	Static information storage and retrieval - erase	1197
V45	365/185.3	Static information storage and retrieval - over erasure	333
V46	365/185.31	Static information storage and retrieval - non substrate discharge	85
V47	365/185.32	Static information storage and retrieval - radiation erasure	77
V48	365/185.33	Static information storage and retrieval - flash	1197
V49	365/45	Static information storage and retrieval - analog storage systems	224
V50	365/65	Static information storage and retrieval - ferroelectric	631
V51	438/201	Semiconductor device manufacturing: process - including insulated gate field effect transistor having gate surrounded by dielectric (i.e., floating gate)	294
V52	438/216	Semiconductor device manufacturing: process - gate insulator structure constructed of diverse dielectrics (e.g., mnos, etc.) or of nonsilicon compound	223
V53	438/257	Semiconductor device manufacturing: process - having additional gate electrode surrounded by dielectric (i.e., floating gate)	1355
V54	438/263	Semiconductor device manufacturing: process - tunneling insulator	215
V55	438/266	Semiconductor device manufacturing: process - having additional, nonmemory control electrode or channel portion (e.g., for accessing field effect transistor structure, etc.)	423

V56	438/267	Semiconductor device manufacturing: process - including forming gate electrode as conductive sidewall spacer to another electrode	222
V57	438/287	Semiconductor device manufacturing: process - gate insulator structure constructed of diverse dielectrics (e.g., mnos, etc.) or of nonsilicon compound	552
V58	438/288	Semiconductor device manufacturing: process - having step of storing electrical charge in gate dielectric	68
V59	438/3	Semiconductor device manufacturing: process - having magnetic or ferroelectric component	1177
V60	438/593	Semiconductor device manufacturing: process - separated by insulator (i.e., floating gate)	397
V61	438/594	Semiconductor device manufacturing: process - tunnelling dielectric layer	281
V62	711/103	Electrical computers and digital processing systems: memory - programmable read only memory (prom, eeprom, etc.)	928

Appendix B4

Name Aliasing Procedure

Procedure to reduce redundancies in the assignees names.

1. Collect ALL PATENTS.
2. Perform Assignee Analysis. Assignees will automatically be sorted by the order of patent portfolio size.
3. Change the order of the list to Alphabetical. Assignees with similar spellings will be grouped closer together.
4. Manually go through the list to find redundancies, add to the Name Aliasing list below.
5. After re-analyzing the Assignee Analysis using the Name Aliasing list, it would be helpful to repeat steps 2-4 again. Personally, I needed to iterate three times in order to converge.

Statistics

	Total Assignees
Before assignee redundancy reduction	1422
After assignee redundancy reduction	1023

Table A-1

Naming Alias List

```
3Com (|3COM Corporation|3Com Technologies|);

3M (|3M Innovative|3M|);

AMD (|Advance Micro Devices*|Adanced Micro Devices*|Advanced Micro
Devices*|Advanced Mirco Devices|Advaned Micro Devices*|AMD|);

Acer (|Acer Peripherals, Inc.|Acer Semiconductor|);

Actrans (|Actrans*|Actrans System Inc.|);

Addams System (|Addams System|Addams Systems Inc.|);

Advantest Corp (|Advantest Corp*|);

Agere (|Agere*|Agere Systems* Inc.|);

Agilent (|Agilent*|Agilent Technologies|);

Alcatel (|Alcatel*|Alcatel N.V.*|Alcatel Cit|);

Allen-Bradley Company (|Allen-Bradley Company *|);

Alliance Semiconductor (|Alliance Semiconductor *|);

Altera (|Altera*|Altera Coporation|);

AmberWave Systems (|AmberWave Systems*|);

American Microsystems Inc (|American Microsystems*|);
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AMIC Technology (|AMIC Technology*|AMIC Technology, Inc.|);

Aplus Flash Technology (|Aplus Flash Technology, Inc.|Aplvs Flash Technology,
Inc.|);

AT&T (|AT&T*|AT&T Technologies,Inc.|AT&T Corp|AT&T IPM Corp.|AT&T
Technologies, Inc.|);

ATT Bell Labs (|ATT Bell Labs|ATT and Bell Labs|);

Azalea Microelectronics (|Azalea Microelectronics *|);

BAE Systems (|BAE SYSTEMS*|BAE Systems|BAE Systems, Inc.|);

BASF (|BASF|BASF Lacke*|);

Bell Labs (|Bell Canada|Bell Communications|Bell Labs|);

California Micro Devices (|California Micro Devices*|California Micro Devices,
Inc.|);

Catalyst Semiconductor (|Catalyst Semiconductor *|);

Caywood,John (|Caywood,John|The John Millard and Pamela Ann
Caywood*|Caywood,John M.|John Millard and Pamela Ann Caywood *|);

Centre Electronique (|Centre Electronique Hor*|);

Chartered Semiconductor (|Chartered Semiconductor *|Chartere Simiconductor
*|Chartered SimiConductor*|);

Chesebrough (|Chesebrough-Pond's USA Co.|Chesebrough-Pond's USA Co., Division
of Concopo, Inc.);

Chrysler (|Chrysler|Chrysler Motors Corporation|);

Citizen (Ciziten|Citizen Watch, Co., Ltd.|);

Compaq (|Compaq|Compaq Information Technologies Group, L.P.|);

Cypress (|Cypress*|);

Daewoo (|Daewoo Electronics Co., Ltd.|Daewoo Telecom Ltd.|);

Dallas Semiconductor (|Dallas Semiconductor Corp.|Dallas Semiconductor|Dallas
Semiconductor Corporation|);

Delco (|Delco*|Delco Electyronic Corp.|);

Dell (|Dell Products, LP|Dell USA, L.P.|);

Dialog Semiconductor (|Dialog Semiconductor*|);

Dongbu Electronics (|Dongbu Electronics*|Dongbu Electronics Co., Ltd.|Donghu
Electronics Co., Ltd.|);

Ericsson (|Ericsson|Ericsson Inc|);

Fairchild Camera (|Fairchild Camera*|Fairchild Camera & Instrument|);

Fairchild Semiconductor (|Fairchild Semiconductor*|);
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FASL (|FASL LLP|Fasl, LLC|);

France Telecom (|France Telecom*|);

Freescale Semiconductor (|Freescale Semiconductor*|Freescale Semiconductor,
Inc.|);

Fuji Xerox (|Fuji Xerox*|Fuji Xerox Co.|);

Fujitsu (|Fujitsu|Fujitisu Limited|Fujitsu Ltd|Fujitsu VLSI Limited|Fujitsu
Fanuc Limited|);

Fujitsu-AMD (|Fujitsu AMD Semiconductor *|Fujitsu and Semiconductor *|);

Gemplus (|Gemplus|Gemplus Card International|Gemplus Electronics|Gemplus
S.C.A|);

General Instrument (|General Instrument Corp.|General Instrument
Corporation|);

Goldstar Electron (|Goldstar Electron Company, Ltd.|Goldstar Electron Co.,
Ltd.|);

Halo LSI (|Halo LSI Design & Device Technology, Inc.|Halo LSI Device & Design
Technology, Inc.|Halo. LSI Design and Device Technologies, Inc.|Halo LSI Devices
& Design *|Halo LSI, Inc.|Halo, Inc.|Halo. LSI Design*|Aalo LSI Design*.|New
Halo|);

Headway Technologies (|Headway Technologes, Inc.|Headway Technologies|);

Hewlett Packard (|Hewlett Packard Company|Hewlett
Packard*|Hewlett-Packard*|HP|);

Hitachi (|Hitachi Europe, Ltd.|Hitachi Global Technologies|Hitachi USLI
Engineering Co., Ltd.|Hitachi VLSI Engineering|Hitachi|Hitachi *|Hitaachi,
Ltd.|Hitachi Device Eng. Co.|Hitachi Device Engenering Co., Ltd.|Hitachi Europe,
Ltd., Hitachi Global Technologies|Hitachi Keiyo Engineering Co., Ltd|Hitachi
Kokusai Electric Inc.|Hitachi ULSI|Hitachi ULSI Engineering Co., Ltd.|Hitachi
ULSI Systems Co., Ltd.|Hitachi ULSI Systems Co., Ltd.|Hitachi ULSI Engineering
Co., Ltd.|Hitachi VLSI*|Hitachi VLSI Engineering Co.|Hitachi VLSI Engineering,
Ltd.|Hitachi, Limited|Hitachi, Ltd. & Engineering Corp.|Hitachi, ULSI System
Co., Ltd.|);

Holtek (|Holtek Microelectronics, Inc.|Holtek Semiconductor Inc.|);

Honeywell (|Honeywell International|Honeywell Information|Honewell
International|Honeywell, Inc.|);

Hon Hai (|Hon Hai*|Hon Hai Precoision Ind. Co., Ltd.|);

Hynix (|Hynix Demiconductor Inc.|Hynix Semiconductor|Hynix Semiconductor
Inc.|Hynix Corporation|Hynix Demiconductor|Hynix *|Hynix Semiconductorr
Inc.|Hynix Semicondutor Inc.|);

Hughes Electronics (|Hughes Electronics|Hughes Microelectronics
Limited|Hughes Microlectronics Limited|);

Hyundai (|Hyudai Electronics Industries co., Ltd.|Hyundai Electronics|Hyundai
Electronics Ind. Co., Ltd.|Hydai Electronics Industries Co., Ltd.|Hyundai
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Electronics America|Hyundai Electronics Co., Ltd.|Hyundai Micro Electronics
Co., Ltd.|Hyunday Electronics Industries Co., Ltd.|);

ICT International CMOS TEchnology (|ICT International CMOS Technolgy, Inc.|ICT
International CMOS Technology, Inc.|ICT, Inc.);

Infineon (|Infineon *|Infincon Technologies*|Infineion Technologies
*|Infincon Technologies AG|Infineion Technologies AG|Infineon AG|Infineon
Technologies|Infineon Technology AG|Infineon Technoloiges AG|);

Information Storage Devices (|Information Storage Devices*|);

Integrated Silicon Solution (Integrated Silicon Solution*|);

Intel (|Intel|Intel Corp*|Intle Corp*|Intel Corpration|Intle Corporation|);

Intersil Americas Inc (|Intersil America Inc.|Intersil Americas Inc|Intersil
Americas Inc|Intersil|Intersil Corporation|Intersil Incorporated|);

IMEC (|Interuniversitair Microroelektronica *|);

Invoice Technology (|inVoice Technology, Inc.|Invoice Technology|);

Kodak (|Kodak *|);

Korea (|Korea Advanced Institute of Science & Technology|Korea Advanced
Institute Science and Technology|Korea Institute of Science and Technology|);

Kyocera (|Kyocera America, Inc.|Kyocera Corporation|);

Lattice Semiconductor (|Lattice Semiconductor Corp.|Lattice Semiconductor
Corporation|);

Lexar Media (|Lexar|Lexar Media, Inc.|Lexar Microsystems, Inc.|);

LG (|LG|LG Semicon*|LG Information & Communications, Ltd.|LG Semicon, Co.,
Ltd.|);

L'Oreal (|L'Oreal|L'Oreal S.A.|);

Macronix (|Macronix International|Macroniox International Co., Ltd.|Macronix
Internatioal, Ltd.|Macronix International Co.|Macronix International
Co.|Macronix International Co., Ltd.|Macronix International Company,
Ltd.|Macronix International, Co., Ltd.|Macronix Int'l Co., Ltd.|Macroniz
International Co., Ltd.|);

Matsushita Electric (|Matsushita Electric *|Matshshita Electronics
*|Panasonic*|Matshshita Electronics Coropration|Matsushita Electirc
Industrial Co., Ltd.|Matsushita Electonics Corporation| Matsushita Electric
Corporation of America|Matsushita Electric Industrial Company,
Ltd.|Matsushita Electric Inudustrial Co., Ltd.|Matsushita
Electronics|Matsushita Electronics Company|Panasonic Technologies Inc.|);

Micrel (|Micrel, Inc.|Micrel, Incorporated|);

MicrochipTechnology (|MicrochipTechnology Incorporated|MicrochipTechnology,
Incorporated|);

Micron (|Micron Communications, Inc.|Micron Quantum Devices, Inc.|Micron
Semiconductor, Inc.|Micron Technologies, Inc|Micron Technology|Micron
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Technololgy, Inc.|MicronTelecommunications, Inc.|Micron, Technology, Inc.|);

Mitsubishi (|Mitsubishi Chemical America, Inc.|Mitsubishi Chemical
Corporation|Mitsubishi Denki|Mitsubishi Electric Corporation|Mitsubishi
Electrica Engineering Company Limited|Mitsubishi Electric Semiconductor
Software Co., Ltd.|Mitsubishi Electric System LSI Design|Mitsubishi Kenki
Kabushiki Kaisha|Mitsubishi Materials Corporation|Mitsubishi Semiconductor
America, Inc.|Mitsubushi Denki Kabushiki Kaisha|);

Mosaid (|Mosaid Technologies Inc.|Mosaid Technologies Incorporated|);

Motorola (|Motorola|Motorola, Inc|);

M-Systems (|M-Systems Flash Disk Pioneers Ltd.|M-Systems|);

Nanya Technology (|Nanya Technology Corp.|Nanya Technology Corporation|);

NEC (|NEC|NEC Electroincs Corporation|NEC Electronics Corporation|NEC
Electronics Inc.||NEC Research Institute, Inc.|);

Nippon Steel (|Nippon Steel Corporaition|Nippon Steel|Nippon Steel
Semiconductor Corp.|);

NTT (|Nippon Telegraph & Telephone Public Corporation|Nippon Telegraph and
Telephone Public Corporation|);

Nokia (|Nokia Corporation|Nokia Mobile Phones, Ltd.|Nokia Mobile|);

Nonvolatile Electronics (|Nonvolatile Electronics Incorporated|Nonvolatile
Electronics, Incorporated|);

Norris Communications (|Norris Communcations Corporation|Norrice
Communications, Inc.|);

Nortel Networks (|Nortel Networks Corporation|Nortell Networks Limited|);

Oki Electric (|Oki Electric industry Co, Ltd.| OKI Data Corporation|Oki
Semiconductor *|Oki Electric|);

Pageant Technologies (|Pageant Technologies, Inc.|Pageant Technologies, Inc.
(Micromem Technologies, Inc.)|);

Philips (|Philips Electroics North America Corporation|Philips
Electronics|Philips North America|Philips NV|Philips Semiconductors|Philips
US|);

Phision Electronic (|Phision Electronic Corp|Phision Electronics Corp.|);

Pioneer (|Pioneer|Pioneer Digital Technologies, Inc.|);

Plessey (|Plessey Handel und Investments A.G.|Plessy Overseas Limited|);

Powerchip Semiconductor (|Powerchip Semiconductor Corp.|Powership
Semiconductor Corporation|Powership Semiconductor Corp.|);

Programmable Microelectronics (|Programmable Microelectronic
Corporation|Programmable Microelectronics Corp.|);

Progressant Technologies (|Progressant Technologies, Inc.|Progressent
Technologies, Inc.|);
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Qualcomm (|Qualcomm|QualComm, Incorporated|);

Quickturn (|Quickturn Design|Quickturn Design Systems, Inc.|);

RCA (|RCA|RCA Corp.|);

Radient Technologies (|Radiant Technologies|Radiant Technologies, Inc.|);

Ramtron (|Ramtron International Corporation|Ramtron Corporation|);

Renesas (|Renesas Technology|Reneses Technology Corp.|Renesas Technology Corporation|Reneses Technology Corp.|);

Rohm (|Rohm|Rohm Co*|Rhohm Co., LTD|Rohm Co. Ltd.|Rohm Co., Inc.|Rohm Company Limited|Rohm Company, Ltd.|Rohm Corporation|Rhon Corporation|Rohn Corporation|);

Rockwell (|Rockwell|Rockwell Automation|Rockwell Automation Technologies, Inc.|Rockwell Technologies, LLC);

Saifun Semiconductor (|Saifun Semiconductor Ltd.|Saifun Semiconductors, Ltd.);

Samsung (|Samsung|Samsune Electronics Co., Ltd.|Samsung Display Devices Co., Ltd.|Samsung Electric Co., Ltd.|Samsung Electro-Mechanics Co., LTD|Samsung Electronic Co., Ltd.|Samsung Electronics|SamSung Electronics Co. Ltd.|Samsung Electronics Co., Inc.|Samsung Electronics Co., Inc.|Samsung Electronics Co., LTE|Samsung Electronics, Co.|Samsung Electronics, Cot., Ltd.|Samsung Electronics, Cp., Ltd.|Samsung Electronics., Ltd.|Samsung Eletronics Co., Ltd.|Samsung SDI Co., Ltd.|SamSung Semiconductor & Telecommuncation Co., Ltd.|Samusung Electronics Co., Ltd.|);

Schlumberger (|Schlumberger Electronics * Limited|Schlumberger Industries|Schlumberger Industries, S.A.|Schlumberger Malco, Inc.|Schlumberger Systemes|Schlumberger Technologies, Inc.|);

Seagate (|Seagate|Seagate Technology LLC|);

SEEQ Technology (|SEEQ Technology, Inc.|Seeq Technology Incorporated|Seeq Technology);

Seiko/Epson (|Seiko Epson|Seiko|Seiko Instruments & Electronics Ltd.|Seiko Precision Inc.|);

Semiconductor Energy Lab (|Semiconductor Energy Lab|Semiconductor Energy Laboratories Co., Ltd.|);

SGS Microelectronics (|SGS Microelectronics S.A.|SGS Microelectronics S.p.A|SGS Microelettronica S.p.A|SGS Microellettronica S.p.A.|);

SGS Thompson (|SGS Thomson|SGS Thomson SA|SGS Thomson-Microelectronics SA|SGS-ATES Componenti Elettronici S.p.A.|SGS-ATES Componeti Electtronici S.p.A.|SGS--Thmomson Microelectronics S.r.l.|SGS-Thomas Microelectronics S.A.|SGS-Thomas Microelectronics s.r.l.|SGS-Thomason Microelectronics S.r.l.|SGS-Thompson Microelectronics, S.r.l.|SGS-Thomson Micoroelectronics S.A.|SGS-Thomson Micrelectronics GmbH|SGS-Thomson Microelectronics Limited|SGS-Thomson Microelectronics s.p.a.|SGS-THOMSON Microelectronics srl|SGS-Thomson Microelelctronics s.r.l.|SGS-Thomson Microeletronics S.r.l.|SGS-Thomson Microellectronics s.r.l.|SGS-Thomson Micrelectronics,

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S.r.l.|SGS_Thomson Microelectronics|SGS-Thomson Microelectronics GmbH|);

Sharp (|Sharp|Sharp Kabushiki|Sharp Kabushika Kaisha|Sharp Kabushiki
K.K.|Sharp Laboratories of America, Inc.|Sharp Microelectronics Technology,
Inc.|SharpKabushiki Kaisha|Sharp|);

Siemens (|Siemens AG|Siemens Automotive Corporation|Siemens Energy &
Automation, Inc.|Siemens, Aktiengesellschaft|Siemens|);

Sierra Semiconductor (|Sierra Semiconductor B.V.|Sierra Semiconductor
Corporation|);

Silicon Access Networks (|Silicon Access Networks, Inc.|Silicon Access
Networks|);

Silicon Storage Technologies (|Silicon Storage Technologies, Inc.|Silicon
Storage Technology, Inc.|);

Siliconix (|Siliconix, Inc.|Siliconix Incorporated|);

Sony (|Sony|Sony Electronics|Sony Electronics Inc.|Sony International *
GmbH|Sony Trans Com, Inc.|Sony United Kingdom Limtied|Sony|);

Star Micronics (|Star Micronics Co., Ltd.|Star Micronics Company Ltd.|);

ST (|STMicroelectronics|STMicroelectronicsStMicroelctronics,
S.r.l|STMicroelecronics S.r.l.|STMicroelecrics S.r.l|STMicroelectronics
Ltd.|STMicroelectronics N.V.|STMicroelectronics Pvt.
Ltd.|STMicroelectronics S.rll.|STMicroelectronics, Inc.|STMicroelectronics,
S.A.|STMicroelectronicsS.r.l.|STMicroelectronis, S.r.L.|STMicroeletronics
S.R.L.|STMicrolelectronics, Inc.|STMicroelctronics,
S.r.l.|STMicroelectrics S.r.l|);

Symbios (|Symbios Logic Inc.|Symbios, Inc.|);

Synaptics (|Synaptics, Inc.|Synaptics, Incorporated|);

Tachyon (|Tachyon Semiconductor Corporation|Tachyon Semiconductors
Corporation|);

TSMC (|Taiwan Semiconductor Manufacting Company|Taiwan Semiconductor
Manufactoring Company|Taiwan Semiconductor Manufacturing Company Ltd.|Taiwan
Semiconductor Mft. Co. Ltd.|Taiwan, Semiconductor Manufacturing
Caompany|Taiwian Semiconductor Manufacturing Company|);

Texas Instruments (|Texas Instrument, Inc.|Texas Instruments|Texas
Instruments Deutschland GmbH|Texas Instrumens Incorporated|Texas Instrument
Incorporated|Texas Instrumenr, Inc.|Texas Instruments, Inc.|Texas Instruments,
Incorporated|);

TI-Acer (|Texas Instruments - Acer Incorporated|Texas Instruments Acer
Incorporated|Texas Instruments--Acer Incorporated|);

Draper Labs (|The Charles Stark Draper Laboratory*|The Charles Stark Draper
Lab*|);

The British Petroleum Company (|The British Petroleum Company p.l.c.|The British
Petroleum Company, P.L.C.|);
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Thin Film Electronics (|Thin Film Electronics|Thin Film Electronics ASA|);

Thomson Components (|Thomson Components-Mostek Corporation|Thomson Components
- Mostek Corp.|);

Tokyo Electron (|Tokyo Electron|Tokyo Electron Device Limited|);

Tokyo Shibaura (|Tokyo Shibaura|Tokyo Shibaura Electric|Tokyo Shibaura
Electric Company, Ltd.);

Toshiba (|Toshiba|Toshiba Corporation|Toshiba Micro-Electronics
Corporation|Kabushiki Kaisha Toshiba|Kabushiki Kaisa Toshiba|Kabushikia
Kaisha Toshiba|Kabushki Kaisha Toshiba|Kabushiki Kaishi Toshiba|);

Tower Semiconductor (|Tower Semiconductor Ltd.|Tower Semiconductors Ltd.|);

TRW (|TRW|TRW Automotive Electronics & Components GmbH & Co. KG|);

Turbo IC (|Turbo IC|Turbo IC, Inc.|);

UBIQ (|UBIQ Inc.|UBIQ Incorporated|);

UMC (|UMC Japan|United Microelectonics Corp.|United Microelectronic
Corp.|United Microelectronics|UMC *|United Micro Electronics
Corporation|United Microelectronics Corp.|United Microelectronics
Corp.|United Microelectronics Corp.|United Microelectronics Crop.|United
Microflectronics Corporation|);

United Semiconductor (|United Semiconductor *|);

University of Maryland (|University of Maryland*|);

Vanguard (|Vanguard|Vanguard International Semiconductor Company|Vanguard
Semiconductor, Ltd.|);

Virage Logic (|Virage Logic Corporation|Virage Logic Corp.|);

WSI (|Wafer Scale Integration, Inc.|WaferScale Integration, Incorporation|);

Warman International (|Warman International Ltd.|Warman International,
Inc.|);

Western Digital (|Western Digital * Inc.|Western Digital Corporation|Western
Digital Technologies, Inc.|);

Westinghouse (|Westinghouse|Westinghouse Elect. Corp.|);

Whitaker (|Whitaker|Whittaker Corporation|);

Winbond Electronics (|Winbond Electonics Corporation|Winbond Electronics
Corporation|Winbond Electronics|Winbond Electronics Corp.|Winbond
Electronics Corp. America|Winbond Electronics Corp.l|Winbond Electronics
Corporation|Winbond Memory Laboratory|Windbond Electronic Corp|Windbond
Electronics Corp.|Windbond Electronics Corporation|);

WiSys Technology Foundation (|WiSys Technology Foundation, Inc.|WiSys
Technology Foundation|);

Worldwide Semiconductor Manufacturing Corp (|Worldwide Semiconductor
Corp.|Worldwide Semiconductor Manufacturing Corporation|Worldwide
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Semiconductor MFG|);
Xicor (|Xicor, Inc.|Xicor Corporation|);
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Appendix B5

5286 flash patent applications were published, but not issued between March 15, 2001 to December 20, 2005. These patents were sorted by assignee.

Assignees Analysis of ALL_APPS_NO_PATENTS_5286 Patent Items from subtracted lists	
Assignees	**Total Patent Items**
unspecified	2864
Micron<LI>Micron (263)</LI><LI>Micron Technology, Inc (5)</LI>	268
Toshiba<LI>Toshiba (171)</LI><LI>KABUSHIKI KAISHA TOSHIBA. (1)</LI>	172
Samsung<LI>Samsung Electronic Co. Ltd. (1)</LI><LI>Samsung (152)</LI><LI>SAMSUNG ELECTRO-MECHANICS CO., LTD. (1)</LI><LI>SAMSUNG ELECTRONICS CO. LTD. (6)</LI><LI>Samsung Electronics Co., Inc. (7)</LI>	167
RENESAS TECHNOLOGY CORP.	128
Hynix<LI>Hynix Semiconductor Inc. (115)</LI>	115
ST<LI>STMicroelectronics, Inc. (16)</LI><LI>STMicroelectronics SA (8)</LI><LI>STMicroelectronics (68)</LI><LI>STMICROELCTRONICS S.r.l (1)</LI><LI>STMicroelectronics Pvt. Ltd. (1)</LI><LI>STMicroelectronics S.r.l (1)</LI>	95
Fujitsu<LI>Fujitsu (88)</LI>	88
IBM	76
Seiko/Epson<LI>Seiko Epson (71)</LI>	71
Matsushita Electric<LI>MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD., (2)</LI><LI>Matsushita Electronics (1)</LI><LI>Matsushita Electric (65)</LI>	68
NEC<LI>NEC ELECTRONICS CORPORATION (36)</LI><LI>NEC Research Institute, Inc. (2)</LI><LI>NEC (24)</LI>	62
Sharp<LI>Sharp (40)</LI><LI>Sharp Laboratories of America, Inc. (20)</LI>	60
Hitachi<LI>Hitachi (44)</LI><LI>Hitachi Global Technologies Netherlands B.V. (2)</LI>	46
Macronix<LI>MACRONIX INTERNATIONAL CO., LTD. (44)</LI>	44
Mitsubishi<LI>Mitsubishi Denki (43)</LI>	43
DongbuAnam Semiconductor Inc.	39
Sony<LI>Sony (39)</LI>	39
TSMC<LI>Taiwan Semiconductor Manufacturing Co., Ltd., (37)</LI>	37
SANDISK CORPORATION	32
STMicroelectronics S.r.l.	27
TSM	27
Infineon<LI>Infineon (19)</LI><LI>Infineon Technologies North America Corp. (3)</LI>	22
Motorola<LI>Motorola (19)</LI>	19
Semiconductor Energy Lab<LI>Semiconductor Energy Lab (19)</LI>	19
Intel<LI>Intel Corporation, a Delaware corporation (2)</LI><LI>Intel (15)</LI><LI>Intel Corporation a Delaware corporation (1)</LI>	18
Headway Technologies, Inc.	17
Sanyo	17
Microsoft	16
Nanya Technology	15
TDK	14
Matrix Semiconductor Inc.	13
SUPER TALENT ELECTRONICS INC.	13
Aplus Flash Technology	11
Hyundai<LI>Hyundai Electronics (10)</LI>	10
Texas Instruments<LI>Texas Instruments Deutschland GmbH (1)</LI><LI>Texas Instruments, Incorporated (1)</LI><LI>Texas Instruments (8)</LI>	10
Winbond Electronics<LI>Winbond Electronics Corp. (2)</LI><LI>Winbond Electronics Corporation (8)</LI>	10
Canon	9
M-SYSTEMS FLASH DISK PIONEERS, LTD.	9
Nantero, Inc.	9
Anam Semiconductor, Inc.	8
Impinj, Inc., a Delaware Corporation	8
AMD<LI>AMD (7)</LI>	7
M-Systems<LI>M-SYSTEMS FLASH DISK PIONEERS LTD. (7)</LI>	7
Symetrix Corporation	7
Tower Semiconductor	7
Applied Materials	6
MATRIX SEMICONDUCTOR	6
Semiconductor Leading Edge Technologies, Inc.	6
Vanguard<LI>Vanguard (6)</LI>	6

Actel Corporation	5
Atmel Corporation	5
Broadcom Corporation	5
Chartered Semiconductor<LI>CHARTERED SEMICONDUCTOR MANUFACTURING LTD. (5)</LI>	5
FUJIO MASUOKA	5
Halo LSI<LI>HALO LSI, Inc. (5)</LI>	5
Nippon Steel<LI>Nippon Steel (5)</LI>	5
Philips<LI>Philips NV (5)</LI>	5
Phison Electronics Corp.	5
Seagate<LI>Seagate Technology LLC (5)</LI>	5
UMC<LI>United Microelectronics (5)</LI>	5
Unity Semiconductor Corporation	5
Carry Computer Eng. Co., Ltd.	4
Fuji Photo	4
Nokia<LI>Nokia Corporation (4)</LI>	4
O2IC, Inc.	4
Oki Electric<LI>Oki Electric (4)</LI>	4
Taiwan Semicondutor Manufacturing Co.	4
AGFA-GEVAERT	3
Axalto SA	3
BAE Systems<LI>BAE Systems Information and Electronic Systems Integration, Inc. (3)</LI>	3
BTG International Inc.	3
California Institute of Technology, a California Non-Profit Corporation	3
Denso	3
Dongbu Electronics<LI>Dongbu Electronics Co., Ltd. (3)</LI>	3
Honda	3
Honeywell<LI>Honeywell International (3)</LI>	3
Interuniversitair Microelektronica Centrum (IMEC)	3
L'Oreal<LI>L'Oreal (2)</LI><LI>L'OREAL S.A. (1)</LI>	3
Matsushita Elec. Ind. Co. Ltd.	3
OSAKA UNIVERSITY	3
ProMOS Technologies Inc.	3
Rohm<LI>Rohm (3)</LI>	3
Semiconductor Components Industries, LLC.	3
Semiconductor Manufacturing International (Shanghai) Corporation	3
Sun Microsystems, Inc., a Delaware Corporation	3
Actel Corporation, a California Corporation	2
ADVANCED POWER TECHNOLOGY, INC., a Delaware corporation	2
Advanced Technology Materials, Inc.	2

Advantest Corp<LI>ADVANTEST CORPORATION (2)</LI>	2
Agere<LI>Agere Systems, Inc. (2)</LI>	2
Alcatel<LI>Alcatel (2)</LI>	2
Altera<LI>Altera (2)</LI>	2
AmberWave Systems<LI>AmberWave Systems Corporation (2)</LI>	2
ARM LIMITED	2
Brother	2
Catalyst Semiconductor<LI>Catalyst Semiconductor, Inc. (2)</LI>	2
Centre National de la Recherche Scientifique-CNRS	2
ELPIDA MEMORY, INC.	2
Fujitsu-AMD<LI>FUJITSU AMD SEMICONDUCTOR LIMITED (2)</LI>	2
General Instrument	2
Innotech Corporation	2
KABUSHHIKI KAISHA TOSHIBA	2
KABUSHI KAISHA TOSHIBA	2
Kodak<LI>Kodak (2)</LI>	2
Kodak Polychrome Graphics, L.L.C	2
Korea<LI>Korea Institute of Science and Technology (2)</LI>	2
Lattice Semiconductor	2
LG ELECTRONICS INC.	2
LSI Logic	2
Magnachip Semiconductor, Ltd.	2
Mentor Graphics Corporation	2
Montana State University - Bozeman	2
Mosel Vitelic, Inc.	2
NEC ELECTRONIC CORPORATION	2
Powerchip Semiconductor	2
Progressant Technologies	2
Rafsec Oy	2
Renesas<LI>Renesas Technology Corporation (1)</LI><LI>RENESAS (1)</LI>	2
Research In Motion Limited	2
Semiconductor Energy Laboratory Co. Ltd.	2
Siemens<LI>Siemens (2)</LI>	2
Sun Microsystems	2
Tadahiro Ohmi	2
Tadahiro OMI	2
Tatung Co., Ltd.	2
Tohoku University	2
Tokyo Electron<LI>Tokyo Electron (2)</LI>	2
UBIQ<LI>UBIQ Incorporated (2)</LI>	2
University of California	2
VIA TECHNOLOGIES, INC.	2
Xilinx, Inc.	2

021C, Inc.	1
02IC, Inc.	1
02IC, Ltd.	1
AAEON TECHNOLOGY INC.	1
Acard Technology Corp.	1
ADTRAN, INC.	1
Advanced Semiconductor Engineering, Inc.	1
Agate Semiconductor, Inc.	1
Alps Electric	1
Altera Corporation.	1
American Megatrends, Inc.	1
A/N INC.	1
Applied Intellectual Properties Co., Ltd.	1
Applied MicroCircuits Corporation	1
Asahi Glass	1
Ascential Software Corporation	1
ASM International N.V.	1
ATMEL NANTES SA	1
Audiem, Ltd.	1
Ballard Power Systems Corporation	1
Battelle	1
Brocade Communications Systems, Inc.	1
Capstone Turbine Corporation	1
Carry Computer Eng., Inc.	1
Cecilware Corporation	1
Celavie, a corporation of France	1
Cisco Technology, Inc., a California Corporation	1
Commissariat a l'Energie Atomique	1
Commissariat a L'Energie Atomique	1
Compaq<LI>Compaq Information Technologies Group, L.P. (1)</LI>	1
C-One Technology Corporation	1
Conti Temic Microelectronic GmbH	1
COVA Technologies, Inc.	1
Dell<LI>Dell Products, L.P. (1)</LI>	1
Dongguk University	1
D-Wave Systems, Inc.	1
Elite Semiconductor Memory Technology Inc.	1
EM Microelectronic-Marin SA	1
Emulex Design & Manufacturing Corporation	1
e-Smart Technologies, Inc., a Nevada Corporation	1
ESM Limited	1
FASL, LLC, a limited liability company	1
Flex-P Industries	1
Fujitsu Limited of Kawasaki, Japan	1
FUJITSU QUANTUM DEVICES LIMITED	1

FUNAI ELECTRIC CO., LTD.	1
GE	1
GEMINI MOBILE TECHNOLOGIES, INC.	1
Gemplus<LI>GEMPLUS (1)</LI>	1
Government of the United States	1
Grandex International Corporation	1
GVC CORPORATION	1
HANA MICRON INC.	1
Harris	1
Headway Technologies, Inc.&Applied Spintronics, Inc.	1
Hewlett Packard<LI>HP (1)</LI>	1
HIGH TECH COMPUTER, CORP.	1
Hitachi, Ltd. and Hitachi ULSI Systems Co., Ltd.	1
HONDA MOTOR CO., LTD.	1
HRL Laboratories, LLC	1
Hughes Electronics<LI>Hughes Electronics (1)</LI>	1
Husky Injection Molding Systems LTD	1
Hyundai Electronics Industries Co., Ltd	1
IGT	1
Impinj, Inc. A Delware Corporation	1
INCOE CORPORATION	1
Industrial Technology	1
Integrated Magnetoelectronics Corporation A California corporation	1
Integrated Silicon Solution<LI>INTEGRATED SILICON SOLUTION, INC. (1)</LI>	1
Intematix Corporation	1
Intermec IP Corp.	1
International Business Mechines Corporation	1
I/O Integrity, Inc.	1
Iota Technology, Inc.	1
KEIO UNIVERSITY	1
Kingston Technology Co.	1
Kodak Polychrome Graphics LLC	1
Koinklije Philips Electronics N.V.	1
KoninklijkePhilips Electronics N.V.	1
Lam Research Corporation	1
Lear Corporation	1
Lexar Media<LI>Lexar Media, Inc. (1)</LI>	1
LG Semicon Co.	1
Linear Technology Corporation	1
Lockheed	1
L'OREL	1
Lucent	1
Marvell International Ltd.	1
Marvell World Trade Ltd.	1

Matsushita Electric Industial Co,. Ltd.	1
Matsushita Industrial Co., Ltd.	1
MediaTek Inc.	1
MediCapture, Inc.	1
Micron Technoloy Inc.	1
Micron Techology, Inc.	1
MITSIBISHI DENKI KABUSHIKI KAISHA	1
Mitsubishi Denki Kabushiki Kaisha, Mitsubishi Electric Engineering Company Limited	1
Mobile-Vision Inc.	1
Monolithic System Technology, Inc.	1
Mosaic Systems, Inc.	1
M-SYSTEMS FLASH DISK POINEERS LTD.	1
Multi Level Memory Technology, Inc.	1
Murata	1
Nanosys, Inc.	1
National Chio-Tung University	1
National Institute of Advanced Industrial Science and Technology	1
NATIONAL UNIVERSITY CORPORATION NAGOYA UNIVERSITY	1
National University of Singapore	1
Nat'l. Inst. of Advanced Indust'l Sci. and Tech.	1
NEK CORPORATION	1
Network Appliance, Inc.	1
New Halo, Inc.	1
NexFlash Technologies, Inc.	1
novem car interior design Metalltechnik GmbH	1
NVE Corporation	1
O2IC, Inc., (a California corporation)	1
Oki Electric Co., Ltd.	1
OnSpec Electronic, Inc.	1
OPTION	1
PDF Solutions	1
P&G	1
PIONEER CORPORATION	1
Precision Instrument Development Center, National Science Council	1
Rambus Inc.	1
RAMOS TECHNOLOGY CO., LTD.	1
Raytheon	1
REGENTS OF THE UNIVERSITY OF NORTH TEXAS	1
Renesas Corporation	1
Renesas Technoloigy Corp.	1

RiTek Corporation	1
R&R Card Systems, Inc.	1
SAE Magnetics (H.K.) Ltd.	1
Saifun Semiconductor	1
SANKYO SEIKI MFG.CO., LTD.	1
SGS Thompson<LI>SGS Thomson (1)</LI>	1
Sharp Laboratories of America Inc.	1
SHOWA DENKO K.K.	1
Shuffle Master, Inc.	1
Shure Incorporated	1
Sierra Wireless, Inc., a Canadian Corporation	1
Silicon Based Technology Corp.	1
SILICON INTEGRATED SYSTEMS CORP.	1
Silterra	1
SILVERBROOK RESEARCH PTY LTD	1
SimpleTech, Inc.	1
Spansion LLC	1
ST Incard S.r.l.	1
StorCard, Inc.	1
Sun Microsystems, Inc. a Delaware Corporation	1
Taiwan Semiconductor Mnaufacturing Co.	1
Taiwan Semincondutor Manufacturing Co.	1
Terra Semiconductor, Inc.	1
Tessera, Inc.	1
The Regents of the University of California and North Carolina State University	1
Thomas & Betts International, Inc.	1
Thoughtbeam, Inc.	1
Tokyo Electron Limited of TBS Broadcast Center	1
UltraCard, Inc.	1
UNITED MIRCOELECTRONICS CORP.	1
UNITY SEMICONDUCTOR INC.	1
USUN TECHNOLOGY CO., LTD.	1
Vantis Corporation	1
Varian Semiconductor Equipment Associates, Inc.	1
V-DA Technology	1
Visa International Service Association	1
Visa U.S.A., Inc.	1
Widevine Technologies, Inc.	1
Xircom, Inc.	1
Zarlink Semiconductor AB	1

Appendix B6

Here, we found the companies associated with the unassigned patent applications.

Inventor analysis of the Patent Applications shows some familiar author's names. The first line of the table below, Daniel C. Guterman has also been named an author of several patents at SanDisk. This procedure is cumbersome to perform on a one-by-one basis for each author. But it may be useful to cross-reference a list of known authors for a specific company and to identify key "submarine" patents.

Inventors	Total US Patent Applications	Company
Guterman, Daniel C. (Fremont, CA)	28	SanDisk?
Iwata, Yoshihisa (Yokohama-shi, JP)	28	
Harari, Eliyahou (Los Gatos, CA)	25	SanDisk?
Shibata, Akihide (Nara-shi, JP)	24	
Iwata, Hiroshi (Ikoma-gun, JP)	23	
Perner, Frederick A. (Palo Alto, CA)	23	
Anthony, Thomas C. (Sunnyvale, CA)	21	
Ding, Yi (Sunnyvale, CA)	21	
Gilton, Terry L. (Boise, ID)	21	
Moore, John T. (Boise, ID)	20	
Norman, Robert D. (San Jose, CA)	18	
Campbell, Kristy A. (Boise, ID)	17	

By combining an agent analysis and an author analysis, we found that the authors of some of the "unspecified" applications had the same name and locations as those listed under for under Macronix. Macronix has filed than 20 applications based on nitride storage.

Appendix C1

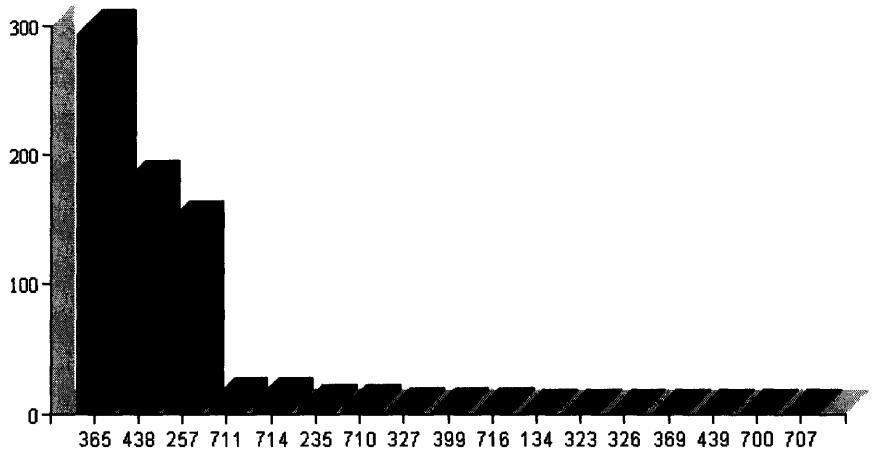
Analysis of Samsung's Patents

Like SanDisk, Samsung is one of Toshiba's original partners for NAND. However, SanDisk shared Toshiba's manufacturing facilities, whereas Samsung's role was to provide second source supply in a different country. The scale of Samsung's operation quickly grew until it overtook Toshiba in sales volume in 2004.

It has over 565 patents covering a range of over 17 US PTO classes. The results of a main class analysis are shown in the figure below. We can see that, unlike the other top flash memory chip suppliers, Intel and Toshiba, Samsung has many device and process level patents as well as system level patents.

In December 2005, Samsung announced in its NAND roadmap that it would switch from floating gate to nitride based storage, starting from the year 2007. Therefore, we are curious to see what kinds of patent protection has been prepared.

Main Class Analysis of 656 US Patents from sublist...



US Main Class	Title	Total US Patents
365	Static information storage and retrieval	294
438	Semiconductor device manufacturing: process	177
257	Active solid-state devices (e.g.,transistors, solid-state diodes)	146
711	Electrical computers and digital processing systems: memory	9
714	Error detection/correction and fault detection/recovery	9
235	Registers	4
710	Electrical computers and digital data processing systems: input/output	4
327	Miscellaneous active electrical nonlinear devices, circuits, and systems	2
399	Electrophotography	2
716	Data processing: design and analysis of circuit or semiconductor mask	2
134	Cleaning and liquid contact with solids	1
323	Electricity: power supply or regulation systems	1
326	Electronic digital logic circuitry	1
369	Dynamic information storage or retrieval	1
439	Electrical connectors	1
700	Data processing: generic control systems or specific applications	1
707	Data processing: database and file management or data structures	1

Within the issued patents, we found sixteen patents related to nitride storage. It should be noted that there is only one patent with an application date of 1998, all of the rest have been applied for after 2003.

Patent Number	Application Date	Inventors	Title
6967373	2/4/2003	Choi, Jeong-Hyuk	Two-bit charge trap nonvolatile memory device and methods of operating and fabrication the same
6960527	9/5/2003	Kang, Sung-Taeg	Method for fabricating non-volatile memory device having sidewall gate structure and SONOS cell structure
6947330	3/28/2003	Lee, Chang-Hyun	Electrically erasable charge trap nonvolatile memory cells having erase threshold voltage that is higher than an initial threshold voltage
6946703	1/9/2004	Ryu, Won-il;Lee, Jo-won;Yoon, Se-wook;Kim, Chung-woo	SONOS memory device having side gate stacks and method of manufacturing the same
6936884	10/14/2003	Chae, Soo-doo;Kim, Ju-hyung;Kim, Chung-woo;Chae, Hee-soon;Ryu, Won-il	Nonvolatile silicon/oxide/nitride/silicon/nitride/oxide/silicon memory
6927131	7/23/2003	Kim, Seong-gyun	Methods of forming a nonvolatile memory device having a local SONOS structure that use spacers to adjust the overlap between a gate electrode and a charge trapping layer
6914013	5/8/2003	Chung, Byung-Hong	Method of forming semiconductor device containing oxide/nitride/oxide dielectric layer
6847556	8/18/2003	Cho, Myoung-kwan	Method for operating NOR type flash memory device including SONOS cells
6844589	12/5/2003	Kim, Seong-Gyun	Non-volatile SONOS memory device and method for manufacturing the same
6835621	6/5/2003	Yoo, Jae-yoon;Park, Moon-han;Kwon, Dae-jin	Method of fabricating non-volatile memory device having a structure of silicon-oxide-nitride-oxide-silicon

6815764	3/17/2003	Bae, Geum-Jong;Lee, Nae-In;Kim, Sang Su;Kim, Ki Chul;Kim, Jin-Hee;Cho, In-Wook;Kim, Sung-Ho;Koh, Kwang-Wook	Local SONOS-type structure having two-piece gate and self-aligned ONO and method for manufacturing the same
6806517	3/17/2003	Kim, Sang Su;Lee, Nae-In;Bae, Geum-Jong;Kim, Ki Chul;Rhee, Hwa Sung	Flash memory having local SONOS structure using notched gate and manufacturing method thereof
6794711	7/14/2003	Kang, Sung-taeg;Han, Jeong-uk;Kim, Soeng-gyun	Non-volatile memory device having select transistor structure and SONOS cell structure and method for fabricating the device
6750525	3/15/2002	Yim, Yong-Sik;Choi, Jung-Dal;Kwack, Hong-Suk;Shin, You-Cheol	Non-volatile memory device having a metal-oxide-nitride-oxide-semiconductor gate structure
6734065	4/18/2003	Yim, Yong-Sik;Choi, Jung-Dal;Kwack, Hong-Suk;Shin, You-Cheol	Method of forming a non-volatile memory device having a metal-oxide-nitride-oxide-semiconductor gate structure
6683010	6/25/1998	Lim, Baek-gyun;Kim, Eu-seok;Yang, Chang-jip;Park, Young-kyou	Method for forming silicon-oxynitride layer on semiconductor device

Publication Number	Application Date	Title
usApplication:20040207002	1/9/2004	SONOS memory device having side gate stacks and method of manufacturing the same
usApplication:20050048702	9/30/2004	Local SONOS-type structure having two-piece gate and self-aligned ONO and method for manufacturing the same
usApplication:20050054167	7/9/2004	Local SONOS-type nonvolatile memory device and method of manufacturing the same
usApplication:20050059209	4/27/2004	Local-length nitride SONOS device having self-aligned ONO structure and method of manufacturing the same
usApplication:20050093058	9/24/2004	Sonos device and methods of manufacturing the same
usApplication:20050112815	10/12/2004	Silicon-oxide-nitride-oxide-silicon (SONOS) memory device and methods of manufacturing and operating the same

Applications Analysis

Samsung has over 167 flash-related patent applications that have been published, but not yet been granted. Among this group, we selected the applications that according to the keywords "charge trap", "nitride", "nrom", "sonos". The six patents found are listed below.