Development of a laboratory course in power electronic control circuitry based on a PWM buck controller

by

Candace N. Wilson

Submitted to the Department of Electrical Engineering and Computer Science in Partial Fulfillment of the Requirements for the Degrees of Bachelor of Science in Electrical Science and Engineering and Master of Engineering in Electrical Engineering and Computer Science at the

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Abstract

Due to the constraints on time and resources within the typical electrical engineering curriculum, it is difficult for students to obtain Integrated Circuit design experience prior to entering industry. This project establishes the foundation for a new laboratory course in power electronics and analog circuit design. There is an introduction to power electronics, particularly the buck converter, and several basic analog circuit building blocks are introduced. A process consisting of circuit design, simulation, construction, and evaluation is developed to provide students with an introduction to Integrated Circuit design. A peak current mode PWM controller for a buck converter is developed to illustrate the fundamental power electronic and analog circuit concepts that are presented.

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1 Introduction

Companies are discovering that often new electrical engineering graduates have very limited knowledge about the integrated circuit (IC) design process. As a result, the initial training period is longer and more extensive than desirable. This is largely because it is fairly challenging to duplicate the intricacies of the IC design process within the resource and time constraints of a typical electrical engineering curriculum. Additionally, it is difficult to remain informed of changes continually developing in industry and to expose students to the many practical concerns involved. This document describes an attempt to create a reasonable and feasible way to make the classroom experience more effective in terms of providing insight and understanding of the IC design process.

This project has developed the foundation for a new laboratory course. The objectives of the new course include the following: 1) introduce students to the fundamentals of power converter control theory, 2) teach students to design analog control circuitry block by block, 3) teach students to simulate models of their circuit designs, 4) instruct students on how to build and debug their circuits and compare experimental results with the simulated results. Ideally, the students will obtain something close to the IC design experience, although they will be using discrete components and constructing on a breadboard or a pre-designed PC board with sockets for inserting components.

The following is a brief overview of the structure of this document. Section 2 contains the power electronics background information required to establish the context for the circuit designs. The buck converter is presented and its general operation is

explained. There is a brief introduction to control theory. Transfer functions are developed for the buck converter and the converter's stability in a closed-loop configuration is addressed. Additionally, in this section the requirements for a PWM control circuit are discussed and an IC version, designed with common commercial operational amplifiers, comparators, and other chips, is developed. Section 3 deals with basic analog circuit building blocks. Commonly used circuits, such as current sources, common emitter amplifiers, and differential pair amplifiers, are introduced and analyzed in detail. Section 4 provides a description of each of the control circuit's functional blocks. Each block is explained and a transistor-level circuit is designed and analyzed. Section 5 contains a brief summary of the project and conclusions and results are formulated. Section 6 is an appendix consisting of diagrams and truth tables for combinational logic gates as well as the full EAGLE schematics for all of the circuit blocks presented in Section 4 as they are laid out on the PC board for the laboratory kits.

2 Background

2.1 Buck Converter

The buck converter is being used as the framework for our converter and controller design. A buck converter is a DC-to-DC power converter which takes some DC input voltage and produces a lower DC output voltage. Figure 2-1 shows the general structure of a buck converter. It consists of 2 switches (S_1 and S_2) which are controlled concurrently such that when S_1 is on (closed), S_2 is off (open), and vice versa. This control is typically periodic with some period T, where $T = \frac{1}{f_s}$ with f_s representing the switching frequency.

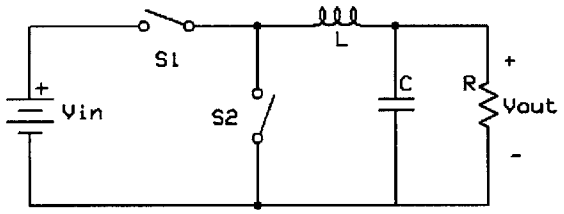

Figure 2-1. Buck converter schematic.

The fraction of the period during which S_1 is on is referred to as the duty ratio or duty cycle (D). The voltage at the node between S_1 and S_2, V_m, is V_{in} when S_1 is on and zero when S_2 is on, as indicated in Figure 2-2. The upper waveform in Figure 2-3 shows an example of what V_m looks like in practice. Note that a significant amount of ringing in the waveform can be observed at the start of every cycle. The inductor (L) and capacitor (C) serve as filtering components. They form a low pass filter which passes the

DC component of V_m and blocks the AC component. The second-order LC filter effectively averages V_m to produce the converter's output voltage:

$$V_{out} = \frac{V_{in} \cdot DT + 0 \cdot (1-D)T}{T} = V_{in} D . \tag{2.1}$$

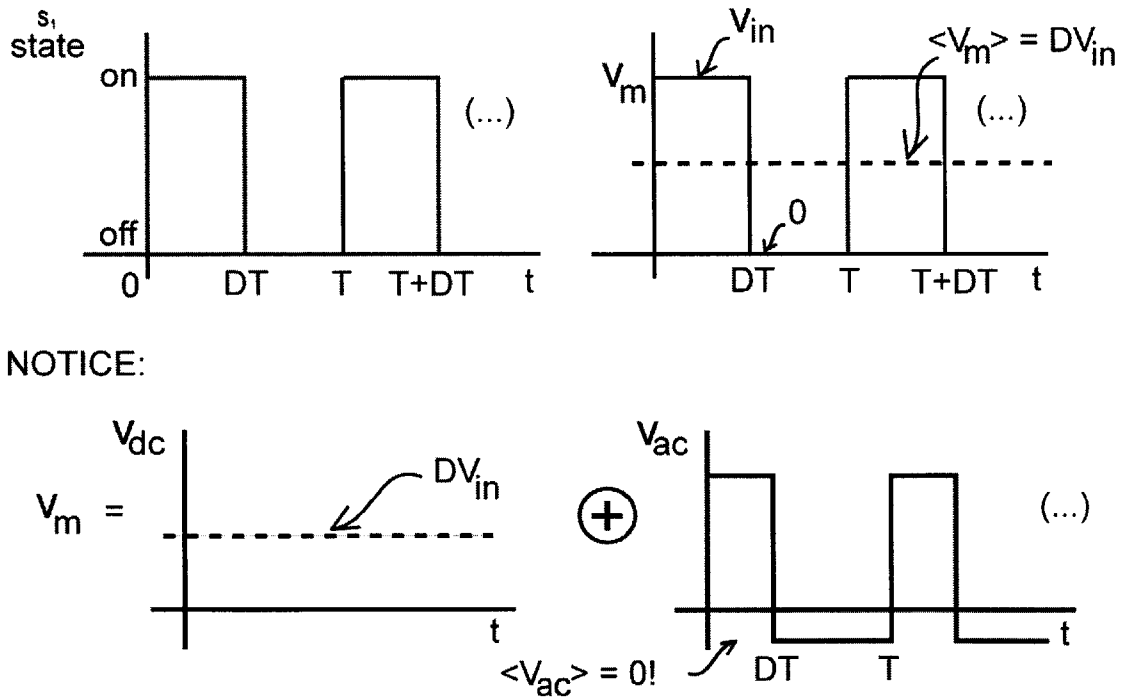

Figure 2-2. Voltage, V_m, at the midpoint between the converter's switches.

The constituitive relation for an inductor is

$$V_L = L \frac{di_L}{dt} . \tag{2.2}$$

Thus, when the voltage across the inductor is positive, the inductor current is increasing and when the voltage is negative, the current is decreasing. During the first part of the cycle, when S_1 is on, the voltage across the inductor is

$$V_L = V_{in} - V_{out}. \tag{2.3}$$

This is a positive voltage because V_{out} is less than V_{in} (by definition) so the inductor current is ramping up. During the second part of the cycle, the inductor voltage is

$$V_L = 0 - V_{out} = -V_{out}. \tag{2.4}$$

This is a negative voltage, thus the inductor current is ramping back down. In equilibrium, the average inductor current is constant, meaning the current must ramp up and down equal amounts. The lower waveform in Figure 2-3 is of a buck converter's inductor current in equilibrium. We can solve (2.2) for di_L to obtain an expression for the inductor current ripple.

$$\Delta i_L = \frac{v_L \cdot \Delta t}{L} \tag{2.5}$$

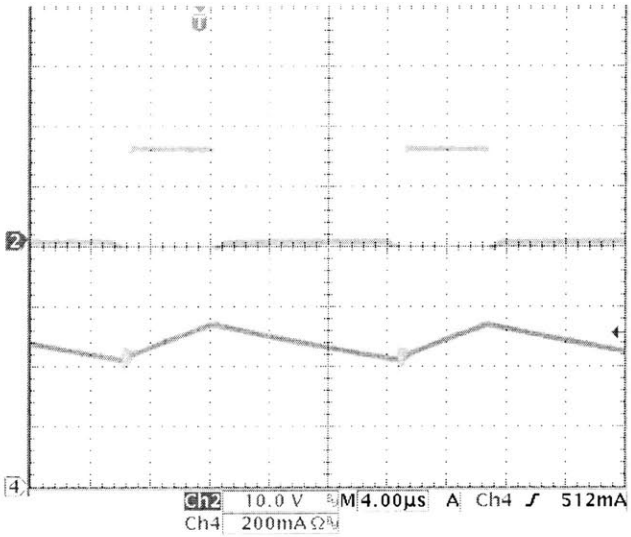

Figure 2-3. Voltage between buck converter switches and inductor current waveform

When designing a buck converter, we typically have some specification for the maximum allowable inductor current ripple. Given the current ripple spec and the inductor voltage expressed in either (2.3) or (2.4), we can derive a constraint that specifies the minimum value inductance required. Solving (2.5) for L yields the inequality

$$L \geq \frac{v_L \cdot \Delta t}{\Delta i_L}. \tag{2.6a}$$

During the first part of the cycle, when S_1 is on, we can substitute (2.3) for v_L and DT for Δt to obtain

$$L \geq \frac{(V_{in} - V_{out}) \cdot DT}{\Delta i_L}. \tag{2.6b}$$

The inductor current ripple shows up as ripple in the output voltage. We can assume that the entire ripple current flows through the capacitor. See the graph of capacitor current in Figure 2-4. The charge injected into the capacitor when the current ripple is positive is

$$q = \frac{1}{2} \cdot \frac{\Delta i}{2} \cdot \frac{T}{2}. \tag{2.7a}$$

Simplification yields

$$q = \frac{1}{8} \cdot \Delta i \cdot T. \tag{2.7b}$$

From the capacitor's constituitive relation, we obtain the following equation for voltage ripple as a function of injected charge

$$\Delta v = \frac{q}{C}. \tag{2.8}$$

Substituting the expression from (2.7) for q in (2.8) gives us an expression for voltage ripple as a function of the inductor current ripple.

$$\Delta v = \frac{\Delta i \cdot T}{8C}. \tag{2.9}$$

Given a spec for the maximum allowable voltage ripple, we can solve (2.9) to determine the required value for C.

$$C = \frac{\Delta i \cdot T}{8 \cdot \Delta v}. \tag{2.10}$$

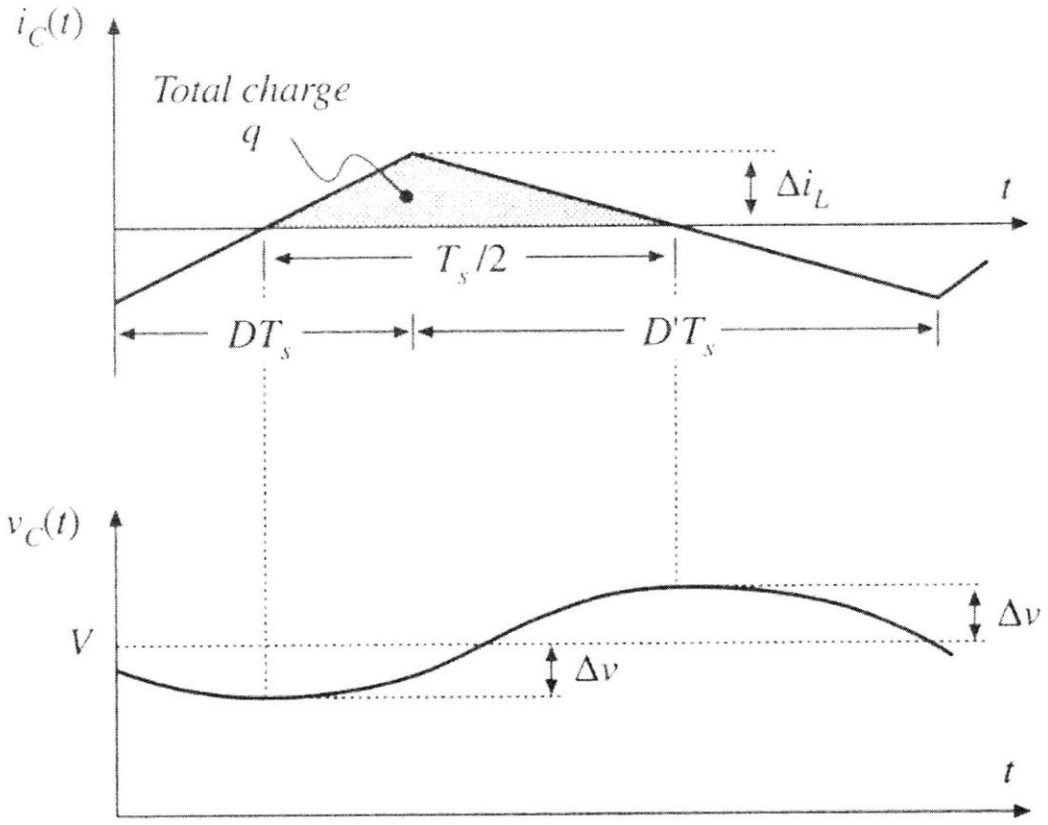

Figure 2-4. The inductor current ripple flows through the capacitor. This ripple current can be integrated to determine the total charge that enters the capacitor.

There are two options for the implementation of the buck converter's switches. We can either use MOSFETs for both switches (synchronous rectification), or we can use a MOSFET for S_1 and implement S_2 with a free-wheeling diode. The second implementation is possible because the inductor current will automatically cause the

diode to conduct when S_1 is turned off. Examples of these switch implementations are contained in Figure 2-5. If we use synchronous rectification, we need a delay circuit, similar to the one shown in Figure 2-6, to ensure that the switches are never on at the same time.

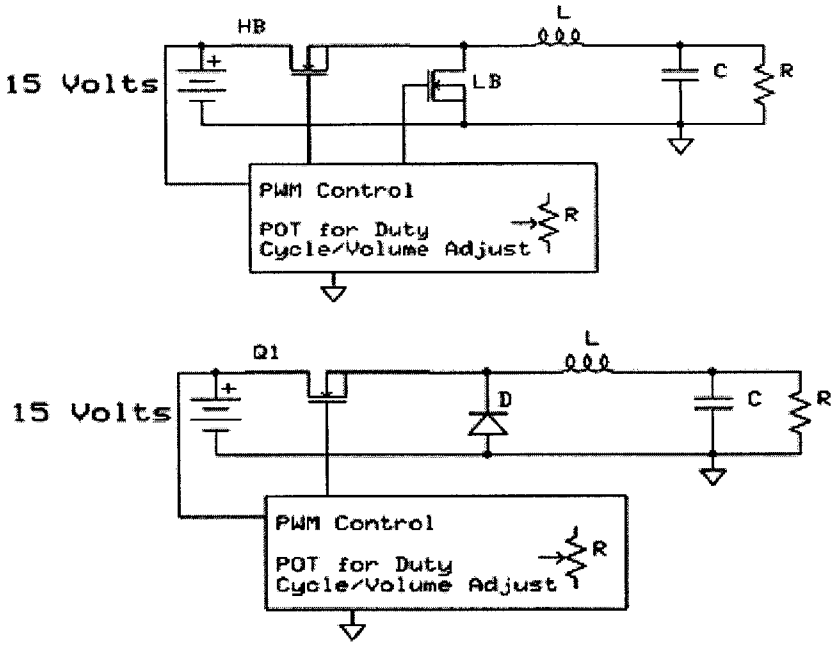

Figure 2-5. The lower switch of a buck converter can be implemented either with a MOSFET or a diode.

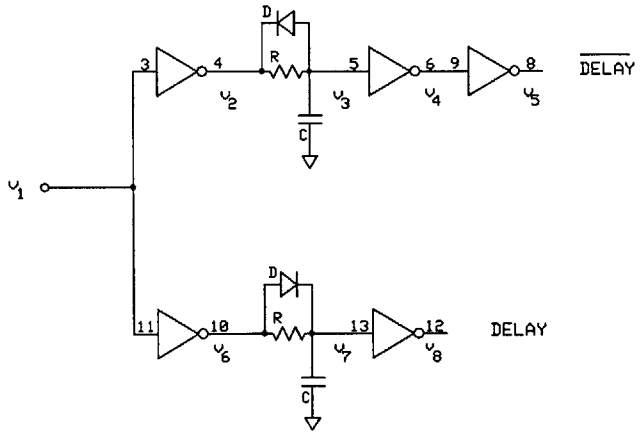

Figure 2-6. A delay circuit is required to ensure that both switches are not on at the same time when the converter's lower switch is implemented with a MOSFET.

For the case when S_2 is implemented with a diode, it is possible for the inductor current to ramp all the way down to zero, at which point the switch will turn off. This is referred to as discontinuous conduction mode (DCM). In order to ensure that this never happens (meaning the converter operates in continuous conduction mode, CCM), the inductor current ripple is not more than twice the average inductor current. Figure 2-7 shows graphically how to determine the requirements for CCM.

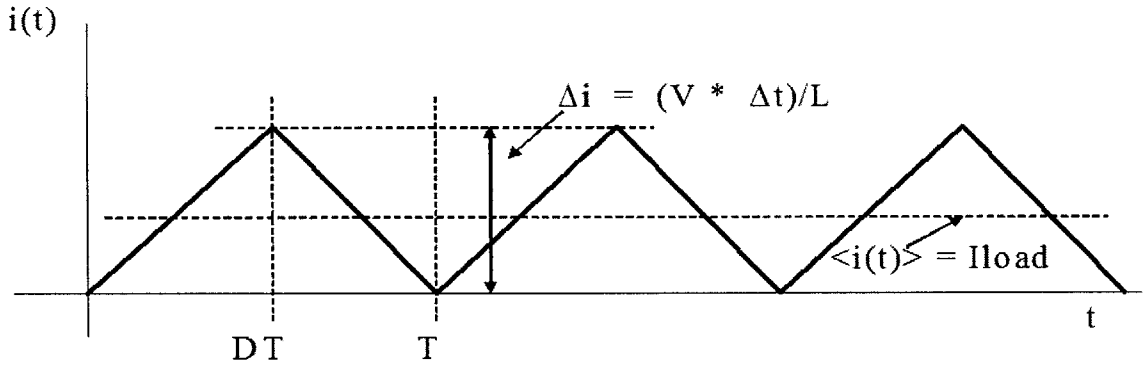

Figure 2-7. Graphical representation of the inductor current at the boundary between CCM and DCM operation.

The boundary between DCM and CCM is when the average inductor current, which is the same as the load current, is equal to half of the inductor current ripple. This condition is expressed mathematically as

$$\langle i_L \rangle = i_{Load} = \frac{\Delta i}{2}. \tag{2.11}$$

To ensure CCM, (2.11) and Figure 2-7 imply the following constraint

$$\langle i_L \rangle = i_{Load} > \frac{\Delta i}{2}. \tag{2.12}$$

For a resistive load,

$$i_{Load} = \frac{V_{out}}{R}. \tag{2.13}$$

Combining (2.12) and (2.13) yields

$$\Delta i < \frac{2 \cdot V_{out}}{R} \tag{2.14}$$

as the requirement for CCM. Substituting the expression for Δi contained in (2.5) and solving for L gives us the minimum inductance required for the converter to remain in continuous conduction mode.

$$L \geq \frac{v_L \cdot \Delta t \cdot R}{2 \cdot V_{out}} \tag{2.15}$$

Again, using the values for the first part of the switching cycle, (2.15) becomes

$$L \geq \frac{(V_{in} - V_{out}) \cdot DT \cdot R}{2 \cdot V_{out}}. \tag{2.16}$$

2.2 Control

The buck converter's output voltage is proportional to both the input voltage and the duty ratio at which its switches are operated. This relation, expressed mathematically in (2.1), is repeated here in (2.17).

$$V_{out} = V_{in} D \tag{2.17}$$

So for a given input voltage, one can set D so that the converter produces the desired output voltage. However, if the input is from an unregulated supply or its value varies over some range, we need a control circuit that manipulates the duty ratio in response to variations in Vin in order to maintain a constant output voltage. . This requires a feedback loop, so that information about the output voltage can be sent to the control circuit. Feedback allows the controller to sense whether the output is too high or too low so it can send the appropriate corrective signals to the converter's switches. Figure 2-8 shows an example of a buck converter with simple control loop. The operational amplifier (op amp) computes the error between the converter's output and some reference voltage then amplifies the error by some factor, K. A comparator then compares the amplified error with a triangle wave and outputs a pulse of variable width. The width of the pulse is determined by the fraction of the period, T, set by the triangle wave that the op amp's output is greater than the level of the triangle wave. That fraction determines the duty ratio at which the switch is operated. This is known as Pulse Width Modulation, or PWM, control.

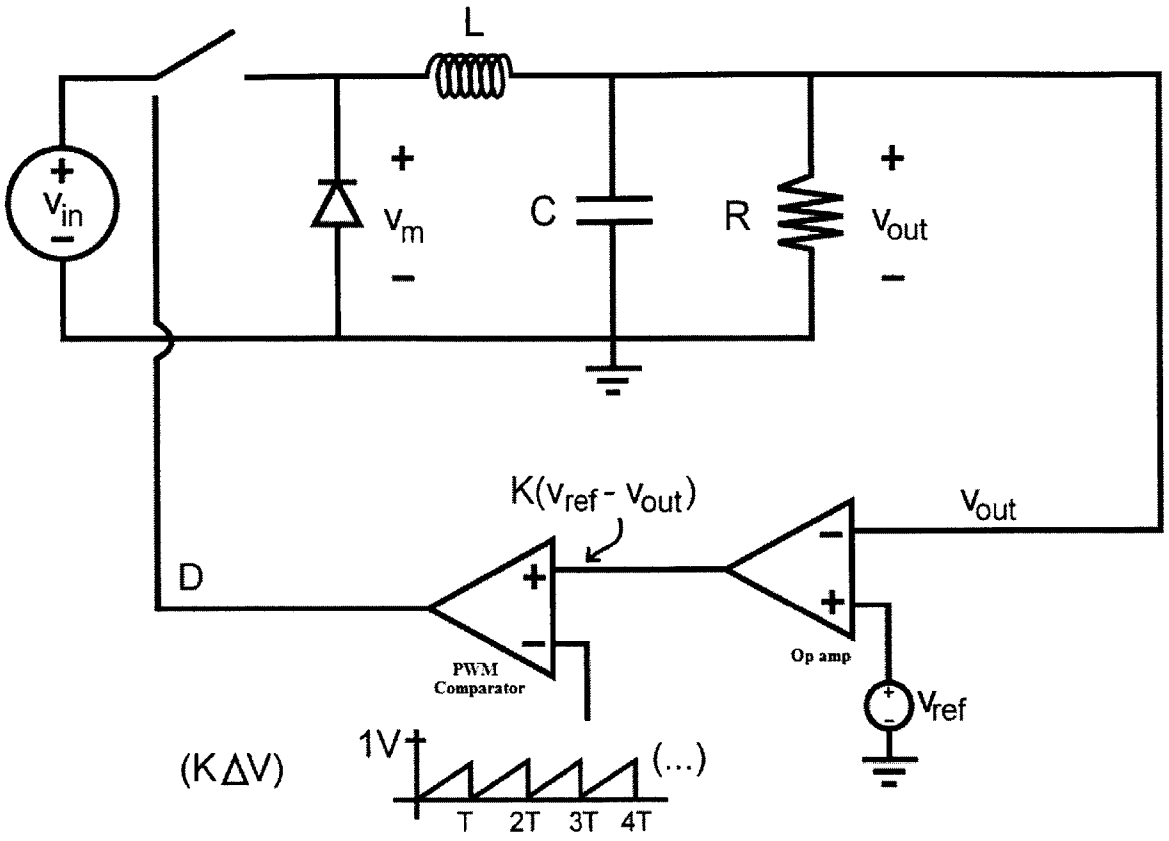

Figure 2-8. Buck converter with a PWM control loop.

In addition to regulating V_{out}, we may be interested in controlling the output (and inductor) current. This can be accomplished by placing a small resistor between the input and S_1 and using the voltage across this current sense resistor to estimate and constrain the inductor current. This is known as peak current mode control because when the current reaches a predetermined maximum level, the controller turns S_1 off regardless of V_{out}. At this point the inductor current ramps down until the start of the next cycle. See Figure 2-9 for an example of a current-mode control circuit for a buck converter. The artificial ramp provides slope compensation which is discussed in detail towards the end

of this section. The other blocks in the control circuit are introduced in Section 2.3 and covered more extensively in Section 4.

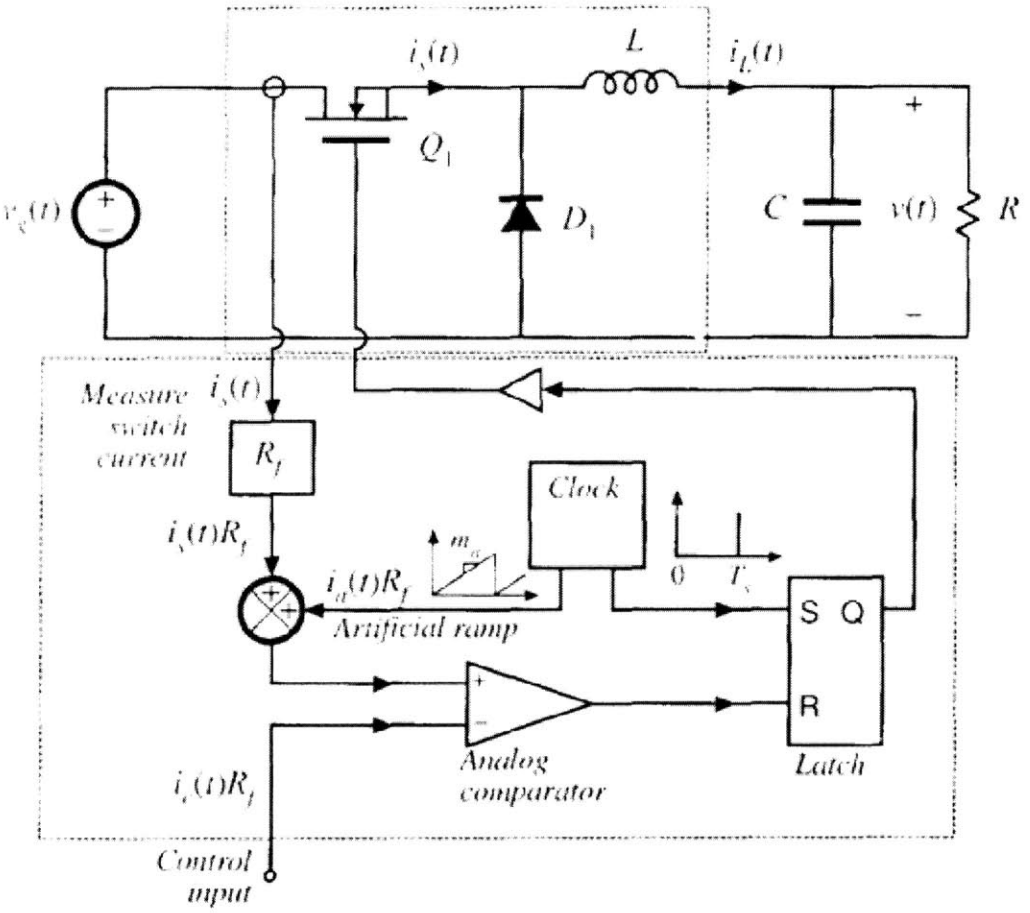

Figure 2-9. Buck converter with current-mode controller.

Modeling the Converter

Before we can design a control loop for the converter, we must have a model of the converter from which we can derive a transfer function. We can develop a linear, averaged model for the converter as explained in [1] and [2]. The switches are modeled as a dependent voltage or current source with duty ratio as a parameter. The averaged

model for a buck converter with voltage mode (duty ratio) control is contained in Figure 2-10.

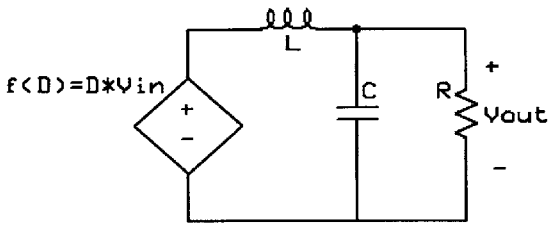

Figure 2-10. Averaged model for buck converter.

There are a few different transfer functions to consider when modeling a converter. The line-to-output transfer function, $H_v(s)$, describes changes in the output voltage due to changes in the input voltage. The control-to-output transfer function, $H_d(s)$, describes changes in the output voltage due to changes in the duty cycle control variable. The output impedance, $Z_{out}(s)$, describes changes in the output voltage due to changes in the load current. We are also concerned with the inductor current. The transfer function, $H_{id}(s)$, describes changes in the inductor current due to changes in d and $H_{iv}(s)$ is the transfer function describing changes in inductor current due to changes in the input voltage. These important transfer functions are derived for the buck converter in [1] and displayed in (2.18)-(2.22).

$$H_v(s) = \frac{v_{out}(s)}{v_{in}(s)}$$

$$H_v(s) = \frac{D}{s^2 LC + s\frac{L}{R} + 1} \tag{2.18}$$

$$H_d(s) = \frac{v_{out}(s)}{d(s)}$$

$$H_d(s) = \frac{\frac{V_{out}}{D}}{s^2 LC + s\frac{L}{R} + 1} \tag{2.19}$$

$$Z_{out}(s) = -\frac{v_{out}(s)}{i_{load}(s)}$$

$$Z_{out}(s) = \frac{sL}{s^2 LC + s\frac{L}{R} + 1} \tag{2.20}$$

$$H_{id}(s) = \frac{i_L(s)}{d(s)}$$

$$H_{id}(s) = \frac{V_{out}(1 + sRC)}{D \cdot R\left(s^2 LC + s\frac{L}{R} + 1\right)} \tag{2.21}$$

$$H_{iv}(s)=\frac{i_L(s)}{v_{in}(s)}$$

$$H_{iv}(s)=\frac{D(1+sRC)}{R\left(s^2LC+s\frac{L}{R}+1\right)} \tag{2.22}$$

Figure 2-11 shows the block diagram for a voltage-mode control loop.

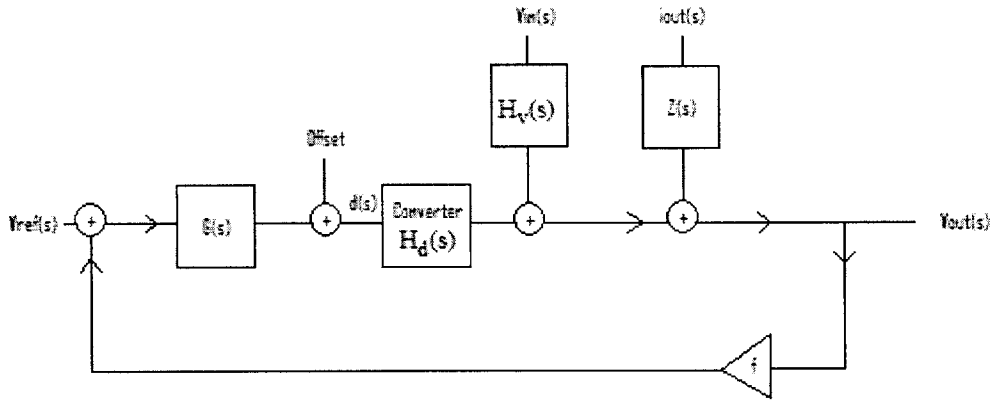

Figure 2-11. Voltage-mode control loop block diagram.

If peak current mode control is used, the switches and inductor can be modeled as a dependent current source with duty ratio as a parameter. This model is shown in Figure 2-12. In this case, the transfer function from input to output voltage becomes

$$H_i(s)=\frac{V_{out}}{I_{in}}(s)=\frac{R}{RCs+1}. \tag{2.23}$$

Controlling the peak current simplifies the model from second order to first order (i.e. 1 pole instead of 2).

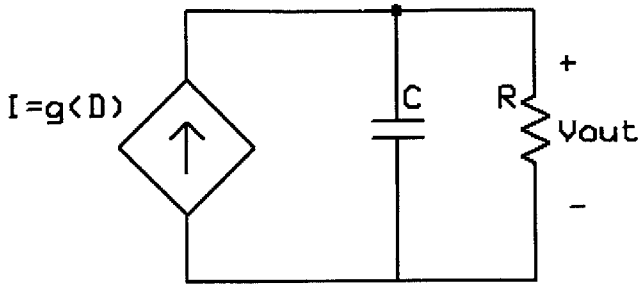

Figure 2-12. Averaged Model for Peak Current-Mode Control.

The complete set of transfer functions for the current-mode control case as derived in [1] are contained in (2.24)-(2.28).

$$H_i(s) = \frac{v_{out}(s)}{i_C(s)}$$

$$H_i(s) = \frac{F_m G_{vd}}{1 + F_m\left(G_{id} + F_v G_{vd}\right)} \tag{2.24}$$

$$H_{v-cm}(s) = \left.\frac{v_{out}(s)}{v_{in}(s)}\right|_{cm}$$

$$H_{v-cm}(s) = \frac{H_v - F_m F_g H_d + F_m\left(H_v G_{id} - G_{iv} H_d\right)}{1 + F_m\left(G_{id} - F_v H_d\right)} \tag{2.25}$$

The new variables introduced in (2.24) and (2.25) are defined for a buck converter as

$$F_g = \frac{D^2}{2Lf_s}$$

$$F_v = \frac{(1-2D)}{2Lf_s} \tag{2.26}$$

$$F_m = \frac{f_s}{M_a}$$

(2.24) and (2.25) can be normalized as shown in (2.27) and (2.28)

$$H_i(s) = \frac{G_{c0}}{\left(\frac{s}{\omega_c}\right)^2 + \frac{s}{Q_c\omega_c} + 1} \tag{2.27}$$

$$H_{v-cm}(s) = \frac{G_{g0}}{\left(\frac{s}{\omega_c}\right)^2 + \frac{s}{Q_c\omega_c} + 1} \tag{2.28}$$

where

$$G_{c0} = \frac{V}{D} \cdot \frac{F_m}{\frac{F_m F_v V}{D} + \frac{F_m V}{DR} + 1},$$

$$\omega_c = \frac{1}{\sqrt{LC}}\sqrt{\frac{F_m F_v V}{D} + \frac{F_m V}{DR} + 1},$$

$$Q_c = R\sqrt{\frac{C}{L}} \cdot \frac{\sqrt{\frac{F_m F_v V}{D} + \frac{F_m V}{DR} + 1}}{\frac{RCF_m V}{DL} + 1},$$

$$G_{g0} = D\frac{1 - \frac{F_m F_g V}{D^2}}{\frac{F_m F_v V}{D} + \frac{F_m V}{DR} + 1}.$$

Figure 2-13 shows the block diagram for a current-mode controller.

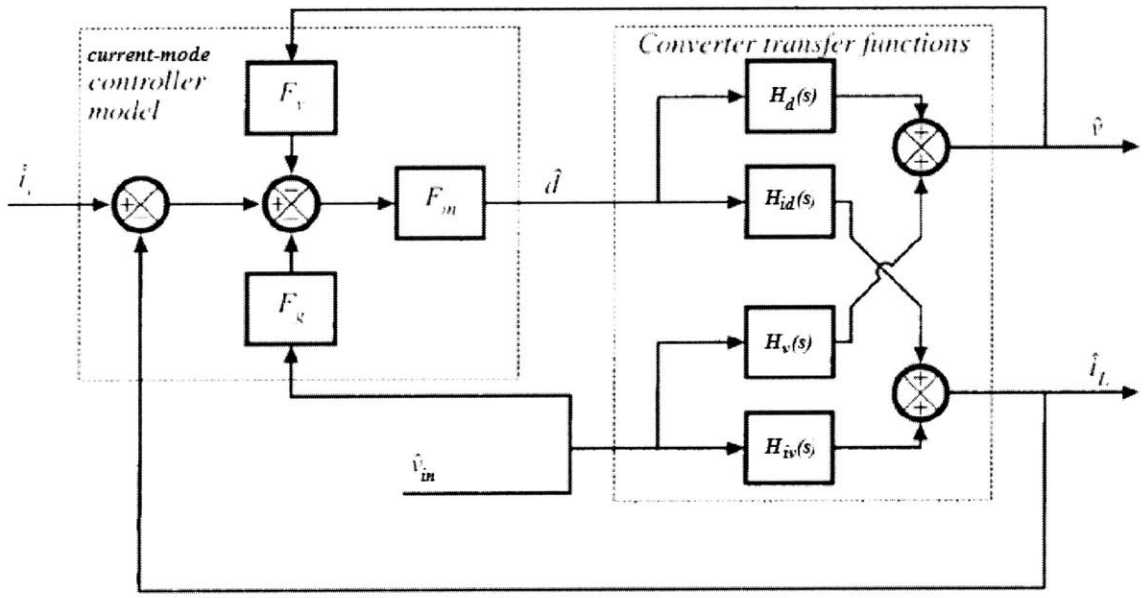

Figure 2-13. Block diagram for converter in current-mode control loop.

Compensation

An error amplifier must be designed to provide some compensation, G(s), to ensure that the overall system is stable. Stable is defined as bounded-input bounded-output (BIBO) stability, meaning any bounded input to the system produces a bounded output. It typically is not enough just to know that a system is stable. It is often critical to know how stable and how accurate the system is. Phase margin is used to indicate degree of stability. It is defined as the difference between the phase of the system and -180 degrees at the frequency when the magnitude response is equal to 1. This frequency is referred to as the crossover frequency. Generally, increasing the phase margin makes the system more stable. Given the phase margin, various stability criteria such as peak overshoot in the step response, rise time, settling time, and peaking in the frequency response magnitude can be determined. A system's response speed is measured in bandwidth. Higher crossover frequency corresponds to higher bandwidth. Steady-state error is used as a measure of the system's accuracy. Steady-state error is the difference between the command signal (for example, the reference voltage) and the feedback signal. This indicates how well the output is following the reference. Disturbance rejection refers to the system's ability to reject disturbances in the forward path. Good disturbance rejection is accomplished by introducing high gain in the loop transfer function at low frequencies. Noise rejection is a measure of the system's insensitivity to high frequency noise. Good noise rejection is obtained by significantly attenuating the magnitude of the loop transfer function at high frequencies. Refer to [3] for an introductory treatment of control theory.

There are numerous methods of compensation. The simplest is proportional control, meaning the compensator is just some constant gain: G(s) = K. Proportional control can be used to stabilize a system by increasing its phase margin, but the system's bandwidth is decreased. There is a tradeoff. Using proportional control, one can't be improved without degrading the other. Additionally, lowering the gain to stabilize a system decreases the disturbance rejection and increases the steady state error. Another option is dominant pole compensation, where the compensator introduces a low frequency pole to force crossover before the phase becomes too negative. This method also lowers the magnitude and decreases bandwidth. Depending on the application, speed may not matter and proportional or dominant pole compensation may be adequate.

Lag and Lead compensation are methods that provide a bit more flexibility than the ones previously mentioned. Lag compensation adds a low frequency pole followed by a zero. The zero counteracts the negative phase introduced by the pole. Lag compensators have transfer functions of the form

$$G(s) = \frac{\tau s + 1}{\alpha \tau s + 1}, (\alpha > 1). \tag{2.29}$$

This is often used to increase the low frequency gain (improving disturbance rejection and steady state error) without lowering the bandwidth or phase margin. If the lag pole is placed at the origin, it becomes proportional-plus-integral (PI) control. This integrator reduces the steady state error to zero in many applications. The drawback is that the error settling time may be significantly increased. Lead compensation adds a zero followed by a pole. The general transfer function is

$$G(s) = \frac{\alpha\tau s + 1}{\tau s + 1}, (\alpha > 1). \tag{2.30}$$

This results in a positive bump in phase (as opposed to the negative one caused by lag compensation) which can be used to increase phase margin if placed near crossover. Lead compensation isn't always desirable, however, because it increases the gain at high frequencies effectively degrading the noise rejection capabilities.

PI compensation will be used for the controller because disturbance rejection, noise rejection, and steady state error are very important for this application while the error settling time isn't as much of a concern. An op-amp implemention of PI control is shown in Figure 2-14. The transfer function for this compensator is

$$\frac{V_o}{V_i}(s) = -\frac{R_2 C s + 1}{R_1 C s}. \tag{2.31}$$

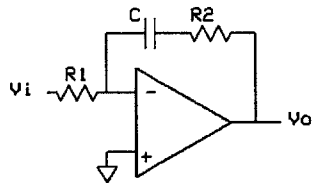

Figure 2-14. Schematic of a PI compensation circuit.

Slope Compensation

The converter will be unstable for duty cycles greater than 0.5 unless we implement slope compensation. The following derivation presented in [1] explains why.

Consider the steady-state inductor current waveform in Figure 2-15. For the first part of the period, the inductor current increases with slope m_1 until it is equal to the peak current value, I_{pk}. So we can calculate I_{pk} as

$$I_{pk} = i_L(dT) = i_L(0) + m_1 dT \tag{2.32}$$

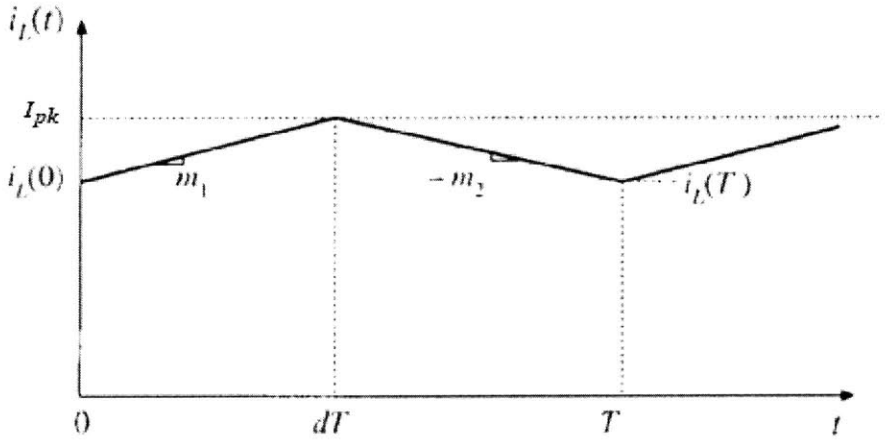

Figure 2-15. Steady-state inductor current.

Solving (2.32) for d gives us

$$d = \frac{I_{pk} - i_L(0)}{m_1 T} \tag{2.33}$$

During the second part of the period, the inductor current decreases with slope $-m_2$. We can calculate the current at the end of the period as

$$i_L(T) = i_L(dT) - m_2 d'T$$

$$= i_L(0) + m_1 dT - m_2 d'T \tag{2.34}$$

In steady-state operation, the following relations hold

$$i_L(0) = i_L(T)$$

$$d = D$$

$$m_1 = M_1$$

$$m_2 = M_2$$

Substituting these relations in (2.34) yields

$$0 = M_1 DT - M_2 D'T\,, \tag{2.35}$$

which can be rearranged as

$$\frac{M_2}{M_1} = \frac{D}{D'}. \tag{2.36}$$

Assume there is a small perturbation, $\hat{i}_L(0)$, in the inductor current. Figure 2-16 shows the inductor current waveforms in the case of steady-state and for a slight perturbation. The slopes of the waveforms are approximately the same. From Figure 2-16, we see that $\hat{i}_L(0)$ can be expressed as

$$\hat{i}_L(0) = -m_1 \hat{d}T \tag{2.37}$$

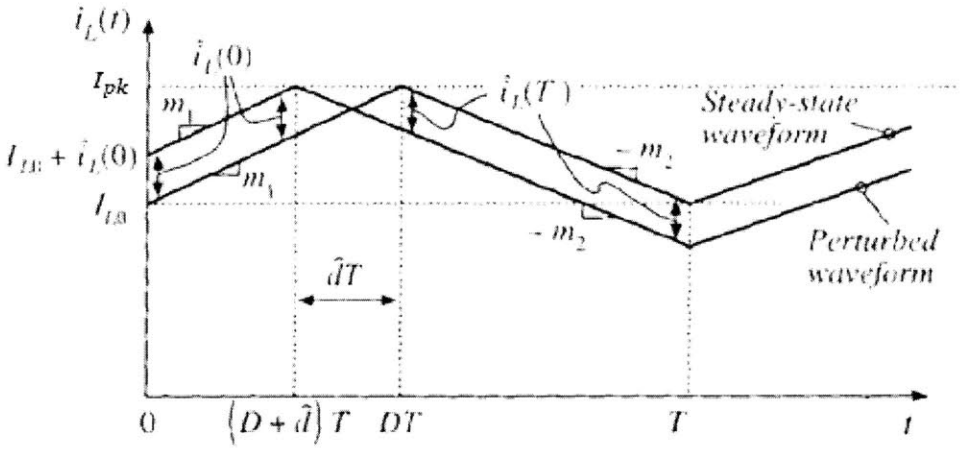

Figure 2-16. Inductor current in steady-state and with a slight perturbation.

Similarly, the perturbation from equilibrium at the end of the period can be expressed as

$$\hat{i}_L(T) = m_2 \hat{d}T \tag{2.38}$$

Combining (2.37) and (2.38) results in

$$\hat{i}_L(T) = \hat{i}_L(0)\left(-\frac{m_2}{m_1}\right) \tag{2.39a}$$

Or equivalently,

$$\hat{i}_L(T) = \hat{i}_L(0)\left(-\frac{D}{1-D}\right) \tag{2.39b}$$

We can calculate the perturbation at the end of the next period and so on. The perturbation after n periods is

$$\hat{i}_L(nT) = \hat{i}_L(0)\left(-\frac{D}{1-D}\right)^n \tag{2.40}$$

As n goes to infinity, the perturbation goes to zero if

$$\left|-\frac{D}{1-D}\right| < 1$$

or equivalently,

$$D < 0.5.$$

Otherwise, the perturbation increases without bound. This demonstrates that the converter is unstable for duty cycles greater than 0.5.

We can introduce a current ramp of slope m_a and sum it with the current sense waveform at the input of the PWM comparator. This causes the inductor current to ramp up during the first part of the period until the sum of the current ramp, i_a, and the inductor current reach the peak current, I_{pk}. This can be expressed mathematically as

$$i_L(dT) + i_a(dT) = I_{pk}, \tag{2.41}$$

or equivalently,

$$i_L(dT) = I_{pk} - i_a(dT) \tag{2.42}$$

This is shown graphically in Figure 2-17.

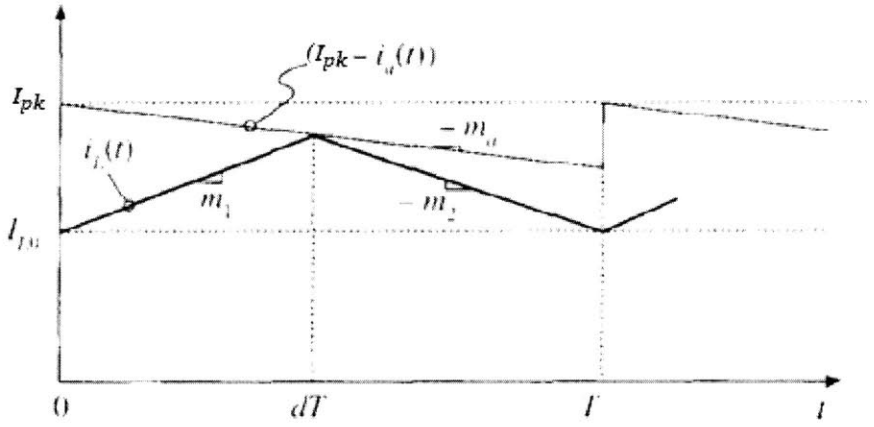

Figure 2-17. Inductor current in steady-state with slope compensation ramp.

Again, assume there is some perturbation, $\hat{i}_L(0)$, in the inductor current. Using the same approach as before, we can see from Figure 2-18 that the perturbation at the beginning of the period can be expressed as

$$\hat{i}_L(0) = -\hat{d}T(m_1 + m_a) \tag{2.43}$$

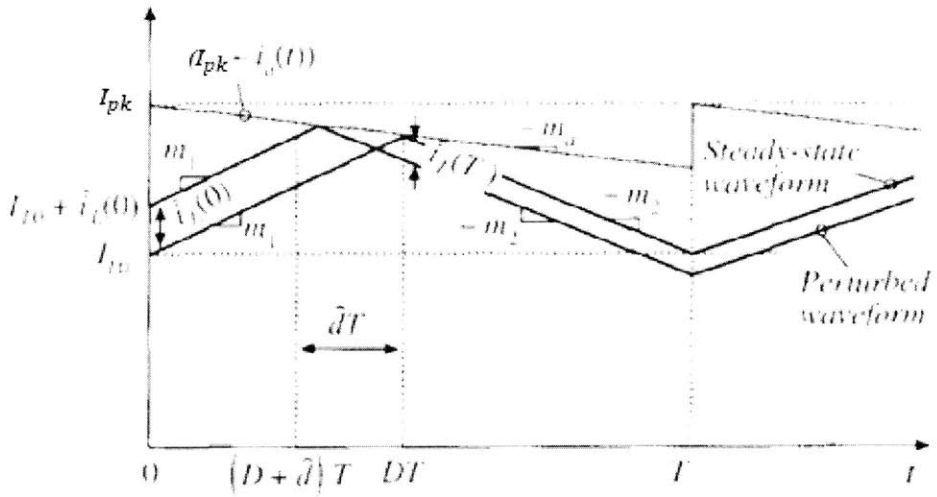

Figure 2-18. Steady-state and perturbed inductor current with slope compensation ramp.

and that at the end of the period as

$$\hat{i}_L(T) = -\hat{d}T(m_a - m_2) \tag{2.44}$$

Combining (2.43) and (2.44) results in

$$\hat{i}_L(T) = \hat{i}_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right) \tag{2.45}$$

After *n* periods, the perturbation becomes

$$\hat{i}_L(nT) = \hat{i}_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right)^n \tag{2.46}$$

As we can see from (2.46), the condition that must be satisfied to ensure that the perturbation goes to zero and the system is stable is

$$\left| -\frac{m_2 - m_a}{m_1 + m_a} \right| < 1 \tag{2.47}$$

Thus, for sufficiently large compensating ramp slope, m_a, the system will be stable for arbitrarily large D.

2.3 PWM Controller Using Commercial Integrated Circuits

The objective is to design our own PWM control chip transistor by transistor. We will first put together a control circuit using commercial operational amplifiers, comparators, and other ICs to help develop an understanding of how the circuit and each functional block operates. Then we will use transistors to design a circuit to replace each block. An existing current mode pulse width modulation control chip, Unitrode's UC3842, was used as a starting point and guide for the initial circuit design. See Figure 2-19 for a functional schematic of the UC3842. For additional information regarding the features and capabilities of the UC3842, refer to [4]. After reviewing the operation of this and similar control chips, we can determine some of the basic requirements for our PWM controller.

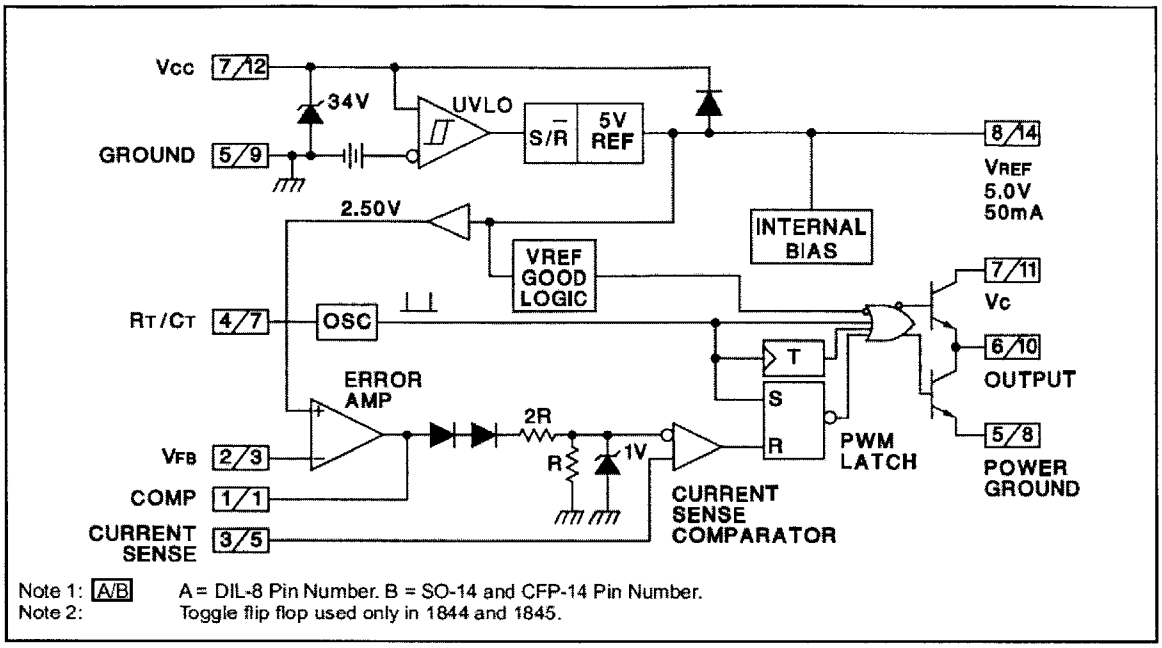

Figure 2-19. Functional Schematic of Unitrode's UC3842.

We need an internal voltage reference to which feedback from the converter's output can be compared to determine if the converter is being regulated properly. There must be an error amplifier to compute the error between the converter's output and the reference voltage and to provide some compensation to ensure that the loop is stable. For peak current mode control, we need an amplifier to sense and amplify the voltage across a current sense resistor placed in series with the high-side switch. A comparator is required to compare the current sense output to the level set by the error amplifier and signal when the current is too high. The converter and controller alternate between two states. In the first state, the high-side switch is on, the low-side switch is off, and the inductor current is ramping up. In the second state, the high side switch is off, the low-side switch is on, and the inductor current is ramping down. We need an RS latch to keep track of which state the system is in. The second state is triggered by a pulse from the PWM comparator indicating that the current has exceeded the threshold. An oscillator

circuit is needed to produce a pulse at the desired switching frequency. This pulse is used to initiate the first state. We must have delay circuitry to prevent shoot-through and a gate drive circuit is required to convert the 0-5V logic signal into a larger magnitude signal and source enough current to charge the capacitance associated with the MOSFETs' gates. Additionally, in order to operate the converter at duty cycles greater than 50%, we must provide some slope compensation to ensure stability. The remainder of this section briefly presents each block and an IC implementation of it. More detailed explanations of the blocks are given in Section 4.

We will assume a 12V supply is available to power our control circuitry. The circuit uses some logic ICs which require a 5V supply. This can be obtained from a linear voltage regulator, such as an LM7805. The desired output voltage for our converter is 5V. We can either directly use the 5V supply as a reference or we can use an op amp to create a 2.5V reference from the 5V supply. Figure 2-20 shows an LM7805 used to create a 5V supply and a possible op amp configuration for generating a 2.5V reference.

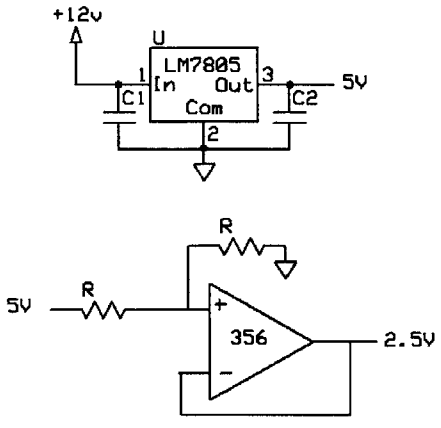

Figure 2-20. A linear regulator used to create 5V supply and op amp configured to generate 2.5V reference.

There are several options for the clock, or oscillator, circuit. We could use an LM555 timer, a 74LS123 or other one-shot chip, a Schmitt inverter, or one of numerous other options. Let's use a relaxation oscillator constructed with an LM311 comparator in a positive feedback configuration. The voltage across the capacitor will be used to generate our slope compensation ramp. The complete operation of the clock circuit is discussed in Section 4.4. See Figure 2-21 for a schematic.

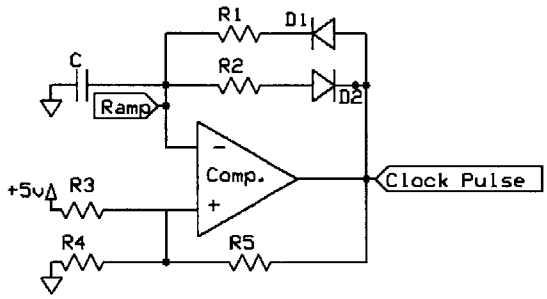

Figure 2-21. Relaxation oscillator used to generate clock pulse and slope compensation ramp.

An RS latch can be implemented with NOR gates, such as those contained in the 74LS02 chip. Having the outputs of a pair of NOR gates each tied to one input of the other creates a latching effect. Applying a high voltage to the other input of one of the NOR gates sets the outputs of the NOR gates such that one is high and the other is low. The high input voltage can then be removed, and the gate outputs will remain the same until the state of the latch is changed by the application of a high voltage to the other NOR gate's input. RS latch operation is explained more in Section 4.7. See Figure 2-22 for a schematic.

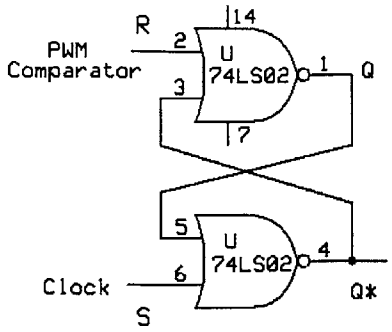

Figure 2-22. RS latch implemented with NOR gates.

For the current sense amplifier, we need a high speed op amp to amplify the voltage drop across the current sense resistor. General op-amps, such as the LM741 or LF356, are not fast enough for this application. Texas Instruments' TLC070 was found to be an appropriate selection. The op amp used for the current sense amplifier operates with a 12V supply. However, the inputs to the amplifier are approximately equal to the input voltage to the converter, which can be as high as 20V. With input voltages so high, transistors within the op amp become saturated and the amplifier no longer functions properly. The average of the two inputs to the op amp is called the common-mode input. The difference between the two inputs, which is what we'd like to amplify, is called the differential-mode input. We refer to the range of common-mode inputs over which the op amp functions properly (i.e. no transistors are saturated) as the common-mode range. This maximum common-mode input is typically a bit lower than the supply voltage. So we must reduce the maximum common-mode input from 20V to something below 12V. This can be accomplished with a resistive voltage divider. We must use high precision, well-matched resistors because any mismatch will affect the output of the amplifier and result in our circuit having poor common-mode rejection. See Figure 2-23 and Figure 2-24 for output waveforms from the current sense amplifier operating normally and when

its common-mode input range has been exceeded. Figure 2-25 contains the schematic of our current sense amplifier, a TLC070 configured as a differencing amplifier with a gain of 39.

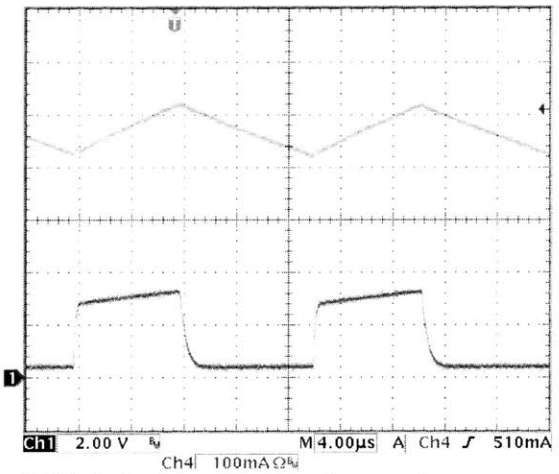

Figure 2-23. Inductor current and current sense waveform.

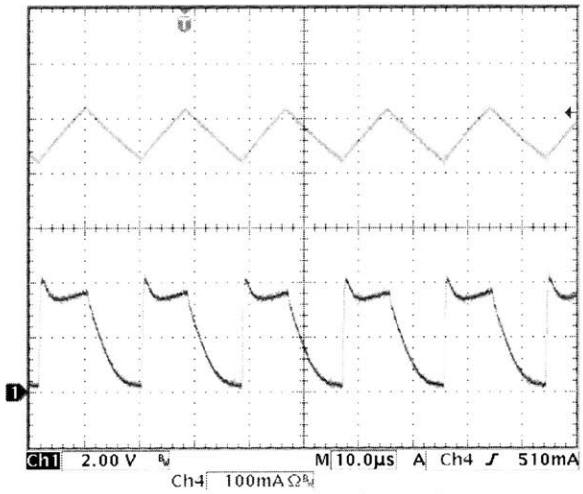

Figure 2-24. Inductor current and current sense waveform when common-mode input is too high.

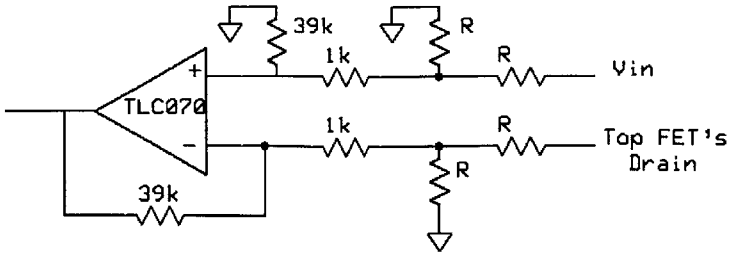

Figure 2-25. Current sense implemented with an op amp configured as a differencing amplifier with gain of about 39.

The delay can be an open-loop delay of a specified amount of time generated by a circuit such as the one shown in Figure 2-26. In this circuit, the delay is set by the time constant of the resistor and capacitor. Alternatively, we can implement a circuit that senses the gate to source voltage of one of the FETs and doesn't allow the other FET to be switched on until that voltage is below some threshold. This is a much safer implementation and makes it much more difficult for shoot-through to occur. An example circuit is contained in Figure 2-27.

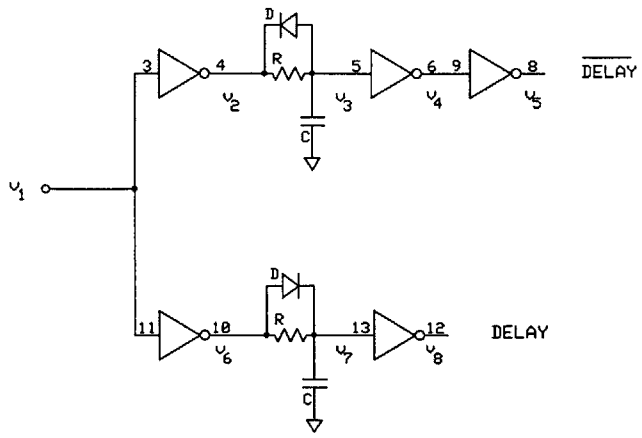

Figure 2-26. Open-loop implementation of delay for shoot-through protection.

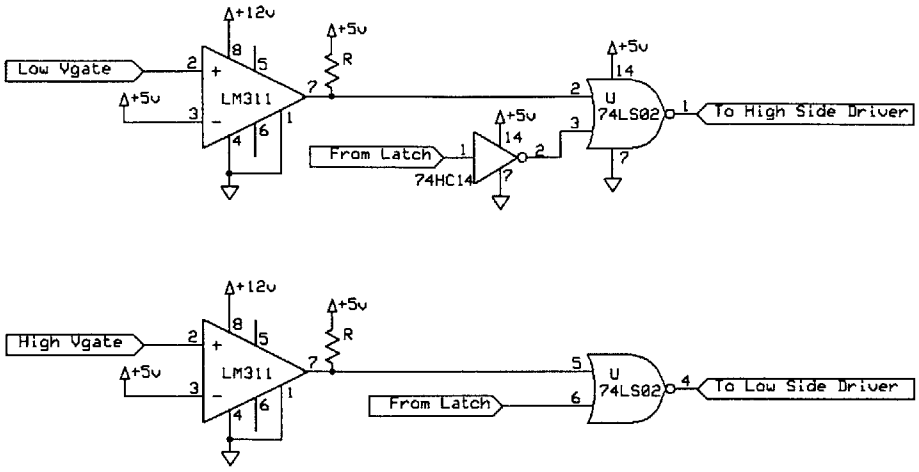

Figure 2-27. Shoot-through is prevented by making sure a FET is sufficiently off before the other FET is switched on.

We need a circuit to turn the MOSFETs on and off as instructed by the signals from the delay circuit. This can be accomplished with a gate driver, such as an IR2125. Figure 2-28 shows the typical connection of an IR2125 driving a low-side FET. Figure 2-29 shows an IR2125 configured to drive the high-side FET of a buck converter.

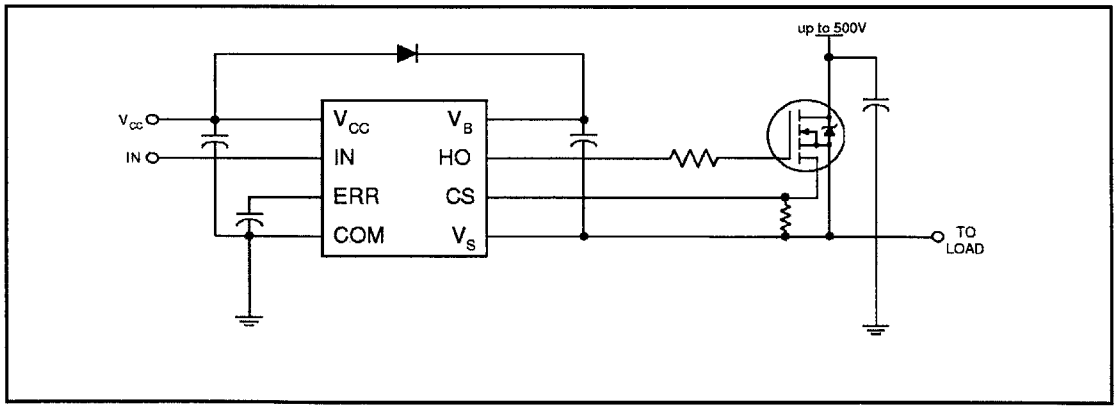

Figure 2-28. IR2125 gate driver used to drive low-side MOSFET.

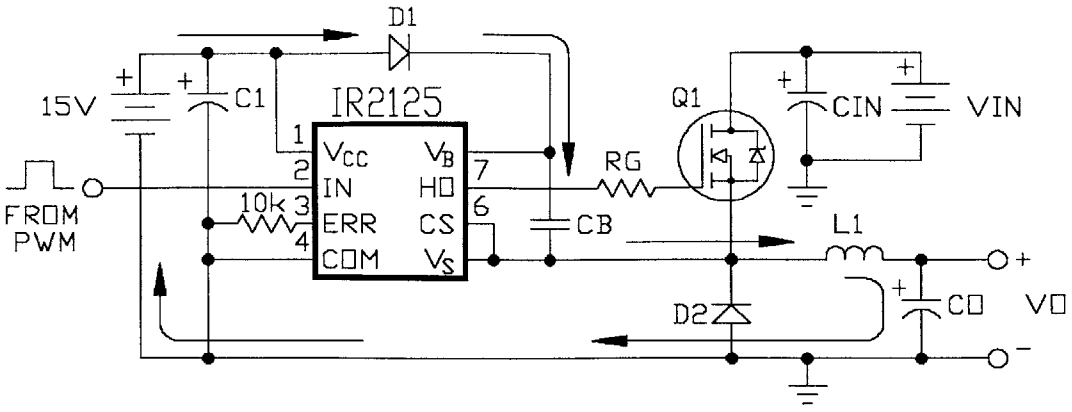

Figure 2-29. IR2125 gate driver used to drive high-side MOSFET.

The error amplifier is just a typical op-amp, such as an LF356, configured as shown in Figure 2-14 and the PWM comparator is implemented with an LM311. See the full control schematic in Figure 2-30.

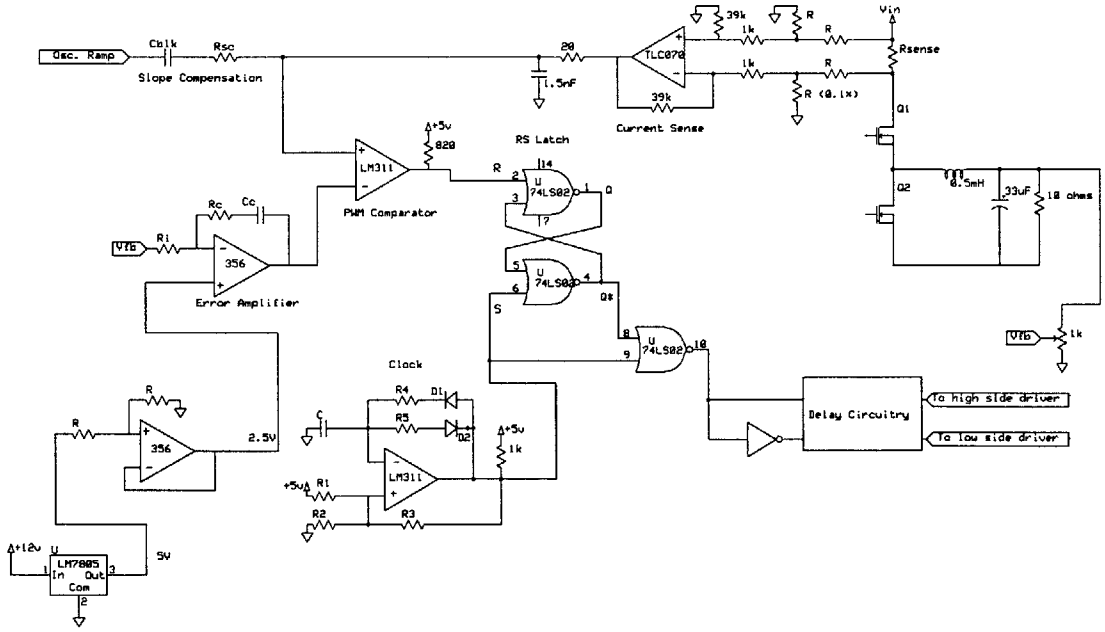

Figure 2-30. PWM peak current mode control circuit for a buck converter.

3 Analog Circuit Blocks

3.1 Current Sources

The collector current of a bipolar junction transistor can be described by (3.1).

$$i_C = I_S e^{v_{BE}/V_T}\left(1+\frac{v_{CE}}{V_A}\right) \tag{3.1}$$

The constant, I_S, depends on the physical device characteristics of the transistor. Collector current, i_C, increases exponentially with base-emitter voltage, v_{BE}. This means that a very slight change in v_{BE} causes a much larger change in i_C. It turns out that v_{BE} is approximately 0.6V over a wide range of typical collector currents. The collector current also depends on collector to emitter voltage, v_{CE}, through its ratio to the Early voltage, V_A. The Early voltage is generally much larger than v_{CE}, so we can assume that term will be negligible and ignore it in our calculations. The denominator of the exponent in (3.1) contains the thermal voltage, V_T. The thermal voltage is defined in (3.2) where k is Boltzmann's constant, q is the magnitude of an electron's charge, and T is temperature in kelvins. The value of V_T is about 26mV at room temperature.

$$V_T = \frac{kT}{q} \tag{3.2}$$

In addition to the relation in (3.1), collector current is also related to the base current, i_B, as indicated in (3.3). The current gain, β, is a very large constant that depends on the transistor's device parameters, and is typically on the order of 100, making collector current much larger than the base current. For an npn transistor, the current flowing out of the emitter is the sum of the currents flowing into the collector and base. Because β is

large, we can neglect base current and assume that the emitter current is approximately equal to the collector current.

$$i_C = \beta \cdot i_B \tag{3.3}$$

Current sources are a fundamental building block for analog circuits. They are used to ensure that transistors are biased into the correct region of operation and often they determine the amount of gain an amplifier has. An example of a single-transistor current source is given in Figure 3-1. The voltage at the base of the transistor is set by a voltage divider consisting of R_1 and R_2. The voltage at the emitter is v_{BE}, or about 0.6V, below that of the base, so the voltage across R_3 can be controlled by setting the voltage at the base. The voltage across R_3 then determines the current through R_3. The current through R_3 is approximately the same as Q's collector current which is the output of the current source. This current source requires a number of resistors whose values can potentially be fairly large. In an IC implementation, resistance is proportional to area so a current source like the one in Figure 3-1 would typically not be used. It is reasonable, however, for a discrete implementation where large resistors are readily available, particularly because it requires only one transistor.

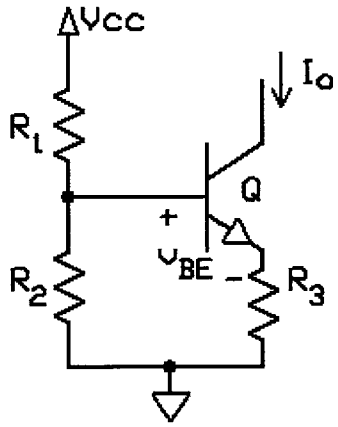

Figure 3-1. Single transistor current source.

A common way of creating a current source on ICs is a circuit called a current mirror. Some reference current, I_{ref}, is mirrored from a transistor to one or more other transistors, resulting in the current through those transistors being approximately equal to, or some scaled factor of, the reference current. A simple current mirror is shown in Figure 3-2. The reference current flows into the diode connected (meaning base and collector tied together) transistor Q_1. Some of the reference current, i_A, does not contribute to the collector current of Q_1, but instead provides current to the two bases.

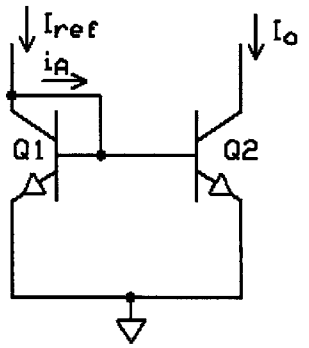

Figure 3-2. Simple current mirror.

Since β is very large, this current is only a small fraction of the collector current. Thus, we will assume that the base currents are negligible and I_{ref} flows entirely into the collector of Q_1. Assuming that Q_1 and Q_2 are well matched, the current, Io, flowing through Q_2 is approximately equal to the reference current flowing through Q_1 because their base-emitter voltages are the same. Additional transistors may be added with their bases and emitters also connected to those of Q_1 and Q_2 and the reference will be mirrored to them as well. As the number of transistors increases, however, the base current being drawn from I_{ref} increases and is no longer negligible. In this case, the collector current of Q_1 can no longer be approximated as I_{ref}. The current, i_A, being drawn by the bases must be calculated and subtracted from I_{ref} to determine the collector current of Q_1 that is being mirrored to the other transistors. The voltage at the collector-base terminal of Q1 is about 0.6V. One way of generating the reference current is to connect a resistor from there to a voltage source, as shown in Figure 3-3. The current I_{ref} is then defined by (3.4).

$$I_{ref} = \frac{V_{CC} - 0.6V}{R_r} \tag{3.4}$$

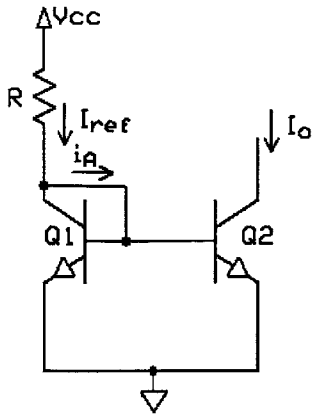

Figure 3-3. Simple current mirror with reference current set by the voltage across R.

The current mirror in Figure 3-2 is only accurate for well matched transistors. Any slight mismatch between the transistors means that they will have different values of I_S so applying (3.1) we see that their collector currents will not be identical even though they have the same v_{BE}. Additionally, collector current has significant temperature dependence. The variables I_S, v_{BE}, and v_T all vary with temperature. So unless the transistors are at the same temperature, which is difficult to ensure with discrete components in separate packages, the collector currents will differ. In some cases, temperature mismatches can lead to a thermal runaway situation. The current flowing through a transistor causes its temperature to increase. The increase in temperature leads to a further increase in current which causes temperature to increase even more. The matching and thermal stability issues can be addressed by adding resistors to the emitters as shown in Figure 3-4. The emitter resistors provide negative feedback which provides some stability to counteract thermal runaway. When the collector current of Q_2 increases, the current through R_2 goes up as well. This means the voltage drop across R_2, and thus the voltage at the emitter of Q_2, also increases. The voltage at the bases of the transistors is held constant because the collector current of Q_1 (and as a result, its v_{BE}) is

unchanged. So the increase in the emitter voltage of Q_2 results in a decrease in v_{BE2} which causes I_{C2} to decrease. Thus R_2 is providing negative feedback which counteracts an increase in I_{C2}. Doing KVL around the emitter resistor and v_{BE} loop of the circuit yields

$$v_{R1} + v_{BE1} = v_{BE2} + v_{R2}.$$

Substituting the results of applying Ohm's law and solving (3.1) for v_{BE} we get

$$i_{C1}R_1 + V_T \ln\left(\frac{i_{C1}}{I_{S1}}\right) = V_T \ln\left(\frac{i_{C2}}{I_{S2}}\right) + i_{C2}R_2.$$

Solving for $i_{C2}R_2$ yields

$$i_{C2}R_2 = i_{C1}R_1 + V_T \ln\left(\frac{i_{C1}}{I_{S1}}\right) - V_T \ln\left(\frac{i_{C2}}{I_{S2}}\right).$$

We can combine the two natural log terms to obtain

$$i_{C2}R_2 = i_{C1}R_1 + V_T \ln\left(\frac{i_{C1}}{I_{S1}} \cdot \frac{I_{S2}}{i_{C2}}\right).$$

Dividing both sides by R_2 gives us the output of the current mirror

$$i_{C2} = i_{C1}\frac{R_1}{R_2} + \frac{V_T}{R_2} \ln\left(\frac{i_{C1}}{I_{S1}} \cdot \frac{I_{S2}}{i_{C2}}\right). \tag{3.5a}$$

Assuming Q_1 and Q_2 are matched, $I_{S1} = I_{S2}$ and (3.5a) reduces to

$$i_{C2} = i_{C1}\frac{R_1}{R_2} + \frac{V_T}{R_2} \ln\left(\frac{i_{C1}}{i_{C2}}\right). \tag{3.5b}$$

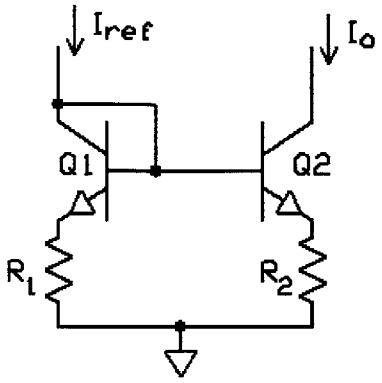

Figure 3-4. Current mirror with emitter resistors to improve accuracy and temperature stability.

The equation in (3.5a) shows that if there are not extreme differences between the I_S and I_C values of the two transistors and if the voltage drops across the emitter resistors are much larger than V_T, the natural log term is negligible and (3.5a) can be simplified to

$$i_{C2} = i_{C1}\frac{R_1}{R_2}. \tag{3.6}$$

So, by adding emitter resistors and ensuring that the voltage drop across them is much larger than 26mV, we've gained stability against thermal runaway and the relationship between the output current and the reference current now depends primarily on the ratio of R_1 to R_2, regardless of how well matched the transistors are. Setting R_1=R_2 mirrors the reference current to the output, but we also have the additional flexibility of choosing R_1 not equal to R_2 and having an output current different from the reference current by some predetermined factor.

In the current source circuits we've discussed thus far, the goal was to generate a constant current of some value that had little variation with changes in transistor device parameters or temperature. There are some situations in which we actually want a current that increases predictably with temperature. These are known as proportional-to-absolute-temperature (PTAT) current sources. Consider the circuit in Figure 3-5. Applying KVL to the lower loop yields

$$v_{BE1} = v_{BE2} + v_R \approx v_{BE2} + i_{C2}R$$

which implies that

$$\Delta v_{BE} = v_{BE1} - v_{BE2} = i_{C2}R.$$

Solving (3.1) for v_{BE} and substituting yields

$$V_T \ln\left(\frac{i_{C1}}{I_{S1}}\right) - V_T \ln\left(\frac{i_{C2}}{I_{S2}}\right) = i_{C2}R.$$

We can combine the two natural log terms to obtain

$$V_T \ln\left(\frac{i_{C1}}{I_{S1}} \cdot \frac{I_{S2}}{i_{C2}}\right) = i_{C2}R.$$

Substituting (3.2) for V_T yields

$$\left(\frac{kT}{q}\right) \cdot \ln\left(\frac{i_{C1}}{I_{S1}} \cdot \frac{I_{S2}}{i_{C2}}\right) = i_{C2}R.$$

The output current is then expressed as

$$i_{C2} = \frac{1}{R} \cdot \left(\frac{kT}{q}\right) \cdot \ln\left(\frac{i_{C1}}{I_{S1}} \cdot \frac{I_{S2}}{i_{C2}}\right). \tag{3.7}$$

This derivation shows that the voltage across (and current through) R is directly proportional to temperature, assuming that the natural log term can be held relatively constant. Because β is large, i_{C2} is approximately equal to the current through R and so is also PTAT. In general, the difference between two base-emitter voltages is PTAT.

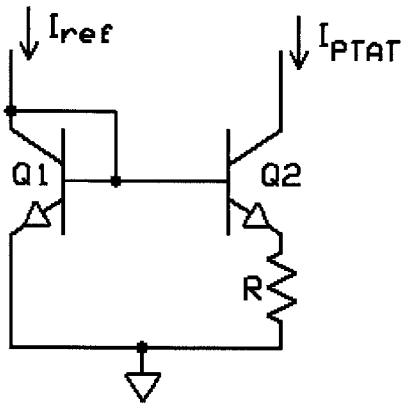

Figure 3-5. Basic PTAT current generator.

Figure 3-6 contains an implementation of a PTAT current source. The current mirror formed by Q_3 and Q_4 keeps the collector currents of Q_1 and Q_2 the same. So I_{C1} and I_{C2} cancel each other in the natural log term of (3.7). By connecting two transistors in parallel to serve as Q_2, we have doubled the area of Q_2 which means that I_{S2} is now twice as large as I_{S1} (assuming the three transistors are well matched) so (3.7) simplifies to

$$i_{C2} = \frac{1}{R} \cdot \left(\frac{kT}{q} \right) \cdot \ln(2).$$

So i_{C2} and i_{C1} are PTAT, as desired. Connecting these two transistors in parallel is analogous to how transistor areas are scaled in an integrated circuit. In order to extract this PTAT current, Q_5 is connected as shown in Figure 3-6 so that the current is mirrored there as well. The collector current of Q_5 is our PTAT output current. This current can now be applied directly to a circuit or it can be converted to a PTAT voltage via a resistor. The output current is determined by the ratio of Q_1 and Q_2's areas. By varying R and the number of transistors connected in parallel to form Q_1 or Q_2, we can control the value of I_{PTAT}.

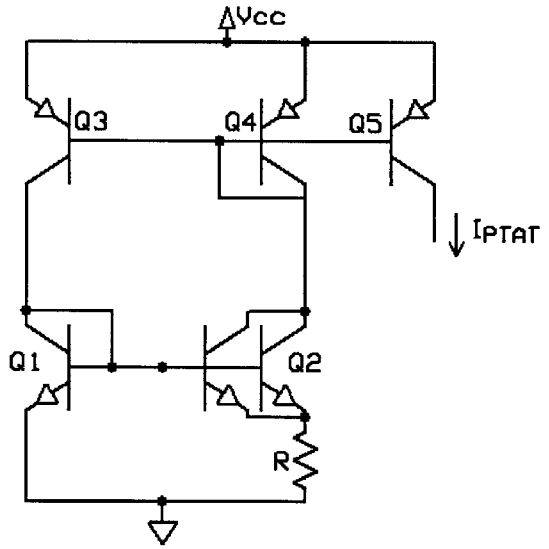

Figure 3-6. Implementation of a PTAT current source.

3.2 Common Emitter Amplifier

One widely used analog circuit building block is the common emitter (CE) amplifier. The basic CE amplifier consists of a single transistor configured as shown in

Figure 3-7. The input signal is applied across the base-emitter junction and the output is taken from the collector. We replace the transistor with its small signal model to determine the characteristics of the circuit. An equivalent circuit for analysis is shown in Figure 3-8. For a derivation of the small-signal model for a bipolar junction transistor, refer to [5].

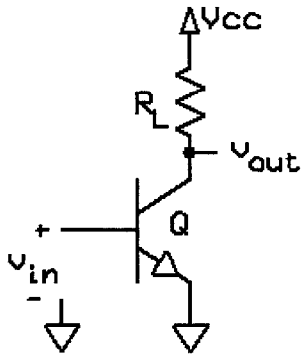

Figure 3-7. Common emitter amplifier schematic.

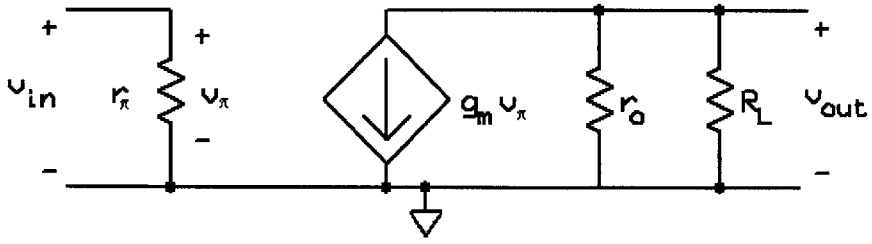

Figure 3-8. Small signal model for common emitter amplifier.

Assume a small signal input, v_{in}, is applied as shown. The input shows up across r_π, thus $v_\pi = v_{in}$. The value of the dependent current source is then $g_m v_{in}$. By applying KCL at the output node, we can see that $-g_m v_{in}$ flows through the parallel combination of

r_o and R_L. Assuming r_o is much larger than R_L, r_o can be neglected. Thus the output voltage is

$$v_{out} = -g_m v_{in} \cdot (R_L \| r_o)$$

$$\approx -g_m v_{in} \cdot R_L$$

The gain of the circuit is then

$$a_v = \frac{v_{out}}{v_{in}} \approx -g_m \cdot R_L \tag{3.8}$$

Input resistance is the resistance seen looking into the input terminal of the amplifier. It is the resistance seen by the output of some previous stage or some input source that may drive this circuit. The input resistance is defined as

$$R_{in} = \frac{v_{in}}{i_{in}}. \tag{3.9}$$

For the CE amplifier, $R_{in}=r_\pi$. Analogous to input resistance, output resistance is the resistance seen looking into the circuit from the output terminal. The formal definition is

$$R_{out} = \left.\frac{v_{out}}{i_{out}}\right|_{v_{in}=0}. \tag{3.10}$$

In this case, setting v_{in} to 0 turns off the dependent current source, making it an open circuit. The resistance seen from the output is then the parallel combination of r_o and the load resistance, R_L. For cases where R_L is much smaller than r_o, R_{out} is simply R_L.

3.3 Emitter Follower Buffer

Another useful analog block is the common collector (CC) or emitter follower (EF) configuration. This circuit, depicted in Figure 3-9, consists of a single transistor with an input voltage applied at the base and output taken at the emitter. The equivalent small signal circuit, shown in Figure 3-10, can be analyzed to determine the characteristics of the EF.

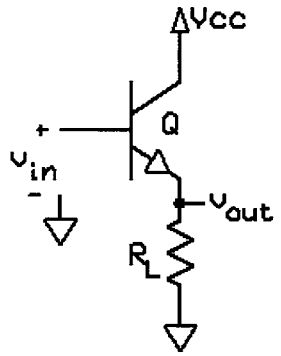

Figure 3-9. Emitter follower schematic.

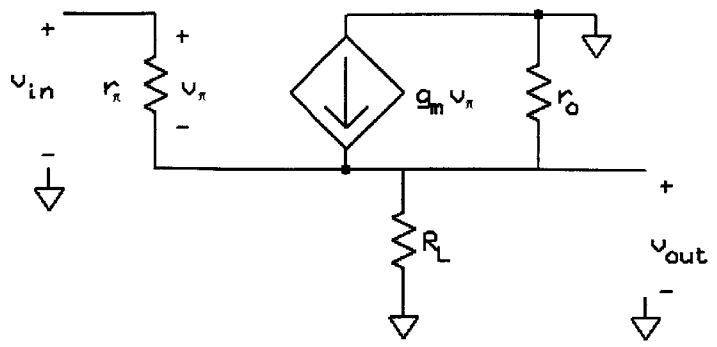

Figure 3-10. Small signal model for emitter follower.

Applying KCL at the output node yields

$$i_{in} + \beta_0 i_{in} + \frac{0V - v_{out}}{r_o} - \frac{v_{out} - 0V}{R_L} = 0 \quad \text{(because } g_m v_\pi = \beta_0 i_{in}\text{)}.$$

Substituting for i_{in} results in

$$\frac{v_{in} - v_{out}}{r_\pi} + \beta_o\left(\frac{v_{in} - v_{out}}{r_\pi}\right) - \frac{v_{out}}{r_o} - \frac{v_{out}}{R_L} = 0.$$

Upon simplification we get

$$\frac{v_{out}}{v_{in}} = \frac{1}{1 + \dfrac{r_\pi}{(\beta_0 + 1)(r_o \| R_L)}} \tag{3.11a}$$

Assuming $\beta_0 >> 1$ and $r_o >> R_L$, we can use the relation $r_\pi = \dfrac{\beta_0}{g_m}$ to obtain

$$\frac{v_{out}}{v_{in}} \approx \frac{g_m R_L}{1 + g_m R_L}. \tag{3.11b}$$

The gain of the EF is less than 1. It turns out that, due to the transistor's factor of β current gain, any resistance connected to the emitter seems larger by a factor of β+1 when viewed from the base of the transistor. Likewise, when looking into the emitter, r_π and any resistance connected to the base seem smaller by a factor of β+1. See [ ] for a derivation of this. Using this information, we can determine R_{in} and R_{out} without too much hassle, as indicated by (3.12). Otherwise we would have to apply a test input source and analyze the circuit to determine the ratio of the input and output voltages and currents.

$$\begin{aligned} R_{in} &= r_\pi + (\beta_0 + 1)(r_o \| R_L) \\ &\approx r_\pi + (\beta_0 + 1) R_L \end{aligned} \tag{3.12a}$$

$$R_{out} = r_o \left\| R_L \right\| \frac{r_\pi}{\beta_0 + 1}$$

Because r_o is very large,

$$\begin{aligned} R_{out} &\approx R_L \left\| \frac{r_\pi}{\beta_0 + 1} \right. \\ R_{out} &\approx R_L \left\| \frac{1}{g_m} \right. \end{aligned} \tag{3.12b}$$

When $\beta_0 >> 1$, $r_o >> R_L$, and $g_m R_L >> 1$, the gain of the emitter follower is approximately 1. This unity gain and the fact that the amplifier reduces the effective

output resistance and increases the effective input resistance seen by adjacent stages by a factor of β+1 make the EF amplifier a good buffer to use before, between, and after other stages.

3.4 Differential Pair

We often need to take some differential voltage as input and amplify it. This can be done with the differential pair circuit block shown in Figure 3-11. Assume a differential voltage, v_d, is applied across the input terminals. We model this as $+\frac{1}{2}v_d$ applied to the base of Q_1 and $-\frac{1}{2}v_d$ applied to the base of Q_2 as indicated in Figure 3-11. The change in collector current for a given change in v_{BE} can be calculated as follows: Ignoring the Early effect, (3.1) becomes

$$i_C = I_S e^{v_{BE}/V_T}. \tag{3.13}$$

We differentiate (3.13) with respect to v_{BE} to obtain

$$\frac{\partial i_C}{\partial v_{BE}} = \frac{1}{V_T} \cdot I_S e^{v_{BE}/V_T}.$$

This expression is equivalent to

$$\frac{\partial i_C}{\partial v_{BE}} = \frac{i_C}{V_T}$$

$$= \frac{I_C}{V_T} \quad \text{(when evaluated at the DC operating point).}$$

So we can see that

$$\frac{\partial i_C}{\partial v_{BE}} = \frac{I_C}{V_T} \equiv g_m . \tag{3.14}$$

The change in collector current for a given change in v_{BE} is known as the transconductance and is typically associated with the variable g_m. (3.14) can be used to determine what the change in i_{C1} and i_{C2} will be as a result of the applied differential input voltage. The expression in (3.14) implies

$$\Delta i_C = g_m \cdot \Delta v_{BE} . \tag{3.15}$$

So the change in i_{C1} will be $g_m \cdot \left(+\frac{1}{2} v_d \right)$ and the change in i_{C2} will be $g_m \cdot \left(-\frac{1}{2} v_d \right)$.

These currents flow through the load resistors. To obtain a differential voltage output, we can take the difference between the voltages at the two collectors, indicated as v_{od} in Figure 3-11. The change in voltage at the collectors in response to the change in i_C is $-\Delta i_C \cdot R_L$. So at the collector of Q_1 we get

$$v_{o1} = -\Delta i_{C1} \cdot R_L .$$

Substituting for Δi_C yields

$$v_{o1} = -g_m \cdot \frac{v_d}{2} \cdot R_L \tag{3.16a}$$

At the collector of Q_2 we get

$$v_{o2} = -\Delta i_{C2} \cdot R_L .$$

Again, substituting for Δi_C yields

$$v_{o2} = -g_m \cdot \left(-\frac{v_d}{2}\right) \cdot R_L$$
$$v_{o2} = g_m \cdot \frac{v_d}{2} \cdot R_L \tag{3.16b}$$

The differential output voltage in response to v_d is

$$v_{od} = v_{o1} - v_{o2}.$$

Substituting the results from (3.16) yields

$$v_{od} = -g_m \cdot \frac{v_d}{2} \cdot R_L - g_m \cdot \frac{v_d}{2} \cdot R_L$$

which can be simplified to

$$v_{od} = -g_m \cdot v_d \cdot R_L. \tag{3.17}$$

The gain of the differential amplifier is

$$a_v = \frac{v_{od}}{v_d} = -g_m \cdot R_L. \tag{3.18a}$$

If we were to define the differential output voltage as $v_{od} = v_{o2} - v_{o1}$, the amplifier would be non-inverting and the gain would be

$$a_v = \frac{v_{od}}{v_d} = g_m \cdot R_L. \tag{3.18b}$$

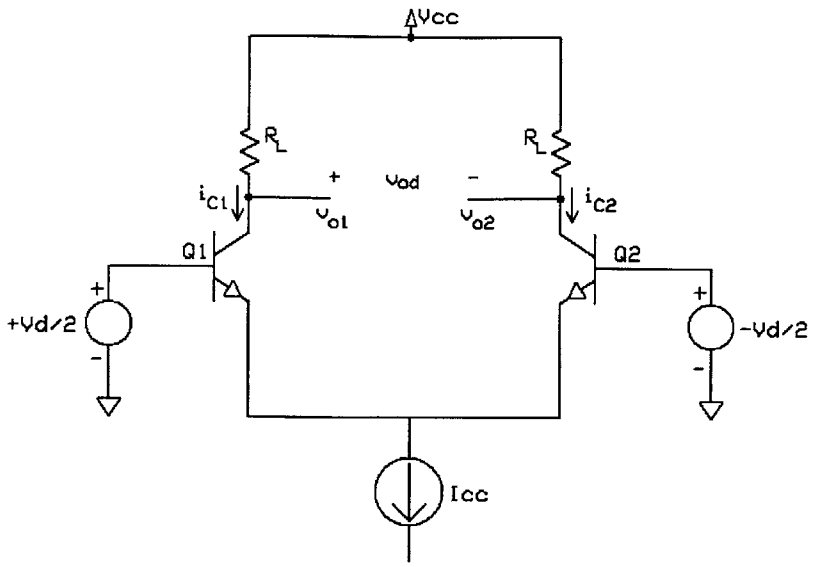

Figure 3-11. Differential pair amplifier schematic.

If, instead of a differential output voltage, we wanted a single-ended output voltage referenced to ground, we could take either v_{o1} or v_{o2} as our output. A single-ended output is advantageous because it is referenced to ground, however the gain is reduced by a factor of 2. For instance, with v_{o1} taken to be the output

$$a_v = \frac{v_{o1}}{v_d} = -\frac{1}{2} \cdot g_m \cdot R_L . \tag{3.19}$$

From the gain expressions derived above, we can see that the gain of the differential pair is proportional to the bias current (through g_m) and the load resistance. Because power dissipation is proportional to current, it is not ideal to use large bias currents to increase the gain. Large resistors are impractical for integrated circuits because resistance is proportional to area and a primary objective in integrated designs is

to minimize size. The solution is to use transistors, instead of resistors, to load the differential pair. This configuration, known as an actively loaded differential pair, is shown in Figure 3-12. The small signal model for the bipolar junction transistor includes an output resistance, designated by r_o. This is the resistance seen looking into the collector of the transistor. The output resistance is proportional to the Early voltage, V_A, and is typically very large.

$$r_o = \frac{V_A}{I_C}. \tag{3.20}$$

The effective resistance seen at the output node is

$$R_{L,eff} = r_{o2} \parallel r_{o4},$$

which becomes

$$= \frac{V_{An}}{I_{C2}} \left\| \frac{V_{Ap}}{I_{C4}} \right.$$

upon substitution of (3.20).

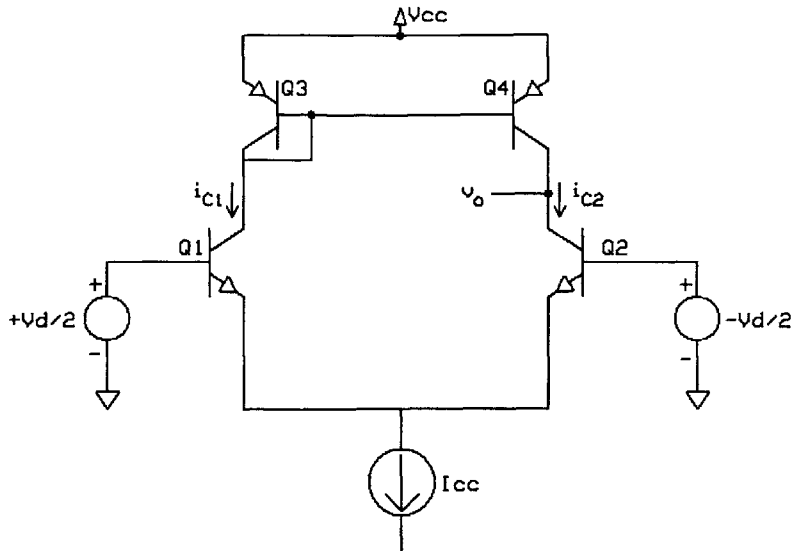

Figure 3-12. Actively loaded differential pair amplifier.

Note that the early voltages for npn and pnp transistors are different. V_A is typically significantly larger for npn transistors. The increased resistance seen at the output node significantly increases the amount of gain the circuit can provide. In the case of the resistively loaded differential pair, the effective load resistance seen at the collectors is actually R_L in parallel with the transistor's r_o. However, because r_o is so much larger than R_L, we were able to ignore it in the previous calculations. The actively loaded differential pair provides a significant increase in gain, but this circuit is only useful when a single-ended output is desired because we can only take the output from the collector of Q_2 as opposed to in the resistively loaded case where we could take a differential output voltage.

Figure 3-13 contains a graph of the v_{od} versus v_d transfer characteristic for a differential pair amplifier. The circuit only amplifies linearly over a small range, about $\pm 25mV$, of differential input voltages. Beyond this range, all of the bias current is flowing through either Q_1 or Q_2 so a further increase in the magnitude of v_d doesn't

change the collector currents or output voltage. Emitter resistors can be added to the input transistors, illustrated in Figure 3-14, to widen the linear range of the amplifier. For a factor of m increase in linear range, set $\frac{1}{2}R_E I_{CC}$ equal to mV_T. Figure 3-15 shows the v_{od} versus v_d transfer characteristic for the case where $\frac{1}{2}R_E I_{CC}$ is about $20V_T$. Upon examining the slope of the curve in Figure 3-15, we can see that the gain of the circuit is reduced by approximately the same factor by which the linear range is increased. The following calculations show that the gain is approximately the ratio of R_L to R_E if we take the output voltage differentially.

Increasing linear range by *m*

$$\frac{1}{2}R_E I_{CC} = mV_T, \tag{3.21}$$

implies a reduction of the gain by a factor of *m* yielding

$$a_v \approx \frac{1}{m} g_m R_L .$$

Substituting the results of (3.21) and the expression for gm gives us

$$a_v = \left(\frac{V_T}{\frac{1}{2}R_E I_{CC}} \right) \cdot \left(\frac{\frac{1}{2}I_{CC}}{V_T} \right) \cdot R_L \tag{3.21}$$

which simplifies to

$$a_v = \frac{R_L}{R_E}$$

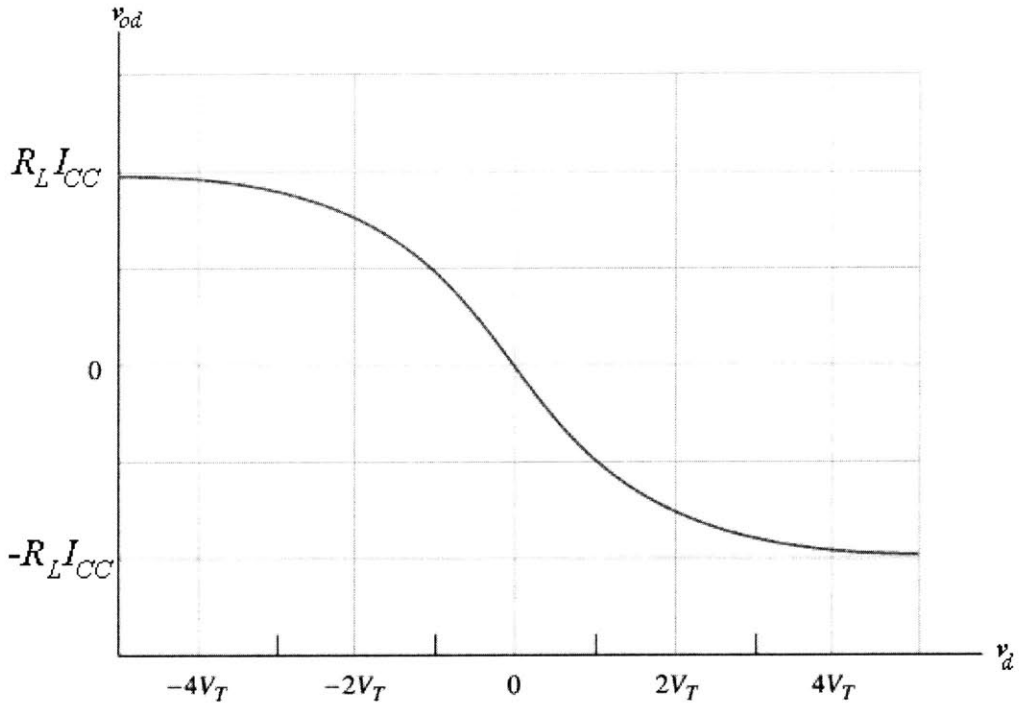

Figure 3-13. Transfer characteristic of vod vs. vd for differential pair amplifier.

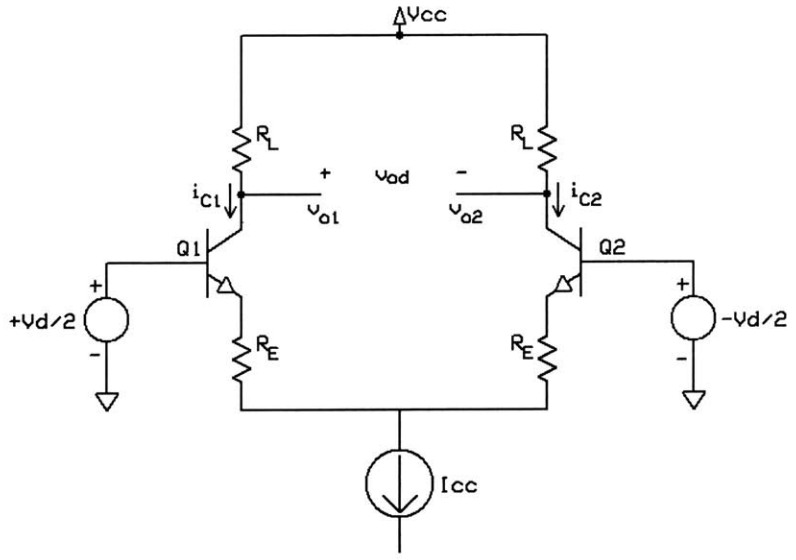

Figure 3-14. Schematic of differential pair amplifier with emitter resistors to increase linear range.

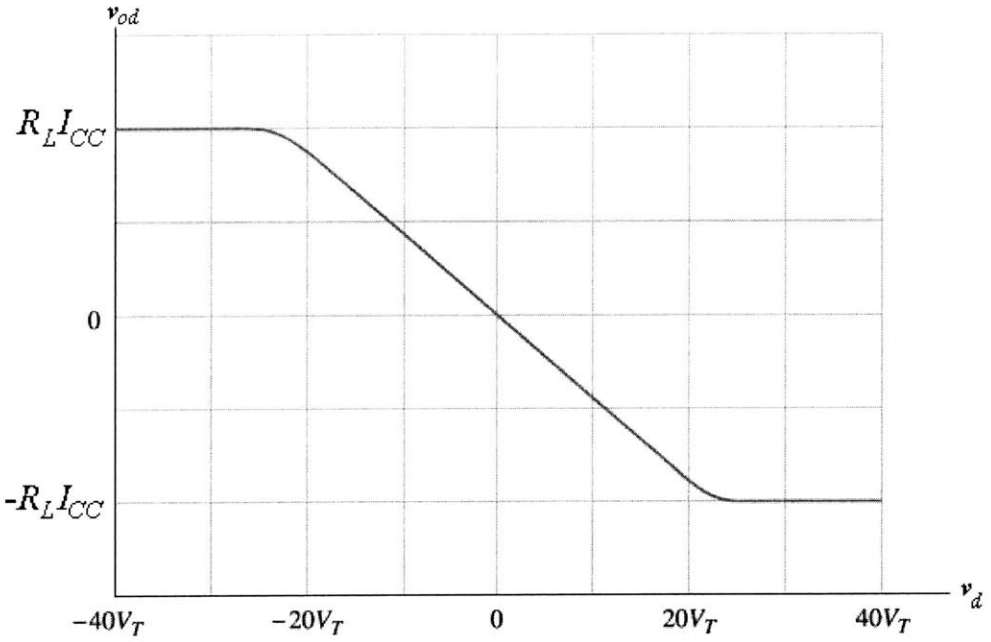

Figure 3-15. characteristic of vod vs. vd for differential pair amplifier with emitter resistors.

The gain of the differential pair, as indicated earlier, is proportional to g_m. Because the expression for g_m contains V_T in its denominator, the circuit gain is inversely proportional to temperature. This temperature dependence may be undesirable. If the gain needs to be relatively independent of temperature, we need to introduce a factor that is directly proportional to temperature to cancel the inverse temperature dependence of g_m. This can be accomplished by using a PTAT current source for I_{CC}, such as the one discussed in Section 3.1. If the bias current, I_{CC}, is proportional to temperature by some factor, A, g_m can be calculated as follows.

$$I_{CC} = A \cdot T$$

The collector currents are

$$I_{C1} = I_{C2} = I_C = \frac{1}{2} A \cdot T .$$

From (3.14)

$$g_m = \frac{I_C}{V_T}$$

Substituting for I_C and V_T yields

$$g_m = \frac{\frac{1}{2} A \cdot T}{\frac{kT}{q}}.$$

which can be reduced to

$$g_m = \frac{A \cdot q}{2k}.$$

As a result of the PTAT current source, g_m (and so the gain of the amplifier) is no longer temperature dependent.

The differential pair is a typical input stage for an amplifier and can be followed by additional gain stages and an output stage to construct an operational amplifier. See Figure 3-16 for an example.

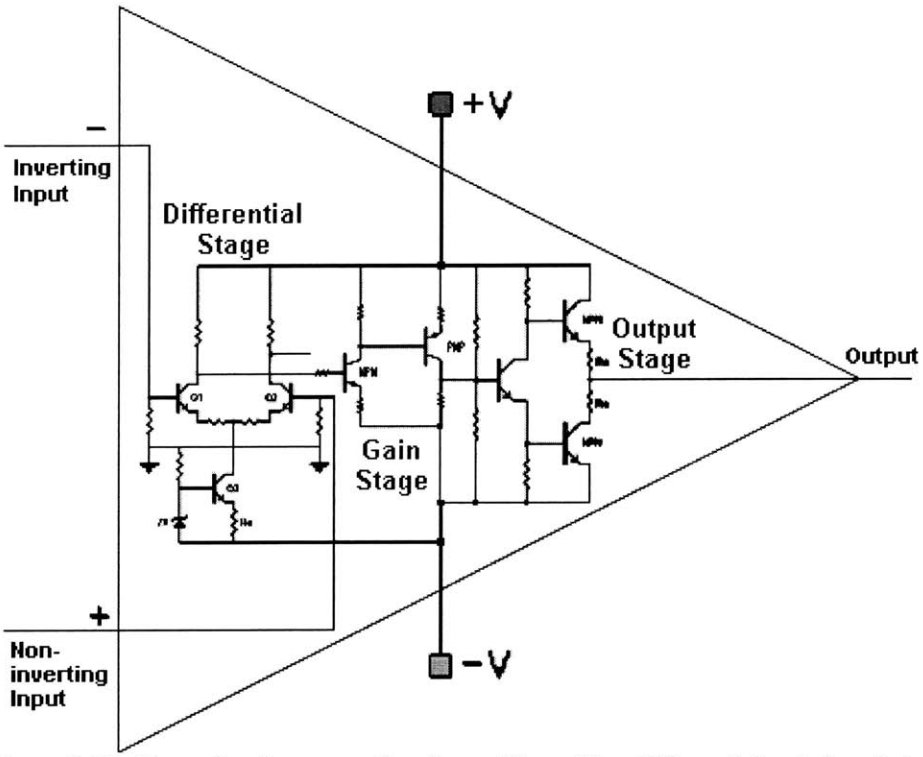

Figure 3-16. Example of an operational amplifier with a differential pair input stage.

4 Control Circuit Blocks

4.1 Bandgap Reference

In order to regulate output voltage, there must be some internal, reliable point of reference. Ideally, there should be a voltage reference that is stable across variations in temperature and supply voltage. The voltage across the base emitter junction of bipolar junction transistors has a negative temperature coefficient, meaning the voltage decreases as temperature increases. Bandgap voltage references operate by effectively summing a base emitter voltage with a voltage that has a positive temperature coefficient. A voltage that increases with temperature is referred to as Proportional to Absolute Temperature (PTAT) as mentioned in Section 3.1. By summing these two voltages with appropriate linear scaling, it is possible for the temperature coefficients to cancel, resulting in a voltage with little to no temperature dependence. This concept, illustrated in Figure 4-1, is what we will use to create our internal reference.

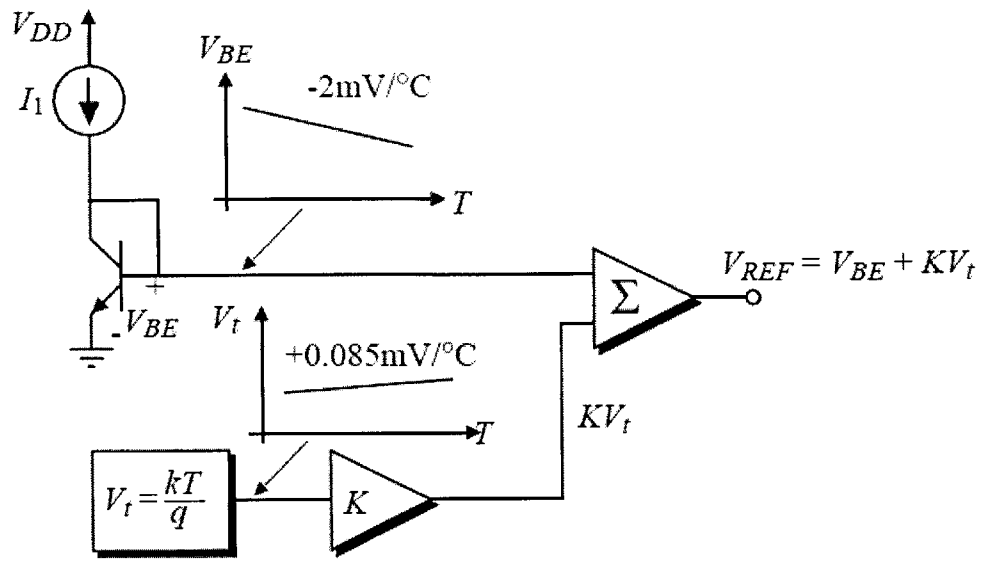

Figure 4-1. A bandgap reference uses a positive temperature coefficient to cancel the negative temperature coefficient of a transistor's base-emitter junction to produce a voltage that is independent of temperature.

As mentioned in the preceding paragraph, a voltage with a negative temperature coefficient can be derived from a transistor's base emitter voltage. It turns out that the difference between two base emitter voltages is a PTAT voltage. Ignoring the effects of finite output resistance (Early effect), the equation for collector current is (3.13), repeated below for convenience.

$$i_C = I_S e^{v_{BE}/V_T} \tag{3.13}$$

The variables I_S and V_T are described in Section 3.1. Solving (3.13) for base emitter voltage we obtain

$$v_{BE} = V_T \ln\left(\frac{i_C}{I_S}\right). \tag{4.1}$$

Take the difference between two base emitter voltages.

$$\Delta v_{BE} = v_{BE_1} - v_{BE_2}$$

Substituting (4.1) for v_{BE} results in

$$\Delta v_{BE} = V_T \ln\left(\frac{i_{C_1}}{I_{S_1}}\right) - V_T \ln\left(\frac{i_{C_2}}{I_{S_2}}\right).$$

Combining the natural log terms yields

$$\Delta v_{BE} = V_T \ln\left(\left(\frac{i_{C_1}}{I_{S_1}}\right)\left(\frac{I_{S_2}}{i_{C_2}}\right)\right).$$

We can substitute (3.2) to obtain

$$\Delta v_{BE} = \frac{kT}{q} \ln\left(\left(\frac{i_{C_1}}{I_{S_1}}\right)\left(\frac{I_{S_2}}{i_{C_2}}\right)\right) \tag{4.2}$$

$$= cT.$$

The difference is directly proportional to temperature with some proportionality constant, c, which depends on the ratios of the collector currents and transistor saturation currents (I_S), in addition to Boltzmann's constant, k, and electron charge, q.

The following expression, stated in [6], can be used to determine the temperature coefficient of the base emitter voltage.

$$v_{BE} = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{mkT}{q} \ln\left(\frac{T}{T_0}\right) + \frac{kT}{q} \ln\left(\frac{J_C}{J_{C0}}\right) \tag{4.3}$$

The bandgap voltage of silicon at 0°K, V_{G0}, is approximately 1.206V and m is a constant equal to 2.3. The collector current density is indicated by the variable J_C. The subscript 0 indicates a quantity evaluated at a reference temperature. If the 0 subscript is not present, the quantity is evaluated at the actual temperature, T. As discussed in [6], the current densities are PTAT, implying that

$$\frac{J}{J_0} = \frac{T}{T_0}. \tag{4.4}$$

The bandgap reference voltage will have the following form

$$V_{ref} = v_{BE} + K \cdot \Delta v_{BE}. \tag{4.5}$$

Plugging (4.2) and (4.3) into (4.5) yields

$$V_{ref} = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{mkT}{q}\ln\left(\frac{T_0}{T}\right) + \frac{kT}{q}\ln\left(\frac{J_C}{J_{C0}}\right) + K \cdot \frac{kT}{q}\ln\left(\left(\frac{i_{C_1}}{I_{S_1}}\right)\left(\frac{I_{S_2}}{i_{C_2}}\right)\right)$$

which simplifies to

$$V_{ref} = V_{G0} + \frac{T}{T_0}\left(V_{BE0} - V_{G0}\right) + (m-1)\frac{kT}{q}\ln\left(\frac{T_0}{T}\right) + K \cdot \frac{kT}{q}\ln\left(\left(\frac{i_{C_1}}{I_{S_1}}\right)\left(\frac{I_{S_2}}{i_{C_2}}\right)\right) \tag{4.6}$$

To determine (and ideally set to zero) the temperature dependence, we differentiate (4.6) with respect to temperature then set the derivative to zero. Note that the temperature coefficient will only be zero at the reference temperature. As the temperature deviates around the reference temperature, the reference voltage will have some (small) temperature dependence. Differentiating (4.6) gives

$$\frac{\partial V_{ref}}{\partial T} = \frac{1}{T_0}(V_{BE0} - V_{G0}) + (m-1)\frac{k}{q}\ln\left(\frac{T_0}{T}\right) - (m-1)\frac{k}{q} + K\cdot\frac{k}{q}\ln\left(\left(\frac{i_{C_1}}{I_{S_1}}\right)\left(\frac{I_{S_2}}{i_{C_2}}\right)\right)$$

$$= \frac{1}{T_0}(V_{BE0} - V_{G0}) + (m-1)\frac{k}{q}\left(\ln\left(\frac{T_0}{T}\right) - 1\right) + K\cdot\frac{k}{q}\ln\left(\left(\frac{i_{C_1}}{I_{S_1}}\right)\left(\frac{I_{S_2}}{i_{C_2}}\right)\right)$$

For zero temperature dependence,

$$\frac{\partial V_{ref}}{\partial T} = 0.$$

$T = T_0$ implies

$$V_{ref0} = V_{BE0} + K\cdot\frac{kT_0}{q}\ln\left(\left(\frac{i_{C_1}}{I_{S_1}}\right)\left(\frac{I_{S_2}}{i_{C_2}}\right)\right) = V_{G0} + (m-1)\frac{kT_0}{q} \qquad (4.7)$$

At room temperature (T_0=298°K),

$$V_{ref0} = V_{G0} + (m-1)\frac{kT_0}{q} \approx 1.12394V$$

Given this value and V_{BE0}, the appropriate scaling factor, K, and collector and saturation currents can be selected so that V_{ref0} will have the desired value and zero temperature coefficient. In a circuit implementation, K is typically controlled by a ratio of resistors.

Figure 4-2 shows an example of a simple, open-loop band-gap reference circuit presented in [7]. The output, V_{ref}, is composed of the base-emitter voltage of Q_3 and the voltage across R_2. Because the voltage across R_3 is the difference between V_{BE1} and V_{BE2}, it is PTAT and the resulting current through R_3 is PTAT (ignoring any temperature dependence the resistors may have). Ignoring base currents, the current through R_2 is the same as the current through R_3. This PTAT current through R_2 makes V_2 PTAT, so V_{ref} is composed of a V_{BE} and a PTAT voltage, as desired. The scaling factors and currents can be obtained through analysis of the circuit as follows.

$$V_3 = I_3 R_3 = v_{BE1} - v_{BE2}$$

Substituting from (4.1) yields

$$V_3 = V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right) - V_T \ln\left(\frac{I_{C2}}{I_{S2}}\right)$$
$$V_3 = V_T \ln\left(\frac{I_{C1}}{I_{S1}} \cdot \frac{I_{S2}}{I_{C2}}\right) \qquad (4.8a)$$

Assuming the transistors are matched, meaning they have the same device parameters, $I_{S1}=I_{S2}$ and (4.8a) simplifies to

$$V_3 = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right). \qquad (4.8b)$$

Since $I_2 = I_3 = \frac{V_3}{R_3}$,

$$V_2 = I_2 R_2 = \frac{R_2}{R_3} V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

$$= \frac{R_2}{R_3} \cdot \frac{kT}{q} \ln\left(\frac{I_{C1}}{I_{C2}}\right) \tag{4.9}$$

(4.9) has the same form as the PTAT term in (4.7) with $K = \frac{R_2}{R_3}$. If the transistors are matched, $v_{BE1}=v_{BE2}$ and $V_1=V_2$. In this case, the ratio of the collector currents, I_{C1} and I_{C2}, can be controlled by the ratio of the resistors, R_1 and R_2. The circuit's output voltage is then

$$V_{ref} = v_{BE3} + V_2$$

Substituting from (4.3) and (4.9) gives us

$$V_{ref} = V_{G0} + \frac{T}{T_0}\left(V_{BE3_0} - V_{G0}\right) + (m-1)\frac{kT}{q}\ln\left(\frac{T_0}{T}\right) + \frac{R_2}{R_3} \cdot \frac{kT}{q}\ln\left(\frac{I_{C1}}{I_{C2}}\right).$$

$$= V_{G0} + \frac{T}{T_0}\left(V_{BE3_0} - V_{G0}\right) + (m-1)\frac{kT}{q}\ln\left(\frac{T_0}{T}\right) + \frac{R_2}{R_3} \cdot \frac{kT}{q}\ln\left(\frac{R_2}{R_1}\right).$$

Differentiating with respect to temperature yields

$$\frac{\partial V_{ref}}{\partial T} = \frac{1}{T_0}\left(V_{BE3_0} - V_{G0}\right) + (m-1)\frac{k}{q}\left(\ln\left(\frac{T_0}{T}\right) - 1\right) + \frac{R_2}{R_3}\cdot\frac{k}{q}\ln\left(\frac{R_2}{R_1}\right).$$

Setting $\frac{\partial V_{ref}}{\partial T} = 0$ at $T = T_0 = 298°K$ gives us

$$V_{BE3_0} + T_0 \cdot \frac{R_2}{R_3}\cdot\frac{k}{q}\ln\left(\frac{R_2}{R_1}\right) = V_{G0} + T_0(m-1)\frac{k}{q} \approx 1.2394V.$$

Plugging in the appropriate values for T_0, k, and q, and using a typical (for Fairchild Semiconductor's 2N3904 npn transistor) v_{BE} value of 0.65V results in the following expression which can be used to select appropriate resistor values for the circuit of Figure 4-2.

$$\frac{R_2}{R_3}\ln\left(\frac{R_2}{R_1}\right) \approx 22.94947.$$

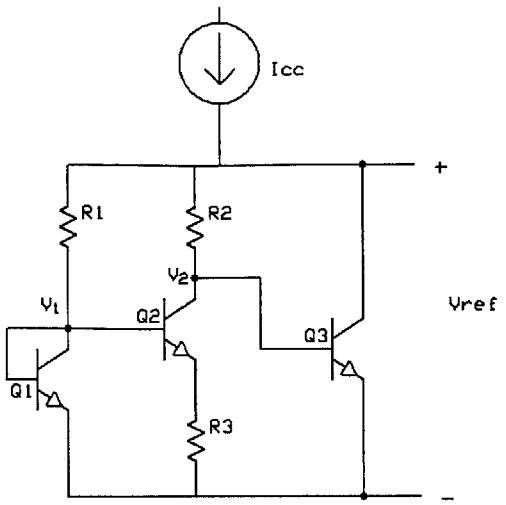

Figure 4-2. Discrete implementation of open-loop bandgap reference.

Typical bandgap reference circuits produce an output voltage of around 1.2V. To obtain a stable voltage reference of some other value, the bandgap voltage is used as the input to a voltage regulator circuit, like the one presented in Section 4.2. Figure 4-3 contains the schematic for a bandgap reference circuit that allows the output voltage to be scaled to some desired value without the use of a separate voltage regulator circuit. Analysis of the circuit reveals that the voltage at the bases of Q_1 and Q_2 is the typical bandgap voltage of about 1.2V. Thus, we can use the voltage divider formed by R_3 and R_4 to obtain a larger output voltage at the emitter of Q_3.

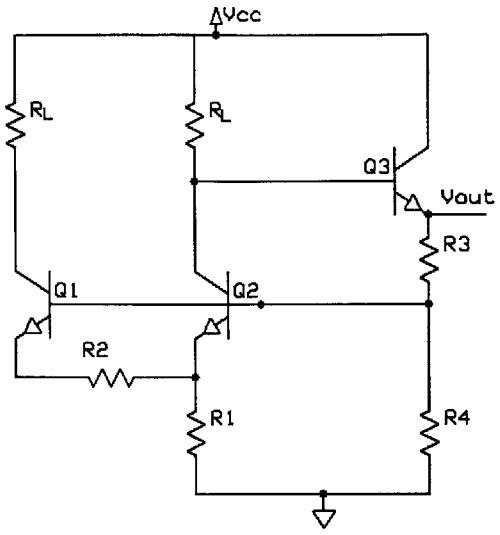

Figure 4-3. Schematic for bandgap reference circuit with output voltage that can be adjusted by changing the ratio of R_3 to R_4.

The example bandgap reference circuits presented thus far have a few shortcomings that make them non-ideal for certain applications. The circuits in Figure 4-2 and Figure 4-3 are both open loop implementations. This means there is no method for counteracting any deviations from the desired operating point. The circuit in Figure 4-2 relies on the voltages V_1 and V_2 being equal so that the current ratio can be controlled by the ratio of R_1 to R_2. However, V_1 and V_2 may not be the same because Q_1 and Q_3 may not be perfectly matched. In this case, we have no control over the ratio of I_{C1} to I_{C2}. Bandgap reference circuits use operational amplifiers (op amps) to provide feedback and stabilize the operating point. An example of such a circuit is contained in Figure 4-4.

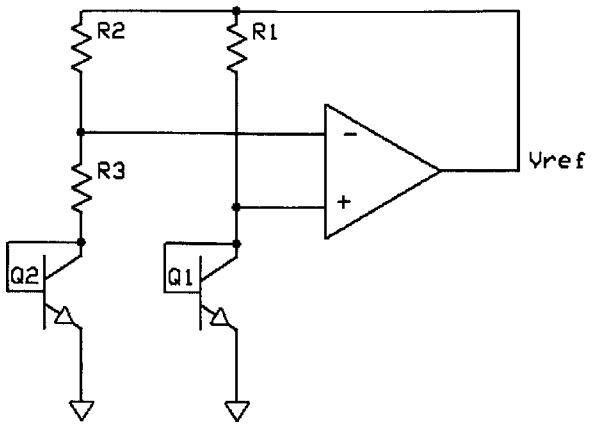

Figure 4-4. Closed-loop implementation of a bandgap reference.

Due to the op amp's large open loop gain (see Section 4.2), the voltages at its input terminals must be the same. From Figure 4-4, we can see that this means the voltage across R_3 is the difference between v_{BE1} and v_{BE2}. So the voltage across (and current through) R_3 is PTAT. Because R_2 is in series with R_3, the current and voltage associated with R_2 are also PTAT. The voltages at the op amp's input terminals being equal gives us the following relation

$$V_{R2} = V_{R1},$$

$$I_{C2}R_2 = I_{C1}R_1,$$

$$\Rightarrow \frac{I_{C1}}{I_{C2}} = \frac{R_2}{R_1}. \tag{4.10}$$

We can use (4.2) to determine R_3's voltage and current. We obtain results identical to those presented in (4.8a) and (4.8b), repeated again here for convenience.

$$V_3 = I_3 R_3 = v_{BE1} - v_{BE2}$$

$$= V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right) - V_T \ln\left(\frac{I_{C2}}{I_{S2}}\right)$$
$$= V_T \ln\left(\frac{I_{C1}}{I_{S1}} \cdot \frac{I_{S2}}{I_{C2}}\right) \tag{4.8a}$$

$I_{S1} = I_{S2} \Rightarrow$

$$V_3 = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right). \tag{4.8b}$$

The current through R_3 and R_2 is then

$$I_{C3} = \frac{V_3}{R_3} = \frac{V_T}{R_3} \ln\left(\frac{I_{C1}}{I_{C2}}\right). \tag{4.11}$$

The output voltage of the circuit is the sum of v_{BE1} and the voltage across R_1. We can use (4.10) and (4.11) to solve for the voltage across R_1 as follows.

$$V_{R1} = V_{R2} = I_{C2} R_2 .$$

Substituting (4.11) for I_{C2} gives

$$V_{R1} = \frac{V_T}{R_3} \ln\left(\frac{I_{C1}}{I_{C2}}\right) \cdot R_2 .$$

Using the result from (4.10) yields

$$V_{R1} = \frac{V_T}{R_3} \ln\left(\frac{R_2}{R_1}\right) \cdot R_2 . \tag{4.12}$$

Thus, V_{ref} can be calculated as

$$\begin{aligned} V_{ref} &= v_{BE1} + V_{R1} \\ &= V_{G0} + \frac{T}{T_0}\left(V_{BE1_0} - V_{G0}\right) + (m-1)\frac{kT}{q}\ln\left(\frac{T_0}{T}\right) + \frac{R_2}{R_3} \cdot \frac{kT}{q}\ln\left(\frac{R_2}{R_1}\right). \end{aligned}$$

Differentiating and solving just as we did for the circuit of Figure 4-3 leads us to the same result,

$$\frac{R_2}{R_3}\ln\left(\frac{R_2}{R_1}\right) \approx 22.94947 \tag{4.13}$$

for zero temperature dependence at room temperature. Using (4.13), we can select the appropriate resistor values for our bandgap reference circuit.

Our bandgap reference circuit requires an op amp that we must implement with transistors. The primary requirement for this circuit is fairly large gain. We will use a design with an actively loaded differential pair input stage followed by a second gain stage consisting of a common emitter amplifier. The complete transistor-level schematic for the bandgap reference, including op-amp, is shown in Figure 4-5. The differential pair consists of pnp transistors Q_3 and Q_4 and the common emitter amplifier consists of Q_7 and R_L. The 0.1μF capacitor helps to keep the output voltage constant. In an IC implementation of the circuits presented in this section it is likely that emitter areas,

instead of only resistors, would be scaled to achieve the desired ratios. See below for a design example.

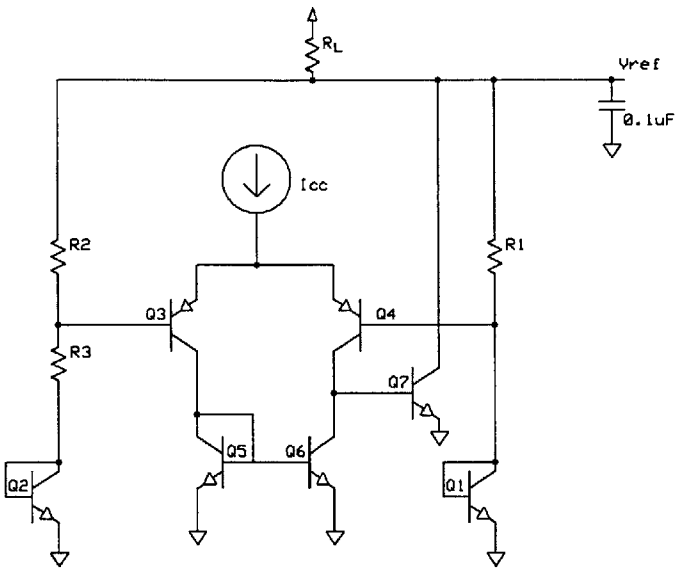

Figure 4-5. Transistor level implementation of closed-loop bandgap reference.

Design Calculations

We begin the design of our bandgap reference by using (4.13), repeated below, to choose values for the resistors R_1, R_2, and R_3.

$$\frac{R_2}{R_3}\ln\left(\frac{R_2}{R_1}\right) \approx 22.94947 \tag{4.13}$$

We can simply choose a convenient ratio for R_2 to R_1 and solve for the required value of R_3. Since we are using discrete components, we may have to try a few different ratios to

get results that are close enough to the standard resistor values we have available. Choosing R_2=11kΩ and R_1=910Ω gives us

$$\frac{11k\Omega}{R_3}\ln\left(\frac{11k\Omega}{910\Omega}\right) \approx 22.94947$$

$$\Rightarrow R_3 = \frac{11k\Omega}{22.94947}\ln\left(\frac{11k\Omega}{910\Omega}\right)$$

$$R_3 = 1.1945k\Omega.$$

The result is approximately 1.2kΩ, which is a standard value. We will use an LM394 SuperMatch pair for Q_1 and Q_2 so their temperatures and v_{BE}'s will be well matched.

Next, we calculate the open loop gain of the op amp circuit in Figure 4-5. From Section 3-4, we know that the gain for an actively loaded differential pair is

$$a_v = g_m R_L$$

where R_L is the net resistance seen at the output of the stage. In this case, we can see that R_L is the parallel combination of r_{o4}, r_{o6}, and $r_{\pi 7}$. The DC bias value of the voltage at Q_6's collector is the same as that of Q_5. Thus the DC value at the base of Q_7 is the same as that at the bases of Q_5 and Q_6. So assuming all transistors are nearly identical, the DC bias current of Q_7 will be the same as the current through Q_5 and Q_6, $\frac{1}{2}I_{CC}$. Transistor parameter values can be obtained from the datasheets distributed by the manufacturer. Let's assume values of 100 for β_n, 100V for V_{An}, and 50V for V_{Ap}. Using these estimated parameters, we can calculate g_m, r_o, and r_π as follows.

$$g_{m5} = g_{m6} = g_{m7}$$

$$= \frac{\frac{1}{2} I_{CC}}{V_T}$$

$$= \frac{I_{CC}}{52mV}$$

$$r_{o4} = \frac{V_{Ap}}{\frac{1}{2} I_{CC}}$$

$$= \frac{100V}{I_{CC}}$$

$$r_{o6} = \frac{V_{An}}{\frac{1}{2} I_{CC}}$$

$$= \frac{200V}{I_{CC}}$$

$$r_{\pi 7} = \frac{\beta_{0n}}{g_{m7}}$$

$$= \frac{5.2V}{I_{CC}}$$

The gain of the first stage is

$$a_{v1} = g_m R_L .$$

Substituting the effective load resistance results in

$$a_{v1} = g_m \cdot \left(r_{o4} \| r_{o6} \| r_{\pi 7}\right),$$

$$= \frac{I_{CC}}{52mV} \cdot \left(\frac{100V}{I_{CC}} \Bigg\| \frac{200V}{I_{CC}} \Bigg\| \frac{5.2V}{I_{CC}} \right).$$

The gain of the second stage is

$$a_{v2} = g_m R_L$$

$$a_{v2} = \frac{I_{CC}}{52mV} R_L$$

For I_{CC}=1mA and R_L=10kΩ,

$$a_{v1} \approx 92.76$$
$$a_{v2} \approx 192.3$$
$$a_v = a_{v1} a_{v2} \approx 17839$$
$$\approx 18{,}000$$

The op amp has a fairly large open-loop gain of almost 18,000. We could even reduce I_{CC} a bit to lower power consumption. As long as the gain is in excess of about 1,000, our bandgap reference should be accurate.

The full Eagle schematics with documented component values for the bandgap reference and all other circuit blocks are contained in the appendix.

4.2 Operational Amplifier

The ideal single-ended operational amplifier (op amp) takes a differential input, provides infinite gain, has infinite input resistance, R_{in}, and zero output resistance, R_{out}. The implications of this ideal model are that the voltages at the two input terminals are equal (otherwise the output voltage would be infinite), no current flows into the input terminals, and the op amp can source and sink infinite current at its output. In reality, op amps have finite gain, a_0, finite input resistance, and non-zero output resistance. However, for a reasonably well designed op amp, the gain and R_{in} are very large and R_{out} is very small. In this case, we can assume the ideal model when analyzing the circuit.

Op amps are often used in a feedback configuration where there is some network, *f*, providing feedback from the output to one of the input terminals. An example of an op amp in a negative feedback configuration is contained in Figure 4-6. Figure 4-7 shows the block diagram for an op amp with gain a_0 and feedback network f. An application of Black's Formula (see [3] for information regarding Black's Formula) yields the following transfer function from input to output voltage:

$$\frac{v_o}{v_i} = \frac{a_0}{1 + a_0 f}. \tag{4.14}$$

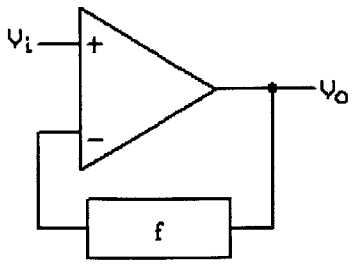

Figure 4-6. Operational amplifier in negative feedback configuration.

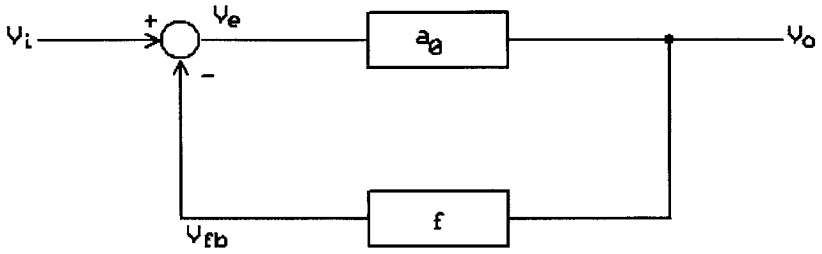

Figure 4-7. Block diagram of a feedback amplifier.

Because a_0 is ideally very large, $a_0 f >> 1$ and (4.14) simplifies to:

$$\frac{v_o}{v_i} \approx \frac{1}{f}. \tag{4.15}$$

(4.15) implies that if the op amp has large open-loop gain, a_0, the gain of the circuit when operated with feedback is dependent only on the gain of the feedback network and so will be relatively insensitive to variations in a_0. This well-defined, controllable gain is the reason that op amps are typically used with feedback.

With the application of feedback, an op amp can be used as a linear voltage regulator. For a feedback network consisting of only passive elements, the magnitude of

f is less than or equal to 1. Thus, (4.15) indicates that v_o will be greater than or equal to v_i. We will use this concept to derive a 2.5V reference, 5V supply, and 12V supply from the bandgap voltage. An example of an op amp used as a voltage regulator is shown in Figure 4-8. The resistive voltage divider formed by R_1 and R_2 is the feedback network. Its gain, f, is simply

$$f = \frac{R_2}{R_1 + R_2}. \tag{4.16}$$

The transistor, Q, is a pass element. The op amp sets Q to pass the amount of current needed to obtain the relation between v_{in} and v_{out} described by (4.14). The remainder of the voltage, the difference between V_{CC} and v_{out}, is dropped across Q.

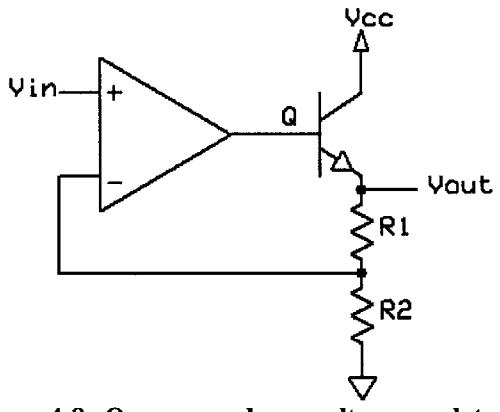

Figure 4-8. Op amp used as a voltage regulator.

Looking again at Figure 4-8, we see that Q, R_1, and R_2 essentially form an emitter follower (EF) buffer at the output of the op amp similar to the one presented in Section 3.3. To create our voltage regulator, we need a circuit that takes a differential input, has high open-loop gain, and has an EF buffer output stage that provides a fraction of the

output voltage as feedback to the negative input terminal. See the schematic in Figure 4-9. The circuit uses an actively loaded differential pair to provide high open loop gain. See below for a design example.

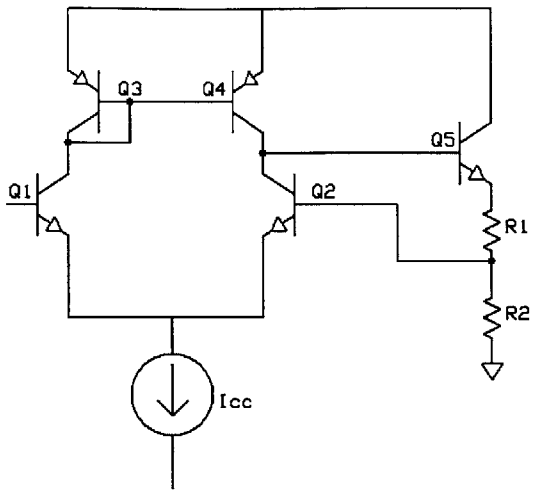

Figure 4-9. Transistor-level schematic of the voltage regulator.

Design Calculations

The voltage output of our bandgap reference circuit is about 1.22V. For the purpose of these design calculations, we shall assume that the bandgap voltage is 1.25V Note that this approximation is reasonable because we have the ability to choose the relative sizes of the resistors to compensate for the bandgap voltage being a bit smaller than we assume.

Assume I_{CC} in Figure 4-8 is 2mA. The collector currents are

$$I_{C1} = I_{C2} = I_C = 1mA.$$

This implies that the transconductance is

$$g_m = \frac{I_C}{V_T},$$

$$= \frac{1mA}{25mV} \approx 0.04.$$

The effective load resistance seen at the output of the differential pair is the parallel combination of three resistances: that seen looking into the collector of Q_2, into the collector of Q_4, and into the base of Q_5. This effective resistance can be expressed as

$$R_L = r_{o2} \| r_{o4} \| (r_{\pi 5} + (\beta_0 + 1) \cdot (R_1 + R_2)) \tag{4.17}$$

Recall from Section 3.4 that the resistance seen looking into the collector of a transistor is

$$r_o = \frac{V_A}{I_C}. \tag{4.18}$$

The transistors we will primarily be using are the 2N3904 (npn) and the 2N3906 (pnp). According to the models specified in datasheets for these transistors, the Early voltage is about 74V for the npn transistors and about 19V for the pnp transistors. We can plug these values into (4.18) to calculate r_{o2} and r_{o4} as follows.

$$r_{o2} = \frac{V_{An}}{I_C}$$

$$= \frac{74V}{1mA} = 74k\Omega$$

$$r_{o4} = \frac{V_{Ap}}{I_C}$$

$$= \frac{19V}{1mA} = 19k\Omega$$

In order for the circuit to have a good output buffer, the resistance seen looking into the base of Q_5 must be very large. The typical current gain, β, for our npn transistors is about 200. If we choose R_1 and R_2 to have a sum of about 10kΩ, their resistance looks to be about 200 times larger, or 2MΩ, when viewed from the base of Q_5. The total resistance seen looking into Q_5's base is then the sum of $r_{\pi 5}$ and 2MΩ. The input resistance of a BJT, r_π, is given by the following expression

$$r_\pi = \frac{\beta_0}{g_m} \tag{4.19}$$

We can calculate the current through R_1 and R_2, which is approximately I_{C5}, because we know that the voltage across the resistors is the output of our voltage regulator. For the 12V supply, we get

$$I_{C5} = \frac{V_{out}}{R_1 + R_2},$$

$$= \frac{12V}{10k\Omega}$$
$$= 1.2mA$$

This implies that the transconductance is

$$g_{m5} = \frac{I_{c5}}{V_T}$$

$$= \frac{1.2mA}{25mV}$$
$$= 0.048$$

Substituting this value for g_m and 200 for β in (4.19) yields

$$r_\pi = \frac{200}{0.048},$$

$$= 4.2k\Omega,$$

when the output of our voltage regulator is 12V. For the 5V supply and 2.5V reference, the lower voltage across the resistors means that I_{C5} and g_m will be smaller so r_π will be even larger.

Combining the calculated value for r_π with the 2MΩ resistance calculated above results in a net resistance seen looking into the base of Q_5 that is still approximately 2MΩ. This resistance is so much larger than the 19kΩ and 74kΩ in parallel with it that

we can neglect it. So the effective resistance seen at the output of the differential pair simplifies to

$$R_L = r_{o2} \| r_{o4} .$$

So the approximate load resistance is

$$74k\Omega \| 19k\Omega \approx 15k\Omega .$$

Using the effective R_L and g_m calculated above for the differential pair, we can determine the open loop gain, a_0, using

$$a_0 = a_v = g_m R_L .$$

Plugging in the values for g_m and R_L gives a gain of

$$a_0 = (0.04) \cdot (15k\Omega) = 600 .$$

While typical values of a_0 are ideally much greater than 1000, 600 is a reasonable open loop gain and for small enough output voltages (equivalently, large enough *f*), the product $600f$ is sufficiently greater than 1 and the approximation made in (4.15) is valid. If we want to increase the open-loop gain, we can increase the value of the current source, I_{CC}.

Creating a 12V supply from a 1.25V input implies a closed-loop gain of

$$\frac{v_{out}}{v_{in}} = \frac{1}{f} = \frac{12V}{1.25V}.$$

This implies

$$f = \frac{1.25V}{12V}$$

$$\approx 0.104.$$

We know that f is the voltage divider formed by R_1 and R_2 so we calculate

$$\frac{R_2}{R_1 + R_2} = 0.104$$

which implies that

$$R_1 \approx 8.6R_2.$$

Thus by choosing R_1=8.6kΩ and R_2=1kΩ, we get the desired gain and the sum of the resistors is almost 10kΩ so the input resistance of the EF buffer is high.

The output resistance of the voltage regulator is the sum of R_1 and R_2 in parallel with the resistance seen looking into the emitter of Q_5. The resistance seen looking into the emitter of Q_5 is the sum of $r_{\pi 5}$, which is 4.2kΩ, and the previously calculated 15kΩ

seen at the output of the differential pair divided by the current gain, β. We calculate this to be about

$$\frac{4.2k\Omega + 15k\Omega}{200} \approx 96\Omega .$$

The 9.6kΩ resistance of R_1 and R_2 is negligible in parallel with 96Ω, so the effective output resistance is about 96Ω.

The 5V and 12V supplies must provide current to the circuits that they power. This current must flow through the output transistor, Q_5 of Figure 4-9. The amount of current that Q_5 can supply is limited by the amount of base current that the differential pair can provide for Q_5. By adding another transistor, Q_6, between the differential pair and Q_5 as in Figure 4-10, the amount of current that the voltage regulator can provide is increased by a factor of β. This is because Q_6 increases the amount of base current available to Q_5 by a factor of β. The addition of Q_6 also decreases the output resistance of the regulator by a factor β.

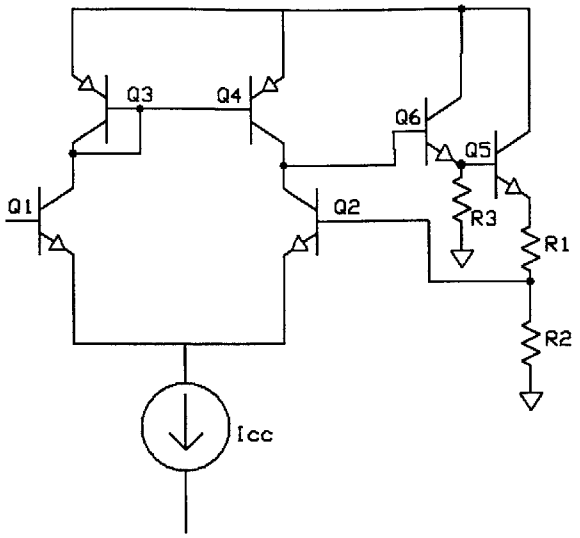

Figure 4-10. Voltage regulator with increased current sourcing capacity.

4.3 Comparator

A comparator is a device with two input terminals, one non-inverting and the other inverting. The comparator produces a single-ended output which is high (near the positive supply rail) when the voltage at the non-inverting input terminal exceeds the voltage at the inverting input terminal. The output is low (near the negative supply rail, which is often ground) when the voltage at the non-inverting input terminal is lower than that of the inverting input terminal. This behavior can be obtained from an op-amp (in an open loop configuration) with sufficient gain such that any small difference between the voltages at the inputs is amplified enough to drive the output to one supply rail or the other.

A differential pair input stage is a good place to start. We know that for a single-ended output the gain will be about $\frac{1}{2} g_m R_L$ so we can choose the bias current and R_L

accordingly. A schematic is shown in Figure 4-11. The total bias current in Q_1 and Q_2 is I_{CC}. For an applied differential input voltage, v_d, there is a decrease of $\frac{1}{2} g_m v_d$ in I_{C1} and an equal increase in I_{C2}. Note that the change caused by v_d is in the opposite direction compared to that of the differential pair circuit analyzed in Section 3-4. This is due to the fact that this circuit uses pnp transistors instead of npn. The change in current causes a decrease of $\frac{1}{2} g_m v_d R_1$ in the voltage across R_1 and an equal increase in the voltage across R_2 (assuming R_1=R_2).

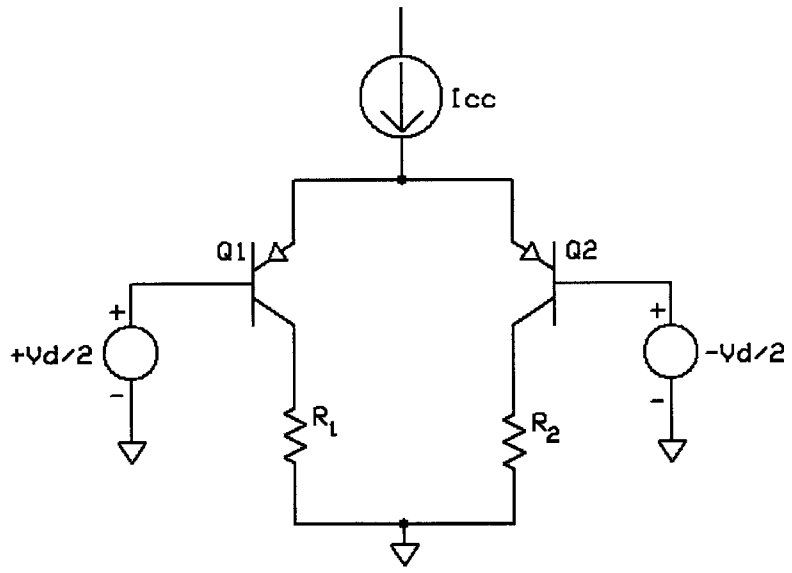

Figure 4-11. Differential pair to be used as the input stage for a comparator.

If we connect the base of an npn transistor (in common emitter configuration) to the varying terminal of R_1, we obtain the desired amplification of the change in voltage. See Figure 4-12 for a schematic. When the voltage at that node is below a v_{BE} drop (about 0.6V), Q_3 will be off so no current will flow through R_3 and the output voltage will be high. When the voltage drop across R_1 increases to more than a v_{BE} drop, Q_3 will

turn on, current will flow through R_3, and the output voltage will go low. Since a positive differential input voltage applied from Q_1 to Q_2 causes the current through R_1 to decrease (which results in a high output voltage), the base of Q_1 is the non-inverting input terminal to the comparator and the base of Q_2 is the inverting one. See below for the design calculations.

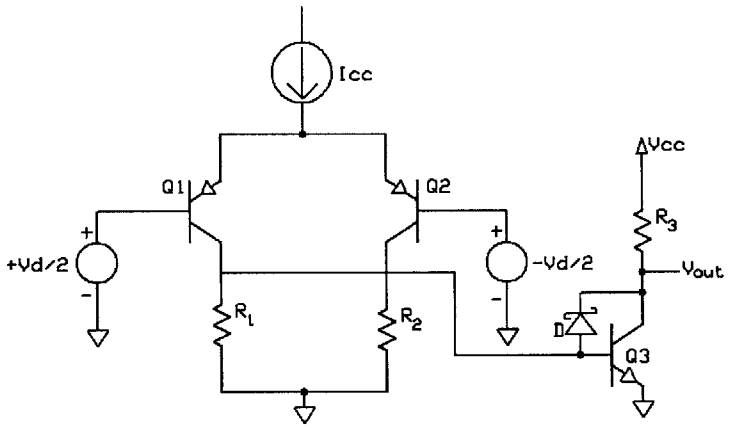

Figure 4-12. Schematic of comparator with clamping diode, D, to increase circuit response time.

Design Calculations

Let I_{CC} = 2mA. Let R_1=R_2=R_L.

$$I_{CC} = 2mA \Rightarrow I_{C1} = I_{C2} = I_C = 1mA$$

The transconductance is

$$g_m = \frac{\partial i_C}{\partial v_{BE}} = \frac{I_C}{V_{th}} = \frac{1mA}{25mV} = 0.04\,.$$

If a 25mV differential voltage is applied, all 2mA of bias current will flow through the transistor with the larger v_{BE} (the one whose base is at the lower voltage). This 2mA of current must be enough to cause the voltage drop across R_L to exceed a V_{BE}

drop and turn on Q_3. If we set R_L=510Ω, the voltage drop will be a little over 1V, which should be sufficient.

$$V_{R_L} = I_{CC} R_L$$

$$= 2mA \cdot 510\Omega = 1.02V$$

For a differential input of significant magnitude (which will typically be the case for our application), the current through R_1 will either be 2mA (for v_d negative) or negligible (for v_d positive), causing the comparator's output voltage to be either $v_{CE,sat}$ or V_{CC}, respectively. We include a clamping schottky diode between the base and collector of Q_3 to prevent the collector voltage from dropping too far below the base voltage into saturation. As Figure 4-13 shows, the time it takes Q_3 to recover from saturation increases the delay of the comparator's output substantially. Including the schottky diode means that the low output voltage will no longer be $v_{CE,sat,}$ but instead will be just a schottky diode drop below 1V (at about 0.7 to 0.8V). This is not a problem because the threshold voltage for the MOSFETS we will be using is about 2V, so 0.8V will be recognized as a logic low.

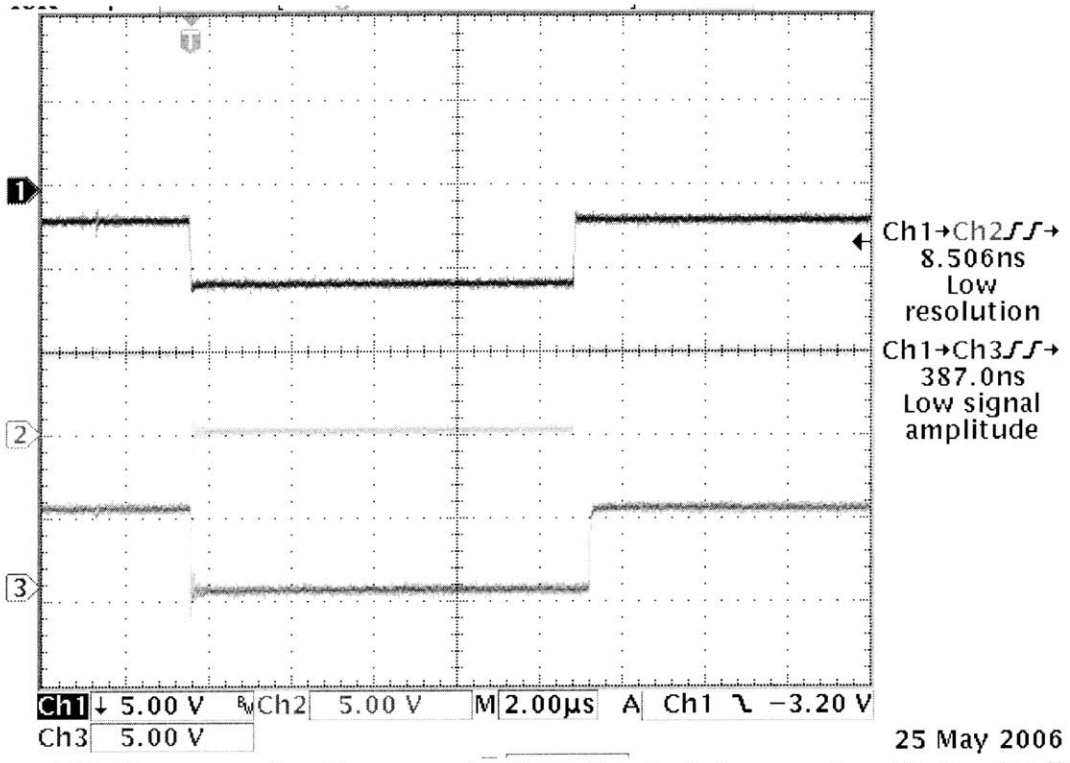

Figure 4-13. Square wave input to comparator (trace 1), output of comparator with clamping diode (trace 2), and output of comparator without clamping diode (trace 3). The rise time is only about 9ns with the clamping diode, compared to about 387ns when there is no clamping diode.

Hysteresis

A positive feedback loop around a comparator can be used to create hysteresis. The positive feedback causes the voltage at the non-inverting input terminal to change in the direction of the output voltage when the output voltage changes (due to the voltage at the other input terminal being increased or decreased beyond the threshold set at the non-inverting terminal). See Figure 4-14 for a schematic of this configuration. The calculations below demonstrate how this circuit can be used to create the desired threshold levels.

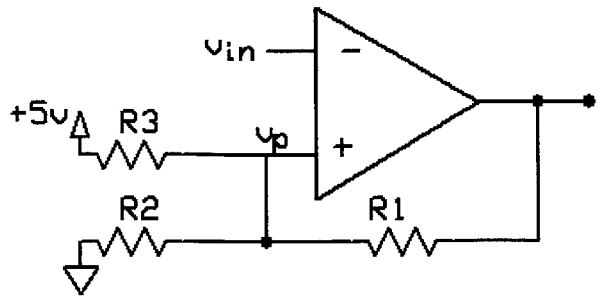

Figure 4-14. Comparator in positive feedback configuration.

When the input voltage is below the voltage at the non-inverting input terminal (V_p), the output voltage is high (5V) and the voltage V_p is given by the following voltage divider relation:

$$V_p = 5V\left(\frac{R_2}{R_2 + R_1 \parallel R_3}\right) = V_{T,high}. \tag{4.20}$$

This is the high threshold voltage. The input voltage must be raised above this value for the output voltage to go low (approx. 0V). When the output voltage goes low, V_p is given by the following voltage divider relation:

$$V_p = 5V\left(\frac{R_2 \parallel R_1}{R_3 + R_2 \parallel R_1}\right) = V_{T,low} \tag{4.21}$$

$V_{T,low}$ is lower than $V_{T,high}$ so this circuit creates a gap between the threshold voltages that the input must pass to cause the output voltage to change state. This circuit can be used to keep noisy input signals from causing the output voltage to falsely switch states. Another application for the comparator with positive feedback is in relaxation oscillator circuits. For more information on using this circuit as an oscillator, see Section 4.4 which covers the clock.

4.4 Clock

The comparator with positive feedback, presented in Section 4.3, can be used as a relaxation oscillator if a capacitor is connected to the negative input terminal and charged and discharged through a resistor connected to the comparator's output. See [8] for a more comprehensive discussion of relaxation oscillators. The resulting voltage waveforms are a square wave at the comparator's output varying between 0V (approximately) and 5V, a square wave at the positive input terminal varying between $V_{T,low}$ and $V_{T,high}$, and a triangle waveform at the negative input terminal as the capacitor voltage ramps up and down between the two thresholds. Example plots are shown in Figure 4-15. The time it takes for the capacitor to charge and discharge, and thus the period of the waveforms, is determined by the time constant defined by the product of the capacitance and the resistance through which it charges and discharges. To obtain an output with a duty ratio other than 0.5, the charge and discharge times must be unequal. This can be accomplished by using separate charge and discharge resistors, with diodes in series to ensure that the current through them will only flows in the desired direction. Figure 4-16 contains a schematic.

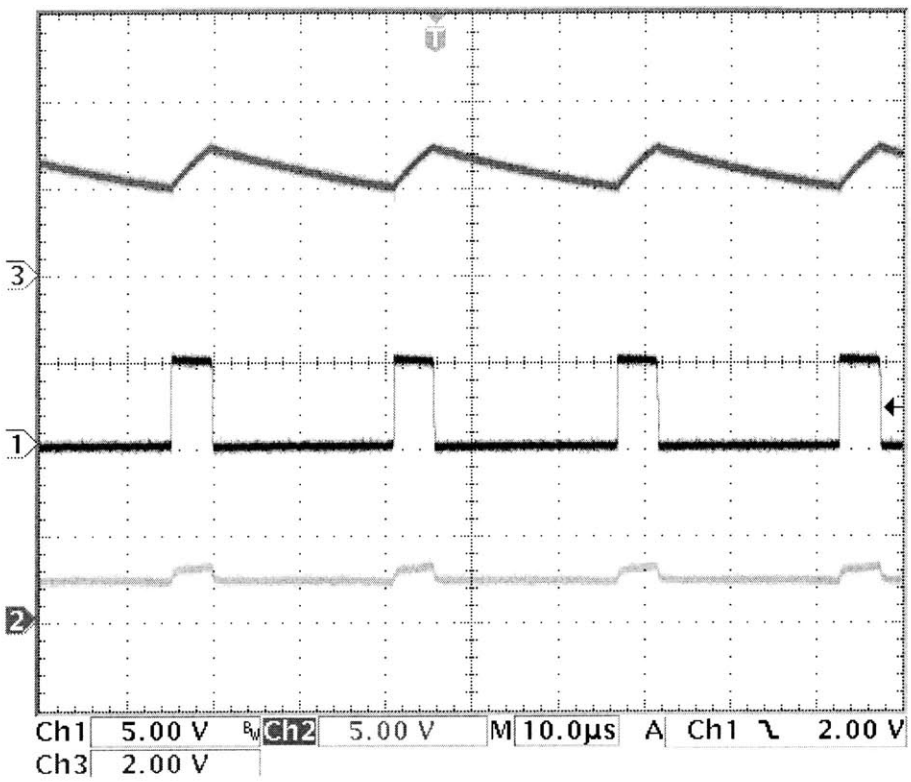

Figure 4-15. Capacitor voltage (trace 3), comparator output voltage (trace 1), and voltage at the positive input terminal (trace 2).

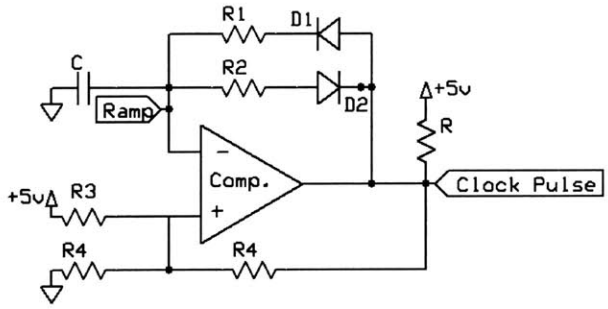

Figure 4-16. Schematic of clock circuit designed around comparator in positive feedback configuration.

In the current comparator design, the output is connected to the 5V supply through a resistor, R. R in series with R_1 of Figure 4-16 is the net resistance that C must charge through. R is typically too large to be neglected and so must be considered in the calculation of the time it takes the capacitor to charge. To remove the dependence of the

capacitor's charge time (and oscillator's frequency) on R, we can add a CMOS inverter to the output of the comparator. The resistor R is now replaced by the on resistance of the p-type MOSFET, which is typically small enough to be ignored. This addition gives us the clock circuit in Figure 4-17. The complete transistor level schematic for the clock circuit with CMOS comparator output is shown in Figure 4-18. The calculations for designing an oscillator of some specified frequency are described below.

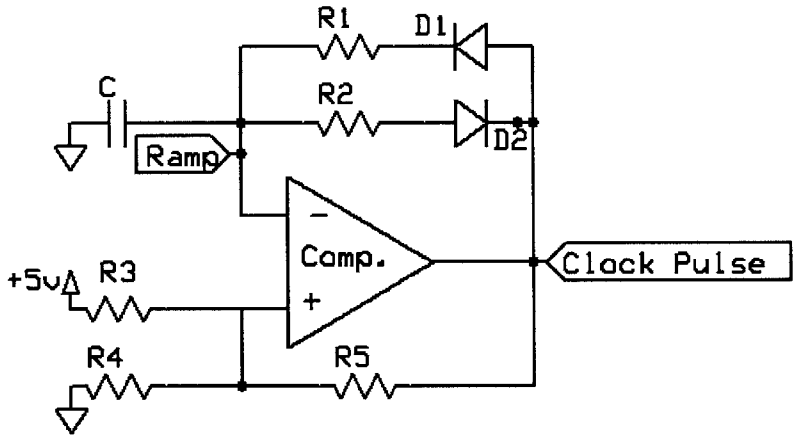

Figure 4-17. Schematic of clock circuit with CMOS inverter added to the output of the comparator.

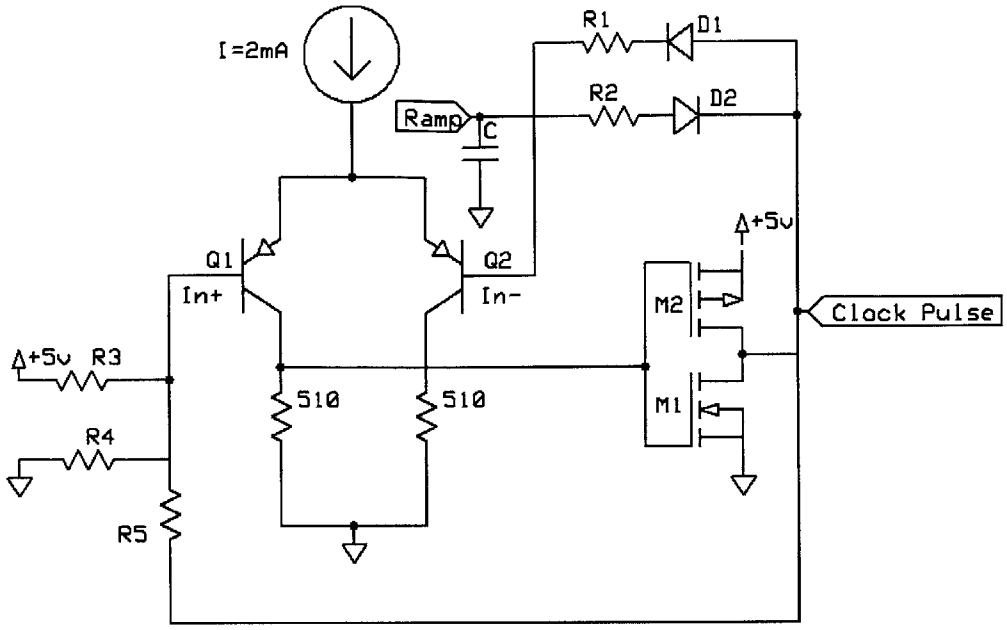

Figure 4-18. Transistor level schematic of clock circuit.

Design Calculations

The desired frequency of oscillation is 50kHz. 50kHz corresponds to a period, T, of 20μs, meaning the sum of the charge and discharge time for the capacitor is about 20μs. We need the oscillator output to be a narrow pulse, so the charge time must be much shorter than the discharge time. Let's try to set the discharge time at about 100 times the length of the charge time. That is equivalent to setting R_2 to be 100 times larger than R_1. If we choose R_3=R_4=R_5=20kΩ, then the threshold voltages at the positive input terminal can be calculated using (4.20) and (4.21) as follows

$$V_{T,high} = 5V\left(\frac{20k\Omega}{20k\Omega + 20k\Omega \parallel 20k\Omega}\right) \approx 3.33V$$

$$V_{T,low} = 5V\left(\frac{20k\Omega \parallel 20k\Omega}{20k\Omega + 20k\Omega \parallel 20k\Omega}\right) \approx 1.67V$$

So the capacitor voltage will oscillate between 1.67V and 3.33V. Using these initial conditions and the equation for charging and discharging a capacitor expressed in (4.22), we can determine the necessary relationship between C, R_1, and R_2 to obtain 50kHz oscillation frequency.

$$v_C = v_f + (v_i - v_f)e^{-t/RC} \tag{4.22}$$

The capacitor is being charged by the 5V supply from an initial voltage of 1.67V so we can modify (4.22) to obtain

$$v_C = 5V + (1.67V - 5V)e^{-t/RC} \tag{4.23}$$

We can solve (4.23) for the time it will take the capacitor voltage to charge to the high threshold value of 3.33V.

$$t_1 = -R_1 C \cdot \ln\left(\frac{3.33V - 5V}{1.67V - 5V}\right) = -R_1 C \cdot (-0.69)$$

When the capacitor is being discharged from 3.33V, (4.22) is modified as follows

$$v_C = 0V + (3.33V - 0V)e^{-t/RC} \tag{4.24}$$

We can solve (4.24) for the time it will take the capacitor to discharge to the low threshold value of 1.67V.

$$t_2 = -R_2 C \cdot \ln\left(\frac{1.67V - 0V}{3.33V - 0V}\right) = -R_2 C \cdot (-0.69)$$

The period, T, is the sum of t_1 and t_2. Thus by choosing some value for C, say 1nF, and setting $R_2=100R_1$, we can solve for the values of R_1 and R_2 that will make the period approximately 20μs.

$$T = t_1 + t_2$$

Plugging in the expressions computed for t_1 and t_2 yields

$$T = 0.69 \cdot C \cdot (R_1 + R_2)$$

$$= 0.69 \cdot C \cdot 101R_1 .$$

We can solve for R_1 as follows

$$R_1 = \frac{T}{69.69 \cdot C}.$$

Substituting

$$T = 20\mu s$$
$$C = 1nF$$

leads to the values

$$R_1 \approx 287\Omega$$
$$R_2 \approx 28.7k\Omega$$

Choosing R_1=300Ω and R_2=27kΩ results in

$$t_1 \approx 0.69 \cdot 1nF \cdot 300\Omega \approx 0.207\mu s$$
$$t_2 \approx 0.69 \cdot 1nF \cdot 27k\Omega \approx 18.63\mu s$$

$$t_1 + t_2 \approx 18.84\mu s$$

which implies an clock frequency of

$$f = \frac{1}{T} \approx 53kHz.$$

4.5 Error Amplifier

The error amplifier serves dual roles of being the summing junction for the reference voltage and the feedback from the converter and also providing the compensation, $G_C(s)$. As determined in the discussion of control and compensation in

Section 2.2, we would like to use PI compensation. This can be accomplished with an op-amp configured as shown in Figure 4-19. However, in addition to designing the error amplifier to obtain the necessary G(s), we would also have to compensate the op-amp itself to ensure its stability in that feedback configuration.

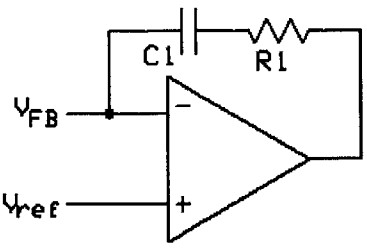

Figure 4-19. Operational amplifier used to provide PI compensation.

To simplify things, an open loop PI compensation scheme can be implemented as shown in Figure 4-20. Adding the capacitor C_2 in Figure 4-20 inserts an additional pole in the transfer function so we've got lead compensation in addition to the integrator. In this circuit, an actively loaded differential pair produces a current that is proportional to the error (reference voltage minus feedback). That current then flows through a net impedance (at the base of Q_3 in Figure 4-20) to create the desired compensation transfer function derived in Section 2.2. Transistor Q_3 is used as an emitter follower buffer so that loading effects due to the next device (in this case, the comparator) do not interfere with the compensation.

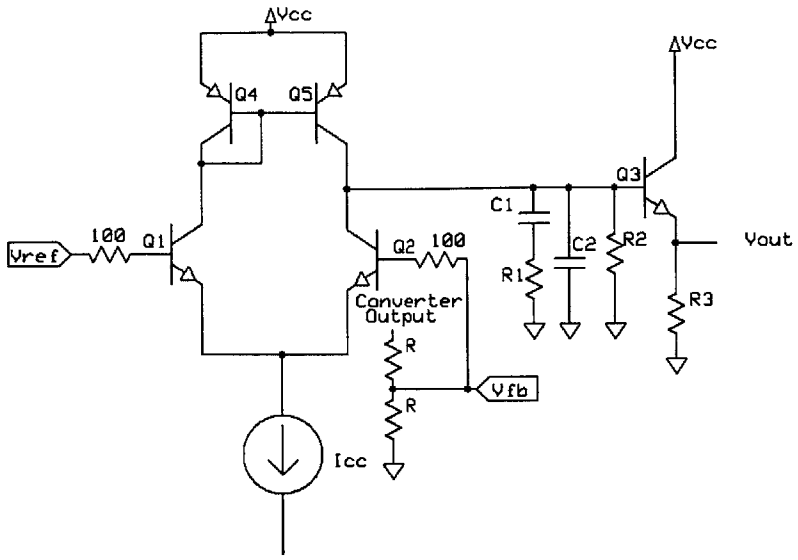

Figure 4-20. Open-loop implementation of error amplifier.

Design Calculations

Assume some differential error voltage, v_e, is applied across the input terminals of the error amplifier in Figure 4-20. The error voltage is the difference between V_{ref} and V_{fb}. From the analysis of an actively loaded differential pair in Section 3-4, we know that the output current, i_o, will be equal to $g_m v_e$. Ignoring the output buffer, we have the equivalent circuit shown in Figure 4-21. The transfer function from v_e to the output can be calculated as follows:

$$Z_{eq} = \left(R_1 + \frac{1}{sC_1} \right) \| \frac{1}{sC_2} \| R_2 \tag{4.25}$$

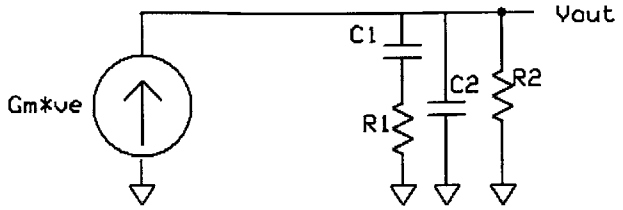

Figure 4-21. Equivalent circuit for calculating error amplifier transfer function, $G_C(s)$.

R_2 is very large and can be ignored for these calculations. Thus we get that the equivalent impedance expressed in (4.25) can be determined as follows.

$$Z_{eq} = \left(R_1 + \frac{1}{sC_1} \right) \| \frac{1}{sC_2}$$

or equivalently,

$$Z_{eq} = \frac{\left(R_1 + \frac{1}{sC_1} \right) \cdot \frac{1}{sC_2}}{R_1 + \frac{1}{sC_1} + \frac{1}{sC_2}}$$

simplification yields

$$= \frac{R_1 C_1 s + 1}{s\left(R_1 C_1 C_2 s + C_1 + C_2\right)}$$

$$= \frac{R_1 C_1 s + 1}{s\left(R_1 \left(C_1 \| C_2\right) s + 1\right)} \cdot \frac{1}{C_1 + C_2} \qquad (4.26)$$

The equivalent impedance expressed in (4.26) is the transfer function from the input current to the output voltage. We can use (4.26) to find the transfer function from the error voltage input to the output voltage.

$$v_{out} = i_o Z_{eq}$$

$$= g_m v_e Z_{eq}$$

So the transfer function from error to output is

$$\frac{v_{out}}{v_e}(s) = g_m Z_{eq}$$

$$= \frac{R_1 C_1 s + 1}{s(R_1(C_1 \parallel C_2)s + 1)} \cdot \frac{g_m}{C_1 + C_2}$$

Substituting for g_m gives

$$\frac{v_{out}}{v_e}(s) = \frac{R_1 C_1 s + 1}{s(R_1(C_1 \parallel C_2)s + 1)} \cdot \frac{\frac{1}{2 \cdot V_T} I_{CC}}{C_1 + C_2} \tag{4.27}$$

which can be used to choose I_{CC} and the resistor and capacitor values that will provide the correct compensating transfer function.

4.6 Current Sense Amplifier

We are using a small, current sense resistor in series with the high-side MOSFET to estimate the inductor current. We need a current sense amplifier that takes the small voltage drop produced across the current sense resistor and amplifies it. As discussed in Section 2.3, the current sense amplifier will not function properly when either of its inputs (or the common-mode) is too close to or greater than the supply voltage. This is

because transistors in the amplifier will be saturated. Since the input voltage to the comparator can be much higher than the control circuit's typical analog supply voltage, the voltages on either side of the current sense resistor must first be lowered with a resistive voltage divider before they can be input to the current sense amplifier.

Closed-Loop Differential Amplifier

The current sensing function can be performed by a closed-loop amplifier that takes the differential input voltage and provides the required amount of gain. This can be accomplished by an op amp configured as a shown in Figure 4-22. The circuit takes the difference between the voltages V_1 and V_2 and amplifies it by a factor of $\frac{R_2}{R_1}$. This circuit can be implemented with almost any transistor-level op amp design.

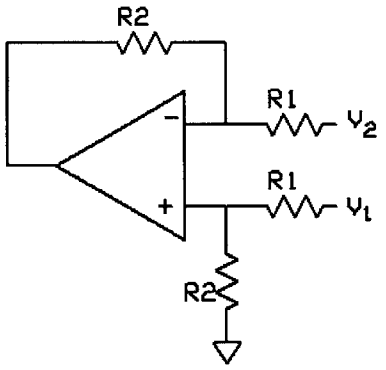

Figure 4-22. Circuit for amplifying the difference between two voltages, V_1 and V_2.

A possible transistor-level implementation of the closed-loop amplifier is depicted in Figure 4-23. This circuit consists of a differential amplifier followed by a closed-loop op amp with gain of about $1+\frac{R_1}{R_2}$. Splitting the gain among two stages in this way

increases the bandwidth, or speed of the circuit as opposed to having all the gain provided by a single stage.

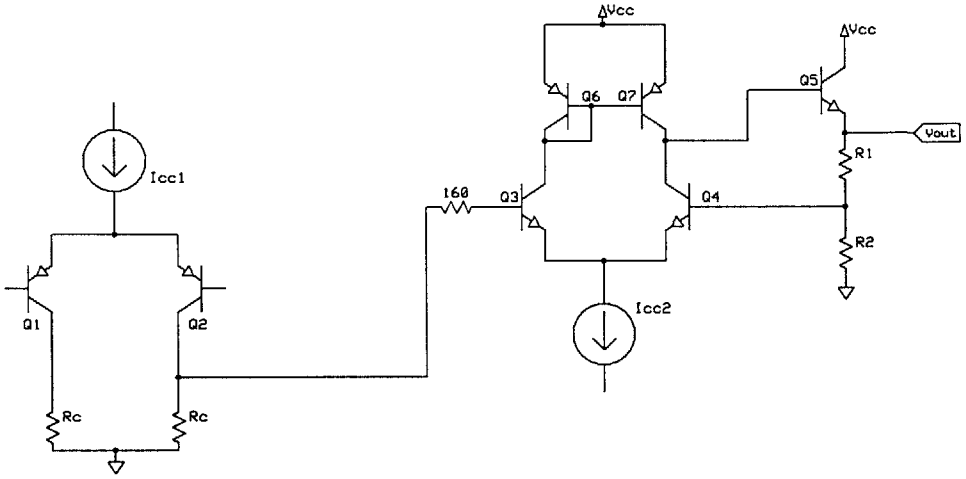

Figure 4-23. Closed-loop implementation of current sense amplifier.

Transconductance Amplifier

A transconductance amplifier takes a voltage input and produces an output current. The output current is proportional to the input voltage by a factor, G_m, which is the transconductance of the amplifier. Figure 4-24 contains a schematic. A transconductance amplifier is a good choice for our current sense application because it is a fairly straightforward circuit that takes in a differential voltage, such as the voltage across the current sense resistor, and outputs a current, which can be easily converted to a voltage by putting it through a resistive load. Additionally, the transconductance amplifier exhibits a much faster response than a closed loop voltage amplifier as can be seen from the fall times of the waveforms in Figure 4-25.

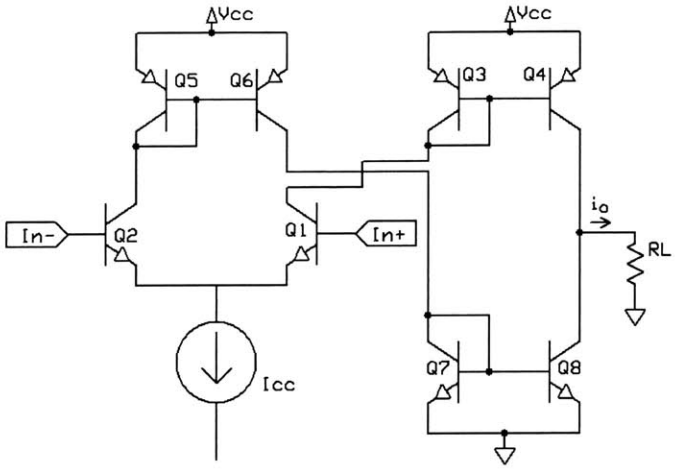

Figure 4-24. Schematic of transconductance amplifier with load resistor, R_L.

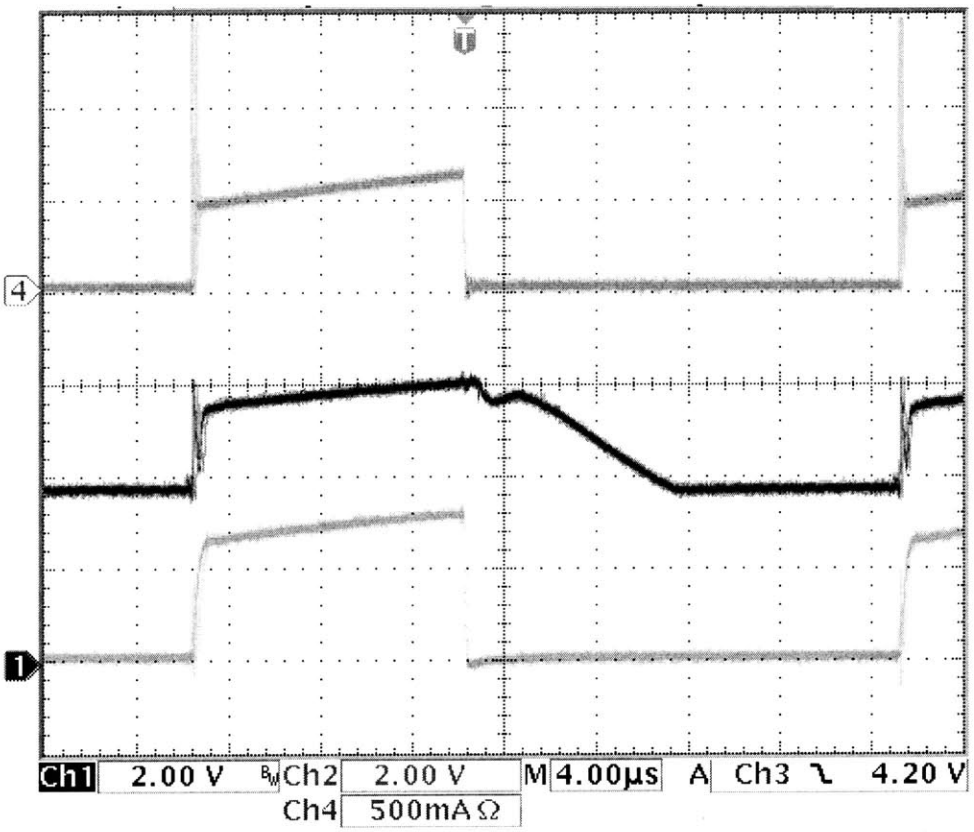

Figure 4-25. Waveforms of the current through the current sense resistor, the output of the closed loop current sense amplifier, and the transconductance amplifier. The transconductance amplifier exhibits a much faster response (fall time).

Assume a differential voltage, v_d, is applied across the input terminals. The v_{BE} of Q_1 increases by $\frac{1}{2}v_d$ and the v_{BE} of Q_2 decreases by $\frac{1}{2}v_d$. As a result, the current through Q_1 increases by $\frac{1}{2}v_d g_m$ and the current through Q_2 decreases by the same amount. Because the collectors of Q_1 and Q_3 are connected, the current through Q_3 must also increase by $\frac{1}{2}v_d g_m$. By the same argument, there is a decrease in the current through Q_5. Transistors Q_3 and Q_4 form a current mirror, which means the current through Q_4 is forced to increase by $\frac{1}{2}v_d g_m$ as well. Likewise, the current mirror formed by Q_5 and Q_6 forces the current through Q_6, Q_7, and Q_8 to decrease by $\frac{1}{2}v_d g_m$. At the output node, the increase in Q_4's current and the decrease in Q_8's current result in a net output current of

$$i_o = i_{c4} - i_{c8}.$$

Substitution yields

$$i_o = \frac{1}{2}g_m v_d - \left(-\frac{1}{2}g_m v_d\right) \tag{4.28}$$

$$= g_m v_d.$$

If a resistive load, R_L, is connected at the output, the output voltage and net voltage gain of the circuit are

$$v_{out} = i_o R_L$$

$$= g_m v_d R_L,$$

$$a_v = \frac{v_{out}}{v_d} = g_m R_L.$$

Recall that g_m is inversely proportional to temperature. Thus the gain of this amplifier is inversely proportional to temperature. This means the slope of the output from the current sense amplifier changes with temperature. We can counteract this unwanted temperature dependence by using a PTAT current source, as described in section 3.1, for I_{CC}.

As mentioned in the discussion of differential pair amplifiers in section 3.4, this amplifier only behaves linearly over a small range (about 25mV) of differential input voltages. With a peak inductor current of 550mA and a current sense resistor of 0.33Ω, we need to be able to linearly amplify differential inputs in excess of 180mV (with the voltage divider reducing the common mode input by a factor of 2, the maximum differential input is actually about 90mV). To extend the linear range, emitter resistors can be added as in Figure 4-26. These resistors also reduce the gain by approximately the same factor that they increase the linear range by (approximately $\frac{I_{CC} R_e}{2V_T}$) so we must account for this attenuation in our calculation of the amplifier's gain.

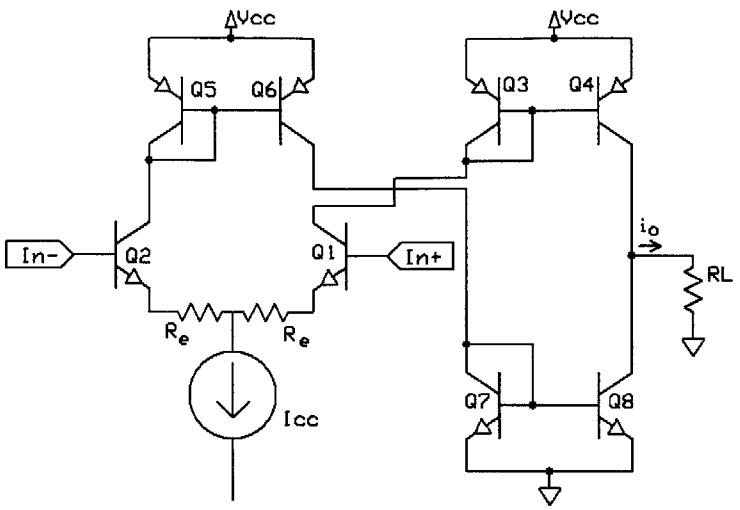

Figure 4-26. Transconductance amplifier with emitter resistors to extend linear range.

Design Calculations

To extend the linear range of the amplifier by 10 to about 250mV requires

$$\frac{I_{CC} \cdot R_E}{2V_T} = 10$$

or equivalently,

$$I_{CC} R_E = 500mV$$

Assuming $I_{CC} = 4mA$, this implies

$$R_E \approx 125\Omega$$

If $I_{CC} = 4mA$, then $I_C = \frac{I_{CC}}{2} = 2mA$. The transconductance is

$$g_m = \frac{I_C}{V_T}$$

$$= \frac{2mA}{25mV} \approx 0.08$$

In order to get a gain of about 40 from the amplifier, taking the factor of 10 attenuation due to the emitter resistors into consideration, we require

$$g_m R_L = 0.08 \cdot R_L \approx 400$$

which implies

$$R_L \approx \frac{400}{0.08} \approx 5k\Omega$$

The larger R_L, the slower the amplifier will be. We can make adjustments and tradeoffs between R_L, I_{CC}, and R_e to ensure that the amplifier's response is fast enough while maintaining enough gain and linear range.

Slope Compensation

As discussed in Section 2, our system under peak current mode control is not stable when operating at duty cycles of greater than 50%. The method for removing this instability is to introduce a slope compensation ramp. The compensation ramp is summed with the current sense waveform at the PWM comparator's non-inverting input. We can use the voltage across the capacitor in the oscillator circuit to create our ramp.

The capacitor voltage should be connected to an EF buffer so that it won't be disturbed. We connect a capacitor to the output of the EF to block the DC component then resistively sum the remaining AC component with the output from the current sense amplifier. This slope compensation scheme is illustrated in Figure 4-27.

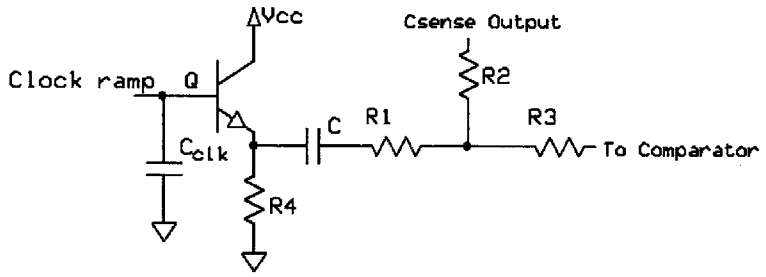

Figure 4-27. Circuit for generating slope compensation ramp.

4.7 Logic and RS Latch

Logic

Digital logic circuits take a binary input of either low or high and similarly, produce an output that is low or high. Often, complementary (n-type and p-type) MOS devices are used to implement logic circuitry on an IC because they are smaller and dissipate less power than bipolar junction transistors. Input voltages below the threshold voltage of the n-type FETs are considered logic low and those above the threshold set by the threshold voltage of the p-type device are logic high. CMOS circuits produce a low output of approximately 0V and a high output approximately equal to the supply voltage, which we will assume to be 5V. See Section 7.1 for symbols, truth tables, and circuit implementations for several common combinational logic gates.

RS Latch

Our control circuit has two states of operation. The first state is triggered by a clock pulse. In this state, the high side FET is on and the inductor current is ramping up. The second state is triggered by a pulse from the comparator when the voltage output of the current sense amplifier exceeds that of the error amplifier. In the second state, the low side FET is on and the inductor current is ramping down. An RS latch serves as a memory device, allowing the circuit to maintain its present state after the signal that triggered the state is no longer being applied.

An RS latch implemented with NOR gates is illustrated in Figure 4-28. The inputs, labeled R and S, are the command signals that set and reset, respectively, the primary output, Q. The other output, Q', is an inverted version of Q. Assume both inputs are low. When S goes high, Q' goes low. Q is high because both R and the other input Q' are low. If S is switched low, Q' remains unchanged because the other input to the NOR gate, Q, is still high. Thus there is no change in the circuit's state although the command signal that triggered the state is no longer being applied. If R goes high, Q goes low. This causes Q' to go high because S is still low. Again, we can see that switching R back low has no affect on the state of the outputs. If both R and S are high, both Q and Q' will be low and the circuit will no longer function properly.

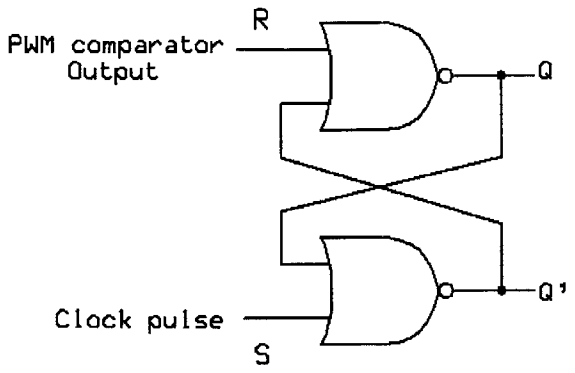

Figure 4-28. RS Latch implemented with NOR gates.

For our RS latch, the clock pulse will be the set the latch and the output of the comparator will reset it. The output, Q, will be used to signal the gate drive circuitry that the high side FET should be on. By taking the signal from Q, as opposed to Q', we have made the latch reset dominant. This means that anytime R is high, which occurs when the inductor current is too high, the output will be low, regardless of the value of S. This is a safety feature to ensure that the high side FET will be shut off when the inductor current becomes too large. To prevent the latch from behaving unpredictably in the case that both R and S are high at the same time, we include the AND gate in Figure 4-29. The AND gate takes Q and the inverse of the clock pulse as input and its output goes to the gate drive circuitry. The AND gate ensures that the high side FET will not be turned on until after the clock pulse. This prevents the occurrence of a situation wherein the signal to the gate drive circuitry may be incorrect because both inputs to the latch went high simultaneously. A schematic for the CMOS implementation of the RS latch is shown in Figure 4-30.

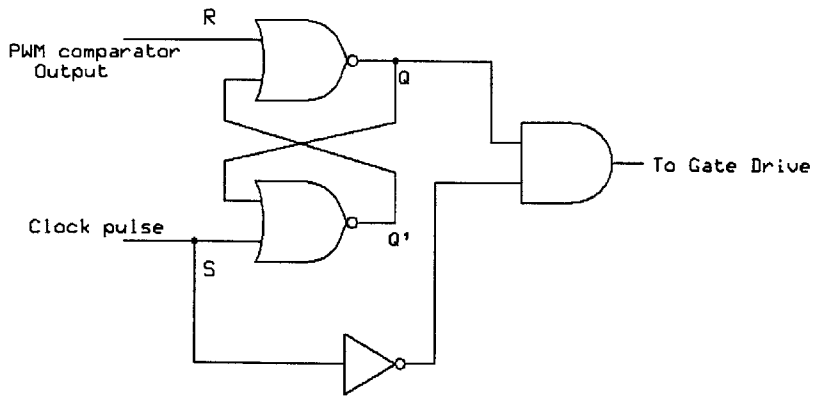

Figure 4-29. RS latch circuit with AND gate to keep high-side MOSFET from turning on until after the clock pulse.

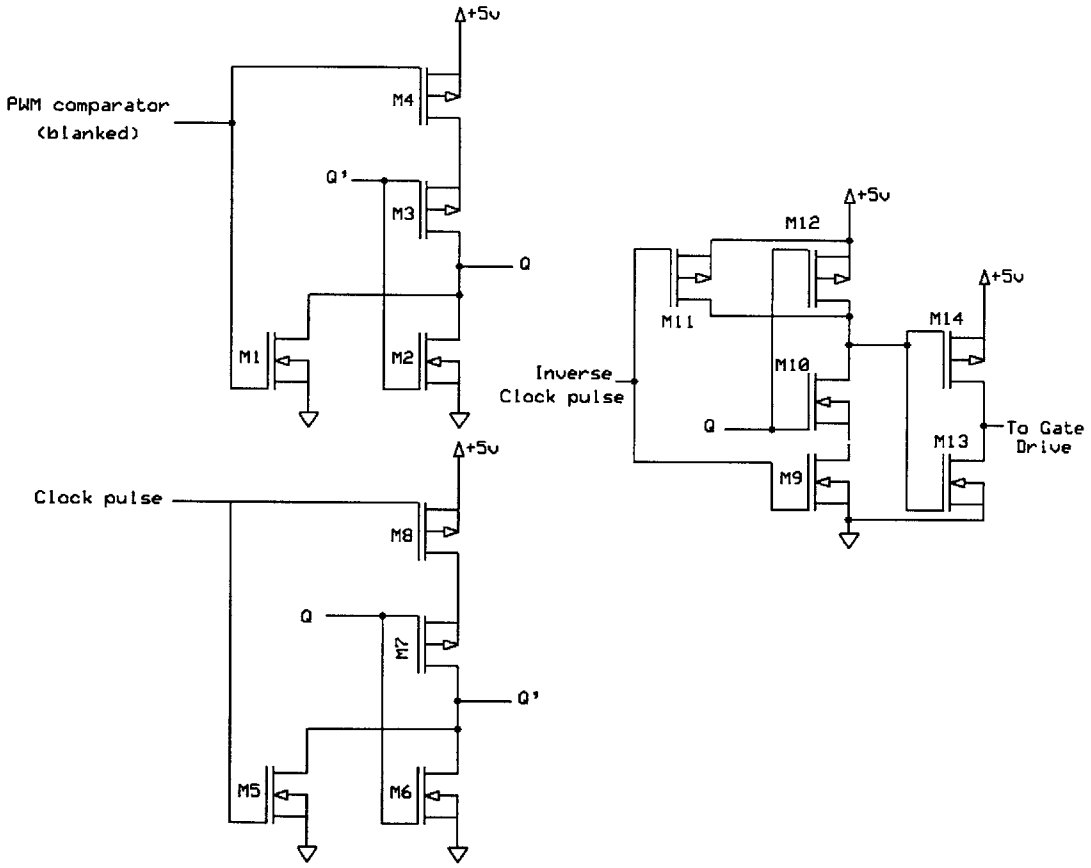

Figure 4-30. CMOS implementation of RS latch circuit.

4.8 Leading Edge Blanking

When the high side FET is turning on, charging of parasitic capacitances associated with the FET, in addition to interactions between other parasitic elements, creates a significant amount of noise and a large spike in the current flowing through the FET. Figure 4-31 shows the waveform of the current flowing through the current sense resistor and the FET. This current spike causes a spike in the voltage seen by the current sense amplifier and could result in the false triggering of the PWM comparator, making it impossible for the control circuit to turn the high side FET on long enough each period for the proper output voltage to be maintained.

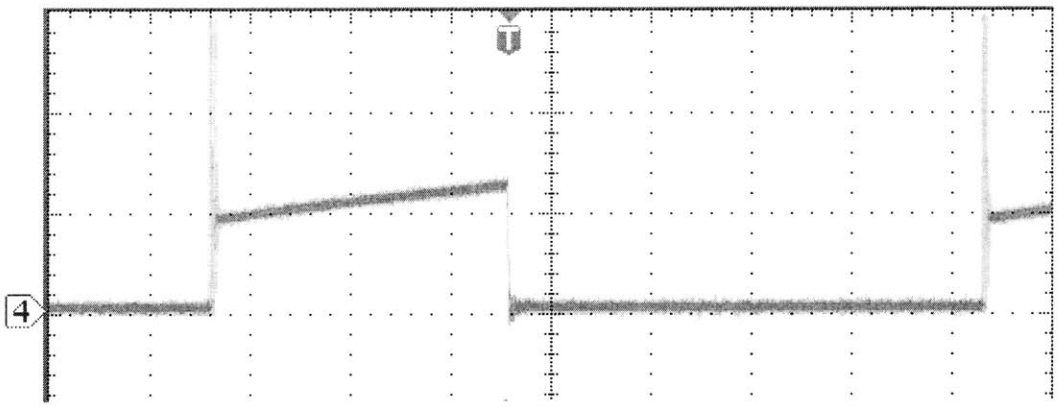

Figure 4-31. There is a large spike in the current through the high-side switch as it turns on at the beginning of each period.

It is often possible to attach a resistor and capacitor to the output of the current sense amplifier creating a low pass filter to reduce the high frequency noise in the signal and hopefully get rid of any large spikes that may falsely trigger the comparator. This is done by choosing the corner frequency of the low pass filter, approximated as

$$f_{3dB} = \frac{1}{2\pi \cdot R \cdot C},$$

to be much lower than the frequency at which the noise occurs so the noise will be filtered out. The corner frequency must be higher than the switching frequency, however, so the amplifier's output can still follow its input signal accurately.

An alternative to the use of an RC filter for dealing with the noise is to blank the output of the comparator for a specified amount of time every period when the high side FET turns on so that the comparator can not trigger the reset of the latch during that time. This technique, known as Leading Edge Blanking (LEB), can be accomplished with a blanking pulse, similar to the clock pulse. We cannot directly use the clock pulse, however, because we have designed our circuit so that the high side FET doesn't begin to turn on until after the clock pulse. So ideally, the blanking pulse needs to be a delayed version of the clock pulse or some pulse that is triggered by the falling edge of the clock pulse. If we produce an inverted version of the blanking pulse that was just described and use an AND gate to combine it with the output from the PWM comparator, as in Figure 4-32, the comparator will not be able to reset the latch for the duration of the blanking pulse, which ideally is the same as the duration of the noise we are trying to blank out.

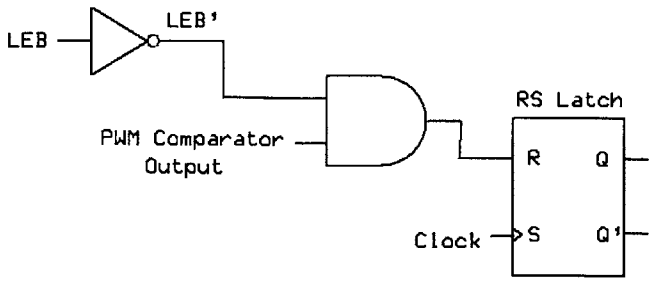

Figure 4-32. Inverse Leading Edge Blanking pulse prevents comparator from resetting latch for a specified amount of time at the beginning of every switching period.

Consider the circuit in Figure 4-33. The voltage across the capacitor will be a delayed version of the clock pulse. By connecting the capacitor to the clock pulse via two different resistors with diodes to control the direction of current flow, the amount by which the rising and falling edges are delayed can be set independently. Assume that R_1 and R_2 are chosen such that the rising edge is delayed just a small amount, but the falling edge is delayed by the desired duration of the blanking pulse. This capacitor voltage will serve as our blanking pulse. The transistors M_1 and M_2 form a CMOS inverter which provides an inversion so the output is an inverted blanking pulse that can be combined with the PWM comparator output via an AND gate as shown in Figure 4-32. Calculations to determine appropriate values for the capacitor and resistors are demonstrated below.

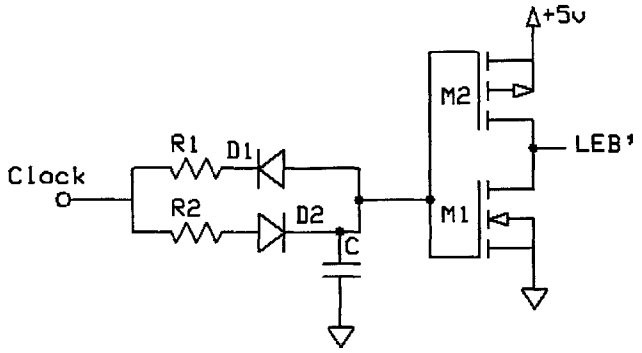

Figure 4-33. Inverse LEB pulse generated from the clock pulse.

Design Calculations

Assume that the duration of the clock pulse is 200ns and that the noise on the leading edge of the current sense output also lasts about 200ns. We will design our LEB pulse to be the clock pulse with rising edge delayed by about 50ns and falling edge delayed by about 250ns. The capacitor charges through R_1 according to the relation

$$v_C = v_f + (v_i - v_f)e^{-t/R_1C}. \tag{4.29}$$

The capacitor is charging from about 0.6V to 4.4V due to the voltage drops across the diodes. The threshold voltage for the pMOS device (ZVP4105A) is about -2V. The threshold voltage for the nMOS device (2N7000) is about 2.1V. This means the capacitor voltage must increase to about 3V (assuming a 5V supply) before M_1 is on, M_2 is off, and the inverse blanking pulse is initiated. We plug the initial and final values into (4.29) to

determine the values of R_1 and C necessary for the capacitor voltage to charge to 3V in about 50ns.

$$3V = 4.4V + (0.6V - 4.4V)e^{-50ns/R_1C}.$$

Manipulating then taking the natural logarithm of yields

$$\ln\left(\frac{3V - 4.4V}{0.6V - 4.4V}\right) = -\frac{50ns}{R_1C}.$$

We can solve for R_1C as follows

$$R_1C = -\frac{50ns}{\ln\left(\frac{3V - 4.4V}{0.6V - 4.4V}\right)}$$

$$\approx 5.0\times10^{-8}.$$

Choosing C to be 100pF implies R_1 should be approximately 500Ω. We can go through a similar procedure to determine R_2 such that the capacitor voltage discharges from 4.4V to the threshold of 2.1V in about 250ns.

$$2.1V = 0.6V + (4.4V - 0.6V)e^{-250ns/R_2C}$$

Manipulating then taking the natural logarithm of yields

$$\ln\left(\frac{2.1V-0.6V}{4.4V-0.6V}\right)=-\frac{250ns}{R_2C}.$$

We can solve for R_1C as follows

$$R_1C=-\frac{250ns}{\ln\left(\frac{2.1V-0.6V}{4.4V-0.6V}\right)}$$

$$\approx 2.69\times10^{-7}.$$

Since we have already chosen C to be 100pF, we can solve the expression for R_1. The result is that R_1 needs to be about 2.69kΩ. The component values for our LEB circuit are summarized below.

$$C=100pF$$
$$R_1=510\Omega$$
$$R_2=2.7k\Omega$$

4.9 Gate Drive

The signal from the RS latch tells us when the converter's MOSFETs should be switched on and off. We need a gate drive circuit to take this 0-to-5V logic signal and convert it into a larger magnitude signal that is capable of sourcing and sinking the current necessary to charge and discharge the MOSFET gate capacitors. An example of a MOSFET gate driver is shown is Figure 4-34. The signal PWM is the logic output from

the RS latch signaling when the FET should be turned on. When PWM is high, Q_1 is on and Q_2 is off. The voltage at the node where the emitters of Q_1 and Q_2 connect, V_m, increases to approximately V_{CC} and charge is pulled from C to charge up the FET's gate. The gate to source voltage of the FET, M, increases and the switch turns on. When PWM goes low, Q_1 turns off and Q_2 turns on. The voltage V_m goes low (~200mV) and the gate discharges through Q_2, turning off M. A resistor, R_g, is connected between the gate drive circuit and M's gate to damp out ringing.

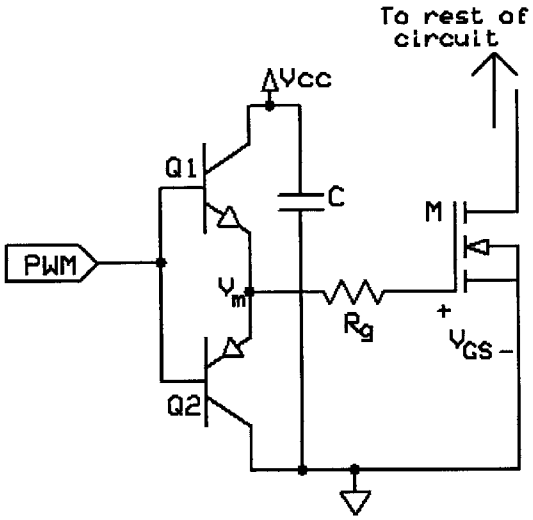

Figure 4-34. Example of a MOSFET gate driver.

The gate drive circuit shown in Figure 4-34 can only be used to drive a MOSFET whose source is connected to ground. If the source of the FET isn't grounded, we need a high-side floating gate driver to drive the gate voltage high enough above the non-grounded source to turn the FET on. A simple high side driver is shown in Figure 4-35.

Assume PWM is low so M_{HS} is off. Then the free-wheeling diode, D, is conducting and the voltage at the node with the source of M_{HS}, V_{src}, is about 0V. C_{bst} charges up through D_{bst} until the voltage across it is approximately V_{CC} (one diode drop less). For PWM low, M_1 is on so current flowing through R_1 and R_2 results in a low voltage at the bases of Q_1 and Q_2, V_m. Thus Q_1 will be off and Q_2 will be on, which confirms that V_{GS} will be below the threshold voltage and M_{HS} will be off. When PWM switches to high, M_1 shuts off and stops current from flowing through R_1 and R_2. This brings V_m high so Q_1 turns on and Q_2 turns off. Charge is pulled from C_{bst} and the gate of the MOSFET begins to charge through Q_1. As M_{HS}'s V_{GS} increases, the inductor current is transferred from D to M_{HS}. When the inductor current has fully transferred to M_{HS}, D turns off and V_{src} increases to approximately V_{in}. Because the voltage across C_{bst} remains unchanged, the voltage at the collector of Q_1 is now approximately V_{CC} volts above the input voltage. This occurrence is known as bootstrapping. The capacitor C_{bst} is used to create a bootstrap voltage supply that is high enough above the voltage at the source to turn M_{HS} on, although our available external supply, V_{CC}, may not be high enough. Thus, no matter how high V_{in} (and the voltage at the source) is raised, C_{bst} allows the gate voltage to be driven high enough for the high side FET to be on. The difference in voltage between V_{CC} and the bootstrap supply shows up across the reverse biased D_{bst}.

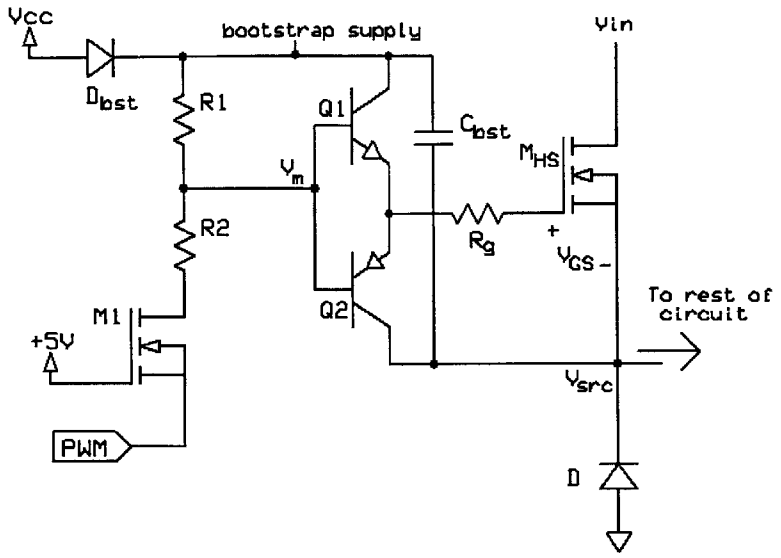

Figure 4-35. Circuit for driving the gate of the high-side MOSFET.

The high side drive circuit in Figure 4-35 has a few disadvantages. Assume PWM is high so M_{HS} is on. When PWM switches low, V_m rapidly goes low. The voltage at the source of M_{HS} decreases slowly, however, as the gate capacitance discharges with some non-zero time constant. So there is a period of time each switching cycle when the base of Q_2 is at a much lower voltage than its collector. The repetitive forward biasing of the base-collector junction damages the transistor and significantly reduces its life expectancy. The structure consisting of an npn transistor on top of a pnp transistor, as Q_1 and Q_2 are in Figure 4-35, is called a push-pull output stage. Currently, integrated designs much more commonly use a totem-pole output stage, that is two npn (or pnp) transistors stacked one above the other. With the totem-pole configuration, the two bases can no longer be tied together because they must be driven by complementary signals. This requires some additional circuitry to invert the PWM signal.

A high-side gate drive circuit that doesn't have the same drawbacks as the one presented in the previous paragraph is shown in Figure 4-36. This circuit uses a

differential pair input stage. The PWM signal from the RS latch is compared against some DC bias voltage, such as 2.5V. When PWM is high, all of the bias current, I_{CC}, flows through Q_1. The voltage drop across R_1 brings the base of Q_3 low enough for Q_3 to conduct. The current flowing through R_3 then brings the voltage at the gate of M_1 high. M_1 turns on and charges the gate of the high-side FET, M_{HS}, switching the FET on. Because there is no current flowing through R_2, the voltage at the base of Q_4 is high and Q_4 is off. This means no current flows through R_4 so the voltage at the gate of M_2 is the same as the voltage at its source and M_2 is off. We can see that when the drive signal goes low, all of I_{CC} flows through Q_2 and going through the same analysis leads us to the result that M_1 is off, M_2 is on, and the gate of M_{HS} discharges through M_2 turning the high-side FET off. Just as in the previous high-side drive circuit, this circuit uses a diode and capacitor to create a bootstrap supply voltage that is capable of driving M_{HS}'s gate high enough above the voltage at its source. Schottky diodes connected to Q_3 and Q_4 prevent the voltage at the base of the transistor from dropping too far below the collector voltage. Schottky diodes are also connected to Q_1 and Q_2 so they aren't driven too far into saturation. When transistors are driven into saturation, in addition to the damage caused to the transistor, the time that it takes them to recover in order to switch states introduces a delay that can significantly reduce the speed of a circuit. By using a differential pair input stage, we get an output from both the collector of Q_1 and Q_2 so we have the two complementary signals required for driving the totem-pole. Note that instead of using a BJT totem-pole output stage, we are using a FET totem-pole output stage and have added transistors Q_3 and Q_4 to drive the totem-pole. This is to increase the current-carrying capability of the output stage so that more current can be supplied to

M_{HS} to charge it quickly. The current to charge the FET is pulled from C_{bst}. We can use the following analysis to determine how large C_{bst} needs to be in order to charge M_{HS} within some specified period of time.

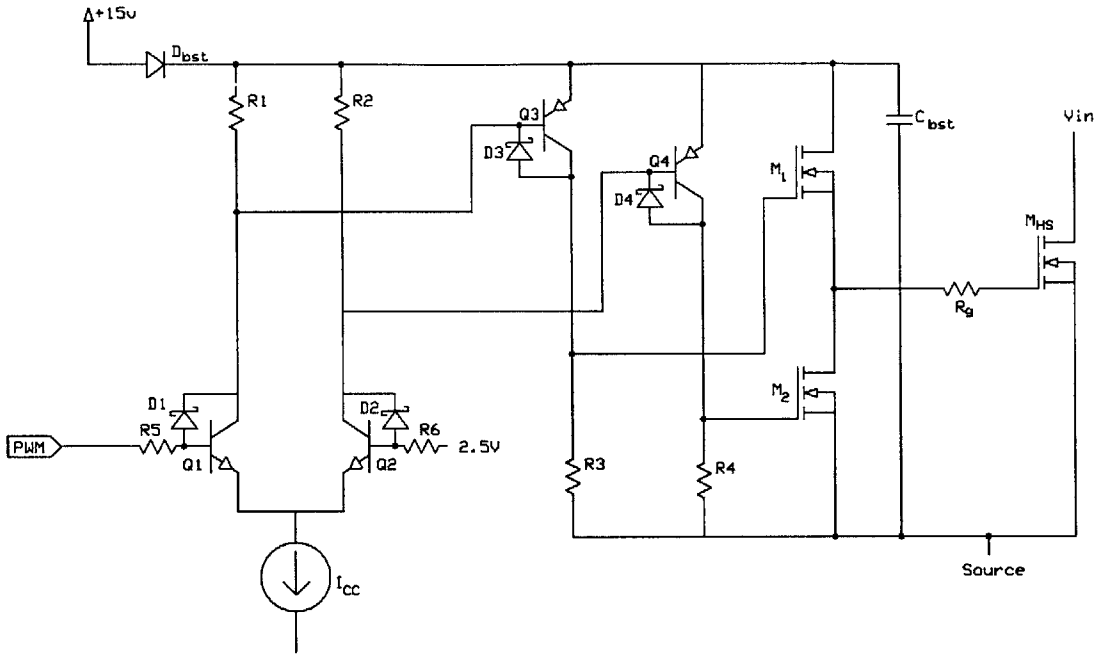

Figure 4-36. Improved high-side gate drive circuit.

The amount of charge needed to turn on the FET depends on the gate capacitance of the FET. The required gate charge, Q_{gate}, is typically specified in the device's datasheet. If the FET needs to be turned on in t_{on} seconds, the current that must flow through M_1 to charge the gate is

$$I = \frac{dq}{qt}$$

$$= \frac{Q_{gate}}{t_{on}}. \qquad (4.30)$$

The bootstrap supply capacitor should maintain a relatively constant voltage across its terminals. There is some ripple in this voltage caused by the current the capacitor supplies to the BJT's and for charging M_{HS}'s gate. Applying the constituitive relation for a capacitor and also the relationship between capacitor voltage and charge, we obtain this expression for the voltage ripple

$$\Delta V = \frac{I}{C \cdot f_s} + \frac{Q_{gate}}{C}, \tag{4.31}$$

where I is the sum of the bias current in the differential pair and the current flowing through Q_3 and Q_4, f_s is the switching frequency set by the clock, and Q_{gate} is the charge required to turn on M_{HS}. Setting a maximum value for ΔV yields a minimum value for the capacitor. The value for C_{bst} chosen when designing the gate drive circuit should be at least twice as large as the minimum value calculated to account for charges and currents that may not have been considered (such as charging the gates of M_1 and M_2) and to ensure that there will be enough charge to turn M_{HS} completely on.

The high-side drive circuit in Figure 4-36 can be modified to drive the low side FET as well. The blocking diode, D_{bst}, is no longer necessary and all the components connected to the source of the converter FET are also connected to ground. The circuit is shown in Figure 4-37. The input from the RS latch to the low side drive circuit needs to be an inverted version of the input to the high side drive circuit. This can be accomplished with an inverter or alternatively, the RS latch signal can be applied to Q_2 and the 2.5V bias can be applied to Q_1. Switching the inputs in that way would result in

the high-side FET and low-side FET being controlled by complementary switching signals. As in the high side circuit, the capacitor C provides current to charge M_{LS}'s gate. (4.31) can be applied here also to determine the minimum value for C.

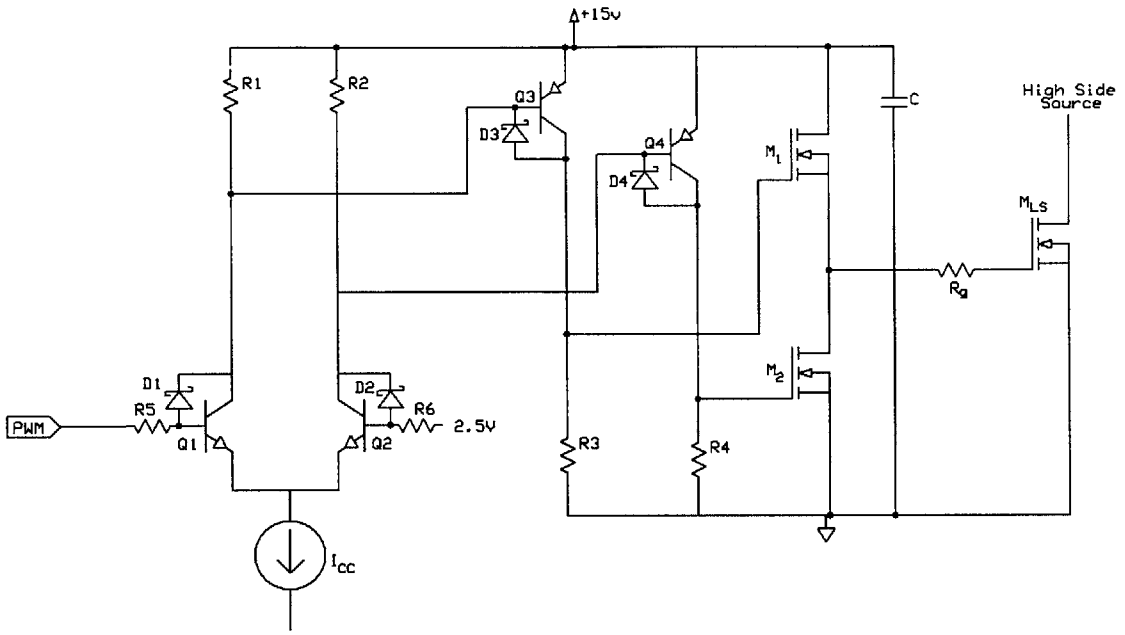

Figure 4-37. Low-side gate drive circuit analogous to the high-side circuit of Figure 4-36.

Shoot-Through Protection

The gate drive circuitry should control the switches in a manner that ensures that each FET is turned off before the other is turned on. While the signals to the FET gates are inverted versions of each other, the time it takes the switch to turn completely on or off is non-negligible and during the switching instances, there is a period of time when both FETs will be on simultaneously, shorting the input voltage to ground. This occurrence is termed shoot-through.

In order to prevent shoot-through, we would like to implement some circuitry to determine that the high side (or low side) FET has completely turned off before turning on the low side (or high side) FET. This can be accomplished with a circuit that indicates whether or not the gate to source voltage (V_{GS}) of the FET is above some level. The output of this V_{GS} sensing circuit would then serve as input, along with the drive signal from the RS latch, to some logic circuitry that will determine when it is safe and appropriate to turn on the FET. We will use a NAND gate to determine when the FET should be turned on, based on outputs from the RS latch, the shoot-through protection circuitry, and any other relevant signals. This logic is "active low" because the NAND gate requires that all inputs be low for it to produce a high output, signaling that the FET is to be turned on.

Consider the high side V_{GS} sensing circuit in Figure 4-38. The base-emitter junction of Q_1 is used to sense V_{GS} of the high side FET. Because β is large, base current can be neglected. This implies that there is no voltage drop across R_3 and so V_{BE} is equal to V_{GS}. When the FET is on, V_{GS} is greater than 0.6V so Q_1 is on and conducts current. This current results in the voltage at the base of Q_2 being about 1.2V (2 diode drops above ground). So Q_2 is on, which means the voltage at the base of Q_3 is low. This means that Q_3 is off and the output at its collector is high. Thus, when the FET is not completely off (as indicated by V_{GS} being above a certain threshold), the signal going to the NAND gate will be high, preventing the low side FET from being turned on. When V_{GS} drops below about 0.6V, Q_1 turns off. This causes the voltage at the base of Q_2 to low, turning Q_2 off. The voltage at the base of Q_3 goes high turning Q_3 on and causing the output at Q_3's collector to go low. Thus when V_{GS} is low, indicating that the FET has

completely turned off, a low signal is sent to the NAND gate indicating that it is safe to turn on the low side FET. Because our enable signal is actually of the opposite sign, meaning low to enable and high to disable, the signal is called enable' as indicated in Figure 4-38. The diodes D_1 and D_2 clamp the voltage at the base of Q_2 at about 1.2V. The resistor, R_1, provides a discharge path for parasitic capacitances. The resistor, R_2, prevents too much current from being pulled away from the gate of the FET. The diode, D_3, clamps the voltage drop from the collector to the base of Q_1 so that the transistor doesn't go into severe saturation, causing a delay in the circuit's operation.

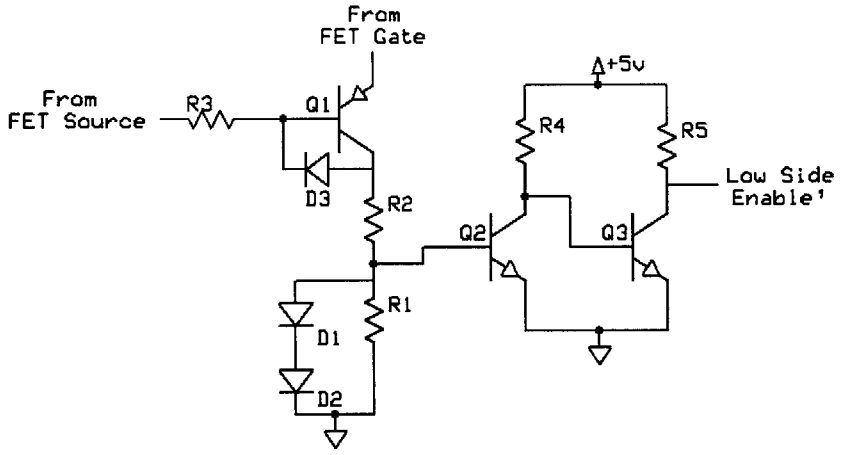

Figure 4-38. This low-side enable' circuit senses V_{GS} of the high-side FET to determine when it is safe to turn on the low-side switch.

To sense V_{GS} of the low side FET, we can use a circuit similar to the one presented in the previous paragraph for the high side. See Figure 4-39. This circuit is more straightforward than the previous one because the source of the FET is grounded. When the V_{GS} of the low side FET is above 0.6V, Q_1 is on, Q_2 is off, and the output signal is high so the high side FET will not be turned on. When V_{GS} of the low side FET drops below 0.6V, Q_1 turns off, Q_2 turns on, and the output signal goes low signaling that

it is ok to turn on the high side FET. For an example on how to choose component values, see the calculations below.

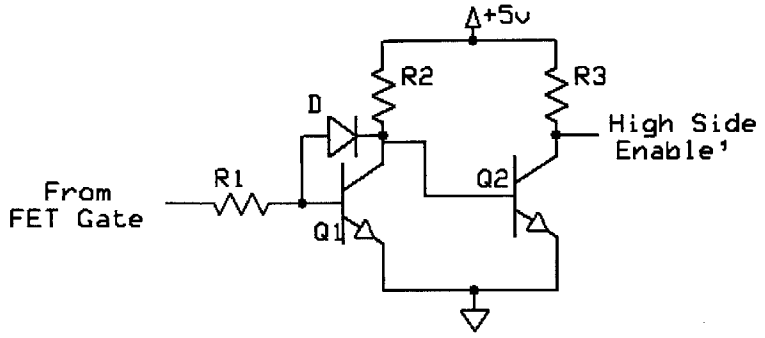

Figure 4-39. This high-side enable' circuit senses VGS of the low-side FET to determine when it is safe to turn on the high-side switch.

Design Calculations

The resistors connected to the bases of the Q_1 transistors in both V_{GS} sensing circuits prevent a voltage source from being applied directly across the base-emitter junction of the transistors. These resistors should be small, on the order of about 100Ω. The load resistors on the CE stages should be about 10kΩ so they don't dissipate too much power. In the high-side circuit, R_2 of Figure 4-38 needs to be large to prevent too much current from being drawn away from the FET's gate. When Q_1 is on, the current flowing through R_1 is

$$I_{R1} = \frac{V_{R1}}{R_1}$$

$$= \frac{1.2V}{R_1}. \qquad (4.32)$$

The current flowing into the base of Q_2 is

$$I_{B2} = \frac{I_{C2}}{\beta_0}.$$

Assuming R_4=10kΩ,

$$I_{B2} \approx \frac{5V \div 10k\Omega}{200}$$

$$\approx 2.5\mu A.$$

The remainder of the current flowing through Q_1 and R_2 flows through diodes D_1 and D_2. The total current though R_2 varies with voltage at the gate of the FET according to the following expression.

$$I_{R2} \approx \frac{V_{gate} - V_{DS,sat} - 1.2V}{R_2}$$

$$\approx \frac{V_{gate} - 200mV - 1.2V}{R_2} \qquad (4.33)$$

Depending on the voltage at the gate, which is determined by the input voltage to the converter, we can use (4.32) and (4.33) to choose values for R_1 and R_2 such that the current through R_2 is acceptably small, but enough to supply Q_2's base current and provide a 1.2V drop across R_2. Reasonable values are:

$$R_1 = 51k\Omega$$
$$R_2 = 100k\Omega$$

4.10 Protection Circuits

Shutdown Capability

Control IC's typically have a shutdown capability which allows the user to disable the chip by applying some signal (high or low, depending on the design) to a designated shutdown pin. We would like to include a similar capability in our circuit. One option is to modify the AND gate at the output of the RS latch to be a 3-input AND gate with one input serving as the shutdown pin. The idea is illustrated in Figure 4-40. This can be accomplished rather easily by placing an additional n-type MOSFET, M_3, in series with the two n-type MOSFETs, M_1 and M_2, in the NAND gate and an additional p-type MOSFET, M_6, in parallel with M_4 and M_5. A schematic for the modified AND gate is shown in Figure 4-40. This circuit effectively creates an inverse shutdown pin. By tying this pin to +5V, the control circuit is enabled and functions normally. If the voltage at this pin is lowered to 0V, the PWM output is lowered to 0V limiting the duty ratio and converter output to 0 until the pin voltage is brought high again.

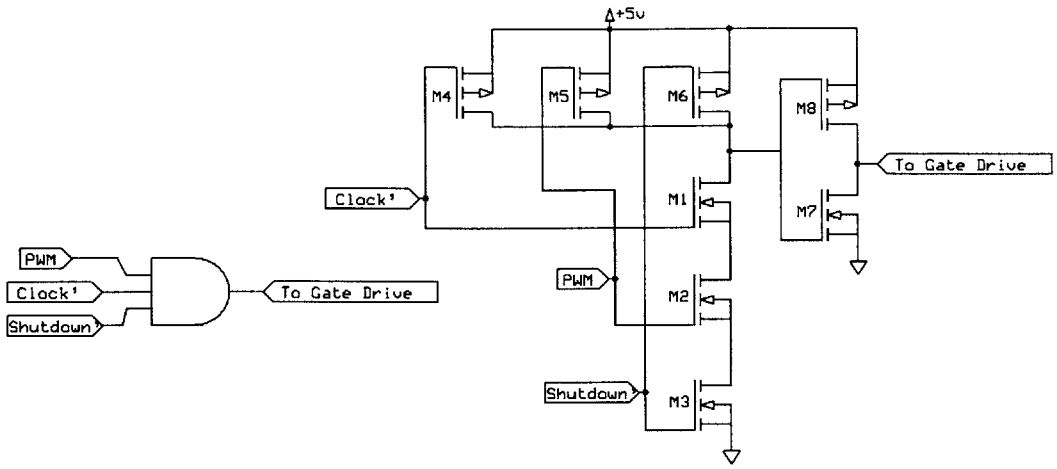

Figure 4-40. Adding an additional input to the AND gate of the RS latch provides shutdown capability for the control circuit.

Under-Voltage Lockout

We would like to incorporate an under-voltage lockout feature into our controller to shutdown the control circuitry when the input voltage to the converter goes below a certain level. This can be accomplished with a comparator whose inputs are a scaled version of the input voltage and our low voltage threshold. Using hysteresis to create 2 different levels for the low voltage threshold, as described in Section 4.3, we minimize the likelihood of noisy signals causing the comparator output to oscillate. The output of the comparator is an UVLO pulse that can be combined with the shutdown function presented in the previous sub-section to form a shutdown signal to send to the AND gate of the RS latch. A schematic is shown in Figure 4-41. When the input voltage is above the threshold voltage set at the comparator's positive input terminal, the comparator output is low. So the inverted output connected to the AND gate is high. The output of this AND gate is the inverted shutdown signal that is sent to the RS latch. So when the converter's input voltage is high enough, the RS latch is enabled. The voltage at the

positive input terminal of the comparator is the low threshold voltage. When the converter's input voltage goes below the threshold, the comparator output switches to high. This causes the voltage at the comparator's positive input terminal to increase to the high threshold voltage. The input to the AND gate is now low, so a low signal is sent to the AND gate of the RS latch effectively shutting off the converter.

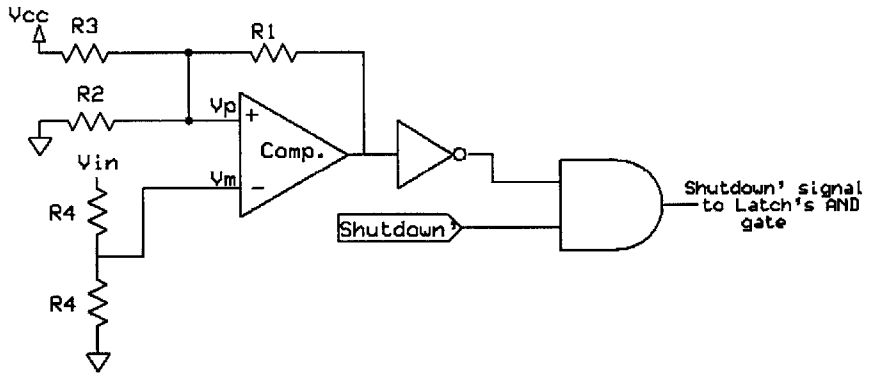

Figure 4-41. Under-voltage lockout circuit for the converter's input voltage.

Assume we use 15V for V_{CC} in Figure 4-41. Modifying expressions (4.20) and (4.21) from Section 4.3 results in the following equations for the high and low threshold voltages.

When the comparator output is high:

$$V_p = 15V\left(\frac{R_1 \parallel R_2}{R_3 + R_1 \parallel R_2}\right) + 5V\left(\frac{R_2 \parallel R_3}{R_1 + R_2 \parallel R_3}\right) = V_{T,high}. \qquad (4.36)$$

When the comparator output is low:

$$V_p = 15V\left(\frac{R_2 \parallel R_1}{R_3 + R_2 \parallel R_1}\right) = V_{T,low}. \tag{4.37}$$

Let's set the minimum input voltage at 7V. Since the maximum input voltage of 20V is well beyond the common mode range of our comparator, we will use a voltage divider to cut the input voltage in half. This means the low voltage threshold should be set at half of 7V, or 3.5V. To establish a significant hysteresis margin, we will require that the input voltage be raised above 10V to enable the RS latch after it has been shut down due to low input voltage. This means the high voltage threshold should be set at half of 10V, or 5V. We can plug these thresholds into (4.36) and (4.37), choose a value for one of the resistors, and solve for the other 2. If we set R_1=10kΩ, the following calculations result:

$$V_{T,high} = 5V = 15V\left(\frac{R_1 \parallel R_2}{R_3 + R_1 \parallel R_2}\right) + 5V\left(\frac{R_2 \parallel R_3}{R_1 + R_2 \parallel R_3}\right)$$

Dividing both sides by 5 and substituting for R_1 yields,

$$1 = 3 \cdot \left(\frac{10k\Omega \parallel R_2}{R_3 + 10k\Omega \parallel R_2}\right) + \left(\frac{R_2 \parallel R_3}{10k\Omega + R_2 \parallel R_3}\right).$$

Explicitly writing out the expressions for the parallel resistor combinations gives us

$$1 = 3\frac{\frac{R_2 \cdot 10k\Omega}{10k\Omega + R_2}}{R_3 + \frac{R_2 \cdot 10k\Omega}{10k\Omega + R_2}} + \frac{\frac{R_2 \cdot R_3}{R_3 + R_2}}{10k\Omega + \frac{R_2 \cdot R_3}{R_3 + R_2}}$$

which can be simplified to

$$1 = \frac{30k\Omega \cdot R_2 + R_2 \cdot R_3}{R_2(R_3 + 10k\Omega) + R_3 \cdot 10k\Omega} \tag{4.38}$$

For the low threshold,

$$V_{T,low} = 3.5V = 15V\left(\frac{R_2 \parallel R_1}{R_3 + R_2 \parallel R_1}\right).$$

Dividing both sides by 15 and substituting for R_1 yields

$$\frac{3.5}{15} = \left(\frac{R_2 \parallel 10k\Omega}{R_3 + R_2 \parallel 10k\Omega}\right)$$

Explicitly writing out the expressions for the parallel resistor combinations gives us

$$\frac{3.5}{15} = \frac{\frac{R_2 \cdot 10k\Omega}{R_2 + 10k\Omega}}{R_3 + \frac{R_2 \cdot 10k\Omega}{R_2 + 10k\Omega}}$$

which can be simplified to

$$\frac{3.5}{15} = \frac{R_2 \cdot 10k\Omega}{R_3(R_2 + 10k\Omega) + R_2 \cdot 10k\Omega} \tag{4.39}$$

Combining (4.38) and (4.39) and solving yields $R_2 \approx 6429\Omega, R3 \approx 12857\Omega$.

Using R_1=10kΩ, R_2=6.2kΩ, and R_3=13kΩ results in $V_{T,low}$=3.41Vand $V_{T,high}$=4.89V. Multiplying these thresholds by 2 gives the minimum V_{in} value before lockout of 6.82V and 9.78V as the minimum input voltage to restore the converter disabled due to low input voltage.

The output stage of the comparator should be an inverter tied to the 5V supply. The on resistance of the output transistor is low compared to the resistor values chosen above, so it shouldn't significantly alter out calculated thresholds. A transistor-level schematic is shown in Figure 4-42.

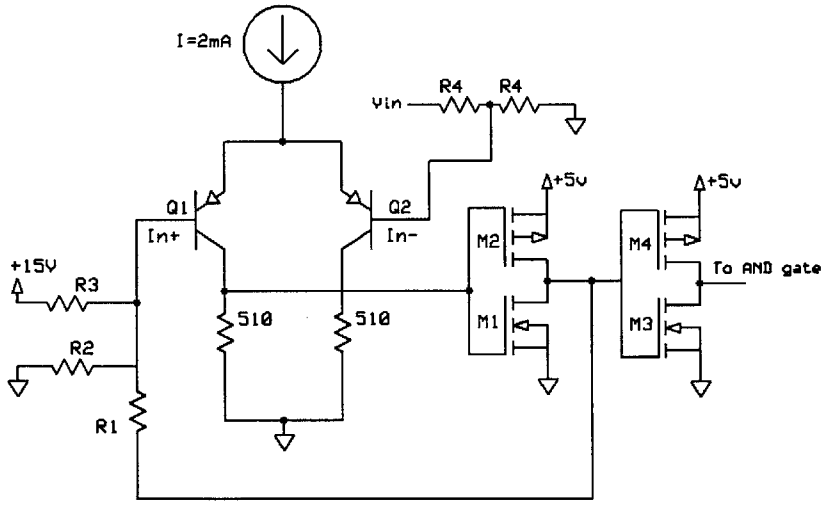

Figure 4-42. Transistor-level schematic of under-voltage lockout circiut.

Over-voltage Protection

We need to include some circuitry to protect the controller from damage due to excessive input or supply voltages. Due to common-mode and power dissipation limitations, the control circuit can not handle input voltages greater than 22V. Placing a 22V zener diode across the input terminals to the converter will clamp the input at 22V. Figure 4-43 contains an over-voltage protection circuit with a 22V zener diode, D_1. When V_{in} becomes too large, D_1 begins to conduct and the voltage at the base of Q_6 increases. This causes Q_6 to turn on and the voltage at its collector, V_{out}, goes low. If we AND this signal, along with the under-voltage signal and that from the user-applied shutdown' signal, the result is a signal that is sent to the RS latch and will shut the converter off if either of three conditions exists: V_{in} is too high, V_{in} is too low, or the user has pressed the "shutdown button". See the illustration in Figure 4-44. A similar configuration with a zener diode can be used to ensure that the supply voltage for the control circuitry doesn't exceed an acceptable level.

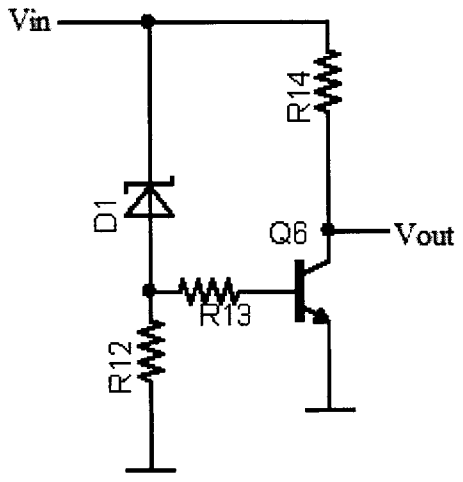

Figure 4-43. Over-voltage protection circuit for the converter's input voltage.

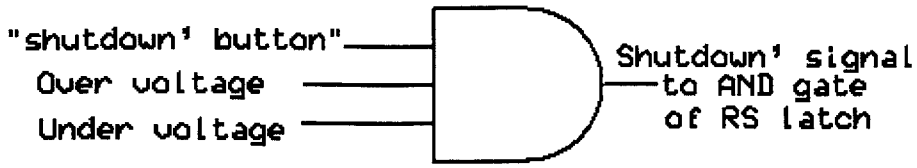

Figure 4-44. Functional diagram of shutdown circuit block.

Control Circuit Supply Voltage

We also need over-voltage protection and under-voltage lockout circuitry for the 15V supply being input to the control circuit. In this case, we can no longer use comparators or logic, because they all require the supply voltage to be correct. Instead, we can use the concept demonstrated in Figure 4-43 for both the over and under-voltage protection. Our circuit is shown in Figure 4-45. When the supply voltage exceeds the threshold set by D_4, as described already, M_2 will be off and so no current will be supplied to the control circuitry. Similarly, D_3 sets the low threshold. When the supply voltage drops below that threshold, D_3 will stop conducting, causing Q_{26} (and M_2) to shutoff.

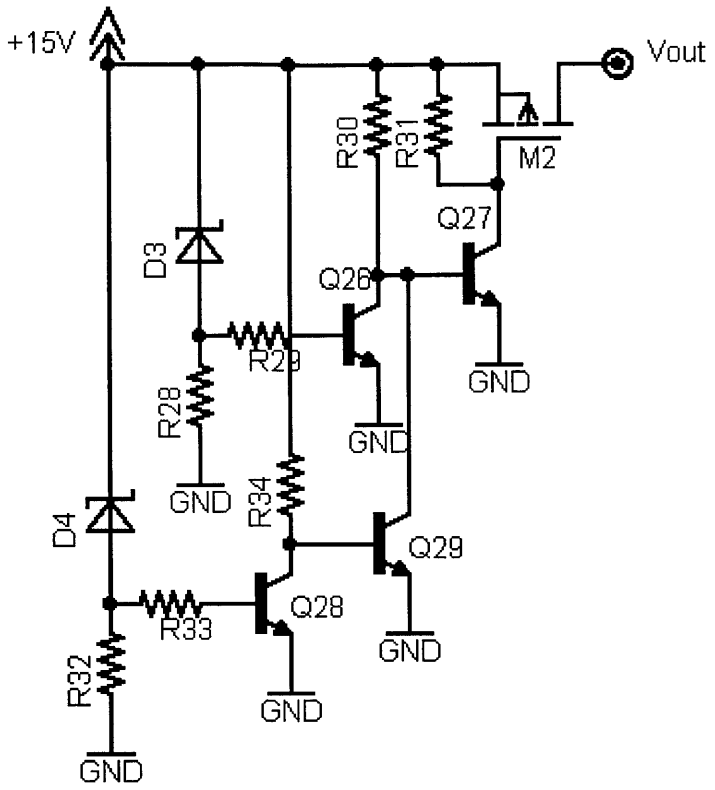

Figure 4-45. Under-voltage and over-voltage protection for control circuit's supply voltage.

5 Results

This project has established the foundation for a new course in power electronic control circuitry. Students will be exposed to a wide range of topics including power electronics, analog circuit design, and the integrated circuit design process. The following list outlines the major areas of emphasis.

- Design Process
  - Hand Calculations
  - Run Simulations
  - Build, Analyze, and Debug
- Analog Circuit Building Blocks
  - Current Sources & mirrors
  - Differential Pair
  - Common emitter amplifier and emitter follower buffer
  - Input, gain, and output stages
- Power Electronics and Control
  - Converter Topology
  - Voltage Control
  - Current Control
  - Transfer function of converter and closed loop system (stability)

We've designed a series of circuits which together perform the function of a current-mode PWM control chip. The prototype controller and converter built produce a 5.04V output and operate over 7V to 20V input range. The output power of the converter is 2.54 Watts and the input power is about 3.03 Watts. That translates to an efficiency of 83.8%. The average inductor current is about 500mA and the current ripple is about 112mA. The output voltage ripple is about 180mV. Figure 5-1 shows waveforms of the inductor current, the output voltage, and the clock pulse.

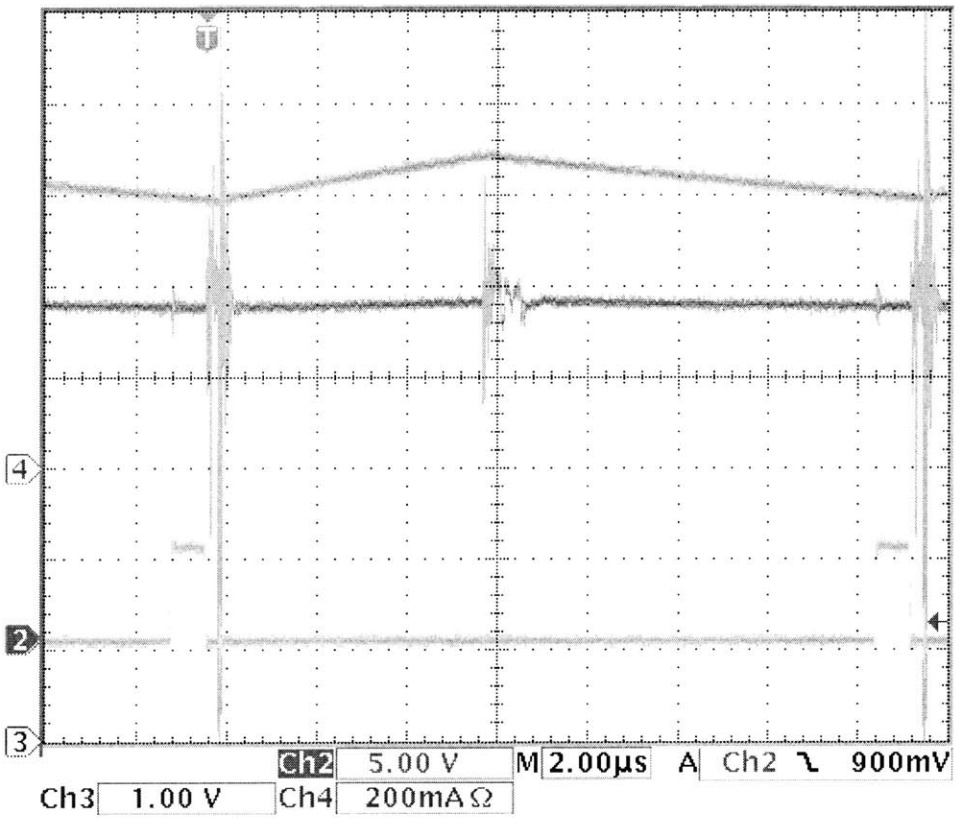

Figure 5-1. Waveforms of inductor current (top), converter output voltage (center), and clock pulse (bottom).

The control circuit has been designed as a modular kit with each functional block on its own removable board. This allows the students to design, build, and test each board individually and also makes it easy for blocks to be replaced. Figure 5-2 shows an example of one of the small circuit blocks.

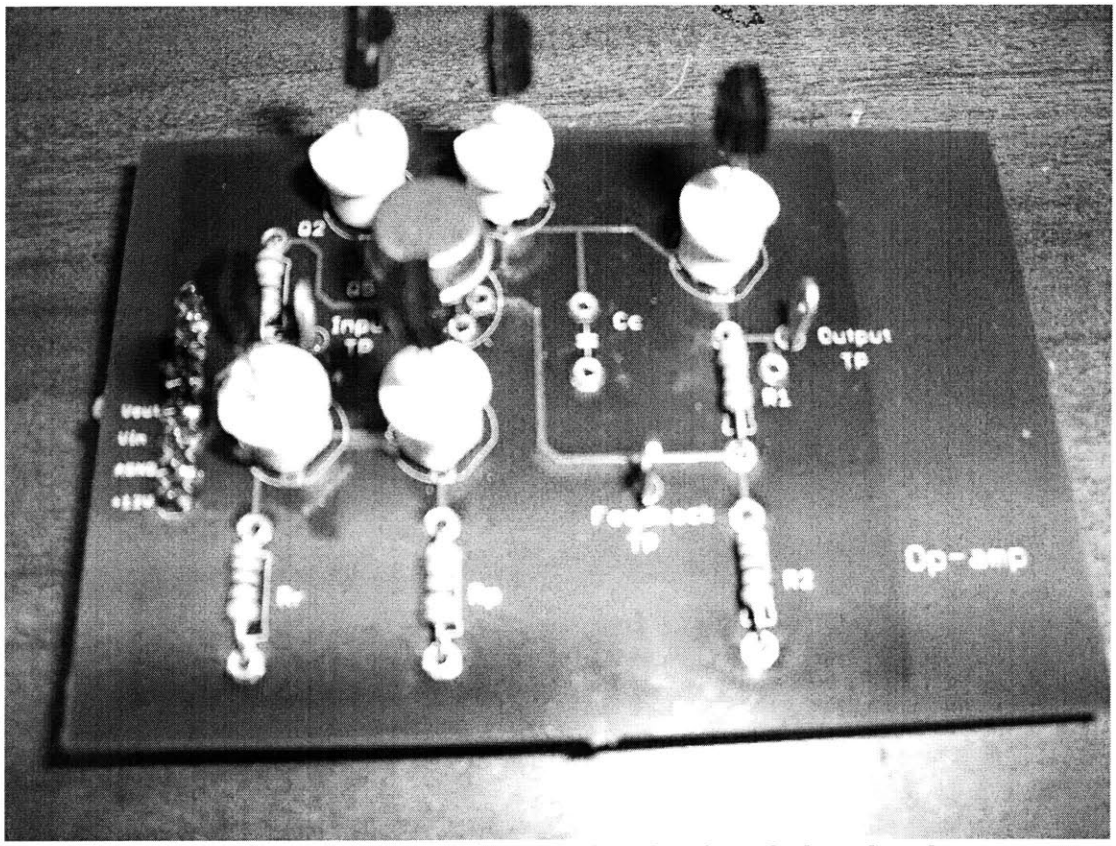

Figure 5-2. Typical 3" x 2" module that plugs in to the large board.

The blocks plug in to the main kit via SIP connectors as illustrated in Figure 5-3. The blocks can be removed and plugged into a breadboard for testing. They also contain switches that isolate the circuit from the SIP connector, allowing the block to be isolated for testing without being physically removed from the main board.

Figure 5-3. Side view of laboratory kit. Individual modules plug in to main board via SIP connector with 0.1" spacing for breadboard compatibility.

A picture of the first prototype is contained in Figure 5-4. The controller consists of about 150 transistors, including CMOS devices. Figure 5-5 shows a breadboard version of the control circuit driving a buck converter built on a totem board.

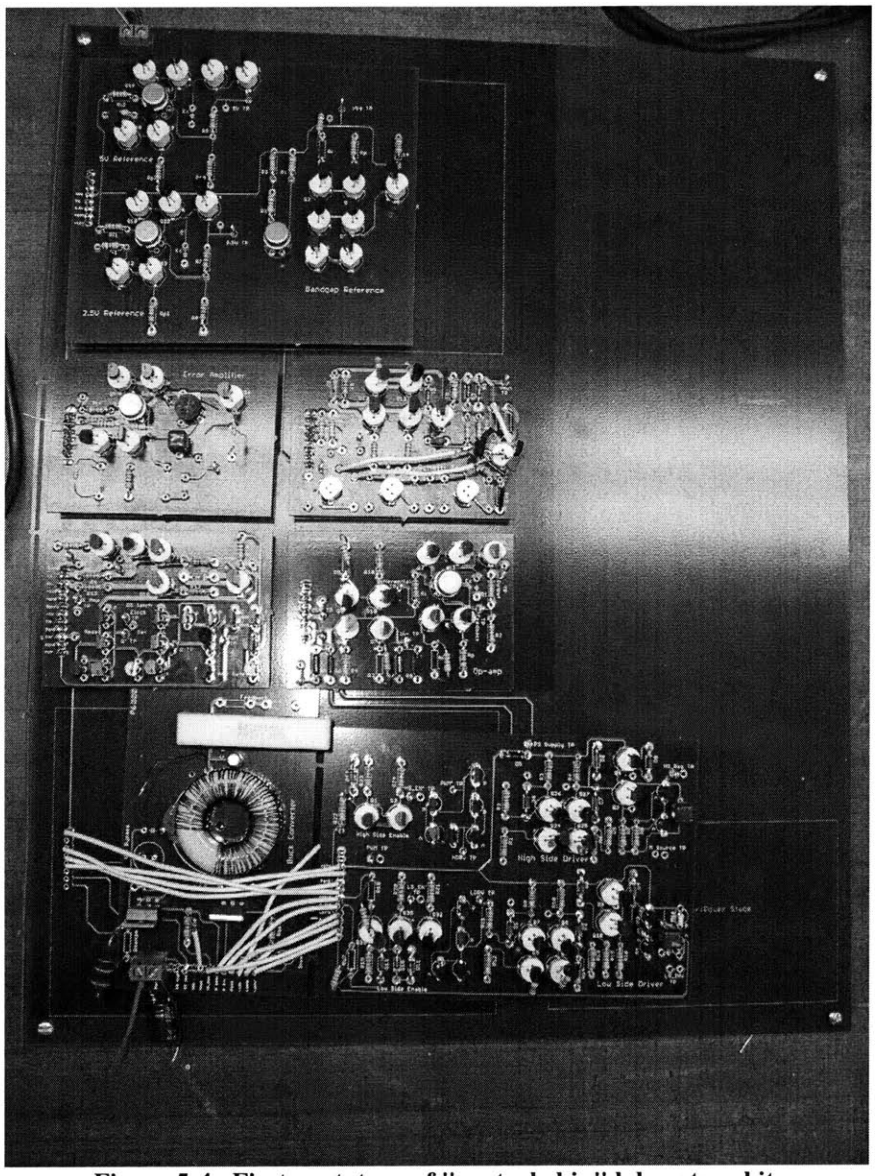

Figure 5-4. First prototype of "control chip" laboratory kit.

There is room for a number of modifications and additions to the designed laboratory kit. In future, we should consider adapting the controller for other converter topologies and developing a way for students to easily implement their own circuit designs on the kit. Additional controller features that might be interesting for students to learn about and design include soft-start and feed-forward compensation. Adapting the

kit to allow for either voltage-mode or current mode control could also be of interest down the road.

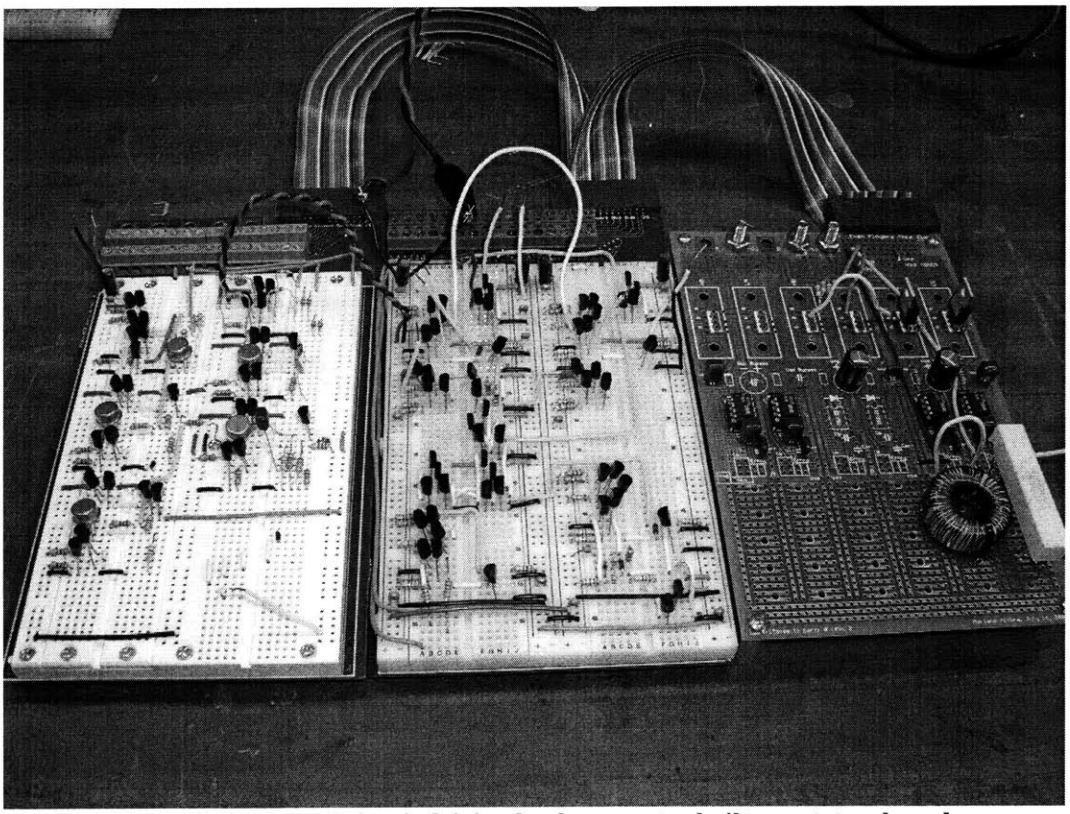

Figure 5-5. Control circuit driving buck converter built on a totem board.

6 References

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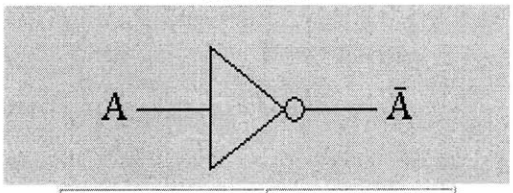
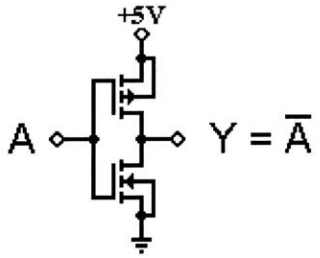
7 Appendix

7.1 CMOS Combinational Logic Gates

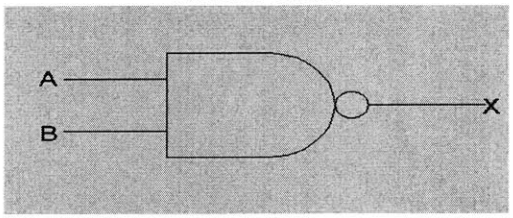
Inverter



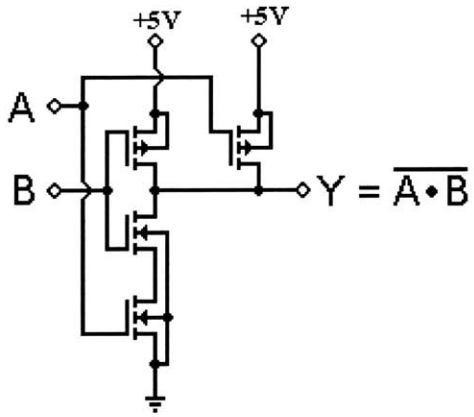
INPUT	OUTPUT
A	$\overline{A}$
0	1
1	0



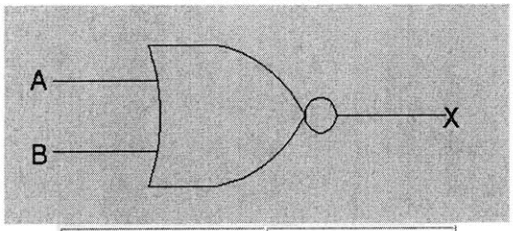
NAND Gate



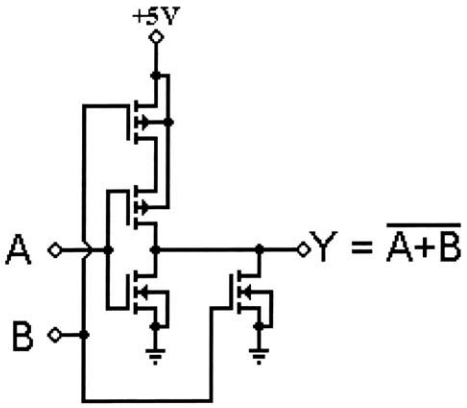
INPUT		OUTPUT
A	B	$X = \overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0



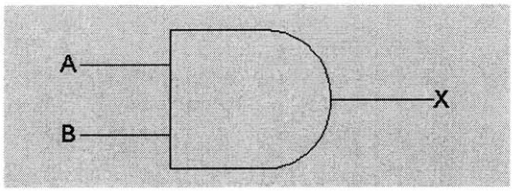
NOR Gate



INPUT		OUTPUT
A	B	$X = \overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0



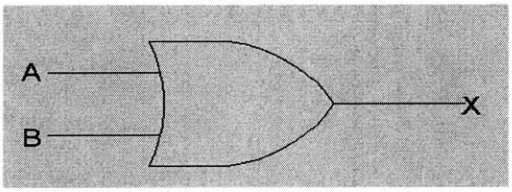
AND Gate



INPUT		OUTPUT
A	B	$X = AB$
0	0	0
0	1	0
1	0	0
1	1	1

Circuit can be implemented by following NAND gate with an inverter.

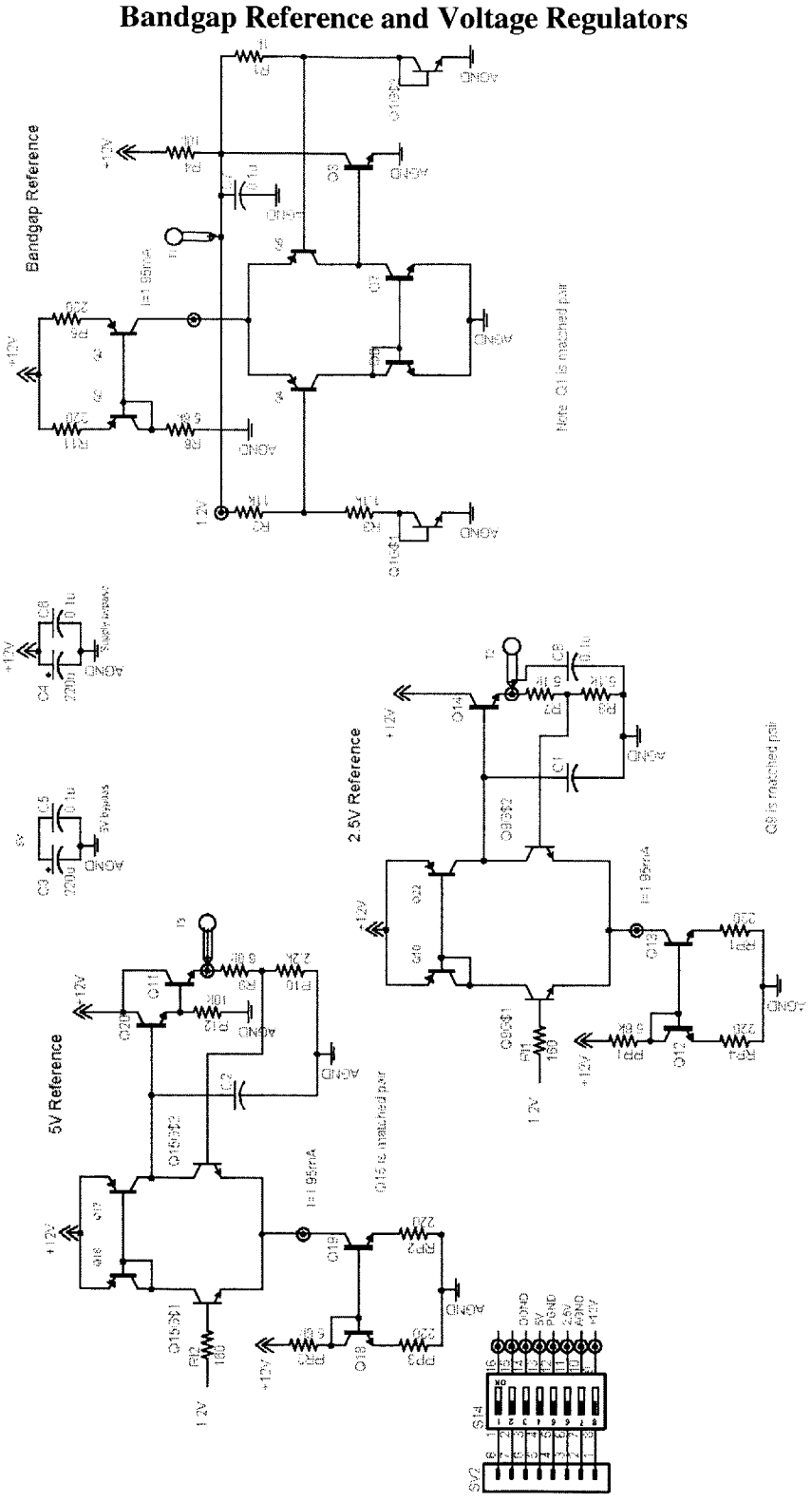
OR Gate



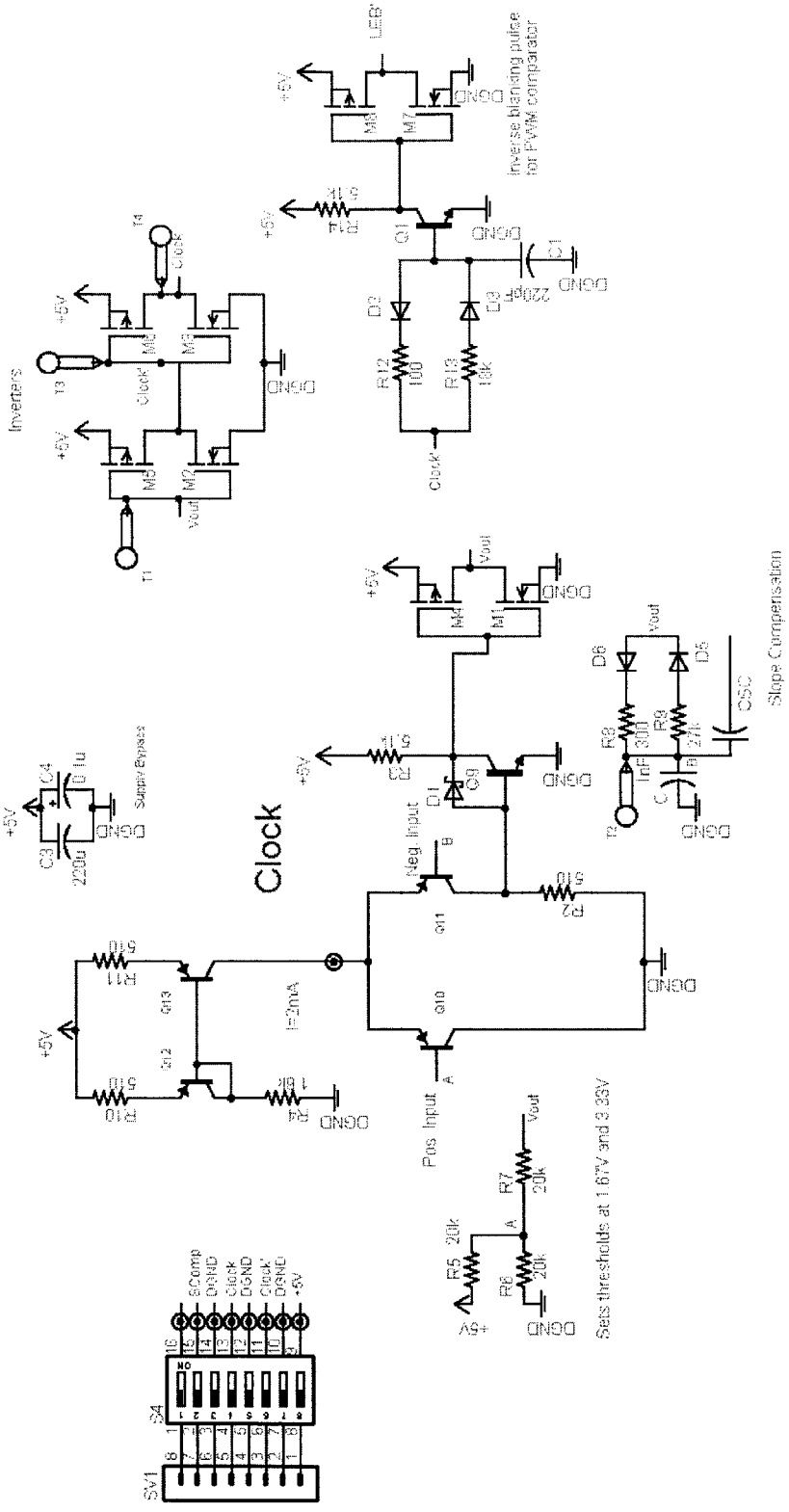
INPUT		OUTPUT
A	B	$X = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

Circuit can be implemented by following NAND gate with an inverter.

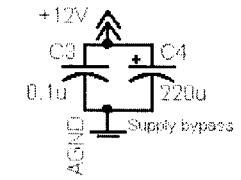
7.2 EAGLE Schematics

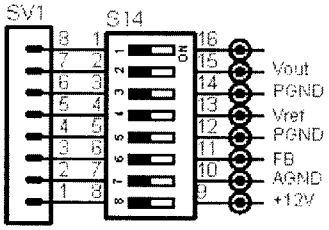


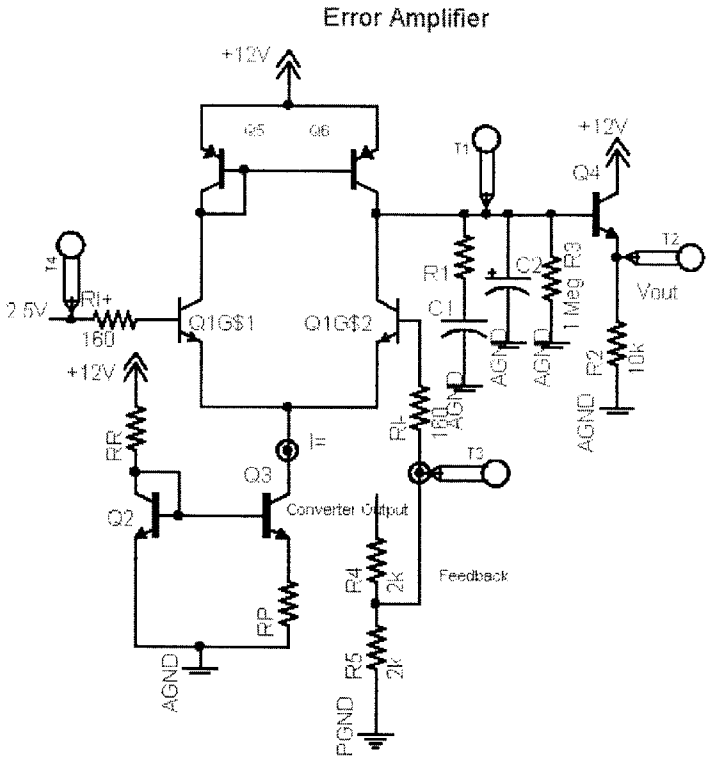
Clock


Clock
Inverse blanking pulse for PWM comparator
Inverters
Supply Bypass
Slope Compensation
Neg Input
Pos Input
Sets thresholds at 1.67V and 3.33V
SComp
DGND
Clock
Clock'
+5V
Vout
AS+

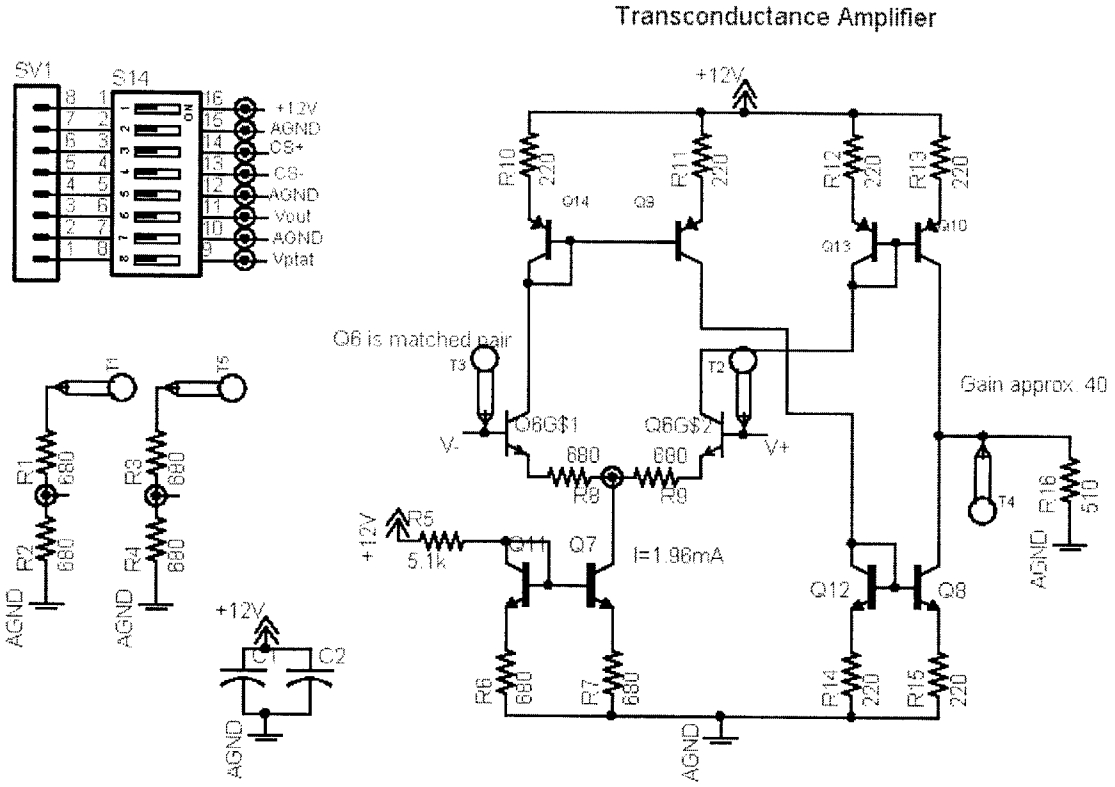
Error Amplifier



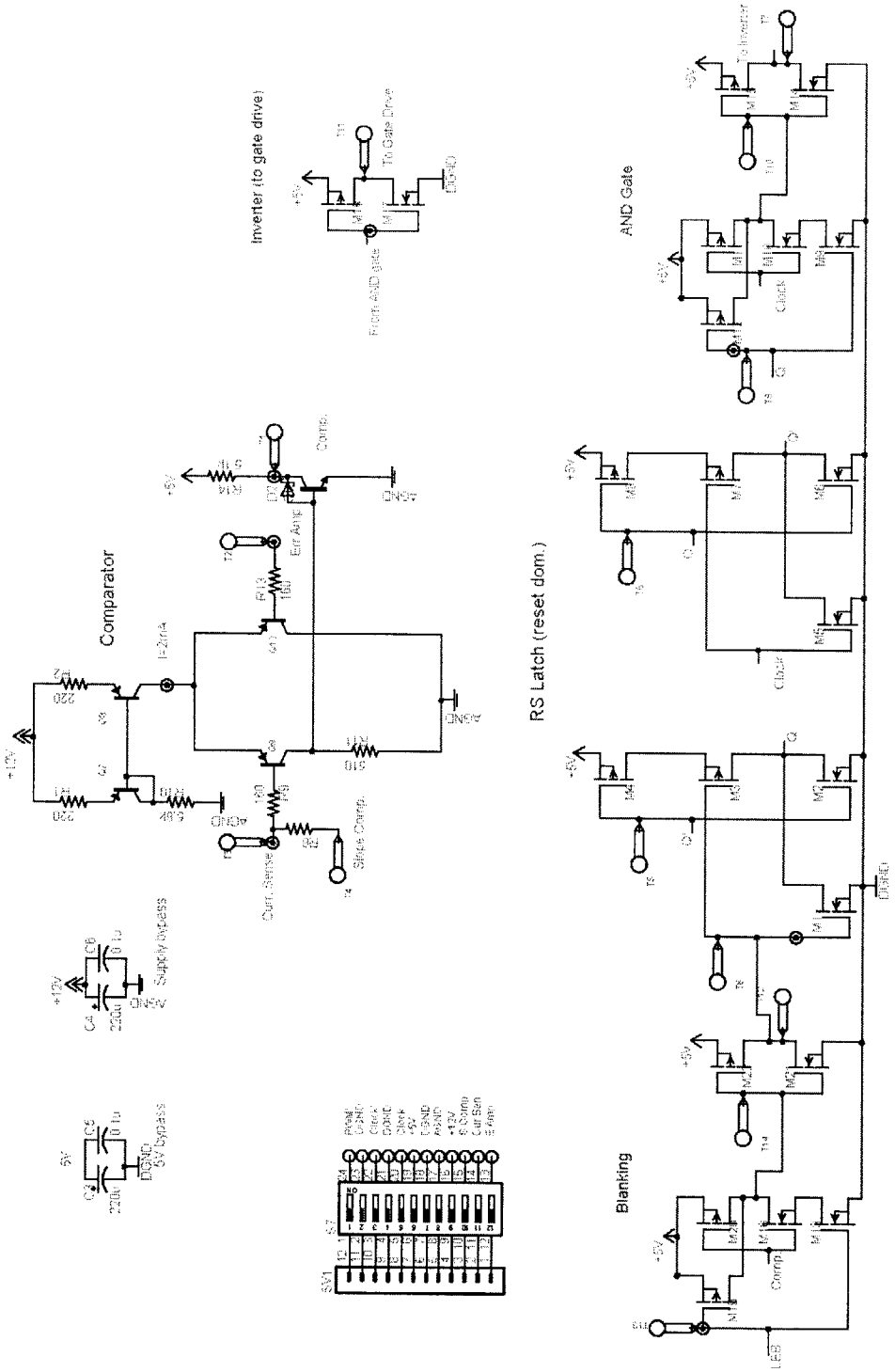




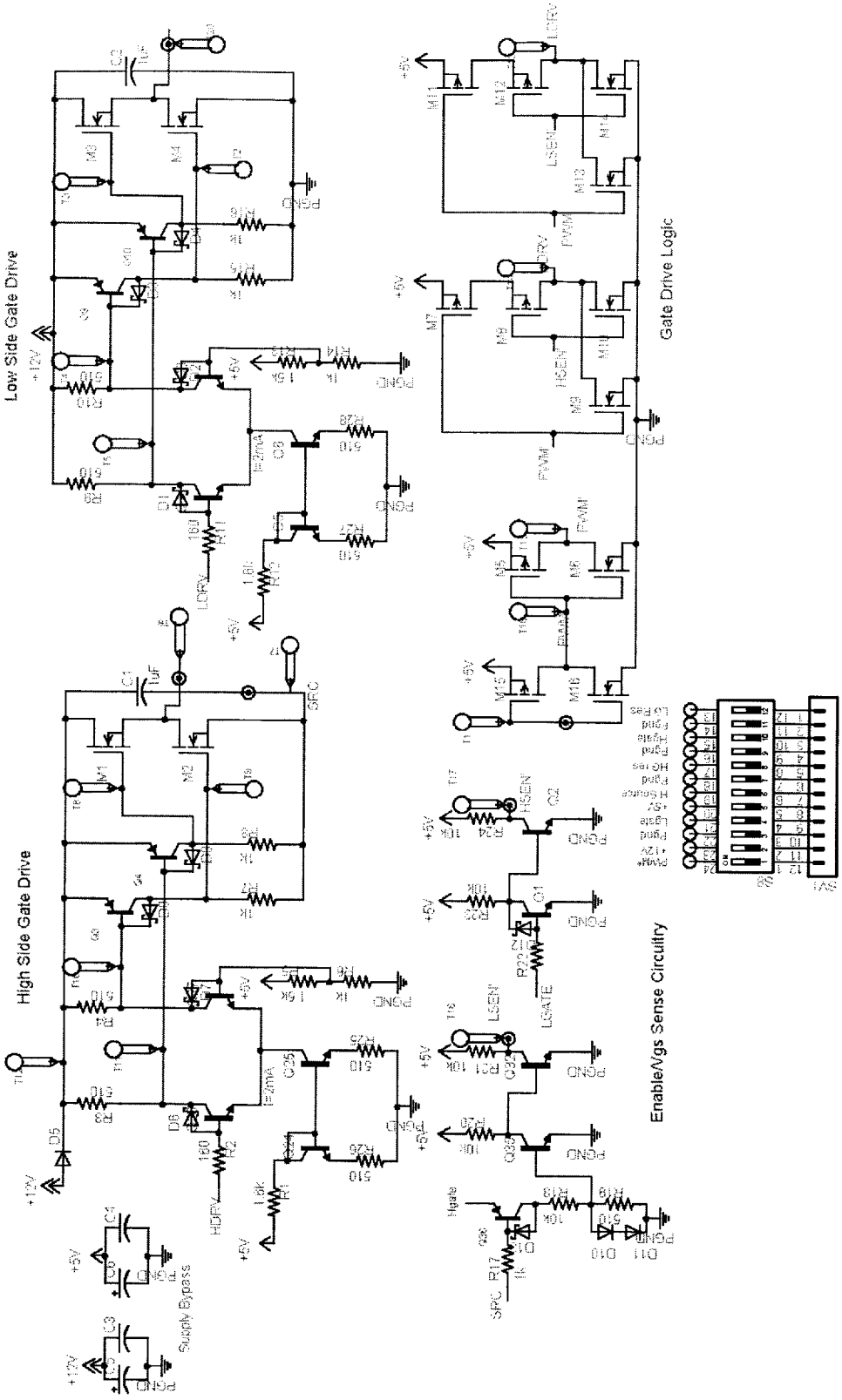
Current Sense Amplifier



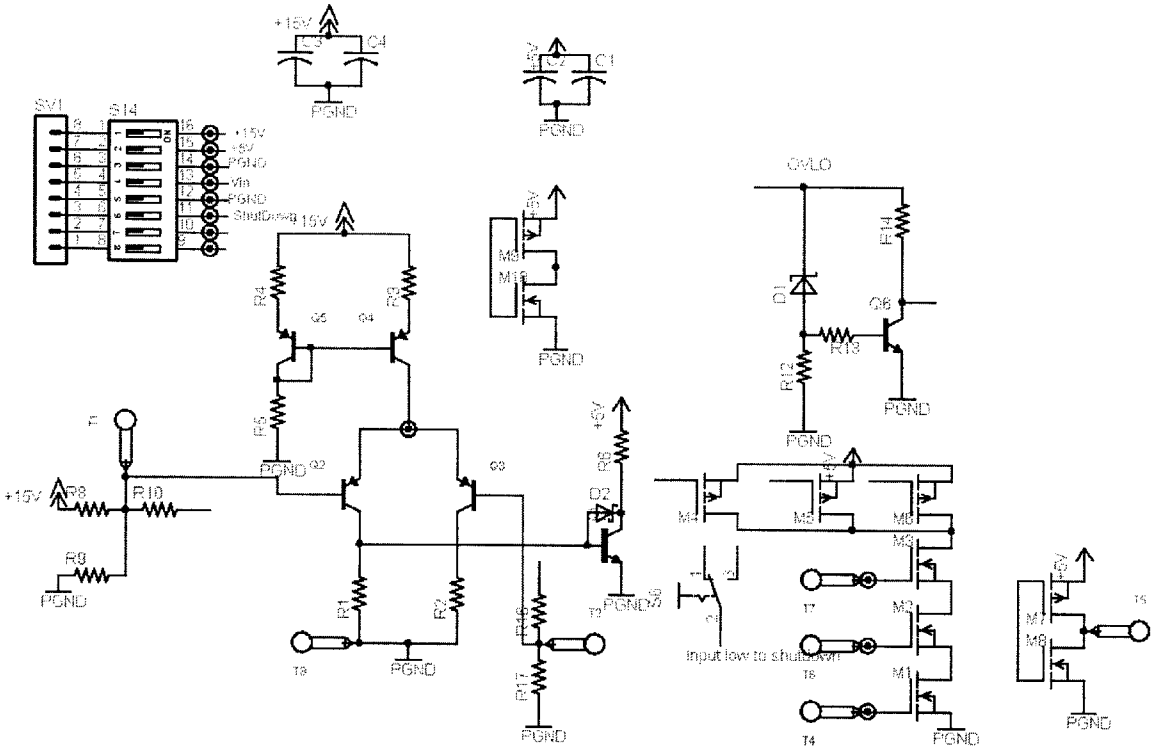
PWM Comparator and RS Latch



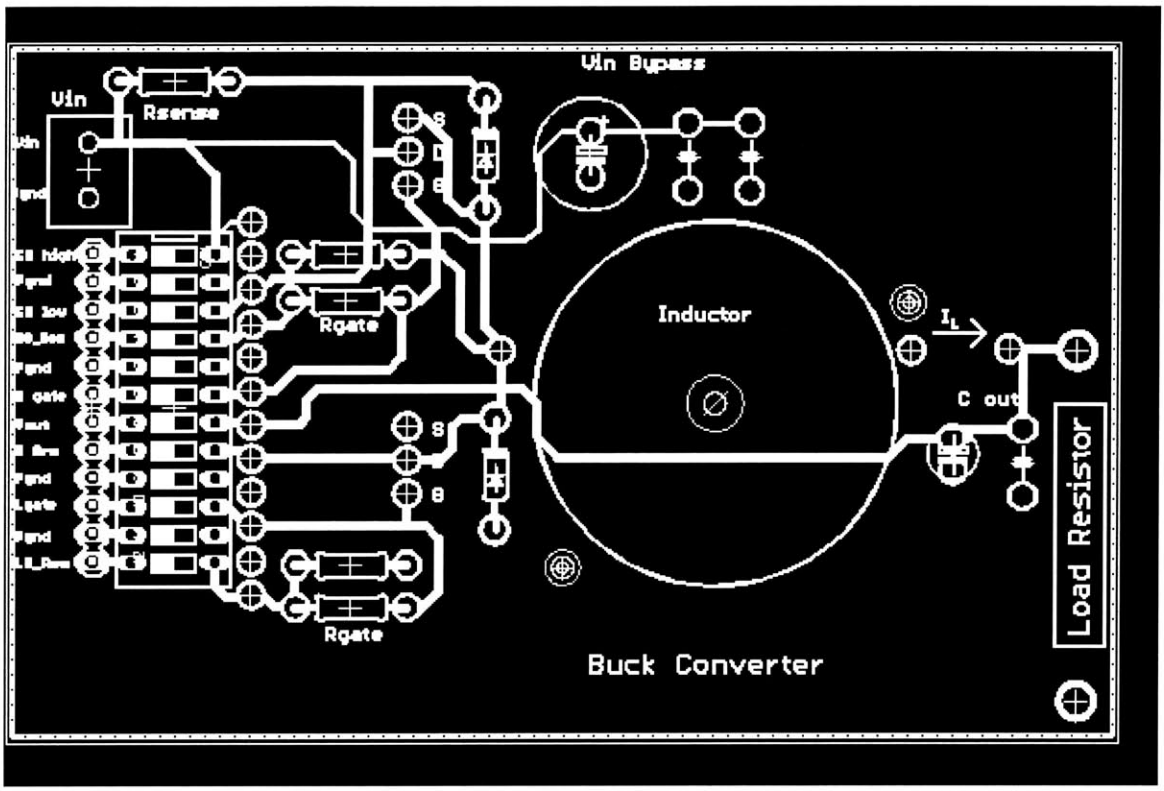
Gate Drive


Low Side Gate Drive
High Side Gate Drive
Gate Drive Logic
Enable/Vgs Sense Circuitry
Supply Bypass
LDRV
HDRV
PWM
LSEN
HSEN
LGATE
SFC
PGND
+5V
+12V

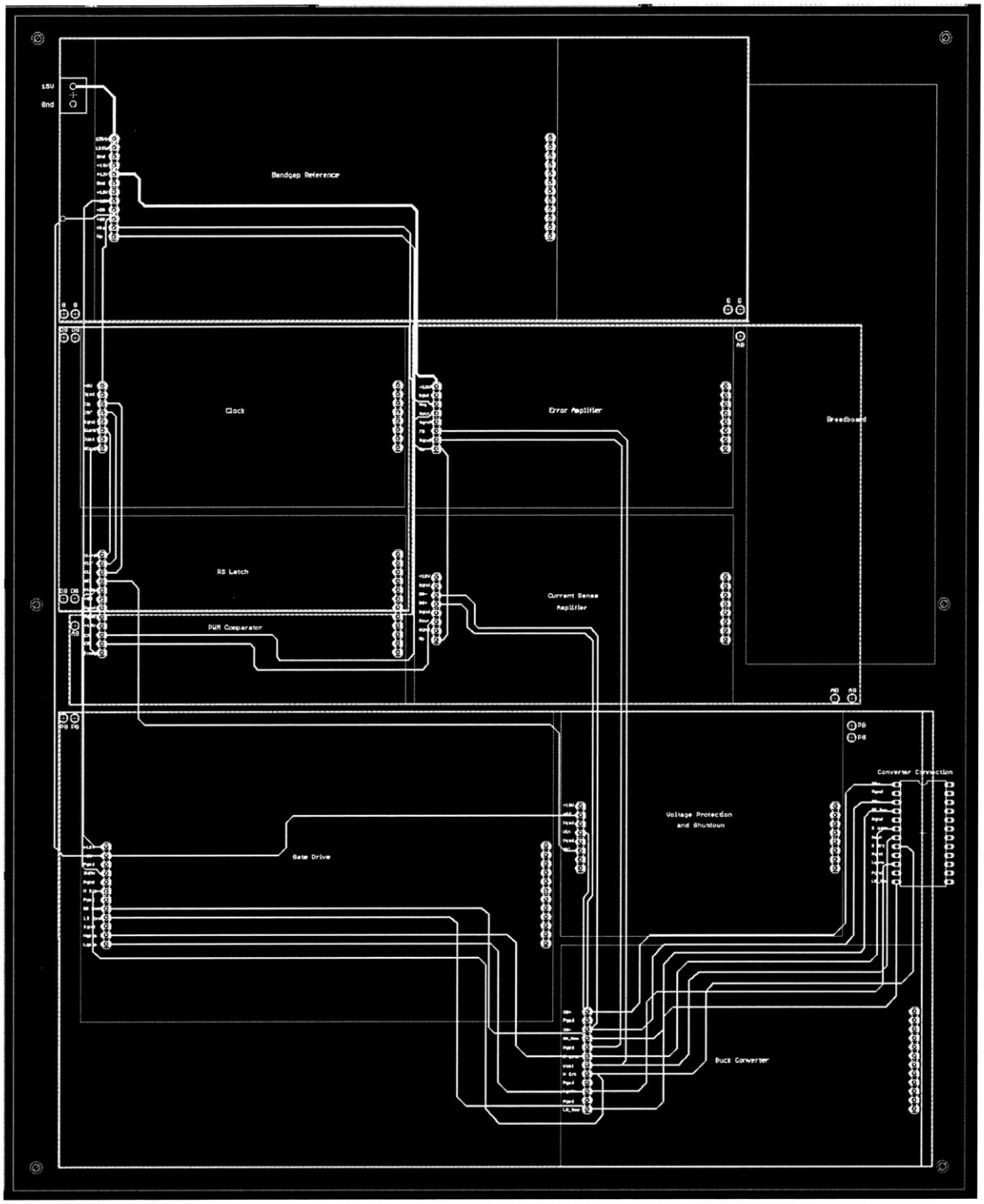
Shutdown and Protection



Buck Converter Board



Board Layout for Kit



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