SPICE Simulation and Modeling of DC-DC Flyback Converter

by

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B.A.Sc.(Hons), University of Toronto, Canada (1994)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

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Abstract

SPICE simulations were done on a hybrid-built 28 V input, 5 V output, 100 W power oval flyback converter. In order to have the simulation results comparable to those derived experimentally, SPICE models for power transistor and Schottky power diode were developed. Similarities and differences from the experimental results are discussed.

A novel current recovery circuit was proposed and tested with the flyback converter. This current recovery circuit, with careful timing, was showed to be inheriting the snubber characteristics. The simulated results showed an increase of efficiency of about 5%. The recovery circuit was proved to be functional under a fair range of turn-on time by a sensitivity analysis. Different voltage and power combination were tested and showed a gain in efficiency of at least 3% in general.

Large signal models for the flyback converter were also developed using both simplified transistor models and the averaged-state method. The averaged-state method was found to provide a faster means for the simulation.

Finally the two-port model of the flyback converter was developed and tested.

Thesis Supervisor: Martin F. Schlecht
Title: Professor of Electrical Engineering

Acknowledgments

I would like to begin by thanking my thesis adviser, Professor Martin F. Schlecht, for his help and guidance, both in my master program and in supervising the research for this thesis, and also for his patience and kindliness.

I would also like to thank Elizabeth Chung, Marty's Secretary. Without her help, I probably couldn't fit in my supervisor's busy schedule.

Finally, I would like to extend special thanks to my family for all the love and support to make this year happened. Thank you.

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Chapter 1

Introduction

1.1 Background

A distributive power supply architecture provides a number of merits compared to a centralized power supply architectures. With converters distributed throughout the electronic system, system efficiency is improved as it draws a lower current (say $10A$ at $50V$) as compared to that of the centralized system (say $100A$ at $5V$). It also provides better voltage regulations and transient response. In order to achieve higher power densities of $50W/in^3$, the switching frequency must be increased. Under the Printed Circuit Board technology, unfortunately, the parasitics inductance caused by component package leads and package-to-package connections make it difficult to achieve efficient operation at such high frequency range.

A research program has been started at M.I.T. to investigate the design of high switching frequency power supplies. This program involves the identification of new circuits [4], topologies, novel semiconductor and magnetic components [7], and packaging techniques [16]. In particular, methods for packaging a high frequency power circuit was studied in [16]. A hybrid circuit approach was used to combine switching and energy storage components in a single thermal package. The hybrid strategy was proved to be capable for the direct mounting of the active devices, and with multilayer metallization higher component densities and better control of the circuit parasitics were achieved.

1.2 Thesis Objectives

The purpose of this thesis is to analyze the built hybrid flyback converter in SPICE [19, 18, 3, 17, 11]. A simple transformer model for use in SPICE is to be developed. Simulation results are compared to measurements and the components are to be modeled to give a reasonably realistic simulation with the circuit. Some energy recovery circuits will be tested with the SPICE model to determine their flexibilities. A large signal computer model [10] which will correctly simulate the transient and the steady state behavior of the circuit is then to be derived from the *exact* SPICE model derived from the first stage. The model will be faster than a straight SPICE simulation because fewer points in time need actually to be calculated. The final stage of the thesis is to investigate the possibility of modeling a two-port network from the simplified circuit. This model is especially valuable for analyzing a distributed power supply system. A performance analysis might be conducted in a distributed system network.

The power circuit used for SPICE simulation and modeling is a $100W$ DC to DC power supply with switching frequency of $0.5MHz$. The circuit accepts a $28V$, $4.5A$ input, and converts it to a $5V$, $20A$ output. The flyback circuit schematic is as follows:

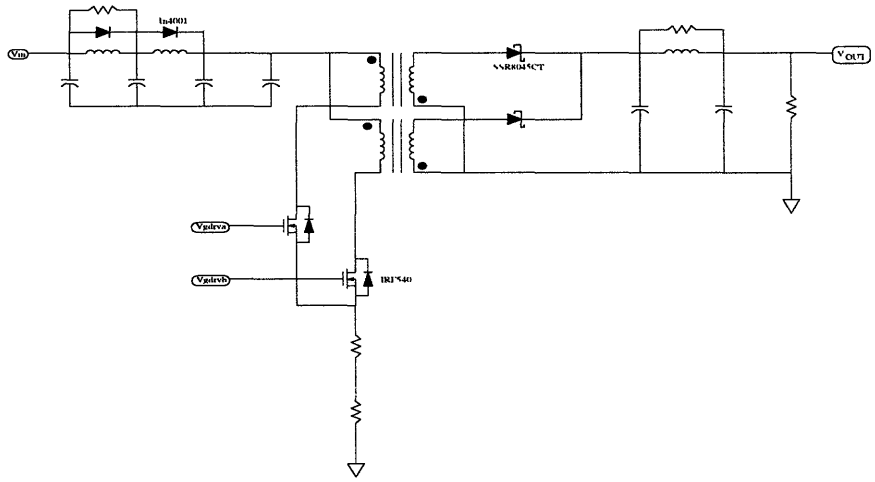

Figure 1-1: $0.5MHz$ DC-DC flyback converter circuit schematic

1.3 Thesis Outline

The thesis basically involves five stages : Chapter 2 discusses the modeling the various important components in the DC-DC converter. It involves a detailed modeling of the components that contributes to a lot of parasitics and power consumption in the circuit, namely the transformer core [8], the power switching HEXFET, $IRF540$ [9, 20] and the Schottky Diode, $SSR8045CT$ [14]. The modelings take the temperature effect and inductances and capacitances of the packaging into account. For the Schottky diode, a detailed model including reverse recovery effect [5, 12] is determined.

Chapter 3 is focused on the SPICE modeling for the whole $0.5MHz$ DC-DC flyback converter. Then it proceeds to simulate the whole $0.5MHz$ DC-DC flyback transformer in SPICE. Performances are evaluated in terms of its resemblance to the built circuit in terms of signal responses, transient responses during switching and the total power consumption (efficiency).

Evaluation of some energy recovery schemes under the determined SPICE model is found in Chapter 4. Some energy recovery strategies are evaluated to enhance the original design. One strategy in Fig. 1-2 is tested and proved to be flexible is a current recovery from the clamped circuit with a precise controlled switching time. Effect of switching delays and mismatches are investigated. Various input voltages and output power combinations are tested and tabulated.

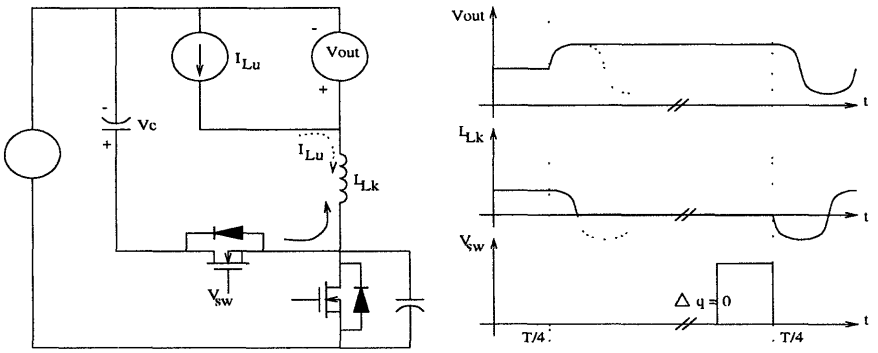

Figure 1-2: A proposed current recovery scheme for enhancing the circuit

Chapter 5 focuses on the large signal modeling of the SPICE model. Two ap-

proaches are to be used. The first one to derive directly from the SPICE model found in Stage 2 by removing high order terms and relatively unimportant components. The second approach are to follow the similar method addressed in [10] for a series resonant converter. The main issue is to focus on its transient response such that the derived model will serve as a good model for control circuits. The control circuit together with the converter circuit is simulated and verified. Merits and shortfalls on each strategy are investigated.

Chapter 6 looks at the Two-Port Modeling. After the large scale model is derived, the model is further simplified just to maintain the transient characteristics of the system. This model is primarily targeted for a large distributed power supply network where about half a hundred such converters are to be simulated together. A lump of these models might then be simulated under the distributed power network.

Chapter 2

SPICE Modeling

This chapter is devoted to the modeling of various nonlinear components which are essential for accurate simulation of the power electronic circuits. Two approaches are used to model the components. The generic models are made by optimizing the parameters of the generic SPICE model to better fit the characteristics of a high voltage device. The Schottky diode adapts this kind of approach. The modeling of the switching power MOSFET is tackled using the subcircuit approach. It is constructed by combining conventional SPICE device models with passive components and controlled sources into a SPICE subcircuit which represents the power device model. This kind of modeling can be complex and slow to simulate, which results in small time step, 1 ns, when running the simulation in Chapter 3.

2.1 Transformer Core

The model in Fig. 2-1 adapts the generic modeling technique. It includes the leakage inductance, L_k, the primary resistance, R_{loss}, the core loss, R_{core} and the magnetizing inductance, L_μ. Instead of using a pair of controlled voltage source for the coupling inductances, A generic coupling function is used. This gives users more flexibility on the control of magnetic coupling coefficient when geometries of the magnetic core are to be taken into account.

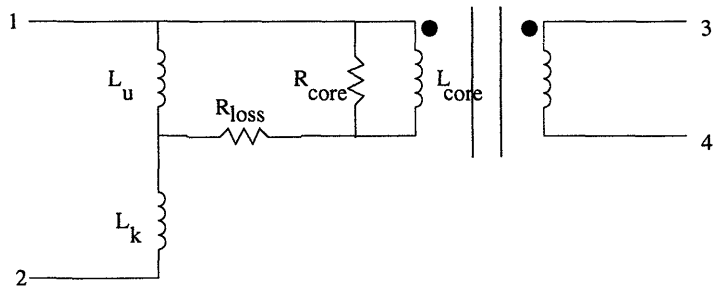

Figure 2-1: SPICE Model for Transformer Core

2.2 Schottky Diode

The current coefficient for a forward biased silicon Schottky diode is about five orders of magnitude larger than that for a bipolar diode. The lower on-state voltage, 0.4 V is a major advantage. The temperature dependence of the forward voltage drop on Schottky are controlled by XTI, the temperature coefficient of I_S. Typically the on-state resistance, $R_{DS_{(on)}}$, increases by approximately a factor of two when the junction temperature is at its rated maximum. A possible solution for this shortcoming is as follows — do a hand calculation to determine the approximate junction operating temperature, and scale $R_{DS_{(on)}}$ by the appropriate value from the $R_{DS_{(on)}}$ versus case temperature graph. In Fig. 2-2, the forward voltage versus forward current characteristics of the model is simulated. The results are comparable to those provided by the databook.

Reverse Recovery plays an important role in the accuracy of the simulation of the flyback converter. Reverse recovery occurs when a forward conducting diode is turned off rapidly, and the internally stored charges cause transient reverse current to flow at high reverse voltage. Although the current in Schottky flows only by drift and there is no need to accumulate or remove excess carriers, A Schottky diode does contain SCL capacitance which must be charged and discharged during switching. The charge storage effects are modeled by the transit time TT in SPICE and is set to zero in the case of Schottky diode. The nonlinear depletion layer capacitance, which depends on the zero-bias junction capacitance CJO, the junction potential VJ, and grading coefficient M is set accordingly in the SPICE code. Figure 2-3 shows the

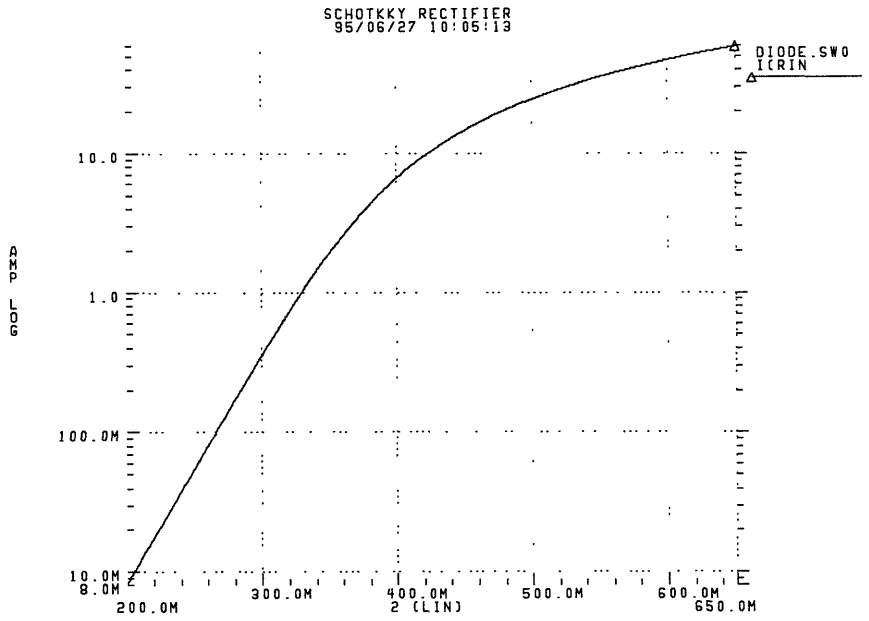

Figure 2-2: Forward Voltage Vs. Forward Current of Schottky Diode

simulated results of the forward and reverse recovery due to SCL capacitance. In Fig. 2-3 both forward and reverse recoveries are demonstrated with a 600 ns, 10 V step. As shown, there is a forward drop of approximately 0.4 V during conduction and a reverse recovery time of less than 200 ns.

As the reverse voltage on a Schottky diode increases, the peak electric field at the metal-semiconductor interface eventually reaches the avalanche state. Avalanche in Schottky diode can be simply be modeled with an ideal diode and a negative voltage source connected parallel across the Schottky diode model.

2.3 Power MOSFET

The greatest limitation in using SPICE to model a power MOSFET is the effect of the gate-drain capacitance, which is highly nonlinear function of V_{gd}, especially at low V_{gd} values. As the MOSFET is a majority carrier device, the transient performance of the MOSFET is governed only by the oxide and SCL capacitances and by the impedances that limit the ability to charge and discharge these capacitances. The

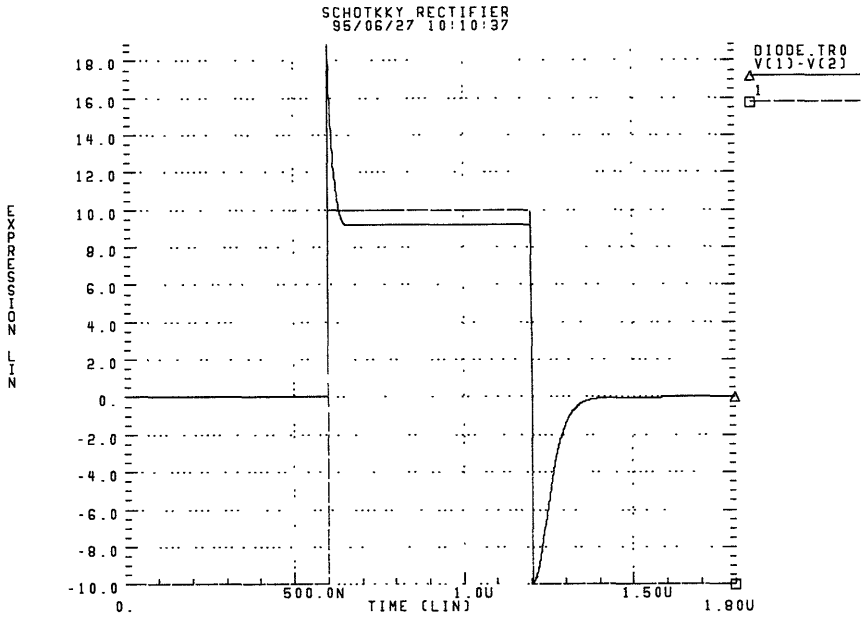

Figure 2-3: Forward and Reverse Recovery in Schottky Diode

SPICE computer model for *HEXFET III* is documented in [13]. The SPICE model proposed is in Fig. 2-4. As shown, the Miller capacitance, C_{gd} is emulated by C_x and E_1. C_x is modeled as a high order polynomial of V_{gd}. Its value changes rapidly when V_{gd} is close to zero volt. E_1 is dependent voltage source of V_{dg}. It offers offset of the voltage across the capacitor, thus allowing C_{gd} to vary rapidly in the local region. It variably reduces the voltage change across the capacitor, a factor of 200 in high voltage devices and 20 in low ones.

The connection of the p-wells to the source level metal gives the MOSFET an antiparallel body diode. The bulk-to-drain diode of the built-in MOSFET model cannot be used for this purpose because the on-state resistance has to be adjusted to give a satisfactory simulation of the MOSFET output characteristics in the linear region. A diode with reverse recovery characteristics and small on-state resistance is used instead of what is documented in [13]. The tradeoff is an increase of computation times.

Inductances and resistances of the gate, source and drain are determined by the packaging of the transistor. R_1 and R_2 in the model is used to control the DC

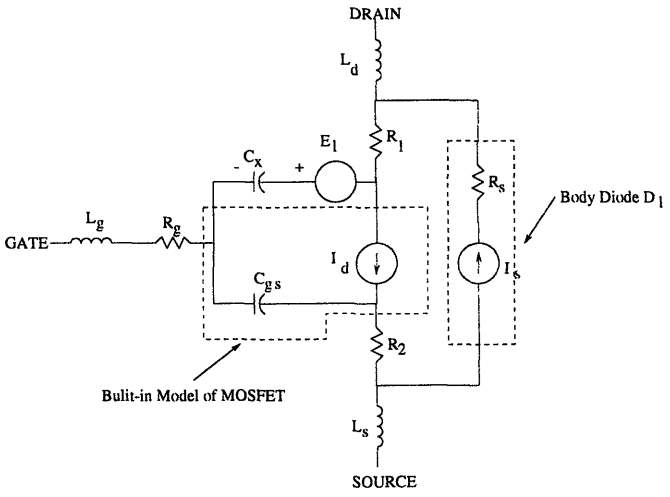

Figure 2-4: The HEXFET model

performance of the model. R_2 is the parasitic resistance in the source. R_1, the epitaxial layer bulk resistance, is calculated as $R_1 = R_{ds(on)} - R_{channel}$, where $R_{ds(on)}$ is simply equal to V/I in low voltage region.

The avalanche of the power MOSFET is modeled with an ideal diode and an about $150V$ voltage source connected in parallel to it.

HEXFET IV power MOSFET is used instead in the flyback converter. It results in a double in die size, channel width, W, and all the corresponding junction capacitances. Resistances decrease by half, also.

The *HEXFET* model is tested with a $500n$ second, $10V$ step. It is noted that due to the manner in which C_{gd} is emulated by C_x and E_1. C_{dg} reaches very high value when V_{gd} reaches $+10V$. This model will not be valid when the gate voltage is much higher than 12 volts.

Figures 2-5, 2-6 and 2-7 are the simulated results for the *HEXFET IV* with a 10 V step change in 500 ns modified from [13]. As shown, there is a degree of correspondence between the theoretical and actual waveforms which indicate that the model produces results in switching regime that are sufficiently accurate for most purposes.

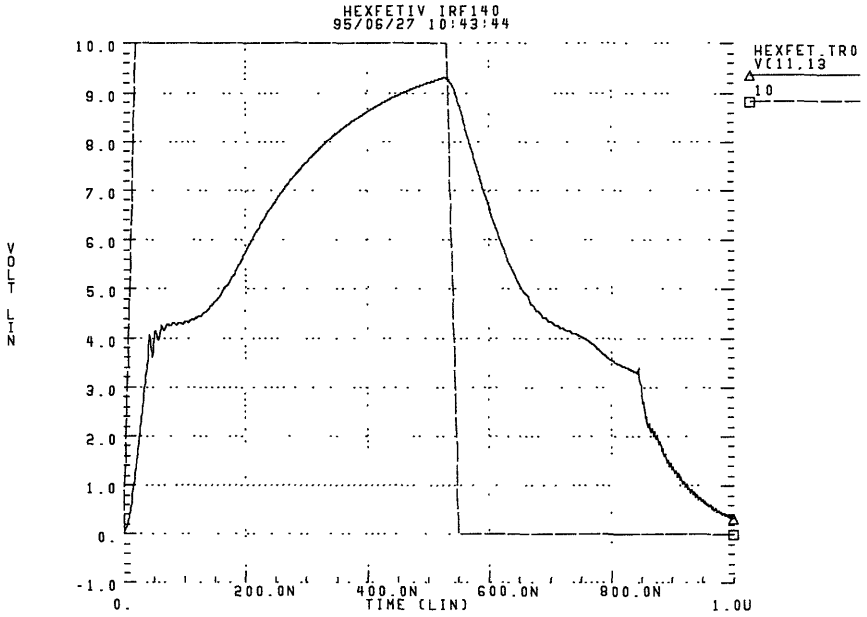

Figure 2-5: Step Response of Gate-Source Voltage in HEXFET IV

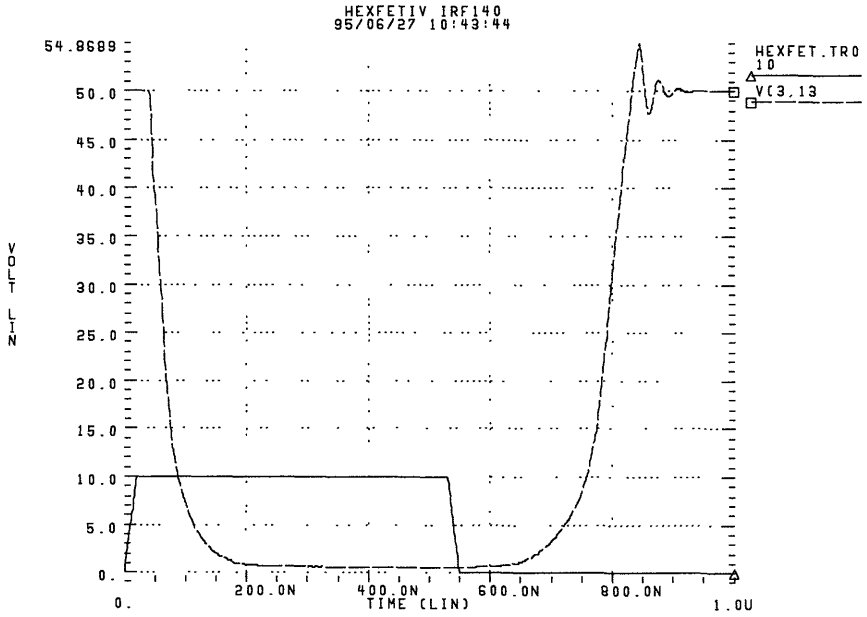

Figure 2-6: Step Response of Drain-Source Voltage in HEXFET IV

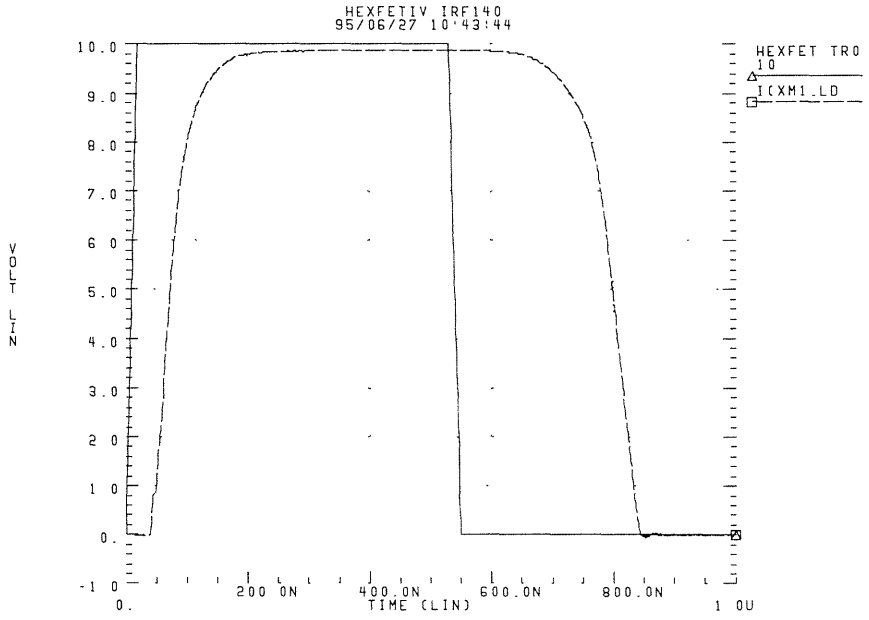

Figure 2-7: Setp Response of Drain Current in HEXFET IV

Chapter 3

SPICE Simulation

This chapter looks at the simulation of the flyback converter using HSPICE, [1, 2] with the expected theoretical results.

3.1 Basic Operation

The basic operation of the transformer-isolated buck-boost converter, or "flyback" converter is as follows. Energy is stored in the magnetic core of the flyback transformer while the transistor is on, and "flies back" to the output through the Schottky diode while the transistor is off. The flyback transformer is designed with an appropriate air gap so that it serves the dual role of inductor and transformer. In that way, isolation and polarity reversal can be achieved in a practical flyback converter with no more power components than are in the basic buck-boost converter. The output voltage, V_{out} is equal to $NV_{in}D/(1-D)$ where N is the transformer ratio, V_{in} is the input voltage, and D is the duty ratio in which the transistor switch is on. The load current is assumed to be such that the transformer is operating in the continuous conduction. In the case of discontinuous conduction, where the magnetizing inductor current, i_{L_μ}, returns to zero amperes before the end of the cycle, the output to input ratio is given by D_1/D_2 where D_1 is the duty ratio and D_2 is the time ratio in which the magnetizing current takes to go back to zero.

There are some design constraints. For instances, in the case of a 5 V output,

we normally require a DC ripple of less than 1%. In the steady state, the ripple in the output is basically the charging and discharging of the output filter with the i_{out}, which is equal to the $\Delta Q/C$, where ΔQ is the change in charge stored in the output capacitance, C. In order to minimize the output voltage ripple, the switching frequency, f_{sw} is chosen to be $\frac{1}{2}MHz$.

In addition, the rising and the falling edge of the i_{out} are very steep. In our case, where the transformer circuit is built in the hermitic sealed hybrid substrate, the components are all attached to parasitics inductances on the conduction legs. The damping resistor of 0.25 Ω is added across the output filter to provide a damping to the high $100MHz$ spike during switching.

This converter is operated in the control current mode, which is discussed more detail in Chapter 5. Basically the magnetizing inductor current is compared with a threshold and the transistor is turned off once this threshold is reached. The control circuit providing the threshold signal is basically a triangular pulse generator which inevitably has a dead time between each cycle. The maximum duty cycle, D_{max} which can be calculated from $v_{out}/v_{in_{min}} = ND_{max}/(1 - D_{max})$ with $v_{in_{min}}$ equals $16V$ is approximately equal to 40%.

3.2 Energy Losses

There are three major losses in the flyback converter, namely the losses in the rectifiers, the conduction losses in the MOSFETs and the loss due to leakage inductance.

The losses of the Schottky diodes includes the on-state losses and the leakage current losses. Since the Schottky diodes have a finite on-state voltage, V_f, of approximately 0.4 V. The on-state loss is simply $V_f I_{out}$, where $I_{out} = 20$ as either one must be on during the period. This gives a loss of energy of 8 W.

The reverse leakage current for a positive centertap Schottky rectifier is about 30 mA (@Rated V_R, $T_A = 100^oC$). The voltage reflected across the rectifier is 2 times the original input voltage times the core ratio, which is $2 \cdot 28 \cdot \frac{1}{2} = 28$. With a duty ratio of 0.2885 (refer to Table 3.1), the leakage current loss is $2 \cdot 0.24 = 0.48$ W.

Also the charging and discharging of the junction capacitance ($1600pF$) gives a $\frac{1}{2}CV^2f_{sw}$ losses., which is approximately equal to $400\mu W$. It is insignificant compared to the forward loss. The total losses due to the Schottky diodes is $8.48W$.

The losses caused by the MOSFETs are switching losses during turn-on and turn-off and the conduction loss. As shown in Fig. 3-1, power is lost during the switching period when both the voltage and current are non-zero (conduction loss will be considered later). The peak of the magnetizing current, I_{μ_p}, is equal to $(V_{in}T_{on})/L_{\mu}$. where $V_{in} = 28, Ton = 577n, L_{\mu} = 12\mu$. This gives a value of $13.5A$. It leads to a I_{d1} of $0.5A$ and I_{d2} of $14A$.

By assuming $T_T = 20ns$ and straight line transient rise and fall, as shown in Fig. 3-1, the turn-on and turn-off losses are simply equal to the triangle area of VI. This corresponds to a turn-on loss of $0.14\ W$ and turn-off loss of $3.92W$.

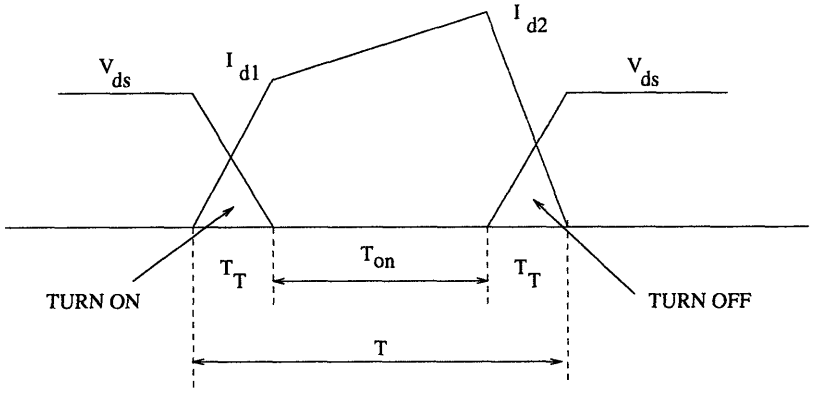

Figure 3-1: Time Profile of the Switching Loss of MOSFET in the Flyback Converter

Conduction loss of the MOSFET is simply given by the integral of $\frac{1}{T}\int i^2(t)R_{ds_{on}}dt$. which end up in the following closed from :

$$\frac{({I_{d1}}^2 + I_{d1}I_{d2} + {I_{d2}}^2)R_{ds_{on}}T_{on}}{3T}$$

For the surface mount MOSFET used in the built flyback converter, the drain-to-source on-state resistance, $R_{ds_{on}}$, is relatively small of about 0.1Ω. This gives a conduction loss of $3.9W$.

The loss due to parasitic capacitance in the two MOSFETs, $400pC$ is $0.16W$. The

total losses due to MOSFETs is $8.12W$.

The leakage inductance of 80 nF gives a $\frac{1}{2}LI^2f_{sw}$ loss. With $I = 13.5$, it accounts for 7.3 W. Hence, the total losses is $23.9W$. There are some uncalculated losses from the transformer core and skin and proximity effect of the copper windings of about $0.5W$. This gives the efficiency of the transformer of about 75.6%. The built circuit has an experimentally determined efficiency of about 79%.

3.3 Simulation

3.3.1 Details of the Circuit Simulated

Figure 3-2 shows the actual circuit that is simulated in SPICE. It should be noted that in the input filter stage, the resistors of 8 $m\Omega$ are added in series with the inductors to give a more realistic comparison with the built circuit. Similarly a resistance of 3 $m\Omega$ is added to the output filter inductor. Instead of adding parasitic resistors to the transformer inductors in both side, a resistor of 8 $m\Omega$ is reflected to the primary side only. The resistor of 12 $m\Omega$ which is added in between the magnetizing inductor, L_μ, and the coupling one, not only simulates the resistive loss in the transformer core, but also provides damping for two parallel inductor sources. SPICE fails to simulate in the presence of voltage/inductor loop. Whenever a pure loop is needed, a resistor of 10 $\mu\Omega$ is added in series to assist the transient analysis in SPICE. (10 $\mu\Omega$ is the smallest possible value for resistance in SPICE.)

The parasitic inductances of the $HEXFET\ IV$, modeled in Section 2.3 due to the packaging of the die, (namely the L_g, L_s, L_d), are removed during the simulation. Parasitic inductance of the drain and source of the transistor, L_d, L_g are combined with the the leakage inductance of the transformer core as a single inductor of value $80nF$. The gate parasitic inductance, L_s is removed in a completely different scenario. In the SPICE code developed, the MOSFET gates are simply driven by a voltage source, in which the switching process is unnecessarily delayed by the parasitic inductances of the modeled transistor.

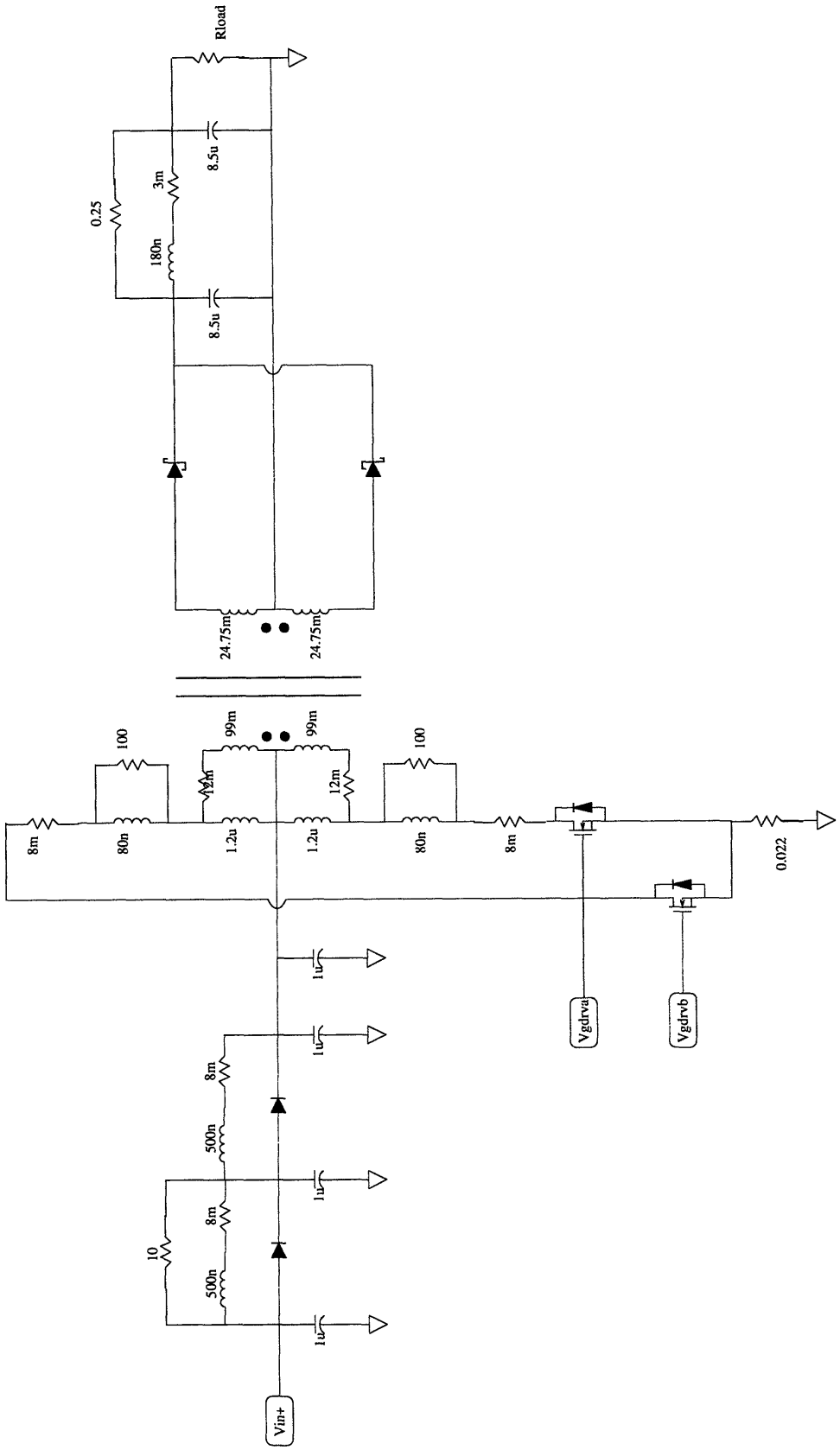

Figure 3-2: Actual Simulated Circuit with Devices Values

3.3.2 Nonconvergence Problem and Alternatives

Since the converter simulation requires details of the current responses of various parts of the circuit which involves large amount of transient responses of lumps of inductances and capacitances, the required time step (turned out to be 1 ns, compared to 200 ns period) is very small. The failure to converge during a transient response is large. Particular attentions should be paid to the details of the device model. For instances, the default values for all parasitic resistances and capacitances are zero. For an ideal diode, which we use frequently in modeling an avalanche effect in both MOSFETs and power diodes, if the parameters RS and CJO are not specified, the device will have no ohmic resistance and no junction capacitance. Zero resistance implies infinite current gain during the forward region, while a zero capacitance means a null switching time. This results in a smaller and smaller internal time step and leads to a convergence failure.

SPICE uses the Newton-Raphson algorithm to simulate the nonlinear circuit equation. Sometimes, the algorithm might be converging very slowly due to the characteristics of the circuits. Increase in the number of iteration points for a given transient step is an alternative to aid convergence. The iteration limit at any point during the transient analysis can be altered by the parameter $ITL4$ in the *.option* command line. Our simulation is run under $ITL4$ of 100 while the default value is 50. As a result of more iteration points, a longer simulation time will be required. There is another alternative : reduce the relative accuracy of all the voltage and currents that are calculated by altering the parameter $RELTOL$. It is not recommended, in general.

The total number of iterations in a simulation run is limited to the value of $ITL5$ option. In our simulation $ITL5$ is set to zero which is the same as setting it to infinity.

To avoid overflowing of too many transient data during initial startup, the third parameter on the $.TRAN$ statement can be used to suppress part of the output at the beginning of the run. For instances, a transient analysis from 0 to 1 ms in steps of 1 ns and retaining output from 0.8 ms to 1 ms, the command would be $.TRAN$ $1n$ $1m$ $0.8n$ $1n$.

3.3.3 Initial Conditions for Active Elements

Initial conditions of the active elements are crucial to the running of the simulation. SPICE provides a routine to guess the initial conditions for the active elements and it is generally not recommended. In the simulations, as all the filtering capacitances are connected to ground, they are assigned with V_{in} or V_{out} depending on which sides they are residing. The difficult part is to assign values to the magnetizing inductance, L_μ, the leakage inductance, L_k and the coupling inductance. Failure to give correct values will either overshoot the output or damp the output to zero after several time steps of simulation. Since it is an oval converter, the initial conditions of the first transformer core is not the same as the second transformer core. In fact their secondary currents must add up to 20 A by KCL, the DC value of i_{out}. The following is a rough estimation for the initial condition in the SPICE code. Values are then fine tuned after the first simulation is completed.

First, as the second switch is off, the second leakage inductor, L_{2p_k} must has 0 initial current. By $V_{out}/(nV_{in}) = D/(1-D)$ with $V_{out} = 5, V_{in} = 28, n = 0.5$, the duty ratio is roughly equal to 0.263, which corresponds to an on time, T_{on}, of 526 ns (period = 2000 ns)

Assuming discontinuous mode, the maximum magnetizing current, $I_{L_{2p_\mu}}$ is given by $V_{in}T_{on}/L_{2p_\mu}$ with $L_{2p_\mu} = 1.2\mu$. The magnetizing current is found to be 12.3 A.

So the coupling inductor, L_{2p}, has the initial condition of -12.3 by KCL as the second leakage inductor current, $i_{L_{2p_k}}$, must be null as the switch is open.

It follows that the coupling inductor of the first transformer core, $i_{L_{1p}}$ must have an initial current of 2.3 A. (The secondary currents must add up to 20 A by KCL which leads to a secondary current for the first transformer core of -4.6 A. After reflecting to the primary side, it is of the value of 2.3 A.)

The magnetizing current, $i_{L_{1p_\mu}}$, and the coupling current, $i_{L_{1p}}$, must add up to the leakage current, $i_{L_{1p_k}}$, which is equal to 4.8 A, DC current of V_{in}. This gives the initial values of the magnetizing current of 2.5 A

After one simulation, the continuous mode initial condition are found as follows :

D	577 ns
$I_{L_{1p}}$	0.5 A
$I_{L_{1p_\mu}}$	2.5 A
$I_{L_{1p_k}}$	2.0 A
$I_{L_{2p}}$	-10.5 A
$I_{L_{2p_\mu}}$	10.5 A
$I_{L_{2p_k}}$	0.0 A

Table 3.1: Inital Conditions for Active Elements in $28V$ in, $5V$ out Case

3.3.4 Results

In Fig. 3-3, the circuit is simulated for 40 μs with a time step of 1 ns and the inductor current in one side is shown. The magnetizing inductance current, $I_{L_{1p_\mu}}$ exhibits continuous conduction as expected. From there, I_{d1} used in Section 3.2 is about 0.5 A as expected and so is 14 A for I_{d2}. The output current, $I_{D_{13}}$ has a high frequency components of about 30 MHz which decays rapidly. This high frequency component is due to the leakage inductance, L_{1p_k}, of 80 nF and the parasitic capacitance of the $HEXFET\ IV$ of $400pF$. The frequency of this LC pair is given by $2\pi\sqrt{LC}$ which is equal to 28 MHz. A parallel 100 Ω resistor, $R_{L_{2p_{kp}}}$ is added assist the exponential decay of the high frequency component. The results match those determined experimentally from the built circuit.

In Fig. 3-4, the output voltage and the output current are seen to be stabilized after 20 μs. The power input and power output of the flyback converter are calculated by averaging the values from 26 μs to 38 μs. The simulated results are input power is 120.06 W and the output power is 100.34 W. This gives an efficiency of 83.6%. This is a bit higher than the built circuit. The possible source of discrepancies are the circuit ignores the core loss in the transformers (without placing a parallel resistor across the coupling inductor) and the losses due to the control circuitry. In our case, the total transformer core loss of the built circuit is around 2/3 W and the control circuit loss is about 1 W. This gives a closer result of 81% efficiency.

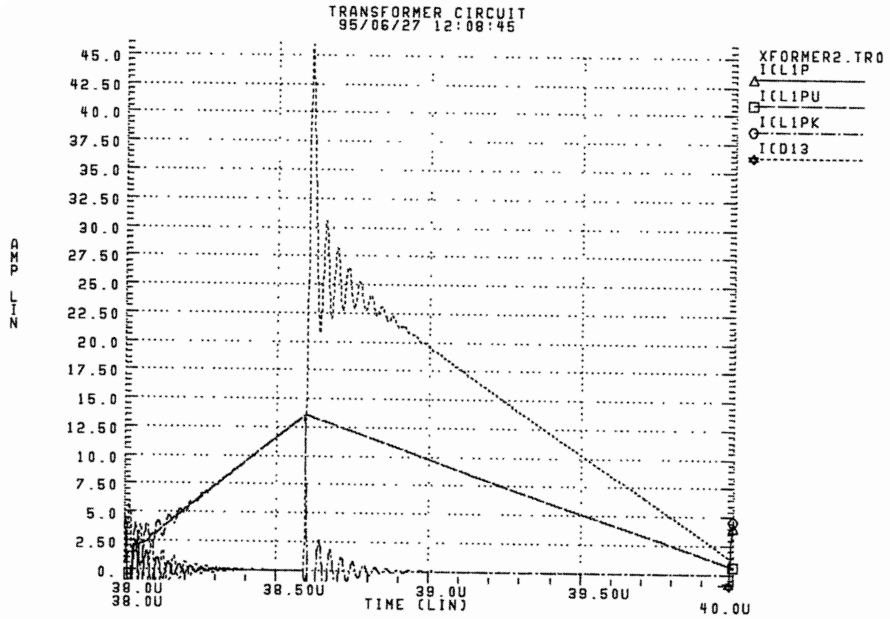

Figure 3-3: Simulated Current Waveform of the Flyback Converter

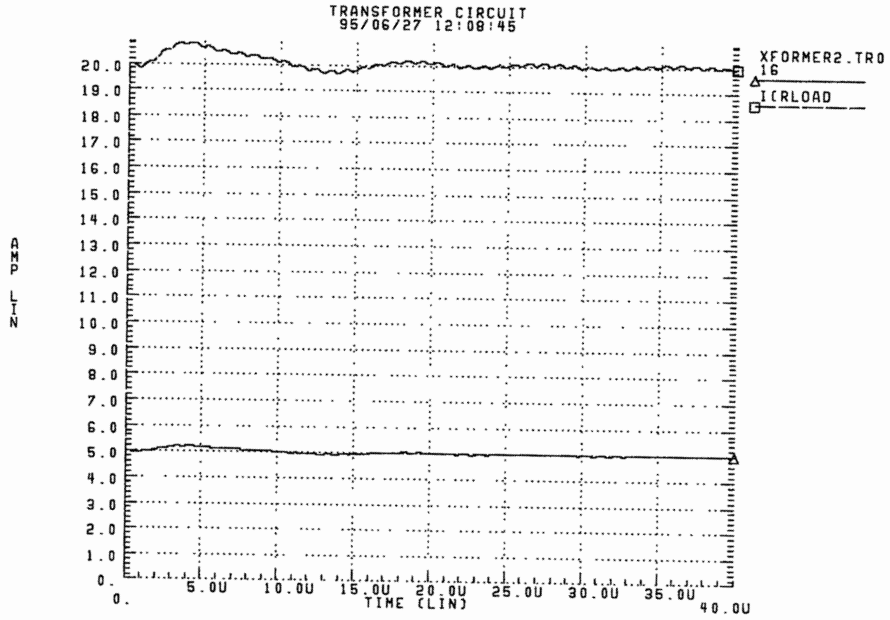

Figure 3-4: Transient of the output voltage and current of the Flyback Converter

Chapter 4

Energy Enhancement Strategies

In Chapter 3, the efficiency is found to be around 80% in the simulated flyback converter. One of the three major sources of energy losses is the leakage inductance loss. In this Chapter, a method of recovering part of this loss is discussed. It includes the details of how to chose various components, the underlying principles of how the circuit works and some simulations on sensitivity analysis on the switching time and various voltage and power combinations.

4.1 Background

As presented in Section 3.2, one of the major energy losses is the leakage inductance loss. The leakage loss which is $\frac{1}{2}LI^2f_{sw}$, where $L = 80\ nH$ and $I = 13.5\ A$, accounts for $7.3\ W$. The leakage inductance, L_{pk}, and the switching MOSFET parasitics capacitance gives a characteristic impedance of $\sqrt{\frac{L_{pk}}{C_{par}}}$ where $L_{pk} = 80\ nH$ and $C_{par} = 400\ pF$. This gives a value of 14.1 Ω. This resistance leads to an overshoot of 170 V $(14.1\Omega \cdot 12V)$ during the transient of the switching. This, in fact, is over the avalanche of the switching MOSFETs, which is equal to 150 V. The method of preventing this to happen during the switching transient is to use a clamp circuit which includes a diode and a clamped capacitance connected parallel to the switch. However, the energy stored in the clamp circuit must be removed by some means. For instance, a capacitance of 10 nF has a a power dissipation of $\frac{1}{2} \cdot 10n \cdot (60V)^2 \cdot \frac{1}{2}MHz$, which is

equal to 12.5 W! (60 V is the voltage across the open switch). The typical method of removing this amount of energy is through a resistance. In this way, energy stored will be lost and there will be an extra cost in an heat sink to remove the heat generated.

4.2 Operation

Instead of using a diode for the clamp circuit, a secondary switch is used. It acts as a simple clamp circuit when the secondary switch is off. The basic operation is that when the primary switch is off, the leakage current flows through the body diode of the secondary switch to the clamped capacitance where charges are stored up. Just before the primary switch is turned on, the secondary switch is switched on, the current flows back into the leakage inductor removing charges from the clamped capacitance and recovering the leakage loss.

4.2.1 Values of the Devices

The clamped capacitance and the switching MOSFET must be chosen in such a way that the energy losses due to the switching is less than the energy recovered.

The clamped capacitance is calculated from $2\pi\sqrt{L_{leakage}C_{clamp}} = f_{sw}$,where $f_{sw} = 500\ kHz$ and $L_{leakage} = 80\ nH$. The required clamped capacitance is 11 nF.

The characteristic impedance, in this case is 2.7 Ω ($\sqrt{\frac{80nH}{11nF}}$). This gives a overshoot of 36.5 V overshoot during the switching transient, which is much lower than that of the primary MOSFET. With a maximum switching voltage of 66 V (56 V from input with 10 V reflected from output), the maximum clamped voltage the MOSFET has to withstand is around 100 V. Thus, a $HEXFET$ of 100 V is chosen for this operation.

The on-state resistance of a surface-mounted $HEXFET\ I$ MOSFET is about $\frac{1}{2}\ \Omega$. With a leakage current of around 10 A for quarter of a cycle, the power dissipation of the recovery circuitry is given by $(\frac{1}{2}\Omega)(10V)^2(\frac{50ns}{2us})$ which is about 1.2 W. The energy loss due to a leakage current loss is about 7 W, thus about 5 W of energy, about 5% increase in efficiency, is expected to be recovered after the implementation.

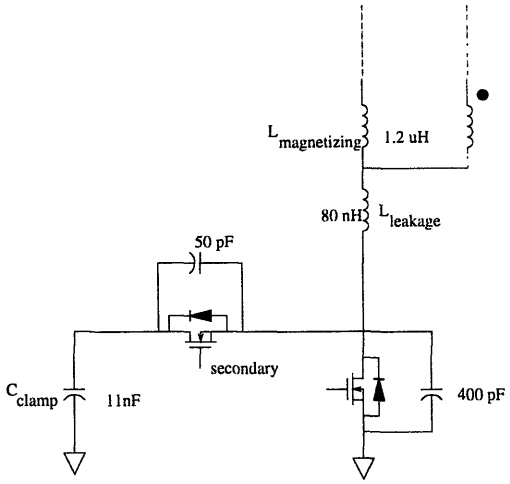

Figure 4-1: Details of the Recovery Circuit

4.2.2 Details Of Operation

The secondary switch is designed to turn on before the primary switch is on and close when the primary switch is off. The secondary starts to turn off when the primary switch begins to turn on, thus providing a path for the leakage inductor current. The leakage inductance is coupled with the clamped capacitor instead. In that way, the rate of change of the device voltage and current is kept low enough for correct and reliable operation during the switch transition.

When the secondary switch is off, the equivalent capacitance is equal to the series combination of 11 nF clamped capacitance and the 50 pF parasitic capacitance of the $HEXFET\ I$, which is approximately equal to 50 pF. When the secondary switch is on, the equivalent capacitance of the recovery circuit is simply 11 nF. When the primary switch is turning off and the second switch is off, the equivalent capacitance is the parallel combination of 400 pF from primary switch and 50 pF from the secondary, which is the sum of the two. This 450 pF rings with the 80 nH leakage inductance to give a high single spike of 167 MHz.

Then when both switches are off, the recovery circuit acts like a simple clamp circuit and the 450 pF equivalent capacitance rings with the 1.2 μH magnetizing inductance. The clamping current oscillates with a frequency of 43 MHz and decays rapidly as the clamping capacitance is charged up.

During the off-state of the primary switch, when the secondary switch is turned on, the parallel combination of 11 nF clamp capacitance and the 400 pF parasitic capacitance of the primary switch rings with the 80 nH leakage inductance resulting in a high spike of 33 MHz. Then the equivalent capacitance rings with the series combination of the magnetizing inductance and the leakage inductance with a frequency of 8.7 MHz. The recovery circuit removes charges from the clamped capacitance by reversing the current flow. The current ease to flow when the voltage of the current equal to the input voltage. At that time, the secondary switch is switching off while the primary switch starts to switch on. When the secondary switch is off and the primary switch is on, the clamped voltage is lower than the input voltage by its characteristic impedance multiplied by the leakage current. It acts as a turn-on snubber for the primary switch. (V_{clamp} is approximately equal to $V_{in} - I_{pk} \cdot \sqrt{\frac{L_{pk}}{C_{clamp}}}$ after the undershoot during ringing, as shown in Fig. 4-2)

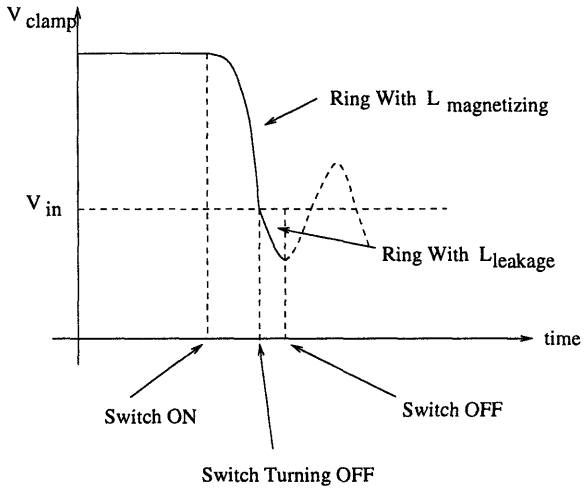

Figure 4-2: Voltage Profile of the Clamp Voltage During Switching On

4.3 Results

As shown in the current waveform in Fig. 4-3, current is recovered during the on-state of the secondary switch.

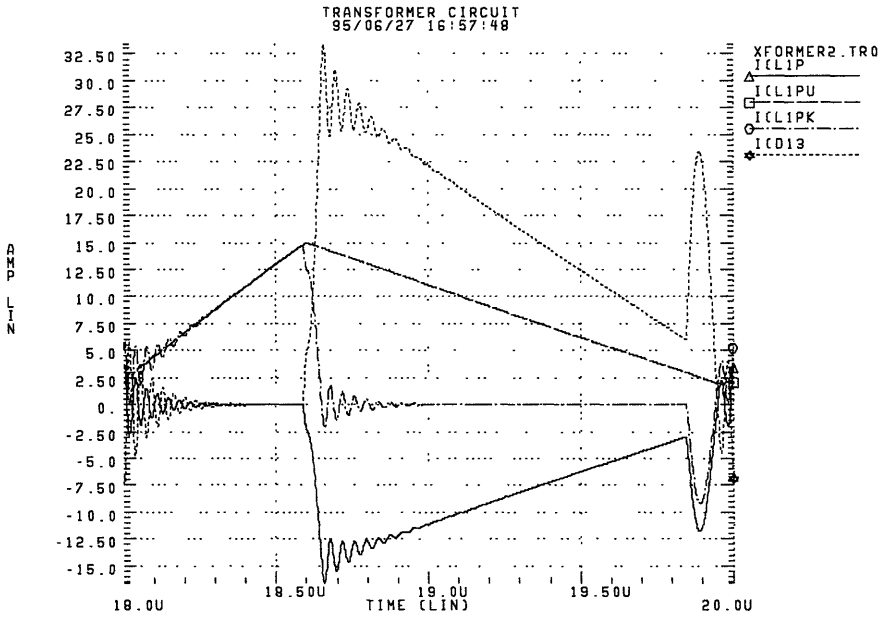

Figure 4-3: Simulated Current Waveform of the Flyback Converter with Recovery Circuit

Both output voltage and output current in Fig. 4-4 have increased under the same duty cycle. The input power is found to be 125.6 W and the output power is 109 W, which gives an efficiency of 89.2%. Comparing with the simulation without the recovery circuit in Section 3.3.4, there is an increase of 5.6%. This appears to be consistent with the analysis done in Section 4.2.

Figure 4-5 shows the details of the simulated waveforms of the clamped current, i_{clamp} during the switching cycle. When the primary switch turns off and the secondary switch remains off, the simulation gives a high spike of frequency of 160 MHz following a rapid transient of frequency of 30 MHz. When the secondary switch starts to turn on while the primary switch is off, there is a high frequency spike of 40 MHz. Then it starts to oscillates for half a cycle of frequency 5 MHz.

The simulated results fall within the same order as expected in Section 4.2. The discrepancies are due to the fact that the parasitic capacitances of the Schottky diodes in the secondary side have not be taken into account during the analysis.

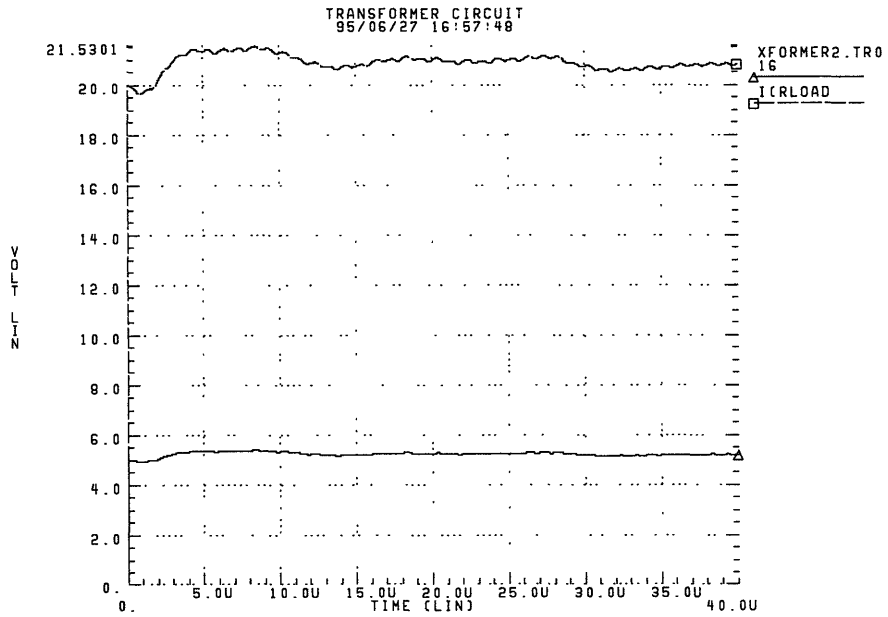

Figure 4-4: Transient of the output voltage and current of the Flyback Converter with Recovery Circuit

4.4 Further Studies

Several simulations are carried out to investigate the effects of varying the parameters on the effectiveness of the recovery circuit. Figures 4-6 and 4-7 show the effect of varying the duration of the turn on of the secondary switch. The results are encouraging. As shown in Fig. 4-6, the output power, P_{out} and the input power, P_{in} remains almost steady. This gives a flat efficiency curve in Fig. 4-7. This sensitivity analysis implies that the recovery circuit can function properly even under a fair amount of fluctuation in the turn-on time. From Table 4.1, the efficiency outperform the non-recovery one by more than 3% throughout.

The studies on the sensitivity on various rated power and different input voltages give a mixed signal. As shown in Figs. 4-8, 4-9, the recovery circuit outperforms the non-recovery one in both cases. However, the gain in efficiency, which is the vertical difference between the two sets of data in each plot, fluctuates by a fair amount from the operation of 50 W to 100 W. In particular, it does not have any regular pattern. In Fig. 4-8, the gain in efficiency seems to be diverging out in 28 V case, while in Fig.

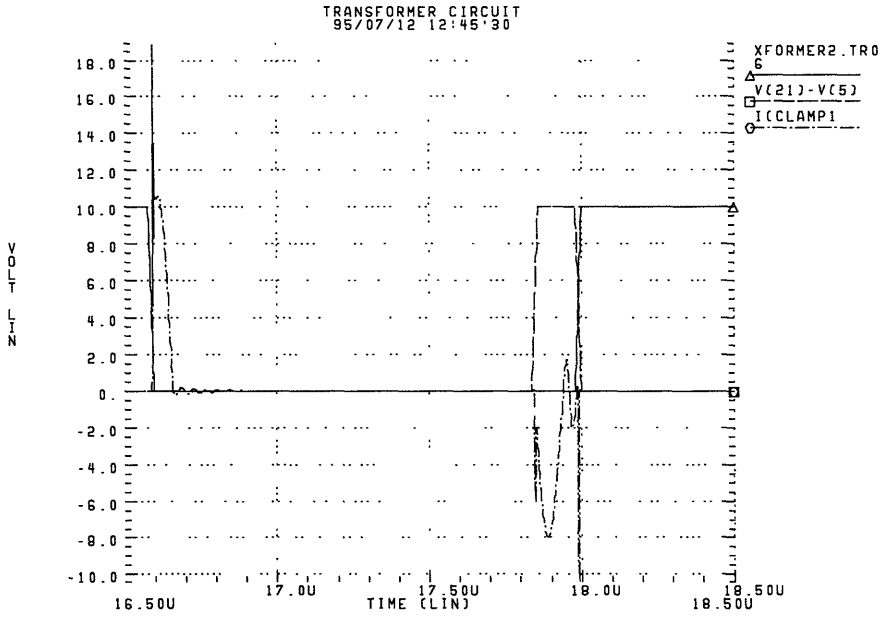

Figure 4-5: Currents Profile during Recovery Circuit Switching

4-9 , the gain seems to be at its maximum in the center for the case 16 V. There is no conclusive result drawn unless further investigation is performed.

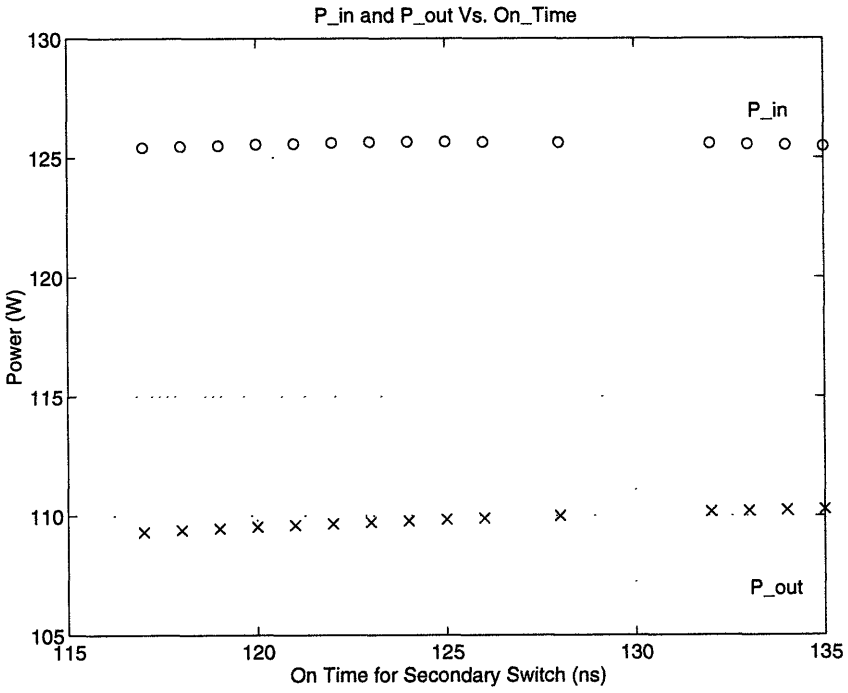

Figure 4-6: Sensitivity Analysis : P_{in} and P_{out} Versus On-time, 28 V case

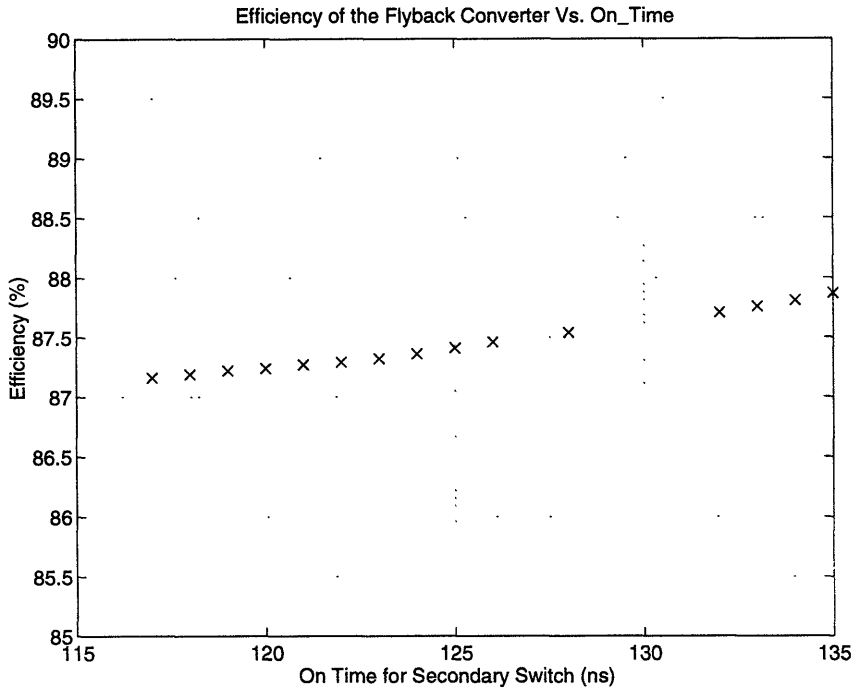

Figure 4-7: Sensitivity Analysis : Efficiency Versus On-time, 28 V case

$Switch_{on}$ (ns)	P_{out} (W)	P_{in} (W)	Efficiency
117	109.32	125.43	87.16
118	109.40	125.48	87.19
119	109.47	125.51	87.22
120	109.54	125.56	87.24
121	109.61	125.59	87.27
122	109.67	125.63	87.29
123	109.73	125.66	87.32
124	109.79	125.67	87.36
125	109.85	125.67	87.41
126	109.90	125.66	87.46
128	110.00	125.65	87.54
132	110.17	125.6	87.71
133	110.21	125.57	87.76
134	110.24	125.54	87.81
135	110.27	125.49	87.87

Table 4.1: Sensitivity Analysis on the Width of the On-State in 28 V in, 5 V out Case at $C_{clamp} = 10\ nF$

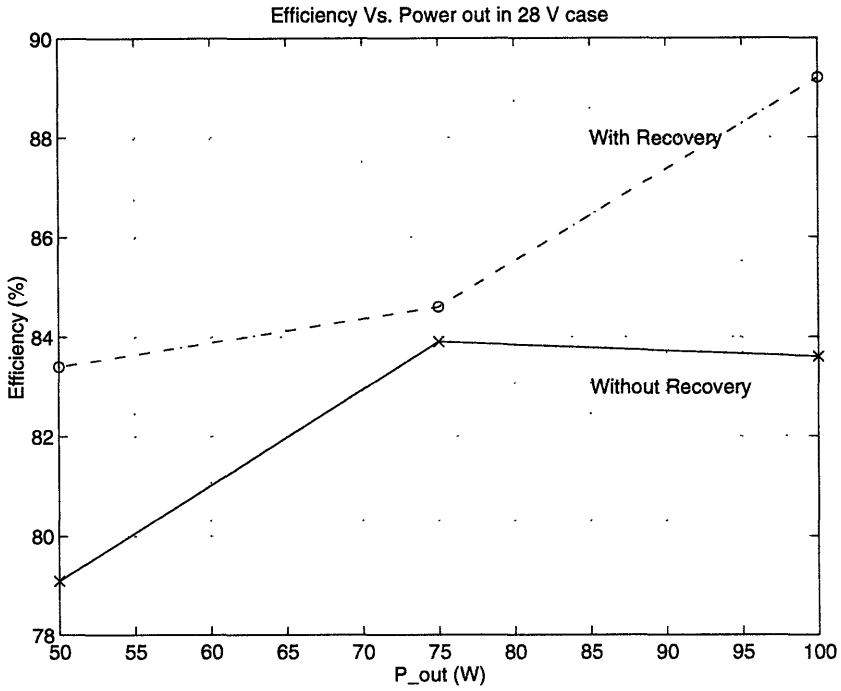

Figure 4-8: Sensitivity Analysis : Efficiency Versus Rated P_{out}, 28 V case

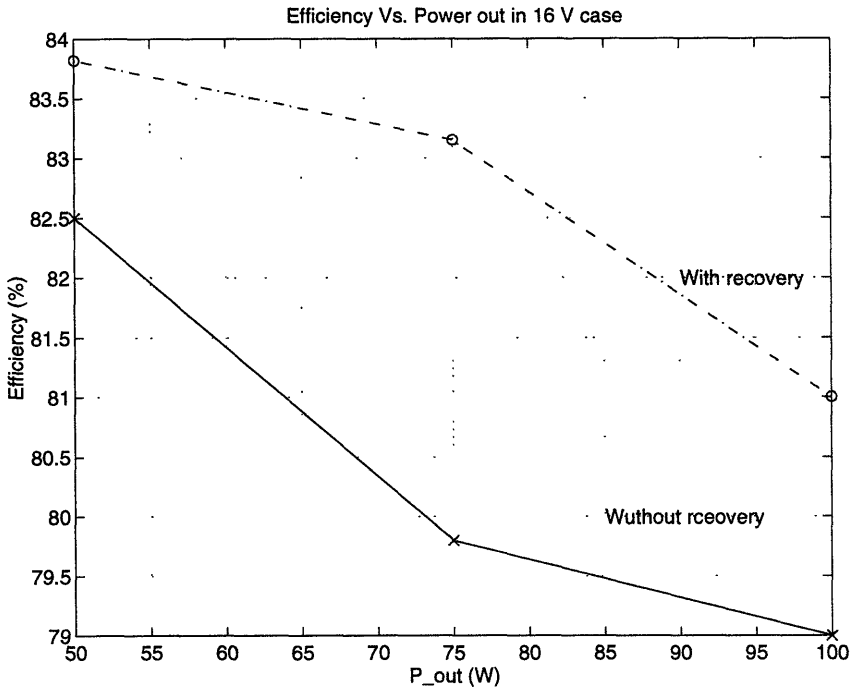

Figure 4-9: Sensitivity Analysis : Efficiency Versus Rated P_{out}, 16 V case

Chapter 5

Large Scale Transient Modeling

In order to fully investigate the performance of the flyback converter for ac, dc and transient conditions, a large signal model is needed. This chapter investigates the SPICE modeling of the flyback converter developed in Chapter 3 and 4 with the current mode control circuit. Two approaches are adapted. The first method is based on the simplification of the SPICE model developed in Chapter 2 and 3. The second method is the development of an averaged model around the operating points. Simulation results from both methods are discussed and compared.

5.1 Current Model Control

The basic current mode control method is shown in Fig. 5-1 for a fixed frequency system. The peak switch current, i_{sense}, is compared to the control signal, $i_{control}$, to determine the on-time of the flyback converter's primary side switch. For a given cycle of operation, turn-on is conincident with the clock pulse and turnoff is conincident with the time that the analog controlled switch current intercepts the control current. This kind of control provides several advantages. The peak current can be easily limited by clamping the control signal, thus enhancing the reliability of the controlled switches. The current feedback loop forces the inductor current to be constant, hence removing a pole and simplifying the system compensation. This also reduces the effect of line voltage changes on the output voltage, providing inherent input line

feedforward correction.

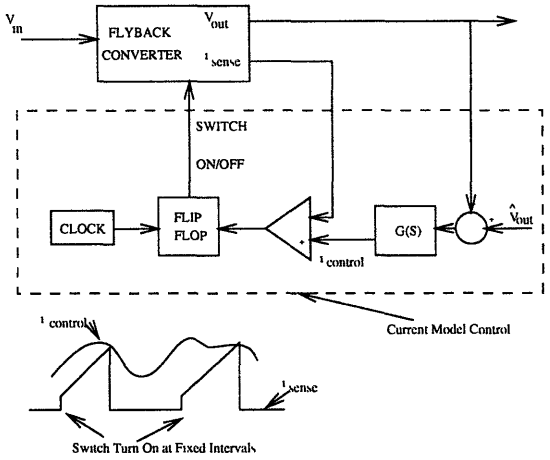

Figure 5-1: Block Diagram of Constant Frequency Current Mode Control

The feedback gain for the continuous conduction current-mode controlled flyback converter is given as

$$G(s) = \frac{g_o(s/z_0 + 1)}{(s/z_0)(s/p_0 + 1)(s/p_1 + 1)(s/p_2 + 1)}$$

The SPICE circuit is realized by cascading ideal op-amp in the following manner. First reorder the transfer function into the following groups

$$\frac{g_0}{s/z_0} \cdot \frac{s/z_0 + 1}{s/p_0 + 1} \cdot \frac{1}{s/p_1 + 1} \cdot \frac{1}{s/p_2 + 1}$$

where g_0 is the midband transconductance of output voltage to the average output current reflected to the primary side. The typical value of g_0 for the flyback converter is between 6 and 7 Ω^{-1}. Then the implementation term by term with op-amp is shown in Fig. 5-2

The op-amps are implemented as voltage controlled voltage source. As the op-amps are treated as ideal, dynamic range of their transfer functions need not to be taken into account. Resistances are all chosen to be 1 Ω. The corresponding passive elements, capacitances and inductances are given by $\frac{1}{2\pi f}$, where f is the frequency of the corresponding poles or zeros. The first term is a pole at zero, and it is emulated

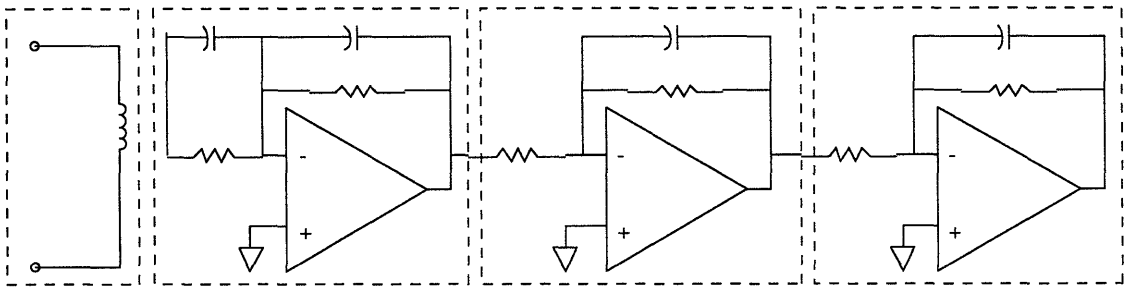

Figure 5-2: Op-Amp Implementation of the Current Mode Control Transfer Function

as the current through the inductor. As mentioned in Section 3.3.1, SPICE does not allow voltage/inductor loops. Therefore, as before, a 10 $\mu\Omega$ resistor is added. This gives a pole at R/L with $L = \frac{1}{2\pi 4k}$ and $R = 10\ \mu\Omega$, which is 0.25 Hz instead of an absolute zero. The implemented control circuit has $z_0 = 4\ kHz$, $p_0 = 18\ kHz$, $p_1 = p_2 = 300\ kHz$. The actual implementation with values is shown in Fig. 5-3

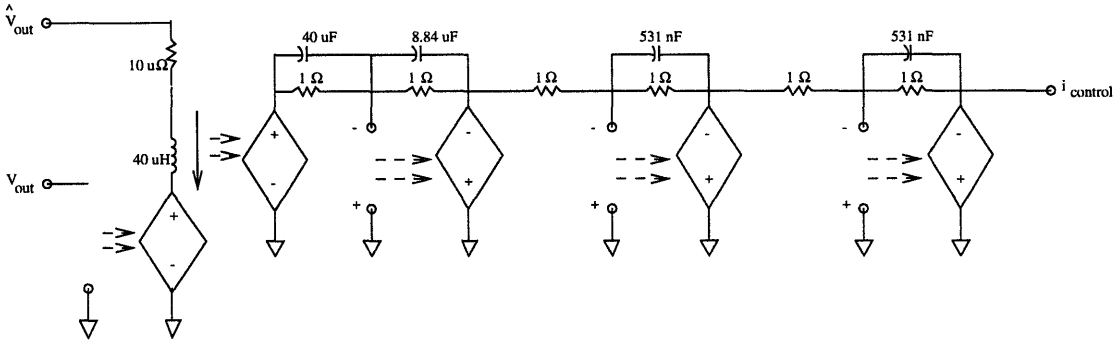

Figure 5-3: SPICE Implementation of the Current Mode Control Transfer Function

The dependent sources emulating the op-amps are inverted as shown. This is to make up the negative sign of the transfer function when signals run across the op-amps, thus removing unnecessary inverter stage.

The transfer function has a plateau of gain of g_0 between the zero frequency of z_0 and the pole of p_0. The DC part settles off quickly as the gain around the DC region is high, while the high frequency components oscillate for a while, but do not contribute to the general waveform of the transient responses. Thus, the response of the transient is mainly dominated by the transconductance of the transfer function around this plateau region. At the frequency of p_0, the time constant is equal to 40 μs ($1/2\pi 4\ kHz$) and at the frequency of p_1, the time constant is about 8.8 μs. Thus,

the expected initial rise time for the flyback converter to startup is around 100 μs.

5.2 Simplified Model

In Chapter 2 and 3, it was found that the time step required for an accurate simulation of the flyback converter is 1 ns. To investigate the transient response under the control mode control is quite inefficient with such a small time step. It requires around 500 μs of simulation time. This order of simulation times require a lot of computation on hourly basis. Also, the simulation results stack up to order of the tenth of mega bytes. In fact, a lot of fine details of the switching operation in the transformer core could be neglected completely. The responses of both the input and the output filters are the major factors to be investigated.

Since the detailed response of the transformer core is not necessary, the leakage inductors in the primary side, L_{pk} are removed. The parallel resistors across the leakage inductors and the series resistors are removed also. The $HEXFET\ IV$ switches are replaced by the same W/L ratioed, simple MOSFET switches. It enabled the time step to increase from 1 ns to 100 ns without the convergence problem during transient analysis.

5.2.1 Results

Figures 5-4, 5-5 and 5-6 are the simulated results with different time steps during the initial startup of the flyback converter using the current control techniques. As shown in the figures, the 90% rise time of the flyback converter with current control is about 20 μs and they take around 100 μs to get to 99%. They are consistent to the predicted results in Section 5.1. All three figures exhibit the same general waveform.

As the time step increases, from 1 ns step in Fig. 5-4 to 10 ns in Fig. 5-5, the waveform becomes coarse and the ripple becomes large. This can be best explained by the fact that the control circuit cannot keep track of the transient change when the time step is too large.

When comparing Fig. 5-5 and Fig. 5-6, besides the fact that the responses become

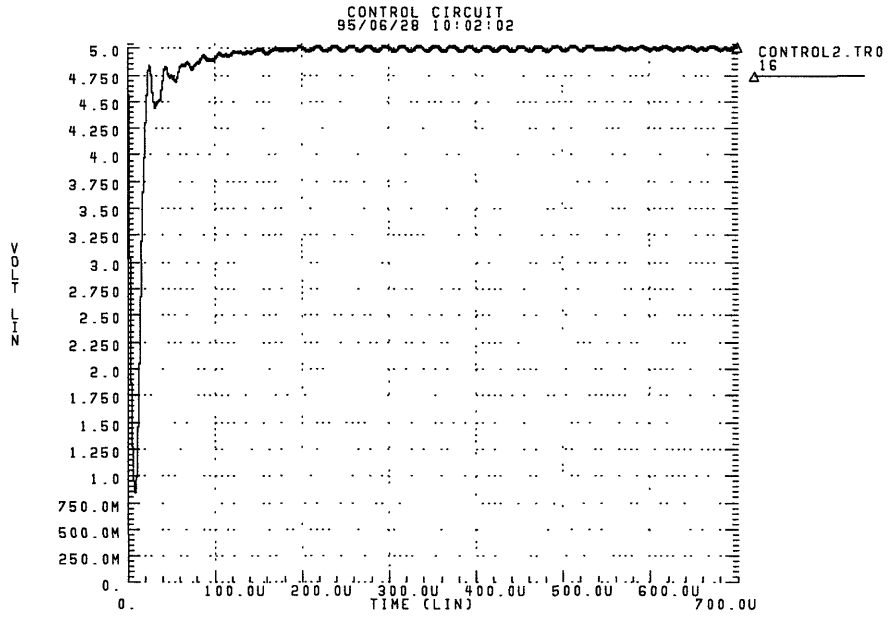

Figure 5-4: Initial Start-Up Response of the Flyback Converter with $1n$ step

coarse when the time step increases from 10 ns to 50 ns in general, there are some similarities in the wave patterns between the time interval of 100 μs and 500 μs and also between 500 μs and 700 μs in both graphs. There are some ripple patterns in each of these two intervals. A possible explanation might be the control signal is sampling too slow that there is aliasing in frequency domain for the high order ripple frequencies. One of the evidence is that in Fig. 5-4 when the time step is equal to 1 ns (high enough sampling rate), such ripple patterns disappear. Further testing on the simulation and on real circuits might be needed to investigate the details of aliasing in the stability of the control circuit.

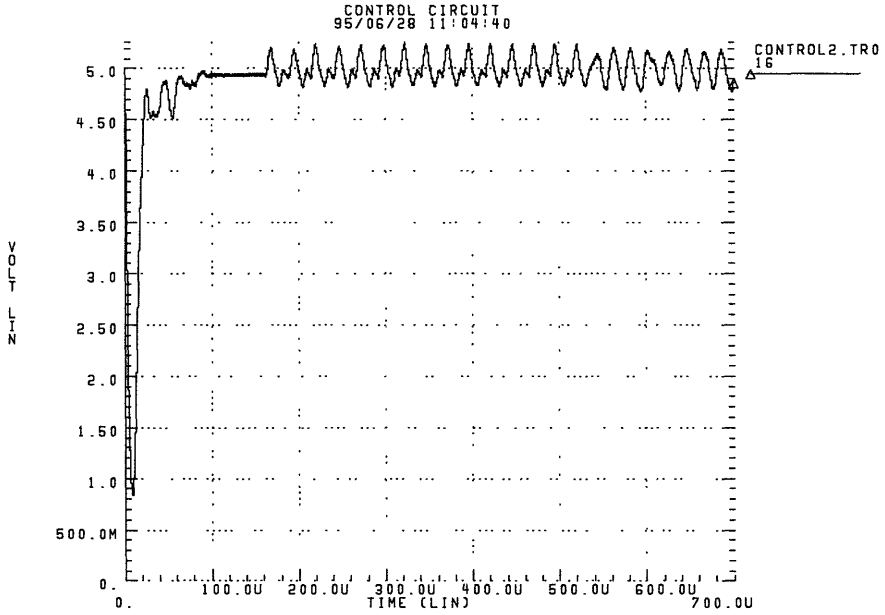

Figure 5-5: Initial Start-Up Response of the Flyback Converter with $10n$ step

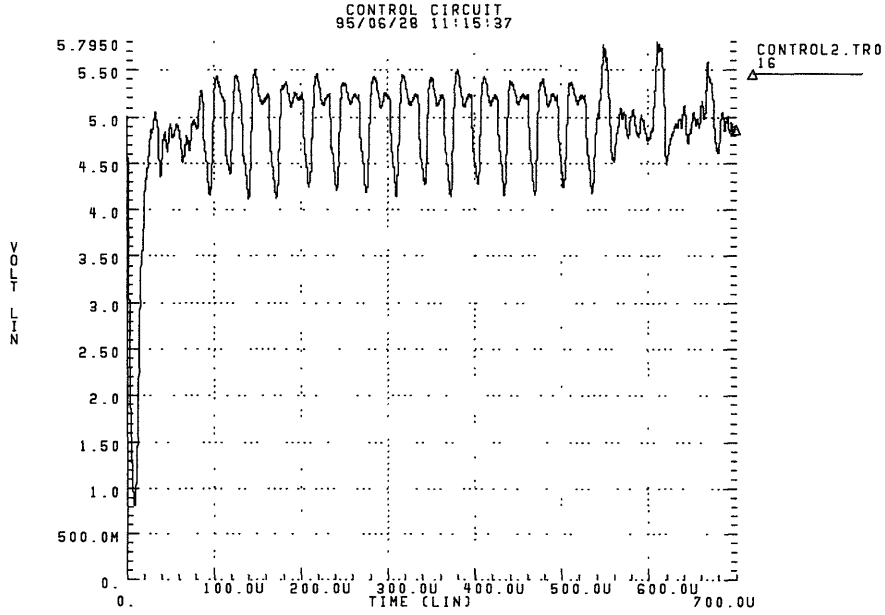

Figure 5-6: Initail Start-Up Response of the Flyback Converter with $50n$ step

5.3 Averaged Model

The switching regulator model developed for SPICE is based on Middlebrook's averaged power stage models [15], which can be applied to ac open and closed-loop analysis. The models also work in dc or large-signal transient analysis, which is needed for our study. These averaged models only assume that the circuit must operate in the continuous conduction mode, where the instantaneous inductor current is not zero anywhere in the switching cycle. The discontinuous conduction is found in [6]. Using state-space averaging, a switching converter can be modeled as an ideal dc-to-dc transformer, in which the turns ratio is controlled by the duty cycle. The SPICE model of the Buck Type is shown in Fig. 5-7.

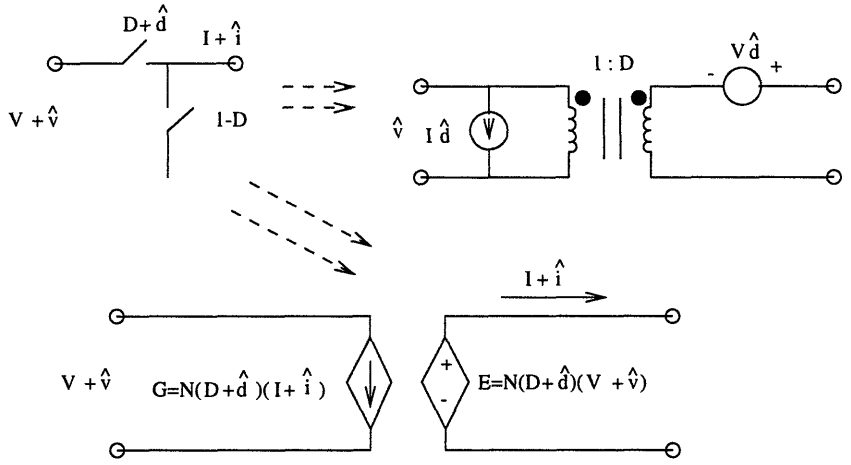

Figure 5-7: Switching Regulator Model for the Buck Type

The SPICE model of the Boost type is shown in Fig. 5-8 This is basically a step up transformer with turns ratio, $(1 - D) : N$.

The flyback converter can be shown as a combination of both the buck and boost power stages with the flyback transformer primary inductance [15]. The SPICE model is shown in Fig. 5-9. It uses the assumption that the flyback transformer is treated as a dc to dc transformer whose turns ratio is determined by the duty cycle, D. The buck power stage used is a step down transformer whose turns ratio is $1 : D$, while the boost power stage is a step up transformer whose turns ratio is $1 - D : N$.

After replacing the transformer core and both switches, $HEXFET$s and power

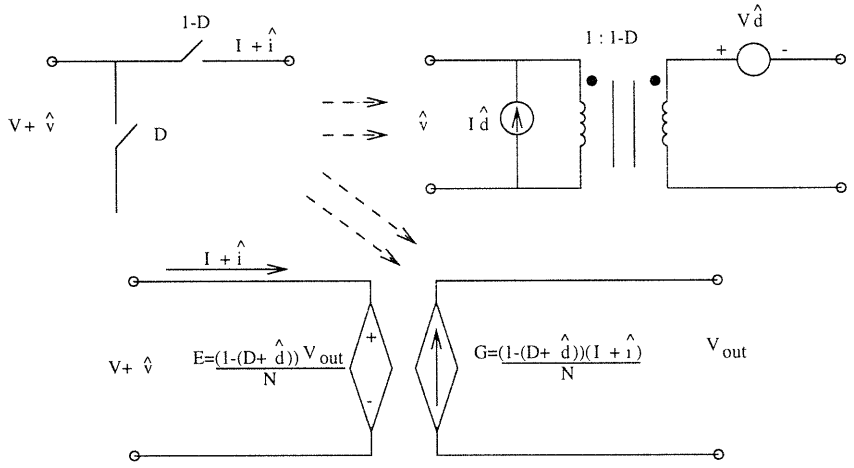

Figure 5-8: Switching Regulator Model for the Boost Type

diodes with the averaged model of the combination of buck and boost power stages. The SPICE code of the averaged model is basically done. It should be noted that switching is ignored and the averaged transient responses is simulated instead.

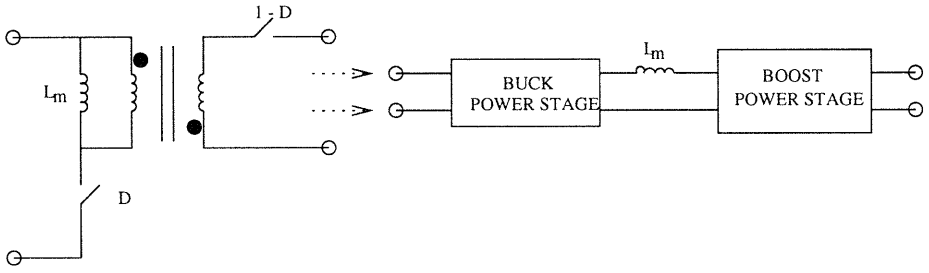

Figure 5-9: Switching Regulator Model for the Flyback Type

5.3.1 Results

Figure 5-10 shows the initial start-up response of the averaged modeled flyback converter with current control. The time step for simulation is 100 ns. There are several advantages over the simplified model discussed in Section 5.2. In particular, the large time step that this model allows is an definite advantage. When comparing the results with those in Section 5.2.1, it is noted that although the time step is much larger used in this model, the general trend of the waveform and the rise time for the initial startup is almost identical. It takes around 100 μs to reach 99% of the nominal

output voltage.

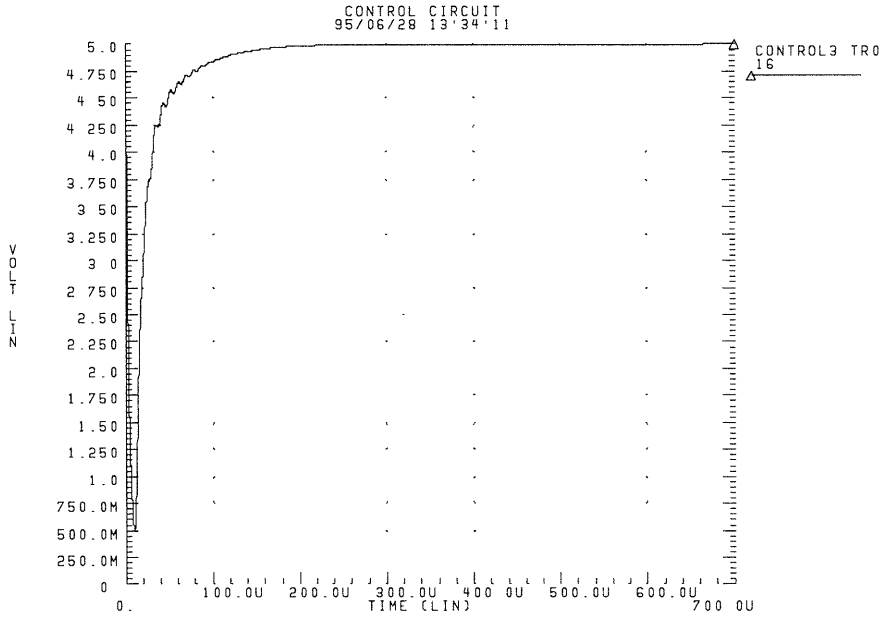

Figure 5-10: Initial Start-Up Response of the Averaged-Model Flyback Converter with $100n$ step

5.4 Further Studies

Audio Susceptability is studied in Figs. 5-11 and 5-12. Audio Susceptability is defined as the ratio of the incremental change of the output voltage around its nominal output voltage to the incremental change of the input voltage around its nominal input voltage, $\frac{\hat{v}_{out}}{\hat{v}_{in}}$. In Fig. 5-11, a $\pm 10\%$ change in the input voltage is applied to the averaged-model flyback converter with current control. From Fig. 5-12, it can be seen that there is an overshoot of 0.83 V around the 5 V nominal output, which is 16.6% change, in response to a 10% upward step change in input voltage. In the downward change, there is an undershoot of 0.89 V, which is around 17.8%. Both of the overshoot and the undershoot settles quickly within 200 μs.

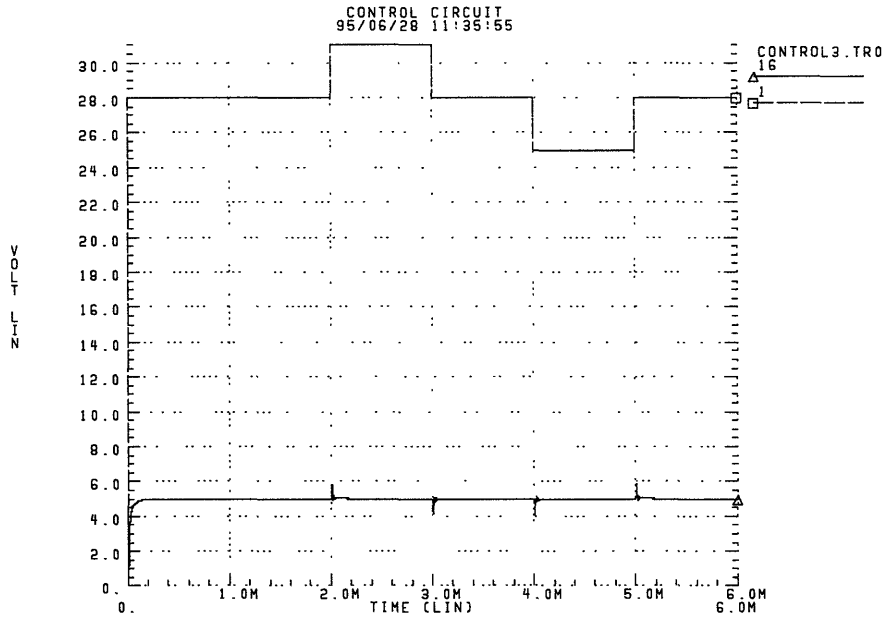

Figure 5-11: Auto Susceptability Response of the Averaged-Model Flyback Converter with $\pm 10\%$ change in v_{in}

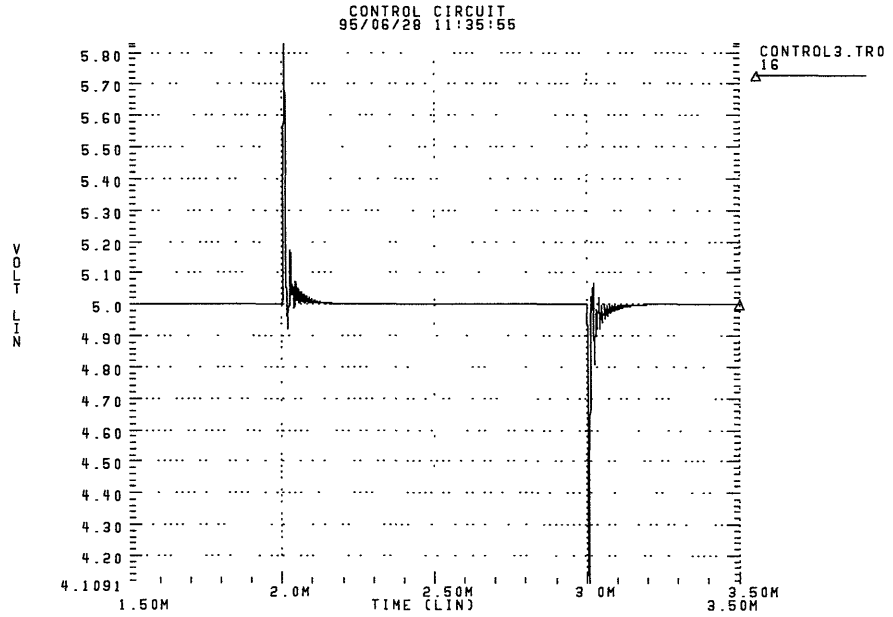

Figure 5-12: Close Up of Auto Susceptability Response of the Averaged-Model Flyback Converter with $\pm 10\%$ change in v_{in}

Loop transmission responses are studied in Figs. 5-13 and 5-14. Loop transmission is the product of the ratio of the incremental change of output voltage around its nominal value to the incremental change of the duty cycle when the input voltage is at its nominal and the minus ratio of the incremental change in duty cycle to the output voltage when the feedback loop is closed, that is $(\frac{\hat{v}_{out}}{\hat{d}})|_{\hat{v}_{in}=0}(\frac{-\hat{d}}{v_{out}})$.

A current step of ± 10 A, (50% of the nominal output current) is connected to the load in parallel. It is noted that both an upward and downward change cause overshoots and undershoots in the output voltage in Fig. 5-13. From Fig. 5-14, for an upward 50% step change in output current, there is an overshoot of 1 V (20% change) and an undershoot of 0.72 V (14.4% change). For the downward 50% change, there is an overshoot of 0.76 V (15.2% change) and an undershoot of 1 V (20% change). It is quite encouraging as a 50% change causes less than 20% change in output. The settling time in both cases is less than 150 μs

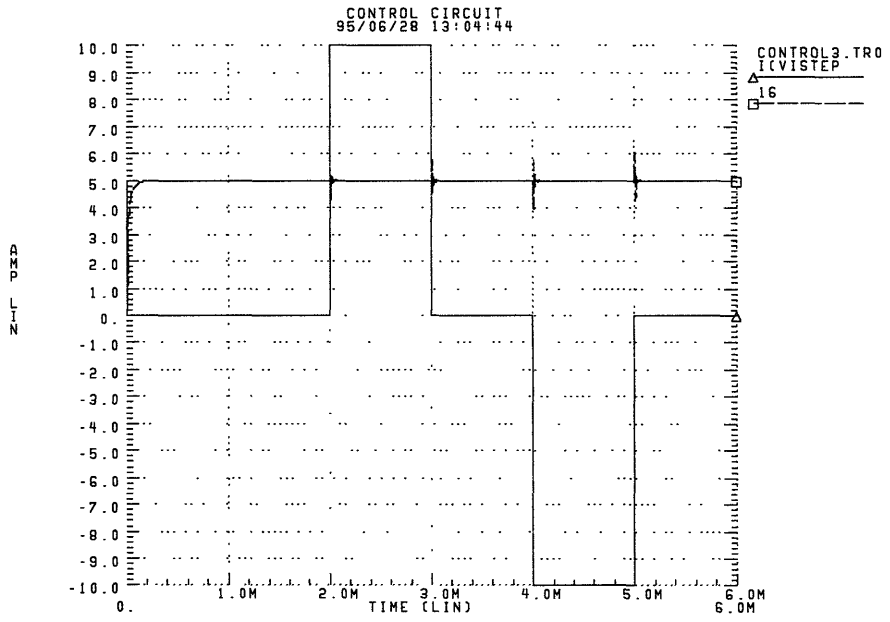

Figure 5-13: Loop Transmission Response of the Averaged-Model Flyback Converter with $\pm 50\%$ change in v_{out}

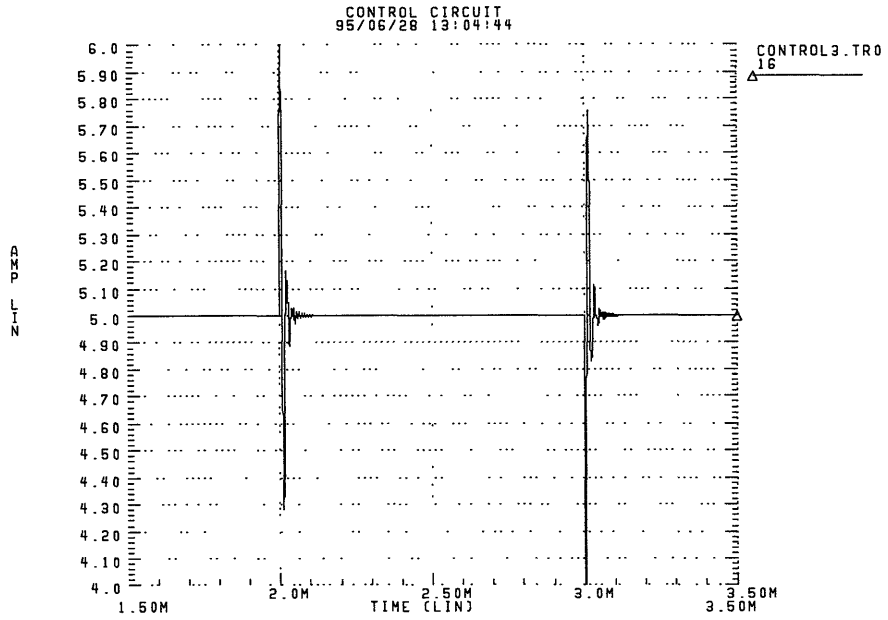

Figure 5-14: Close Up of Loop Transmission Response of the Averaged-Model Flyback Converter with $\pm 50\%$ change in v_{out}

Chapter 6

Two-Port Modeling

In Section 5.3, the averaged model of the flyback converter is developed. This model not only can enhance the speed in simulating the transient response of the current-controlled converter, but also provide a means for the AC analysis from which the frequency response of the input impedance and the output impedance can be found. In this Chapter, the impedances of the current-controlled flyback converter are determined in a particular case. The results are then used in the development of a two-port network. General development details are discussed.

6.1 AC Analysis

The input impedance of the current-controlled flyback converter is defined as the ratio of the incremental change in the input voltage around its nominal value to the incremental change in its input current around its nominal value with a given load. The magnitude and phase of the input impedance with load of 100 W, 0.25 Ω resistance are shown in Figs. 6-1 and 6-2 respectively. The DC gain is 16.8 dB with phase of $-180°$. This corresponds to a negative resistance of 6.9 Ω which is approximately equal to 6.2 (28/4.5), the nominal resistance at DC. The dip of the dB graph occurs around 100 kHz, the input impedance has a lowest value at that region.

The output impedance is simulated by removing the load and injecting a current

i_{out} into the output node. The output impedance is defined as v_{out}/i_{out}. As shown in Figs. 6-3 and 6-4 , the output impedance tends to zero on either DC or high frequency end. It attains the maximum at around 20 kHz with a value of 0.446.

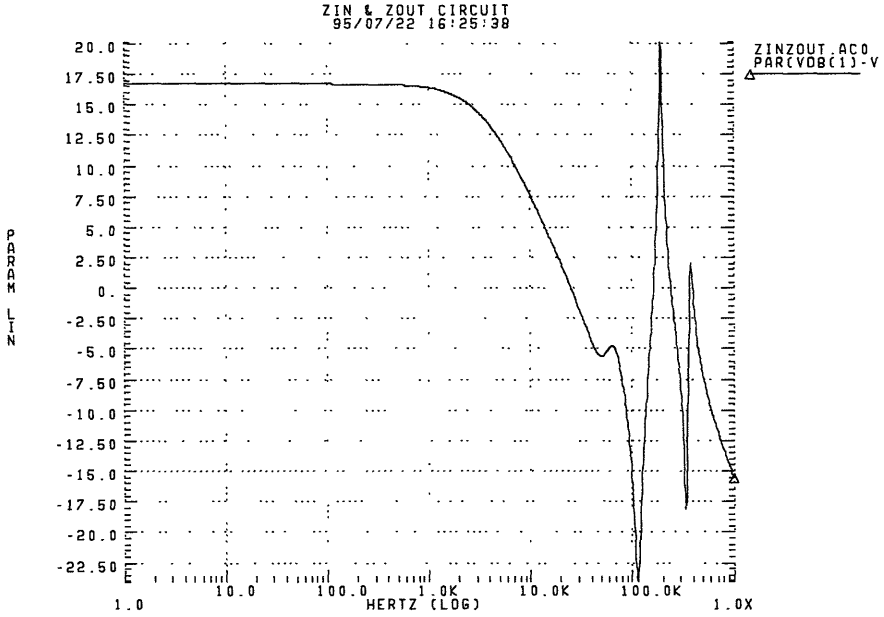

Figure 6-1: Magnitude of the Input Impedance of the Flyback Converter with Current Control (Averaged Model)

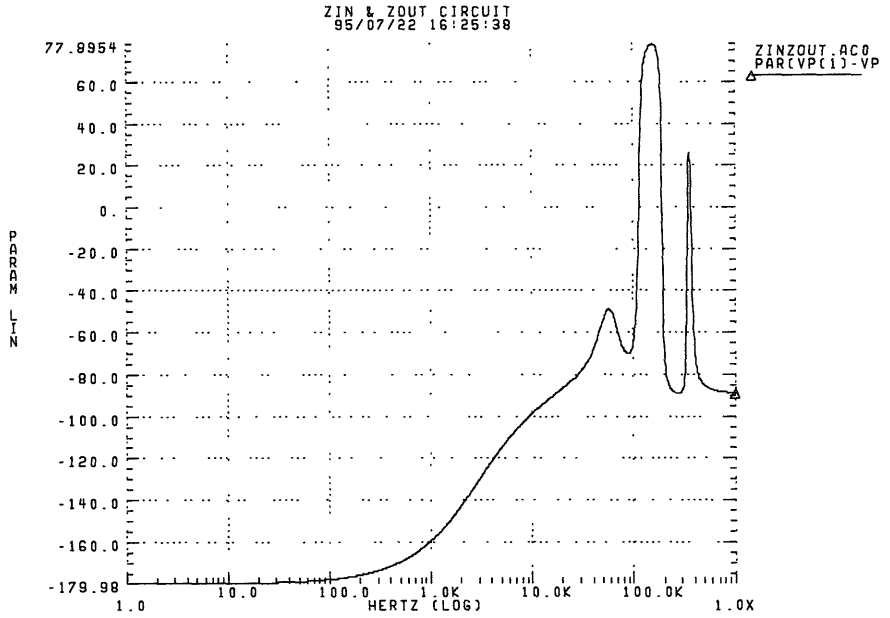

Figure 6-2: Phase of the Input Impedance of the Flyback Converter with Current Control (Averaged Model)

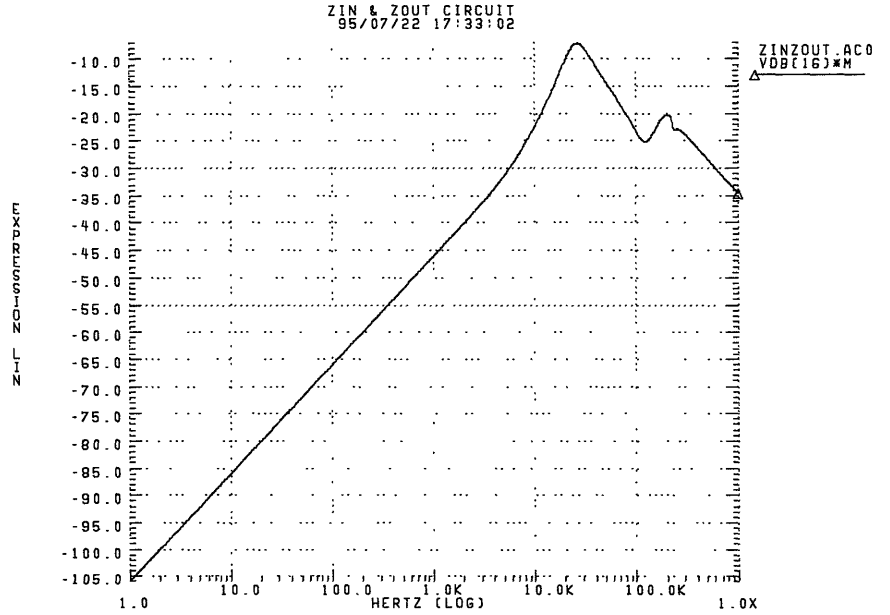

Figure 6-3: Magnitude of the Output Impedance of the Flyback Converter with Current Control (Averaged Model)

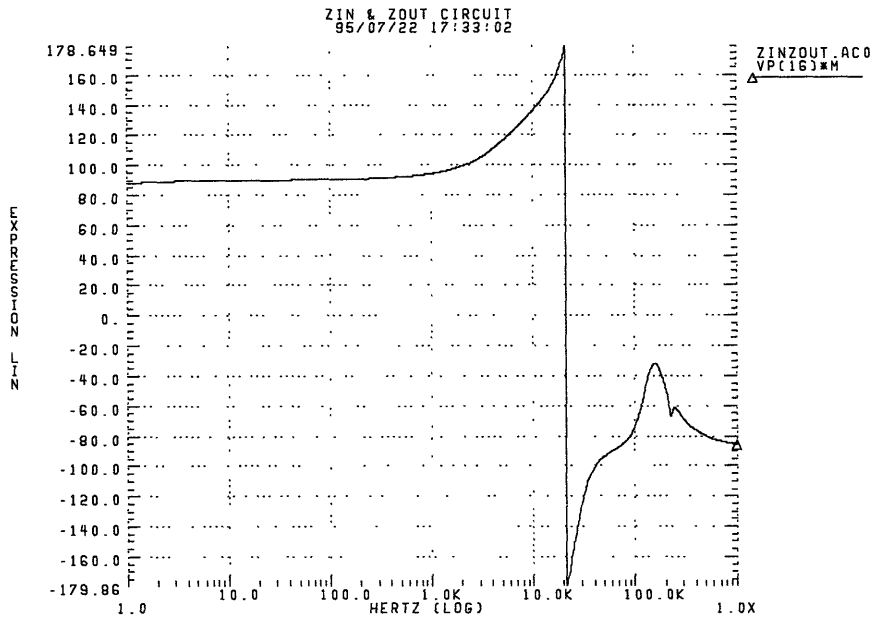

Figure 6-4: Phase of the Output Impedance of the Flyback Converter with Current Control (Averaged Model)

6.2 Two Port Network

6.2.1 Implementation of Input and Output Impedance in SPICE

Both the input impedance, Z_{in}, and output impedance, Z_{out} are given in the form of data derived from experiments. No particular empirical formulas are derived as the impedances alter as the loading condition of the flyback converter is changed. In the case of our study, the input and output impedance used are taken from Section 5.1 The data are gathered using the *.PRINT* command in SPICE.

As Z_{in}, the input impedance, is the ratio of incremental change of input voltage around its nominal value to the incremental change of the input current around its nominal, i.e. $\frac{\hat{v}_{in}}{\hat{i}_{out}}$, the input port is modeled as such in Fig. 6-5. As shown, $Z_{in} = \frac{V_{in}-V_{in\_nom}}{I_{in}-I_{in\_nom}}$ in the figure, while Z_{out} is simply defined as the $\frac{V_{in\_nom}-V_{out}}{I_{out}}$ and it is implemented as shown.

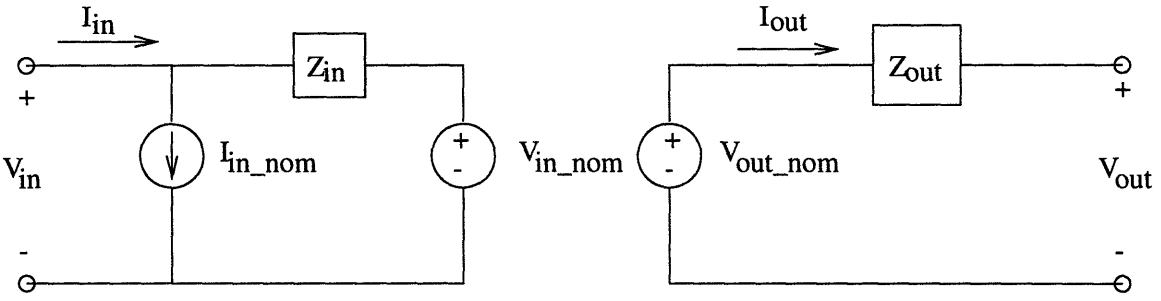

Figure 6-5: Proposed Model for the Two Port Network of the Flyback Converter

The data gathered from the ac analysis of the current-controlled flyback converter are tabled as a frequency response table. The G and E elements (controlled sources) in SPICE can be used as a linear functional block or element with the specific response in the frequency response table. The frequency response is obtained by performing an AC analysis and setting $AC = 1$ in the input source (Laplace transform of an impulse is 1). The input and output of G and E elements are related as $Y(j2\pi f) = H(j2\pi f) \cdot X(j2\pi f)$. In our case, the transfer function is $Z(s) = \frac{V(s)}{I(s)}$. In other words, $I(s) \cdot Z(s) = V(S)$. This implies that with $I(s)$ as the input, $V(s)$ can be obtained as

a function of $Z(s)$. This method is used for implementing the complex impedances. The impedances are implemented as dependent voltage sources which are dependent on the line current. The line current is related to the external input and this is how the two port network interact with the external sources and loads. The SPICE implementation of the Two Port Network is shown in Fig. 6-6.

The general form of the dependent voltage source with frequency response tables is

$$\text{Exxx } n_+ \; n_- \text{ FREQ } in_+ \; in_- \; f_1, \, db_1, \, \phi_1, \, ..., \, f_i, \, db_i, \, \phi_i$$

The f_i is the frequency point in Hertz, db_i is the magnitude in dB and ϕ_i is the phase in degrees. At each frequency the network response, magnitude and phase, is calculated by interpolation. The magnitude is interpolated logarithmically as a function of frequency. The phase is interpolated linearly.

The data are entered in three columns. The first column is the frequency in Hertz, second column is magnitude in dB, and third column is phase in Degree. The phase can be wrapped and unwrapped. However, the SPICE phase output is always the wrapped one.

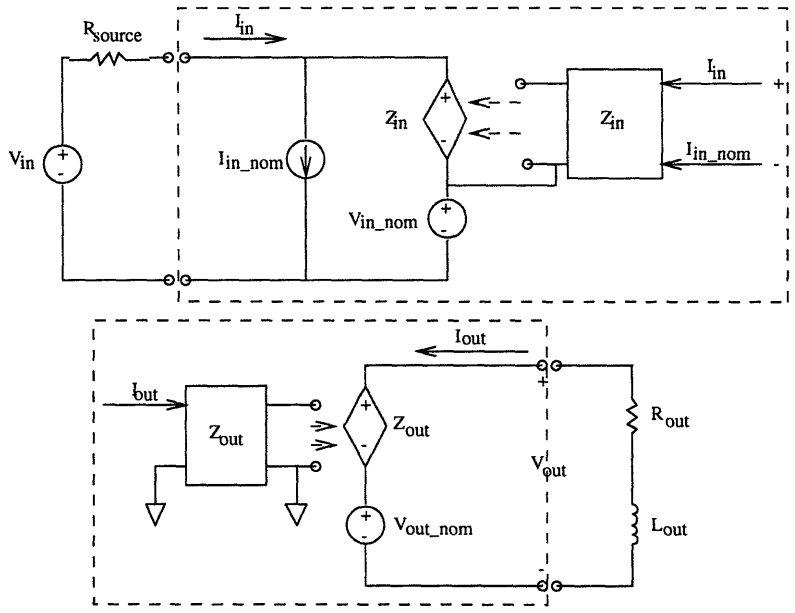

Figure 6-6: SPICE Implementation of the Two Port Network of the Flyback Converter

6.2.2 Results

Figure 6-7 is the magnitude and phase of the input impedance simulated by AC analysis. The shape of both the magnitude and phase is the same as in Fig. 6-1 and 6-2 in Section 6.1. The waveforms appear to be a bit coarser. It is due to the fact that the data points of the responses are obtained from interpolation. The number of samples used in the simulation is only 60.

In Fig. 6-8, the magnitude and phase of the output impedance are similar to those obtained from Figs. 6-3 and 6-4 in Section 6.1. As discussed above, the waveforms appear to be a bit coarser. It is noted that the phase is shifted by 360° in the region between 20 kHz and 30 kHz range. As discussed in the previous section, such a phase wrapping (±360°) does not affect the responses of the filter.

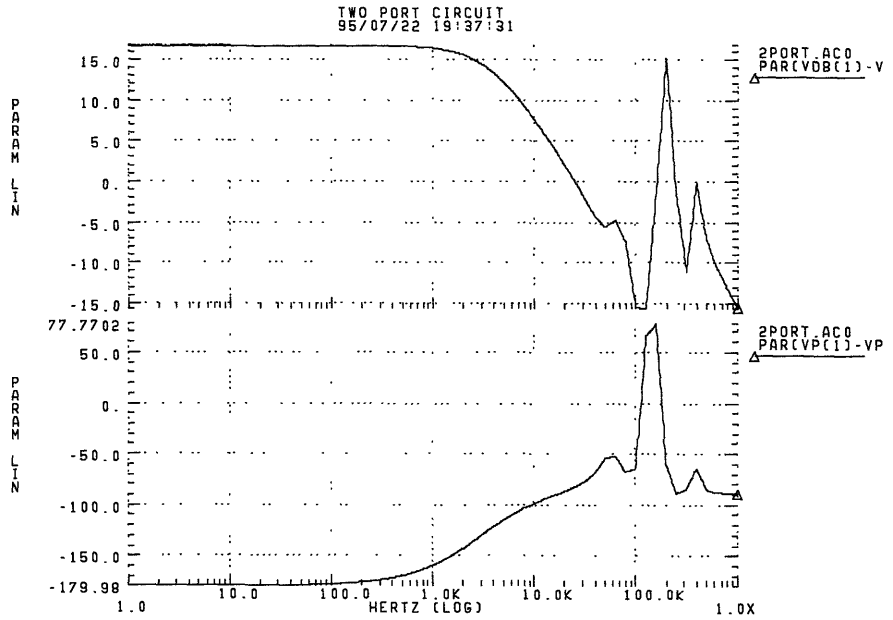

Figure 6-7: Magnitude and Phase of the Input Impedance of the Two Port Network

6.2.3 Further Studies

As shown in Fig. 6-6, the input external source consists of an ideal source with its series input resistor. The value of the resistor plays an important role in the convergence

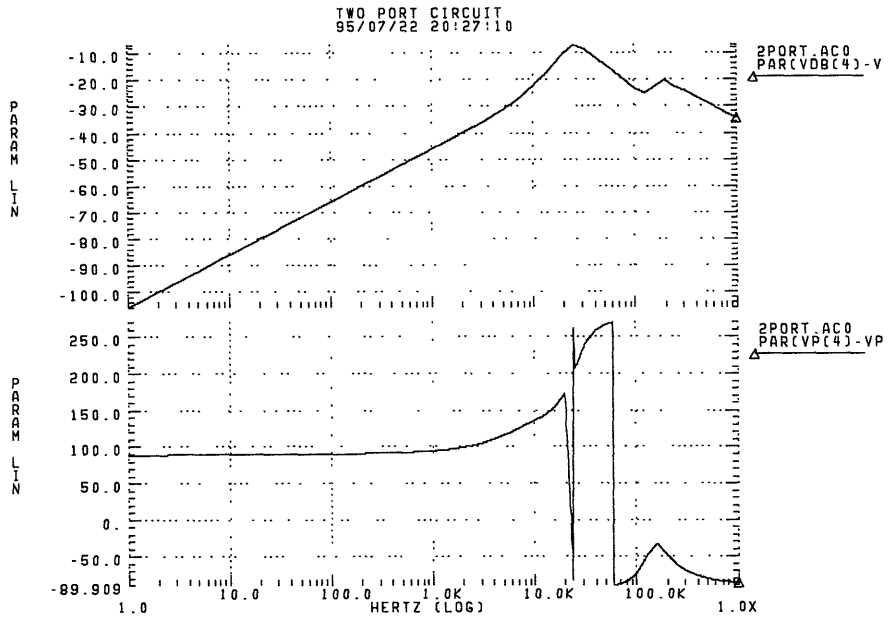

Figure 6-8: Magnitude and Phase of the Output Impedance of the Two Port Network

of the transient simulation of the two port network. For AC analysis, the frequency response is determined by the transfer function at that particular frequency. For operating point and DC sweep analysis, the relation is the same but the frequency is set to zero. The transient analysis is more complicated, the output is the convolution of the input current waveform with the transfer function.

It is found that at DC point, the input impedance of the two port network appear to be negative. The total input resistance looking from the ideal source is the sum of the R_{source} and Z_{in} in Fig. 6-6. The two port model implemented is an incremental model that provides a mean to test the stability of implementing different type of R_{source}s.

In Fig. 6-9, R_{in} is chosen to be 1 Ω and the frequency is at 25 Hz. The input voltage and current is 180° out of phase. This is consistent with the model. When the input voltage rise up, the input current is driven down to maintain the constant power.

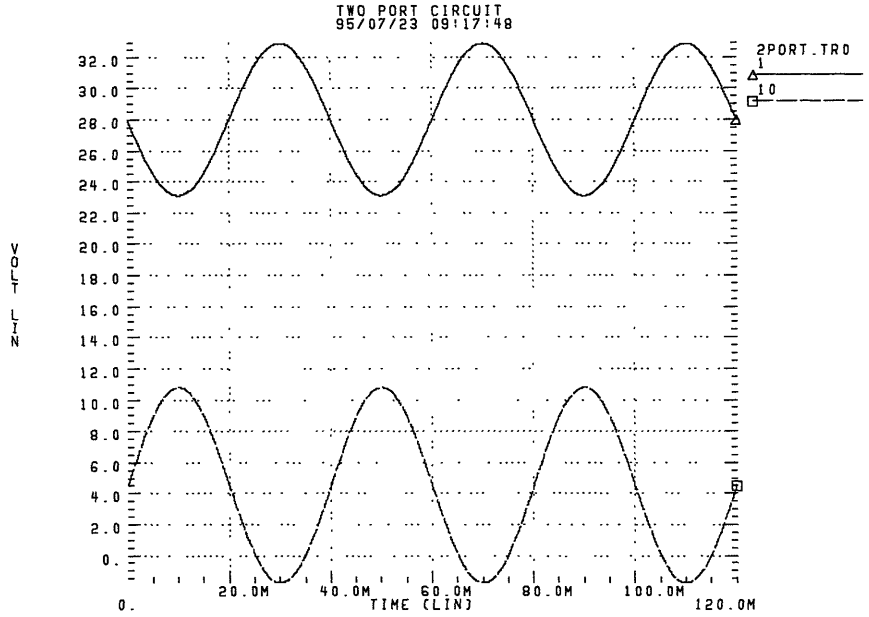

Figure 6-9: Response of the Two Port Network with an Input Voltage and Input Resistance

Chapter 7

Conclusion

The SPICE simulation of the hybrid built 28 V input, 5 V output, 100 W power double-ended flyback converter is generally completed. Three different classes of SPICE codes are developed for different needs.

In chapter 2, SPICE models of power transistor and Schottky diodes are tailor-made to suite the design of the flyback converter. Particular attention are paid to reverse recovery effect of the power diodes, the nonlinearity of the gate-drain capacitance of the power MOSFET and core and resistive losses of the transformer core.

In chapter 3, the whole flyback converter is simulated. Both rough energy losses estimation and experimental determined results agree with the simulation results. The simulated efficiency is 83.6% which is a bit higher due to the neglect of core losses and control circuit losses.

In chapter 4, a snubber-like current recovery circuit is proposed and tested. This current recovery circuit, with careful timing show an increase of efficiency of about 5%. Sensitivity analysis shows that the recovery circuit is functional under a fair range of turn-on time. Different voltage and power combinations are tested and there is a gain in efficiency of at least 3% in general.

In chapter 5, both the simplified model and averaged-model are developed to investigate the effectiveness of the large scale transient model. It is found that the simplified model although gives more detail on the response requires a much smaller

time step, $\leq$ 10 ns, to simulate. The averaged model, on the other hand, only simulates the average response of the control waveform, can be used with larger time step, 100 ns and still maintains the general shape of the transient response.

In the last chapter, the averaged model is used to determine the input and output impedances of the closed-loop flyback converter by AC analysis. Results are used for modeling the two port network. By making use of viewing the impedances as a transfer function from current to voltage, the two port network of the flyback converter is completed.

On the whole, there are three different classes of SPICE codes developed for the flyback converter in different type of design stage. The detailed model is developed for the sake of element selection during the transformer design stage. The large signal model is in general for the use of the design of controller circuit for the transformer. The final stage is used as a simple module in a large power network where details of the converter is no longer needed.

7.1 Further Research

In Section 4.4, some different combinations of voltage and power pairs are studied and the simulation results compared. It is found that the efficiency and power profile is not quite explainable.

One of the suggestion is that the efficiency versus power-out curve operates differently in the case without current recovery and that with current recovery. The efficiency frontier with recovery circuit is in the lead of that without recovery. For instance, in Fig. 7-1, if the 28 V data fall into the marked region, then the efficiency without recovery circuit starts falling while that with recovery is start rising only, giving the simulation results in Fig. 4-8. Similarly, if 16 V data fall into the marked domain described in the figure, then the trend in Fig. 4-9 is explainable. Such an investigation is important for designer to find an optimal solution for a given input voltage and most efficient output power.

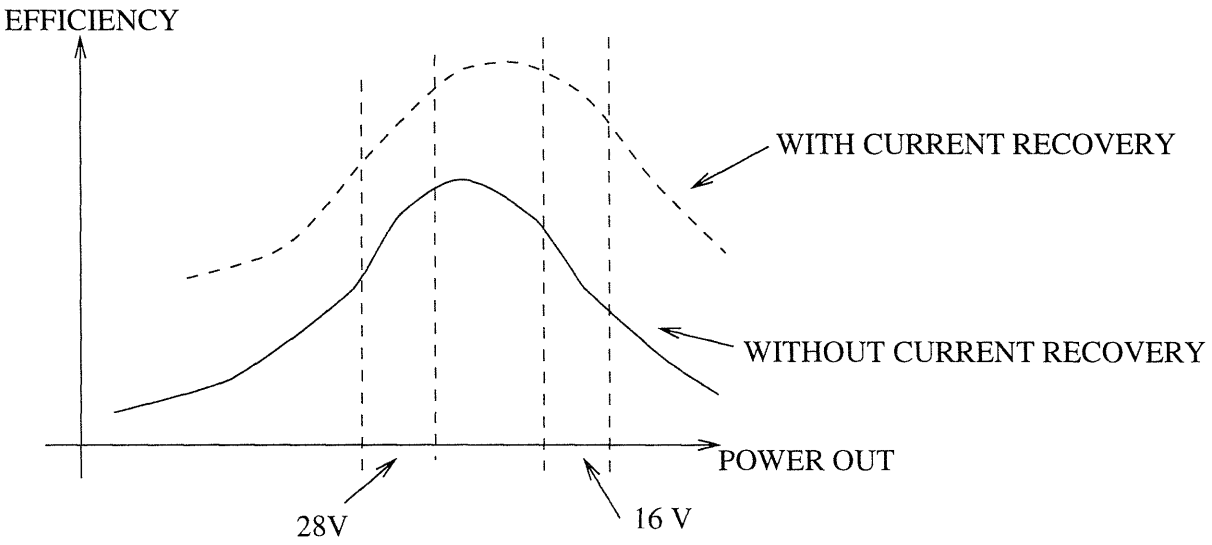

Figure 7-1: Suggested Efficiency Profile on different Power Out

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Appendix A

SPICE Program Listings

A.1 Schottkey Diode

```
Schotkky Rectifier

* forward voltage Vs. forward current
*Vin 1 0 DC 1
* forward and reverse recovery
*Vin 1 0 pulse (-10 10 600n 0 0 600n 1200n)

Rin 1 2 92.5m

D1 2 0 SSR8045CT                                                    10

.model SSR8045CT d
+ is=4e-6 n=1.02 eg=0.69 bv=45 ibv=30e-3 cja=2u  rs=3.7e-3
+ phi=0.25 exa=0.5 exp=0.325 cta=6e-4 ctp=6e-4 trs=2.15e-3
+ tlev=2 tlevc=1 xti=2.04

* forward voltage Vs. forward current
.dc sweep vin dec 1000 .1 10
.plot dc i(rin)

                                                                    20
* forward and reverse recovery
```

```
*.tran 1n 1800n 0 1n
*.plot tran i(d1)

.options post brief
.end
```

A.2 HEXFET IV

```
HEXFETiv IRF140

Vcc 1 0 dc 50
Vin 10 0 pulse (0 10 0 20n 20n 510n 4u)

l1 1 2 51n
r1 2 3 5
r2 10 11 56
ls 13 0 3n

Xm1 3 11 13 irf140

.subckt IRF140 1 5 10
m140 4 7 8 8 hexfet140 w=1.064 l=1.2u
.model hexfet140 nmos (level=3 theta=.12 uo=450 vto=3.47 cgso=730p)
d1 9 2 dsd
.model dsd d is=2.8e-12 rs=8e-3
ld 1 2 4.5n
r1 2 4 .0275
r2 8 9 .01
ls 9 10 2n
e1 4 3 4 7 4 .95
cx 3 7 poly 1200p 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 4.76e-20 0 -2.2e-21
rg 7 6 .5
lg 6 5 3n
cds 1 10 400p
.ends IRF140
```

.tran 1n 1u 0 1n

.OPTIONS POST brief

.plot tran v(11,13) V(3,13)

.plot tran i(xm1.ld)

.end

A.3 Flyback Transformer (w/o Energy Recovery Circuit)

Transformer Circuit

* Primary Side

*Vin=28v

*Vin+ 1 0 DC 28

*Pout=100w

*Vgdrva 6 0 pulse (10 0 577n 20n 20n 1383n 2u)

*Vgdrvb 11 0 pulse (0 10 980n 20n 20n 577n 2u)

* current recovery circuit add-on

*Vgdrvc 21 5 pulse (0 10 1837n 20n 20n 123n 2u)

*Vgdrvd 23 10 pulse (0 10 837n 20n 20n 123n 2u)

*Pout=75w

*Vgdrva 6 0 pulse (10 0 500n 20n 20n 1460n 2u)

*Vgdrvb 11 0 pulse (0 10 980n 20n 20n 500n 2u)

* current recovery circuit add-on

*Vgdrvc 21 5 pulse (0 10 1835n 20n 20n 125n 2u)

*Vgdrvd 23 10 pulse (0 10 835n 20n 20n 125n 2u)

*Pout=50w

*Vgdrva 6 0 pulse (10 0 415n 20n 20n 1545n 2u)

*Vgdrvb 11 0 pulse (0 10 980n 20n 20n 415n 2u)

* current recovery circuit add-on

*Vgdrvc 21 5 pulse (0 10 1856n 20n 20n 104n 2u)

*Vgdrvd 23 10 pulse (0 10 856n 20n 20n 104n 2u)

```
*Vin=16v
Vin+ 1 0 DC 16

*Pout=100w
*Vgdrva 6 0 pulse (10 0 840n 20n 20n 1120n 2u)
*Vgdrvb 11 0 pulse (0 10 980n 20n 20n 840n 2u)
** current recovery circuit add-on
*Vgdrvc 21 5 pulse (0 10 1750n 20n 20n 210n 2u)
*Vgdrvd 23 10 pulse (0 10 750n 20n 20n 210n 2u)
*Pout=75w
*Vgdrva 6 0 pulse (10 0 840n 20n 20n 1120n 2u)
*Vgdrvb 11 0 pulse (0 10 980n 20n 20n 840n 2u)
** current recovery circuit add-on
*Vgdrvc 21 5 pulse (0 10 1750n 20n 20n 210n 2u)
*Vgdrvd 23 10 pulse (0 10 750n 20n 20n 210n 2u)
*Pout=50w
Vgdrva 6 0 pulse (10 0 747n 20n 20n 1213n 2u)
Vgdrvb 11 0 pulse (0 10 980n 20n 20n 747n 2u)
** current recovery circuit add-on
Vgdrvc 21 5 pulse (0 10 1774n 20n 20n 186n 2u)
Vgdrvd 23 10 pulse (0 10 774n 20n 20n 186n 2u)

*Vin=50v Pout=100w,75w,50w
*Vin+ 1 0 DC 50
*Vgdrva 6 0 pulse (12 0 370n 20n 20n 1590n 2u)
*Vgdrvb 11 0 pulse (0 12 980n 20n 20n 370n 2u)
** current recovery circuit add-on
*Vgdrvc 21 5 pulse (0 10 1867n 20n 20n 93n 2u)
*Vgdrvd 23 10 pulse (0 10 867n 20n 20n 93n 2u)

d15 1 2 d1n4001
d14 2 3 d1n4001

*Vin=28v
*c13 1 0 1u ic=28
*c14 2 0 1u ic=28
```

```
*c15 3 0 1u ic=28
*c11 3 0 1u ic=28

*Vin=16v
c13 1 0 1u ic=16
c14 2 0 1u ic=16
c15 3 0 1u ic=16
c11 3 0 1u ic=16

*Vin=50v
*c13 1 0 1u ic=50
*c14 2 0 1u ic=50
*c15 3 0 1u ic=50
*c11 3 0 1u ic=50

* current recovery circuit add-on
clamp1 22 0 11n ic=0
clamp2 24 0 11n ic=0

* Vin=28v
*l3 1 52 500n ic=4.5
* Vin=16v
l3 1 52 500n ic=7.875
* Vin=50v
*l3 1 52 500n ic=2.52

rl3 52 2 8m

* Vin=28v
*l4 2 53 500n ic=4.5
* Vin=16v
l4 2 53 500n ic=7.875
* Vin=50v
*l4 2 53 500n ic=2.52

rl4 53 3 8m
```

```
r27 1 2 10                                                    100
r42 7 8 .011
r34 8 0 .011

Xs1 5 6 7 IRF140IV
Xs2 10 11 7 IRF140IV
* current recovery circuit add-on
Xs3 22 21 5 IRF140I
Xs4 24 23 10 IRF140I

* Vin=28v                                                     110
*L1p 3 101 99m ic=.5
* Vin=16v
*L1p 3 101 99m ic=.5
* Vin=50v
L1p 3 101 99m ic=.5

Rl1p 101 4 12m

* Vin=28v
*L1pu 3 4 1.2u ic=2                                          120
*L1pk 4 55 80n ic=2.5
* Vin=16v
L1pu 3 4 1.2u ic=3.5
L1pk 4 55 80n ic=4
* Vin=50v
*L1pu 3 4 1.2u ic=1
*L1pk 4 55 80n ic=1.5

Rl1pk 55 5 8m
Rl1pkp 4 55 100                                              130

L2p 3 102 99m ic=-10.5

Rl2p 102 9 12m
```

```
L2pu 3  9 1.2u ic=10.5
L2pk 9 510 80n ic=0

Rl2pk 510 10 8m
R12pkp 9 510 100

* Secondary Side

L1s 0 13 24.75m ic=21
L2s 0 15 24.75m ic=-1

d13 15 14 SSR8045CT
d12 13 14 SSR8045CT

c18 14 0 8.5u ic=5
c19 16 0 8.5u ic=5

l1 14 516 180n ic=20

rl1 516 16 3m

r26 14 16 0.25
* Pout=100w
*rload 16 0 .25
* Pout=75w
*rload 16 0 .3333
* Pout=50w
rload 16 0 .5

K1 L1p L2s 1
K2 L2p L1s 1

.subckt IRF140IV 1 5 10
m140 4 7 8 8 hexfet140 w=1.064 l=1.2u
d1 9 2 dsd
```

```
*ld 1 2 4.5n
ld 1 2 0
r1 2 4 .0275
r2 8 9 .01
*ls 9 10 2n
ls 9 10 0
e1 4 3 4 7 4 .95
cx 7 3 poly 600p 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2.38e-20 0 -1.1e-21
rg 7 6 .5
*lg 6 5 3n
lg 6 5 0
cds 1 10 400p
*daval 1 11 dideal
*vaval 11 0 dc 120
.ends IRF140IV

.subckt IRF140I 1 5 10
m140 4 7 8 8 hexfet140 w=.133 l=1.2u
d1 9 2 dsd
*ld 1 2 4.5n
ld 1 2 0
r1 2 4 .22
r2 8 9 .08
*ls 9 10 2n
ls 9 10 0
e1 4 3 4 7 4 .95
cx 7 3 poly 75p 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .2975e-20 0 -.1375e-21
rg 7 6 4
*lg 6 5 3n
lg 6 5 0
cds 1 10 50p
*daval 1 11 dideal
*vaval 11 0 dc 120
.ends IRF140I

.model d1n4001 d is=.1p rs=1.6e-2 bv=100 cjo=15p
```

```
.model hexfet140 nmos (level=3 theta=.12 uo=450 vto=3.47 cgso=730p)
.model dsd d is=2.8e-12 rs=8e-3
.model dideal d is=1p rs=1e-5
.model SSR8045CT d is=4e-6 n=1.02 eg=0.69 bv=45 ibv=30e-3 cja=15n rs=3.7e-3
+ phi=0.25 exa=0.5 exp=0.325 cta=6e-4 ctp=6e-4 trs=2.15e-3 tlev=2
+ tlevc=1 xti=2.04

.tran 1n 40u 0u 1n UIC
.plot tran i(l1p) i(l1pu) i(l1pk)
.plot tran i(l2p) i(l2pu) i(l2pk)
.plot tran par('i(d13)+i(d12)')
.plot tran i(rload)
.plot tran i(clamp1)
*.measure tran Pout avg par('v(16)*i(rload)') from=26u to=38u
*.measure tran Pin avg par('-1*(v(1)*i(vin+)+v(6)*i(vgdrva)+v(11)*i(vgdrvb))')
*+ from=26u to=38u
* current recovery circuit add-on
*.measure tran Pin avg par('-1*(v(1)*i(vin+)+v(6)*i(vgdrva)+v(11)*i(vgdrvb)+
*+ (v(21)-v(5))*i(vgdrvc)+(v(23)-v(10))*i(vgdrvd))') from=26u to=38u
.option post brief itl4=100 itl5=0
.end
```

A.4 Flyback Converter with Control (Simplified SPICE Modal)

Control Circuit

```
* Primary Side

Vin+ 1 0 DC 28
*Vstep 999 0 pwl(0 0 1.999999m 0 2m 3 2.9999999m 3 3m 0 3.9999999m 0 4m -3
*+ 4.9999999m -3 5m 0 )
*Istep 0 16 pwl(0 0 1.999999m 0 2m 10 2.9999999m 10 3m 0 3.9999999m 0 4m -10
*+ 4.9999999m -10 5m 0)
*Vgdrva 6 0 pulse (10 0 546n 20n 20n 1454n 2u)
```

```
*Vgdrvb 11 0 pulse (0 10 980n 20n 20n 546n 2u)
Egdrva 6 0 600 0 1
Egdrvb 11 0 601 0 1
* current recovery circuit add-on
*Vgdrvc 21 5 pulse (0 10 1837n 20n 20n 123n 2u)
*Vgdrvd 23 10 pulse (0 10 837n 20n 20n 123n 2u)

d15 1 2 d1n4001
d14 2 3 d1n4001

c13 1 0 1u ic=28
c14 2 0 1u ic=28
c15 3 0 1u ic=28
c11 3 0 1u ic=28
* current recovery circuit add-on
*clamp1 22 0 11n ic=0
*clamp2 24 0 11n ic=05

l3 1 52 500n ic=4.5
rl3 52 2 8m

l4 2 53 500n ic=4.5
rl4 53 3 8m

r27 1 2 10
r42 7 8 .011
r34 8 0 .011

Xs1 5 6 7 IRF140IV
Xs2 10 11 7 IRF140IV
* current recovery circuit add-on
*Xs3 22 21 5 IRF140I
*Xs4 24 23 10 IRF140I

L1p 3 101 99m ic=.5
Rl1p 101 5 12m
```

```
L1pu 3 5 1.2u ic=2
*L1pk 4 5 80n ic=2.5
*Rl1pk 55 5 8m
*Rl1pkp 4 5 100

L2p 3 102 99m ic=-10.5
Rl2p 102 10 12m
L2pu 3  10 1.2u ic=10.5
*L2pk 9 10 80n ic=0
*Rl2pk 510 10 8m
*R12pkp 9 10 100

* Secondary Side

L1s 0 13 24.75m ic=21

L2s 0 15 24.75m ic=-1

d13 15 14 SSR8045CT
d12 13 14 SSR8045CT

c18 14 0 8.5u ic=5
c19 16 0 8.5u ic=5

l1 14 516 180n ic=20
rl1 516 16 3m

r26 14 16 0.25
rload 16 0 .25

K1 L1p L2s 1
K2 L2p L1s 1

* Feeback Control

.param pi=3.141592654 g0=7 z0=4k p0=6k p1=300k p2=300k
```

```
vref 199 0 dc 5
evout 200 0 16 199 1
vcur 200 300 dc 0
rsp 300 201 1e-5
lsp 201 0 '1/(2*pi*z0)'
hsp0 202 0 vcur g0
rszsp1 202 203 1
cszsp1 202 203 '1/(2*pi*z0)'
rszsp2 203 204 1
cszsp2 203 204 '1/(2*pi*p0)'
eszsp1 0 204 opamp 0 203
rsp1 204 205 1
rsp2 205 206 1
csp1 205 206 '1/(2*pi*p1)'
esp1 0 206 opamp 0 205
rsp3 206 207 1
rsp4 207 208 1
csp2 207 208 '1/(2*pi*p2)'
esp2 0 208 opamp 0 207

vsw1 400 0 pulse(10 0 999n 1n 1n 999n 2u)
vsw2 401 0 pulse(0 10 999n 1n 1n 999n 2u)
vper1 500 0 pwl 0 1.136 2u 43.19 R
vper 501 0 pwl 0 1.136 2u 43.19 R td=1u
*eIsense 700 0 vol='v(7)/.022'
eduty1 600 400 pwl(1) 208 500 -1p '-v(400)' 1p 0
eduty2 601 401 pwl(1) 208 501 -1p '-v(401)' 1p 0

.subckt IRF140IV 1 4 10
m140 1 4 10 10 hexfet140 w=1.064 l=1.2u
.ends IRF140IV

*.subckt IRF140IV 1 5 10
*m140 4 7 8 8 hexfet140 w=1.064 l=1.2u
*d1 9 2 dsd
**ld 1 2 4.5n
```

```
*ld 1 2 0
*r1 2 4 .0275
*r2 8 9 .01
**ls 9 10 2n
*ls 9 10 0
*e1 4 3 4 7 4 .95
*cx 7 3 poly 600p 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2.38e-20 0 -1.1e-21
*rg 7 6 .5
**lg 6 5 3n
*lg 6 5 0
*cds 1 10 400p
*daval 1 11 dideal
*vaval 11 0 dc 120
*.ends IRF140IV

.subckt IRF140I 1 5 10
m140 1 5 10 10 hexfet140 w=.133 l=1.2u
.ends IRF140I

*.subckt IRF140I 1 5 10
*m140 4 7 8 8 hexfet140 w=.133 l=1.2u
*d1 9 2 dsd
**ld 1 2 4.5n
*ld 1 2 0
*r1 2 4 .22
*r2 8 9 .08
**ls 9 10 2n
*ls 9 10 0
*e1 4 3 4 7 4 .95
*cx 7 3 poly 75p 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .2975e-20 0 -.1375e-21
*rg 7 6 4
**lg 6 5 3n
*lg 6 5 0
*cds 1 10 50p
*daval 1 11 dideal
*vaval 11 0 dc 120
```

```
*.ends IRF140I

.model d1n4001 d is=.1p rs=1.6e-2 bv=100 cjo=15p
.model hexfet140 nmos
*.model hexfet140 nmos (level=3 theta=.12 uo=450 vto=3.47 cgso=730p)
.model dsd d is=2.8e-12 rs=8e-3                                          160
.model dideal d is=1p rs=1e-5
.model dideal1 d is=1e-5 rs=1e-5
.model dideal2 d is=.1p rs=6
.model SSR8045CT d is=4e-6 n=1.02 eg=0.69 bv=45 ibv=30e-3 cja=15n rs=3.7e-3
+ phi=0.25 exa=0.5 exp=0.325 cta=6e-4 ctp=6e-4 trs=2.15e-3 tlev=2
+ tlevc=1 xti=2.04

.tran 10n 2m 0 10n UIC
*.ic i(xs2.cds)=53
*.plot tran i(l1p) i(l1pu)                                               170
*.plot tran i(l2p) i(l2pu)
*.plot tran par('i(d13)+i(d12)')
*.plot tran i(rload)
.option post brief itl4=100 itl5=0
.end
```

A.5 Flyback Converter with Control (Averaged Model)

Control Circuit

```
* Primary Side

Vin+ 1 999 DC 28
Vstep 999 0 pwl(0 0 1.999999m 0 2m 3 2.9999999m 3 3m 0 3.9999999m 0 4m -3
+ 4.9999999m -3 5m 0 )
*Istep 0 16 pwl(0 0 1.999999m 0 2m 10 2.9999999m 10 3m 0 3.9999999m 0 4m -10
*+ 4.9999999m -10 5m 0)
 Egdrva 6 0 208 0 1                                                      10
```

```
Egdrvb 11 0 208 0 1
*Vgdrvb 11 0 dc 0.286
* current recovery circuit add-on
*Vgdrvc 21 5 pulse (0 10 1837n 20n 20n 123n 2u)
*Vgdrvd 23 10 pulse (0 10 837n 20n 20n 123n 2u)

d15 1 2 d1n4001
d14 2 3 d1n4001

c13 1 0 1u ic=28
c14 2 0 1u ic=28
c15 3 0 1u ic=28
c11 3 0 1u ic=28
* current recovery circuit add-on
*clamp1 22 0 11n ic=0
*clamp2 24 0 11n ic=05

l3 1 52 500n ic=4.5
rl3 52 2 8m

l4 2 53 500n ic=4.5
rl4 53 3 8m

r27 1 2 10
r42 7 8 .011
r34 8 0 .011

x1 3 7 901 0 6 pwmbck
lp1 901 902 1.2u
x2 902 0 15 0 6 pwmbst

x3 7 3 904 0 11 pwmbck
lp2 904 905 1.2u
x4 905 0 0 13 11 pwmbst

d13 15 14 SSR8045CT
```

```
d12 13 14 SSR8045CT

c18 14 0 8.5u ic=5
c19 16 0 8.5u ic=5

l1 14 516 180n ic=20
rl1 516 16 3m

r26 14 16 0.25
rload 16 0 .25

* Feeback Control

.param pi=3.141592654 g0=.1 z0=4k p0=6k p1=300k p2=300k
vref 199 0 dc 5
evout 200 0 16 199 1
vcur 200 300 dc 0
rsp 300 201 1e-5
lsp 201 0 '1/(2*pi*z0)'
hsp0 202 0 vcur g0
rszsp1 202 203 1
cszsp1 202 203 '1/(2*pi*z0)'
rszsp2 203 204 1
cszsp2 203 204 '1/(2*pi*p0)'
eszsp1 0 204 opamp 0 203
rsp1 204 205 1
rsp2 205 206 1
csp1 205 206 '1/(2*pi*p1)'
esp1 0 206 opamp 0 205
rsp3 206 207 1
rsp4 207 208 1
csp2 207 208 '1/(2*pi*p2)'
esp2 0 208 opamp 0 207

.subckt pwmbck 1 2 3 4 5
* buck step down transformer model
```

```
* nodes 1 & 2 are the input; 3 & 4 are the output; 5 is the duty cycle
* N=1 is the transformer turns ratio
* 1:D*N is the effective turns ratio
rd 5 0 1x
ro 6 3 .01
* Ro is the output resistance
g1 1 2 poly(2) 6 3 5 0 0 0 0 0 100
* G1 gain = N/R0
e2 6 4 poly(2) 1 2 5 0 0 0 0 0 1
*E2 gain = N, the transformer ratio
.ends pwmbck

.subckt pwmbst 1 2 3 4 5
* boost step-up transformer model
* nodes 1 & 2 are the input; 3 & 4 are the output; 5 is the duty cycle
* N=0.5 is the transformer turns ratio
* (1-D):N is the effective turns ratio
rd 5 0 1x
ri 1 6 .01
* Ri is the input resistance
ro 3 4 100x
g2 4 3 poly(2) 1 6 8 0 0 0 0 0 200
* G2=1/(RI*N)
e1 6 2 poly(2) 3 4 8 0 0 0 0 0 2
* E1=1/N
rd1 8 0 1x
vd1 8 7 dc 1
ed1 7 0 5 0 -1
.ends pwmbst

.model d1n4001 d is=.1p rs=1.6e-2 bv=100 cjo=15p
.model hexfet140 nmos (level=3 theta=.12 uo=450 vto=3.47 cgso=730p)
.model dsd d is=2.8e-12 rs=8e-3
.model dideal d is=1p rs=1e-5
.model dideal1 d is=1e-5 rs=1e-5
.model dideal2 d is=.1p rs=6
```

```
.model SSR8045CT d is=4e-6 n=1.02 eg=0.69 bv=45 ibv=30e-3 cja=15n rs=3.7e-3
+ phi=0.25 exa=0.5 exp=0.325 cta=6e-4 ctp=6e-4 trs=2.15e-3 tlev=2
+ tlevc=1 xti=2.04

.tran 100n 6m 0 100n UIC
*.ic i(xs2.cds)=53
.plot tran i(l1p) i(l1pu) i(l1pk)
.plot tran i(l2p) i(l2pu) i(l2pk)
.plot tran par('i(d13)+i(d12)')
.plot tran i(rload)
*.plot tran i(clamp1)
*.plot tran v(208)
*.measure tran Pout avg par('v(16)*i(rload)') from=26u to=38u
*.measure tran Pin avg par('-1*(v(1)*i(vin+)+v(6)*i(vgdrva)+v(11)*i(vgdrvb))')
*+ from=26u to=38u
* current recovery circuit add-on
*.measure tran Pin avg par('-1*(v(1)*i(vin+)+v(6)*i(vgdrva)+v(11)*i(vgdrvb)+
*+ (v(21)-v(5))*i(vgdrvc)+(v(23)-v(10))*i(vgdrvd))') from=26u to=38u
.option post brief itl4=100 itl5=0
.end
```

A.6 Z_{in}, Z_{out} from Flyback Converter with Control (Averaged Model)

```
Zin & Zout Circuit

* Primary Side

* Zin with 100W Load
Vin+ 1 0 dc 28 ac 1
HIvin+ 9999 0 ccvs vin+ -1
* Zout
*Vin+ 1 0 dc 28

Egdrva 6 0 208 0 1
```

```
Egdrvb 11 0 208 0 1

d15 1 2 d1n4001
d14 2 3 d1n4001

c13 1 0 1u ic=28
c14 2 0 1u ic=28
c15 3 0 1u ic=28
c11 3 0 1u ic=28

l3 1 52 500n ic=4.5
rl3 52 2 8m

l4 2 53 500n ic=4.5
rl4 53 3 8m

r27 1 2 10
r42 7 8 .011
r34 8 0 .011

x1 3 7 901 0 6 pwmbck
lp1 901 902 1.2u
x2 902 0 15 0 6 pwmbst

x3 7 3 904 0 11 pwmbck
lp2 904 905 1.2u
x4 905 0 0 13 11 pwmbst

d13 15 14 SSR8045CT
d12 13 14 SSR8045CT

c18 14 0 8.5u ic=5
c19 16 0 8.5u ic=5

l1 14 516 180n ic=20
rl1 516 16 3m
```

```
r26 14 16 0.25
                                                                    50
* Zin with 100W Load
rload 16 0 .25
* Zout
*Iout 0 16 dc 20 ac 1

* Feeback Control

.param pi=3.141592654 g0=.1 z0=4k p0=6k p1=300k p2=300k
vref 199 0 dc 5
evout 200 0 16 199 1                                                60
vcur 200 300 dc 0
rsp 300 201 1e-5
lsp 201 0 '1/(2*pi*z0)'
hsp0 202 0 vcur g0
rszsp1 202 203 1
cszsp1 202 203 '1/(2*pi*z0)'
rszsp2 203 204 1
cszsp2 203 204 '1/(2*pi*p0)'
eszsp1 0 204 opamp 0 203
rsp1 204 205 1                                                      70
rsp2 205 206 1
csp1 205 206 '1/(2*pi*p1)'
esp1 0 206 opamp 0 205
rsp3 206 207 1
rsp4 207 208 1
csp2 207 208 '1/(2*pi*p2)'
esp2 0 208 opamp 0 207

.subckt pwmbck 1 2 3 4 5
* buck step down transformer model                                  80
* nodes 1 & 2 are the input; 3 & 4 are the output; 5 is the duty cycle
* N=1 is the transformer turns ratio
* 1:D*N is the effective turns ratio
```

```
rd 5 0 1x
ro 6 3 .01
* Ro is the output resistance
g1 1 2 poly(2) 6 3 5 0 0 0 0 0 100
* G1 gain = N/R0
e2 6 4 poly(2) 1 2 5 0 0 0 0 0 1
*E2 gain = N, the transformer ratio                                    90
.ends pwmbck

.subckt pwmbst 1 2 3 4 5
* boost step-up transformer model
* nodes 1 & 2 are the input; 3 & 4 are the output; 5 is the duty cycle
* N=0.5 is the transformer turns ratio
* (1-D):N is the effective turns ratio
rd 5 0 1x
ri 1 6 .01
* Ri is the input resistance                                           100
ro 3 4 100x
g2 4 3 poly(2) 1 6 8 0 0 0 0 0 200
* G2=1/(RI*N)
e1 6 2 poly(2) 3 4 8 0 0 0 0 0 2
* E1=1/N
rd1 8 0 1x
vd1 8 7 dc 1
ed1 7 0 5 0 -1
.ends pwmbst
                                                                       110

.model d1n4001 d is=.1p rs=1.6e-2 bv=100 cjo=15p
.model hexfet140 nmos (level=3 theta=.12 uo=450 vto=3.47 cgso=730p)
.model dsd d is=2.8e-12 rs=8e-3
.model dideal d is=1p rs=1e-5
.model dideal1 d is=1e-5 rs=1e-5
.model dideal2 d is=.1p rs=6
.model SSR8045CT d is=4e-6 n=1.02 eg=0.69 bv=45 ibv=30e-3 cja=15n rs=3.7e-3
+ phi=0.25 exa=0.5 exp=0.325 cta=6e-4 ctp=6e-4 trs=2.15e-3 tlev=2
+ tlevc=1 xti=2.04
```

```
.ac dec 200 1 1x

* Zin with 100W load
.print ac par('vdb(1)-vdb(9999)') par('vp(1)-vp(9999)')
* Zout
*.print ac vdb(16) vp(16)

.option post brief itl4=100 itl5=0
.end
```

A.7 Two Port Model

Two Port Circuit

```
.param IN_V=28, OUT_V=5, IN_I=4.5, OUT_I=20, R_IN=1

*external source with resistance
Vin 99 0 dc 'IN_V+R_IN*IN_I' ac 1 sin('IN_V+R_IN*IN_I', '0.05*IN_V', 25)
R1 99 1 R_IN

Iin_nom 1 0 dc IN_I
Vin_nom 2 0 dc IN_V
Vout_nom 3 0 dc OUT_V

* external load with resistance, inductance
Rl 4 5  .25
Ll 5 6 800m
Vdummy 6 0 dc 0 ac 1

* Zin
Hin 10 0 ccvs Vin -1
VIin_nom 11 0 dc IN_I

* Sample Zin taken from simulation of ZINZOUT.CIR
EZin 1 2 freq 10 11
```

+	1.00000	16.7018	−179.9788
+	1.25893	16.7018	−179.9734
+	1.58489	16.7018	−179.9665
+	1.99526	16.7018	−179.9578
+	2.51189	16.7018	−179.9469
+	3.16228	16.7018	−179.9331
+	3.98107	16.7018	−179.9158
+	5.01187	16.7018	−179.8940
+	6.30957	16.7018	−179.8665
+	7.94328	16.7018	−179.8319
+	10.00000	16.7018	−179.7884
+	12.58925	16.7017	−179.7336
+	15.84893	16.7017	−179.6646
+	19.95262	16.7017	−179.5778
+	25.11886	16.7016	−179.4685
+	31.62278	16.7015	−179.3309
+	39.81072	16.7013	−179.1576
+	50.11872	16.7010	−178.9396
+	63.09573	16.7005	−178.6651
+	79.43282	16.6997	−178.3195
+	100.00000	16.6985	−177.8847
+	125.89254	16.6965	−177.3376
+	158.48932	16.6934	−176.6494
+	199.52623	16.6886	−175.7841
+	251.18864	16.6808	−174.6970
+	316.22777	16.6686	−173.3329
+	398.10717	16.6494	−171.6244
+	501.18723	16.6190	−169.4909
+	630.95734	16.5714	−166.8390
+	794.32823	16.4972	−163.5662
+	1.00000k	16.3824	−159.5708
+	1.25893k	16.2071	−154.7722
+	1.58489k	15.9444	−149.1427
+	1.99526k	15.5607	−142.7495
+	2.51189k	15.0190	−135.7877
+	3.16228k	14.2852	−128.5746

```
+  3.98107k     13.3367    −121.4827
+  5.01187k     12.1699    −114.8335
+  6.30957k     10.8013    −108.8139
+  7.94328k      9.2628    −103.4615
+ 10.00000k      7.5922     −98.7071
+ 12.58925k      5.8231     −94.4281
+ 15.84893k      3.9770     −90.4776
+ 19.95262k      2.0551     −86.6599
+ 25.11886k     33.3045m    −82.6051
+ 31.62278k     −2.1262     −77.4102
+ 39.81072k     −4.3413     −68.7740
+ 50.11872k     −5.6183     −54.0918
+ 63.09573k     −4.7545     −51.7676
+ 79.43282k     −7.4093     −67.6884
+ 100.00000k    −15.5118    −64.6909
+ 125.89254k    −15.7601     65.5917
+ 158.48932k     −1.7242     77.7702
+ 199.52623k     15.1959    −60.3973
+ 251.18864k     −1.4242    −88.4740
+ 316.22777k    −11.0619    −84.0042
+ 398.10717k   −154.2660m    −63.8778
+ 501.18723k     −7.2703    −85.3216
+ 630.95734k    −10.5802    −87.6231
+ 794.32823k    −13.1724    −88.4706
+   1.00000x     −15.4905    −88.9168
```

```
* Zout
Hout 20 0 ccvs Vout_nom 1

* Sample Zout taken from simulation of ZINZOUT.CIR
Ezout 4 3 freq 20 0
+   1.00000    −106.0182     87.7135
+   1.25893    −104.0208     88.1853
+   1.58489    −102.0224     88.5608
+   1.99526    −100.0234     88.8598
+   2.51189     −98.0241     89.0981
```

+ 3.16228	−96.0245	89.2884
+ 3.98107	−94.0247	89.4408
+ 5.01187	−92.0249	89.5635
+ 6.30957	−90.0250	89.6629
+ 7.94328	−88.0251	89.7443
+ 10.00000	−86.0251	89.8122
+ 12.58925	−84.0251	89.8700
+ 15.84893	−82.0252	89.9209
+ 19.95262	−80.0252	89.9676
+ 25.11886	−78.0252	90.0126
+ 31.62278	−76.0252	90.0583
+ 39.81072	−74.0252	90.1070
+ 50.11872	−72.0253	90.1615
+ 63.09573	−70.0253	90.2246
+ 79.43282	−68.0254	90.2997
+ 100.00000	−66.0255	90.3907
+ 125.89254	−64.0257	90.5026
+ 158.48932	−62.0260	90.6415
+ 199.52623	−60.0265	90.8147
+ 251.18864	−58.0272	91.0319
+ 316.22777	−56.0284	91.3051
+ 398.10717	−54.0302	91.6498
+ 501.18723	−52.0329	92.0866
+ 630.95734	−50.0371	92.6424
+ 794.32823	−48.0431	93.3545
+ 1.00000k	−46.0513	94.2742
+ 1.25893k	−44.0613	95.4749
+ 1.58489k	−42.0704	97.0599
+ 1.99526k	−40.0702	99.1699
+ 2.51189k	−38.0420	101.9794
+ 3.16228k	−35.9497	105.6655
+ 3.98107k	−33.7367	110.3397
+ 5.01187k	−31.3306	115.9628
+ 6.30957k	−28.6598	122.3152
+ 7.94328k	−25.6704	129.0964
+ 10.00000k	−22.3297	136.1797

```
+ 12.58925k   −18.6104    144.0385
+ 15.84893k   −14.4813    154.5871
+19.95262k    −10.1106    173.1494
+25.11886k    −7.1998    −152.6250
+ 31.62278k    −8.3875    −118.3243
+ 39.81072k   −11.2986    −101.0761
+ 50.11872k   −14.2032     −93.3550
+ 63.09573k   −17.0421     −88.9442
+ 79.43282k   −20.0239     −84.1397
+100.00000k    −23.2382     −73.6079
+125.89254k    −25.0973     −48.6497
+158.48932k    −22.4771     −32.1906
+199.52623k    −20.2320     −48.1169
+251.18864k    −22.8295     −61.3746
+316.22777k    −24.1252     −70.3972
+398.10717k    −26.2016     −76.3238
+501.18723k    −28.3002     −80.0588
+630.95734k    −30.3848     −82.5294
+794.32823k    −32.4438     −84.2687
+ 1.00000x    −34.4827     −85.5459
```

```
.ac dec 200 1 1x
.print ac par('vdb(1)-vdb(10)') par('vp(1)-vp(10)')
.print ac par('vdb(4)-vdb(20)') par('vp(4)-vp(20)')
.tran 100u 120m
.option post brief
.end
```