Enhancing SPICE Model Parameters to Accurately Design and Simulate Circuits with Temperature Dependence, with a Special Emphasis on Bandgap References

by

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Submitted to the
Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements
for the degree of

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ABSTRACT

This study provides a detailed look at the design methodology for bandgap voltage references. The study describes a methodology by which the designer can accurately design and simulate a bandgap reference such that the measured results match the simulated results. This methodology requires an understanding of the individual building blocks with which the bandgap reference is composed. As such, SPICE models for MOS and Bipolar transistors are examined. SPICE parameter extraction was achieved using available graphical and non graphical techniques from the literature. The bandgap circuit is broken down into an ideal representation for examination. This allows the bandgap output voltage, which is the sum of a base-emitter voltage and a voltage that is proportional to absolute temperature, to be broken into its separate parts for analysis. Second order effects are taken into account to complete the modeling of the bandgap reference.

The information obtained from the examination of the transistor models and bandgap circuit design is used to formulate a new design procedure. This procedure requires accurate models for the fundamental components namely MOS and Bipolar transistors as well as resistors. Finally, a redesign of the bandgap reference is shown that will yield an output voltage which has a more stable value with varying process conditions and temperature.

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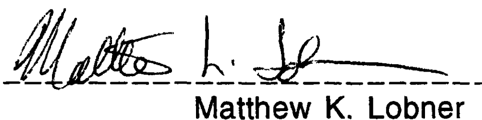

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1.0 BACKGROUND

1.1 Statement of Problem

The design of bandgap references has been a well established area of knowledge for the past fifteen years. Every design attempts to meet some specification pertaining to drift of output voltage over temperature. The bandgap circuits of today are being designed to meet specifications around thirty parts per million. Essentially what this amounts to is a variation of less than three millivolts over a temperature range of one hundred degrees. The design itself, which will be discussed later, involves matching a bipolar base emitter junction voltage's negative temperature coefficient with a PTAT (Proportional to Absolute Temperature) positive temperature coefficient. Ultimately, success is achieved when the fabricated version of the bandgap produces a steady output voltage over the temperature range of design. Unfortunately, most designers expect either two iterations in fabrication or costly laser trimming to achieve success with the bandgap circuitry. The designer's goal is to accurately predict the final output from the foundry. This will require matching a bandgap simulation with the measured response utilizing models generated from the bare components of the bandgap: MOSFETS, BJTS, and polysilicon resistors. The goal of this thesis is to provide a methodology to accomplish this task. The methodology begins with SPICE parameter extraction. An explanation of individual parameter variations is presented. Finally, this information is incorporated in the redesign of the bandgap.

The fundamental difficulty lies in the fact that the models used in simulation programs do not accurately represent a foundry's process [1] [2]. An important point to remember is that slight variations in key parameters will cause serious problems in circuit performance. It is not enough to simply run a simulation with generic models in order to check functionality. With the increased need for higher performance circuits (whether it be a bandgap reference, an operational amplifier, an A/D converter, or any other

type of analog IC circuit), the default model parameters of SPICE should simply provide a guideline for the design [3]. An extracted model from the process with its variation across temperature should be used in simulation. For most CMOS processes, the parasitic bipolar transistors needed to generate a base emitter junction are often not characterized by the foundry. In addition, characterization of the resistors used in the process are often limited to the sheet resistance value and matching.

Looking at a plot of the measured bandgap results and the simulated results (before fabrication), one sees the inaccuracies that occur when the proper models are not used. (SEE FIGURE 1.1)

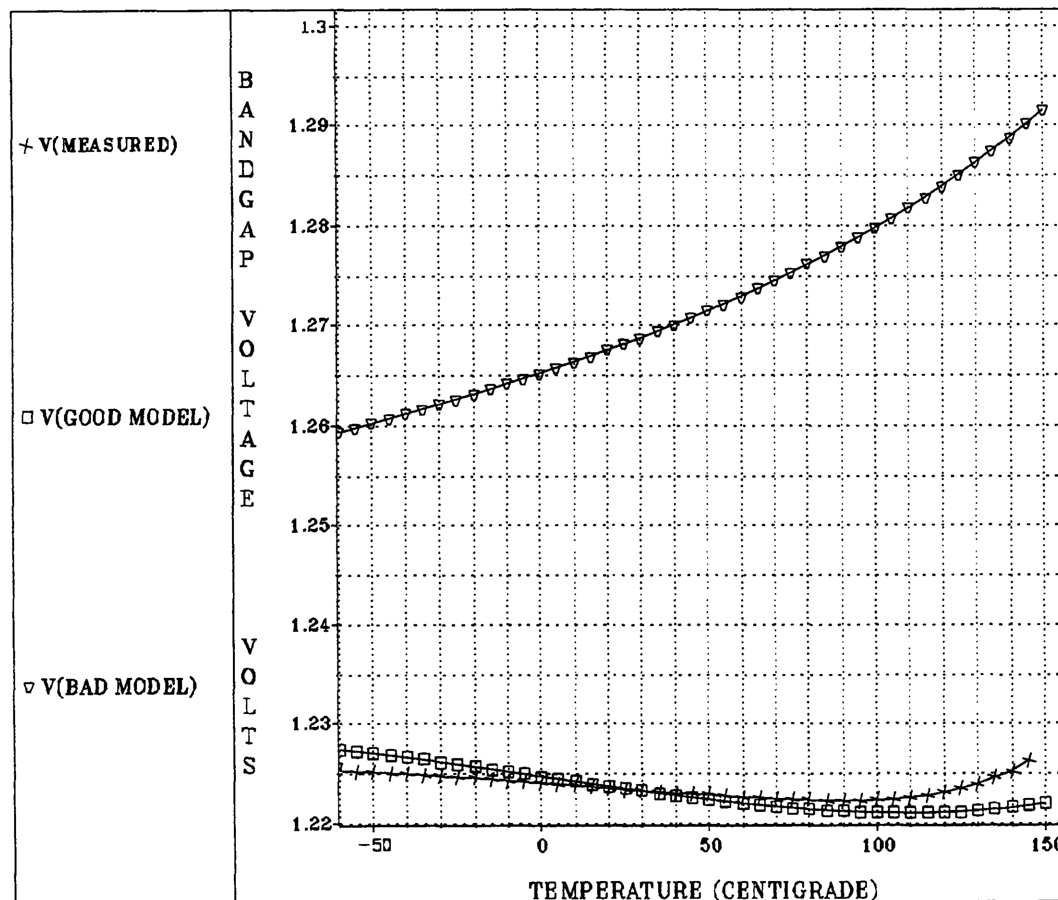

FIGURE 1.1 Bandgap Model Comparison

A methodology needs to be established so that designers obtain accurate models *before* beginning simulation of a circuit.

A benchmark of tests dependent on the application is necessary so that emphasis be placed on the useful parameters in that specific application [4]. A "complete" model is not necessary; only the design space used in the application needs to be modeled. A look at a plot of a simulation using parameters sent from ORBIT and the actual measured data for a single transistor shows a large discrepancy. (SEE FIGURE 1.2).

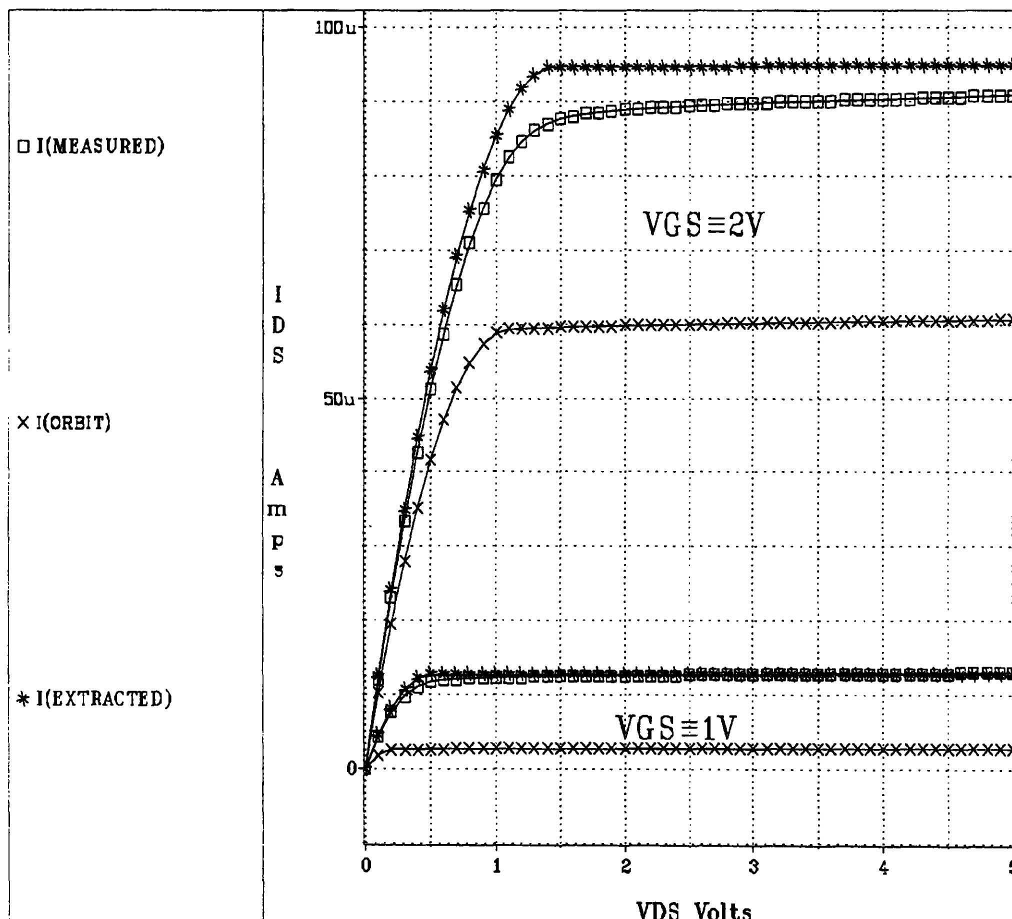

FIGURE 1.2 Transistor Model Comparison

Obviously, if the models do not accurately represent one single transistor, it is impossible to imagine the models accurately representing a complex, analog circuit.

Looking at a plot where the output of the bandgap is simulated with and without second order resistor temperature coefficients, one sees that this single parameter yields a completely different result. (SEE FIGURE 1.3)

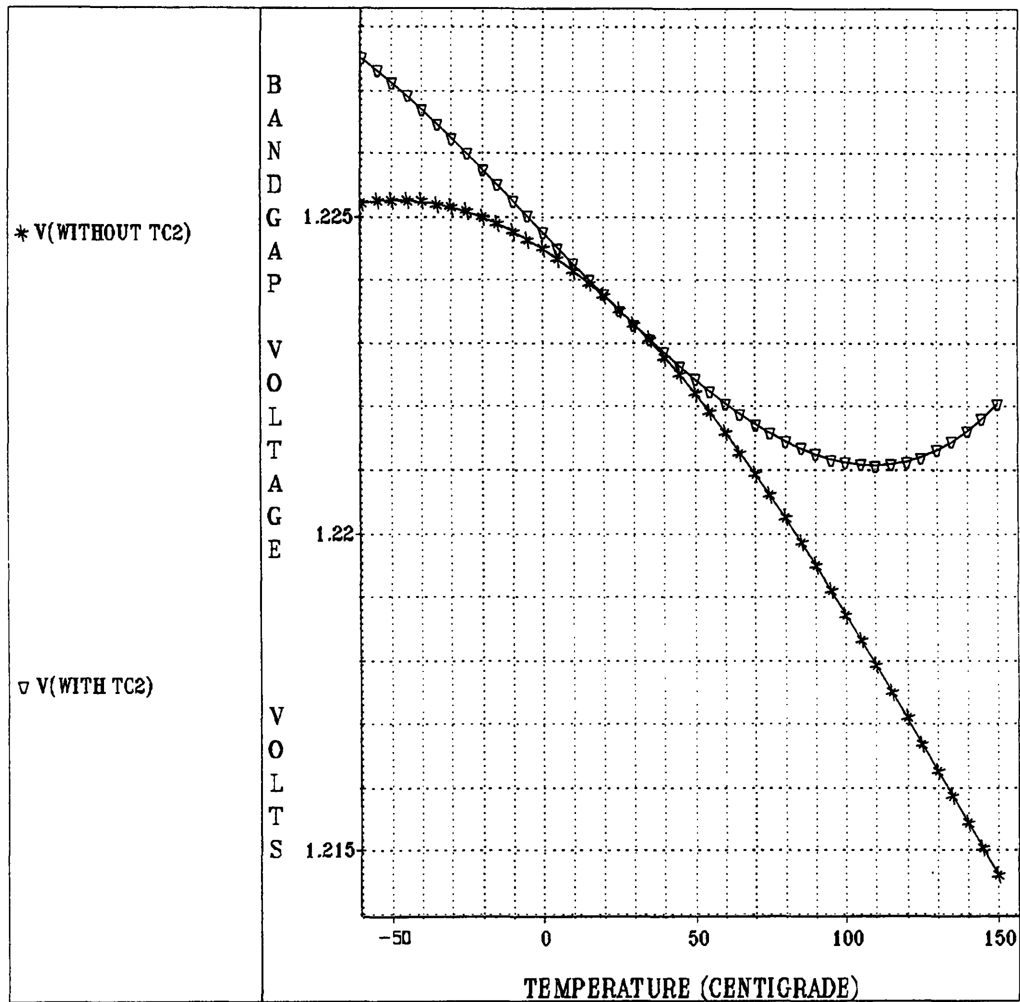

FIGURE 1.3 Bandgap with Missing Parameter

If all parameters are not specified for a given model, SPICE will use default parameters as an inadequate substitute.

A design process which can overcome these difficulties and provide the designer a useful approach to bandgap design is the goal of this thesis. This thesis specifies the development of a methodology to accurately design and simulate the bandgap reference. What follows from this goal is the ability to match a simulated response with a fabricated (measured) response. To achieve this goal, an examination of two areas is required:

(1) SPICE models and parameter extraction
(2) Theoretical and Realistic Bandgap Design

1.2 SPICE and Device Models

The extraction of SPICE parameters presents a problem if the designer does not have ample software support. There are three basic levels of extraction:

(1) Graphical - measurement -- This approach utilizes the available literature to obtain tests which will isolate various parameters which the designer is interested in obtaining. The results yielded by this approach are a good starting point for a model. However, the number of individual tests required can be prohibitive to obtaining a good model.

(2) A limited software approach -- This was the method that was used for this project. It requires a rough guess of the parameters to input into an optimizer. One such tool is the SANCAD Model Station II. Using this tool, the designer is capable of inputting parameter guesses along with various sets of measured data. (i.e. forward curves, reverse curves, gummel plots, etc.) The program then optimizes the input parameters to fit the input data.

(3) Full software approach -- This method utilizes a program like HP IC-CAP which will extract a complete model for a costly $40K-$60K. This cost does not include any of the electronic measuring tools which are needed to extract the models.

A more complete description of the parameter extraction done for this thesis will be presented later. However, the process for all devices was essentially the same. Using a double ring of bond pads to allow for access to more pins, test structures were laid out on the periphery of the test chip. These structures included a variety of NMOS and PMOS devices, various sizes of parasitic BJT devices, and two values of polysilicon resistors. Measurements were made using these devices in various configurations in order to obtain data useful for parameter extraction. This data was then used to formulate rough guesses for the parameters needed to simulate the

bandgap circuit. If certain parameters could not be measured, the values sent by ORBIT, the foundry where the chip was manufactured, were used. Once a complete model was obtained, this model was input to a program called Model Station II written by Sancad. The program uses measured data and the input model to create a more accurate model for simulation purposes.

This procedure was carried out in 10 degree (MOS) or 20 degree (BJT) steps over the range of -40 C to 80 C using a Temptronic Thermostream TP0412A. The temperature on the chip was regulated with the Thermostream. Using a temperature sensor placed underneath the body of the IC package (between the packaged part and the socket used to hold it in place), the Thermostream was able keep the temperature of the die at an accurate and stable level by blowing air onto the top of the packaged part. Measurements were made placing a Fluke 2190A Digital Thermometer at the same location as the temperature sensor to check the accuracy of the Thermostream. The results are shown in Table 1.1.

DESIRED TEMP	BLOW TEMP	RECORDED TEMP
-40	-46	-39.5
-20	-22	-18.7
0	0	0.7
20	17	21.3
40	41	41.6
60	61	61.2
80	80	81.1

TABLE 1.1 Errors in Temperature Measurements

1.3 Bandgap Design and Analysis

The first examination of the temperature dependence of the base emitter junction was presented in 1967 by Robert Widlar [5]. Both the base emitter voltage and the difference between two base emitter voltages from transistors of different sizes were examined.

In 1974, Paul Brokaw presented a completely bipolar bandgap reference which after laser trimming yielded temperature coefficients ranging from 5 to 60 ppm (parts per million)[6]. In 1978, Robert Blauschild and others presented an NMOS reference that obtained a stable reference using the difference between the enhancement and depletion threshold voltages [7]. The output voltage had a temperature coefficient of 6 ppm. In 1983, Gray and Song presented a CMOS bandgap reference which implemented switched capacitor technology for resistors and a parasitic p-n-p transistor[8]. This circuit achieved 13.1 ppm and 25.6 ppm temperature drift over the commercial and military ranges, respectively. These designs provide a framework for the state-of-the-art in temperature drift in bandgap references.

The bandgap circuit used on the test chip uses the superposition of a voltage developed across a polysilicon resistor and the voltage across the base-emitter junction of a parasitic vertical bipolar device. The parasitic bipolar device uses the substrate, the n-well, and a p+ diffusion to create the emitter, base, and collector, respectively. The original circuit was designed using Rockwell foundry HSPICE models. New models were obtained for the ORBIT process, and the circuit was adapted to these new models. Unfortunately, the process of adaptation was more trial and error than true redesign. The value of the polysilicon resistor was adjusted to yield the smallest temperature coefficient at the output. As FIGURE 1.1 shows, this circuit achieved 26 ppm over the range from -60 to 150 degrees C.

FIGURE 1.4 shows the bandgap circuit that was used for simulation. FIGURE 1.5 shows the layout of the fabricated circuit. The bandgap circuit analysis begins with an assumption that the loop consisting of M01, M02, Q1, Q2, and R1 generates a PTAT current. This current is then mirrored to the output branch through M09 and M10. Note that the current source is PTAT. The bandgap voltage is then the superposition of the base-emitter voltage of Q12 and the voltage across RBG. There exists a voltage (and a resistance value) that will minimize the temperature coefficient over the region of interest.

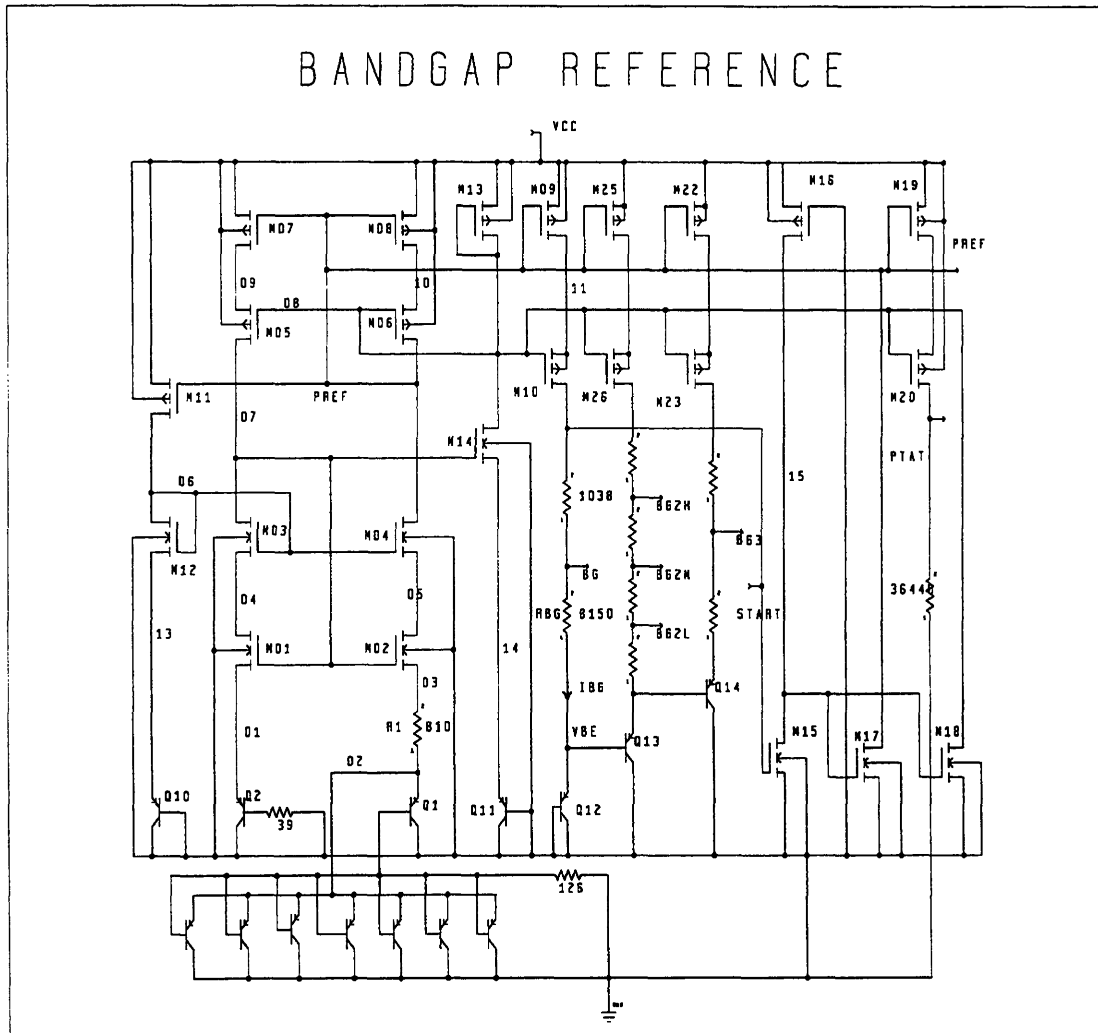

FIGURE 1.4 Bandgap Circuit

A word needs to be said about the start up of the circuit. The bandgap is stable in two states: when it is completely off and when the loop generating the PTAT current is satisfied. A look at the circuit shows that there is no outside starting source. The initial "kick start" is provided by transistors M15-M19. It is clear that M16 will always be on sourcing current. Initially, the gate of M15 will be low and the gates of M17 and M18 will rapidly charge up to a voltage where current can flow. This current is pulled from the branches where the PTAT current is generated and provides a quick push to force that circuit into its stable operating state. Once on, the voltage on the gate of M15 is high and the current provided by M16 is simply shunted to ground through M15.

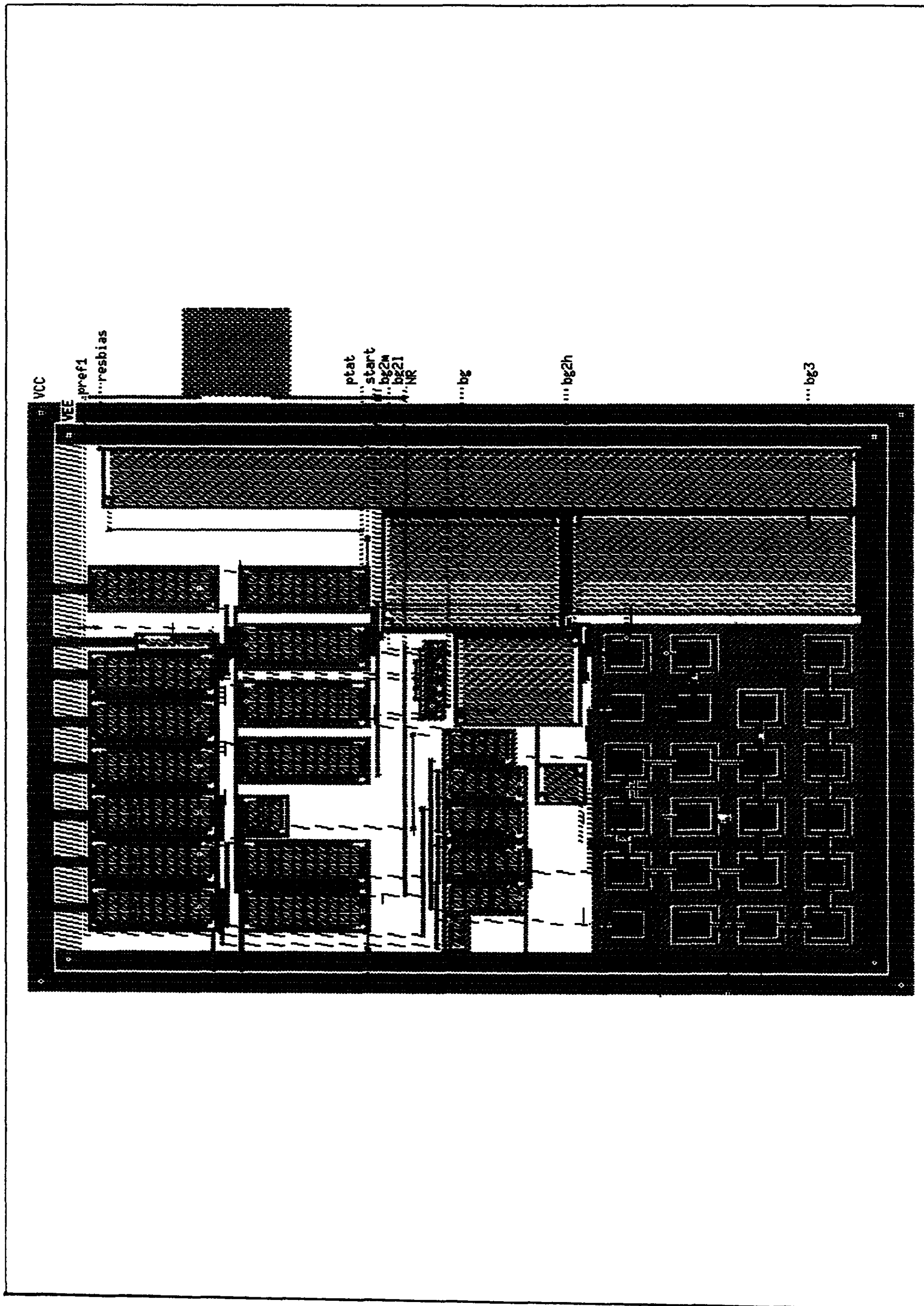

FIGURE 1.5 Bandgap Layout

The fact that the test chip bandgap circuit worked as well as it did (26 ppm) using this trial and error methods shows why the circuit has endured as a voltage reference. Despite the fact that

there may be as much as a 25% variation in absolute resistance values, the bandgap output will remain relatively flat. An in depth examination of the bandgap which will be presented later shows that although the point where zero temperature coefficient may vary (depending on the absolute resistance values), the temperature coefficient in the area of interest will not suffer greatly.

Using the same setup with the Thermostream, a temperature sensor was placed between the packaged part and the socket holding the part. The temperature recorded here was used as the temperature of the die. Measurements were made every 3 degrees to obtain an accurate plot over the temperature range of interest. The testing was achieved using the following equipment:

(1) Datron 1081 Autocal Standards Multimeter
(2) HP3488A Switch/Control Unit (MUX)
(3) HP6201B DC Power Supply
(4) HP4145B Semiconductor Analyzer
(5) Temptronic Thermostream TP0412A-2-60
(6) IBM 386 with GPIB bus

The testing was automated using MS QuickBasic and the GPIB bus to provide equal temperature saturation time for the die. (The Thermostream blows colder air than the required temperature until an equilibrium is reached. Forty-five seconds was found to be a reasonable interval between 3 degree steps for the machine to reach equilibrium.) The HP3488A allowed multiple points to be measured without significant change in temperature across the die.

1.4 Simulation and Design Issues Pertinent to Bandgap Circuits

The bandgap designer is facing a difficult challenge in that success is achieved by balancing two unlike quantities: a PTAT voltage and a base emitter voltage. As the equations in Chapter 4 will show, there is an ideal voltage at which the temperature coefficient is minimized. Due to circuit limitations or foundry variations, this voltage might be unachievable (or unpredictable). Fortunately, the relative flatness of the output voltage despite variation in the absolute resistance values makes the circuit usable.

However, the actual manufactured product will not be exactly what was expected. In addition, the curvature compensation that most bandgap circuits employ will not always act as expected. Due to variations in second order temperature coefficients (which are rarely specified or measured), the bandgap voltage will take on a variety of shapes and will have a variety of temperature coefficients.

The problems that exist deal with the issues of accurate modeling in the simulation models (both for stable and varied temperatures), convergence, and correct simulation procedure. The models that exist for SPICE are a combination of a physical representation and an empirical representation of the device under examination. Parameters can be tweaked to achieve a better fit; however, model parameters should in general remain a constant in the simulation process. The parameters should be extracted and then fixed.

A broad picture of the goals of this project as well as the obstacles in the way of achieving those goals has been presented. CHAPTER 2 gives a detailed look at the simulation of MOS devices in SPICE. Each parameter and its effect on circuit simulation will be evaluated. Emphasis will be placed on the SPICE Level 3 model. CHAPTER 3 presents a detailed look at the simulation of Bipolar devices in SPICE. Each parameter which affects the bandgap circuit (predominately the DC parameters) will be examined. Emphasis will be placed on the Gummel-Poon model. CHAPTER 4 examines the bandgap circuit. An examination of each contributing component is presented. The derivation for the ideal output voltage is presented followed by a more realistic discussion. This will aid in determining the effect that each component has on the output voltage. The variance in output voltage due to variation in resistance values and temperature coefficients will be examined. Due to imprecise foundry specifications, these variations will cause deviations from simulated outputs. Finally, a design procedure for bandgap circuits will be discussed.

2.0 SPICE AND MOSFETS

2.1 Introduction

An understanding of MOS (Metal-Oxide-Semiconductor) transistors (and the modeling of MOS devices used in SPICE) is necessary to gain insight on the contributions these devices have in the operation of the bandgap. It is not enough to know the basic equations governing the operation of this type of transistor. It is important to note which parameters are affected by temperature and which are not. It is likewise important to know what changes will occur in the operating state with variations of each individual parameter. A brief examination of the basic model and equations will be presented. This will be followed by a detailed description of the additional parameters used by the SPICE Level 3 model.

2.2 Static model

The MOS transistor is a field effect transistor in which a doped silicon channel is controlled by the application of an external field through a metal-oxide junction. The MOSFET is a four terminal device consisting of a drain, a source, a gate, and a bulk (substrate) connection. (FIGURE 2.1).

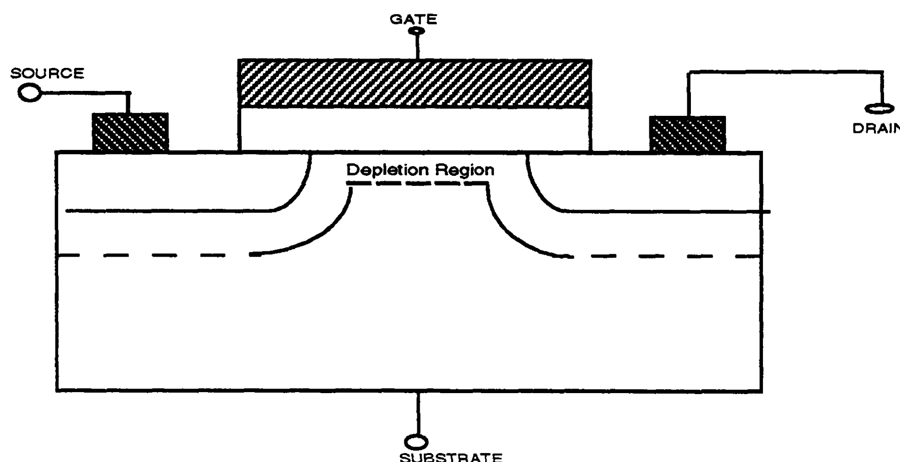

FIGURE 2.1 MOS Structure

The "flatband" condition occurs when there exists an equal carrier concentration at the surface of the transistor and the substrate. In order to create such a condition, an external voltage, V_{FB} (flat-band), must be applied across the gate and bulk. This will overcome the contact potentials and the interface charge. In order to create a channel for current flow, the creation of an inversion layer is necessary. The definition of inversion is when the carrier concentration at the surface is greater and of the opposite type than the concentration in the substrate. This occurs when the surface potential (the potential across the depleted region) equals twice the Fermi potential measured at the neutral edge in a p-type semiconductor. The voltage needed to create this case is called the threshold voltage [9].

2.3 Table of parameters

A brief summary of the parameters used by SPICE Level 1 and 3 will be presented to provide an index of the names, symbols, units, and temperature dependence of these parameters [9].

Symbol	SPICE keyword	Level Used	Parameter name	Typical Value	Units	Temperature Dependence
V_{TO}	VTO	1 - 3	Zero-bias threshold voltage	1.0	V	Yes
KP or UO*COX	KP	1 - 3	Trans-conductance parameter	$3*10^{-5}$	A/V^2	Yes
γ	GAMMA	1 - 3	Body-effect parameter	0.35	$V^{1/2}$	No
$2\phi_p$	PHI	1 - 3	Surface inversion potential	0.65	V	Yes
λ	LAMBDA	1,2	Channel length modulation	0.02	V^{-1}	No
Tox	TOX	1 - 3	Thin oxide thickness	$1*10^{-7}$	m	No
N_A	NSUB	1 - 3	Substrate doping	$1*10^{15}$	cm^{-3}	No

vmax	VMAX	2,3	Maximum drift velocity of carriers	$5*10^4$	m/s	No
η	ETA	3	Static feedback on theshold voltatge	1.0	unitless	No
Θ	THETA	3	Mobility modulation	0.05	V^{-1}	No
δ	DELTA	2,3	Width effect on threshold voltage	1.0	unitless	No
κ	KAPPA	3	Saturation field factor	1.0	unitless	No
Xj	XJ	2,3	Metallurgical junction depth	$1*10^{-6}$	m	No
Xjl	LD	1-3	Lateral diffusion	$0.8*10^{-6}$	m	No
rD	RD	1-3	Drain ohmic resistance	10	Ω	No
rS	RS	1-3	Source ohmic resistance	10	Ω	No
Is	IS	1-3	Bulk junction saturation current	$1*10^{-15}$	A	No
NFS	NFS	2,3	Surface-fast state density	$1*10^{10}$	unitless	No
L,W	L,W	1-3	Length/Width	VARIED	m	No

TABLE 2-1 MOS SPICE Parameters

2.4 Basic equations

The basic equations and model used are called the LEVEL 1 model. The application of a gate source voltage greater than the threshold voltage causes current conducting channel formation. The addition of a voltage across the drain-to-source will cause current to flow by drift. The threshold voltage is given by the equation:

$$V_{TH} = V_{FB} + 2\phi_p + \gamma\sqrt{2\phi_p - V_{BS}} \tag{2.1}$$

Utilizing the following equations:

$$I_X = \frac{dQ_I}{dt} \tag{2.2}$$

(current in a section dx)

$$dQ_I = C'_{OX} W[V_{GS} - V_C(x) - V_{TH}]dx \tag{2.3}$$

(mobile charge present)

$$\frac{1}{dt} = \mu_O \frac{dV_C(x)}{dx^2} \tag{2.4}$$

I_X can be found in the entire channel by:

$$I_{DS} = \mu_O C'_{OX} (\frac{W}{L_{eff}})[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}] \tag{2.5}$$

There are three regions of operation for the MOSFET: subthreshold, linear, and saturation. LEVEL 1 simulations only support the last two. Saturation occurs when the V_{DS} voltage is large enough that a portion of the channel is pinched off. This occurs when the voltage between the channel and the gate equals (or exceeds) the threshold voltage. At this point the channel length is shortened to include only the region where the voltage is less than the threshold voltage. In this region the current is no longer a function of V_{DS}.

SPICE LEVEL 1 uses the following equations to implement the two regions:

Linear region:

FOR $V_{gs} > V_{th}$ AND $V_{ds} < V_{gs} - V_{th}$

$$I_{DS} = KP\frac{W}{L - 2X_{jl}}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS}(1 + \lambda V_{DS}) \tag{2.6}$$

Saturation region:

FOR $V_{gs} > V_{th}$ AND $V_{ds} > V_{gs} - V_{th}$

$$I_{DS} = \frac{KP}{2}\frac{W}{L - 2X_{jl}}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{2.7}$$

where

$$KP = \mu_o C'_{OX}$$
$$V_{TH} = V_{TO} + \gamma\left(\sqrt{2\phi_p - V_{BS}} - \sqrt{2\phi_p}\right) \qquad \text{(2.8 and 2.9)}$$

In the above equations, V_{TO} represents the zero-bias threshold voltage and the λ term is an empirical correction factor for conductance in the saturation region.

2.5 SPICE LEVEL 3 Model

Unfortunately, the LEVEL 1 model does not provide a very accurate picture of the operation of the MOSFET. What is needed is a model that will incorporate the physical second-order effects that ultimately limit the operation of the MOSFET. These effects include back-gate and small geometry effects on the threshold voltage; static feedback from drain-to-gate on the threshold voltage; saturation current limitation due to limited drift velocity and finite output conductance; surface field dependent mobility; weak inversion (subthreshold); and temperature variations of parameter [10].

The SPICE LEVEL 3 model is empirical in nature. The goal of the LEVEL 3 model is to improve on accuracy and to provide simpler calculations than the LEVEL 2 model for all MOSFETs including short and narrow channel transistors. It is my intention to provide an explanation of each new parameter and its effect on the output of the SPICE simulations both with and without temperature variation.

The drain-to-source current for SPICE LEVEL 3 is modeled by a surprisingly simple equation:

$$I_{DS} = \beta\left(V_{GS} - V_{TH} - \frac{1+F_B}{2}V_{DS}\right)V_{DS} \qquad (2.10)$$

where

$$F_B = \frac{\gamma F_S}{4\sqrt{2\phi_p - V_{BS}}} + F_n \qquad (2.11)$$

This simplification from the LEVEL 2 representation uses a Taylor series expansion for the drain-to-source current equation in LEVEL 2 which was derived eliminating the assumption that the fixed charge in the depletion region was independent of the changing drain-to-source voltage. The simplified form in Eqn. 2.10 allows an explicit saturation voltage (V_{DSAT}) to be found. The saturation voltage is defined as the drain voltage at which the carriers reach the maximum velocity (defined by VMAX) at the drain. Any voltage greater than V_{DSAT} will move the pinchoff point further in from the drain edge. In the region between the pinchoff point and the drain edge, the carriers will still be moving at VMAX.

At this point it would be useful to examine the individual parameters which affect the terms in the above equations.

2.5.1 Threshold voltage and related parameters

The SPICE LEVEL 3 threshold voltage is defined as follows:

$$V_{TH} = V_{FB} + 2\phi_p - \sigma V_{DS} + \gamma F_s \sqrt{2\phi_p - V_{BS}} + F_n\left(2\phi_p - V_{BS}\right) \quad (2.12)$$

Unlike the LEVEL 1 threshold model, the LEVEL 3 model presents a tie between the threshold voltage and the geometry of the channel (W and Leff). The link that exists is explained by a reduction of the fixed charge in the depletion region due to the source and drain depletion regions. This occurs when Leff and the width of the depletion region are close in value. The LEVEL 2 model alters the value of γ, the body effect parameter, in order to compensate for this effect. The LEVEL 3 model includes a new definition for the threshold voltage as seen be Eqn 2.12. V_{TO} is the threshold voltage when V_{BS} is set to zero. If this parameter is raised, the device takes a larger voltage to enter saturation. Consequently, as FIGURE 2.2 shows, the entire current curve is pushed down.

σ is an empirical parameter which relates the dependence of the threshold voltage to V_{DS}. The inversion potential is reached at lower voltages in the presence of stronger drain-to-source fields.

Consequently, a lower threshold voltage will result from larger V_{DS}. The model parameter ETA (η) is related by :

$$\sigma = \eta \frac{8.15 \times 10^{-22}}{C_{ox} L_{eff}^{3}} \tag{2.13}$$

FIGURE 2.3 shows the relationship between ETA and I_{DS}. As expected, the plot shows that as VDS is increased, the effect of ETA is more significant.

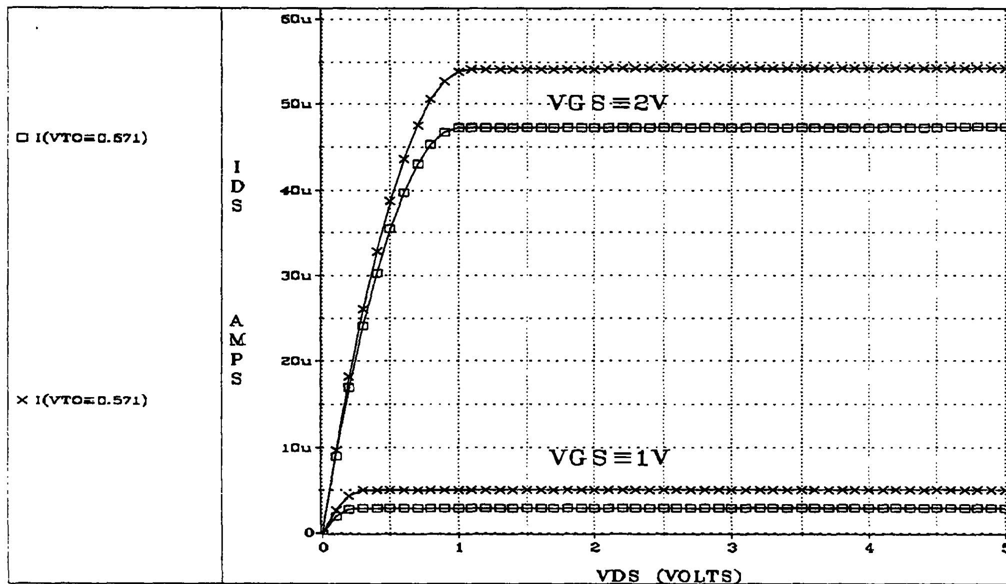

FIGURE 2.2 IDS Variation with VTO

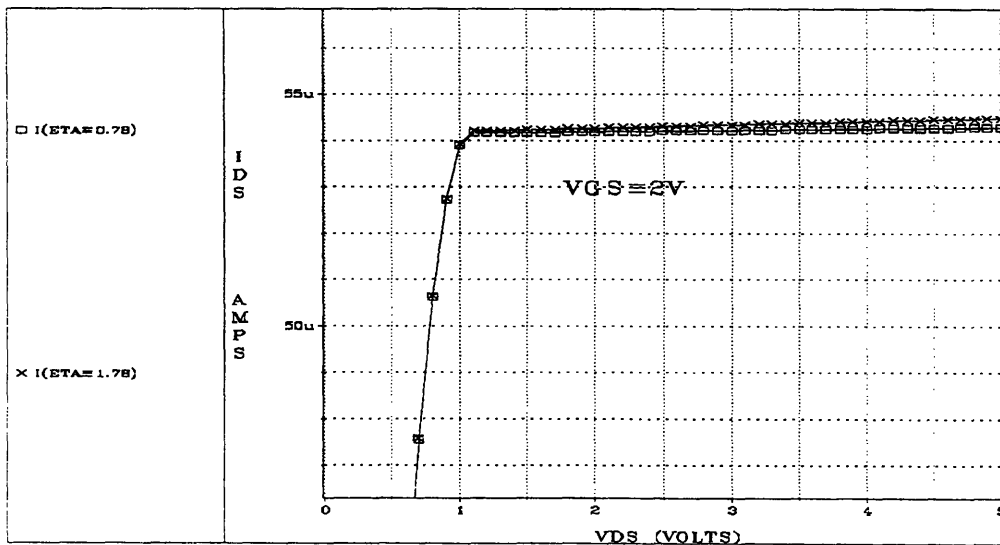

FIGURE 2.3 IDS Variation with ETA

Fs provides correction for short channel effects:

$$F_S = 1 - \frac{X_j}{L_{eff}}\left(\frac{X_{jl} + W_C}{X_j}\sqrt{1 - \left(\frac{W_p}{X_j + W_p}\right)^2} - \frac{X_{jl}}{X_j}\right) \tag{2.14}$$

where Xj = junction depth

Xjl = lateral diffusion

Wc = width of depleted cylindrical region

Wp = width of depleted region on the flat source junction

FIGURE 2.4 shows the location of each of these variables on a MOSFET.

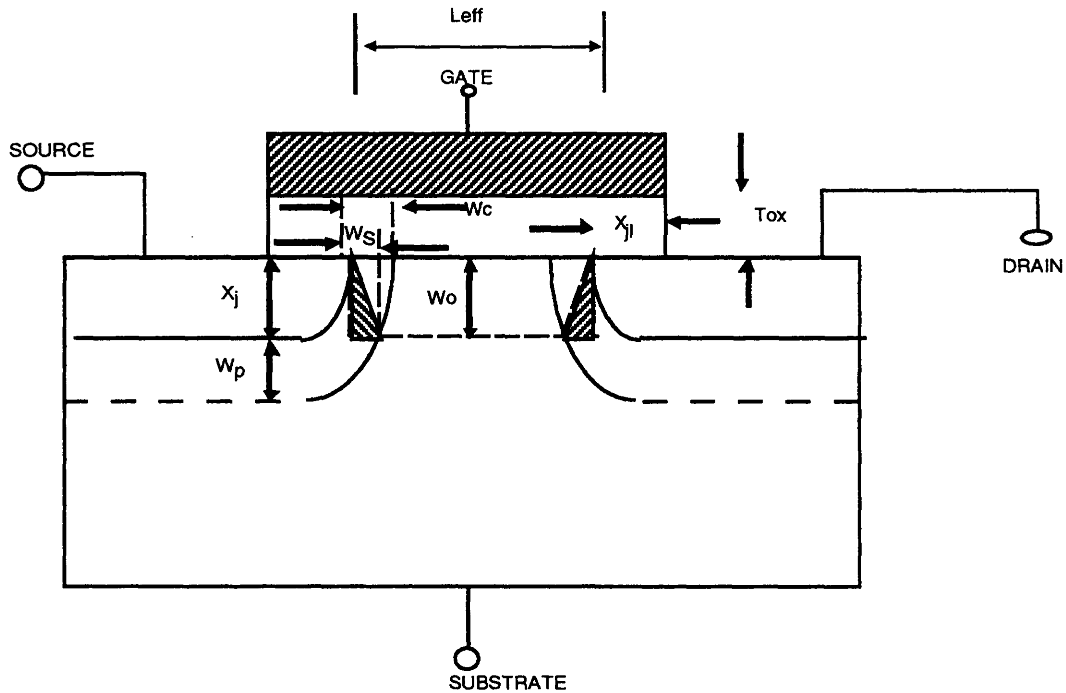

FIGURE 2.4 MOS Structure Geometries

FIGURE 2.5 shows the relationship between XJ and I_{DS}. The effect of XJ is more pronounced in the saturation region. In the linear region, the VDS dependence is small. Consequently, the effect of the parameter Fs will also be small.

Fn provides correction for narrow channel effects. Due to the two dimensional distribution of the substrate charge in the depletion region, the thickness of the depletion region varies

gradually from directly under the channel to the point of pinchoff underneath the oxide. An empirical parameter, F_n, is necessary to fit the experimental data. The SPICE parameter δ is closely related by:

$$F_n = \frac{\varepsilon_s \delta \pi}{2C_{ox}W} \tag{2.15}$$

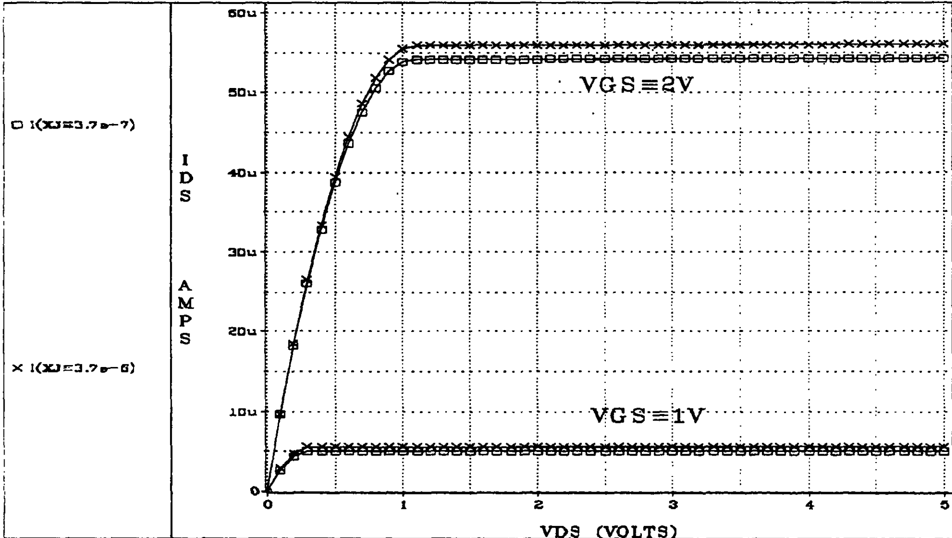

FIGURE 2.5 IDS Variation with Xj

FIGURE 2.6 shows the relationship between δ and I_{DS}. The plot shows that there is a greater effect for larger gate voltages.

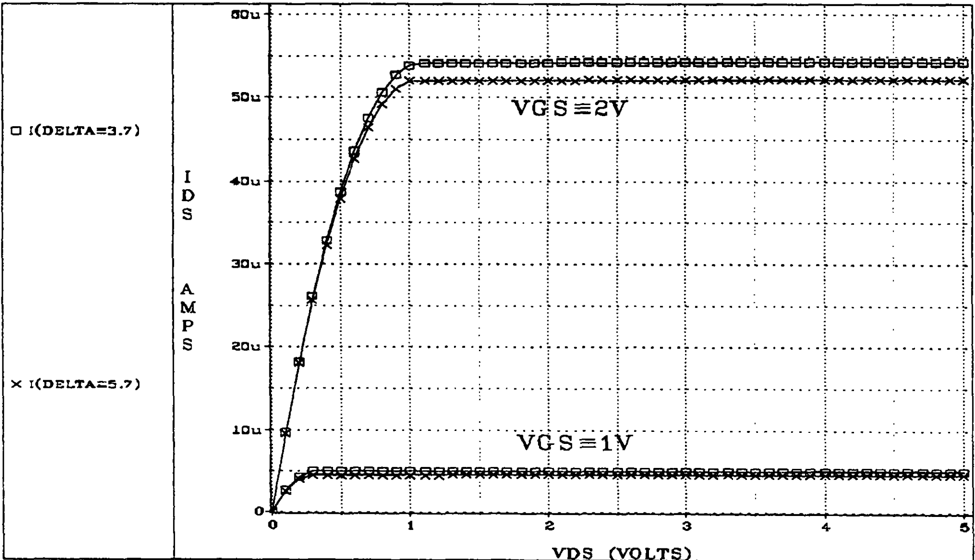

FIGURE 2.6 IDS Variation with DELTA

PHI ($2\phi_p$) is the surface inversion potential. It is the voltage necessary such that the concentration of electrons exceeds the concentration of holes in the substrate (for a p type substrate). The equation governing PHI is given by:

$$\phi_p = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \qquad (2.16)$$

Eqn 2.16 shows that the inversion potential is a function of the doping level of the substrate (another parameter specified in the LEVEL 3 model). The surface moves from equilibrium through depletion until the final state of inversion is achieved when the voltage between the gate and bulk is equal to the threshold voltage. In FIGURE 2.7, one notes that for a variation in PHI, the curves are changed only for large gate voltages and only in the saturation region.

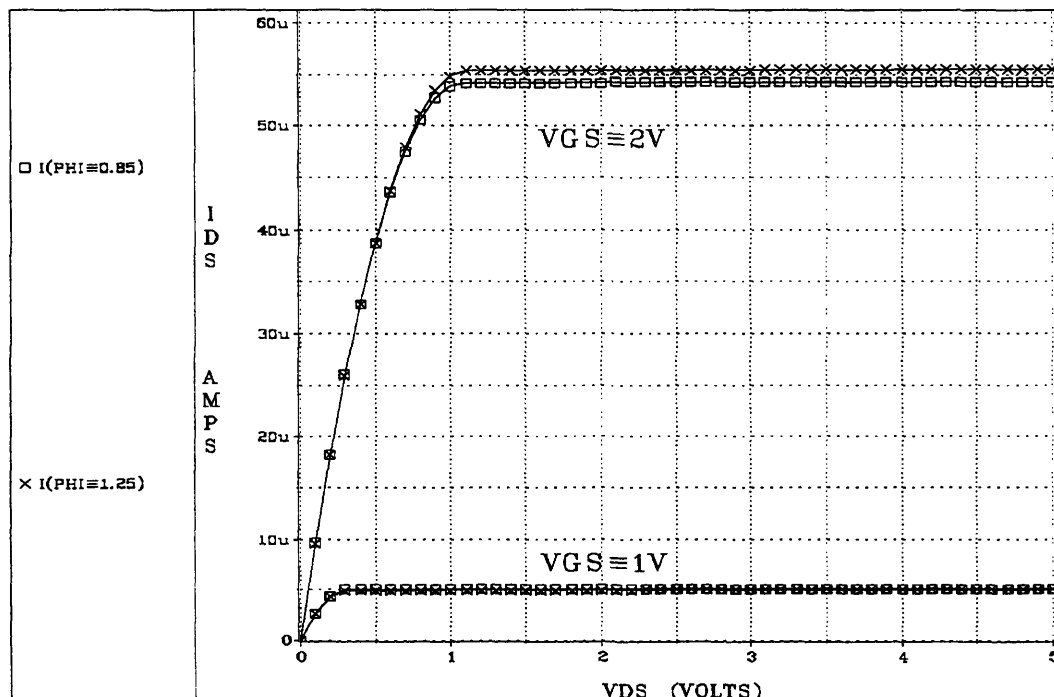

FIGURE 2.7 IDS Variation with PHI

The parameter NSUB represents the substrate doping level (the level of impurity atoms introduced into the substrate.) Not only does it

affect PHI, but also it is related to the widths of all depletion regions in the MOSFET. These depletion widths are important in the determination of the Fs parameter as seen in Eqn 2.14.

Finally, the parameter GAMMA(γ) is called the body effect parameter.

$$\gamma = \frac{\sqrt{2q\varepsilon_s N_A}}{C\,ox} = \frac{t_{OX}}{\varepsilon_{OX}}\sqrt{2q\varepsilon_s N_A} \qquad (2.17)$$

It is used to model how much effect the back bias has on the threshold voltage. In order to cause inversion, the surface potential must exceed the voltage between the substrate (bulk) and source. γ allows the effect of different bulk to source voltages to be simulated accurately. Equation 2.17 shows that γ is proportional to the square root of NSUB and inversely proportional to the square root of C'OX. For large γ , a larger threshold voltage results. Consequently, less current will flow in a given biased MOSFET. This effect is seen in FIGURE 2.8.

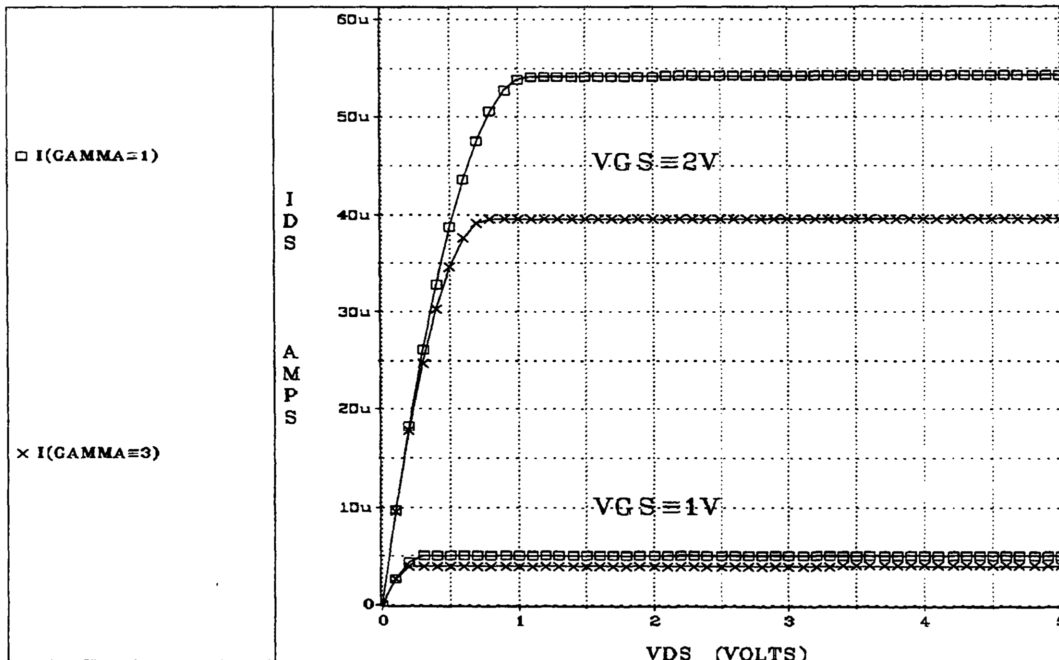

FIGURE 2.8 IDS Variation with GAMMA

Many of the above threshold related parameters also have some form of temperature dependence. Two of the most dominant are the effects of n_i (intrinsic carrier concentration) and PHI. Eqn 2.16

shows the relationship between PHI and temperature. The intrinsic carrier concentration is related in the following manner:

$$n_i = 1.45\times10^{10}\left(\frac{T}{300}\right)^{1.5} e^{\left(\frac{q}{2k}\right)\bullet\left(\frac{1.16}{300}-\frac{E_G}{T}\right)} \tag{2.18}$$

Using these results and the relationship for VTH:

$$\Delta V_{TH}(T) = \left[\phi_p(T_{NEW}) - \phi_p(T)\right] - \gamma\sqrt{2}\left[\sqrt{\phi_p(T_{NEW})} - \sqrt{\phi_p(T)}\right] \tag{2.19}$$

One notes that VTO will be smaller with higher temperatures [11]. However, for a given bias condition, less current will result with higher temperature even if the required threshold voltage is smaller. (SEE FIGURE 2.9) This is due to a decrease in mobility at higher temperatures which will be explained in the next section. It is also important to note that due to the dependence of GAMMA on oxide thickness (Tox), a larger Tox will cause a larger change in threshold voltage with temperature.

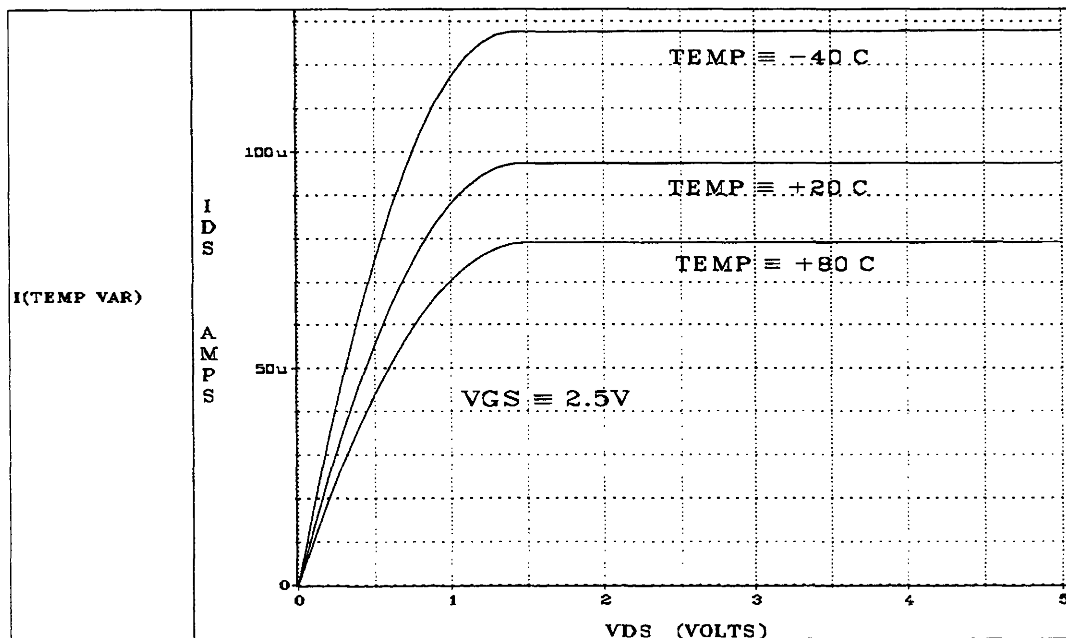

FIGURE 2.9 **IDS Variation with Temperature**

Figures 2.10-2.13 show the results of the extraction process over temperature for VTO and PHI for an NMOS and PMOS 10x10µm

transistor. The figures show both the SPICE adjusted parameter and the extracted parameter. The adjusted parameters were found by taking the nominal temperature extracted parameter set and allowing SPICE to adjust the values when a different temperature was defined. The same physical setup used to obtain the data in the lab was used in the SPICE simulations.

The plots show that the SPICE predicted parameter VTO matches the measured (extracted) values of VTO with a minor DC level shift. However, the PHI parameter shows a large difference between extracted and simulated value.

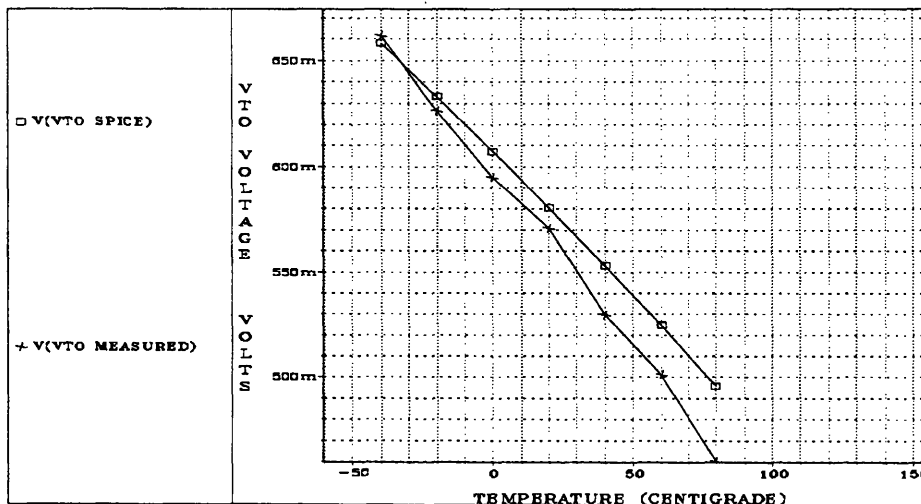

FIGURE 2.10 VTO Variation with Temperature (NMOS)

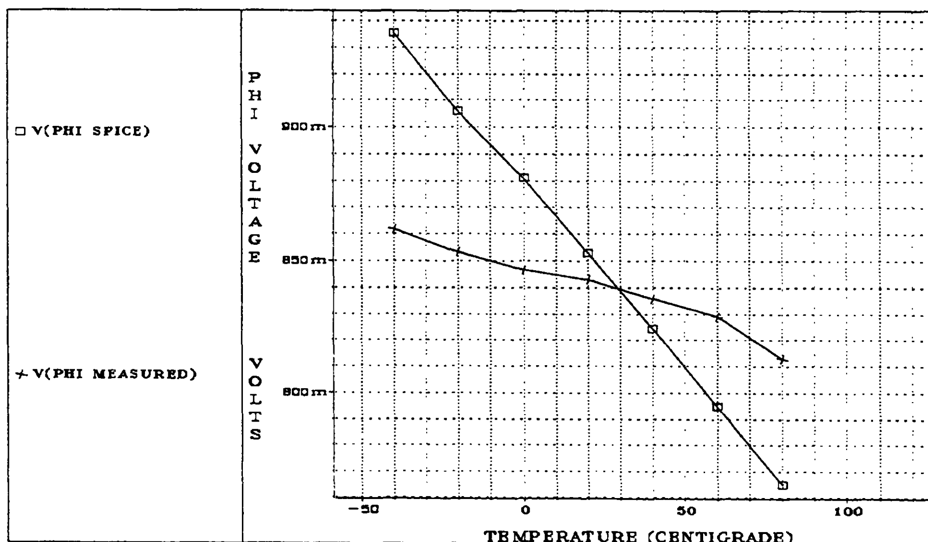

FIGURE 2.11 PHI Variation with Temperature (NMOS)

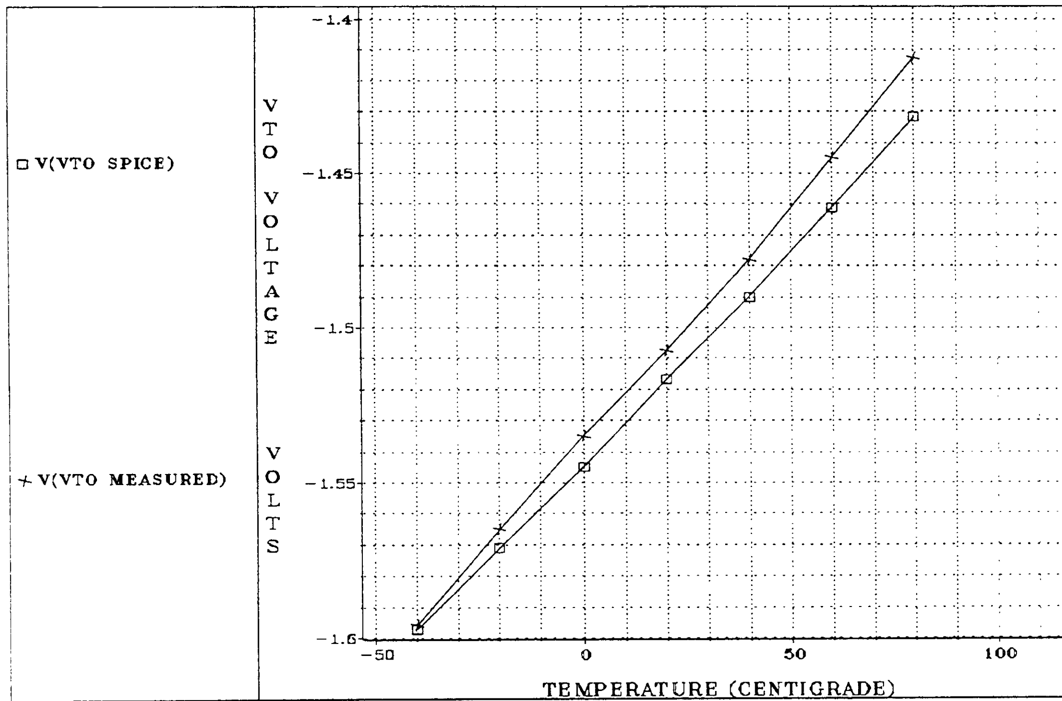

FIGURE 2.12 VTO Variation with Temperature (PMOS)

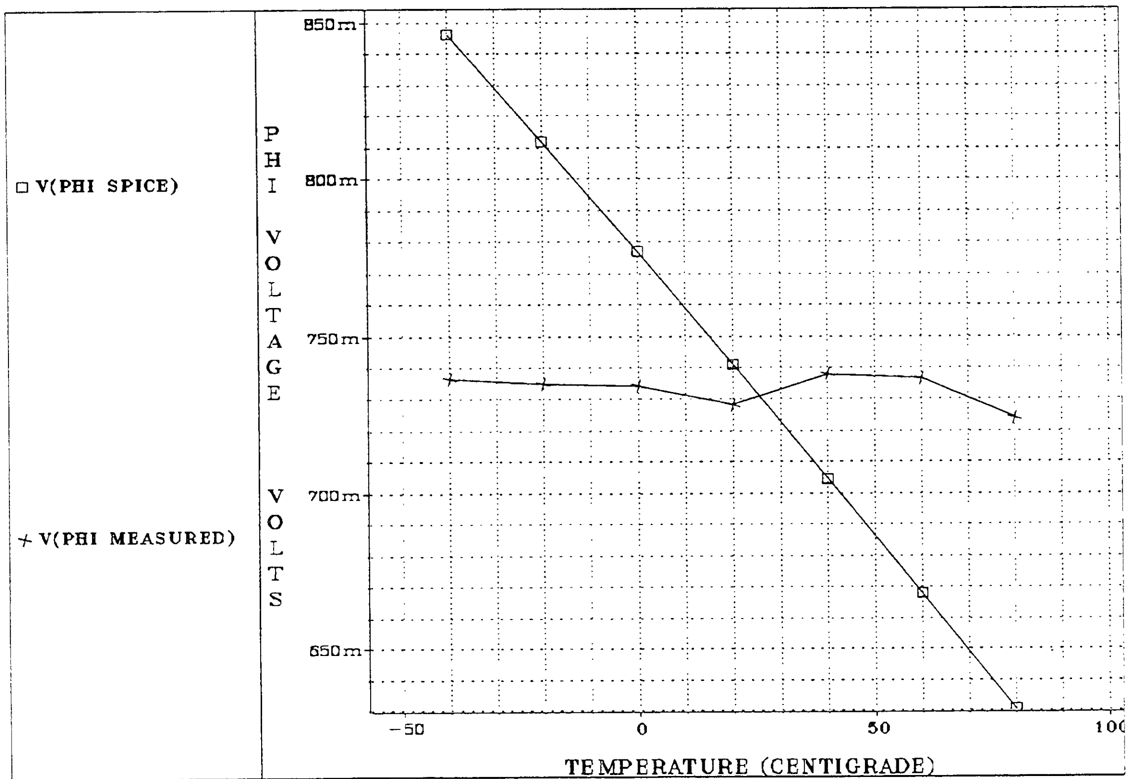

FIGURE 2.13 PHI Variation with Temperature (PMOS)

2.5.2 Surface mobility and related parameters

Another observed effect is the reduction in mobility with increased gate voltages. The mobility of the carriers is related to the velocity of the carriers and the electric field which propels them:

$$v(x) = \frac{dx}{dt} = -\mu E_x(x) = \mu \frac{dV_c(x)}{dx} \tag{2.20}$$

This mobility is used to calculate the surface mobility which shows the reduction due to the gate field contribution.

$$\mu_s = \frac{\mu_O}{1 + \theta(V_{GS} - V_{TH})} \tag{2.21}$$

The SPICE parameter UO represents the mobility μ_O at low gate voltages where the effects of gate field reduction are minimized. The THETA parameter controls how much of a reduction is needed to provide accurate modeling. In SPICE LEVEL 3, the surface mobility is then used to compute the effective mobility seen in the channel. There is an additional constraint placed by the limited speed the carriers can obtain (specified in the VMAX parameter.)

$$\mu_{eff} = \frac{\mu_s}{1 + \mu_s V_{DS} / v_{\max} L_{eff}} \tag{2.22}$$

In the equation for IDS, one finds that the current is proportional to the mobility. Consequently, if UO increases, the resulting current will increase for a given bias condition. FIGURE 2.14 shows the relationship between THETA and I_{DS} and that a more pronounced effect is seen as the gate voltage increases [10].

The VMAX parameter represents the maximum drift velocity of the carriers. For MOSFET's with channel lengths shorter than 10 microns, a smaller amount of current will result from a short channel device than from a larger device with the same geometrical ratio. This occurs because the carriers have reached the scattering limited velocity in the channel before the drain-source voltage is equal to V_{GS} - V_{TH}. The charge in the channel is nearly pinched off but in reality charge must exist to sustain the saturation current. The amount of charge in this "pinched off" region is related to the speed at which the carriers can move. One notes that for increased

VMAX, the effective mobility is increased. Consequently, larger drain currents will result in a given transistor. (See FIGURE 2.15) In addition, the plot also shows that the saturation voltage required is higher for larger VMAX. SPICE uses the following equations to calculate this voltage [9]:

$$V_a = \frac{V_{GS} - V_{TH}}{1 + F_B} \tag{2.23}$$

$$V_b = \frac{v_{max} L_{eff}}{\mu_s} \tag{2.24}$$

$$V_{DSAT} = V_a + V_b - \sqrt{V_a^2 + V_b^2} \tag{2.25}$$

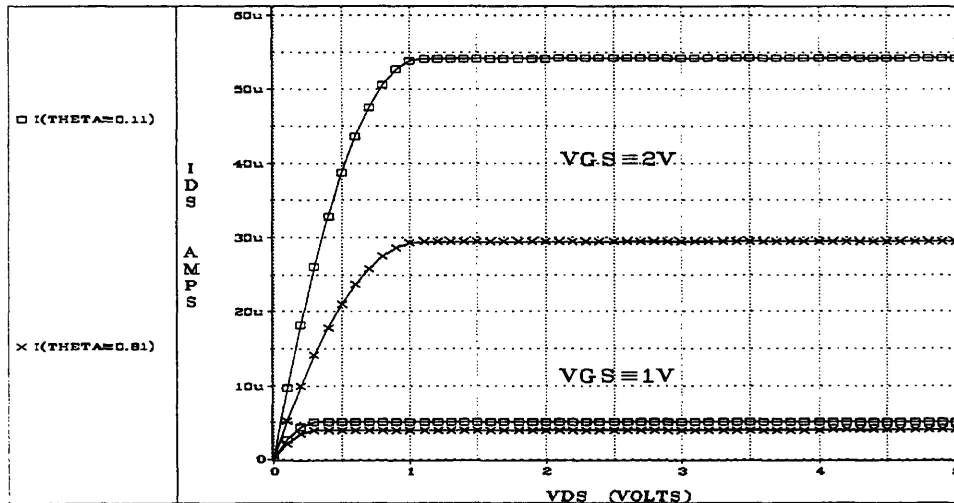

FIGURE 2.14 IDS Variation with THETA

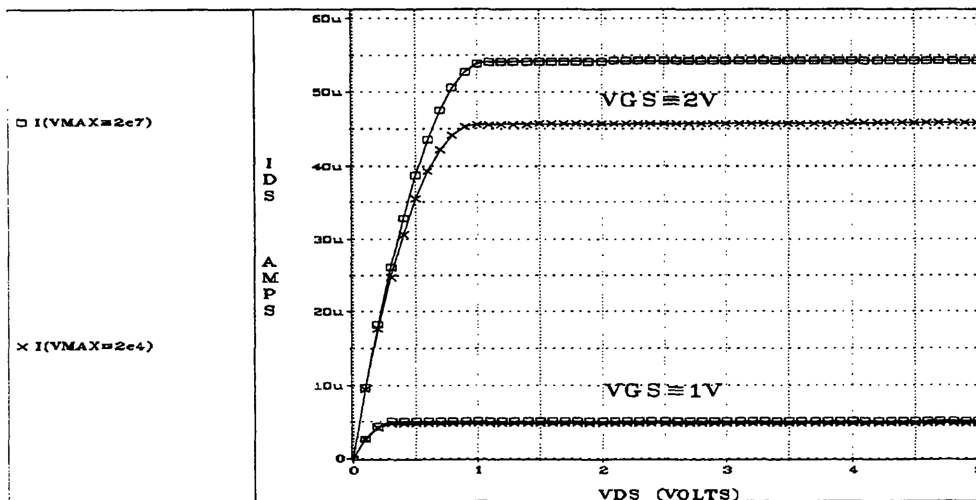

FIGURE 2.15 IDS Variation with VMAX

There exists a large temperature dependence in the UO parameter. In fact, it is precisely because of this dependence that low temperature CMOS applications require smaller bias voltages to produce the same currents that demands large bias voltages at higher temperatures. Mobility actually increases with a decrease in temperature. There are three scattering mechanisms that affect mobility [11] :

(1) lattice scattering
(2) ionized impurity scattering
(3) vertical .field dependent scattering

As a MOSFET's gate voltage rises and carriers are pushed to the surface, surface scattering causes a large reduction in mobility. For transistors doped on the surface, this is a problem and as the temperature is dropped the lattice scattering is reduced causing a reduction in the surface scattering. The vertical field dependency is reduced by using devices built in wells. These devices in general will have less scattering than light shallow implants. Impurity scattering is not affected by temperature in the range examined (-40 to 85 degrees C) and is a reduction in any environment. In general, there is an overall increase in mobility when there exists a decrease in scattering. No temperature variation in the parameter VMAX was observable. SPICE models the temperature variation in the UO parameter with the following equation:

$$\mu_O(T_1) = \mu_O(T_2)\left(\frac{T_1}{T_2}\right)^{1.5} \qquad (2.26)$$

FIGURES 2.16-2.17 show the extracted results of mobility over temperature for an NMOS and PMOS 10x10 transistor. The SPICE model does an excellent job matching the measured response. A possible improvement to the model might include the ability to change the exponent in the equation for UO to provide more accuracy.

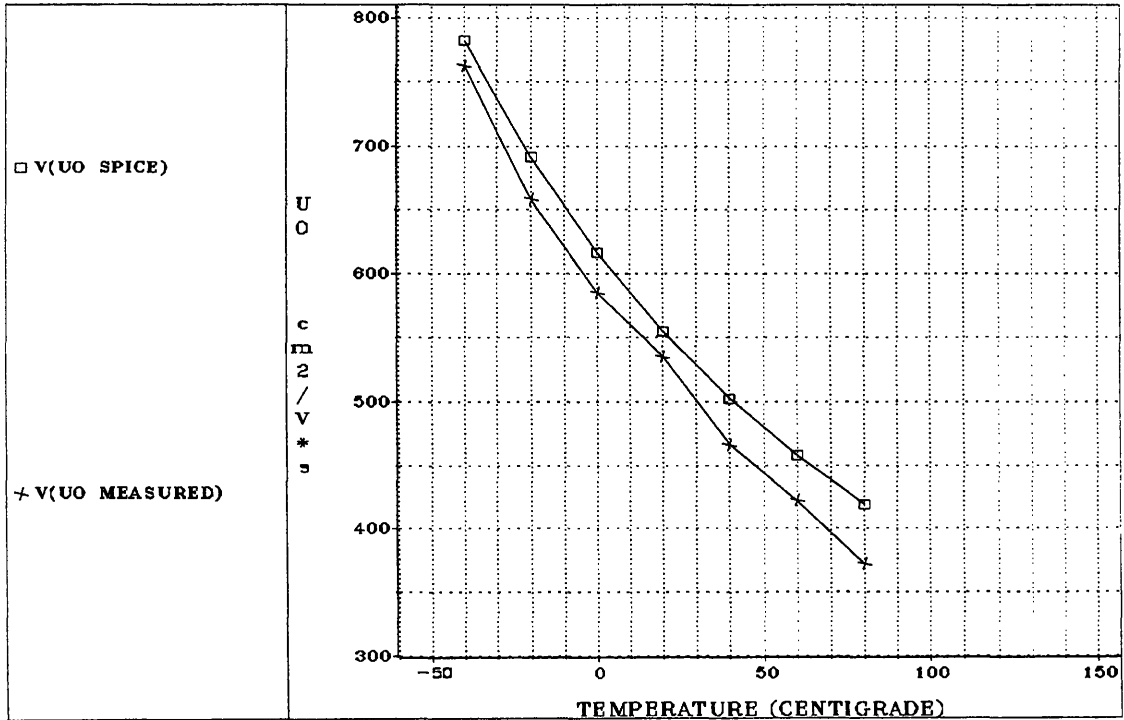

FIGURE 2.16 UO Variation with Temperature (NMOS)

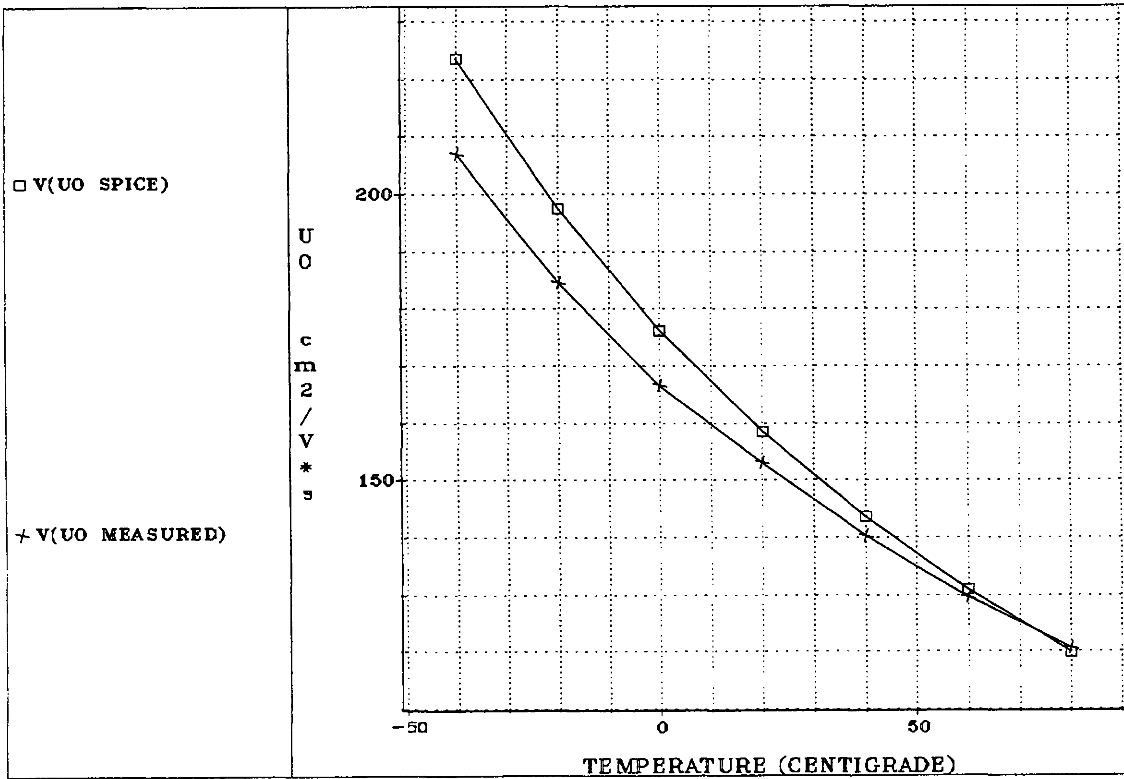

FIGURE 2.17 UO Variation with Temperature (PMOS)

2.5.3 Geometrical parameters

In addition to the parameters already discussed, there are a handful of geometrical parameters that are used in the LEVEL 3 model. These parameters are listed below:

(1) KAPPA -- This parameter is an empirical parameter used in the equation to more accurately model the channel length modulation. The effect is shown in FIGURE 2.18. It only has effect in the saturation region where channel length modulation (change in channel length with pinchoff) occurs. The plot shows that deviations in KAPPA will not greatly effect circuit performance.

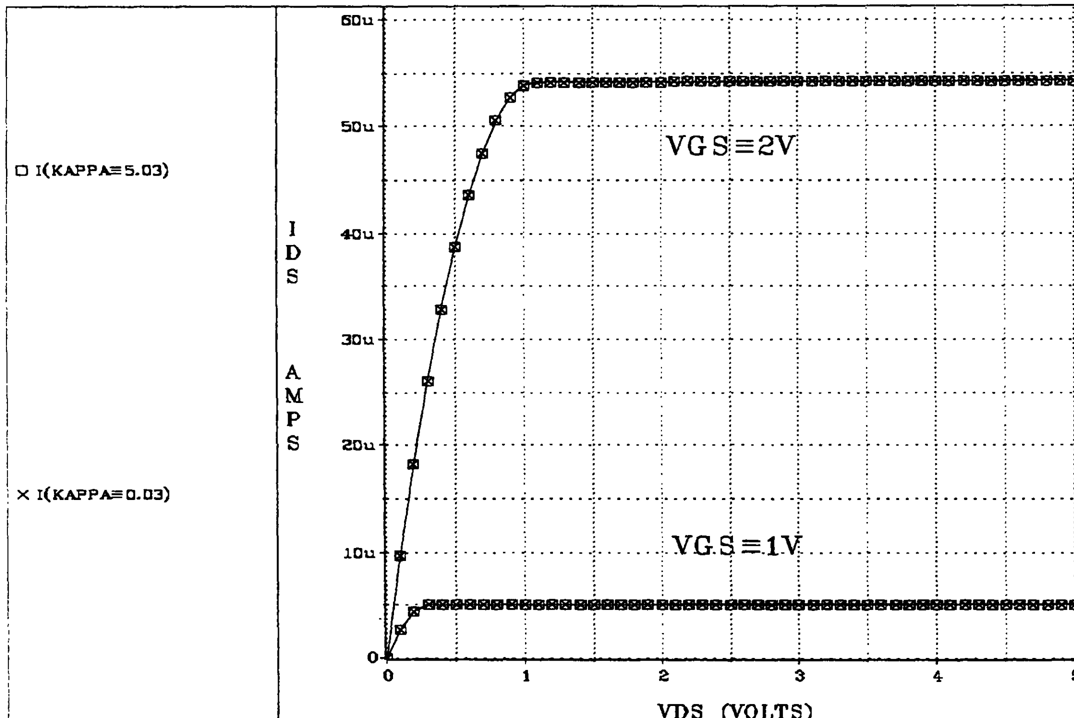

FIGURE 2.18 IDS Variation with KAPPA

(2) Xj and Xjl (LD) -- These parameters represent the junction depth and lateral diffusion as shown in FIGURE 2.4. The effect of the parameter Xj is shown in FIGURE 2.5. As the plot shows, Xj does not change the saturation voltage. It simply pushes the entire curve up at every point. Xj and Xjl will however cause a change in the threshold voltage as seen in Eqn 2.14.

(3) Tox - This parameter represents the oxide thickness. FIGURE 2.19 shows the variation in the drain current with the oxide thickness. The oxide thickness is inversely proportional to the oxide capacitance (Cox). This explains the decrease in drain current with increasing oxide thickness.

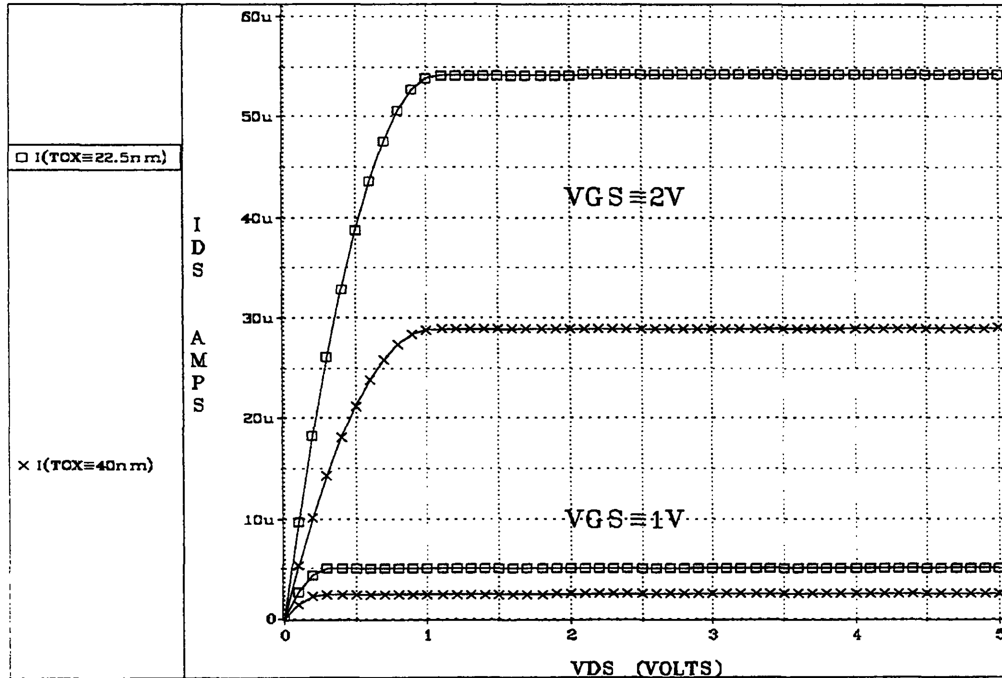

FIGURE 2.19 IDS Variation with TOX

2.6 Extraction method

The extraction of MOS parameters presented one of the greater difficulties in obtaining working models for the devices used in the bandgap. Originally, I had hoped to use the available literature on MOS extraction to write an extraction routine for the project. Unfortunately, the parameters that were extracted did an average job matching the measured results. This was most likely due to errors in creating a perfect algorithm and testing procedure from the literature. The next step was to use these models as a starting point for the SANCAD Model Station optimizer. However, upon comparing the optimized results of my extracted parameters from the test chip with the optimized ORBIT parameters, I found that the

latter method yielded a better fit. Figures 2.20-2.22 show all models compared at three temperatures. Table 2.2 shows four sets of parameters: the original ORBIT parameters obtained from the foundry, the ORBIT optimized parameters, the parameters my program obtained, and my optimized parameters.

PARAMETER	ORBIT ORIGINAL	ORBIT OPTIMIZED	EXTRACTED PARAMETERS	EXTRACTED OPTIMIZED
UO	521.3	535.3	359.3	402.9
VTO	0.9175	0.5709	0.526	0.735
TOX	2.25e-08	2.25e-08	2.25e-08	2.25e-08
GAMMA	N/A	1.005	0.994	0.926
PHI	N/A	0.8429	0.7936	0.7098
NSUB	5.7e+16	6.35e+16	7.00e+16	7.07e+16
XJ	3e-07	3.74e-07	N/A	3.39e-05
ETA	0.396	0.7855	3.81	3.81
DELTA	2.144	3.745	-0.450	-0.132
KAPPA	0.135	0.0314	2.20	3.23
THETA	0.0327	0.1144	-0.008	0.0328
VMAX	4.95e+04	2.56e+07	9.16e+05	3.02e+06
LD	2.02e-07	9.01e-08	N/A	2.01e-07
NFS	5.99e+11	5.14e+10	N/A	5.99e+11

TABLE 2.2 MOS Parameter Comparison

The MATLAB code for the extraction program is included as APPENDIX A. The procedure for extraction follows the recommendations made in one of the existing articles on MOS extraction [12]. A brief summary of the process will be presented. The procedure is as follows:

(1) Obtain the oxide thickness (T_{OX}) and other fixed parameters.

(2) VT, θ (THETA) and β (BETA)for a given VBS are extracted by measuring the drain current for VDS = 0.1 at specified gate voltages.

(3) Rt, LD (Xjl), ΔW are extracted by measuring IDS at VDS = 0.1, VBS = 0 , and VGS at some constant voltage for transistors with varied lengths and widths.

(4) A rough guess for UO and θ is then made using the available data from part 2.

(5) γ (GAMMA) is extracted using the threshold voltages for varied VBS voltages obtained in part 2.

(6) η (ETA) is extracted measuring the threshold voltage for varied VDS.

(7) δ is extracted using the measured and predicted threshold voltage for a specific VBS.

(8) VMAX is extracted using measurements of ID for VG = 5, VBS = 0, and two drain voltages (VD = 0.1 and VD = 0.6(VG-VTO)).

(9) κ (KAPPA) is extracted using an ID measurement at VG = 5, VD = 5, and VBS = 0.

There are *other* extraction algorithms that have a more iterative approach. I attempted to code these in MATLAB and did not meet with any success in extracting a viable model. The references for these alternative MOS extraction methods are given in APPENDIX B.

FIGURES 2.20-2.22 show the results of the extraction procedure that were used in the simulation of the bandgap. It is apparent from these plots that the models breakdown in two areas: high gate voltages and high temperatures. However, the models accurately model the measured response in the region where they will be used in the bandgap. This is an important fact that must not be overlooked. It is not necessary to obtain a model that is accurate in *every* condition and all design spaces. It *is* necessary to obtain a model that will yield correct results in the design area in which it will be used. The models for the NMOS and PMOS devices used in the simulations of the bandgap are presented in APPENDIX C. This model corresponds to the optimized version of the ORBIT parameters fit to measured data taken from the test chip.

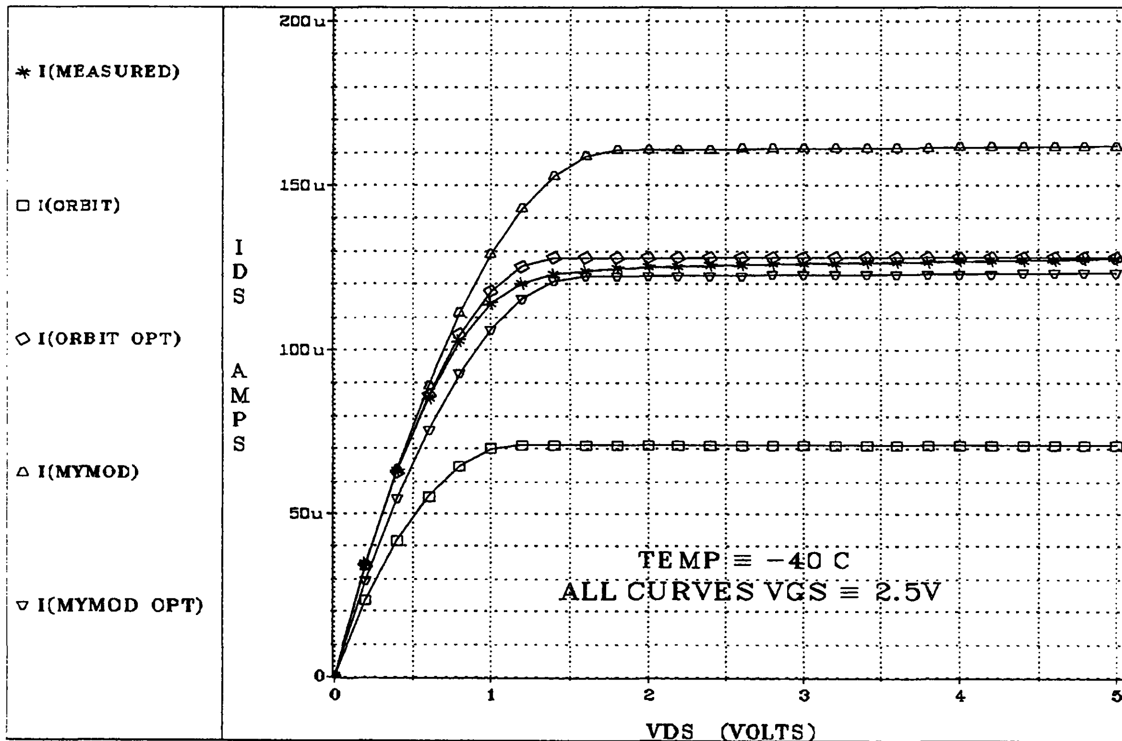

FIGURE 2.20 Model Comparison at -40 degrees C

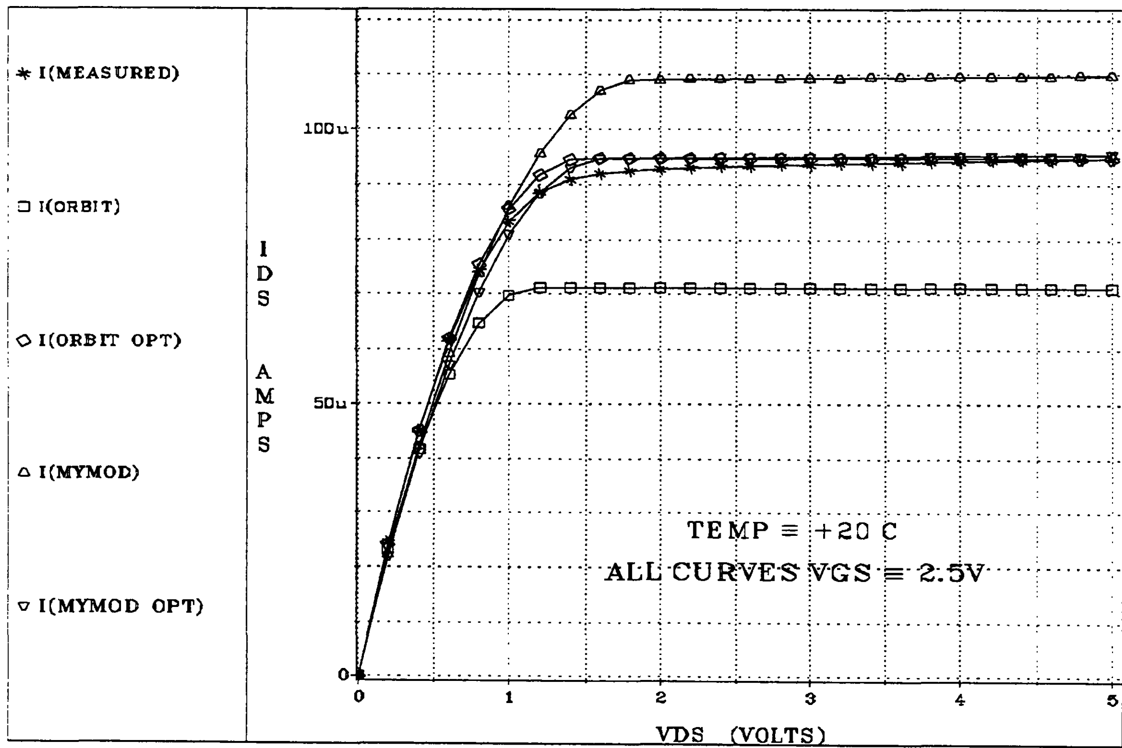

FIGURE 2.21 Model Comparison at +20 degrees C

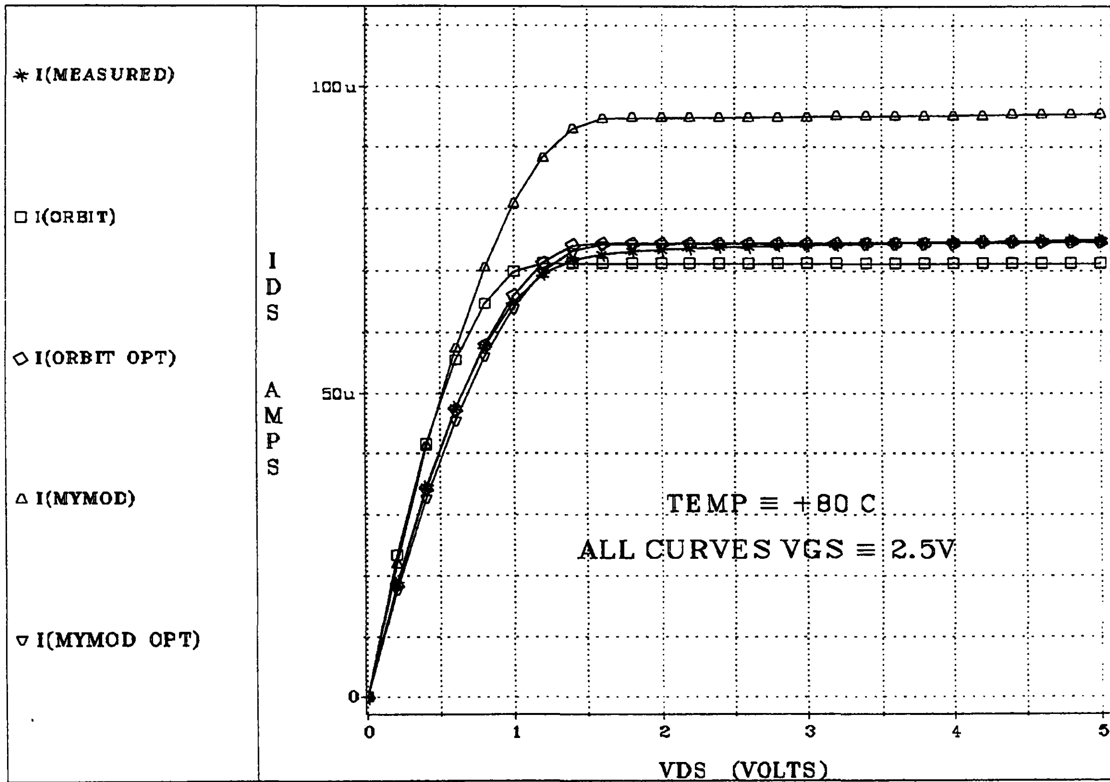

FIGURE 2.22 **Model Comparison at +80 degrees C**

3.0 BIPOLAR TRANSISTORS

3.1 Introduction

The generation of the bandgap voltage requires the use of a base emitter junction. Many CMOS processes do not give bipolar transistor specifications as the device is a parasitic for the process. (The choices are limited to a vertical PNP junction or a horizontal PNP junction in an N-well process). Consequently, the designer is at a real disadvantage in the design of the bandgap circuit: even if a parasitic model can be found for a different foundry there is little hope that two foundries' models will match and yield the same result. The best approach is to obtain a sample parasitic device from the foundry from which parameters may be extracted for SPICE use. With this in mind, a look at the operation and models of the BJT will provide insight on an approach to obtaining these parameters.

3.2 Basic operation

The parasitic BJT operates in the same fashion as a normal bipolar device with the exception being for vertical parasitic devices the substrate (which must serve either as the collector or emitter) must be tied to a particular voltage to prevent forward biasing. This does not present a problem for the bandgap circuit because the need is solely for a base emitter voltage and not for an actual bipolar transistor. The device itself consists of the p substrate, an N-well and a p+ diffusion into the N-well. As with normal bipolar devices, a forward biased emitter base junction has two effects:

(1) The barrier for holes is lowered allowing emitter to base injection (a good result as these holes represent the wanted current component in the pnp device.).

(2) The barrier for electrons is lowered allowing base to emitter injection (a bad result as recombination will prevent holes from being swept across into the collector).
Similarly, if the collector base junction is reverse biased, there will be two effects:

(1) The barrier for electrons from the base to the collector is raised.

(2) The barrier for holes from the collector to base is raised.
If the diffusion length in the base is long relative to the actual width of the base region, the holes injected from the emitter will be swept across to the collector [13].

Ideally, the base current should be small as it is composed of the electrons needed to replace the back injection from the base to the emitter, the electrons needed to replace holes recombining in the base, and thermally generated electrons in the diffusion region of the collector.

FIGURE 3.1 shows a high level model of the currents generated in the PNP bipolar transistor. The values of these currents can be discovered solving the following equations:

$$I_E = I_{E_p}(0) + I_{E_n}(0'') \tag{3.1}$$

$$I_C = I_{C_p}(W) + I_{C_n}(0') \tag{3.2}$$

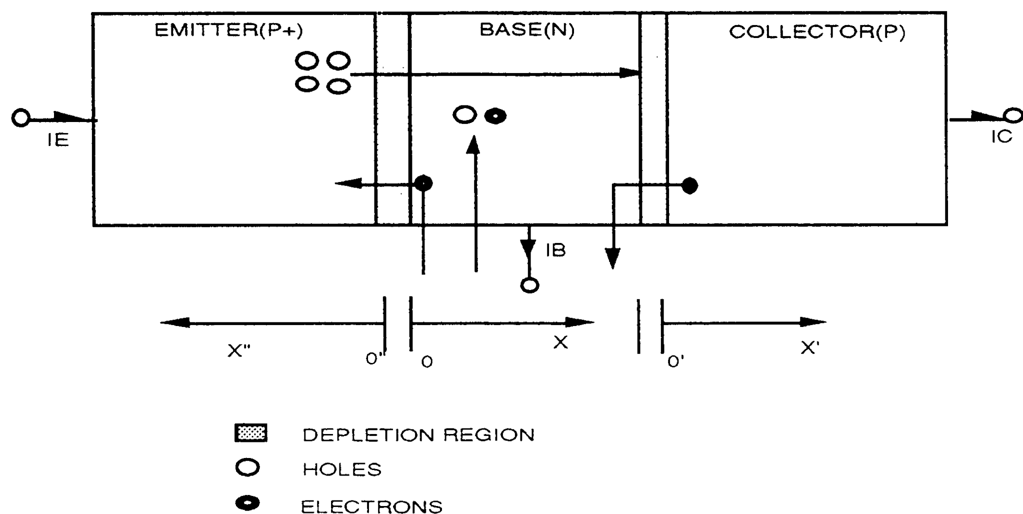

FIGURE 3.1 PNP Bipolar Structure

These equations require solutions involving the derivative (with respect to the position x in FIGURE 3.1) of different carrier concentrations in the various regions. The solutions will yield the following results:

$$I_E = qAn_i^2\left[\frac{D_E}{L_E N_E}+\frac{D_B}{WN_B}\right]\left(e^{\frac{qV_{EB}}{kT}}-1\right)-qAn_i^2\left[\frac{D_B}{WN_B}\right]\left(e^{\frac{qV_{CB}}{kT}}-1\right) \qquad (3.3)$$

$$I_C = qAn_i^2\left[\frac{D_B}{WN_B}\right]\left(e^{\frac{qV_{EB}}{kT}}-1\right)-qAn_i^2\left[\frac{D_C}{L_C N_C}+\frac{D_B}{WN_B}\right]\left(e^{\frac{qV_{CB}}{kT}}-1\right) \qquad (3.4)$$

$$I_B=I_E-I_C \qquad (3.5)$$

where D_X is the diffusion constant for the X region
W is the base width
L_X is the diffusion length for the X region
N_X is the doping in region X

These equations can be simplified depending on which region of operation the transistor is biased. FIGURE 3.2 shows the regions of operation and the assumptions that can be made in each.

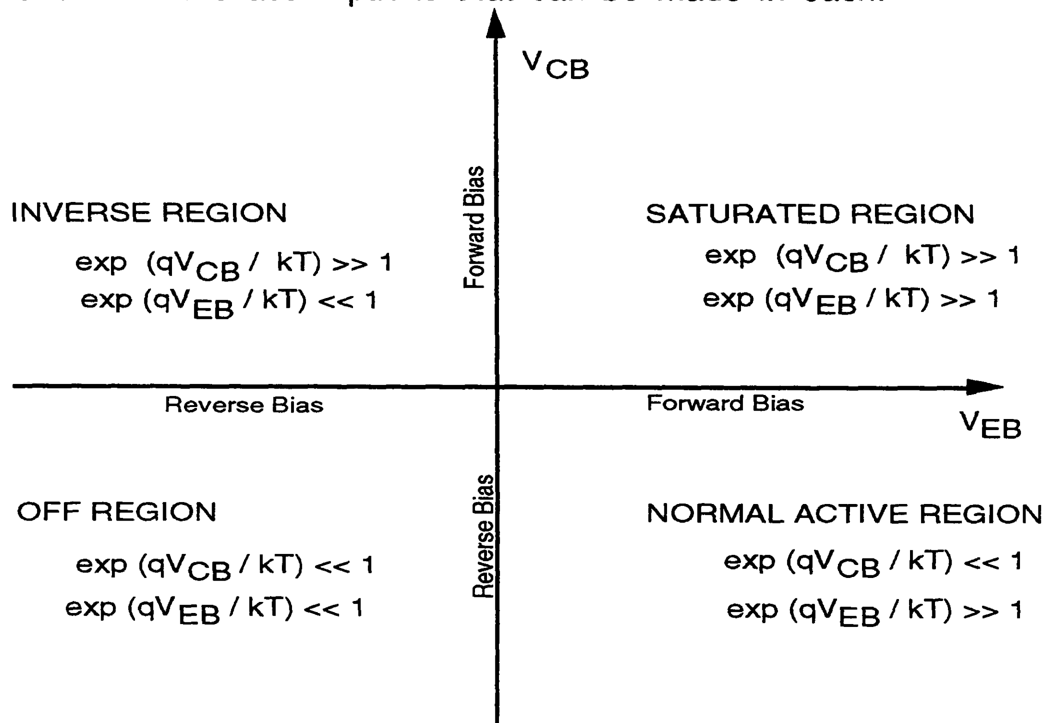

FIGURE 3.2 PNP Operating Regions

3.3 Table of Parameters

A brief summary of the SPICE parameters useful in modeling the BJT for the bandgap circuit is presented below [9].

Symbol	SPICE keyword	Level Used	Parameter name	Default Value	Units	Temperature Dependence
I_S	IS	EM1	Saturation current	1E-16	A	Yes
β_F	BF	EM1	Maximum forward current gain	100	unitless	Yes
β_R	BR	EM1	Maximum reverse current gain	20	unitless	Yes
n_F	NF	GP	Forward current emission coeff.	1	unitless	No
n_R	NR	GP	Reverse current emission coeff.	1	unitless	No
C_2	$ISE=C_2I_S$	EM3	Base-emitter leakage sat. current	0	A	Yes
C_4	$ISC=C_4I_S$	EM3	Base-collector leakage sat. current	0	A	Yes
I_{KF}	IKF	GP	Corner for forward β high current rolloff	∞	A	No
I_{KR}	IKR	GP	Corner for reverse β high current rolloff	∞	A	No
n_{EL}	NE	GP	Base-emitter leakage emission coeff.	1.5	unitless	No
n_{CL}	NC	GP	Base collector leakage emission coeff.	2	unitless	No
V_A	VAF	EM3	Forward early voltage	∞	V	No
V_B	VAR	GP	Reverse early voltage	∞	V	No
E_g	EG	EM1	Energy gap for temperature effect on Is	1.11	eV	Yes
r_C	RC	EM2	Collector resistance	0	Ω	Yes

r_e	RE	EM2	Emitter resistance	0	Ω	Yes
r_b	RB	EM2	Base resistance	0	Ω	Yes
$X_{T\beta}$	XTB	GP	Forward and reverse β temp. coefficients	0	unitless	No
X_{TI}	XTI	GP	Saturation current temp. exponent	3	unitless	no

TABLE 3.1 BJT SPICE Parameters

3.4 Ebers-Moll Model

3.4.1 EM1 Model (I_S, β_F, β_R, Eg, Tnom)

The bipolar transistor can be modeled as a pair of pn junctions in which the operation of each is influenced by the other. The basic EM1 model will represent all four regions of operation described in FIGURE 3.2. It is a DC model meaning that no charge storage in the device is characterized. There are presently two models that are used in the EM description: a transport version and an injection version. Both models yield the same information. The difference between the two is that initially the two models differ in variable assignment. The injection version which provides good insight into the model will be examined here. FIGURE 3.3 shows the EM1 static model. Looking at the model, it is apparent that the following relationships hold:

$$I_E = I_F - \alpha_R I_R = \left(I_{FO}(e^{qV_{EB}/kT} - 1)\right) - \left(\alpha_R I_{RO}(e^{qV_{CB}/kT} - 1)\right) \tag{3.6}$$

$$I_C = \alpha_F I_F - I_R = \left(\alpha_F I_{FO}(e^{qV_{EB}/kT} - 1)\right) - \left(I_{RO}(e^{qV_{CB}/kT} - 1)\right) \tag{3.7}$$

$$I_B = (1-\alpha_F)I_F + (1-\alpha_R)I_R \tag{3.8}$$

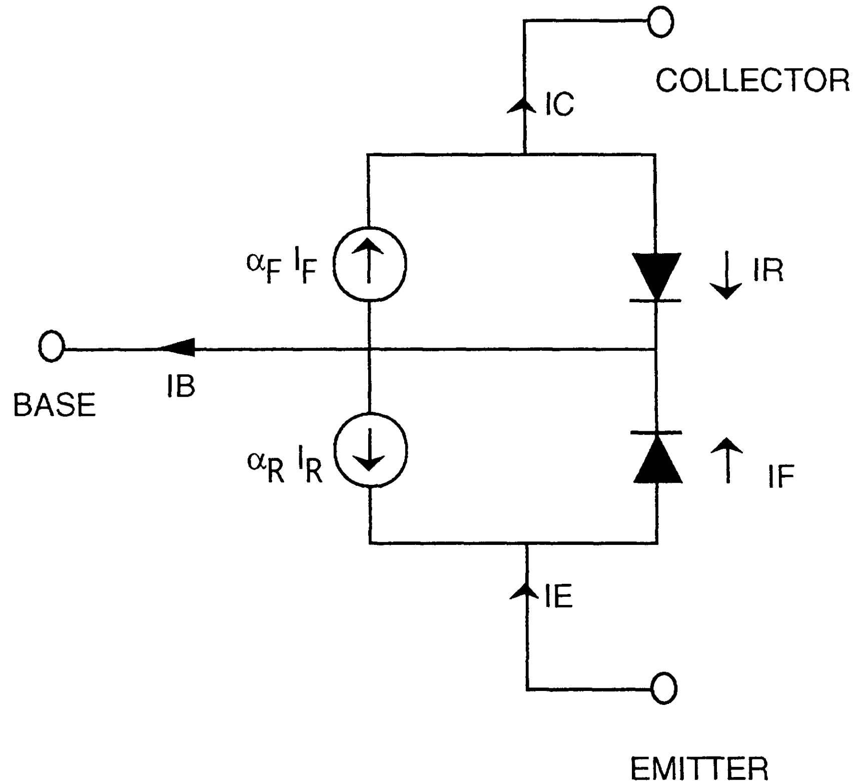

FIGURE 3.3 Ebers-Moll Injection Model

Using these results and the equation given in Eqn 3.4 and 3.5, all of the variables used in Eqn 3.6-3.8 are easily defined. The model as shown uses two diodes to represent the emitter-base and collector-base junctions. The currents IF and IR represent the amount of current that is flowing in the device due to the base emitter and base collector junctions respectively if the opposite junction was replaced with a simple contact. The two current dependent current sources represent the interaction between the two junctions which in the physical realm is the base area.

Examining one of the operating regions (normal forward active region), it is clear that the model presents an accurate description of the device. In the active region, the base collector diode is essentially an open circuit. The diode can then be removed from the model. The current controlled current source that is left ($\alpha_F I_F$) models that amount of current collected by the collector. (Hopefully, if the device is working properly, this will be close to I_F!) This is a

basic but correct representation of transistor operation in the active region.

It is apparent from the model that four parameters need to be specified. However, a new constant can be defined to reduce the necessary amount to three.

$$\alpha_F I_{FO} = \alpha_R I_{RO} = I_S \quad (3.9)$$

The other two parameters α_R and α_F are usually expressed in the transport version of the EM1 model as β_R and β_F.

$$\beta_F = \frac{\alpha_F}{1-\alpha_F} \quad (3.10)$$

$$\beta_R = \frac{\alpha_R}{1-\alpha_R} \quad (3.11)$$

FIGURE 3.4 shows the modifications made that are made for the transport model.

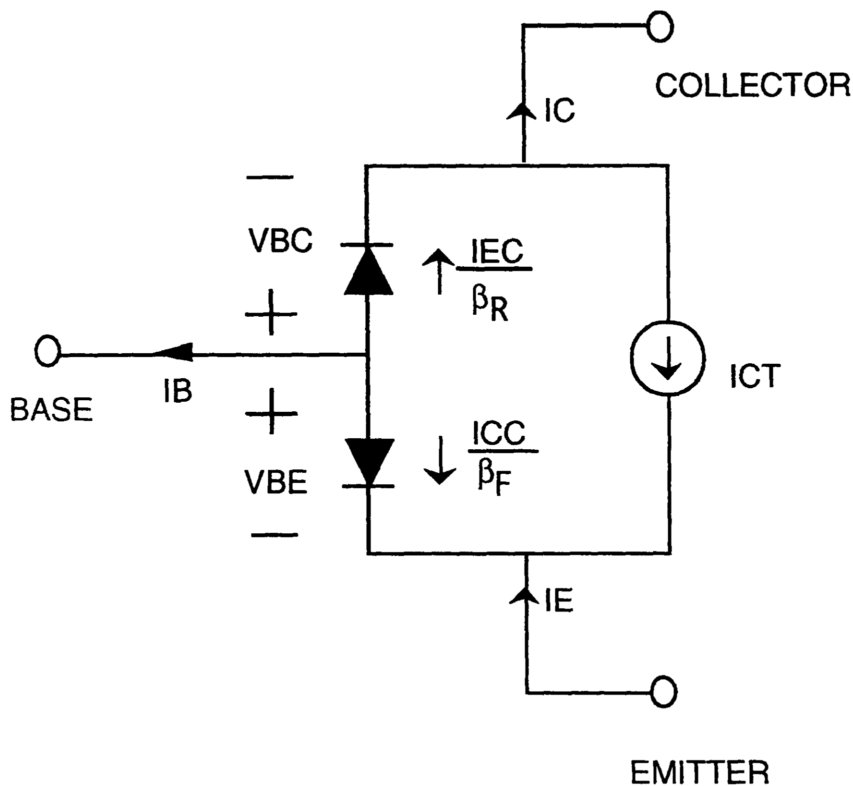

FIGURE 3.4 Ebers-Moll Transport Model

Finally, the EM1 model also includes a temperature variation coefficient for the saturation current, Eg. Consequently, this and TNOM must be specified to represent the effect temperature has on the saturation current. The saturation current dependence on temperature will be more thoroughly examined in CHAPTER 4.

The SPICE equations in the saturated region for the EM1 model (the region of operation for the bandgap) are:

$$I_C = I_S\left[\left(e^{qV_{BE}/kT} - e^{qV_{BC}/kT}\right) - \frac{1}{\beta_R}\left(e^{qV_{BC}/kT} - 1\right)\right] + \left[V_{BE} - \left(1 + \frac{1}{\beta_R}\right)V_{BC}\right]GMIN \tag{3.12}$$

$$I_B = I_S\left[\frac{1}{\beta_F}\left(e^{qV_{BE}/kT} - 1\right) + \frac{1}{\beta_R}\left(e^{qV_{BC}/kT} - 1\right)\right] + \left[\frac{V_{BE}}{\beta_F} + \frac{V_{BC}}{\beta_R}\right]GMIN \tag{3.13}$$

where GMIN is the conductance SPICE adds to each node to aid in convergence. (GMIN may be lowered to aid in convergence if that is a problem in simulations of larger circuits) [14]. FIGURES 3.5 and 3.6 show the effects of changing the parameters β_F and I_S. FIGURE 3.5 shows that an error in β_F will yield the incorrect bias current in a given branch. For the bandgap circuit this will cause a deviation in meeting the required bias for the minimum temperature coefficient.

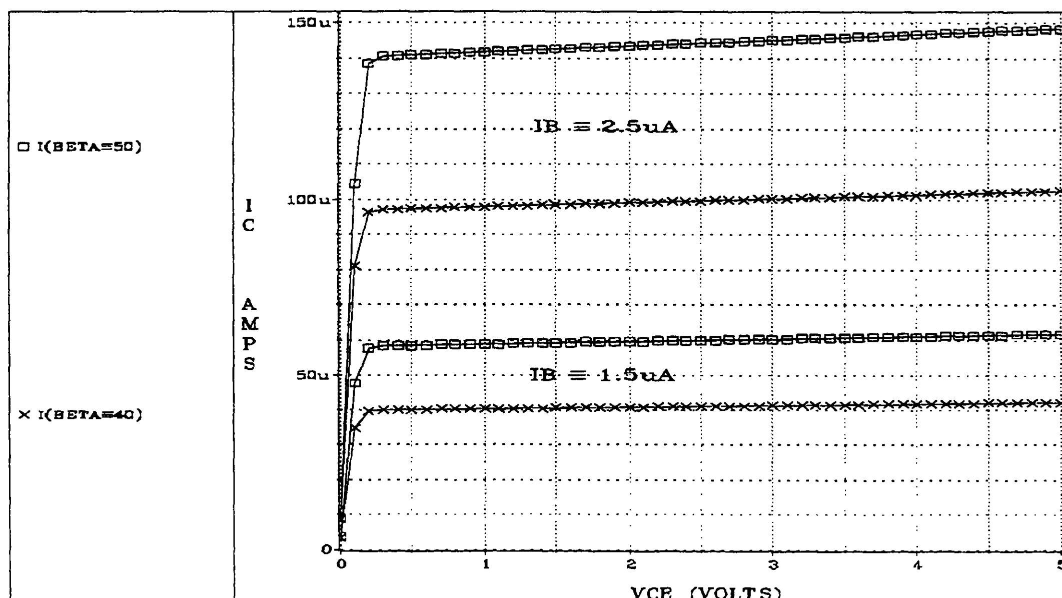

FIGURE 3.5 IC Variation with BETA

A change in the I_S parameter will not significantly affect the DC bias solution in the region where the bandgap operates. It will affect the location of the DC current at low VCE voltages.

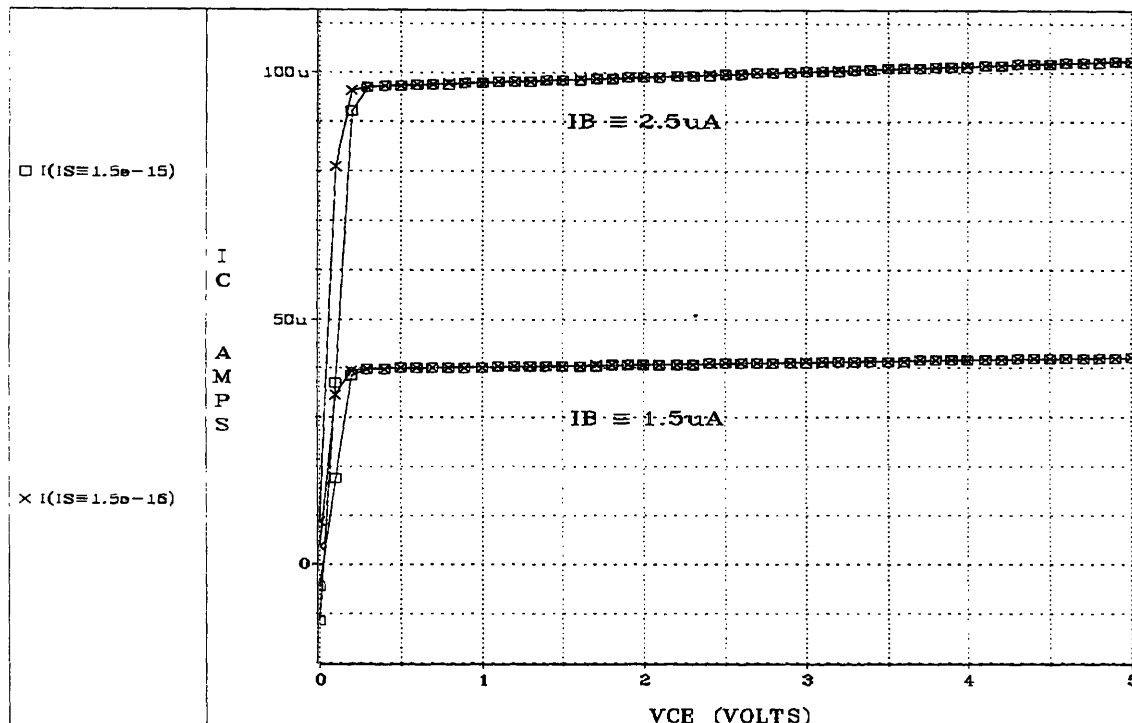

FIGURE 3.6 IC Variation with Is

3.4.2 EM2 Model (re, rb, rc)

The EM2 model begins to model the charge storage effects that the BJT device has limiting the frequency and time responses. In addition, it provides a more accurate model of the DC operation of the device. The charge storage effects (and parameters) will not be discussed as they do not enter into the bandgap equations [15].

The EM2 model incorporates the resistances seen at the three terminals into the device model (Rc, Re, and Rb). The collector resistance causes a decrease in the slope of the current in the saturated region of the device. The emitter resistance causes a reduction in the voltage seen by the base-emitter junction. In modern devices, the emitter is the most heavily doped region in the transistor. Consequently, the resistance seen is usually dominated by the contact resistance. The base resistance predominately

affects the small signal and transient responses. However, the combination of Re and Rb with the current in the base and emitter can cause a reduction in the collector current. The combination of the two effects presents a difficulty in measuring the base resistance. The effect in SPICE is a modification of the ideal model presented in the EM1 case. The modifications are shown in FIGURE 3.7.

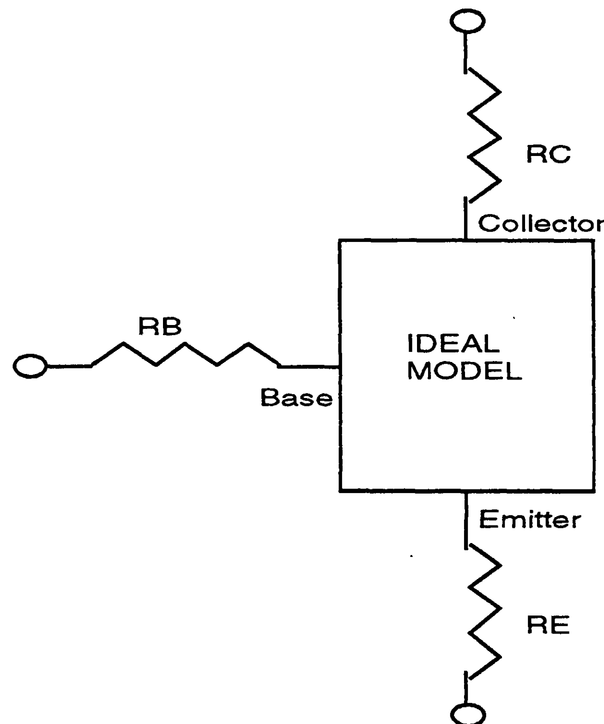

FIGURE 3.7 EM2 Model Changes

FIGURE 3.8 shows the effect of modifications to the parameter RC. It is apparent that an error in the RC parameter will not significantly affect the bias condition of the circuit. The values of RE and RB likewise do not significantly affect the DC bias case (with the small DC currents needed for the bandgap). A variation in RE will cause a small change in the base-emitter voltage. However, a factor of 4 change in the RE parameter only causes a 2mV shift. The same is true with the RB parameter where a factor of 2 change causes a 0.4 mV shift. This is not significant because a 2mV DC shift in the VBE voltage has no effect on the temperature coefficient of the output.

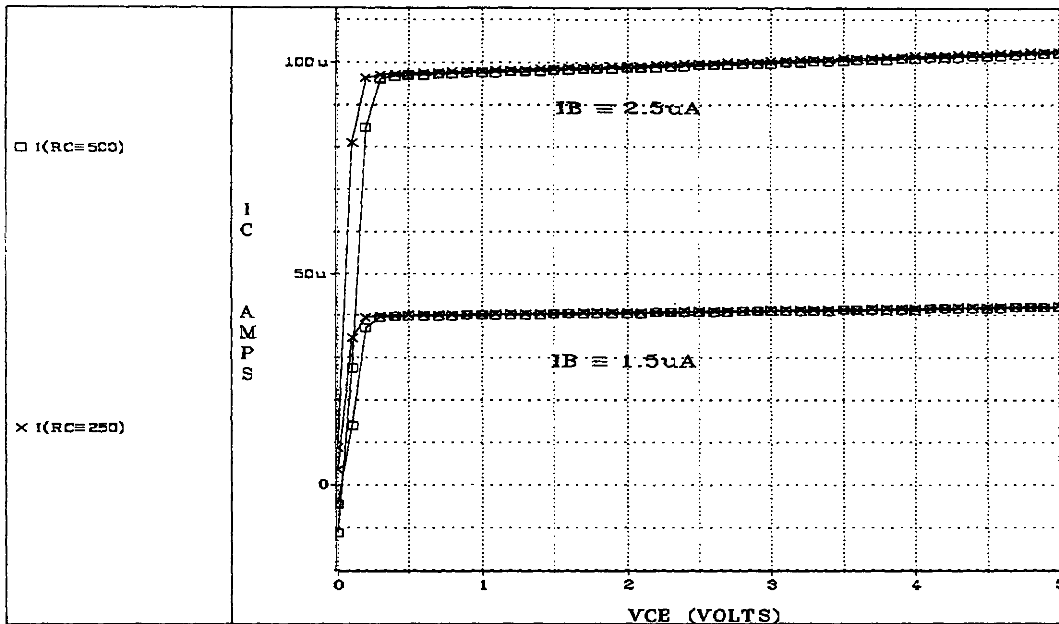

FIGURE 3.8 IC Variation with RC

3.4.3 EM3 Model (VA, nEL, nCL, ISE, ISC)

The EM3 model represents second order effects for dc operation, charge storage modeling, and temperature effects. The areas which affect the bandgap circuit simulation include:

(1) Base-width modulation and β_F variation with current and voltage

(2) Variation of device parameters with temperature.

Base width modulation (the "Early effect") is the resulting change in base width due to the applied collector base junction voltage. The width of the space charge region between the reverse biased collector base junction (assuming active operation) is very dependent on the applied voltage. The parameter VA is used to model this affect. The base width is also used in the computation of other parameters including β_F and I_S. Consequently, these values will now be a function of VCB as well. SPICE modifications are made as follows:

$$W_B(V_{BC}) = W_B(0)\left(1+\frac{V_{BC}}{V_A}\right) \tag{3.14}$$

$$I_S(V_{BC}) \cong I_S(0)\left(1+\frac{V_{BC}}{V_A}\right) \tag{3.15}$$

$$\beta_F(V_{BC}) \cong \beta_F(0)\left(1+\frac{V_{BC}}{V_A}\right) \tag{3.16}$$

There are three areas of interest when examining β_F variation with current: low current, mid current, and high current. In the mid current region, β_F as defined in the EM1 model still holds. It is now defined as β_{FM}. In the low current region, extra components of the base current which were ignored previously now cause a reduction in β. This is modeled with nEL, the low current forward region emission coefficient, and C2 (note that C2*I_S = ISE), a parameter which is used to fit the location of the base current when the applied VBE is zero volts. (SEE FIGURE 3.18) In the high current case, the injection of minority carriers into the base region is comparable to the level of majority carriers. This will cause a reduction in the slope of the collector current where the base-emitter junction is heavily forward biased. The parameter θ is used to model this slope as it gives the location of the asymptote of the collector current at zero VBE. Parameters are also given for the inverse area of operation. These parameters are nCL, C4 (note that C4*I_S = ISC), and θ_R. The modifications that these add to SPICE will be shown in the Gummel-Poon section.

For temperature variation, the model uses the following functional form to fit measurements with simulations:

$$F(T) = F(T_{NOM})\left[1 + TC_1(T - T_{NOM}) + TC_2(T - T_{NOM})^2\right] \tag{3.17}$$

This functional template is used for the parameters for β_F, Re, and Rc. Temperature variation plots will also be shown in the Gummel-Poon section. FIGURES 3.9-3.11 show the variation with parameters VAF, ISE, and NE respectively. FIGURE 3.9 shows that a variation in VAF will create an inaccurate estimate of the slope in the forward

active region. FIGURE 3.10 shows that a decrease in ISE will cause the entire forward curve to be pushed up. This will be caused by an inaccurate representation of the slope on the gummel plot. (FIGURES 3.17 and 3.18).

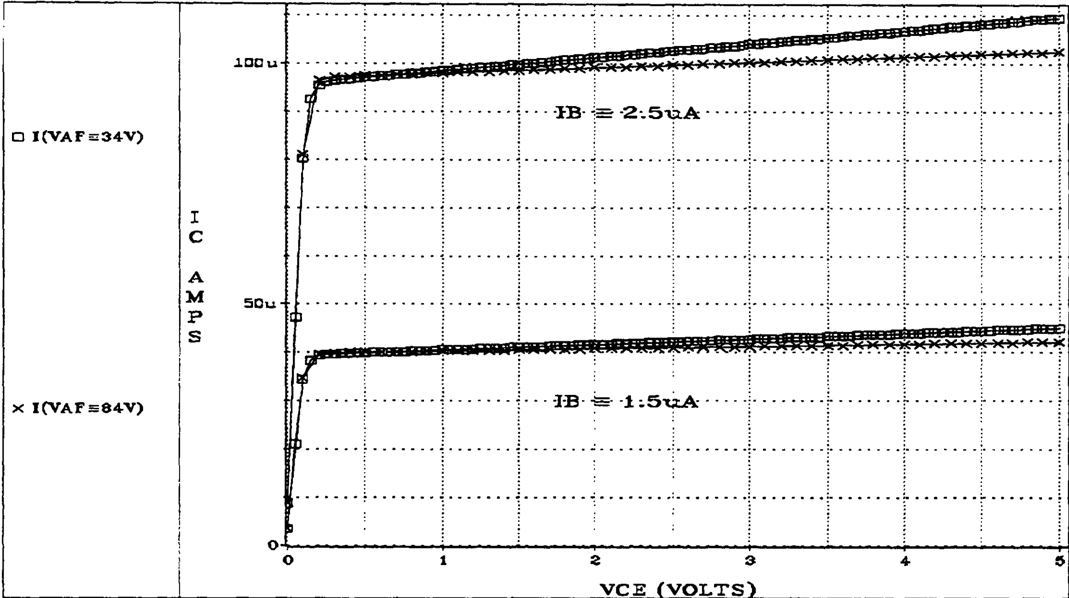

FIGURE 3.9 IC Variation with VAF (Early Voltage)

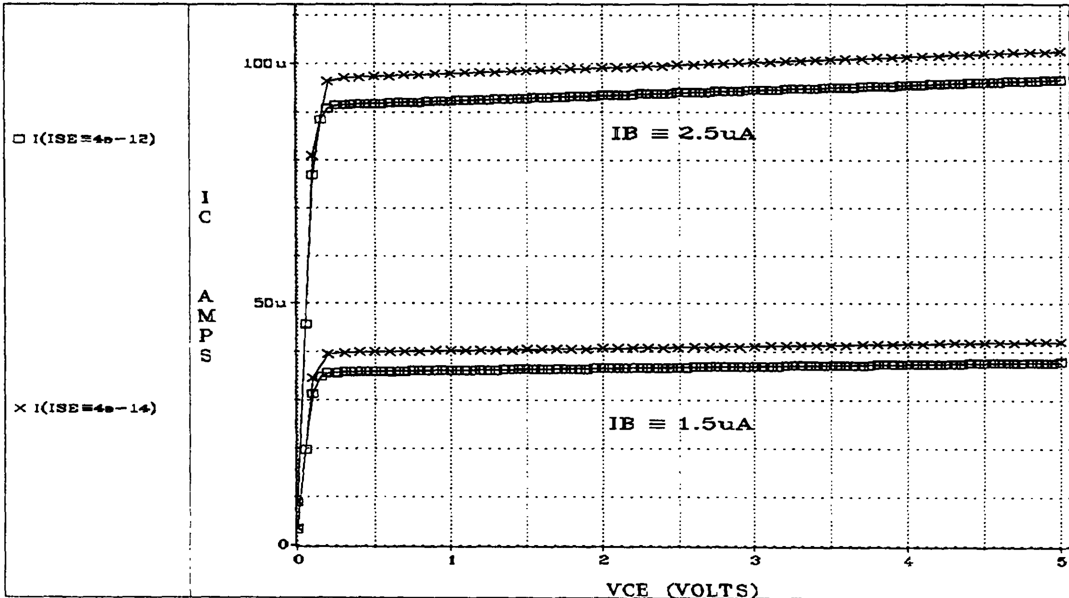

FIGURE 3.10 IC Variation with ISE (C2)

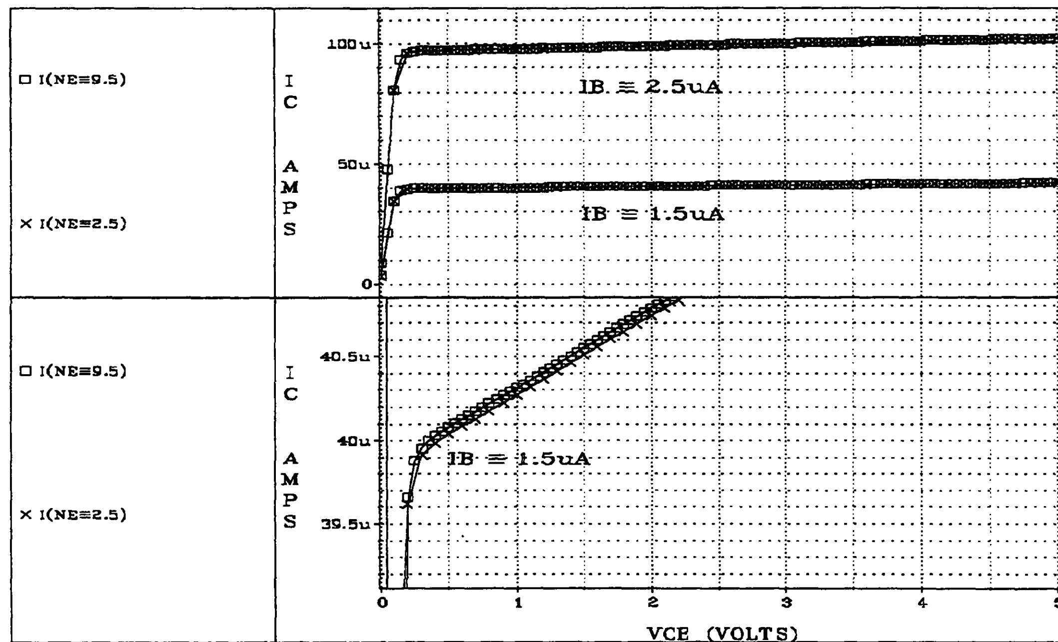

FIGURE 3.11 IC Variation with NE

3.5 Gummel-Poon Model (VB, IKF, IKR, XTB, XTI, NF, NR)

The Gummel-Poon model is similar to the EM3 model in that it attempts to provide better dc modeling with the inclusion of second order effects [9] [15]. Most of the parameters used in EM1-3 models apply to the Gummel-Poon model. The model is more concise but less intuitive than the EM3 model. It is designed for simulation in that the equations used to describe the transistor's operation are kept to a minimum. The Gummel-Poon model provides the following additions to BJT modeling:

- a complete description of basewidth modulation
- the effects of high-level injection
- a new derivation and description of the saturation current
- new temperature dependence relationships for β, Eg, ISE, and ISC
- accurate modeling of the exponential factor of collector current through NF and NR

The Gummel-Poon model defines knee currents to describe high level injection (rather than θ as in EM3). The forward active parameter, IKF, is shown in FIGURE 3.18. The parameter IKR will be the same except in the reverse active region. The Gummel-Poon

model also includes an inverse early voltage VB to describe operation in the reverse active region. Finally, the parameters NF and NR model the exponential collector current dependence. It is seen in FIGURE 3.18 that the parameter NF specifies the slope of IC vs. VBE line. NR measures the same slope in the reverse active region. The new modified SPICE equations in the saturation region are as follows [9]:

$$I_C = \frac{I_S}{q_b}\left[\left(e^{qV_{BE}/n_F kT} - e^{qV_{BC}/n_R kT}\right) - \frac{q_b}{\beta_R}\left(e^{qV_{BC}/n_R kT} - 1\right)\right] - C_4 I_S\left(e^{qV_{BC}/n_{CL} kT} - 1\right) + \left[\frac{V_{BE}}{q_b} - \left(\frac{1}{q_b} + \frac{1}{\beta_R}\right)V_{BC}\right]GMIN \tag{3.18}$$

$$I_B = I_S\left[\frac{1}{\beta_F}\left(e^{qV_{BE}/n_F kT} - 1\right) + \frac{1}{\beta_R}\left(e^{qV_{BC}/n_R kT} - 1\right)\right] + C_2 I_S\left(e^{qV_{BE}/n_{EL} kT} - 1\right) + C_4 I_S\left(e^{qV_{BC}/n_{CL} kT} - 1\right) + \left[\frac{V_{BE}}{\beta_F} + \frac{V_{BC}}{\beta_R}\right]GMIN \tag{3.19}$$

FIGURE 3.12 shows the effect of an increase in the parameter IKF. Larger base currents show a more pronounced difference.

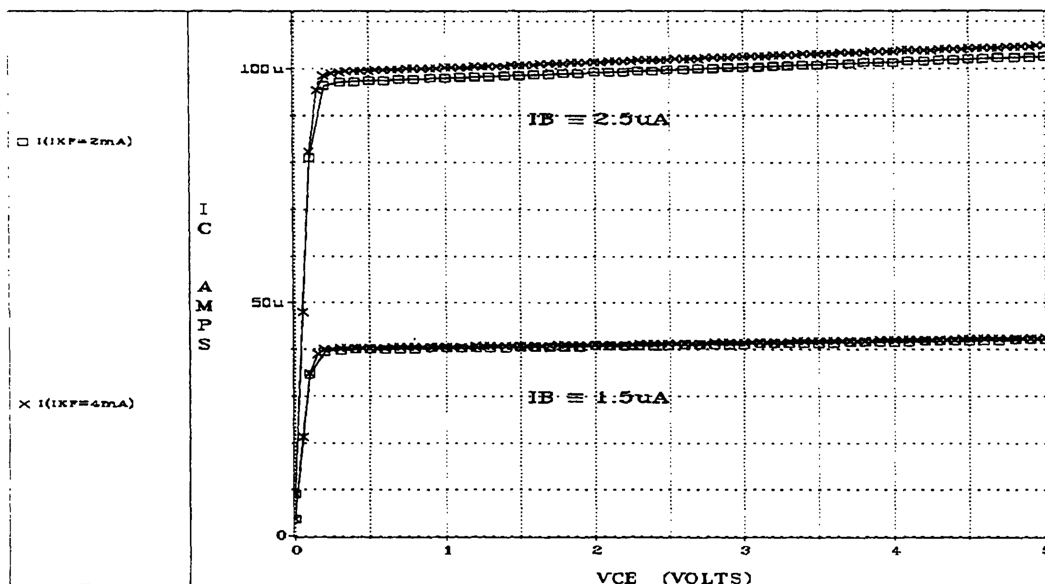

FIGURE 3.12 IC Variation with IKF

It is important to note that a small variation in the parameter NF will cause a large change in the base-emitter voltage despite having little affect on the forward collector curves as exemplified in FIGURE 3.13. As TABLE 3.2 shows, a variation of 5% will cause a 40 mV change in the absolute value of the base emitter voltage. This variation will cause a large discrepancy in the output voltage of the bandgap circuit.

	VBE@ -40	VBE@ +20	VBE@ +80
NF= 0.97	0.8044	0.6912	0.5749
NF=1.02	0.8456	0.7266	0.6043

TABLE 3.2 VBE Variation with NF

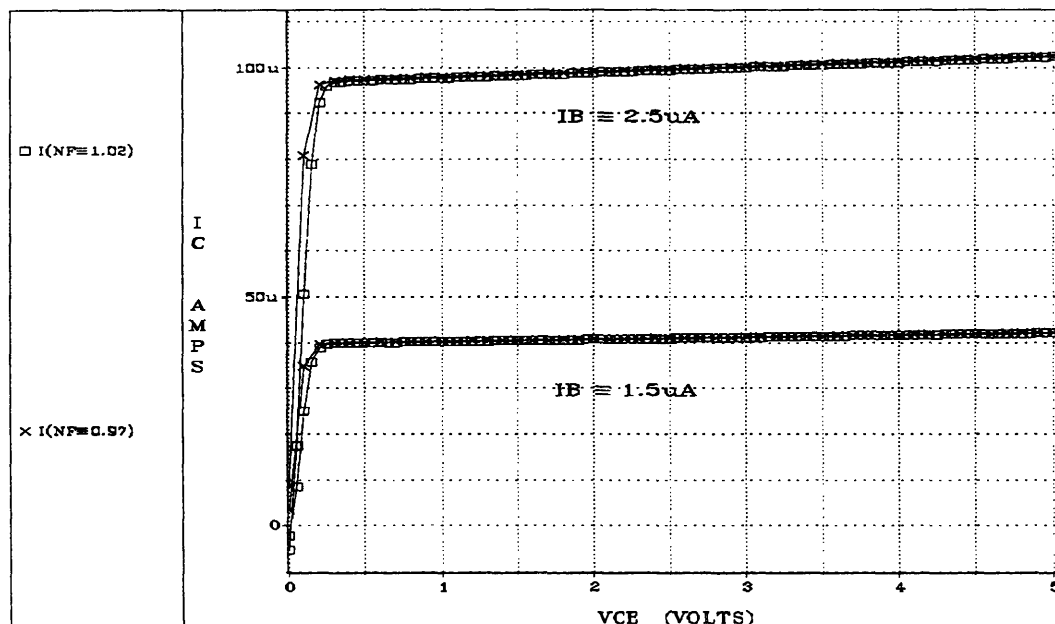

FIGURE 3.13 IC Variation with NF

Finally, rather than using a quadratic form to fit the temperature variation in the parameter β, the Gummel-Poon model uses the following relationship:

$$\beta_F(T_2) = \beta_F(T_1)\left(\frac{T_2}{T_1}\right)^{X_{T\beta}} \tag{3.20}$$

The parameters ISE and ISC also have similar temperature relationships. Looking at ISE:

$$I_{SE}(T_2) = I_{SE}(T_1)\left(\frac{T_2}{T_1}\right)^{-X_{T\beta}}\left[\frac{I_S(T_2)}{I_S(T_1)}\right]^{1/n_{EL}} \tag{3.21}$$

FIGURES 3.14-3.16 show the measured and simulated parameters β_F, ISE, and I_S over temperature. FIGURE 3.14 shows that the simulated and measured parameter β_F match fairly well thus justifying the exponential relationship specified in Eqn 3.20. The other two parameters, ISE and I_S, were not as accurately modeled. The problem lies in the extraction process for the extreme temperatures. Using the parameters extracted from room temperature data, I allowed the optimizer to fit the room temperature parameters to *all* measured data including data from temperature extremes. Unfortunately, the SANCAD solutions did not provide any of the expected variance in the parameters for ISE or IS. Although the model fits the data at the extreme temperatures, a better model could be attained by graphically measuring starting points for all parameters at all temperatures of interest. This would require hand measurements for parameter extraction at each temperature increment (20 degree steps). These parameters could then be used as the starting points for each temperature.

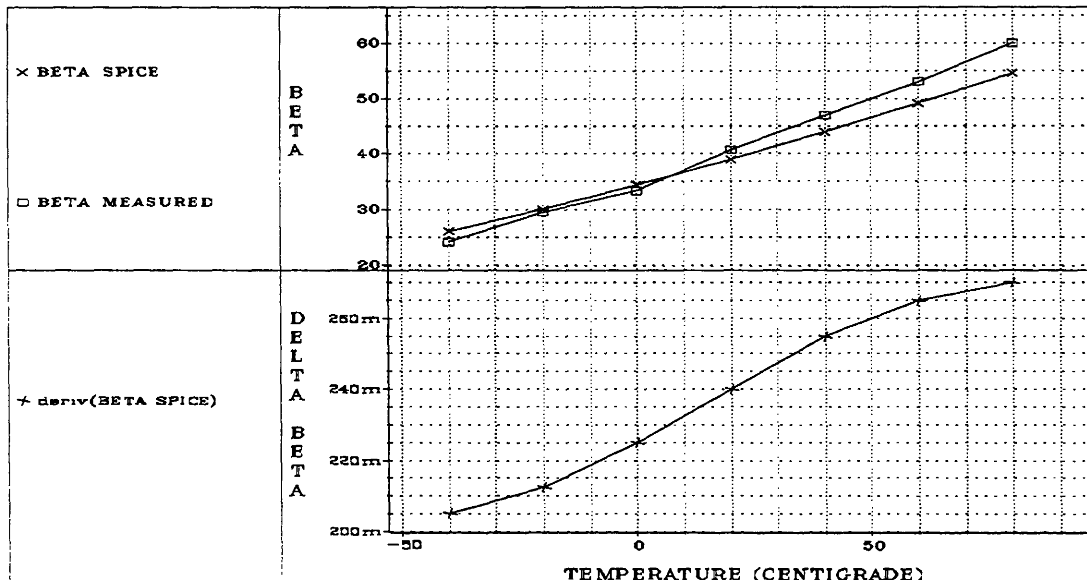

FIGURE 3.14 BETA Variation with Temperature

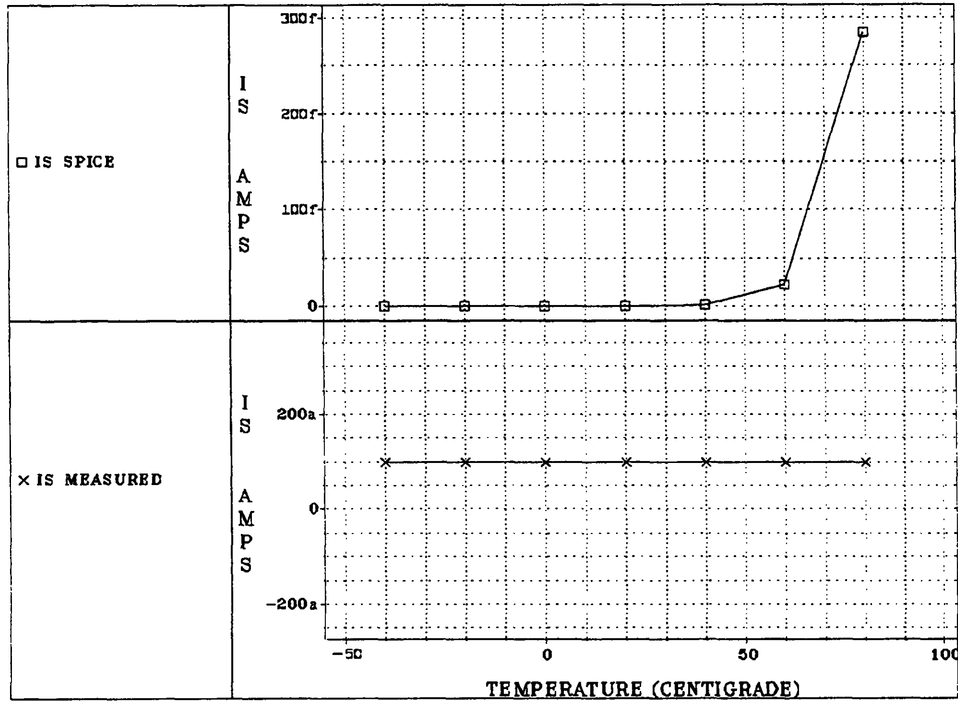

FIGURE 3.15 Is Variation with Temperature

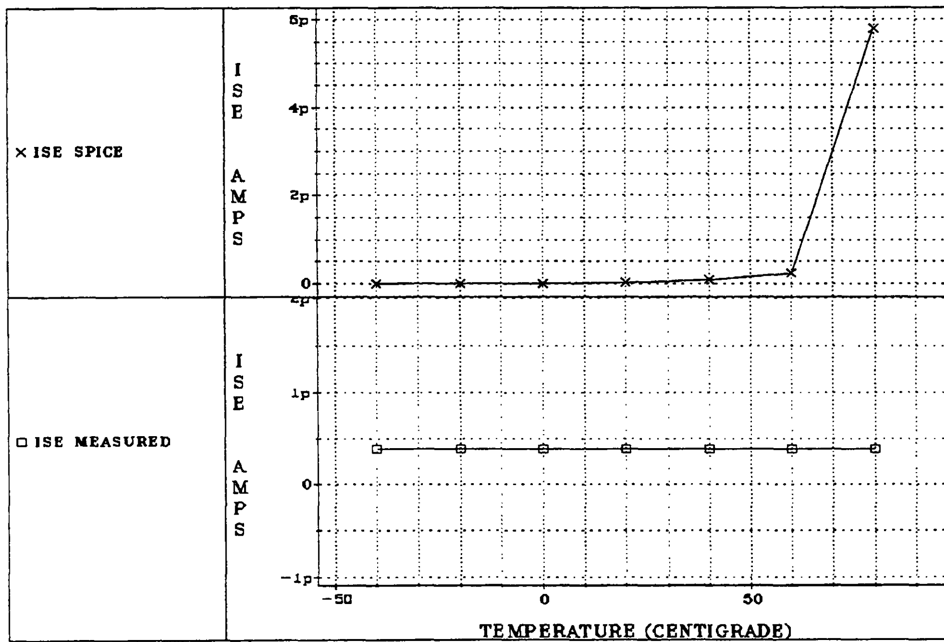

FIGURE 3.16 ISE Variation with Temperature

3.6 Bipolar Extraction

The approach taken for the bipolar parameter extraction differed from the MOS process. In the MOS process, I had hoped to

find an automated method which would produce a LEVEL 3 model. Data would be collected from the MOSFET under test and input into a program that would return a SPICE model. This data would consist of various data points from different configurations both in the linear and saturated region. Unfortunately, the combination of the time spent and the marginally adequate results proved that it would be more fruitful to take a more graphical approach. A graphical approach is an approach in which it is assumed that different presentations of data on a plot will yield various parameters for a device under test. There is a large body of literature that presents methods for graphically extracting parameters once the data has been obtained.

It was important to use the graphical method because ORBIT does not provide a model for parasitic bipolar devices. Consequently, the only information on these devices is the data collected in lab. Without any base parameters, it is more logical to obtain parameters from measured responses rather than from computer methods. At the very least, the designer can be sure that the models extracted will match the device they were taken from.

There are five tests that need to be run to obtain the primary DC parameters:

(1) Forward gummel plot (IKF, IS, ISE, BF, NF, RC)
(2) Reverse gummel plot (IKR, ISC, NR, NC, BR)
(3) Forward active curves (BF, VAF)
(4) Reverse active curves (BR, VAR)
(5) Re snap back plot (RE)

The device configurations for each of these tests is shown in FIGURE 3.17.

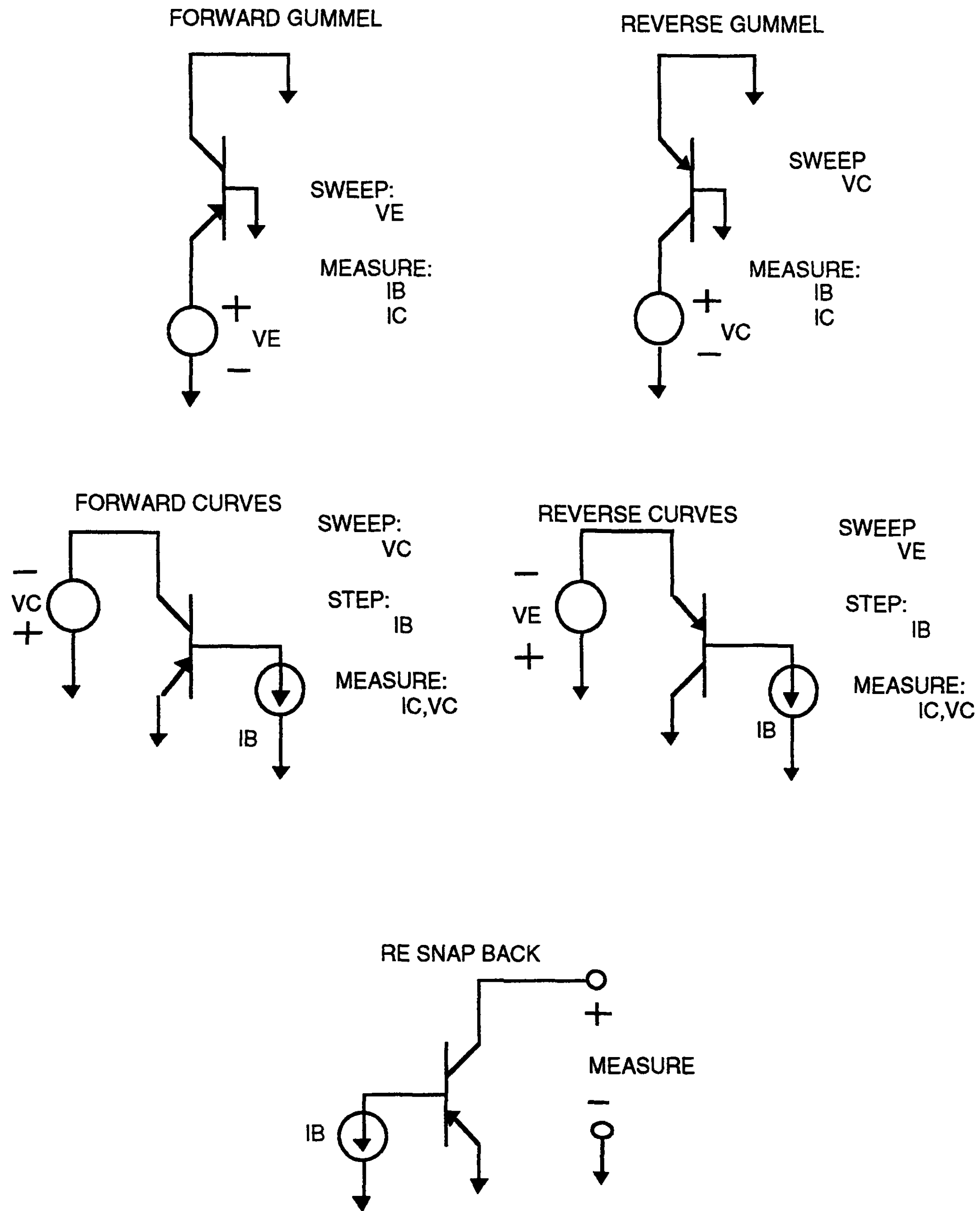

FIGURE 3.17 PNP BJT Extraction Test Setups

A sample plot of each test (excluding the reverse forward curves) is shown in FIGURES 3.18-3.21. The pertinent parameters that can be obtained are also shown on the plot for each test. These graphical parameters provide a starting point for the SANCAD optimizer. TABLE 3.3 shows the measured and optimized plots for a single bipolar transistor at 20 degrees C.

PARAMETER	MEASURED	OPTIMIZED
IS	1.0e-16	9.97e-17
BF	35.71	40.75
BR	6.5	6.5
IKF	0.002	0.002
ISE	3.0e-14	3.89e-14
ISC	N/A	5.0e-13
VAF	34	84.92
VAR	33.5	33.5
RC	392	395
RE	8.0	8.0
NF	2.5	2.50039
NR	1	1
NC	2	2
NE	2.5	2.5

TABLE 3.3 BJT Parameter Comparison

The actual parameters used in the bandgap simulation are plotted with the measured data in FIGURES 3.22-3.24. The parameters are shown for three temperatures: -40, 20, and 80 degrees C. As aforementioned, more accurate models could be obtained if a graphical solution for each temperature step were input to be optimized as opposed to using room temperature parameters as the starting point. Nevertheless, useful models for the bandgap circuit have been extracted providing enough information to give reasonable prediction (simulation) results as exemplified in FIGURES 3.22-3.24. The actual SPICE model used is presented in APPENDIX C with the MOS models.

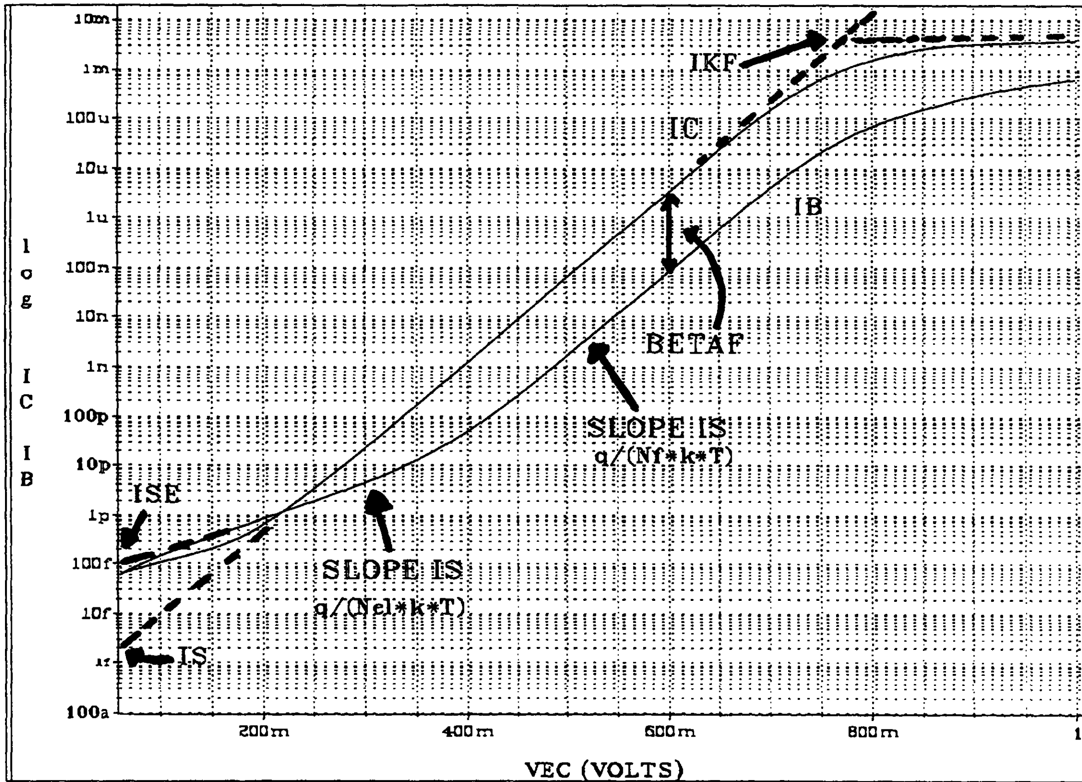

FIGURE 3.18 Forward Gummel Plot

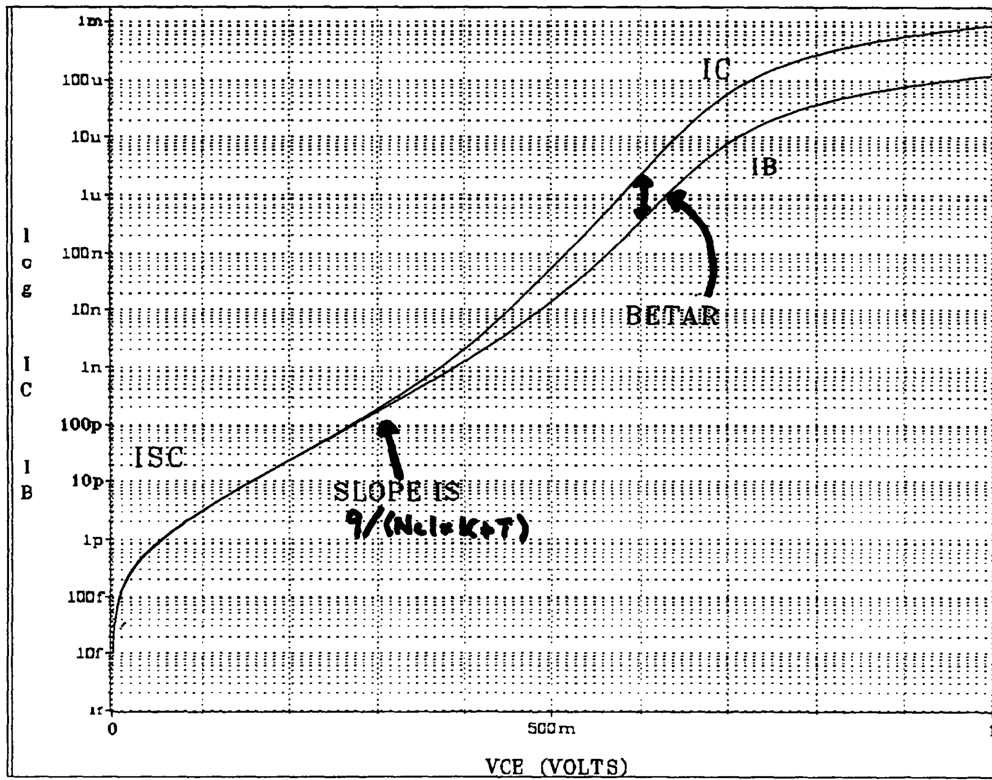

FIGURE 3.19 Reverse Gummel Plot

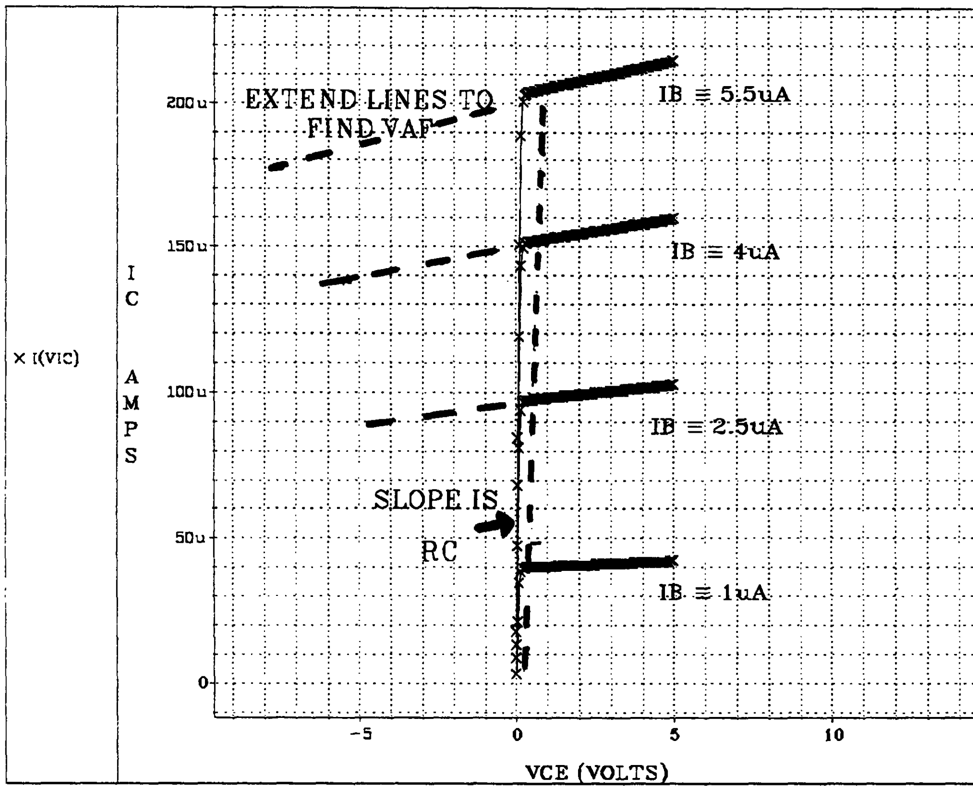

FIGURE 3.20 Forward Collector Curves

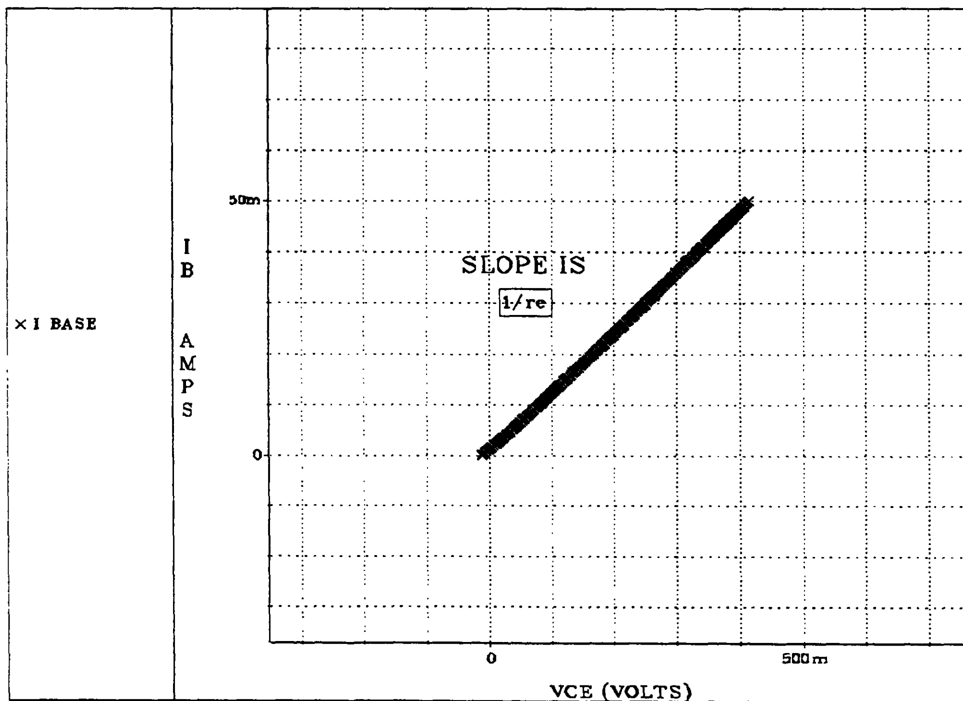

FIGURE 3.21 RE Snap Back Plot

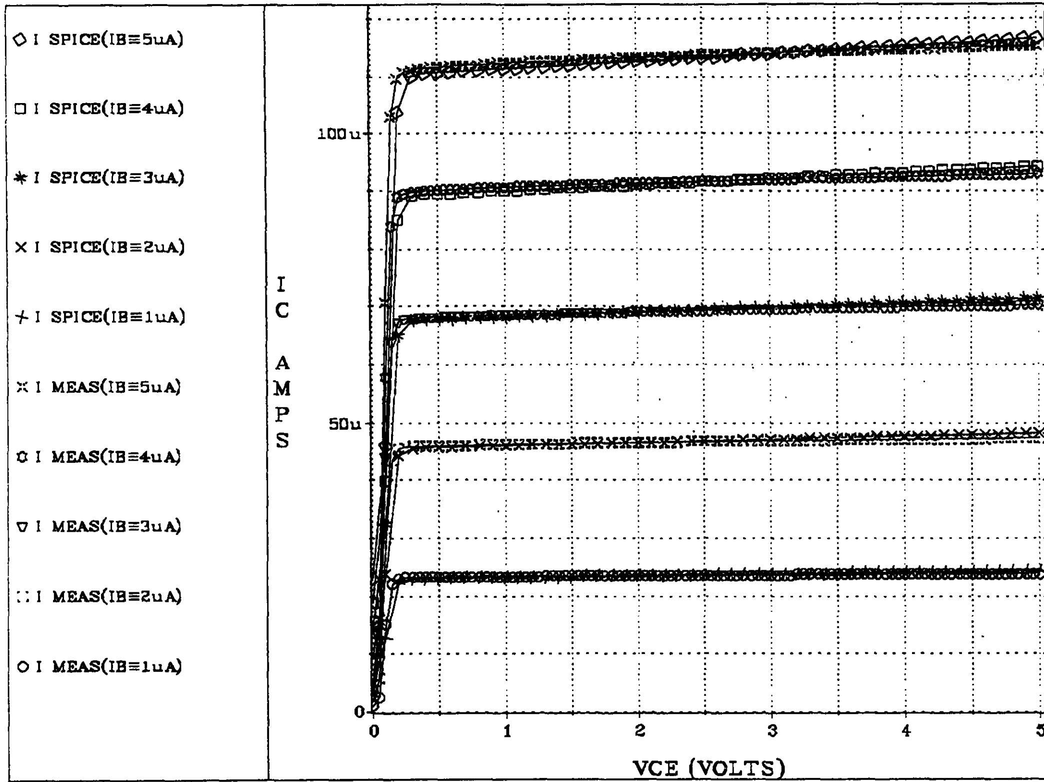

FIGURE 3.22 Model Comparison at -40 degrees C

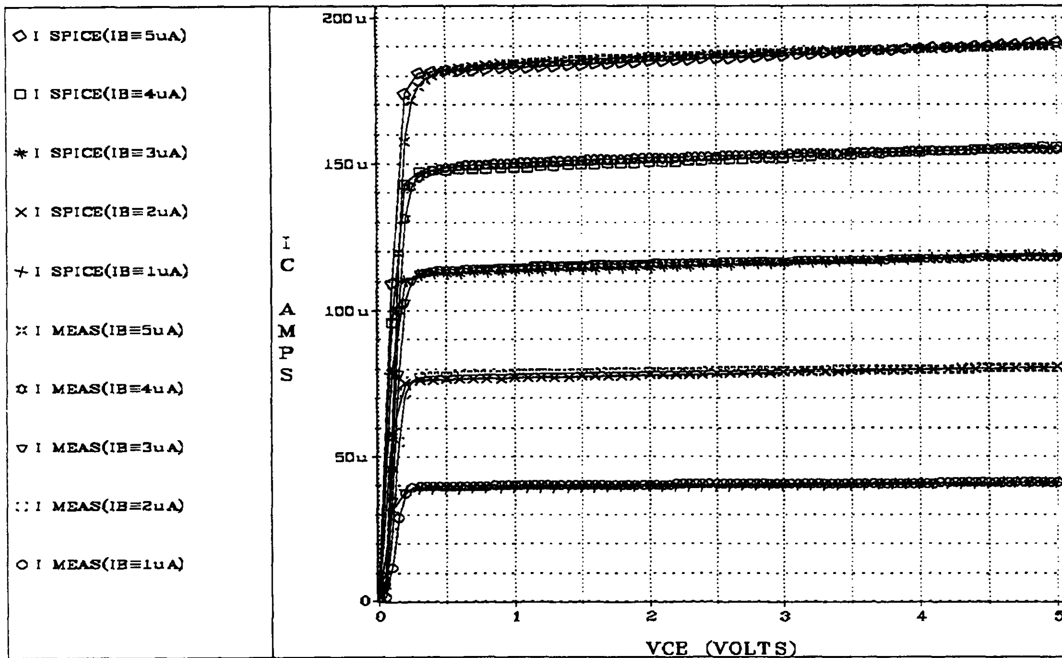

FIGURE 3.23 Model Comparison at +20 degrees C

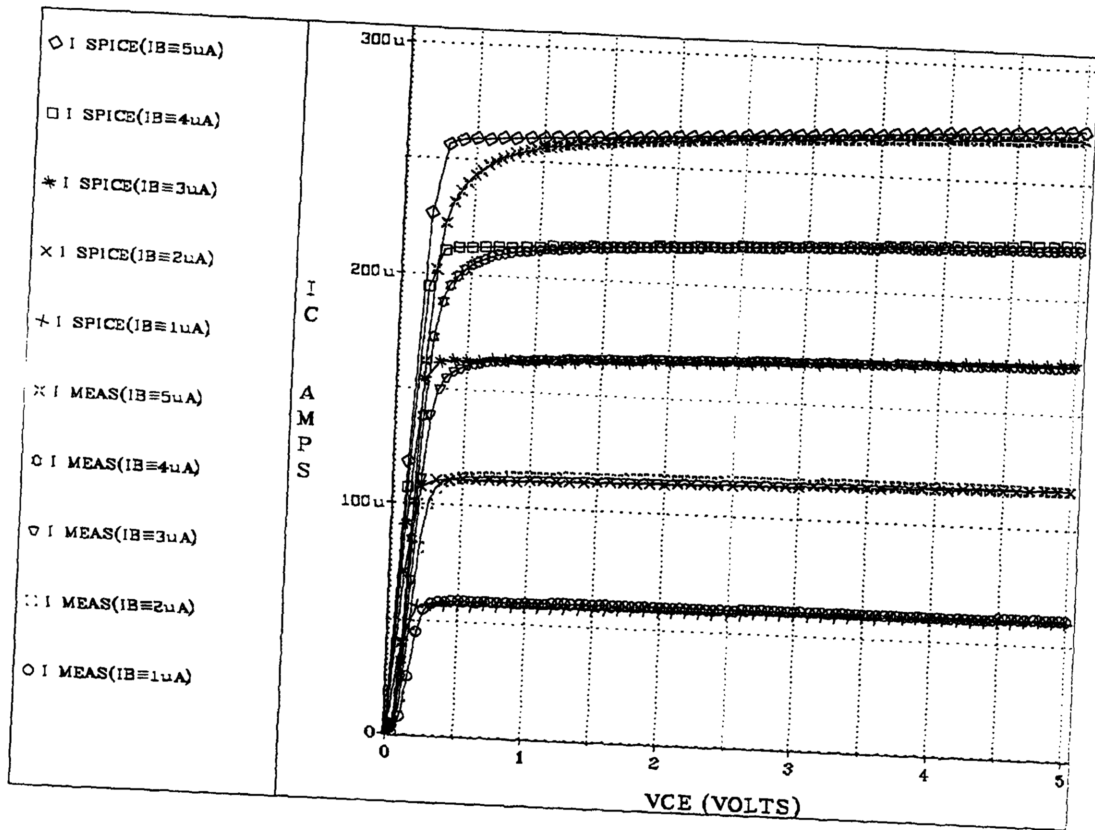

FIGURE 3.24 Model Comparison at +80 degrees C

4.0 BANDGAP

4.1 Bandgap basics

The bandgap circuit attempts to create a stable voltage over temperature by balancing a PTAT (proportional to absolute temperature) voltage with a base-emitter junction voltage (which has negative PTAT characteristics).

$$V_{OUT} = V_{BE} + KV_T \tag{4.1}$$

Essentially, the need is to create a negative temperature coefficient to cancel the positive coefficient introduced by the resistor from which the output voltage is taken. A simplified bandgap is shown in FIGURE 4.1 as a basis for analysis.

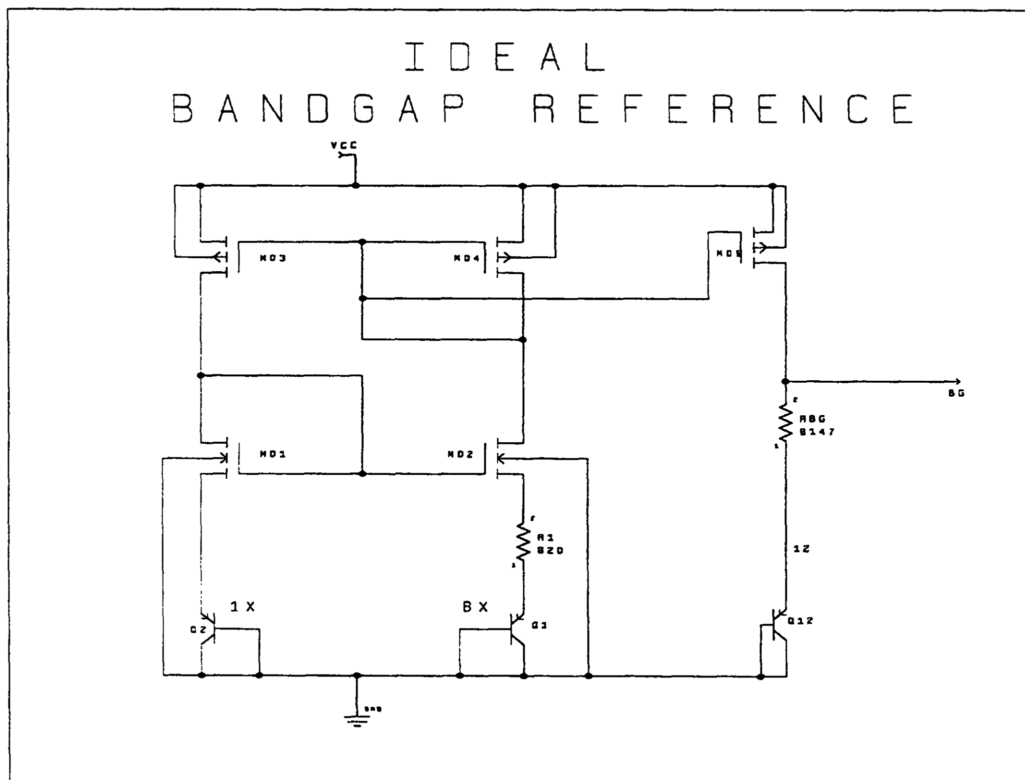

FIGURE 4.1 Ideal Bandgap Core

Assuming for the moment that there is a mechanism to provide current flow to the branch containing R1, an examination of the loop marked PTAT LOOP in FIGURE 4.1 shows that the voltage across the resistor R1 can be written as:

$$V_{R1} = (V_{BE1} - V_{BE2}) + (V_{GS1} - V_{GS2}) = \Delta V_{BE} - \Delta V_{GS} \tag{4.2}$$

This voltage will set the current in the branch consisting of R1, Q1, MO2, and M04. The current generated here is mirrored to the adjacent branch and the output branch consisting of RBG and Q12. The output VBG is seen to be given by the equation:

$$V_{BG} = \left(\frac{V_{R1}}{R_1}\right) R_{BG} + V_{BE3} \tag{4.3}$$

It is apparent that there are four distinct types of voltages that influence the bandgap output voltage: a V_{BE} voltage, a ΔV_{BE}, a ΔV_{GS}, and voltages across various resistances.

4.1.1 V_{BE} voltage

The voltage of a base-emitter junction that is on can be written as [16]:

$$V_{BE(on)} = V_T \ln\left(\frac{I_C}{I_S}\right) \tag{4.4}$$

The saturation current can be shown to be:

$$I_S = \frac{qAn_i^2 D_n}{Q_B} = Bn_i^2 T\mu_n \tag{4.5}$$

and the collector current is assumed to have temperature dependence:

$$I_C = GT^{\alpha} \tag{4.6}$$

where the variables included are:

A = emitter base junction area
μ_n = base region electron mobility

B = temperature independent constant
D_n = diffusion coefficient for electrons
n_i = intrinsic carrier concentration
Q_b = fixed base charge
α = constant for temperature dependence (1 for PTAT)

Using the relationships:

$$\mu_n = CT^{-n} \tag{4.7}$$

$$n_i^2 = D_n T^3 e^{\left(\frac{-V_{Go}}{V_T}\right)} \text{ and } \gamma=4-n \tag{4.8}$$

it can be shown that the base emitter voltage is:

$$V_{BE(on)} = V_{GO} - V_T((\gamma-\alpha)\ln T - \ln EG) \tag{4.9}$$

and

$$\frac{dV_{BE(on)}}{dT} = \frac{k}{q}[-(\gamma-\alpha)\ln T - (\gamma-\alpha) + \ln EG] \tag{4.10}$$

It is important to note that the base emitter voltage is not linearly dependent on T. In fact, as Eqn. 4.10 shows there is a -T*lnT dependence. The discouraging part of this information is that unless the resistor has the exact same temperature dependence in the positive direction, the bandgap curve will be bowed and must be designed for an optimal temperature. This optimal temperature is the point at which the bowed curve reaches its extrema where there is the least temperature dependence. This point is where:

$$\frac{\partial V_{BE}}{\partial T} = -\frac{\partial V_{RBG}}{\partial T} \tag{4.11}$$

Figure 4.2 exhibits the relationship specified in Eqn 4.11. Using an ideal current source to generate a PTAT current for the output branch and imposing typical resistance first and second order temperature coefficients, one can see the relationship between the output voltage and the derivatives (with respect to temperature) of the voltages from which the output is composed. (FIGURE 4.3 shows the generation of the ideal bandgap voltage.)

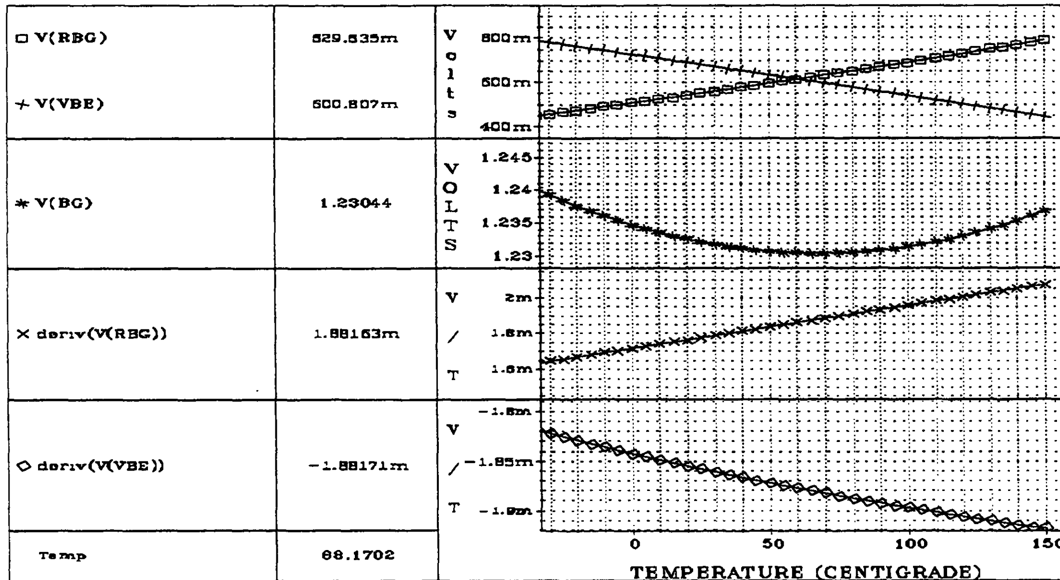

FIGURE 4.2 Ideal Bandgap Output

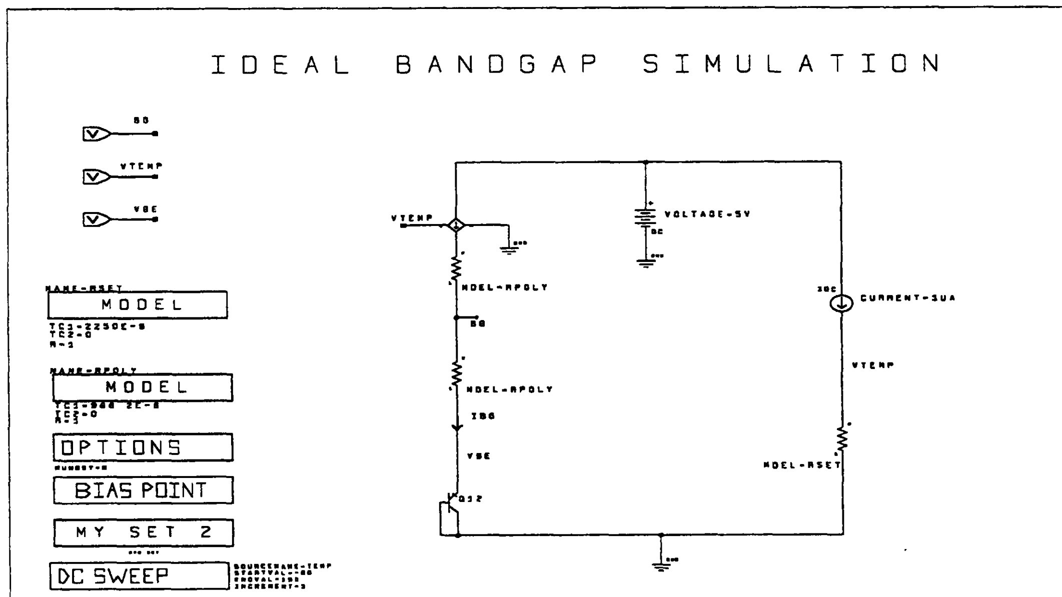

FIGURE 4.3 Circuit for Ideal Bandgap Simulation

SPICE generation of the V_{BE} voltage is embedded in the solution it finds for the collector current in a BJT. A look at the parameters involved will provide insight into what parameters might be varied to match a measured result. For a diode connected BJT (the case used in the bandgap circuit), V_{CB} is equal to zero. Consequently, SPICE is left with the following equation to provide an accurate collector current:

$$I_C = \frac{I_S\left(e^{V_{BE}/NF \bullet VT} - 1\right)}{0.5\left(\frac{1}{1-\frac{V_{BE}}{VAR}}\right)\left(1+\left(1+4\left(\frac{I_S\left(e^{V_{BE}/NF \bullet VT}-1\right)}{IKF}\right)\right)^{1/2}\right)} \qquad (4.12)$$

SPICE parameters IS, NF, VAR, and IKF in addition to the VBE voltage are the only variables which will affect the value of IC [14]. FIGURE 4.4 shows the measured and simulated results including the derivative with respect to temperature of the responses. A small DC offset in FIGURE 4.4 causes the simulated voltage to be higher than the measured case. However, it appears that the extracted model has done an accurate job of representing the base emitter junction. The derivative of the simulated junction shows the negative -T*lnT dependence. The measured derivative is inconclusive most likely due to the combination of too few samples and the inability to keep the temperature exactly stable.

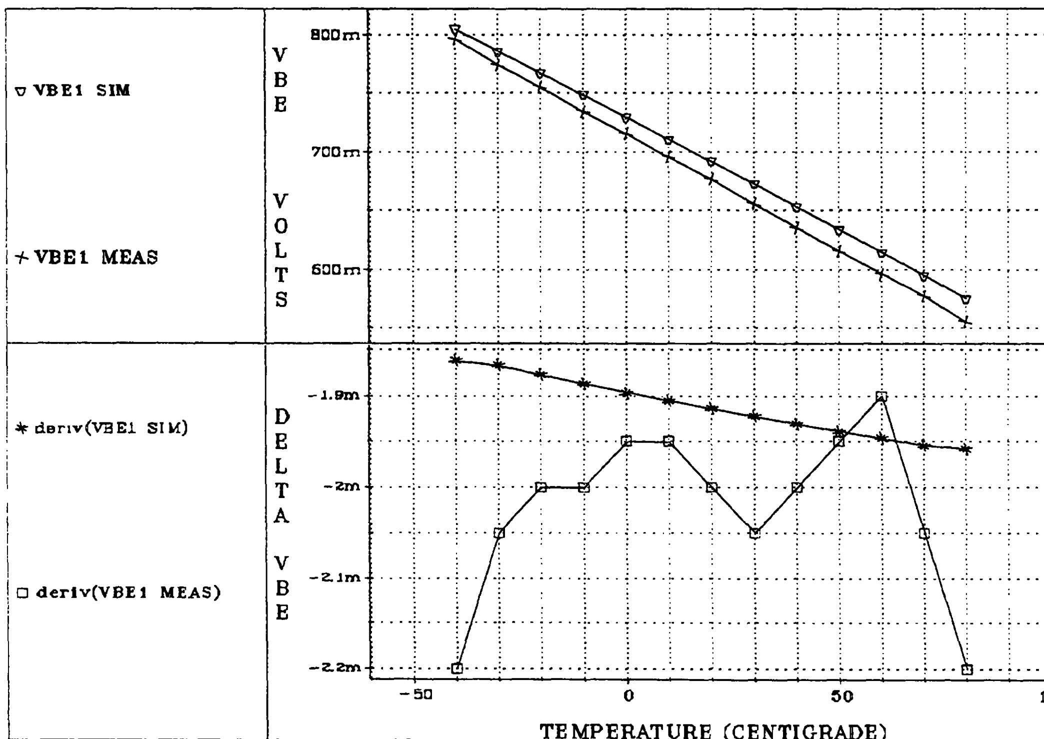

FIGURE 4.4 VBE Variation with Temperature

4.1.2 ΔV_{BE}

Using Eqn. 4.5, one notes that the saturation current is proportional to the area of the base emitter junction. Consequently, if there are two branches with equal current and scaled areas as in FIGURE 4.1, the difference between the two base emitter voltages can be written as:

$$\Delta V_{BE} = V_T \ln\left(\frac{A_8}{A_1}\right) \qquad (4.13)$$

where the A's represent the area of the transistor base emitter junctions. Unlike the actual base emitter voltage, the difference between two base emitter voltages is PTAT. One would imagine the derivative of the ΔV_{BE} with respect to temperature to be constant and small due to all first order temperature effects falling out in the difference. FIGURE 4.5 shows that there is a slight quadratic term in the simulation value of ΔV_{BE}. This may be due to slight differences in the temperature coefficients of the mobility or the intrinsic carrier concentration. However, the change over 200 degrees in the derivative is only 2uV. Consequently, the nonlinear term can be ignored. FIGURE 4.5 shows the measured and simulated ΔV_{BE} responses. Due to the inability to measure both transistors at the same time, the measured response appears piece wise in comparison with the SPICE result.

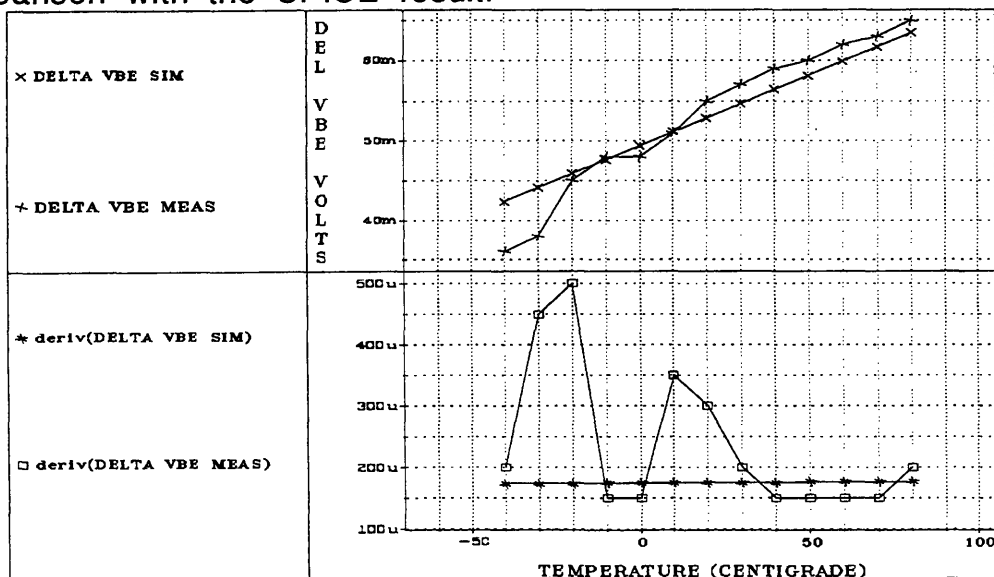

FIGURE 4.5 DELTA VBE Variation with Temperature

4.1.3 Δ VGS

Using a LEVEL 1 approximation for the current in the MOSFETs in each branch [17]:

$$I_{MO1} = \frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)_1 \left(V_{GS1} - V_{TH_N}\right)^2 \left(1+\lambda V_{DS1}\right) = I_{M03} = \frac{\mu_p C_{OX}}{2}\left(\frac{W}{L}\right)_3 \left(V_{SG3} - V_{TH_P}\right)^2 \left(1+\lambda V_{SD3}\right) \quad (4.14)$$

$$I_{MO2} = \frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)_2 \left(V_{GS2} - V_{TH_N}\right)^2 \left(1+\lambda V_{DS2}\right) = I_{M04} = \frac{\mu_p C_{OX}}{2}\left(\frac{W}{L}\right)_4 \left(V_{SG4} - V_{TH_P}\right)^2 \left(1+\lambda V_{SD4}\right) \quad (4.15)$$

Neglecting the Δ V_{GS} of mirror transistors MO3 and MO4 and using the assumptions that :

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 \quad \text{and} \quad \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 \quad (4.16)$$

Solving these equations yields:

$$\Delta V_{GS} = \left(\frac{2I_{M01}}{\mu_n C_{OX}\left(\frac{W}{L}\right)_1}\right)^{\frac{1}{2}} \left(\left(1+\lambda_n V_{DS2}\right)+\left(1+\lambda_p V_{DS4}\right)\right)^{\frac{1}{2}} - \left(\left(1+\lambda_n V_{DS1}\right)+\left(1+\lambda_p V_{DS3}\right)\right)^{\frac{1}{2}} \quad (4.17)$$

Assuming that $\lambda_X V_{DS_{XX}} << 1$, (using a typical value for λ, the term is 0.02) this may be simplified to yield:

$$\Delta V_{GS} = \left(\lambda_p (V_{SD4} - V_{SD3}) + \lambda_n (V_{DS1} - V_{DS2})\right)\left(\Delta V_{BE} + \Delta V_{GS}\right)^{\frac{1}{2}} \left(K \mu_n R_1\right)^{-\frac{1}{2}} \quad (4.18)$$

Finally, letting the temperature independent parameters be represented by C, assuming that Δ V_{BE} >> Δ V_{GS} and using the following temperature relations from [17] and [18]:

$$\mu_p = \mu_O T^{-2.42} \quad \text{and} \quad R_1 = R_O T^{0.1} \quad (4.19)$$

A useful equation for the change in gate source voltage is:

$$\Delta V_{GS} = CT^n \qquad \text{where n is approximately 1.5} \qquad (4.20)$$

FIGURE 4.6 shows the simulated ΔV_{GS} as a measured response could not be accessed. The plot appears to show that within the region of interest (-40 to 85 degrees C) ΔV_{GS} is approximately linear. Only at higher temperatures does the response become nonlinear. Consequently, this term may be ignored on a first order level.

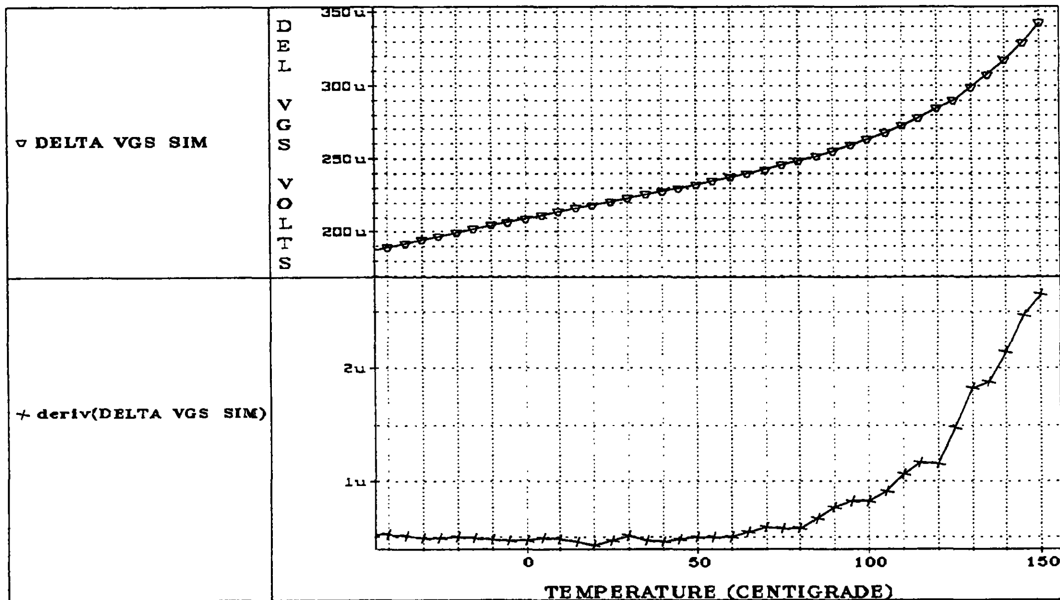

FIGURE 4.6 DELTA VGS Variation with Temperature

4.1.4 Polysilicon Resistors

Polysilicon resistors were used for both R1 and RBG in the bandgap circuitry. Typically, polysilicon resistors exhibit a temperature coefficient that is near 1000ppm/C. However, the ratio is much better when two resistors are matched (20 ppm/C). Unfortunately, the design rules and process descriptions usually do not give these values. It would be useful to have an accurate SPICE model from the foundry which contained both linear and quadratic temperature dependent terms. In addition, the specifications given by the foundry are usually in the form of a minimum, a typical, and a maximum value in ohms per square. (The Orbit specifications for the 1.2 micron process list these values at 15, 24, and 30 ohms per

square respectively.) Unfortunately, the bandgap circuit needs very accurate resistors (the variation of output voltage with resistance values will be presented later).

SPICE models the resistor with two temperature coefficients:

$$R(T) = R_O \bullet R \bullet (1 + TC1(T - T_{NOM}) + TC2(T - T_{NOM})^2) \quad (4.21)$$

where R is a multiplicative factor

Using Matlab, measured data can be fit to a polynomial form in order to extract the relevant parameters. Using one of the resistors on the chip, the following parameters were extracted for the polysilicon resistors in the Orbit 1.2 micron process:

FOR TNOM = 20 degrees and Ro = 36.870 kΩ

TC1 = 966.2E-06

TC2 = 8.07E-08

FIGURE 4.7 shows the measured and simulated resistance values for one of the bandgap resistors. As the plot shows, the difference between the two is at most 0.1%.

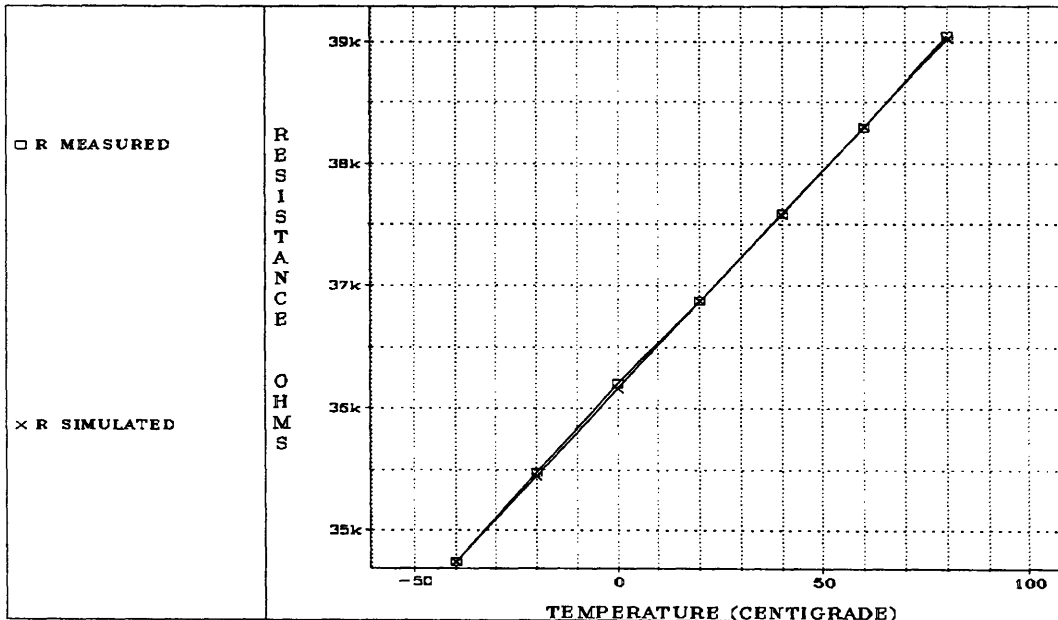

FIGURE 4.7 Resistor Modeling

Another problem that exists with polysilicon resistors is the variation of temperature coefficients both across a single wafer and

between different wafers. (Thus presenting the difficulty of choosing the correct temperature coefficients for simulations.) TABLES 4.1 and 4.2 shows the variation in temperature coefficients for differing values of resistance and for different packaged parts. The problems that these variations as well as variations in the absolute value of the resistors introduce will be explored later in this chapter.

Resistance Value	(CHIP A) R1 @To = 7819.0	(CHIP A) R2 @To = 1014.6	(CHIP A) R3 @To = 36950	(CHIP A) R4 @To = 484.7	(CHIP A) R5 @To = 473.6
TC1	943.0e-6	949.8e-6	966.0e-6	1111e-6	1143e-6
TC2	78.0e-8	87.9e-8	60.4e-8	49.1e-8	44.0e-8

TABLE 4.1 TC Values CHIP A

Resistance Vakue	(CHIP B) R1 @To = 7671.0	(CHIP B) R2 @To = 998.9	(CHIP B) R3 @To = 36320
TC1	971.6e-6	975.5e-6	972.0e-6
TC2	55.0e-8	49.8e-8	46.7e-8

TABLE 4.2 TC Values CHIP B

4.2 The Ideal Bandgap Output Voltage

Typically, a bandgap reference is designed such that at a certain temperature, there will be zero temperature coefficient. Assuming that our bandgap voltage is comprised of a V_{BE} voltage and a PTAT term, V_{out} may be written as:

$$V_{BG} = V_{OUT} = V_{GO} - V_T(\gamma - \alpha)\ln T + V_T(K + \ln EG) \qquad (4.22)$$

where K is the PTAT multiplier used in the summation of a V_{BE} voltage and a PTAT voltage. (Eqn 4.1)

E is the temperature independent factor of the intrinsic carrier concentration and electron mobility (Eqns 4.7 & 4.8)

G is the temperature independent term of the collector current in the BJT (Eqn 4.6)

Vgo is the band-gap voltage of silicon extrapolated to zero degree Kelvin

In order for the temperature coefficient to be zero:

$$\frac{dV_{OUT}}{dT}\bigg|_{T=T_O} = 0 = \frac{V_{TO}}{T_O}(K + \ln EG) - \frac{V_{TO}}{T_O}(\gamma - \alpha)\ln T_O - \frac{V_{TO}}{T_O}(\gamma - \alpha) \tag{4.23}$$

Using these two equations, it is seen that [16]:

$$V_{OUT}(T) = V_{GO} + V_T(\gamma - \alpha)\left(1 + \ln\frac{T_O}{T}\right) \tag{4.24}$$

This equation is extremely useful as it gives the output voltage in terms of one independent variable: the temperature. The value that is chosen for T_O (the point at which there is zero temperature coefficient) yields what the "magic" output voltage needs to be. The choice of T_O, given α and γ, is a function of the parameters K, E, and G which are the constants defined above. Typically, α will be close to one (a PTAT current source) and γ will be close to 1.6 (using the same mobility dependence expressed in Eqn 4.19).

Once To is chosen, the other parameters may be chosen to yield the correct Vout that was predicted by Eqn 4.24. Using Eqns 4.2, 4.3, and 4.6 (and assuming ideally that ΔV_{GS} is negligible), K and G can be seen to be:

$$K = \frac{R_{BG}}{R_1}\ln\left(\frac{A_8}{A_1}\right) \qquad G = \frac{k}{qR_1}\ln\left(\frac{A_8}{A_1}\right) \tag{4.25}$$

E is a parameter which theoretically involves topics in solid state physics that are outside the scope of this thesis. Using the relationship for μ_n given in Eqn 4.7 and the relationship for n_i given in Eqn 4.8, E is given by:

$$E = \frac{ACDk}{Q_B} \tag{4.26}$$

More insight into the components of the parameter E can be obtained in Sze's *Physics of Semiconductor Devices.* [18]. One way to avoid delving into the details of the parameter E is to measure a V_{BE} voltage and solve Eqn 4.9 for E. Using one of the parasitic bipolar transistors on the test chip, I was able to measure an accurate value of E. The definition of G highlights a key problem with the bandgap circuit: it is dependent on the absolute value of a resistor. Design becomes difficult when the absolute value of R1 is allowed to vary up to 10%.

In the design of the bandgap on the test chip, this process was not followed. The design followed a trial and error pattern in the choice of the correct resistances to obtain the smallest temperature coefficient. Unfortunately, these simulations relied on models that inaccurately represented the foundry. Using this method, K, E, and G become the fixed parameters which determine the temperature at which the bandgap is centered. TABLE 4.3 shows the measured and simulated results. The simulated value of E corresponds to the solution of Eqn 4.9 using a base emitter voltage generated by SPICE. Due to the inability to accurately measure the true resistances on the chip, both the measured and simulated cases have the same K and G parameter values.

PARAMETER	MEASURED	SIMULATED
K	20.92	20.92
G	2.21E-07	2.21E-07
E (Using Vbe @300K)	0.098	0.163
To(predicted)	-172 C	-24 C
To(actual)	< -60 C	-40 C
Vout @To (predicted)	1.2110 V	1.2184 V
Vout @To (actual)	@-60 1.2250 V	1.2250 V

TABLE 4.3 Bandgap Parameter Values

Testing was unable to proceed below -60 degrees C. The plot of the two results is shown in FIGURE 4.8. The measured bandgap plot

shows that somewhere below -60 there is a maximum. The second critical point (the local minima located at 100 degrees) is caused by non-linear temperature coefficients of the resistors R1 and RBG, a second order effect which will be explained later. These second order terms were removed from the simulation.

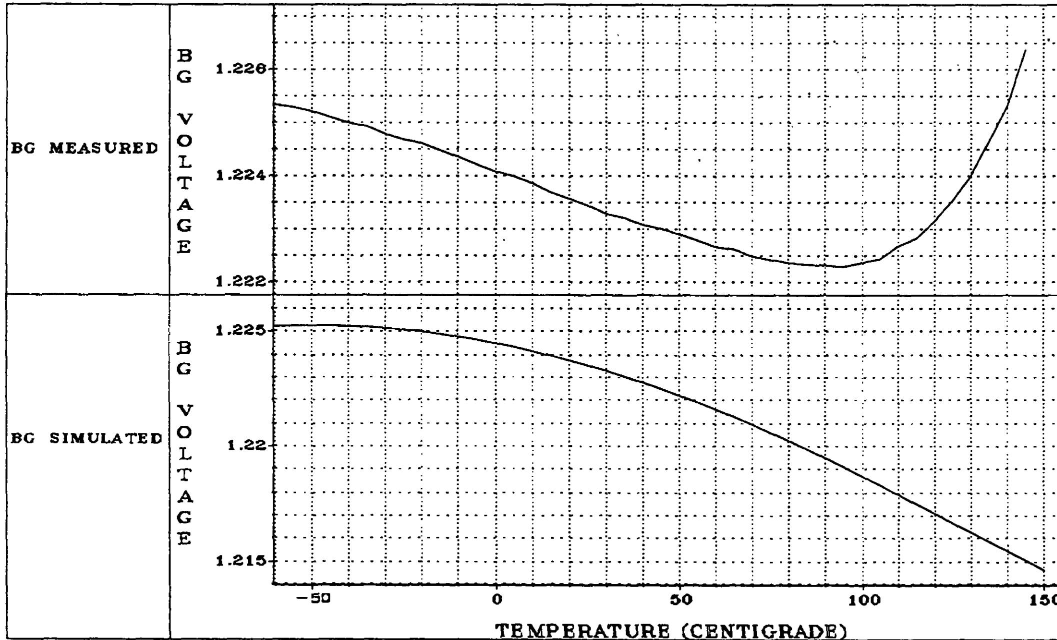

FIGURE 4.8 Bandgap Output -- Simulated (NO TC2) vs. Measured

It is interesting to note at this point that bandgap references are typically designed utilizing one base emitter voltage. This usually provides a voltage near 1.25 Volts. To achieve higher voltages, this bandgap voltage must be amplified with a DC amplifier to the needed voltage. There is an alternative method which was investigated on this chip: the utilization of multiple base emitter junctions. If two base emitter junctions are used, the resulting expression for the output voltage becomes:

$$V_{OUT}(T) = 2V_{GO} + 2V_T(\gamma - \alpha)\left(1 + \ln\frac{T_O}{T}\right) \quad (4.27)$$

This equation shows that the slope of Vout on either side of To will be twice as great as the case with one base emitter voltage. This would appear to cause a doubling of the ppm/C figure of the

bandgap reference. However, an inspection of the definition of temperature coefficient:

$$TC = \frac{1}{V_{OUT}}\left(\frac{V_{MAX} - V_{MIN}}{T_{MAX} - T_{MIN}}\right) \qquad (4.28)$$

shows that our temperature coefficient has remained constant due to the fact that the output voltage is now twice as high. In addition, as will be shown later, the actual testing results did not show a significant difference in slope of V_{OUT} for one, two, or three base emitter voltages. (SEE FIGURE 4.9) The causes for this will be discussed later.

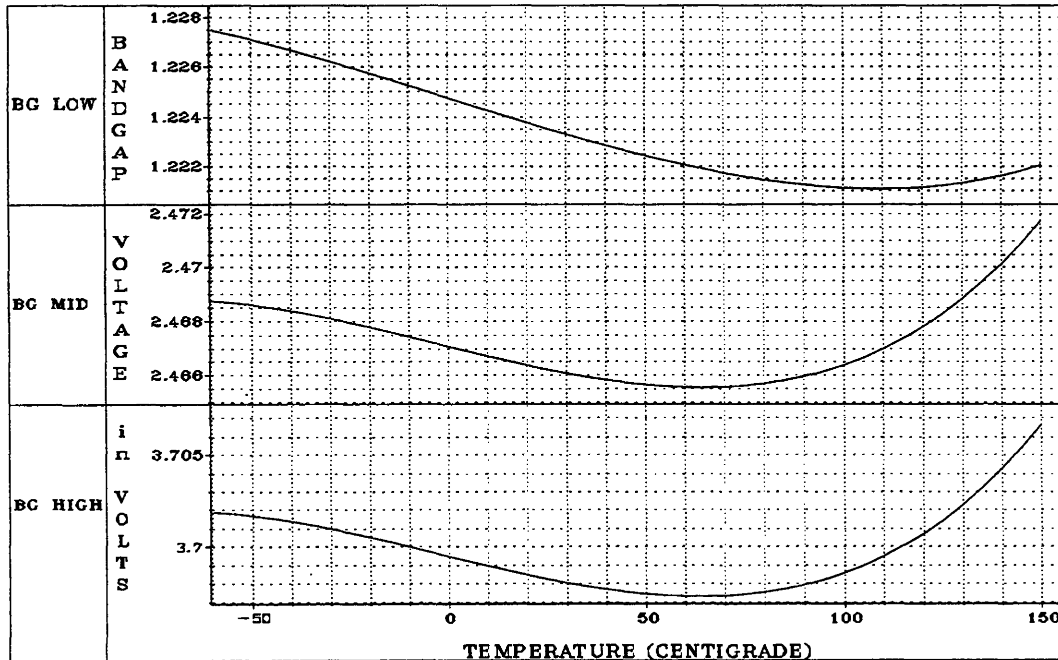

FIGURE 4.9 Higher Bandgap Voltage Generation

Another fact to note is that the equation for V_{OUT} appears to yield a curve that bows down (concave down). However, in practice, the bow may be concave up or even quadratic in form. Due to quadratic temperature coefficients, the actual bowing may take a variety of shapes.

At this point, we can use the measured data and the ideal case equations to compare the actual results with the predicted results.

4.3 The Realistic Bandgap Output Voltage

An examination of the second order effects that will cause deviations from the ideal case is necessary to provide insight into the actual form of the output voltage. FIGURE 4.10 shows the actual circuit which was tested.

FIGURE 4.10 Actual Bandgap Circuit

The bandgap circuit in FIGURE 4.10 operates in a similar manner to the ideal bandgap circuit presented in Section 4.1. The startup circuit has been previously explained (Section 1.3). The startup circuitry will cause current to be injected into the branch containing M02, M04, M06, M08, R1 and Q1. The value of current in this branch must be such that KVL is satisfied around the voltage loop consisting of the gate-source voltages of M01 and M02, the base emitter voltages of Q1 and Q2, and the voltage across R1. The resistances RBC1 and RBC2 have been added to match the base resistance of one PNP transistor with the base resistance of another PNP transistor with an emitter area eight times larger [8]. If the KVL loop is satisfied, the current in the branch will be:

$$I_{BRANCH} = \frac{\Delta V_{BE} - \Delta V_{GS}}{R_1}$$

The current in the branch consisting of M01, M03, M05, M07, and Q2 will be equal to I_{BRANCH} through the use of cascoded mirrors formed by M01, M02, M03, and M04 and M05, M06, M07, and M08. The branches containing Q10, M12, M11 and Q11, M14, and M13 are used to set the bias voltages on the gates of M01 and M02 (Q10 branch) and M07 and M08 (Q11 branch). The current I_{BRANCH} is mirrored to the output stages where it is used to generate the output voltages. Examining the branch consisting of Q12, RBG, M10, and M09, one sees that the output voltage is given by the equation (where V_{R1} is the voltage across R1):

$$V_{BG} = \left(\frac{V_{R1}}{R_1}\right) R_{BG} + V_{BE(Q12)}$$

This is the same expression seen in Eqn 4.3. There are also higher voltages generated at BG2M and BG3 through the use of stacked base emitter voltages. In addition, a PTAT voltage is generated at node PTAT which is simply the voltage across R10.

Listed below are the deviations from the ideal case for which the bandgap output voltage was solved:

1. The bandgap current is not PTAT (or related to T^{α})

The actual current which is given in Eqn 4.6 is related to ΔV_{GS}, ΔV_{BE} and the resistor R1. ΔV_{GS} was shown to be related to $T^{1.5}$. ΔV_{BE}, which was predicted to be PTAT, has a small quadratic term. The resistor which was assumed to be PTAT has a quadratic coefficient as well. In addition, the mirror to the output branch shows a decrease in current with temperature. The overall effect is the generation of a current in the output branch which has the form of:

$$I_{BANDGAP} = I_O(1 + TC_1(T - T_O) + TC_2(T - T_O)^2) \quad \text{where } TC_1 > 0 \text{ and } TC_2 < 0 \tag{4.29}$$

2. The voltage across the R_{BG} is not PTAT

The actual voltage across R_{BG} is the bandgap current times the resistance R_{BG}. Both terms have quadratic terms with opposite signs. (The resistor has a positive TC_2 as opposed to the negative TC_2 of the current in the branch)

$$V_{RBG} = I_{BANDGAP}R_{BG} = \left(I_O(1 + TC_1(T - T_o) + TC_2(T - T_o)^2)\right)\left(R_O(1 + TC_3(T - T_o) + TC_4(T - T_o)^2)\right) \tag{4.30}$$

3. The base emitter voltage has a negative quadratic term (as predicted by the equation given for $V_{BE(on)}$.)

Examining the equation for $V_{BE(on)}$ shows that the derivative with respect to temperature (Eqn 4.10) yields a negative term which is proportional to the $\log_e$ of T. This will cause $V_{BE(on)}$ to take on a concave down shape as seen in FIGURE 4.4.

4. The resistors R1 and RBG may not have the same temperature coefficients.

The actual maximum (or minimum) will occur when the derivative (with respect to temperature) of the voltage across RBG is equal and opposite to the derivative of the base emitter voltage. For a given current, the only control the circuit designer has is the voltage across RBG. The base emitter voltage characteristics will be immutable for a given process. FIGURE 4.11 and FIGURE 4.12 show the bandgap voltages and the derivatives for RBG and VBE for a concave up and a concave down bowing simulation.

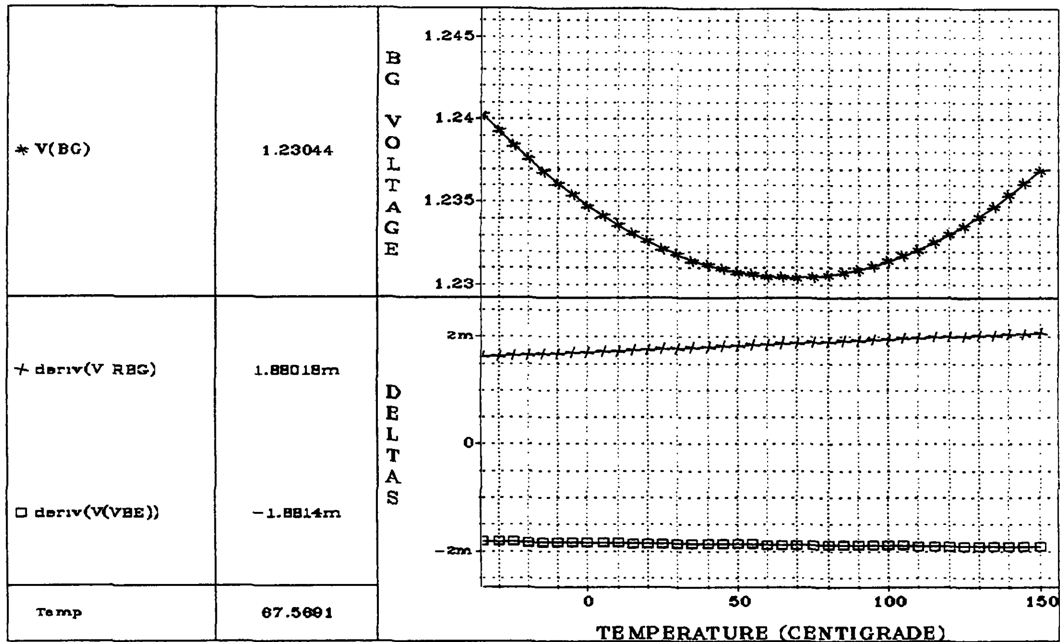

FIGURE 4.11 Bandgap Voltage with Concave Up Form

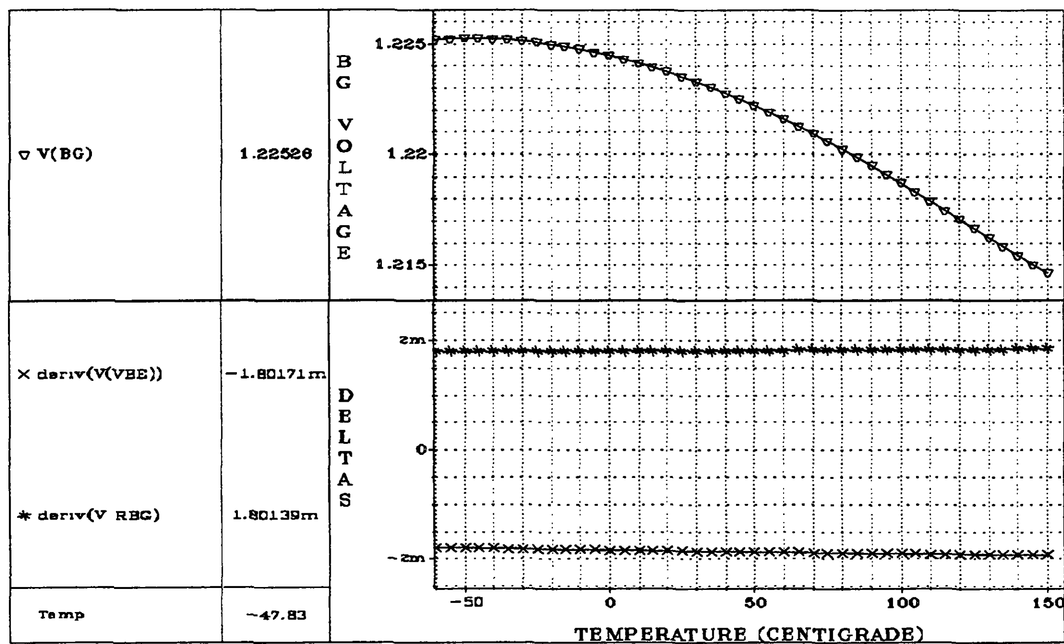

FIGURE 4.12 Bandgap Voltage with Concave Down Form

In the concave up situation(FIGURE 4.11), the plot shows that for T<To:

$$\left|\frac{dV_{BE}}{dT}\right| \geq \left|\frac{dV_{RBG}}{dT}\right|$$

This would correspond to situation where the output voltage is falling with temperature. For temperatures T>To:

$$\left|\frac{dV_{BE}}{dT}\right| \leq \left|\frac{dV_{RBG}}{dT}\right|$$

This would correspond to the situation where the output voltage is rising with temperature. This is precisely a concave up description. The concave down simulation is the opposite of the case presented.

Assuming that the V_{BE} voltage has a form similar to that discussed in section 4.1.1, the designer is left with adapting the voltage across RBG. The voltage across RBG is a product of IBANDGAP and RBG as seen in Eqn 4.30. Another definition of the voltage across the bandgap resistor(ignoring ΔV_{GS}) is:

$$V_{RBG} = \left(\frac{V_{R1}}{R_1}\right)R_{BG} = \frac{\left(\Delta V_{BEO}\left(1 + TC1_{\Delta VBE}(T - T_O) + TC2_{\Delta VBE}(T - T_O)^2\right)\right)}{R_1'\left(1 + TC1_{R1}(T - T_O) + TC2_{R1}(T - T_O)^2\right)}\left(R_{BG}'\left(1 + TC1_{RBG}(T - T_O) + TC2_{RBG}(T - T_O)^2\right)\right) \quad (4.31)$$

It is clear that in order to minimize the voltage variation with temperature, this voltage must have the same (and negative) linear slope as the base emitter voltage and an equal and opposite second derivative. Using the same expansion that was used with the resistors, a TC1 and TC2 (at a specific To) can be found for the base emitter voltage. The new equation for plotting the output voltage consists of the addition of the V_{RBG} shown in Eqn 4.31 and the new base emitter voltage equation using the TC1 and TC2 values extracted. Only the effects of the non-linearity in the ΔV_{GS} term and the current mirror have been ignored. It is now possible to explicitly solve the derivatives to interpret what the response will look like. This process was completed using the simulated values across temperature for VBE and ΔVBE. The extracted TC values are shown in TABLE 4.4

@To=20 C	TC1(VBE)	TC2(VBE)	TC1(ΔVBE)	TC2(ΔVBE)
SIMULATED	-0.00276	-6.237e-7	0.0033	+2.31e-7
MEASURED	-0.00294	+1.921e-7	0.0043	-2.15e-5

TABLE 4.4 TC Values for BJT

Using these values and the values obtained for the resistors in 4.2.4, the output voltages can be plotted explicitly without the simulator. Various parameters can be changed including the absolute values of resistors at To in order to provide a proper fit. Note that this procedure is used as an interpretation tool. It may not give the correct resistance values to use. The function of this procedure is to predict what the form of the output will look like. (It can also be used to interpret the results of a first iteration and provide information about adjustments for a second iteration.)

Looking at a plot of the measured response and the simulated response using identical temperature coefficients for the resistors, it is clear that the second derivatives for the base emitter voltage and the voltage across RBG do not match. (SEE FIGURE 4.13)

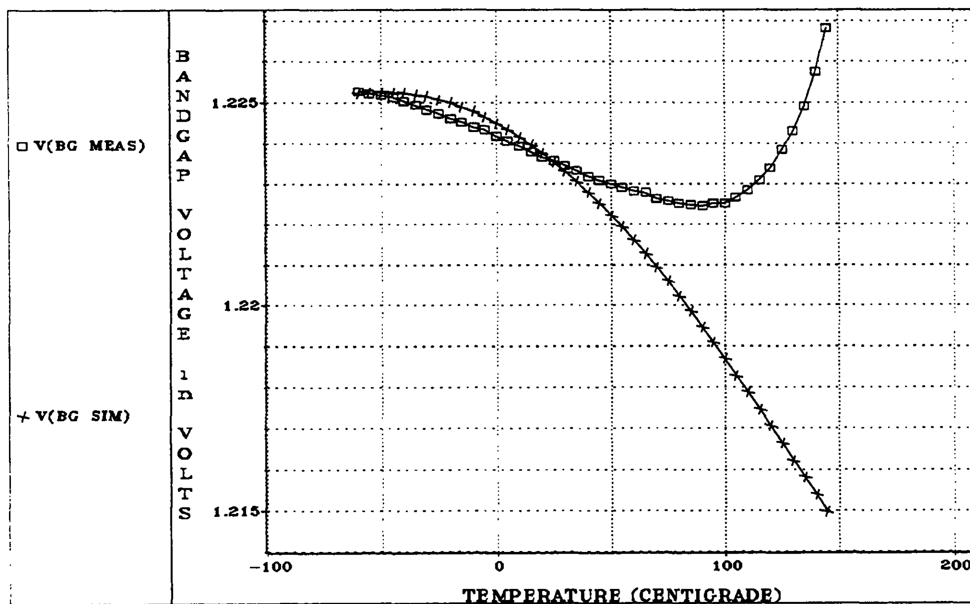

FIGURE 4.13 Bandgap Output--Measured and Simulated

These variations in the second derivative are what produce the different shapes that the output voltage might take. In the ideal case, the equations showed that the output would always take a concave down situation. However, using a realistic approach with different temperature coefficients, it is clear that the output can take any form. In this specific case, the measured bandgap output is concave up. This result can be duplicated in SPICE with a slight

change in the TC2 of RBG. (SEE FIGURE 4.14) Using the temperature coefficient equations, it is obvious which parameter in the simulation does not match the measured response. Most likely, the variation that causes discrepancies will come from the resistance parameters. These values as shown previously have the most variation within a given process.

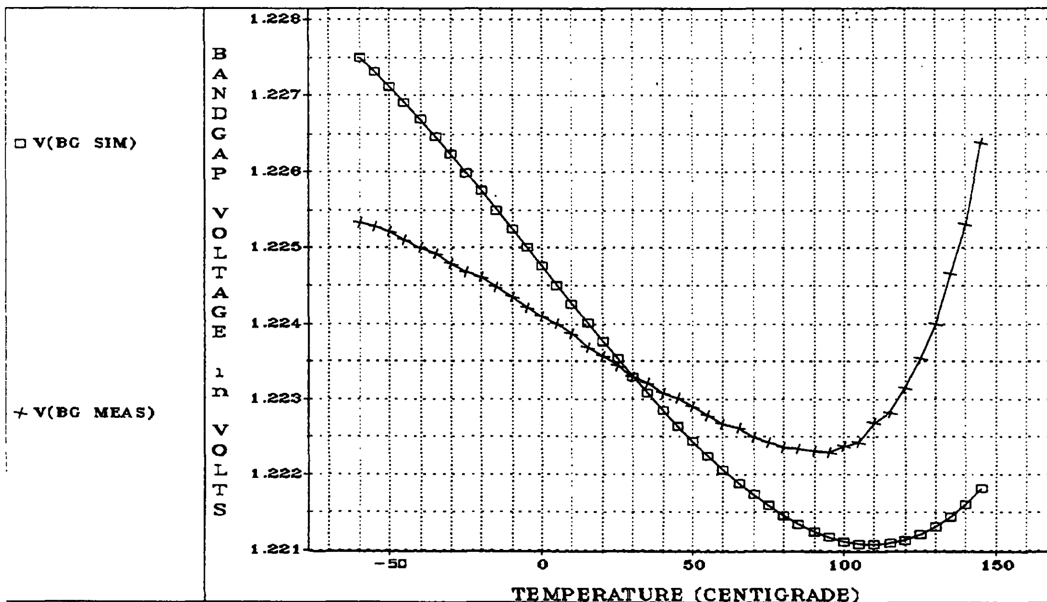

FIGURE 4.14 Bandgap Voltage--Measured and Simulated

This brings up the question of what output voltage variation can occur with variation of resistor parameter values (including both the absolute value of the resistor and its temperature coefficients). There are two areas of variation that must be considered for absolute resistance values. The first involves the difference between the expected resistance value and what the foundry produced. The second involves the difference between resistance values for different die. The first effect is a primary cause why even well-designed bandgap circuits need to have a resistor laser trimmed. In the case of this test chip, the recommended value of 24 ohms per square was used in the layout. However, the measured average was computed to be 20.8 ohms per square. This will produce a minimum error of 13% between predicted and measured resistance values. FIGURES 4.15 and 4.16 show the

output voltage variation for a 5% and 10% error in the absolute resistance value. As the plots show, a 5% error in either R1 or RBG does not have a pronounced effect on the overall TEMPCO of the circuit. (There is a greater effect if the resistance values are lower rather than higher than expected.) However, a 10% error will cause the TEMPCO to increase by a factor of four.

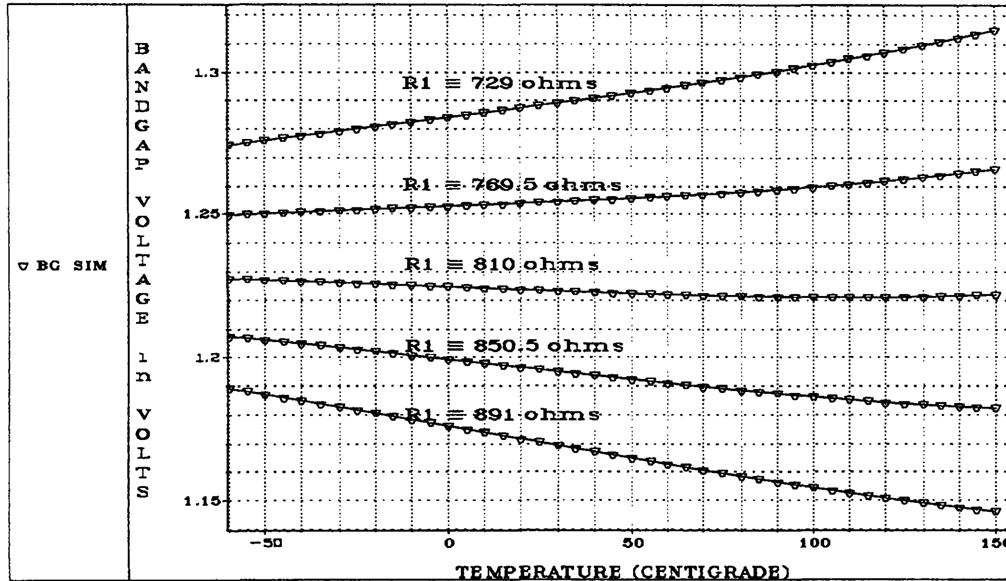

FIGURE 4.15 Output Variation with R1

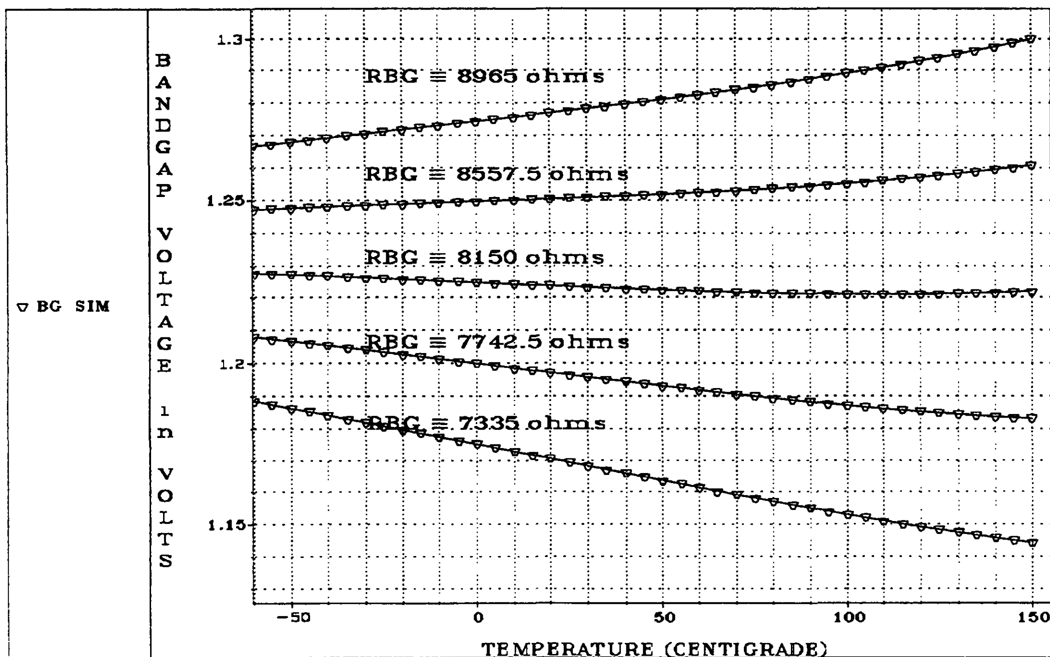

FIGURE 4.16 Output Variation with RBG

It is important to note that if both resistors have similar errors a smaller (insignificant) change results as illustrated by FIGURE 4.17. A reduction in R1 causes an increase in the PTAT current which is mirrored to the output branch. However, that same reduction in RBG will cause less PTAT voltage to be added to the output voltage. The effects cancel! The second effect does not cause significant variation at the output. There is less than a 4% variation across various die in absolute resistance values. This merely causes different die to produce random absolute voltage levels. The TEMPCO will not change a significant amount.

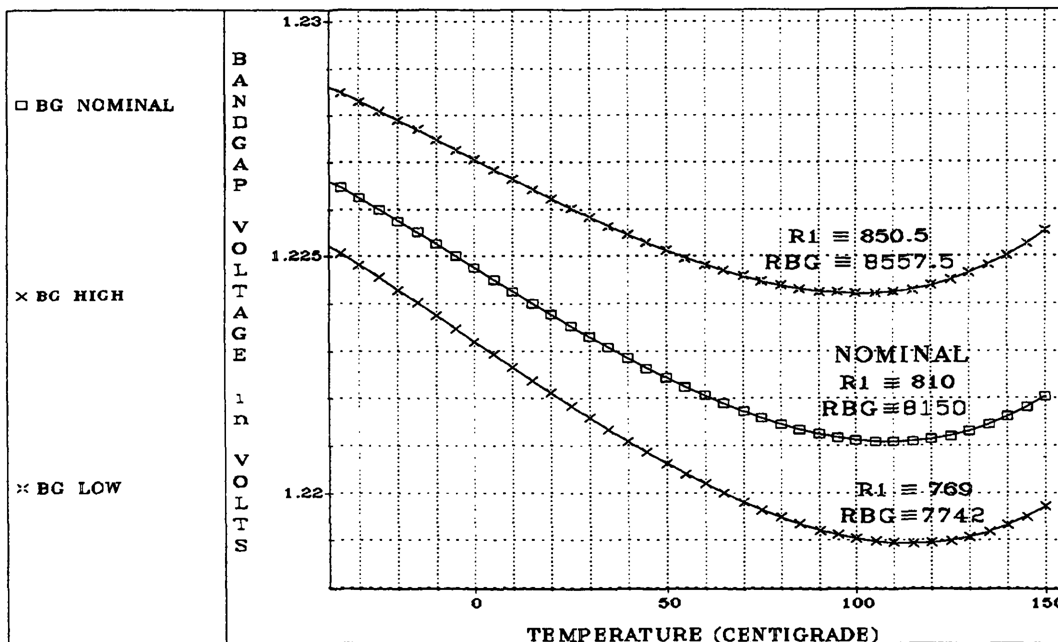

FIGURE 4.17 Output Variation with R1 and RBG

The significant change that is brought about by variation in the resistance values is a shift in the center temperature of the output voltage. This can be seen in the dependence of G on the absolute value of the resistor R1 seen in Eqn 4.24. As exhibited in FIGURES 4.15 and 4.16, this can cause a large change in the TEMPCO if the variations do not occur to both resistors.

The other type of variation that may occur is the variation in the temperature coefficients of the resistors across a given die. FIGURES 4.18 and 4.19 show the change in the output voltage as the

temperature coefficients of RBG (TC1 and TC2) are varied. FIGURE 4.19 shows that a small change in the quadratic term can cause the form of the output voltage to change from a concave down to a concave up (or quadratic). The ideal case ignores any quadratic variation in the resistance values which yields the result that the output voltage must always be concave down.

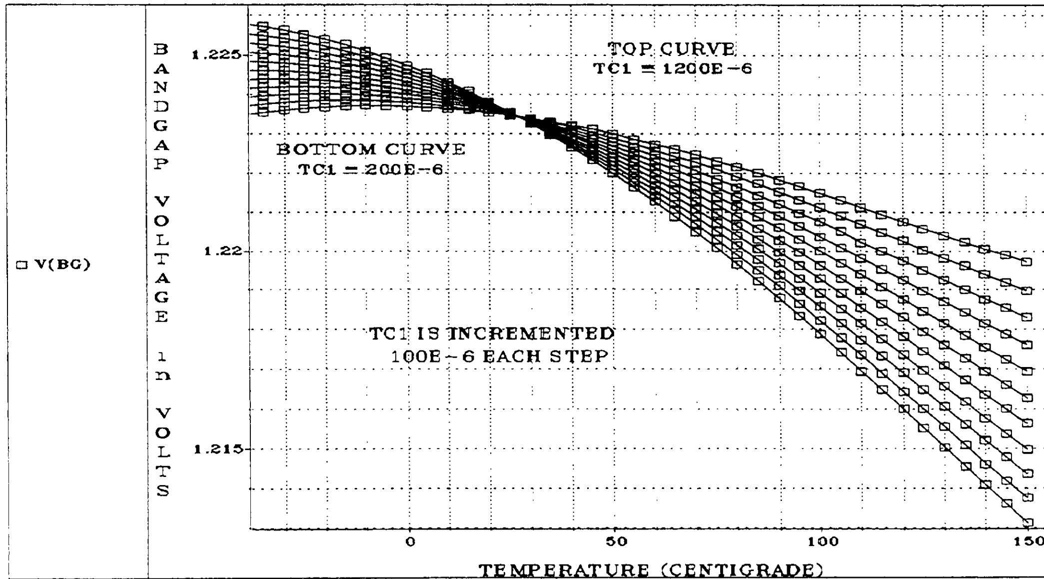

FIGURE 4.18 Output Variation with TC1

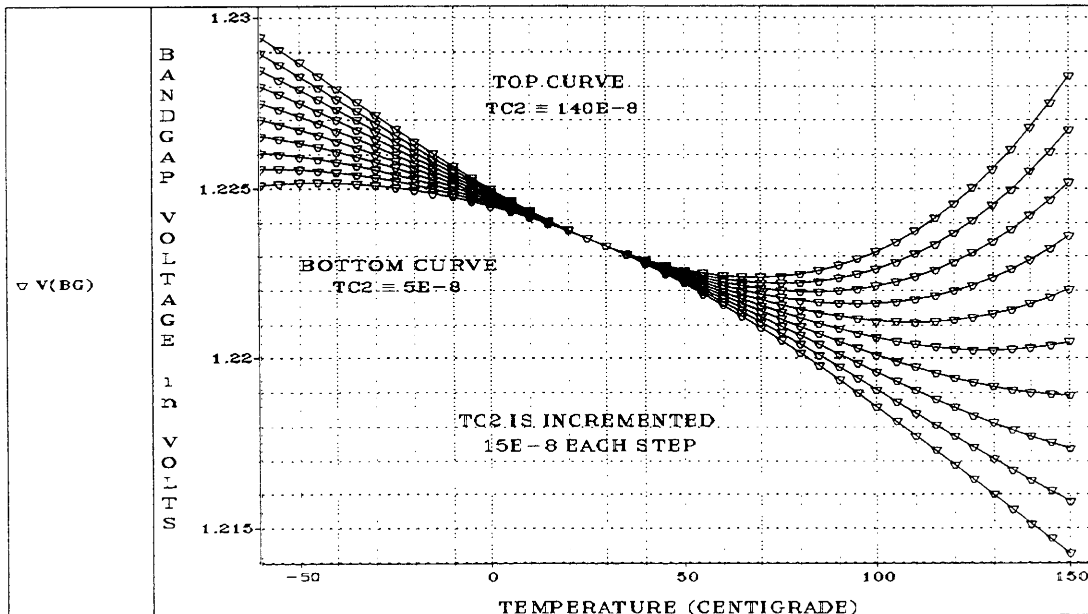

FIGURE 4.19 Output Variation with TC2

4.4 Higher voltage generation

This bandgap circuit, as FIGURE 4.9 and FIGURE 4.10 show, generates two additional output voltages at higher absolute values. FIGURE 4.20 shows the measured and simulated responses for other voltages generated by the circuit. It is clear that in the region of interest (-40 to 85 degrees C) the TEMPCO actually gets better according to the definition in Eqn 4.28. There is approximately the same variation (around 4mV) for all voltages in the region of interest. The ideal equation in Eqn 4.27 predicted that the TEMPCO would stay constant (due to the higher voltage Vout) but the variation would double. The explanation lies in the assumption that the value of K in Eqn 4.22 does not have a temperature dependence. Certainly, two base emitter junctions will have twice the variation with temperature. However, with different temperature coefficients (TC1 and TC2) for R1 and RBG, K will have a temperature dependence. This will allow the PTAT voltage to provide an equal and opposite slope that will generate the *same variation* as with one base emitter junction.

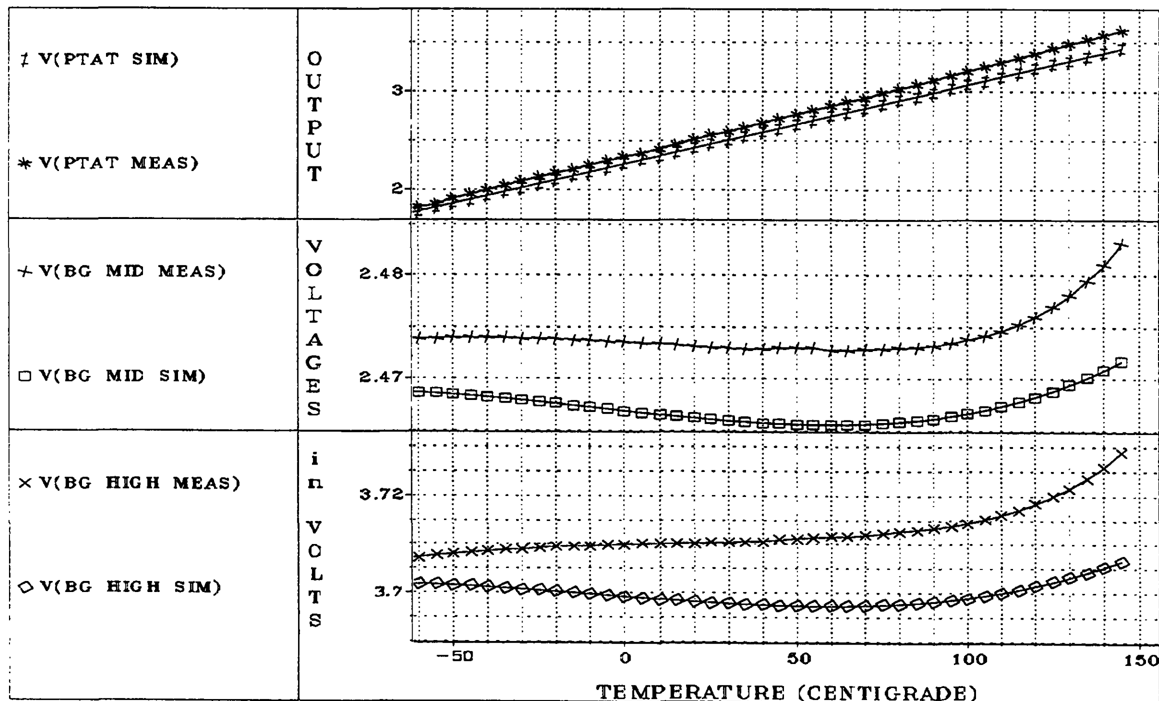

FIGURE 4.20 All Outputs -- Measured and Simulated

4.5 Design approach

With this new intuition on bandgap operation, it is useful to define a procedure for bandgap design that will improve the trial and error technique. Few articles exist on the design *procedure* of bandgap circuits. Most articles deal with the *operation* of the circuit or improvements made to existing designs. In fact, one article pointed out that a bandgap czar had been designated to reduce the chance of errors occurring in the design process [2]. I would suggest the following method:

(1) Choose the To about which the bandgap will be centered .
(2) Solve the ideal equations to find the predicted Vout.
(3) Use the information provided by the foundry to find the parameters (i.e. G, E, etc.) that define To.
(4) Use these parameters to find correct resistance values for the resistances in the circuit.
(5) Find ACCURATE models for NMOS, PMOS, Bipolar, and passive devices. This step is essential in hoping to achieve a TEMPCO less than 40 ppm.
(6) Simulate the base emitter junction voltage and use this information to extract TC1, TC2, and VBE centered at To.
(7) Simulate ΔVBE to obtain the same temperature coefficients as in part 4.
(8) Plot the output voltage using these temperature coefficients (and the extracted resistor coefficients) and change resistance values as necessary to find an acceptable TEMPCO.
(9) It would be useful at this point to include the expected variation in the resistance values and simulate. Perhaps a better combination of resistance values may be more resilient to process variation.
(10) For higher voltage generation, Eqn 4.28 may be used to find the ideal V_{out} and the same procedure should be followed. The only difference is that the TC1 and TC2 of the sum of the two V_{BE} voltages needs to be extracted.

(11) Include on the test chip at least one resistor, one MOSFET, and two parasitic Bipolar devices that can be probed. This will be invaluable for determining the actual parameters that the process produced.

4.6 Second iteration changes

Perhaps the designer had a little luck on the first iteration and produced a temperature centered, accurate bandgap. Unfortunately, many designs need to go through two iterations to shift the output to the specified To. On second iteration bandgap circuits, the output voltage center temperature shift (the temperature where the output has zero temperature coefficient) is usually accomplished with a change in the resistance value of RBG. What is the new value of resistance that will ideally give us a center at the To which was specified in the first iteration? Certainly, with the models extracted from the process, the simulator should provide the correct answer. Having a theoretical value would provide a means of checking the accuracy of the simulation.

The temperature center is located at the point where:

$$\left|\frac{\partial V_{BE(on)}}{\partial T}\right| = \left|\frac{\partial V_{RBG}}{\partial T}\right| \tag{4.32}$$

The specification required a center located at some To, but the measured response showed the center was at Tmeas. Consequently, using Eqn. 4.9 and Eqn 4.32, it is seen that:

$$\left|\frac{k}{q}\left[-(\gamma-\alpha)\ln(T_{MEAS})-(\gamma-\alpha)+\ln(EG)\right]\right| = \left|\frac{k}{q}\ln\left(\frac{A_8}{A_1}\right)\frac{R_{BG}}{R_1}\right| \tag{4.33}$$

Our center should have been at To. In order to make the same equality true at To, one side of Eqn 4.33 has to be multiplied by a constant, Fo. This Fo will be the ratio which RBG needs to be multiplied by to shift the center to To.

$$\left|\frac{k}{q}\left[-(\gamma-\alpha)\ln(T_O)-(\gamma-\alpha)+\ln(EG)\right]\right| = F_O\left|\frac{k}{q}\ln\left(\frac{A_8}{A_1}\right)\frac{R_{BG}}{R_1}\right| \quad (4.34)$$

Solving for Fo and simplifying yields:

$$F_O = \frac{\left|-(\gamma-\alpha)\ln(T_O)-(\gamma-\alpha)+\ln(EG)\right|}{\left|-(\gamma-\alpha)\ln(T_{MEAS})-(\gamma-\alpha)+\ln(EG)\right|} \quad (4.35)$$

Typical values for the constants in this equation have been shown to be:

$$\gamma = 1.8$$
$$\alpha = 1$$
$$E = 1$$
$$G = 2.7\times10^{-7}$$

Using these values Fo will reduce to the following:

$$F_O = \frac{\left|-0.8\ln(T_O)-16\right|}{\left|-0.8\ln(T_{MEAS})-16\right|} \quad (4.36)$$

It is important to note that having an accurate value of EG in this case is not required. TABLE 4.5 shows the variation in Fo with a change in the value of EG to be less than 0.5%. (Assume To = 300K and Tmeas = 220K).

	Nominal ln(EG)=15.2	ln(EG)=19.2	ln(EG)=12.2
Fo	1.009	1.010	1.015

TABLE 4.5 Fo Variation

4.7 Design Improvements

A final word must be said about improvements to this design to increase performance. The first suggestion that can be made is an alteration in the layout. The original layout simply snaked polysilicon for the resistors used in the circuit. It would seem from measurements that polysilicon turns do not have the exact same resistance characteristics as a row of straight polysilicon squares.

Consequently, in a high valued resistor with a multitude of turns, an error is introduced unnecessarily. A better layout technique would be to layout strips of polysilicon and join alternating ends with metal 1 or metal 2 (whichever has lower resistance).

Another addition that I would add to the circuit is a reset function that will allow the bandgap to be forced to restart itself. This can be realized by the addition of a transistor whose drain is attached to the gates of M17 and M18, source is connected to ground, and gate is pulled out as a reset switch. If the gate receives 5 Volts, it will steal all the current from M15 causing the circuit to reset.

Finally, a change in the resistance values is needed. A short sighted change would be to simply adjust the resistance values (without removing the polysilicon turns) used in the first run using the Fo value from Section 4.5. However, in the long run, it would be more useful to layout the resistors correctly with metal connections. Assuming the circuit will be used in multiple applications, it would be more useful to have a circuit whose resistances can be predicted with a higher degree of accuracy.

This circuit is being refabricated with the above suggestions. The higher voltage outputs have been removed as amplifiers will provide the means for generating voltages above the bandgap output. The new circuit is shown in FIGURE 4.21.

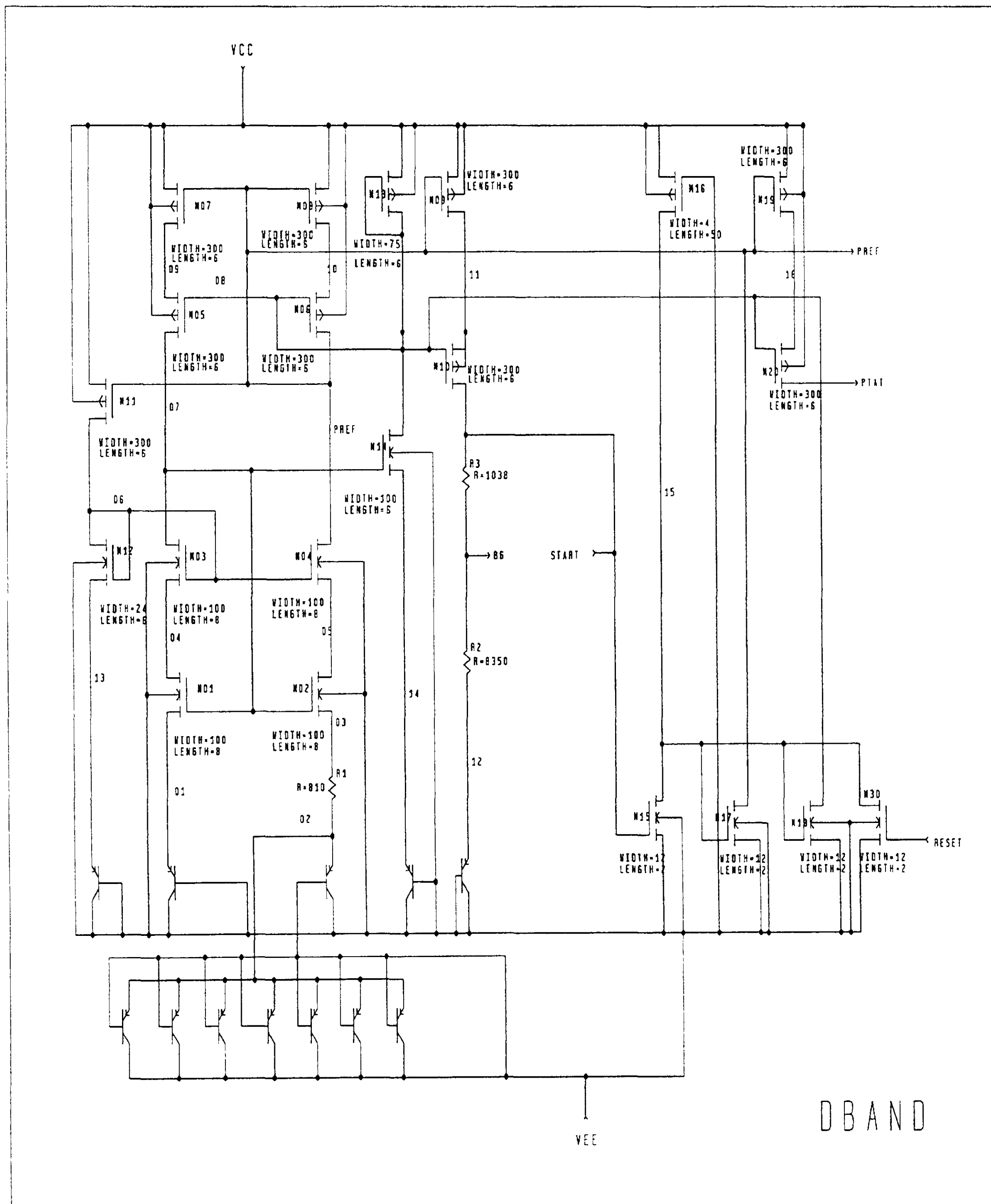

FIGURE 4.21 Redesign of Bandgap Circuit

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APPENDIX A. MOS Extraction Matlab Code

```
%This program takes measured IV responses of a MOSFET and returns
%a rough guess of the SPICE LEVEL3 parameters

clear;
format long;


%------------------------------------------------------------
------------------
%Constants----------------------------------------------
-------------
%------------------------------------------------------------
------------------

k=1.38e-23;         'J/K';
T=300;              'K';
q=1.602e-19;              'C';
ni=1.5e10;          'cm^3';

do=.0631353;
d1=.8013292;
d2=-.01110777;

esi= 1.04e-12;          'F/cm';
tox=22.5e-7;            'cm';
eo=8.86e-14;            'F/cm';
kox=3.9;
eox=kox*eo;             'F/cm';
Cox=(eox/tox);          'F/cm^2';

Eg=1.16-(7.02e-4)*T*T/(T+1108);

ALPHA=1;
Nsub1=1e16;             'cm^3';
Fs=1;
sigma=0;

% THESE VALUES WILL BE THE DEFAULT VALUES FROM ORBIT'S
PROCESS WHICH
```

```
% WILL BE USED IN CASE THE DATA DOES NOT PROVIDE A SENSIBLE
ANSWER

Xjl = .3e-4;        'cm';
dW  = .6e-4;        'cm';

%*****************************************************
*******************
%  INPUT DATA FILE NAME
%*****************************************************
******************

N1010_P80

%*****************************************************
******************


%-----------------------------------------------------
-----------------
%  PROCEDURE FOR EXTRACTING Rt, Xjl, and delta W----------------
---------------
%-----------------------------------------------------
-----------------

clg;

for i = 1:length(v_ll)
     rds(i)=.05/i_ll(i);
end

plot(v_ll,rds)
hold on


for i = 1: length(v_ll)
   rds2(i) = .05/ ii_ll(i);
end

plot(v_ll,rds2)
axis([-1 4 -100 3500]);
grid on;
```

```
a_ll=polyfit(v_ll,rds,1);
b_ll=polyfit(v_ll,rds2,1);

for i = 1:20
     yval(i)  =  a_ll(1)*(i-1)+a_ll(2);
      yyval(i)=b_ll(1)*(i-1)+b_ll(2);
    xval(i) = (i-1);
end

plot(xval,yval,'go',xval,yval,'r-')
plot(xval,yyval,'go',xval,yyval,'r-')
title ('Rds vs. Lnom...........Part2')

pause;


%------------------------------------------------------------
------------------
%Delta W extraction
%------------------------------------------------------------
------------------

clg;


for i = 1:length(v_ww)
      gds(i)=i_ww(i)/.10;
end

plot(v_ww,gds,'b*',v_ww,gds,'y-')
hold on
axis ([0 2 -.00001 .00001])
grid on;

a=polyfit(v_ww,gds,1);

for i = 1:20
    yval(i) = a(1)*(i-1)+a(2);

    xval(i) = (i-1);
end

plot(xval,yval,'go',xval,yval,'r-')
```

```
title('GDS vs. Wnom Plot......Part2a')

pause;



%------------------------------------------------------------
------------------
%VT,   THETA,   BETA   Extraction-----------------------------------
-------------
%------------------------------------------------------------
------------------


for i = 1:5

AA(i)  =  V2(i)-V1(i);
BB(i)  =  V3(i)-V1(i);
CC(i)  =  V3(i)-V2(i);

TEMP1(i)=I1(i)*I2(i)*AA(i)-I1(i)*I3(i)*BB(i)+I2(i)*...
     I3(i)*CC(i);
TEMP2(i)  =  -I1(i)*CC(i)+I2(i)*BB(i)-I3(i)*AA(i);

a(i) = TEMP1(i)/TEMP2(i);

TEMP3(i)  =  I1(i)*I2(i)*AA(i)*V3(i)-I1(i)*I3(i)*BB(i)*...
      V2(i)+I2(i)*I3(i)*CC(i)*V1(i);
TEMP4(i)  =  I1(i)*I2(i)*AA(i)-I1(i)*I3(i)*BB(i)+I2(i)*...
      I3(i)*CC(i);

b(i) = TEMP3(i)/TEMP4(i);

TEMP5(i)  =  -I1(i)*CC(i)*V1(i)+I2(i)*BB(i)*V2(i)-I3(i)*...
      AA(i)*V3(i);
TEMP6(i)  =  -I1(i)*CC(i)+I2(i)*BB(i)-I3(i)*AA(i);

c(i) = TEMP5(i)/TEMP6(i);

%------------------------------------------------------------
------------------
```

```
VT(i) = b(i) - (ALPHA/2)*VDS;

THETA(i) = 1/(b(i)-c(i)-(ALPHA/2)*VDS - (a(i)/ZETA));

BETA(i) = a(i)/(VDS*(b(i)-c(i)-(ALPHA/2)*VDS-(a(i)/ZETA)));

end;


%------------------------------------------------------------
------------------
%INSERT HERE A ROUGH GUESS OF UO---------------------------
-----------------
%------------------------------------------------------------
------------------


uo = ((Leff)/(Weff*Cox))*((iid(2)-iid(1))/(vvg(2)-vvg(1)))/VDS;


%------------------------------------------------------------
------------------
% COMPUTE   GAMMA  HERE--------------------------------
%------------------------------------------------------------
------------------

VBS(2)= -1.25;
VBS(3)= -2.5;
VBS(4)= -3.75;
VBS(5)= -5;

for i = 1:4
Vth_prime(i)=VT(i+1);
end;

for i = 1:10

     phi=(2*k*T/q)*log(Nsub1/ni);

          for j = 1:4
                         x_term(j)=Fs*sqrt(phi-VBS(j+1));
     end;
```

```
    xxval=rot90(x_term,-1);
    yyval=rot90(Vth_prime,-1);

    temporary=polyfit(xxval,yyval,1);

    Nsub1 = (temporary(1)^2/(2*q*esi))*Cox^2;
    Xd=sqrt((2*esi)/(q*Nsub1));
    Wp=Xd*sqrt(phi);
    Wc = do*Xj+d1*Wp+d2*Wp*Wp/Xj;
    gamma1=temporary(1);
    radical = 1 - ((Wp/Xj)/(1+(Wp/Xj)))^2;
    coeff=(Xjl+Wc)/Xj;
    Fs = 1 - (Xj/Leff)*(coeff*sqrt(radical)-(Xjl/Xj));
 end;

%----------------------------------------------------------
------------------
%   COMPUTE   ETA  and  SIGMA-------------------------------
%----------------------------------------------------------
------------------



sig=polyfit(VD,vth,1);

sigma1=-1*sig(1);

eta = (sigma1*(Cox)*((Leff)^3)/(8.15*1e-22));


%----------------------------------------------------------
------------------
%  COMPUTE ∂ (delta) for narrow channel factor------------------
-----
%----------------------------------------------------------
------------------

vth_narr = VT(1)-gamma1*sqrt(phi)+gamma1*Fs*sqrt(phi+2.5)-
sigma1*VDS;
Fn1 = (VT(3)-vth_narr)/(phi+2.5);
delta1 = 4*Cox*Weff*(VT(3)-vth_narr)/(2*pi*esi*(phi+2.5));
```

```
%------------------------------------------------------------
------------------
%   COMPUTE Vmax (for saturation velocity in channel)-------------
-------
%------------------------------------------------------------
------------------


Vgs=5;

us=uo/(1+THETA(1)*(Vgs-VT(1)));

b=1/us;



for qq=1:2
        ueff(qq)=Imax(qq)*(Leff)/(Cox*(Weff)*(Vgs-VT(1)-.5*...
             (1+Fb)*Vmax(qq))*Vmax(qq));
      ymax(qq)=1/ueff(qq);
      xmax(qq)=Vmax(qq)/(Leff);
     yvalmax(qq)=ymax(qq)-b;

end;

aa1=polyfit(xmax,yvalmax,1);
bb1=polyfit(xmax,ymax,1);
vmax1=1/aa1(1);
vmax=vmax1/100;

Va  =  (Vgs-VT(1))/(1+.1);
Vb  =  vmax1*Leff/us;

Vdsat1  =  Va+Vb  -  sqrt(Va*Va+Vb*Vb);
Vdsat1
pause;


% AT THIS POINT WE WILL NEED TO RECORD VDSAT TO FIND IDSAT---
--------------
%------------------------------------------------------------
------------------
```

```
Idsat1_calc = us*Cox*((Weff)/(Leff))*(Vgs - VT(1) - .5*...
     (1+Fb)*Vdsat1)*Vdsat1;

uonew=Idsat1_meas/(Cox*((Weff)/(Leff))*(Vgs - VT(1) - .5*...
(1+Fb)*Vdsat1)*Vdsat1);


%-------------------------------------------------------------
------------------


Ldel = Leff*(1 - (Idsat1_meas/IDD));

kappa1 = Ldel^2/(Xd*Xd*(5 - Vdsat1));


%PRINTOUT VALUES OF INTEREST
%-------------------------------------------------------------
------------------

Nsub1
kappa1
uo
uonew
Xjl
dW
gamma1
eta
delta1
vmax
'THETA'
THETA(1)
'Vto'
VT(1)

fid = fopen('N1010_P80.dat','w');
fprintf(fid,'********   MODEL PARAMETERS GENERATED FROM MATTs
CODE   ****\n');
fprintf(fid,'*******      1.2um ORBIT PROCESS    ******\n');
fprintf(fid,'.MODEL  N_1010_N40     MOS3    \n');
```

```
fprintf(fid,'+          LEVEL = 3.000000E+000\n');
fprintf(fid,'+          UO    = %.6E  \n', uonew);
fprintf(fid,'+          VTO   = %.6E  \n', VT(1));
fprintf(fid,'+          TOX   = %.6E  \n', tox);
fprintf(fid,'+          GAMMA = %.6E  \n', gamma1);
fprintf(fid,'+          PHI   = %.6E  \n', phi);
fprintf(fid,'+          NSUB  = %.6E  \n', Nsub1);
fprintf(fid,'+          XJ    = %.6E  \n', Xj);
fprintf(fid,'+          ETA   = %.6E  \n', eta);
fprintf(fid,'+          DELTA = %.6E  \n', delta1);
fprintf(fid,'+          KAPPA = %.6E  \n', kappa1);
fprintf(fid,'+          THETA = %.6E  \n', THETA(1));
fprintf(fid,'+          VMAX  = %.6E  \n', vmax);
fprintf(fid,'+          LD    = %f   \n', 0);
fprintf(fid,'+          RD    = %f   \n', 0);
fprintf(fid,'+          RS    = %f   \n', 0);
fprintf(fid,'+          IS    = %f   \n', 0);
fprintf(fid,'+          JS    = %f   \n', 0);
fprintf(fid,'+          NFS   = %f   \n', 0);

status = fclose(fid);
```

APPENDIX B. Additional MOS Extraction References

K. Burke, et al, " Worst-Case MOSFET Parameter Extraction for a 2um CMOS Process," *Proc. IEEE 1994 Int. Conference of Microelectronic Test Structures,* Vol. 7, March 1994.

M.F. Hamer, " First-Order Parameter Extraction on Enhancement Silicon MOS Transistors," *IEE Proceeedings*, Vol. 133, Pt. I, No. 2, April 1986.

K. Jeppson, P.Karlsson, " An Analytical Strategy for Fast Extraction of MOS Transistor DC Parameters Applied to the SPICE MOS3 and BSIM Models," *Proc. IEEE 1992 Int. Conference of Microelectronic Test Structures*, Vol. 5, March 1992.

K. Jeppson, P. Karlsson, " An Efficient Parameter Extraction Algorithm for MOS Transistor Models," *IEEE Transactions on Electron Devices*, VOl. 39, No. 9, September 1992.

J. Joosten, S. Swaving, H. Tuinhout, " A Fully Analytical MOSFET Model Parameter Extraction Approach," *IEEE Proceedings on Microelectronic Test Structures*, Vol. 1, No. 1, February 1988.

W. Lane, J. Power, " Enhanced SPICE MOSFET Model for Analog Applications Including Parameter Extraction Schemes," *Proc. IEEE 1990 Int. Conference of Microelectronic Test Structures,* Vol. 3, March 1990.

APPENDIX C. SPICE Models

1. BIPOLAR PNP MODEL

```
***************************************************************
*********************
*****  Model Station II                  by SANCAD San Diego, CA
*****
***************************************************************
*********************
.MODEL PNP PNP (
+ IS     = 1.5973e-16   BF     = 40.7496     NF     = 0.97628
+ VAF    = 84.9272      IKF    = 0.00200181  ISE    = 3.89444e-14
+ NE     = 2.50039      BR     = 6.5         NR     = 1
+ VA     = 33.5         IKR    = 0.2         ISC    = 5.00389e-13
+ NC     = 2            RB     = 250         IRB    = 1
+ RBM    = 50           RE     = 8.00127     RC     = 250
+ CJE    = 1e-12        VJE    = 0.75        MJE    = 0.33
+ TF     = 1e-09        XTF    = 2           VTF    = 0.5
+ ITF    = 0.8          PTF    = 0.8         CJC    = 5e-12
+ VJC    = 0.75         MJC    = 0.33        XCJC   = 1
+ TR     = 1e-09        CJS    = 1e-13       VJS    = 0.75
+ MJS    = 0.5          XTB    = 1.8         EG     = 1.206
+ XTI    = 3            KF     = 0           AF     = 1
+ FC     = 0.5          )
```

2. NMOS LEVEL 3 Model

```
***************************************************************
*****  Model Station II                  by SANCAD San Diego, CA
*****
***************************************************************
.MODEL NMOS NMOS (
+ VTO    = 0.57095      UO     = 535.338     TOX    = 2.25e-08
+ GAMMA  = 1.00507      PHI    = 0.842916    NSUB   = 6.3518e+16
+ XJ     = 3.74333e-07  ETA    = 0.78553     DELTA  = 3.74957
+ KAPPA  = 0.0314718    THETA  = 0.114497    VMAX   = 2.56161e+07
+ LD     = 9.01519e-08  RD     = 4.95191     RS     = 53.0447
+ IS     = 1e-15        JS     = 5e-06       NFS    = 5.14e+10
+ LEVEL  = 3            )
```

3. PMOS LEVEL 3 Model

```
********************************************************
*********************
*****  Model Station II                  by SANCAD San Diego, CA
*****
********************************************************
.MODEL PMOS PMOS (
+ VTO      = -1.50774      UO      = 153.072      TOX     = 2.25e-08
+ GAMMA    = 0.326443      PHI     = 0.728454     NSUB    = 9.85208e+18
+ XJ       = 4.52883e-07   ETA     = 0.352616     DELTA   = 0.972751
+ KAPPA    = 0.637708      THETA   = 0.0916216    VMAX    = 307860
+ LD       = 2.62109e-07   RD      = 0            RS      = 0
+ IS       = 1e-15         JS      = 1e-05        NFS     = 1e+10
+ LEVEL    = 3             )
********************************************************
********************
```