# Workfunction Tuning of n-Channel MOSFETs Using Interfacial Yttrium Layer in Fully Silicided Nickel Gate

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*Abstract*—**Continual scaling of the CMOS technology requires thinner gate dielectric to maintain high performance. However, when moving into the sub-45 nm CMOS generation, the traditional poly-Si gate approach cannot effectively reduce the gate thickness further due to the poly-depletion effect. Fully silicided Ni metal gate (FUSI) has been proven to be a promising solution. Ni FUSI metal gate can significantly reduce gate-line sheet resistance, eliminate boron penetration to channels and has good process compatibility with high-k gate dielectric. But Ni FUSI has a mid-gap workfunction which is not suitable for high-performance CMOS applications where the band-edge workfunction is required. In this paper, we propose to tune the nickel (Ni) fully silicided metal gate (FUSI) workfunction via an yttrium/Si/Ni gate stack structure. The workfunction of such structure indicates that the Y interlayer can effectively tune the Ni FUSI workfunction from the mid gap to the conduction band edge of silicon by controlling the interlayer thickness. The gate stack workfunction starts to saturate to the pure yttrium value when the yttrium interlayer is >1.6 nm. This indicates the chemical potential of the material adjacent to gate electrode/gate insulator plays an important role in the determination of the workfunction.**

*Index Terms*—**metal gate, FUSI, Ni silicidation**

## I. INTRODUCTION

As the metal oxide semiconductor field effect transistors (MOSFETs) are being continuously scaling down to the sub 45-nm-generation technology, it is necessary to reduce the gate insulator thickness (effective oxide thickness) to less than 1.2 nm.[1] With the gate insulator reduction, however, a degradation in the transistor's performance due to gate depletion becomes a serious problem. Boron penetration is another major concern due to the scaling down of gate insulator. The fully silicided (FUSI) poly-Si gate which shows a metal-like behavior is a promising candidate for solving the aforementioned problems associated with poly-silicon gates.[2,3] Among all the materials used for silicidation, Ni attracts a lot of attention for silicided ultrashallow junctions due to its lower Si consumption compare to Co and simpler thermal process compare to Ti.

On the other hand, a typical NiSi metal gate has a workfunction of 4.6 - 4.7eV which is close to the silicon mid-gap energy. In bulk CMOS technology, however, two separate workfunctions are required for the n-MOS and p-MOS devices. Therefore, substantial effort has been devoted to the tuning of the NiSi workfunction to the band edges (4.9-5.1eV for p-MOSFETs, 4.0-4.2eV for n-MOSFETS). These include the use of p-type and n-type dopants in pre-silicided poly-silicon film,[4-7] Ni alloy,[8] and forming different Ni silicide phase.[7,9] In this letter, we propose a new method to tune gate workfunction from 4.33 to 3.65 eV via the introduction of an yttrium (Y) layer in the proposed Ni FUSI structure.

## II. METHODS AND EXPERIMENT

The starting material was p-type Si wafers of resistivity 4-8 $\Omega^{-1}cm^{-1}$. The wafers were cleaned with the standard RCA I and RCA II solutions followed by a dip in a 10% HF solution to remove any native oxide. An oxide layer was then thermally grown on the wafer in pure $O_2$ ambient at 900°C. Four groups of samples with oxide thicknesses of 6 nm, 10 nm, 15 nm and 19 nm were prepared. In order to study the effect of interlayer yttrium, a thin layer of yttrium of thickness ranging from 0.3 nm to 19.2 nm was sputtered deposited, followed by a 100 nm Si layer, onto the samples without breaking vacuum. The base pressure of the sputtering machine for the deposition of Y and Si was $4\times10^{-7}$ Torr. After the deposition of the Y and Si structure, the samples were then dipped into a 10% HF solution to remove native oxide on the Si surface before deposition of a layer of 65 nm Ni film by sputtering. The samples were then rapid thermal annealed (RTA) in $N_2$ ambient at 400 °C for 120 s to form fully silicided film. A piranha solution ($1H_2O_2:3H_2SO_4$) was used to remove the unreacted Ni after RTA. For comparison, a sample without any Y interlayer and another sample with a thick Y were fabricated on the thin oxide films.

For the electrical characterization of the Ni FUSI samples, metal-oxide-silicon (MOS) capacitors with a top metal contact diameter of 180 μm were fabricated. In the lithography process, isotropic solution $HNO_3$:$H_2O$:$NH_4F$ was used to selectively etch the unwanted silicide and unreacted Y. The back contact was formed by evaporating a 250 nm gold layer at the back of the p-type Si wafer.

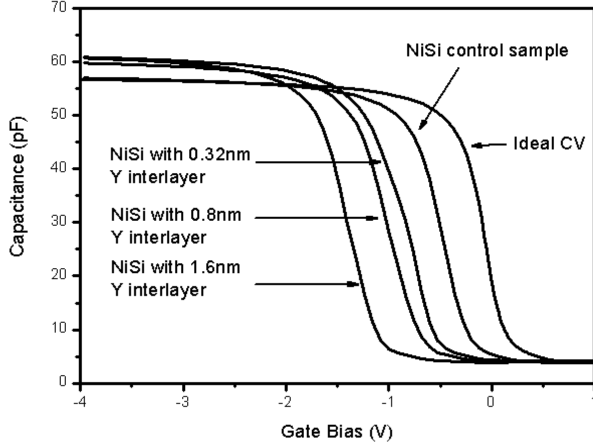


Fig. 1 Capacitance-Voltage curve of Ni-FUSI MOS devices. The left shift is due to the presence of the yttrium interlayer and increases with yttrium film thickness. The Cmax of the devices with a yttrium interlayer is 10% higher than that of the NiSi control sample.

## III. RESULTS AND DISCUSSION

Figure 1 shows the high frequency (100 kHz) *C-V* curves of the control and NiSi samples with different thicknesses of Y interlayer. All the samples experience a similar amount of stretch out in their *C-V* curves which were possibly caused by interface trap charges at the respective substrate-oxide interface. The interface trapped charge density was calculated to be ~ $4x10^{10}$ $eV^{-1}$ $cm^{-2}$. On the other hand, the shift of the flatband voltage of the NiSi control sample without any Y interlayer is attributed to fixed charges in the silicon oxide layer. Note that for samples with a Y layer, the left shift in the *C-V* curves increases with the interlayer Y thicknesses from 0.3 nm to 19.2 nm and the underlying mechanism will be discussed in a later section. The accumulation capacitance ($C_{max}$) of the samples with the Y layer is also 10% larger than that of the control sample. Since Y could react with $SiO_2$ to form yttrium silicade[10] (dielectric constant = 14), thus reducing the silicon oxide thickness, the increase in the $C_{max}$ values could be due to: (i) a reduction in silicon oxide thickness and (ii) the introduction of a new dielectric layer of $YSiO_x$ with a dielectric constant of about 14 in series with the original silicon oxide capacitor. It is also noticed that the $C_{max}$ of the pure yttrium sample witch was not gone through any thermal treatment is the same as the Ni FUSI control sample. This suggests the yttrium silicate reaction can only happen during high temperature annealing. The leakage current measured from the corresponding *I-V* characteristic has a similar value for both the yttrium interlayer samples and pure yttrium control samples, suggesting that the addition of the yttrium interlayer does lead to serious device degradation.

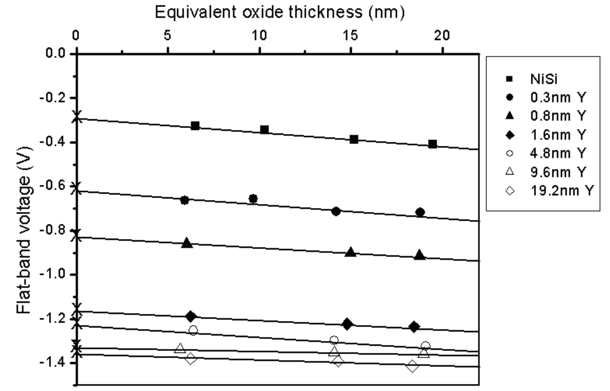


Fig. 2 Effect of the Y interlayer thickness on the flat-band voltage of the formed FUSI gate.

Figure 2 shows the extracted flatband voltage ($V_{FB}$) from the *C-V* curves as a function of the equivalent oxide thickness (EOT) of the FUSI gates shown in Fig. 1. The EOT of the capacitor was estimated from the $C_{max}$ value assuming the silicon oxide relative permittivity value of 3.9. Figure 2 clearly shows a significant decrease in $V_{FB}$ with increasing the thickness of the Y interlayer from 0.3 nm to 1.6 nm. Beyond 1.6 nm, $V_{FB}$ saturates with increasing Y thickness.

In a MOS system, the gate workfunction ($\Phi_m$) can be expressed as

$$\Phi_m = \Phi_s + V_{FB0} \quad (1)$$

where the $\Phi_s$ is the Fermi level of the Si substrate, and $V_{FB0}$ is the flatband voltage extrapolated to the zero oxide thickness (as indicated with crosses in Figure 2). Figure 3 plots the gate workfunction values of the FUSI structures with different Y thicknesses. When there is absence of the Y layer in the system (i.e. pure NiSi gate), the gate workfunction is 4.69 eV. This is a typical workfunction value for a Ni-silicided FUSI system[2]. With the introduction of the Y layer, the value of the workfunction decreases with increasing Y interlayer thickness. The reduction of the workfunction value saturates at ~3.56eV which corresponds to an interlayer thickness of 19.2 nm.

It is reasonable to expect that when the Y layer is thin, all Y can be consumed by Si to form $YSi_2$. When the Y layer becomes thicker, Y will compete with Ni to react with the Si. It is known that Si and Ni are the faster diffusion species during the yttrium silicidation and nickel silicidation process[10, 11], respectively. As a result, it could be expected that the diffusivity of Y is much lower than Ni in the sandwich structures. It has been reported[12, 13] that the reaction time between a few hundreds angstroms of Y and Si would be in the order of hours. This is very much slower than the reaction time between a similar thickness of Ni and Si. Therefore, when the Y layer becomes thicker, part of the thickness Y films is expected to be unreacted or remain as high Y concentration content at 400 °C, 120 s as a substantial amount of Si would have been consumed by the top Ni to form Ni-silicide instead, leading to certain amount of unreacted Y layer adjacent to the $SiO_2$ interface. Transmission electron microscopy/energy dispersive x-ray analysis results shown in Figure 4 suggest that the Y contents still remain at FUSI/$SiO_2$ interface and do not diffuse up into the top NiSi films after the RTP process. The presents of relative high concentration of Si and Ni

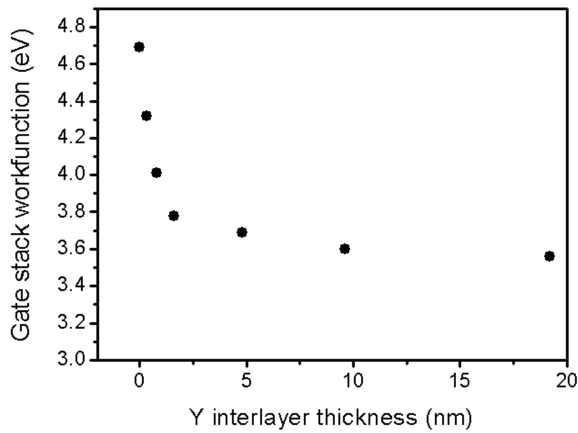


Fig. 3 Extracted workfunction as a function of the yttrium thickness. The gate electrode workfunction dramatically drops when induce yttrium interlayer. Its value trends to saturate to the bulk yttrium workfunction when the yttrium interlayer thicker than 1.6nm.

at FUSI/$SiO_2$ interface also suggest the formation of Y silicide or a Y-Si-Ni ternary alloy reaction could happen during RTP process.

It is generally agreed that the material adjacent to the gate electrode/gate insulator interface plays a dominant roll in the determination of the gate workfunction. This localized gate workfunction can be expressed as

$$\Phi = -\mu + \frac{emC_{dipole}}{\varepsilon_0} \qquad (2)$$

where μ is the bulk chemical potential for the gate electrode material, e is the electronic charge, $\varepsilon_0$ is the permittivity of vacuum, m is the dipole moment of surface dipole and $C_{dipole}$ is the concentration of surface dipole[14,15]. The second term in equation (2) represents the modification of interface dipole on the gate workfunction. Pure Y has a very low workfunction and the calculated value from our pure Y control samples is around 3.34eV which is slightly higher than the reported value of 3.1-3.2eV (by photo-emission method) [16]. As shown in Figure 3, the workfunctions of the samples with a Y interlayer decreases as the Y film thickness increases. When the unreacted Y layer becomes thicker, the influence of the top NiSi and $YSi_2$ stacked gate layers on the gate workfunction of the capacitor structure will gradually diminish as they are shielded from the $SiO_2$ interface. As a result the effective chemical potential of the gate stack shown in equation (1) approaches that of pure Y as the effect of Y becomes dominant. When the thickness of the unreacted Y layer reaches a critical value, which corresponds to about 1.6 nm in our study (use the one near saturation), the contribution of the NiSi and YiSi layer on the workfunction will be completely eliminated. This effectively allows the workfunction to be tuned from a value of about 4.7 eV of a pure NiSi close to that of pure Y.

Although the observations suggest that the chemical potential of the bottom layer material has a very dominant effect on the effective gate workfunction in equation (1), it should be noted that based on Figure 3, the gate workfunction with a Y interlayer does not reach the value of a pure Y workfunction (i.e. but slightly higher). This could be explained by the formation of interface dipole during the high temperature annealing

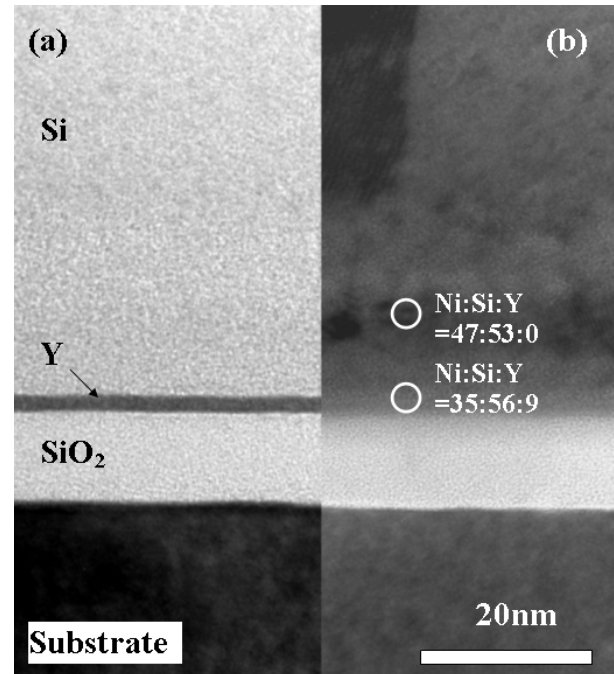


Fig. 4 TEM graph for (a) as-deposited Ni/Si/Y(1.6nm)/$SiO_2$ sample and, (b) after RTP. The TEM/EDS analysis suggests that the Y content remains high at FUSI gate bottom after RTA.

process which increased the saturation value of the workfunction by ~0.15 eV.

## IV. CONCLUSION

In summary, it was found that an ultrathin yttrium interlayer introduced between a $SiO_2$ gate dielectric and a Ni-silicided FUSI gate can effectively tune the FUSI gate workfunction from 4.69 eV to about 3.56eV. As the introduction of Y layer is CMOS compatible, the resultant gate structures can lead to an effective FUSI gate workfunction of 4.08 eV which is ideal for the n-MOSFETs applications. We found that the chemical potential at the FUSI/gate dielectrics interface play a dominant role in determining the localized workfunction in FUSI gate.

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