# Microprocessor Manufacturing Throughput Time Variability

by
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B.S. Mechanical Engineering, University of California - Berkeley, 1989

Submitted to the Sloan School of Management and the Department of Mechanical Engineering in partial fulfillment of the requirements for the degrees of Master of Science in Management and Master of Science in Mechanical Engineering

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and the
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## Abstract

Variability in manufacturing throughput times creates factory performance fluctuations that contribute to poor customer service. Recognizing the importance of on-time delivery in customer satisfaction, Intel wants to use the concept of variability to make better, more accurate planning and scheduling decisions.

This project examines the manufacturing throughput times for five microprocessor products which Intel makes. The analysis follows the same five products through the four manufacturing stages of wafer fabrication, wafer sort, assembly, and test in Intel's production process. Lot-for-lot transaction information directly from the factory shop floor tracking systems provides the cycle time data.

The analysis characterizes the overall throughput time and variability for each production stage. The individual lot throughput times generate summary statistics and distributions which show the variability for the different stages, the different processes run in each stage, and the selected microprocessor products. The analysis compares actual throughput time distributions with common mathematical models such as the normal and gamma distribution. Aggregate data analysis shows the difficulty in predicting manufacturing throughput times from past performance.

In addition to the variability characterization, a deeper analysis occurs for the wafer fabrication stage. Examining potential throughput time variability sources exhibited in this stage results in a description of the various shop floor prioritization rules and incentives. Individual lot entry and exit events show how processing selections affect the factory flow and the individual throughput times. Correlations between factory inventory levels and throughput times show some relationship between these two indicators.

The different sources of variability uncovered during this project helps highlight areas for further investigation. The variability information also provides the inputs for a new manufacturing planning and scheduling system. By incorporating throughput time variability in the scheduling decisions, Intel can make the tradeoffs between the probability of on time delivery and the expected manufacturing leadtime to better satisfy customers.

Thesis Supervisors: Professor Stephen C. Graves, Management
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# Chapter 1 - Introduction and Overview

## *Company Background and Industry History*

Intel sits atop the semiconductor industry, ranking #93 on the Fortune 500, with estimated net revenues of over $8 billion for 1993. As the world's largest computer chip maker, Intel components appear in products ranging from automobiles and automated teller machines to the newest personal computers and personal digital assistants. But when Robert Noyce and Gordon Moore founded Intel twenty-five years ago in 1968, the semiconductor industry was still in its infancy. The large scale integration of transistors onto silicon was just an emerging business with an uncertain future.

Intel pioneered semiconductor memories, and the company faced the challenge of having to develop both the manufacturing process technology and the product design simultaneously. By the mid-1970's Intel had invented the first microprocessor, but it was IBM's choice of the Intel 8088 microprocessor as the brains of the first IBM PC in the early 1980's that really launched Intel's microprocessor business.

The overwhelming popularity of the IBM PC cemented Intel's microprocessor architecture, now in its fifth generation with the Pentium™ processor, as the dominant design for the world's personal computers. Spawning dozens of corporations, personal computer sales have entered into mass-market and retail distribution channels, with Intel selling tens of millions of microprocessors a year.

## *The New Computer Industry*

With the tremendous growth in the computer industry over the past years, competition has increased and customer service has become an important priority for both computer manufacturers and their component suppliers. With personal computer use becoming more widespread, manufacturers increasingly compete on price and availability. In response, they employ more just-in-time manufacturing methods and demand 100% on time delivery to the exact day specified. Manufacturers no longer tolerate late deliveries, and few accept early deliveries. This forces the suppliers to deliver better customer service.

As the world's largest semiconductor manufacturing firm, Intel supplies the microprocessors that power over 70% of the worlds personal computers in addition to a variety of other semiconductor-based products. Despite the tremendous success of the company's product lines, Intel's largest complaint is delivery performance. The inconsistent and mostly disappointing progress in improving the company's "Vendor of Choice" indicator (the percentage of customers rating Intel as an excellent or primary supplier), makes customer service a high priority.

Service and delivery become even more important with the threat of new competition in the microprocessor marketplace. Many companies are interested in producing products to compete with Intel's main microprocessors. For example, the new PowerPC™ chip poses the threat of lower demand and narrower profit margins. Japanese firms have also shown a renewed interest in the lucrative microprocessor business.

For Intel, uncertainty in manufacturing throughput times contributes to poor customer service. With the increasing competition in the semiconductor industry, the ability to deliver a high level of customer service will differentiate the players. On time delivery plays a key role in customer satisfaction, and the ability to more accurately schedule manufacturing capacity will help enable better on time delivery.

### *The New Planning System*

In response to this need for better customer service, the company began an effort to develop a new manufacturing planning system. Known as the Integral Planning and Delivery System, or Integral, the new system represents paradigm shifts for Intel in both planning concepts and planning systems.

Instead of building up a large finished good inventory for delivery to the customers, the prioritized customer demand will get matched directly to the expected factory supply. Planning will occur in daily or weekly, rather than monthly, cycles, and a detailed capacity analysis will help schedule orders.

To ensure orders get filled on time, the systems must accurately predict the timing of factory supply output and match it with the customer demand. Thus, the new planning system incorporates manufacturing throughput time variability in determining the probability the expected output date meets the order due date.

### *Project Overview*

This project focuses on characterizing the throughput time variability exhibited by the different manufacturing operations. Ultimately, this information will provide the inputs for the new planning and scheduling system and the methodology for determining capacity consumption. Beyond the overall description of the variability, the analysis highlights some of the potential sources of variability.

The project examines the manufacturing throughput times for five microprocessor products which Intel produces. The analysis follows the same five products through the four-factory manufacturing process of wafer fabrication, wafer sort, assembly, and test. Lot-for-lot transaction information collected directly from the factory shop floor tracking systems provide the necessary data to calculate throughput times.

The analysis characterizes the overall throughput time and variability for each production stage. The individual lot throughput times generate summary statistics and distributions which show the variability for the different stages, the different processes run in each stage, and the selected microprocessor products. In an attempt to determine the predictability of throughput times, the analysis compares actual throughput time distributions with common mathematical models such as the normal and gamma distribution as well as evaluates correlations between past performance and throughput times. In addition, the analysis examines the relationship between factory inventory levels and throughput times.

In addition to the variability characterization, a deeper analysis occurs of the wafer fabrication stage. Examining potential throughput time variability sources results in a description of the various shop floor prioritization rules and incentives. Individual lot entry and exit events show how processing selections affect the factory flow and the individual throughput times.

### *Company Impacts*

A fundamental business change will result from the knowledge and use of throughput time variability information in planning and scheduling. The ability to make tradeoffs between the scheduled leadtime and the customer service level distinguishes the new system from traditional order scheduling. Through some criteria, orders will get ranked in terms of importance for on-time delivery. Based on this ranking, different levels of customer service can be associated with each order. Selecting different levels of customer service associates a different planned leadtime with an order; a leadtime based on the distribution of actual factory performance data rather than single point estimates. Intel feels that using a distribution rather than just a point estimate will significantly improve delivery performance.

The current system vision uses the throughput time distribution information to assist the sales and marketing organization choose expected completion dates for orders taken. Intel feels that because throughput times determine expected completion dates, the organization that communicates those dates to the customers would better understand the tradeoffs between choosing a longer or shorter time, and the probability of meeting that time. The long run goal for the system involves including current factory conditions, such as the current work in process level, the current product mix, or the expected available capacity, in determining when to expect lot completions.

### *Variability Sources*

Highlighting the sources of variability represents another key benefit in examining factory throughput times. Determining the causes of variation helps define the critical parameters that enable leadtime predictability. Examining the different dispatching and work scheduling rules helps build an understanding of the fundamental practices that contribute

to different throughput times. Helping pinpoint the relationship between factory practices and the throughput time variability leads to opportunities for further investigation.

### *Future Directions*

In addition to including factory conditions in the prediction of throughput times, variability concepts touch a number of potential areas for further investigation, such as:

- Determining inventory levels
- Executing integrated order commits
- Guiding internal factory analyses
- Including yield variability in planning

Understanding the factory output variability can help determine optimally sized inventory buffers to minimize the expense of both shortfalls and surpluses. Strategic location of these inventories can insulate the customers from some of the effects of factory variability.

The ultimate vision for the new planning and delivery system is known as "Integrated Commit". This process allows for the receipt and scheduling of a customer order on-line.

The factory throughput time variability analysis done for this project can also guide subsequent studies on individual factories and their internal workings. Studying an individual factory in-depth can help pinpoint the sources of extreme variability which impact customer service.

Finally, factory and process yields represent another important planning parameter which exhibits variability. A yield analysis can use the same methods used to analyze and characterize the variability in factory throughput times. Thus, factory planning can occur while using the major sources of manufacturing variability.

Understanding manufacturing throughput time variability helps enable better delivery performance. Since variability affects areas ranging from order scheduling to capacity modeling, including variability information in planning and scheduling results in more reality-based decision making. In addition to enabling better decision making, focusing on variability issues helps target the sources of variability. Reducing variability levels increases planning accuracy and makes the entire manufacturing process more predictable.

Customer service has become an important competitive element in the new computer industry. The ability to accurately plan, schedule, and promise delivery to the customer represents not a source of competitive advantage, but a basic requirement for industry participation.

## Chapter 2 - Manufacturing at Intel

Understanding the role of throughput times in planning and scheduling manufacturing activities requires an understanding of the production systems being analyzed. The brief summary of Intel's organization and its semiconductor production process that follows provides the necessary background for understanding the source of the throughput time information studied. Rather than provide a detailed description of the different processes, this chapter highlights the major activities performed by each organization in the manufacturing of Intel's semiconductor components.

### *Intel Corporate Structure*

In a simplistic way, the Intel organization consists of four major functional groups falling under the control of the Office of the President. Figure 2.1 shows these four areas as Technology Development, Product-line Divisions, Sales and Marketing, and Manufacturing.

The Technology Development (TD) organization defines the basic sequence of chemical and mechanical steps used to fabricate semiconductors as well as the different processes and materials used in the different factories. The TD group defines both the process operations and the equipment employed. In addition to holding responsibility for choosing the proper mix of technologies to ensure the consistent production of the latest designs, TD also defines a set of design rules that the product-line divisions must follow in creating the next generation of product.

The Product-line Divisions (Divisions) represent the profit and loss centers for the company. Each division holds responsibility for the design and marketing of its product line. The divisions not only design new products, but also help define the product manufacturing. For example, the division will define which package a chip uses,

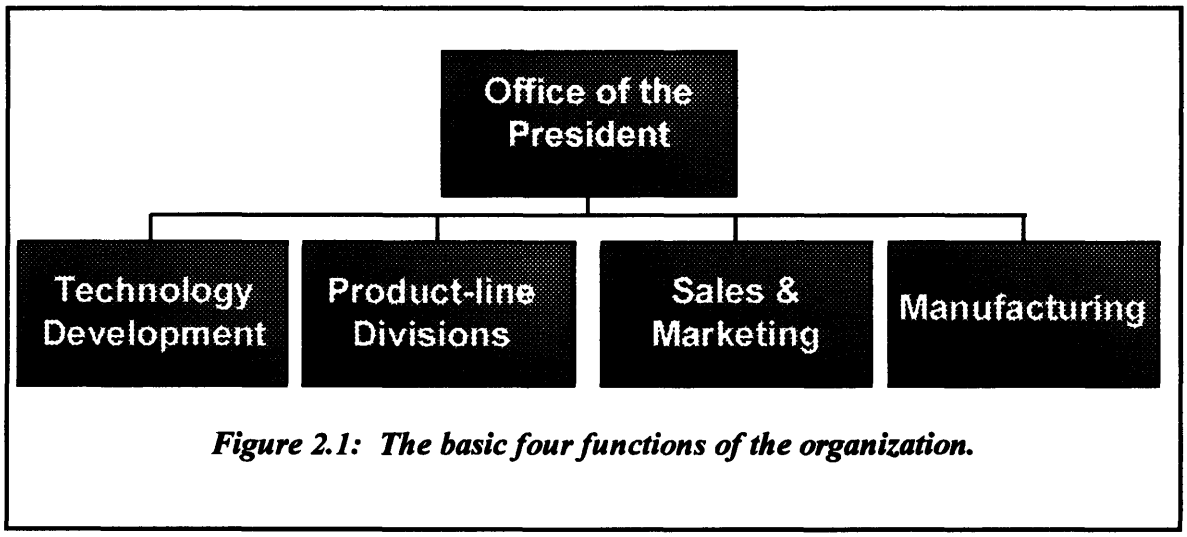


***Figure 2.1: The basic four functions of the organization.***

considering issues like heat dissipation, cost, and reliability.

Known as geographies because of the way they divide up the world, the Sales & Marketing regions consist of the Americas, Europe, Asia-Pacific, and Japan. As the company's link to the customer, each geography accepts and manages the customer orders and needs for the geographic region it serves. Geographies provide the demand forecasts that the manufacturing organization tries to meet. The geographies also hold responsibility for customer satisfaction, and therefore control the finished goods inventory.

### *The Manufacturing Organization*

Intel produces some 22,000 unique end items starting from around 500 silicon-based products in factories located in the U.S., Europe, and the Far East. In addition to the familiar microprocessors found in personal computers, Intel produces memory components, embedded microcontrollers, and multimedia and supercomputing processors.

The manufacturing organization exists as a cost center that supports the different product divisions. Manufacturing accepts new products designed by the divisions and manufactures them employing new processes developed by the technology development group.

Manufacturing builds Intel's various products in quantities specified by the manufacturing planning organization. Forecasts of the sales & marketing organizations, guided by product-line strategies, provide the basis for the manufacturing volumes.

### *The Four Factory Production Chain*

Intel's manufacturing process consists of a four-factory chain which takes raw silicon wafers and turns them into chips. While subtle differences exist in the processes used depending on the type of chip, the general description that follows applies for Intel's microprocessor manufacturing. Figure 2.2 shows the four production stages along with the two primary inventory locations for the manufacturing process. Any individual factory runs a number of different processes, each having an expected throughput time. Due to the different flows through the factory, the actual throughput times range above and below this expectation with some variability.

While each factory houses a single stage of the production process, in most instances fab and sort factories are collocated as are assembly and test factories. Eight major locations (both domestic and international) process wafers which get sent to one of three major assembly/test sites.

The chip making process begins with the fabrication factory, or fab, where products spend the bulk of the total manufacturing time. Whole silicon wafers, as the substrate material of semiconductor devices, undergo a series of precisely chemically engineered steps.

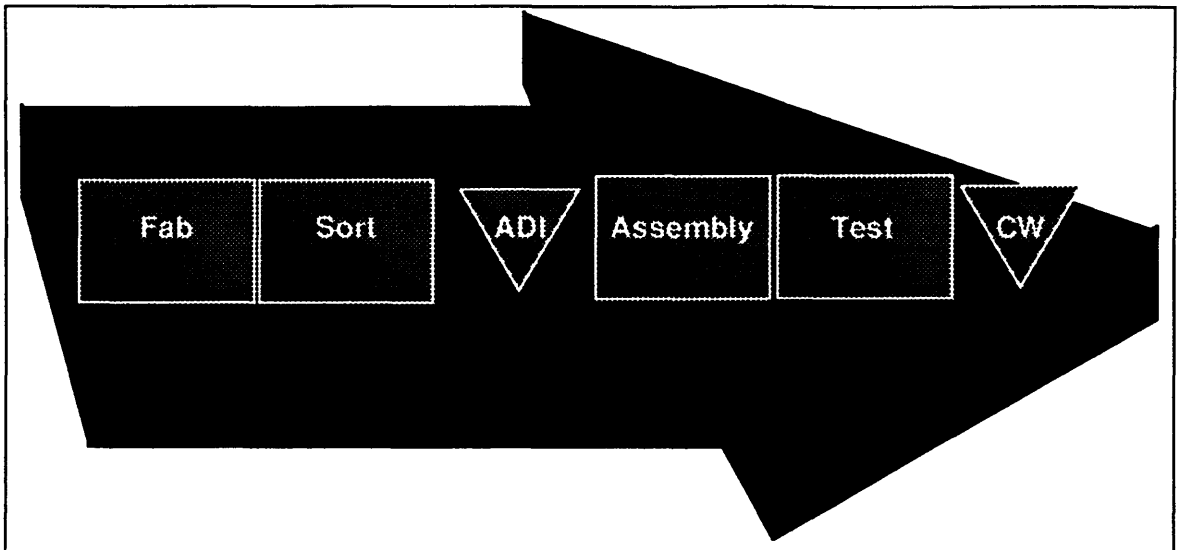


***Figure 2.2: Intel's four-factory production process flow with primary inventory points. Typically, fab and sort factories are collocated as are assembly and test factories.***

Processes such as photolithography, chemical vapor deposition, and ion implantation add or subtract material in different layers to create the complex microelectronic circuitry of a chip.

Typically wafers travel through fab in lots of 25 wafers. All wafers in a lot undergo identical processing, and produce a single product. Wafers may be 4, 6, or 8 inches in diameter and, depending on the complexity of the product, hold hundreds of individual squares known as die, where each die represents a potential chip.

Each fab houses equipment for a certain level of sophistication, with newer equipment producing the latest products. The wafer fabrication for Intel's products gets distributed among the different factories considering both the fab's technological capability and production capacity. In addition, except for very new or very old products, no one factory will produce all the volume of any single product which minimizes the risk in the event of disaster.

Once the wafers complete the many, often over 150, fabrication steps, the lot moves to the sort factory. In sort, each individual die on a wafer gets electrically probed to test the success of the manufacturing process. A number of electrical leads from an electronic tester make physical contact with the die and perform a functional test. If a chip does not operate as expected, the tester deposits a dot of ink, marking the chip as bad so it will not undergo further processing.

The time a lot takes to travel through the probe step of the sort factory depends on the number of individual die per wafer. Testing each and every die means the more die per

wafer, the longer the processing time. In general, however, the time spent in sort represents the least amount of all the factories.

Once sorted, the lot then feeds the first primary inventory point known as assembly die inventory (ADI). Located at each assembly site, ADI serves as a decoupling point between the first two manufacturing stages and the last two. The buffering inventory absorbs any fluctuations in either the manufacturing process and transportation time upstream or the assembly and test process, finished goods inventory, and customer demand downstream.

The assembly factory actually encases the silicon chip in a ceramic or plastic package to create a usable chip. A diamond toothed cutter saws whole wafers into individual die and then the unmarked, good die get attached to the package leadframes. Ultra-thin wire bonds connect the silicon die to the metal leads and the package is sealed, readying the chip for use. Chips must also pass quality tests including hot/cold and gross/fine package leakage.

Lot sizes during the assembly stage vary depending on the size and weight of the package. Depending on the fab/sort production yield (the number of good die per wafer processed) as well as the package type, wafer lots may be split or combined to form correctly sized assembly lots.

The test factory creates the finished product that customers see. Both internal electronic operation (clock speed, voltage range) and environmental performance abilities (temperature, humidity) determine the price Intel can charge for a chip. In contrast to the sort factory, where only a functional test gets performed, now that the chip can be plugged in and used, it undergoes a much more sensitive testing regimen. The test factory measures the speed and performance characteristics of each chip to both classify the products and reaffirm functionality. Since the tests segregate chips with different performance characteristics, lots will again be split or combined depending on the yields of the different performance levels.

To ensure quality, units undergo an environmental and electronic stress test known as burn-in. The test factory also labels the chips with identifying marks and sometimes with either the generic Intel logo or a customer specific design. The units then get packaged into tubes, trays, or reels and boxed for shipping.

The factory components warehouse stores the now ready for sale chips. In some cases, the products get shipped directly from this point, but more often, the units get transferred to a distribution center. In many cases the factory inventory and distribution location may be identical, and only a logical distinction separates the inventories, where the manufacturing organization controls factory inventory and the geography controls the distribution inventory. The majority of customer orders get filled from geographic distribution inventory.

*Where Does the Time Go?*

Any item spends the majority of its manufacturing throughput time in fabrication, with most of the time there spent waiting in queue. For most products, the time spent in fab accounts for over half the manufacturing time. Depending on the product complexity, wafer lots can spend anywhere from 10 to 60 days in a fab. For comparison, typical times spent in either the sort, assembly, or test factories can range from less than one day to two weeks.

The complexity of the processes run in fab dictate the long throughput times. Even when only a few processes run in a fab, the processes re-use the same pieces of equipment several times, which means time must be spent waiting for machine availability. Fab throughput times observed were 1.5 to 6 times the theoretical minimum time. In general, a typical product will spend three to five times its theoretical minimum going through the fab. This means a lot spends some 75% of its time in the fab waiting in queue.

The amount of time spent in the fab depends on the loading of the factory. In cases where the fab is not capacity constrained, the factories can make more setup changes and the lots can run at much closer to their theoretical throughput time. For those factories running at maximum capacity, the amount of activity and work in process results in longer runs with fewer setups, more waiting, and longer throughput times.

For sort, the throughput time depends more on the number of die per wafer, which determines how long a lot takes to process. In addition, since lots require only a few processing steps, machine availability constraints also impact the amount of time a lot takes to run through the sort factory. In sort, with actual processing times measured in minutes or hours but throughput times in days, a lot spends over 90% of the time waiting in queue.

In assembly and test, the type of package and the number of leads govern its throughput time. Highly complex packages increase the assembly processing time, while tester availability for the more complex packages constrains the test throughput. In addition, the number of processing steps, each with significant processing time, means more opportunities for a lot to wait in queue. Like the fab, the assembly and test factories try to minimize the number of setups, and the expected throughput times fall in the same range of 1.5 to 6 times the theoretical minimum throughput time.

Most of Intel's semiconductor products traverse the four-factory manufacturing process. With the number of different factories all running a number of different processes for a tremendous number of different products, the problems faced by planning and scheduling due to differences in factory throughput times become apparent.

## Chapter 3 - The Current Planning and Scheduling Process

Understanding why Intel undertook the effort to replace its current planning and scheduling system with the new Integral system under development requires a brief overview of the current process. This chapter attempts to highlight those reasons in describing the organization, the information flow, and the roles and responsibilities each group has within the customer order to product delivery cycle for the current planning process.

### *The Planning Organization*

From a manufacturing planning perspective, the Intel organization reduces into three distinct groups: geographies, divisions, and manufacturing.

The geographies represent the company's link to the customer, and have accountability for customer satisfaction. Dividing the world up into different areas, the geographies are responsible for the sales forecasts for all products in their part of the world. The geographies also take and enter customer orders into the system.

Each division holds responsibility for a specific product line or product set. The divisions determine product strategy and pricing, and define the aggregate plan based on all forecasts from the various geographies. Thus, a division planner communicates the desired quantities for the division's product line considering the overall product strategy.

Manufacturing builds the actual products, with factories adjusting the mix and volume in an attempt to meet the build plan. The factories have autonomy in executing the production plans, and only need to meet their build targets on a weekly basis as committed once a month.

### *The Planning Cycle*

The current planning cycle occurs on a monthly basis, and takes about three weeks to complete. The cycle begins with the geographic planners submitting a forecast for every product line over the planning horizon. These forecasts account for actual customer order backlog, inventory replenishments, and anticipated business.

Each division collects the forecasts from the geographies and aggregates them into a single forecast. The divisions then adjust the plan based on the specific product strategy. For example, an upcoming price change may increase the anticipated sales of a product, so more should be planned. A product may be phasing out, so less should be planned. A new product may not be selling now, but anticipation inventory is desired so more should be planned. The manufacturing organization cannot use the unadjusted demand forecast to load their factories directly because near-term opportunities in the marketplace often

conflict with long term product strategy. Using purely short-term financial measures may sacrifice a future position for short-term gain.

The desire to convert the marketplace from an old technology to a new technology shows how two different product strategies can conflict. While immediate financial gains could result from continuing to sell an older product, restricting its supply generates new demand for (and frees up manufacturing capacity to produce) a newer product.

Once each division compiles the geographic forecasts and adjusts for individual product strategies, the divisions bring the adjusted plans to a meeting with all the other divisions. At this meeting, each division's plans get modified again in an attempt to fit as much production as possible into the available capacity. It is essentially a chance for each division to "fight for their products" to get as much capacity as possible to meet their targets. This meeting also represents Intel's attempt to rationalize the production with the overall corporate strategy in mind.

These re-revised plans then go to a central master scheduling office. The master scheduling office acts as the liaison between the individual divisions and the factories. The master scheduling office takes the build plans from the divisions and distributes the quantities amongst the factories based on each factory's capacity and capabilities. For example, production of a microprocessor requiring sub-micron technology must occur at a factory with that technology. Some products can be produced at only a few sites, some at many. The master scheduling office also divides the production of any one product as a means of spreading risk.

The factories then commit to the build plan. A customer service planner will then segment the factory outputs to the different geographies. This lets the geographies know what to expect per their forecasts. Each factory is responsible for its detailed near term schedule, which gets created from the first two months of the build plan. This drives the ordering of supporting materials, packaging, etc. Since factories set their own short-term schedule based on the current forecast, they have little visibility (other than demand forecast due dates) into the priority of any particular order. Expediting occurs on an ad hoc basis.

Because of the long leadtimes required for production, the farther up the factory chain away from the end customer, the harder it becomes to drive the schedule with firm orders. Thus, fab/sort sites tend to work more from forecasts, supplying products into the large, buffering assembly die inventory in the middle of the factory chain.

### *Managing Customer Orders*

From the order entry side, orders get taken by the geographies and input into the sales tracking system (STAR). Currently, committed factory output is known only for the current month and the next month. If an ordered product is unavailable during that two month window, the customer is given a promise date using a standard leadtime. This

leadtime gets chosen without accounting for the current demand for a product, or the planned production. The promise dates get set using the following process:

1. Customer calls in order and requests due date (Date #1).
2. If the uncommitted supply within the requested leadtime can fill the order, then the geography takes the order to support the first date (Date #1). Otherwise, Intel checks standard leadtime and commits to another date (Date #2). This date rarely matches the customer requested date, and is never early. The standard leadtime does not accurately account for available supply or capacity constraints, nor does it have any regard for specific product or order characteristics.
3. If the manufacturing runs late or a different factory schedule takes precedence, a revised commit date gets entered (Date #3). The date can change multiple times with no apparent penalty.
4. On time delivery gets measured based on whether the shipment was "on-time" relative to the final commit date, not the original commit date.
5. Since customers expect poor delivery performance, they request earlier delivery than they truly require hoping the late delivery will be closer to their actual need date. This, of course, only leads to more congestion in the factory.

Contractual agreements dictate whether customers can revise orders and by how much. Some contracts allow up to a 50% increase, known as an upside, to a 100% decrease in order quantity. The contracts also state how long before the delivery date a customer may change an order. The frequency of customer revisions to orders depends on the product. The more customer specific the product, the less likely order specifications will change. More generic products like microprocessors may get revised based on fluctuations in consumer demand, by changes in the product mix, or by availability of substitutes from other suppliers.

This kind of behavior towards customer satisfaction represents just one illustration of the problems faced by the current planning and scheduling process. The customers need better customer service to remain competitive in their industry. Intel needs to deliver better customer service to remain competitive in its industry.

### *The Changing Customer Environment*

Computer manufacturers that rely on Intel as the supplier of the primary components for their products face tremendous challenges in the increasingly competitive PC market. Intel's most important strategic customers all compete with each other in a market that exhibits tremendous price sensitivity and little brand loyalty.

These conditions create tremendous demand fluctuations for the PC manufacturers that make forecasting both order volume and product mix difficult. But since cost competitiveness drives sales, the manufacturers minimize inventories and employ just-in-time methods. Manufacturers now demand 100% on time delivery, with little tolerance for either late or *early* shipments. Because of Intel's poor delivery performance history,

some customers have even requested Intel to stock on consignment. This forces Intel to carry all the risk and burden in order to guarantee customer satisfaction.

As the key supplier to its customer's operations, Intel must respond to its customer demands. It not only bears the burden of starving a customer's production line when shipments arrive late and holding inventory when shipments arrive early, but also must respond to the same changes in order mix and volume faced by the computer manufacturers.

Increasing product complexity and higher customer sophistication add to Intel's challenge. As with most firms, the customer can specify not only the product specifications, but also the delivery terms. Thus, a customer order for 100,000 units may get shipped in 10,000 unit increments over time, or it may get shipped all at once after being held in inventory until a sufficient quantity is built (the more common scenario at Intel). This means Intel must manage the production of the large orders while meeting the customer's product specifications, carrying the cost of the inventory, and delivering on time.

In addition, many core products will have companion or supporting products that enhance performance. Customers that need both the main and the companion chips order them together in matched quantities. Since Intel must ship these bundled items together -- items that often have very different throughput times, volumes, yields, and processing -- the production must again be closely coordinated to ensure on time delivery.

### *Current System Drawbacks*

These customer order fluctuations create tremendous production difficulty for Intel because the current planning cycle occurs only monthly. When a customer's demand volume or mix changes, the manufacturing organization cannot react quickly enough because the factory mix and volume for the current month were committed during the previous month's planning cycle. This means any changes only get reflected during the next planning cycle having actual output, or at best during the next month's production. When the customers demand weekly deliveries, reflecting changes on a monthly basis becomes unacceptable.

The demand fluctuations and the monthly cycle create even more problems further up the production chain. When the factory throughput times in the fabrication stage run upwards of 60 days, production must begin based on forecasts for what products will be needed two months out.

Within the current planning system itself, the changes that occur over each month create still more problems. Since the information only gets updated monthly, maintaining the numerous changes over time becomes an unwieldy task. Many of these changes don't get reflected in the current plan, so decisions made on what appears in the system could be based on incorrect or inaccurate information.

As an example, while the factory output is determined on a weekly basis, the commitment process only occurs monthly. This means the amount of knowledge of upcoming factory output can vary from the next 8 weeks (just after the cycle completes) down to just the next 4 weeks (just before the next cycle completes). This shrinking and growing of the product availability sometimes impacts Intel's ability to schedule customer requests. If a customer order was desired in six weeks, but at the time Intel only had visibility of the next 5 weeks of factory output, that order would get scheduled for sometime in what is currently the third month of the schedule. Once the planning cycle completed, that order may be satisfied during the early part or the later part of what becomes weeks 5-8 of the new schedule. Satisfying customers with accurate on time delivery becomes impossible without better visibility to production output.

Intel faces the same challenges as its customers. In order to maintain a competitive position, the company must manage inventory costs and become flexible and responsive to its customers. This conflicts with holding more inventory to ensure customer satisfaction through on time delivery. The costs of holding extra inventory coupled with the costs of lost business due to mismatched supply demonstrate the need of a more accurate and flexible planning system.

## Chapter 4 - The Next Generation Planning System (Integral)

Incorporating manufacturing throughput time variability represents just one of many changes that the next generation planning system will bring. As the previous chapter indicated, several areas of the current planning process require improvement. This chapter describes the changes the new system brings, its underlying philosophy, and more specifically where the throughput time variability concept impacts the development.

### *Addressing Customer Needs*

Manufacturing planning systems rarely address variability in making scheduling decisions. Typically, only average values determine decisions about manufacturing leadtimes and expected delivery dates. With a variable manufacturing process, the actual values fall above and below these average values in a distribution, with some orders arriving early and some arriving late. If planning and scheduling occurs using only point estimates for leadtimes, these estimates often become inflated in an attempt to minimize the effect of factory fluctuations. This impacts customer service by creating factory schedules using only higher than average times, which result in longer throughput times and higher work in process inventories.

The problem of high work in process inventories and long leadtimes gets exacerbated when the products being produced do not match the customer's needs. This occurs at Intel because the current planning system runs on a monthly cycle and sets factory schedules based on a fixed monthly forecast. Because of the dynamic nature of the computer manufacturing industry, these monthly forecasts often commit the factories to the wrong mix or volume of products, and the monthly planning cycle means changes to customer orders or factory schedules take too long to become reflected in a new plan.

With the ever-evolving nature of the microprocessor business, current products become obsolete very quickly so having excess inventory can be costly. The costs of excess inventory coupled with the costs of lost business due to mismatched supply demonstrate the need for a more accurate and flexible planning system.

In response to the need for better customer service, Intel began an effort to develop a new manufacturing planning system. Touted as the company's next generation planning system, it addressed both how to better serve the external customers purchasing Intel's products and how to better serve the internal system users (geographies, divisions, factories) in enabling better delivery performance. Known as the Integral Planning and Delivery System, or Integral, the new system represents paradigm shifts for Intel in both planning concepts and planning systems.

The Integral team undertook a two-pronged approach to address the different paradigm shifts. First, modernizing the basic planning principles enables a change in the planning

process. Second, the use of distributed databases in a client-server environment provides a better, more flexible system that will replace old, obsolete ones.

In modernizing the planning principles, the Integral team outlined a handful of key goals which address the critical shortcoming of the current system. Those goals are:

- Daily build-to-order capability in assembly and test factories
- Daily, lot-level work in process and inventory visibility
- Weekly overall planning cycle with daily updates
- Demand prioritized factory loading
- Link to Intel capacity model

Addressing the problems of the current system and achieving the above goals brought a new approach to planning at Intel. The order mapping process lies at the heart of this new approach. The order mapping process links customer orders directly to current work in process through an order prioritization scheme. Managing this order mapping process requires accurate factory supply information as well as a good capacity model to predict when that current work in process will complete.

Rather than build up a large finished goods inventory for delivery to the customers, the prioritized, real customer demand will get matched directly to the known, capacity feasible factory supply. Most completed orders will ship from the finishing factory straight to the customer, eliminating the unnecessary expense, time, and handling of the majority of finished goods inventories.

In enabling better access to more accurate information, the new system provides fewer opportunities for manual intervention and the introduction of errors. Using shorter time buckets, where planning will occur in weekly rather than monthly cycles, means the system reflects changes sooner and more often, minimizing the impact of drastic changes. This makes the planning groups more responsive, since having better insight to the current production status means more accurate information to make decisions.

### *Manufacturing Performance Linked to Customer Service*

The decisions using the new build to order concept now have an explicit link to on-time delivery. Forging a link between manufacturing performance and customer delivery performance, the implementation of a new planning system enables the examination of the factory metrics used to judge its execution.

In order to ensure orders get filled on time, the system must accurately predict the timing of factory supply output and match it with the customer demand. A detailed capacity analysis helps accomplish this task. As part of this capacity analysis, the new planning system must incorporate manufacturing throughput time variability.

### *Including Variability Concepts in Planning*

Addressing variability occurs in several different areas within the new planning system such as:

- Order scheduling and order mapping
- Capacity resource consumption
- Variability highlighting
- Planning parameter comparison

Understanding throughput time variability helps the order scheduling and order mapping process because estimating the leadtime of a lot through the factory plays an important role in scheduling an order. Just using point estimates does not capture the stochastic nature of the leadtimes, which provides the motivation for including variability. The factory leadtime estimates help determine when to expect a particular lot out of a factory, and whether that lot can satisfy a particular customer order. Including some estimate of the variability helps determine a range of expectations for potential delivery, which planners can use to make more accurate scheduling decisions.

Variability also plays an important role in capacity scheduling. In much the same way that current work in process gets scheduled to satisfy customer orders, that same factory supply gets scheduled through critical capacity resources. Accurate capacity scheduling means predicting when a particular lot will consume a critical factory resource. Understanding the variability of throughput times gives a better estimate of the timing for resource utilization.

Having characterized the throughput time variability through the different factories also helps highlight extremely variable areas for process improvement. In addition to cycle time reduction, controlling throughput time variability represents a key to successfully executing a build-to-order strategy. The more predictable a manufacturing process, the more accurately it can be scheduled.

Finally, analyzing the throughput times will directly result in means (averages) and variances calculated using actual factory data. These actual values provide a basis for comparison against the estimates currently used by the manufacturing planning systems. Using planning parameters based on actual data will help move the planning decisions to more reality-based information.

The above discussion provides the motivation for studying the manufacturing throughput time variability. In the sections that follow, the actual throughput times are analyzed as well as the potential sources for the variability. In addition, Chapter six provides a methodology for the use of the information.

## Chapter 5 - Throughput Time Data Analysis

Characterizing the manufacturing throughput time variability for Intel's various operations requires an analysis of factory data. This chapter describes the factory data collection and analysis. It describes the information sources, the types of products produced, the different processes run, and the typical leadtime expectations.

In conducting this analysis, each factory was treated as an essentially independent "black box", where lot entry and exit time stamps determine the throughput times. This project excludes the transportation times between the different factories and the amount of time spent waiting to enter a given factory as part of the throughput time analysis. While these times certainly exhibit variability, and often make up a significant portion of the total leadtime, the focus for this analysis was to characterize the throughput time variability for the actual manufacturing time spent inside each factory.

### *Collecting Factory Information*

As discussed in Chapter 3, each factory operates independently in trying to meet its output goal for the current month as determined during the planning cycle. Since each factory can act independently, each site runs an independent shop floor execution system. These shop floor execution systems track the progress of work in process lots through the various manufacturing operations. The systems keep a tally of the location, status, and the extent of completion for each lot in a factory.

The central planning system requires inputs from the independent factory systems to update its information on available factory supply. An automated computer program extracts the shop floor tracking transactions directly from the factory system and feeds them to the central planning system through a data transfer process.

In addition to feeding the central planning system, the same data in the extract files also provides lot-for-lot throughput time information, which forms the basis for this analysis. A custom program scans the transaction extract file, matching the entering and exiting transactions for a given manufacturing lot (eliminating all the in-process transactions). For example, in the case of the fab, the entering transaction corresponds to issuing raw silicon wafers to the shop floor, and the exiting transaction corresponds to the receipt of the lot back to the stockroom between fab and sort. In all cases, the initial entering transaction would not occur if the raw materials were unavailable, but the calculated throughput times include any impacts of materials shortages or machine breakdowns while in process.

Calculating the difference between the date and time a lot enters the factory and the corresponding date and time it exits the factory determines its throughput time. In most cases, since the factories examined work a seven-day-per-week schedule, calculating the entry and exit time difference provided the throughput time. However, in those cases where a holiday or factory shutdown occurred, that time was eliminated from the

calculation. Along with the matched entry and exit date, the extract file provides the manufacturing product identifier for sorting out the different products.

Because the date and time stamp marking the entry and exit transactions held not only the date, but also the hour, minute, and second the transaction occurred, the difference could be calculated to the second. In conducting this analysis, differences were maintained as raw decimal numbers which were used in calculating the summary statistics. These statistics were rounded to the nearest tenth for presentation and comparison. Units of days were used since planning occurs using days as the time increment. The nearest tenth was used because any finer detail implies accuracy in the throughput time that cannot necessarily be assumed. Thus, any average throughput time has a tolerance window of one tenth of a day, or 2.4 hours.

Data collection, otherwise known as the scanning of the lot transaction files, began in mid-May and continued through late October. Only those production lots that entered a factory on or after the mid-May start date and completed on or before the data collection cutoff date appear in the lot sample. Since production lots tend to receive priority processing in the factory, special engineering or test lots do not appear in the analysis.

The data collection process for one of the factories providing data for this project was examined during a visit to the facility. The data collected was compared with the actual calculated times done at the factory as well as with the data from other factories not used in this analysis. These comparisons verified the validity of the data collected and used in this analysis.

### *Factory Fundamentals*

As described in Chapter 2, the Intel manufacturing process consists of a four-factory production chain: fab, sort, assembly, and test. For this particular project, the analysis follows the same order as the four production stages. Beginning with the fabrication factory, overall throughput time data provided the basis for analyzing a handful of key products. From the total data set, a detailed data analysis occurred for five high volume products. The analysis examines each product through each of the four stages. Table 5.1 lists the five products and their typical applications. Table 5.2 shows the factories which provided data for the detailed analyses.

The five products examined represent some of the key revenue generating products for the company. The core family of microprocessors will ship some 40 million units in 1993, while Intel's newest microprocessor has just begun to ship in full production volumes. These products take up a significant portion of microprocessor production capacity for the company.

Each factory of each type runs a number of different processes that represent production flows through the factory. Those flows have throughput times that depend on the type of

| Product | Main Applications |
|---|---|
| Product #1 | High end desktop systems; calculation intensive applications |
| Product #2 | Lower cost version of Product #1 for desktop systems |
| Product #3 | Laptops/low power applications |
| Product #4 | Updated version of Product #2; functionally identical |
| Product #5 | High end desktop systems and high speed data servers |

***Table 5.1: The five products examined and their main industry uses.***

product produced. The sections below summarize the different processes within each factory type and describe the basis for the lot groupings made.

The distinctions between the process used and the products produced become important when examining the factory flows. Because the different processes and products define machine settings or process recipes, they impact the preservation of machine setups, work staging, and lot batching. In conducting the analyses, logical grouping of the data occurred based on the different factory processes.

### *Fab Throughput Time Analysis*

All five products get their start at Intel's flagship fab facility located in Rio Rancho, New Mexico. As one of Intel's largest and most sophisticated factories, the fab processes wafers for the majority of Intel's high-end microprocessors.

Starting with raw silicon wafers, the fab runs three basic processes to create die on wafers. Often, the basic processes will receive slight changes, creating a sub-process. Most basic fab processes have a handful of sub-processes which define the actual machine settings

| Factory | Location |
|---|---|
| Fab | Rio Rancho, New Mexico |
| Sort | Rio Rancho, New Mexico |
| Assembly | Penang, Malaysia |
| Assembly | Chandler, Arizona |
| Test | Penang, Malaysia |

***Table 5.2: The factories providing throughput time information.***

and running times for the process steps, where the basic process will define the number of layers used to create the chip.

While the fab process determines the sequence of precise chemically engineered steps to add and subtract material, the specific product determines which designed patterns get used to create the layers of a chip's complex microelectronic circuitry. Thus, the same fabrication process can create a number of different products. Each basic process produces around 20 distinct components.

Each individual lot in the data sample has a calculated throughput time based on the factory entry and exit times. Grouping these lots into appropriate categories creates different throughput time distributions. Table 5.3 shows a summary of the three basic processes run in the fab with their corresponding planned leadtimes and calculated average throughput times. From a planning perspective, each fab process and sub-process has a defined planned leadtime. Note how the planned leadtimes listed match well with the actual calculated aggregate throughput times.

One possible explanation for this seemingly self-fulfilling behavior may result from the aggregation of the different products all using the same process. While the Process #1 may produce several products, some lots run much higher volumes and have lower than average throughput times, and some run lower volumes and have higher than average throughput times. Thus, the aggregate distribution actually consists of the distributions for several different products, which in the aggregate, all meet the planned leadtime. In addition, the work in process usually gets selected by an age priority scheme. Thus, lots running closer to or above the expected time will run first, so the net average throughput time comes close to the planned time.

Using a product-process cross reference listing, the process producing each product was attached to each record in the data sample. This allowed for sorting the data by the process name. Table 5.4 lists a sample of those fab sub-processes and their corresponding calculated average throughput times. From a product specific vantage, Table 5.5 shows a listing of the highest volume products, along with their corresponding processes, factory estimated throughput times, and calculated average throughput times.

| Fab Process | Planned Leadtime (days) | Calculated Average Throughput Time (days) | Number of Lots |
|---|---|---|---|
| Process #1 | 35 | 34.3 | 2346 |
| Process #2 | 52 | 52.6 | 2373 |
| Process #3 | 59 | 61.3 | 618 |

*Table 5.3: Fab basic processes with their corresponding leadtimes and production volumes.*

| Basic Process | Sub-Process | Calculated Average Throughput Time (days) | Number of Lots |
|---|---|---|---|
| Process #1 | Process #1a | 33.7 | 1741 |
| | Process #1b | 35.2 | 348 |
| Process #2 | Process #2a | 51.9 | 1491 |
| | Process #2b | 54.3 | 625 |
| Process #3 | Process #3a | 61.4 | 431 |

*Table 5.4: Fab sub-processes with corresponding average throughput times and production volumes.*

While each fab process has an estimated leadtime for overall planning purposes, different throughput times arise due to differences in production volumes. Note the differences between the calculated throughput times for the sub-processes and the overall process throughput time averages for those processes with very high production volumes; now compare the product specific calculated throughput times with those for their corresponding processes. For those products that have the highest production volumes, their calculated throughput times consistently fall below the calculated average for the process used. The results match expectations because the higher the production volume, the higher the potential for a lot to preserve a setup or match a process setting, and thus receive faster processing.

| Product Name | Process | Planned LT (days) | Calc Average TPT (days) | Number of Lots |
|---|---|---|---|---|
| Product #1 | Process #1a | 35 | 32.8 | 785 |
| Product #2 | Process #1a | 35 | 33.9 | 663 |
| Product #3 | Process #2a | 52 | 50.0 | 570 |
| Product #4 | Process #2b | 52 | 53.8 | 490 |
| Product #5 | Process #3a | 59 | 60.3 | 372 |

*Table 5.5: A sample of high volume products run on various processes in the fab with their corresponding throughput times.*

A distribution of throughput times produced the calculated averages shown in the above tables. Figure 5.1 and Figure 5.2 show the aggregate throughput time distributions, ignoring outliers, for Process #1 and Process #2 respectively. Throughput times outside a three-standard-deviation bound above and below the average defined the outliers. For comparison, the actual throughput time histograms overlay a normal curve matching the calculated distribution parameters (mean and standard deviation) for the data samples.

For these and all similar figures, each column represents the number of values greater than or equal to the bin label, but less than the next label falling into the corresponding bin. Notice how the distributions nearly fit the normal curve, but some significant differences exist. These two figures for the aggregate process throughput times shows the distribution for the overall times for a process producing multiple products.

Table 5.6 summarizes the data shown in the two figures. Note how the distributions come close to falling in a normal distribution. This indicates that no artificial limitations affect the throughput times. In other words, no ceiling that limits the maximum possible throughput time appears in the picture of the distribution.

Also, note how the elimination of a small percentage (approximately 1%) of the outlying points dramatically reduces the standard deviation and range of values with minimal effect on the mean. This again indicates some confidence that the data shows a valid and representative sample of the throughput time distributions. If the outlying points were not so evenly clustered around the average, it would indicate that some extremely unusual circumstances created the outlying values, and those values greatly affected the average. Instead, the average remained pretty much the same, and the outlier elimination reduced the variance.

Figure 5.3 and Figure 5.4 show throughput time histograms for the higher running products on Process #1 and Process #2 respectively. Figure 5.3 shows the throughput time distribution for 785 lots of Product #1 product running on Process #1a. The sample has an average throughput time of 32.8 days and a standard deviation of 2.89 days. Figure 5.4 shows the throughput time distribution for 570 lots of Product #3 running on Process #2a. The sample has an average throughput time of 50.0 days and a standard deviation of 5.1 days. As expected, both the average and the standard deviation for these specific products fall below the values calculated for their overall processes (see Table 5.5). These distributions show the typical spread in throughput times for high volume products running in the factory.

For these two examples, notice how the distributions look far from normal. This indicates that an individual product receives different handling from another, and the overall aggregate throughput time does not apply for any single product.

An autocorrelation analysis conducted on the series of daily average throughput times indicated that after only about 13 days the correlation between the throughput times of the past days and the prediction of future throughput times tends towards zero. Since the leadtimes for these fab lots fall well above 13 days, this indicates that knowing what the throughput times for products completing today does not help predict what the time will be for lots starting today. This suggests the long term average throughput time represents the best predictor of future leadtimes.

As described in Chapter 2, the chip manufacturing process spends the bulk of its time in wafer fabrication, with some three quarters of that time waiting in queue. As the above analysis shows, the fab processes have longer leadtimes that fall in a variable distribution. Thus, throughput time variability in fab presents a good opportunity for minimization. Fortunately, as just the first stage in the production chain, more opportunity exists to minimize the fab variability impact on the end customer at the downstream sites.

| Fab Statistics | Process #1 Aggregate | Process #1 No outliers | Process #2 Aggregate | Process #2 No outliers |
|---|---|---|---|---|
| Mean (days) | 34.3 | 34.2 | 52.6 | 52.4 |
| Standard Deviation | 3.8 | 3.4 | 7.7 | 6.3 |
| Variance | 14.1 | 11.7 | 59.8 | 39.6 |
| Range | 49.4 | 21.3 | 124.2 | 44.2 |
| Minimum | 6.7 | 24.3 | 6.0 | 30.0 |
| Maximum | 56.1 | 45.6 | 130.2 | 74.2 |
| Count (lots) | 2346 | 2323 | 2373 | 2341 |
| Fraction of points ignored as outliers | | 1.0% | | 1.3% |

*Table 5.6: Summary statistics for Process #1 and Process #2 distributions.*

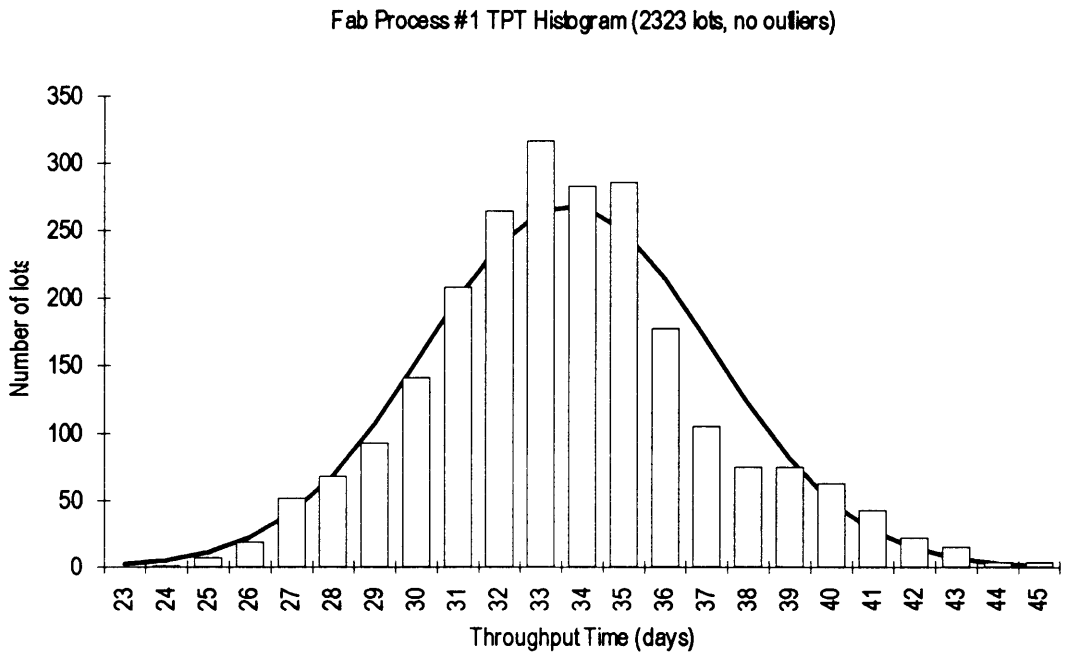


*Figure 5.1: Throughput time distribution for fab Process #1.*

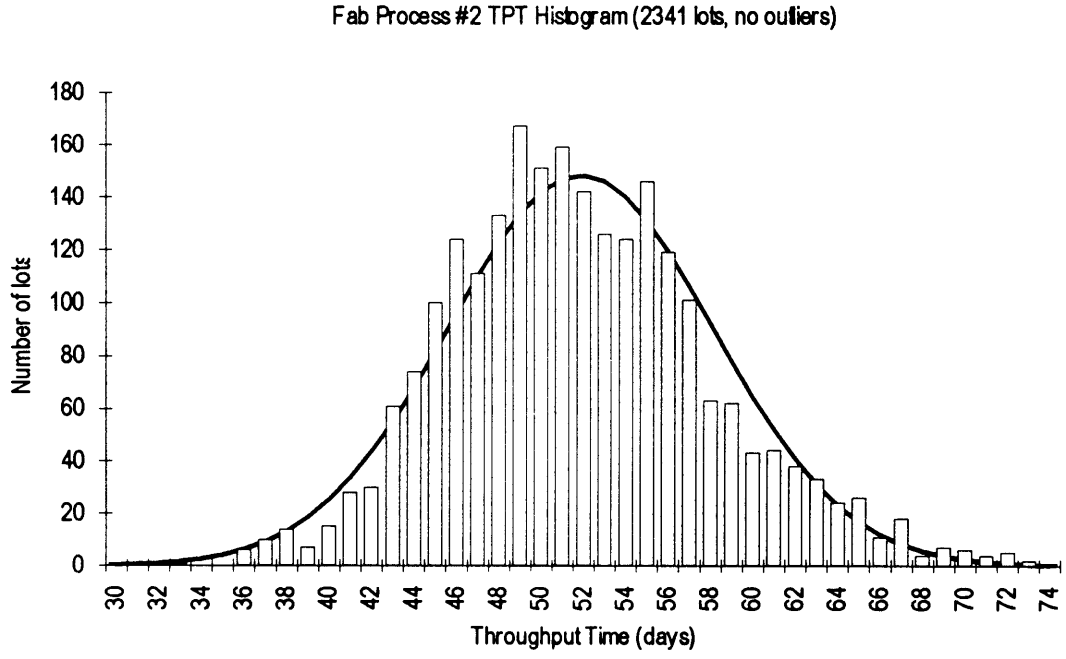


*Figure 5.2: Throughput time distribution for fab Process #2*

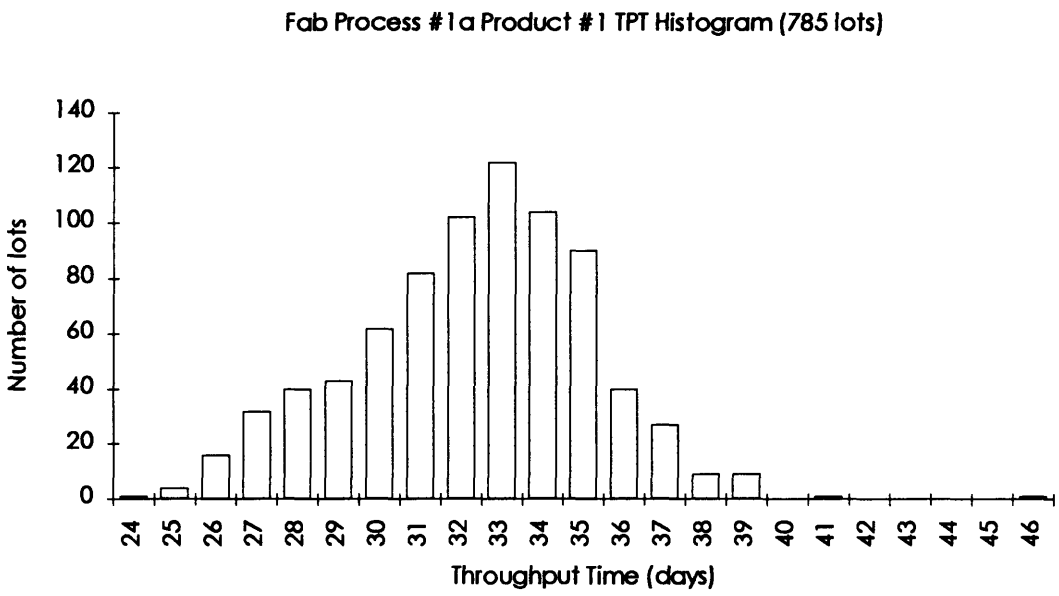


***Figure 5.3: Throughput time distribution for Product #1.***

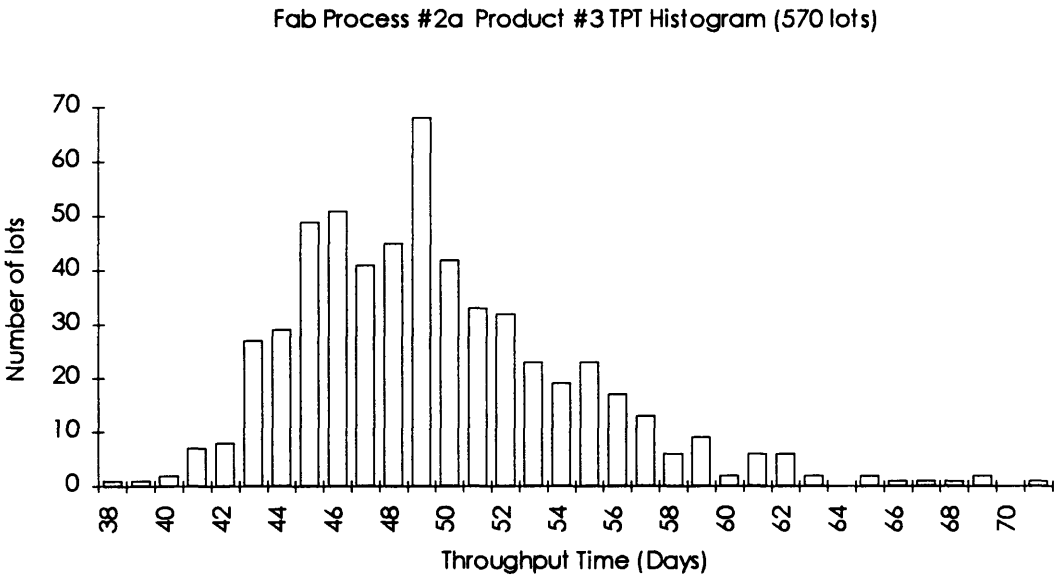


***Figure 5.4: Throughput time distribution for Product #3.***

*Sort Throughput Time Analysis*

Since fab and sort sites tend to be collocated, the next stage of throughput time analysis focused on the sort facility in New Mexico. This sort factory processes wafers coming primarily from a couple of different fabs, both located in Rio Rancho, New Mexico.

Receiving the completed wafers from the fab, the sort factory performs a functional test on each and every die on a wafer. The time taken to process a wafer lot depends on the number of wafers in the lot (since some lots may lose wafers during fab processing), the number of die per wafer, and the complexity of the product. As each die on the wafer gets probed, the dwell time (the time the probe spends in contact with the die) depends on the complexity of the functional test that determines whether the chip gets packaged or not.

Thus, in the sort factory, no overall process exists as in the fab factory. Because of the potential product-to-product differences in processing times described above, the throughput time data analysis occurred in product specific lot groupings.

Figure 5.5 shows the aggregate throughput time histogram for all lots in the sort sample. Like the fab throughput time graphs, the columns display to the number of values falling into the corresponding bin. For example, in the case of the zero bin, this column shows the number of throughput times greater than zero but less than 0.5 days.

In contrast with the even distribution about the average for fab throughput times, the sort throughput times skew heavily to the right. Since a less-than-zero throughput time cannot occur, and because the sort throughput times are relatively short, the values tend to get stacked up near zero and the distribution looks more like a gamma distribution rather than a normal distribution. The theoretical throughput times for the sort factory are quite short (usually measured in hours, not days) relative to the fab process. This means a lot spends the bulk of its time in queue rather than in process, and the distribution shows more the spread in queue times rather than in processing times.

The distribution also indicates that the majority of lot throughput times fall between 0.5 and 1.5 days. The theoretical factory throughput time for any lot in sort is much less than 0.5 days, so all throughput times higher than this consist mainly of queue time. The cumulative percentage curve for the throughput time distribution indicates that over 90% of all lots travel through the sort factory in less than 2.5 days.

Figure 5.6 show a typical throughput time distribution for one of the five products analyzed in the previous fab section. Note how its distribution looks quite similar to the overall sort factory distribution, indicating some commonalty in waiting times. This results because the equipment sets and operations tend to be similar among all the products, so the queue times tend to be similar. Table 5.7 summarizes the statistics for the distributions of the aggregate sort information and the five individual products.

In examining the five products, all show the consistent pattern of Figure 5.6 with a peak near zero and a long tail of higher throughput times. In addition, all the throughput time mean and standard deviation values fall within reasonable tolerances of each other. This indicates that the single aggregate sort throughput time distribution can serve as a good approximation for any specific product. Autocorrelation results support the use of the overall average throughput time as the best predictor of future throughput times. With such short throughput times, no time exists for any predictability to build up from day to day.

| **Sort Statistics** | **Products** | | | | | |
|---|---|---|---|---|---|---|
| *All lots* | *Aggregate* | *#1* | *#2* | *#3* | *#4* | *#5* |
| Mean (days) | 1.7 | 1.2 | 1.6 | 1.5 | 2.0 | 1.7 |
| Standard Deviation | 1.8 | 1.3 | 1.5 | 1.2 | 2.0 | 1.8 |
| Variance | 3.1 | 1.8 | 2.4 | 1.4 | 4.1 | 3.4 |
| Range | 26.8 | 26.5 | 12.3 | 9.5 | 26.7 | 16.6 |
| Minimum | 0.2 | 0.2 | 0.2 | 0.3 | 0.3 | 0.2 |
| Maximum | 27.0 | 26.6 | 12.6 | 9.8 | 27.0 | 16.8 |
| Count (lots) | 7618 | 784 | 732 | 506 | 771 | 389 |
| *No outliers* | | | | | | |
| Mean (days) | 1.6 | 1.1 | 1.4 | 1.4 | 1.8 | 1.5 |
| Standard Deviation | 1.1 | 0.8 | 1.1 | 0.8 | 1.0 | 1.2 |
| Variance | 1.2 | 0.6 | 1.3 | 0.6 | 1.0 | 1.5 |
| Range | 6.8 | 4.9 | 5.9 | 4.8 | 7.4 | 7.0 |
| Minimum | 0.2 | 0.2 | 0.2 | 0.3 | 0.3 | 0.2 |
| Maximum | 7.0 | 5.1 | 6.1 | 5.0 | 7.7 | 7.2 |
| Count (lots) | 7478 | 772 | 718 | 494 | 761 | 381 |
| Fraction of points ignored as outliers | 1.8% | 1.5% | 1.9% | 2.4% | 1.3% | 2.1% |

***Table 5.7: Summary statistics for products in the sort factory.***

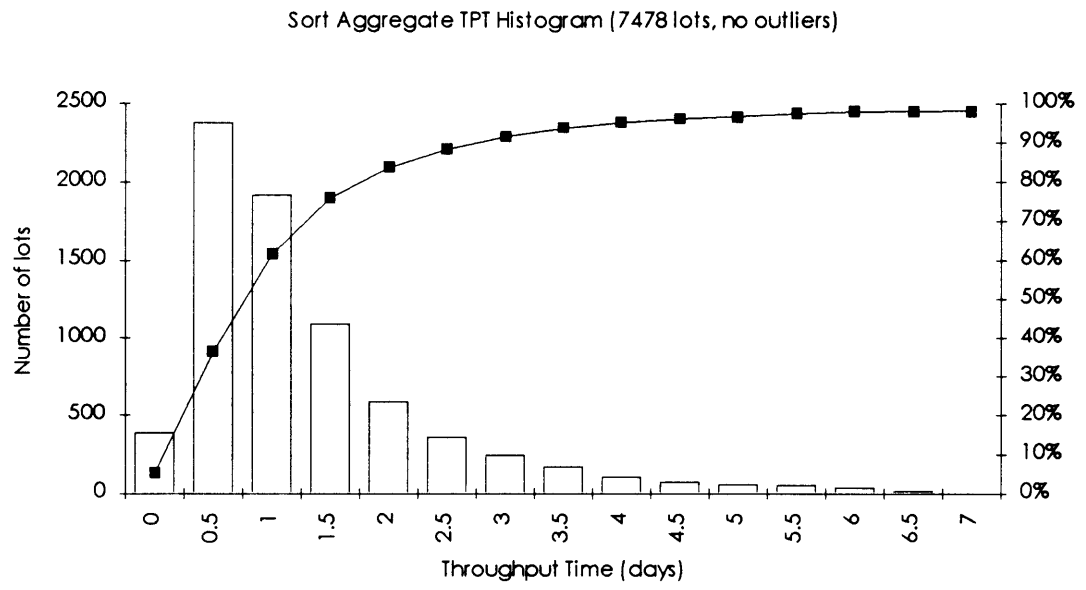


***Figure 5.5: Aggregate throughput time histogram for the sort factory with cumulative percentage overlay.***

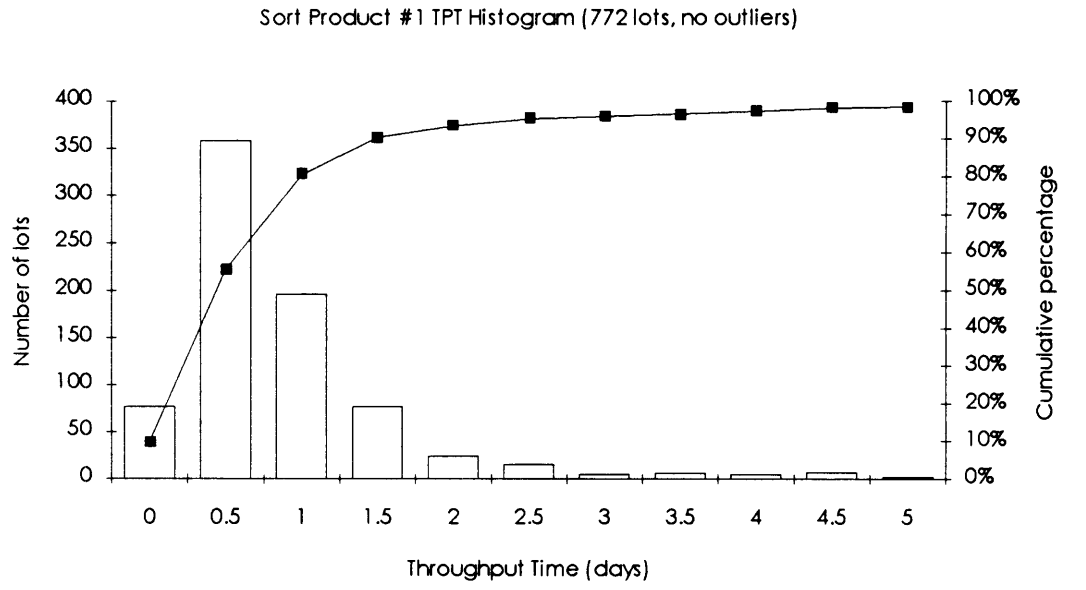


***Figure 5.6: Throughput time histogram for Product #1 in the sort factory with cumulative percentage overlay.***

*Assembly Throughput Time Analysis*

After going through the sort process, the wafers get shipped to an assembly site for packaging. The packaging of a chip not only makes the electrical connections so the chip can communicate with the outside world, but also serves to dissipate heat, repel moisture, and block electromagnetic interference. The customers define how they want their microprocessor packaged.

In general, Intel microprocessors appear in two main package types: ceramic and plastic. Assembly throughput times vary depending on the complexity of the package and the number of connections made as well as the severity of testing. For instance, chips sold packaged for military use undergo extensive testing beyond the normal regimen.

The five products analyzed through wafer fab and sort in New Mexico now appear at two different assembly locations. Four of the five products travel half way around the world to Intel's largest assembly factory in Penang, Malaysia, and one product goes the shorter distance to Chandler, Arizona. Both these sites package chips from wafers fabricated at sites scattered around the world.

As discussed earlier, the calculated throughput times do not include transportation times between factories or the time lots spend waiting to enter a factory. From a logistical standpoint, the time spent in transit depends primarily on the distance traveled. Lots going from New Mexico to Penang by air freight usually get scheduled for 4 or 5 days in transit. Lots traveling domestically can reach their destination overnight, but normally take a couple of days. The total travel time depends on the flight schedules going to the destination as well as the customs schedules. If a lot arrives too late to clear customs, and the office is closed for the weekend, an extra few days gets added to the in transit time.

Completed wafers arrive whole at the assembly site with ink dots showing the results of the sort process. The wafer gets sawed into individual die with the good die going into packages. Package type and device complexity as well as special customer requirements determine the factory flow. Analysis of the five products occurred based on both the product and its specific package. Thus, throughput times are only comparable for similar products receiving identical packaging.

Figure 5.7 shows the throughput time distribution for Product #1 packaged at the Penang assembly site. All the lots represented in this distribution received a ceramic package. Lot sizes vary based on the size and weight of the package, but all lots within the factory have a consistent number of units. Figure 5.8 shows the throughput time distribution for Product #3 packaged at the Arizona site. This product received a very complex plastic package. Note how for this product no lots took less than 1.5 days to complete.

While the assembly process takes a bit longer than the sort process, the overall distributions look similar in their right-skewness. Because of the longer processing times,

no lots travel through the assembly factory in less than a day, with very few making the trip in less than two days. However, as with the other factories, most of the time spent is waiting in queue. Because of the number of different processing steps, the number of opportunities to get caught waiting also increases. With typical throughput times at around 4 times the theoretical minimum, a lot will spend some 75% of its time waiting. Both the distributions shown in the figures represent typical throughput times for the two factories.

Table 5.8 lists the summary statistics for the five specific products in their respective assembly factories. Like the other factories, a large reduction in variance occurs by just ignoring a small percentage of the very high throughput time lots.

Because each distinct product-package combination has a unique set of manufacturing parameters, aggregation becomes impossible. The assembly plant will treat each unique combination as a separate factory flow primarily to prevent mixing of different chips that appear in similar packages.

Like the sort factory, the assembly factory has relatively short throughput times, and autocorrelation results for day-to-day times indicate no predictability beyond the overall average.

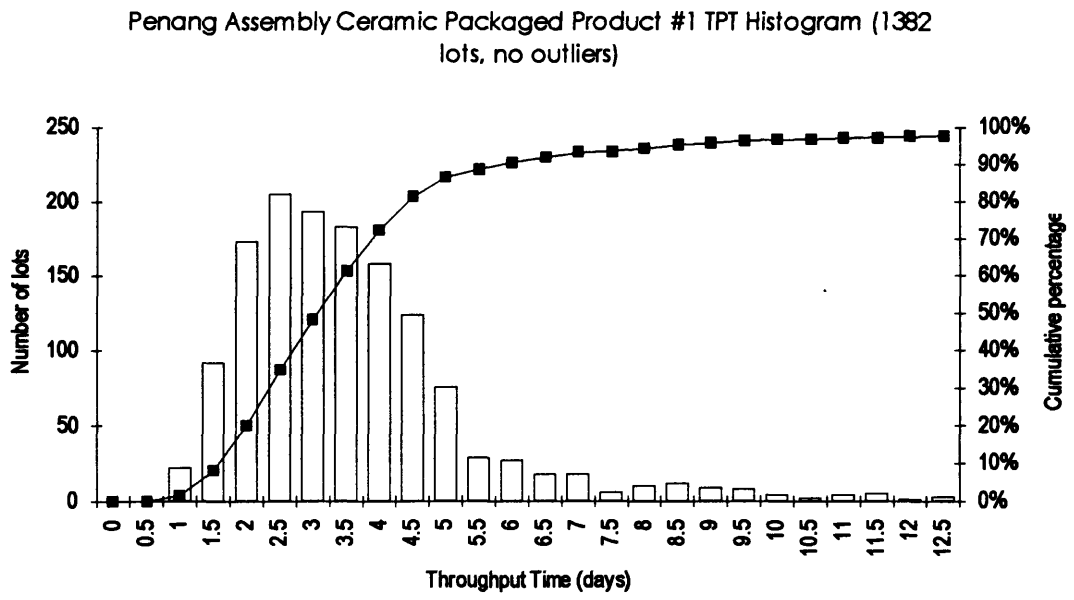


***Figure 5.7: Assembly throughput time distribution for ceramic packaged Product #1 processed in Penang, Malaysia.***

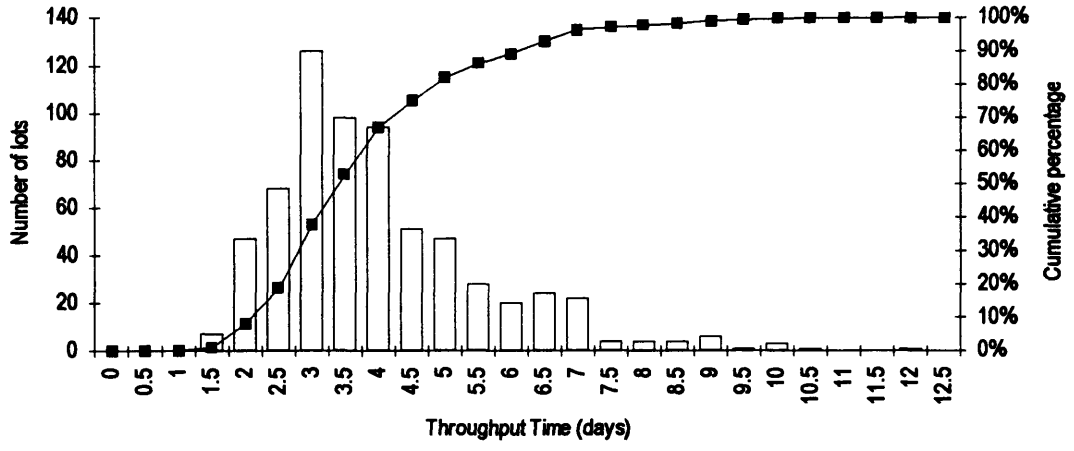


***Figure 5.8: Assembly throughput time distribution for plastic packaged #3 product processed in Chandler, Arizona.***

| **Assembly Statistics** | **Products** | | | | |
|---|---|---|---|---|---|
| | *#1* | *#2* | *#3* | *#4* | *#5* |
| Assembly Site<br>Package Type | *Penang*<br>*Ceramic* | *Penang*<br>*Ceramic* | *Arizona*<br>*Plastic* | *Penang*<br>*Plastic* | *Penang*<br>*Ceramic* |
| *All lots* | | | | | |
| Mean (days) | 4.2 | 4.7 | 4.3 | 6.1 | 4.7 |
| Standard Deviation | 2.9 | 2.4 | 1.6 | 3.9 | 3.0 |
| Variance | 8.3 | 5.8 | 2.5 | 15.2 | 8.9 |
| Range | 35.6 | 17.5 | 10.8 | 24.7 | 12.0 |
| Minimum | 1.2 | 1.7 | 1.6 | 2.1 | 1.3 |
| Maximum | 36.8 | 19.2 | 12.4 | 26.8 | 13.2 |
| Count (lots) | 1415 | 712 | 656 | 501 | 122 |
| *No outliers* | | | | | |
| Mean (days) | 3.8 | 4.5 | 4.2 | 5.8 | 4.7 |
| Standard Deviation | 1.8 | 1.9 | 1.4 | 3.1 | 3.0 |
| Variance | 3.2 | 3.8 | 1.9 | 9.8 | 8.9 |
| Range | 11.6 | 10.1 | 7.3 | 15.3 | 12.0 |
| Minimum | 1.2 | 1.7 | 1.6 | 2.1 | 1.3 |
| Maximum | 12.8 | 11.8 | 8.9 | 17.4 | 13.2 |
| Count (lots) | 1382 | 698 | 644 | 494 | 122 |
| Fraction of points ignored as outliers | 2.3% | 2.0% | 1.8% | 1.4% | 0.0% |

***Table 5.8: Summary statistics for products in the assembly factory.***

*Test Throughput Time Analysis*

Once packaged by the assembly factory, the chips can communicate with the outside world. The test factory now determines what performance level the chip satisfies, which determines the orders the chips can satisfy. The test factory ensures orders get filled with product meeting the quality specifications defined by the company and requested by the customer.

Within the test factory, a process known as binning separates the chips by their various performance characteristics into separate quantities known as bins. This process not only classifies products by their functional abilities, but also eliminates any poor quality units. General tests will separate out chips according to the clock speed at which they can still function properly. More specific tests under different environmental conditions, like temperature and voltage, further determine a chip's functionality. Bins with quantities needed to satisfy a given specification continue through the factory. Those bins without demand get moved to a staging area.

To ensure quality, units undergo an environmental and electronic stress test known as burn-in. Burn-in represents the bulk of the processing time a chip spends in the test factory. Depending on the customer specification, burn-in can last anywhere from 3 to 168 hours. Queue time, however, tends to dwarf even these figures. Customers will request different burn-in specifications depending on their desire to ensure proven quality.

After the testing process determines all the performance characteristics and allocates all the material that satisfies the different specifications, those quantities get assigned to fill either specific customer orders or replenish generic inventories. From this assignment the factory knows what finishing process to use to mark the packages and pack the units for shipping. For example, a generic product may receive the Intel logo and get packed into a plastic tray for shipping while a customer specific product would receive its own marking and get packed into a tape and reel format.

Because the different characteristics of a given assembly package require package specific testing equipment and testing processes, capacity utilization issues become important. Units not only require different amounts of time on a testing machine or in a burn-in environment, but also depending on the package dimensions, the number of units that a machine can run simultaneously changes.

As the lots travel through the testing factory, different quantities fall into the various bins. These quantities split from their original lot and often combine with similar bins from other lots to form new lots. This creates an extremely complex manufacturing process flow which confounds any attempt to calculate factory throughput times. This becomes especially complicated when the yield for a given performance characteristic is very low.

For example, a new microprocessor product may sell at speeds of fast, faster, and fastest. If only a small fraction of each lot yields the fastest chips, many of these bins must combine in order to fill an order, and many lots must start in order to produce a sufficient quantity. In the meantime, the majority of the chips may fall into the fast bin, but their supply may well exceed demand for these lower performing chips, and excess inventory becomes a problem.

Due to the extremely complex process flow through the test factory, throughput time analysis occurred for only those lots that traveled directly from the beginning to the end, commonly known as the primary bin flow. With functionally identical products assembled into different packaging undergoing different testing regimens, all with different burn-in times and equipment requirements, factory throughput times become dependent not only on the product and package but also the customer specifications.

Based on the specification-dependent throughput time conclusion, a throughput time analysis for the five products followed in the manufacturing process was performed for the specifications with the highest volume of lots that traveled directly from the beginning to the end of the test factory.

Figure 5.9 shows a typical test throughput time distribution for a microprocessor product, in this case Product #1. The times shown represent all lots that satisfy a high clock speed, 6-hour burn-in specification. Product #1 appears primarily in high-end desktop systems used for calculation intensive applications. The high demand for these kind of parts tends to drive the throughput times lower.

Figure 5.10 shows the test throughput time distribution for microprocessor Product #4 satisfying a medium clock speed specification. Product #4 comes in low, medium, and high speed flavors. Since this part represents a middle performance specification, one expects lower demand. But this speed has the highest yield, so due to the excess supply, lots will often get held up in processing, extending their throughput times.

For products with high demand, test throughput times tend to be relatively low when compared with products with lower demand. In addition, the complex test factory process flows contribute to more variable throughput times. For example, with different quantities from each lot able to satisfy a particular specification, those lots eventually combine to form a single completed lot. This means some smaller quantity lots may end up waiting for a while before they can combine with other lots. Throughput time data appears for each lot that forms a final quantity. The smaller lots end up appearing in the throughput time distribution as the higher values.

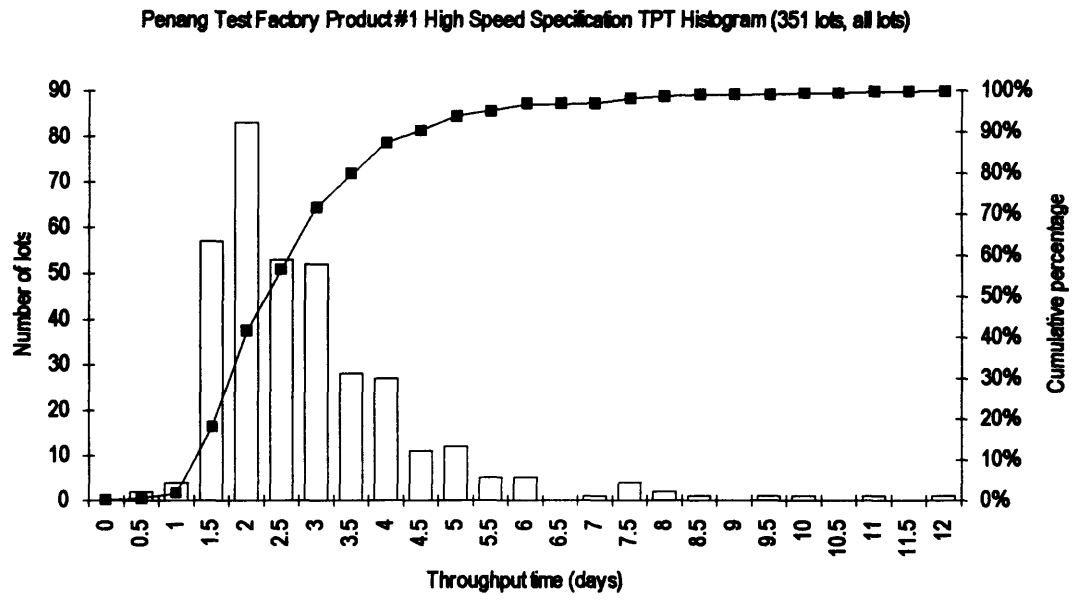


*Figure 5.9: Penang test factory throughput time distribution for Product #1 satisfying high demand high speed performance specification.*

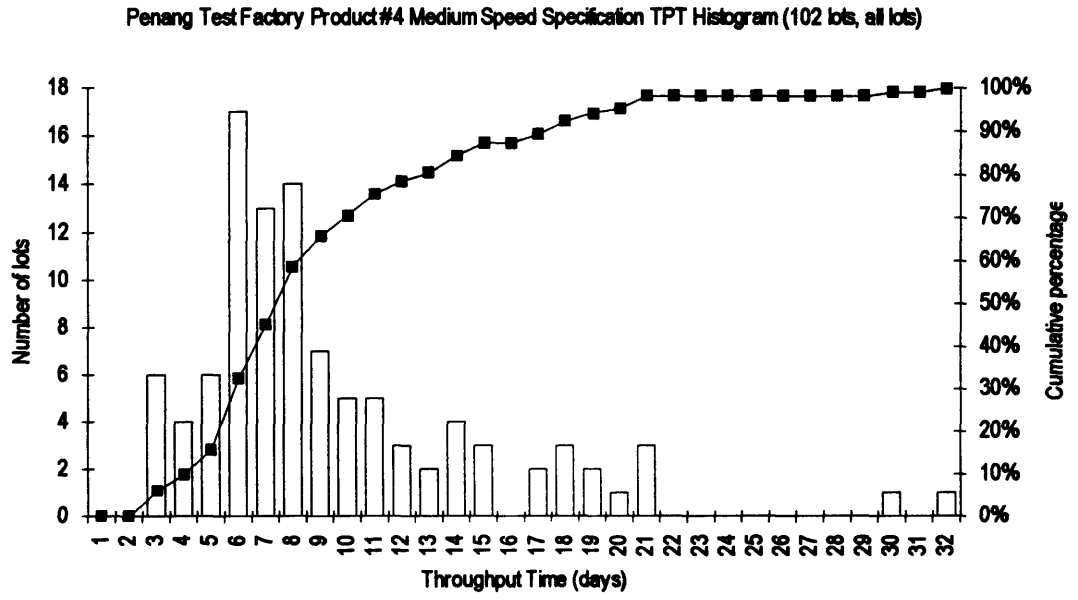


*Figure 5.10: Penang test factory throughput time distribution for Product #4 satisfying a lower demand medium speed performance specification.*

Table 5.9 lists the summary statistics for the 3 products which have direct primary bin flows. The splitting and combining of lots through the test factory makes an assessment of the accuracy or validity of the calculated leadtimes difficult. Primary bin flows represent the products and specifications with the higher demand, but the majority of products running through the test factory do not follow this path.

For those products that do not appear in the analysis, the production flow becomes extremely complex. The first part of the test process classifies the units by speed. The different speed bins will then combine with other lots matching the characteristics to form larger lots. Those units undergo various tests which again splits units from the group. The units split from the group may get classified as having passed a certain test, but not another, while the main quantity continues through the process. The split units may wait or may combine with other lots to continue towards satisfying a different specification depending on the customer demand. Thus, tracing the separation and combination of lots through the factory to calculate a throughput time becomes quite difficult, warranting the focus on the primary bin flows.

| Test Statistics | Product #1 | Product #2 | Product #4 |
|---|---|---|---|
| Specification | High speed | High speed | Med speed |
| Mean (days) | 3.2 | 3.5 | 10.0 |
| Standard Deviation | 1.5 | 1.5 | 5.4 |
| Variance | 2.4 | 2.4 | 29.6 |
| Range | 11.4 | 9.7 | 29.0 |
| Minimum | 0.8 | 0.6 | 3.5 |
| Maximum | 12.2 | 10.3 | 32.6 |
| Count (lots) | 351 | 132 | 102 |

***Table 5.9: Summary statistics for test products.***

### *Data Analysis Conclusions*

A number of conclusions result from conducting the data analysis on the different factories which may help in formulating future strategies:

- The basic throughput times fit neither normal nor gamma distributions
- Autocorrelations indicate no link between past times and future times
- Lots start in clumps with their cohorts
- Lots do not travel in FIFO order through the factory

#### Mathematical Distributions

From the previous figures for the fab throughput time distributions, the normal distributions based on the calculated parameters appear quite close to the actual values for the aggregate processes. However, the distributions for the specific products do not match well with a normal distribution. Chi-square goodness-of-fit tests performed between the calculated and actual values cannot conclude a good fit.

Appendix A shows the chi-square goodness of fit analysis performed for Process #1 and Process #2. For Process #1, the total chi-square value amounted to 115.2, while based on the number of degrees of freedom and a 95% confidence bound, the chi-square value must be less than 10.9 to conclude goodness of fit. For process #2, the total came to 132.4, but the total must be less than 28.1 to conclude goodness of fit. Thus, in both cases, while the figures for the throughput times look somewhat normally distributed, chi-square testing cannot conclude that a normal distribution fits.

Normal distributions seem closest for fab throughput times given the high magnitude of the values and their even spread above and below the mean. Referring to the figures for the other three factory types, the distributions obviously do not fit a normal curve. The condition of no less-than-zero throughput times indicates a non-negative distribution like a gamma distribution would fit the data better.

#### Autocorrelation Analysis

Autocorrelations run for the day-to-day series of daily average throughput times fail to indicate any predictability of future leadtimes based on the past. For the fab processes with their longer throughput times, correlation coefficients between one day's average and another started at 0.8 for a one day difference, but fell to zero within 20 days or so. Since the average leadtimes exceed 30 days, this indicates that knowing the throughput times for lots finishing today helps little in predicting the times seen by lots starting today. Figure 5.11 shows the rapid descent of the correlation coefficient for Product #1 fab throughput times.

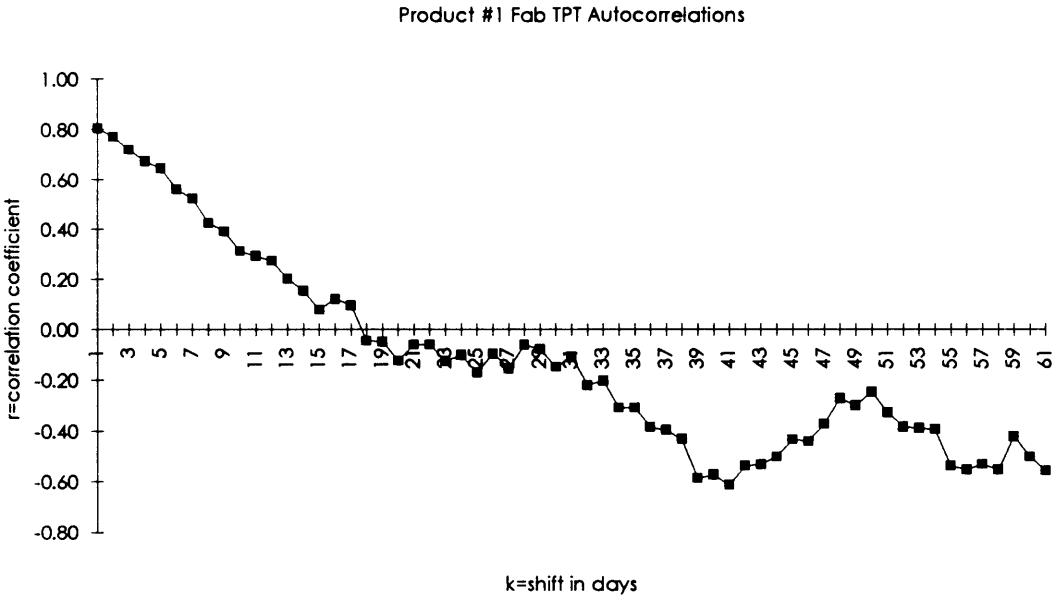


***Figure 5.12: Autocorrelation coefficients for Product #1 fab throughput times.***

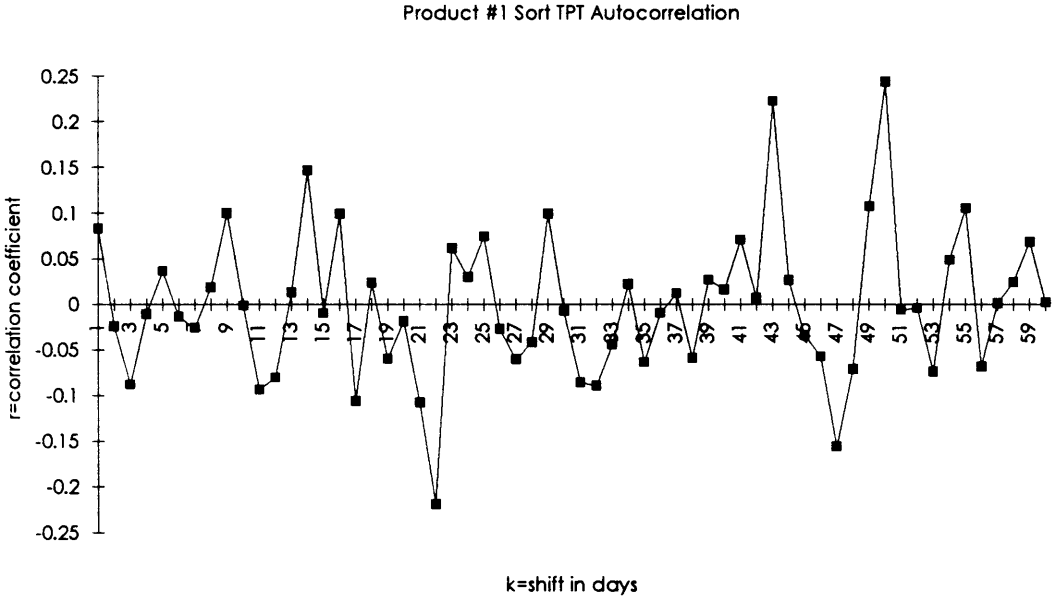


***Figure 5.11: Autocorrelation coefficients for Product #1 sort throughput times.***

For the sort factory, with its much shorter throughput times, the autocorrelation results showed no correlation at all. This was expected since the average throughput times for some products often fall less than two days, and for Product #1 shown in Figure 5.12 the average throughput time is just 1.1 days. Thus, the day-to-day average throughput times have little ability to predict future throughput times.

Despite the slightly longer leadtimes for the assembly factory, the autocorrelation results for the products going through the assembly factory also indicated little predictability beyond the overall average throughput time.

Lot Starts

An examination of the starting times for specific product lots on any given day indicate that the lots start in clumps at roughly the same time. This means several lots of the same product enter the factory simultaneously, but an examination of their completion times shows they exit in a random order over random times. Since identical lots require the same machine setups, starting those lots all at the same time increases their chances of processing with their cohorts. Differences in processing along the way must separate those lots from each other.

In some cases, these cohort lots may get separated by different events within the factory. For instance, the last lot to run before a setup change will be well ahead of the lot that would have run next. If a machine breaks down, lots that have made it through that operation will continue, while lots that were waiting will continue to wait or get held up in traffic competing for space on the remaining machines. Also, lots requiring rework will take longer.

Appendix B shows a sample transaction listing for one product. The shaded area depicts a group of lots started at the same time, but finishing at different times. Notice how the last lot to start actually finishes first, well ahead of its cohorts. Even though these lots are identically processed, they still change order within the factory. This leads to the next subject of FIFO flow.

First In First Out Flow

An examination of the entry and exit order for lots in the data sample producing the identical product show that lots do not travel through the factory in FIFO order. This implies that lots can skip ahead and fall behind their cohorts within the factory. Thus, a lot started today may finish before a lot started yesterday. This kind of behavior directly impacts throughput time variability.

When a lot started today finishes before a lot started yesterday, it automatically means that one lot took more time and one lot took less time. This difference in processing times

contributes to throughput time variability. If lots were processed more in FIFO order, the lots would have a better chance of having closer throughput times, or at least not have automatically different throughput times, lowering the variability.

Figure 5.13 shows a typical look at the non-FIFO flow of a single product through the fab. the plot shows the difference between the starting order and the ending order, where a positive change means a lot finished ahead of where it started. Of course, any single lot that gets out of order can result in a number of lots out of order, but the graph shows the frequency of position changes.

Figure 5.14 shows the same FIFO analysis for the sort factory. In this case, with the exception of some large position changes, the changes in order are more confined. This may result from the shorter throughput times not allowing enough time for order changes to occur. Extreme position changes may result from special handling (in the case of an advance) or from a quality hold (in the case of a fallback).

The data conclusions drawn above assume stable throughput times during the data collection period. Since fairly mature products and processes appear in the analysis, the data collected from the factories reflects well established throughput times and the assumption holds.

The fab represents the only factory where a throughput time may significantly change over time. With the introduction of a new product or process into the fab, throughput time targets ramp downwards over the course of a few months until they match the target for the overall process. The flagship New Mexico fab providing data for this project has produced high-end microprocessors using well-established processes for the past several years.

Figure 5.15 shows the daily average fab throughput time for completions of Product #1 lots. The figure demonstrates the stability of the processing times for the fab over the course of the analysis period. In addition to the overall stability of the process represented by the seven-day moving average, note how the moving average predominantly appears below the 35-day target. This confirms both the stability assumption and the high volume product conclusion.

While the fab throughput time represents the longest amount in the full manufacturing process, the throughput time variability has its highest impact in the test factories. With the other factories, differences in throughput times can offset, so long as the overall output meets the weekly targets. But in the test factory, where products often time become customer specific and the number of specifications grows, any variance in throughput time alters the ability to deliver to the customer.

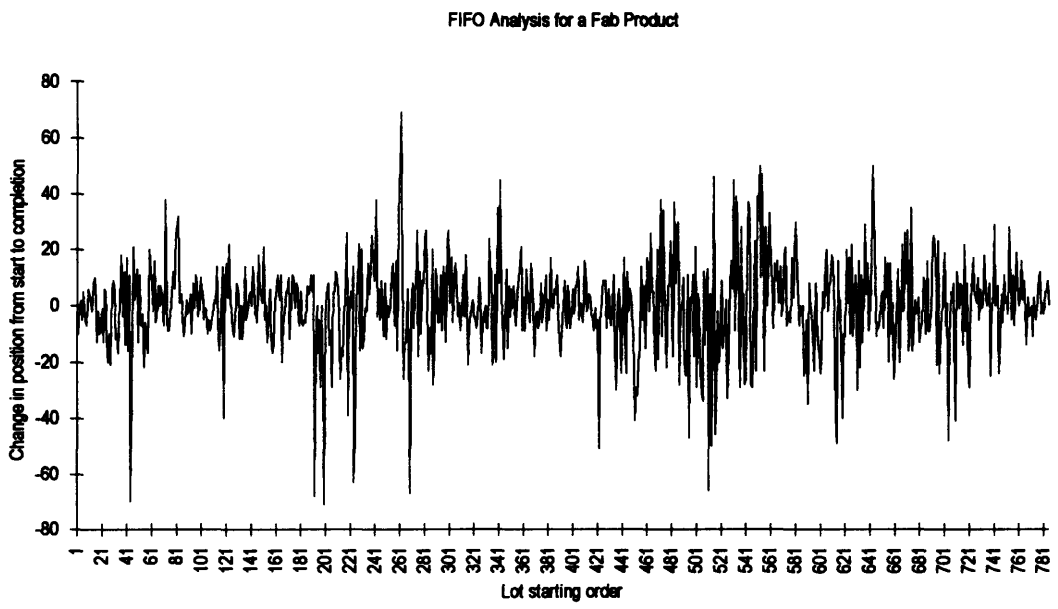


*Figure 5.13: FIFO order changes for a fab product.*

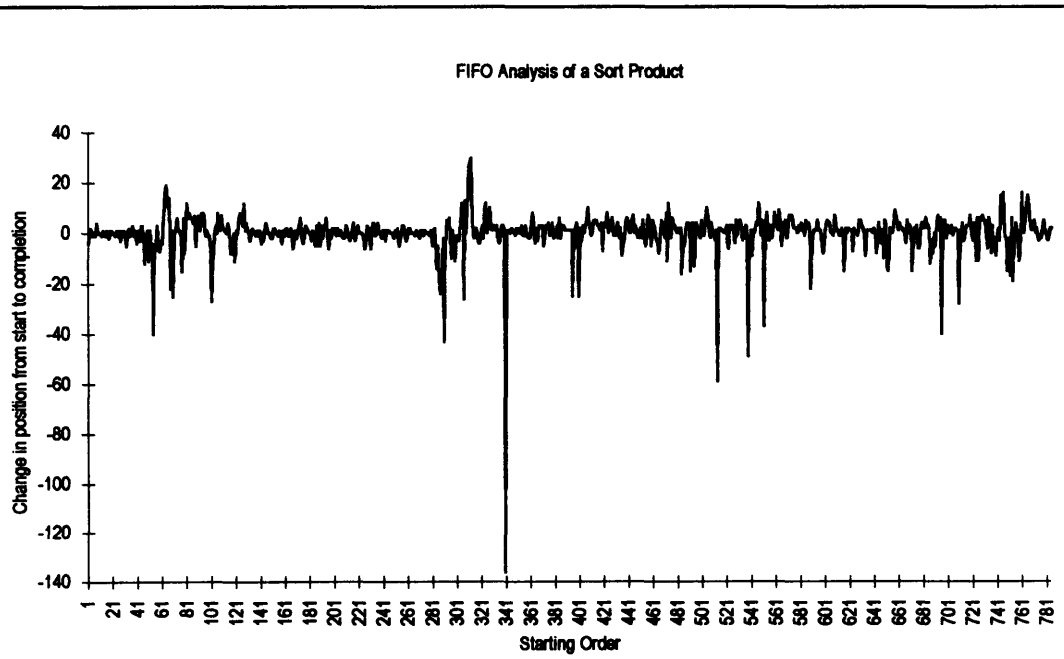


*Figure 5.14: FIFO changes for a sort product.*

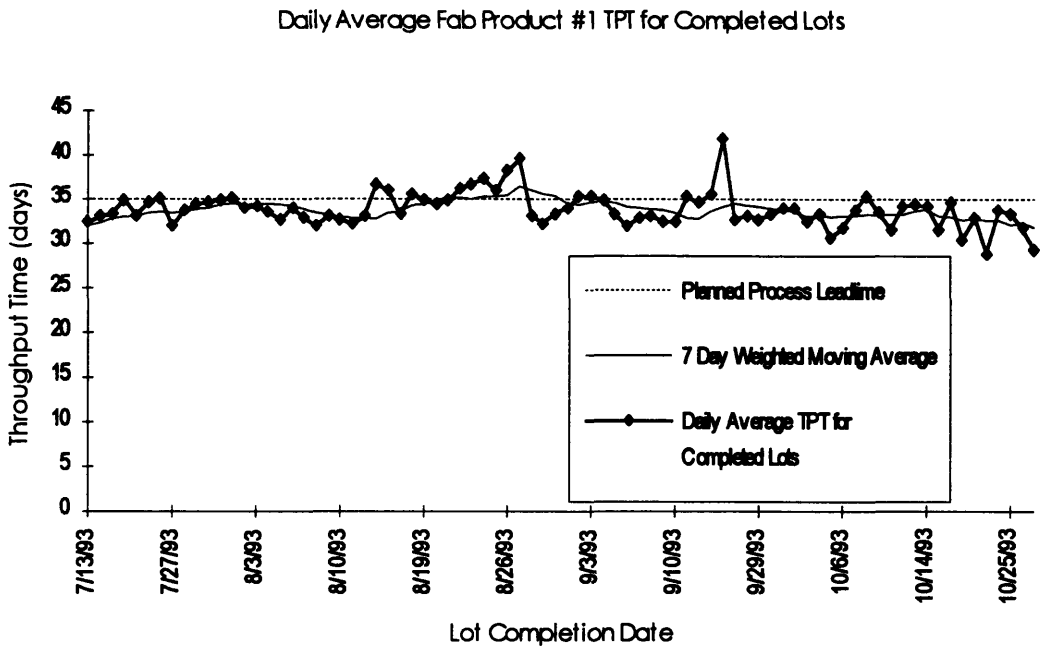


***Figure 5.15: Daily Average TPT for Product #1.***

# Chapter 6 - The Variability Methodology

Knowing the throughput time characteristics of the various production stages allows the development of a methodology to include leadtime variability information in planning and scheduling. This chapter describes the proposed methodology based on the data analysis performed.

### *Company Impacts*

As discussed in Chapter 4, addressing variability occurs in two main areas within the new planning system:

- Order scheduling and order mapping
- Capacity resource consumption

A fundamental business change will result from the knowledge and use of throughput time variability information in planning and scheduling. The ability to make tradeoffs between the scheduled leadtime and the customer service level distinguishes the new system from traditional order scheduling. Through some criteria, orders will get ranked in terms of importance for on-time delivery. Based on this ranking, different levels of customer service can be associated with each order. Selecting different levels of customer service associates a different planned leadtime with the order; a leadtime based on the distribution of actual factory performance data rather than single point estimates. Intel feels that using a distribution rather than just a point estimate will significantly improve delivery performance.

A detailed capacity analysis represents another of the key features that Intel's new manufacturing planning system provides. In addition to using leadtime information in order scheduling, the new system relies on accurate throughput time data as the basis for capacity calculations. Determining the timing of capacity consumption requires an estimate of when a lot will arrive at a production stage; throughput times provide that estimate. Thus, the methodology proposed impacts both the order scheduling and capacity planning elements.

The current system vision uses the throughput time distribution information to assist the sales and marketing organization choose expected completion dates for orders they take. On the manufacturing side, factories would still commit to a single target throughput time, fully knowing that the actual times would vary. Intel feels that because the throughput times determine expected completion dates, the organization that communicates those dates to the customers would better understand the tradeoffs between choosing a longer or shorter time, and the probability of meeting that time. In addition, setting multiple targets for the factories would create confusion. The distribution information becomes useful to the manufacturing organization if it can help inform and educate the factories

about their throughput time variability, and create an impetus for addressing the sources of variability.

The long run goal for the system involves including current factory conditions, such as the current work in process level or the expected available capacity, to determine expected completion times. This enables a fully integrated customer order to manufacturing supply cycle that accounts for known delays and adjusts expectations accordingly. This helps maintain a high customer service level while balancing the factory load.

### *Setting Expectation Levels*

The tradeoff between expected factory throughput time and customer service level sets an expectation level, or probability, that the customer order will ship on time. Increasing the expected leadtime adds a margin of safety to the usual throughput time, which increases the probability that the order will finish within that time window. The sales and marketing organization would use different leadtimes to schedule orders, but the factories would still work to a single throughput time target.

For example, suppose the factory leadtime target equals the average for the throughput time distribution. If the throughput time distribution followed a symmetric distribution like the standard normal distribution, then choosing a leadtime equal to the average associates a 50% probability that the leadtime value will exceed the average and a 50% probability it will beat the average. However, if the sales and marketing organization selected a leadtime equal to the average plus one standard deviation, the chances of the actual value exceeding that time decreases to 16%, which means an 84% on-time chance. Thus, having sales and marketing increase the assumed leadtime increases the probability that manufacturing will complete on time.

The long manufacturing leadtimes force the factories to start work before knowing the actual orders. Work gets released to the factories based on the current forecast. Thus, having sales and marketing use longer-than-average throughput times does not cause manufacturing to release work early to the factory. Actually, as orders arrive they will get scheduled based on the order due date and the probability of on time delivery desired.

For example, if an order is due in five days, choosing some current work in process that would take an average of five days to complete associates a 50% probability of completing on time (again, assuming a symmetrical distribution). The new planning system will examine the expected factory supply for work with a probability to complete within 5 days that matches the desired level. In other words, based on the leadtime distribution for the remaining work the proportion that completes within 5 days equals or exceeds the desired probability.

The costs of excess inventory offset the benefits of planning using longer-than-average throughput times. Thus, it becomes unrealistic to expect 100% on-time delivery without

incurring some negative side-effects. Common sense and judgment in conjunction with the importance of the order must guide the selection of leadtimes.

### *Determining Probabilities From Leadtime Distributions*

As the data analysis showed, the throughput time distributions for the various production stages follow neither the normal nor the gamma mathematical distributions. As a computer and data based application, the new manufacturing planning system must easily determine the proper values based on a minimum of data. The lack of standard mathematical models requires a numerical solution.

The analysis also showed that no simple set of parameters formed an easy predictive model for future throughput times. The autoregressions indicated little correlation between day-to-day throughput times. Thus, only the distributions themselves provide any information towards future performance, and the overall average represents the best predictor of future leadtimes.

The proposed methodology uses the following steps to determine the times associated with a probability:

- Select a round number of the latest data points (i.e. 500).
- Sort the throughput times in ascending order
- Equate probabilities with the fraction of data points
- Choose the minimum throughput time such that the corresponding fraction of points equals or exceeds the desired probability of on time delivery

The data collected provides lot-for-lot throughput times. By selecting a round number of lots like the latest 200, 500, or 1000 lots processed for a given product, easy determination of the throughput time values associated with different probabilities can occur.

Suppose the latest 500 data points for a particular product represent one month's worth of production. This means the distribution of those throughput times will be large enough to capture most of the different events that occur over a month without emphasizing any one event.

Ordering those 500 lots in ascending order results in a sorted list of throughput times. Finding the probability associated with any leadtime means finding the fraction of points in the list represented by that time. Thus, the 400th time in the sorted list corresponds to 80% probability, since 400 points represents 80% of a 500 number listing.

The number of points included in any specific products list can vary based on its volume and variability. The number of points needs to be sufficient to generate a typical distribution of throughput times, but can be altered to capture as much or as little of the past history as desired.

*A Simple Example*

Suppose the following 20 times represent a typical distribution of throughput times for one product at one production stage (in days):

| Entry | Value | Entry | Value | Entry | Value | Entry | Value |
|---|---|---|---|---|---|---|---|
| 1 | 1.5 | 6 | 3.0 | 11 | 2.5 | 16 | 2.4 |
| 2 | 0.9 | 7 | 2.5 | 12 | 2.7 | 17 | 1.2 |
| 3 | 2.2 | 8 | 2.6 | 13 | 2.3 | 18 | 4.1 |
| 4 | 2.4 | 9 | 1.0 | 14 | 5.6 | 19 | 3.2 |
| 5 | 4.7 | 10 | 3.6 | 15 | 2.1 | 20 | 1.3 |

Figure 6.1 shows the histogram for the points listed above. Those points, when sorted in ascending order, appear as:

| Entry | Value | Entry | Value | Entry | Value | Entry | Value |
|---|---|---|---|---|---|---|---|
| 1 | 0.9 | 6 | 2.1 | 11 | 2.5 | 16 | 3.2 |
| 2 | 1.0 | 7 | 2.2 | 12 | 2.5 | 17 | 3.6 |
| 3 | 1.2 | 8 | 2.3 | 13 | 2.6 | 18 | 4.1 |
| 4 | 1.3 | 9 | 2.4 | 14 | 2.7 | 19 | 4.7 |
| 5 | 1.5 | 10 | 2.4 | 15 | 3.0 | 20 | 5.6 |

The distribution has an average of 2.6 days and a standard deviation of 1.2 days. However, note how according to the cumulative percentage on the histogram, 50% of the values fall below 2.5 days. From the sorted listing, note that at 2.6 days, 13 of 20 points fall at or below the average. This suggests a probability of 65% is associated with the mean.

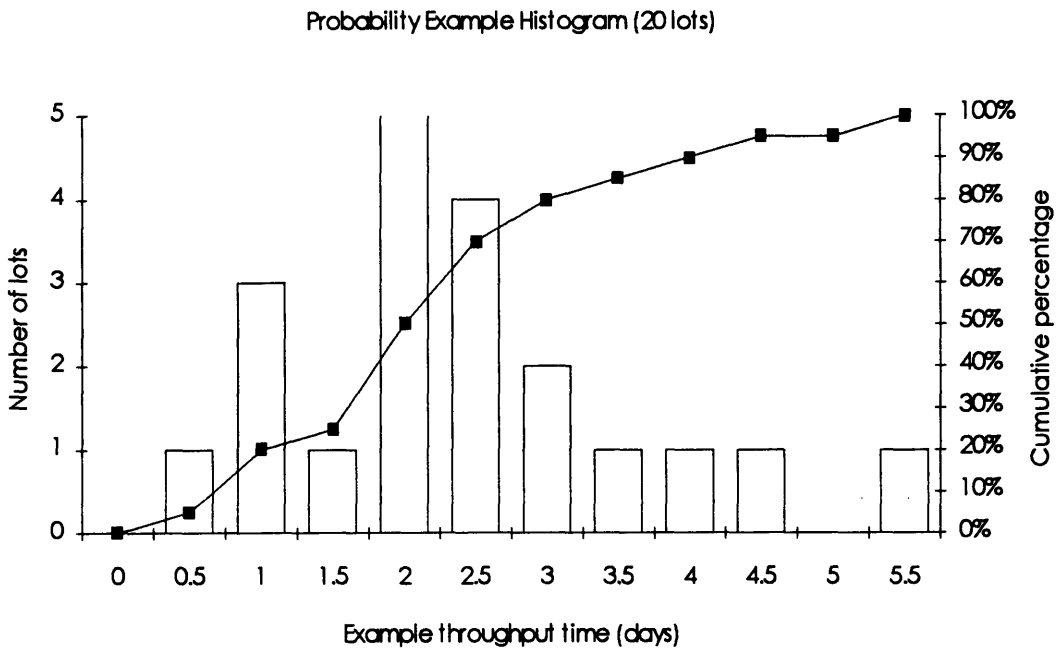


***Figure 6.1: Distribution of example throughput times***

Suppose an order needs to be scheduled to complete this stage within 4 days with an 80% probability of on time delivery. Using the sorted list above, we see that 4 days corresponds to the 18th point in the list. Based on the distribution, this work has a 90% (18/20 = 0.9) chance of finishing within 4 days. Since the 90% probability exceeds the 80% desired, using the work starting at this stage will satisfy the order. If this stage could not meet the desired level, then a later stage would be used. Since this stage slightly exceeded the desired level, an earlier stage may better match the time and probability.

### *Representative Samples*

The number of points chosen to represent the throughput time distribution depends on how much information captures the essence of the variability. The more points that appear in the sample, the more of past history that appears in the values, while using too small a sample may not capture the overall throughput time distribution. Keeping more points also allows more extreme values to appear. Thus, too large a sample may not properly reflect the influence of other factors such as process changes or capacity increases if it includes much of the past.

Figures 6.2, 6.3, 6.4, and 6.5 show the assembly factory throughput time distributions for the last 1000, 500, 250, and 100 lots of Product #1 respectively. As the distributions show, the last 1000 lots capture the overall distribution but also capture the extreme throughput time points indicated by the times greater than 12.5 days. The 500 lot sample mimics the 1000 lot distribution without the extreme points. The 250 lot sample begins to lose the shape of the distribution and also loses some of the lower throughput times as well as the high ones. The 100 lot distribution shows the spread of the values, but does not capture the shape of the distribution, and shows a multi-modal histogram.

Thus, in the case of Product #1 assembly throughput times, a sample greater than 250, and perhaps closer to 500 seems to provide the better sense of the distribution. The actual sample size used would depend on the level of detail desired for estimating probabilities, and the amount of past historical information that provided the best leadtime estimates.

Figures 6.6, 6.7, 6.8, and 6.9 show the advantage of using the actual distribution rather than a mathematical model. The figures show the evolution of the throughput time distribution for 400 lot groups -- a quantity between 250 and 500 -- taken from the 1000 lots shown in figure 6.2. Starting with the first 400 lots completed and moving forward traces the changes in the distribution.

Table 6.1 shows the summary statistics for each 400 lot distribution. Notice how the distributions change over time. The groupings cover the time period from early July to mid-August, mid-July to late August, mid-August to early September, and late August to late September respectively. Over this period, the mean throughput time drops from 5.1 days to 2.9 days and the standard deviation drops from 4.2 days to 2.2 days. This indicates that over these months, the processing of this product became more stable and consistent.

| Completion Statistics | Lots 1-400 | Lots 201-600 | Lots 401-800 | Lots 601-1000 |
|---|---|---|---|---|
| Mean (days) | 5.1 | 4.2 | 3.2 | 2.9 |
| Standard Deviation | 4.2 | 3.2 | 2.3 | 2.2 |
| Variance | 17.3 | 10.2 | 5.2 | 4.7 |
| Range | 34.9 | 34.2 | 29.6 | 29.6 |
| Minimum | 1.9 | 1.7 | 1.2 | 1.2 |
| Maximum | 36.8 | 36.0 | 30.8 | 30.8 |
| Count (lots) | 400 | 400 | 400 | 400 |

***Table 6.1: Summary statistics for Product #1 assembly completions taken at various intervals for the last 1000 lots completed.***

The histograms shown in Figures 6.6 through 6.9 show how the throughput time distributions looked. Notice how over this time period, the height of the distributions near the mean increase indicating a higher concentration of points. The number of extreme points, lots with throughput times greater than 12.5 days decreases as do the number of lots having throughput times between 6.0 and 12.0 days. Also notice how the minimum throughput times shift with the decreasing means.

Using the actual distribution captures not only the variability in the throughput times, but also the fluctuations in the overall shape and boundaries of the values. The danger in using the actual distribution stems from the analysis in the previous chapter which showed the difficulty in predicting future throughput times from past performance. Using the past history of the latest 400 lots to complete as an estimate for probabilities involving future completions may not reflect the current conditions and the times for the lots already in progress. Thus, the more points included in the distribution used for the predictions, the longer the lag in completely refreshing the information, resulting in a less responsive prediction.

### *Implementing the Methodology*

Understanding the tradeoffs and the impacts in selecting different leadtimes for different orders becomes critical to the success of using the new methodology. The scheme presented above allows for easy machine computation and for data collection with minimal interaction.

The methodology works with any kind of throughput time distribution and allows for a flexible quantity of data. Independent from any standard mathematical distributions, no parameters need calculation. Only the maintenance of a sorted list of values and a knowledge of the total number of entries in the listing.

However, the self-fulfilling prophecy represents one danger that exists in using inflated throughput time expectations to determine the probability of on time delivery. A lot expected to complete in 4 days, scheduled to complete in 5 days based on the desired probability, that actually takes five days will still meet the on time delivery criteria. In meeting the criteria, the lot consumed an extra day as work in process and it increased the overall throughput time average. If this occurs repeatedly, this results in an overall increase in the throughput time distribution, which means new orders scheduled with a similar on time probability must carry a larger leadtime cushion. This presents a problem of ever-growing throughput times.

This problem gets exacerbated when order scheduling consistently occurs using large on time delivery probabilities (values close to 100%). In this situation, finding suitable work in process to fulfill the order becomes difficult. In implementing this methodology, the proper incentives must exist to prevent the abuse of the leadtime cushion. The incentives must carry an understanding of the costs associated with carrying extra inventory or work in process.

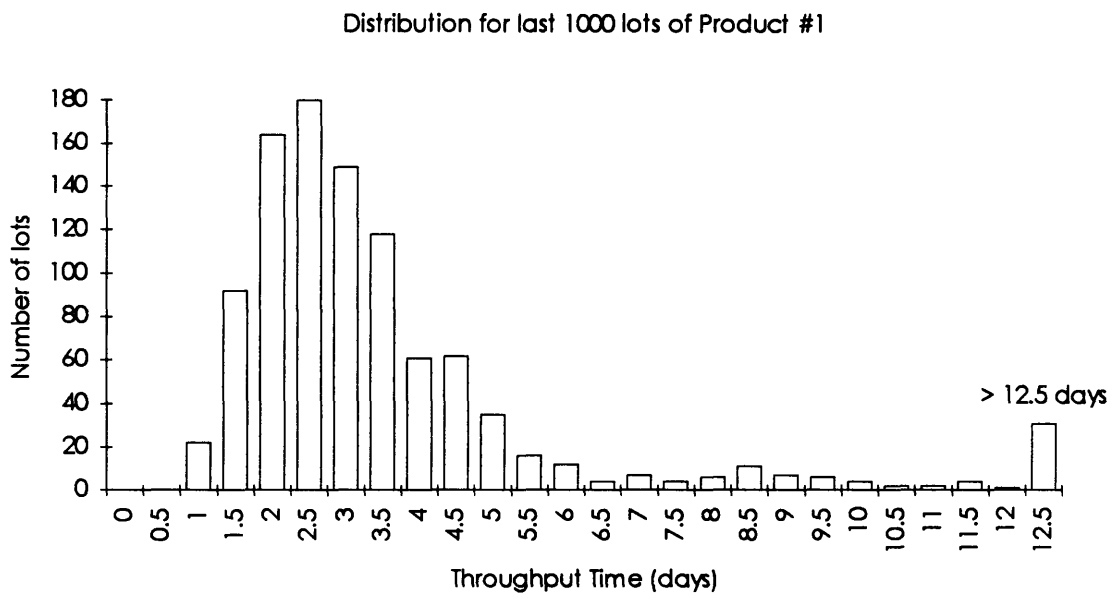


***Figure 6.2: Last 1000 assembly lot throughput times for Product #1.***

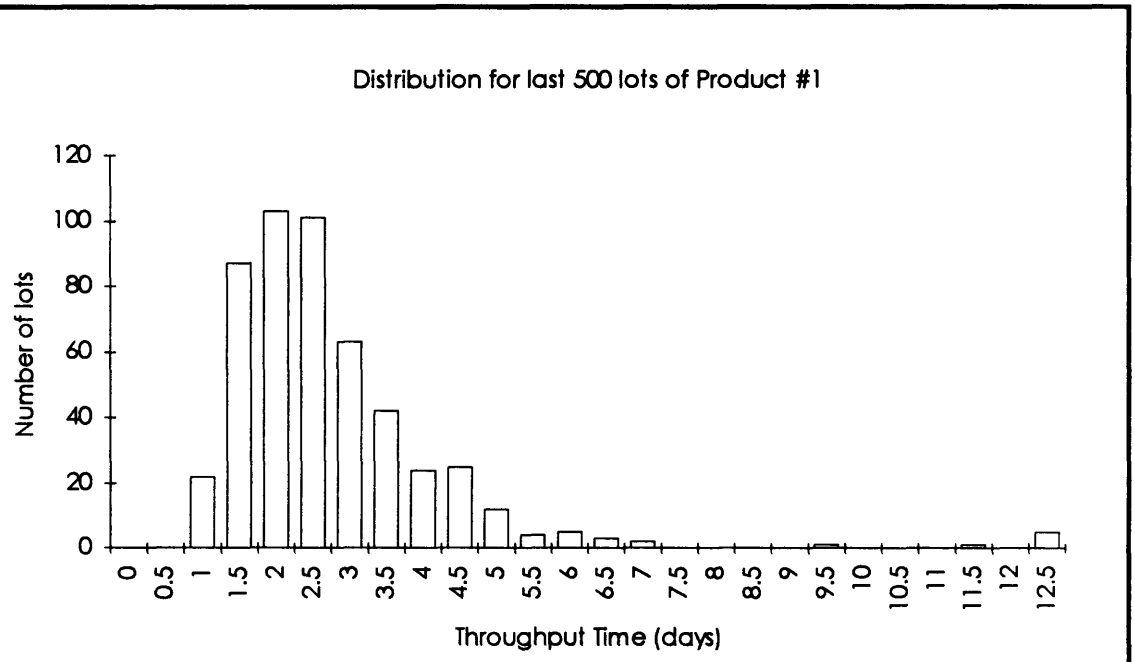


***Figure 6.3: Last 500 assembly lot throughput times for Product #1.***

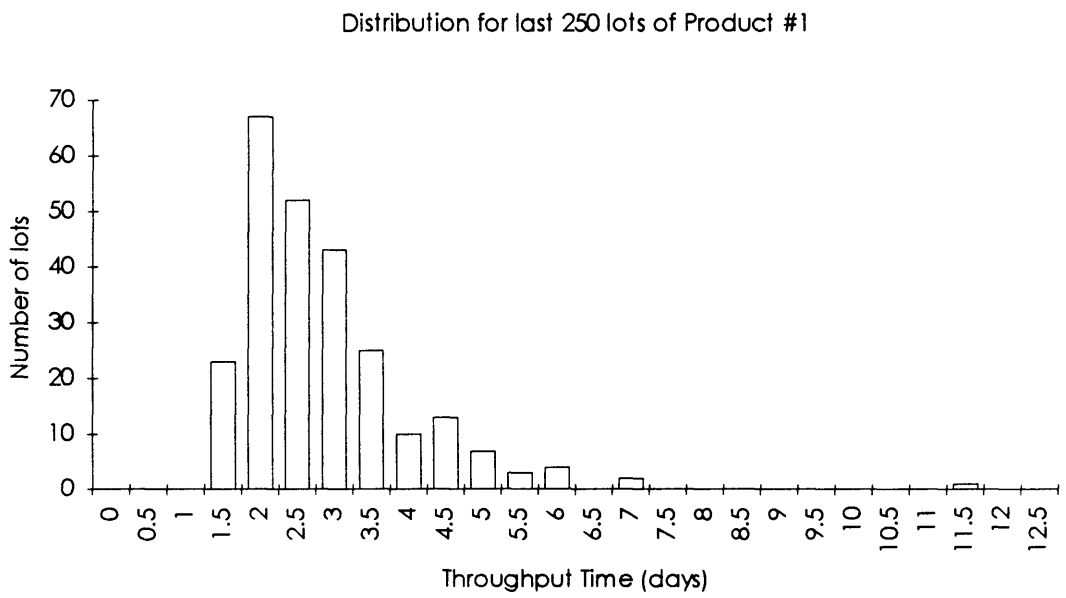


***Figure 6.4: Last 250 assembly lot throughput times for Product #1.***

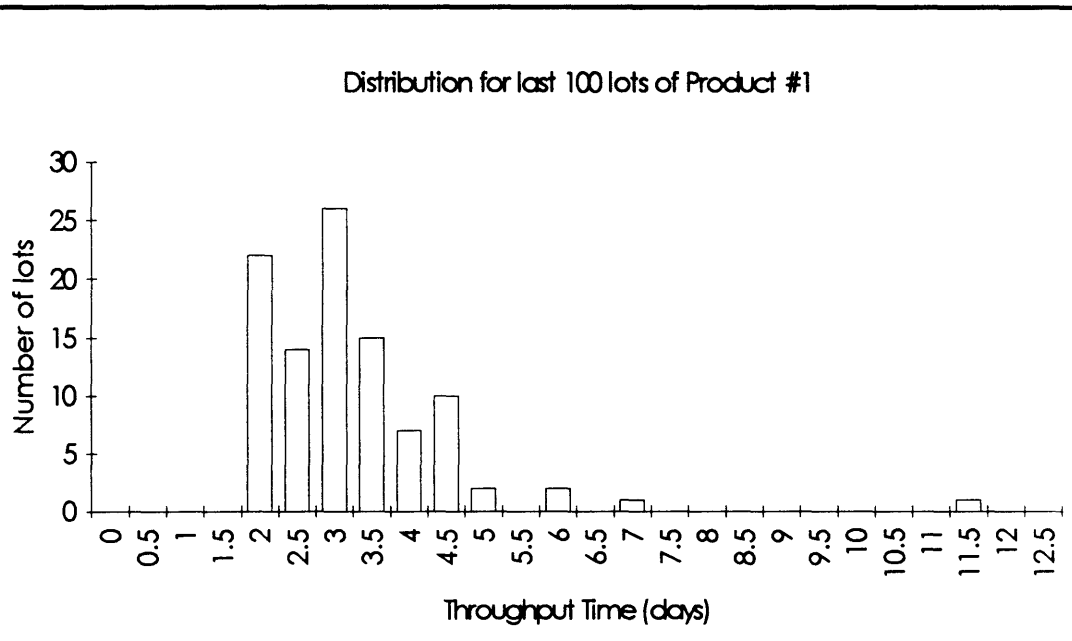


***Figure 6.5: Last 100 assembly lot throughput times for Product #1.***

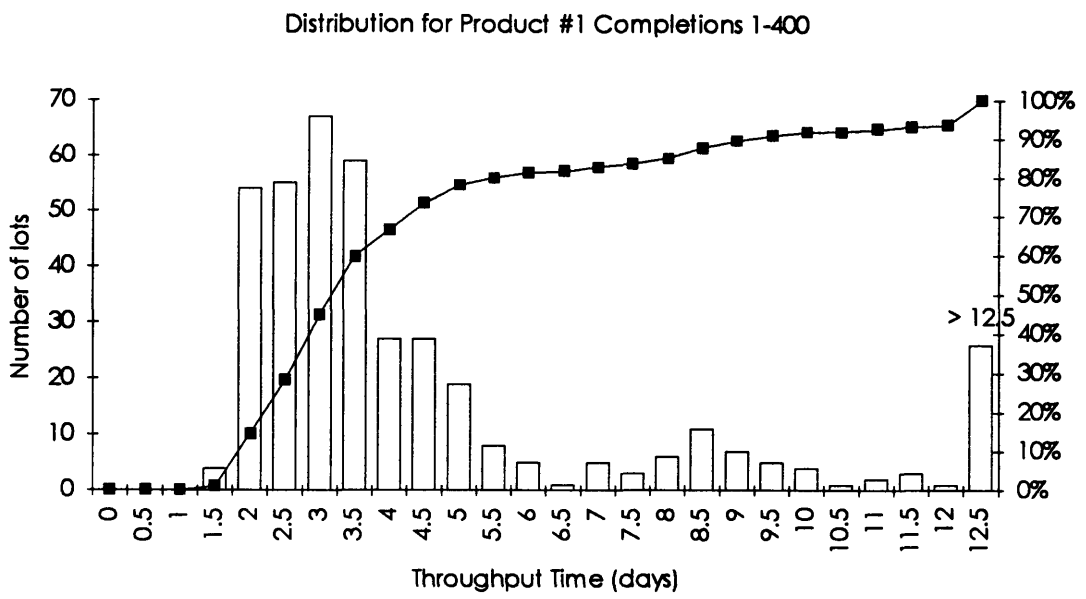


***Figure 6.6: Product #1 assembly lot throughput times for completions 1-400.***

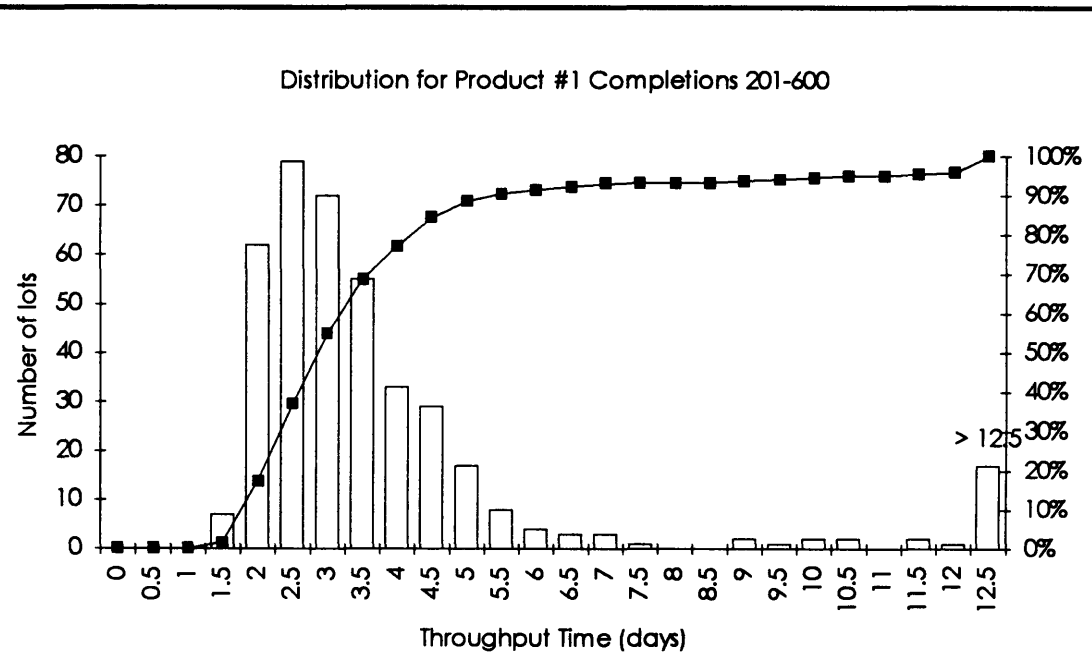


***Figure 6.7: Product #1 assembly lot throughput times for completions 201-600.***

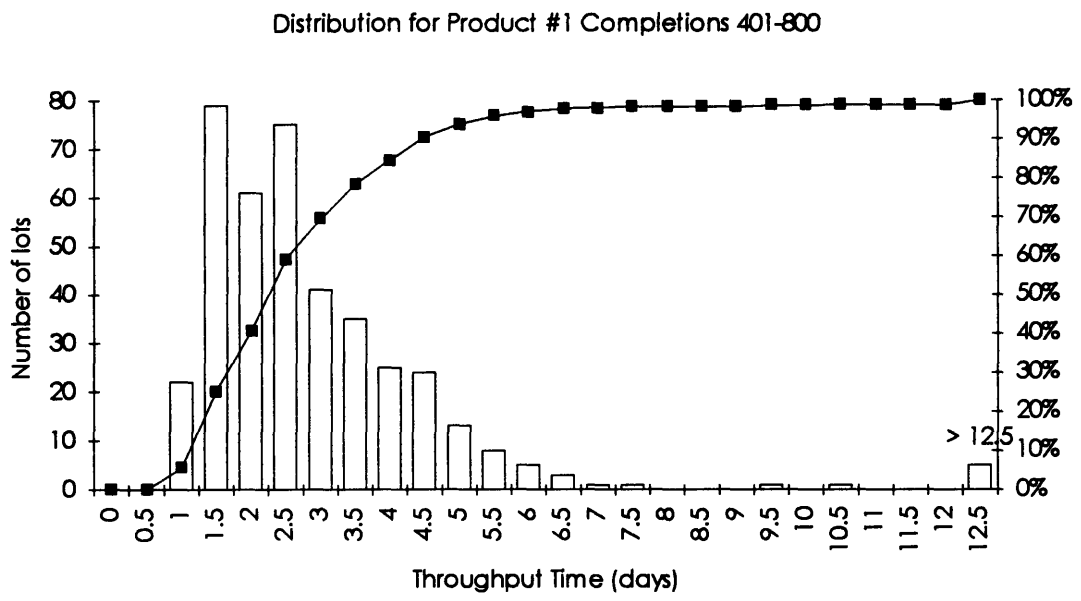


***Figure 6.8: Product #1 assembly lot throughput times for completions 401-800.***

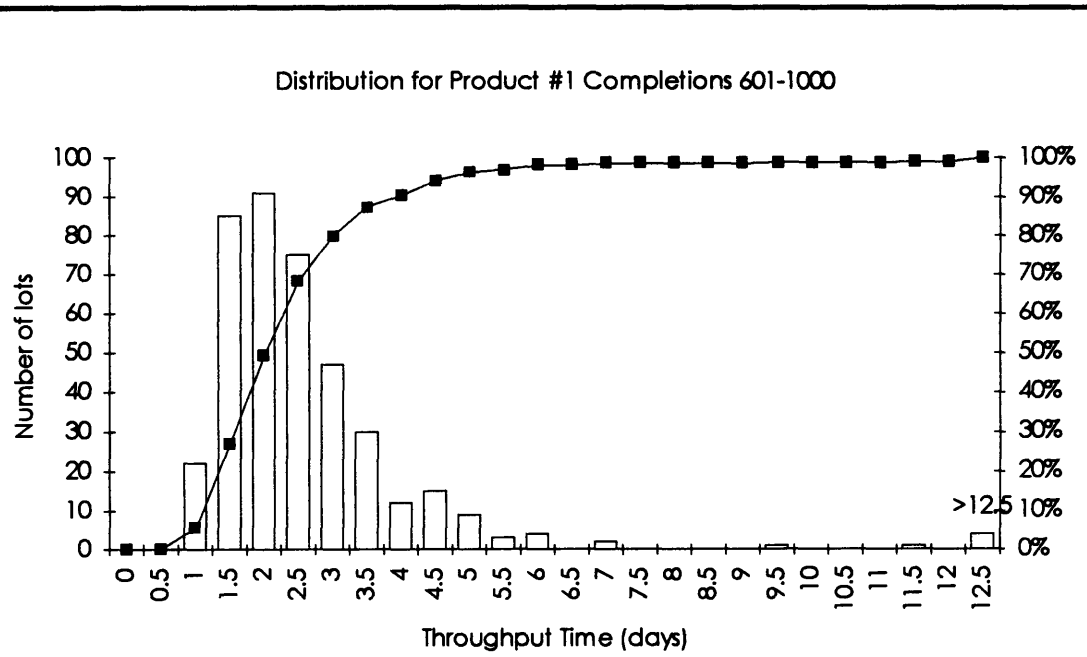


***Figure 6.9: Product #1 assembly lot throughput times for completions 601-1000.***

# Chapter 7- Variability Sources

Understanding the corporate impacts of manufacturing throughput time variability requires an understanding of the variability sources that create the different factory leadtime distributions. During the course of the analysis conducted, a number of different topics arose regarding the causes of the variable throughput times. This chapter discusses those potential variability causes and suggests possible abatement strategies to help both manufacturing and planning address variability.

### *Throughput Time Predictability*

As the throughput time analysis evolved, it became clear that no simple set of variables could create an accurate prediction of future throughput times based on the past times. Lots started from day to day all completed with random throughput times above and below the average, and no set of parameters available from the shop floor tracking data allowed the prediction of the leadtimes.

In the case of the fab, anecdotal evidence from production personnel and Operations Management theory, specifically Little's Law, suggest a link between throughput times and the work in process inventory. However, because different random factors affect lots of one product differently from another, it becomes much more difficult to quantify that relationship.

Figure 7.1 shows the week-by-week relationship between the inventory level and the throughput time for Process #1 in the fab. In general, it appears that the two indicators move in conjunction, but tracing cause and effect becomes difficult. The correlation coefficient for these two indicators came to 0.68.

With the fab throughput times observed, a lot can spend several weeks in the factory. Attempts to correlate the lot throughput times with the inventory changes during the period lots spent in the factory were inconclusive. Delays and other factors confounded the effects of inventory changes on the overall throughput times. With only weekly inventory levels available, the lot-to-lot variability tended to overshadow any underlying trends in throughput times due to the work in process.

Autocorrelation analysis showed no viable relationship between past performance and future throughput times beyond the overall average time. Since products of different volumes or importance receive different treatment within the factory, one expects lower than average throughput times for those products at the expense of other products. Yet any random event within the factory affects all lots within the factory. Add the fact that fab processes repeatedly use the same equipment for each successive layer, and creating a predictive throughput time model based on known factory parameters becomes a difficult task.

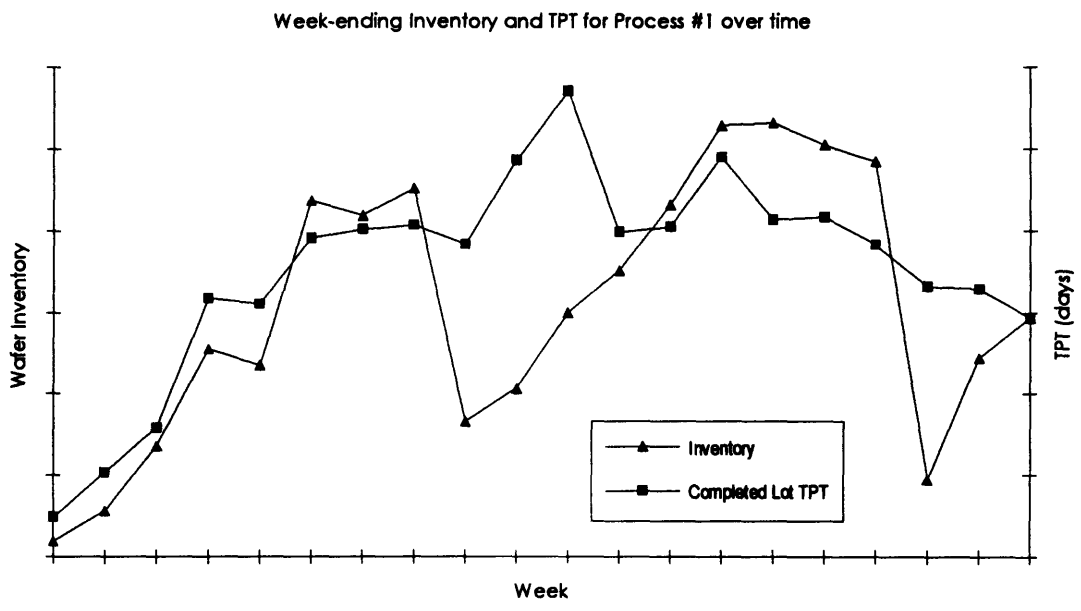


***Figure 7.1: Week by week relationship between week-ending inventory and throughput time for Process #1.***

Other attempts were made to create throughput time predictability using moving averages. Both single day and multiple day moving averages were created as an attempt to predict throughput times (one example appears in Figure 5.15). However, as the analysis in Chapter 5 showed, autocorrelations indicated that very little information beyond the long term average throughput time helps predict what would occur with lots started today. Lot completions occur with such random throughput times that the latest completion does little to help predict what will happen over the next 30 or 40 days to a lot starting today.

Despite the relatively small fractional change an extra day makes for the fab throughput time, the fab may still hold the highest impact. The longer fab throughput times in comparison to the other factory types mean the fab incurs the majority of the manufacturing costs associated with a chip. Coupled with the extremely high expense of building and operating a fab facility, the long leadtimes result in fabs that rarely run with excess capacity. While other factories can absorb variability with excess capacity, the fab must rely on inventory to counteract factory fluctuations. The extra inventory contributes to the lengthening of throughput times and their variability.

The analysis conducted in this project found no set of parameters that could predict future throughput times based on data from past observations. The best estimate of the overall times came from the overall mean on a product specific basis. Using a simulation to

model the various operations within the factory presents one possible avenue for investigation into throughput time predictability.

### *Non-FIFO Factory Flow*

Regardless of the factory, certain decisions within each facility emerge as potential sources of variability. The longer leadtimes and interdependent factory processes within a fab allow more of those decisions to occur, and contribute to the fab's variability. The relatively fast processing in the other factories minimizes the impact at those sites. The flow of lots through any factory exhibits the common theme that the first lot to enter a factory is not the first lot to exit the factory.

As was shown in Chapter 5, the fab exhibited the most disrupted first in, first out flow, even within a product grouping. The shorter throughput time factories showed much less disruption, with only a few lots moving a large number of places impacting the overall order. Due to the complex splitting and recombination of lots within a test factory, the concept of FIFO flow becomes irrelevant.

One expects the lack of first in, first out behavior for different lots on the shop floor since it enables setup preservation. The incentives for all factories focus purely on gross output, and do not emphasize low volume lots. Therefore, to save setup time and process more, high volume lots needing the same processing get batched together at the expense of low volume lots that require equipment changes and adjustments. This enhances both the overall factory output and the individual machine utilization rates; an outcome that brings accolades and rewards.

One of the biggest factory incentives is simply output per week. This means the factory activity increases towards the end of each week, and downstream factories receive the majority of the material expected at the end of the week. Because the fab has traditionally been considered the constraint to production, fab output gets emphasized even more. This means more behavior like that outlined above, where high volume lots receive priority processing, saving time, and increasing output numbers.

Surprisingly, however, lots of identical products also do not exhibit FIFO flow. This means a lot started today may finish before a lot of the identical product started yesterday (or after a lot started tomorrow). Setup preservation cannot explain this phenomenon since the lots are identical.

### *Random Events*

For any one product, every factory strives for FIFO flow through their facility, but random events occur to disrupt it. Within a fab, where the complex process flow brings a lot repeatedly through the same machines, the timing of its movements can contribute significantly to its throughput time outcome. A "lucky" lot that happens to complete one operation just as it's needed for another operation will result in faster than average processing times. "Unlucky" lots, or those unable to travel directly through a factory process, result in slower than average times.

Within a grouping of identical lots all needing the same processing, any lot that requires rework will lose its place in the FIFO order and disrupt the intended flow. Currently, approximately 3% of the lots within a fab undergo some kind of rework. Quality issues within the other factories also contribute to the non-FIFO flows at those sites. If a lot reaches the sort factory but gets put on hold for some evaluation, other lots will skip ahead in the order.

In addition to rework, if a machine breaks down in the middle of processing a particular lot, that lot gets held up, which allows others to pass it in the FIFO order. Machine breakdowns also affect the overall throughput times for all lots within a factory due to the reduction in capacity.

### *Local Dispatching*

Expediting or different priorities within the factory also disrupt the flow. Lots receive different treatment depending on their status (VIP, Hot), their due dates (late, early), their type (production, engineering), and their volume (high, low). In addition, random events like machine breakdowns will have a greater effect on lower volume lots because those lots have fewer in process to smooth out fluctuations, where for high volume lots, early lots from some days make up for late lots from previous days.

The production control function within a factory determines the status of a lot. A VIP lot will receive processing above all other lots, even if it requires a setup change. The factory uses VIP lots to ensure a lot that would normally take a long time gets processed as fast as possible. Usually, VIP lots represent engineering tests with critical results impacting the entire factory.

Production control uses the hot lot status to flag lots needing help getting through the factory. Lots running late or lower volume lots going stale may receive a hot status to move them along. Since hot lots get processed before normal production lots, a hot lot may pass its counterparts in the FIFO order.

Finally, the factory conditions govern the production control decisions dispatching work to various operations. If a machine breakdown occurs or a large amount of work in process exists at an operation, fewer lots that feed the operation get processed. This attempt at balancing the loads within the factory results in some lots having to wait, adding to their throughput times.

### *Variability Abatement*

Production control and factory incentives represent the two main drivers of throughput time variability. Within any factory, the production control priorities determine which lots get processed first, and which lots wait. The factory incentives for output and machine utilization drive high volume lots through the factory at the expense of lower volume lots.

By reducing the number of special status lots, fewer opportunities for disruption would exist which would help eliminate some variability. Late lots should only bear a hot status so long as no other lots are later than the expedited one. This way, late lots will catch up to their counterparts without passing others that should finish earlier. Preserving this order can achieve a more consistent throughput time, reducing the variability.

The output focused factory incentive needs to change to embody lower volume, but extremely important lots. As an example from the fab, when a microprocessor sells as part of a chip set, or a group of chips designed to work together, the microprocessor represents the high volume lots and the supporting chips the low volume lots (since many more of the smaller supporting chips get produced with each lot). Thus, the high volume lots may make their way through the fab much quicker than the supporting chips. However, both chips must finish processing in order to supply them together as part of a set. The factory incentive for output has effectively reduced the usable production because the high volume microprocessors must now wait for the support chips to catch up.

For the lots within any given product grouping, eliminating the effects the random events of machine breakdowns and rework prove difficult. Better control over this type of variability requires a closer study of the different scenarios that result in the loss of FIFO order.

Improving throughput time variability not only helps planning with better leadtime predictability, but also helps improve the overall throughput times for lots within the factory. With increasing time-based competition coupled with the expense associated with running a fab, the impact of long cycle times becomes even more exacerbated. The importance of both faster throughput times and better yields grows with the expense of production.

Figure 7.2 shows a reproduction of an estimate of cycle time impacts on both manufacturing cost and die yield. It shows that to achieve near theoretical throughput times (below 2 times theoretical), the capital investment in excess capacity becomes

prohibitively expensive. Above this point, as the throughput time extends to larger multiples of the theoretical time, the cost increases steadily. The chart shows the minimum cost at somewhere around 2.5 times theoretical.

However, yield decreases linearly with cycle time. The longer a lot spends in the factory, the more likely some defect causing event will occur. Also, a longer throughput time might indicate that processing interruptions may have occurred leading to lower quality output. Thus, addressing the issues of cycle times as well as variability becomes important.

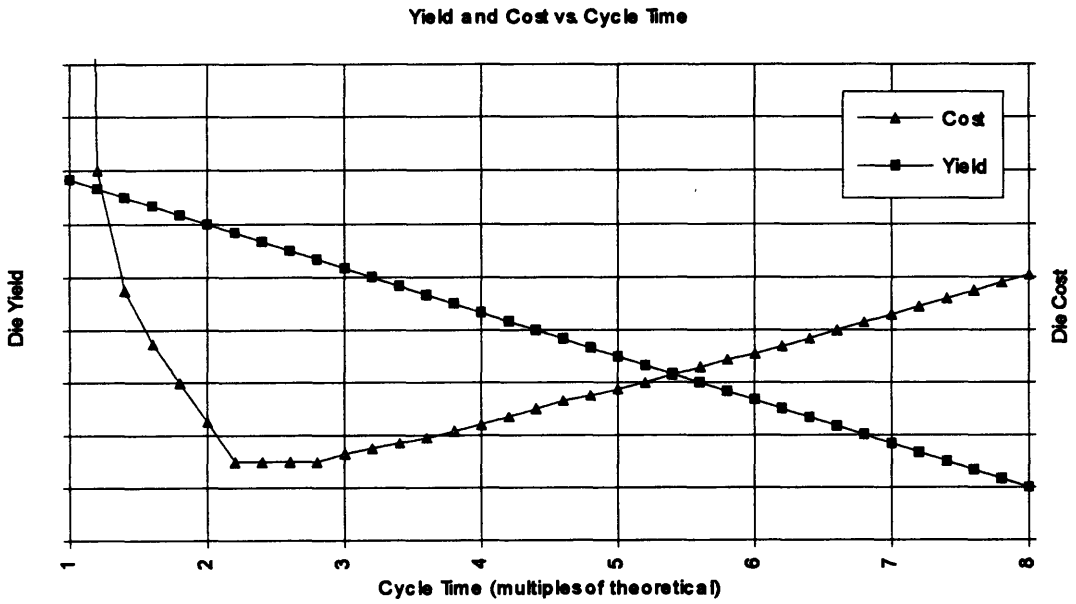


*Figure 7.2: Impact of cycle time on die yield and die cost*

Source: Thomas Group Inc. © 1986

## Chapter 8 - Future Directions and Recommendations

The throughput time variability analysis conducted as part of this project characterized the different leadtime distributions for each stage of Intel's manufacturing process. The characterizations will help provide inputs to planning and scheduling decisions and help enable a more accurate planning and scheduling system. The analysis uncovered a number of different sources for manufacturing throughput time variability which other projects can address.

This chapter indicates seven areas with opportunities to extend the scope and application of this work for future projects and study:

- Integrated commit
- Detailed internal factory analysis
- Yield variability planning
- Inventory level optimization
- Delivery performance indicators
- Multi-parameter characterization
- Comparisons with factory actuals

### *Integrated Commit*

As described in Chapter 4, the Integral Planning and Delivery system represents a paradigm shift in Intel's planning principles. Throughput time variability information enables tradeoffs between manufacturing leadtimes and customer service levels. Called Integrated Commit, the ultimate vision for making these tradeoffs marries supply and demand in a single process.

Within the Integrated Commit framework, customer orders will link directly to factory supply in real time. This means the system must simultaneously determine the available factory supply and the timing of this availability given the current factory conditions and the customer service level desired. Thus, the new process integrates customer demand and factory supply in real time. This scheduling process must comprehend all the different areas of variability to ensure customer orders ship on-time in the correct quantities.

The order taking process will automatically assign the factory supply satisfying the customer order and maintain the capacity consumption as well. As described previously, the manufacturing throughput time variability plays an important role in both order scheduling and capacity resource allocation.

Thus, the variability methodology must extend on a product specific level so the new system can commit any end item to a customer order. The amount of data required for a given level of granularity in scheduling (i.e., hours vs. days) and the large number of

distinct end items Intel sells requires further investigation for the incorporation of leadtime variability.

### *Detailed Internal Factory Analysis*

The factory throughput time analysis was performed at an aggregate level treating each factory as a whole. Chapter 7 describes the main sources of throughput time variability discovered during the analysis. However, effectively targeting areas for variability reduction requires an in-depth analysis of the operations within each factory that comprise the overall throughput time. In addition, detailed operation-by-operation knowledge of throughput time variability enables a much more accurate capacity model for scheduling purposes.

Understanding the causes of extreme variability by following the detailed processes within any given production stage will help highlight the key areas impacting the leadtimes. The analysis performed for this project shows the kind of throughput time distributions produced by the different factory types and discusses some of the main sources of variability, but it needs more detail to determine the specific variability causes.

Characterizing the direct causes of throughput time variability also creates the opportunity for a much more accurate capacity model. Distributions of throughput times can help determine when to expect capacity consumption or order delivery in an integrated fashion more accurately than point estimates for operation times.

### *Yield Variability Planning*

Factory yields represent another key planning parameter not addressed by this project. Since yields fall in a distribution in the same way as throughput time, the manufacturing planning system can make tradeoffs between yield and customer service in the same way as for throughput times.

Since an order can ship late but cannot ship without full quantity, this added restriction makes incorporating yield variability slightly more difficult. However, making the tradeoffs and choices for satisfying customer orders can still occur with knowledge of yield distributions.

### *Inventory Level Optimization*

Comprehending yield variability in conjunction with throughput time variability also allows for optimally sizing inventories. An inventory level that accounts for fluctuations in both the leadtime and quantity based on the known throughput time and yield distributions could represent potential savings in excess inventory costs. Properly sizing inventories not only saves carrying costs, but also ensures the availability of the needed products at each production stage.

In addition to properly sizing inventory levels, the knowledge of the different distributions for the planning parameters allows for the potential elimination of some costly inventories. If the leadtime and variability reduction occurred to the point where fewer buffers could still deliver the same level of customer service, then increased inventory savings and better planning accuracy result.

### *Delivery Performance Indicators*

During the time period for this project, Intel's Business Performance Metrics Team developed a new set of indicators to both measure the success of the new systems development and to encourage improvement in Intel's planning and delivery performance. Intel management chartered the group to create a set of corporate performance indicators in order to assess the progress and success of the Integral project, the other systems under development, and of Intel's business as a whole. The metrics should ensure the progress towards the overall objective of "reducing customer leadtime and improving delivery precision while increasing Intel's responsiveness and ease of doing business and reducing the cost to Intel".

The Metrics team defined six separate metrics to measure Intel's business:

- On time delivery performance
- Cycle time (manufacturing throughput time)
- Inventory
- Customer inquiry satisfaction
- Planning productivity
- Planning cycle time (administrative processing time)

Both long term goals and interim implementation targets define the desired improvements in the listed metrics. Some of the metrics, such as the planning productivity indicator, deal with the administrative improvements the new system should bring about, while others deal with improvements in the company's operations.

The comprehension of manufacturing throughput time variability can both play a part in the improvement of the operations and provide valuable information in the calculation of the indicators. The previous section discussed the potential use of throughput time variability for optimizing inventory levels. This would result in inventory levels set by some optimization algorithm rather than setting an arbitrary target level or number of inventory turns (the ratio of total inventory used during the year to the average inventory level held).

The calculated throughput times, and the different product groupings used in the analysis for this project can also provide the basis for the cycle time performance metric. Calculated leadtimes provide a baseline for comparison to current metrics and can assist in

setting new targets. In addition, the data collection methods provide a good starting point for the automation of throughput time calculations.

### *Multi-parameter Characterization*

As discussed in Chapter 7, throughput time predictability proved difficult when based solely on past leadtime data. However, anecdotal evidence from the fab production personnel suggests a link between several manufacturing parameters such as throughput time, work in process inventory, line yield, die yield, product mix, and the number of lots started into the factory.

For example, as throughput times increase, yields may decrease due to the extended period of potential exposure to contaminants and risk of damage. Longer throughput times may also contribute to higher costs, since problems get recognized later and affect more lots when leadtimes grow longer. But those higher throughput times may result from the current inventory level, which in turn may depend on the number of lots started at any one time.

The close relationship between all these factors suggests a comprehensive multi-parameter characterization of the factory can occur. This may require complex simulation in order to achieve valuable results, but gaining an understanding of the interdependencies between all these different factory variables allows for optimization across all the factors.

### *Comparisons with Factory Actuals*

Finally, the calculated throughput times provide a basis for comparison between the leadtime planning parameters used for factory scheduling and the actual throughput times seen by the lots. The analysis discussed in Chapter 5 indicated product specific leadtimes for products of different volumes within the factory, but planning occurs using an overall process leadtime.

The factories recognize and acknowledge that lower volume lots often have longer throughput times, but they still schedule using a single estimate. The study and characterization of manufacturing throughput time variability can help communicate the product-to-product differences that exist within the factory. These differences can then be explicitly planned for a more accurate schedule or used to make production control tradeoffs between those lots requiring priority handling.

### *Implementation Issues*

A single statement summarizing the key implementation issues faced when addressing the subject of manufacturing throughput time variability is "structure influences behavior". The factory incentive system and the corporate organization represent the two structures which in particular influence the behaviors seen in this analysis.

The factory incentive for output encourages the production environment to take full advantage of the resources available. However, an emphasis placed solely on the quantity, but not the mix, of output, creates an incentive to just produce, rather than provide the needed quantities of different products. Thus, setups are preserved, and high volume lots receive processing priority at the expense of low volume lots. This increases throughput time variability.

In the use of factory throughput time distributions to set expected leadtimes for orders, the danger of a self-fulfilling prophecy creates a hazard to implementation. In cases where a high probability of on time delivery is desired, longer leadtimes are chosen and expected. This allows for a longer leadtime without penalty. If the result is a longer leadtime, the overall distribution shifts, and hence creates longer leadtimes for all production. Thus, choosing different leadtimes may add to leadtime variability in the attempt to minimize the effects of variability.

The Intel organizational structure also limits the ability to implement methodologies that address variability. While each factory has output driven incentives, no incentive exists for cross-factory or cross-organizational optimization. Each individual site strives to meet its individual goals in a locally optimized system.

The separation between the geographies, divisions, manufacturing, and planning systems creates an artificial barrier to information sharing. Without any structure to guide towards a globally optimized objective, these groups continue to focus on individual incentives. Thus, the organizational structure itself creates impediments to implementation.

### *In Closing*

The increasing competitiveness in today's computer industry forces manufacturers to adopt better production techniques. These new methods force their suppliers to deliver better customer service and more reliable on time delivery.

This project examined the manufacturing throughput time variability of Intel's various production stages. The analysis characterized the throughput time variability for the different factory types and discussed a number of different factors which influence both the throughput times and their variability. The areas mentioned above highlight some of the most promising potential extensions to the use of throughput time variability information.

A new planning and scheduling system which incorporates manufacturing variability concepts impacts several different areas both directly and indirectly. By introducing new ideas in the area of manufacturing systems, the new systems can potentially provide the required impetus for business process change.

Throughput time variability impacts all areas of Intel's business from manufacturing to order fulfillment to business process performance indicators. Manufacturing throughput time variability represents only the beginning of fully incorporating variability concepts in all aspects of their operations.

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# Appendix A - Goodness of fit analysis

Goodness of fit analysis

| Fab Process #1 Summary Statistics (no outliers) | | TPT (days) | Actual Number of Lots | Normal Expected Count | Chi Square Values |
|---|---|---|---|---|---|
| | | 23 | 0 | 2.2 | 2.2 |
| Mean | 34.2 | 24 | 1 | 5.2 | 3.4 |
| Standard Deviation | 3.4 | 25 | 7 | 11.3 | 1.6 |
| Variance | 11.7 | 26 | 19 | 22.5 | 0.5 |
| Kurtosis | 0.2 | 27 | 52 | 41.2 | 2.8 |
| Skewness | 0.3 | 28 | 68 | 69.4 | 0.0 |
| Range | 21.3 | 29 | 93 | 107.4 | 1.9 |
| Minimum | 24.3 | 30 | 141 | 152.8 | 0.9 |
| Maximum | 45.5 | 31 | 208 | 199.7 | 0.3 |
| Count | 2323 | 32 | 265 | 239.9 | 2.6 |
| | | 33 | 317 | 264.7 | 10.3 |
| | | 34 | 283 | 268.3 | 0.8 |
| Chi Square DOF = 23 - 3 | 20 | 35 | 286 | 250.0 | 5.2 |
| Chi Square (0.95, 20) = | 10.9 | 36 | 177 | 214.0 | 6.4 |
| | | 37 | 105 | 168.3 | 23.8 |
| | | 38 | 75 | 121.6 | 17.9 |
| | | 39 | 75 | 80.8 | 0.4 |
| | | 40 | 63 | 49.3 | 3.8 |
| | | 41 | 43 | 27.6 | 8.6 |
| | | 42 | 22 | 14.2 | 4.2 |
| | | 43 | 15 | 6.7 | 10.2 |
| ***Cannot conclude*** | | 44 | 4 | 2.9 | 0.4 |
| ***goodness of fit.*** | | 45 | 4 | 1.2 | 6.8 |
| | | Totals | 2323 | | 115.2 |

Normal Expected Count based on the total number of lots and a normal distribution having a mean and standard deviation equalling the values listed in the above table.

Chi-Squared value = (Actual count - Expected count)^2 / Expected count

Goodness of fit analysis

| Fab Process #2 Summary Statistics (no outliers) | | TPT (days) | Actual Number of Lots | Normal Expected Count | Chi Square Values |
|---|---|---|---|---|---|
| | | 30 | 1 | 0.4 | 1.1 |
| Mean | 52.4 | 31 | 0 | 0.6 | 0.6 |
| Standard Deviation | 6.3 | 32 | 0 | 1.0 | 1.0 |
| Variance | 39.6 | 33 | 1 | 1.7 | 0.3 |
| Kurtosis | 0.3 | 34 | 0 | 2.7 | 2.7 |
| Skewness | 0.4 | 35 | 0 | 4.1 | 4.1 |
| Range | 44.2 | 36 | 6 | 6.2 | 0.0 |
| Minimum | 30.0 | 37 | 10 | 9.2 | 0.1 |
| Maximum | 74.2 | 38 | 14 | 13.2 | 0.0 |
| Count | 2341 | 39 | 7 | 18.5 | 7.1 |
| | | 40 | 15 | 25.2 | 4.1 |
| | | 41 | 28 | 33.6 | 0.9 |
| Chi Square DOF = 45 - 3 = | 42 | 42 | 30 | 43.6 | 4.2 |
| Chi Square (0.95, 20) = | 28.1 | 43 | 61 | 55.2 | 0.6 |
| | | 44 | 74 | 68.1 | 0.5 |
| | | 45 | 100 | 81.9 | 4.0 |
| | | 46 | 124 | 96.2 | 8.0 |
| | | 47 | 111 | 110.1 | 0.0 |
| | | 48 | 133 | 122.8 | 0.8 |
| | | 49 | 167 | 133.7 | 8.3 |
| | | 50 | 151 | 141.9 | 0.6 |
| | | 51 | 159 | 146.8 | 1.0 |
| | | 52 | 142 | 148.2 | 0.3 |
| | | 53 | 126 | 145.8 | 2.7 |
| | | 54 | 124 | 139.9 | 1.8 |
| | | 55 | 146 | 130.9 | 1.7 |
| | | 56 | 119 | 119.4 | 0.0 |
| | | 57 | 101 | 106.3 | 0.3 |
| | | 58 | 63 | 92.2 | 9.2 |
| | | 59 | 62 | 78.0 | 3.3 |
| | | 60 | 43 | 64.3 | 7.1 |
| | | 61 | 44 | 51.8 | 1.2 |
| | | 62 | 38 | 40.6 | 0.2 |
| | | 63 | 33 | 31.1 | 0.1 |
| | | 64 | 24 | 23.2 | 0.0 |
| | | 65 | 26 | 16.9 | 5.0 |
| | | 66 | 11 | 12.0 | 0.1 |
| | | 67 | 18 | 8.3 | 11.4 |
| | | 68 | 4 | 5.6 | 0.4 |
| | | 69 | 7 | 3.7 | 3.0 |
| | | 70 | 6 | 2.4 | 5.6 |
| | | 71 | 4 | 1.5 | 4.3 |
| | | 72 | 5 | 0.9 | 18.7 |
| ***Cannot conclude*** | | 73 | 2 | 0.5 | 4.0 |
| ***goodness of fit.*** | | 74 | 1 | 0.3 | 1.5 |
| | | Totals | 2341 | | 132.4 |

Normal Expected Count based on the total number of lots and a normal distribution having a mean and standard deviation equalling the values listed in the above table.

Chi-Squared value = (Actual count - Expected count)^2 / Expected count

## Appendix B - Sample transaction listing

Appendix B - Sample transaction listing

| From Date | From Time | To Date | To Time | Calc TPT (days) |
|---|---|---|---|---|
| 5/20/93 | 15:02:02 | 6/16/93 | 10:04:19 | 26.7933 |
| 5/22/93 | 0:03:15 | 6/17/93 | 2:00:14 | 26.0812 |
| 5/22/93 | 0:07:00 | 6/22/93 | 2:50:05 | 31.1133 |
| 5/22/93 | 13:36:19 | 6/21/93 | 10:36:49 | 29.8753 |
| 5/22/93 | 13:36:35 | 6/22/93 | 1:53:48 | 30.5120 |
| 5/22/93 | 23:47:30 | 6/21/93 | 18:58:35 | 29.7994 |
| 5/22/93 | 23:47:57 | 6/21/93 | 12:24:39 | 29.5255 |
| 5/22/93 | 23:48:52 | 6/22/93 | 8:27:17 | 30.3600 |
| 5/22/93 | 23:49:14 | 6/17/93 | 6:08:56 | 25.2637 |
| 5/23/93 | 13:38:47 | 6/21/93 | 8:54:20 | 28.8025 |
| 5/23/93 | 23:54:56 | 6/22/93 | 10:38:29 | 29.4469 |
| 5/23/93 | 23:56:48 | 6/23/93 | 1:48:09 | 30.0773 |
| 5/24/93 | 0:00:04 | 6/22/93 | 10:30:18 | 29.4377 |
| 5/24/93 | 0:03:35 | 6/23/93 | 8:43:58 | 30.3614 |
| 5/24/93 | 0:06:52 | 6/21/93 | 12:29:45 | 28.5159 |
| 5/24/93 | 0:08:15 | 6/21/93 | 10:48:08 | 28.4444 |
| 5/24/93 | 12:44:58 | 6/21/93 | 16:03:29 | 28.1379 |
| 5/24/93 | 12:45:02 | 6/22/93 | 16:30:59 | 29.1569 |
| 5/24/93 | 12:45:04 | 6/22/93 | 16:07:53 | 29.1408 |
| 5/24/93 | 12:45:11 | 6/23/93 | 10:01:39 | 29.8864 |
| 5/24/93 | 12:45:17 | 6/22/93 | 6:13:07 | 28.7277 |
| 5/25/93 | 0:44:54 | 6/21/93 | 8:52:09 | 27.3384 |
| 5/25/93 | 14:32:19 | 6/22/93 | 3:55:43 | 27.5579 |
| 5/25/93 | 14:33:13 | 6/22/93 | 15:34:01 | 28.0422 |
| 5/25/93 | 14:34:05 | 6/21/93 | 16:06:22 | 27.0641 |
| 5/25/93 | 14:34:55 | 6/23/93 | 15:26:47 | 29.0360 |
| 5/25/93 | 14:35:56 | 6/21/93 | 14:13:55 | 26.9847 |
| 5/25/93 | 14:36:51 | 6/23/93 | 19:57:57 | 29.2230 |
| 5/25/93 | 14:40:45 | 6/22/93 | 4:38:14 | 27.5816 |
| 5/25/93 | 14:41:49 | 7/2/93 | 21:47:27 | 38.2956 |
| 5/25/93 | 14:42:28 | 6/25/93 | 5:28:26 | 30.6153 |
| 5/25/93 | 14:43:24 | 6/21/93 | 14:17:44 | 26.9822 |
| 5/25/93 | 14:44:03 | 6/22/93 | 16:53:46 | 28.0901 |
| 5/25/93 | 14:44:38 | 6/22/93 | 14:42:57 | 27.9988 |
| 5/26/93 | 12:29:22 | 6/22/93 | 9:07:02 | 26.8595 |
| 5/26/93 | 12:29:23 | 6/24/93 | 13:02:37 | 29.0231 |
| 5/26/93 | 23:48:15 | 6/22/93 | 13:43:12 | 26.5798 |
| 5/26/93 | 23:49:07 | 6/23/93 | 17:20:59 | 27.7305 |
| 5/26/93 | 23:49:46 | 6/24/93 | 1:31:35 | 28.0707 |
| 5/26/93 | 23:50:31 | 6/23/93 | 17:50:19 | 27.7499 |
| 5/26/93 | 23:51:52 | 6/25/93 | 12:59:34 | 29.5470 |
| 5/26/93 | 23:52:46 | 6/24/93 | 12:44:40 | 28.5360 |
| 5/26/93 | 23:54:31 | 6/25/93 | 0:01:21 | 29.0047 |
| 5/26/93 | 23:55:23 | 6/25/93 | 5:26:33 | 29.2300 |

Calc TPT = (To Date + To Time) - (From Date + From Time)