A Josephson Junction Bridge Track and Hold Circuit

by

Kimo Y.F. Tam

Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of

Doctor of Science in Electrical Engineering

at the Massachusetts Institute of Technology

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Abstract

A high-speed monolithic Josephson junction track and hold (T/H) circuit was designed, fabricated, and tested. The circuit consists of a novel Josephson junction bridge current switch and a superconducting hold inductor. The bridge, under the control of a common-mode clock current, modulates a balanced, differential input current. A two-junction Superconducting Quantum Interference Device (SQUID) in a flux-lock loop configuration serves as the readout circuit. The T/H was fabricated at MIT Lincoln Laboratory in the Dual-dielectric Selective Niobium Anodization Process (DSNAP) using conservative 5 μm minimum geometry and 1000 A/cm^2 critical current density. It was designed to be tolerant to a wide range of absolute critical current density, sheet resistance, and contact resistance rather than for optimum speed or resolution. The input signal range of the T/H is conservatively specified at ±320 μA, and the output current is quantized in 20 μA steps, resulting in 5-bit dynamic range. Calculations and simulations of the T/H predict a 750 MHz analog tracking and sampling bandwidths, 4.6-bit effective dc resolution, an acquisition time of 725 ps, a 700 MS/s peak sampling rate, and an unlimited hold time. Measurements of the fabricated T/H show that it has 900 MHz analog tracking and sampling bandwidths, 4.5-bit effective dc resolution, and an acquisition time of 550 ps, commensurate with a 900 MS/s peak sampling rate.

Thesis Supervisor:	Professor James K. Roberge
Title:	Professor of Electrical Engineering

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My parents, grandmother, Aunt Evelyn, the sumo, and Leo.

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1 - Introduction

1.1 - Josephson Junction Characteristics and Models

The field of Josephson junctions is exceedingly rich, and the literature is extensive. The Josephson junction (JJ) is also quite versatile; it finds application in a wide variety of superconducting circuits. The purpose of this section is to summarize the set of equations and models necessary to design and analyze the track and hold bridge rather than to comprehensively review either the Josephson junction or superconductivity as a whole. Several textbooks address superconductivity and the Josephson junction in great detail (see, for example, [1] – [3]).

1.1.1 - Josephson Supercurrent

A Josephson junction consists of two superconducting electrodes separated by a thin dielectric barrier. Through the junction can flow a superconducting current component (a supercurrent, I_S) which is well described by the fundamental Josephson current-phase equation:

$$I_S = I_c \sin\phi \tag{1.1}$$

where ϕ is the phase difference between the wavefunctions describing the superelectrons in the two superconductors, and I_c is the critical current of the junction. The critical current is a function of temperature, as will be shown later, and of magnetic field. Specifically, I_c can be suppressed by subjecting the junction to a magnetic field. This magnetic field can be applied via a control current passed through a wire placed in close proximity to the junction.

The critical current is also a strong function of the dielectric thickness:

$$I_c = I_{c,o} \exp\left(\frac{-d}{d_o}\right) \tag{1.2}$$

where $I_{c,o}$ is the extrapolated zero-barrier critical current, d is the barrier thickness, and d_o ~ 10^{-10} m is a constant. The critical current of the junction also depends on the dimensions of its electrodes. In the small-area limit, the supercurrent is nearly uniformly distributed, and it is natural to introduce the critical current density, J_c:

$$J_c = I_c / A, \quad A << \lambda_J^2 \tag{1.3}$$

where A is the area (normal to the direction of current flow) of the junction, and λ_J is a characteristic length, the Josephson penetration depth. For planar tunnel junctions such as those used to fabricate the track and hold, the Josephson penetration depth is given by:

$$\lambda_J = \sqrt{\frac{h/2e}{2\pi\mu_o(d+\lambda_1+\lambda_2)J_c}} \tag{1.4}$$

where $h \approx 6.626 \times 10^{-34}$ J·s is Planck's constant, $e \approx 1.602 \times 10^{-19}$ C is the electron charge, $\mu_o \approx 1.257 \times 10^{-6}$ H/m is the permeability of free space, λ_1 and $\lambda_2 \sim 10^{-8}$ m are the magnetic penetration depths in the two superconductors, and d is again the thickness of the dielectric.

In the small-area regime, junctions having different critical currents can be made by simply scaling the areas of the junctions. However, the critical current in the large area regime ($A >> \lambda_J^2$) saturates at a value nearly independent of the area of the junction. The maximum achievable critical current is independent of the critical current density [1]:

$$I_{c,\max} = KJ_c\lambda_J^2 = K\frac{h/2e}{2\pi\mu_o(d+\lambda_1+\lambda_2)} \tag{1.5}$$

where K is a constant of order unity.

1.1.2 - Josephson Voltage-Phase

The second fundamental Josephson junction equation, the voltage-phase relationship, relates the voltage across the junction to the time rate of change of the phase:

$$V = \frac{\hbar}{2e}\frac{d\phi}{dt} = \frac{\Phi_o}{2\pi}\frac{d\phi}{dt} \tag{1.6}$$

where $\hbar = h/2\pi \approx 1.055 \times 10^{-34}$ J·s is the reduced Planck's constant. The flux quantum, Φ_o, is an important fundamental constant given by:

$$\Phi_o \equiv \frac{h}{2e} \approx 2.068\times10^{-15}\ \text{Wb} = 2.068\ \text{pH}\cdot\text{mA} = 2.068\ \text{ps}\cdot\text{mV} \tag{1.7}$$

Eqn. 1.6 implies that a positive dc voltage applied across a Josephson junction will give rise to a linearly increasing phase, and hence a sinusoidally varying supercurrent. The frequency of this oscillation is:

$$\omega_J = 2\pi\cdot f_J = \frac{2\pi}{\Phi_o}V_{dc} \tag{1.8}$$

where ω_J is the Josephson oscillation frequency and V_{dc} is the average voltage across the junction. Since $\Phi_o^{-1} \approx 484$ GHz/mV, the frequency of oscillation is generally in the microwave range for typical junction voltages.

Eqn. 1.6 can be also be cast in another form to elucidate the relationship between the phase and the magnetic flux, Φ, in a superconducting loop. By Faraday's Law, the integrated electric field (voltage) along a closed contour is equal to the time rate of change of the enclosed magnetic flux (i.e., the integrated magnetic flux density, B):

$$V = \frac{d\Phi}{dt}, \quad \Phi = \int \mathbf{B} \cdot d\mathbf{A} \tag{1.9}$$

Therefore:

$$\phi = 2\pi \frac{\Phi}{\Phi_o} \tag{1.10}$$

where the constant of integration is assumed to be zero.

Eqn. 1.10 illustrates that one flux quantum threading a superconducting loop amounts to a 2π phase difference around the loop. An important consequence of this correlation is that the supercurrent described by Eqn. 1.1, which is 2π-periodic in ϕ, is also Φ_o-periodic in Φ. This phenomenon is useful in numerous superconducting circuits.

1.1.3 - The S State and Josephson Inductance

It is clear from the fundamental Josephson equations (Eqn. 1.1 and Eqn. 1.6), that a constant current yields a constant phase and hence zero voltage across the junction. If the current through the junction satisfies the constraint, $|I| \leq I_c$, it can be carried entirely as a supercurrent, $I = I_S$, without a voltage drop. This condition is called the superconducting or S state. If the current varies slowly or if the variations are small, the phase velocity also will be small, but nonzero. Eqn. 1.8 shows that a small voltage will be induced by the time varying phase. It is appropriate to generalize the S state to include this case, and model the induced voltage with an equivalent nonlinear reactance.

For small phase perturbations ($\tilde{\phi}$) around a bias point (ϕ), Eqn. 1.1 can be expanded in a Taylor series yielding an incremental supercurrent proportional to the incremental phase:

$$\tilde{I}_S = (I_c \cos\phi)\tilde{\phi} \tag{1.11}$$

Using Eqn. 1.6, one finds that the incremental voltage across the junction is proportional to the time derivative of the incremental current:

$$\tilde{V} = L_J(\phi)\frac{d\tilde{I}_S}{dt} \tag{1.12}$$

The nonlinear coefficient, $L_J(\phi)$, is the Josephson inductance:

$$L_J \equiv \frac{L_c}{\cos\phi} \underset{|I|<I_c}{=} \frac{L_c}{\sqrt{1-(I/I_c)^2}} \tag{1.13}$$

where the junction's characteristic inductance, L_c, is given by:

$$L_c \equiv \frac{\Phi_o}{2\pi I_c} \tag{1.14}$$

1.1.4 - Normal Current and the R State

A Josephson junction's supercurrent results from Cooper pairs tunneling across the dielectric barrier. If the voltage across the junction exceeds the gap voltage, V_g, a normal (or quasiparticle) current process becomes energetically favorable. The normal current, I_N, consists of Cooper pairs which split and tunnel across the barrier as normal, unpaired electrons. The gap voltage is related to the energy gaps in the superconducting electrodes by:

$$V_g = \frac{\Delta_1 + \Delta_2}{e} \tag{1.15}$$

where Δ_1 and Δ_2 are the energy gaps in the electrodes. The gap voltage is about 3 mV for the niobium superconductors from which Josephson junctions are commonly fabricated. The normal current is nearly ohmic for $|V| > V_g$, and is characterized by a normal resistance, R_N, or normal conductance, G_N:

$$I_N = \frac{V}{R_N} = G_N V \tag{1.16}$$

The product of the critical current and the normal resistance defines the characteristic voltage of the junction:

$$V_c \equiv I_c R_N \tag{1.17}$$

The characteristic voltage as a function of the gap voltage can be expressed in closed form using the classical Bardeen, Cooper, and Schrieffer (BCS) theory of superconductivity. For electrodes having similar energy gaps, this relationship is given by [1]:

$$V_c(T) = \frac{\pi}{2}\frac{\Delta(T)}{e}\tanh\frac{\Delta(T)}{2k_B T} = \frac{\pi}{4}V_g(T)\tanh\frac{\Delta(T)}{2k_B T}, \quad T < T_c \tag{1.18}$$

where T is the absolute temperature, T_c is the transition temperature of the superconductor, $k_B \approx 1.381 \text{ x } 10^{-23}$ J/s is Boltzmann's constant, and $\Delta(T)$ is the temperature-dependent energy gap. The BCS theory also yields expressions for the temperature dependence of the energy gap. In the vicinity of T_c, the approximate temperature dependence of the gap is given by [1]:

$$\Delta(T) \approx 3.2 k_B T_c \sqrt{1 - T/T_c} \tag{1.19}$$

The temperature dependence of the critical current follows from Eqn. 1.17 and Eqn. 1.18:

$$I_c(T) = G_N \frac{\pi}{2}\frac{\Delta(T)}{e}\tanh\frac{\Delta(T)}{2k_B T} = G_N \frac{\pi}{4}V_g(T)\tanh\frac{\Delta(T)}{2k_B T}, \quad T < T_c \tag{1.20}$$

The characteristic voltage, critical current, and energy gap vanish at the transition temperature. However, below about half the transition temperature, the energy gap is only weakly dependent on temperature and can be approximated by:

$$\Delta(T) \approx \Delta(0) \approx 1.76 k_B T_c, \quad T < T_c / 2 \tag{1.21}$$

where $\Delta(0)$ is the energy gap at absolute zero. Then, the characteristic voltage is approximately related to the gap voltage by:

$$V_c \approx \frac{\pi}{4} V_g \tag{1.22}$$

On the basis of Eqn. 1.8, the characteristic frequency, ω_c, and its associated characteristic time constant, τ_c, are defined in terms of V_c:

$$\omega_c \equiv 2\pi f_c = \tau_c^{-1} = \frac{2\pi V_c}{\Phi_o} = \frac{R_N}{L_c} \tag{1.23}$$

Using the typical values of V_c, one obtains: $\omega_c \sim 1$ THz and $\tau_c \sim 0.1$ ps.

Inspection of Eqn. 1.1 reveals that current in excess of the critical current , $|I| > I_c$, cannot consist entirely of a supercurrent, I_S, so the normal current must be nonzero. However, since the normal current is ohmic, a nonzero current implies a nonzero voltage. Therefore, the $|I| > I_c$ state is deemed the resistive or R state. The R state is also referred to as the normal state. The R state is invariably accompanied by Josephson oscillations with a frequency given by Eqn. 1.8.

1.1.5 - The Capacitance and the Capacitance Parameter

The components of the Josephson junction current presented so far, I_S and I_N, are intrinsic to the device. In practice, the small dielectric thickness necessary for tunneling

in a Josephson junction leads to a high geometric shunt capacitance, especially for planar tunnel junctions. The value of this capacitance is given by the well-known expression:

$$C = \frac{\varepsilon A}{d} \tag{1.24}$$

where A and d are the area and thickness of the junction, respectively, and ε is the dielectric permittivity. The capacitance contributes a displacement current to the total junction current:

$$I_D = C\frac{dV}{dt} \tag{1.25}$$

Combined with L_J and R_N, the capacitance forms a nonlinear RLC equivalent circuit model of the Josephson junction. To describe this circuit, it is convenient to introduce the junction RC time constant and the plasma frequency:

$$\tau_N \equiv \omega_N^{-1} = R_N C \tag{1.26}$$

$$\omega_p \equiv \sqrt{\frac{1}{L_c C}} = \sqrt{\frac{2\pi I_c}{\Phi_o C}} \tag{1.27}$$

Using the Josephson voltage-frequency relationship, Eqn. 1.8, one can also define the plasma voltage:

$$V_p \equiv \frac{\Phi_o}{2\pi}\omega_p \tag{1.28}$$

A Josephson junction is a highly nonlinear device whose qualitative behavior depends strongly on whether it is dominated by its RC time constant, τ_N, or its L/R time constant, τ_c. The dimensionless Stewart-McCumber capacitance parameter is often used to characterize this dependence. It is given by:

$$\beta_c = \frac{\omega_c}{\omega_N} = \omega_c \tau_N = \left(\frac{\omega_c}{\omega_p}\right)^2 = \left(\frac{R_N}{\sqrt{L_c / C}}\right)^2 = \frac{2\pi I_c R_N{}^2 C}{\Phi_o} \tag{1.29}$$

Relatively high-capacitance Josephson junctions with $\beta_c >> 1$ are deemed underdamped. Low-capacitance junctions with $\beta_c << 1$ are described as overdamped. The crossover between the two regimes occurs at $\beta_c \sim 1$.

The McCumber capacitance parameter, β_c, is a function of device geometry and fundamental constants. However, the characteristics of a junction can be tailored by adjusting the value of an external shunt resistor. Another capacitance parameter, β_{ce}, can be defined for this resistively shunted junction:

$$\beta_{ce} = \left(\frac{\omega_{ce}}{\omega_p}\right)^2 = \left(\frac{R_{Ne}}{\sqrt{L_c / C}}\right)^2 = \frac{2\pi I_c R_{Ne}{}^2 C}{\Phi_o} = \beta_c \left(\frac{R_{Ne}}{R_N}\right)^2 \tag{1.30}$$

where the extrinsic normal resistance is given by:

$$R_{Ne} = G_{Ne}{}^{-1} = \frac{1}{R_N{}^{-1} + R_{sh}{}^{-1}} \tag{1.31}$$

where R_{sh} is the external shunt resistance, G_{Ne} is the total shunt conductance, and ω_{ce} is the extrinsic characteristic frequency, which is given by:

$$\omega_{ce} = \frac{2\pi V_{ce}}{\Phi_o} = \frac{R_{Ne}}{L_c} = \omega_c \frac{R_{Ne}}{R_N} \tag{1.32}$$

where the extrinsic characteristic voltage is given by:

$$V_{ce} = I_c R_{Ne} = V_c \frac{R_{Ne}}{R_N} \tag{1.33}$$

An extrinsic RC time constant can be defined similarly:

$$\tau_{Ne} \equiv \omega_{Ne}^{-1} = R_{Ne}C \tag{1.34}$$

1.1.6 - The RSJN Model

The basic current equation for the Josephson junction contains the three current components introduced in the preceding sections:

$$I_J = I_S + I_N + I_D = I_c \sin\phi + G_N V + C\frac{dV}{dt} \tag{1.35}$$

A simple substitution gives the basic current equation for a shunted junction:

$$I_J = I_S + I_N + I_D = I_c \sin\phi + G_{N,e} V + C\frac{dV}{dt} \tag{1.36}$$

In conjunction with Eqn. 1.6, this equation constitutes the resistively shunted junction (RSJ) model of the Josephson junction. The corresponding equivalent circuit is shown in Fig. 1.1.

The nonlinear resistively shunted junction (RSJN) model compensates for the principal disparity between the basic RSJ model and actual Josephson junctions, the measured voltage dependence of the junction conductance. In the latter case, the incremental conductance below the gap voltage is usually much lower than the normal

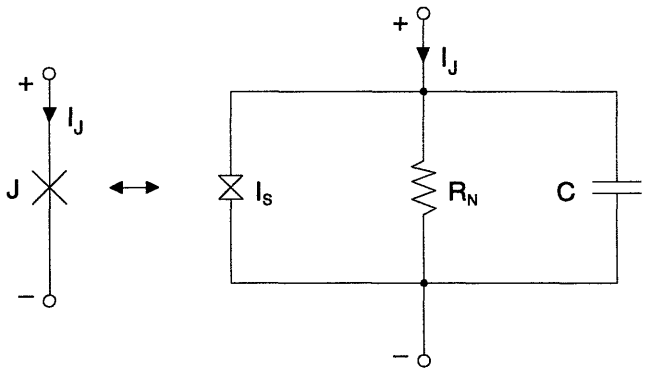

Figure 1.1 - Josephson junction symbol and RSJ circuit model.

conductance above the gap, especially when $\beta_c >> 1$. The RSJN model substitutes a voltage-dependent conductance, $G_N(V)$, for the normal conductance of the RSJ model. A simple piecewise-linear model of $G_N(V)$ facilitates hand analysis and is conducive to computer simulations:

$$G_N(V) = R_N^{-1}(V) = \begin{cases} G_N, & |V| > V_g \\ G_o, & |V| < V_g \end{cases} \tag{1.37}$$

This model introduces one additional parameter, the subgap or leakage conductance, $G_o = R_o^{-1}$. The definition of the subgap RC time constant is immediate:

$$\tau_o \equiv \omega_o^{-1} = R_o C \tag{1.38}$$

A simple substitution covers the extrinsic (or externally shunted) case where the RSJN junction is shunted by an external resistor:

$$G_{Ne}(V) = R_{Ne}^{-1}(V) = \begin{cases} G_{Ne}, & |V| > V_g \\ G_{oe}, & |V| < V_g \end{cases} \tag{1.39}$$

where the extrinsic leakage conductance is given by:

$$G_{oe} = R_{oe}^{-1} = R_o^{-1} + R_{sh}^{-1} \tag{1.40}$$

from which the definition of the extrinsic subgap RC time constant follows:

$$\tau_{oe} \equiv \omega_{oe}^{-1} = R_{oe} C \tag{1.41}$$

It is appropriate to introduce a modified capacitance parameter for the subgap regime of the extrinsic nonlinear shunted junction:

$$\beta_{oe} = \left(\frac{R_{oe}}{\sqrt{L_c / C}} \right)^2 = \frac{2\pi I_c R_{oe}^{\ 2} C}{\Phi_o} = \beta_c \left(\frac{R_{oe}}{R_N} \right)^2, \quad |V| < V_g \tag{1.42}$$

The notation, $\beta_{oe} = \beta_o$, is suitable for the special case of infinite R_{sh}.

1.1.7 - Junction I-V Curves

The dc *I-V* curve of the Josephson junction can be obtained if the basic equation of the Josephson junction, Eqn. 1.35, is solved for the time-average voltage. The time-average voltage is obtained using a low pass filter that suppresses the Josephson oscillations. Thus the *I-V* curve is only suitable for describing phenomena that occur at frequencies well below the Josephson oscillation frequency (i.e., for $\omega << \omega_J$). The numerical solutions to the basic equation agree well with experimental *I-V* curves. There are two limiting cases. In the first case, relatively high-capacitance Josephson junctions with $\beta_c >> 1$ are deemed underdamped and have hysteretic *I-V* curves.

Fig. 1.2 shows the *I-V* curve of a typical underdamped junction as predicted by the RSJN model without an external shunt resistor. As the current through the junction is increased from zero, the junction remains in the zero-voltage S state until the critical current is exceeded. Thereafter, the junction switches into the R state and the incremental resistance approaches R_N asymptotically. However, when the current is subsequently reduced, the junction remains in the R state until the current has been reduced well below I_c and close to zero.

Low-capacitance junctions with $\beta_c << 1$ are described as overdamped and have non-hysteretic *I-V* curves. Fig. 1.3 shows the *I-V* curves of such a junction as predicted by the RSJN model (without an external shunt resistor) and the RSJ model. Qualitatively, both the curves are similar. Once again, as the drive current is increased from zero, the junction remains in the S state until the critical current is surpassed, beyond which the junction switches into the R state and the incremental resistance approaches R_N asymptotically. In contrast to the underdamped junction, the overdamped junction returns

to the S state when the current falls below I_c and the *I-V* curve is retraced as the current returns to zero.

In the limit of high external shunt conductance, the *I-V* curve predicted by the RSJN model approaches that given by the RSJ model. The latter model is particularly useful for describing underdamped junctions since the *I-V* curve in the R state can be expressed in closed form for $\beta_c = 0$. For externally shunted junctions, one obtains [3]:

$$V = V_c \text{sign}(I)\sqrt{(I/I_c)^2 - 1} = R_{Ne}\text{sign}(I)\sqrt{I^2 - I_c^2}, \quad |I| > I_c \tag{1.43}$$

where the sign() function has unit magnitude and returns the sign of its argument.

This equation allows the calculation of a first-order correction to the piecewise-

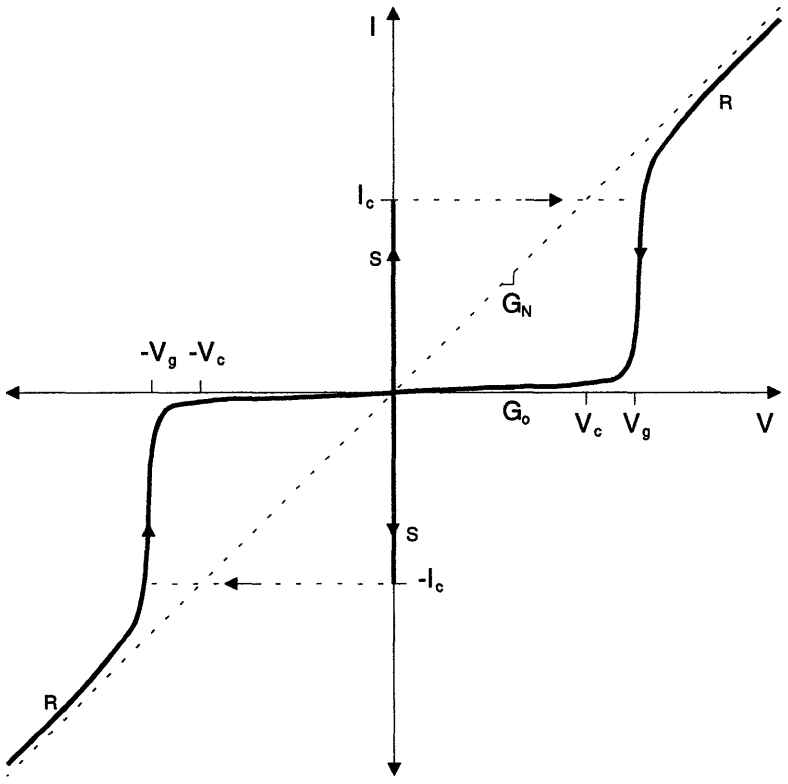

Figure 1.2 - Typical dc *I-V* curve of an underdamped ($\beta_c >> 1$) Josephson junction. The curve is based upon the RSJN model and is hysteretic.

linear model of the extrinsic incremental resistance in the R state, yielding:

$$r_{oe}(I) = \frac{dV(I)}{dI} = \frac{R_{Ne}}{\sqrt{1-(I_c/I)^2}}, \quad |I| > I_c \tag{1.44}$$

This expression is even-symmetric and approaches R_{Ne} for large $|I|$, in agreement with the actual *I-V* curve. For a junction biased at a fixed current, I_B, the incremental resistance is given by the equivalent expression:

$$r_{oe}(I_B) = R_{Ne}\frac{1+\delta_I}{\sqrt{(1+\delta_I)^2-1}} \tag{1.45}$$

where the fractional current overdrive current, δ_I, is given by:

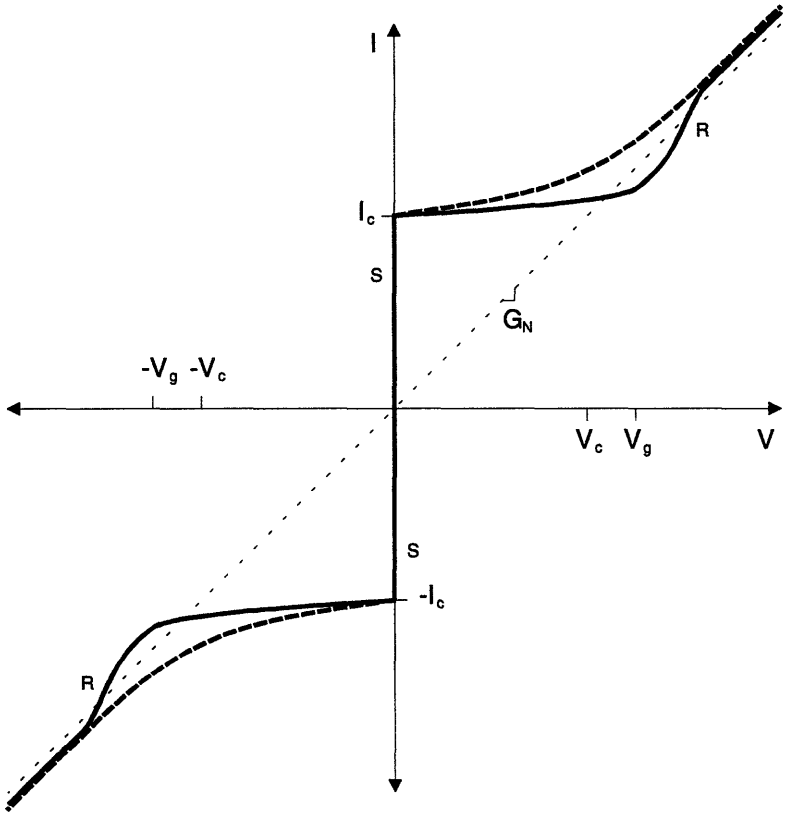

Figure 1.3 - Typical dc *I-V* curves of an overdamped ($\beta_c << 1$) Josephson junction. The solid curve is based upon the RSJN model; the dashed curve is based upon the RSJ model. Both curves are single-valued.

$$\delta_I = \left|\frac{I_B}{I_c}\right| - 1 \tag{1.46}$$

While this expression for r_{oe} is only strictly valid for the RSJ model at $\beta_c = 0$, it gives a fair qualitative description of the current dependence of the R-state incremental resistance of an overdamped RSJN junction, as can be seen in Fig. 1.3.

The hysteresis of a Josephson junction's *I-V* curve has a direct impact on the operation of the T/H circuit, which contains junction switches that must make R→S transitions while carrying a nonzero current. Fig. 1.4 shows the intermediate case, β_c on the order of unity. The junction's *I-V* curve is hysteretic, but the junction returns to the S state before the current reaches zero. The magnitude of current below which the junction

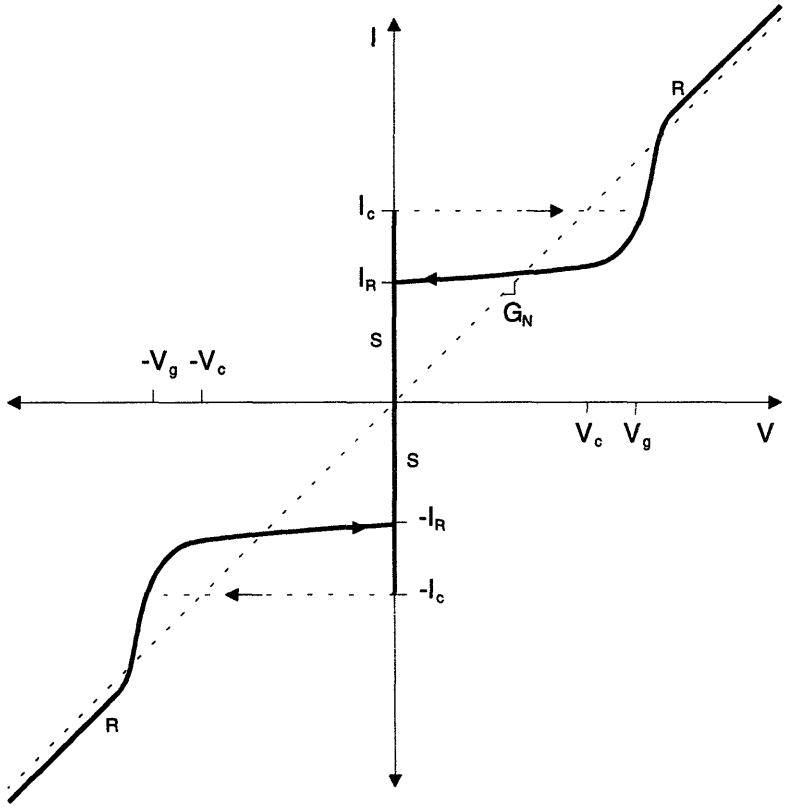

Figure 1.4 - Typical dc *I-V* curve of an moderately damped ($\beta_c \sim 1$) Josephson junction. The curve is based upon the RSJN model; it is not single-valued, but it exhibits lower hysteresis than the underdamped case.

returns to the S state is called the return current, I_R. In the shunted RSJN model, the ratio of the junction's return current to its critical current is given by [3]:

$$r(\beta_{oe}) \equiv \frac{I_R}{I_c} = \frac{4}{\pi\sqrt{\beta_{oe}}} = \frac{4}{\pi R_{oe}}\sqrt{\frac{\Phi_o}{2\pi I_c C}}, \quad \beta_{oe} >> 1 \tag{1.47}$$

where the last equality follows from Eqn. 1.42. Note that I_R is inversely proportional to R_{oe}. Typical planar tunnel junctions have a large capacitance and are highly hysteretic. In order to obtain a substantial I_R, it is necessary to resistively shunt the junction, but the junction does not need to be made fully non-hysteretic.

1.2 - Track and Hold Circuits

In its simplest form, a track and hold circuit (T/H) consists of an energy storage element and a switch. Ideally, the output of the T/H equals its input when the switch is in its track mode, but is held constant once the T/H is switched into its hold mode, regardless of subsequent changes in the input. Typical deviations from ideality include a nonzero dc offset between the input and output, a linear gain error, a nonlinear transfer function, finite bandwidth, nonzero acquisition time, and output droop (finite hold time). Semiconductor T/H's generally use a capacitor for energy storage because transistor and diode switches with very high off-mode impedances and low leakage provide a large ratio of hold time to sample time [4], [5]. Since superconductive switches generally have very low off-state resistances, comparable to the normal resistance of a Josephson junction [1], [2], semiconductor T/H topologies are not directly applicable to a superconductive implementation. However, in a superconductive technology, the dual of a series R-C T/H, a parallel R-L T/H, can be realized by using inductors made from wires having zero dc resistance and Josephson junction switches with zero on-state resistance. This combination results in an infinite hold time to sample time ratio. Furthermore, the

extremely high switching speeds of Josephson junctions can result in switching times on the order of 10 ps [3], [6].

The track and hold has many applications in data acquisition and data conversion systems. A single T/H can serve as an analog memory cell, or multiple T/H cells can be arranged in parallel to form a single-shot transient recorder. One is often used to de-glitch a high-speed D/A converter. A high-speed T/H can be especially useful as a front end to an analog-to-digital (A/D) converter because it defines a unique sampling instant for the entire A/D each clock cycle and greatly reduces the slew rate of the signal seen by the A/D.

Many semiconductor A/D architectures are prone to errors due to rapidly changing input signals, either because the conversion process takes place over a relatively long time (e.g., successive approximation A/D) or because of clock and signal timing skew between physically separate parts of the converter (e.g., parallel FLASH A/D). Despite their high speed, many superconductive A/D architectures are not immune to these problems. Like their semiconductor counterparts, superconductive parallel FLASH A/D converters [7] – [11], consist of order 2^N nominally identical comparators that are driven by the same input signal and clock. Delay mismatch due to the large area of a FLASH A/D, in addition to clock skew due to nonzero clock rise time and variable clock thresholds resulting from process variations, conspire to yield significant dispersion of effective sampling edges across the many comparators. The high-speed linearity of an A/D is limited by an amplitude error that is a direct result of this timing uncertainty and a nonzero slew rate [12]. The worst-case amplitude error occurs for a high-frequency, full-scale sine wave input at its zero-crossing. For small time errors, the amplitude error is given by:

$$\varepsilon_{LSB} \approx 2^N \pi \cdot f \Delta t \tag{1.48}$$

where ε_{LSB} is the magnitude of the error in least significant bits (LSB's), N is the bit-resolution of the A/D, f is the input frequency, and Δt is the total time error. In addition to this error, a parallel FLASH converter without correction hardware may suffer as much as a 1/2 full-scale error if the thresholds at the midpoint of its input range cross over due to timing skew [5], [13]. A T/H minimizes this error contribution by reducing Δt to the smallest possible value, limited by the phase stability of the external time base.

Superconducting comparators may also suffer from distorted switching characteristics at high slew rates, resulting in dynamic thresholds that differ substantially from static thresholds [8]. Also adversely affected by fast input slew rates are high-speed superconductive wiggle (bit-parallel or periodic FLASH) A/D converters [14] – [17]. In this architecture, the input signal is distributed by a passive binary dividing ladder and presented to N comparators with periodic transfer characteristics. This type of A/D is subject to less timing skew due to its significantly lower area [18]. However, at high input slew rates, the periodic threshold curves of the comparators (especially the LSB) are subject to distortion that degrades the linearity of the A/D [12], [19], [20]. A T/H addresses this source of error by providing a relatively time-invariant input signal to the A/D during its conversion interval.

It is not always best to precede an A/D with a T/H. The additional circuit area and power that a T/H consumes make it less desirable in low-speed applications. Also, the inclusion of a T/H complicates the system timing and reduces the fraction of a clock period available for A/D conversion since at least the front end of the A/D converter must latch while the T/H is still in hold mode. However, since superconducting A/Ds typically have conversion times commensurate with the high switching speeds of Josephson junctions [10], [12], the tradeoff of drastically reduced slew rate for reduced conversion time that a T/H offers is generally quite advantageous.

A number of high-speed semiconductor T/H's and sample and holds have been reported in the literature [21], [4], [22]. Typically, these GHz-class GaAs MESFET and silicon bipolar integrated circuits have been part of high-speed (Gs/sec), moderate-resolution (6-bit to 8-bit) A/D conversion systems. Surprisingly, there has been little development in superconducting T/H's. Early work on superconducting analog sampling circuits focused on the development of circuits suitable for sampling fast, repetitive waveforms. The first such sampler was proposed by Zappe in 1975 [23]. Fig. 1.5 shows a simple circuit of this type and typical current waveforms. The sampler is essentially a single Josephson junction fed by the sum of two currents — an unknown input signal (I_{sig}) and an adjustable bias (I_{bias}). The single-junction comparator switches when the sum of the currents exceeds the critical current of the junction (I_c). By slowly sweeping the bias current and observing the evolution of the switching point, the unknown amplitude of the input can be determined at each switching time. This type of circuit achieves time resolution on the order of 10 ps [24] due to the rapid switching response of the junction, but it suffers from the jitter of room-temperature electronics and the inability to sample the falling edge of a waveform.

In order to overcome these shortcomings, subsequent designs augmented the bias with a fast pulse generated by a Josephson pulser [25], [26], [27]. Fig. 1.6 shows the improved circuit and its mode of operation. In this scheme, the pulse (I_p) is swept across

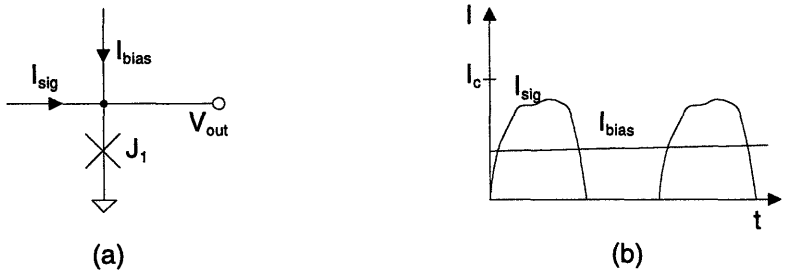

Figure 1.5 - Josephson analog sampling circuit based on a single-junction current comparator. (a) Circuit schematic. (b) Typical waveforms.

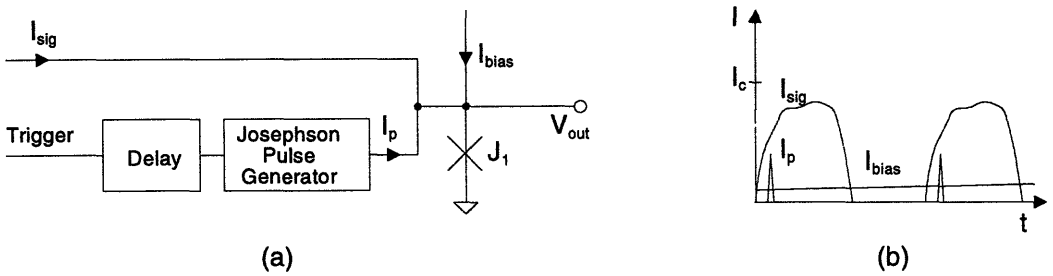

Figure 1.6 - Improved Josephson analog sampler incorporating a Josephson pulse generator. (a) Simplified circuit schematic. (b) Typical waveforms. In some implementations, the junction, J_1, is replaced by a more complicated comparator circuit.

the repetitive input by a varying external delay. At each value of delay the amplitude of the signal (I_{sig}) can be determined by adjusting the bias (I_{bias}) until the sum of the input, bias, and pulse equals the critical current of the junction (I_c). In the presence of measurement noise the latter condition is best determined by choosing the bias so that the average output voltage of the junction corresponds to the output voltage expected from a 50% switching probability. A sampler of this type was shown to have a 6 ps intrinsic time resolution and exhibited 10 ps resolution on a complex, non-monotonic periodic waveform [26].

While these superconducting samplers have displayed impressive speed, they are severely limited by their need for a repetitive input signal. These samplers are not suitable for use with A/D converters since they do not offer a well-defined output signal as does a true sample and hold circuit. Another class of Josephson sampling circuits, first suggested by Davidson in 1980 [28], [29] is capable of producing the necessary time-invariant output sample from a rapidly changing non-repetitive input. The circuit, shown in Fig. 1.7a, contains a switch consisting of two identical Josephson junctions (J_1, J_2) with clock lines fed through identical resistors (R_1, R_2), a common ground point between the junctions, and two transformers ($L_{1a,b}$, $L_{2a,b}$) connected in series across the junctions. The input signal is magnetically coupled into the circuit through the primary of the first

transformer, and the output signal is available via the secondary of the second transformer.

Fig. 1.7b shows the operation of the circuit for an input signal having a bandwidth much less than that of the sampler. While the common-mode clock signal is applied (I_{clk}), the junctions are held in their normal state, and the differential current induced in L_{1b} is attenuated by the L-R high-pass filter. The magnitude of I_{clk} is significantly larger than the sum of the critical currents so that both junctions are sure to be in the R state. If the input signal is in the rejection band of this filter, nearly zero current will circulate in the secondary loop. Otherwise, the error may be significant. On the falling edge of the clock, the junctions return to their superconducting state, retaining approximately the same small secondary current (within the constraints of fluxoid quantization in the superconducting loop) that represents the sampling nonlinearity error. At subsequent times, the change in the circulating current in the loop will be proportional to the change in input current. The principal limitation of this architecture is that the output is only available while the input signal is forced to zero.

A T/H that is a variant of the Davidson sampler has also been proposed [8]. The

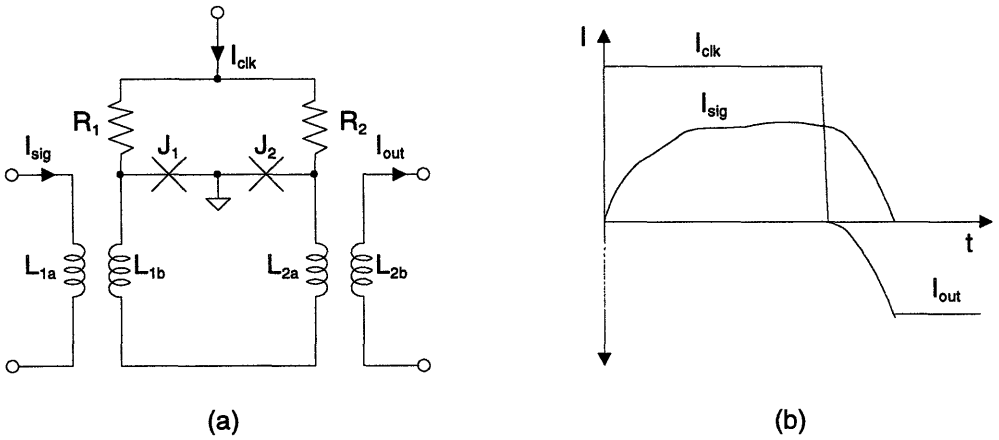

Figure 1.7 - Davidson sampling circuit for sampling non-repetitive signals. (a) Circuit schematic. (b) Typical waveforms. The transformers are ideal and have unity current gain in this example. The circuit is balanced ($I_{c1} = I_{c1}$, $R_1 = R_2$), and the loop inductance is dominated by the secondary of the input transformer ($L_{1b} >> L_{2a}$).

circuit, which is depicted in Fig. 1.8a, is implemented with a hold inductor in parallel with two series Josephson junctions (J_1, J_2) that are switched by a control current injected between them (I_{clk}). Fig. 1.8b illustrates the operation of the circuit. In track mode, the junctions are driven into their resistive state by the clock current, forcing the input current to flow in the superconducting inductor. In the hold mode, the junctions are superconducting, and changes in the input flow through the junctions. However, the circuit is susceptible to clock feedthrough since both the signal and the clock are applied in a single-ended fashion with respect to ground.

A true superconducting track and hold circuit with 1.2 GHz bandwidth and 34 dB dynamic range has been demonstrated [30]. Fig. 1.9a shows the essence of the circuit, which uses magnetic suppression of the critical current of a large sine-shaped junction (J_1) to realize a current switch that modulates the flow of current into a hold inductor (L_2) in parallel with the switch. Fig. 1.9b shows a typical threshold characteristic, $I_{c1}(I_{clk})$, for a sine-shaped junction; the non-negligible critical current at the first minimum is evident. Unfortunately, the resolution of the device depends on the critical current at the null, which invariably differs from zero and is dependent on the detailed shape of the junction. Furthermore, the large dimensions needed to guarantee the accurate geometry of the shaped junction result in high capacitance and reduced speed. Finally, the shaped-

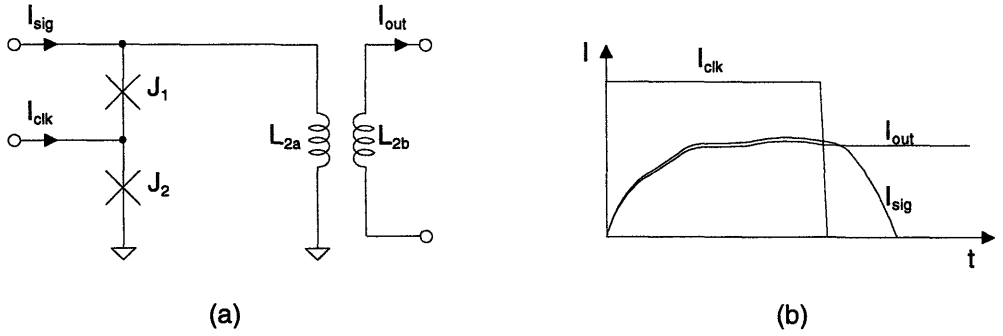

Figure 1.8 - Single-ended Josephson track and hold. (a) Circuit schematic. (b) Typical waveforms. The transformer is ideal and has unity current gain in this example. Also, clock feedthrough has been neglected.

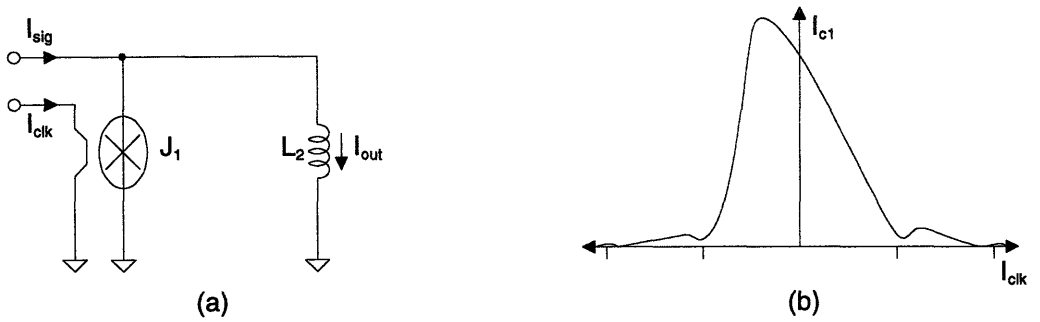

Figure 1.9 - Josephson track and hold using magnetic suppression of the junction critical current. (a) Simplified circuit schematic. (b) Sine-shaped junction threshold curve.

junction T/H requires prohibitively large control currents to drive the junction into its off state. The next chapter describes the proposed design and fabrication of a novel Josephson T/H architecture whose performance is superior in several ways to the superconducting T/H's demonstrated to date.

2 - T/H Design & Simulation

2.1 - T/H Architecture

It is relatively easy to design a nearly ideal superconducting hold inductor with zero dc resistance and low capacitance. It is more difficult to design a superconducting switch that has wide tracking bandwidth, good hold-mode isolation, and short switching time. Fig. 2.1a shows the hold state of an ideal voltage T switch, consisting of two series (inline) switches (S_{S1}, S_{S2}) and a parallel (shunt) switch (S_{P1}). The high ON admittance of switch S_{P1} shunts to ground most of the current that passes through the finite OFF impedance of switch S_{S1} and reduces the impact on the voltage held on the capacitor. The proposed Josephson T/H bridge is essentially the current dual of the voltage T switch. The ideal π gate shown in Fig. 2.1b consists of two parallel switches (S_{P1}, S_{P2}) and a series switch (S_{Sa}). The high OFF impedance of switch S_{Sa} minimizes the change in the held current by reducing the fraction of the total voltage induced by the input across the finite OFF admittance of switch S_{P1} which appears across switch S_{P2} and the inductor.

In superconducting technology, Josephson junctions (JJ's) are used as switching

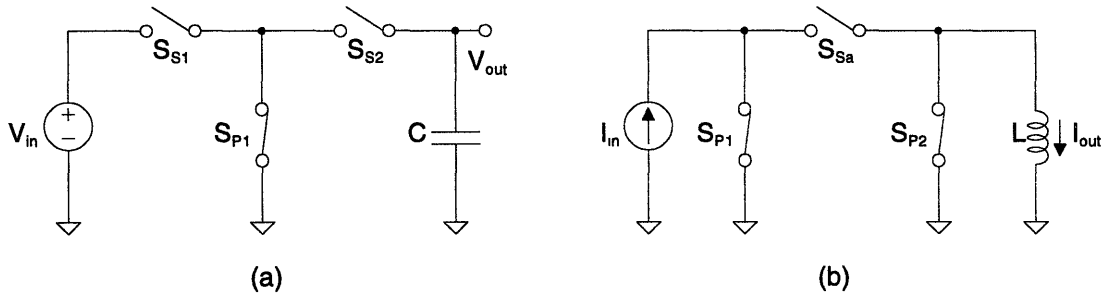

Figure 2.1 - (a) Ideal voltage T/H in hold mode consisting of a T switch and a capacitor. (b) Ideal current T/H in hold mode consisting of a π switch and an inductor. In track mode all open switches are closed and all closed switched are opened.

elements in place of three-terminal active devices such as transistors. As mentioned in the previous chapter, the critical current of a JJ can be suppressed by an external magnetic field, forcing the device into its resistive state for all but a very small range of input currents. The impedance of a JJ can also be controlled by a directly injected current, somewhat as a voltage is used to modulate the impedance of a semiconductor diode switch. A particularly useful feature of the Davidson sampler described in the previous chapter is its use of a common-mode current to control the state of two parallel junctions carrying a differential signal current. In a symmetric JJ switch, this technique allows the switch to be controlled by directly injected currents without affecting the current in the hold inductor. A symmetric Josephson current bridge suitable for this type of mode control can be derived from the π gate shown in Fig. 2.1b by first adding a second series switch (S_{Sb}) across the ground terminals of the two shunt switches (S_{P1}, S_{P2}) and closing the left and right loops. The resulting ideal circuit is shown in Fig. 2.2.

A Josephson junction implementation of the ideal double π gate T/H is depicted in Fig. 2.3. Each of the four switches from Fig. 2.2 is realized with a pair of JJ's in series: the two parallel switches (S_{P1}, S_{P2}) are implemented with the J_{P1a}, J_{P1b} pair and the J_{P2a}, J_{P2b} pair, respectively, and the two series switches (S_{Sa}, S_{Sb}) are implemented with the J_{S1a}, J_{S2a} and J_{S1b}, J_{S2b} pairs.

By grouping the junctions and bias current sources into four nominally identical switch cells (*1a*, *2a*, *1b*, and *2b*), Fig. 2.4 emphasizes the regularity of the circuit, which is

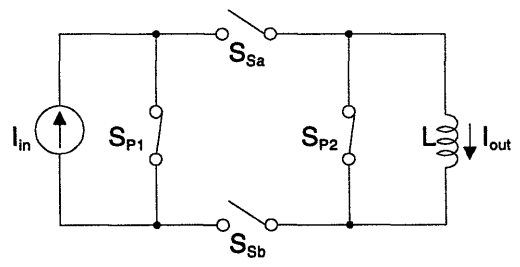

Figure 2.2 - Ideal current T/H bridge in hold mode consisting of a double π switch and an inductor.

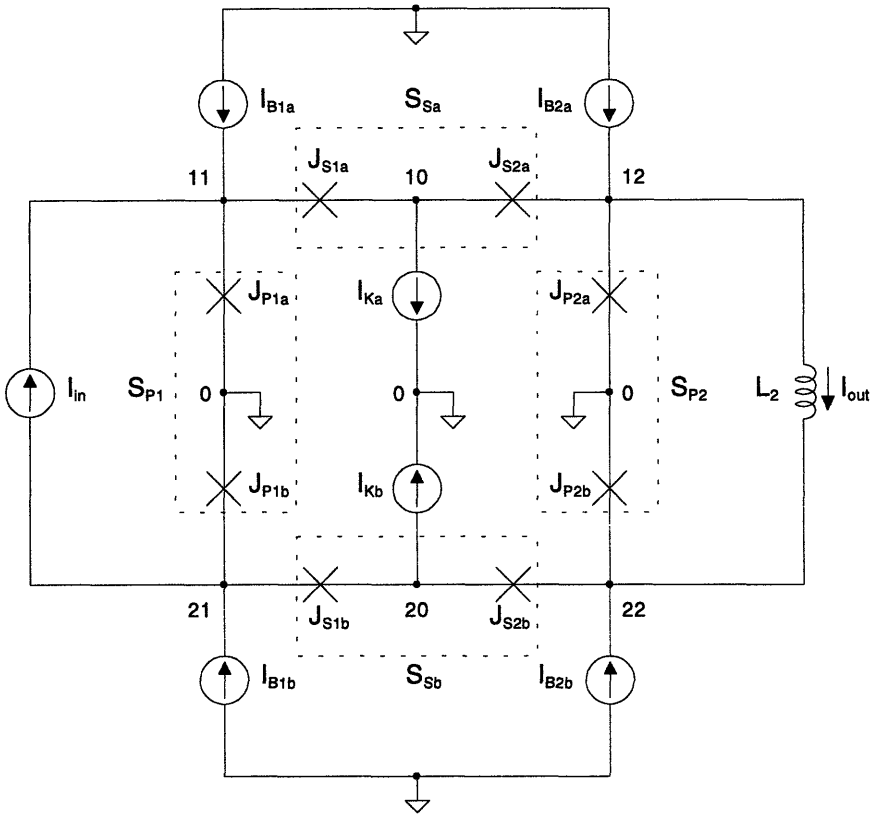

Figure 2.3 - Complete Josephson junction bridge T/H using a symmetric double π switch. The junctions are grouped to show the implementation of the two series and two parallel switches.

symmetric both about the horizontal plane defined the three central ground connections and the vertical plane defined by the clock current sources. The four corners of the bridge are formed by these basic cells, each of which consists of a series junction, a parallel junction, and a dc bias current. The four bias currents are equal (i.e., $I_{B1a} = I_{B2a} = I_{B1b} = I_{B2b} = I_B$). The top (or *a*) half of the bridge is controlled by clock current source I_{Ka}, and the bottom (or *b*) half of the bridge is controlled by clock current source I_{Kb}. The two clock signals are synchronized, unipolar, zero-offset square waves having identical amplitudes equal to twice that of the bias current ($\max(I_{Ka}) = \max(I_{Kb}) = I_K = 2I_B$).

In track mode, I_{Ka} and I_{Kb} are zero. If the circuit is balanced, the common-mode bias currents flow through their respective parallel junctions to ground (e.g., I_{B1a} flows

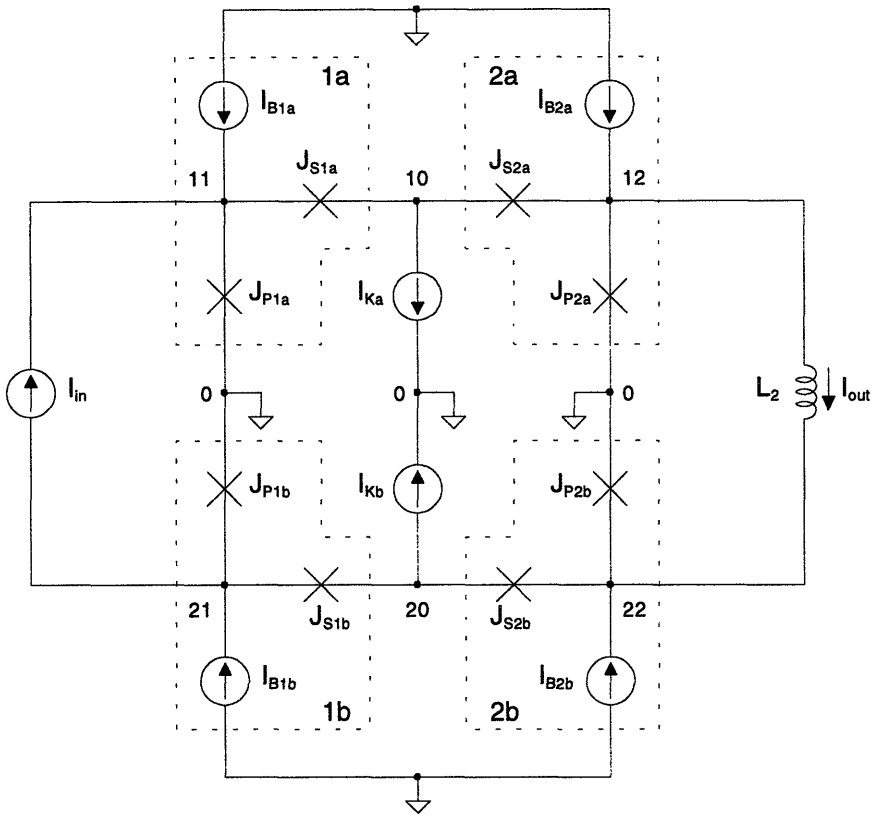

Figure 2.4 - Complete Josephson junction bridge T/H showing the four symmetric cells.

through J_{P1a} to ground). The amplitude of the bias current is sufficient to keep the parallel junctions in the normal state ($I_B \geq I_{c,P}$). Since the series junctions carry no bias current, they remain in the superconducting state. Thus, at sufficiently low amplitudes and frequencies, the differential input current flows through the two series switches and the hold inductor, making I_{out} equal to I_{in}.

In hold mode, the clock currents are raised, steering the bias currents from the parallel junctions to the series junctions. The magnitude of the clock current is sufficient to drive the series junctions into the normal state ($I_K \geq 2I_{c,S}$). Deprived of their control currents, the parallel junctions fall back into the superconducting state, allowing the input current to flow in the input loop formed by the input current source and S_{P1} (J_{P1a}, J_{P1b}), and the output current to circulate in the hold loop formed by the hold inductor and S_{P2}

(J_{P2a}, J_{P2b}). The main design issues and the detailed conditions under which the preceding simplified description is accurate are discussed in the following sections.

2.2 - Low-Speed Design Issues

2.2.1 - Input Signal Range

Although a variety of factors and circuit parameters impact the performance of the T/H bridge, one necessary condition must be satisfied for the circuit to operate. When the T/H switches from track mode to hold mode, it is imperative that the two parallel junctions that comprise the hold loop (J_{P2a}, J_{P2b}) enter the S state before the series junctions (J_{S1a}, J_{S2a}, J_{S1a}, J_{S2b}) enter the R state. If this condition is not met, the bridge will be entirely resistive for a nonzero interval of time, causing the circulating current to be partially quenched and introducing a sampling error. This problem will be mitigated to some extent by a fast clock rise time, but a good T/H design should not have systematic clock-edge-rate-dependent anomalies. Since the bridge is symmetric about the three central ground terminals, it is sufficient to analyze the failure mode of only the top half circuit.

Fig. 2.5 is a subcircuit of Fig. 2.4 showing only cell *2a* and other circuit elements relevant to the following first-order analysis. Due to the symmetry of the circuit, the total top clock current (I_{Ka}) divides equally between cell *1a* and cell *2a*; the half controlling cell *2a* is shown as I_K. For the following analysis, all of the input current is assumed to reach node 10 (i.e., none is shunted to ground in cell *1a*). Assuming that the bias currents (I_{B1a}, I_{B2a}, I_{B1b}, I_{B2b}) and clock currents (I_{Ka}, I_{Kb}) are positive, the worst case is a large negative input current. The full-scale input current, I_{FS}, is defined as the magnitude of the largest input current that the T/H can capture accurately:

$$I_{FS} \equiv \max(|I_{in}|) \tag{2.1}$$

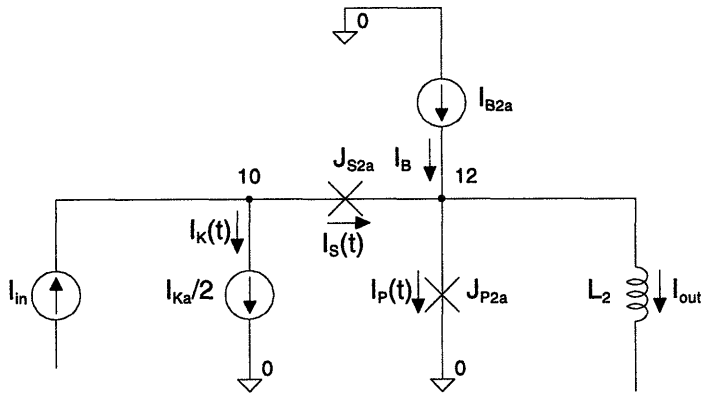

Figure 2.5 - Upper right switch cell (*2a*) of the Josephson junction bridge for analysis of the input signal range.

Since the T/H allows bipolar inputs, the full scale input range, I_{range}, is twice the full scale input current.

Conservation of current at node 12 with a negative full-scale dc input, $I_{in} = -I_{FS}$, gives:

$$I_B + I_S(t) - I_P(t) = I_{out} = -I_{FS} \tag{2.2}$$

where the subscripts have been abbreviated to generalize the equation. In the case of node 12, I_B is the bias current (I_{B2a}), $I_P(t)$ is the current through the parallel junction (J_{P2a}), $I_S(t)$ is the current through the series junction (J_{S2a}), and I_{FS} is the full-scale input current, which is assumed to be time invariant for this analysis.

At a clock edge, the clock current, $I_K(t)$, is a unipolar, monotonically increasing function of time with an amplitude equal to the bias current. It is given by:

$$I_K(t) = I_B \alpha(t) \tag{2.3}$$

where the function $\alpha(t)$ ($0 \le \alpha(t) \le 1$, all t) describes the time dependence of the clock. In track mode, $\alpha(t) = 0$; in hold mode, $\alpha(t) = 1$. Hence, the following equations describe the time evolution of the branch currents:

$$I_P(t) = I_B(1-\alpha(t)) \tag{2.4}$$

$$I_S(t) = I_{in} - I_K = -I_{FS} - \alpha(t) I_B \tag{2.5}$$

$$I_{in} = I_{out} = -I_{FS} \tag{2.6}$$

In track mode with a low-speed input, $I_K(t) = 0$, $I_P(t) = I_B$, and $I_S(t) = -I_{FS}$. When the T/H is switched from track mode to hold mode at a sampling edge, the clock current increases from zero, and the bias current is steered from the parallel junction to the series junction. Since the circuit is balanced and the clock current is a common-mode signal with respect to the inductor, the change of the clock current does not change the held current.

At the switching time t_o, $\alpha(t_o) = \alpha_o$, the magnitude of the current in the parallel junction is just low enough to allow it to enter the S state (i.e., its return current, $I_{R,P}$) while the magnitude of the current in the series junction is just below the current needed to drive it into the R state (i.e., its critical current, $I_{c,S}$):

$$I_P(t_o) = I_B(1-\alpha_o) = I_{R,P} \tag{2.7}$$

$$-I_S = I_{FS} + \alpha_o I_B = I_{c,S} \tag{2.8}$$

Solving these equations for the full-scale input current yields:

$$I_{FS} = \frac{I_{range}}{2} = I_{R,P} - (I_B - I_{c,S}) = I_{R,P} - I_{c,S}(1+\delta_{I,S}) \tag{2.9}$$

From Eqn. 2.9, the full-scale input current of the T/H is maximized by maximizing the return current of the parallel junction and minimizing the series junction overdrive, $\delta_{I,S}$.

In order to achieve the optimum performance from the T/H, a single bias current amplitude must satisfy several constraints. The magnitude of the bias current must be greater than the critical current of the parallel junction in order to switch the bridge into

track mode. If the parallel junction current overdrive, $(I_B - I_{c,P})$, is chosen to be larger than the full-scale input, the bias current will be sufficient to drive the parallel junctions into the R state despite the presence of any circulating current in these junctions. This excess current will allow the bridge to return to track mode quickly in the presence of a nonzero input signal, and accelerate the acquisition transient. In order to switch the bridge into hold mode, the bias current must also be at least as large as the critical current of the series junction. However, in this case the overdrive, $(I_B - I_{c,S})$, need not be large to guarantee correct operation of the bridge since only one series junction in each pair must switch to isolate the input (left) and output (right) halves of the bridge. This requirement is easily satisfied because the signal current will always add to the clock current in one junction of each series junction pair (J_{S1a} and J_{S2b} when $I_{out} > 0$, J_{S1b} and J_{S2a} when $I_{out} < 0$). The relaxed constraint on the series junction overdrive current is fortuitous since $(I_B - I_{c,S})$ subtracts directly from I_{range}.

In summary, the fractional overdrive currents should satisfy:

$$\delta_{I,P} \approx \frac{I_{FS}}{I_{c,P}} \sim 1 \tag{2.10}$$

and

$$\delta_{I,S} << 1 \tag{2.11}$$

These conflicting requirements can be satisfied if the critical currents of the junctions are chosen such that:

$$\frac{I_{c,S}}{I_{c,P}} = \gamma_{Ic} > 1 \tag{2.12}$$

where γ_{Ic} is the critical current ratio. Thus, the main degree of freedom in setting the full-scale input signal range is the choice of the return current of the parallel junction, $I_{R,P}$:

$$I_{FS} = \frac{I_{range}}{2} \approx I_{R,P} \tag{2.13}$$

The development in the preceding chapter shows that the return current is a parameter of the junction switch that can be modified by adjusting the value of a shunt resistor.

It is not necessary for the input parallel junctions (J_{P1a}, J_{P1b}) to enter the S state before the series junctions (J_{S1a}, J_{S2a}, J_{S1b}, J_{S2b}) enter the R state when the T/H is switched from track mode to hold mode. It is only necessary that they do fall back into the S state when the clock current has reached final value. However, in order to preserve the symmetry of the bridge and encourage the dynamic equality of clock current between the input and output halves of the bridge, it is advantageous to resistively shunt the parallel junctions on the input side in the same way as those on the hold side (J_{P2a}, J_{P2b}). The series junctions must also be resistively shunted so that they are able to make the R→S transition when the bridge is switched into the track mode, but the return current does not have to be large.

As the preceding calculations show, the range of input signals over which the T/H bridge will accurately capture a sample is principally limited by the return current of the parallel junctions. The low-frequency track-mode input range is less restricted. Since little signal current flows in the parallel junctions in track mode, the maximum full-scale input of either polarity is equal to the critical current of the series junctions. Similarly, since the series junctions isolate the input loop from the hold loop in hold mode as long as both loops are superconducting, the hold-mode input range is equal to the critical current of the input shunt junctions.

2.2.2 - Resolution

Unlike a semiconductor T/H, which stores a sample of the input as a nominally constant voltage, a superconducting T/H stores a sample of the input signal as a persistent supercurrent. In a T/H application, the advantages of the total absence of dissipation in a superconducting hold loop are offset to some extent by the quantum effects of the loop. In order to satisfy fluxoid quantization, the phase around a superconducting loop, such as the hold loop formed by J_{P2a}, J_{P2b}, and L_2, must equal an integer multiple of 2π:

$$n(2\pi) = \phi_{L2} + \phi_{P2a} + \phi_{P2b} \tag{2.14}$$

where the phase drop across the inductor is related to its current, I_{L2}, by Eqn. 1.9:

$$\phi_{L2} = \frac{2\pi\Phi_{L2}}{\Phi_o} = \frac{2\pi L_2 I_{L2}}{\Phi_o} \tag{2.15}$$

and the junction phases, ϕ_i ($i = P2a$ or $P2b$), are related to their supercurrents, $I_{S,i}$, by Eqn. 1.1:

$$\sin(\phi_i) = \frac{I_{S,i}}{I_{c,i}} \tag{2.16}$$

In hold mode, the held signal current circulates in the hold loop. Thus, all of the currents in the preceding expressions are equal. Assuming that the critical currents of the parallel junctions are equal ($I_{c,P2a} = I_{c,P2b} = I_{c,P}$), Eqn. 2.14 can be rewritten:

$$n(2\pi) = \beta_L \sin(\phi_{P2a}) + \phi_{P2a} + \phi_{P2b} \tag{2.17}$$

where β_L, a dimensionless inductance parameter that characterizes the loop, is given by:

$$\beta_L = \frac{L_2}{L_c} = \frac{L_2 2\pi I_{c,P}}{\Phi_o} \tag{2.18}$$

The current, I, is then given by Eqn. 1.1.

For the low-inductance regime, $\beta_L << 1$, Eqn. 2.17 yields a single solution for the current ($I = 0$). However, in the high-inductance regime ($\beta_L >> 1$) used for the T/H, there exist multiple stable states, nearly uniformly distributed in current. To help evaluate the allowed values of current, Eqn. 2.14 can be cast into yet another form:

$$n\Phi_o = I_n\left\{L_2 + \frac{\Phi_o}{2\pi I_n}[\phi_{P2a}(I_n) + \phi_{P2b}(I_n)]\right\} \tag{2.19}$$

where n is an integer representing the number of stored flux quanta and I_n is the corresponding current solution. Using the definition of the Josephson inductance, Eqn. 1.14, this equation can be rewritten:

$$n\Phi_o = I_n\left\{L_2 + L_c\frac{I_{c,P}}{I_n}[\phi_{P2a}(I_n) + \phi_{P2b}(I_n)]\right\} \tag{2.20}$$

The term in braces has the dimensions of inductance. It consists of a linear inductor, L_2, and two large-signal nonlinear inductors of the form:

$$L_{eff,i} = L_c\frac{I_{c,P}}{I_n}\phi_i(I_n) \tag{2.21}$$

For small values of ϕ_i (or $I_n/I_{c,P}$), the sine function in Eqn. 2.16 can be linearized, giving a principal value of the phase nearly equal to $I_n/I_{c,P}$. Then the effective nonlinear inductance given by Eqn. 2.21 reduces to the characteristic Josephson inductance:

$$L_{eff,i}|_{\min} = L_c \tag{2.22}$$

Yet, even in the limiting case where the loop current approaches the critical current, $|I_n| \sim I_{c,P}$, the principal value of the phase is only $\pi/2$, so the maximum large-signal inductance is still only:

$$L_{eff,i}|_{\max} = \frac{\pi}{2} L_c \tag{2.23}$$

Note that the current solutions in the superconducting loop depend on the large-signal effective inductances (L_{eff}) of the junctions, given above, which assume a rather narrow range of values. They do not depend on the incremental Josephson inductance (L_J), given by Eqn. 1.13, which has a singularity at $|I| = I_c$.

Since a superconducting T/H performs quantization in addition to the conventional signal capture function, it is appropriate to apply performance metrics normally associated with A/D converters such as bin widths, step sizes, differential linearity, and bit-resolution. The current step size, I_{step}, is the difference between neighboring values of allowed current in the hold loop. For $\beta_L >> 1$, the loop has a large number of closely spaced current solutions and the nonlinear variation of L_{eff} is weak compared to L_2. Therefore, one can evaluate Eqn. 2.20 at n and $n + 1$ using a single value of L_{eff} without introducing a large error. The difference between the resulting expressions is:

$$I_{step,n} \equiv I_{n+1} - I_n \approx \frac{\Phi_o}{L_2 + L_{eff}(I_n)} \tag{2.24}$$

The step size is largest near $I_n = 0$:

$$I_{step} = I_{step,max} \approx \frac{\Phi_o}{L_2 + L_c} = \frac{\Phi_o}{L_2(1+\beta_L^{-1})} \tag{2.25}$$

For $\beta_L >> 1$, the first order estimate of bin width, $I_{step} \approx \Phi_o/L_2$ is quite accurate.

The step size nonlinearity (ΔI_{step}) measures the deviation in step size from the ideal step size. In order to compute the nonlinearity, it is necessary to evaluate the limits of I_{step}. The step size decreases as the amplitude of the loop current, $|I_n|$, is increased. The minimum step size, which occurs near $|I_n| = I_{c,P}$, is easily calculated, giving:

$$I_{step,min} \approx \frac{\Phi_o}{L_2 + L_{eff,max}} = \frac{\Phi_o}{L_2 + (\pi/2)L_c} \tag{2.26}$$

If the ideal step size is taken to be that at $I_n = 0$ (i.e., the maximum step size), the step size nonlinearity in LSB's is given by:

$$\Delta I_{step,max} = \frac{I_{step,min} - I_{step,max}}{I_{step,max}} \approx \frac{(1-\pi/2)L_c}{L_2 + (\pi/2)L_c} = \frac{1-\pi/2}{\beta_L + \pi/2} \tag{2.27}$$

Clearly, the maximum ΔI_{step} is much less than one LSB for large β_L. However, the above calculation is a worst-case analysis that assumes that all current states within the limits, $|I_n| < I_{c,P}$, are available. The nonlinearity can be reduced further by restricting the input signal range to a subset of the allowed current states close to $I = 0$. For the T/H, the range of interest is only $|I_n| < I_{R,P} < I_{c,P}$, so the preceding analysis is pessimistic.

Counting the zero current solution, there are approximately N_{max} allowed values of current between $-I_{c,P}$ and $+I_{c,P}$, where N_{max} is given by:

$$N_{max} \approx 2\left(\frac{\beta_L}{2\pi}\right) + 1 = 2\left(\frac{L_2 I_{c,P}}{\Phi_o}\right) + 1 \tag{2.28}$$

In the T/H, the magnitude of the full-scale input current is limited by the return current rather than the critical current. Therefore, using Eqn. 2.13, the approximate dynamic range, N, of the T/H is given by:

$$N \approx 2\left(\frac{L_2 I_{R,P}}{\Phi_o}\right)+1 \tag{2.29}$$

The best case bit-resolution of the T/H is therefore:

$$B = \log_2(N) \tag{2.30}$$

ignoring errors due to noise and component mismatches.

2.2.3 - Offset Errors and Common-Mode Rejection

Random variations in component values can cause the T/H to incur errors when tracking or sampling an input signal well within the bandwidth of the circuit. Since the T/H bridge takes a differential input signal and applies it differentially to the inductor, it is immune to most common-mode device mismatches (i.e., those which are the same on the *a* and *b* sides of the bridge). The currents induced by common-mode variations, such as the bias current sources, interfere destructively. The T/H bridge is, however, susceptible to differential component mismatches (i.e., asymmetries between nominally equal components on the opposing *a* and *b* sides of the bridge). The following analysis considers the effects of these random variations on the dc track-mode error of the T/H.

The mean voltage across the hold inductor, L_2, is zero for a dc input. Therefore, the voltages across J_{P2a} and J_{P2b} are equal:

$$V_{P2a} = V_{I2} = V_{22} = V_{P2b} \tag{2.31}$$

where the V_i are the node voltages shown in Fig. 2.4. When the T/H is in track mode, the series junctions are in the S state and there is no voltage drop across these junctions. Thus, the voltages across J_{P1a} and J_{P1b} are also equal:

$$V_{P1a} = V_{I1} = V_{21} = V_{P1b} \tag{2.32}$$

The series junctions switch to the R state only after the parallel junctions have switched to the S state and have captured the signal. As a result, mismatch between the series junctions has little impact on the tracking or sampling error of the T/H. Nevertheless, the critical currents of the series junctions should be closely matched so that a minimal series junction current overdrive, $\delta_{I,S}$, is needed to ensure that all the series junctions switch to the R state.

In order to perform a first-order analytical calculation of the mismatch error, the real *I-V* curves of the parallel junctions are approximated by the zero-capacitance closed form given by Eqn. 1.43. Furthermore, the variations of the device parameters are assumed to be small compared to their respective nominal values. The analysis is performed in two parts, assuming that the input signal is zero. First, the errors introduced by the J_{P1a}, J_{P1b} junction pair and their bias currents are calculated. Then, the errors caused by the J_{P2a}, J_{P2b} pair and their bias currents are computed. In the latter computation, the errors due to the J_{P1a}, J_{P1b} pair are included as an additional, independent perturbation of I_{B2a} and I_{B2b}.

The following equality must be satisfied for the J_{P1a}, J_{P1b} pair:

$$R_{Ne,P1a}\sqrt{I_{P1a}{}^2 - I_{c,P1a}{}^2} = V_{P1a} = V_{P1b} = R_{Ne,P1b}\sqrt{I_{P1b}{}^2 - I_{c,P1b}{}^2} \tag{2.33}$$

where the currents through the junctions, I_{P1a} and I_{P1b}, are given by:

$$I_{P1a} = I_{B1a} - I_{err,P1} \qquad I_{P1b} = I_{B1b} + I_{err,P1} \tag{2.34}$$

The error current due to J_{P1a} and J_{P1b}, $I_{err,P1}$, is taken to flow in the same direction as the input and output currents.

The bias currents for cells *1a* and *1b* are written as the sum and difference of an average bias current, I_{B1}, and a mismatch bias current, ΔI_{B1}:

$$I_{B1a} = I_{B1} + \frac{\Delta I_{B1}}{2} \qquad I_{B1b} = I_{B1} - \frac{\Delta I_{B1}}{2} \tag{2.35}$$

Since the mismatch, ΔI_{B1}, is an algebraic quantity, the choice of which junction's bias current it augments is arbitrary. Similarly, the parallel junction critical currents can be written as:

$$I_{c,P1a} = I_{c,P1} + \frac{\Delta I_{c,P1}}{2} \qquad I_{c,P1b} = I_{c,P1} - \frac{\Delta I_{c,P1}}{2} \tag{2.36}$$

where $I_{c,P1}$ is the average critical current and $\Delta I_{c,P1}$ is the critical current mismatch. Finally, the extrinsic junction normal state resistances can be expressed as:

$$R_{Ne,P1a} = R_{Ne,P1} + \frac{\Delta R_{Ne,P1}}{2} \qquad R_{Ne,P1b} = R_{Ne,P1} - \frac{\Delta R_{Ne,P1}}{2} \tag{2.37}$$

where $R_{Ne,P1}$ is the average extrinsic normal resistance and $\Delta R_{Ne,P1}$ is the difference.

Since the errors are assumed to be small, the error due to each of these three parameter mismatches can be evaluated separately wile assuming that the remaining two mismatches are zero. Furthermore, terms that are quadratic and higher order in the mismatches can be ignored to first order. A straightforward calculation yields:

$$I_{err,P1}(\Delta I_{B1}, 0, 0) \approx \frac{\Delta I_{B1}}{2} = \frac{\Delta I_{B1}}{2I_{B1}}(1 + \delta_{I,P1}) I_{c,P1} \qquad \frac{\Delta I_{B1}}{I_{B1}} << 1 \tag{2.38}$$

where $\delta_{I,P1}$ is the average current overdrive for the J_{P1a}, J_{P1b} pair. A similar calculation gives:

$$I_{err,P1}(0,\Delta I_{c,P1},0) \approx -\frac{(\Delta I_{c,P1})I_{c,P1}}{2I_{B1}} = -\frac{\Delta I_{c,P1}}{2I_{c,P1}}(1+\delta_{I,P1})^{-1} I_{c,P1}$$
$$\frac{\Delta I_{c,P1}}{I_{c,P1}} << 1 \tag{2.39}$$

A more tedious calculation reveals:

$$I_{err,P1}(0,0,\Delta R_{Ne,P1}) \approx \frac{\Delta R_{Ne,P1}}{2R_{Ne,P1}}\frac{I_{B1}{}^2 - I_{c,P1}{}^2}{I_{B1}} = \frac{\Delta R_{c,P1}}{2R_{Ne,P1}}\frac{(1+\delta_{I,P1})^2 - 1}{1+\delta_{I,P1}} I_{c,P1}$$
$$\frac{\Delta R_{Ne,P1}}{R_{Ne,P1}} << 1 \tag{2.40}$$

To first order, the total error due to J_{P1a}, J_{P1b}, I_{B1a}, and I_{B1b} is the sum of these three components:

$$I_{err,P1} \approx \frac{\Delta I_{B1}}{2} - \frac{(\Delta I_{c,P1})I_{c,P1}}{2I_{B1}} + \frac{\Delta R_{Ne,P1}}{2R_{Ne,P1}}\frac{I_{B1}{}^2 - I_{c,P1}{}^2}{I_{B1}} \tag{2.41}$$

This analysis can be repeated for the J_{P2a}, J_{P2b} pair and their bias currents, with the following substitution:

$$I_{B2a} = I_{B2} + \frac{\Delta I_{B2}}{2} + I_{err,P1} \qquad I_{B2b} = I_{B2} - \frac{\Delta I_{B2}}{2} - I_{err,P1} \tag{2.42}$$

The total error can then be written by inspection:

$$I_{err} \approx \left[\frac{\Delta I_{B1}}{2} - \frac{(\Delta I_{c,P1})I_{c,P1}}{2I_{B1}} + \frac{\Delta R_{Ne,P1}}{2R_{Ne,P1}}\frac{I_{B1}{}^2 - I_{c,P1}{}^2}{I_{B1}}\right]$$
$$+\left[\frac{\Delta I_{B2}}{2} - \frac{(\Delta I_{c,P2})I_{c,P2}}{2I_{B2}} + \frac{\Delta R_{Ne,P2}}{2R_{Ne,P2}}\frac{I_{B2}{}^2 - I_{c,P2}{}^2}{I_{B2}}\right] \tag{2.43}$$

where the second bracketed term is simply the contribution from J_{P2a}, J_{P2b}, I_{B2a}, and I_{B2b}.

In order to derive a simpler, statistical expression for the error, the bias currents, critical currents, and extrinsic normal resistances are taken to be independent Gaussian random variables each characterized by a mean and standard deviation. The Δ quantities in Eqn. 2.43 represent the differences between two independent random variables; the variances of these random variables sum when the difference is taken. Thus, the following substitutions must be made:

$$\begin{aligned} I_{err} &\Rightarrow \sqrt{2}\sigma I_{err} \\ \Delta I_{B1}, \Delta I_{B2} &\Rightarrow \sqrt{2}\sigma I_B \\ \Delta I_{c,P1}, \Delta I_{c,P2} &\Rightarrow \sqrt{2}\sigma I_{c,P} \\ \Delta R_{Ne,P1}, \Delta R_{Ne,P2} &\Rightarrow \sqrt{2}\sigma R_{Ne,P} \end{aligned} \tag{2.44}$$

where σI_{err}, σI_B, $\sigma I_{c,P}$, and $\sigma R_{Ne,P}$ are, respectively, the standard deviations of the error current, bias current, critical current, and extrinsic normal state resistance of the parallel junctions. Eqn. 2.43 itself involves the sum of several independent random variables. Again, the variances add, yielding the desired result:

$$\sigma I_{err} \approx \sigma I_B + \frac{(\sigma I_{c,P}) I_{c,P}}{I_B} + \frac{\sigma R_{Ne,P}}{R_{Ne,P}} \frac{I_B^2 - I_{c,P}^2}{I_B} \tag{2.45}$$

where I_B, $I_{c,P}$, and $R_{Ne,P}$ are, respectively, the mean bias current, mean critical current, and mean extrinsic normal state resistance of the parallel junctions.

The error current computed above is independent of the input signal. It is a dc offset current which affects the value of the output current in track mode as well as any sampled current values. A small offset is usually tolerable in most high-speed signal-processing applications. However, if the T/H is to be used as part of a multi-point transient recorder, the differences in offsets between the many T/H's result in an error that must be minimized. For optimum performance, the spread of the offsets across the bank

of T/H's should be less than 1 LSB. Thus, a transient recorder requires a higher degree of process uniformity than a single T/H.

The Josephson junction bridge T/H is designed to accept a differential input signal. If the circuit is perfectly balanced, a common-mode input component will cause no change in the output current. Clearly, a common-mode input signal, $I_{in,CM}$, is indistinguishable from a change in the average bias currents in cells *1a* and *1b*. If the common-mode signal is small, the preceding error analysis can be reapplied. The common-mode error, $I_{err,CM}$, is the difference between the error given by Eqn. 2.43 at bias current ($I_{B1} + I_{in,CM}$) and that at bias current I_{B1}. The result is:

$$I_{err,CM} \approx \frac{I_{CM}}{I_{B1}}\left[\frac{(\Delta I_{c,P1})I_{c,P1}}{2I_{B1}} + \frac{\Delta R_{Ne,P1}}{2R_{Ne,P1}}\frac{I_{B1}^{\,2} + I_{c,P1}^{\,2}}{I_{B1}}\right] << I_{err} \tag{2.46}$$

Clearly, the common-mode error is a second-order effect for small common-mode input signals. The common-mode gain follows immediately:

$$A_{I,CM} \equiv \frac{I_{err,CM}}{I_{CM}} \approx \frac{1}{I_{B1}}\left[\frac{(\Delta I_{c,P1})I_{c,P1}}{2I_{B1}} + \frac{\Delta R_{Ne,P1}}{2R_{Ne,P1}}\frac{I_{B1}^{\,2} + I_{c,P1}^{\,2}}{I_{B1}}\right] \tag{2.47}$$

The common-mode rejection ratio (CMRR) is the ratio of the differential gain to the common-mode gain. Since the Josephson junction bridge T/H has unity differential gain, its CMRR is simply the inverse of its common-mode gain. The moderate CMRR of the T/H is more than sufficient because it does not have to resolve a small differential signal superimposed on a large common-mode signal, as do operational amplifiers in some configurations.

2.3 - High-Speed Design Issues

The performance of the T/H in track mode and hold mode can be evaluated to first order using passive, linearized circuit models appropriate for each mode. In order to synthesize these models, one should begin with expressions for the incremental impedance, Z_J, of the junction switches in the R state and S state. The incremental impedance of a resistively shunted junction in the R state is predominantly real, $Z_J \approx R_J$. To first order, R_J for a resistively shunted junction is simply the extrinsic normal resistance, R_{Ne}, given by Eqn. 1.31. A better estimate of R_J for a shunted junction that accounts for the nonlinearity of the *I-V* curve for finite overdrive is r_{oe}, given by Eqn. 1.45. Below ω_{ce}, the incremental impedance of a shunted junction in the S state is reactive, with a value equal to the reactance of the Josephson inductance, L_J, given by Eqn. 1.13. Since junctions in the S state (in either track mode or hold mode) will not have to operate close to $I = I_c$, the additional approximation $L_J \approx L_c$ is adequate for the following analyses.

2.3.1 - Track-Mode Dynamics

Fig. 2.6 shows the small-signal equivalent T/H circuit in track mode. The four passive circuit elements in the bridge represent the total impedances of the four two-junction switches, and are given by:

$$\begin{aligned} R_{P1} &= R_{J,P1a} + R_{J,P1b} \qquad L_{Sa} = L_{J,S1a} + L_{J,S2a} \\ R_{P2} &= R_{J,P2a} + R_{J,P2b} \qquad L_{Sb} = L_{J,S1b} + L_{J,S2b} \end{aligned} \tag{2.48}$$

The quantity of interest, the track-mode transfer function, is easily computed from the circuit, giving:

$$a_{i,track}(s) \equiv \frac{i_{out}}{i_{in}} = \frac{1}{1 + (\tau_1 + \tau_2 + \tau_3)s + \tau_2\tau_3 s^2} \tag{2.49}$$

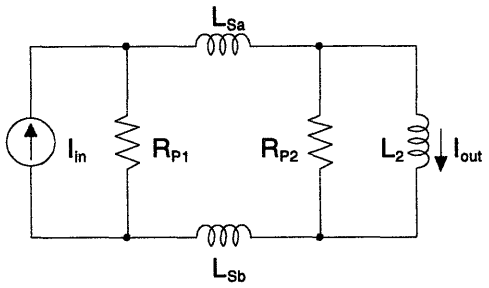

Figure 2.6 - Equivalent linear circuit for the T/H in track mode.

where

$$\tau_1 = L_2/R_{P1} \quad \tau_2 = L_2/R_{P2}$$
$$\tau_3 = L_S/R_{P1} \quad L_S = L_{Sa} + L_{Sb} \tag{2.50}$$

In the $\beta_L >> 1$ limit, L_2 is dominant, and the inductances of the series junctions have a minimal impact on isolating the conductances of the two parallel paths, so Eqn. 2.49 can be simplified, yielding:

$$a_{i,track}(s) \underset{|s|<<\tau_3^{-1}}{\approx} \frac{1}{1+(\tau_1+\tau_2+\tau_3)s} \underset{L_2>>L_S}{\approx} \frac{1}{1+\tau_{track}s} \tag{2.51}$$

where the track-mode time constant is given by:

$$\tau_{track} = \omega_{track}^{-1} = (2\pi f_{track})^{-1} = L_2/R_{J,P} \tag{2.52}$$

The T/H has essentially a one-pole transfer function with a corner frequency determined by the hold inductor and the incremental resistance of one resistively shunted parallel junction. Clearly, the technique of decreasing the shunt resistance across the parallel junctions to raise the return current and improve the signal range has the undesirable effect of reducing the small-signal bandwidth.

2.3.2 - Hold-Mode Dynamics

A similar analysis can be performed in hold mode with the aid of the equivalent circuit shown in Fig. 2.7. Again, it is convenient to define several intermediate quantities:

$$\begin{aligned} L_{P1} &= L_{J,P1a} + L_{J,P1b} \quad & R_{Sa} &= R_{J,S1a} + R_{J,S2a} \\ L_{P2} &= L_{J,P2b} + L_{J,P2b} \quad & R_{Sb} &= R_{J,S1b} + R_{J,S2b} \end{aligned} \tag{2.53}$$

The hold-mode transfer function is then:

$$a_{i,hold}(s) \equiv \frac{i_{out}}{i_{in}} = \alpha_1 \frac{\tau_{hold} s}{1 + \alpha_2 \tau_{hold} s} \tag{2.54}$$

where

$$\begin{aligned} \tau_{hold} &= L_{P1}/R_S & R_S &= R_{Sa} + R_{Sb} \\ \alpha_1 &= \frac{L_{P2}}{L_{P2} + L_2} & \alpha_2 &= \frac{L_{P2} + L_2(1 + L_{P2}/L_{P1})}{L_{P2} + L_2} \end{aligned} \tag{2.55}$$

The T/H bridge has no dc path from input to output, so the transfer function has a zero at the origin. The prefactor, α_1, accounts for the current division in the hold loop of the T/H bridge. In a topology such as the Davidson sampler, the overall hold-mode transfer function is approximately equal to α_1 at all frequencies. The bridge topology

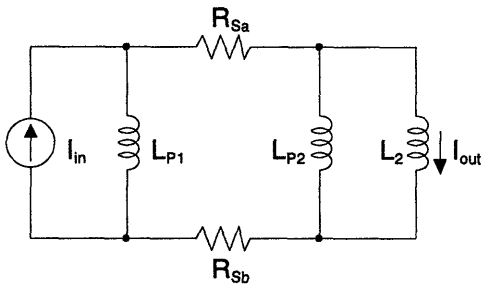

Figure 2.7 - Equivalent linear circuit for the T/H in hold mode.

achieves far superior hold-mode isolation at frequencies below τ_{hold}^{-1}. In the high-frequency limit, the hold-mode transmission attains a plateau and the bridge looks like a parallel inductive divider to first order:

$$a_{i,hold}(s) \underset{|s|>>\alpha_2\omega_{hold}}{\approx} \frac{\alpha_1}{\alpha_2} = \frac{L_{P1}L_{P2}/(L_{P1}+L_{P2})}{L_{P1}L_{P2}/(L_{P1}+L_{P2})+L_2} \underset{L_{P1}=L_{P2}=L_P}{=} \frac{L_P}{L_P+2L_2} \qquad (2.56)$$

This expression is only approximately correct. Clearly, the validity of neglecting the real part of the parallel junctions' shunt impedance must be reexamined in the $\omega_{hold} \sim \omega$ frequency regime. However, an exact solution is not necessary since this frequency range is well beyond the operating bandwidth of the T/H.

2.3.3 - Acquisition Dynamics and Sampling Rate

The maximum sampling rate of the T/H is inversely related to the acquisition time. The latter specification is the minimum track-mode pulse width that allows the T/H to acquire a full-scale change in input current to the specified level of accuracy. In general, the total acquisition time of a T/H consists of three terms: the switch turn-on time, the slew-rate limited large signal acquisition time, and the linear settling time. In practice, the switch turn-on time may be limited by the rise and fall times of the external clock because of the extremely high intrinsic switching speed of the Josephson junctions.

In the Josephson junction bridge T/H, the switch turn-on time is the period needed for the parallel junctions to switch from the S state to the R state and the series junctions to switch from the R state to the S state. If the clock rise and fall times are fast enough, the switch turn-on time will be dominated by the junction switching times. The worst-case acquisition transient requires the current held in L_2 to swing from $-I_{FS}$ to $+I_{FS}$ (or, equivalently, from $+I_{FS}$ to $-I_{FS}$). The parallel junctions must make S→R transitions before the current in the inductor can begin to decay towards zero. On the other hand, the R→S transitions of the series junctions can take place concurrently with the initial decay of the

held current because these junctions are responsible for the admission of the new input current rather than the dissipation of the held current. Provided the series junctions make R→S transitions well before the held current nears zero, the acquisition transient will not be significantly retarded. Since the parallel junction S→R switching time is in the critical delay path and is comparable to the series junction R→S switching time, the bridge turn-on time is given by the former:

$$t_{turn-on} = \tau_{S\rightarrow R,P} \tag{2.57}$$

Two processes affect the speed of the S→R switching process. Initially, the junction experiences a turn-on delay, τ_D, due to its supercurrent. For small overdrive, the delay time is approximately given by [3]:

$$\tau_D \approx \omega_p^{-1}\sqrt{\frac{\pi}{\delta_I}} \tag{2.58}$$

After the initial delay, the junction voltage rises to the gap voltage on the time scale of the capacitive recharge time, τ_R. The voltage across a current-source-driven junction with low G_{oe} is slew-rate limited, so the voltage trajectory is nearly linear, and τ_R is given by:

$$\tau_R = \frac{CV_g}{I_B} \tag{2.59}$$

If, however, G_{oe} is large enough to steal a significant fraction of the current drive, the voltage approaches the gap voltage exponentially on the time scale of a the extrinsic subgap RC time constant:

$$\tau_R \approx \tau_{oe} = R_{oe}C \tag{2.60}$$

To first order, the total S→R switching time is proportional to the sum of the aforementioned time constants:

$$t_{S\to R} \approx \eta_{S\to R}(\tau_D + \tau_R) \tag{2.61}$$

where $\eta_{S\to R}$ is a factor on the order of unity.

Once the bridge has turned on, it behaves as if it were in track mode. After the slew-rate limited regime, the track-mode transfer function (Eqn. 2.49) describes the subsequent time evolution of the acquisition transient. The analysis of this mode showed that the T/H has approximately a first-order transfer function. The time-domain response to a full-swing step at $t = 0$ is readily obtained via the inverse Laplace transform:

$$I_L(t) = I_{FS}\left[1 - 2\exp\left(\frac{-t}{\tau_{track}}\right)\right] \tag{2.62}$$

The maximum slope of the first-order response occurs at $t = 0$:

$$\left.\frac{dI_L}{dt}\right|_{\max,1st} = \frac{2I_{FS}}{\tau_{track}} = \frac{2I_{FS}R_{J,P}}{L_2} < \frac{2V_c}{L_2} \tag{2.63}$$

The slew rate limit of the T/H is achieved when the two parallel junction voltages are near the gap voltage and sum across the inductor, giving:

$$\left.\frac{dI_L}{dt}\right|_{\max,slew} \approx \frac{2V_g}{L_2} = \frac{8V_c}{\pi L_2} > \left.\frac{dI_L}{dt}\right|_{\max,1st} \tag{2.64}$$

Since maximum slope of the first-order transient is less than the maximum achievable slew rate of the T/H, the T/H's acquisition transient should be nearly first-order and should display no slew rate limiting.

As a result, the time evolution of the error signal is simply:

$$I_{err}(t) = I_{FS} - I_L(t) = 2I_{FS}\exp\left(\frac{-t}{\tau_{track}}\right) \tag{2.65}$$

The linear settling time, $t_{lin,acq}$, to B-bit accuracy is given implicitly by:

$$I_{err}(t_{lin,acq}) = \frac{I_{range}}{2^B} = \frac{I_{FS}}{2^{B-1}} = 2I_{FS}\exp\left(\frac{-t_{lin,acq}}{\tau_{track}}\right) \tag{2.66}$$

from which one obtains:

$$t_{lin,acq} = B\ln 2\tau_{track} \tag{2.67}$$

Finally, the total acquisition time for the case of a fast clock rise time, $t_{r,K}$, is:

$$t_{acq} = t_{S\to R} + t_{lin,acq} \approx \eta_{S\to R}(\tau_D + \tau_R) + B\ln 2\tau_{track}, \quad t_{S\to R} > t_{r,K} \tag{2.68}$$

Since the circuit time constant, τ_{track}, is much longer than those associated with the junction, τ_D and τ_R, the linear settling time dominates the total acquisition time. If, on the other hand, the clock rise time is longer than the S→R transition time, the acquisition time will be limited by the former:

$$t_{acq} \approx t_{r,K} + t_{lin,acq} \approx t_{r,K} + B\ln 2\tau_{track}, \quad t_{S\to R} < t_{r,K} \tag{2.69}$$

In order for the T/H to switch to hold mode, the parallel junctions must make S→R transitions and the series junctions must make R→S transitions. In the fast clock limit, the hold-mode settling time is limited by the parallel junctions, which are part of the hold loop. The R→S transition involves two events, the decay of the mean voltage across the junctions and the subsequent damping of the plasma oscillations. The exponential decay of the mean junction voltage is initiated by an instability in the R state which typically occurs near the plasma voltage, V_p [3]. The process is characterized by the extrinsic

subgap RC time constant, τ_{oe}. In underdamped junctions, the plasma oscillations decay within an exponential envelope having a time constant of $2\tau_{oe}$, which is long compared to the oscillation period, ω_p^{-1}. In overdamped junctions, the decay is not oscillatory and takes place with a time constant which is the inverse of the subgap characteristic frequency. By definition, the inverse of the characteristic frequency and the RC time constant are comparable in the regime of interest, $\beta_{oe} \sim 1$. Therefore, the underdamped decay time can be used, to first order. If the clock rise time is not the limiting factor, the minimum hold time is equal to the overall R→S transition time, which is given by:

$$t_{hold} = t_{R\to S} \approx \eta_{R\to S}\tau_{oe}, \quad t_{R\to S} > t_{r,K} \tag{2.70}$$

where $\eta_{R\to S} \sim 3$. In the limit of long clock rise time, the minimum hold time is given by:

$$t_{hold} = t_{r,K}, \quad t_{R\to S} < t_{r,K} \tag{2.71}$$

The maximum sampling rate is achieved if the duty cycle of the sampling clock can be adjusted so that the track period is equal to the acquisition time and the hold time is at its minimum. With this optimum duty cycle, the sampling rate is given by:

$$f_{samp}\big|_{\max} = \frac{1}{t_{samp}\big|_{\min}} = \frac{1}{t_{acq} + t_{hold}} \tag{2.72}$$

In practice, a 50% duty cycle sampling clock is usually much easier to implement than the optimum. With the constraint of equal track and hold periods, the sampling rate is limited by the larger of the two periods:

$$f_{samp} = t_{samp}^{-1} = \frac{1}{2\max(t_{acq}, t_{hold})} \tag{2.73}$$

In the Josephson junction bridge T/H, the acquisition time dominates, so the maximum sampling rate is:

$$f_{samp} = t_{samp}^{-1} = \frac{1}{2t_{acq}} \approx \begin{cases} \left[2\left(t_{S\to R} + B\ln 2\tau_{track}\right)\right]^{-1}, & t_{S\to R} > t_{r,K} \\ \left[2\left(t_{r,K} + B\ln 2\tau_{track}\right)\right]^{-1}, & t_{S\to R} < t_{r,K} \end{cases} \tag{2.74}$$

2.3.4 - Dynamic Errors

The T/H may experience dynamic mismatch errors in addition to the quasi-static errors discussed in earlier. These errors result from variations in the amplitude of the clock currents and their interactions with the rest of the T/H circuit. In the actual implementation of the T/H, the two clocks are synthesized from a single source and therefore are almost perfectly synchronized. However, if the amplitudes of the clock currents are unequal, the T/H will experience an error. Since the series junctions remain superconducting until after the hold loop has closed, the clock error is similar to a bias current error. However, this error will manifest itself only after the input current is sampled, not in track mode. Only the fraction of the clock mismatch that occurs before the T/H switches to hold mode affects the sampling error. Thus, the sampling error due to a small clock mismatch is given by:

$$I_{err,clk} \approx -\frac{\Delta I_K}{2}\frac{I_B - I_{R,P}}{I_K} \qquad \frac{\Delta I_K}{I_K} << 1 \tag{2.75}$$

where $I_{R,P}$ is the nominal return current of the parallel junctions, $\Delta I_K = I_{Ka} - I_{Kb}$ is the difference between the two clock current amplitudes, and $I_K = (I_{Ka} + I_{Kb})/2$ is the average clock current amplitude.

Component mismatch, combined with the nonzero rise time of the clock signal, gives rise to another type of dynamic error. The following analysis evaluates this error independently of the error sources that have already been calculated. If the return currents of $J_{P,2a}$ and $J_{P,2b}$ are unequal and the slew rate of the clock is finite, the two junctions cannot return to the S state simultaneously. As a result, the hold inductor will see a nonzero voltage for a nonzero time interval. The time integral of this voltage has the dimensions of flux. This flux injection error, Φ_{inj}, is akin to the charge injection error experienced in semiconductor T/H circuits. To first order, its magnitude is given by:

$$\Phi_{inj} = \int_0^{\Delta t} V dt \approx V_{ce,P} \Delta t = I_{c,P} R_{Ne,P} \Delta t \tag{2.76}$$

where $V_{ce,P}$ is the extrinsic characteristic voltage of the parallel junctions and the flux injection time, Δt, is related to the rise time of the clock, $t_{r,K}$, by:

$$\Delta t \approx t_{r,K} \frac{|\Delta I_{R,P}|}{I_B} = t_{r,K} \frac{|\Delta I_{R,P}|}{(1+\delta_{I,P}) I_{c,P}} \tag{2.77}$$

The current error due to flux injection, $I_{err,inj}$, is simply the ratio of the injected flux to the hold inductance:

$$I_{err,inj} = \frac{\Phi_{inj}}{L_2} \approx \frac{R_{Ne,P}}{L_2} t_{r,K} \frac{|\Delta I_{R,P}|}{(1+\delta_{I,P})} = \frac{t_{r,K}}{t_{track}} \frac{|\Delta I_{R,P}|}{(1+\delta_{I,P})} \tag{2.78}$$

where t_{track} is the track-mode time constant. In a typical implementation of the T/H, the clock edges should be at least as fast as the signal being sampled, so the ratio of times, $t_{r,K}/t_{track}$, should be no worse than unity. Therefore, since $I_{FS} \approx I_{R,P}$, the return currents of the parallel junctions must be matched to roughly a part in 2^B, where B is the bit-accuracy

of the T/H, to keep flux injection error on the order of 1 LSB. The dependencies of the return current are:

$$I_R \propto \frac{I_c}{\sqrt{\beta_{oe}}} \propto \frac{1}{\sqrt{C}} \propto \sqrt{I_c} \propto \frac{1}{R_{oe}} \tag{2.79}$$

Clearly, the extrinsic subgap resistance, R_{oe}, has the strongest effect on the return current. Yet, this dependence is only inversely linear. Thus, at a given level of component variations, the T/H is no more susceptible to flux injection error than to the other types of errors discussed earlier.

Finally, if the amplitude of the clock current differs from twice the magnitude of the bias current, the parallel junctions will carry a residual common-mode bias current in hold mode. This common-mode current will limit the largest signal that the T/H can acquire since it will consume a fraction of the total return current available to the circulating output current. In practice, the amplitude of the clock and bias currents are adjusted to minimize this common-mode mismatch and maximize the full-scale input of the T/H.

2.4 - Simulation

The Josephson junction bridge T/H was simulated extensively using numerical computer models. The simulations were designed to verify the analytical calculations of the performance of the circuit. The calculations of the track mode and hold mode behavior were more rigorous than the analysis of the complex switching dynamics of the bridge. Thus, the prime focus of the simulations was the confirmation of the proper sampling operation of the circuit. The simulations were also targeted at extracting key specifications of the T/H: input signal range, tracking bandwidth, sampling bandwidth, acquisition time, resolution, and signal to noise ratio.

The simulations explored a wide range of topological modifications, speed vs. resolution tradeoffs, and parameter variations. Only those simulations which are most relevant to the final design are presented below. A comprehensive discussion of the implementation of the T/H is given in the next section. A more complete process description can be found in the next chapter.

2.4.1 - Software and Models

The JSIM (Josephson SIMulator) [31], [32] Josephson circuit simulation software from the University of California at Berkeley was used for most of the simulations of the T/H. It was selected because it is relatively fast and can be compiled to run on a personal computer. JSIM is based on the SPICE family of nodal, nonlinear circuit simulators. It supports circuits containing linear resistors, capacitors, inductors, transformers, lossless transmission lines, independent voltage and current sources, and Josephson junctions. JSIM only implements transient (time-domain) analysis; dc, parameter sweep, bias point, linearized ac, and Monte Carlo analyses are not supported. Three types of independent sources are supported: sinusoidal, piecewise linear, and pulse.

The JSIM Josephson junction model is based on an RSJN prototype with a piecewise linear conductance. The JSIM junction model uses six main parameters, one more than the RSJN model. Both models include the critical current (I_c), capacitance (C), normal resistance (R_N), subgap resistance (R_o), and gap voltage (V_g). In addition, the JSIM model specifies a nonzero gap transition voltage (ΔV) so that the subgap and normal regimes of the I-V curve can be connected by a segment having finite conductance.

With the exception of the capacitance, the values for the model parameters were extracted from the measured I-V curves of Josephson junctions fabricated in the same Lincoln Laboratory process as the T/H. The nominal critical current density of these junctions is J_c = 1000 A/cm^2. The specific capacitance was calculated from soliton

Table 2.1 - Nominal JSIM Model Parameters of a Lincoln Laboratory Josephson Junction (J_c = 1000 A/cm^2, A = 100 μm^2).

Parameter	Value
I_c	1.0 mA
C	4.5 pF
R_N	2.0 Ω
R_o	50 Ω
V_g	2.9 mV
ΔV	0.2 mV

resonance measurements of junctions processed at Lincoln Laboratory. Table 2.1 lists the nominal JSIM model parameters of a 10 x 10 μm^2 junction.

2.4.2 - Circuit Element Values

Since the Josephson junction bridge T/H is the first design of its type, a conservative approach was taken to select the device sizes in the final design. Where possible, ease of fabrication and testing were favored over optimum performance. In a 1000 A/cm^2 Josephson junction process, junction critical currents on the order of 100 μA – 1 mA can be achieved easily using conservative geometries (3 – 10 μm). Therefore, the T/H uses 640 μA parallel junctions and 960 μA series junctions; the critical current ratio, γ_{Ic} = 3:2, is a quotient of small integers, facilitating layout. A small (~ 1%) pseudo-random dither is applied to the junction critical currents in the simulation to suppress numerical artifacts which might otherwise arise from the rigid phase locking of identical junctions.

The bias current is taken to be 960 μA for simulation, corresponding to $\delta_{I,P} = 0.5$ and $\delta_{I,S} = 0$. Experimentally, the bias current must be adjusted to account for uncertainty of the critical current. As shown earlier, $\delta_{I,S}$ will be determined by the distribution of the series junctions' critical currents. The parallel junction critical currents and current overdrive are sufficient for full-scale inputs in the 320 μA – 640 μA range.

The size of the hold inductor was selected to give moderate resolution and bandwidth. This choice simultaneously relaxes the sensitivity and noise requirements of the low-speed test apparatus and the bandwidth requirements of the high-speed test equipment. Thus, experiments can measure unambiguously both the resolution and speed of the T/H. The characteristic inductance of the parallel junctions is L_c = 515 fH. By choosing L_2 = 102.5 pH, the maximum current step size, given by Eqn. 2.25, is I_{step} = 20.0 μA. This signal level is easily resolved using the instrumentation available. With full-scale inputs in the 320 μA – 640 μA range, roughly 5-bit to 6-bit performance is expected. This bit-resolution is consistent with the typical on-chip parameter spreads offered by the Josephson junction process used to fabricate the T/H.

The main degree of freedom in the T/H design is the choice of the parallel junctions' shunt resistor, $R_{sh,P}$. Its value influences both the input signal range and the bandwidth. It is the independent variable in many of the simulation results presented in the following subsections.

2.4.3 - Input Signal Range

Since γ_{Ic} = 1.5, $I_{c,S}$ is larger than any achievable value of $I_{R,P}$. Thus, the tracking range of the T/H should not limit the full-scale input range of the T/H. Fig. 2.8 shows a simulation of the T/H with typical parameters ($R_{sh,P}$ = 0.375 Ω) tracking a slow trapezoidal input pulse having a peak amplitude of 640 μA. The offset is negligible and the gain is nearly unity, as expected. The output current exhibits a small (< 5 μA, p-p) ripple, which is evident when the input reaches its plateau. Although the ripple is not unexpected, the apparent period of these oscillations is an artifact of the simulation's output time step. In track mode, the Josephson oscillations of the parallel junctions, which are in the R state, induce a time varying current in the hold inductor.

The lag in the output response is consistent with the finite track-mode bandwidth of the circuit. For a first order system such as the T/H, the first error coefficient (e_1),

which measures the steady-state output lag with a ramp input, is equal to the characteristic time of the system, in this case τ_{track}. The simulation shows $e_1 \approx 220$ ps; the inferred half-power bandwidth is 725 MHz, in close agreement with the 700 MHz track-mode bandwidth calculated using $R_{J,P} \approx r_{oe,P}$ in Eqn. 2.52.

The quasi-static input range of the T/H is determined by sampling a slow ramp input. Fig. 2.9 shows the initial part of this type of simulation for a T/H with typical parameters. The slew rate of the input, dI/dt = 10 μA/ns, is equal to the maximum slew rate of a 1.28 mA p-p sine input at 2.5 MHz. Since the T/H always has at least one junction in the R state, the simulator's maximum time step must be commensurate with the period of the Josephson oscillations rather than the lower speeds of the input and clock. Consequently, the computation time of a true low-speed simulation is prohibitive.

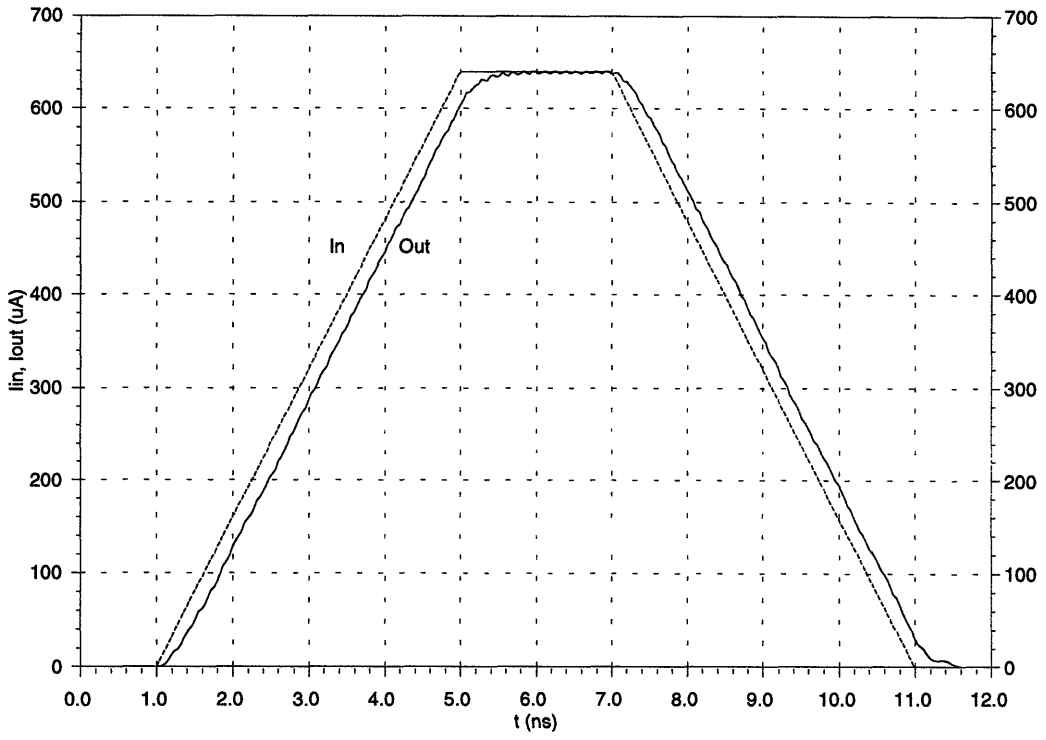

Figure 2.8 - Simulated tracking performance of the T/H with a slow trapezoidal input signal. The figure shows the input signal (In) and the output signal (Out). $R_{sh,P} = 0.375\ \Omega$.

Fortunately, the T/H is fast enough that, with a slow input, a 1 GS/s sampling rate can be used to determine the quasi-static input range of the T/H. Since the ramp is slow, the T/H can acquire the input to the required accuracy within the 675 ps track period used for the simulation; the 275 ps hold period gives ample time for the output to settle. The resulting 1 ns sampling period gives two samples near each of the allowed output current steps; these steps, which are separated by about 20 μA, are clearly visible in the simulated output. The Josephson oscillations of the parallel junctions are again evident when the T/H is in track mode, but these oscillations are absent in hold mode, as expected.

The signals of interest for determining the input range are the output current samples. Since the output current is relatively flat when the T/H is in hold mode, these

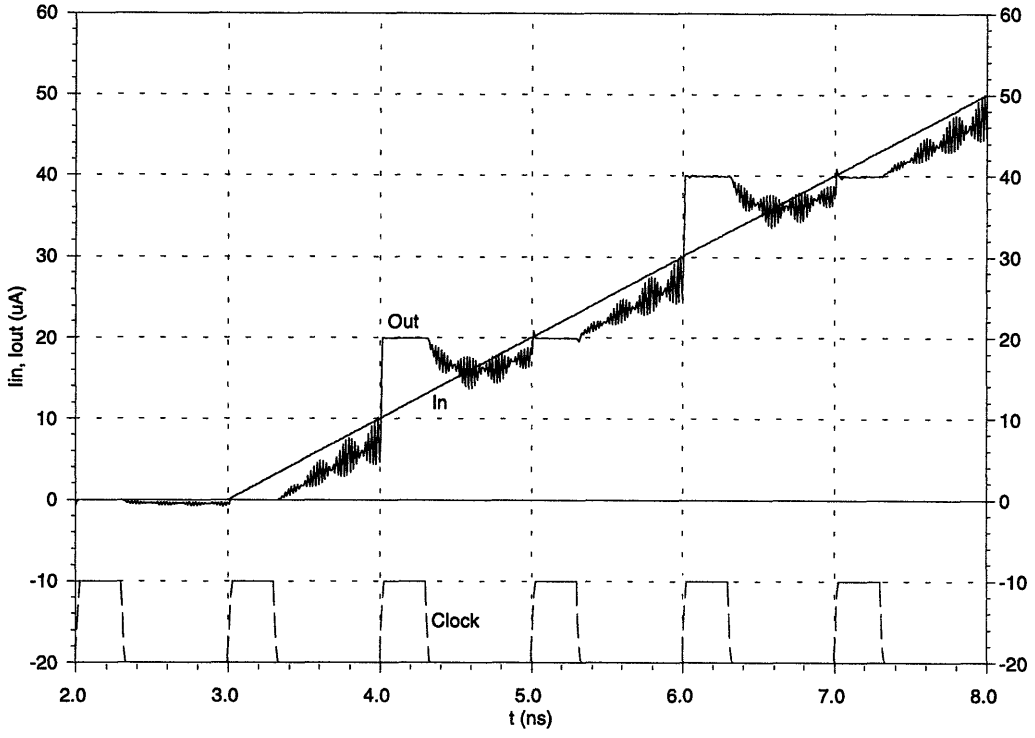

Figure 2.9 - Simulated sampling performance of the T/H with a slow ramp input. The input signal (In) and output signal (Out) are shown. The clock is shown schematically by the dashed curve at the bottom; hold mode corresponds to a high clock level. The rise and fall times of the clock are 25 ps. $R_{sh,P} = 0.375\ \Omega$.

values can be obtained by simply decimating in time the values of the output currents produced by simulations such as that shown in Fig. 2.9. Fig. 2.10 shows the quasi-static sampling response curve of a T/H with $R_{sh,P}$ = 0.375 Ω. The values of sampled output current were extracted from two simulations and plotted vs. the input current at the sample time. The data in the first quadrant are taken from a simulation with a slowly rising ramp input; the data in the third quadrant are taken from a simulation with a slowly rising ramp input.

As was demonstrated in previous sections, the full-scale input of the T/H, I_{FS}, is approximately equal to the return current of the parallel junctions, $I_{R,P}$. The return current is determined by the extrinsic subgap capacitance parameter, β_{oe}, which is inversely

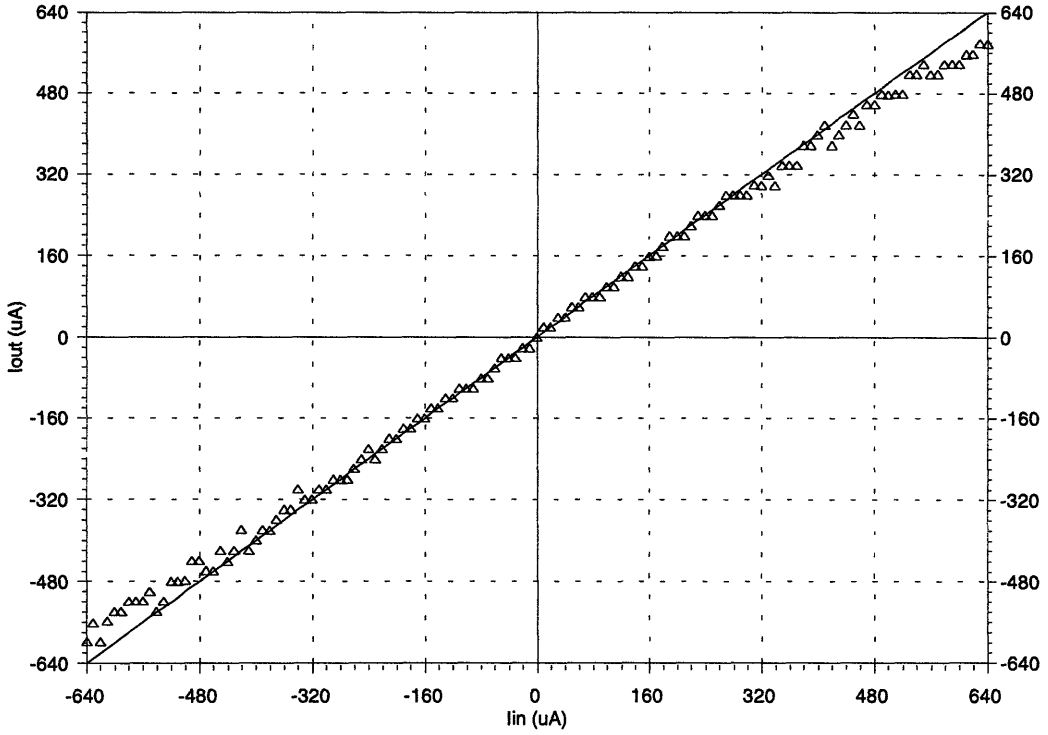

Figure 2.10 - Simulated quasi-static sampling response curve of the T/H ($R_{sh,P}$ = 0.375 Ω) extracted from samples of a slow ramp input. The output samples are shown as triangles; a unity-gain reference line is also shown. The data are extracted from time-domain simulations with 675 ps track time, 275 ps hold time, and 25 ps clock rise and fall times.

proportional to the extrinsic subgap resistance, R_{oe}. To first order, the return current of an externally shunted Josephson junction is also inversely proportional to the external shunt resistance, R_{sh}, since the intrinsic subgap resistance, R_o, is generally quite high. However, neither $I_{R,P}$ nor I_{FS} can exceed the critical current of the parallel junctions, $I_{c,P}$.

The parallel junctions in the T/H are non-hysteretic with $R_{sh,P} = 0.375\ \Omega$, so $I_{R,P} = I_{c,P}$. The first-order calculations presented in earlier sections predict that the sampling input range of the T/H should equal the maximum theoretical input range, –640 μA to +640 μA. The simulations of the T/H show that, with $|I_{in}| < 640\ \mu A$, the T/H can attain sampled currents no less than about –600 μA and no more than about +580 μA. Furthermore, the accuracy of the T/H degrades as the amplitude of the input signal approaches these limits.

The disparity between the calculated and simulated performance is not unexpected, since the former neglected the complex dynamics of the sampling process. The details of these dynamics become more important as the magnitude of the input signal approaches the critical current of the parallel junctions because switching transients occurring after the series junctions have already made the S→R transition can momentarily push the parallel junctions into the R state, partially dissipating the held current. Thus, the agreement between the calculation and simulation should improve as $I_{R,P}$ is reduced by increasing $R_{sh,P}$.

The current samples shown in Fig. 2.10 should differ by amounts that correspond to integer numbers of flux quanta (in this case, $n \cdot 20\ \mu A$). Fig. 2.11 shows the distribution of the absolute value of nonzero nearest neighbor steps, $|I_{n+1} - I_n|$, normalized by the number of flux quanta in the difference. The data are extracted from the simulated quasi-static sampling response curve. Most of the steps are clustered within a few percent of 20 μA and all of the steps are within 5% of the nominal value. Only a small part of the variation is due to the nonlinear large-signal inductance of the parallel junctions

calculated earlier ($\Delta I_{step,max} \approx 0.003$ LSB = 0.6 μA). Most of the spread results from the pseudo-random sampling of the small hold-mode ripple of the T/H by the decimation routine used to extract the hold-mode current samples. The ripple should not interfere with the operation of the T/H since its rms value is much less than 1 LSB.

Fig. 2.12 shows the quasi-static sampling response curve of the same T/H with $R_{sh,P}$ increased to 0.75 Ω. The parallel junctions are now hysteretic ($I_{R,P}/I_{c,P} = 0.72$). As expected, the maximum sampled signal amplitude is lower, as is the range of input signals over which the T/H accurately samples the input. To map out the dependence of the input range of the T/H on $R_{sh,P}$, this type of simulation was repeated using a range of shunt resistances.

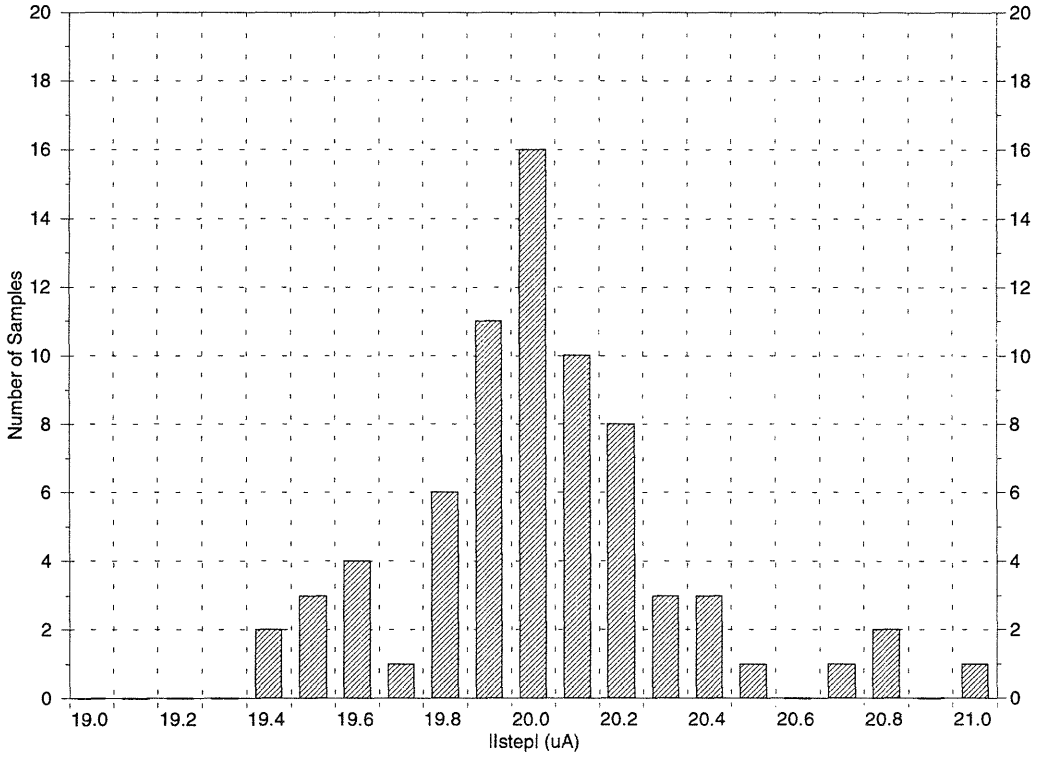

Figure 2.11 - Distribution of the absolute value of the normalized nearest neighbor current steps extracted from the simulated quasi-static sampling response curve of the T/H ($R_{sh,P}$ = 0.375 Ω). Step values corresponding to multiple flux quanta are normalized by the number of flux quanta; step values corresponding to zero flux quanta are not shown.

The maximum full-scale input, I_{FS}, is defined as the magnitude of the largest input signal that the T/H can sample accurately. The desired accuracy or, equivalently, the allowable error must be stipulated in order to determine I_{FS} from simulation. There are numerous choices for the measure of error. The output samples can be compared either to the input or to the best fit linear sampling response curve. Then, I_{FS} can be defined as half of the continuous range over which the maximum difference, average difference, or rms difference is less than some allowable error.

Fig. 2.13 shows the calculated full-scale input of the T/H, $I_{FS} = I_{range}/2$, as well as several measures of I_{FS} deduced from simulations vs. the shunt resistance of the parallel junctions. The full-scale input is readily measured if it is demarcated by the maximum

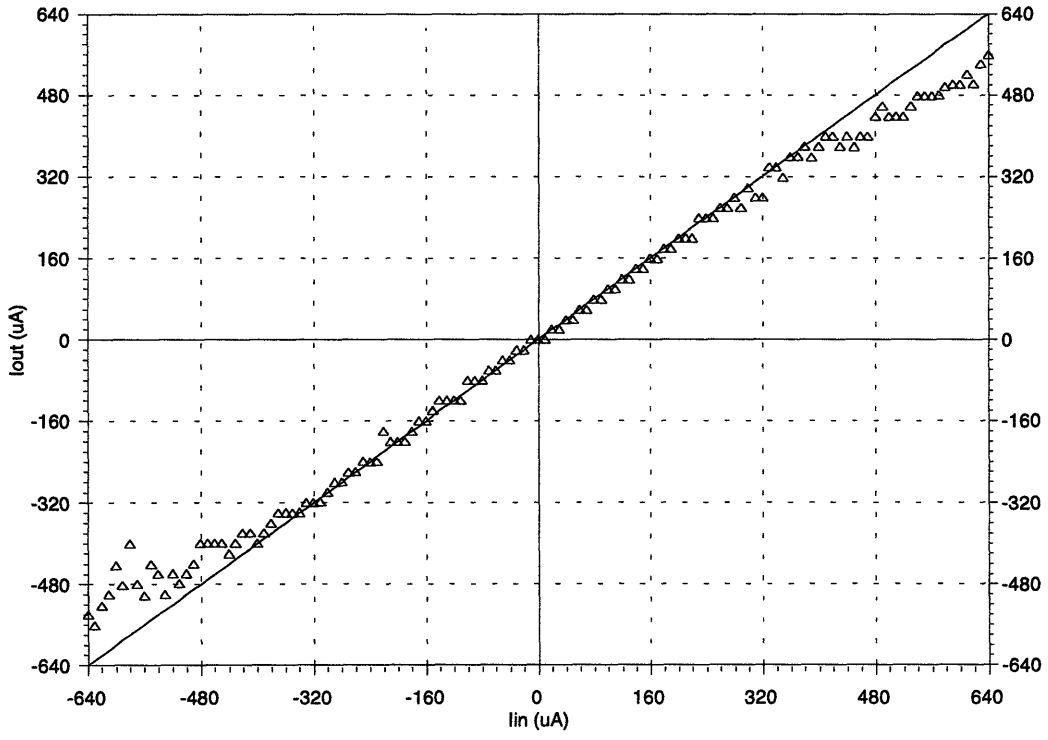

Figure 2.12 - Simulated quasi-static sampling response curve of the T/H ($R_{sh,P}$ = 0.75 Ω) extracted from samples of a slow ramp input. The output samples are shown as triangles; a unity-gain reference line is also shown. The data are extracted from time-domain simulations with 675 ps track time, 275 ps hold time, and 25 ps clock rise and fall times.

deviation from the input signal, although this definition is susceptible to sporadic aberrations in the sampling response curve. The ∇'s in Fig. 2.13 show the maximum-error-limited I_{FS}, defined as half of the total range over which the absolute error is no more than 3 LSB's (60 μA).

It is more difficult to determine I_{FS} if it is defined in terms of the rms deviation from the input signal, but this definition is more robust. The Δ's in Fig. 2.13 show the rms-error-limited I_{FS}, defined as half of the total range over which the rms error is no more than 1 LSB (20 μA). The simulation at $R_{sh,P}$ = 1.0 Ω appears to be an aberration, as it deviates from the otherwise monotonic decline in full-scale input with increasing $R_{sh,P}$.

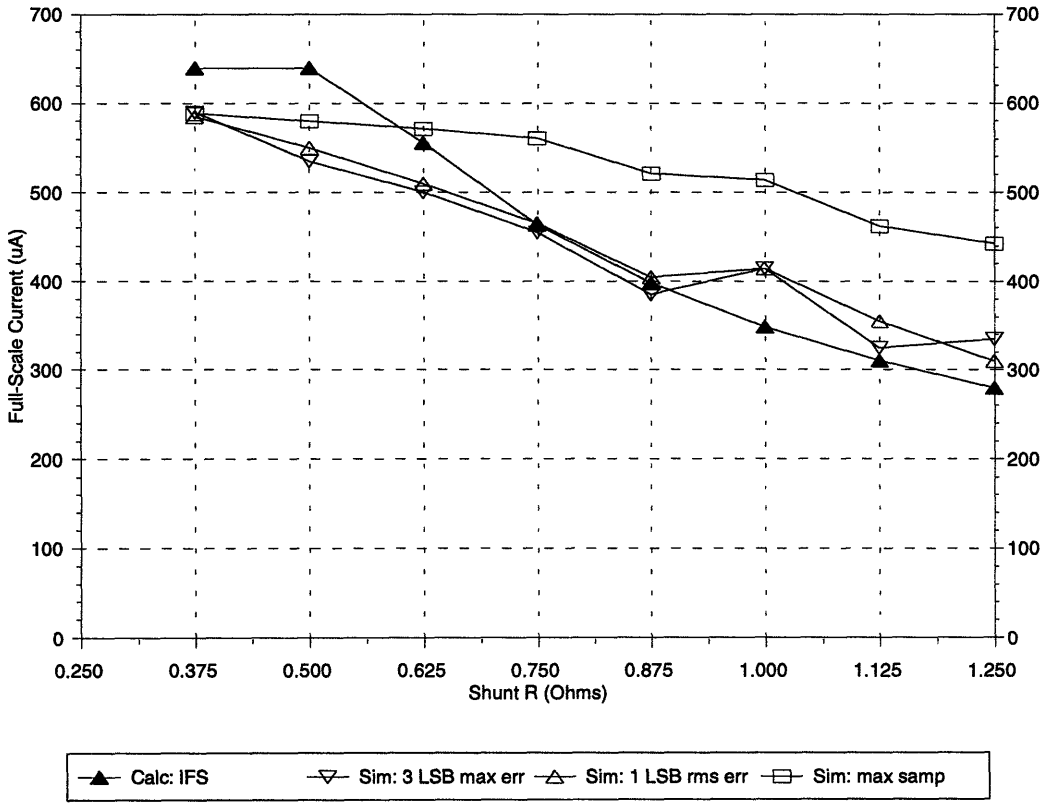

Figure 2.13 - Simulated and calculated quasi-static sampling input range of the T/H as functions of parallel junction shunt resistance. The filled triangles show the calculated maximum full-scale input current, I_{FS}. The ∇'s show the simulated input signal range over which the maximum error is less than 3 LSB. The Δ's show the simulated input signal range over which the rms error is less than 1 LSB. For comparison, the squares show the simulated maximum output current.

Nevertheless, both gauges of the simulated full-scale input are in fair agreement with each other and with the calculation of I_{FS}; the agreement improves with increasing $R_{sh,P}$.

2.4.4 - Tracking Bandwidth

The small-signal track-mode bandwidth of the T/H, f_{track}, is another key specification of the T/H that is directly influenced by the choice of $R_{sh,P}$. In summary, the hand analysis of the T/H showed that the half-power track-mode bandwidth is proportional to the incremental normal-state resistance of the parallel junctions, R_J. The two estimates of R_J for a shunted junction, $R_J \approx R_{Ne}$ and $R_J \approx r_{oe}$, are linear functions of R_{Ne}, the extrinsic normal-state resistance. Thus, f_{track} is proportional to R_{Ne}. It is not directly proportional to $R_{sh,P}$, the external shunt resistance of the parallel junctions, because R_N can be of the same order as R_{sh}.

The simulations presented below are intended to confirm the predicted track-mode bandwidth of the T/H. In a conventional circuit simulator such as SPICE, an incremental ac sweep simulation could be used to determine the detailed small-signal frequency response of a circuit. Because JSIM only supports time-domain simulations, which take considerable computation time, another technique must be employed. If the track-mode transfer function of the T/H is assumed to be first-order, its current gain at any frequency is given by:

$$a_{i,track}(f) = \frac{i_{out}}{i_{in}} = \frac{1}{\sqrt{1+(f/f_{track})^2}} \tag{2.80}$$

This expression is easily inverted to give:

$$f_{track} = \frac{f}{\sqrt{(a_{i,track}(f))^{-2} - 1}} \tag{2.81}$$

Using Eqn. 2.81, f_{track} can be computed from the simulated time-domain current gain of the T/H at some input frequency, f. If f is chosen such that $a_{i,track} = 2^{-1/2}$, the half-power bandwidth is obvious, but this choice cannot be made a priori. Nevertheless, if f is chosen close to the expected value of f_{track}, Eqn. 2.81 will be least sensitive to errors in the estimation of the current gain due to roundoff error and Josephson oscillations. By comparing the bandwidths obtained by this technique at several different frequencies, the original assumption of a first-order frequency response can be validated.

Fig. 2.14 shows the results of two time-domain simulations of the T/H in track mode; one was performed with $R_{sh,P} = 0.375\ \Omega$ and the other with twice the parallel shunt resistance. The input is a 500 MHz sine with a 320 μA peak amplitude. The peak

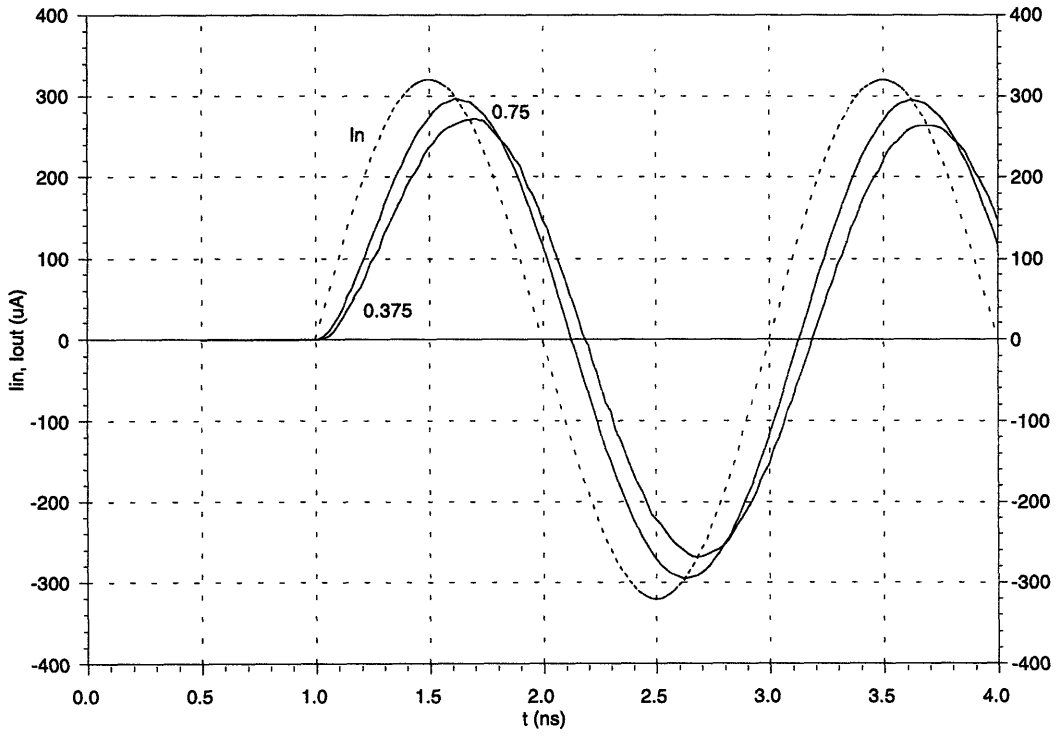

Figure 2.14 - Simulated tracking performance of the T/H with a 640 μA p-p, 500 MHz sinusoidal input and two different values of parallel shunt resistor. The plot shows the input signal (In) and the output signal for $R_{sh,P} = 0.375\ \Omega$ (0.375) and for $R_{sh,P} = 0.75\ \Omega$ (0.75).

amplitudes of the input and output signals are much larger than the ripple on the output current, but safely below the tracking input signal range of the T/H for either value of $R_{sh,P}$. Since JSIM does not support dc sources, the input is delayed 1 ns to allow the bias currents (not shown) to be elevated to their desired steady-state values. The T/H shows no unusual transient dynamics associated with the turn on of either the bias currents or the input generator. The half-power track-mode bandwidths of the T/H, computed via Eqn. 2.79, are 748 MHz and 1.16 GHz for the 0.375 Ω and 0.750 Ω shunt resistances, respectively. As expected, f_{track} increases less than linearly with increasing $R_{sh,P}$.

Fig. 2.15 shows two more time-domain simulations of the T/H with the same circuit parameters as in Fig. 2.14, but with a 1 GHz input frequency. Again, the circuit

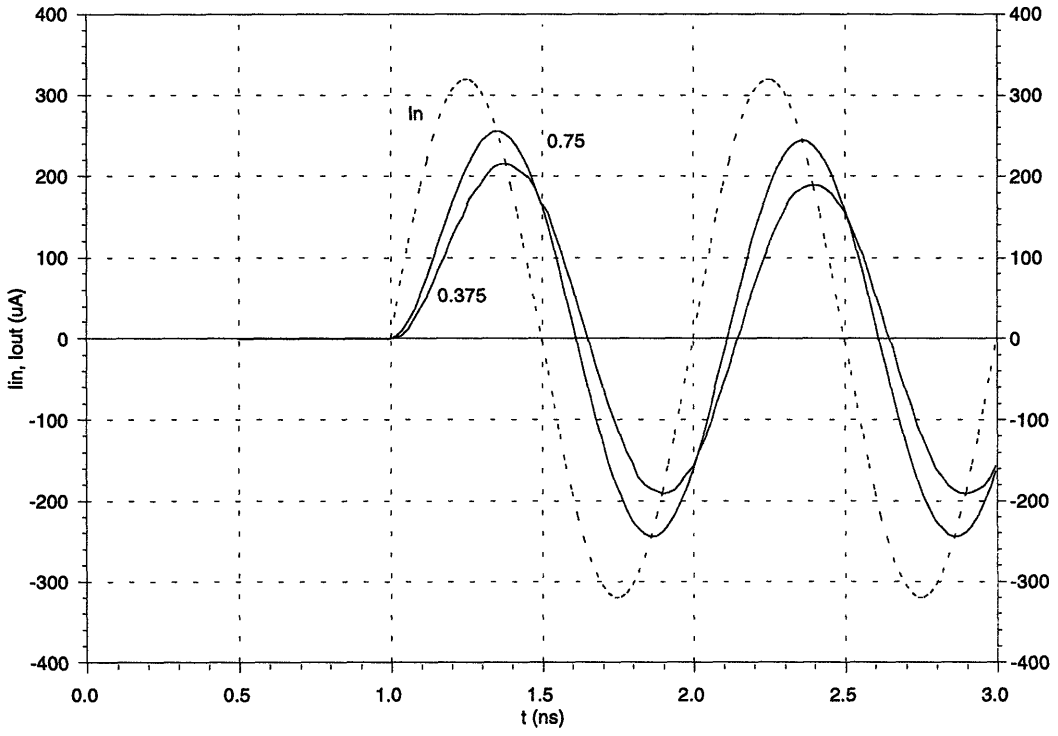

Figure 2.15 - Simulated tracking performance of the T/H with a 640 μA p-p, 1 GHz sinusoidal input and two different values of parallel shunt resistor. The plot shows the input signal (In) and the output signal for $R_{sh,P}$ = 0.375 Ω (0.375) and for $R_{sh,P}$ = 0.75 Ω (0.75).

shows no anomalous transient behavior. The extracted half-power bandwidths are 750 MHz and 1.18 GHz for the 0.375 Ω and 0.750 Ω shunt resistances, respectively. These values agree well with the corresponding bandwidths extracted from the 500 MHz time-domain simulations. Additional simulations show generally good agreement between the track-mode bandwidths extracted at various input frequencies ranging from 250 MHz to 2 GHz. These results suggest that the frequency response of the T/H is close to first-order.

Numerous simulations like those depicted in Fig. 2.14 and Fig. 2.15 were run using a fixed input amplitude of 320 μA, but a range of $R_{sh,P}$ values and input frequencies. The results of these simulations are summarized in Fig. 2.16. The data points on the simulated bandwidth curve are the averages of the simulated bandwidths

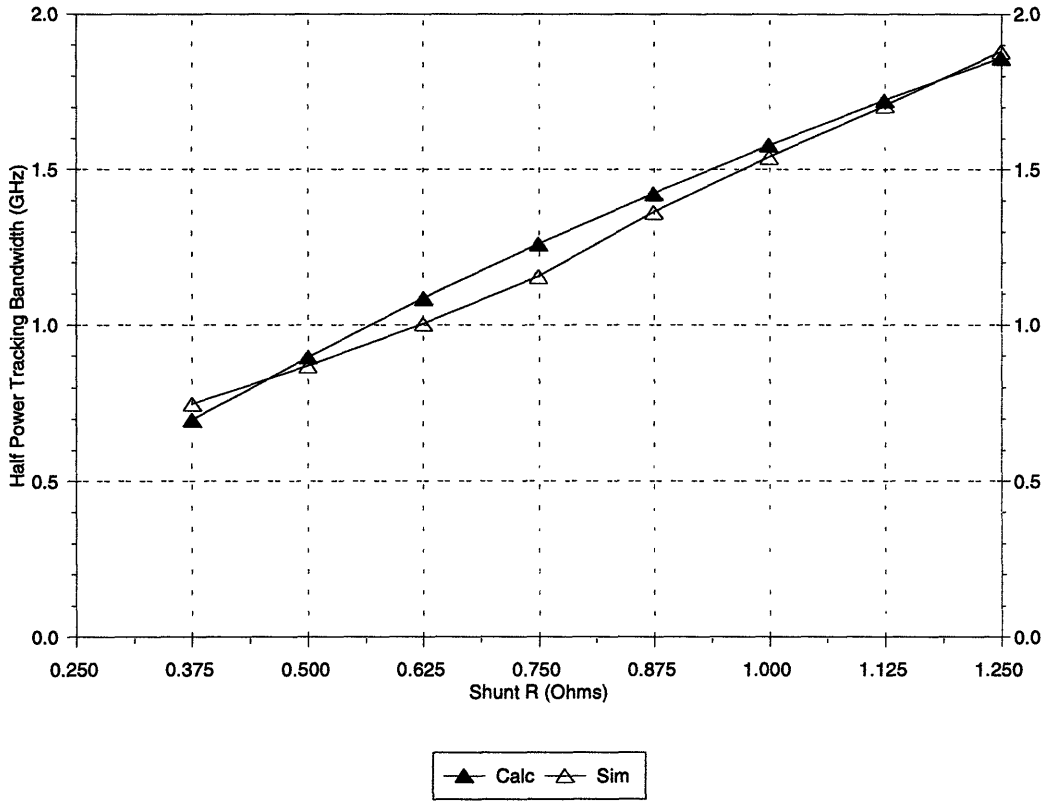

Figure 2.16 - Simulated and calculated track-mode bandwidth of the T/H vs. parallel junction shunt resistance. The filled triangles show the calculated bandwidth, f_{track}. The empty triangles show the average bandwidth extracted from 1 GHz and 2 GHz time-domain simulations.

computed using 1 GHz and 2 GHz input frequencies. These frequencies span the bandwidths that result from the range of shunt resistances shown, and the bandwidths inferred at these input frequencies are representative of those obtained over the 250 MHz – 2 GHz band of input frequencies. The simulated tracking bandwidth is in good agreement with the calculated bandwidth, also shown in Fig. 2.16, which is calculated using Eqn. 2.52 with the extrinsic normal-state resistance of the parallel junctions approximated by $R_{J,P} \approx r_{oe,P}$. Taking $R_{J,P} \approx R_{Ne}$ gives a 25% lower calculated bandwidth.

2.4.5 - Hold-Mode Isolation

The linear circuit analysis of the Josephson junction bridge T/H showed that it should have excellent hold-mode isolation over the entire tracking bandwidth of the circuit. Moreover, the T/H should have infinite dc isolation in hold mode since the incremental impedance of the series signal path is resistive and the incremental impedances of the shunt signal paths are inductive. These models are expected to be valid for frequencies well below ω_{ce}. However, simulations of the hold-mode performance of the T/H revealed some unexpected behavior.

Fig. 2.17 shows the bandlimited output current of the T/H with a 640 μA p-p, 1 GHz sinusoidal input current. The bandwidth of the smoothing filter is several decades above the input frequency. The peak amplitude of the output component at 1 GHz is about 100 nA, yielding a hold-mode current gain of 325 μA/A. This degree of isolation is more than sufficient, as the perturbation of the output current is 200 times less than one LSB. In hold mode, the amplitude of the raw output current, which includes the Josephson oscillations, is about three times larger than the filtered output.

The simulated output response at 1 GHz differs from the calculated response is two ways; its amplitude is larger, and its phase differs by about 90°. To aid in analyzing this disparity, Fig. 2.18 shows the gains and phases of the calculated and simulated hold-mode transfer functions of the T/H vs. frequency. The simulated data are taken from

time-domain simulations, such as that depicted in Fig. 2.17. The calculated curves are based on Eqn. 2.54, but over the range of input frequencies for which the linearized model is appropriate (well below 100 GHz), the hold-mode transfer function is well approximated by a zero at the origin:

$$a_{i,hold}(s) \approx \alpha_1 \tau_{hold} s, \quad \omega << (\alpha_2 \tau_{hold})^{-1} \tag{2.82}$$

On the other hand, the simulations suggest an alternative form for the hold-mode transfer function, given by:

$$a_{i,hold\_sim}(s) \approx -\alpha_{1,sim}(1 - \tau_{hold,sim} s) = -\alpha_{1,sim} + \alpha_{1,sim} \tau_{hold,sim} s \tag{2.83}$$

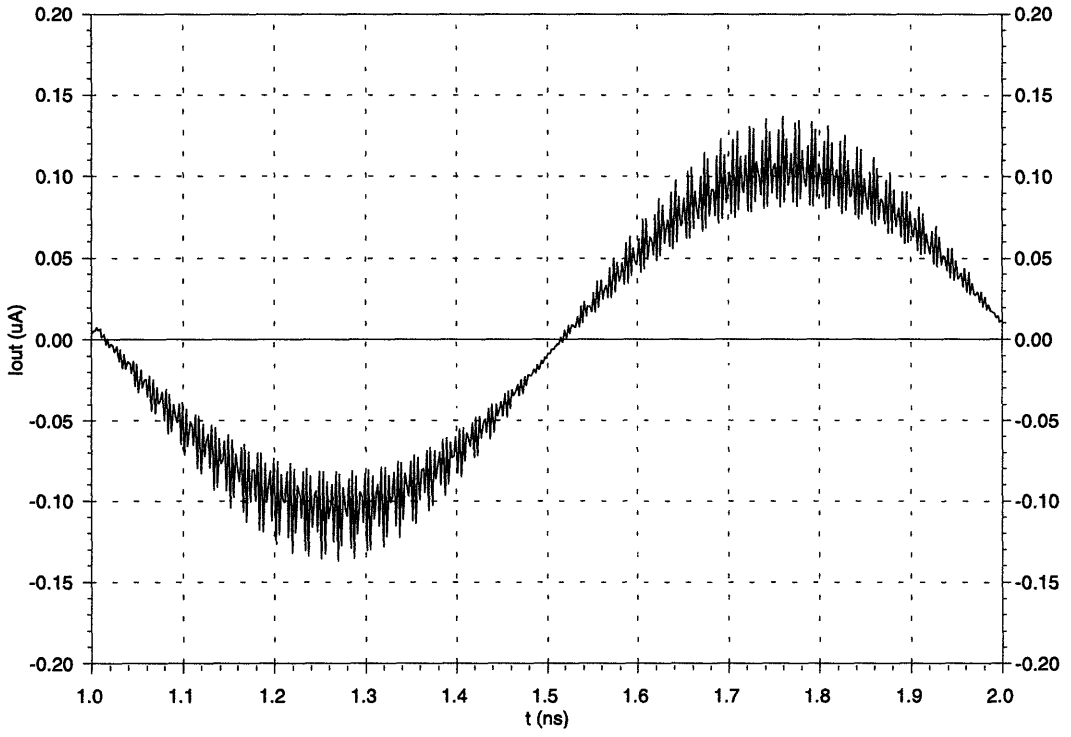

Figure 2.17 - Simulated hold-mode performance of the T/H with a 640 μA p-p, 1 GHz sinusoidal input signal. The output current is low-pass filtered to attenuate the Josephson oscillations. $R_{sh,P} = 0.375\ \Omega$.

This transfer function is unusual in that it consists of a right-half-plane zero and an inversion at dc. The gain and phase curves fitted to the simulated data in 2.18 are based on this expression with $\alpha_{1,sim}$ = 325 μA/A and $\tau_{hold,sim}$ = 18.1 ps.

The simulations show that the current admitted by the T/H in hold mode can be attributed to a frequency-independent portion, proportional to $-\alpha_{1,sim}$, in parallel with a frequency-dependent part, proportional to $\alpha_{1,sim}\tau_{hold,sim}s$. The latter component is well described by the calculations based on the linearized hold-mode model of the T/H. Since the $\alpha_{1,sim}\tau_{hold,sim}$ product (5.9 fs) and the $\alpha_1\tau_{hold}$ product (8.2 fs) are comparable in magnitude, the calculated and simulated curves are nearly coincident for $\omega > \tau_{hold,sim}^{-1}$.

The source of the frequency-independent part of the simulated hold-mode

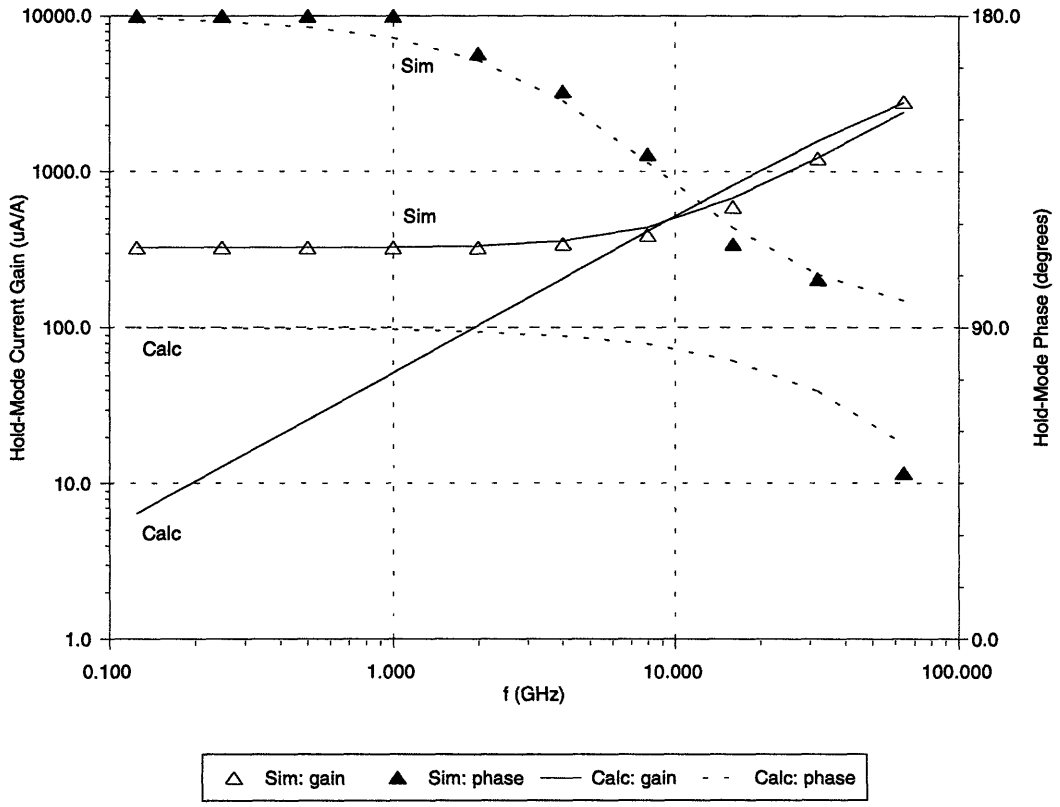

Figure 2.18 - Simulated and calculated hold-mode transfer functions of the T/H ($R_{sh,P}$ = 0.375 Ω). The gain (log-log) and phase (semi-log) are plotted vs. frequency. The open and filled triangles show the simulated gain and phase, respectively. The solid lines and broken curves show the gains and phases, respectively, obtained by calculation (Calc) or by fitting first-order curves to the simulated data (Sim).

isolation is not clear, however. The linearized hold-mode circuit shows no direct dc path between the input and output of the T/H, and the sign of this term is incorrect for simple feedthrough. It is present in sinusoidal simulations down to 10 MHz and appears as a small step aberration in pulse simulations. Numerical error cannot be ruled out, although the simulated hold-mode gain is independent of input signal amplitude, component mismatches, and numerical convergence tolerances, and is only weakly dependent on the current overdrive of the series and parallel junctions. The JSIM junction model, because of the discontinuous conductance which results from the non-physical piecewise-linear *I-V* curve, is also suspect.

Examination on a fast time scale of the raw simulation data used to create Fig. 2.17 shows that the fast Josephson oscillations are amplitude-modulated by the slower, 1 GHz input current. The junctions in the bridge may in fact allow parametric modulation of the output current by a complex nonlinear mechanism that cannot be described by the simple linear circuit model. If the input current modulates a process that takes place at a fixed frequency on the order of the Josephson oscillation frequency, the frequency-independent part of the hold-mode isolation might be attributed to the higher transmission of the bridge in that frequency range. However, further study of this phenomenon is not warranted since the simulated low-frequency coupling between input and output is very weak.

2.4.6 - Acquisition Dynamics and Sampling Rate

The acquisition time of a T/H is intimately related to its maximum sampling rate. As shown earlier, the acquisition time of the Josephson junction bridge T/H is dominated by the linear settling time, so its acquisition time should be closely related to its tracking bandwidth as well.

Fig. 2.19 shows the transient response of a typical Josephson junction bridge T/H ($R_{sh,P}$ = 0.5 Ω), initially holding a +320 μA output current, as it switches from hold mode

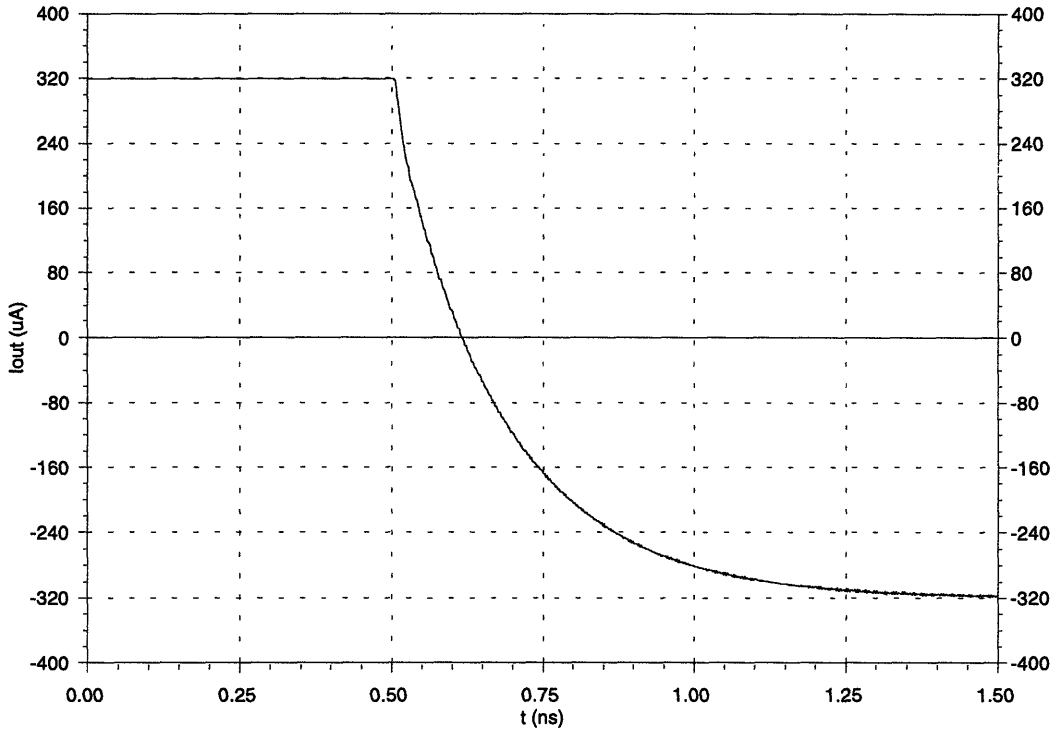

Figure 2.19 - Simulated +320 μA to –320 μA acquisition transient of the T/H. The clock, which has a rise time of 5 ps, switches from hold mode to track mode at 0.5 ns. $R_{sh,P} = 0.5\ \Omega$.

to track mode while a –320 μA dc current is applied to its input. The resulting –640 μA swing corresponds to the negative of the full-scale input range of a T/H designed to have 5-bit resolution, since the LSB size is 20 μA. Once again, small oscillations in the output current are visible. The 5-ps clock used for the simulation is extremely fast by semiconductor standards, but it still affects the bridge turn-on time because its rise time is comparable to $\tau_{S\rightarrow R} \approx 4$ ps. The bridge turn-on time, which is approximately equal to the delay from the start of the clock transition to the time the output slew rate reaches its maximum value, is under 8 ps. The linear acquisition transient is first-order, as expected, with a 90% to 10% fall time of 500 ps; the output settles to within 1 LSB of final value in about 630 ps. Since the bridge is symmetric, the 10% to 90% rise time is also 395 ps.

In order to compare the simulated acquisition dynamics to the calculated dynamics, it is useful define the acquisition bandwidth in terms of the 10% to 90% linear acquisition rise time:

$$\omega_{acq} = 2\pi f_{acq} \equiv \frac{\ln 9}{\tau_{r,acq}} \approx \frac{2.2}{\tau_{r,acq}} \tag{2.84}$$

The acquisition rise time, $\tau_{r,acq}$, can be determined from a time-domain simulation of the T/H, as above, or deduced experimentally. The theoretical acquisition rise time for a first-order system is easily calculated, giving:

$$t_{r,acq} = (\ln 9)\tau_{track} \approx 2.2\tau_{track} \tag{2.85}$$

In the ideal first-order case, the acquisition bandwidth is equal to the half-power tracking bandwidth. In general, the acquisition bandwidth is a good estimate of the tracking bandwidth if the acquisition transient is predominantly linear first-order or linear second-order.

Fig. 2.20 shows the simulated acquisition bandwidth of the T/H for numerous values of $R_{sh,P}$; the calculated acquisition bandwidth, which is the same as the tracking bandwidth, is shown for comparison. The output swing was kept constant at 640 μA for all simulations, even though I_{range} might be greater for small values of $R_{sh,P}$. All of the simulated acquisition transients were well behaved and first-order. The simulated acquisition bandwidth is in good agreement with the calculated acquisition bandwidth, also shown in Fig. 2.20, which is calculated with the extrinsic normal-state resistance of the parallel junctions approximated by $R_{J,P} \approx r_{oe,P}$.

Fig. 2.21 shows the simulated and calculated acquisition times as well as the simulated and calculated maximum sampling rates. Since all of the simulations whose data contributed to Fig. 2.21 were conducted with the same 640 μA output swing, the

acquisition times represent settling to 5-bit accuracy. Once again, the agreement between the simulations and calculations is good. The sampling rate shown in Fig. 2.21 is the worst case imposed by a 50% clock duty cycle. Since the bridge turn-on and hold-mode settling times are very short compared to the linear acquisition time, the best-case sampling rate is nearly a factor of two better than the sampling rate indicated in Fig. 2.21 if the clock rise time is sufficiently short.

2.4.7 - Sampling Bandwidth and Effective Bit-Resolution

The preceding simulations have demonstrated the basic functionality of the T/H and have revealed most of its key specifications. The following simulations are most similar to the actual type of application for which the T/H is intended — high-speed

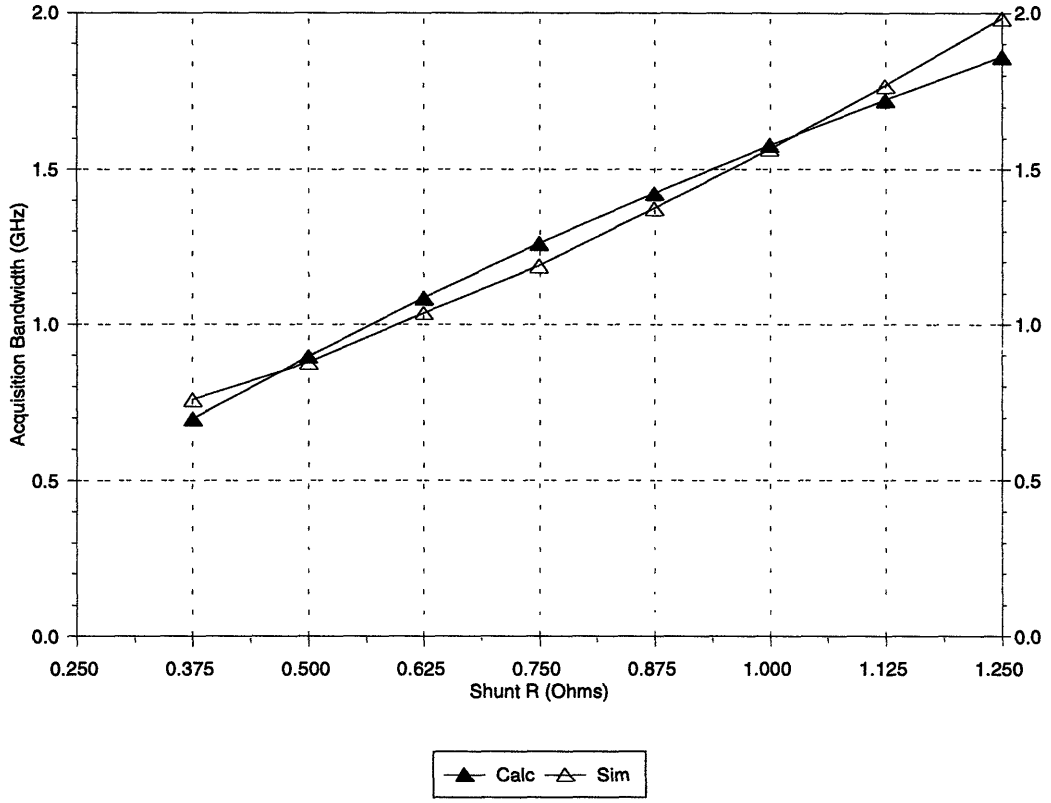

Figure 2.20 - Simulated and calculated acquisition bandwidths of the T/H vs. parallel junction shunt resistance. The filled triangles show the calculated acquisition bandwidth, $f_{acq,calc} = f_{track}$. The empty triangles show the acquisition bandwidth extracted from time-domain simulations with a 5-ps clock rise time.

sampling of a fast input signal. To facilitate the direct comparison of the last few key specifications of the T/H over a range of $R_{sh,P}$ values, a 640 μA peak-to-peak sine is selected as the largest input signal applied to the T/H. Although for small values of $R_{sh,P}$ the T/H might otherwise achieve a higher input signal range and a wider dynamic range, this choice of input signal amplitude limits the maximum dynamic range to 5 bits for all choices of shunt resistance.

Fig. 2.22 shows the results of a beat-frequency simulation performed on the T/H with $R_{sh,P}$ = 0.375 Ω. By choosing super Nyquist sampling, where the sampling rate is less than twice the input frequency, frequencies beyond the half-power bandwidth of the T/H can be used without requiring the track time to be less than the acquisition time.

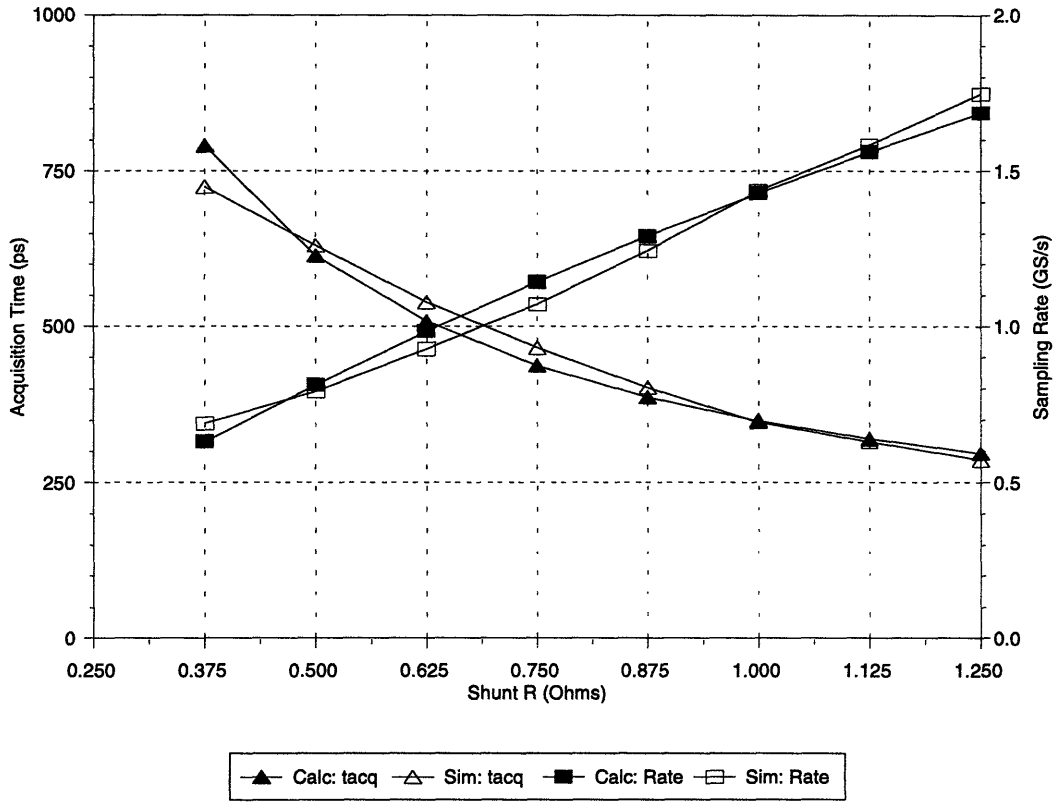

Figure 2.21 - Simulated and calculated acquisition times and sampling rates of the T/H vs. parallel junction shunt resistance. The triangles show the total acquisition time to less than 1 LSB (20 μA) error with a 640 μA change in held current and a 5 ps clock rise time. The squares show the resulting maximum sampling rate, assuming the worst case of 50% sampling clock duty cycle.

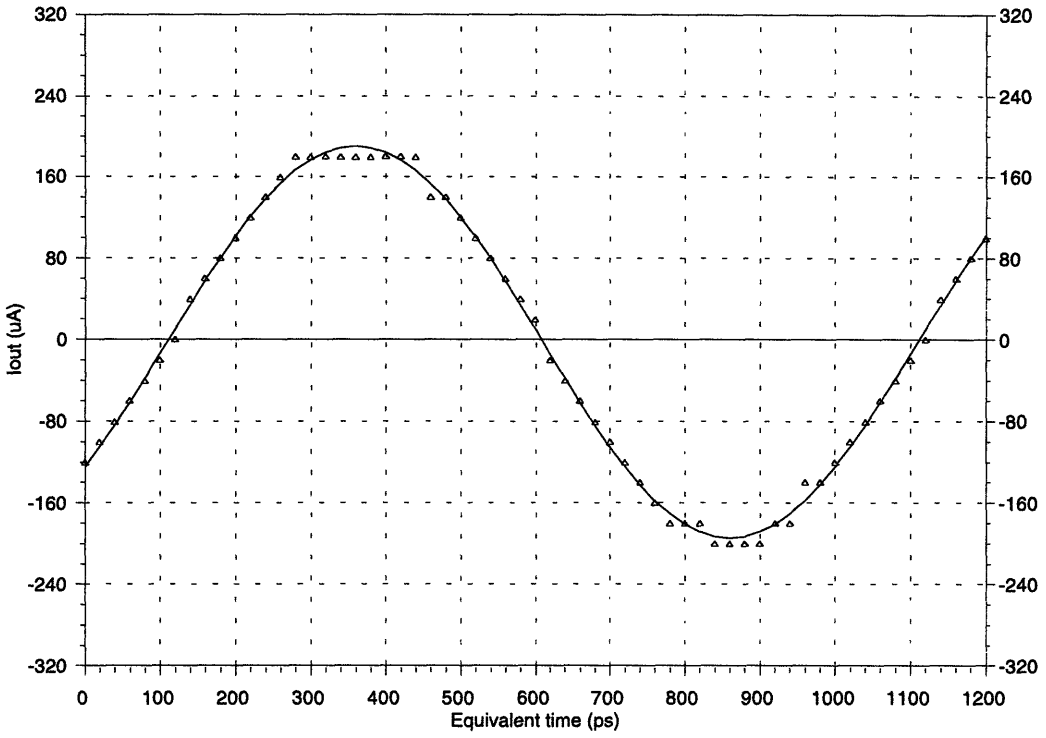

Figure 2.22 - Simulated beat-frequency sampling performance of the T/H ($R_{sh,P}$ = 0.375 Ω) with a 1 GHz, 640 μA p-p, sinusoidal input. The output samples are shown as triangles; the solid curve is an offset sine, fitted to the sampled data so as to minimize the rms error. The data are extracted from time-domain simulations with 1389 ps track time, 581 ps hold time, and 25 ps clock rise and fall times. The total sampling period is 2.02 ns, corresponding to an approximate sampling rate of 495 MS/s.

Although aliasing is deliberately exploited by the super Nyquist technique, it is not detrimental because the spectrum of the input is narrow. The sampling period, 2.02 ns, differs from the closest integer number of periods of the input sine, 2 ns, by 20 ps, so samples taken on successive clock cycles are equivalent to samples taken at 20 ps intervals along one period of the repetitive input signal. These samples are plotted vs. the equivalent time in Fig. 2.22.

A 1 GHz sine, also shown in Fig. 2.22, is numerically fit to the samples using an algorithm that minimizes the least-square error by choosing values for three free parameters — phase, amplitude, and dc offset. The value of the phase is unimportant, but

the dc offset is less than 1/8 LSB. The amplitude of the fitted sine is considerably less than that of the input signal because the input frequency exceeds the half-power bandwidth of the T/H.

The input signal used for the simulation in Fig. 2.22 is about half the full-scale input, I_{FS}, of the T/H with $R_{sh,P}$ = 0.375 Ω. The quasi-static sampling curve, Fig. 2.10, predicts that the T/H can accurately sample input currents whose amplitudes are restricted to this range. As expected, Fig. 2.22 shows that the samples generally lie within 1 LSB of the fitted curve, approaching the theoretical quantization noise limit. Assuming that the magnitude of the quantization error is a random variable whose distribution is uniform from 0 to 1 LSB, the rms quantization noise of an ideal N-bit quantizer is given by:

$$QN_{rms} = \frac{q}{\sqrt{12}} \tag{2.86}$$

where q is the size of 1 LSB, 20 μA in this case. The T/H is a non-ideal quantizer, so its total rms sampling error includes sampling errors due to the imperfect operation of the circuit (e.g. nonlinearity and missing codes) in addition to the fundamental quantization noise. The total rms error for the simulation shown in Fig. 2.22 is 6.71 μA, compared to the best-case quantization noise limit of 5.77 μA.

Fig. 2.23 shows the results of a 1 GHz, 495 MS/s beat-frequency simulation performed on the T/H with a larger parallel junction shunt resistance, $R_{sh,P}$ = 1.125 Ω. The increase in $R_{sh,P}$ yields a higher half-power tracking bandwidth, and hence a larger output signal. However, the rms sampling error also increases, particularly near the peaks of the sine wave, since the increase in $R_{sh,P}$ brings with it an undesirable decrease in I_{FS}. The total rms error for this simulation is 14.3 μA.

The sampling half-power bandwidth, f_{samp}, of the T/H is the frequency at which the fundamental component of the output power (i.e., the power of the best-fit sine) falls

to half of its value for low-frequency inputs. It is again convenient to exploit the first-order frequency response of the T/H and employ Eqn. 2.81 to determine f_{samp} in the same fashion as it was used to obtain f_{track} from a small number of time-domain simulations.

Fig. 2.24 shows the simulated half-power sampling bandwidth and the calculated sampling bandwidth, which is the same as the tracking bandwidth, vs. $R_{sh,P}$. Once again, the tracking bandwidth is calculated using the extrinsic normal-state resistance of the parallel junctions approximated by $R_{J,P} \approx r_{oe,P}$. All simulations were conducted using a 320 μA peak, 2 GHz sine input. The input frequency was chosen to be relatively high in order to reduce the amplitude of the output current, thereby mitigating the large-signal

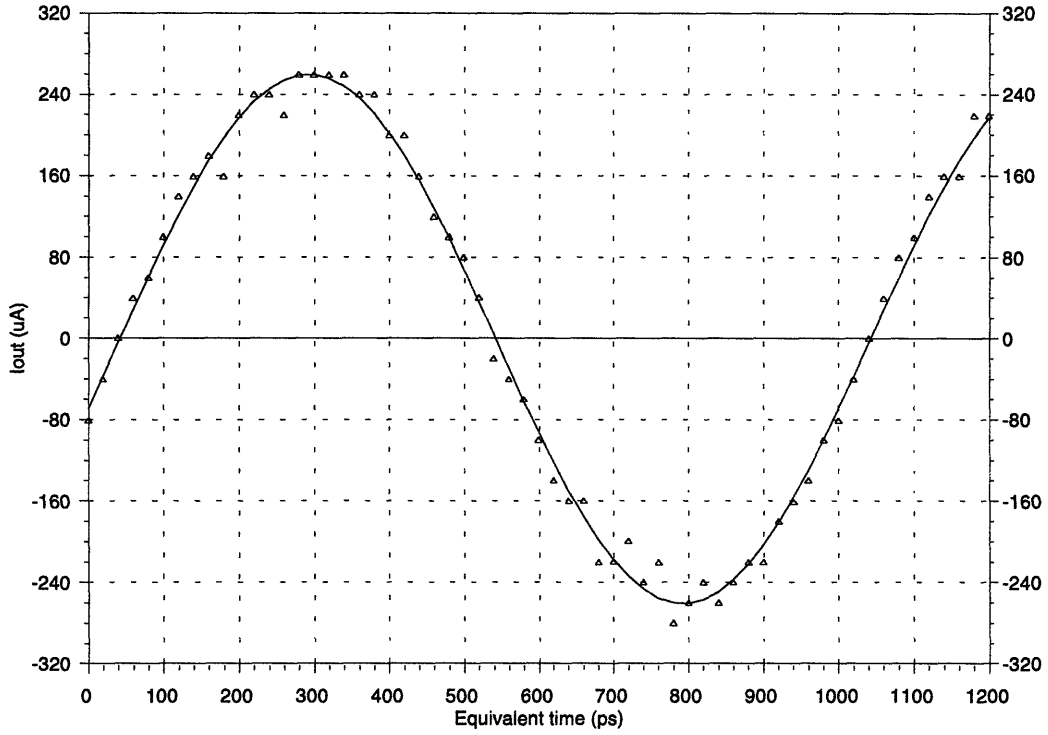

Figure 2.23 - Simulated beat-frequency sampling performance of the T/H ($R_{sh,P}$ = 1.125 Ω) with a 1 GHz, 640 μA p-p, sinusoidal input. The output samples are shown as triangles; the solid curve is an offset sine, fitted to the sampled data so as to minimize the rms error. The data are extracted from time-domain simulations with 1389 ps track time, 581 ps hold time, and 25 ps clock rise and fall times. The total sampling period is 2.02 ns, corresponding to an approximate sampling rate of 495 MS/s.

gain-compression effects that result from the reduced input range observed at large values of $R_{sh,P}$. The agreement between theory and simulation is better than 10% over most of the range of $R_{sh,P}$.

The effective resolution, in bits, is the second key specification of the T/H that can be assessed using beat-frequency simulations. The effective bit-resolution is a function of $R_{sh,P}$, which affects both the signal range and the sampling error. Fixing the maximum attainable resolution of the T/H at 5 bits in the simulations by limiting the full-scale input current to 320 μA moderates the impact of the signal range reduction, but leads to a more insightful comparison between T/H's having differing values of $R_{sh,P}$. The input frequency also influences the number of effective bits since it affects the amplitude of the

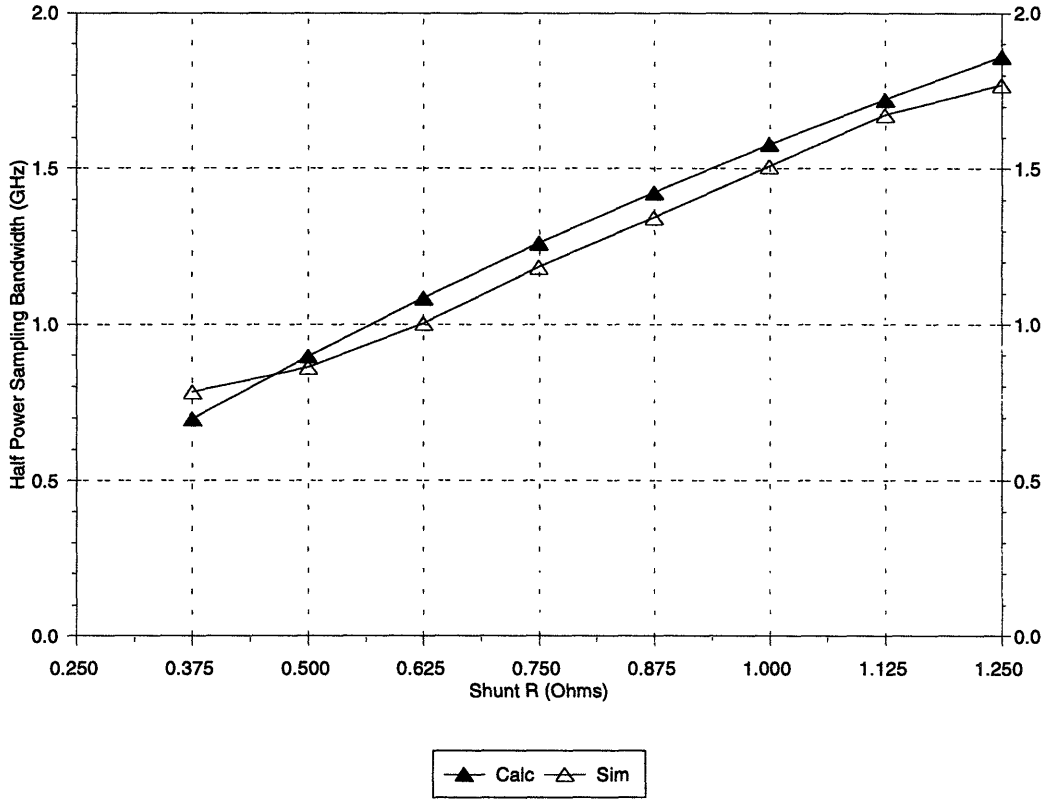

Figure 2.24 - Simulated and calculated sampling bandwidth of the T/H vs. parallel junction shunt resistance. The filled triangles show the calculated sampling bandwidth, $f_{samp} = f_{track}$. The empty triangles show the sampling bandwidth extracted from time-domain simulations with a 2 GHz input frequency and 498 MS/s sampling rate (1382 ps track time, 578 ps hold time, and 25 ps clock rise and fall times).

output, and hence the number of available codes. Dynamic errors may also become more pronounced at high input frequencies.

The rms value of a full-scale sine wave input signal is given by:

$$S_{rms} = \frac{I_{FS}}{\sqrt{2}} = \frac{I_{range}}{2\sqrt{2}} = \frac{2^N q}{2\sqrt{2}} \tag{2.87}$$

where N is the bit-resolution and q is the weight of the LSB, as before. The best signal-to-noise ratio, attained when a full-scale sine is applied to an ideal N-bit quantizer (i.e., one that exhibits only quantization noise), is given by the well-known expression:

$$SNR_{ideal} = \frac{2^N}{\sqrt{1.5}} \approx (6.02N + 1.76)\text{dB} \tag{2.88}$$

The actual *SNR* of a real quantizer with finite bandwidth will be lower than SNR_{ideal}, because the actual noise will be larger than the ideal quantization noise and the output signal may be lower than full-scale. The effective number of bits (*ENOB*) is computed in terms of the observed *SNR* by solving Eqn. 2.88 for N, giving:

$$ENOB \approx \frac{SNR - 1.76\text{dB}}{6.02\text{dB}} \tag{2.89}$$

where the *SNR* is expressed in dB.

Fig. 2.25 shows the simulated *SNR* and *ENOB* of the T/H vs. frequency for several values of $R_{sh,P}$, as well as the curves for an ideal 5-bit quantizer preceded by ideal first-order low-pass filters having either 500 MHz or 1 GHz half-power bandwidths. The signal-to-noise ratio of an ideal quantizer with finite bandwidth should decrease by about 6.02 dB per octave of frequency well beyond the half-power bandwidth, and its effective bit-resolution should decrease by one bit per octave. Both of these effects are

manifestations of the reduced signal power beyond the corner frequency (and constant quantization noise). Although by no means ideal, the T/H with $R_{sh,P}$ = 0.375 Ω, which has a half-power bandwidth of about 0.7 GHz, follows the expected trend. However, the *SNR* and *ENOB* of the other two T/H's shown in Fig. 2.25 are roughly independent of frequency. In these cases, the decreasing signal amplitude at higher input frequencies also reduces the sampling distortion due to the limited input signal range of the T/H with large $R_{sh,P}$.

In order to quantify the effective resolution of the T/H at low input frequencies for a range of $R_{sh,P}$ values, the simulated quasi-static sampling response curves, such as those depicted in Fig. 2.10 and Fig. 2.12, were analyzed again. In each case, a straight line was

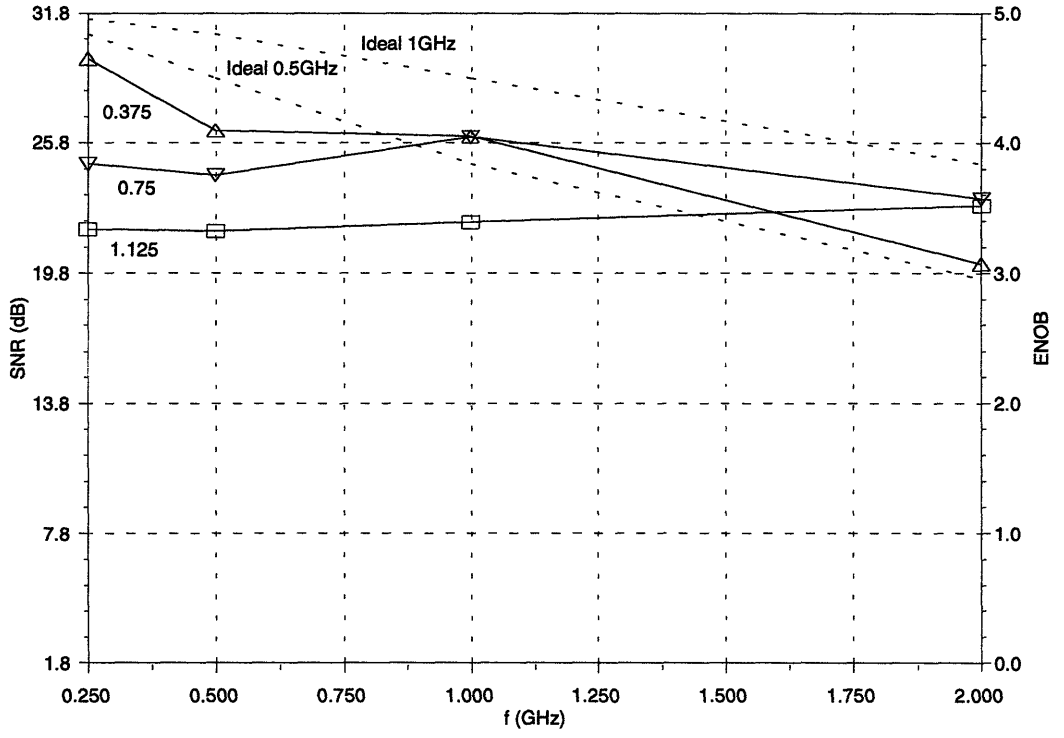

Figure 2.25 - Simulated *SNR* and *ENOB* of the T/H vs. frequency. The Δ's represent the data for $R_{sh,P}$ = 0.375 Ω, the∇'s show the data for $R_{sh,P}$ = 0.750 Ω, and the squares show the data for $R_{sh,P}$ = 1.125 Ω. The two broken curves, labeled Ideal 1 GHz and Ideal 0.5 GHz, are the *SNR* and *ENOB* of ideal 5-bit quantizers preceded by first-order low-pass filters having half-power bandwidths of 500 MHz and 1 GHz, respectively.

fitted to the sampled data over the limited –320 μA to +320 μA range. The fitting algorithm sought the minimum rms error by adjusting the gain and offset of the straight line.

Fig. 2.26 shows the simulated rms quasi-static sampling error of the T/H vs. $R_{sh,P}$, obtained by the aforementioned method. The deviation of the best-fit gains from unity was 1.8% at $R_{sh,P}$ = 0.375 Ω, less than 3.5% for $R_{sh,P} \leq 1$ Ω, and less than 8% for all values of $R_{sh,P}$. The figure also shows three horizontal reference lines representing the rms quantization noise limits, QN_{rms}, at 3-bit, 4-bit, and 5-bit resolutions, assuming a 640 μA full-scale input range. The theoretical quantization noise, given by Eqn. 2.86, is 5.77 μA rms at 5-bit resolution and doubles with every lost bit of resolution. The *ENOB* can

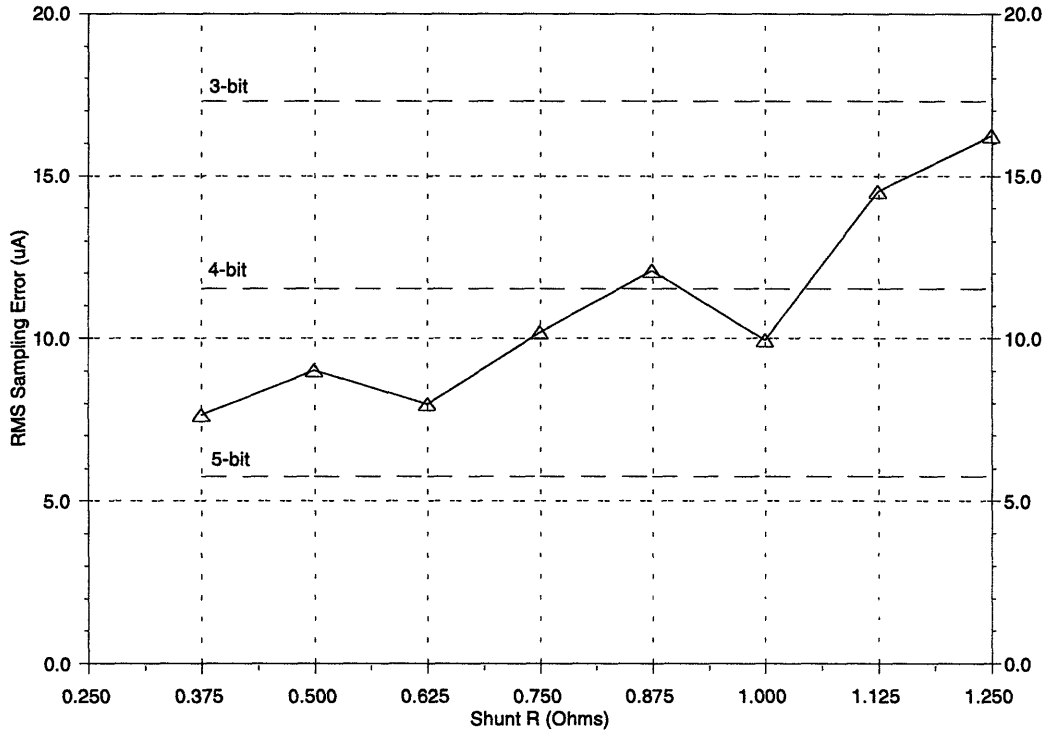

Figure 2.26 - Simulated rms quasi-static sampling error of the T/H vs. $R_{sh,P}$. The simulated data is taken from time-domain simulations with slow ramp inputs and a clock with a 675 ps track time, 275 ps hold time, and 25 ps rise and fall times. Also shown are the quantization noise limits for I_{range} = 640 μA at 3-bit, 4-bit, and 5-bit resolutions.

be expressed in terms of the rms sampling error as:

$$ENOB \approx N - \log_2\left(\frac{SN_{rms}}{QN_{rms}}\right) \tag{2.90}$$

where N is the ideal bit-resolution of the T/H, SN_{rms} is the actual rms sampling noise, and QN_{rms} is the theoretical quantization noise at N-bit resolution. The low-frequency *ENOB* of the T/H, computed using Eqn. 2.90, is as high as 4.6 bits for $R_{sh,P}$ = 0.375 Ω, and is between 4 bits and 5 bits for $R_{sh,P} \leq 1$ Ω. For larger values of parallel junction shunt resistance, the *ENOB* falls off because of the shrinking I_{range} and increasing large-signal distortion. These results concur with the *ENOB* vs. frequency results presented in Fig. 2.25.

2.5 - Target Specifications

As mentioned in the previous section, a very cautious design philosophy was adopted in choosing the component values in implementation of the T/H because the Josephson junction bridge T/H is the first circuit of its type. Another factor that influenced this philosophy is the relatively wide uncertainty of the key process specifications, especially the critical current and the contact resistance of the resistors (i.e., that due to the metallurgical contact between the normal metal resistors and its superconducting leads). Moreover, a conservative design, which maximizes neither speed nor resolution, facilitates testing as well as fabrication.

Fig. 2.27 shows the complete implementation of the Josephson junction bridge T/H. All of the junctions are shunted by external resistors. This circuit, rather than one containing ideal current sources, was actually used for all of the simulations of the preceding section. The bias, clock, and input current sources are implemented using voltage sources and resistors. The two clock currents, I_{Ka} and I_{Kb}, are generated from a

single clock voltage, V_K, to guarantee their synchronization. Due to the low impedance levels of the shunted junctions, the clock resistors, $R_{Ka} = R_{Kb} = 100\ \Omega$, can be selected to match the 50 Ω clock transmission line and still act as relatively high-impedance current sources. The input to the T/H is composed of two complementary voltage sources rather than a floating current source. The input resistors, $R_{ina} = R_{inb} = 50\ \Omega$, are also large compared to the junction impedances. The four bias currents are also implemented as resistors (R_{B1a}, R_{B2a}, R_{B1b}, R_{B2b}) in series with voltage sources (V_{Ba}, V_{Bb}). Although the bias currents are nominally equal, using two voltage sources allows one to null the dc offset of the T/H.

It is clear from the simulations and calculations of the preceding sections that the shunt resistance of the parallel junctions, $R_{sh,P}$, is the most important degree of freedom in

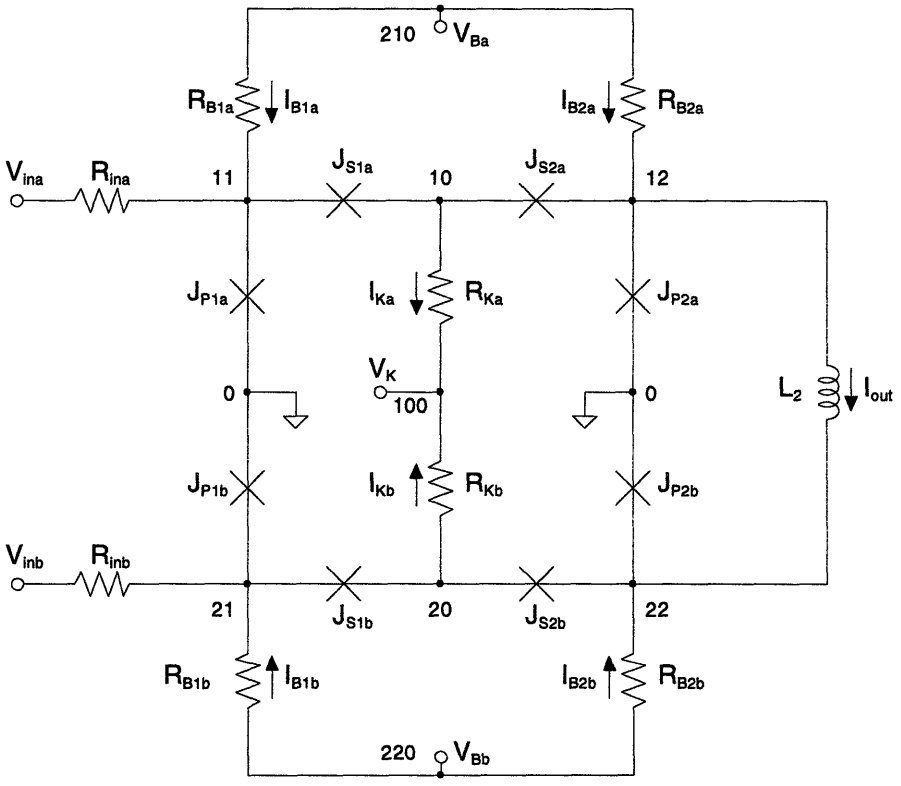

Figure 2.27 - Complete implementation of the Josephson junction bridge T/H. Current sources are implemented as resistors and voltage sources; the input is implemented as two sources.

the implementation of the T/H. Lower values of $R_{sh,P}$ favor a wider input signal range at the expense of speed, while higher values yield higher speed in exchange for reduced signal range and poorer output signal fidelity. While I_{range} depends only on the square root of the critical current and the capacitance of the parallel junctions, it depends almost linearly on $R_{sh,P}$.

Unfortunately, even the largest value of $R_{sh,P}$ for which the T/H was extensively simulated, 1.25 Ω, requires a resistor with a sub-square aspect ratio. The shunt resistors must be made as short as possible in order to achieve such small resistances with a minimum of parasitic capacitance and wiring inductance. Unfortunately, the resistance variation, as a fraction of the total resistance, due to any fixed bias between the drawn length of the resistor and its actual length, increases as the resistor is made shorter. In addition, the fractional contribution of the contact resistance, which can be modeled to first order as an excess in the effective length of the resistor, also grows as the resistor becomes shorter. Furthermore, the resistors in the Lincoln process were not well characterized in the sub-square regime at the time of the design.

Consequently, the nominal value of $R_{sh,P}$ was chosen to be the smallest value studied in the simulations of the T/H, 0.375 Ω. This choice results in an input signal range, I_{range}, that exceeds 640 μA at the target critical current density and better than 4 effective bits of resolution at low frequency, even if the shunt resistors are more than two times larger than the nominal value. The layout of the hold inductor, L_2, is similar to an earlier design whose inductance is well known, and its value is relatively large compared to the anticipated parasitic inductances. Therefore, the actual value of L_2, and consequently the value of the step size, I_{step}, should be close to the target values. The extra available input signal range above 640 μA allows the T/H to achieve nominal 5-bit resolution even if the critical current falls below its target value of J_c = 1000 A/cm^2. By

Table 2.2 - Nominal Josephson Junction Bridge T/H Component Values

Parameter	Value	Parameter	Value
$I_{c,P}$	640 μA	$I_{c,S}$	960 μA
I_B	960 μA	I_{Ka}, I_{Kb}	1.92 mA
$R_{sh,P}$	375 mΩ	$R_{sh,S}$	625 mΩ
R_B	100 Ω	R_{Ka}, R_{Kb}	100 Ω
R_{ina}, R_{inb}	50 Ω	L_2	102.5 pH

heavily shunting the parallel junctions, the T/H will also be tolerant to parasitic capacitance which could further reduce I_{range} by increasing β_{oe} of the parallel junctions.

Table 2.2 summarizes the nominal component values of the final Josephson junction bridge T/H design. The bias current, I_B, is trimmed at the time of test to barely exceed the largest of the series junction critical currents, $I_{c,S}$. The bias, clock, and input resistances do not include the source impedances of the external voltage sources. Since these resistors are much longer than they are wide, the contact resistance is negligible. The total hold inductance, L_2, includes the parasitic inductance and the inductance of the readout circuit's transformer primary.

Table 2.3 lists the important calculated and simulated specifications of the T/H obtained at the nominal critical current, shunt resistance, and hold inductance. The T/H is specified for operation over an input signal range extending from –320 μA - +320 μA, although the maximum full-scale input allows a much wider range (at the expense of increased sampling errors). The extrinsic normal-state resistance of the parallel junctions is taken to be $R_{J,P} \approx r_{oe,P}$ to obtain the calculated bandwidths. The maximum sampling rate is computed assuming a 50% clock duty cycle. With the exception of the hold-mode isolation, the simulations agree well with the calculations.

Table 2.3 - Nominal Calculated and Simulated Performance of the Josephson Junction Bridge T/H

Parameter	Calculated Value	Simulated Value
Maximum full-scale input current	I_{FS} = 640 μA	I_{FS} = 585 μA
Operating input current range	–320 μA - +320 μA	–320 μA - +320 μA
Current step size (LSB weight)	I_{step} = 20.0 μA	I_{step} = 20.0 μA
Nominal resolution	N = 5 bits	N = 5 bits
Effective dc resolution	*ENOB* (dc) = 5.0 bits	*ENOB* (dc) = 4.6 bits
Tracking half-power bandwidth	f_{track} = 700 MHz	f_{track} = 750 MHz
Tracking error coefficient	e_1 = 227 ps	e_1 = 220 ps
Acquisition time (5-bits)	790 ps	725 ps
Maximum sampling rate (5-bits)	633 MS/s	690 MS/s
Sampling half-power bandwidth	f_{samp} = 700 MHz	f_{samp} = 785 MHz
Effective resolution (1 GHz)	*ENOB* = 4.2 bits	*ENOB* = 4.1 bits
Hold time	∞	∞
Hold-mode gain (1 GHz)	$a_{i,hold}$ = 52 μA/A	$a_{i,hold}$ = –325 μA/A

2.6 - Readout

The T/H provides an output signal in the form of a current in a large hold inductor. To couple to the next stage of superconducting electronics, a small transformer is inserted in series with the hold inductor. In a high-speed application, the secondary of the transformer could be tied to the input of an A/D converter, current comparator, or other signal processing subsystem. However, for the purpose of validating the operation of the T/H, the secondary of the readout transformer forms part of the loop inductance of a dc Superconducting Quantum Interference Device (SQUID), a highly sensitive detector of magnetic flux. In order to obtain the desired high accuracy (at the expense of speed), the SQUID is configured in a flux-locked loop [33].

Fig. 2.28 shows a symmetric dc SQUID with the inputs and outputs needed for its incorporation into a flux-locked loop. The SQUID consists of two Josephson junctions (J_{11}, J_{12}) with equal critical currents ($I_{c11} = I_{c12}$) and some loop inductance, $L_{loop} = L_{11b} + L_{12a}$. A bias current ($I_{bias}$) delivered by a resistor (R_{bias}) drives the SQUID at the midpoint of the loop inductance so that $L_{11b} = L_{12a}$. The output voltage is monitored at the same point. Magnetic flux is coupled into the loop via the two mutual inductances (M_{11}, M_{12}). The total flux, Φ, is given by the sum:

$$\Phi = \Phi_{T/H} + \Phi_{ext} = M_{11} I_{out} + M_{12} I_{ext} \tag{2.91}$$

where $\Phi_{T/H}$ is the flux from the T/H applied via M_{11}, Φ_{ext} is the external flux applied via M_{12}, I_{out} is the output current of the T/H, and I_{ext} is the current supplied by the external electronics. The external flux is supplied by the sum of three external currents, and is given by:

$$\Phi_{ext} = \Phi_{fb} + \Phi_B + \Phi_{ac} = M_{12} I_{ext} = M_{12} (I_{\Phi fb} + I_{\Phi B} + I_{\Phi ac}) \tag{2.92}$$

where $I_{\Phi fb}$ is a dc feedback current and Φ_{fb} is the associated feedback flux, $I_{\Phi B}$ is a dc

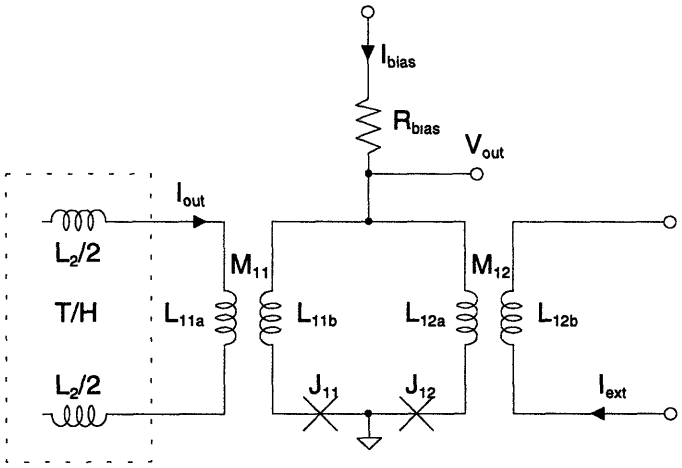

Figure 2.28 - Schematic of the dc SQUID that serves as the readout circuit of the T/H.

current which supports the dc flux bias, Φ_B, and $I_{\Phi ac}$ is a small sinusoidal current at frequency $f_{\Phi ac}$ which generates the ac drive flux, Φ_{ac}.

As a result of the quantum interference in the loop, the total critical current of the SQUID, I_C, is a periodic function of the magnetic flux; its period is exactly Φ_o. When $\Phi = n\Phi_o$, where n is an integer, $I_C(\Phi)$ reaches its maximum value, which is simply the sum of the critical currents of the two junctions:

$$I_C|_{\max} = I_{c11} + I_{c12} \tag{2.93}$$

For a symmetric SQUID, the minima of $I_C(\Phi)$ lie midway between the maxima. The depth of modulation, $\Delta I_C = I_C|_{max} - I_C|_{min}$, measures the extent to which the critical current of the SQUID can be modulated by the external flux. The fractional depth of modulation, $\Delta I_C / I_C|_{max}$, decreases smoothly from unity and approaches a limiting value of zero as the SQUID's loop inductance is increased from zero. On the other hand, the absolute depth of modulation, ΔI_C, is a monotonically increasing function of I_C. The universal depth of modulation curve, which is determined numerically, increases from 0 to an asymptotic value of Φ_o/L_{loop} as a function of the SQUID's inductance parameter, $\beta_L = 2\pi L_{loop} I_C/\Phi_o$. In the vicinity of $\beta_L \approx 2\pi$, the depth of modulation is approximately given by [1]:

$$\Delta I_C \approx \frac{\Phi_o}{2L_{loop}} \tag{2.94}$$

The Josephson junctions must have non-hysteretic *I-V* curves for proper operation of the dc SQUID; in most tunnel junction processes external shunt resistors are required. Fig. 2.29a shows the typical variation of critical current as a function of Φ. Fig. 2.29b shows the resulting time-average *I-V* curves at the extremes of modulation. The separation of the curves is due to the ac Josephson oscillation current circulating in the loop. The *I-V* curves merge near the dc voltage at which this current begins to be

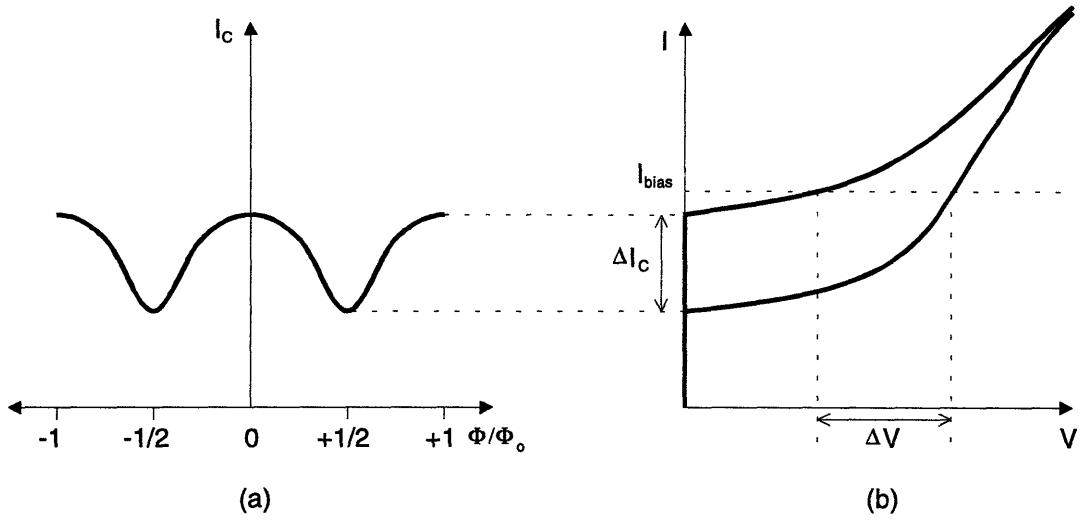

Figure 2.29 - Modulation of the dc SQUID's critical current and *I-V* curve by a magnetic flux. (a) Critical current vs. flux. (b) *I-V* curves. This figure, from [33], illustrates the maximum modulation.

attenuated; this voltage is that at which ω_J approaches the corner frequency of the loop impedance [33]:

$$V_{merge} \approx \frac{\Phi_o r_{oe}}{\pi L_{loop}} \tag{2.95}$$

where r_{oe} is the extrinsic small-signal resistance of one of the junctions.

If a dc bias current, I_{bias}, is applied to the SQUID, the output voltage will also be a periodic function of Φ. This voltage is the signal that is measured when the SQUID is placed in a flux-locked loop. When the critical current of the SQUID is at a minimum, the output voltage is at a maximum. If the bias current is chosen such that the SQUID's output voltage is always less than V_{merge}, the voltage at which the I-V curves become indistinct, the voltage modulation will be proportional to the critical current modulation, to first order:

$$\Delta V \approx \frac{r_{oe}}{2} \Delta I_C \tag{2.96}$$

It can be shown that $\beta_L \approx 2\pi$ is a good compromise between two effects which act to reduce ΔV — the reduced depth of modulation at low β_L and the lower shunt resistance needed to keep the junctions non-hysteretic at high β_L [33].

By modulating the critical current of the SQUID's junctions, the ac drive flux, Φ_{ac}, stimulates an ac output voltage which can be detected using a synchronous detector, such as a lock-in amplifier. The amplitude and spectrum of the ac output voltage depend on the dc flux operating point of the SQUID, Φ_{dc}, which is given by:

$$\Phi_{dc} = \Phi_{fb} + \Phi_B + \Phi_{T/H} = M_{12}(I_{\Phi fb} + I_{\Phi B}) + M_{11}I_{out} \tag{2.97}$$

The dependence of the output voltage on Φ_{dc} is best illustrated by two examples. Fig. 2.30a shows the output voltage waveform that results from the ac drive flux when the total dc flux is such that the SQUID is biased at a minimum of the V-Φ transfer characteristic. In the vicinity of the null, the V-Φ curve is even symmetric, so the output voltage is a rectified version of the ac flux drive. Therefore, the dominant component of the output voltage is at $2f_{\Phi ac}$ and the component at $f_{\Phi ac}$ is at its minimum. Fig. 2.30b shows the output voltage waveform that results when the total dc flux is such that the

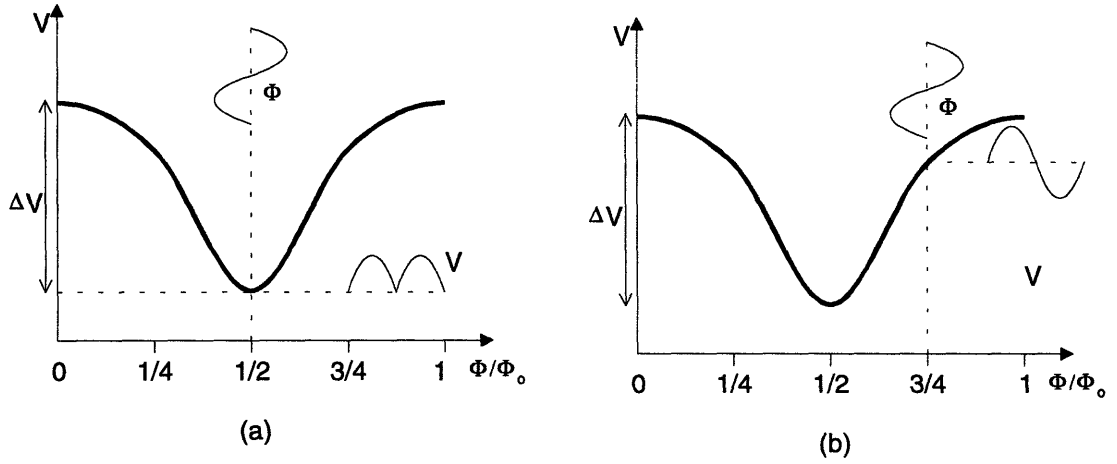

Figure 2.30 - Schematic SQUID voltage waveforms resulting from a small ac flux at differing dc fluxes. (a) $\Phi_{dc} = (n + 1/2)\Phi_o$. (b) $\Phi_{dc} = (n + 3/4)\Phi_o$. The figures are from [33].

SQUID is biased where the V-Φ transfer characteristic is nearly linear. In this case, the V-Φ curve is odd symmetric about the bias point, and the fundamental component of the output voltage at $f_{\Phi ac}$ is close to its maximum value.

In order to derive an analytic model of the SQUID, the nonlinearity of its V-Φ curve can be approximated as piecewise linear, as in [33], or as parabolic near its null. Using the latter approximation and taking $M_{11} = M_{12}$ gives:

$$V \approx K_0(\Phi - \Phi_{null})^2 = K_1(I - I_{null})^2 \tag{2.98}$$

where Φ and I are the flux and current applied to the SQUID, Φ_{null} and I_{null} are the flux and current needed bias the SQUID at its minimum voltage, and the scale factors are related by $K_1 = M_{11}K_0$. The total current can be written as the sum of ac and dc components:

$$I = I_{\Phi ac} \sin 2\pi f_{\Phi ac} + (I_{\Phi fb} + I_{out} + I_{\Phi B}) \tag{2.99}$$

where $I_{\Phi ac}$ is the peak amplitude of the ac flux bias current.

If $I_{\Phi B} = I_{null}$, so that the SQUID is biased near a null in its V-Φ curve, the output voltage of the SQUID is approximately given by:

$$V \approx K_1(I_{\Phi ac} \sin 2\pi f_{\Phi ac} + I_{\Phi fb} + I_{out})^2 \tag{2.100}$$

This voltage contains components at dc, $f_{\Phi ac}$, and $2f_{\Phi ac}$. The lock-in amplifier demodulates and measures the component at $f_{\Phi ac}$, which is given by:

$$V(f_{\Phi ac}) \approx 2K_1 I_{\Phi ac}(I_{\Phi fb} + I_{out}) \sin 2\pi f_{\Phi ac} \tag{2.101}$$

Thus, the SQUID can be modeled as a multiplier for small perturbations about the null. The rms value of the fundamental component of the SQUID's output voltage is given by:

$$V(f_{\Phi ac})|_{rms} \approx \sqrt{2} K_1 I_{\Phi ac} (I_{\Phi fb} + I_{out}) \tag{2.101}$$

The readout SQUID was designed to be tolerant to process variations. The nominal critical currents of the Josephson junctions in the readout SQUID are $I_{c11} = I_{c12} =$ 250 μA. These junctions are shunted with 0.77 Ω resistors to attain a nominal capacitance parameter of $\beta_c = 0.5$. The total loop inductance is approximately $L_{loop} = 4$ pH, giving $\beta_L \approx 6.1$, as desired, and a modulation depth of $I_C = 260$ μA. Since the junctions are heavily shunted, $r_{oe} \approx R_{shunt}$ and the maximum peak-to-peak output voltage is 100 μV, to first order. The mutual inductances are approximately $M_{11} = M_{12} \approx 1$ pH, resulting in a 2 mA period for the SQUID threshold curves. The bias resistor is $R_{bias} = 20$ Ω. The details of the flux-locked loop instrumentation are given in the next chapter.

3 - T/H Implementation and Test

3.1 - DSNAP Josephson Junction Process

The Josephson junction bridge T/H was fabricated at MIT Lincoln Laboratory using the Dual-Dielectric Selective Niobium Anodization Process (DSNAP). A description of the process can be found in [34]. DSNAP is an all-refractory trilayer process that uses a 5-cm diameter silicon wafer as the substrate. The superconducting wires and Josephson junction electrodes are sputtered niobium patterned by reactive ion etching and plasma etching. Thermally evaporated SiO dielectrics patterned by liftoff separate overlying Nb layers. The process also offers palladium-gold resistors patterned by lift-off and thin-film capacitors. DSNAP has a validated minimum feature size of 3.5 μm and better than 1.5 μm mask alignment. The nominal critical current density can be chosen in the range 400 – 4000 A/cm^2.

The DSNAP process requires ten masks to define up to nine physical layers. The ANOD mask determines which portions of a 30 nm Ta layer are anodized, and thus defines the contacts to the superconducting Nb ground plane. Anodized areas grow to a 55 nm thick Ta_2O_5 layer that serves as the dielectric for high-quality parallel-plate capacitors; these capacitors are not required for the present design. The NBTA mask defines the extent of the 150 nm Nb ground plane. Patterned ground plane serves as the bottom plate of the capacitors as well as a flux shield below most superconducting circuits. The ground plane vastly reduces the parasitic inductance of wires that are run over it. The SIO1 mask defines cuts in the 200 nm first dielectric that allow the first metal layer to make contact with the Nb ground plane. The JJ mask demarcates the anodization of the counter electrode of the Nb-AlO_x-Nb trilayer that consists of a 250 nm base electrode, a

~5 nm tunnel barrier, and a 35 nm counter electrode. The anodized counter electrode, which bounds the active area of the junction, is niobium pentoxide.

The TRIL mask defines the islands of trilayer that serve as the Josephson junctions, as well the first wiring layer. The PDAU mask defines the resistor layer, which consists of 100 nm of alloyed Pd-Au and 20 nm of Ti. The nominal sheet resistance of the resistors is ~ 2.5 Ω/□, but the contact resistance is not well characterized. The SIO2 mask defines vias in the 350 nm second dielectric that allow the second metal layer to contact the base electrode, counter electrode, or resistor layers. The CONT mask defines the areas where contact will be made to the base electrode of the trilayer. A base electrode contact results from the intersection of windows in the SIO2, JJ, and CONT masks. The NB2 mask defines the 450 nm second niobium wiring layer. Finally, the TIAU layer defines the titanium-gold pads which are patterned by liftoff.

Fig. 3.1 shows the schematic cross section of three structures in the DSNAP process: a resistor, a ground contact, and a Josephson junction with its associated base electrode contact. The vertical coordinate is greatly exaggerated to elucidate the layer structure. Most circuit elements are fabricated over the ground plane. The specific Josephson junction capacitance, which is simply the capacitance of the trilayer structure,

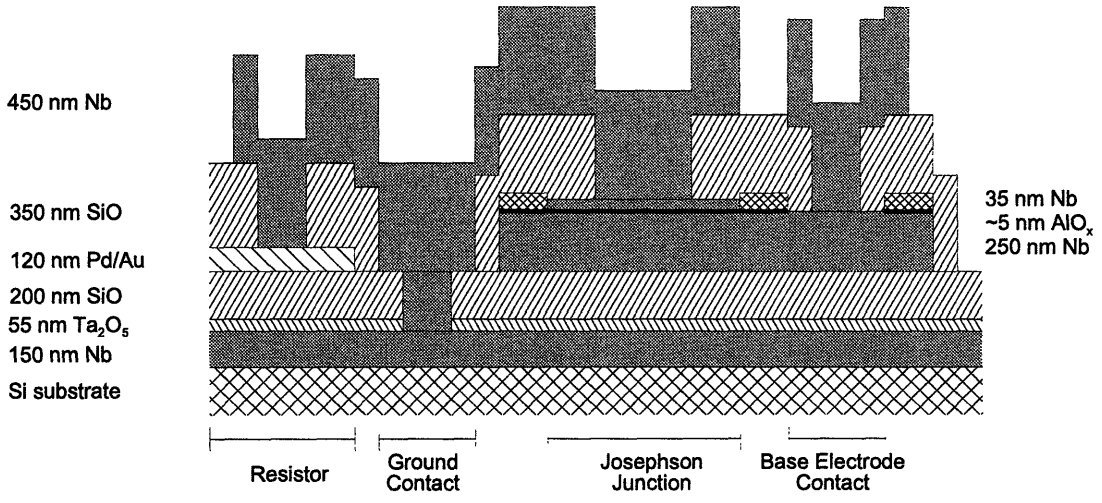

Figure 3.1 - Schematic cross section of the DSNAP process layer structure.

is estimated to be 45 fF/μm^2. The specific capacitance between the first wiring layer and the ground plane is 0.23 fF/μm^2 and the specific capacitance of between the second wiring layer and the ground plane is 0.087 fF/μm^2. Therefore, for typical junction geometry, the intrinsic junction capacitance will dominate the total shunt capacitance of the junction.

The inductance of a superconducting microstrip line consisting of a superconducting line over a superconducting ground plane can be approximated by assuming that most of the magnetic energy is confined to the region between the superconductors, giving [1]:

$$L = \mu_o \kappa \frac{l}{w}\left[h + \lambda_1 \coth\left(\frac{t_1}{\lambda_1}\right) + \lambda_2 \coth\left(\frac{t_2}{\lambda_2}\right)\right] \tag{3.1}$$

where h is the spacing between the superconductors; l, w, t_1, and λ_1 are the length, width, thickness, and penetration depth, respectively, of the superconducting line; t_2 and λ_2 are the thickness and penetration depth of the superconducting ground plane; and κ is a factor of order unity that accounts for the fringe field. In general, κ depends on the geometry of the microstrip and can be calculated to first order using conformal mapping.

Alternatively, a numerical finite element analysis employing an energy-minimization algorithm can be utilized to give a more accurate computation of the inductance that accounts for edge effects [35]. For instance, this type of numerical calculation yields an inductance per unit length for 5 μm wide lines of approximately 82 fH/μm and 132 fH/μm in the first and second wiring layers, respectively. Most wires are routed over the ground plane to minimize the parasitic inductance; trilayer is used for lines that require the lowest inductance. However, since the two wiring layers have non-negligible capacitance to ground, holes in the ground plane must be opened below wires designed to serve as large, low-capacitance inductors.

In the DSNAP process, the standard deviations of the two key process parameters, critical current density and sheet resistance, were approximately 3% across the 5 cm wafer. As was shown earlier, the short-range variations of these parameters directly affect the mismatch errors of the T/H. The uniformity available in the DSNAP process is consistent with about 5-bit accuracy since the current and resistance mismatches across a single chip are expected to be better than across a wafer. Unfortunately, while DSNAP offers adequate local device matching, its wafer to wafer variations are considerably larger. The uncertainty of the absolute critical current is on the order of ±40% and the uncertainty of the absolute sheet resistance is as large as ±20% for large resistors. Moreover, the total resistance of small junction shunt resistors is affected by contact resistance, as noted earlier

3.2 - Chip Layout and Fabrication

The layout of the Josephson junction bridge T/H is contained in one chip of a mask set having 21 usable chips of numerous designs. The T/H die has dimensions of 5.15 mm x 5.15 mm with a 3.95 mm x 3.95 mm usable area. The chip has 24 high-speed pads interleaved with an equal number of ground pads. The chip is designed for flip-chip mounting in an American Cryoprobe BCP-2 high-speed cryogenic probe that provides the 50 Ω transitions between the coplanar waveguides on the chip and the coaxial waveguides that interface with room-temperature test equipment. The probe's two cylindrical μ-metal magnetic shields surround the superconducting chip. The BCP-2 is specified to have less than 3 dB insertion loss at frequencies up to 15 GHz and better than –33 dB worst-case crosstalk between adjacent lines in the 0 - 10 GHz band (better than –27 dB in the 0 - 20 GHz band).

Fig. 3.2 shows a screen capture of the layout of the T/H chip. The chip contains three small T/H cells, located at the corners of the die, that differ only in the size of the

shunt resistors. Each circuit has six dedicated pins: two inputs, two biases, a clock, and an output. In addition, four lines are shared by all three circuits. A SQUID feedback line runs sequentially through the readout circuits of all three T/H's. Also, a SQUID bias line and a signal ground line serve all three T/H's in parallel. The signal ground line provides a clean reference for the external electronics that must measure the small SQUID output voltages.

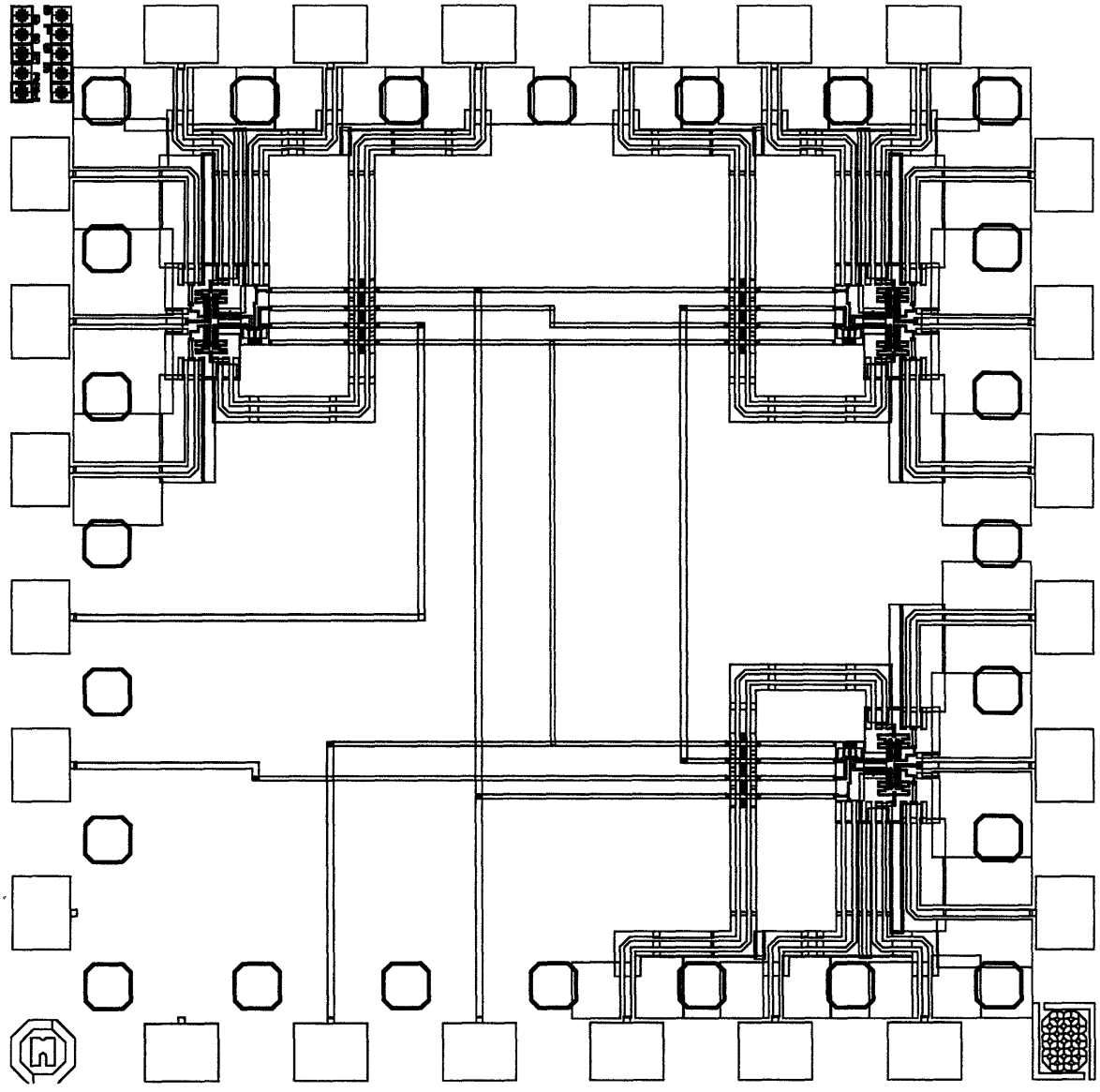

Figure 3.2 - Layout of the T/H chip.

The NOM T/H cell is designed for the nominal process targets of J_c = 1000 A/cm^2 and 2.5 Ω/□ sheet resistance. The HIGH T/H cell is designed for a critical current of J_c = 1400 A/cm^2 or a total resistance 20% higher than desired; its resistors are 20% lower than the nominal resistors. The LOW T/H cell is designed for a critical current of J_c = 600 A/cm^2 or a total resistance 20% lower than desired. The conservative nominal component values chosen for the T/H design notwithstanding, the multiplicity of circuits improves the likelihood that one of the three will operate as desired despite inaccurate modeling and calculations or wide deviations of process parameters from their target values. The resistors in the three designs were chosen so that the fractional return current, I_R/I_c, is close to the target value for at least one of the T/H's. In retrospect, the areas of the junctions should have been scaled as well, so that at least one of the circuits might have close to the desired return current and input signal range.

Fig. 3.3 shows the layout of one of the T/H circuits. The clock is supplied via a 50 Ω coplanar transmission line that meets with two parallel 100 Ω resistors at the left side of the T/H. Similarly, the 50 Ω lines carrying the positive and negative inputs contact the upper left and lower left corners of the T/H and drive their respective 50 Ω input resistors. The bias lines, each of which feeds a pair 100 Ω bias resistors in parallel, are connected to the top and bottom of the T/H. The 50 Ω coplanar lines consist of a 30 μm wide line in a 68 μm wide slot. The 50 Ω and 100 Ω resistors are 5 μm wide. The bias resistors convey the bias current to the four switching cells that comprise the Josephson junction bridge. Each switching cell contains an 8×8 μm^2 shunted parallel junction and an 8×12 μm^2 shunted series junction. The 5 μm length of the shunt resistors, the minimum allowed in the process, favors compactness and low parasitics over lower fractional uncertainty in length. A low-capacitance 100 pH inductor is implemented as a pair of 9 μm wide Nb lines, each running over a 20 μm gap in the

ground plane. The hold loop is completed by a low-inductance loop running over the ground plane that forms the primary of the readout SQUID.

The readout SQUID, located to the right of the T/H, is a standard cell common to a number of designs on the mask set containing the T/H layout. Thus, a small amount of wiring is needed to couple it to the hold inductor of the T/H. The SQUID consists of two 5×5 μm^2 shunted junctions at the bottom of the SQUID cell and a rectangular loop inductance into which flux is coupled by two symmetric transformers with horseshoe-shaped inductors. The external SQUID feedback and bias fluxes are supplied via the transformer terminals on the right side of the SQUID. The SQUID bias current is applied via the bias resistor in the upper right corner of the SQUID cell and the output is taken via the output line at the top of the SQUID cell. The total cell area, to the edges of the coplanar waveguides, is 400×400 μm^2.

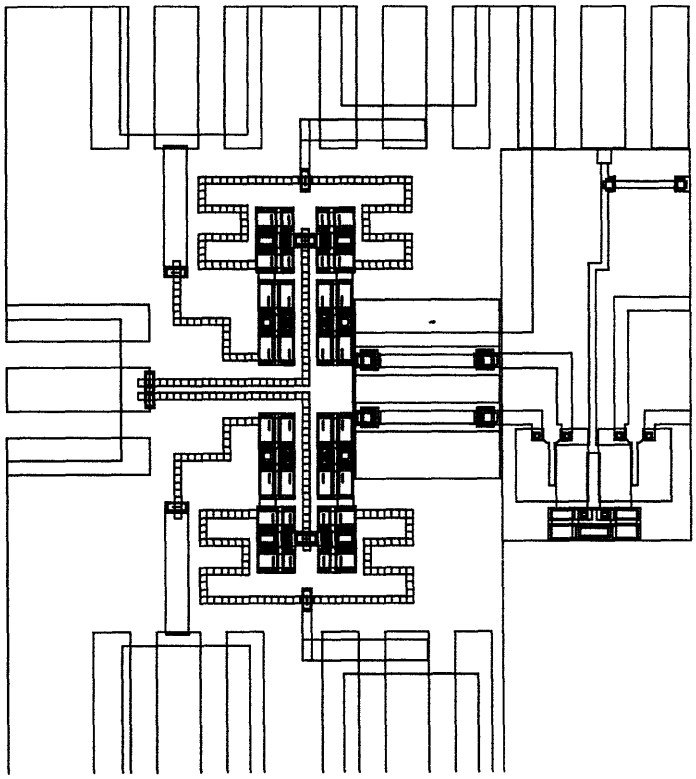

Figure 3.3 - Layout of a T/H circuit.

Fig. 3.4 shows the completed T/H chip. Three DSNAP wafers, each containing one such T/H chip, were fabricated at Lincoln Laboratory. The measured critical currents were in the range J_c = 600 – 800 A/cm^2. The sheet resistance was close to the target value of 2.5 Ω/□, so the large input, clock, and bias resistors were within 5% of their nominal values. However, the small junction shunt resistors were 20 – 25% higher than expected due to contact resistance and lithographic error. Unfortunately, a gross mask defect rendered the LOW T/H cell useless on all three wafers. The experimental results presented in the following sections are taken from the HIGH T/H on the chip having the

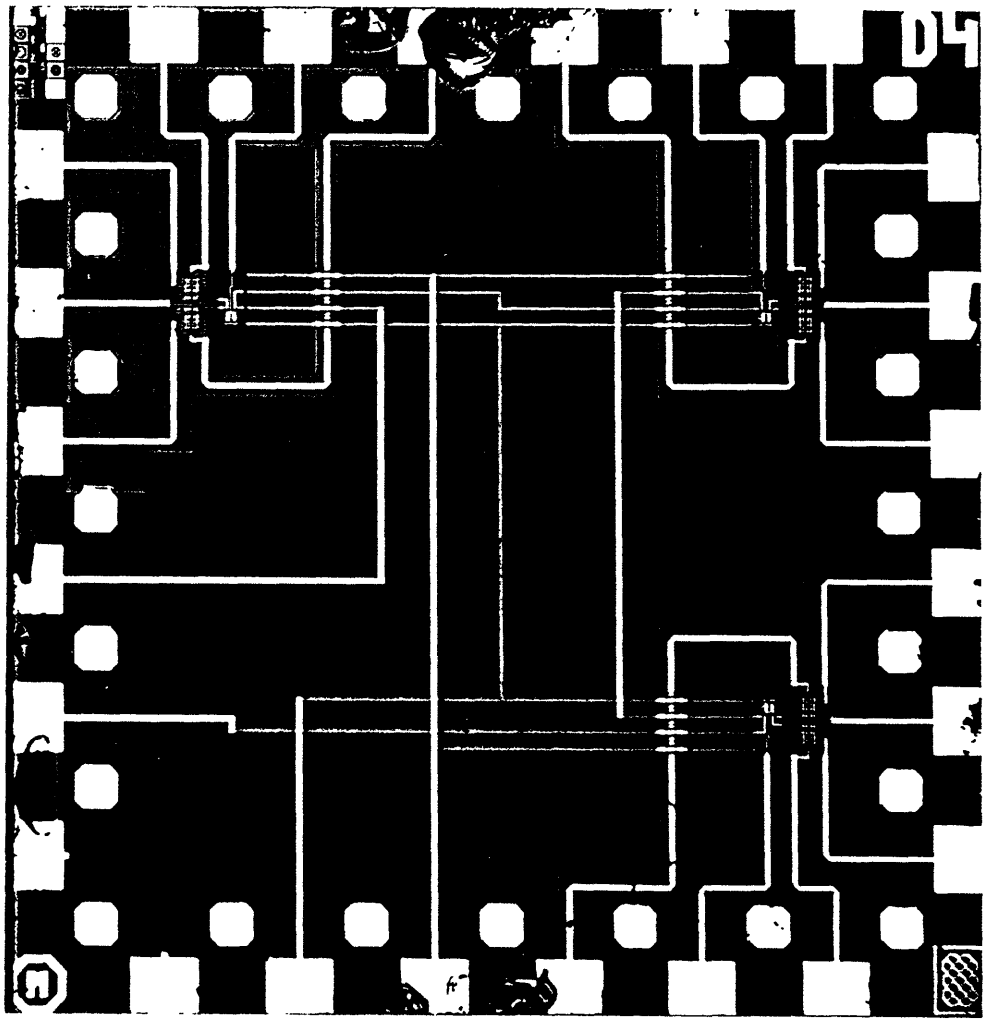

Figure 3.4 - Micrograph of the complete T/H chip.

highest critical current, J_c = 800 A/cm^2, because the NOM T/H on that chip was not functional. The qualitative behavior of the T/H's on the lower J_c chips was similar, but the reduced critical current resulted in a smaller input signal range.

3.3 - SQUID Readout Electronics

The flux-locked loop used to measure the quasi-static output current of the T/H is similar to that described in [33]. Fig. 3.5 is a block diagram of the flux-locked loop. As demonstrated earlier, the SQUID, when biased at a null, is effectively a multiplier whose fundamental output voltage is proportional to the sum of its input currents, ($I_{\Phi fb}$ + I_{out}). Although the SQUID effectively multiplies the ac flux bias, $I_{\Phi ac}$, by the sum of the input currents, in practice $I_{\Phi ac}$ is simply added to the feedback current. Fig. 3.5 uses a solid line to indicate the physical connection of $I_{\Phi ac}$ to the SQUID and a dashed line to indicate the operational connection.

The lock-in amplifier acts as a mixer whose output at baseband measures the net

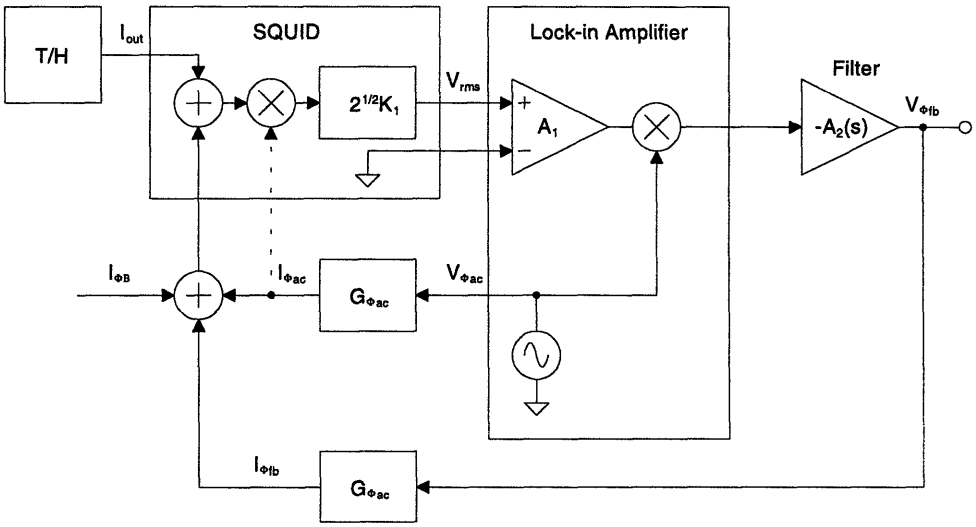

Figure 3.5 - Block diagram of the flux-locked loop circuit used to measure the output current of the T/H. Physically, the ac flux bias, $I_{\Phi ac}$, is an additive input to the SQUID, as shown by the solid connection. However, in this synchronous detection scheme, its net effect is multiplicative, as indicated by the dashed connection.

flux (or current) deviation from the null. The simplified model of the lock-in shown in Fig. 3.5 does not include the band-pass filter preceding the multiplier that attenuates harmonics of the ac drive at the frequency $f_{\Phi ac}$. Also omitted is the lock-in's integrated digital loop filter that follows the multiplier. In the present implementation, this filter is bypassed in favor of a separate analog filter and amplifier because the latency of the digital filter gives rise to poor loop stability. The loop filter attenuates modulation harmonics and reduces the noise bandwidth of the measured output signal, $V_{\Phi fb}$. The filter also determines the dynamics of the flux-locked loop.

The flux-locked loop is completed by feeding back, with the appropriate sign, the output of the lock-in amplifier via a resistor to generate $I_{\Phi fb}$. The negative feedback and large loop gain drive the error (i.e., the magnitude of the SQUID output at the drive frequency) towards zero, forcing the SQUID to operate near its null. If $M_{11} = M_{12}$, the feedback current will be the negative of the output current of the T/H, to within the error of the flux-locked loop. Thus, the output current of the T/H can be measured by reading the feedback voltage, $V_{\Phi fb}$.

The closed-loop transfer function of the flux-locked loop is given by:

$$\frac{V_{\Phi fb}}{I_{out}} = \frac{-G_{\Phi fb}{}^{-1}}{1 - LT^{-1}(s)} \tag{3.2}$$

where the loop transmission, $LT(s)$, is given by:

$$LT(s) = -G_{\Phi fb} A_1 A_2(s)(\sqrt{2} I_{\Phi ac} K_1) \tag{3.3}$$

Since both ends of the feedback line on the T/H chip are available as external connections, the sign of the loop transmission is easily selected by appropriately choosing the direction of positive current flow. If $LT(s) >> 1$, the fractional loop error, defined as the fractional deviation from a transresistance of $-G_{\Phi fb}$, is approximately given by:

$$G_{\Phi fb}\frac{V_{\Phi fb}}{I_{out}}+1\approx LT^{-1}(s) \tag{3.4}$$

The loop filter is a first-order low-pass filter with gain, whose transfer function is given by:

$$A_2(s)=\frac{A_2}{\tau_{loop}s+1} \tag{3.5}$$

where τ_{loop} is the loop filter time constant.

The SQUID is excited with an ac bias at $f_{\Phi ac}$ = 10 kHz with an amplitude of $I_{\Phi ac}$ = 1.00 mA. It is biased at I_{bias} = 0.36 mA; at this bias point the measured SQUID parabolicity is $K_1 \approx 0.07$ mV/mA^2. The feedback resistor is $G_{\Phi fb}^{-1}$ = 1.00 KΩ, so that I_{out} = 1 mA results in $V_{\Phi fb}$ = –1 V. The sensitivity of the lock-in is set to produce a 10 V output for a 100 μV rms input, giving a gain of $A_1 = 10^5$ V/V. The dc gain of the loop filter is set to 200 V/V. Therefore, the dc loop transmission is $LT(0)$ = –2000 and the magnitude of the fractional loop error is 0.05%. The loop gain is sufficiently large that the mismatch between the SQUID's mutual inductances, M_{11} and M_{12}, would likely dominate the overall gain error of the flux-locked loop.

Since the purpose of the flux locked loop is to obtain dc measurements of the output current of the T/H, the loop time constant may be chosen to give a loop crossover frequency well below frequencies where the dynamics of the lock-in or other parasitic poles or delays become important. The loop time constant was chosen to give a crossover frequency about 500 Hz. As a result, the loop response would appear to be nearly instantaneous for manual quasi-static measurements. In practice, the flux-locked loop was capable of about 1 μA resolution and repeatability over a signal range of ±1 mA. Thus the instrumentation resolution was an order of magnitude better than the resolution of the device under test, the T/H.

3.4 - Low-Frequency Characterization:

This section presents the low-speed test results of the T/H. For these tests, the input to the T/H was a balanced dc current. A switched dc power supply and a fast pulse generator were used as clock sources. As noted earlier, these measurements were taken from a HIGH T/H on a chip having a critical current of about J_c = 800 A/cm^2 (chip CT3B8-D4). The average critical current of the parallel junctions, determined by examining the *I-V* curve resulting from driving the T/H's two external bias pins in parallel and observing the voltage developed at the clock pin, was close to 500 μA. This value is about 22% below the 640 μA target.

The T/H's bias currents were chosen to achieve the minimum required parallel junction overdrive, resulting in a wide input signal range without compromising the isolation of the bridge. Also, since the *I-V* curves of the parallel junctions contained some fine structure, the bias current was adjusted so that these junctions would operate near a point where the *I-V* curves were smooth. For the T/H described below, a bias current of about 630 μA per parallel junction (1.25 mA per bias line), corresponding to 25% parallel junction overdrive, satisfied the preceding criteria. Some T/H's on other chips operated best at 35% or more overdrive.

Fig. 3.6 shows the dc tracking performance of the T/H obtained by stepping the input current in 10 μA increments and measuring the output of the flux-locked loop. The offset of the T/H and SQUID were nulled prior to performing this test. The slope of the line that is least-squares fitted to the measured data is 0.99 μA/μA. The deviation from unity gain may be due to either the T/H or the readout SQUID. The output of the T/H's SQUID readout does not strictly follow the input, but contains a small, periodic error component with an rms value of about 5.5 μA and a period of about 190 μA in this case. The magnitude and periodicity of this error vary depending on the conditions under which the chip is cooled. Errors as low as about 1 μA rms, close to the measurement accuracy

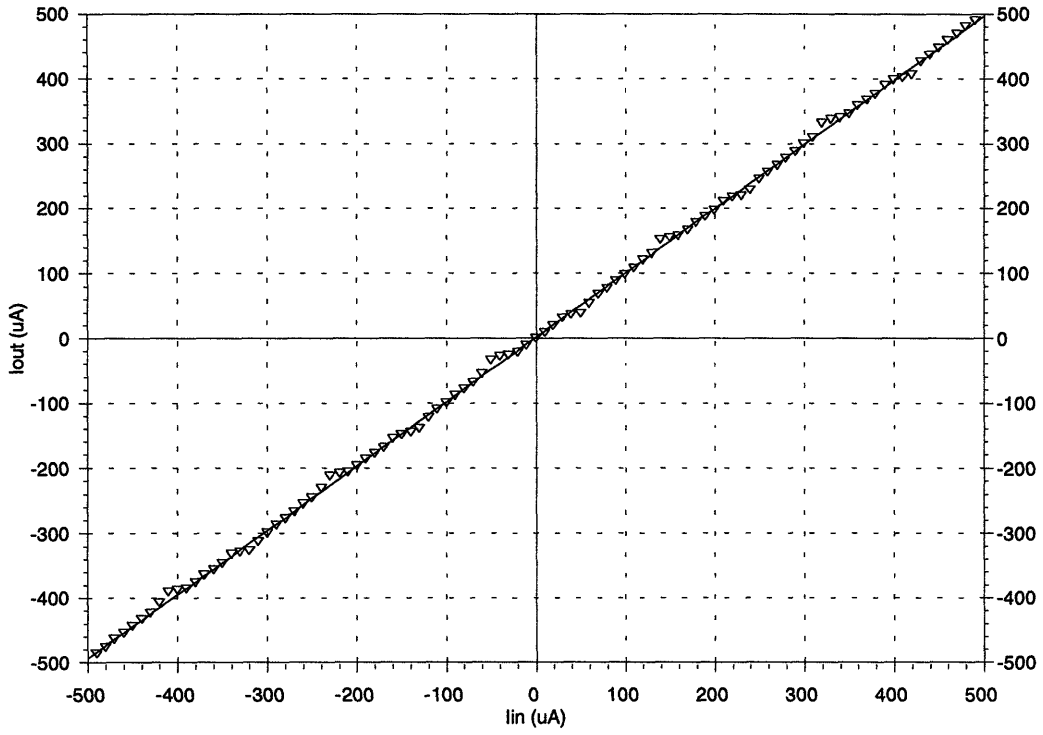

Figure 3.6 - Measured dc tracking performance of the T/H. The gain of the best-fit straight line is 0.99 μA/ μA. The data were taken from the HIGH T/H on chip CT3B-D4.

of the flux locked loop, have been observed, showing that the error is not fundamental to the T/H itself. Since the error fluctuates between cool-downs, it may be due to the influence of flux trapped during the cooling process. However, it is difficult to consistently reduce the error to the 1 μA level.

The maximum dc input current that the T/H could track is less than 700 μA, more than adequate to support any achievable sampled current. The ratio of serial junction to parallel junction critical currents appears to be lower than expected, as the maximum input current is less than the value of about 750 μA expected from the measured parallel junction critical current and the drawn ratio of junction areas. This observation is

qualitatively consistent with the fact that the necessary parallel junction overdrive was lower than expected.

Fig. 3.7 shows the response of the T/H in hold mode. The data points are obtained by connecting the clock to –2.5 mA dc current source with no input applied and observing the output of the flux locked loop while sweeping the input current. The dc offset is 37 μA and the hold-mode gain is +8.5 μA/mA. The hold-mode gain is independent of bias conditions and is close to 1% for a number of T/H's. The nonzero hold-mode gain is not intrinsic to the T/H, but is apparently due to direct magnetic coupling from the input to the readout SQUID. This phenomenon is not well understood, as the superconducting ground plane should prevent flux penetration in the readout SQUID. However, coupling on the order of 1% between numerous dc signal lines and

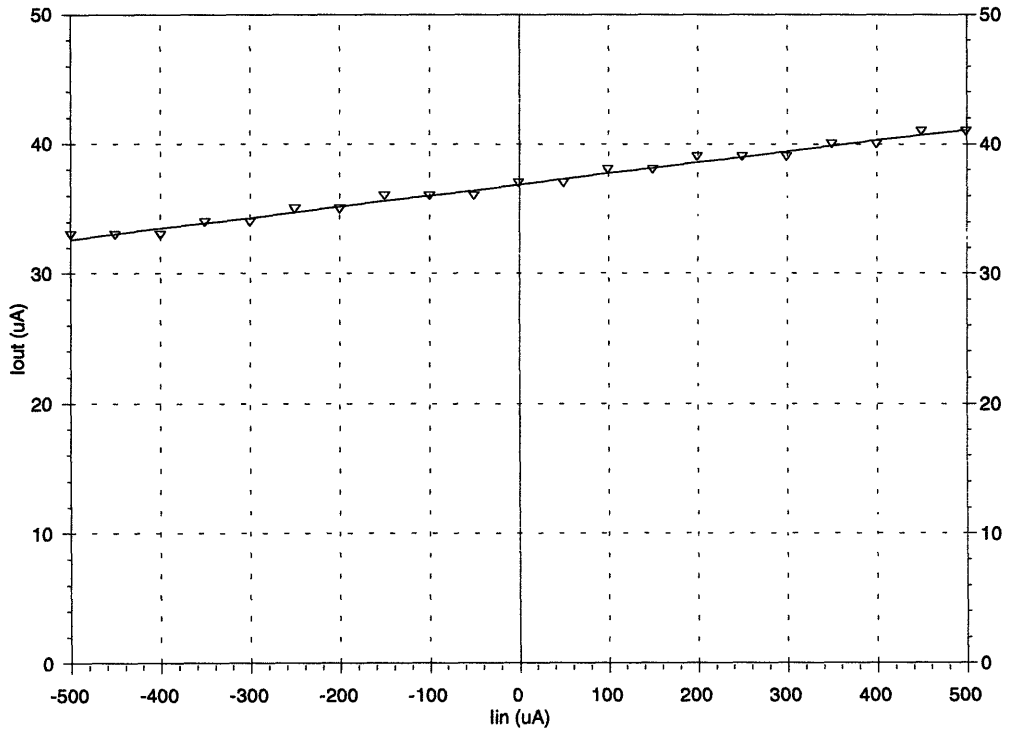

Figure 3.7 - Measured hold-mode response of the T/H.

the SQUID has been observed in other circuits fabricated in the DSNAP process using the same SQUID. The source of the observed feedthrough in hold mode is not the same as the small negative hold-mode gain seen in the simulations of the T/H. Regardless of the source, the feedthrough is not unacceptable, as it contributes less than 3 μA to the output current over the entire ± 320 μA input range of the T/H.

Similarly, the nonzero dc offset is due, at least in part, to direct coupling from the clock to the readout SQUID. Some offset attributable to component mismatches in the T/H itself is expected. However, the observed offset does not always correspond to an integer number of flux quanta in the hold loop, as would be true of any sampled dc offset resulting only from the T/H. Rather, the offset also depends on the sign and amplitude of the clock current; the bias currents have a similar effect. In summary, the measured hold-mode performance of the T/H is limited by feedthrough extrinsic to the T/H itself. Since the clock feedthrough is only a dc offset, it does not affect the linearity of the T/H. The 37 μA offset due to clock feedthrough is subtracted from the measured data in the following figures.

Fig. 3.8 shows the dc sampling response curve of the T/H as well as a straight line fitted to the data to minimize the rms error over the ±320 μA input range. A manual switch and a –2.5 mA dc current source served as the clock for this test. The experimental sampling response in Fig. 3.8 in should be compared with the simulated response in Fig. 2.10. The measured maximum and minimum sampled values are +425 μA and –404 μA, respectively. Thus, the maximum sampled output current is about 81% of $I_{c,P}$. For comparison, Fig. 2.13 shows that the maximum sampled output current predicted by simulation is 90% of $I_{c,P}$. For input currents exceeding about 400 μA in magnitude, the T/H is susceptible to occasional errors that give sampled output currents differing from those indicated in Fig. 3.8.

Since the reduced accuracy at the extremes of its usable input range was anticipated, the T/H is specified for operation over the restricted input range of ±320 μA. The straight line fit in Fig. 3.8 is chosen to minimize the rms error over this range. The offset is 10.6 μA and the gain is 0.947 μA/μA, in good agreement with the gains required to fit a straight line to the simulated quasi-static sampling response of the T/H. Over the input range of ±320 μA, the output of the T/H has 33 levels which are spread nearly uniformly between –300 μA and +308 μA. Thus, the T/H achieves 5-bit nominal resolution, as desired. The mean LSB size is 19.0 μA, from which an effective hold inductance of L_2 = 109 pH can be inferred. This value of hold inductance is consistent with the 100 pH hold inductor structure in series with the parasitic wiring inductance of

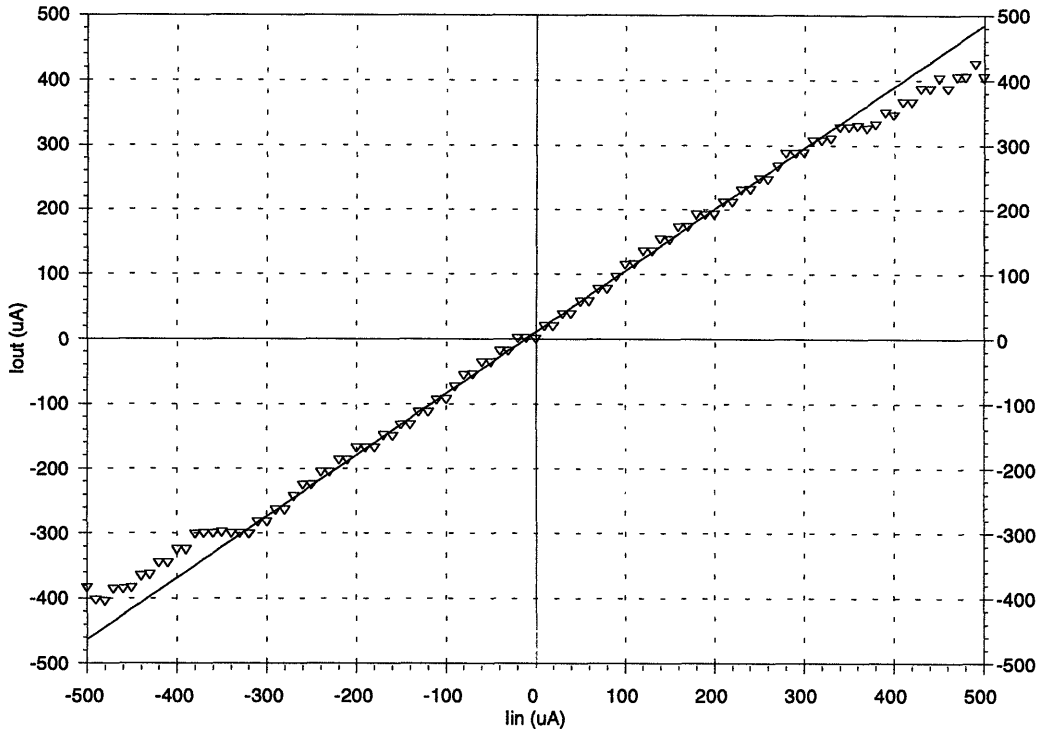

Figure 3.8 - Measured dc sampling response curve of the T/H with a slow step clock. The clock feedthrough is subtracted from the data. The gain is of the straight line, fitted to minimize the rms error over the input range of ±320 μA, is 0.947 μA/μA. The data are taken from the HIGH T/H on chip CT3B-D4.

the SQUID readout. The rms sampling error over the ±320 μA input range is 6.86 μA, yielding 4.7 effective bits of dc resolution at a 19.0 μA LSB size, in good agreement with the simulated values shown in Fig. 2.26, which are close to 4.5 effective bits for $R_{sh,P}$ < 0.75 Ω.

Fig. 3.9 shows another dc sampling response curve of the T/H with a straight line fitted to the data to minimize the rms error over the ±320 μA input range. In this case, the clock source was a fast pulse generator that produced a single 10 ns wide, 2.5 mA sampling pulse offset by –2.5 mA. The 90% – 10% fall time of the sampling edge was 120 ps. With this clock scheme, the T/H is kept in hold mode except during the short interval during which the clock pulse is high. Again, the T/H could generate a sampled

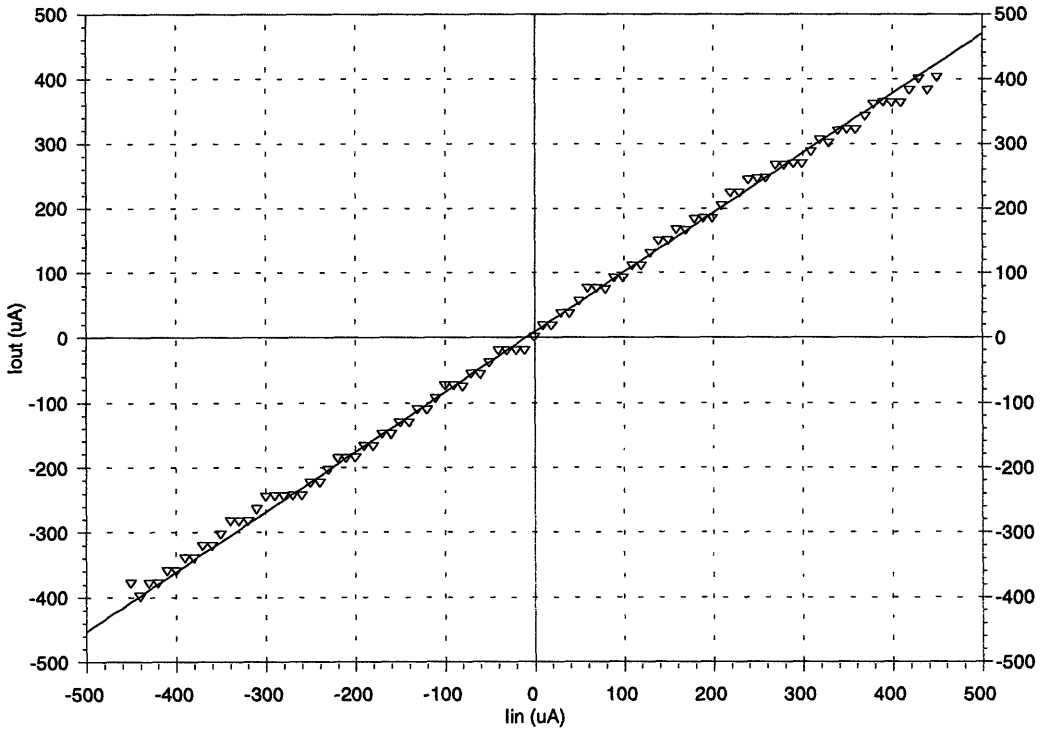

Figure 3.9 - Measured dc sampling response curve of the T/H with a 10 ns sampling pulse. The clock feedthrough is subtracted from the data. The gain is of the straight line, fitted to minimize the rms error over the input range of ±320 μA, is 0.922 μA/μA. The data are taken from the HIGH T/H on chip CT3B-D4.

current no larger than about 400 μA in amplitude. The straight line fit in Fig. 3.9 is again chosen to minimize the rms error over the input range of ±320 μA. The offset of this line is 8.2 μA and its gain is 0.922 μA/μA, in good agreement with the results for a much slower clock. Due to the slightly lower gain in this case, the T/H has only 32 levels spread nearly uniformly between –283 μA and +306 μA over an input range of ±320 μA. The mean LSB size is 19.1 μA, in very good agreement with the result using a slow clock. The sampling error over the ±320 μA input range is 8.33 μA rms, corresponding to 4.5 effective bits of dc resolution at a 19.1 μA LSB size, again in good agreement with the effective dc resolution predicted by simulation.

In summary, the measured performance of the T/H with dc inputs agrees well both qualitatively and quantitatively with that predicted by simulation. The principal observed anomalies, clock and input signal feedthrough, are extrinsic to the T/H. In any case, the magnitude and nature of these anomalous effects are such that they do not affect the key dc specifications of the T/H, its input signal range and its accuracy.

3.5 - High-Frequency Characterization:

This section presents the high-speed test results of the T/H. For these tests, the input to the T/H was a balanced dc current or a balanced sinusoidal current. A fast pulse generator, synchronized to the input, acted as the clock source for all of these tests.

Since the flux locked loop lacked the capability to measure the output of the T/H at speed, the acquisition time of the T/H was determined by measuring the sampled current generated by the T/H for a full-scale change in held current for varying sample pulse widths. Fig. 3.10 shows the T/H's response as the circuit, initially holding a sample of zero, is briefly subjected to a dc input of 320 μA. The abscissa is the measured full-width at half-maximum (FWHM) of the sampling pulse. The rise time of the sampling pulse is 60 ps and the fall time is 120 ps. When the sampling pulse width is less than

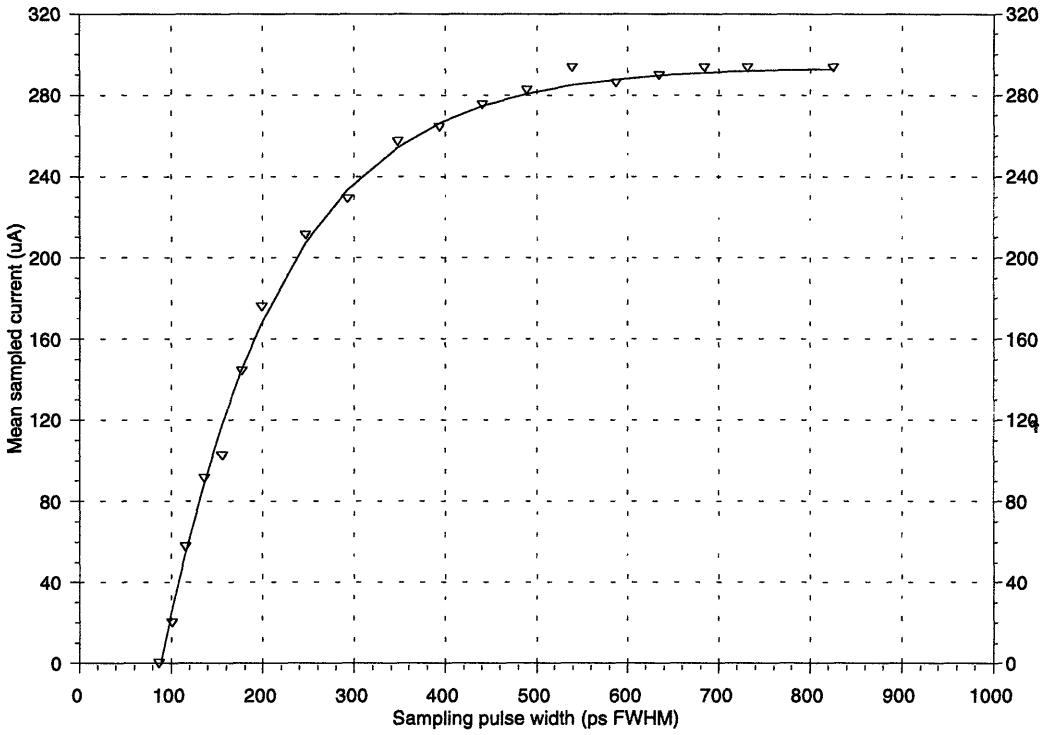

Figure 3.10 - Measured T/H acquisition transient with a 320 μA change in held current. The clock feedthrough is subtracted from the data which are taken from the HIGH T/H on chip CT3B-D4.

about 100 ps, the pulse does not attain its full amplitude, so the T/H cannot begin to acquire the new input before it is commanded to return to hold mode. For increasing sampling pulse widths, the output of the T/H captures a progressively more accurate sample of the input current.

The data points, which represent the averages of five samples taken at each value of pulse width, lie close to the exponential curve fitted to the data. The time constant of the exponential curve is 130 ps, corresponding to a half-power acquisition bandwidth of 1.2 GHz, and its final value is 300 μA, in agreement with the measured dc gain of the T/H. The 10% – 90% acquisition rise time is 290 ps. The linear acquisition time to 5-bit accuracy is 450 ps; since the rise and fall times of the sampling pulse are nonzero, the

total acquisition time to 5-bit accuracy is 550 ps. The measured linear acquisition time is 275 ps less than the value obtained from the simulation of the T/H using the target component values. The measurement of the linear acquisition time is not very accurate because the rise and fall times of the sampling pulse are a large fraction of the pulse width. Nevertheless, the real T/H should be faster than the nominal design because the shunt resistance across the parallel junctions is higher and the bias current overdrive is lower. This improvement in acquisition speed is mitigated to some extent by the longer rise and fall times of the sampling clock. If the T/H were driven with a clock having similar rise and fall times, but with a 50% duty cycle, its sampling rate would be over 900 MS/s.

Fig. 3.11 shows a block diagram of the high-speed test setup. The master clock is the frequency synthesizer that produces a variable-frequency sinusoidal output phase-locked to a 10 MHz reference. The sinusoidal output is passed through a continuously variable delay line that allows the phase of the sine to be adjusted with respect to the reference and subsequently through a 2 GHz bandwidth hybrid that develops the complementary sinusoidal outputs that drive the inputs of the T/H. The entire sinusoidal signal path is calibrated at each frequency to correct for the amplitude variation of the

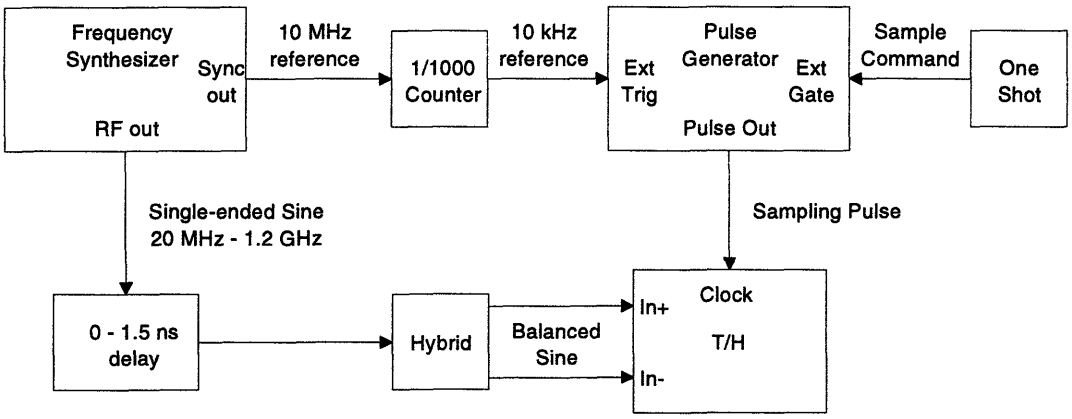

Figure 3.11 - Block diagram of the instrument configuration used to test the T/H with high-speed sine inputs.

oscillator's output and the frequency response of the hybrid. The frequency of the reference is divided by 1000 using a digital counter in order to bring the reference frequency within the lock range of the pulse generator which is triggered on the 10 kHz reference. The output of the pulse generator is inhibited except when commanded by a one-shot pulse generator to produce a single pulse with a fixed phase relationship to the 10 kHz reference, and hence with respect to the sinusoidal input. The pulse generator also allows its output to be delayed from 0 – 63 ns in nominal 1 ns steps. This feature is utilized with low-frequency inputs to the T/H to capture up to 64 samples of the input at different effective sampling times. The actual delays, which differ by as much as 800 ps from nominal, are measured to about 10 ps accuracy and used to calculate the relative position of the sampling pulse with respect to the sinusoidal input. For input frequencies above 800 MHz, the 1.5 ns delay line in the sine wave signal path is used to sweep the pulse across the sine wave in 50 ps increments of equivalent time.

Fig. 3.12 shows the measured sampling performance of the T/H with a 50 MHz, 320 μA peak sinusoidal input. The data points, shown as triangles, are single output samples, rather than the average of many samples. Repeated samples taken at one value of delay generally agree to about 1 LSB. The curve fitted to the data has an amplitude of 283 μA and an offset of 6.1 μA. The output samples lie close to the fitted curve, with an rms error of 12.6 μA. The largest deviations occur near the peaks and troughs of the sine wave. This behavior is expected since the accuracy of the T/H degrades at the extremes of its input range.

Fig. 3.13 shows the measured sampling performance of the T/H with a faster 800 MHz, 320 μA sinusoidal input. The curve fitted to the data has an amplitude of 211 μA and an offset of 2.0 μA. Again, the output samples lie close to the fitted curve, but the error is only 9.5 μA rms. The T/H can more accurately sample the input at this higher

frequency since the amplitude of the its output is lower, in agreement with the simulations of the circuit.

Measurements of the type used to generate Fig. 3.12 and Fig. 3.13 were repeated for a range of frequencies from 20 MHz to 1.2 GHz. Fig. 3.14 shows the amplitude of the best-fit sine vs. input frequency for these measurements as well as a fitted first-order frequency response. The fitted curve has a dc amplitude of 280 μA, corresponding to a gain of 0.88 μA/μA, and a half-power bandwidth of 900 MHz. Clearly, the frequency response of the T/H closely follows the expected first-order dependence. The small difference between the dc gain inferred from these measurements and the direct measurement of the dc transfer function of the T/H may be due to an error in the

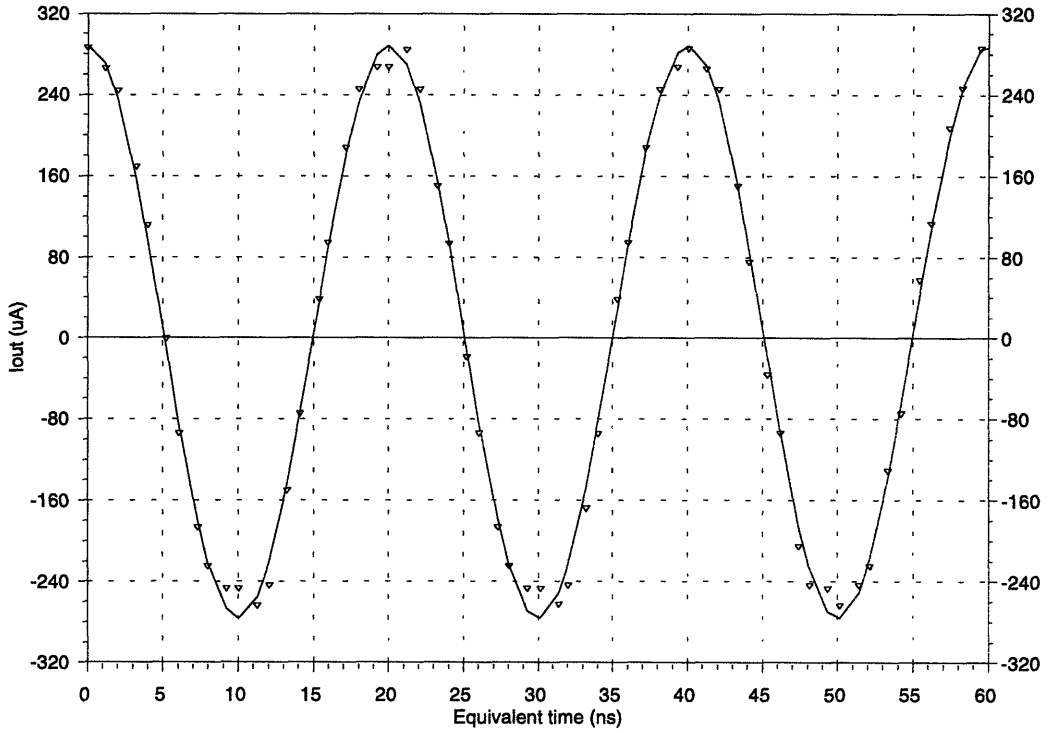

Figure 3.12 - Measured sampling performance of the T/H with a 50 MHz, 640 μA p-p, sinusoidal input. The output samples are shown as triangles; the solid curve is an offset sine, fitted to the sampled data so as to minimize the rms error. The sampling pulse width is 10 ns. The clock feedthrough is subtracted from the data which are taken from the HIGH T/H on chip CT3B-D4.

measurement of the ac inputs to the T/H or slight variations in the output impedance and phase accuracy of the hybrid.

The measured half-power sampling bandwidth of the T/H is 15% higher than that obtained from simulations of the T/H using the target component values. This result is not surprising, since the junction shunt resistors were some 20% higher than the target value. The tracking bandwidth of the T/H cannot be measured directly, but it should be close to the 900 MHz sampling bandwidth.

Fig. 3.15 shows the signal-to-noise ratio and effective bit-resolution of the T/H vs. frequency. The *SNR* and *ENOB* are extracted from the measured sampling response of the T/H with sinusoidal inputs. This figure should be compared with the simulated data

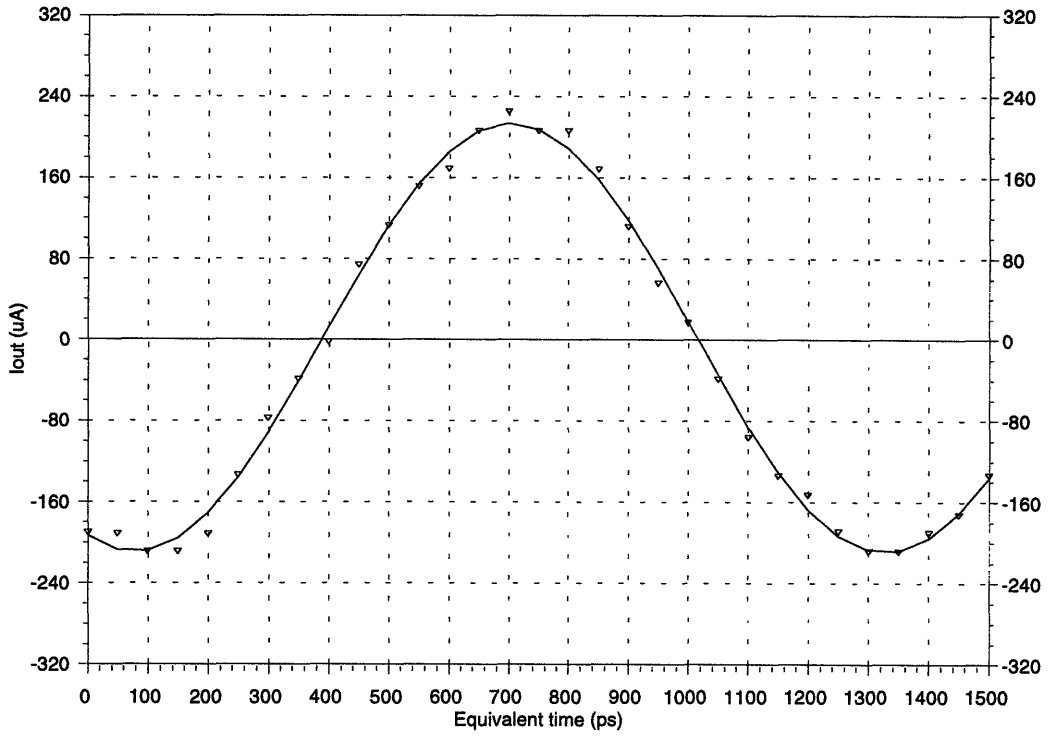

Figure 3.13 - Measured sampling performance of the T/H with an 800 MHz, 640 μA p-p, sinusoidal input. The output samples are shown as triangles; the solid curve is an offset sine, fitted to the sampled data so as to minimize the rms error. The sampling pulse width is 10 ns. The clock feedthrough is subtracted from the data which are taken from the HIGH T/H on chip CT3B-D4.

shown in Fig. 2.25.

Over the frequency range where both measured and simulated data are available, the measured *SNR* is about 3 dB worse than the *SNR* determined from simulation of the T/H using the target component values. Measurement noise, including additive noise in the input signal path as well as jitter and errors in measuring the delay paths, may contribute to the apparent disparity. However the reduced accuracy is also due to the low critical current of the fabricated T/H. The reduced J_c results in a reduced sampling accuracy over a given input signal range and leads to a lower best-fit gain. The reduced sampling accuracy at the limits of the input signal range increases the sampling noise; this effect is most noticeable near the peaks and troughs of a full-scale input sine, as seen in

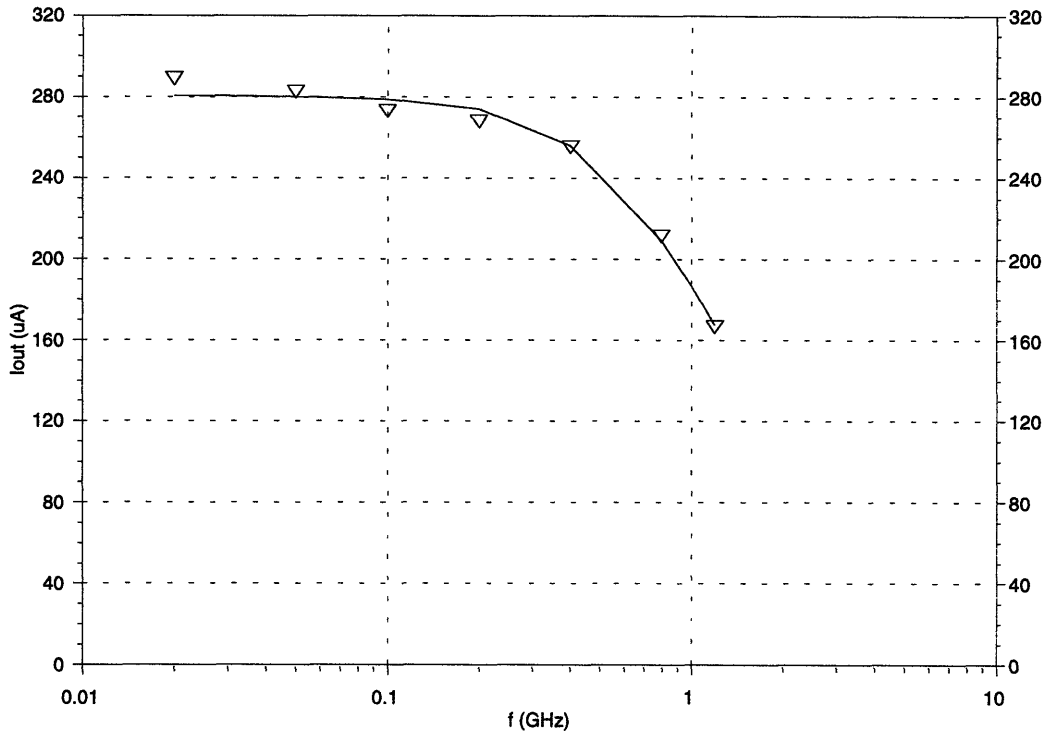

Figure 3.14 - Magnitude of the best-fit T/H output vs. frequency with a full-scale sine wave input. A first-order frequency response curve is fitted to the data. The sampling pulse width is 10 ns and the data are taken from sine-fit measurements performed on the HIGH T/H on chip CT3B-D4.

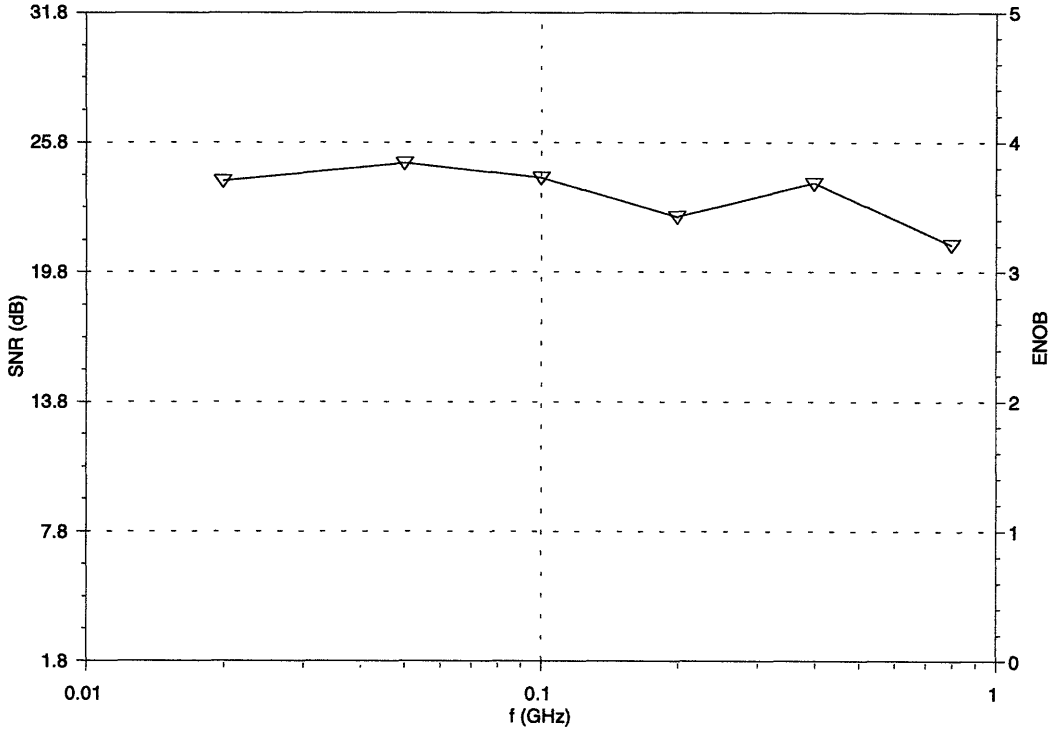

Figure 3.15 - Measured *SNR* and *ENOB* of the T/H vs. frequency. The sampling pulse width is 10 ns and the data are taken from sine-fit measurements performed on the HIGH T/H on chip CT3B-D4.

Fig. 3.12. The lower gain reduces the output signal power, as evidenced in Fig. 3.14.

Table 3.1 compares the measured performance of the T/H to that predicted from the simulation of the T/H using the target component values. The sampling rate is inferred from the acquisition time, assuming a 50% duty cycle sampling clock. The measured bit-resolution at 1 GHz is taken to be the mean of the values at 0.8 GHz and 1.2 GHz. The measured effective dc resolution cited in Table 3.1 is that obtained using a pulsed clock. Overall, the real T/H was 15% – 25% faster than simulation because of the larger shunt resistance. However, the real T/H had a smaller input signal range and was also less accurate because critical current was below target.

Table 3.1 - Measured and Simulated Performance of the Josephson Junction Bridge T/H

Parameter	Measured Value	Simulated Value
Maximum full-scale input current	I_{FS} = 400 μA	I_{FS} = 585 μA
Operating input current range	–320 μA - +320 μA	–320 μA - +320 μA
Current step size (LSB weight)	I_{step} = 19.0 μA	I_{step} = 20.0 μA
Nominal resolution	N = 5 bits	N = 5 bits
Effective dc resolution	*ENOB* (dc) = 4.5 bits	*ENOB* (dc) = 4.6 bits
Tracking half-power bandwidth	f_{track} = 900 MHz	f_{track} = 750 MHz
Acquisition time (5-bits)	550 ps	725 ps
Maximum sampling rate (5-bits)	900 MS/s	690 MS/s
Sampling half-power bandwidth	f_{samp} = 900 MHz	f_{samp} = 785 MHz
Effective resolution (1 GHz)	*ENOB* = 3.5 bits	*ENOB* = 4.1 bits

4 - Conclusion

The Josephson junction bridge is a novel topology for implementing the current switch of a true track and hold circuit in a superconductive device technology. An important technique exploited by the bridge is its use of a common-mode clock current to control a Josephson junction circuit that modulates a differential signal current. Since the T/H captures current samples in a superconducting loop, its hold time is infinite. Moreover, the fast switching speed of the Josephson junctions that comprise the bridge allows the T/H to rapidly switch between track mode and hold mode. However, the acquisition time, as well as the tracking and sampling bandwidths of the T/H are limited by the classical *L/R* time constant of the hold inductor and the resistance of the parallel Josephson junctions of the bridge in track mode. An analysis of the acquisition dynamics that take place as the T/H switches from track mode to hold mode shows that the shunt resistance of the parallel junctions must be made small for these junctions to have a large return current so that the T/H will have a large input signal range. The resolution of the T/H is limited by flux quantization in the superconducting hold loop. Therefore, there is a tradeoff between resolution and speed in the design of the T/H.

In order to facilitate testing of the T/H, it was designed for moderate speed and dynamic range. Since the circuit's principle of operation was untested, the design parameters were chosen conservatively to maximize the tolerances to process spreads. In particular, in anticipation of high resistance spreads in the sub-square regime, the parallel junctions were excessively shunted by roughly twice the conductance needed to achieve the specified input signal range. In the same process, a more aggressive design should have roughly twice the bandwidth of the present design with comparable dynamic range.

The T/H was fabricated at MIT Lincoln Laboratory in the Dual-dielectric Selective Niobium Anodization Process (DSNAP) using conservative 5 μm minimum geometry and 1000 A/cm^2 critical current density. Since, in this regime of critical current and barrier thickness, the critical current depends exponentially on the barrier thickness while the capacitance depends only inversely linearly, the capacitance of a Josephson junction having a given critical current decreases approximately inversely linearly with increasing critical current density. The shunt resistance needed to achieve a given return current to critical current ratio increases approximately as the square root of the critical current density. Therefore, at a given resolution (roughly determined by the product of the hold inductance and the critical current of the parallel junctions), the shunt resistance of the parallel junctions (and hence the bandwidth of the T/H) can be doubled by increasing the critical current density of the Josephson junctions in which the T/H is fabricated by about a factor of four.

Another approach to improving the speed of the T/H is to replace each of the shunted parallel junctions with a stack of N shunted junctions as reported in [29]. The total resistance of the stack is increased by a factor of N, but the return current of each junction is not reduced. Unfortunately, in preliminary simulations of the T/H using stacked junctions, the increase in bandwidth has been accompanied by a degradation of resolution.

Experiments confirmed the theory of operation of T/H within the limitations of the test equipment, readout circuit, and process variations. The measured performance of the T/H agreed well, both qualitatively and quantitatively, with that predicted by calculations and simulations. The flux-locked loop SQUID readout provided high-precision measurements of the T/H's output current, but severely limited the speed at which the output current could be measured. Nevertheless, experiments unambiguously verified the characteristics of the T/H for single-shot sampling of high-speed input

signals. Using an on-chip superconducting sampler in a subsequent design would allow the high-speed transient dynamics of the T/H to be studied for repetitive sampling of constant or periodic inputs.

References

[1] T. Van Duzer and C.W. Turner, *Principles of Superconductive Devices and Circuits*, New York: Elsevier, 1981.

[2] T.P. Orlando and K.A. Delin, *Foundations of Applied Superconductivity*, New York: Addison-Wesley, 1991.

[3] K.K. Likharev, *Dynamics of Josephson Junctions and Circuits*, New York: Gordon and Breach, 1986.

[4] K. Poulton, J.J. Corcoran, T. Hornak, "A 1 GHz 6-bit ADC System," *IEEE Journal of Solid-State Circuits*, Vol. SC-22, No. 6, December 1987.

[5] K. Tam, "A Monolithic GaAs Sample and Hold and 6-bit A/D Converter," Master of Science Thesis, MIT, May 1992.

[6] K.K. Likharev and V.K. Semenov, "RSFQ Logic/Memory Family: A New Josephson-Junction Technology for Sub-Terahertz-Clock-Frequency Digital Systems," *IEEE Transactions on Applied Superconductivity*, Vol. 1, No. 1, March 1991.

[7] S.H. Dhong, R.E. Jewett, and T. Van Duzer, "Josephson Analog-to-Digital Converter Using Self-Gating-AND Circuits as Comparators," *IEEE Transactions on Magnetics*, Vol. MAG-19, pp. 1282-1285, May 1983.

[8] C.A. Hamilton, F.L Lloyd, and R.L. Kautz, "Superconducting A/D Converter Using Latching Comparators," *IEEE Transactions on Magnetics*, Vol. MAG-21, No. 2, March 1985.

[9] D.A. Petersen, H. Ko, and T. Van Duzer, "Dynamic Behavior of a Josephson Latching Comparator for use in a High-Speed Analog-to-Digital Converter," *IEEE Transactions on Magnetics*, Vol. MAG-23, No. 2, March 1987.

[10] E.S. Fang, D. Hebert, and T. Van Duzer, "A Multi-Gigahertz Josephson Flash A/D Converter with a Pipelined Encoder Using Large-Dynamic-Range Current-Latch Comparators," *IEEE Transactions on Magnetics*, Vol. MAG-27, pp. 2891-2894, March 1991.

[11] H. Luong, D. Hebert, T. Van Duzer, "Fully Parallel Superconducting Analog-to-Digital Converter," *IEEE Transactions on Applied Superconductivity*, Vol. 3, pp. 2633-2636, March 1993.

[12] E.S. Fang and T. Van Duzer, "Speed-Limiting Factors in Flash-Type A/D Converters," *IEEE Transactions on Magnetics*, Vol. MAG-25, pp. 822-825, March 1989.

[13] C.W. Mangelsdorf "A 400-MHz Input Flash Converter with Error Correction," *IEEE Journal of Solid State Circuits,* Vol. 25, No. 1, February 1990.

[14] H. Ko and T. Van Duzer, "A New High-Speed Periodic-Threshold Comparator for Use in a Josephson A/D Converter," *IEEE Journal of Solid State Circuits,* Vol. 23, pp. 1017-1021, August 1988.

[15] H. Ko, "A FLASH Josephson A/D Converter Constructed with One-Junction SQUIDs," *IEEE Transactions on Magnetics,* Vol. MAG-25, No. 2, March 1989.

[16] P. Bradley and Huan Dang, "Design and Testing of Quasi-One Junction SQUID-Based Comparators at Low and High Speed for Superconductive Flash A/D Converters," *IEEE Transactions on Applied Superconductivity*, Vol. 1, pp. 134-139, September 1991.

[17] N. Shimizu, Y. Harada, N. Miyamoto, E. Goto, "A New A/D Converter with Quantum Flux Parametron," *IEEE Transactions on Magnetics,* Vol. MAG-25, No. 2, March 1989.

[18] D.A. Petersen, H. Ko, R.E. Jewett, K. Nakajima, V. Nandakumar, J.W. Spargo, and T. Van Duzer, "A High-Speed Analog-to-Digital Converter Using Josephson Self-Gating-AND Comparators," *IEEE Transactions on Magnetics,* Vol. MAG-21, No. 2, March 1985.

[19] Y. Harada, J.B. Green, "High-Speed Experiments on a QFP-Based Comparator for ADC's with 18-GHz Sample Rate and 5-GHz Input Frequency," *IEEE Transactions on Applied Superconductivity*, Vol. 2, pp. 21-25, March 1992.

[20] P. Bradley, "A 6-bit Josephson FLASH A/D Converter with GHz Input Bandwidth," *IEEE Transactions on Applied Superconductivity*, Vol. 3, pp. 2550-2557, March 1993.

[21] F. Thomas, F. Debrie, F. Gloanec, M. Le Paih, P. Martin, T. Nguyen, S. Ruggeri, J.-M. Uro, "1-GHz GaAs ADC Building Blocks," *IEEE Journal of Solid State Circuits,* Vol. 24, No. 2, April 1989.

[22] C. Schiller and P. Byrne, "A 4-GHz 8-bit ADC System, " *IEEE Journal of Solid State Circuits,* Vol. 26, No. 12, December 1991.

[23] H.H. Zappe, "A Subnanosecond Josephson Tunneling Memory Cell with Nondestructive Readout," *IEEE Journal of Solid State Circuits,* Vol. 10, pp. 12-19, 1975.

[24] C.A. Hamilton, F.L Lloyd, and R.L. Peterson, and J.R. Andrews, "A Superconducting Sampler for Josephson Logic Circuits," *Applied Physics Letters*, Vol. 35, pp. 718-719, 1979.

[25] S.M. Faris, "Generation and measurement of ultrashort current pulses with Josephson devices," *Applied Physics Letters*, Vol. 36, pp. 1005-1007, June 1980.

[26] D.B. Tuckerman, "A Josephson ultrahigh-resolution sampling system," *Applied Physics Letters*, Vol. 36, pp. 1008-1010, June 1980.

[27] C.A. Hamilton, F.L Lloyd, and R.L. Kautz, "Analog Measurement Applications for High Speed Josephson Switches," *IEEE Transactions on Magnetics*, Vol. MAG-17, pp. 577-582, January 1981.

[28] A. Davidson, "Sample-and-Hold Gate Suitable for Small Josephson Junction Devices," *IBM Technical Disclosure Bulletin*, Vol. 22, No. 9, February 1980.

[29] J.P. Sage, J.B. Green, and A. Davidson, "Design, Fabrication, and Testing of a High-Speed Analog Sampler," *IEEE Transactions on Applied Superconductivity*, Vol. 3, pp. 2562-2565, March 1993.

[30] D. Go, C.A. Hamilton, F.L. Lloyd, M.S. DiIorio, R.S. Withers, "A Superconducting Analog Track-and-Hold Circuit," *IEEE Transactions on Electron Devices*, Vol. 35, pp. 498-501, April 1988.

[31] E.S. Fang and T. Van Duzer, "A Josephson Integrated Circuit Simulator (JSIM) for Superconductive Electronics Application," *Extended Abstracts of International Superconductivity Electronics Conference (ISEC)*, Tokyo, Japan, June 1989.

[32] E.S. Fang and T. Van Duzer, "JSIM Preliminary User's Guide," Software Release Documentation, EECS/ERL, University of California at Berkeley, 1989.

[33] J.C. Clarke, W.M. Goubau, and M.B. Ketchen, "Tunnel Junction dc SQUID: Fabrication, Operation, and Performance," *Journal of Low Temperature Physics*, Vol. 25, pp. 99-144, 1976.

[34] M. Bhushan and E.M. Macedo, "Nb/AlO_x/Nb Trilayer Process for the Fabrication of Submicron Josephson Junctions and Low-Noise dc SQUIDs," *Applied Physics Letters*, Vol. 58, pp. 1323-1325, March 1991.

[35] W.H. Chang, "Numerical Calculation of a Multi-Superconductor Transmission Line System," *IEEE Transactions on Magnetics*, Vol. MAG-17, pp. 746-766, January 1981.